

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Tuominen et al.
U.S. Patent No.: 7,609,527 Attorney Docket No. 50095-0191IP1
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Title: ELECTRONIC MODULE

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,609,527 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 7,609,527 (“the ’527 patent”)
APPLE-1002	File History of U.S. Patent No. 7,609,527
APPLE-1003	Expert Declaration of Dr. R. Jacob Baker, Ph.D., P.E.
APPLE-1004	U.S. Patent No. 5,616,520 to Nishiuma et al. (“Nishiuma”)
APPLE-1005	U.S. Publication No. 2002/0149117 to Shibata (“Shibata”)
APPLE-1006	RESERVED
APPLE-1007	U.S. Publication No. 2002/0159242 to Nakatani et al. (“Nakatani”)
APPLE-1008	Japanese Patent Publication No. 2001-085473 to Onda with Certified Translation (“Onda”)
APPLE-1009	Japanese Patent Publication No. 11-191574 to Matsuda with Certified Translation (“Matsuda”)
APPLE-1010	U.S. Patent No. 4,912,844 to Parker (“Parker”)
APPLE-1011	U.S. Publication No. 2003/0034557 to Gupta et al. (“Gupta”)
APPLE-1012	RESERVED
APPLE-1013	Japanese Patent Publication No. 2002-280713 to Yoneyama with Certified Translation (“Yoneyama”)
APPLE-1014	U.S. Patent No. 5,719,438 to Beilstein et al. (“Beilstein”)

APPLE-1015	U.S. Patent No. 5,866,942 to Suzuki et al. (“Suzuki”)
APPLE-1016	U.S. Publication No. 2004/0007774 to Crane et al. (“Crane”)
APPLE-1017	U.S. Patent No. 4,774,633 to Dehaine et al. (“Dehaine”)
APPLE-1018	U.S. Patent No. 7,297,572 to Salmon (“Salmon”)
APPLE-1019	U.S. Publication No. 2003/0047806 to Stelzl et al. (“Stelzl”)
APPLE-1020	U.S. Patent No. 4,068,022 to Glick (“Glick”)
APPLE-1021	J.A. Scarlett, <i>The Multilayer Printed Circuit Board Handbook</i> , Electrochemical Publications Limited, 8 Barns Street, Ayr Scotland © 1985
APPLE-1022	J.A. Scarlett, <i>An Introduction to Printed Circuit Board Technology</i> , Electrochemical Publication Limited, 8 Barns Street, Ayr Scotland © 1984
APPLE-1023-1024	RESERVED
APPLE-1025	U.S. Publication No. 2003/0090883 to Asahi (“Asahi”)
APPLE-1026-1030	RESERVED
APPLE-1031	Rudolf F. Graf, <i>Modern Dictionary of Electronics</i> , Newnes, 7 th ed. © 1999
APPLE-1032	Alan Freedman, <i>Computer Desktop Encyclopedia</i> , Osborne/McGraw-Hill, 9 th ed. © 2001
APPLE-1033	Frank Hargrave, <i>Hargrave’s Communications Dictionary</i> , IEEE Press © 2001
APPLE-1034	RESERVED

APPLE-1035	William D. Callister, Jr., Materials Science and Engineering: An Introduction, 5 th Ed., John Wiley & Sons, Inc. © 2000
APPLE-1036	Simon Thomas, <i>3D-Integration: Trends and Opportunities – An Overview</i> (Materials Research Society 2003)
APPLE-1037	R. Kujala, et. al., <i>Solderless Interconnection and Packaging Technique for Embedded Active Components</i> (IEEE 1999)
APPLE-1038	U.S. Patent Publication No. 2001/0026010 to Horiuchi (“Horiuchi”)
APPLE-1039	U.S. Patent No. 6,038,133 to Nakatani et al. (“Nakatani-II”)
APPLE-1040	U.S. Patent No. 5,250,843 to Eichelberger (“Eichelberger”)
APPLE-1041	International Patent Application WO1996012296 to Suwa et al. and Certified Translation (“Suwa”)
APPLE-1042	Japanese Patent Application No. 2002-83926 to Enomoto et al. and Certified Translation (“Enomoto”)
APPLE-1043	European Patent Publication No. EP1069616 to Kurita (“Kurita”)
APPLE-1044	Aggrarwal, A., et al., <i>A Model for Hierarchical Memory</i> , IBM T. J. Watson Research Center, Proceedings of the Nineteenth Annual ACM Symposium on Theory of Computing, 305-314 © 1987
APPLE-1101	Complaint for Patent Infringement (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1
APPLE-1102	Amended Complaint for Patent Infringement (April 11, 2024), Case No. 1-24-cv-00129 (WDTX), Document 31 (redacted)

- APPLE-1103 K. Vidal Memorandum on *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, June 21, 2022
- APPLE-1104 *United States District Courts – National Judicial Caseload Profile* (June 2024) (retrieved from https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0630.2024.pdf)
- APPLE-1105 Exhibit 10 to Complaint for Patent Infringement – Infringement Claim Chart for '527 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-10
- APPLE-1106 Return of Service (February 8, 2024), Case No. 1-24-cv-00129 (WDTX), Document 8

LISTING OF CLAIMS

Claim 1	
[1pre]	An electronic module, comprising:
[1a]	a first conductive-pattern layer having a first surface,
[1b]	first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[1c]	a component having flat contact zones,
[1d]	second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and
[1e]	an insulating-material layer on the first surface of the first conductive-pattern layer,
[1f-i]	wherein the component is embedded in the insulating-material layer
[1f-ii]	and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.
Claim 2	
[2a]	The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,
[2b]	and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.

Claim 3	
[3]	The electronic module of claim 1, wherein the first solid contact bumps include a layered structure, containing at least two layers of at least two different materials.
Claim 4	
[4]	The electronic module of claim 1, wherein the component is a microcircuit.
Claim 5	
[5]	The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.
Claim 6	
[6a]	The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer,
[6b]	and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.
Claim 7	
[7]	The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer by means of said second solid contact bumps.
Claim 8	
[8]	The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

Claim 9	
[9]	The electronic module of claim 1, wherein the insulating-material layer is a glass-fiber reinforced epoxy sheet.
Claim 10	
[10]	The electronic module of claim 1, wherein the insulating-material layer is a flexible organic sheet.
Claim 11	
[11]	The electronic module of claim 1 wherein the metallurgically electrical connection are ultrasonic or thermo-compression connections.
Claim 12	
[12]	The electronic module of claim 11 wherein the metallurgically electrical connections are facilitated by the presence of one or more metals selected from the group consisting of copper, aluminum, gold and tin.
Claim 13	
[13pre]	An electronic module, comprising:
[13a]	a first conductive-pattern layer having a first surface,
[13b]	a second conductive-pattern layer having a second surface,
[13c]	an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
[13d]	first solderless contact bumps made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[13e]	a component having fiat contact zones embedded in the insulating-material layer,
[13f]	second solderless contact bumps made on the flat contact zones and metallurgically and electrical connected thereto, and

[13g]	wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solderless contact bumps made on the first surface of the first conductive-pattern layer by means of the second solderless contact bumps made on said flat contact zones.
Claim 14	
[14]	The electronic module of claim 13, wherein the first solderless contact bumps include a layered structure, containing at least two layers of at least two different materials.
Claim 15	
[15]	The electronic module of claim 14, wherein the component is a microcircuit.
Claim 16	
[16]	The electronic module of claim 13, wherein the second conductive-pattern layer is configured to protect the component against electromagnetic radiation.
Claim 17	
[17]	The electronic module of claim 13, comprising a plurality of components having flat contact zones and second solderless contact bumps made on the flat contact zones, the flat contact zones being metallurgically and electrically connected to the first contact bumps made on the first surface of the first conductive-pattern layer by means of said second solderless contact bumps.
Claim 18	
[18]	The electronic module of claim 17, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

Claim 19	
[19pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:
[19a]	a first conductive-pattern layer having a first surface,
[19b]	first solderless contact bumps made on the first surface of the first conductive-pattern layer,
[19c]	an insulating-material layer on the first surface of the first conductive-pattern layer, and
[19d]	a component embedded in the insulating-material layer and having flat contact zones,
[19e]	second solderless contact bumps made on the flat contact zones of the component,
[19f]	wherein, the flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via the first solderless contact bumps made on the first surface of the first conductive-pattern layer and the second solderless contact bumps made on the flat contact zones of the component.
Claim 20	
[20]	The multi-layered electronic module according to the claim 19, comprising a plurality of memory circuits.
Claim 21	
[21]	The multi-layered electronic module according to claim 19, wherein the electronic modules are electrically connected to each other in order to form a multilayered functioning totality.
Claim 22	
[22pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of said plurality of electronic modules comprises:

[22a]	a first conductive-pattern layer having a first surface,
[22b]	first solderless contact bumps made on the first surface of the first conductive-pattern layer,
[22c]	an insulating material layer on the first surface of the first conductive-pattern layer, and
[22d]	a component embedded in the insulating-material layer, the component having flat contact zones,
[22e]	second solderless contact bumps made on the fiat contact zones of the component, and
[22f]	wherein the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first conductive-pattern layer by means of the second solderless contact bumps made on the fiat contact zones and the first solderless contact bumps made on the first surface of the first conductive-pattern layer.
Claim 23	
[23]	The multi-layered electronic module according to claim 22, comprising a plurality of memory circuits.
Claim 24	
[24]	The multi-layered electronic module according to claim 22, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.
Claim 25	
[25pre]	A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:
[25a]	a first conductive-pattern layer having a first surface,
[25b]	a second conductive-pattern layer having a second surface,

[25c]	an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
[25d]	first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,
[25e]	a component having flat contact zones embedded in the insulating-material layer,
[25f]	second solid contact bump solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and
[25g]	wherein the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to the first conductive pattern layer via respective first and second solid contact bumps.
Claim 26	
[26]	The multi-layered electronic module according to claim 25, comprising a plurality of memory circuits.
Claim 27	
[27]	The multi-layered electronic module according to claim 25, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-27 (“the Challenged Claims”) of U.S. Patent No. 7,609,527 (“the ’527 patent”).

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Apple certifies that the ’527 patent is available for IPR. The present Petition is being filed within one year of service of a complaint by ImberaTek, filed February 5, 2024 and served February 6, 2024. *See* APPLE-1101; APPLE-1106.

Petitioner is not barred or estopped from requesting review of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested

Petitioner requests institution of IPR and cancellation of the Challenged Claims based on the following grounds:

Ground	Claims	Basis under 35 U.S.C. § 103
1A	1-2, 4-6, 11-13, 15-16, 19, 21, 25, 27	Nishiuma
1B	7-8, 17-18	Nishiuma in view of Nakatani
1C	20, 26	Nishiuma in view of Nakatani and Yoneyama
1D	3, 14	Nishiuma in view of Shibata
2	1-27	Yoneyama in view of Onda

Grounds 1A-2 are further supported by the expert testimony of Dr. R. Jacob Baker. *See* APPLE-1003, ¶¶1-319.

The '527 patent claims priority through several intervening applications to a foreign application filed February 26, 2003. APPLE-1002, 53-54; APPLE-1001, Cover, 1:6-10 (cross-reference paragraph). Petitioner does not concede that any claim of the '527 patent is entitled to the benefit of the alleged priority application filing dates; nonetheless, all references forming the basis of the grounds predate the filing of each of these applications. Petitioner accordingly treats February 26, 2003 as the Critical Date for purposes of the analysis in this Petition. APPLE-1003, ¶¶39, 42.

Reference ¹	Filing Date	Publication Date	Pre-AIA Prior Art Status
Nishiuma (APPLE-1004)	December 30, 1994	April 1, 1997	§§102(a)-(b), (e)
Nakatani (APPLE-1007)	November 16, 2001	October 31, 2002	§§102(a), (e)
Shibata (APPLE-1005)	July 16, 2001	October 17, 2002	§§102(a), (e)
Yoneyama (APPLE-1013)	--	September 27, 2002	§102(a)

¹ This Petition cites certified English translations of Yoneyama and Onda to identify relevant aspects of the underlying prior art references. Exhibits APPLE-1013 and APPLE-1008 include both the English translation and the underlying Japanese reference for Yoneyama and Onda, respectively.

Onda (APPLE-1008)	--	March 30, 2001	§§102(a)-(b)
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Nishiuma, Nakatani, Shibata, Yoneyama, and Onda are all analogous art to the '527 patent in that they are all in the same field of endeavor and/or reasonably pertinent to the problems said to be addressed by the '527 patent. APPLE-1003, ¶55. For example, like the '527 patent, each of the prior art references applied in Grounds 1A-2 describes techniques for manufacturing and packaging electronic modules. *Id.*; APPLE-1001, 1:13-28; *infra*, §IV; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

C. Level of Ordinary Skill in the Art

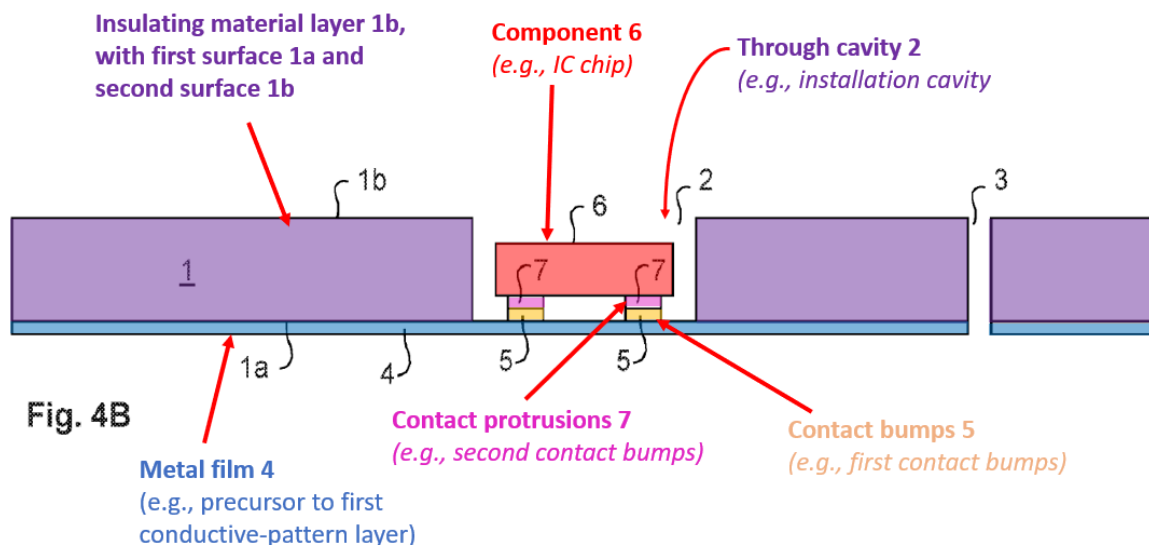
A person of ordinary skill in the art relating to the subject matter of the '527 patent as of the Critical Date (“POSITA”) would have had a Bachelor’s degree in electrical engineering, materials science, applied physics, or a related technical field, and 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. APPLE-1003, ¶¶39-41. Additional education could substitute for professional experience, and *vice versa. Id.*

III. SUMMARY OF THE '527 PATENT

A. Brief Description

The '527 patent describes “an electronic module which includes one or more

components embedded in an installation base.” APPLE-1001, 1:16-18, 3:56-57; APPLE-1003, ¶¶42-46. In the method, “[a]n unpatterned metal film 4, which acts as the conducting surface of the installation base for the components 6 to be installed and connected, is made on the first surface 1a of the insulating substance layer 1.” *Id.*, 6:22-26. “[C]onductive patterns 14 are formed from the conductive layer 4.” *Id.*, 10:28-29, FIGS. 6A-6C.



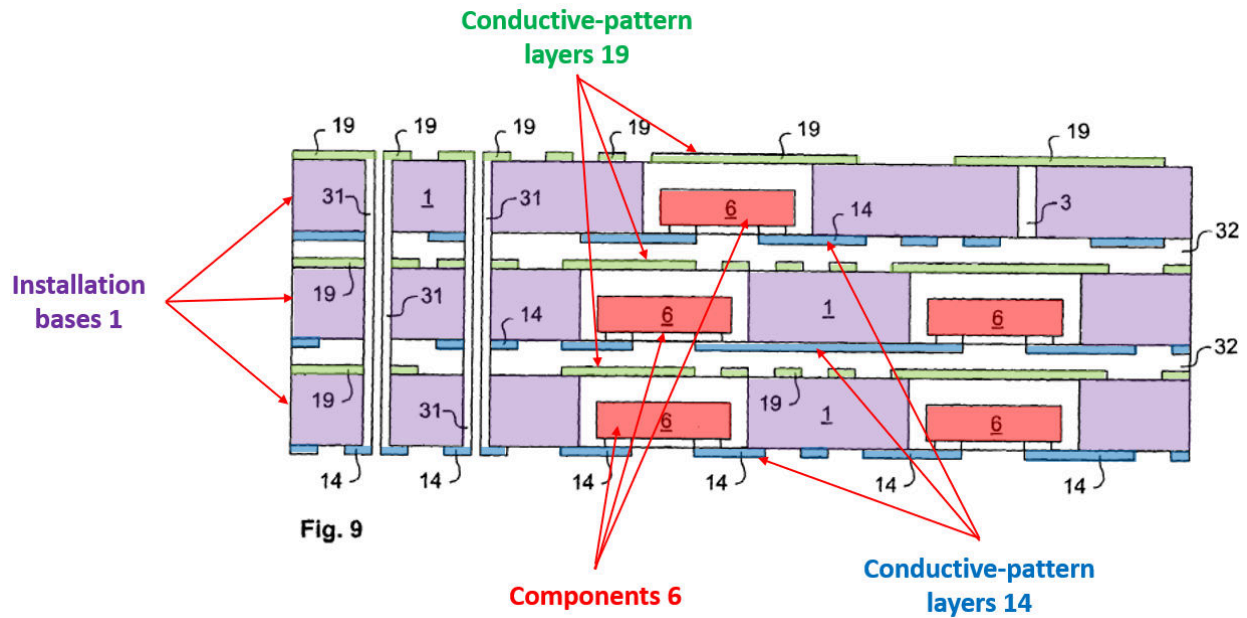
APPLE-1001, FIG. 4B (annotated)

As shown above, “component 6, which includes contact bumps 7 in the connection zones of the component, is connected to the installation base.” *Id.*, 9:19-21. “[C]ontact bumps 5 are also formed on top of the conductive layer 4 [and t]he contact bumps 7 of the component are then connected to the contact bumps 5

of the installation base [by] the ultrasonic or thermo-compression methods.” *Id.*, 9:36-41; *see also id.*, 7:33-35, FIGS. 7A-7C, 8A-8C.

The specification explains that, through use of the contact bumps, “[s]oldering is not needed in the connections of the components, [and] instead an electrical connection between the connection zones on the surface of the component and the ... installation base is created, for example, by ultrasonic welding, thermo-compression, or some other such method” *Id.*, 4:19-26, 4:51-52, 5:8-11.

The ’527 patent describes with reference to FIG. 9, “a multi-layered electronic module, which includes three installation bases 1 laminated on top of each other, together with their components 6, and a total of six conductive-pattern layers 14 and 19.” *Id.*, 11:53-56.



APPLE-1001, FIG. 9 (annotated)

B. Prosecution History

The Applicant amended the claims in response to the first and only Office Action during prosecution as shown below. APPLE-1003, 58-58, 84-90; APPLE-1003, ¶¶47-51.

1. (Currently Amended) An electronic module, comprising:

- a first conductive-pattern layer having a first surface,
- ~~first solid~~ contact bumps solderlessly made on the first surface of the first conductive-pattern layer, layer and metallurgically and electrically connected thereto,
- a component having flat contact zones,
- second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and
- an insulating-material layer on the first surface of the first conductive-pattern layer.

wherein the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, metallurgically and electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.

APPLE-1002, 84

See also id., APPLE-1002, 91-93.

The Examiner subsequently allowed the application, and referenced the first and second contact bumps in the reasons for allowance: “the best prior art references... fail[] to teach or fairly suggest ... the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.” APPLE-1002, 102-105. However, as discussed in §IV, the application never should have been allowed. All features recited in the Challenged Claims are disclosed in one or more of Nishiuma, Yoneyama,

Nakatani, Shibata, and Onda, none of which were considered by the Office, and the claimed combinations of these features would have been obvious before the Critical Date. APPLE-1003, ¶¶50-51, 54-319.

C. Claim Construction

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. Here, Petitioner submits that formal claim constructions are presently unnecessary in view of the substantial overlap between the prior art teachings applied in Grounds 1A-2 and the preferred embodiments of the '527 patent.² *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“claim terms need only be construed to the extent necessary to resolve the controversy”); APPLE-1003, ¶¶52-53. This Petition also applies the prior art in a manner consistent with Patent Owner’s allegations of infringement before the district court. *See* APPLE-1105.

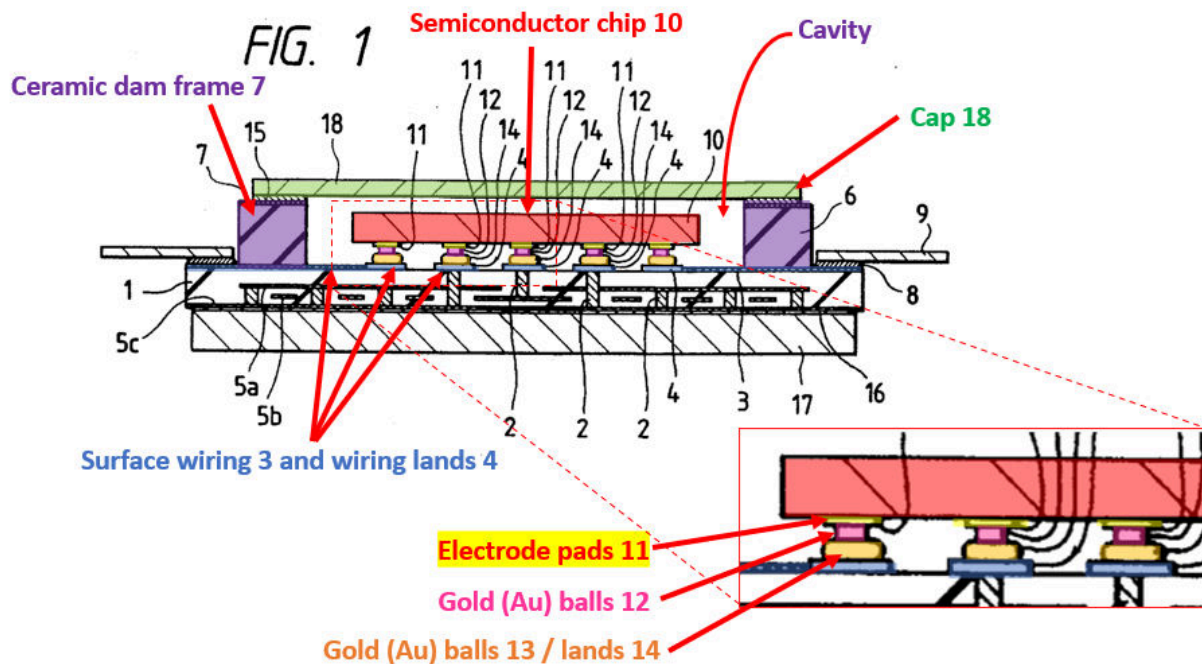
² Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A – Nishiuma Renders Obvious Claims 1-2, 4-6, 11-13, 15-16, 19, 21, 25 and 27

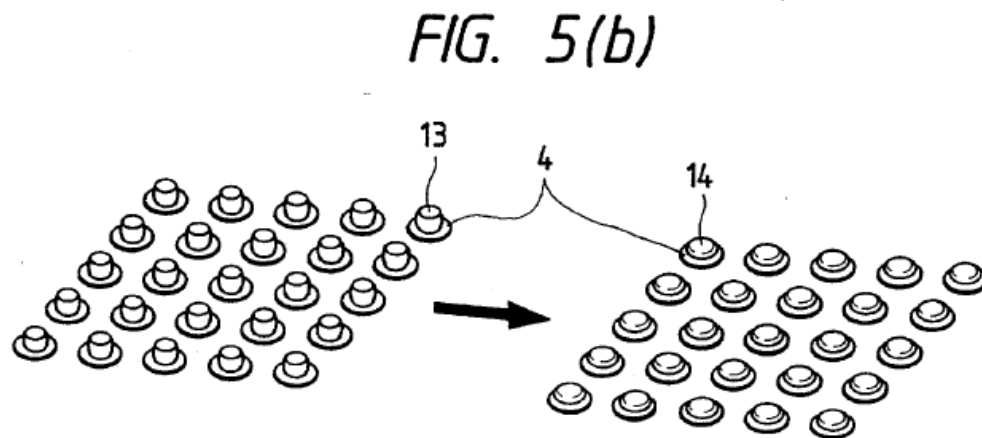
1. Nishiuma Overview (APPLE-1004)

Nishiuma describes a “semiconductor integrated circuit device” formed as “a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.” APPLE-1004, Abstract, 6:66-7:2; APPLE-1003, ¶¶56-58. Nishiuma’s ceramic “square dam frame 6” “forms a cavity in which the semiconductor chip 10 is mounted.” APPLE-1004, 7:48-54. Nishiuma’s “cap 18” is bonded to “the frame 6 through a sealing metallize 7 and brazing filler metal 15.” *Id.*, 7:51-55.



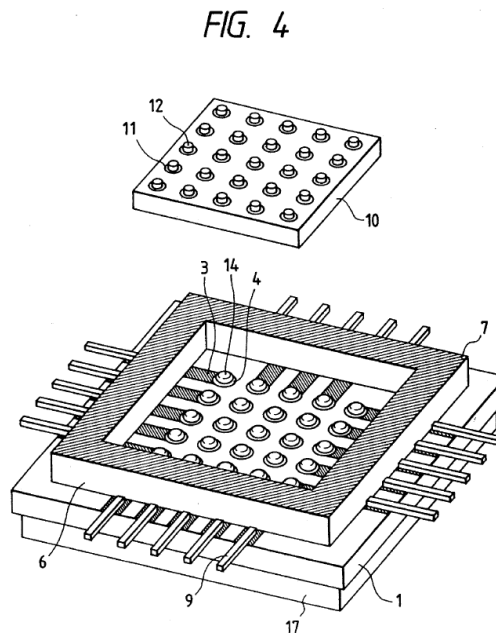
APPLE-1004, FIG. 1 (annotated and modified to include excerpt)

As shown in FIG. 1, Nishiuma's wiring substrate 1 includes surface wiring 3 and wiring lands 4 made of "thick films of refractory metal." APPLE-1004, 7:67-8:3. Nishiuma's gold (Au) balls 13 (not shown in FIG. 1) are bonded to wiring lands 4 "using heat or ultrasonic energy or both" and flattened to form Au lands 14. *Id.*, 8:18-19, 8:28-29, 9:4-6.



APPLE-1004, FIG. 5(b)

Nishiuma's "semiconductor chip 10" includes "electrode pads 11" that are "made of [gold] similarly to the integrated circuit wirings." APPLE-1004, 8:10-16. Au balls 12 are "bonded to the electrode pads 11 of the semiconductor chip 10" using "heat or ultrasonic energy or both" and are then bonded to Au lands 14 by "thermocompression bonding" to achieve electrical connection between the semiconductor chip and surface wiring. *Id.*, 8:17-19, 9:13-16, 7:43-47.



2. Analysis

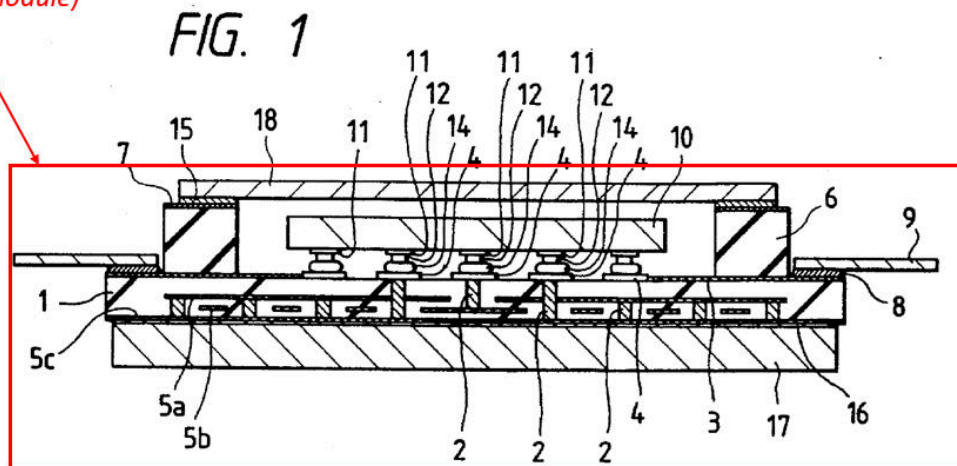
a) Claim 1

[1pre]

To the extent the preamble is limiting, Nishiuma renders [1pre] obvious. APPLE-1003, ¶¶59-60. Nishiuma describes a semiconductor integrated circuit device that constitutes an “*electronic module*” as claimed. APPLE-1004, 1:11-17 (“The present invention relates to a semiconductor integrated circuit device fabrication technique and a semiconductor integrated circuit device ... and particularly to a technique for connecting a semiconductor chip to a printed wiring board by face down bonding of a semiconductor chip to a wiring substrate using metallic bumps”); *cf.* APPLE-1001, 1:18-23 (’527 patent describing that an

electronic module “can be a module like a circuit board, which includes several components [such as] semiconductor components”). For example, Nishiuma’s FIG. 1 depicts that “the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.” APPLE-1004, 6:66-7:2; APPLE-1003, ¶¶56-59.

Semiconductor
integrated circuit device
(electronic module)



APPLE-1004, FIG. 1 (annotated)

Additionally or alternatively, the portion of Nishiuma’s device from the surface wirings 3 and above by itself constitutes an “*electronic module*,” as addressed further below in element [19pre]. APPLE-1003, ¶¶60, 126-128.

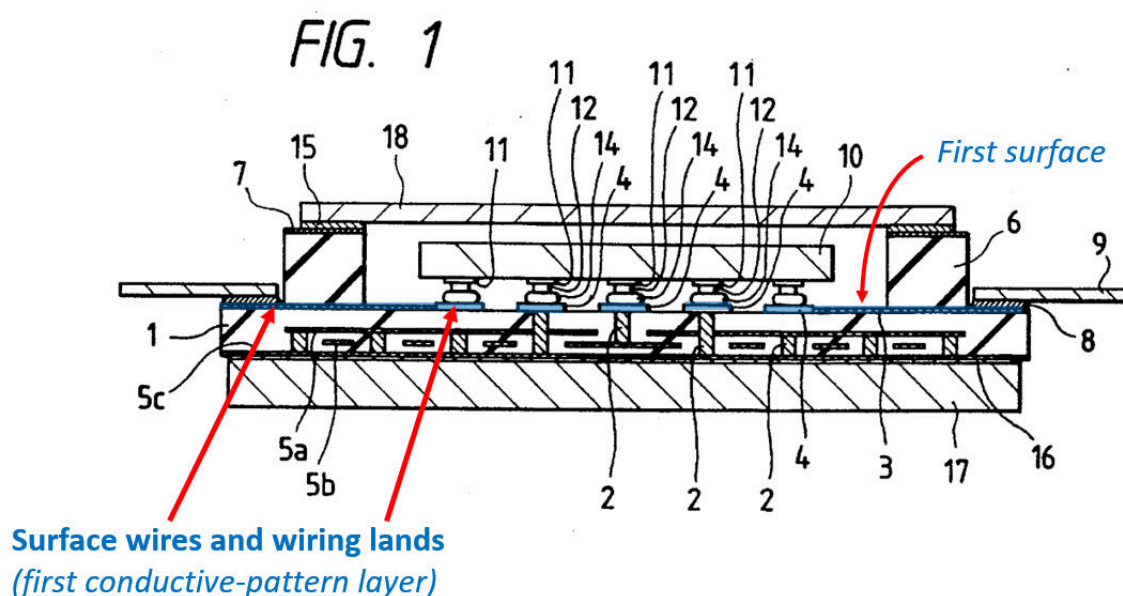
[1a]

Nishiuma renders obvious element [1a]. APPLE-1003, ¶¶61-65. For

example, Nishiuma describes that “a plurality of surface wires 3 and a plurality of wiring 1 and electrodes 4 are formed” on the printed wiring board surface.

APPLE-1004, 7:7-10, 7:14-16, FIG. 1. Nishiuma further explains that the printed wiring board surface may include wiring lands 4. *Id.*; APPLE-1003, ¶¶61-63.

Nishiuma's surface wires and wiring lands collectively provide a “*first conductive-pattern layer*” having “*a first surface*,” atop the surface wiring and wiring lands.



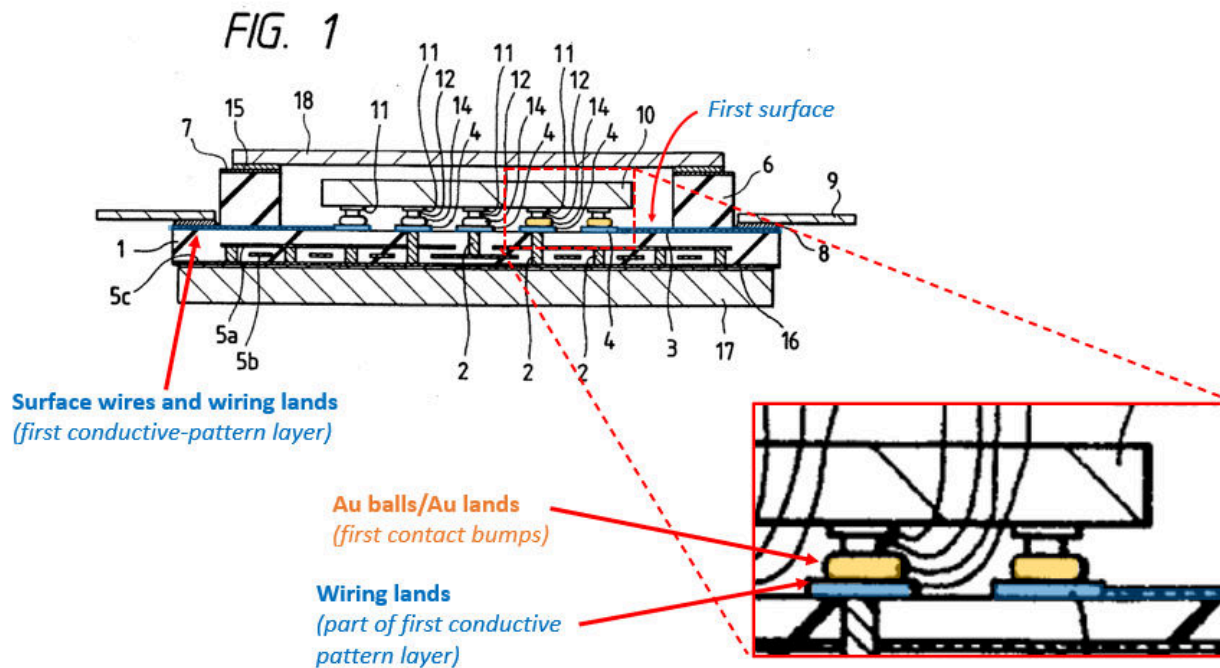
APPLE-1004, FIG. 1 (annotated)

Indeed, it would have been obvious to a POSITA that the surface wires and wiring lands, described by Nishiuma as formed of the same materials and with the same screen-printing technique, cooperate as a conductive layer to transmit power and information signals. APPLE-1004, 7:16-18 (“The surface wirings 3 are wirings for input/output signals, GND, and power source, one end of each of

wirings is connected to one of the wiring lands 4.”), 7:11-14 (“surface wiring 3[and] lands 4 ... are made of thick films of a refractory metal”), 7:66-8:3 (“surface wiring 3 and wiring land 4...are formed on the surface of the printed wiring board 1 by a known screen printing method”), 2:60-3:10; *cf.*, APPLE-1001, 6:50-57 (similarly describing layers comprised of multiple components); APPLE-1105 (ImberaTek’s infringement charts treating multiple components as a layer); APPLE-1003, ¶¶63-65. The dispersed arrangement of electrodes and contact points provided by the surface wires and wiring lands form further forms patterning in the conductive layer as claimed.

[1b]

Nishiuma renders obvious element [1b]. APPLE-1003, ¶¶66-71. For example, Nishiuma describes that “Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1....” APPLE-1004, 8:28-29. After bonding the Au balls to the wiring lands, “Au lands 14 are formed by pressing and flattening the Au balls 13....” *Id.*, 8:46-48. Au balls 13 before pressing/flattening and/or Au lands 14 after pressing/flattening provide “***first solid contact bumps***” made on a first surface of the wiring lands (***first surface of the first conductive-pattern layer***) as claimed. APPLE-1003, ¶¶66-67.



APPLE-1004, FIG. 1 (modified to include close-up, annotated)

Nishiuma describes that the “Au balls 13 are bonded to the wiring lands 4” “using heat or ultrasonic energy or both or a thermo-compression bonding.”

APPLE-1004, 2:60-3:21, 8:17-19, 8:28-29. A POSITA would have understood and found obvious that Nishiuma’s “ball-bonding method” is a *solderless* method of directly bonding gold balls to wiring lands. *Id.*, 7:43-47; APPLE-1003, ¶¶68-69. Indeed, Nishiuma explicitly touts that the “[a]ccording to the present invention, since *solder, which is prone to thermal fatigue, is not used*, reliability of the connection part between the semiconductor chip and the wiring substrate is

improved.” APPLE-1004, 4:10-13³; *see also id.*, 4:25-31, 9:27-59, 10:23-56.

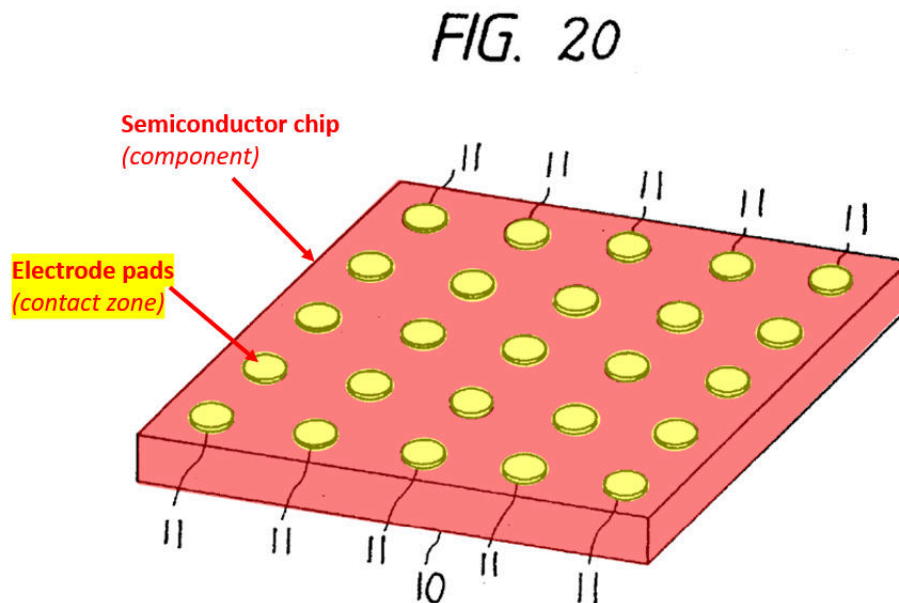
A POSITA likewise would have understood and found obvious that the bonding of the gold balls to the wiring lands results in a *metallurgical and electrical connection* between the balls (*first solid contact bumps*) and the top of the wiring lands (*first surface of the first conductive-pattern layer*). APPLE-1003, ¶¶70-71, 35-38. The heat, ultrasonic energy, and thermo-compression techniques described in Nishiuma each provides metallurgical bonding that allows an electrical current to flow between the semiconductor chip and board wiring through the Au and wiring lands. *See* APPLE-1004, 10:19-21 (“improve the reliability of connection ...”), 7:43-47 (“The wiring lands 4 of the printed wiring board 1 is *electrically connected* to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding.”). The ’527 patent notably describes the same solderless processes including “ultrasonic welding” and “thermo-compression” as those described in Nishiuma, which yield the metallurgical and electrical connections as claimed. *Cf.* APPLE-1001, 6:41-49, 4:19-65; APPLE-1004, 8:17-19, 8:28-29, 14:37-46.

[1c]

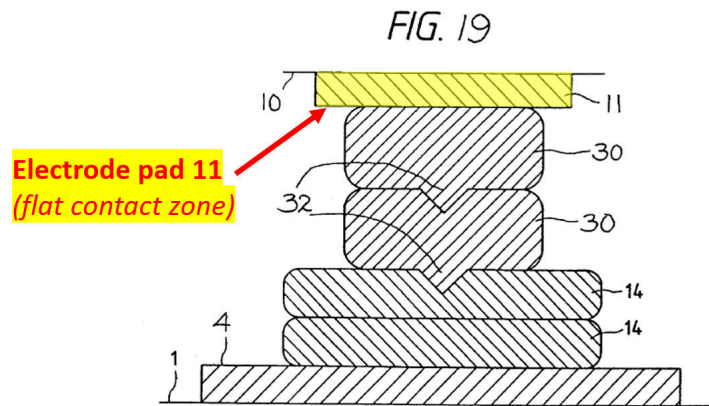
Nishiuma renders obvious element [1c]. APPLE-1003, ¶¶72-75. For

³ All emphasis added unless indicated otherwise.

example, Nishiuma describes that the semiconductor chip 10 (*component*) includes electrode pads 11 that, for example, can be “made of Au similarly to the integrated circuit wirings” and that provide *contact zones* for electrically connecting the semiconductor chip 10 to the wiring lands 4 via contact bumps. *Id.*, 8:13-16, FIG. 1; *see also id.*, 7:2-6, 8:13-16 (“electrode pads 11 are formed by boring holes in the surface protection film”), 17:46-48, FIGS. 3-4; APPLE-1003, ¶¶72-74. As illustrated in FIGS. 19 and 20 (reproduced below), the electrode pads have flat contact surfaces and Nishiuma therefore discloses and renders obvious “*flat contact zones*” consistent with the plain meaning of a contact zone that is “flat” as claimed. APPLE-1003, ¶¶73-74.



APPLE-1004, FIG. 20 (annotated)



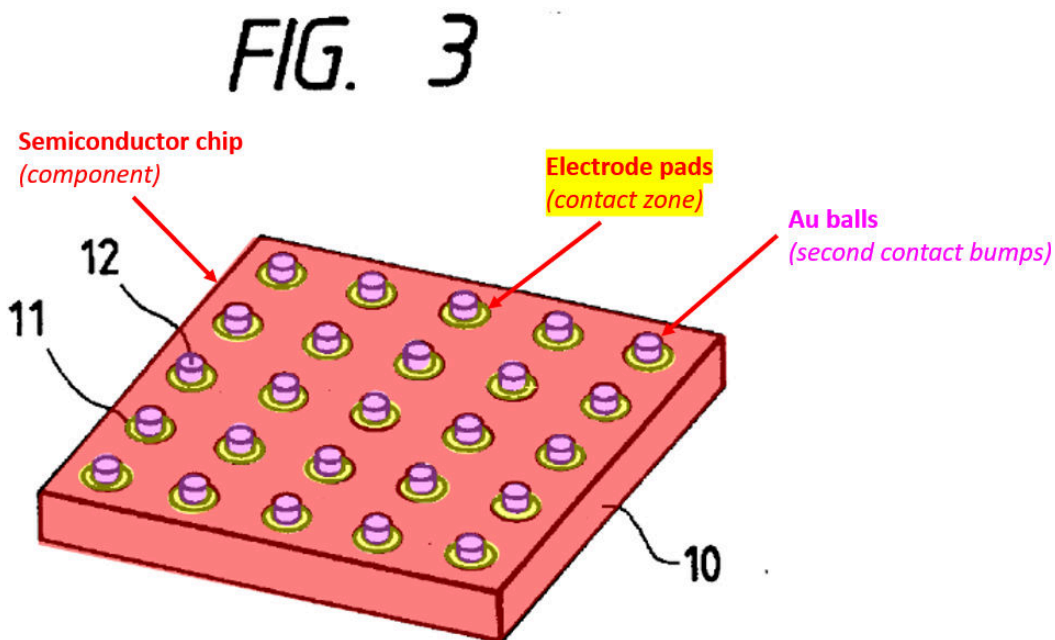
APPLE-104, FIG. 19 (annotated)

The claims recite no language requiring that the flat contact zones also not protrude from a surrounding surface of the component, and neither the specification nor file history support include lexicography or disavowals that would support such a limiting interpretation. Nonetheless, non-protruding flat contact zones were also well-known by the Critical Date and would have been obvious to use in Nishiuma's device. APPLE-1003, ¶75; APPLE-1008, FIGS. 1, 5-10. Nishiuma contemplates use of various high-frequency semiconductor chips and attributes no particular significance to the use of protruding electrode pads—even suggesting that the electrode pads could be formed in a manner that would not yield protrusions. APPLE-1004, 8:10-16 (“electrode pads 11 are formed by boring holes in the surface protection film”), 17:31-42, 7:2-6, 8:10-12, 1:57-2:17; APPLE-1003, ¶75. A POSITA would have considered the option of selecting a chip having non-protruding electrode pads to be an obvious design choice

depending on the application, and would have been motivated to use non-protruding pads in certain applications to reduce the thickness of the chip, and consequently, the electronic module as a whole. APPLE-1003, ¶75.

[1d]

Nishiuma renders obvious element [1d]. APPLE-1003, ¶¶76-81. For example, Nishiuma describes “Au balls 12 ... [that] are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10.” APPLE-1004, 7:41-43, 8:17-19. Au balls 12 constitute “*second solid contact bumps*” made on the electrode pads 11 (*contact zones*) of the semiconductor chip (*component*) as claimed. APPLE-1003, ¶¶76-77.



APPLE-1004, FIG. 3 (excerpted, annotated)

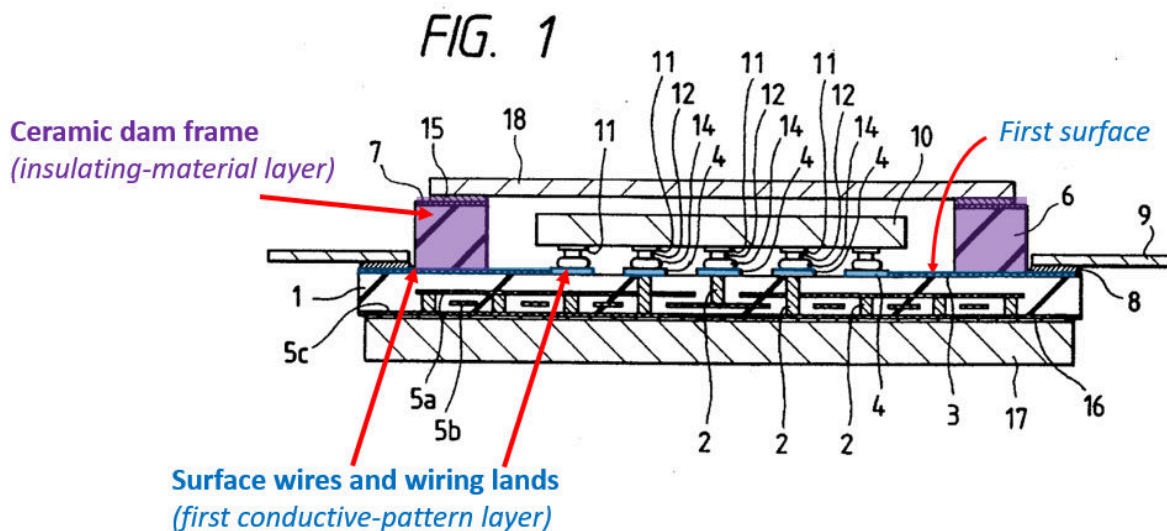
Nishiuma describes that the “Au balls 12 are bonded to the electrode pads 11 ... by a known ball-bonding method using heat or ultrasonic energy or both.” APPLE-1004, 8:17-19; *see also id.*, 2:64-67 (describing methods including “heat or ultrasonic energy, or both or a thermo-compression bonding.”), 10:56-65, 17:19-22. As described above, a POSITA would have understood and found obvious that Nishiuma’s “ball-bonding method” is a *solderless* method in which gold balls are bonded directly to the electrode pads, and Nishiuma explicitly contrasts these methods with solder-based bonding methods that are prone to fatigue. APPLE-1004, 4:10-13; *see also id.*, 8:17-19, 2:64-67, 4:25-31, 9:27-59, 10:23-65, 17:19-22; APPLE-1003, ¶¶78-79.

A POSITA similarly would have understood and found obvious that the bonding of the gold balls to the electrode pads results in a *metallurgical and electrical connection* between the balls (*second solid contact bumps*) and the pads (*flat contact zones*). APPLE-1003, ¶¶80-81, 35-38. The heat, ultrasonic energy, and thermo-compression techniques described in Nishiuma each provides metallurgical bonding that allows an electrical current to flow between the semiconductor chip and board wiring through the gold balls and electrode pads. *Id.*; *see also* APPLE-1004, 10:19-21, 7:41-47 (“electrically connected”). The ’527 patent notably describes the same solderless processes including “ultrasonic welding” and “thermo-compression” as those described in Nishiuma, which yield

metallurgical and electrical connections as claimed. *Cf.* APPLE-1001, 6:41-49, 4:19-65; APPLE-1004, 8:17-19, 8:28-29, 14:37-46.

[1e]

Nishiuma renders obvious element [1e]. APPLE-1003, ¶¶82-84. For example, Nishiuma describes that “[a] square dam frame 6 for sealing is formed around the semiconductor chip 10 on the wiring board 1.” APPLE-1004, 7:48-55, 8:5-9. As shown in FIG. 1, dam frame 6 is disposed on a top surface of the surface wiring 3 (*first surface of the first conductive-pattern layer*). APPLE-1004, FIG. 1; APPLE-1003, ¶82.



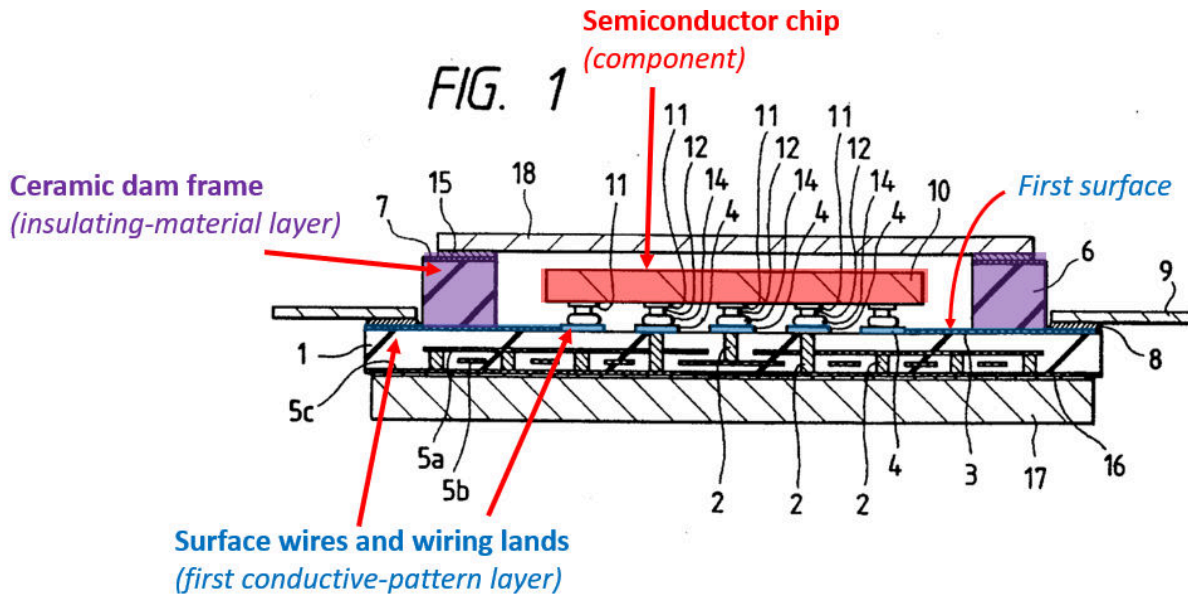
APPLE-1004, FIG. 1 (annotated)

Nishiuma further describes that “[t]he dam frame 6 is made of ceramic such as alumina or aluminum nitride,” which a POSITA would have understood to be an

electrical insulator, and which would have been obvious to implement as an insulator to prevent electrical signals from wiring 3 from conducting to other components contacted by dam frame 6 or causing undesirable electrical short circuiting. APPLE-1004, 7:49-51; APPLE-1003, ¶¶83-84 (citing APPLE-1010, 1:9-17 (describing ceramic as “a suitable electrically insulating material”); APPLE-1011, [0006] (describing chip carrier packages formed from ceramic and alumina insulators)). Accordingly, Nishiuma’s dam frame provides an “*insulating-material layer*” as claimed.

[1f-i]

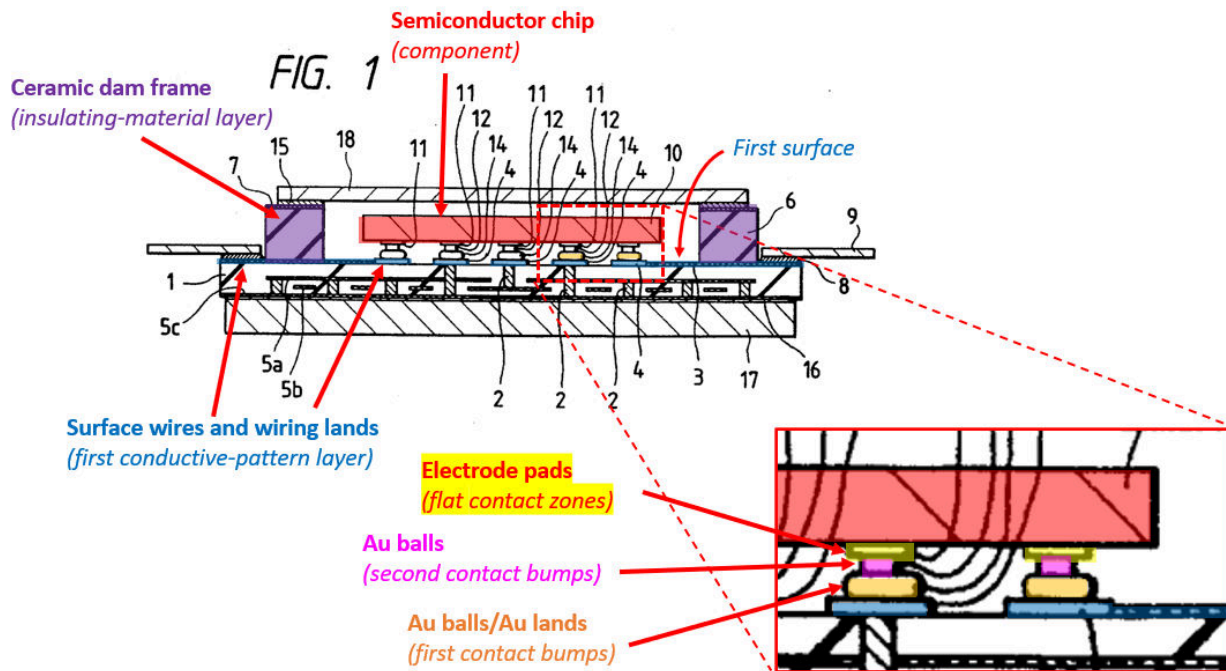
Nishiuma renders obvious element [1f-i]. APPLE-1003, ¶¶85-87. For example, Nishiuma describes that “[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted.” APPLE-1004, 7:53-54. As shown in FIG. 1, Nishiuma’s device thus provides a semiconductor chip (*component*) embedded in the ceramic dam frame (*insulating-material layer*). APPLE-1004, FIGS. 1, 6, *cf.*, APPLE-1001, 7:58-8:2 (explaining that the component is “embedded entirely inside the installation base” when the “insulating-material layer 1 ... [is] thicker than the component to be installed”), 8:13-14; APPLE-1003, ¶¶85-87.



APPLE-1004, FIG. 1 (annotated)

[1f-ii]

Nishiuma renders obvious element [1f-ii]. APPLE-1003, ¶¶88-91. For example, Nishiuma teaches that the Au balls 12 (*second solid contact bumps*) formed on the semiconductor electrode pads (*flat contact zones of the component*) are connected to the Au lands 14 (*first solid contact bumps*) formed on the surface wiring and wiring lands of the circuit board (*first surface of the first-conductive pattern layer*) after bonding Au lands 14 to Au ball 12. APPLE-1004, 7:43-47, 9:13-22, FIG. 1.



APPLE-1004, FIG. 1 (modified to include closeup, annotated)

Nishiuma further explains that “[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding.” APPLE-1004, 7:43-47, 2:60-67 (“heat or ultrasonic energy, or both or a thermo-compression bonding”); APPLE-1003, ¶¶89-91. A POSITA would have understood and found obvious that Nishiuma’s “thermo-compression bonding” between Au balls 12 and Au lands 14 is a *solderless* method that achieves *electrical and metallurgical connection* between the two gold balls. APPLE-1004, 4:10-12 (“since solder, which is prone to thermal fatigue, is not used [in the present invention], reliability of the connection ...is improved”), 9:13-9:22, 8:17-

19, 11:13-18, 13:11-13, 14:13-34, FIGS. 28a-c; APPLE-1003, ¶¶89. Bonding of the Au balls on the electrode pads to Au lands on the surface wiring/lands results in a ***metallurgical and electrical connection*** in a manner consistent with the '527 patent's own description of thermocompression bonding as a solderless method of forming metallurgical and electrical connections. APPLE-1003, ¶¶89, 91, 35-38; APPLE-1001, 6:41-49; APPLE-1004, 8:17-19, 8:28-29, 9:13-26, 14:37-46. As a result of the solderless connection, the electrode pads (***contact zones***) are effectively metallurgically and electrically connected to the surface wiring and wiring lands of the circuit board (***first surface of the first-conductive pattern layer***) after bonding Au lands 14 to Au ball 12. APPLE-1004, 7:43-47, 9:13-22, FIG. 1; APPLE-1003, ¶91.

b) Claim 2

[2a]

Nishiuma renders obvious claim [2]. APPLE-1003, ¶92. For example, as described above in element [1e], Nishiuma teaches that the ceramic dam frame (***insulating-material layer***) has a first surface against the surface wiring/lands (***first conductive pattern layer***) of the printed wiring board and a second surface opposite the first surface. APPLE-1004, 7:48-50 ("A square dam frame 6 for sealing is formed ... on the wiring board 1"), FIG. 1; *supra* §IV.A.2.[1e]. The first and second surfaces of Nishiuma's dam frame (***insulating-material layer***) are

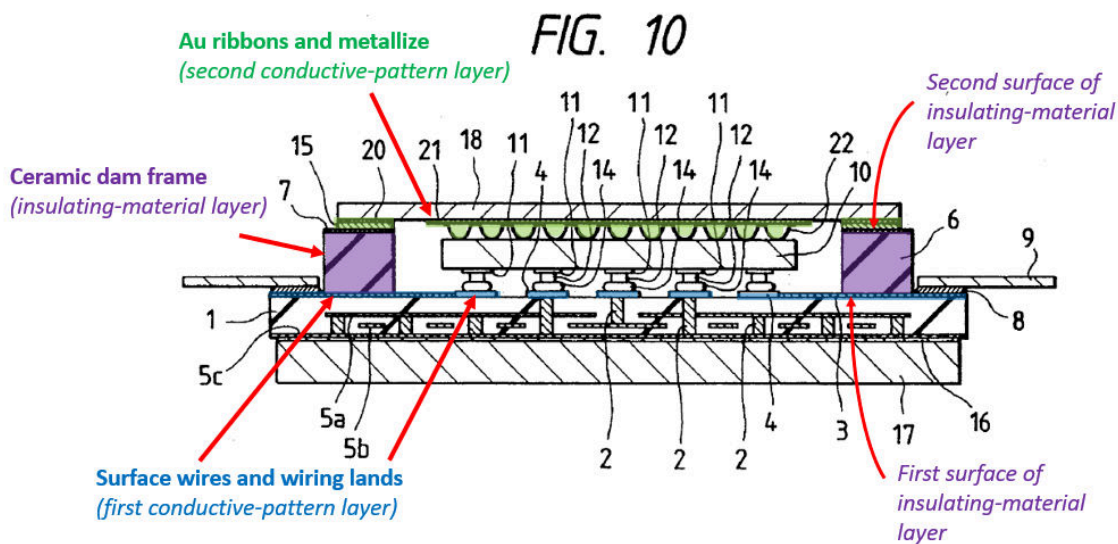
shown in the annotated version of Nishiuma's FIG. 10 below. *Infra*, §IV.A.2.[2b].

[2b]

Nishiuma describes that “the semiconductor integrated circuit device ... has a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.” APPLE-1004, 6:66-7:2, 7:48-60; APPLE-1003, ¶¶93-98. Nishiuma's “cap 18 is bonded to the surface of the frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing.” APPLE-1004, 7:51-61, 9:31-38, 16:38-40.

Nishiuma further describes a configuration of the package structure that includes “a heat conductive media of Au ribbons... in the space between the back of the semiconductor chip 10 ... and the bottom of [the] cap 18 to cool the semiconductor chip 10 by conducting heat through the cap.” *Id.*, 7:58-60, 11:18-24, 11:25-28 (“Both ends of the Au ribbons 22 are bonded to a heat conductive medium forming metallize 21 provided on the bottom of the cap 18[] ...”), 11:29-12:37; FIG. 10. Nishiuma's sealing metallize and brazing filler metal, optionally with the Au ribbons and metallize 21 on the bottom of cap 18, provide a “**second conductive-pattern layer**” as claimed. APPLE-1003, ¶¶94-95. The metallize, brazing filler metal, and Au ribbons are all formed from metallic materials that are both electrically and thermally conductive, and a POSITA would have recognized these elements as cooperating to seal and dissipate heat away from the

semiconductor chip, and they are arranged to form a square pattern around the cavity perimeter and a ribbon pattern over the semiconductor chip. APPLE-1004, 11:36-62 (describing the process for forming a heat conductive media of the semiconductor integrated circuit device), 11:18-28, FIGS. 12-13; APPLE-1003, ¶¶94-97. Nishiuma's second conductive-pattern layer, including at least sealing metallize 7 and brazing filler metal 15, is positioned on the second surface of the dam frame 6 opposite the first surface that abuts the surface wiring 3. APPLE-1003, ¶95.



APPLE-1004, FIG. 10 (annotated)

A POSITA also would have understood the Au ribbons as shown in FIG. 10 to be a variant of the same embodiment of the device shown in FIG. 1 since the Au

ribbons are an addition to the device depicted in FIG. 1. APPLE-1003, ¶95. To the extent it is argued that FIG. 10 represents an embodiment distinct from FIG. 1, however, it would have been obvious to a POSITA to implement Nishiuma's cap with the heat conductive Au ribbons as described with regard to FIG. 10 in the FIG. 1 embodiment to "decrease the thermal resistance of the semiconductor chip" and prevent thermal stresses on the chip and the connection between the chip and the printed circuit board, as Nishiuma expressly describes. APPLE-1004, 11:64-12:37; APPLE-1003, ¶98. A POSITA would have had a reasonable expectation of success in implementing Nishiuma's semiconductor package structure with the Au ribbons and metallize of FIG. 10 because Nishiuma teaches these embodiments are compatible, and the addition of thermally conductive patterns to a cap of a semiconductor device package to dissipate heat is well-known in the art. APPLE-1004, 11:18-19 ("FIG. 10 shows a semiconductor integrated circuit device similar to the one shown in FIG. 1"), 17:32-42; APPLE-1003, ¶98 (citing APPLE-1014, 19:51-54; APPLE-1015, FIG. 11; APPLE-1016, [0144]-[0146]).

c) Claim 4

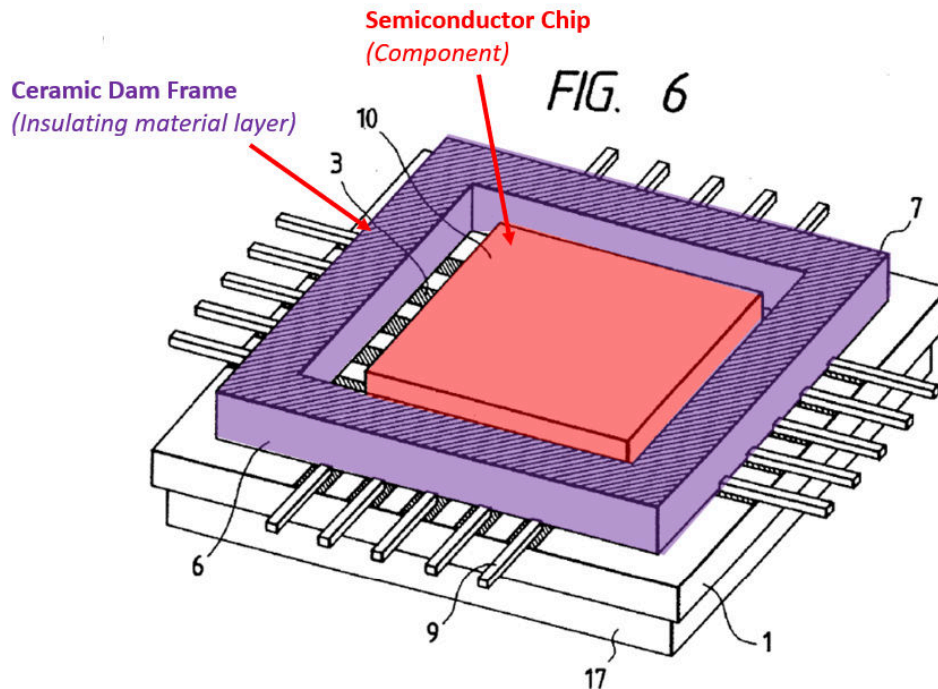
Nishiuma renders obvious claim [4]. APPLE-1003, ¶¶99-100. For example, Nishiuma describes a "semiconductor integrated circuit device" formed as "a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, Abstract, 6:66-7:2. Nishiuma's

semiconductor chip (**component**) is a microcircuit that includes semiconductor material and an integrated circuit like the microcircuits described in the '527 patent itself. For example, Nishiuma discloses that the component can be “a compound semiconductor chip made of[] ... GaAs and having a semiconductor integrated circuit operated on radio frequencies.” APPLE-1004, 17:23-30; *see also id.*, 7:2-6, 8:10-16; *cf.*, APPLE-1001, 1:41-49, APPLE-1003, ¶¶99-100 (citing APPLE-1031 – APPLE-1033); APPLE-1017, 4:14-20 (“an electronic microcircuit card... includes at least one integrated circuit.”).

d) Claim 5

Nishiuma renders obvious claim [5]. APPLE-1003, ¶¶101-103. As described above, Nishiuma’s semiconductor chip (e.g., chip 10) is sealed within a cavity formed in the ceramic dam frame. *Supra* §§IV.A.2.[1e]-[1f-i]; APPLE-1004, 66-7:2; 7:48-8:2, 18:1-5, FIGS. 1, 6; APPLE-1003, ¶¶101, 82-87.

Nishiuma’s semiconductor chip (**component**) is thus entirely protected inside the ceramic dam frame (**insulating-material layer**) surrounding the semiconductor chip and the semiconductor chip is also sealed between the printed wiring board and cap. APPLE-1004, FIG. 6; APPLE-1003, ¶¶102-103 (comparing Nishiuma’s FIG. 6 to the preferred embodiments described in APPLE-1001, FIGS. 1-8C).



APPLE-1004, FIG. 6 (annotated)

e) Claim 6

[6a]

See *supra* §IV.A.2.[2a]; APPLE-1003, ¶¶104, 92-98.

[6b]

Nishiuma renders obvious claim element [6b]. APPLE-1003, ¶¶105-109.

For example, Nishiuma's device includes a cap 18 that is "bonded to the surface of the frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing."

APPLE-1004, 7:51-54. Cap 18, sealing metallize 7, and brazing filler metal 15 are all formed from conductive materials, and whether taken individually or collectively, provide a "**conductive film**" on the second surface of the dam frame 6

(*insulating-material layer*). APPLE-1003, ¶105-106; APPLE-1004, 7:55-59; 7:58-60; *see also id.*, 7:48-60, 11:32-42, 11:56-62. Alternatively, and to the extent (i) element [6b] does not require direct contact between the conductive film and the second surface of the insulating-material layer or (ii) Nishiuma’s dam frame 6 together with metallize 7 and brazing filler metal 15 are collectively taken as the claimed “*insulating-material layer*,” cap 18 alone—or even just the Au plating on cap 18—each also constitutes a “*conductive film*” on the second surface of the insulating-material layer as claimed, since they are all formed of conductive metals. APPLE-1003, ¶107; *cf.* APPLE-1001, 6:27-29 (“metal film [] can also be a surfaced metal film, or some other film including several layers or several materials”).

The language in [6b] that recites “for protecting the component against electromagnetic radiation” is an intended use of the conductive film imparting no additional structural limitation that would not already be met by a conductive film and is therefore not entitled to patentable weight. Regardless, each of the structures described in the preceding paragraph protect the semiconductor chip (*component*) against electromagnetic radiation. APPLE-1003, ¶108. Indeed, a POSITA would have understood and found obvious the metallic materials of Nishiuma’s conductive film—such as the gold-plated copper cap—naturally protect the chip from electromagnetic radiation due to the EM shielding properties

of the disclosed metals. APPLE-1003, ¶109 (citing APPLE-1018, 15:47-16:14; APPLE-1019, [0025]).

f) Claim 11

Nishiuma renders obvious claim [11]. APPLE-1003, ¶¶110-111. For example, as explained above (*supra* §§IV.A Elements [1b], [1d], [1f-ii]), Nishiuma describes that the Au balls 13 and 12 are bonded to the component electrode pads and to the surface wiring, respectively, by “using heat or ultrasonic energy or both” or a “thermo-compression bonding” (APPLE-1004, 8:19; *see also* 2:64-67, 10:56-60, 17:19-23) and that “[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding.” *Id.*, 7:43-47, 2:60-3:21, 8:28-29, 4:10-12, 9:17-9:22, 8:17-19, 14:13-34, FIGS. 28a-c; APPLE-1003, ¶110. Nishiuma’s thermo-compression and ultrasonic bonding techniques result in a metallurgical and electrical connection in the same manner as described in the ’527 Patent. APPLE-1003, ¶¶111, 35-38, 69-71; APPLE-1001, 6:41-63; APPLE-1004, 8:17-19, 8:28-29, 9:13-26, 14:37-46.

g) Claim 12

Nishiuma renders obvious claim [12]. APPLE-1003, ¶¶112-114; APPLE-1001, 6:41-49, 6:61-63, 6:50-54. For example, as explained above (*supra* §§IV.A.2 Elements [1b], [1d], [1f-ii]), Nishiuma describes how connections

between the Au balls 13, Au balls 12, electrode pads, and surface wiring are achieved through ultrasonic connection or thermo-compression bonding techniques. APPLE-1004, 7:43-47, 2:60-3:21, 8:28-29, 4:10-12, 9:17-9:22, 8:17-19, 10:56-60, 17:19-23 14:13-34, FIGS. 28a-c; APPLE-1003, ¶¶112, 69-71, 81. Nishiuma's Au balls 12, Au balls 13 and Au lands 14 are all formed from gold, and the connections involving Au balls 12, Au balls 13, Au lands 14 are all facilitated by the presence of gold. APPLE-1003, ¶¶113-114.

h) Claim 13

[13pre]-[13a]

See supra §§IV.A.2.[1pre]-[1a]; APPLE-1003, ¶¶115-116, 59-66.

[13b]

See supra §IV.A.2.[2b]; APPLE-1003, ¶117. As described above, Nishiuma's sealing metallize and brazing filler metal, optionally along with the Au ribbons and metallize 21 on the bottom of the cap 18, provide a "**second conductive-pattern layer**" which has **a second surface** as claimed. APPLE-1004, 7:51-60, 9:31-38, 11:18-12:37, 16:38-40, FIG. 10; APPLE-1003, ¶¶117, 93-98.

[13c]

See supra §§IV.A.2.[1e], [2a]-[2b]; APPLE-1003, ¶118. As described above, Nishiuma's square dam frame is formed on the wiring board 1 (**first conductive-pattern layer**) and is covered by a cap "bonded to the surface of the

frame 6 through a sealing metallize 7 and brazing filler metal 15 for sealing”
(*second conductive-pattern layer*). APPLE-1004, 7:51; *see also id.*, 7:48-55, 8:5-9,
9:31-38, 16:38-40. Nishiuma’s square dam frame (*insulating-material layer*) is
*between the first surface of the first conductive-pattern layer and the second
surface of the second conductive-pattern layer*, as claimed. APPLE-1004, FIG. 1;
APPLE-1003, ¶¶118, 82-84, 92-98.

[13d]-[13f]

See supra §§IV.A.2.[1b]-[1f-i]; APPLE-1003, ¶¶119-121, 66-87.

[13g]

See supra §§IV.A.2.[1f-i]-[1f-ii]; APPLE-1003, ¶¶122-123, 85-91. As
described above, Nishiuma describes that “[t]he wiring lands 4 of the printed
wiring board 1 is electrically connected to the electrode pads 11 of the
semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-
compression bonding.” *Id.*, 7:43-47, 10:34-43; APPLE-1003, ¶¶85-91.

Accordingly, Nishiuma describes that the electrode pads (*flat contact zones*) are
metallurgically, electrically and solderlessly connected to the Au lands 14 (first
solderless contact bumps) by the Au balls 12 (*second solderless contact bumps*).
APPLE-1003, ¶¶122-123; *supra*, §§IV.A.2.[1f-ii].

i) Claim 15

See supra §§IV.A.2.[4]; APPLE-1003, ¶¶124, 99-100.

j) Claim 16

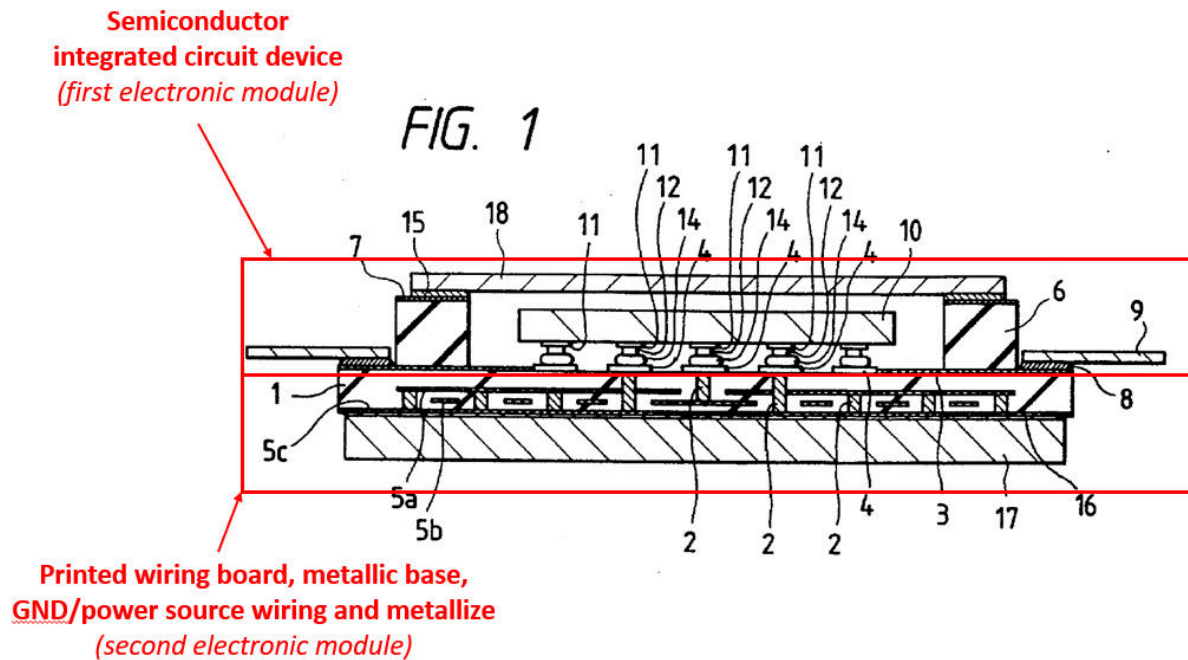
See supra §IV.A.2.[6b]; APPLE-1003, ¶¶125, 105-109. As described above with respect to element [6b], Nishiuma’s sealing metallize and brazing filler metal, and optionally/alternatively the metallize 21 on the bottom of the cap 18, are configured to protect the semiconductor chip (*component*). APPLE-1004, 7:48-60, 11:32-42, 11:56-62; APPLE-1003, ¶¶105-109.

k) Claim 19

[19pre]

The preamble is not limiting, but regardless, Nishiuma renders [19pre] obvious. APPLE-1003, ¶¶126-128. As described above, Nishiuma’s semiconductor integrated circuit device including a semiconductor chip provides an electronic module. *Supra* §IV.A.2.[1pre]; APPLE-1004, 6:66-7:2; APPLE-1003, ¶¶126, 59-60. Nishiuma’s printed wiring board “in which the GND wiring 5a and the power source wiring 5b are formed,” optionally with the GND metallize 5c and/or metallic base 17, provides a second electronic module on which the semiconductor chip is attached. APPLE-1004, 6:66-7:2 (“the semiconductor integrated circuit device ...has a package structure fabricated by sealing semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.”); APPLE-1001, 1:18-23 (’527 patent describing that an electronic module “can be a module like a circuit board, which includes several components [such as] semiconductor

components”); APPLE-1003, ¶¶127-128.



APPLE-1004, FIG. 1 (annotated)

For purposes of the mappings to the elements of claim 19, Nishiuma’s semiconductor integrated circuit device including semiconductor chip (first *electronic module*) mounted on a printed circuit board (second *electronic module*) comprises *a multi-layered electronic module*, and at least the first electronic module includes the features described in the limitations of claim 19. APPLE-1003, ¶128.

[19a]-[19f]

See supra §§IV.A.2.[1a]-[1f-ii]; APPLE-1003, ¶¶129-134, 61-91.

l) Claim 21

As described above, Nishiuma's semiconductor chip is attached to Nishiuma's printed wiring board. *Supra* §§IV.A.2.[1a]-[1f-ii], [19pre]; *see e.g.*, APPLE-1004, 6:66-7:2, 7:10-26, FIG. 1; APPLE-1003, ¶¶135-136, 61-91, 126-128. Accordingly, in this mapping, the semiconductor chip (a first *electronic module*) is *electrically connected* to the printed wiring board (a second *electronic module*) to form Nishiuma's full semiconductor integrated circuit device—that is, *a multilayered functioning totality*. APPLE-1003, ¶¶135-136.

m) Claim 25

[25pre]

See supra §IV.A.2.[19pre]; APPLE-1003, ¶¶137, 126-128.

[25a]

See supra §IV.A.2.[1a]; APPLE-1003, ¶¶138, 61-65.

[25b]

See supra §§IV.A.2.[2a]-[2b], [13b]; APPLE-1003, ¶¶139, 92-98, 117.

[25c]

See supra §§IV.A.2.[1e], [2a]-[2b], [13c]; APPLE-1003, ¶¶140, 82-84, 92-98, 118.

[25d]-[25g]

See supra §§IV.A.2.[1b]-[1d], [1f-i]-[1f-ii]; APPLE-1003, ¶¶141-144, 66-81, 85-91.

n) **Claim 27**

See supra §IV.A.2.[21]; APPLE-1003, ¶¶145, 135-136.

**B. GROUND 1B – Nishiuma-Nakatani Renders Obvious
Claims 7-8 and 17-18**

1. Nakatani Overview (APPLE-1007)

Nakatani describes “a conventional surface acoustic wave device built-in module” which may include multiple devices. APPLE-1007, [0016], [0024], Abstract, [0118], [0123], [0127]; APPLE-1003, ¶146. FIG. 7 shows the conventional device having two surface acoustic wave devices 601 positioned within a concave portion 615. APPLE-1007, [0017], [0019], [0118]-[0119], [0124]-[0135], FIGS. 5, 6A-C.

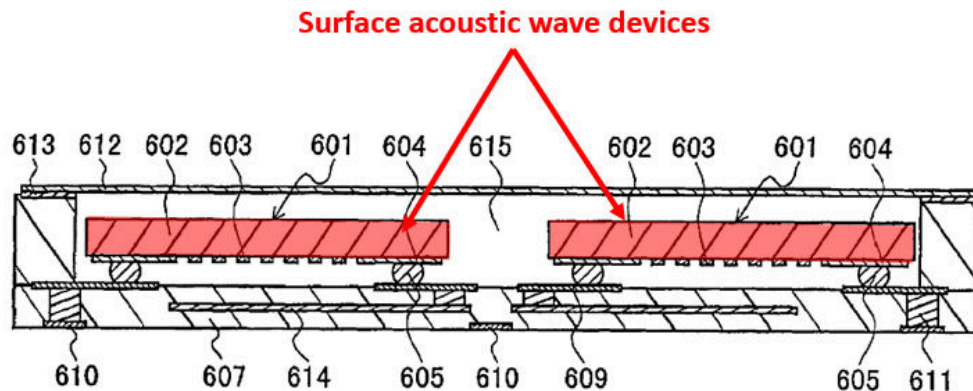


FIG. 7
PRIOR ART

APPLE-1007, FIG. 7

2. Combination of Nishiuma and Nakatani

Nishiuma describes that “semiconductor device components, including the capacitors can be mounted on the surface of the printed wiring substrate.” APPLE-1004, 4:37-40, 9:65-10:3 (“it is also possible to mount chip parts including capacitors on the surface of the printed wiring board...”). Nishiuma thus suggests that multiple components can be connected to the wiring substrate but provides few details in this regard. APPLE-1003, ¶¶147, 56-58. A POSITA would have looked to references like Nakatani to investigate the option of mounting additional IC chips in an installation cavity similar to Nishiuma’s. APPLE-1007, [0018]-[0020], [0118], [0127] FIGS. 5-7; *supra*, §IV.B.1; APPLE-1003, ¶148. It would have been obvious to implement Nishiuma’s device in accordance with Nakatani’s suggestion for mounting multiple IC chips in an installation cavity and electrically connecting the IC chips via a conductive pattern-layer. APPLE-1003, ¶¶149-155. Multiple reasons would have prompted a POSITA to pursue this combination:

First, a POSITA would have been motivated to mount additional IC chips like Nishiuma’s semiconductor chips or Nakatani’s surface acoustic wave (“SAW”) chips in the cavity of Nishiuma’s electronic module to expand the module’s capabilities and overall processing power. APPLE-1003, ¶150.

Second, a POSITA would have been motivated to mount additional chips in the cavity of Nishiuma’s electronic module because the “demand for higher

performance and miniaturization of electronic equipment” increased the desire for “higher density and higher function[ing]” semiconductor packages. APPLE-1007, [0002]-[0003], [0027], [0075]; APPLE-1003, ¶151. Nakatani describes that the semiconductor package’s thickness is improved and the package is more compact by having multiple thin chips mounted on a substrate. APPLE-1007, [0001], [0024]-[0025], [0027].

Third, providing additional IC chips in Nishiuma’s cavity would have been obvious as a predictable application of a known technique of implementing multiple components in a module as taught by Nakatani to a known system as taught by Nishiuma to achieve entirely predictable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious); APPLE-1003, ¶¶152, 22-34.

Fourth, the combination would have been obvious as the mere duplication of parts without new or unexpected results. *In re Harza*, 274 F.2d 669, 774 (CCPA 1960) (“mere duplication of parts has no patentable significance unless a new and unexpected result is produced.”); *see also Low Temp Indus., Inc. v. Duke Mfg. Co.*, No. 2021-2137, 2021 WL 6124455, at *5-6 (Fed. Cir. 2021); APPLE-1003, ¶153. Implementing a plurality of Nishiuma’s components would have been a predictable design choice to increase an ultra-thin semiconductor module’s capability, and

would have been well within the skill of the POSITA as shown by Nakatani.

APPLE-1003, ¶¶153-154.

A POSITA would have reasonably expected success implementing the combination for the reasons described above, especially given that Nakatani describes coupling electronic components in a similar cavity and using a similar technique as described by Nishiuma. APPLE-1004, 2:60-67, 8:16-9:21; Figs. 1, 39; APPLE-1007, [0016]-[0023], [0118]-[0126], FIGS. 5-7; APPLE-1003, ¶¶147-155.

3. Analysis

a) Claim 7

Nishiuma-Nakatani renders obvious claim [7]. APPLE-1003, ¶¶156-157. For example, in the combination, Nishiuma's device predictably includes at least two IC chips as Nakatani suggests. *Id.* Nishiuma's techniques for mounting a single semiconductor chip in the cavity is therefore predictably extended to each of the multiple IC chips (*plurality of components*), each chip including electrode pads (*flat contact zones*) electrically connected to Au lands (*first solid contact bumps*) on the printed wiring substrate (*first conductive-pattern layer*) by Au balls 12 (*second solid contact bumps*) so that each chip realizes the benefits of the connections described for a single chip in Nishiuma. *Supra* §IV.B.2 (Nishiuma-Nakatani Combination); APPLE-1004, 2:60-67, 8:16-9:21, 4:37-40, 9:65-10:3,

Figs. 1, 39; APPLE-1007, [00026] (“at least two electric elements (203) such as semiconductor chips or surface acoustic wave devices... mounted on wiring patterns”), [0127] (“a plurality of the surface acoustic wave devices 501 ... may be mounted together”), [0016]-[0023], FIGS. 4-7; APPLE-1003, ¶157.

b) Claim 8

Nishiuma-Nakatani renders obvious claim [8]. APPLE-1003, ¶¶158-161. For example, in the combination, Nishiuma’s device predictably includes at least two IC chips, as Nakatani suggests, which are each connected to the printed wiring substrate and thus electrically connected to each other by means of the surface wiring. *Supra* §IV.B.2 (Nishiuma-Nakatani Combination); APPLE-1004, 1:11-17, 2:36-50, 4:37-40, 7:38-47, 9:13-25; Figs. 1, 39; APPLE-1007, [0019] (“A plurality of surface acoustic wave device 601 built into the module shown in FIG. 7 and the external circuit are connected via [first and second wiring patterns, internal circuit and via holes]”), [0020] (“After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected”), [0028], [0127], FIGS. 4-7; APPLE-1003, ¶¶158-159. A POSITA also would have found that provision of an electrical connection between a pair of IC chips to be an obvious design choice that would be readily achieved using the conventional wiring patterns and interconnection techniques described in each of Nakatani and Nishiuma. APPLE-1003, ¶161

APPLE-1004, 7:16-26. For example, a POSITA would have electrically connected the IC chips in the combination to facilitate communication of data signals between the chips. APPLE-1003, ¶¶160-161.

c) Claim 17

See supra §IV.B.3 (Ground 1B Claims [7]); APPLE-1003, ¶¶162, 156-157.

d) Claim 18

See supra §§IV.A.2, IV.B.3 (Ground 1A Claim [4], Ground 1B Claim [8]); APPLE-1003, ¶¶163, 99-100, 158-161. For the same reasons described above in Ground 1A, in the Nishiuma-Nakatani combination at least one of the plurality of components is a microcircuit, and further as described with respect to claim 8, the components in the combination are electrically connected to each other by means of the first conductive-pattern layer. *Id.*

C. GROUND 1C – Nishiuma-Nakatani-Yoneyama Renders Obvious Claims 20 and 26

1. Combination of Nishiuma, Nakatani and Yoneyama

Nishiuma describes a multi-layered electronic module including a printed wiring board “in which the GND wiring 5a and the power source wiring 5b are formed,” optionally with the GND metallize 5c and/or metallic base 17 (one “electronic module”) on which a semiconductor chip (another “electronic module”) is attached. *Supra* §IV.A.2.[19pre]; APPLE-1004, 6:66-7:2, FIGS. 1, 9-10, 18; APPLE-1003, ¶¶164, 56-58. Nishiuma describes an integrated circuit device but is

not specific about the device's function. APPLE-1004, title ("Semiconductor integrated circuit device..."), 6:66-7:6, 8:10-12. A POSITA would have looked to references like Yoneyama (*see infra* §IV.E.1) to investigate potential functions of integrated circuit devices, including memory circuits. APPLE-1013, [0018]; APPLE-1003, ¶¶165, 185-188. It would have been obvious to implement Nishiuma-Nakatani's device in accordance with Yoneyama's suggestion to implement multiple integrated circuit devices as memory circuits and multiple reasons would have prompted a POSITA to pursue this combination:

First, it would have been obvious to a POSITA to implement Nishiuma-Nakatani's integrated circuits as memory circuits, as Yoneyama teaches, because a memory circuit is one of a limited number of broad classes of functions of the integrated circuit. APPLE-1003, ¶166.

Second, a POSITA would have understood that Nishiuma's flip-chip bonding techniques would have provided high-connection density and improved electrical performance to a memory circuit and would have found it obvious to implement Nishiuma-Nakatani's integrated circuits as memory circuits for this reason. APPLE-1003, ¶167.

Third, implementing integrated circuits as multiple memory circuits as Yoneyama teaches would have been obvious as a predictable application of a known technique of implementing memory circuits to a known system as taught by

Nishiuma-Nakatani to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶168. Indeed, semiconductor chips like Nishiuma's commonly included multiple memory circuits (e.g., registers, cache, RAM) to facilitate efficient data retrieval and processing before the Critical Date. *Id.*; *see also* APPLE-1044, 1.

A POSITA would have reasonably expected success implementing the combination for all of the reasons described above. APPLE-1003, ¶¶164-169.

2. Analysis

e) Claim 20

Nishiuma-Nakatani-Yoneyama renders claim [20] obvious. APPLE-1003, ¶¶170-171. For example, multiple integrated circuits, as taught by Nishiuma and Nakatani, are implemented as memory modules, as suggested by Yoneyama.

Supra §IV.C.1; APPLE-1013, [0018]; APPLE-1003, ¶¶170, 164-169.

Accordingly, Nishiuma-Nakatani-Yoneyama renders obvious a multi-layered electronic module comprising a plurality of memory circuits. APPLE-1003, ¶171.

f) Claim 26

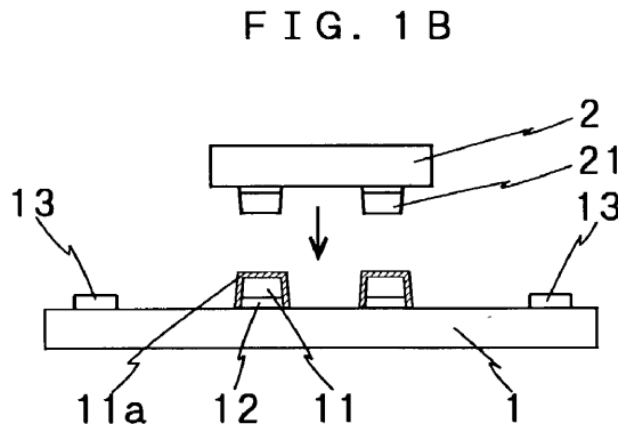
See supra §IV.C.2.[20]; APPLE-1003, ¶¶170-172.

D. GROUND 1D – Nishiuma-Shibata Renders Obvious Claims 3 and 14

1. Shibata Overview (APPLE-1005)

Shibata describes a method for coupling semiconductor chips using bump

electrodes that use metals with relatively low melting points to alloy one metal with another inside the bump to prevent adverse effects from high temperature on the semiconductor elements. APPLE-1005, [0011], APPLE-1003, ¶¶173-174.



APPLE-1005, FIG. 1B

Shibata describes that the first and second bump electrodes 11 and 21 can be joined by “a third metal layer having a lower melting point,” such as gold or tin, which “melts at a relatively low temperature and diffuses into the bump electrode or the electrode terminal to thereby provide diffusive joining.” *Id.*, [0014], [0032], [0053], [0082].

2. Combination of Nishiuma and Shibata

Nishiuma describes techniques for solderlessly bonding electrodes of a semiconductor chip to a printed wiring board using Au balls. APPLE-1004, 7:43-47, 9:13-22, FIG. 1. A POSITA would have understood that connections between

components and substrates may be improved by addition of other metals to promote joining or absorb thermal stresses between the component and substrate and would have looked to similar references like Shibata for details about how to implement additional metal layers. APPLE-1003, ¶¶173-175; APPLE-1005, [0060], [0014], [0022], [0084]. Shibata describes using layers of low-melting point metals between the contact bumps to improve connection between bumps. APPLE-1005, [0053], [0011]-[0014], [0032], [0074]. A POSITA would have been motivated to implement Nishiuma's semiconductor device with Shibata's teachings to join gold contact bumps using a low melting temperature material layer to improve diffusive joining between bumps. APPLE-1005, [0014], [0022], [0084], [0074]; APPLE-1003, ¶176.

In the Nishiuma-Shibata combination, a semiconductor integrated circuit device, per Nishiuma, is implemented with an additional metal layer on at least one contact bump, as Shibata teaches. APPLE-1004, 8:10-9:16, FIG. 1; APPLE-1005, [0053], [0011]-[0014], [0032]; APPLE-1003, ¶¶175-177. Multiple reasons would have prompted a POSITA to pursue this combination:

First, a POSITA would have understood that addition of a metal layer between the contact bumps, as taught by Shibata, improves connection between the bumps by improving diffusive joining of the component to the surface wiring through the bumps and by absorbing thermal stresses. APPLE-1005, [0014],

[0022], [0060], [0074], [0084]; APPLE-1004, 10:57-11:18; APPLE-1003, ¶178.

Second, a POSITA would have understood that Shibata's method of using an additional metal layer between gold balls would be complementary to Nishiuma's method for accommodating height differences between gold balls. APPLE-1004, 10:57-11:12, 13:5-10, FIG. 9; APPLE-1003, ¶179.

Third, implementing an additional metal layer on at least one contact bump would have been obvious as a predictable application of a known technique of using additional metals to improve the connection between contact bumps as taught by Shibata to a known system as taught by Nishiuma to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶180.

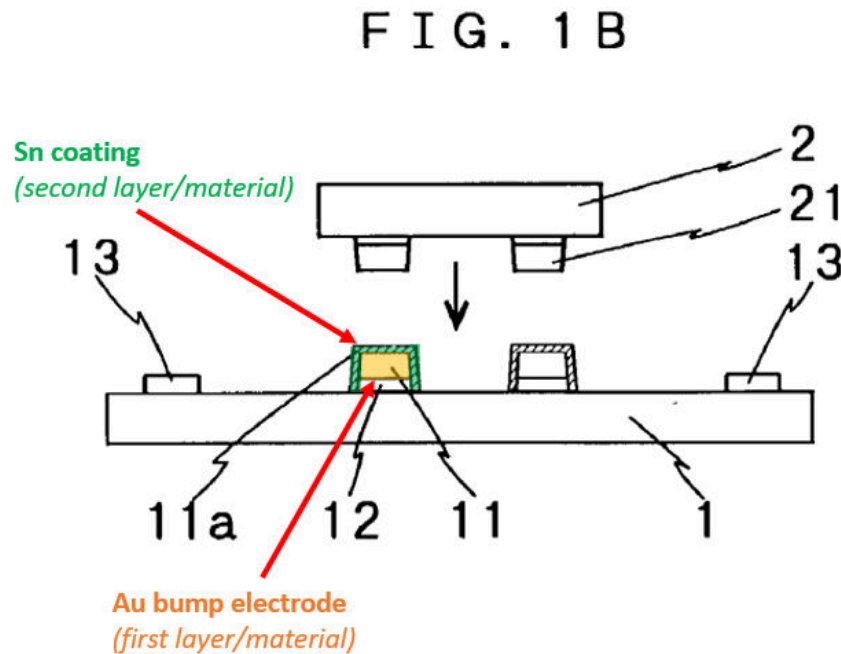
The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for the reasons described above and given that Nakatani describes coupling electronic components using a similar technique as Shibata. APPLE-1004, 2:60-67, 8:16-9:21, 17:14-17; Figs. 1, 39; APPLE-1005, [0051]-[0052], FIG. 1B; APPLE-1003, ¶¶175-181.

3. Analysis

a) Claim 3

Nishiuma-Shibata renders obvious claim [3]. APPLE-1003, ¶¶182-183, 175-181. For example, as shown in FIG. 1B, a layer of low melting temperature

metal, such as tin is layered over at least one of the gold bumps of Nishiuma to improve bonding between the gold bumps. *Supra* §IV.D.2 (Nishiuma-Shibata Combination); APPLE-1005, [0032], [0053], [0074].



APPLE-1005, FIG. 1B (annotated)

Accordingly, in the combination, Nishiuma's Au ball 13 / Au land 14 is coated with a layer of low melting temperature metal, such as tin, according to Shibata's teaching, and thus the first contact bumps include a layered structure containing at least two layers of at least two different materials. APPLE-1003, ¶¶182-183.

b) Claim 14

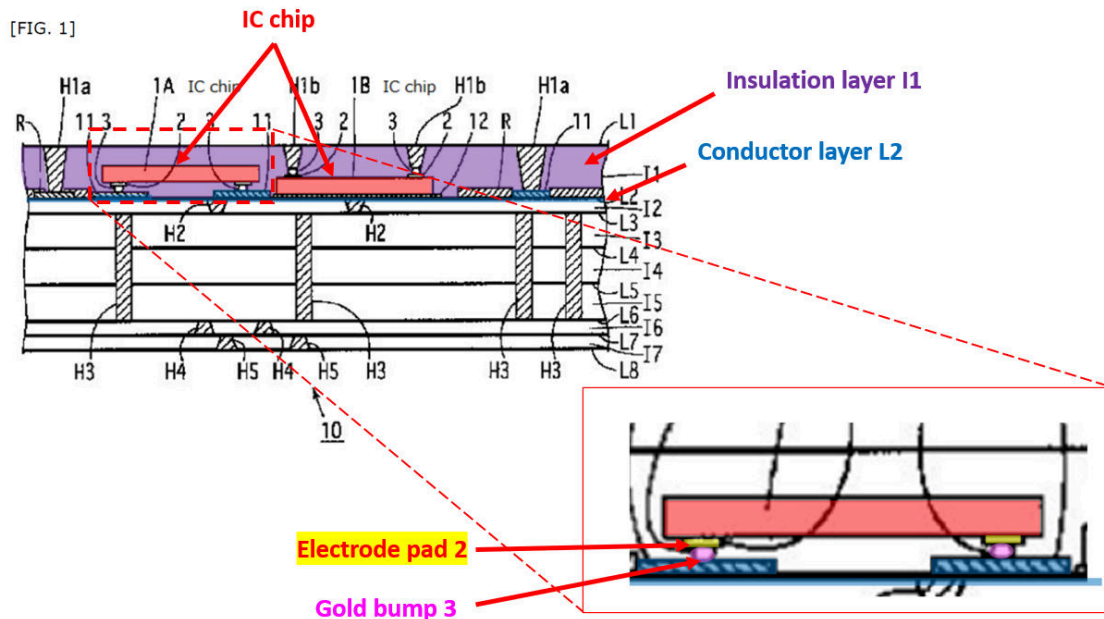
See supra §IV.C.2 (Ground 1C, Claim [3]); APPLE-1003, ¶¶182-184.

E. GROUND 2 – Yoneyama-Onda Renders Obvious Claims 1-27

1. Yoneyama Overview (APPLE-1013)

Yoneyama describes “a circuit board ... in which electronic components such as a semiconductor integrated circuit chip with active surfaces on which a plurality of external connection electrodes have been formed[] ... are mounted inside.” APPLE-1013, [0001]; APPLE-1003, ¶¶185-188.

As illustrated in FIG. 1, Yoneyama describes that the “circuit board has eight conductor layers L1-L8 on which circuit patterns have been formed, and each conductor layer is finished with an electric insulation layer I1-I7.” APPLE-1013, [0011], [0013]-[0015], [0017], [0042], FIGS. 1-2, 5-6. Two or more components such as IC chips in this embodiment are, respectively, “mounted face-down and face-up on a single wiring board” such that the active surfaces of the components face in opposite directions. *Id.*, [0027], [0030], FIG. 1.



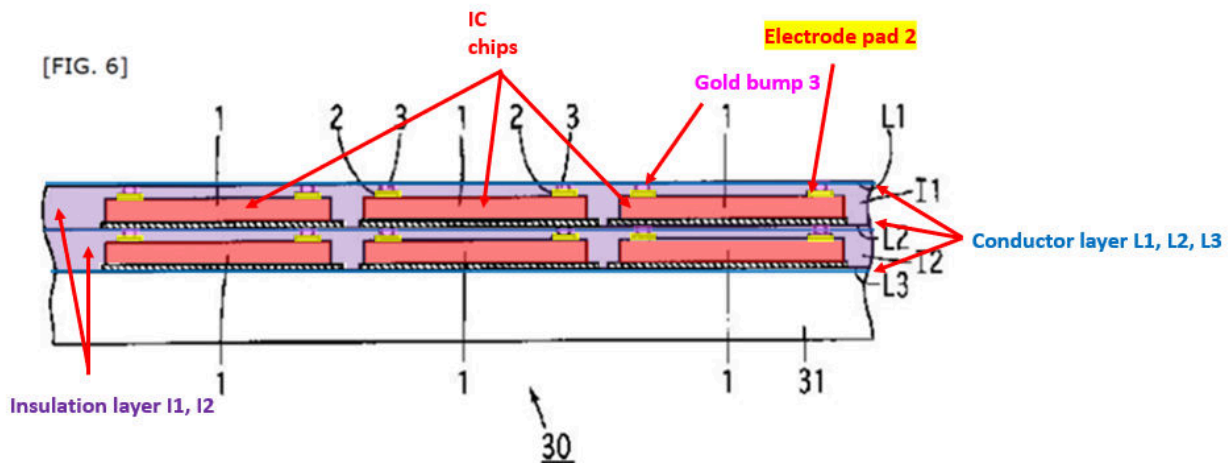
APPLE-1013, FIG. 1 (annotated)

Yoneyama's FIG. 1 shows a circuit board 10 in which "IC chips 1A and 1B are embedded in a multilayer substrate ... and solder bumps or gold bumps 2 are formed on multiple electrode pads on their active surfaces." *Id.*, [0033]⁴. "IC chip 1A is mounted on pad 11 of the circuit pattern formed on the surface of conductor layer L2 in the face-down state described above...[i]n other words, IC chip 1A is mounted by flip-chip bonding by way of bumps 2 to a pad 11." *Id.*, [0034].

Yoneyama describes with respect to FIG. 6, a "multilayer mounting

⁴ Although there is some discrepancy in Yoneyama's reference numbers, the Reference Numbers section (APPLE-1013, 14) clarifies "electrode pad 2" and "bump 3," consistent with the figures.

structure” in which IC chips are mounted in successively stacked modules. Such a multilayer structure can use “a circuit board 20 in which IC chips 1 are embedded inside while face-down” or “use a circuit board 30 in which IC chips 1 are flip-chip bonded while face-up.” APPLE-1013, [0016], FIG. 6; *see also id.*, [0010]-[0018], FIG. 5; APPLE-1003, ¶188.

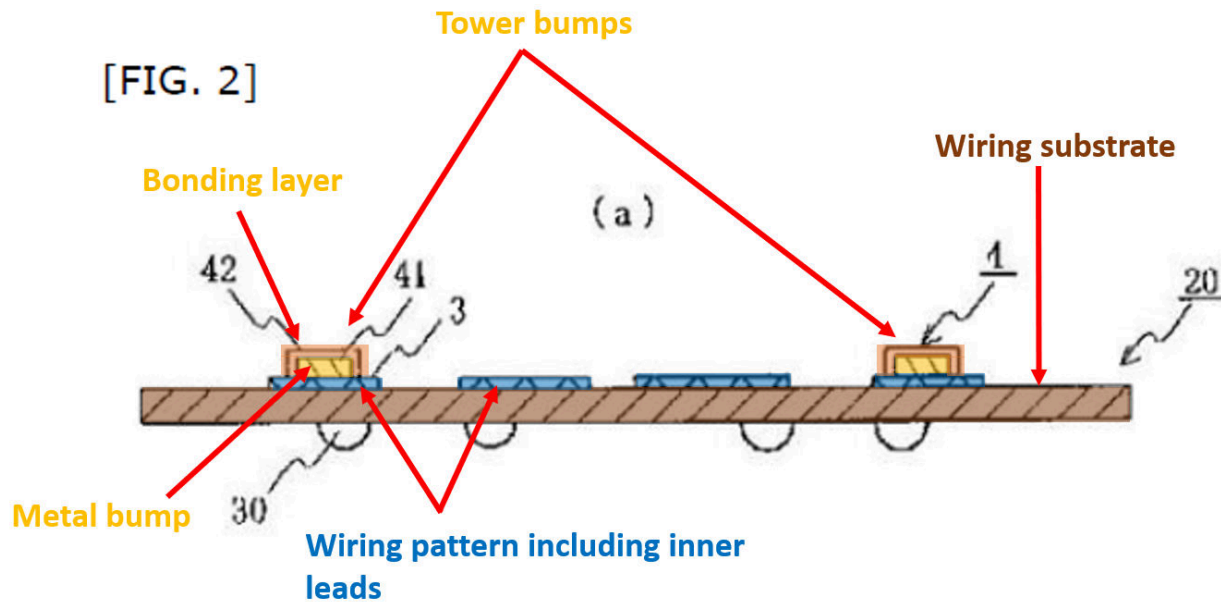


APPLE-1013, FIG. 6 (annotated)

2. Onda Overview (APPLE-1008)

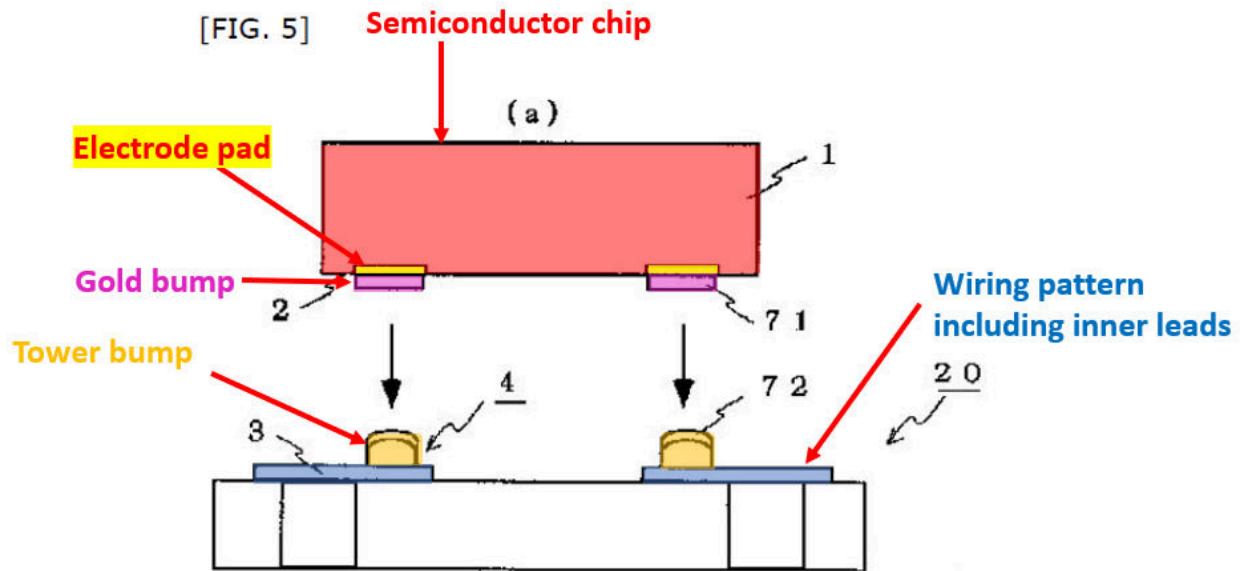
Onda describes techniques for connecting a wiring substrate to a semiconductor chip in which “tower bumps 4 are formed on the connecting portions [of the wiring pattern] to connect with the semiconductor chip.” APPLE-1008, [0045], [0039]-[0042], [0070], FIGS. 1-10; APPLE-1003, ¶¶189-190. “The tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to [] electrode pads 2 of the semiconductor chip 1.” APPLE-1008, [0045],

[0056], [0063], [0073]-[0075], [0078], [0101].



APPLE-1008, FIG. 2

For example, in Figure 5(a), Onda illustrates the process of mounting a “semiconductor chip 1 on the manufactured wiring substrate 20.” *Id.*, [0067]-[0070]. “[A]fter preparing the wiring substrate 20... and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed” to the wiring layer using heat and pressure. *Id.*, [0068]; *see also* [0069]-[0083], [0092]-[0098], Figs. 6(a), 8(a), 9(a) (showing similar methods).



APPLE-1008, FIG. 5

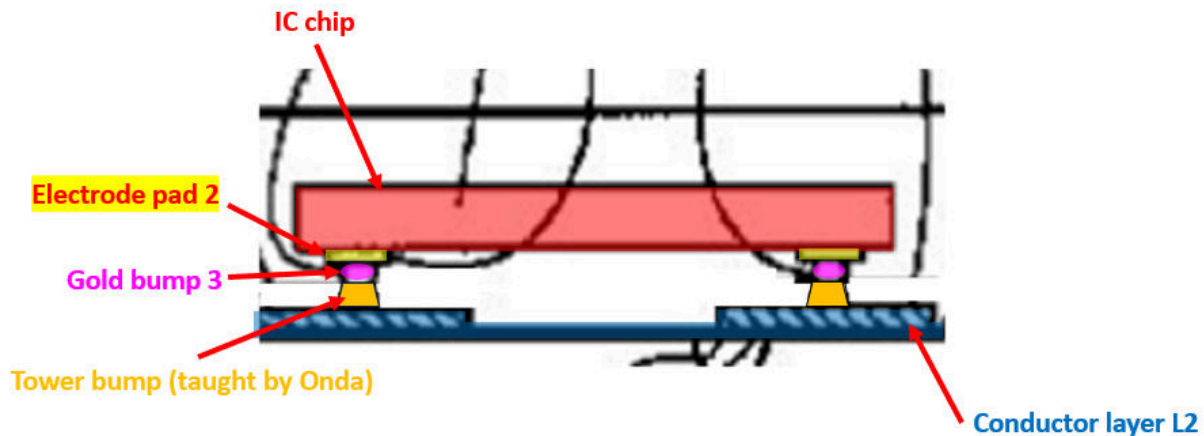
3. Combination of Yoneyama and Onda

Yoneyama describes that to connect an IC chip to the conductor layer, “IC chip 1A is mounted on pad 11 of the circuit pattern formed on the surface of conductor layer L2 in the face-down state described above...[i]n other words, IC chip 1A is mounted by flip-chip bonding by way of bumps 2 to pad 11.” APPLE-1013, [0034], [0012]. However, Yoneyama does not limit the described connection between the IC chip and the circuit pattern to this arrangement, and a POSITA would have been aware of other conventional connection schemes having known benefits that would also be suitable for electrically connecting the bumps to the pads of the circuit pattern on the conductor layer. APPLE-1003, ¶191.

Recognizing that devices commonly are connected to circuit board wiring

patterns by conductive contact bumps formed on the device electrode pads and wiring, a POSITA would have turned to references like Onda to investigate the implementation of pairs of conductive bumps for electrically connecting Yoneyama's IC chip to the circuit pattern. APPLE-1003, ¶¶192, 189-190. Like Yoneyama, Onda describes techniques for coupling a device's electrode pads to circuit board wiring, although Onda makes the electrical connection using conductive bumps formed on the wiring substrate and on the device electrode pads. APPLE-1008, [0039], [0045]-[0046], [0072]-[0074], [0085]-[0086], [0093]-[0094], [0100]-[0101], [0107]-[0108], [0114]-[0115] FIGS. 5-9; APPLE-1003, ¶¶193, 185-190. For example, Onda describes forming a tower bump on the PCB wiring pattern to provide an electrical connection to the semiconductor device and buffer thermal stresses. *See* APPLE-1008, [0046]; APPLE-1003, ¶¶193-194. Onda describes that two conductive bumps can couple a device to a wiring substrate: "gold plating (gold bumps) 71 are formed on each electrode pad 2 [of the device and the] wiring layer of the substrate including inner leads 3 is provided with tower bumps 4 consisting of copper bumps 4 consisting of copper bumps

(metal bumps 41).”⁵ APPLE-1008, [0073].



APPLE-1013, FIG. 1 (excerpted/annotated, modified to include Onda’s teaching to use two conductive bumps to electrically couple the chip to the wiring pattern); APPLE-1003, ¶¶194-195.

It would have been obvious to a POSITA to implement the combination of tower bumps and electrode bumps as taught by Onda into Yoneyama’s device in place of the single metal bump described by Yoneyama for a number of reasons:

First, a POSITA would have understood that using electrode bumps on the device and tower bumps on the circuit pattern to electrically connect the device to

⁵ Integration of Onda’s technique for forming contact bumps on the substrate and device eliminates any need for adhesives or anisotropic conductive film in the Yoneyama-Onda combination. APPLE-1013, [0034]; APPLE-1003, ¶194.

the printed circuit board would improve the ease of making the electrical connection between the device and circuit board. APPLE-1003, ¶196.

Second, a POSITA would have understood that the addition of a metal tower bump to electrically connect an IC chip to circuit wiring of a conductor layer would improve the device's resistance to thermal stresses. APPLE-1003, ¶¶197-198; APPLE-1008, [0012], [0015], [0041], [0046]. For example, Onda describes that providing a tower bump on the circuit board for connection to the bumps on the semiconductor chip may "prevent[] cracking of semiconductor chips due to thermal stress." APPLE-1008, [0010]; *see also id.*, [0008]-[0012], [0070]; APPLE-1011, [0004] (reliability concerns arise from "a mismatch between the coefficients of thermal expansion between the semiconductor chip and the substrate."), [0014] (describing thermal mismatch between a substrate and chip carrier); APPLE-1003, ¶198.

Third, a POSITA would have understood that providing conductive bumps to electrically connect the device and circuit board would allow for the selection of materials that increase connection strength between the device and circuit board. APPLE-1008, [0076]; APPLE-1003, ¶199.

Fourth, implementing a circuit board embedded with IC chips electrically coupled to the circuit board by conductive bumps formed on the wiring and device electrodes would have been obvious as a predictable application of a known

technique for coupling devices to a printed circuit board as taught by Onda to a known system as taught by Yoneyama to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶200.

The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all of the reasons above and given the similarities between the connection methods described by Yoneyama and the techniques suggested by Onda. APPLE-1013, [0012]-[0016], [0033]-[0034], Figs. 1, 6; APPLE-1008; [0068]-[0083], [0092]-[0098]; APPLE-1003, ¶¶191-201.

4. Analysis

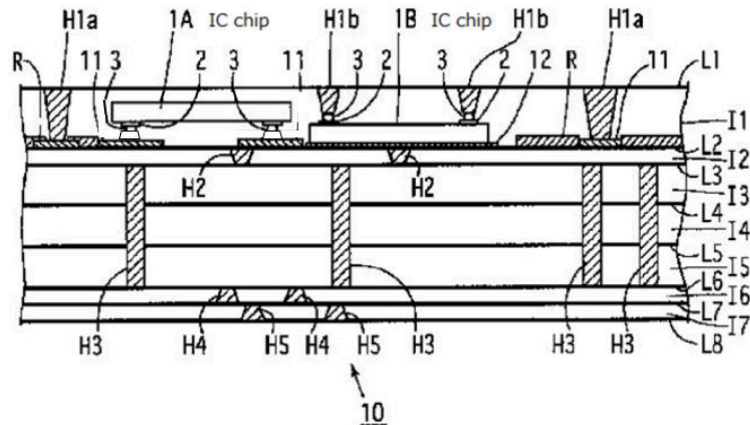
a) Claim 1

[1pre]

To the extent the preamble is limiting, Yoneyama-Onda renders [1pre] obvious. APPLE-1003, ¶¶202-204. Yoneyama describes “a circuit board with embedded electronic components” such as IC chips that constitutes an “*electronic module*” as claimed. APPLE-1013, [0058], [0001], [0020], [0025], [0031]-[0034]; *cf.* APPLE-1001, 1:18-23 (’527 patent describing that an electronic module “can be a module like a circuit board, which includes several components [such as] semiconductor components”).

Circuit board with
embedded electronic
components
(electronic module)

[FIG. 1]

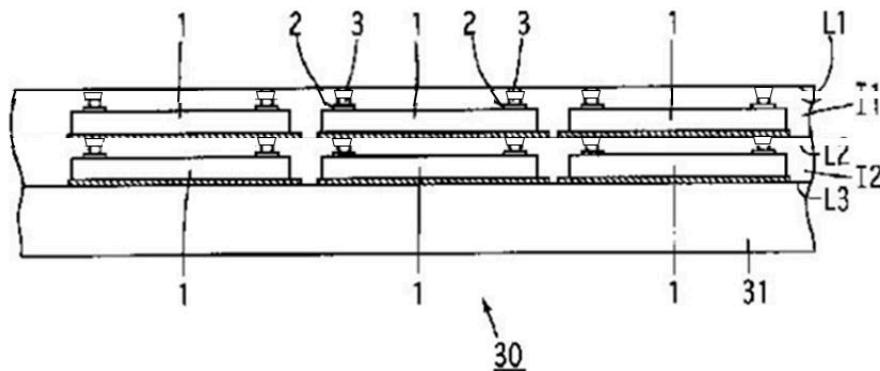


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps)

FIG. 6, reproduced below, depicts another configuration of Yoneyama's also provides an electronic module. APPLE-1013, [0016]-[0017]; APPLE-1003, ¶¶203-204.

Circuit board with
embedded electronic
components
(electronic module)

[FIG. 6]



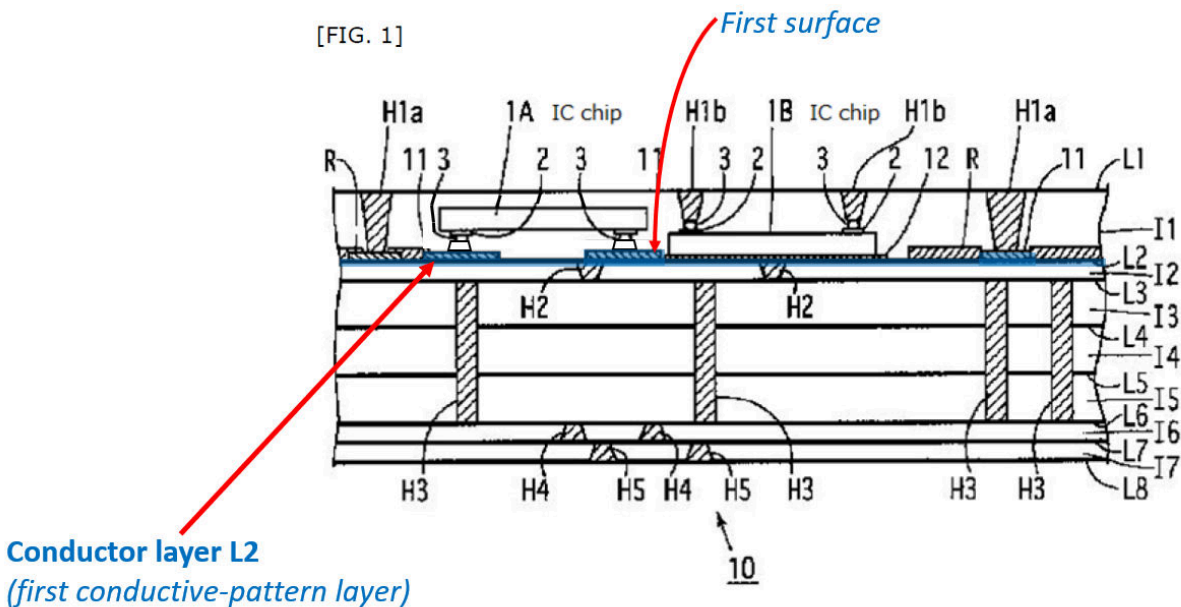
APPLE-1013, FIG. 6 (annotated, modified to include tower bumps)

As shown below in [19pre], each iterative portion of the multi-layer stack shown in FIG. 6 also discloses and renders obvious a respective “*electronic module*” consistent with the description of such modules in the ’527 patent. *Infra*, [19pre]; *cf.*, APPLE-1001, 1:18-23; APPLE-1003, ¶¶204, 287-288.

[1a]

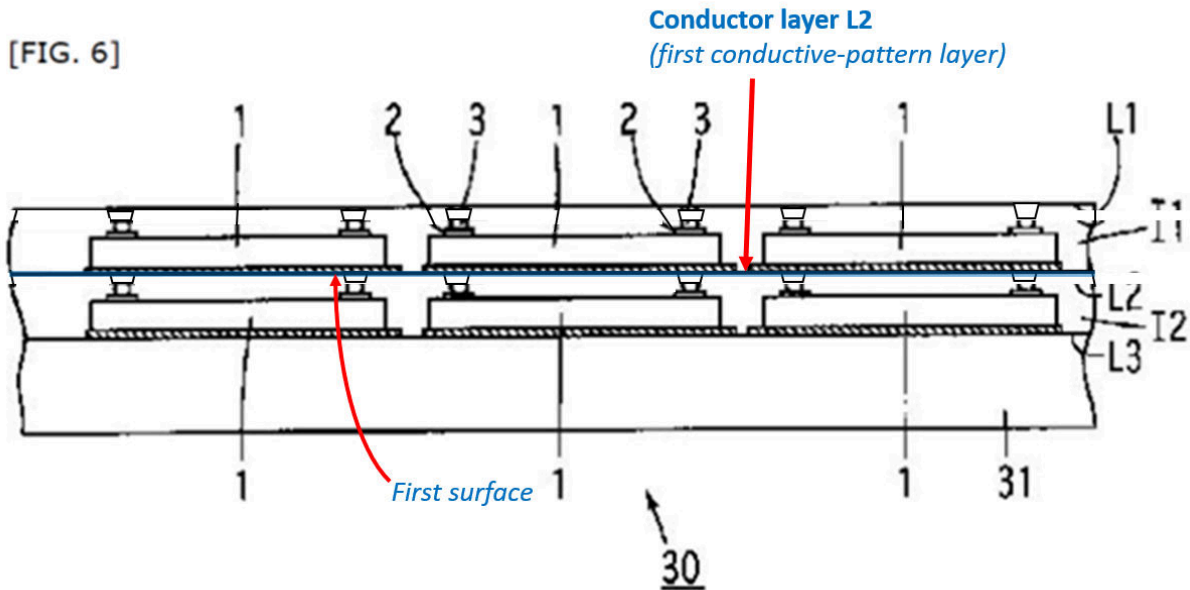
Yoneyama-Onda renders [1a] obvious. APPLE-1003, ¶¶205-207. For example, Yoneyama describes that “[e]ach conductor layer L1-L8 has the required circuit pattern” and that circuit patterns can include electrode pads 11. APPLE-1013, [0015], [0034]-[0037], [0042], [0051], [0011]-[0012]. Yoneyama’s conductor layer L2 including pads 11, which provide an electrically conductive path to electrode pads of the IC chip, are patterned to match the arrangement of the

electrode pads on the IC chip, provides a “*first conductive-pattern layer with a first surface*” as claimed. *Id.*, [0015], [0036]; *cf.*, APPLE-1001, 6:50-57; APPLE-1105; APPLE-1003, ¶¶205-206.



APPLE-1013, FIG. 1 (annotated, modified to include tower bumps)

Yoneyama’s FIG. 6 configuration also provides “*first conductive-pattern layer with a first surface*” as claimed. APPLE-1003, ¶207.

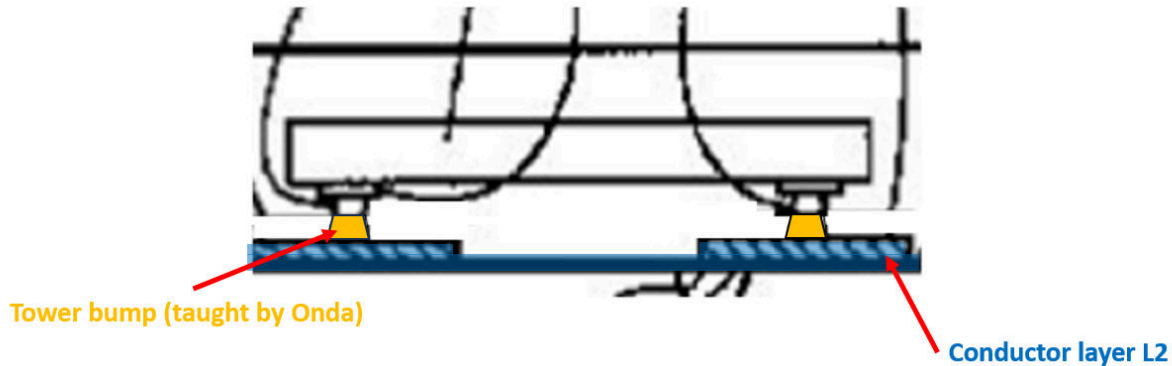


APPLE-1013, FIG. 6 (annotated, modified to include tower bumps)

[1b]

Yoneyama-Onda renders [1b] obvious. APPLE-1003, ¶¶208-214. For example, Yoneyama describes that an IC chip is mounted to pads of a conductive layer using gold bumps. APPLE-1013, [0034]; APPLE-1003, ¶208. To the extent that Yoneyama does not expressly disclose electrically connecting the IC chip to the conductor layer via gold bumps and contact bumps formed on the pads of the conductor layer, Onda teaches this conventional solution for bonding a component to a circuit board. APPLE-1008, [0039], [0044]-[0045], FIGS. 5-10; APPLE-1003, ¶208. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Yoneyama's IC chip bonded to the conductive layer pad using two conductive bumps, including a tower

bump (*first contact bumps*) formed on the pad of the conductive layer (*first surface of the first conductive pattern layer*) as suggested by Onda. *Supra* §IV.E.3 (Yoneyama-Onda Combination); APPLE-1003, ¶¶209, 191-201.

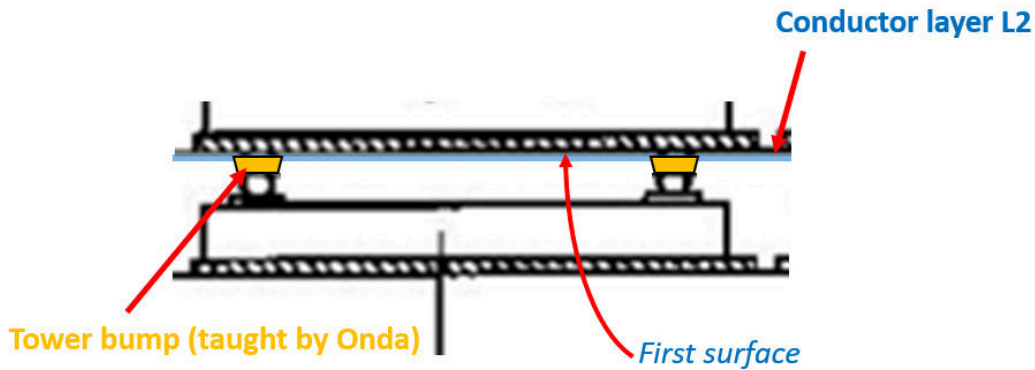


APPLE-1013, FIG. 1 (excerpted and annotated, modified to include tower bumps)

Onda describes that in a “post-bumping method,” “metal bumps 41 are formed on the wiring pattern including inner leads 3 by metal plating (electroless or electroplating).” APPLE-1008, [0062]. Onda’s metal plating process is thus a *solderless* process for making the tower bumps on the conductive layer. APPLE-1003, ¶¶210-211. Onda describes that “tower bumps 4 should be made of a conductive material that does not undergo a phase transformation at high temperatures,” and a POSITA would have understood that the tower bumps, being formed of conductive materials, are *metallurgically and electrically connected* to Yoneyama’s conductive layer to couple the IC chip to the conductive layer.

APPLE-1008, [0099] (“electrical connection between a semiconductor device and a wiring substrate using gold-gold bonding will be described”), [0014], [0039], [0042], [0045], [0057], [0101]-[0106]; APPLE-1003, ¶¶212, 35-38. Accordingly, a POSITA would have understood that tower bumps formed on the circuit wiring provide the “*first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto*” as claimed. APPLE-1003, ¶¶208-212.

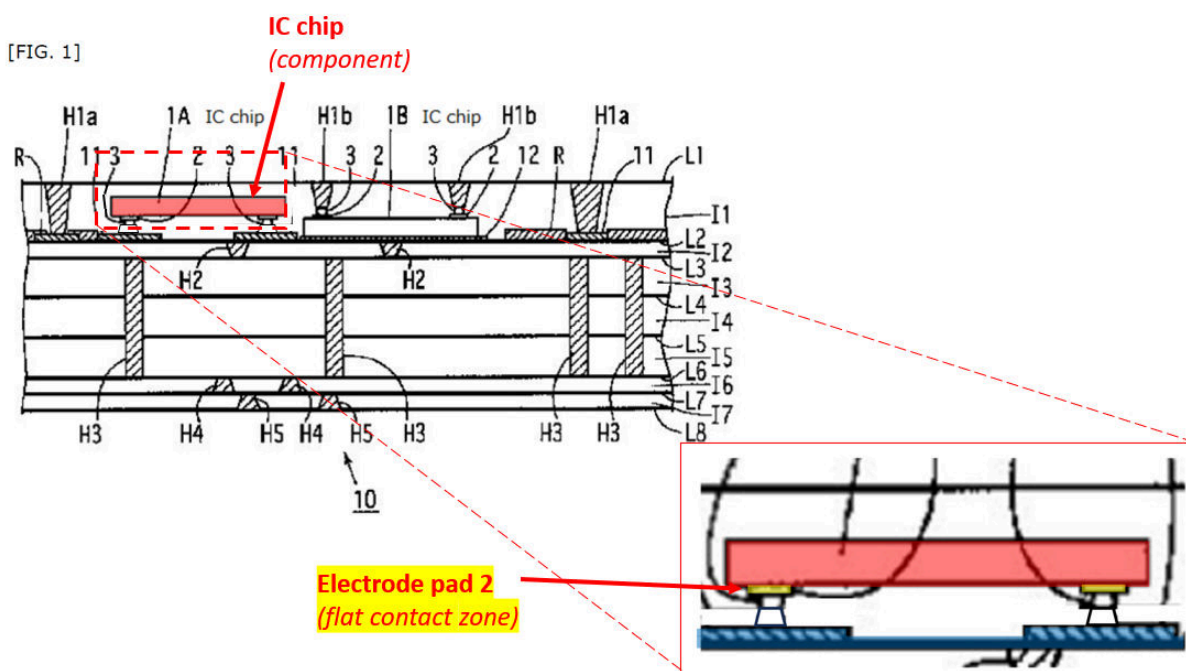
Yoneyama’s FIG. 6 configuration likewise provides “*first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto.*” APPLE-1003, ¶¶213-214. Yoneyama’s FIG. 6 shows “a plurality of IC chips 1 are mounted face-up by flip chip bonded[ing]...on conductor layer L3” and are bonded to “conductor layer L2 on which a wiring pattern has been formed.” APPLE-1013, [0017], FIG. 6. Although modified FIG. 6 shows tower bumps (*first solid contact bumps*) positioned below the L2 conductor layer, Yoneyama describes that the wiring pattern is formed on the conductor layer prior to bonding to the component, and thus a POSITA would have understood that in the combination, the tower bumps would also be formed *on the first surface of the first conductive-pattern layer* prior to bonding a component. APPLE-1003, ¶214.



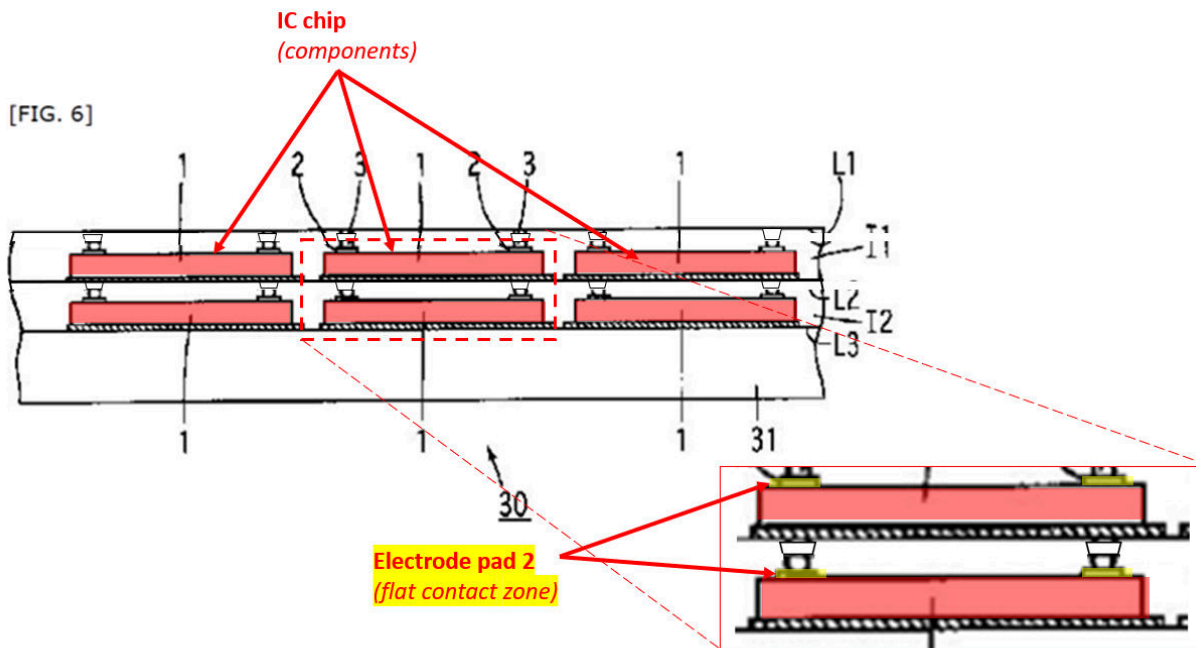
APPLE-1013, FIG. 6 (excerpted and annotated, modified to include tower bumps)

[1c]

Yoneyama-Onda renders [1c] obvious. APPLE-1003, ¶¶215-218. For example, Yoneyama describes that “IC chips 1A and 1B are bare chips [having] multiple electrode pads on their active surfaces.” APPLE-1013, [0033], [0006], [0008]; APPLE-1003, ¶¶215.



APPLE-1013, FIG. 1 (annotated, modified to include excerpt and tower
bumps)



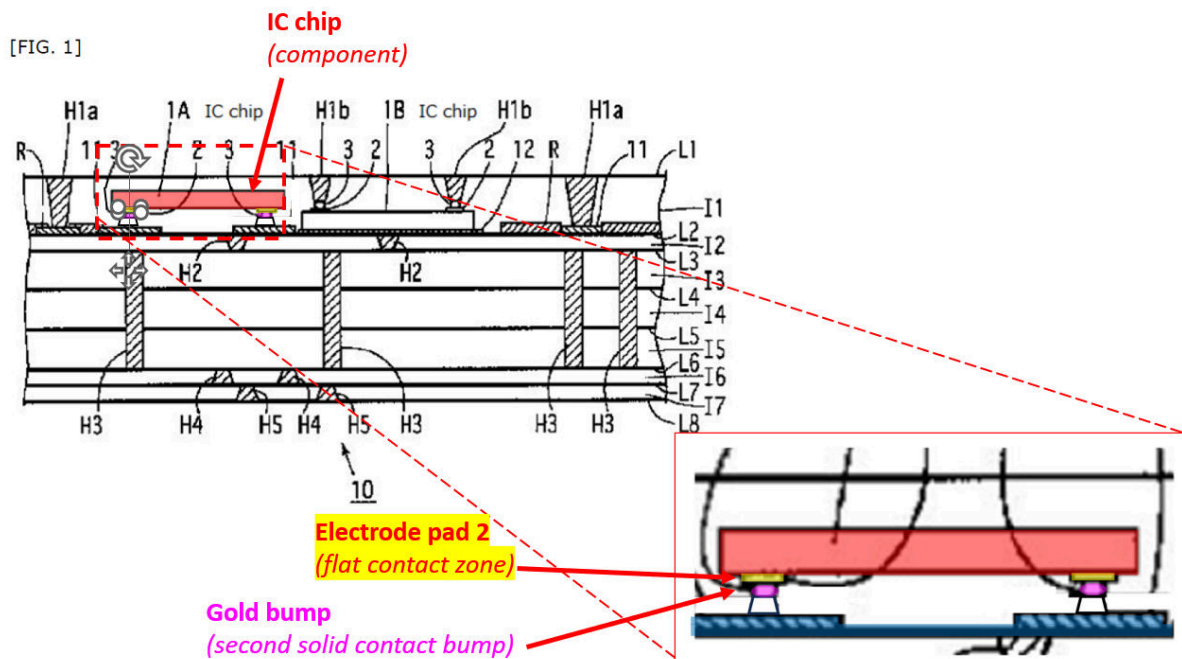
APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps)

As shown above, the electrode pads 2 in Yoneyama's chips have a flat contact surface and a POSITA would have understood the electrode pads 2 to be "*flat contact zones*" as claimed. APPLE-1003, ¶¶215-218, 220. To the extent Patent Owner argues that the claims further require the flat contact zones to be non-protruding (which is not required, *see supra*, Ground 1A, [1c]), Onda discloses non-protruding pads that would have been obvious to apply in the combination to reduce the thickness of the device and because the option of non-protruding pads would have been an obvious design choice before the Critical Date, especially considering that only two options exist (protruding or not). APPLE-1008, [0037]-

[0038], FIGS. 1, 5-10; APPLE-1013, [0006]; APPLE-1003, ¶219.

[1d]

Yoneyama-Onda renders [1d] obvious. APPLE-1003, ¶¶221-225. For example, Yoneyama describes that “gold bumps... are formed on multiple electrode pads” of the IC chips. APPLE-1013, [0033], [0036]. Yoneyama’s gold bumps formed on electrode pads of the semiconductor chip provide the “*second solid contact bumps made on the flat contact zones*” as claimed. APPLE-1003, ¶221.

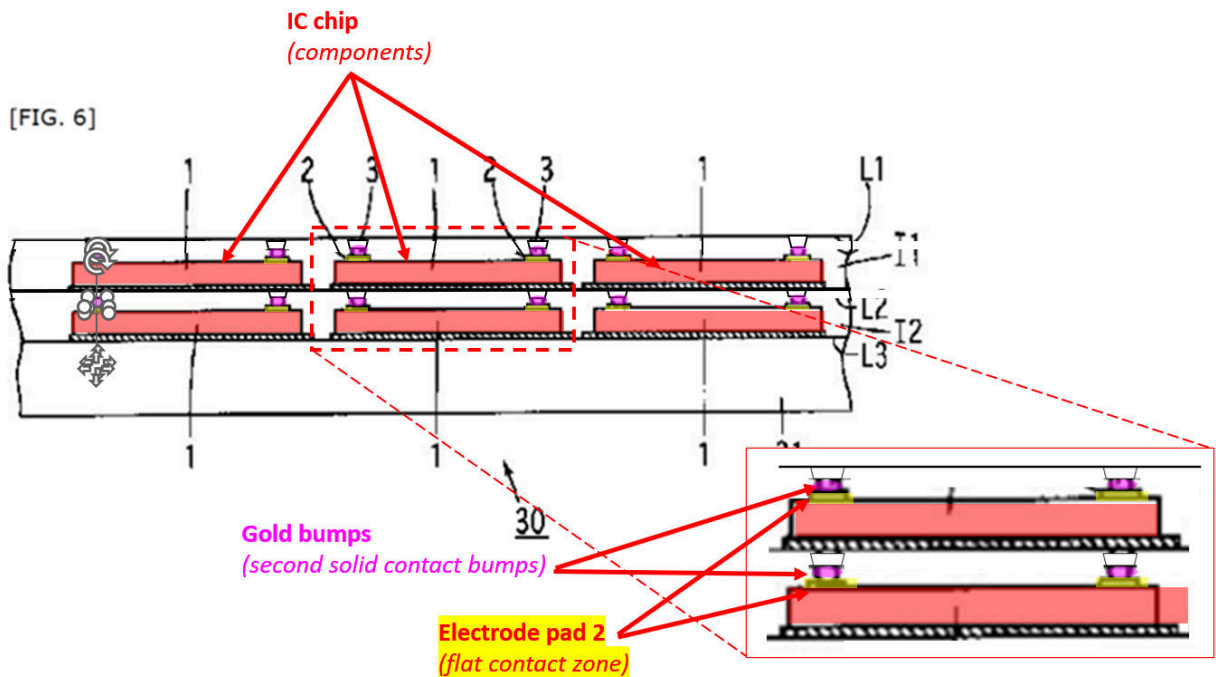


APPLE-1013, FIG. 1 (annotated, modified to include excerpt and tower bumps)

Yoneyama’s description that the bumps formed on the electrode pads may

be *either* “solder bumps *or* gold bumps” confirms that the gold bumps are distinguished from solder bumps and are thus *solderlessly* formed on the electrode pads. APPLE-1013, [0033]; APPLE-1003, ¶222. A POSITA would have also understood that the connection between the gold bumps and electrode pads is an *electrical and metallurgical* connection because the gold bumps and electrodes are both made of conductive metal materials bonded to each other. APPLE-1003, ¶223 (citing APPLE-1008, [0068], [0078]; APPLE-1004, 8:10-16).

Yoneyama’s FIG. 6 configuration also provides “*second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto.*” APPLE-1003, ¶¶224-225.

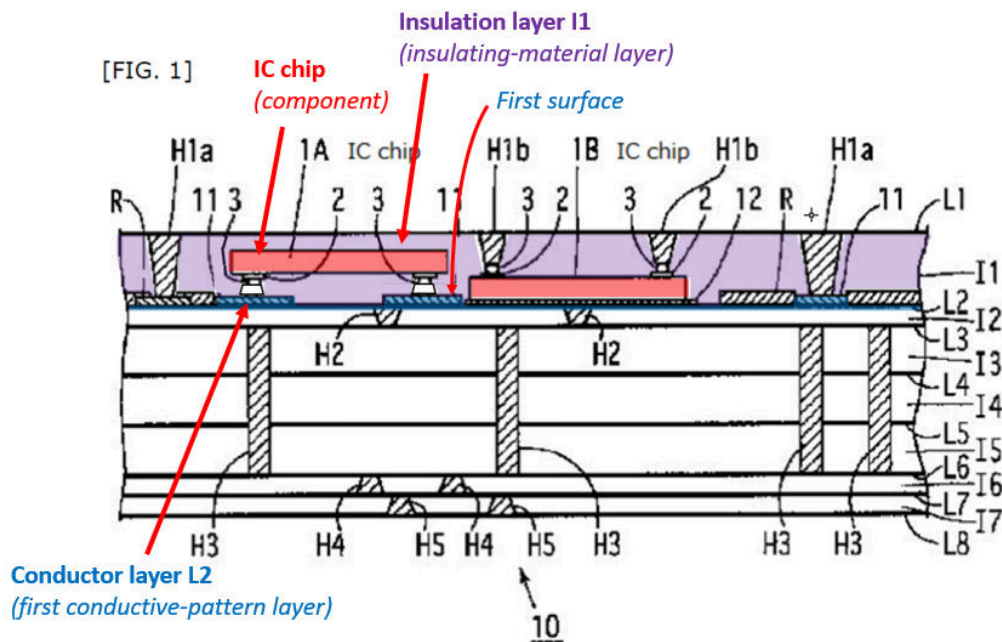


APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps)

[1e]-[1f-i]

Yoneyama-Onda renders elements [1e]-[1f-i] obvious. APPLE-1003, ¶¶226-229. For example, Yoneyama describes “forming an insulation layer I1 on the IC chips 1” over electrical conductor layer L2. APPLE-1013, Abstract, [0011], [0017], [0035], [0049]. Yoneyama’s insulation layer I1 provides an “*insulating-material layer*” in which the IC chips (*component*) is *embedded* as claimed. APPLE-1003, ¶¶226-227. Yoneyama describes that “each conductor layer is finished with an electric insulation layer I1-I7 formed by printing an electric insulation resin between the conductor layers.” *Id.*, [0011], [0001] (“embedded

electronic components”), [0017], [0021], [0026], [0035], [0049], FIG. 1; APPLE-1003, ¶228. As shown in FIG. 1, Yoneyama teaches an insulation layer I1 formed on electrical conductor layer L2 over the IC chips such that the IC chips are embedded in the insulation layer. APPLE-1003, ¶¶227-228. Accordingly, Yoneyama’s insulation layer I1 is formed “*on the first surface of the first conductive-pattern layer*” as claimed. APPLE-1003, ¶227.

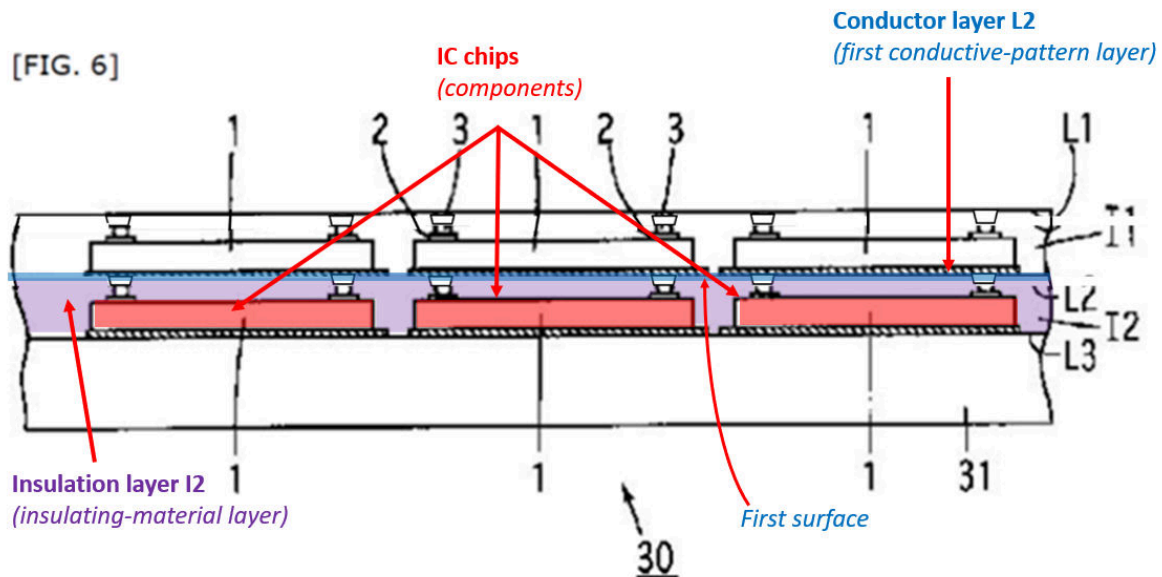


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps)

Yoneyama’s FIG. 6 configuration likewise provides “*an insulating-material layer on the first surface of the first conductive-pattern layer, wherein the component is embedded in the insulating-material layer.*” APPLE-1003, ¶229. Yoneyama describes that “an insulating resin is applied for form insulating layer

I2” before conductor layer L2 is bonded to the component. APPLE-1013, [0017].

Accordingly, a POSITA would have understood that the insulating layer I2 (insulating-material layer) is *on the first surface* of conductive pattern layer L2 (*first conductive pattern layer*).



APPLE-1013, FIG. 6 (annotated, modified to include excerpt and tower bumps)

[1f-ii]

Yoneyama-Onda renders [1f-ii] obvious. APPLE-1003, ¶¶230-234. For example, Yoneyama describes that “IC chip 1A is flip-chip bonded face-down so that bumps 2 are located on some pads 11.” APPLE-1013, [0036]. As described above, in the combination, bumps 2 formed on the IC chip electrodes (*second solid contact bumps made on the flat contact zones of the component*) as taught by

Yoneyama are electrically connected to tower bumps 4 formed on the circuit board (*first solid contact bumps made on the first surface of the first conductive-pattern layer*) as Onda teaches. *Supra* §IV.E.3 (Yoneyama-Onda combination); APPLE-1008, [0040], [0068]; APPLE-1003, ¶¶230, 191-201.

Further, in the combination, the metal bumps and tower bumps are connected using heat and pressure, as taught by Onda. APPLE-1008, [0068] (“after preparing the wiring substrate 20... and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed” after which “a heating tool is used to heat... and a pressurizing tool is used to apply pressure... to cause a metal diffusion reaction and establish a connection”); *see also* APPLE-1013, [0048] (describing that during bonding of the chip to the circuit board, “IC chip 1A is temporarily fixed by a bonding device, followed by final pressure bonding”), APPLE-1009, [0007], [0012]-[0013]; APPLE-1003, ¶231. A POSITA would have understood and found obvious that the connection between the gold bumps and tower bumps – both formed from conductive metal materials – in the combination is a *metallurgical and electrical* connection which is made *solderlessly*. APPLE-1013, [0033] (“solder bumps or gold bumps 2 are formed on multiple electrode pads on [the IC chip] active surfaces”); APPLE-1008, [0017] (“the semiconductor chip is electrically connected to the wiring patterns via the tower bumps”), [0018] (“tower

bumps on the wiring substrate comprise metal bumps ... and a plating layer for bonding that establishes an electrical connection with the semiconductor chip provided on the metal bumps”); APPLE-1003, ¶232.

That the bonding of the metal bumps of Yoneyama to the metal tower bumps of Onda results in a metallurgical and electrical connection between the bumps, in either of Yoneyama’s configurations shown in FIGS. 1 or 6, is apparent and confirmed by the fact that Yoneyama and Onda describe that same solderless thermocompression process for forming the connection that the ’527 patent describes as yielding metallurgically and electrically connected components. APPLE-1003, ¶¶233-234, 35-38; APPLE-1001, 6:41-49; APPLE-1013, [0048]; APPLE-1008, [0068]. As a result of the solderless connection, the electrode pads (“flat contact zones”) are effectively metallurgically and electrically connected to the pads of the (*first surface of the first-conductive pattern layer*) after bonding the metal bumps and tower bumps. APPLE-1013, [0048], FIGS. 1, 6; APPLE-1003, ¶¶230-234.

b) Claim 2

[2a]

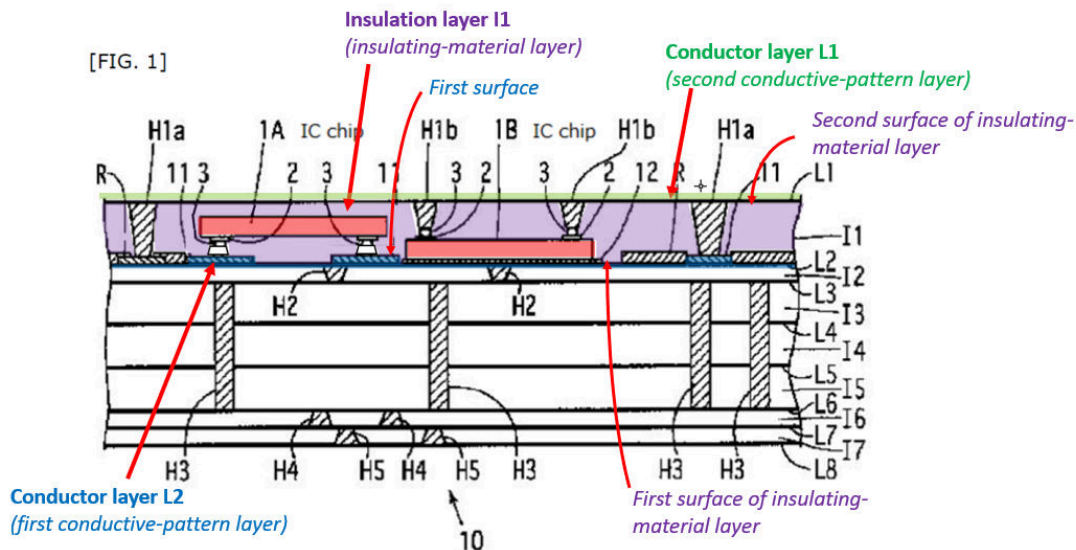
Yoneyama-Onda renders obvious claim [2]. APPLE-1003, ¶¶235-239. For example, with regard to element [2a], Yoneyama describes that “an insulating resin is applied [to the surface of conductor layer L2] to form insulating layer I1, and

then conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1.” APPLE-1013, [0017]; *supra* §IV.E.4.[1e].

Accordingly, Yoneyama describes that the insulating-material layer has a first surface where it is formed on conductor layer L2 and a second surface where conductor layer L1 will be formed. *Id.*, [0017], Figs. 1, 6; APPLE-1003, ¶¶235-236.

[2b]

With regard to element [2b], Yoneyama describes that the insulating layer I1 is formed on conductor layer L2 and “conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1.” APPLE-1013, [0017]; APPLE-1003, ¶¶237-239; *supra* §IV.E.4.[2a].

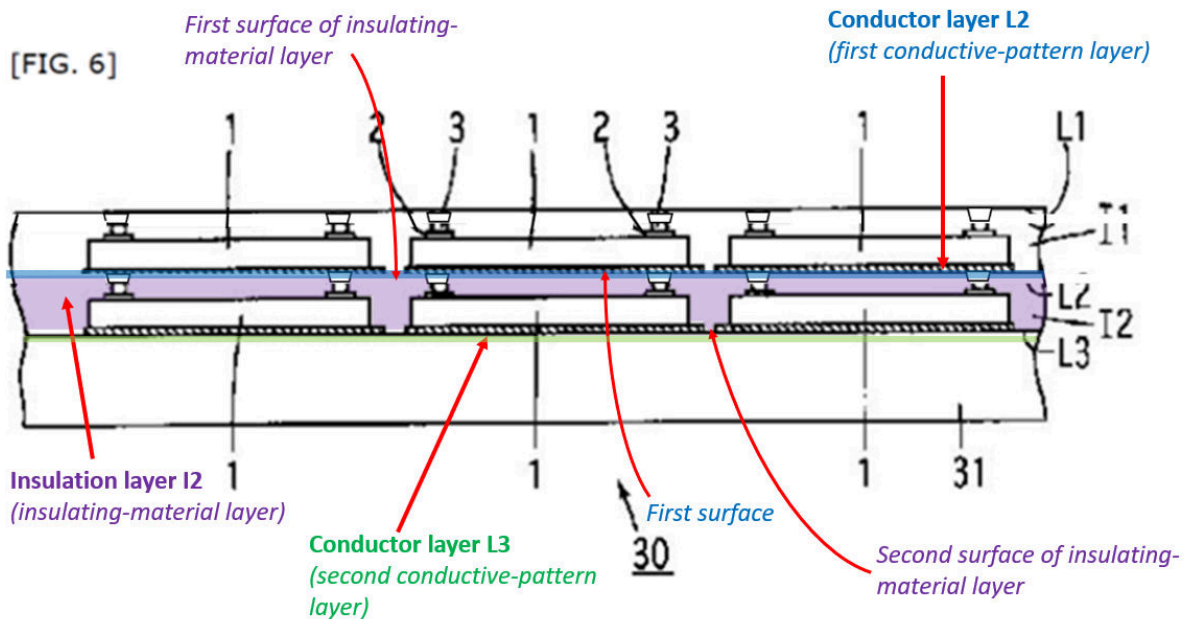


APPLE-1013, FIG. 1 (annotated, modified to include tower bumps)

As shown in FIG. 1, Yoneyama teaches that conductor layer L1 is formed on the

second surface of the insulating-material layer. APPLE-1003, ¶238.

Yoneyama's FIG. 6 configuration also provides "*a second conductive-pattern layer on the second surface of the insulating-material layer.*" APPLE-1003, ¶239.



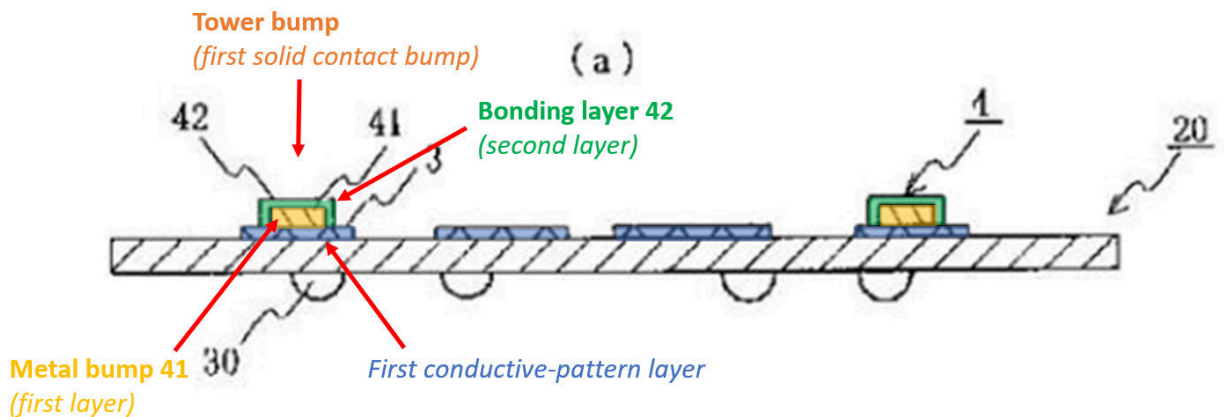
APPLE-1013, FIG. 6 (excerpted and annotated, modified to include tower bumps)

c) Claim 3

Yoneyama-Onda renders obvious claim [3]. APPLE-1003, ¶¶240-243. For example, Onda describes that "tower bumps 4 should be made of a conductive material that does not undergo a phase transformation at high temperatures [such as] high-purity gold, copper, and nickel." APPLE-1008, [0042]. Onda further describes that "tower bumps 4 are composed of a metal bump 41 and a bonding

layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1...[g]old, solder, or tin can be used, for example, in the bonding layer 42.” APPLE-1008, [0045]; APPLE-1003, ¶240.

[FIG. 2]



APPLE-1008, FIG. 1B (annotated)

For example, Onda expressly describes that the metal bump is formed from a first material (e.g., copper) and the bonding layer is formed from a second material (e.g., tin). See APPLE-1013, [0071]-[0080] (copper/tin), [0099]-[0105] (copper/gold), [0106]-[0110] (copper/aluminum). Moreover, Onda offers multiple options for materials that can form the metal bump and the bonding layer, and it would have been obvious to a POSITA to select two different materials, as Onda teaches, for example, a gold metal bump (as Yoneyama describes) and a tin bonding layer for improved bonding with the contact bumps of the component. APPLE-1003, ¶¶240-242. Accordingly, in the Yoneyama-Onda combination,

tower bumps (*first solid contact bumps*) include a metal bump and a bonding layer (*a layered structure*) with at least two layers of two different materials. APPLE-1003, ¶¶240-243.

d) Claim 4

Yoneyama-Onda renders obvious claim [4]. APPLE-1003, ¶¶244-245. For example, Yoneyama describes “a circuit board with embedded electronic components” like “a semiconductor integrated circuit chip with active surfaces on which a plurality of external connection electrodes have been formed.” APPLE-1013, [0001], [0004], [0024]; APPLE-1003, ¶245 (citing APPLE-1031, APPLE-1032, APPLE-1033).

e) Claim 5

Yoneyama-Onda renders obvious claim [5]. APPLE-1003, ¶¶246-247. For example, Yoneyama describes “a circuit board with embedded electronic components.” APPLE-1013, [0002], [0020], [0021], Figs. 1, 6; APPLE-1001, 5:4-11, 7:19-32; APPLE-1003, ¶247 (comparing Yoneyama’s embedded components to the description in the ’527 patent). In particular, Yoneyama describes preparing the circuit board with embedded components in which “the second electrical insulating layer in the second step is formed by coating and then curing an insulating resin such that the thickness of the second electrical insulating layer is greater than the thickness of the fixed first electronic component and equal to or

slightly less than the thickness of the second electronic component up to the plurality of external connection electrodes.” APPLE-1013, [0026], [049] (“an insulating resin is printed on both mounted IC chips 1A and 1B to a thickness that is a little less than that of the IC chips 1A and 1B, and cured to form insulating layer.”); APPLE-1003, ¶¶246-247.

f) Claim 6

[6a]

See supra §IV.E.4.[2a]; APPLE-1003, ¶¶248, 235-236.

[6b]

Yoneyama-Onda renders obvious claim element [6b]. APPLE-1003, ¶¶249-253. For example, Yoneyama describes that a “conductor layer L1 on which a wiring pattern has been formed is formed on the surface of insulating layer I1.” APPLE-1013, [0017]. Yoneyama further explains how the conductor layer L1 is formed by “a lamination method, such as laminating copper foil with resin or copper foil between prepregs, or a plating method is used.” APPLE-1013, [0050], [0011]. Copper foil with resin, between prepregs, or with plating provides a “*conductive film*” on the second surface of the insulating layer I1 (*insulating-material layer*). APPLE-1003, ¶¶249-250; *cf.* APPLE-1001, 6:27-29 (“metal film [] can also be a surfaced metal film, or some other film including several layers or several materials”).

The language in [6b] reciting “for protecting the component against electromagnetic radiation” is an intended use of the conductive film that imparts no additional structural limitation that would not already be met by a conductive film and is therefore not entitled to patentable weight. Regardless, each of the structures described in the preceding paragraph that provide the claimed conductive film in Yoneyama serve to protect the IC chip (*component*) against electromagnetic radiation. APPLE-1003, ¶251. Indeed, a POSITA would have understood and found obvious the metallic materials of Yoneyama’s conductive film—such as the copper foil—naturally protect the chip from electromagnetic radiation due to the EM shielding properties of the disclosed metals. APPLE-1003, ¶¶252-253 (citing APPLE-1018, 15:47-16:14; APPLE-1019, [0025]).

g) Claim 7

Yoneyama-Onda renders claim [7] obvious. APPLE-1003, ¶¶254-255. For example, Yoneyama describes “a plurality of IC chips 1 are mounted face-up by flip-chip bonded of the surface of a substrate 31 made of a material described above on conductor layer L3 on which a wiring pattern [h]as been formed by a means used in semiconductor processing.” APPLE-1013, [0017], [0025] (“at least two first and second electronic components with active surfaces on which a plurality of external connection electrodes have been arranged are mounted on a substrate surface covered with an electrical conductor layer on which a wiring

circuit has been formed”). “Therefore, each electronic component mounted on each conductor layer is connected by way of vias H2, H3, and H4, which become components of electronic circuits.” *Id.*, [0039].

h) Claim 8

Yoneyama-Onda renders claim [8] obvious. APPLE-1003, ¶¶256-258. For example, Yoneyama describes “the present invention is a circuit board with embedded electronic components obtained by mounting at least two electronic components with active surfaces on which a plurality of external connection electrodes have been arranged on a substrate surface on which a wiring circuit has been formed.” APPLE-1013, [0021], FIG. 6. Yoneyama describes that “[e]ach conductor layer L1-L8 has the required circuit pattern, and the required chip-shaped electronic components are connected to these circuit patterns as necessary.” *Id.*, [0015], [0042] (same); APPLE-1003, ¶256. “Therefore, each electronic component mounted on each conductor layer is connected by way of vias H2, H3, and H4, which become components of electronic circuits.” *Id.*, [0039]. A POSITA also would have found that provision of an electrical connection between a pair of IC chips to be an obvious design choice that would be readily achieved using the conventional wiring patterns and interconnection techniques described in Yoneyama. *Id.* For example, a POSITA would have electrically connected Yoneyama’s components to enable communication of data signals between the

components. APPLE-1003, ¶¶257-258.

i) Claim 9

Yoneyama-Onda renders obvious claim [9]. APPLE-1003, ¶¶259-260. For example, Yoneyama describes that “[e]ach one of insulating layers I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin.” APPLE-1013, [0011], [0034] (same); APPLE-1003, ¶¶259-260 (citing APPLE-1021, 59 (“The multilayer printed circuit laminate consists of two or more copper clad epoxy glass laminates... bonded together with prepreg which has, in turn, been manufactured from woven glass fabric and epoxy resin.”), 60; APPLE-1022, 25).

To the extent the presence of glass fibers are not explicitly disclosed in layer I1, they were nonetheless conventional and well-known, as evidenced by their use in Yoneyama’s insulating layer I2-I7. APPLE-1003, ¶260. It would have been obvious to a POSITA to implement Yoneyama’s insulating layer I1 with the “large amount of filler” being a glass-reinforced epoxy sheet as Yoneyama teaches to use in layers I2-I7, and a POSITA would have been motivated to do so to provide an economical insulating material between conductive layers and to realize production efficiencies and cost savings that ordinarily result from re-use of the same or similar materials across different parts of a device (especially since layers I2-I7 can already include a glass-reinforced epoxy sheet according to Yoneyama). APPLE-

1013, [0035]; APPLE-1003, ¶260. A POSITA would have reasonably expected success because doing so would have merely involved substitution of a known insulating material for another to yield predictable results. APPLE-1003, ¶¶259-260.

j) Claim 10

Yoneyama-Onda renders obvious claim [10]. APPLE-1003, ¶¶261-265. For example, as described above, Yoneyama describes that “[e]ach one of insulating layers I2 to I7 is composed of glass cloth impregnated with a thermosetting resin such as an epoxy resin.” APPLE-1013, [0011], [0034] (same). Yoneyama describes that the “insulating layer I1 is formed by mixing a large amount of filler with a thermosetting resin such as epoxy resin” (APPLE-1013, [0011]), where epoxy resin is an organic material, and which a POSITA would have understood to have at least some flexibility, thus providing a “*flexible organic sheet*.” The ’527 Patent notably lacks any definition of the term “flexible.”

To the extent it is determined that Yoneyama does not explicitly disclose the use of a flexible organic sheet in insulating layer I1, they were nonetheless conventional and well-known by the Critical Date, and it would have been obvious to a POSITA to implement Yoneyama’s insulating layer I1 using a flexible organic sheet given that such materials were well-known insulating materials and Yoneyama’s description of similar materials (e.g., epoxy resin). APPLE-1003,

¶¶262-264. For example, Onda describes additional insulating materials that can be used in the insulation layer, including “a base film of polyimide or a liquid crystal polymer.” APPLE-1008, [0037], [0045], [0052], [0060], [0073], [0086]; APPLE-1003, ¶262. A POSITA would have been motivated to implement Yoneyama’s insulating layer I1 with a flexible organic sheet to provide an economical insulating material between conductive layers and to expand the functionality of the printed circuit board by allowing the circuit board to flex and better conform to external stresses that would commonly occur in the handling of an electronic module. APPLE-1013, [0035]; APPLE-1003, ¶¶263-265 (citing APPLE-1021, 24 (describing that “it is possible to replace one or more of the rigid layers with a flexible layer, usually made on a polyimide base” to add functionality by “extend[ing] beyond the profile of the rigid area of the board to serve as a connection to a component which is not co-planar with the board face,” “act[ing] as a hinge between two rigid areas” or “carry[ing] electrical signals to a moving part of an equipment”); APPLE-1001, 8:3-10 (describing suitable materials for the insulating-material layer including polyimide)); APPLE-1007, [0012] (describing “a tape-like film of such as polyimide”), [0100] (describing materials suitable for use in an organic film for the support); APPLE-1009, [0005]-[0006] (describing a polyimide tape), [0012]; APPLE-1021, 45). The use of a flexible organic sheet also would have been an obvious design choice that a POSITA would have been

selected to accommodate known uses and applications of electronic devices that benefit from additional flexion in the device. *Id.* A POSITA would have reasonably expected success because doing so would have merely involved substitution of a known insulating material for another to yield predictable results. APPLE-1003, ¶265.

k) Claim 11

Regardless of the scope of the limitation “metallurgically electrical connections,” Yoneyama-Onda renders obvious claim [12] under any reasonable interpretation. APPLE-1003, ¶¶266-267. Yoneyama and Onda in fact use the same connection processes as those described in the ’527 patent that are said to produce metallurgically electrical connections. APPLE-1003, ¶266; APPLE-1001, 6:41-49, 6:961-63, 6:50-54. For example, as explained above (*supra* §§IV.E.4.[1b], [1d], [1f-ii]), in the Yoneyama-Onda combination, the metal bumps and the tower bumps are connected metallurgically and electrically using a thermo-compression method as Yoneyama and Onda describe. *Supra* §IV.E.3 (Yoneyama-Onda Combination); APPLE-1008, [0068] (describing “a heating tool is used to heat... and a pressurizing tool is used to apply pressure... to cause a metal diffusion reaction and establish a connection” between the chip and wiring substrate via electrode pads, tower bumps and metal bumps); *see also* APPLE-1013, [0048] (describing that during bonding of the chip to the circuit board, “IC

chip 1A is temporarily fixed by a bonding device, followed by final pressure bonding”); APPLE-1009, [0007], [0012]-[0013] (explaining a bonding process using ultrasonic vibrations, heat and thermocompression); APPLE-1003, ¶¶266-267, 35-38, 208-214, 221-225, 230-234.

I) Claim 12

Yoneyama-Onda renders obvious claim [12]. APPLE-1003, ¶¶268-270. For example, in the combination, the tower bumps “comprise metal bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip, and a plating layer for bonding that establishes an electrical connection with the semiconductor chip provided on the metal bumps” as Onda teaches. APPLE-1008, [0018]; APPLE-1003, ¶¶268, 191-201; *supra* §IV.E.3 (Yoneyama-Onda Combination). Onda further describes that “tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1...[g]old, solder, or tin can be used, for example, in the bonding layer 42.” APPLE-1008, [0045], [0006]; APPLE-1003, ¶268.

As an example, Onda describes “gold bumps are provided on the plurality of electrode pads, a tin plating layer for bonding is provided on the tower bumps, and the electrical connections are composed of gold-tin junctions utilizing the melting point (217°C) at the first eutectic point due to the gold and tin.” APPLE-1008,

[0020], [0071]-[0083], [0006], FIG. 6; *see also* APPLE-1013, [0033] (describing “gold bumps”); APPLE-1003, ¶¶269-270. Accordingly, Yoneyama-Onda teach that the connections between the metal bumps and tower bumps are facilitated by the presence of metals such as gold and tin. APPLE-1003, ¶¶268-270.

m) Claim 13

[13pre]-[13a]

See supra §IV.E.4.[1pre]-[1a]; APPLE-1003, ¶¶271, 202-207.

[13a]

See supra §IV.E.4.[1a]; APPLE-1003, ¶¶272, 205-207.

[13b]

See supra §IV.E.4.[2b]; APPLE-1003, ¶¶273-274, . As described above, Yoneyama’s conductor layer L1 provides a “***second conductive-pattern layer***” which has ***a second surface*** as claimed. APPLE-1013, [0017], FIGS. 1, 6; APPLE-1003, ¶¶274, 237-239.

[13c],

See supra §IV.E.4.[1c], [2a]-[2b]; APPLE-1003, ¶¶275-276, 226-229, 235-239. As described above, Yoneyama’s insulating layer I1 is formed on the conductive layer L2 (***first conductive-pattern layer***) and is covered by conductive layer L1 (***second conductive-pattern layer***). APPLE-1013, [0011], [0001], [0017], [0021], [0026], [0035], [0049], FIGS. 1, 6. In either of the configurations shown in

FIGS. 1 and 6, Yoneyama's insulating layer I1 (*insulating-material layer*) is *between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer*, as claimed. APPLE-1013, FIGS. 1, 6; APPLE-1003, ¶¶275-276.

[13d]-[13g]

See supra §§IV.E.4.[1b]-[1f-ii]; APPLE-1003, ¶¶277-279, 208-234.

n) Claim 14

See supra §IV.E.4.[3]; APPLE-1003, ¶¶281, 240-243.

o) Claim 15

See supra §IV.E.4.[4]; APPLE-1003, ¶¶282, 244-245.

p) Claim 16

See supra §IV.E.4.[6b]; APPLE-1003, ¶¶283, 249-253.

q) Claim 17

See supra §§IV.E.4.[7]; APPLE-1003, ¶¶284, 254-255.

r) Claim 18

See supra §IV.E.4.[4], [8]; APPLE-1003, ¶¶285, 244-245, 256-258.

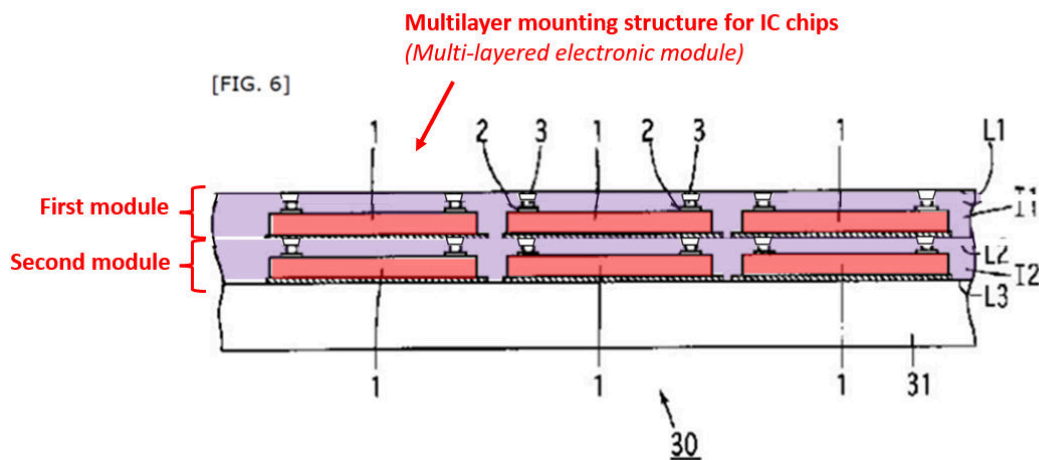
s) Claim 19

[19pre]

The preamble is not limiting, but regardless, Yoneyama-Onda renders obvious claim element [19pre]. APPLE-1003, ¶¶286-287. For example, Yoneyama describes, with respect to the FIG. 6 configuration, a “multilayer

mounting structure” in which “identical IC chips are stacked in multiple layers.”

APPLE-1013, [0016]-[0018], [0015] (“Each conductor layer L1-L8 has the required circuit pattern”), [0042] (same).



APPLE-1013, FIG. 6 (annotated, modified to include tower bumps)

For example, Yoneyama describes with respect to FIG. 6 “a plurality of IC chips 1 are mounted face-up by flip chip bonded of the surface of a substrate 31 made of a material described above on conductor layer L3 on which a wiring pattern [h]as been formed.” APPLE-1013, [0017]. After an insulating layer is formed around the IC chip, “conductor layer L2 on which a wiring pattern has been formed is formed on the surface of insulating layer I2 in the same manner as described above [and] a plurality of IC chips 1 are mounted face-up on the surface of conductor layer L2 by flip chip bonding.” *Id.*; APPLE-1003, ¶¶286-287.

[19a]-[19f]

See supra §§IV.E.4.[1a]-[1f-ii]; APPLE-1003, ¶¶288-293, 205-234.

t) Claim 20

Yoneyama-Onda renders claim [20] obvious. APPLE-1003, ¶¶294-297. For example, Yoneyama describes that a “future application [of the multilayer IC chip mounting structure] is in memory modules, since identical IC chips are stacked in multiple layers.” APPLE-1013, [0018]. Accordingly, Yoneyama-Onda renders obvious a multi-layered electronic module comprising a plurality of memory circuits. APPLE-1003, ¶¶294-297.

u) Claim 21

Yoneyama-Onda renders claim [21] obvious. APPLE-1003, ¶¶298-299. For example, Yoneyama describes with respect to FIG. 5 that “[t]he other pads 21 on conductor layer L2 are connected to conductor layer L1 by way of vias H1 [and] conductor layer L2 is connected to conductor layer L3 by way of vias,” such that each conductor layer is connected to adjacent layers by vias. APPLE-1013, [0013], [0039]. “Each conductor layer L1-L8 has the required circuit pattern, and the required chip-shaped electronic components are connected to these circuit patterns as necessary.” *Id.*, [0015]; *see also id.*, [0042]. “Thus, vias are provided to electrically connect the necessary conductor layers through their respective insulation layers” so that the electronic modules are electrically connected to form

a functioning totality. *Id.*, [0014], [0039]; APPLE-1003, ¶¶298. Yoneyama's FIG. 6 configuration differs from FIG. 5 in that the IC chips in FIG. 6 are mounted face-up (*see* APPLE-1013, [0016]), but a POSITA would have understood and found obvious that similar structures for interconnecting layers of the device as provided in FIG. 5 would similarly apply to FIG. 6. APPLE-1003, ¶¶299. For example, electrically connecting the electronic modules in Yoneyama's FIG. 6 configuration would have been obvious to achieve known and predictable advantages of such interconnections, including to enable communication between IC chips in different layers/modules of the device via electrical sent through the inter-layer/module connections. *Id.*

v) Claim 22

[22pre]

See supra §IV.E.4.[19pre]; APPLE-1003, ¶¶300, 286-287.

[22a]-[22f]

See supra §§IV.E.4.[1a]-[1f-ii]; APPLE-1003, ¶¶301-306, 205-234.

w) Claim 23

See supra §IV.E.4.[20]; APPLE-1003, ¶¶307, 294-297.

x) Claim 24

See supra §IV.E.4.[21]; APPLE-1003, ¶¶308, 298-299.

y) Claim 25

[25pre]

See supra §IV.E.4.[19pre]; APPLE-1003, ¶¶309, 286-287.

[25a]

See supra §IV.E.4.[1a]; APPLE-1003, ¶¶310, 205-207.

[25b]

See supra §§IV.E.4.[2a]-[2b], [13b]; APPLE-1003, ¶¶311, 235-239, 273-274.

[25c]

See supra §§IV.E.4.[1e], [2a]-[2b], [13c]; APPLE-1003, ¶¶312, 226-229, 235-239, 275-277.

[25d]-[25g]

See supra §IV.E.4.[1b]-[1d], [1f-i]-[1f-ii]; APPLE-1003, ¶¶313-316, 208-234.

z) Claim 26

See supra §IV.E.4.[20]; APPLE-1003, ¶¶317, 294-297.

aa) Claim 27

See supra §IV.E.4.[21]; APPLE-1003, ¶¶318, 298-299.

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. Section 325(d)

The asserted combinations in this Petition are materially different from the

art references addressed during prosecution of the '527 patent. The presently cited references – i.e., Nishiuma, Nakatani, Shibata, Yoneyama, and Onda—were never considered, or even cited during prosecution.⁶ APPLE-1001, Cover (56); APPLE-1002. These references offer new and distinct teachings that provide the features erroneously deemed missing from the prior art by the Examiner. Neither part of the *Advanced Bionics* two-part framework is met and denying institution under §325(d) would be inconsistent with the Board's precedent.

B. Section 314(a)

The *Fintiv* factors weigh against exercising discretionary denial. This Petition's merits are compelling, and the evidence presented herein is substantial, counseling against discretionary denial under *Fintiv*. The related litigation remains in its infancy.

Factor 1 is neutral or favors institution. A motion to transfer to the Northern District of California is pending. While a motion to stay has not been filed, even without inferring how the district court would rule, the pending motions at least

⁶ The petition in IPR2023-00069 previously cited Nishiuma and Nakatani, but that proceeding terminated pursuant to settlement before institution. ImberaTek had not even submitted a preliminary response before that IPR terminated.

increase the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. Even if the district court proceeding is not transferred, the Board will likely issue its final written decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is also uncertain and subject to change due to a number of factors, including Apple's pending motion to transfer.

Factor 3 favors institution because Petitioner has diligently filed this Petition while the litigation remains in its early stages. As noted above, Apple's motion to transfer remains pending.

Factor 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the district court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds. The strength of the merits alone outweigh any inefficiencies borne of parallel litigation.

VI. CONCLUSION AND FEES

The Challenged Claims are unpatentable. Please charge fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple Inc. is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or pending petitions for *inter partes* review for the '527 Patent. The '527 patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024. The '527 patent has also been the subject of a civil action in *Samsung Electronics Co., Ltd. et al v. ImberaTek LLC*, IPR2023-00069 (PTAB), filed October 18, 2022; and *ImberaTek LLC v. Samsung Electronics Co., Ltd. et al.*, 2-22-cv-00233 (EDTX), filed June 24, 2022, and was challenged in IPR2023-00069 (terminated).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0191IP1@fr.com.

Respectfully submitted,

Dated: February 6, 2025

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,971 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 6, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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