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The document is designated as:

JP Patent Application Publication No. 2001-339165A ("Sakamoto")

A handwritten signature in blue ink, appearing to read 'F. McGee'.

Frank McGee

October 14, 2024

(51) Int. CI ⁷	ID number			FI	Theme code (ref.)
H 05 K	3/46	H 05 K	3/46	Q	5E346
H 01 L	23/12	H 01 L	23/12	501B	
	501			501Z	
				N	
				P	

Request for Examination: No

Number of Claims: 5 OL Total Pages: 14

(21) Filed Application No. : 2000-388457
(P2000-388457)

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(22) Filed: Dec. 21, 2000
(2000.12.21)

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(31) Priority Claim No.: 2000-78206
(P2000-78206)

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(32) Priority Date: Mar. 21, 2000
(2000.3.21)

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(33) Country of Priority Claim: Japan (JP)
(31) Priority Claim No.: 2000-49121

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Continued on last page

(54) [TITLE OF INVENTION] MULTILAYER PRINTED WIRING BOARD AND PACKAGE SUBSTRATE

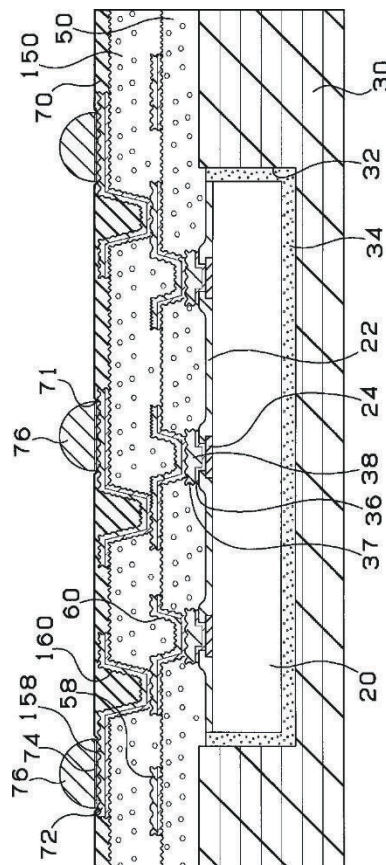
(57) [ABSTRACT]

PROBLEM

A multilayer printed wiring board that can be directly electrically connected to an IC chip without a lead component is proposed.

MEANS TO SOLVE THE PROBLEM

In the multilayer printed wiring board, an IC chip 20 is incorporated in a core substrate 30 in advance, and a transition layer 38 is provided on a die pad 24 of the IC chip 20. Therefore, the IC chip and the multilayer printed wiring board can be electrically connected without using lead components or sealing resin. In addition, by providing the transition layer 38 on the die pad 24, even if the die pad 24 has a fine pitch (150 μm) and/or a small size (20 μm or less), buildup layers can be stacked, and connectivity and reliability between the die pad 24 and the via hole 60 is improved.



CLAIMS

[Claim 1]

A multilayer printed wiring board, in which an interlayer insulating layer and a conductor layer are repeatedly formed on a substrate and a via formed in the interlayer insulating layer, and that is electrically connected through the via, wherein electronic components are incorporated in the substrate.

[Claim 2]

The multilayer printed wiring board according to claim 1, wherein electronic components are mounted on the surface thereof.

[Claim 3]

The multilayer printed wiring board according to claim 1 or claim 2, wherein the substrate is provided with terminals for connecting with an external substrate.

[Claim 4]

A multilayer printed wiring board, in which an interlayer insulating layer and a conductor layer are repeatedly formed on a substrate and a via is formed in the interlayer insulating layer, and that is electrically connected through the via, wherein electronic components are incorporated in the substrate, and an upper part of a die pad of the electronic components is formed with a transition layer for connecting to the via of the lowest interlayer insulating layer.

[Claim 5]

The multilayer printed wiring board according to any one of claims 1 to 4, wherein the substrate is a package substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNOLOGICAL FIELD OF THE INVENTION

The present invention relates to a build-up multilayer printed wiring board, and more particularly to a multilayer printed wiring board and a package substrate containing electronic components such as IC chips.

[0002]

CONVENTIONAL TECHNOLOGY

An IC chip is electrically connected to a printed wiring board by a mounting method such as wire bonding, TAB, flip chip, or the like. Wire bonding involves die-bonding an IC chip to a printed wiring board with an adhesive, connecting the pads of the printed wiring board and the pads of the IC chip with wires such as gold wires, and then protecting the IC chip and the wires by using sealing resin such as thermosetting resin or thermoplastic resin. For TAB mounting, bumps of the IC chip and pads of a printed wiring board are collectively connected by wires called leads by soldering or the like, and then sealed with resin. Flip chip mounting is performed by connecting an IC chip and pads of a printed wiring board via bumps and filling the gaps between the bumps with resin.

[0003]

PROBLEM TO BE SOLVED BY THE INVENTION

However, with each mounting method, the IC chip and the printed wiring board are electrically connected by connecting lead components (wires, leads, and bumps). Each of these lead components can be easily cut or corroded, which may cause

disconnection with the IC chip or malfunction. With each mounting method, the IC chip is sealed with a thermoplastic resin such as an epoxy resin to protect the IC chip. However, if air bubbles are introduced in the sealant filling process, the air bubbles can become a starting point for breakage of the lead components and corrosion of the IC pads, thus reducing reliability. When sealing with thermoplastic resin, it is necessary to create a resin loading plunger and mold for each part. Even when using thermosetting resin, the materials of the lead components, solder resist, and the like must be considered when selecting resins that are mutually compatible, as each of these issues causes an increase in cost.

[0004] An object of the present invention is to solve the above-mentioned problems, and to propose a multilayer printed wiring board and a package substrate which can be directly electrically connected to an IC chip without lead components.

[0005]

MEANS FOR SOLVING THE PROBLEM

As a result of intensive research, the present inventors have discovered that a structure that enables leadless, bumpless electrical connection with the IC chip can be achieved without using a sealing resin, by providing an opening portion, through hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip or the like beforehand, laminating an interlayer insulating layer, providing a via on the IC chip pad by photoetching or laser to form a conductor circuit that is a conductor layer, and then repeatedly forming the interlayer insulating layer and the conductor layer to provide a multilayer printed wiring board. [0006] Furthermore, the present inventors have also proposed that electronic components such as an IC chip or capacitor could also be packaged on a surface of the multilayer printed wiring board, by providing an opening portion, through hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip or the like beforehand, laminating an interlayer insulating layer, providing a via on the IC chip pad by photoetching or laser to form a conductor circuit that is a conductor layer, and then repeatedly forming the interlayer insulating layer and the conductor layer to provide a multilayer printed wiring board. As a result, leadless, bumpless electrical connection can be made with the IC chip without using a sealing resin. In addition, electronic components such as IC chips and capacitors having different functions can be mounted, and a multi-layer printed wiring board with higher functionality can be obtained. As a specific example, by embedding an IC chip having a calculating function as a built-in IC chip and mounting a cache memory and a capacitor on the surface layer, it is possible to arrange the IC chip, the cache memory, and the capacitor close to each other.

[0007] Furthermore, as a result of intensive research, the present inventors have proposed providing a transition layer containing a conductor layer by preparing an opening portion, through hole, or counterbore in the resin insulating substrate and storing electronic components such as an IC chip or the like in advance. An electrical connection with an IC chip can be achieved in a leadless and bumpless manner without using a sealing resin by laminating an interlayer insulating layer on the transition layer, providing a via on the transition layer by photoetching or laser to form a conductive circuit, which is a conductive layer, and then repeatedly forming interlayer insulating layers and conductor layers to form a multilayer printed wiring board.

Since the transition layer is formed on the IC chip portion, the IC chip portion is flattened, and thus the upper interlayer insulating layer is also flattened and the film thickness is uniform. Furthermore, the transition layer allows shape stability to be maintained during the formation of the via in the upper layer.

[0008] The transition layer defined in the present invention will be described. The transition layer refers to a midway intermediate layer provided for direct connection between an IC chip, which is a semiconductor element, and a printed wiring board without using conventional IC chip mounting technology. The transition layer is formed of two or more metal layers and is made larger than the die pad of an IC chip, which is a semiconductor element. As a result, electrical connection and alignment are improved, and via hole processing by laser or photoetching can be performed without damaging the die pad. Therefore, reliably embedding, accommodating, storing, and connecting the IC chip to the printed wiring board is possible. Therefore, a metal, which is a conductor layer of a printed wiring board can be directly formed on the transition layer. Examples of such conductor layers include via holes in interlayer resin insulating layers and through holes on substrates.

[0009] The reason for providing the transition layer on the pad of the IC chip is as follows. First, if the die pad is fine and small in size, alignment becomes difficult when forming a via, so a transition layer is provided to facilitate alignment. By providing a transition layer, a buildup layer can be stably formed even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less. If a via in the interlayer insulating layer is formed by photoetching while the die pad does not have a transition layer is formed thereon, and if the diameter of the via is larger than the diameter of the die pad, the polyimide layer, which is the protective layer of the die pad surface, will be dissolved or damaged when removing residues at the bottom of the via and during the de-smearing process performed as a roughening process of the interlayer insulating layer surface. On the other hand, in the case of using laser, and if the via diameter is larger than the die pad diameter, the die pad, passivation, and polyimide layers (protective film of the IC) are destroyed by the laser. Furthermore, if the pad of the IC chip is very small and the via diameter is larger than the die pad size, alignment for the photoetching or laser method becomes difficult, and connection failures between the die pad and the via can frequently occur.

[0010] On the other hand, by providing a transition layer on the die pad, even if the die pad pitch is 150 μm or less and the pad size is 20 μm or less, the via can be reliably connected to the die pad, improving reliability.

Furthermore, by interposing a transition layer with a larger diameter on the pad of the IC chip, the die pad can be immersed in an acid or an etchant or subjected to various annealing processes during post-processes such as de-smearing and plating processes with no risk of dissolving

or damaging the protective films (passivation, polyimide layer) of the IC.

[0011] Although the functions are achieved by the respective multilayer printed wiring board, in some cases, BGA, solder bumps, and PGA (conductive connection pins) can be used for connecting with external substrates such as motherboards and daughterboards in order to function as a package substrate for semiconductor devices. Moreover, this configuration can shorten the wiring length and reduce the loop inductance as compared with a case of connecting with a conventional mounting method.

[0012] Resin substrates for incorporating electronic components such as IC chips used in the present invention include epoxy resin, BT resin, resins such as phenol resin or the like impregnated with a reinforcing material such as glass epoxy resin or a core material, or a laminate pre-preg impregnated with epoxy resin, but any material generally used in printed wiring boards can be used. In addition, a double-sided copper-clad laminate, a single-sided plate, a resin plate having no metal film, or a resin film can also be used.

[0013] Physical vapor deposition such as vapor deposition or sputtering is performed on the entire surface of the core substrate in which the IC chip is incorporated to form a conductive metal film on the entire surface. The metal is preferably one or more layers of metal such as tin, chromium, titanium, nickel, zinc, cobalt, gold, and copper. The thickness is preferably 0.001 to 2.0 μm . A thickness of 0.01 to 1.0 μm is particularly preferable.

[0014] When forming the transition layer by a semi-additive process, a dry film resist can be formed on the metal film formed on the IC chip and the core substrate to remove the portion corresponding to the transition layer, the transition layer can then be thickened by electroplating, and afterwards the resist can be removed and an etchant can be used to similarly form the transition layer on top of the IC chip pad.

[0015] On the other hand, when the transition layer is formed by a subtractive process, the layer is thickened on the metal film by electroless or electrolytic plating. Types of plating that can be used include copper, nickel, gold, silver, zinc, iron, and the like. Copper is preferably used for its electrical properties, economy, and the fact that the conductor layer, which is a build-up to be formed later, is mainly made of copper. The thickness is preferably in the range of 1 to 20 μm . With any greater thickness, undercutting may occur during etching, and a gap may occur between the formed transition layer, the via, and the interface. Next, an etching resist is formed, exposed and developed, and then etching was performed to expose the metal on the portions other than the transition layer, in order to form the transition layer on the pad of the IC chip.

[0016]

EMBODIMENTS OF THE INVENTION

Provided hereunder is a description of an embodiment of the present invention with reference to the accompanying drawings. First, the configuration of the multilayer printed wiring board according to Embodiment 1 of the present invention will be described with reference to FIG. 6, which illustrates the cross-section of the multilayer printed wiring board 10.

[0017] As illustrated in FIG. 6, the multilayer printed wiring board 10 includes a core substrate 30 storing an IC chip 20, interlayer resin insulating layer 50, and interlayer resin insulating layer 150. Via 60 and conductor circuit 58 are formed in the interlayer resin insulating layer 50, and via 160 and conductor circuit 158 are formed in the interlayer resin insulating layer 150.

[0018] The IC chip 20 is covered with an IC protective film (passivation + polyimide) 22, and a die pad 24 forming an input/output terminal is provided in an opening of the IC protective film 22. A die transition layer 38 is formed on the pad 24.

[0019] A solder resist layer 70 is provided on the interlayer resin insulating layer 150. The conductive circuit 158 under the opening 71 in the solder resist layer 70 is provided with a solder bump 76 or conductive connection pin (not illustrated) for connecting to an external substrate such as a daughterboard or motherboard, or the like (not illustrated).

[0020] In the multilayer printed wiring board 10 of the present Embodiment, the IC chip 20 is incorporated in the core substrate 30 in advance, and the transition layer 38 is provided on the pad 24 of the IC chip 20. Therefore, alignment is simplified when forming the via, and a buildup layer can be stably formed even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less. If a via in the interlayer insulating layer is formed by photoetching with the die pad on which a transition layer is not formed, and if the diameter of the via is larger than the diameter of the die pad, the polyimide layer, which is the protective layer of the die pad surface, is dissolved or damaged during the de-smearing process performed when removing residue at the bottom of the via as a roughening process of the interlayer insulating layer surface. On the other hand, in the case of using laser, and if the via diameter is larger than the die pad diameter, the die pad, passivation, and polyimide layers (protective film of the IC) are destroyed by the laser. Furthermore, if the pad of the IC chip is very small and the via diameter is larger than the die pad size, alignment for the photoetching or laser method becomes difficult, and connection failures between the die pad and the via can frequently occur.

[0021] On the other hand, by providing a transition layer on the die pad, even if the die pad pitch is 150 μm or less and the pad size is 20 μm or less, the via can be reliably connected to the die pad, improving reliability. Furthermore, by interposing a transition layer with a larger diameter on the pad of the IC chip, the die pad can be immersed in an acid or an etchant or subjected to various annealing processes during post-processes such as de-smearing and plating processes with no risk of dissolving or damaging the protective films (passivation, polyimide layer) of the IC.

[0022] Subsequently, the method for manufacturing the multilayer printed wiring board described above with

reference to FIG. 6 will be described with reference to FIG. 1 to FIG. 5.

[0023] (1) First, an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as glass cloth is impregnated with a resin such as epoxy or the like is used as a starting material (see FIG. 1 (A)). Next, a recessed part 32 for accommodating an IC chip is formed on one side of the core substrate 30 by counterbore processing (see FIG. 1 (B)). Here, the recessed part is provided by counterbore processing, but a core substrate with a storing portion can be formed by laminating an insulating resin substrate with an opening and an insulating resin substrate without an opening.

[0024] (2) Afterwards, an adhesive material 34 is applied to the recessed part 32 using a printing machine. At this time, potting or the like may be performed in addition to applying. Next, the IC chip 20 is placed on the adhesive material 34 (see FIG. 1(C)).

[0025] (3) Furthermore, an upper surface of the IC chip 20 is pressed or struck so as to be completely stored in the recessed part 32 (see FIG. 1 (D)). Thereby, the core substrate 30 can be made smooth.

[0026] (4) Thereafter, physical vapor deposition such as vapor deposition or sputtering is performed on the entire surface of the core substrate 30 accommodating the IC chip 20 to form a conductive metal film 33 on the entire surface (FIG. 2 (A)). The metal is preferably one or more layers of metal such as tin, chromium, titanium, nickel, zinc, cobalt, gold and copper. The thickness is preferably 0.001 to 2.0 μm . A thickness of 0.01 to 1.0 μm is particularly preferable. In particular, the metal is preferably nickel, chromium, or titanium. This is because these metals do not allow intrusion of moisture from the interface, and metal adhesion is excellent. The thickness of chromium should be such that cracks do not occur in the sputtered layer and sufficient adhesion to the sputtered copper layer can be obtained.

[0027] A plated film 36 may be formed on the metal film 33 by electroless plating (FIG. 2(B)). Types of plating that can be formed include nickel, copper, gold, silver, and the like. Copper is preferably used because of its electrical properties, economy, and the fact that the conductor layer, which is a build-up to be formed later, is mainly copper. The thickness of the plated film should be in a range of 0.01 to 5 μm . A thickness of 0.1 to 3 μm is particularly preferable. Desirable combinations of the first thin film layer and the second thin film layer are chromium-copper, chromium-nickel, titanium-copper, and titanium-nickel. These combinations are superior to other combinations in terms of bond-ability with metals and electrical conductivity.

[0028] (5) Thereafter, a resist is applied or a photosensitive film is laminated, exposed and developed to form a plating resist 35 to form an opening above the pad of the IC chip, and thus an electrolytic plated film 37 is formed (FIG. 2 (C)). The thickness of the electrolytic plated film 37 is preferably about 1 to 20 μm . The films can be formed of nickel, copper, gold, silver, zinc, or iron. After removing the plating resist 35, the electroless plated film 36 and the metal film 33 under the plating resist 35 are removed by etching to form a transition layer 38 on the pad 24 of the IC chip (FIG. 2(D)).

Here, the transition layer is formed by a plating resist, but after uniformly forming an electrolytic plated film on the electroless plated film 36, an etching resist can be formed, exposed, and developed to form portions other than the transition layer to expose and etch the metal, in order to form a transition layer on the pad of the IC chip. In this case, the thickness of the electroplated film should be in a range of 1 to 20 μm . This is because if the thickness is greater, undercutting may occur during etching, and a gap may be generated at the interface between the formed transition layer and the via.

[0029] (6) Next, an etchant is sprayed onto the substrate to etch the surface of the transition layer 38 to form a roughened surface 38 α (see FIG. 3 (A)). A roughened surface can also be formed using electroless plating or oxidation-reduction treatment.

[0030] (7) A thermosetting cycloolefin resin sheet having a thickness of 30 to 50 μm is laminated on the substrate that has undergone the above steps under vacuum at a pressure of 5 kg/cm^2 while raising the temperature to 50 to 150 $^{\circ}\text{C}$, resulting in an interlayer resin insulating layer 50 made of a cycloolefin resin (see FIG. 3 (B)). The degree of vacuum during vacuum pressure bonding is 10 mmHg. Alternatively, the insulating layer may be formed by applying a liquid insulating resin by spin coating or the like.

[0031] (8) Next, a via opening 48 is formed in the interlayer resin insulating layer 50 by a CO_2 gas laser (see FIG. 3 (C)). Chromic acid is used to remove resin residue in the opening 48. Alignment when forming the via is simplified, and the via on the die pad 24 is positively connected, and thus connectivity and reliability between pads and the via is improved, by providing a transition layer 38 made of copper

[Electroplating aqueous solution]

Sulfuric acid 2.24 mol/L

Copper sulfate 0.26 mol/L

Additive (Capalacid HL, manufactured by Atotech Japan)

19.5 mL/L

[Electroplating conditions]

Current density 1 A/ dm^2

Time 65 min.

Temperature $22 \pm 2^{\circ}\text{C}$

[0036] (12) After removing the plating resist 54 with 5% NaOH, the electroless plated film 52 under the plating resist is dissolved and removed by etching using a mixed solution of nitric acid, sulfuric acid, and hydrogen peroxide, forming the conductor circuits 58 and the via 60 with a thickness of 16 μm made of the electroless plated film 52 and electrolytic plated film 56, to form roughened surfaces 58 α and 60 α using an etchant containing a dicopper complex and an organic acid (FIG. 4 (C)).

[0037] (13) Next, the above steps (8) to (13) are repeated to form additional upper interlayer resin insulating layers 150 and conductor circuits 158 (including via 160) (see FIG. 5 (A)).

[0038] (14) Next,

46.67 parts by weight of a photosensitive oligomer (molecular weight 4,000) where 50% of epoxy groups of a cresol novolak-type epoxy resin (manufactured by Nippon Kayaku Co., Ltd.) are acrylated, dissolved in diethylene glycol dimethyl ether (DMDG) to achieve a concentration of 60 weight%; 15 parts by weight of a 80 weight% bisphenol A type epoxy resin (trade name Epicoat 1001 manufactured by Yuka Shell Co. Ltd.) dissolved in methyl ethyl ketone; 1.6 parts by

on the die pad 24. Thereby, a buildup layer can be stably formed. By interposing a transition layer with a larger diameter on the pad of the IC chip, the protective film (passivation, polyimide layer) 22 of the die pad 24 and the IC can be dissolved and the risk of damage can be eliminated by immersing in an acid or etching solution and performing various annealing processes during a subsequent process such as a plating process or the like, during a desmearing process for roughening the interlayer resin insulating layer surface and removing residue in the via bottom. In this case, permanganic acid is used to remove resin residue, but oxygen plasma can also be used for de-smearing.

[0032] (9) Next, the surface of the interlayer resin insulating layer 50 is roughened to form a roughened surface 50 α (see FIG. 3 (D)). Note that this roughening step can be omitted.

[0033] (10) Next, after applying a palladium catalyst to the surface of the interlayer resin insulating layer 50, the substrate is immersed in an electroless plating solution to form an electroless plated film 52 on the surface of interlayer resin insulating layer 50 (FIG. 4 (A)).

[0034] (11) A commercially available photosensitive dry film is applied on the substrate 30 after the above processing, a chrome glass mask is placed thereon, and then the film is exposed at 40 mJ/cm^2 , and then developed with 0.8% sodium carbonate, providing a plating resist 54 having a thickness of 25 μm . Next, electrolytic plating is performed under the following conditions to form an electrolytic plated film 56 having a thickness of 18 μm (see FIG. 4 (B)). The additive in the electrolytic plating aqueous solution is Capracid HL manufactured by Atotech Japan.

[0035]

weight of an imidazole curing agent (trade name 2E4MZ-CN manufactured by Shikoku Kasei Co., Ltd.); 3 parts by weight of a polyfunctional acrylic monomer (trade name R604 manufactured by Kyoei Chemical Co., Ltd.); 1.5 parts by weight of a similarly polyvalent acrylic monomer (trade name DPE6A manufactured by Kyoei Chemical Co., Ltd.); and 0.71 parts by weight of a dispersion antifoaming agent (trade name S-65 manufactured by San Nopco Inc.); are taken in a container, stirred and mixed to prepare a mixed composition, to which 2.0 parts by weight of benzophenone (manufactured by KANTO CHEMICAL CO., INC.) as a photopolymer initiator; and 0.2 parts by weight of Michler's ketone (manufactured by KANTO CHEMICAL CO., INC.) as a photosensitizer are added to obtain a solder resist composition (organic resin insulating material) having a viscosity adjusted to 2.0 $\text{Pa} \cdot \text{s}$ at 25 $^{\circ}\text{C}$.

The viscosity was measured using a B-type viscometer (DVL-B type manufactured by Tokyo Keiki Co., Ltd.,) using rotor No. 4 at 60 rpm, and rotor No. 3 at 6 rpm.

[0039] (15) Next, the solder resist composition is applied to a thickness of 20 μm on the substrate 30, and dried under the conditions of 70° C for 20 minutes and 70° C for 30 minutes. A 5 mm-thick photomask having a pattern drawn thereon is brought into close contact with the solder resist layer 70, exposed to ultraviolet rays of 1000 mJ/cm², and developed with a DMTG solution to form openings 71 with a land diameter of 620 μm and an opening diameter of 460 μm . (See FIG. 5 (B)).

[0040] (16) Next, the substrate on which the solder resist layer (organic resin insulating layer) 70 is formed is coated with nickel chloride (2.3×10^{-1} mol/L), sodium hypophosphate (2.8×10^{-1} mol/L), and sodium citrate (1.6×10^{-1} mol/L) in an electroless nickel plating solution of pH = 4.5 for 20 minutes to form a 5 μm thick nickel plating layer 72 in the opening 71. Furthermore, the substrate is mixed with potassium gold cyanide (7.6×10^{-3} mol/L), ammonium chloride (1.9×10^{-1} mol/L), and sodium citrate (1.2×10^{-1} mol/L), and immersed in an electroless plating solution containing sodium hypophosphite (1.7×10^{-1} mol/L) at 80°C for 7.5 minutes to form a gold plating layer 74 with a thickness of 0.03 mm on the nickel plating layer 72, forming solder pads 75 on the conductor circuits 158 (see FIG. 5 (C)).

[0041] (17) Thereafter, solder paste is printed in the openings 71 of the solder resist layer 70 and reflowed at 200°C to form solder bumps 76. As a result, the multilayer printed wiring board 10 containing the IC chip 20 and having the solder bump 76 can be obtained (see FIG. 6). It is also possible to provide the conductive connection pin by printing solder paste.

[0042] In the above-described Embodiment, thermosetting cycloolefin resin sheets are used for interlayer resin insulating layers 50 and 150. Instead, an epoxy resin can be used for the interlayer resin insulating layer 50. This epoxy resin contains a poorly soluble resin, soluble particles, a curing agent, and other components. Each component is described below.

[0043] The epoxy resin that can be used in the production method of the present invention is composed of particles that are soluble in acids or oxidizing agents (hereinafter referred to as soluble particles) dispersed in resins that are poorly soluble in acids or oxidizing agents (hereinafter referred to as poorly soluble resins). Incidentally, the terms "poorly soluble" and "soluble" used in the present invention refer to those that have a relatively high dissolution rate when immersed in a solution containing the same acid or oxidizing agent for the same period of time. For the sake of convenience, those with a relatively slow dissolution rate are called "poorly soluble."

[0044] Examples of soluble particles include resin particles soluble in acids or oxidants (hereinafter referred to as soluble resin particles), inorganic particles soluble in acids or oxidants (hereinafter referred to as soluble inorganic particles), metal particles soluble in acids or oxidants (hereinafter referred to as soluble metal particles) and the like. These soluble particles may be used alone or as a combination of two or more.

[0045] The shape of the soluble particles is not particularly limited, and may be spherical, crushed, or the like. Moreover, it is desirable that the soluble particles have a uniform shape. This is because a roughened surface with uniform roughness can be formed.

[0046] The average particle diameter of the soluble particles is desirably 0.1 to 10 μm . Within this particle size range, particles having two or more different particle sizes may be contained. That is, this particle size range can, for example, contain soluble particles with an average particle size of 0.1 to 0.5 μm and soluble particles with an average particle size of 1 to 3 μm . As a result, a more complicated roughened surface can be formed, enabling excellent adhesiveness to the conductive circuit. In the present invention, the particle diameter of the soluble particles is the length of the longest portion of the soluble particles.

[0047] Examples of the soluble resin particles include those composed of thermosetting resins, thermoplastic resins, and the like, and those having a faster dissolution rate than the poorly soluble resin when immersed in a solution composed of an acid or an oxidizing agent, but are not particularly limited thereto. Specific examples of the soluble resin particles include those composed of epoxy resins, phenol resins, polyimide resins, polyphenylene resins, polyolefin resins, fluorine resins, and the like, and may be composed of one of these resins or consist of a mixture of two or more resins.

[0048] Resin particles made of rubber can also be used as the soluble resin particles. Examples of said rubber include polybutadiene rubber, various modified polybutadiene rubbers such as epoxy-modified, urethane-modified, and (meth)acrylonitrile-modified, (meth)acrylonitrile-butadiene rubber containing a carboxyl group, and the like. The use of rubber makes the soluble resin particles more soluble in acids or oxidizing agents. That is, when the soluble resin particles are dissolved using an acid, an acid other than a strong acid can be used for dissolving, and when the soluble resin particles are dissolved using an oxidizing agent, a permanganate with relatively low oxidizing capability may be used for dissolving.

Even when chromic acid is used, dissolving can be performed with low concentration. Therefore, no acid or oxidizing agent remains on the resin surface, and as described below, when a catalyst such as palladium chloride is applied after the roughened surface is formed, there is no fear of the catalyst not being applied or the catalyst not being oxidized.

[0049] Examples of soluble inorganic particles include particles made of at least one selected from the group consisting of aluminum compounds, calcium compounds, potassium compounds, magnesium compounds, and silicon compounds.

[0050] Examples of aluminum compounds include alumina, aluminum hydroxide, and the like. Examples of calcium compounds include calcium carbonate, calcium hydroxide, and the like. Examples of potassium compounds include potassium carbonate and the like. Examples of magnesium compounds include magnesite, dolomite, basic magnesium carbonate, and the like, and examples of silicon compounds include silica, zeolite, and the like. These may be used alone or in combination of two or more.

[0051] Examples of soluble metal particles include particles made of at least one selected from the group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, calcium, and silicon. In addition, these soluble metal particles may be coated with a resin or the like to ensure insulation.

[0052] When two or more kinds of the soluble particles are mixed and used, a combination of resin particles and inorganic particles is desirable as the combination of the two kinds of soluble particles to be mixed. This is because both soluble particles have low conductivity, the insulating properties of the resin film can be ensured, and thermal expansion can be easily adjusted with the poorly soluble resin, preventing peeling from occurring between the interlayer resin insulating layer and the conductor circuit.

[0053] The poorly soluble resin is not particularly limited as long as it can maintain the shape of the roughened surface when forming the roughened surface on the interlayer resin insulating layer using an acid or an oxidizing agent. Examples include resins, thermoplastic resins, composites thereof, and the like. Photosensitive resins obtained by imparting photosensitivity to these resins may also be used. By using a photosensitive resin, the interlayer resin insulating layer can be exposed and developed to form openings for the via. Among these, those containing a thermosetting resin are desirable. This is because the shape of the roughened surface can be maintained even by the plating solution or various heat treatments.

[0054] Specific examples of poorly soluble resins include epoxy resins, phenolic resins, phenoxy resins, polyimide resins, polyphenylene resins, polyolefin resins, and fluorine

resins. These resins may be used alone or in combination of two or more. A thermosetting resin, a thermoplastic resin, or a composite thereof may be used. Furthermore, an epoxy resin having two or more epoxy groups in one molecule is more desirable. This is because in addition to being able to form the aforementioned roughened surface, this provides excellent heat resistance and the like such that stress concentration does not occur in the metal layer even under heat cycle conditions, and peeling of the metal layer is unlikely to occur.

[0055] Examples of epoxy resins include cresol novolak-type epoxy resin, bisphenol A-type epoxy resin, bisphenol F-type epoxy resin, phenol novolac type epoxy resin, alkylphenol novolak-type epoxy resin, bisphenol F-type epoxy resin, naphthalene-type epoxy resin, dicyclopentadiene-type epoxy resin, epoxidized products of condensates of phenols and aromatic aldehydes having phenolic hydroxyl groups, triglycidyl isocyanurate, alicyclic epoxy resins, and the like. These may be used alone or in combination of two or more. As a result, this can provide excellent heat resistance and the like.

[0056] In the resin film used in the present invention, it is desirable that the soluble particles are dispersed almost uniformly in the poorly soluble resin. This is because roughened surface having uniform roughness can be formed, and even if the via or through hole is formed in the resin film, the adhesion of the metal layer of the conductive circuit formed thereon can be ensured. Also, a resin film containing soluble particles only in the surface layer forming the roughened surface may be used. As a result, portions other than the surface layer of the resin film are not exposed to the acid or the oxidizing agent, so the insulation between the conductor circuits via the interlayer resin insulating layer is reliably maintained.

[0057] In the resin film, the amount of the soluble particles dispersed in the poorly soluble resin is desirably 3 to 40 weight% of the resin film. If the content of the soluble particles is less than 3 weight%, it may not be possible to form a roughened surface having the desired unevenness, and content exceeding 40 weight% will cause the soluble particles to be dissolved by acid or oxidization to dissolve deep into the resin film, making it impossible to maintain the insulation between conductor circuits via the interlayer resin insulating layer made of the resin film, which may cause a short circuit.

[0058] Other than the soluble particles and hardly soluble resin above, the resin film preferably contains a curing agent and other components and the like. Examples of curing agents include imidazole-based curing agents, amine-based curing agents, guanidine-based curing agents, epoxy adducts of these curing agents, microencapsulated products of these curing agents, triphenylphosphine, and organic phosphine compounds such as tetraphenylphosphonium-tetraphenylborate.

[0059] The content of the curing agent is preferably 0.05 to 10 weight% with respect to the resin film. If less than 0.05 weight%, the curing of the resin film will become insufficient, so that the degree of penetration of the acid or the oxidizing agent into the resin film increases, and the insulating properties of the resin film may be impaired. On the other hand, if exceeding 10 weight%, the excessive curing agent component may modify the composition of the resin, which may lead to deterioration of reliability.

[0060] Examples of other components include fillers such as inorganic compounds and resins that do not affect the formation of the roughened surface. Examples of inorganic compounds include silica, alumina, dolomite, and the like, and examples of resins include polyimide resins, polyacrylic resins, polyamideimide resins, polyphenylene resins, melanin resins, olefin resins, and the like. By including these fillers, it is possible to improve the performance of the multilayer printed wiring board by matching the coefficient of thermal expansion and improving the heat resistance and chemical resistance.

[0061] Moreover, the resin film may contain a solvent. Examples of solvents include ketones such as acetone, methyl ethyl ketone and cyclohexanone, ethyl acetate, butyl acetate, cellosolve acetate, and aromatic hydrocarbons such as toluene and xylene. These may be used alone or in combination of two or more. However, these interlayer resin insulating layers are melted and carbonized when a temperature of 350 °C or higher is applied.

[0062] After the resin film is attached, a laser is used to open the via in the interlayer resin insulating layers. After that, the interlayer resin insulating layer is immersed in an acid or an oxidizing agent to form a roughened layer. Strong acids such as sulfuric acid, phosphoric acid, hydrochloric acid and formic acid can be used as the acid, and chromic acid, chromic sulfuric acid, permanganate and the like can be used as the oxidizing agent. Thereby, a roughened layer is formed on the surface of the interlayer resin insulating layer by dissolving or dropping the soluble particles. After applying a catalyst such as Pb to the interlayer resin insulating layer on which the roughened layer is formed, electroless plating is performed. A resist is applied on the electroless plated film, exposed to light, and developed to form a non-formed portion of the plating resist. Electroplating was applied to the non-formation portion to remove the resist, and the electroless plated film on the interlayer resin insulating layer was removed by etching to form the via and conductor circuit.

[0063] FIG. 7 (A) is a perspective view of the multilayer printed wiring board 10 according to Embodiment 1 and FIG. 7 (B) is an explanatory diagram illustrating an enlarged part of the multilayer printed wiring board 10. On the surface of the multilayer printed wiring board 10 of Embodiment 1, solder bumps (ball grid array) 76 are arranged in a hound's tooth pattern over the entire surface of the board. In Embodiment 1, by forming the solder bumps 76 also on the IC

chip 20, the wiring length from the IC chip 20 can be shortened.

[0064] FIG. 8 (A) is a perspective view of the multilayer printed wiring board 10 according to a modified example of Embodiment 1 and FIG. 8 (B) is an explanatory diagram illustrating an enlarged part of the multilayer printed wiring board 10. Solder bumps (ball grid arrays) 76 are arranged in a hound's tooth pattern on the surface of the multilayer printed wiring board 10 of the modified example at the four corners excluding the top of the IC chip 20. This modified example has the advantage that the solder bumps 76 are less susceptible to thermal and electromagnetic influences from the IC chip by avoiding the top of the IC chip 20.

[0065] Subsequently, a multilayer printed wiring board according to another modified example of Embodiment 1 of the present invention will be described with reference to FIG. 9. In Embodiment 1 described above, the case where the BGA is provided has been described. Embodiment 2 is substantially the same as Embodiment 1, but is constructed in a PGA system in which connections are made via conductive connection pins 96 as illustrated in FIG. 9.

[0066] Next, a multilayer printed wiring board according to Embodiment 2 of the invention will be described with reference to FIG. 10. In the above-described Embodiment 1, the IC chip is accommodated in the recessed part 32 provided in the core substrate 30 by counterboring. On the other hand, in Embodiment 2, the IC chip 20 is accommodated in the through hole 32 formed in the core substrate 30. In Embodiment 2, since the heat sink can be directly attached to the back side of the IC chip 20, there is an advantage that the IC chip 20 can be efficiently cooled.

[0067] Subsequently, a multilayer printed wiring board according to Embodiment 3 of the present invention will be described with reference to FIG. 11. In Embodiment 1 described above, the transition layer 38 is formed on the pads 24 of the IC chip 20 and the via 60 of the interlayer resin insulating layer 50 are connected to the transition layer 38. In contrast, in Embodiment 3, the via 60 are directly connected to the pads 24 without providing a transition layer. Since Embodiment 3 can reduce the number of steps compared to Embodiment 1, it has the advantage of being inexpensive.

[0068] Next, a multilayer printed wiring board according to Embodiment 4 of the invention will be described with reference to FIG. 12. In Embodiment 1 described above, the IC chip is accommodated in the multilayer printed wiring board. On the other hand, in Embodiment 4, the IC chip 20 is accommodated in the multilayer printed wiring board, in addition to an IC chip 120 being mounted on the surface of the board. An arithmetic CPU is accommodated as an equipped IC chip 20, and a cache memory is mounted as an IC chip 120 on the front surface.

[0069] The pads 24 of the IC chip 20 and the pads 124 of the IC chip 120 are connected by the transition layer 38-via 60-conductor circuit 58-via 160-conductor circuit 158-solder bump 76U. On the other hand, the pads 124 of the IC chip 120

and the pads 92 of the daughter board 90 are connected by solder bumps 76U-conductor circuits 158-via 160-conductor circuit 58-via 60-through holes 136-via 60-conductor circuits 58-via 160-conductor circuits 158-solder bumps 76U.

[0070] In Embodiment 4, the IC chip 20 and the cache memory 120 can be arranged close to each other while the low-yield cache memory 120 is manufactured separately from the IC chip 20 for the CPU, enabling high-speed operation of the IC chip. In this Embodiment 4, by embedding an IC chip and placing it on the surface, it is possible to mount electronic components such as IC chips with different functions, thereby obtaining a multi-layer printed wiring board with higher functionality. Although not illustrated, a capacitor can also be mounted on the surface. As a result, the IC chip 20, the cache memory 120, and the capacitor can be arranged close to each other, enabling high-speed operation of the IC chip.

[0071]

EFFECT OF THE INVENTION

With the structure of the present invention, the connection between the IC chip and the printed wiring board can be established without a lead component. Therefore, resin sealing becomes unnecessary. Furthermore, by providing the transition layer on the die pad, even if the die pad has a fine pitch (150 μm) and/or a small size (20 μm or less), it becomes possible to stack buildup layers, and improve connectivity and reliability with via holes. Furthermore, compared with the conventional IC chip mounting method, the wiring length from the IC chip to the substrate to the external substrate can be shortened, and the loop inductance can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 (A), (B), (C), and (D) are manufacturing process diagrams of a multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 2 (A), (B), (C), and (D) are manufacturing process diagrams of a multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 3 (A), (B), (C), and (D) are manufacturing process diagrams of a multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 4 (A), (B), and (C) are manufacturing process diagrams of a multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 5 (A), (B), and (C) are manufacturing process diagrams of a multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 6 is a cross-sectional view of the multilayer printed wiring board according to Embodiment 1 of the present invention.

FIG. 7 (A) is a perspective view of the multilayer printed wiring board according to Embodiment 1 and FIG. 7 (B) is an explanatory diagram illustrating an enlarged part of the multilayer printed wiring board.

FIG. 8 (A) is a perspective view of the multilayer printed wiring board according to a modified example of Embodiment 1 and FIG. 8 (B) is an explanatory diagram illustrating an enlarged part of the multilayer printed wiring board.

FIG. 9 is a cross-sectional view of a multilayer printed wiring board according to a modified example of Embodiment 1 of the present invention.

FIG. 10 is a cross-sectional view of a multilayer printed wiring board according to Embodiment 2 of the present invention.

FIG. 11 is a cross-sectional view of a multilayer printed wiring board according to Embodiment 3 of the present invention.

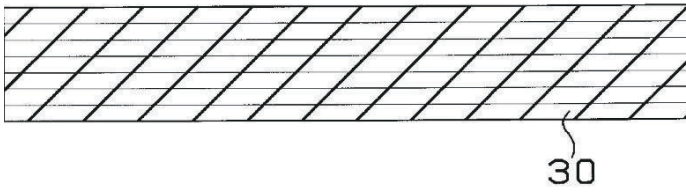
FIG. 12 is a cross-sectional view of a multilayer printed wiring board according to Embodiment 4 of the present invention.

DESCRIPTION OF REFERENTIAL NUMERALS AND CODES

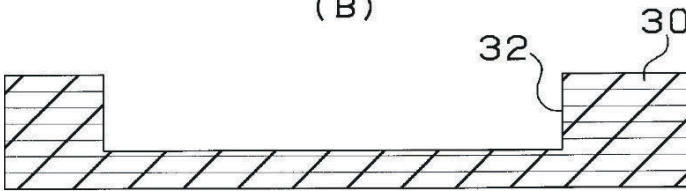
- 20. IC chip (electronic component)
- 24. Pad
- 30. Core substrate
- 32. Recessed part
- 36. Resin layer
- 38. Transition layer
- 50. Interlayer resin insulating layer
- 58. Conductor circuit
- 60. Via
- 70. Solder resist layer
- 76. Solder bump (terminal)
- 90. Daughter board (external board)
- 96. Conductive connection pins (terminals)
- 97. Conductive adhesive
- 120. IC chip (electronic component)
- 150. Interlayer resin insulating layer
- 158. Conductor circuit
- 160. Via

[FIG. 1]

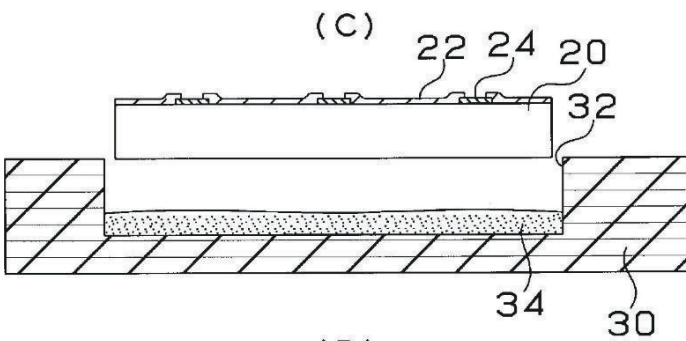
(A)



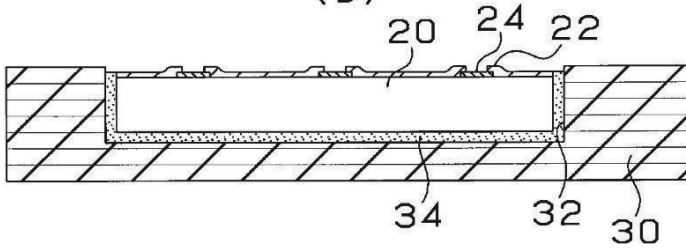
(B)



(C)

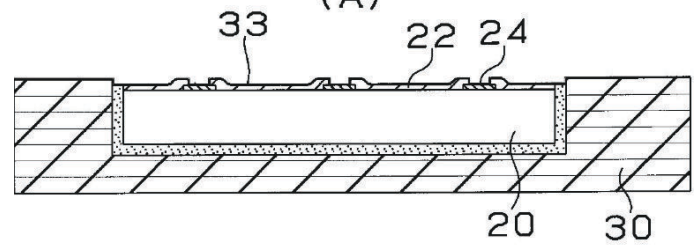


(D)

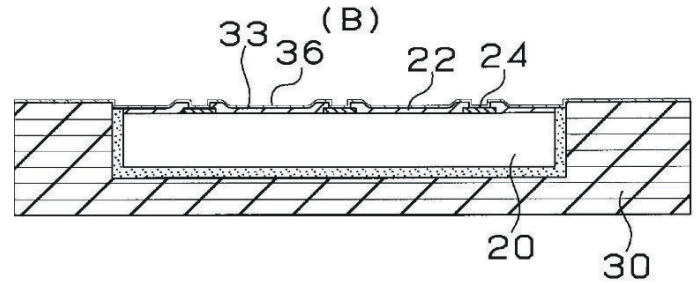


[FIG. 2]

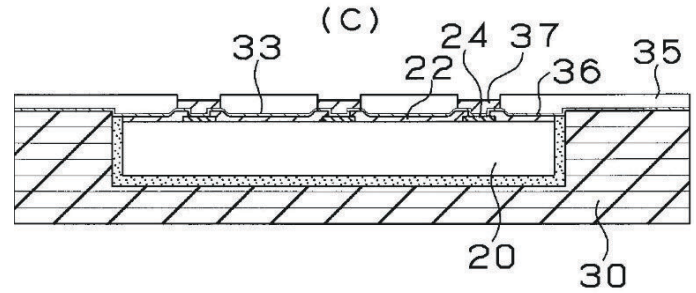
(A)



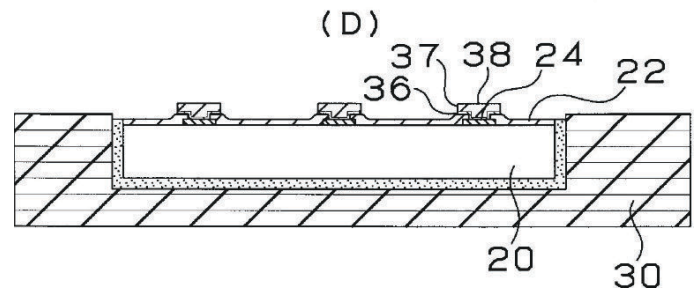
(B)



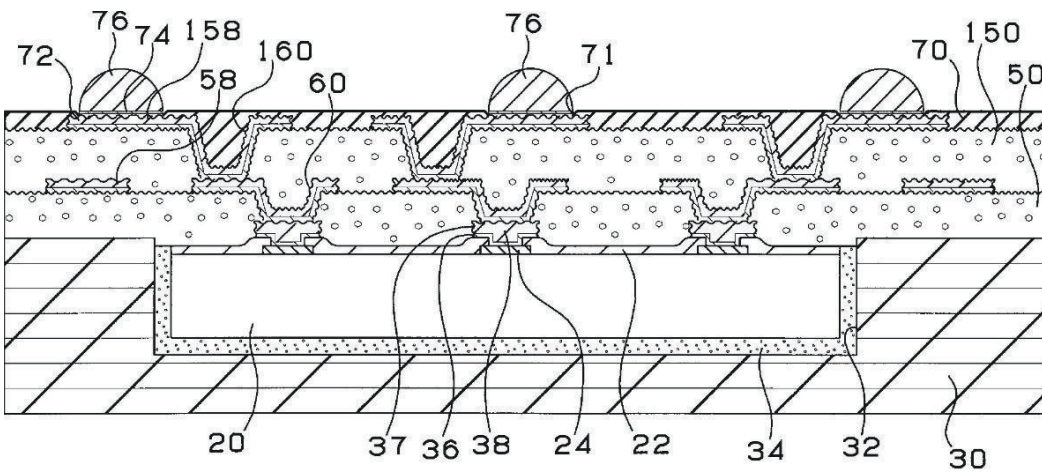
(C)



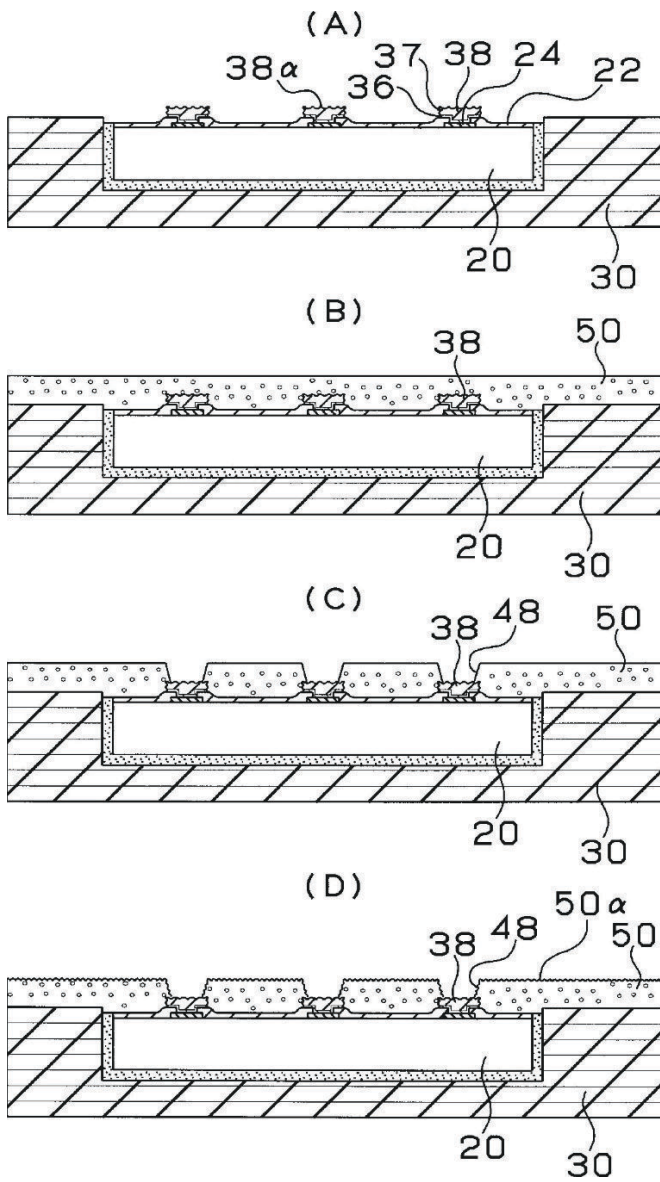
(D)



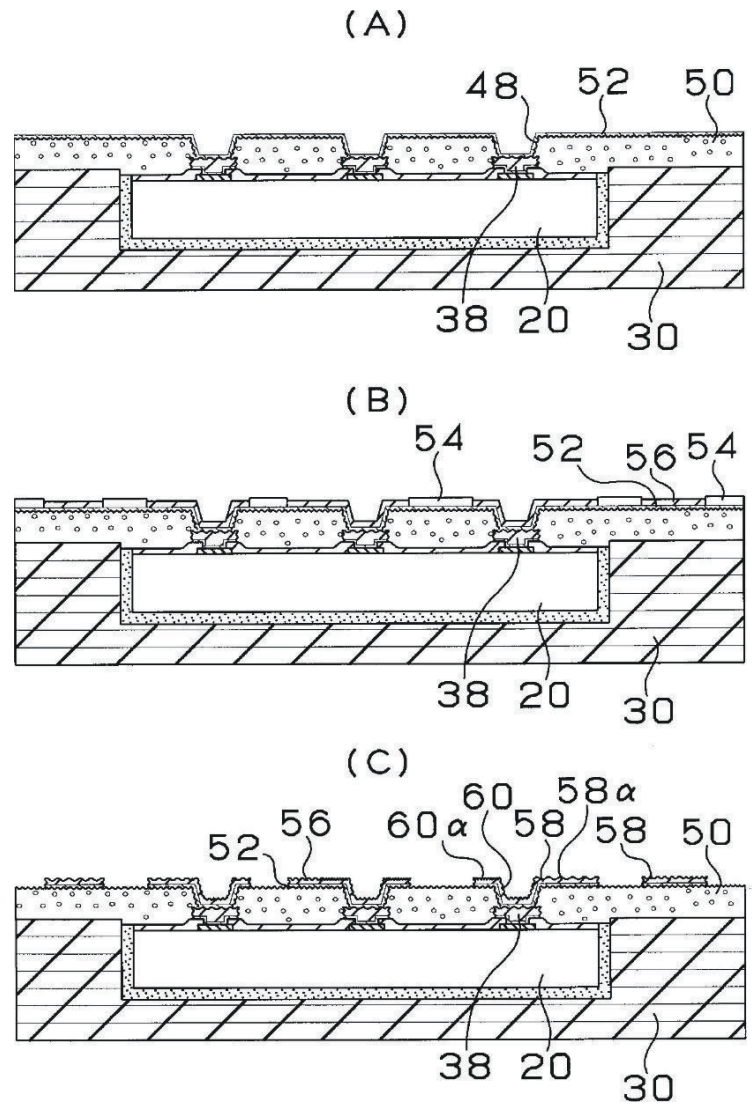
[FIG. 6]



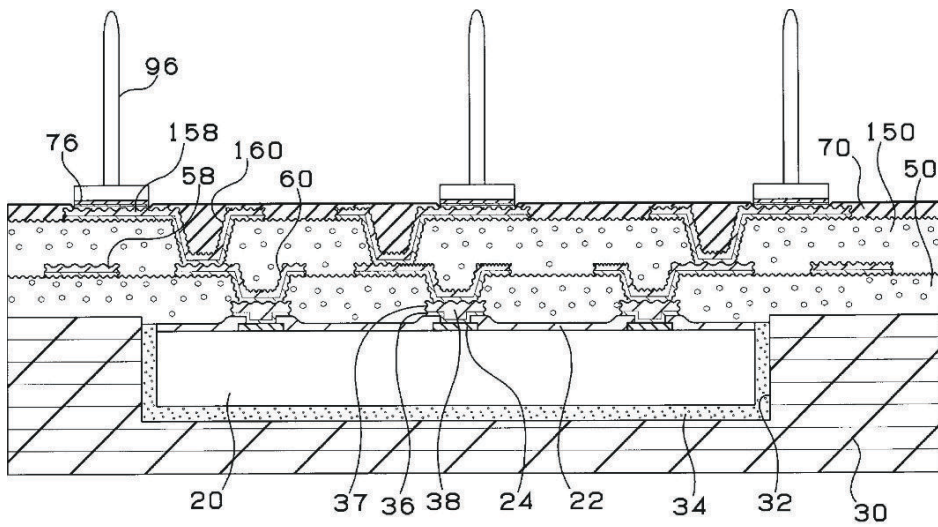
[FIG. 3]



[FIG. 4]

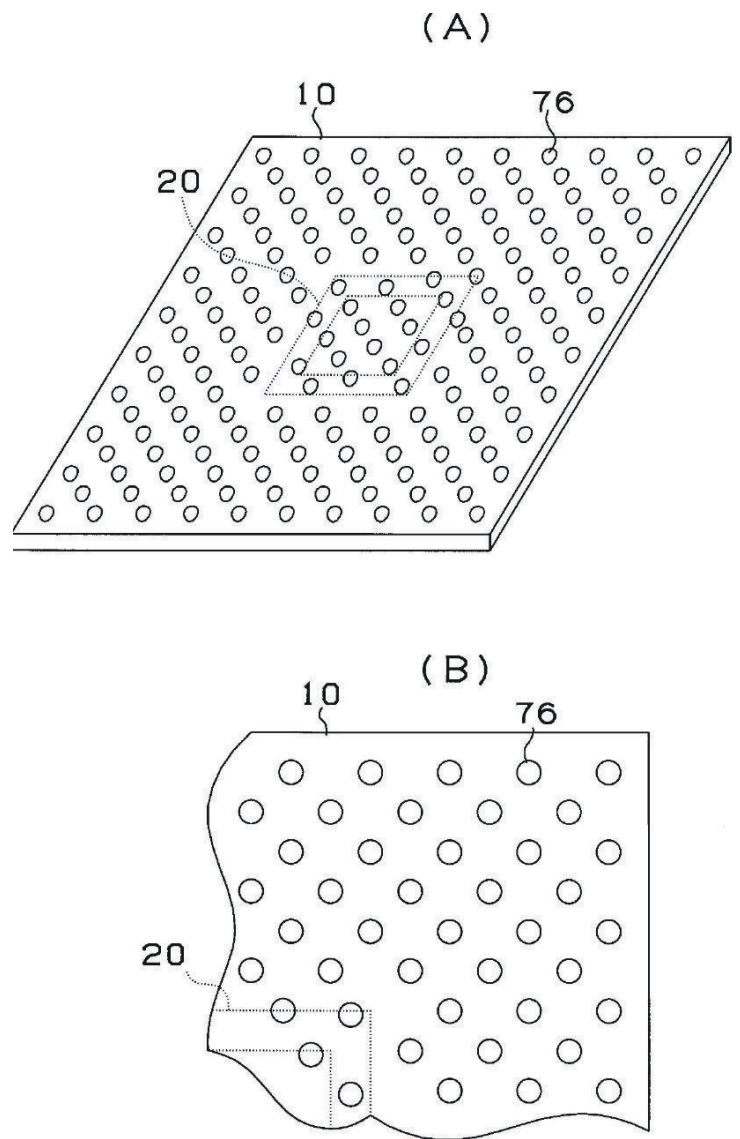
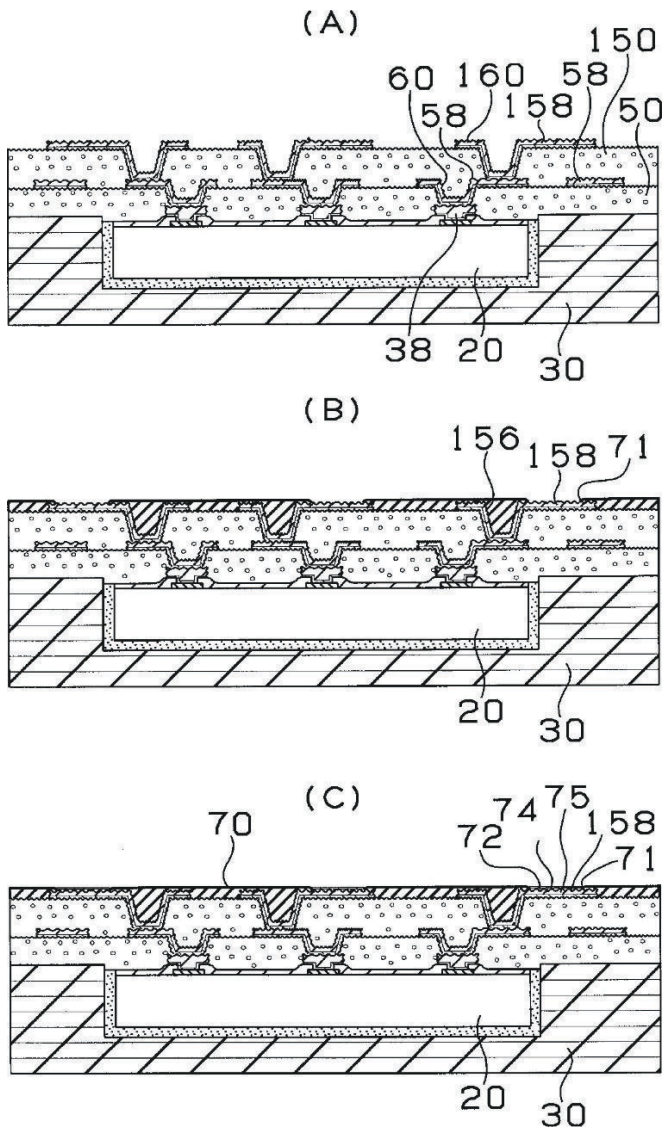


[FIG. 9]

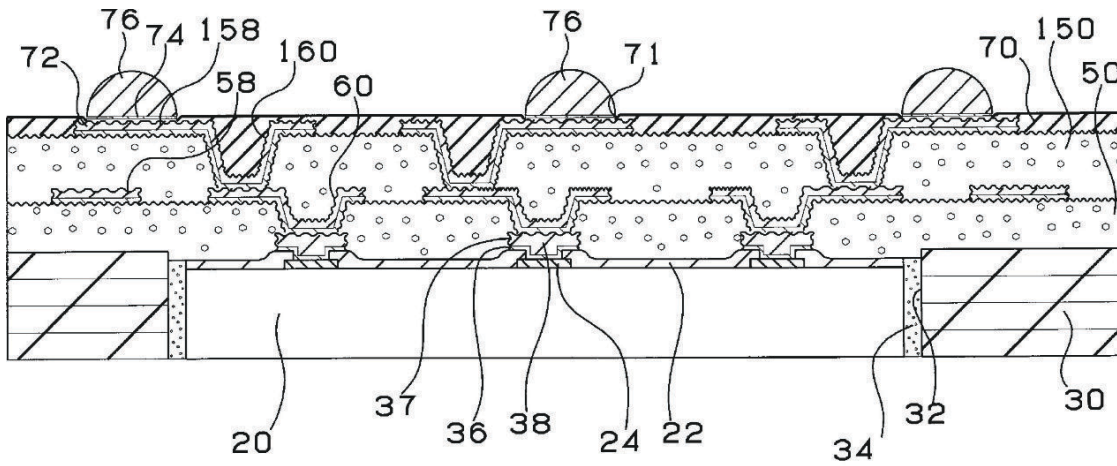


[FIG. 3]

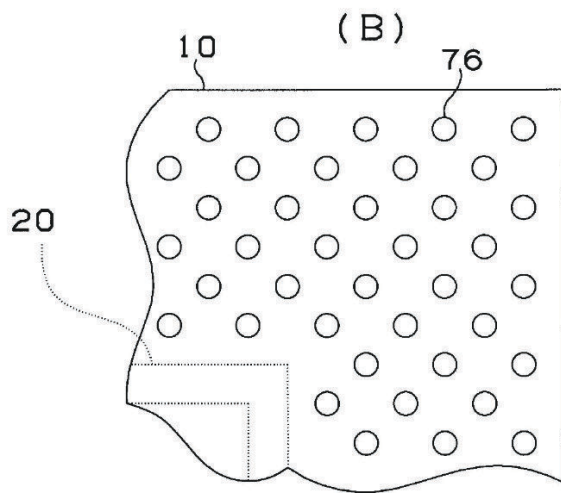
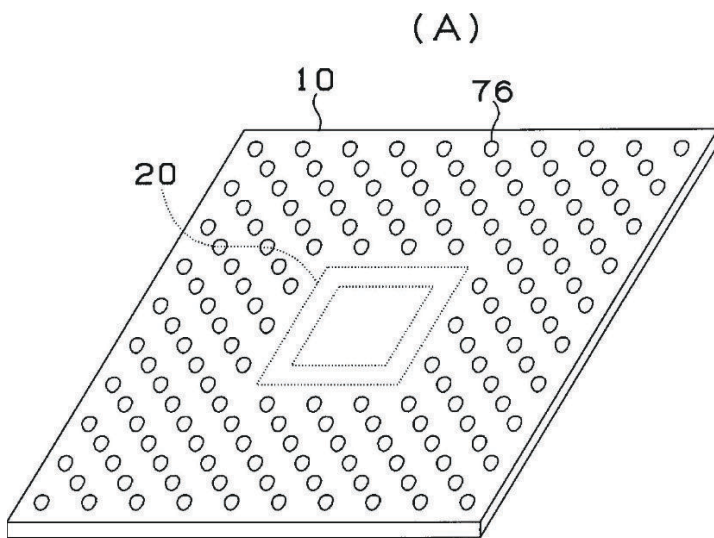
[FIG. 4]



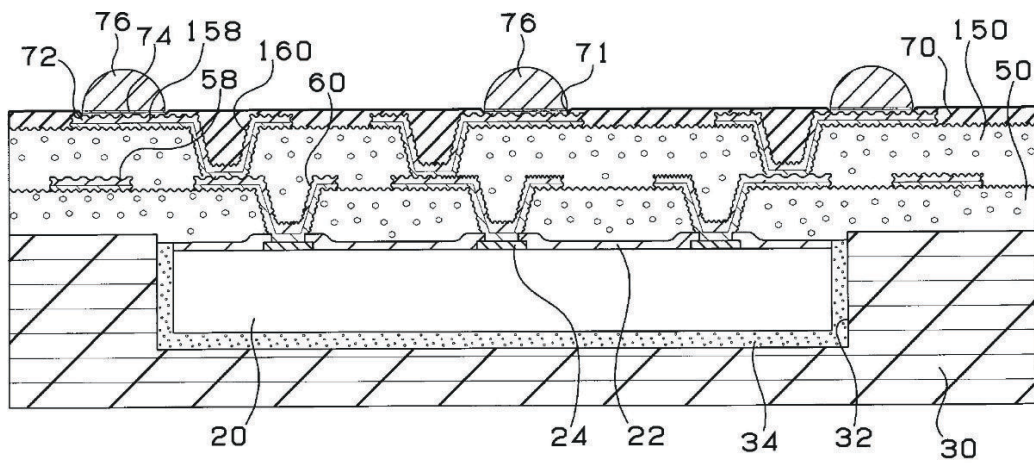
[FIG. 10]



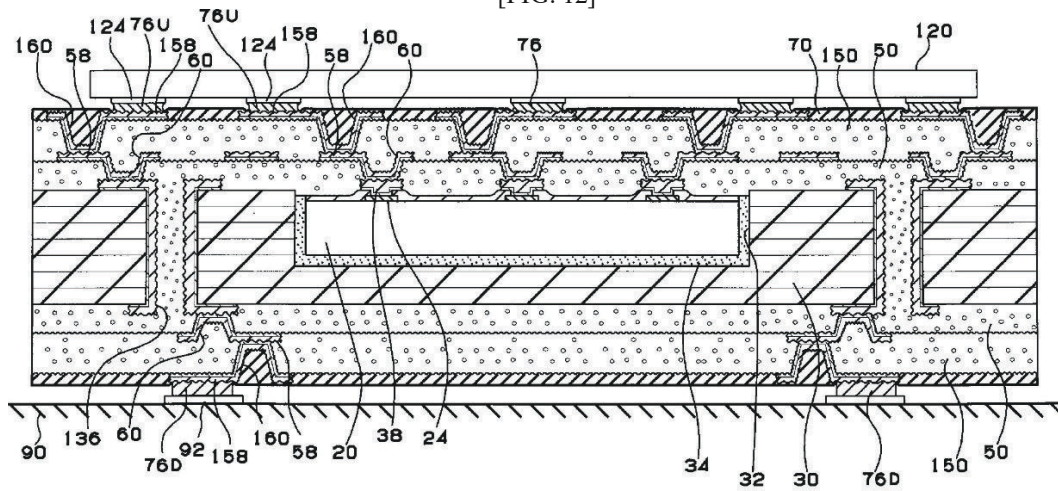
[FIG. 8]



[FIG. 11]



[FIG. 12]



Continued from first page

(51) Int. Cl⁷

ID number

FI

Theme Code (Reference)

H 01 L 23/12

F

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F term (reference) 5E346 AA43 FF45 HH07