

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title: METHOD FOR EMBEDDING A COMPONENT IN A BASE

DECLARATION OF DR. DEAN NEIKIRK

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 5, 2025

By: 

Dean Neikirk, Ph.D.

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I, Dr. Dean Neikirk, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of Apple (“Apple” or “Petitioner”). I understand that Apple is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 7,732,909 (“the ’909 patent”) (APPLE-1001). I have been asked to provide my independent analysis of the ’909 patent in light of the prior art publications cited below.

2. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’909 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’909 patent.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

3. I have summarized in this section my educational background, career history, and other qualifications relevant to this matter. I have also included a current version of my curriculum vitae as Appendix A.

4. I am currently an emeritus Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin, holding the Emeritus Cullen Trust for Higher Education Professorship in Engineering. I

received a B.S. in Physics and Mathematics from Oklahoma State University in 1979, an M.S. in Applied Physics from the California Institute of Technology in 1981, and a Ph.D. in Applied Physics from the California Institute of Technology in 1984. Until January 2021, I was a tenured professor and endowed chair in the Cockrell School of Engineering at the University of Texas at Austin, where I have been a member of the engineering faculty since 1984. From 1992 to 2020 I held the Cullen Trust for Higher Education Professorship in Engineering at the University of Texas. From 2014 to 2020 I was the Associate Dean of Graduate Studies where I oversaw graduate student services for over 78 doctoral programs and 116 master's degree programs. I have also served as the Graduate Advisor of the Department of Electrical and Computer Engineering (ECE) at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, and the Secretary of the General Faculty at UT-Austin.

5. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in IC fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, IC packaging, multi-chip modules, electromagnetics, computer aided design methods for circuit simulation, sensors of all sorts, and micro-

electromechanical systems. In recognition of my research and classroom teaching accomplishments, I received the 1984-85 Engineering Foundation Faculty Award from the University of Texas at Austin Engineering Foundation Advisory Council, the 1985-90 General Motors Foundation Centennial Teaching Fellowship, the 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, the 1990-1992 Temple Foundation Endowed Faculty Fellowship, the 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, the 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, and the 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching. In recognition of my service to the University of Texas at Austin I also received the 2015 University of Texas at Austin Civitatis Award.

6. My research over the last thirty-five years has concentrated heavily in the areas of optical systems, microelectronics, semiconductor devices, IC fabrication, device packaging, multi-chip modules, and new sensors. This research work has been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well as research on device packaging, the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging

arrays. My research related to the development of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization venture between The University of Texas and two outside startup companies.

7. My early research was in the interaction of light with optically active materials, including color centers in crystals for use as light emitters. Each of my academic degrees involved significant studies in solid state physics, semiconductor devices, device packaging, electrical engineering, electronic systems, electromagnetics, optics, radio frequency systems, and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, and optical systems. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and quasioptical imaging antenna arrays, including research on integrated-circuit fabrication, semiconductor devices, integrated circuits, antennas, sensors, and IC packaging. I designed and fabricated the first monolithic integrated-circuit imaging antenna array for use at wavelengths in the far infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. For this work on the first high resolution focal plane antenna array for use at wavelengths between 0.1 mm and 1 mm I was awarded the 1984 Marconi International

Fellowship Young Scientist Award “for contributions to the development of millimeter wave integrated circuits especially in the area of detectors and imaging arrays.” In recognition of my early research efforts, I received the 1985–1986 IBM Corporation Faculty Development Award, and the 1986 National Science Foundation Presidential Young Investigator Award.

8. As represented by the publications listed in my CV, I have extensive experience with microelectronics, semiconductors, and IC fabrication.

9. I am a lifetime senior member of the Institute of Electrical and Electronics Engineers (IEEE) and served as Associate Editor for Solid State and VLSI Electronics, IEEE Transactions on Education from March 1991 through October 1994.

10. Through my work on electronic systems and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

11. I have also co-authored over 250 technical papers in international journals and conferences and presented over 30 invited lectures and professional society presentations. My publications have addressed technologies such as integrated circuits for antenna arrays, multilayer interconnection lines for highspeed digital integrated circuits, determining conductor loss in transmission lines, optical and electromagnetic devices for infrared detection, RF oscillator

circuits, memory-switching double-barrier quantum-well diodes circuits, RF and infrared detection circuits, and other topics related to semiconductor and IC fabrication.

12. A detailed list of my other professional activities, memberships, and speaking engagements is included in my CV, which is attached as Appendix A.

13. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '909 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time. Based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the 2000s and specifically during the time of the alleged invention of the '909 patent. Indeed, I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

III. LEGAL PRINCIPLES

14. I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

A. Anticipation

15. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

16. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (the so-called critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Obviousness

17. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention

(“POSITA”), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.

18. The '909 patent was filed May 4, 2007 as a continuation of Application No. 10/502,336 (now U.S. Pat. No. 7,294,529 (“the '529 patent”)), which claims priority to PCT/FI03/00065 filed January 28, 2003, and further to Finish Application No. 20020191 filed January 31, 2002. APPLE-1001, Cover, APPLE-1002, 74, 107. For purposes of my analysis here, I have applied a date of January 31, 2002 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than January 31, 2002.

19. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or

motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the predictable combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

20. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. I have followed this approach in my analysis.

21. I have also been informed that, according to 35 U.S.C. § 112, a patent claim may lack written description if the specification and earlier-filed priority applications fail to describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of

the application and that the patentee invented what is claimed. I understand that even if a description would render obvious a claimed invention, such obviousness is not sufficient to satisfy the written description requirement for that claim. I have also been informed that a patent claim may be indefinite if, read in light of the specification and prosecution history, it fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

22. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have used the date of January 31, 2002 for reasons explained in ¶ 18 (above) and ¶¶ 24-25 (below). However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the early to mid-2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

23. A person of ordinary skill in the art at the time of the '909 patent (a "POSITA") would have had at least a Bachelor's degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. In view of the pertinent prior art discussed herein, my analysis would be the same applying a slightly higher or lower level of skill.

24. I have used January 31, 2002 as the point in time from which my analysis from the perspective of a POSITA is based, but my analysis would be similar even if the date was slightly earlier or later.

V. MATERIALS CONSIDERED

25. My analyses set forth in this declaration are based on my experience in the field of IC packaging and multi-chip modules. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the early- to mid-2000s and specifically during the time before the alleged priority date (January 31, 2002) for the '909 patent, and I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

26. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the critical date for the '909 patent; my own knowledge and experiences gained from my work experience in the field; and my experience in working with others, including teaching and advising others in the field. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- | | | |
|-----|------------|--|
| 27. | APPLE-1001 | U.S. Patent No. 7,732,909 (“the ’909 patent”) |
| 28. | APPLE-1002 | U.S. Patent No. 7,732,909 File History |
| 29. | APPLE-1004 | Certified Translation of JP Application Publication
2001-339165A (“Sakamoto”) |
| 30. | APPLE-1005 | U.S. Patent Application Publication No.
2002/0175402 (“McCormack”) |
| 31. | APPLE-1006 | U.S. Patent No. 6,489,685 (“Asahi”) |
| 32. | APPLE-1007 | U.S. Patent Application Publication No.
2001/0030059 (“Sugaya”) |
| 33. | APPLE-1008 | U.S. Patent Application Publication No.
2002/0020898 (“Vu”) |
| 34. | APPLE-1009 | U.S. Patent No. 7,294,529 (“the ’529 Patent”) |
| 35. | APPLE-1010 | RESERVED |
| 36. | APPLE-1011 | Certified Translation of JP Patent No. 3207174
(“Hayashi”) |
| 37. | APPLE-1012 | Certified Translation of JP Patent Application
Publication No. 2002-016327 (“Eiji”) |
| 38. | APPLE-1013 | U.S. Patent No. 6,335,571 (“Capote”) |
| 39. | APPLE-1014 | U.S. Patent No. 6,297,551 (“Dudderar”) |
| 40. | APPLE-1015 | U.S. Patent No. 6,404,052 (“Kurita”) |

41. APPLE-1016 Certified Translation of JP Patent Application
Publication No. 2001-068624A (“Imoto”)
42. APPLE-1017 Certified Translation of PCT Publication No. WO
00/09623 (“Watanabe”)
43. APPLE-1018 U.S. Patent No. 4,179,802 (“Joshi”)
44. APPLE-1019 U.S. Patent No. 5,608,262 (“Degani”)
45. APPLE-1020 U.S. Patent No. 5,321,210 (“Kimbara”)
46. APPLE-1021 U.S. Patent No. 5,146,674 (“Frankeny”)
47. APPLE-1022 JP Patent Application Publication No. 2001-
339165A (“Sakamoto”)
48. APPLE-1023 JP Patent No. 3207174 (“Hayashi”)
49. APPLE-1024 JP Patent Application Publication No. 2002-
016327 (“Eiji”)
50. APPLE-1025 JP Patent Application Publication No. 2001-
068624A (“Imoto”)
51. APPLE-1026 PCT Publication No. WO 00/09623 (“Watanabe”)
52. APPLE-1027 Certified Translation of JP Patent Application
Publication No. 2001-156457 (“Takayama”)
53. APPLE-1028 JP Patent Application Publication No. 2001-
156457 (“Takayama”)

54. APPLE-1029 U.S. Patent No. 5,745,984 (“Cole”)
55. APPLE-1030 R. Aschenbrenner, A. Ostmann, U. Beutler, J. Simon and H. Reichl, “Electroless nickel/copper plating as a new bump metallization,” in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 18, no. 2, pp. 334-338, May 1995, doi: 10.1109/96.386270
56. APPLE-1031 W. W. Flack, Ha-Ai Nguyen, E. Capsuto and C. McEwen, “Characterization of a thick copper pillar bump process,” 2007 12th International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces, San Jose, CA, USA, 2007, pp. 208-213
57. APPLE-1032 Xiang Dai, M. V. Brillhart, M. Roesch and P. S. Ho, “Adhesion and toughening mechanisms at underfill interfaces for flip-chip-on-organic-substrate packaging,” in IEEE Transactions on Components and Packaging Technologies, vol. 23, no. 1, pp. 117-127, March 2000
58. APPLE-1033 D. Suryanarayana, T. Y. Wu and J. A. Varcoe, “Encapsulants used in flip-chip packages,” in IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 16, no. 8, pp. 858-862, Dec. 1993
59. APPLE-1034 U.S. Patent Application Publication No. 2001/0033889 (“Bhatt”)

60. This declaration refers to selected portions of the cited references for the sake of brevity. These references are examples. It should be understood that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties. Of course, I have also considered the claims of the '909 patent. The following table provides a quick sheet enumerating claim elements for ease of reference:

Claim Element	Language
[1pre]	A circuit board, comprising:
[1a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[1b]	conductive patterns on both sides of the insulating material layer;
[1c]	at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;
[1d]	conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

[1e]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[2]	The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.
[3]	The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.
[4]	The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.
[5]	The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.
[6]	The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.
[7]	The circuit board of claim 6, wherein the filler material contains epoxy.
[8pre]	The circuit board of claim 1, wherein
[8a]	said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and
[8b]	the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

[9]	The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
[10]	The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.
[11pre]	The circuit board of claim 1, wherein
[11a]	said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and
[11b]	said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.
[12pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:
[12a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[12b]	conductive patterns on both sides of the insulating material layer;
[12c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and
[12d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

[13]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.
[14]	The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.
[15]	The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.
[16]	The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.
[17pre]	The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise
[17a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[17b]	conductive patterns on both sides of the insulating material layer,
[17c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[17d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

[18]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.
[19pre]	The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises
[19a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[19b]	conductive patterns on both sides of the insulating material layer,
[19c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[19d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[20pre]	The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises
[20a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[20b]	a conductive pattern on the insulating material layer,
[20c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and

[20d]	contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[21]	The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.
[22]	The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.
[23]	The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.
[24]	The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
[25]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.
[26]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.
[27pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising:
[27a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;

[27b]	conductive patterns on both sides of the insulating material layer;
[27c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and
[27d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and
[27e]	at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.
[28]	The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.
[29]	The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.
[30]	The circuit board of claim 1, comprising a metal plate above the microcircuit.
[31]	The circuit board of claim 1, comprising a metal plate below the microcircuit.
[32]	The circuit board of claim 1, comprising a metal plate above and below the microcircuit.
[33]	The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

VI. OVERVIEW OF THE '909 PATENT

A. Summary of the '909 Patent

61. The '909 patent relates to a method for embedding a component in a base, such as a circuit board, and an electronic module having electronic components embedded in a base. APPLE-1001, Title, Abstract. As illustrated the annotated FIG. 4D below, the electronic module includes a baseboard and a hardened insulating polymer layer, together forming an insulating material layer; conductive patterns on both sides of the insulating material layer; integrated circuit components (e.g., microcircuits 18) embedded inside the baseboard and between the two conductive pattern layers; each component having contact areas on a first surface; the first surface being against the hardened insulating polymer layer; contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the components and the conductive patterns on the lower side of the insulating material layer. APPLE-1001, FIG. 4D, cls. 1, 12.

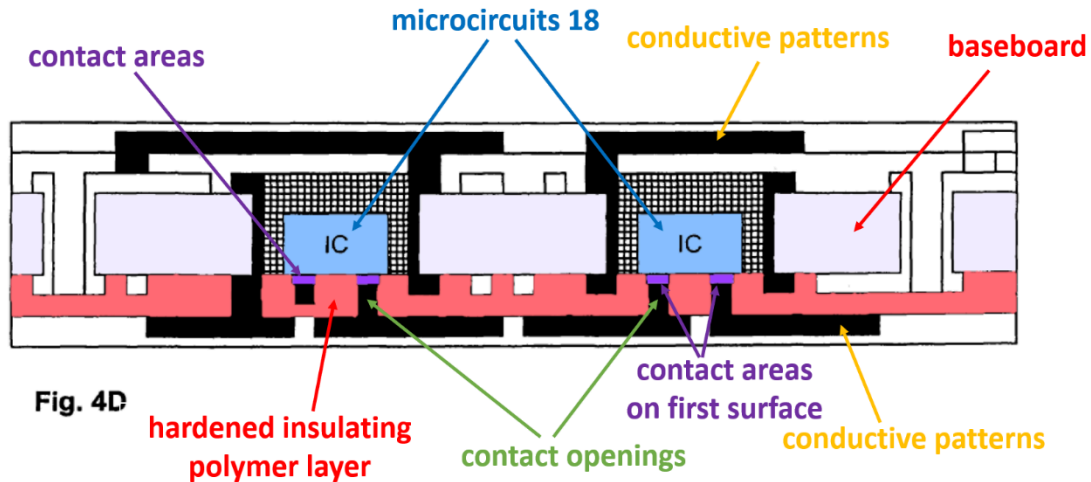


Fig. 4D

APPLE-1001, FIG. 4D (Annotated)

62. The '909 patent additionally describes growing conductive material on the sidewalls of the holes where microcircuits 18 are embedded, in order to create protection against electromagnetic interference (EMI) around the microcircuits. *E.g.*, APPLE-1001, 3:61-4:9 (“In stage [1]C, metal is grown into the through holes made in stage B. ... The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallization can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. ... Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste.”), 8:34-41 (“The invention also permits electromagnetic protection to be made around the component embedded in the base. This is because the method of FIG. 1 can be modified in such a way that the holes 6 depicted in stage 1E can be made in

connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components”), 8:64-66, cl. 1.

63. The '909 patent further describes copper in the contact openings containing “at least one of electrochemically deposited copper and chemically deposited copper.” *Id.*, cls. 1, 12, 6:21-25 (“the feed-throughs (holes 13) are first of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 14 is increased by electrochemical deposition.”).

B. Prosecution History of the '909 Patent

64. The '909 patent issued on June 8, 2010 from a continuation of application No. 10/502,336 (now U.S. Pat. No. 7,294,529 (“the '529 Patent”)), which claims priority to PCT/FI03/00065, filed January 28, 2003, which further claims priority to Finish application No. 20020191 filed January 31, 2002.

65. During prosecution, only a single office action was issued, rejecting then pending claims 1-6, 8-10, 12-25, 28, 30 and 31 under 35 U.S.C. §102(b) as being anticipated by Vu et al. (2002/0020898) (“Vu”). Then pending claims 11 and 27 under 35 U.S.C. § 103(a) were also rejected as being unpatentable over Vu, in view of an official notice stating, “formation of plated Cu layers using both

[chemical and electrochemical] methods in formation of a seed layer and a bulk Cu layer was known prior to applicant's invention." APPLE-1002, 53-58.

Additionally, in the same office action, then pending claims 7, 26 and 29 were objected to but otherwise were considered allowable. Specifically, the original claims 7 and 26 each recite "conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit," and the original claim 29 recites "a metal foil below at least one of the microcircuits." *Id.*, 53-58, 100-104. In response to the office action, applicant amended the independent claims to incorporate the features of claims 7 and 26, and added new claim 32 to recite the features of claim 29. *Id.*, 43-45 ("Claim 1 has been amended to incorporate the features of Claim 7, Claim 14 has been amended to incorporate the features of Claim 26 (with Claims 7 and 26 consequently canceled). Further, new Claim 32 has been added to recite the features of Claim 29.")

66. However, I note that the original independent claim 14 (now independent claim 12) was apparently not correctly amended in response to the office action, as it failed to incorporate all the features of original claim 26 that the Applicant said it did. *Compare id.*, 36 *with id.*, 101-104. Particularly, current claim 12 does not recite "conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit," which was the allowable subject matter recited in the original claim 26. APPLE-1001, cl. 12. Thus, current

claim 12 from the amended original 14 that is missing key subject matter, and its dependent claims 13-25 for at least the same reason, appear to fail to overcome the § 102(b) rejections based on Vu as indicated in the office action. APPLE-1002, 53-58. A notice of allowance was subsequently issued with this apparent error, which also ended prosecution prematurely without application of what is, in my opinion, the more pertinent prior art such as Asahi, Hayashi, Dudderar, Eiji, Joshi and Watanabe. APPLE-1002, 18-21. Based on my knowledge and experience, and my review of the publications I discuss in more detail below, I do not agree that the '909 patent claims are patentable over the prior art. Those of skill in the art were aware of electronic modules that shared the same structural design and the known use of conductive material on the sidewalls of the holes for accommodating electronic components to achieve protection against electromagnetic interference (EMI).

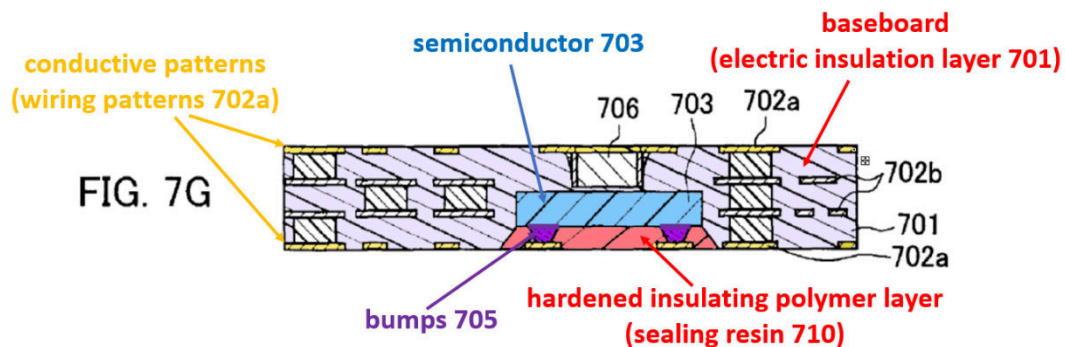
VII. OVERVIEW OF THE CITED REFERENCES

A. Overview of Asahi (APPLE-1006)

67. U.S. Patent No. 6,489,685 to Asahi is titled “Component Built-In Module and Method of Manufacturing the Same.” APPLE-1006, Face. Asahi was filed on January 3, 2002 and patented on December 3, 2002.

68. Asahi is generally directed to “a component built-in module in which an electronic component such as a semiconductor and/or a circuit component is

provided inside an electric insulation layer, and to a method for manufacturing the same.” APPLE-1006, 1:8-12; *see also*, Title, Abstract, 3:44-46. For example, FIG. 7 reproduced below shows Asahi’s Seventh Embodiment where the component built-in module includes an electric insulation layer 701, wiring patterns 702a (and 702b), and a semiconductor 703 embedded in electric insulation layer 701. *Id.*, 15:50-17:44; *see also*, 6:33-9:17 (First Embodiment), 9:18-11:25 (Second Embodiment), 11:26-12:51 (Third Embodiment), 17:55-18:13 (Eighth Embodiment), FIG. 8.



APPLE-1006, FIG. 7F (Annotated)

69. Asahi explains that “wiring patterns [] are made of a material having an electric conductivity, and a metal foil, a conductive resin composition, a lead frame obtained by processing a metal plate, etc. may be used, for instance. The use of a metal foil or a lead frame allows fine wiring patterns to be formed by etching or the like, thereby facilitating the formation of the same. ... A copper foil is preferable particularly, since it has low cost and has a high electric conductivity. ...

The use of the lead frame allows a metal having a low electric resistance to be formed thick.” *Id.*, FIG. 7, 7:23-65.

70. In Asahi, wiring patterns with a subscript “a” refer to those exposed to the outside of the component built-in module such as wiring patterns 702a on both surfaces of the module; wiring patterns with a subscript “b” refer to those embedded in the module (e.g., wiring pattern 702b). *Id.*, 7:56-65 (“This applies to the descriptions of second to fourth and seventh to tenth embodiments.”), FIG. 7; *see also*, 6:33-37, 8:66-9:4 (“It should be noted that the present embodiment [First Embodiment] is described by taking as an example the case where the wiring patterns 102a on both surfaces of the component built-in module are not embedded inside the electric insulation layer; however, the wiring patterns on at least one surface of the layer may not necessarily be exposed, but may be covered with the electric insulation layer.”), 16:13-43, 17:35-36 (“providing a component built-in module that has the wiring patterns 702a on surfaces thereof”).

71. Bumps 705 (in one example, “stud bumps” are used) may be used on an active surface of the semiconductor to form electric connections between semiconductor 703 and “wiring patterns 702a” on a surface of the insulation layer 701, while alternative mounting processes such as “soldering” and “flip chip bonding” can also be used. *Id.*, FIG. 7, 16:43-66; *see also*, 8:9-10 (“bump 105”), 10:33-45 (various mounting techniques, e.g., “a bump 205 formed by gold wiring

bonding, or a bump formed by soldering, may be formed on the semiconductor 203 side”), 11:47-54, 13:27-29 (“bumps 405”), 14:25-27 (“bumps 505”), 15:9-12 (“bumps 605”), 17:59-61 (“bumps 805”).

72. Asahi describes the use of “a sealing resin” which can be “[a]n underfill resin used for ordinary flip chip bonding,” to “prevent a gap from being formed” between the semiconductor and the wiring patterns. *Id.*, 10:45-53; *see also*, 8:2-6, 11:56-65, 16:52-62, 17:55-18:13, FIGS. 7 (showing sealing resin 710 between semiconductor 703 and wiring patterns 702a), 8. According to Asahi, “[a]n effect of preventing the semiconductor 703 from being damaged and improving the reliability can be expected with the use of the sealing resin 710.” *Id.*, 16:59-62.

73. The electric insulation layer “preferably is made of a mixture of a filler and an insulating resin” which contains polymer. *Id.*, 3:11-38 (“the insulating resin preferably contains at least one selected from an epoxy resin, a phenol resin, a fluorocarbon resin, a cyanate resin, a polytetrafluoroethylene (PTFE) resin, a poly(phenylene oxide)(PPO) resin, and a polyphenylether (PPE) resin.”). Further, Asahi describes curing the electric insulation layer “upon making the electric connection” using heat and pressure. *Id.*, 5:35-46, 10:62-67 (“In the case where a thermosetting resin is used as an insulating resin, the thermosetting resin in the electric insulation layer 201 is cured by heating after pressing, whereby the electric

insulation layer 201 in which the semiconductor 203 is embedded can be formed in a plate form.”), 15:65-67 (“the electric insulation layer 701 may be made of an insulating resin, a mixture of a filler and an insulating resin, or the like”), 17:33-34 (“By heating after pressing, the electric insulation layers 701 are cured”).

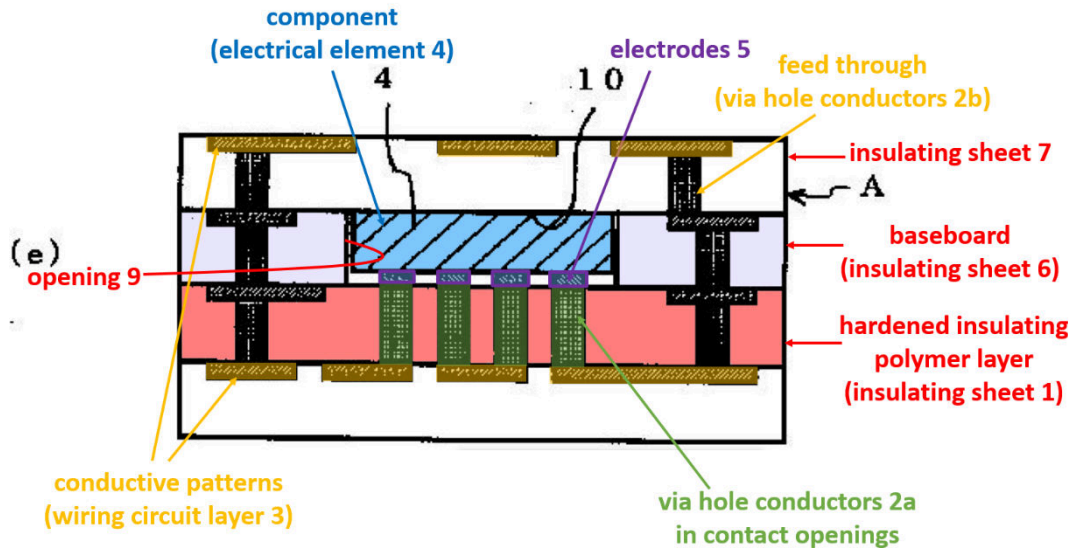
74. In addition, Asahi discloses a multi-layered structure with electronic components, preferably semiconductor bare chips, in each layer, to achieve “high density and improved function of circuit components.” *E.g.*, APPLE-1006, 1:14-42, 3:44-49 (“In each of the first and second component built-in modules, the electronic component preferably is a semiconductor bare chip”), 12:63-65 (“semiconductors 403 as electronic components ... and circuit components 406 as electronic components”), FIG. 4 (showing a multi-layered structure with three substructure layers having electronic components in each layer), FIGS. 7-10 (each showing a multi-layered structure with at least two layers having electronic components in each layer).

75. The multi-layered structure was a well-known common feature in the component built-in devices by the Critical Date, to achieve benefits such as high density, high performance, and short-distance wiring. *E.g.*, APPLE-1007 (corroborating prior art), [0004], [0034]; APPLE-1004 (corroborating prior art), [0005], [0055]; APPLE-1005 (corroborating prior art), Abstract, FIGS. 11-13; APPLE-1008(corroborating prior art), FIG. 13; APPLE-1016, FIGS. 5-9.

B. Overview of Hayashi (APPLE-1011)

76. JP Patent No. 3207174 to Hayashi is titled “Electrical Element Mounted Wiring Board and Manufacturing Method of Same.” APPLE-1011, Face. Hayashi was filed on February 1, 1999 and issued on September 10, 2001. *Id.*

77. Hayashi describes “a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate, and to a manufacturing method for such a wiring substrate.” APPLE-1011, [0001]-[0003]; *see also*, Title, [Claim 1], [Claim 2], [0007], [0027], [0038], [0041], FIG. 1(e). The electrical element includes “a semiconductor element.” *E.g., id.*, [0001]-[0003], [0027], [0038] (“a silicon semiconductor memory chip” as an example of the semiconductor element), [0041] (“IC element”). The annotated FIG. 1(e) below shows electrical element 4 in an opening 9 formed in an insulating sheet 6 which is laminated directly above insulating sheet 1 and below insulating sheet 7. *Id.*, [0027]-[0028] (“so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7”); *see also*, [0039] (“an opening slightly larger than the size of the electrical element was formed by punching an insulating sheet b”), [0040].



APPLE-1011, FIG. 1(e) (Annotated)

78. A “wiring circuit layer 3,” which is a “circuit pattern” is provided on both sides of and within the insulating layer composed of insulating sheets 1, 6, 7. *Id.*, [0024]-[0025]; *see also*, [Claim 1] (“a wiring circuit layer formed on the surface and inside of the insulating substrate”), [0009]. These wiring circuit layers are inter-connected through via hole conductors 2b in all the insulating sheets. *Id.*, [0012] (“via-holes passing through in the thickness direction are formed in the insulating sheet 1. ... general via-hole conductors 2b are also formed in addition to the via-hole conductors 2a for connecting electrical elements”), [0021], [0028], [0036]-[0038], [0041], FIGS. 1(b)-(e) (showing multiple conductive patterns of wiring circuit layer 3 on both sides of insulating sheets 1, 6 and 7, respectively, and interconnected through via hole connectors 2b). Electrodes 5 (e.g., contact pads) of the electrical element 4 are electrically connected with via-hole conductors 2a

(in insulating sheet 1), which are electrically connected to wiring circuit layer 3 on the surface of insulating sheet 1. *Id.*, [Claim 1], [Claim 2], [0008]-[0012], [0014], [0018], [0020], [0024], [0026], [0030], [0034], [0035], [0038], [0041], [0042], FIG. 1(e).

79. According to Hayashi, its insulating sheet 1 contains “a thermosetting resin with thermosetting temperature T_1 .” *Id.*, [0012]. Hayashi explains that “the thermosetting resin forming the insulating sheet is not particularly limited as long as the thermosetting resin has electrical characteristics, heat resistance, and mechanical strength as an insulating material. For example, an aramid resin, phenol resin, epoxy resin, imide resin, fluororesin, phenylene ether resin, bismaleimide-triazine resin, urea resin, melamine resin, silicone resin, urethane resin, unsaturated polyester resin, or allyl resin, etc. can be used alone or in combination.” *Id.*, [0015]. A POSITA would have recognized this as a list containing a variety of polymers. Insulating sheet 1, along with the other insulating sheets, is hardened through thermal curing. *Id.*, [Claim 1], [Claim 2], [0010], [0012], [0013], [0019], [0029], [0032], [0035], [0040].

80. Additionally, Hayashi describes that multiple layers of similar substructure of FIG. 1(e) can be laminated on top of each other to increase mounting density, these substructures are electrically connected through via hole conductors 2b and the wiring circuit layers 3 provided in each insulating sheet. *Id.*,

[0004] (desire for “high-density mounting of a plurality of electrical elements”), [0007] (“the mounting density of the elements can be increased”), [0009], [0012], [0021], [0024], [0025], [0028], [0032] (“a plurality of electrical elements can be provided by forming a plurality of void portions in the same or different layers in a multilayer wiring substrate to stow and mount the electrical elements.”), [0034] (“an electrical element mounted wiring board that can easily provide not only a single but also a plurality of electrical elements inside the wiring board, thereby reducing the size of the wiring board and increasing the mounting density of the electrical elements can be provided”), [0036]-[0038], [0041], [0042], FIGS. 1(b)-(e).

C. Overview of Dudderar (APPLE-1014)

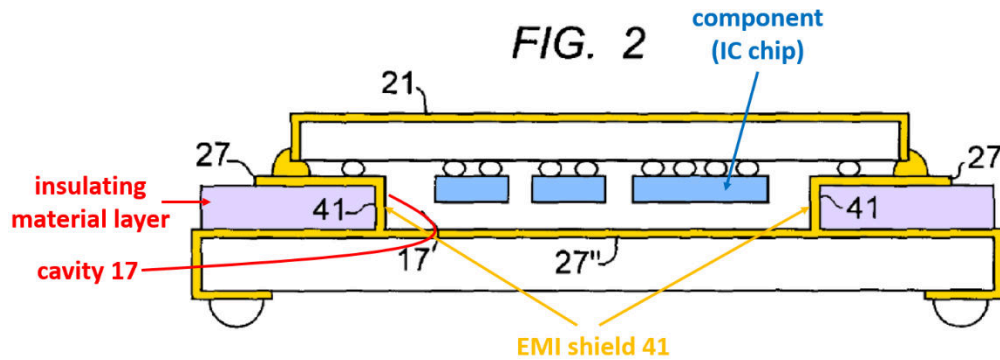
81. U.S. Patent No. 6,297,551 to Dudderar et al. is titled “Integrated Circuit Packages with Improved EMI Characteristics.” APPLE-1014, Face. Dudderar was filed on September 22, 1999 and issued as a patent on October 2, 2001. *Id.*

82. Dudderar describes “a recessed chip MCM [(multichip module)] package with integrated electromagnetic shielding,” where “[t]he surfaces of the cavity which houses the IC devices are coated with metallization.” *Id.*, Abstract. According to Dudderar, “[a]s is known, EMI is disruptive to the proper operation of circuit components located near the source of the EMI. Accordingly, there is an

identifiable need to reduce EMI.” *Id.*, 1:42-45. Dudderar explains, high frequency applications such as wireless applications and specialized computing devices are especially susceptible to EMI. *Id.*, 1:10-41.

83. To achieve reduced EMI susceptibility, Dudderar teaches providing a grounded EMI shield that surrounds a cavity in a printed circuit board for embedding semiconductor components such as integrated circuit chips. *Id.*, 1:48-63, 2:44-54 (“Referring to FIG. 1, integrated circuit devices 11, 12 and 13 are shown flip-chip bonded to multi-chip module (MCM) substrate 14. ... Substrate 16 is typically an epoxy PCB with a cavity 17 to accommodate devices 11, 12 and 13 on the MCM substrate 14 in a recessed configuration.”), 2:63-3:4 (“The upper side of the package is provided with metallization 21 ... the backside of the substrate [14], with the substrate ground plane metallization, is combined with the EMI shield. The EMI shield metallization 21 can be as thick as desired ...”), 3:49-52, 4:45-52, 5:45-46, FIG. 2, cl. 1.

84. In one embodiment of Dudderar, “[a]n alternative arrangement for the EMI shield metallization is shown in FIG. 2[,]” where “the EMI shield metallization extends along the inside wall of cavity 17 as shown at 41, and connects with the EMI cavity shield metallization 27” as in the arrangement of FIG. 1.” *Id.*, 4:45-50, FIG. 1 (reproduced below with annotation).



APPLE-1014, FIG.2 (Annotated)

D. Overview of Joshi (APPLE-1018)

85. U.S. Patent No. 4,179,802 to Joshi et al. is titled “Studded Chip Attachment Process.” APPLE-1018, Face. Joshi was filed March 27, 1978 and issued as a patent on December 25, 1979.

86. Joshi describes methods for connecting integrated circuit chips to a substrate or carrier, through metal studs (e.g., copper studs) formed on the chip or substrate using various plating methods with limited amount of solder. *Id.*, Title, Abstract, 1:6-11, 2:8-40, 3:1-3 (“copper studs ... are formed by electroplating copper”), 3:21-26, 3:52-68 (“One method of forming the studs on the substrate (or chip) is to first provide a flash coat of conductive metal (e.g., copper) on the surface thereof. ... Then the copper studs are additively plated on the exposed flash coat... the studs could be formed using any other acceptable plating process including ... using standard additive ... processing”), 4:14-34, cl. 6 (“electroplating copper in the stud areas”).

87. According to Joshi, its described interconnection method achieves “improve[d] thermal characteristics of the interconnections,” “improved chip/carrier attachment,” “improved input/output characteristics from the chip to the carrier,” “reduction in the thermal resistance between the chip and the substrate,” and improved “reliability of these interconnections.” *Id.*, 4:14-34.

E. Overview of Eiji (APPLE-1012)

88. JP Patent Application Publication No. 2002-016327 to Eiji et al. is titled “Wiring Substrate and Manufacturing Method Therefor.” APPLE-1012, Face. Eiji was filed April 23, 2001 and published January 18, 2002.

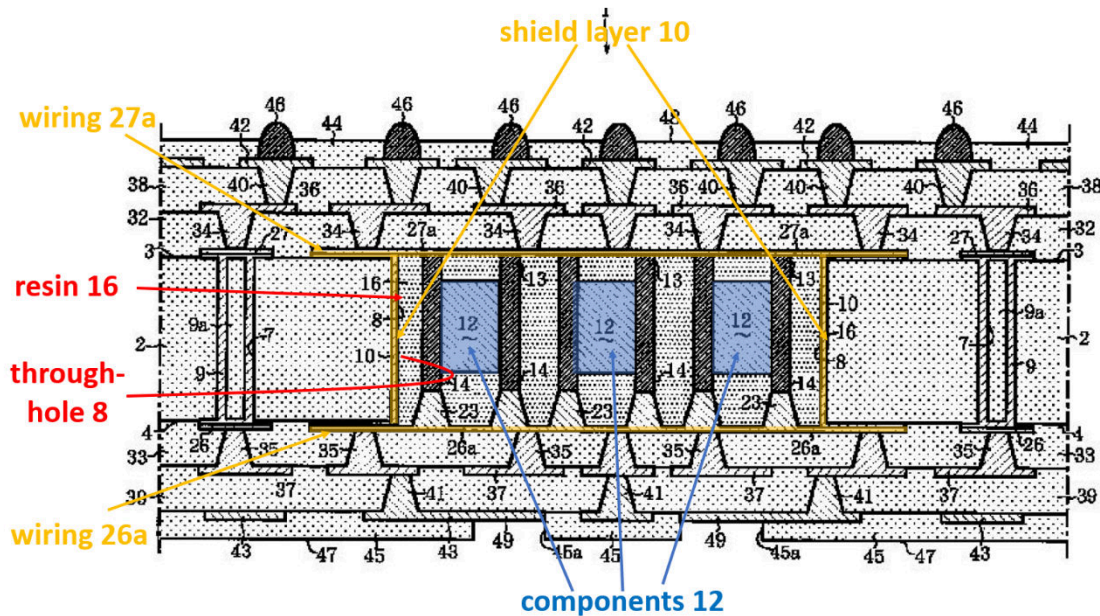
89. Eiji describes reducing EMI susceptibility of electronic components built into an insulating substrate, through a solution where “a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded[.]” *Id.*, Abstract, FIG. 1; *see also*, [0001], [0005], [0006] (“electronic components embedded in through-holes or recessed portions [of the insulating substrate] can be shielded from external electromagnetic waves, and noise generated from circuits composed of these electronic components to the outside can be reduced”), [0007], [0009], [0011]-[0012] (“an approximately 25 μm -thick shielding layer 10 is formed by copper plating on the inner surface of the outer

circumference of the through-hole 8”), [0017] (“electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8 and through-holes 7 after applying catalyst metal nuclei for plating such as Pd”), [0023], [0041]-[0042], cls. 1, 6.

90. Eiji gives examples of the electronic components including “active components such as low-noise amplifier (LNAs), transistors, semiconductor devices, and FETs, as well as SAW filters, LC filters, antenna switch modules, couplers, and diplexers, and any of the components listed above made into chip form.” *Id.*, [0006].

91. Eiji also describes filling the through-hole with a resin (e.g., resin 16), “[i]n this way, electronic components are securely embedded in through-holes or recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer.” *Id.*, [0007], [0010], [0019] (“after filling the through-hole 8 from the front surface 3 side with melted resin 16, which is primarily epoxy resin, curing is performed to hold the resin at about 100 °C for about 60 minutes. As a result, as shown in the figure, the resin 16 solidifies and each [electronic component] is embedded at a predetermined location in the through-hole 8 by the resin 16”), cls. 2, 7, FIGS. 1, 3; *see also*, [0031]. Eiji further describes wiring layers 26 and 27, “formed in the upper and lower openings to the through-hole 8.” *See e.g.*, APPLE-1012, [0011],

[0023]. These metal layers are formed from “copper foil” with thickness of more than “several 10 μm thick.” *Id.*, [0017], [0021], [0025], FIGS. 1, 4



APPLE-1012, FIG. 1 (Annotated)

F. Overview of Watanabe (APPLE-1017)

92. International Publication No. WO 00/09623 to Watanabe et al. is titled “Adhesive for Bonding Circuit Components, Circuit Board, and Method for Producing the Same.” APPLE-1017, Face. The international filing date of Watanabe is August 13, 1998, and it was published on February 24, 2000. *Id.*

93. One aspect of Watanabe describes the use of a “conductive adhesive” having conductive particles to make electrical connections between terminals (or electrodes) on a semiconductor chip (e.g., an integrated circuit (IC) chip) and on an insulating substrate where the chip is mounted. *E.g., id.*, Abstract, 1, 5, 14.

94. Watanabe explains that “[c]hip components have many connection terminals..., while printed circuit boards, polyimide and polyester-based flexible circuit boards, and other substrates have many connection terminals formed on organic insulating substrates. Organic insulating substrates with electrodes (connection terminals) corresponding to the terminals of a semiconductor chip are used as substrates for mounting chip components. The organic insulating substrate can be a laminate made by impregnating a synthetic resin film such as polyimide resin or polyester resin film, or a glass substrate such as a glass cloth or glass non-woven fabric substrate with a resin such as a polyimide resin, epoxy resin, or phenol resin and then curing the resin.” *Id.*, 14. Watanabe further explains that “[a]nother type that can be used is a multilayer wiring board having electrodes for connection to chip terminals, a surface insulating layer on which these electrodes are formed, a predetermined number of insulating layers, a predetermined number of wiring layers located between each insulating layer, and conductor holes that electrically connect predetermined electrodes and wiring layers.” *Id.*

95. Watanabe also describes that “the conductive particles can be, for example, particles of metals such as Au, Ag, Cu or solder, and a conductive layer of Ni, Cu, Au, or solder is preferably provided on a spherical polymer core material such as polystyrene. A surface layer of Su [*sic*], Au, solder, etc. can also be formed on the surface of conductive particles.” *Id.*, 12. I note that there is no

“Su” chemical element; when read in context of the preceding sentence, a POSITA would have understood as “Cu.”

VIII. GROUND 1A: CLAIMS 12-27 ARE OBVIOUS IN VIEW OF ASAHI

A. Analysis of Asahi with Respect to Claims 12-27

96. As shown in this section, Asahi renders obvious claims 12-27.

[12pre] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:

97. Asahi provides preamble [12pre] to the extent it is limiting. Asahi provides an electronic component built-in module (the recited multi-layered circuit board) that includes electronic components such as semiconductors embedded in an electric insulation layer of a wiring board and laminated on top of each other. APPLE-1006, FIGS. 4-10, 12:53-19:37. For example, Asahi’s embodiments described in FIGS. 4-10 each include a hole, cavity or recess formed in the insulating layer of a wiring board to receive an electronic component. *Id.*

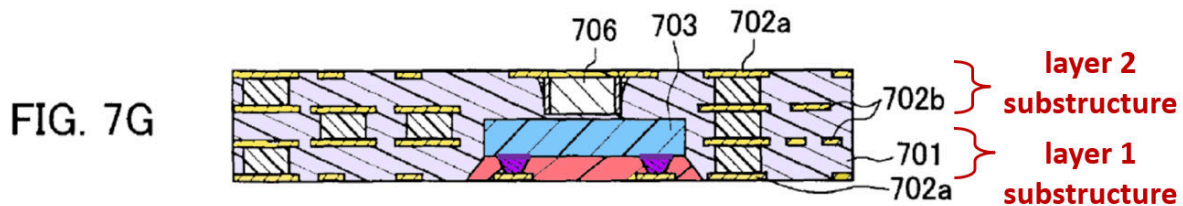
98. Asahi describes the use of “generally used wiring board” such as “a glass-epoxy substrate” for its electric insulation layer to “reduc[e] the production cost.” APPLE-1006, 3:60-65; *see also id.*, 1:23-25, 3:11-38; 14:29-30, 15:62-16:2 (“A component built-in module takes a board form, and the electric insulation layer... may contain a reinforcing material such as a glass cloth or an unwoven fabric”), cls. 11, 21. Additionally, Asahi describes “in each of the first and second component built-in modules [of a multi-layered circuit board], the electric

insulation layer in contact with the electronic component and the electric insulation layer in contact with the first inner via preferably are provided integrally[,]” such that “the two electric insulation layers have a common composition and are continuous seamlessly,” with benefits of electric insulation layers being “provided continuously without a boundary, thereby improving the reliability.” APPLE-1006, 3:66-4:7. As explained above, Asahi’s electric insulation layer of each laminated substructure has the same composition of a “generally used wiring board” such as “a glass-epoxy substrate” with “a reinforcing material such as a glass cloth or an unwoven fabric.” *Id.*; *see also supra* §VII.A. (Asahi overview). A POSITA would have understood that an unwoven fabric of glass refers to a material made by loosely arranging glass fibers without weaving them into a traditional fabric structure.

99. Asahi’s construction is like the example circuit board material described in the ’909 patent. APPLE-1001, 3:46-55 (“a suitable baseboard 1 is selected for the circuit board manufacturing process. The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, such as an FR4-type board.”). Accordingly, Asahi provides a multi-layered circuit board, including at least two circuit board substructures laminated on top of each other.

100. As a further example, Figure 7F (reproduced below) illustrates an example of Asahi’s multi-layered structure, having at least two circuit board

101. Asahi's Figure 7G, annotated below, shows the multi-layered circuit board structure after lamination has occurred. In Figure 7G, the layer 2 substructure is positioned and laminated on top of the layer 1 substructure, so as to provide at least two circuit board substructures (layer 1 substructure and layer 2 substructure) on top of each other.



APPLE-1006, FIG. 7G (Annotated)

102. The following analyses of elements [12a]-[12d] highlight how Asahi provides each of the recited elements of the “at least one of said circuit board substructures,” as demonstrated by the layer 1 circuit board substructure.

103. By the Critical Date, the multi-layered structure was a well-known common feature in component built-in devices, and the multi-layered structure was further well-known and used to achieve benefits such as high density, high performance, and short-distance wiring. *See e.g.*, APPLE-1007, APPLE-1008, APPLE-1016. A POSITA would have been well-aware of the conventional use of multi-layered structures in component built-in devices.

104. For example, Sugaya (U.S. application publication No. 2001/0030059, filed December 15, 2000), corroborates the well-known use of such structures to POSITA, and relates to a circuit component built-in module capable of mounting the circuit component with high density and having high heat releasing property and high reliability. APPLE-1007, Abstract. Sugaya explicitly describes that “[i]n recent years, with the demand for high performance and miniaturization of electronic equipment, high density, high performance and short-distance wiring of a circuit component have been desired increasingly [and a]ccordingly, a wiring substrate capable of including a high density, high-performance and short-distance wiring circuit component has been demanded.” APPLE-1007, [0004]. Sugaya describes that “[t]he formation of a multi-layer circuit may be a solution to attain a higher-density wiring substrate” to address the demand. *Id.*; *see also id.* at [0034] (“it is preferable in the configuration that the wiring substrate includes one or a plurality of circuit component built-in modules... it is possible to realize a highly reliable multilayer circuit component built-in module in which the circuit components are mounted with high density.”).

105. Sugaya describes an example circuit component built-in module having a three-layered structure. APPLE-1007, [0217], [0225] (“Although FIG. 9A shows the circuit component built-in module 900 having a three-layered structure, a structure having any number of layers can be formed depending on the

design.”). Sugaya’s FIG. 9A is reproduced below showing a three-layered structure with circuit components 908a, 908b and 908c embedded in the various substructure layers.

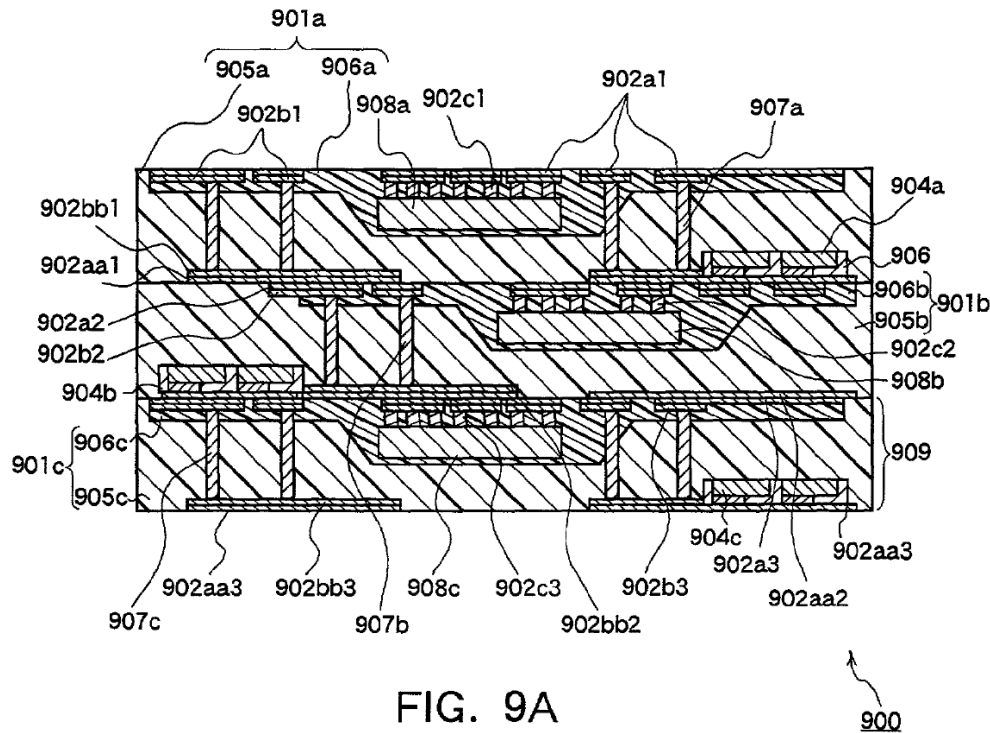


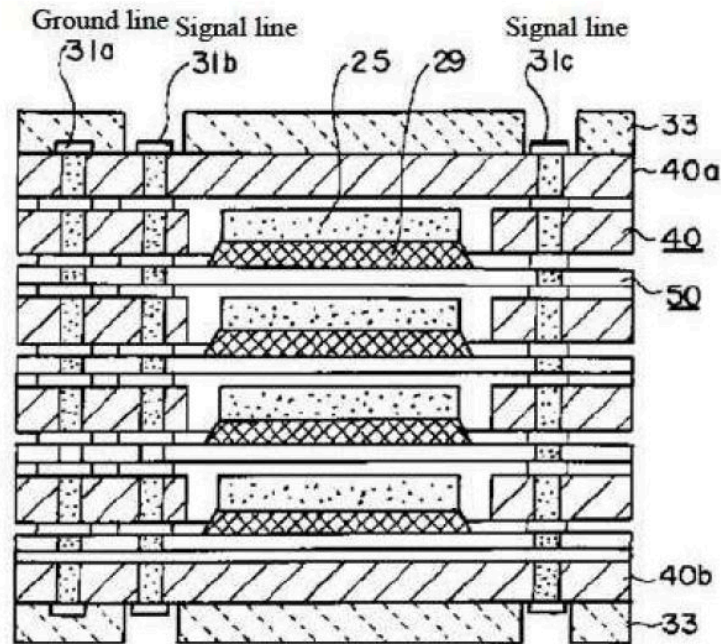
FIG. 9A

APPLE-1007, FIG. 9A

106. Another example as corroborating evidence, prior art Imoto (JP patent application publication No. 2001-068624, published March 16, 2001) describes a semiconductor device having a multi-layered structure that includes any number of layers. *See e.g.*, APPLE-1016, [0010] (“This embodiment is an example of four laminated semiconductor elements, but the number of semiconductor elements to be laminated is not limited to four, as in the present invention. Any required number of two or more can be laminated.”), FIGS. 5-9; *see also* cls. 1, 2, 8

(reciting “a plurality of wiring substrates” and “plurality of conductive via insulating substrates”). FIG. 8 below shows a four-layered structure with a semiconductor element 25 embedded in each substructure layer. *Id.*, [0021].

FIG. 8

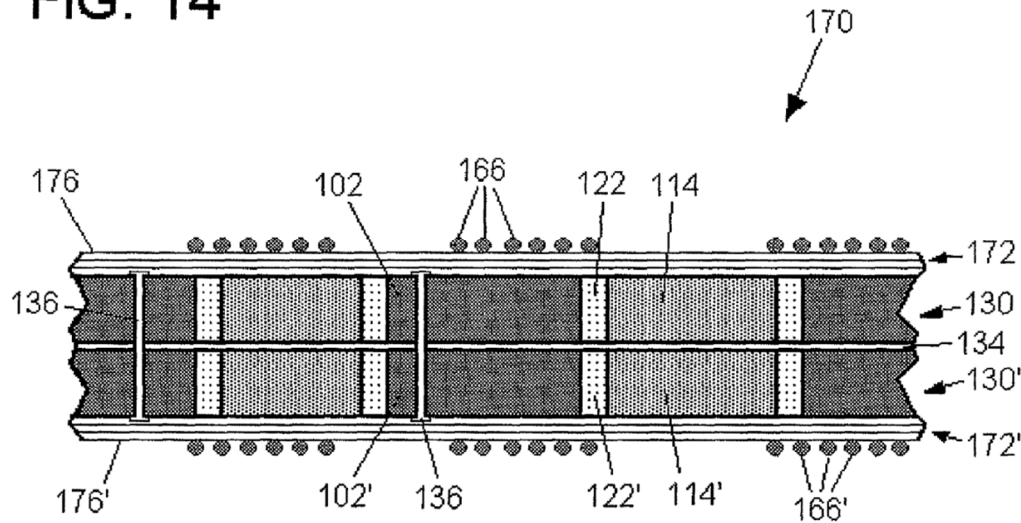


APPLE-1016, FIG. 8

107. Yet another prior art example as corroborating evidence is Vu (U.S. patent application publication No. 2002/0020898, filed on June 18, 2001 and published on February 21, 2002). APPLE-1008, Face. Vu describes microelectronic substrates with a plurality of microelectronic devices encapsulated in each microelectronic substrate core. *See e.g.*, APPLE-1008, [0019]-[0027] (short descriptions of FIGS. 9-17 showing a “dual substrate assembly”), [0045]-[0057], FIGS. 9-17. For example, Vu’s FIG. 14 reproduced below illustrates a

plurality of microelectronic devices 114 and 114' embedded in each of the two substrate layers (130 and 130') of a dual substrate assembly.

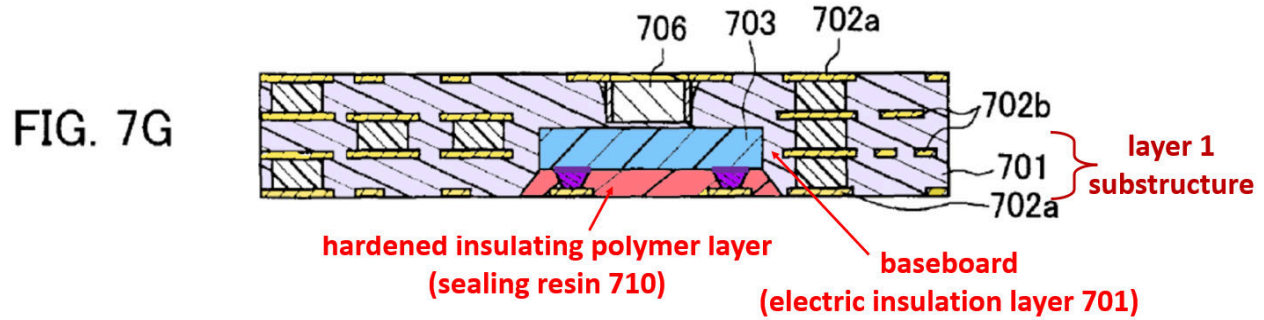
FIG. 14



APPLE-1008, FIG. 14

[12a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

108. Asahi includes a circuit board substructure (e.g., layer 1 substructure below) which provides an insulating material layer including a baseboard (e.g., unified “electric insulation layer 701” of layer 1 substructure after lamination of the various layers and components) and a hardened insulating polymer layer (e.g., “sealing resin 710”). APPLE-1006, FIG. 7, 3:66-4:7, 15:51-17:44; 16:52-62, FIGS. 7, 8; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13 *supra*, §VIII.A. (Asahi overview), analysis of [12pre].



APPLE-1006, FIG. 7G (Annotated)

109. As annotated in FIG. 7G above, the Asahi's layer 1 substructure includes electric insulation layer 701 (the recited baseboard) and sealing resin 710 (the recited hardened polymer insulating layer). For example, Asahi describes embedding electronic components, such as semiconductors and circuit components, in an electric insulation layer. APPLE-1006, Abstract, 6:33-9:17 (First Embodiment), 9:18-11:25 (Second Embodiment), 11:26-12:51 (Third Embodiment), 15:50-17:44 (Seventh Embodiment), 17:55-18:13 (Eighth Embodiment) ("the semiconductor 803 and the circuit component 806 are embedded in the electric insulation layer 801"), FIGS. 7, 8.

110. I note that Asahi's "electric insulation layer" has a composition just like that of the baseboard 1 recited by the '909 patent. *Supra*, §VIII.A, analysis of [12pre]. In particular, as described above, the '909 patent describes that the baseboard can be "a glass-fibre reinforced epoxy board." APPLE-1001, 3:46-55. Similarly, Asahi's electric insulation layer of each laminated substructure has a

composition of “a glass-epoxy substrate” with “a reinforcing material such as a glass cloth or an unwoven fabric.” APPLE-1006, 3:60-65, 15:62-16:2 (“A component built-in module takes a board form, and the electric insulation layer... may be made of an insulating resin, a mixture of a filler and an insulating resin, or the like. It may contain a reinforcing material such as a glass cloth or an unwoven fabric.”); *see also id.*, 1:23-25, 3:11-38; 14:29-30, cls. 11, 21.

111. Asahi describes the “sealing resin” (e.g., sealing resin 808) between the embedded semiconductor and the wiring patterns on the electric insulation layer, to protect the junction portions by preventing a gap from being formed between the semiconductor and the wiring patterns, thereby also preventing damage to the semiconductor, and improving reliability of the electronic module as a whole. APPLE-1006, 8:2-6, 10:45-54, 11:56-65, 16:52-62, 17:62-62 (“Junction portions between the semiconductor 803 and the wiring patterns 802a are protected with a sealing resin 808”); FIGS. 7, 8. Additionally, Asahi describes that “sealing resin 710” (the recited hardened insulating polymer layer), includes “[a]n underfill resin used for ordinary flip chip bonding,” and “may be injected between the semiconductor 703 and the wiring pattern 702a” to “prevent[] the semiconductor 703 from being damaged and improv[e] the reliability.” APPLE-1006, 16:52-62, FIGS. 7, 8; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13. Based on my knowledge and experience in the field, a POSITA would have understood and

found obvious that Asahi's underfill resin used for ordinary flip chip bonding includes polymer material and is hardened after curing, e.g., with heat. APPLE-1007 (corroborating prior art describing a circuit component built-in-module using flip chip bonding for mounting a semiconductor chip to a wiring pattern of a substrate), [0021], [0024] (the thermosetting resin used between the junction portions of the flip chip "includes at least one resin selected from the group consisting of an epoxy resin, a phenol resin, a cyanate resin and a polyphenylene ether resin because these resins are excellent in thermal resistance or insulating property"—a list of polymers), [0038] ("sealing at least a connection portion between the first wiring pattern and the circuit component with a second mixture including an inorganic filler and [the] uncured thermosetting resin"), [0041] ("curing the second mixture" between the wiring pattern and the circuit component), [0060] ("heating at the temperature where the thermosetting resin of the first and second mixtures and the conductive substance of the conductive substance of the inner via conductor are cured"), [0093] ("wiring pattern 102a is connected to the circuit component 103a by, for example, a flip chip bonding").

112. Additionally, based on my review of Asahi, a POSITA would have recognized and found obvious that the underfill resin is a hardened insulating polymer based on Asahi's express description of resin materials. For example, Asahi already describes its electric insulation layer as "made of a mixture of a filler

and an insulating resin,” and “the insulating resin preferably contains at least one selected from an epoxy resin, a phenol resin, a fluorocarbon resin, a cyanate resin, a polytetrafluoroethylene (PTFE) resin, a poly(phenylene oxide)(PPO) resin, and a polyphenylether (PPE) resin,” which a POSITA would have recognized as a list containing polymers. APPLE-1006, 3:11-38. Asahi also describes the importance of “selecting an appropriate insulating resin material,” so that “it is possible to improve a heat resistance, an electric insulation, and high frequency characteristics.” *Id.* Based on my knowledge and experience in the field, a POSITA would have been motivated to use a similar polymer material for the sealing resin to match the physical properties of the electric insulation layer that interfaces with the sealing resin, to achieve similar desired characteristics.

113. Based on my knowledge and experience in the field, a POSITA would have been motivated to utilize similar polymer material for the sealing resin to achieve similar desired characteristics as those described by Asahi – namely, improved heat resistance, electric insulation and optimized high frequency characteristics. *See supra*, § VIII.A, analysis of [12pre] (describing that the electric insulation layer is made of glass-epoxy containing “a reinforcing material such as a glass cloth or an unwoven fabric”). Additionally, a POSITA would have been motivated to utilize a similar polymer material for the sealing resin as Asahi described in order to further avoid stresses due to mismatch in “a heat

conductivity, a coefficient of linear expansion, a dielectric constant, etc.” between the sealing resin and the surrounding electric insulation layer. *Supra*, §VII.A.

(Asahi overview); APPLE-1006, 3:14-16; APPLE-1013, 2:1-6 (corroborating prior art, describing “underfilling the air gap between the chip and the substrate completely with a solid underfill encapsulant material that consists of a composite of polymer and an inorganic filler”). For example, a POSITA would have recognized that doing so would have further enhanced the reliability of Asahi’s electronic module by avoiding stresses due to mismatch in “a heat conductivity, a coefficient of linear expansion, a dielectric constant, etc.” between the sealing resin and the surrounding electric insulation layer. APPLE-1006, 3:14-16; APPLE-1007 (corroborating prior art), [0031] (“it is preferable in the configuration of the circuit component built-in module of the present invention that the coefficient of linear thermal expansion of the second mixture is in between the coefficient of the circuit component and the coefficient of the first mixture [having the circuit component incorporated therein], because the second mixture that intervenes between the circuit component and the first mixture serves as a relaxing substance for thermal stress.”); APPLE-1013 (corroborating prior art), 2:1-6 (“another approach to fatigue life involves underfilling the air gap between the chip and the substrate completely with a solid underfill encapsulant material 104 that consists of a composite of polymer and an inorganic filler and that has a thermal expansion of

20---30 ppm/° C. and an elastic modulus of 2-20 GPa.... Underfilling the chip with a subsequently cured encapsulant has been shown to reduce solder joint fatigue failure caused by thermal expansion mismatch between the chip and the substrate. ... The cured encapsulant reduces the fatigue cycling of the solder joints by virtue of the relative stiffness, or high modulus, of the underfill material in conjunction with the strong solid contact made between the underfill material, the semiconductor chip, the solder joints, and the underlying printed circuit.”).

114. Asahi describes that materials like the polymer materials used for the electric insulation layer are “cured by heating after pressing, whereby the electric insulation layer 201 in which the semiconductor 203 is embedded can be formed in a plate form.” APPLE-1006, 10:62-67; *see also id.*, 5:35-39 (“in each of the first and second methods, the electric insulation layer is cured upon making the electric connection”). Based on my knowledge and experience in the field and my review of Asahi, a POSITA would have recognized, and at least found obvious, from Asahi’s description that the sealing resin is thus hardened, including through a curing process by heating of a suitable material “used for ordinary flip chip bonding,” such that the semiconductor embedded in the electric insulation layer and sealing resin “can be formed in a plate form,” and to effectuate Asahi’s objectives of the sealing resin (e.g., to prevent a gap between the semiconductor and the wiring patterns, prevent damages to the semiconductor, and improve

reliability). APPLE-1006, 10:62-67. This is consistent with the '909 patent's description of hardening a polymer layer through curing. APPLE-1001, 5:32-35 ("The polymer film 7 is hardened with the aid of curing. Curing generally comprises a heat treatment, but the process can also employ some treatment other than heat to harden the polymer.").

[12b] conductive patterns on both sides of the insulating material layer;

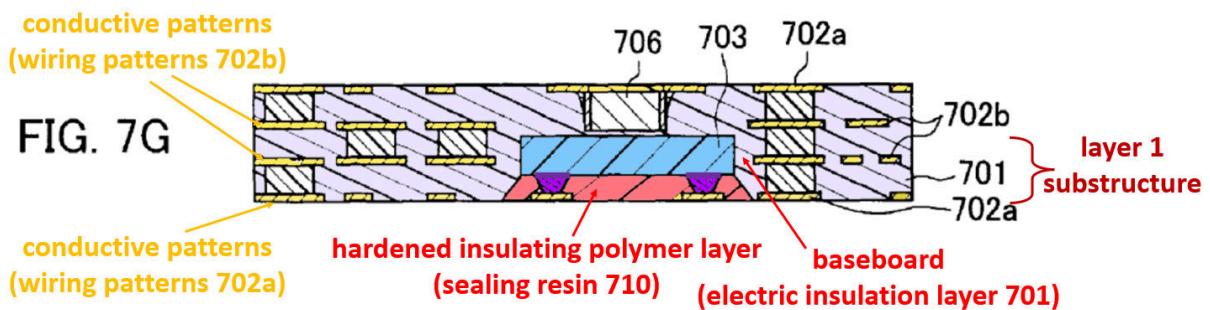
115. Asahi provides element [12b]. Asahi includes conductive patterns (e.g., conductive wiring patterns 702a and 720b) on both sides of the insulating material layer. For example, Asahi describes conductive wiring patterns 702a at the lower side (i.e., on the lower surface of the component built-in module) and at least one layer of wiring patterns 702b on an upper side of the layer 1 substructure (the recited conductive patterns on both sides of the insulating material layer).

Supra, §VIII.A, analysis of element [12a]; APPLE-1006, FIG. 7. Asahi describes "first wiring patterns in a plurality of layers that are laminated with the electric insulation layer being interposed therebetween," and at least one electronic component embedded in the electric insulation layer is mounted on any one of such first wiring patterns in the plurality of layers. APPLE-1006, Abstract, 1:67-2:3. For example, Asahi describes in the Eighth Embodiment, "wiring patterns 802a" are provided on the surfaces of the module shown in FIG. 8, and the semiconductor

803 is connected to the wiring patterns 802a via bumps 805. APPLE-1006, 17:55-63.

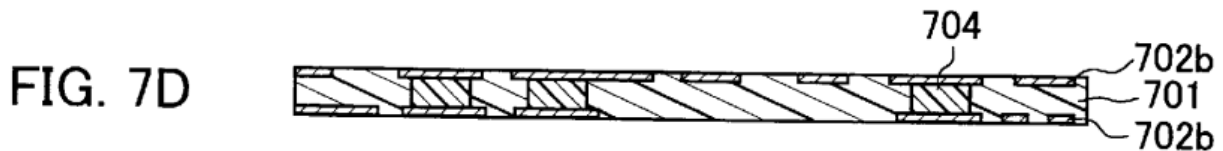
116. I note that Asahi's "wiring patterns" in electrical connection with various components and conductive vias are made of conductive material(s) and have "patterns," thus are conductive patterns, as claimed. *Id.*, 3:39-43 ("the first wiring patterns preferably are made of at least one selected from a metal foil, a lead frame, and a conductive resin composition. This allows a fine wiring pattern having a low electric resistance to be formed.").

117. The annotated FIG. 7G below illustrates this configuration, with wiring patterns 702a and 702b (the recited conductive patterns) on both sides of the insulating material layer that forms the layer 1 circuit board substructure composed of electric insulation layer 701 and sealing resin 710. In particular, wiring patterns 702b are formed at an upper side of the insulating material layer that forms the layer 1 circuit board substructure, and wiring patterns 702a are formed at a lower side of the insulating material layer of the substructure.



APPLE-1006, FIG. 7G (Annotated)

118. As shown in FIG. 7D, the wiring pattern 702b on the lower surface of the “electric insulation layer 701 provided with the wiring patterns 702b on both of its surfaces,” once laminated in the multi-layer stack of FIG. 7G, provides wiring patterns on the upper side of the layer 1 circuit board substructure, as illustrated in FIG. 7G (shown above). APPLE-1006, FIG. 7, 16:13-21, 17:12-14.

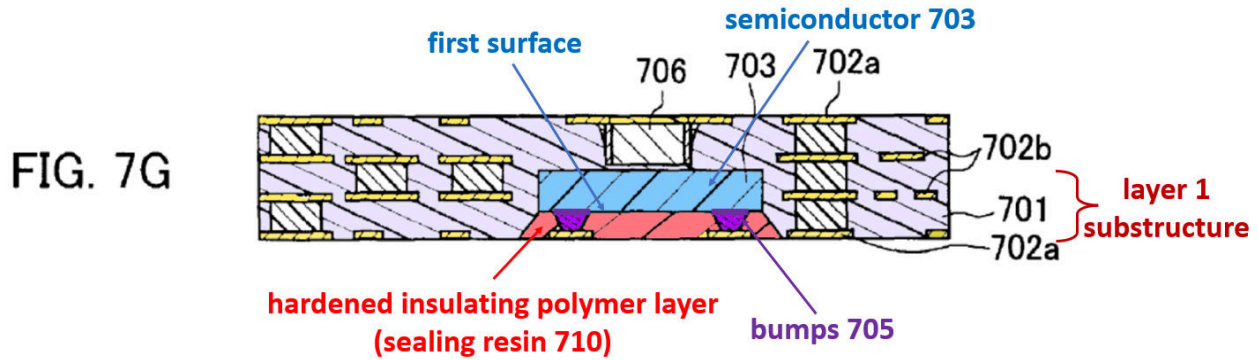


APPLE-1006, FIG. 7D

119. The wiring patterns, including wiring patterns 702a and 702b, are “made of a material having an electric conductivity, and a metal foil, a conductive resin composition, a lead frame obtained by processing a metal plate, etc. may be used.” APPLE-1006, 7:23-26. Accordingly, Asahi’s wiring patterns 702a and 702b are conductive patterns, as claimed. APPLE-1006, FIG. 7, 16:39-17:44 (In parallel, semiconductor 703 is mounted on “the wiring patterns 702a on the [lower] surface[]” of the insulating material layer of the layer 1 circuit board substructure.)

[12c] at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and

120. Asahi provides element [12c]. Asahi, e.g., layer 1 substructure, includes at least one microcircuit (e.g., “semiconductor 703”) embedded in the insulating material layer (as I previously discussed for element [12a]), the embedded microcircuit having contact areas (e.g., bumps 705) on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer (e.g., sealing resin 710), the at least one microcircuit being inside the insulating material layer in a hole in the baseboard (e.g., electric insulation layer 701) and having the first surface against the hardened insulating polymer layer. For example, as I previously discussed, Asahi describes a “semiconductor 703” that is embedded in the insulating material layer of the layer 1 circuit board substructure. *Supra*, §§VII.A. (Asahi overview), VIII.A, analysis of element [12a]; APPLE-1006, FIG. 7, 3:44-46, 15:62-17:40 (“By pressing and heating, the semiconductor 703 ... [is] embedded in the electric insulation layers 701”). The below annotated FIG. 7G illustrates this configuration.



APPLE-1006, FIG. 7G (Annotated)

121. Based on my knowledge and experience in the field, a POSITA would have understood Asahi's description of semiconductor 703 to provide a microcircuit. I note that, a POSITA would have understood that semiconductors (e.g., semiconductor 703) in devices having "high density" circuitry such as "large scale integrated circuits (LSIs)" provide a microcircuit, as microcircuits are miniaturized electronic circuits that contain a network of interconnected semiconductor devices (e.g., transistors and diodes) and passive components (e.g., resistors, inductors, and capacitors), on a small substrate. APPLE-1006, 1:32-42.

122. Additionally, Asahi's semiconductor 703 has a first surface with contact areas thereon (e.g., a semiconductor die's pads on its active surface), where conductors such as bumps (e.g., bumps 705) are formed to provide electrical connections between the semiconductor 703 and wiring patterns 702a. APPLE-1006, 16:39-66. I note that Asahi describes "stud bumps 705" as an example (e.g., in the Seventh Embodiment, and Asahi also describes "bumps" in general for

forming connections between the semiconductors and wiring patterns)¹; *see also*, *id.*, 8:9-10 (“a bump 105”, analogous to 705), 10:44-45 (“bump 205 and the conductive adhesive may be used in combination”), 11:47-54 (305 can be a conductive copper adhesive), 13:27-29 (“bumps 405”), 14:25-27 (“bumps 505”), 15:9-12 (“bumps 605”), 17:59-61 (“bumps 805”).

123. The semiconductor 703 is inside the material layer positioned in a cavity or hole (e.g., “hole 712” in electric insulation layer 701). APPLE-1006, 17:4-24; FIGS. 7F-7G. As shown in FIG. 7G above, the first surface of semiconductor 703 (i.e., the bottom surface of the semiconductor) is positioned so as to be against sealing resin 710 (the recited hardened insulating polymer layer). *Supra*, §VIII.A, analysis of element [12a]; APPLE-1006, FIG. 7, 16:39-66.

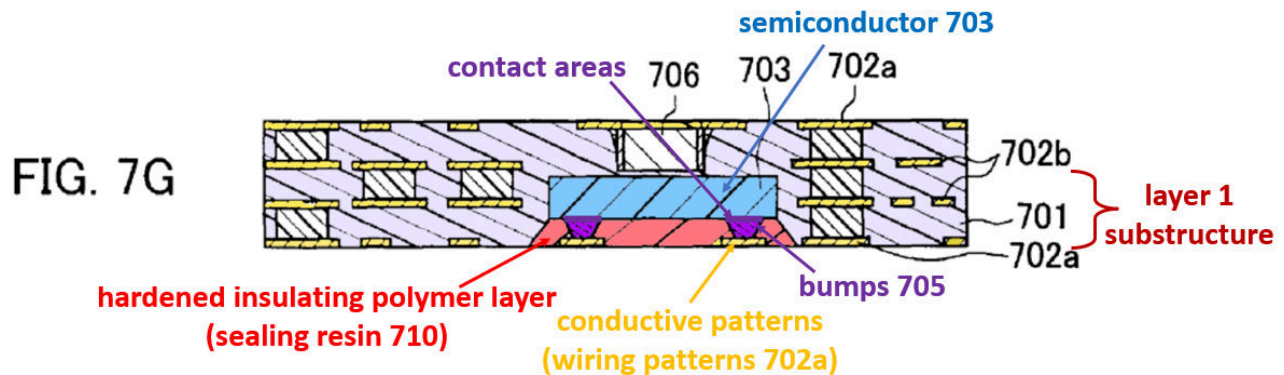
124. Accordingly, Asahi provides the features of claim element [12c].

¹ Asahi refers to the bumps providing electrical connection between the semiconductor and wiring pad as “stud bumps” with regard to the embodiment of FIGS. 7A-G.

[12d] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

125. Asahi provides element [12d]. Asahi's multi-layered circuit board has, in its layer 1 substructure as I previously discussed, contact openings in the hardened insulating polymer layer (e.g., hardened sealing resin 710) and copper (e.g., bumps 705) in the contact openings for forming electrical contacts between the contact areas (e.g., flat die pads) of the microcircuit (e.g., semiconductor 703) and at least one of the conductive patterns (e.g., wiring patterns 702a), wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper. *Supra*, §VIII.A., analysis of [12pre]. For example, Asahi describes contact openings formed in the hardened sealing resin 710 to accommodate bumps (e.g., bumps 705) or the like. As I previously discussed in the analysis of element [12c] (§VIII.A), bumps 705 form electrical contacts between the contact areas of semiconductor 703 (the recited microcircuit) and wiring patterns 702a (the recited at least one of the conductive patterns). APPLE-1006, 17:59-63 ("The semiconductor 803 and the circuit component 806 are connected via bumps 805 and via solder 807, respectively, with the wiring patterns 802a. Junction portions between the semiconductor 803 and the wiring patterns 802a are protected with a sealing resin 808."), FIG. 7E-7G. The annotated FIG.

7G below illustrates this configuration, with bumps 705 extending through the sealing resin 710 and in connection with the contact areas of semiconductor 703 and with wiring patterns 702a. In order to extend between (and electrically connect) the semiconductor contact areas and wiring patterns, the bumps extend through contact openings formed in the sealing resin.



APPLE-1006, FIG. 7G (Annotated)

126. Asahi describes methods for mounting semiconductor 703 on wiring patterns 702a and forming mechanical and electrical connections between the semiconductor and wiring patterns, including by “flip chip bonding” utilizing “gold-gold junction, or stud bumps, and soldering,” among other means. *Supra*, §VIII.A., analysis of element [12c]; APPLE-1006, 16:39-66, 8:9-10 (“a bump 105”, analogous to 705), 10:44-45 (“bump 205 and the conductive adhesive may be used in combination”), 11:47-54 (305 can be a conductive copper adhesive), 13:27-29 (“bumps 405”), 14:25-27 (“bumps 505”), 15:9-12 (“bumps 605”).

127. As sealing resin 710 is injected between semiconductor 703 and wiring patterns 702a and later cured, contact openings are formed in the hardened sealing resin 710 (the recited hardened insulating polymer layer) to accommodate bumps 705 or the like. *Supra*, §VIII.A, analysis of element [12a].

128. Further Asahi describes that the electrical contacts in the contact openings include “copper.” *Id.*, 11:47-54 (“Examples of the conductive adhesive 305 include, for instance, adhesives obtained by kneading gold, silver, a copper, silver-palladium alloy, etc. with a thermosetting resin”).

129. Based on my knowledge and experience in the field and my review of Asahi, a POSITA would have recognized and found obvious, from Asahi’s description, that bumps for mounting semiconductor on the wiring patterns would have been beneficially made of copper, a conventional and widely used conductive material in flip chip bonding. A POSITA would have been well aware of the conductive properties of copper, as well as its ease of workability and economical cost. Indeed, Asahi expressly describes benefits of high conductivity and low migration of copper in making electrical connections of its high-density component built-in module. *E.g.*, APPLE-1006, 8:19-35 (“Copper particularly is preferable since it has a high conductivity and migration of the same hardly occurs”).

130. To the extent Asahi does not expressly describe use of copper for bumps 705 in the contact openings, I note that a POSITA would have implemented

copper as a conventional and suitable material choice to effectuate Asahi's electrical contact objective. A POSITA would have understood that the use of copper in forming contact bumps for electrically connecting a semiconductor to a conductive wiring pattern was well-known by the Critical Date. APPLE-1020, 10:15-21 (corroborating prior art describing "copper bumps"); APPLE-1021, 4:37-65 (corroborating prior art describing "copper studs"); APPLE-1018 (corroborating prior art), Title, Abstract, 1:6-11, 2:8-40, 3:1-3 ("copper studs"). A POSITA would have further understood that not only could the bump itself be formed using copper, but a copper plating (or a conductive adhesive including copper, per Asahi) could also be employed on the bump to enhance conductive properties. *See e.g.*, APPLE-1030 (corroborating prior art, describing electroless copper plating in bump metallization); APPLE-1031 (corroborating prior art describing copper plating bump)); *see also* APPLE-1006, 8:9-10 ("a bump 105", analogous to 705), 10:44-45 ("bump 205 and the conductive adhesive may be used in combination"), 11:47-54 (305 can be a conductive copper adhesive), 13:27-29, 14:25-27, 15:9-12.

131. Claim 12 requires further that "the copper contains at least one of electrochemically deposited copper and chemically deposited copper." I understand that this limitation of the claim is known as a "product-by-process element" in that they merely recite a process by which copper is deposited – in particular that copper is deposited by an electrochemical or chemical process. I

understand that these recited “product-by-process element” processes have no patentable weight for the purposes of determining unpatentability of claim 12. In this case, Asahi describes copper in the contact openings, as claimed, and thus meets the requirements of claim element [12d].

132. Moreover, even if the process “product-by-process element” were considered limiting, Asahi renders obvious claim element [12d]. This is because a POSITA would have recognized, and found obvious, from Asahi’s description, that the copper used in the bumps electrically connecting the semiconductor contact areas to the conductive pattern contains at least one of electrochemically deposited copper and chemically deposited copper. A POSITA would have understood this because Asahi expressly describes plating surfaces of the wiring patterns so that “their corrosion resistance and electric conductivities can be improved.” APPLE-1006, 7:50-52. Based on Asahi’s description, a POSITA would have been motivated to utilize plating techniques for forming bumps in the contact openings to achieve similar benefits of improved corrosion resistance and electric conductivities, with the additional advantage of improved solderability for forming bumps 705. APPLE-1006, 16:39-66 (“stud bumps, and soldering”). Given Asahi’s express disclosure of using copper (e.g., to avail the system of copper’s high conductivity), a POSITA would have readily implemented the copper bumps in the contact openings using chemical and/or electrochemical plating techniques

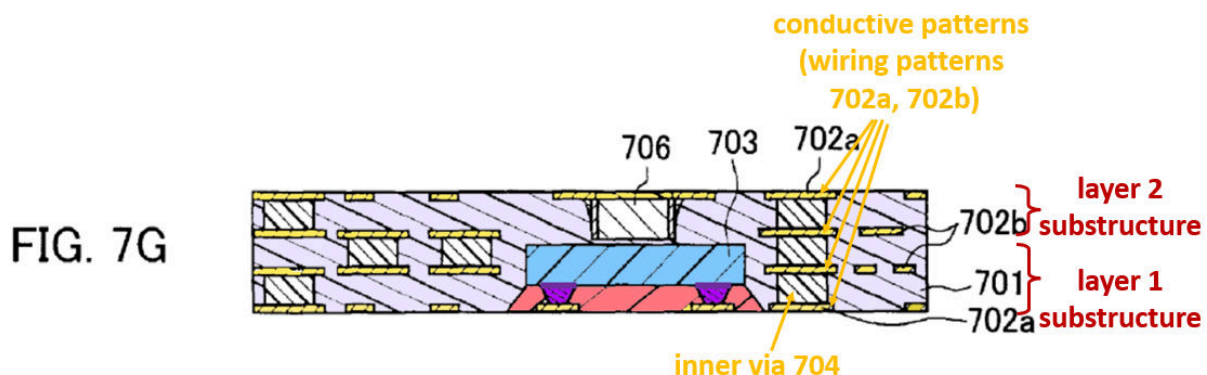
that were well-known in the field before the Critical Date for forming chip or substrate bumps, including the use of multiple plating layers on top of each other, for the benefits described above. APPLE-1006, 8:19-35. Indeed, techniques for plating bumps with copper using electroplating and electroless plating methods were well-known well before the Critical Date. *See e.g.*, APPLE-1020, 10:15-21 (corroborating prior art describing “copper bumps ... formed by electroplating”); APPLE-1021, 4:37-65 (corroborating prior art describing “copper studs” formed by electroplated copper); APPLE-1018 (corroborating prior art), Title, Abstract, 1:6-11, 2:8-40, 3:1-3 (“copper studs ... formed by electroplating copper” over a “flash coat” of copper, where “flash coat” is often done via chemical deposition); APPLE-1030 (corroborating prior art describing electroless copper plating in bump metallization); APPLE-1031 (corroborating prior art describing copper plating bump)).

133. A POSITA would have recognized that electroplating, such as electrolytic plating, is an electrochemical plating technique, and that electroless plating is a chemical plating technique. In electroplating, an electric current drives a chemical reaction to deposit a layer of metal onto a conductive surface. This process involves immersing the object to be plated (the cathode) and a piece of another conductor (the anode) in an electrolyte solution containing metal ions. Unlike electroplating, electroless plating does not require an external electric

current to deposit metal onto a surface. Instead, it relies on a chemical reaction that occurs between the plating solution and the object to be plated.

[13] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

134. Asahi provides the features of claim 13. In particular, the two circuit board substructures of layer 1 substructure and layer 2 substructure on top of each other are electrically connected to each other to form a multi-layered functioning totality of Asahi's "component built-in module." The annotated FIG. 7G below illustrates this configuration. Asahi's substructures are electrically connected by inner via (e.g., via 708 filled with conductive paste 704) that connects wiring patterns 702a/702b of the respective substructures. APPLE-1006, 15:51-17:44, FIG. 7; *see also id.*, Abstract, 1:32-39, 2:27-3:3 ("...any one of the first wiring patterns in the plurality of layers and the second wiring pattern[s] are connected electrically through an inner via"); 3:53-56, 4:19-5:62, FIGS. 1-10, cl. 1.



APPLE-1006, FIG. 7G (Annotated)

[14] The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.

135. Claim 14 is ambiguous as to whether the at least two microcircuits both require all elements recited in [12c].

136. Nonetheless, the prior art expressly describes such features. Claim 14 appears to require simple duplication of the microcircuit described in claim 12. *Supra* §VIII, Elements [12pre]-[12d]. Duplication of the microcircuit would have been obvious to a POSITA in view of Asahi's description. Further, I note that the '909 patent offers no new or unexpected result that would arise from the duplication of the microcircuit of claim 12.

137. Additionally, Asahi expressly describes "high-density component-mounting" that involves mounting a plurality of "semiconductors and circuit components" to the wiring patterns 702a and 702b (e.g., within single layer 1 substructure). APPLE-1006, 17:41-44; *see also* 12:61-13:35 ("circuit components 406 can be mounted throughout an entirety of external surfaces at a high density."); *supra*, §VIII.A., analysis of element [12c] ("microcircuit"). Such techniques for embedding a plurality of microcircuits in an insulating material layer or substrate were well-known by the Critical Date. *See e.g.*, APPLE-1008 (corroborating prior art), [0044], [0045], [0047], [0053], [0054], FIGS. 1-7, 9-21; APPLE-1014 (corroborating prior art), 1:15-16, 2:44-46, 4:66-5:3, FIGS. 1, 2. A POSITA would have recognized and found obvious, from Asahi's description, that

each of the microcircuits (e.g., each of the semiconductors) would be mounted according to the arrangement and configuration consistent with Asahi's description (e.g., of semiconductor 703) (*supra*, §VIII.A., analysis of elements [12c]-[12d]) and located within the first substructure layer (e.g., mounted to wiring patterns 702a), furthering Asahi's high density mounting objectives.

138. Indeed, Asahi illustrates and describes multiple components connected to wiring pattern 702a within the same substructure layer, and a POSITA would have accordingly implemented the components to include multiple semiconductor components, furthering Asahi's express objection of mounting semiconductors at "high density."

139. Asahi's FIG. 4 as referenced for the FIG. 7 embodiment is reproduced below for illustration. APPLE-1006, 17:41-44. Consistent with above, Asahi emphasizes again that "semiconductors and circuit components ... may be mounted on the wiring patterns 402a on **both** sides," confirming that *at least two microcircuits*, in the form of semiconductors 403 or circuit components 406, are mounted on the multi-layered circuit board. APPLE-1006, 14:5-10, 13:33-35, FIG. 4 (showing multiple semiconductors and circuit components on both sides of wiring patterns 402a of layer 2 substructure and on the upper side of wiring patterns 402a of layer 1 substructure); *see also id.*, 19:22-26, FIG. 10.

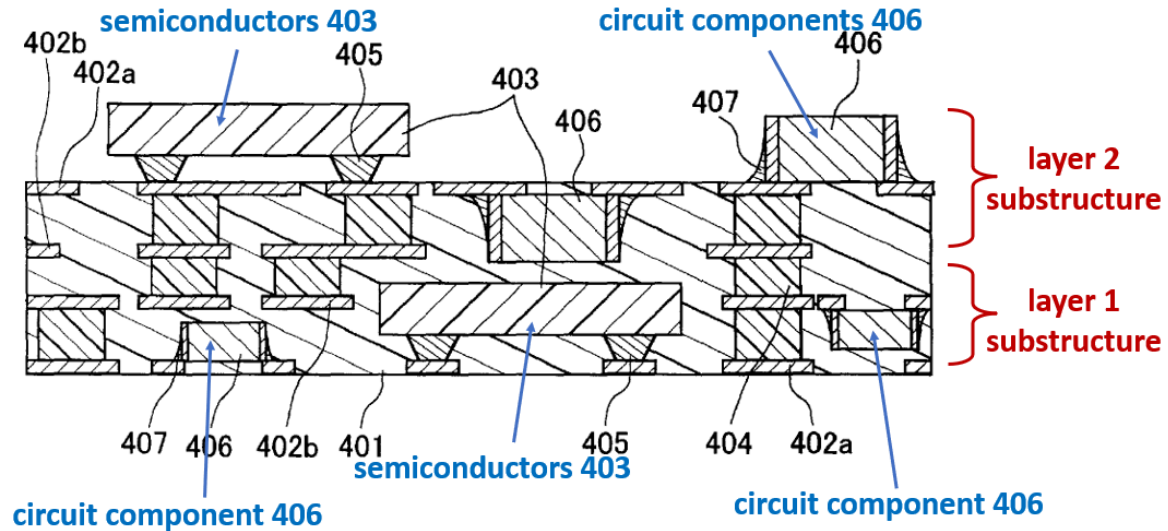


FIG. 4

APPLE-1006, FIG. 4 (Annotated)

[15] The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.

140. Asahi renders claim [15] obvious. As I previously discussed in the analyses of claims [13] and [14] (§VIII.A, Ground 1A), Asahi's layer 1 and layer 2 circuit board substructures each comprise a plurality of semiconductors and circuit components interconnected through wiring patterns and inner vias to form an integrated high-density component built-in module. APPLE-1006, 13:33-35, 14:5-10, 19:22-26, FIGS. 4, 10. Based on my knowledge and experience in the field and my review of Asahi, a POSITA would have understood and found obvious, from Asahi's description, that such semiconductors and circuit components in "high density" circuitry devices such as "large scale integrated circuits (LSIs)" described by Asahi include at least one memory circuit. Indeed, such circuits

provide memory, and memory circuits were a common type of integrated circuit used to store data in semiconductor devices used in computers, smartphones, embedded systems, and other electronic devices. APPLE-1011, [0038] (corroborating evidence providing “a silicon semiconductor memory chip” as an example for electrical elements embedded in an insulating substrate); APPLE-1008 (corroborating prior art), [0040] (“memory (DRAM, SRAM, SDRAM, etc.)” as example for electronic components embedded in an insulating substrate), [0055].

[16] The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.

141. Asahi renders claim [16] obvious. As I previously discussed in the analyses of claims [12]-[14] (§VIII.A, Ground 1A), Asahi teaches a multi-layered circuit board with a plurality of semiconductors and circuit components in various substructure layers that are electrically connected to each other through wiring patterns of each layer and inner vias, to achieve high-density component mounting.

142. For example, Asahi expressly describes constructing a multi-layered circuit board module according to the techniques illustrated and described with reference to FIGS. 7A-7G to achieve a configuration having at least three circuit board substructures on top of each other (e.g., as shown in FIG. 4). APPLE-1006, FIG. 4. The annotated FIG. 4 below illustrates an example three-layer structure with layers 1, 2 and 3 laminated (through wiring patterns 402a, 402b and inner vias

404), thereby providing at least three circuit board substructures on top of each other and electrically connected to each other. APPLE-1006, 17:41-44 (“other semiconductors and circuit components are mounted on the wiring patterns 702a on the surfaces, whereby a component built-in module shown in FIG. 4 is obtained.”); FIGS. 4, 7, 10 and related descriptions.

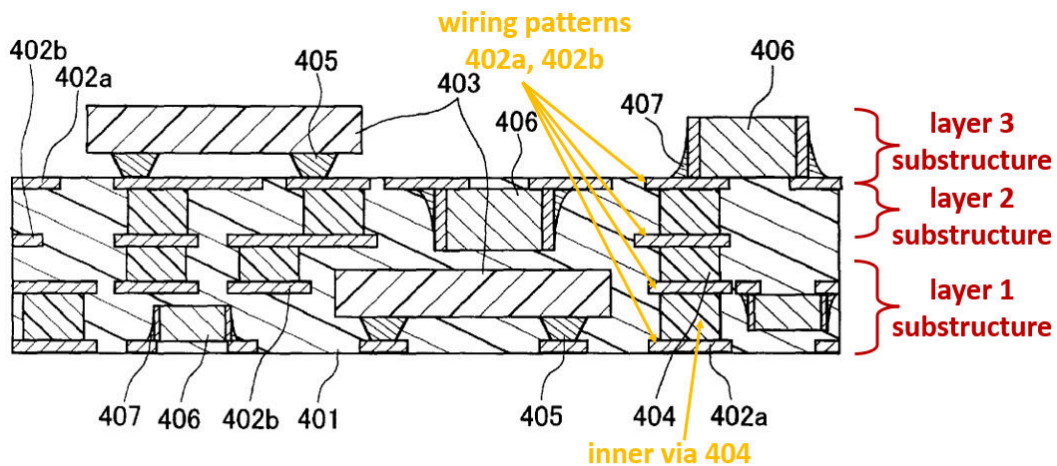


FIG. 4

APPLE-1006, FIG. 4 (Annotated)

143. A POSITA would have implemented the circuit board structure (e.g., including the configuration discussed above at [12pre]), to have a third substructure on top, in accordance with Asahi’s teachings. APPLE-1006, FIG. 4.

144. Even if Asahi did not expressly describe the conventional feature of “at least three circuit board substructures on top of each other and electrically connected to each other” recited by [16] (which it does), based on my knowledge and experience in the field and my review of Asahi, a POSITA would have been

motivated, based on Asahi's description, to construct the module (e.g., including the configuration discussed above at [12pre]) to have at least three circuit board substructures on top of each other and electrically connected to each other to enhance the component density and functionality of the module, in accordance with Asahi's express objectives, and with a reasonable expectation of success based on Asahi's express techniques for implementing such multi-layer structures. Such multi-layered structures were well-known, as I have described above. *See supra* §VIII.A, analysis of element [12pre]; *see also* corroborating references APPLE-1007, Abstract, [0004], [0034], [0217], [0225], FIG. 9A; APPLE-1016; [0010], [0021], FIGS. 5-9, cls. 1, 2, 8; APPLE-1008, [0019]-[0027], [0045]-[0057], FIGS. 9-17.

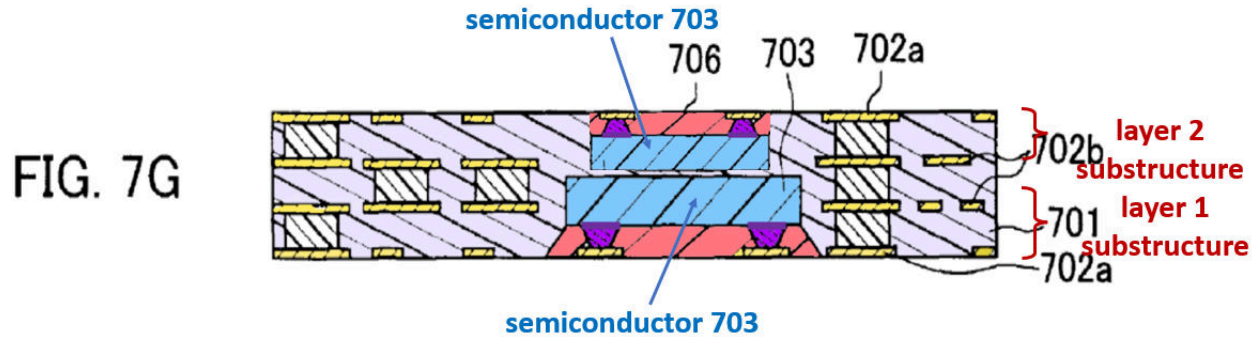
[17pre] The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise

145. To the extent the preamble is limiting, Asahi teaches [17pre], for the reasons I discussed above (§VIII.A) regarding element [12pre].

146. Asahi expressly describes mounting semiconductors and circuit components on both sides of wiring patterns 402a/702a, such that a component is mounted in each of two substructures, as I discussed above (§VIII.A) regarding element [12a]; *see also* APPLE-1006, 19:1-37. For example, Asahi describes a plurality of “semiconductors 403” and “circuit components 406” are “embedded in the electric insulation layer 401,” through mounting on wiring patterns 402a “on

both sides.” APPLE-1006, 12:61-13:35, 14:5-10, 17:41-44 (“other semiconductors and circuit components are mounted on the wiring patterns 702a on the surfaces, whereby a component built-in module shown in FIG. 4 is obtained”), FIGS. 4, 10. Asahi’s disclosure makes clear that a component built-in module includes multiple circuit board layers in which semiconductors and other circuit components are embedded.

147. Accordingly, Asahi’s description would have revealed to a POSITA, and rendered obvious, example configurations in which first and second substructure layers each include a semiconductor component mounted to conductive patterns, to achieve a high-density configuration having the functionality provided by multiple semiconductor components. A first semiconductor is mounted to wiring pattern 402a/702a (e.g., at a bottom of the module) within the first substructure layer and a second semiconductor is mounted to wiring pattern 402a/702a (e.g., at a top of the module, e.g., at the location of component 706) within the second substructure layer.



Modified FIG. 7G (Annotated)

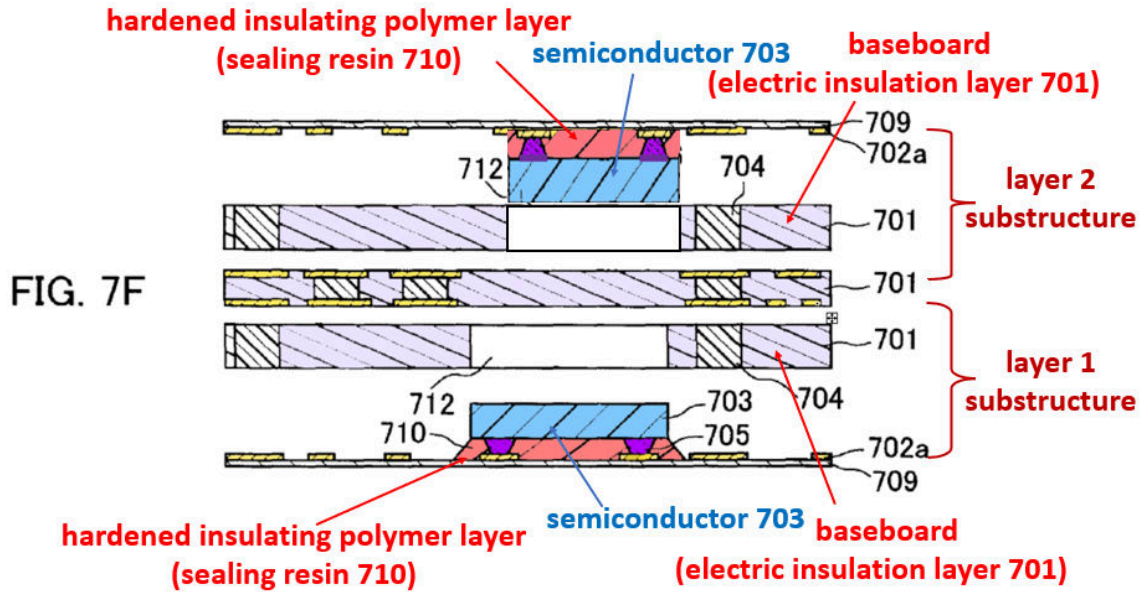
148. In the example, as shown above, each of the semiconductors are mounted according to Asahi's descriptions, and thus utilize a hardened insulating polymer (e.g., "sealing resin 710") in which the semiconductor is embedded to improve reliability as Asahi describes. *Supra*, §VIII.A, analysis of element [12c]; APPLE-1006, 16:52-62, FIGS. 7, 8; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13. Based on Asahi's description, a POSITA would have found it obvious to implement the component built-in module to include one semiconductor 703 embedded in layer 1 substructure and another semiconductor 703 (replacing component 706 in the original FIG. 7) embedded in layer 2 substructure, with the two substructures having similar configuration, furthering a high-density component figuration according to Asahi's straightforward suggestions.

[17a] an insulating material layer including a baseboard and a hardened insulating polymer layer,

149. Asahi provides element [17a]. As I previously discussed in the analysis of element [12a] (§VIII.A), layer 1 circuit board substructure of Asahi's

component built-in module comprises an insulating material layer composed of an electric insulation layer (the recited baseboard) and a sealing resin layer (the recited hardened insulating polymer layer). As I previously discussed in the analysis of element [17pre] (§VIII.A), the layer 2 circuit board substructure of the modified FIG. 7 has a similar configuration, also including an insulating material layer composed of an electric insulation layer (the recited baseboard) and sealing resin layer (the recited hardened insulating polymer layer).

150. As shown below in modified FIG. 7F (e.g., implementing component 706 as a semiconductor 703, likewise with sealing resin), consistent with Asahi's suggestions, the top insulation layer 701 includes hole 712 to receive the semiconductor 703 of the layer 2 substructure, such that the top insulation layer 701 provides the baseboard of layer 2 substructure. Together with the sealing resin, this top insulation layer 701 provides the insulating material layer of the layer 2 substructure. Similarly, the bottom 701 layer includes hole 712 to receive the semiconductor 703 of the layer 1 substructure and provides the claimed baseboard of the layer 1 substructure. Together with the sealing resin, the bottom 701 layer provide the insulating material layer of layer 1 substructure. *Supra*, §VIII.A, Ground 1Aanalysis of element [12a].



Modified Based on APPLE-1006, FIG. 7F (Annotated)

[17b] conductive patterns on both sides of the insulating material layer,

151. Asahi provides element [17b]. *Supra*, §VIII.A, analyses of elements [12b] and [17pre]-[17a]. As I show below in the modified FIGS. 7F-7G, layer 1 and layer 2 substructures each comprises conductive wiring patterns 702a (the recited conductive patterns) on the upper side of its insulating material layer, and conductive wiring patterns 702b (the recited conductive patterns) on the lower side of its insulating material.

FIG. 7F

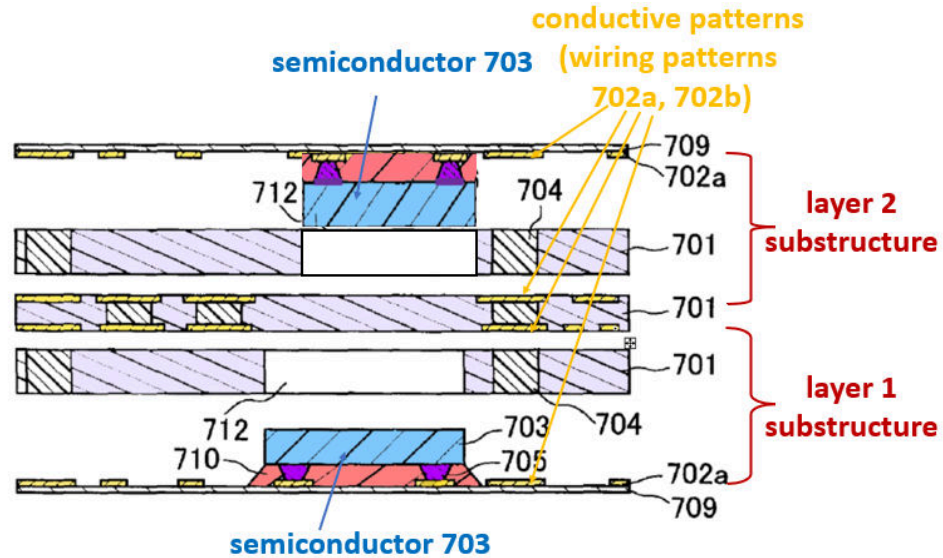
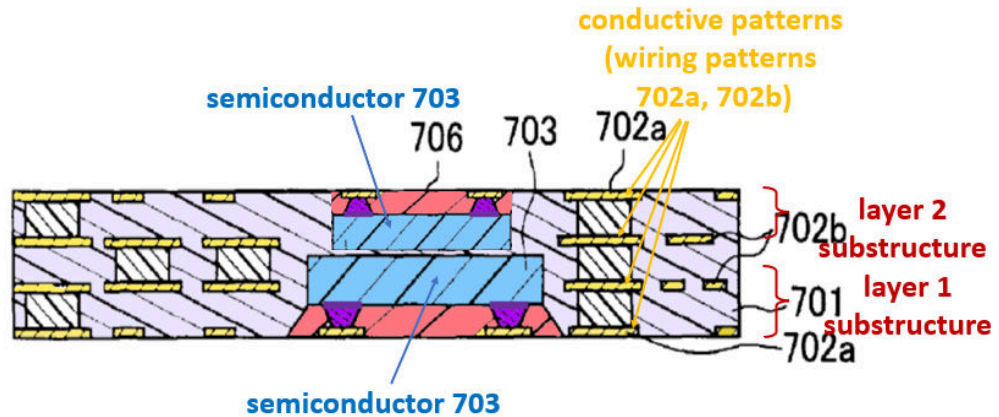


FIG. 7G



Modified APPLE-1006, FIGS. 7F-7G (Annotated)

[17c] at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and

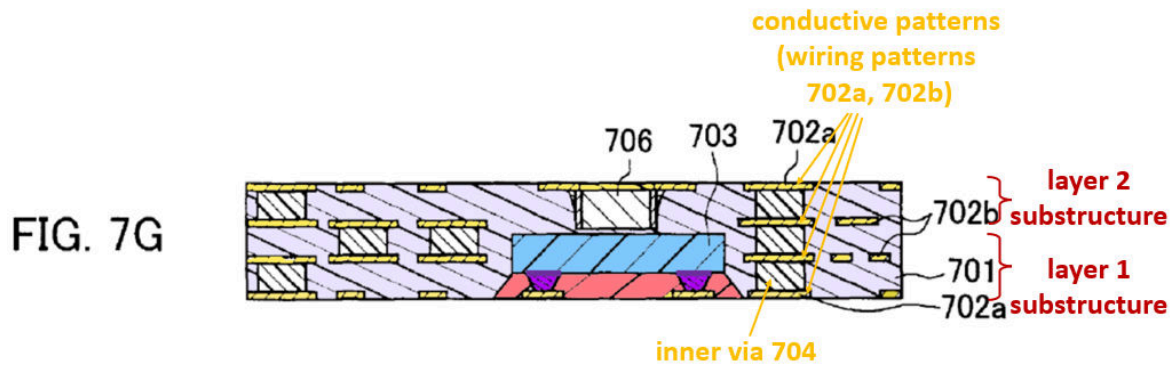
152. Asahi provides element [17c] for at least the same reasons as I previously discussed in the analysis of elements [12c] and [17pre]. *Supra*, §VIII.A.

[17d] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

153. Asahi renders element [17d] obvious for at least the same reasons as I previously discussed in the analyses of elements [12d] and [17pre]. *Supra*, §VIII.A.

[18] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.

154. Asahi renders claim [18] obvious. *Supra*, §VIII.A, analysis of claim [13]. As illustrated below in the annotated FIG. 7G, layer 1 substructure (the recited first circuit board substructure) and layer 2 substructure (the recited second circuit board substructure) are electrically connected to each other to form a multi-layered functioning totality through wiring patterns 702a, 702b and inner vias 704. APPLE-1006, FIG. 7G.



APPLE-1006, FIG. 7G (Annotated)

[19pre]-[19d] The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, conductive patterns on both sides of the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

155. Asahi renders claim 19 obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d] and claim [18].

Supra, §VIII.A.

[20pre]-[20d] The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, a conductive pattern on the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

156. Asahi renders each element of claim 20 obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d], [17pre]-[17d] and claim [19]. *Supra*, §VIII.A.

[21] The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.

157. Asahi renders claim [21] obvious for at least the same reasons as I previously discussed in the analyses of element [12a] (e.g., regarding the sealing resin containing “epoxy resin”) and claim [20]. *Supra*, §VIII.A.

[22] The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.

158. Asahi renders claim [22] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre] (*see e.g.*, discussion of Asahi’s electric insulation layers being “a board form” containing “glass-epoxy,” and “a reinforcing material such as a glass cloth or an unwoven fabric”) and claim [20]. *Supra* §VIII.A; APPLE-1006, 3:60-65, 14:30, 16:1-2, cls. 11, 21.

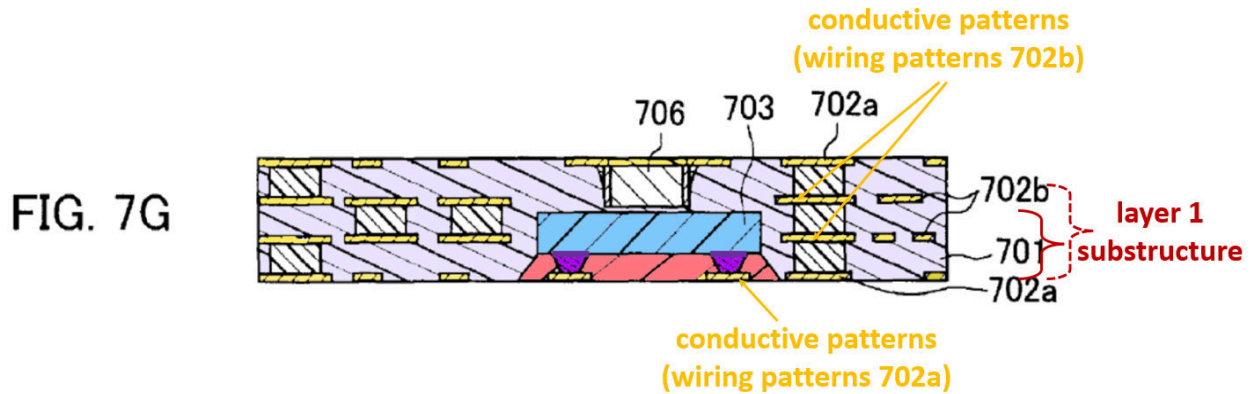
[23] The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.

159. Asahi renders claim [23] obvious for at least the same reasons as I previously discussed in the analyses of claims [12], [18], and [19]. *Supra*, §VIII.A. In particular, Asahi renders claim [23] obvious under two alternative mappings.

160. First, I note that the dependency of claim 23 is such that only “at least one” of the at least two circuit board substructures includes the features recited in elements 12a-12d. In particular, claim 23 depends on claim 19, which depends on claim 18 which then depends on claim 12, and, as stated, these claims recite that “at least one,” not both, of the at least two circuit board substructures have the features of elements 12a-12d. Thus, because only “at least one” of the circuit board substructures need to have the features of elements 12a-12d, the two substructure layers of claim 12 can be alternatively divided (compared to the division that I previously discussed and shown in the analysis of element [12pre] of §VIII.A), such that a layer of wiring patterns 402b/702b is above the height of semiconductor 403/703 and included in the layer 1 substructure, resulting in semiconductor 403/703 (the recited at least one microcircuit of the first circuit board substructure) located between at least one layer of wiring patterns 402b/702b and a layer of wiring patterns 402a/702a (the recited conductive patterns on both sides of the insulating material layer of the first circuit board substructure).

Indeed, Asahi explicitly explains that there can be more than two layers of wiring patterns on a wiring board (such as the wiring board as shown in FIGS. 7C and 7D). APPLE-1006, 2:27-36 (“a wiring board including second wiring patterns in at least two layers”), 4:60-62; 14:33-35, 15:17-18 (“a wiring board 610 that includes wiring patterns ... 602b in a plurality of layers”), 19:6-8, cls. 2, 15.

161. The annotated FIG. 7G below illustrates the first and second alternative manners in which Asahi discloses claim 23. According to the first manner (indicated by a dashed bracket in the annotated FIG. 7G below), the layer 1 substructure includes the wiring patterns 702b layer above the top surface of semiconductor 703, such that semiconductor 703 is **entirely** between at least this wiring patterns 702b layer and the wiring patterns 702a layer on the bottom surface of the layer 1 substructure. According to the second manner (indicated by a solid bracket in the annotated FIG. 7G below), semiconductor 703 is at least partially between the lower patterns 702b layer and the wiring patterns 702a. Nothing in the plain language of the claim expressly recites that the component is “entirely” or “exclusively” between the conductive patterns, allowing for Asahi to meet the claim limitation according to either of the described mappings.



APPLE-1006, FIG. 7G (Annotated)

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

162. Asahi renders claim [24] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d]. *Supra*, §VIII.A. As with element [12d], I understand that the claim [24] recitation of “chemically deposited” copper and a second layer of “electrochemically deposited” copper on the first layer of chemically deposited copper, are known as “product-by-process elements” and are generally not considered to be limiting for purpose of invalidity. With regard to claim [24], Asahi provides two layers of copper (the recited first layer of [] copper and a second layer of [] copper on the first layer of [] copper), and thus discloses claim 24. *Supra*, §VIII.A., analysis of element [12d] (discussing the obviousness of using both electroless copper plating, which is a chemical

deposition of copper, and electroplating of copper, which is an electrochemical deposition of copper).

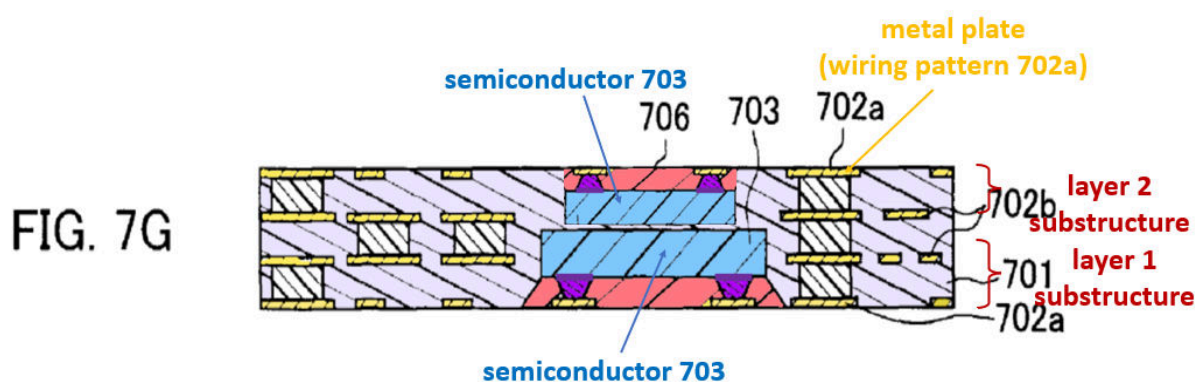
163. Even if the recited processes are limiting, Asahi provides claim 24, as I previously discussed in the analysis of element [12d] demonstrating chemically deposited and electrochemically deposited copper on top of each other in the contact openings, based on Asahi's disclosure of plating and preference for copper as a high conductivity material for making electrical connections, as these are common plating techniques used for forming chip and substrate bumps in ordinary flip chip bonding, and utilize multiple plating layers. APPLE-1006, 7:50-52, 8:19-35; *see also* APPLE-1002, 53-58 (Official Notice during original prosecution, stating, "formation of plated Cu layers using both methods in formation of a seed layer and a bulk Cu layer was known prior to applicant's invention.").

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

164. Asahi renders claim [25] obvious for at least the same reasons as I previously discussed in the analyses of claims [20], [19], [17], [12]. *Supra*, §VIII.A. For example, as I previously discussed above in the analysis of element [12b] (§VIII.A), Asahi discloses that wiring patterns, such as wiring patterns 402a/702a and 402b/702b, are made of "a metal foil" or "a lead frame obtained by processing a **metal plate**." APPLE-1006, 7:23-26, 17:41-44. Asahi explains that

“the number of layers is not limited” for the inner wiring patterns 102b, and “a plurality of layers of inner wiring patterns 102b exist.” APPLE-1005, 9:4-10.

Asahi thus discloses the recited metal plate that may be processed to form a wiring pattern. The modified FIG. 7G below illustrates an example of such configuration, where the wiring patterns 702a of the layer 2 substructure represent the position of the recited metal plate above the embedded semiconductor (the recited at least one of the microcircuits) of the layer 2 substructure. *Supra*, §§VIII.A, analyses of claims [14]-[16] and element [17pre].

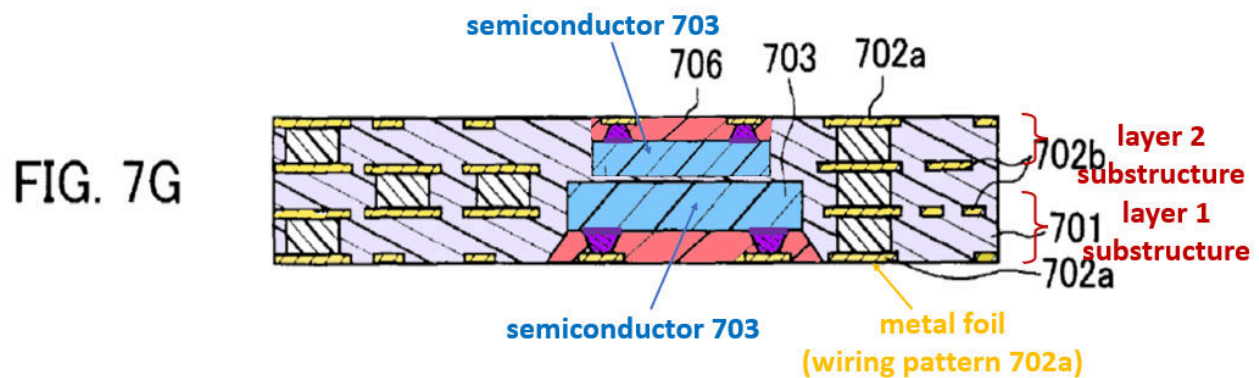


Modified Based on APPLE-1006, FIG. 7G (Annotated)

[26] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.

165. Asahi renders claim [26] obvious for at least the same reasons as I previously discussed in the analysis of claim [25]. *Supra*, §VIII.A. For example, in the below annotated FIG. 7G, wiring patterns 702a of the layer 1 substructure provide a metal plate or metal foil **below** the embedded semiconductor 703 (the

recited at least one of the microcircuits) of the layer 1 substructure. APPLE-1006, 3:39-41 (“the first wiring patterns preferably are made of at least one selected from a metal foil, ...”), 7:23-29 (“The wiring patterns 102a and 102b are made of a material having an electric conductivity, and a metal foil... may be used for instance [and t]he use of a metal foil or a lead frame allows fine wiring patterns to be formed by etching or the like”), cls. 5, 18 (“the first wiring patterns are made of at least one selected from a metal foil, ...”).



Modified Based on APPLE-1006, FIG. 7G (Annotated)

[27pre]-[27d] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising: an insulating material layer including a baseboard and a hardened insulating polymer layer; conductive patterns on both sides of the insulating material layer; at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and

166. Asahi renders obvious elements [27pre]-[27d] for at least the same reasons as I previously discussed in the analyses of elements [17pre]-[17d]. *Supra*, §VIII.A.

[27e] at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.

167. Asahi renders obvious element [27e] for at least the same reasons as I previously discussed in the analyses of claims [25] and [26]. *Supra*, §VIII.A. In particular, above I have described with regard to claim [25] the use of “metal foil” for wiring patterns, such as wiring patterns 702a, which I explained with regard to claim [26] as located in the layer 1 substructure below the embedded semiconductor 703 of the layer 1 substructure.

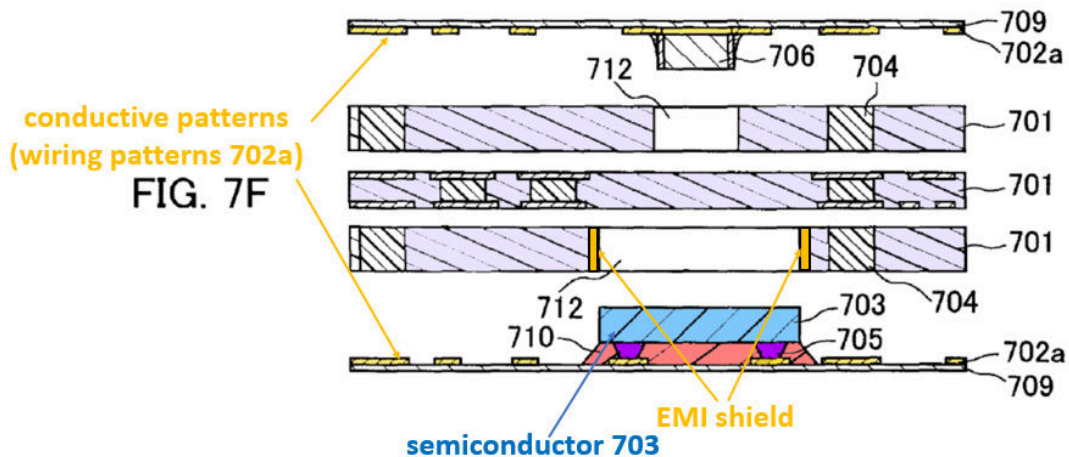
IX. GROUND 1B: CLAIMS 1-33 ARE OBVIOUS IN VIEW OF THE ASAHI-DUDDERAR COMBINATION

168. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a

POSITA would have understood that the teachings of Asahi and Dudderar render claims 1-33 obvious, based on Dudderar's additional description of EMI shielding and copper metallization.

A. The Predictable Combination of Asahi and Dudderar

169. Based on my knowledge and experience in the field and my review of Asahi and Dudderar, a POSITA would have been motivated to combine the teachings of Asahi and Dudderar to enhance Asahi's circuit board through implementation of an EMI shield and copper metallization on the sidewalls of the cavity, as Dudderar teaches. Implementing Asahi's circuit board with an EMI shield and copper metallization on the cavity sidewalls would have enhanced Asahi's device, and would have been consistent with Asahi's teachings of using metal on the sides of a component, e.g., solder 707 on the sides of component 706. *E.g.*, APPLE-1006, 16:43-46, FIG. 7E. The annotated composite figure below illustrates this modification, of adding an EMI shield, in accordance with Dudderar, to the sidewalls of through-hole 712 in insulating layer 701, before inserting semiconductor 703 at a lamination process.



Composite Based on APPLE-1006, 7F (Annotated)

170. In the combined system, Asahi's cavity sidewalls incorporate copper metallization as an EMI shield, as Dudderar suggests, to protect the semiconductor 703, as illustrated in the composite figure above. A POSITA would have been motivated to combine the teachings of Asahi and Dudderar to arrive at the combination for multiple reasons.

171. First, a POSITA would have been motivated to combine Asahi and Dudderar to alleviate the common and well-known "EMI problems" associated with integrated circuit packages caused by external electromagnetic waves, and to enhance protection and stabilization of the embedded components. APPLE-1014, 1:10-63; (discussing prior art trying to "combat EMI problems in IC packages"), 5:45-46 ("The EMI metallization on the PCB side of the structure is typically copper"). For example, Dudderar describes "[a]s is known, EMI is disruptive to

the proper operation of circuit components located near the source of the EMI...

Accordingly, there is an identifiable need to reduce EMI susceptibility.” *Id.*, 1:41-44. A POSITA would have understood that EMI problems can interrupt circuit operation, and would have been motivated to combine the teachings of Asahi and Dudderar to prevent such disruption of the semiconductor. *See also*, APPLE-1012 (corroborating prior art describing the problems of EMI susceptibility of electronic components built into an insulating substrate, and a solution through adding an EMI shielding layer on the sidewalls of a through-hole for accommodating the electronic components), Abstract, FIG. 1; APPLE-1016, [0022] (corroborating prior art describing “shielding effect” against EMI); APPLE-1015, 4:7-9, 5:24-36, 12:39-50 (corroborating prior art describing the use of a “shield layer” or “shield section” so that “noise does not penetrate to the electrical element contained inside the housing section of the multilayer substrate”).

172. Second, combining Asahi and Dudderar would have been a common application of known techniques (forming an EMI shield on the sidewalls of a cavity or through-hole provided in an insulating substrate for accommodating IC chips) to a known device (Asahi’s component built-in module having a through hole 712 in a wiring board to receive semiconductor 703).

173. Based on my knowledge and experience in the field and my review of Asahi and Dudderar, a POSITA would have had a reasonable expectation of

success modifying Asahi with Dudderar, because of the similarities between the systems. For example, both Asahi and Dudderar relate to embedding semiconductor components such as IC chips within cavities of an epoxy board, and both using flip-chip bonding to mount the chips on a metal-lined carrier before inserting into the cavities, both also putting metal on the sides of embedded components. APPLE-1006, Title, Abstract, 3:44-46, 3:60-65, 6:33-46, 7:66-8:18, 15:62-67, 16:41-17:40, 17:55-18:13, FIG. 7; APPLE-1014, 2:43-54, FIG. 2.

174. Based on my analysis, a POSITA would have recognized that applying Dudderar's suggestions to Asahi's electronic module would not have significantly altered or hindered the functions performed by Asahi's electronic module. Moreover, based on my knowledge and experience in the field, a POSITA would have found making the proposed modifications to be straightforward, since the modifications would have been implemented largely by adding a metal layer on the sidewalls of the hole, such as by using standard metallization for circuit boards extending it along the sidewalls of the cavity, for EMI shielding. Dudderar already demonstrates this configuration to be successful. And the use of EMI shield layer on the sidewalls of a cavity for disposing electronic components in a circuit board was known. *See e.g.*, APPLE-1012 (corroborating prior art describing the problems of EMI susceptibility of electronic components built into an insulating substrate, and a solution through adding an

EMI shielding layer on the sidewalls of a through-hole for accommodating the electronic components), Abstract, FIG. 1. Moreover, Asahi and Dudderar describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons I noted above.

B. Analysis of Asahi and Dudderar with Respect to Claims 1-11, 28-33

175. As shown in this section, the Asahi-Dudderar combination, when predictably combined for at least the reasons described above, provides claims 1-11 and 28-33.

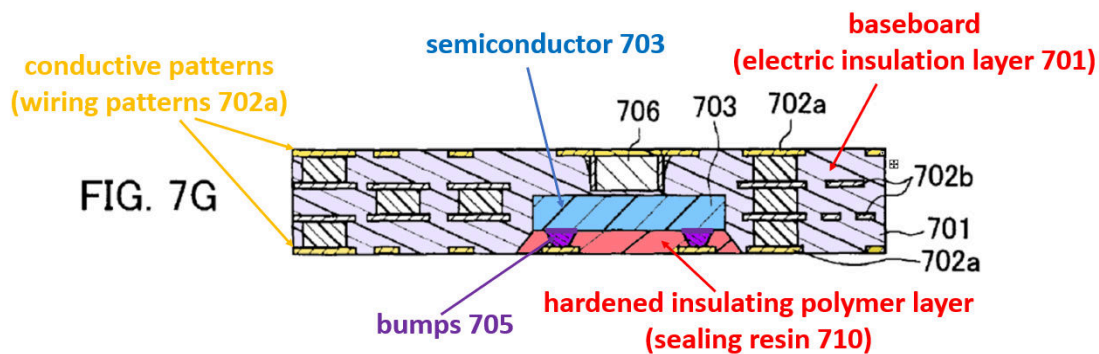
[1pre]-[1c] A circuit board, comprising: an insulating material layer including a baseboard and a hardened insulating polymer layer; conductive patterns on both sides of the insulating material layer; at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;

[1e] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

176. Asahi-Dudderar renders obvious elements [1pre]-[1c] and [1e] for at least the same reasons as I previously discussed in the analyses of elements [12a]-[12c] and [12d] in Ground 1A. *Supra*, §VIII.A.

177. The Asahi-Dudderar combination additionally provides claim 1 in a second manner. For example, in the Asahi-Dudderar combination, the *entire*

unified electric insulation layer 701 of the configuration in FIG. 7G (formed by laminating all three layers of 701 of FIG. 7F) provides the recited baseboard of [1a] and the wiring patterns 702a formed on both surfaces of the entire module provide the recited conductive patterns on both sides of the insulating material layer of [1b]. *Supra*, §VIII.A, analyses of elements [12a]-[12b]; *see also* APPLE-1006, FIGS. 3, 8 and related descriptions.

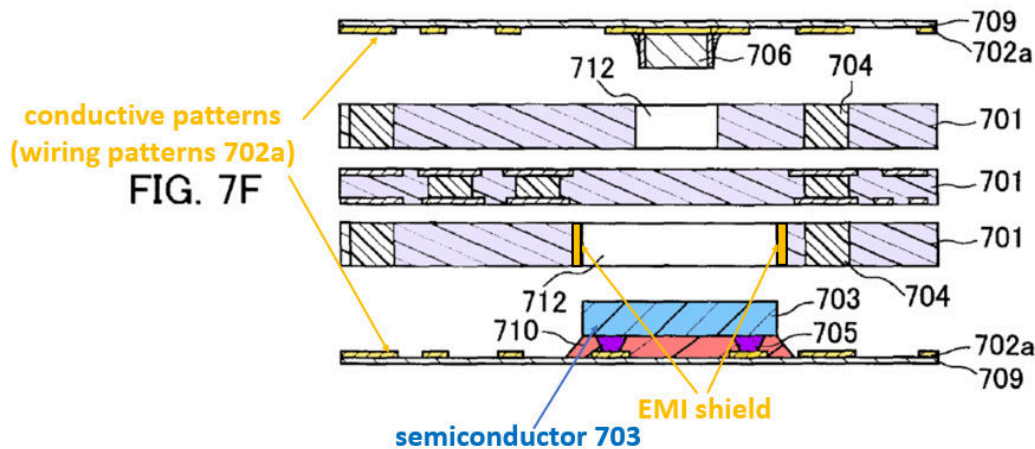


APPLE-1006, FIG. 7G (Annotated)

[1d] conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

178. The Asahi-Dudderar combination renders element [1d] obvious. For example, in the combined Asahi-Dudderar device (*see supra*, §IX.A (Asahi-Dudderar combination)), metallization (e.g., copper) is located along the sidewalls of hole 712 in the electric insulation layer 701 for EMI shielding (the recited conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit), in accordance with Dudderar.

APPLE-1014, 3:24-27, 4:45-49; *see also id.*, 3:3-4; APPLE-1006, 5:47-49, 9:40-46, 10:18-25, 16:27-46, 17:25-34, 19:60-20:10. This is illustrated in annotated composite figure below.



Composite Based on APPLE-1006, FIG. 7F (Annotated)

179. Dudderar describes edge EMI shield metallization portion 27' outside of cavity 17 on the printed circuit board (PCB 16) as “part of a standard PCB,” and alternatively providing edge EMI shield metallization 41 along the inside walls of cavity 17. APPLE-1014, 3:24-27, 4:45-49; *see also id.*, 3:3-4 (EMI shield metallization “can be as thick as desired ... e.g. less than 4 μm ...”). Based on my knowledge and experience in the field, a POSITA would have understood that both the edge EMI metallization 27' on the outside of the cavity and edge EMI metallization 41 on the inside of the cavity, as “part of a standard PCB,” are formed through the same standard PCB process. APPLE-1014, 3:3-4, 3:24-27,

4:45-49. Asahi also expressly teaches applying metal on the sides of a component.
E.g., APPLE-1006, 16:43-46 (element 707 on sides of component 706), FIG. 7E.

180. A POSITA would have further understood that the lamination of a multilayer wiring board is also a conventional PCB process, which would not have compromised the functionality of the EMI shield on the sidewalls of the cavity when the insulation layers (e.g., 701) are laminated together, because this metallization shield layer would have either extended through part of the non-cured middle 701 layer (the electric insulation layers 701 having a low viscosity during lamination and before curing), or compressed along with the electric insulation layers, with some potential bending from the compression during lamination. APPLE-1006, 5:47-49 (“the electric insulation layer before being laminated preferably is in a non-cured state”), 9:40-46 (“The electric insulation layer ... may be heated to a temperature not higher than the curing temperature and dried, so that the viscosity thereof can be decreased....”), 10:18-25 (metal layers formed in the electric insulation layer “in a non-cured state”), 16:27-35, 17:25-34, 19:60-20:10.

[2] The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

181. Asahi-Dudderar renders claim [2] obvious for at least the same reasons as I previously discussed in the analyses of element [12a] (see analysis related to the sealing resin of Asahi containing “epoxy resin”) and claim [21].

Supra, §VIII.A.

[3]² The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.

182. Asahi-Dudderar renders claim [3] obvious for at least the same reasons that I previously discussed in the analyses of elements [12pre] and [12a] (§VIII.A.). Again, a POSITA would have found it obvious for the combination's sealing resin to contain similar material, such as "glass-epoxy" or epoxy resins with glass fillers, as the electric insulation layer, to further avoid stresses due to mismatch in "a heat conductivity, a coefficient of linear expansion, a dielectric constant, etc." between the sealing resin and the surrounding electric insulation layer. *Supra*, §VIII.A., analyses of [12pre]-[12a]. Based on my knowledge and experience in the field, I note that a POSITA would have found it obvious to implement glass fibers, which was a common choice, for glass fillers in a resin. Using glass fibers as fillers in a resin was a well-known economical solution in the field that provides effective structural properties and enhances module robustness. *See e.g.*, APPLE-1012 (corroborating prior art), [0038] ("in addition to the glass-

² Based on my review and understanding of the '909 patent, I do not find description in the '909 patent's specification of the recited "the hardened insulating polymer layer contains epoxy and glass fibres" limitation. Nonetheless, the prior art teaches this limitation.

epoxy resin composite material described above, the insulating substrate 2 can be made of glass woven fabrics or composite materials of glass fibers and resins”); *see also e.g.*, APPLE-1032 (corroborating prior art on glass fillers used in underfill resins for flip-chip packaging), Title, Abstract, 121-124, 127 (references citing “glass fiber” and “glass spheres”); APPLE-1033 (corroborating prior art describing inserting glass filled epoxy under flip-chip packages for enhanced reliability), Title, 858-860.

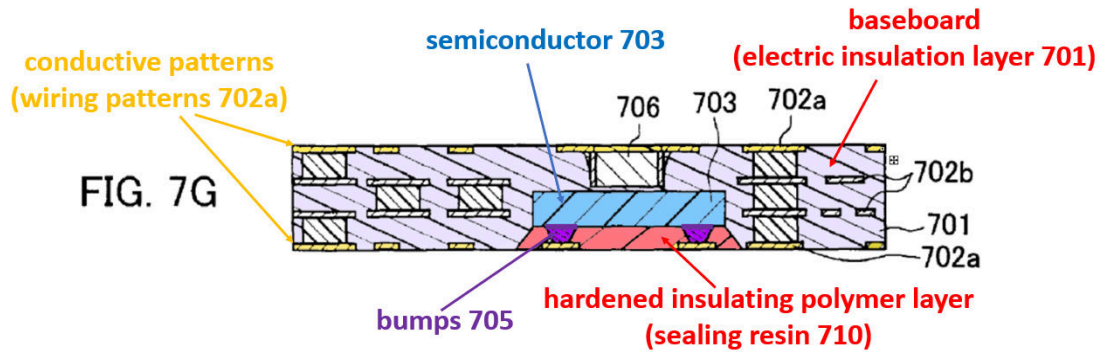
[4] The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

183. Asahi-Dudderar renders claim [4] obvious for at least the same reasons as I previously discussed in the analysis of claim [22], for example, the combined system’s electric insulation layer 701 (the recited baseboard) is an epoxy board “contain[ing] a reinforcing material such as a glass cloth or an unwoven fabric.” *Supra*, §VIII.A; APPLE-1006, 3:60-65, 14:30, 16:1-2, cls. 11, 21.

[5] The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.

184. Asahi-Dudderar renders claim [5] obvious. For example, as shown below in annotated FIG. 7G, the semiconductor 703 (the recited microcircuit) is located between wiring patterns 702a (the recited conductive patterns) on both sides of the unified insulating material layer composed of the unified electric insulation layer 701 (the recited baseboard) and sealing resin 710 (the recited

hardened insulating polymer layer). APPLE-1006, 11:26-12:51, 17:45-18:13; *see also supra* §VIII.A., analyses of elements [12pre]-[12c], §IX.B., analyses of elements [1pre]-[1c].



APPLE-1006, FIG. 7G (Annotated)

[6] The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.

185. Asahi-Dudderar renders obvious claim [6]. The Asahi-Dudderar combination includes a filler material in the hole to secure integrated circuit component 20 in place, in accordance with Dudderar's teachings. As I described above, Asahi provides a semiconductor 703 (the recited microcircuit) positioned in a hole 712. APPLE-1006, 17:14-40; *supra* §VIII.A, analysis of element [12c]. Additionally, Dudderar incorporates by reference Degani, which describes the use of a filler material in the cavity in the printed wiring board, including a suggestion to use "a compliant encapsulating material encompassing the [embedded] chips," to "protect[] the chips, interconnections and adjacent surfaces of the substrate."

APPLE-1019, 3:4-56, 5:24-34 (“the cavity ... is filled with an encapsulating material... such as silicone gel”), 5:63-65 (“the cavity is filled by ... epoxy resin”), cls. 2, 6; APPLE-1014, 2:15-18 (incorporating the disclosure of U.S. Patent No. 5,608,262 to Degani by reference); *see also* APPLE-1006, 2:15-10; 16:59-62.

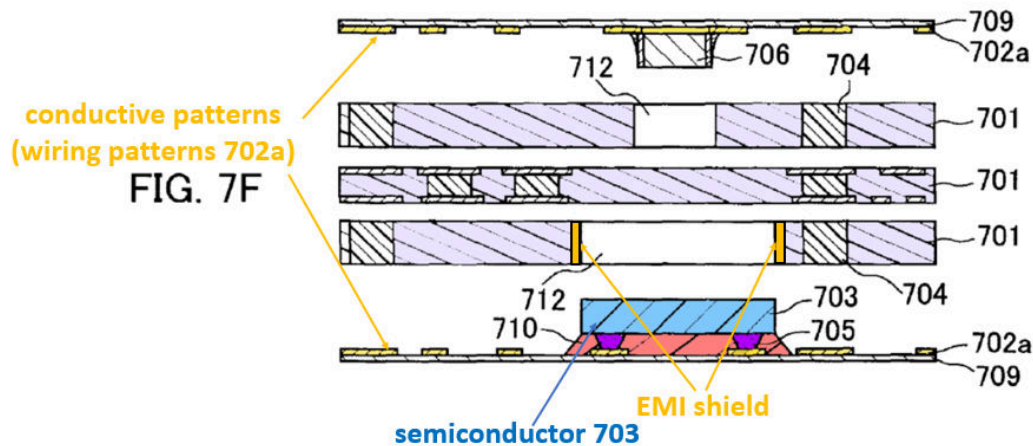
186. Based on my knowledge and experience in the field, and my review of Asahi and Dudderar, a POSITA would have recognized and found obvious that in the manufacturing process of Asahi, there is sufficient clearance in hole 712 to facilitate fit of the components. For example, in Asahi’s process, carrier 709 temporarily secures semiconductor 703 in the hole 712 during lamination, but once carrier 709 is removed, a thin wiring layer 702a remains with sealing resin at the connection portion. APPLE-1006, 17:14-40. Based on the disclosures of Asahi and Dudderar, a POSITA would have found it obvious to fill hole 712 with a filler material to better secure each semiconductor 703 (the recited microcircuit) in a predetermined position (“in place in the hole” as recited), consistent with Dudderar’s suggestions. APPLE-1014, 2:9-18 (pointing the POSITA to Degani’s disclosure for options for using a recessed chip package); APPLE-1019, 3:4-56, 5:24-34, 5:63-65.

187. Moreover, a POSITA would have predictably combined the teachings of Asahi and Dudderar by using a similar conformable encapsulating material of Dudderar before lamination of the layers of Asahi’s component built-in module, or,

alternatively, by flowing the uncured resin of electric insulation layer 701 (e.g., the middle 701 layer of FIG. 7F shown below and labeled as 701b for ease of reference) with decreased viscosity into the gap of hole 712 around semiconductor 703 during lamination “[b]y pressing and heating,” for example. APPLE-1006, 5:47-49, 9:40-46, 10:18-25, 16:27-35, 17:14-40, 19:60-20:10.

188. A POSITA would have understood that it was conventional and well-known to flow uncured insulating layer material into the gap around a component during processing to provide various benefits. *See e.g.*, APPLE-1011 (corroborating prior art), [0040]; APPLE1017 (corroborating prior art), 1:30-33 (“a method has come to be commonly studied in which an underfill material of an epoxy resin type is injected into a chip-/substrate gap in order to relax the stress at the bonding interface.”); APPLE-1008 (corroborating prior art), [0037], [0042] (“The encapsulation material 122 secures the microelectronic device 114 within the microelectronic substrate core 102 and provides mechanical rigidity for the resulting structure...”).

189. A POSITA would have understood that the volume of electric insulation layer 701b would flow in the holes to fill in any gaps during the lamination process, during which the uncured 701 layers are pressed and fused together with heating, and semiconductor 703 and circuit component 706 are pressed into the 701b layer from opposite directions. APPLE-1006, 17:18-24.



Composite Based on APPLE-1006, FIG. 7F (Annotated)

[7] The circuit board of claim 6, wherein the filler material contains epoxy.

190. Asahi-Dudderar renders claim [7] obvious for at least the same reasons as I previously discussed in the analyses of element [12pre] in Ground 1A (see discussion related to the insulation layer 701 containing an epoxy resin) and claim [6] above in Ground 1B (see discussion related to the use of filler material). *Supra*, §§VIII.A, IX.B.

[8pre] The circuit board of claim 1, wherein

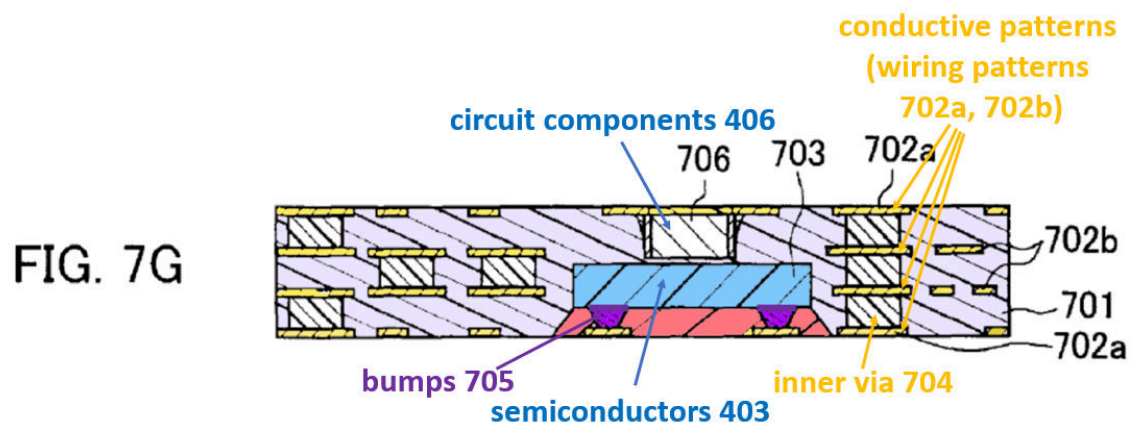
191. Asahi-Dudderar renders obvious element [8pre] for at least the same reasons as I previously discussed in the analyses of element [12pre] in Ground 1A and element [1pre]-[1e] in Ground 1B. *Supra*, §§VIII.A, IX.B.

[8a] said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and

192. Asahi-Dudderar renders obvious element [8a] for at least the same reasons as I previously discussed in the analyses of claims [14] and [15] in Ground 1A. *Supra*, §VIII.A.

[8b] the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

193. Asahi-Dudderar renders obvious element [8b]. For example, as I previously discussed in Ground 1A with regard to claims [13], [16], [18], the wiring patterns (e.g., 702a and 702b) of various layers of Asahi's component built-in module are electrically connected to each other through inner vias (e.g., inner vias 704). *See supra* §VIII.A. This is illustrated in annotated FIG. 7G below.



APPLE-1006, FIG. 7G (Annotated)

194. As I also discussed above in the analysis of element [12d] in Ground 1A and in the analysis of element [1e] in Ground 1B, each of Asahi-Dudderar's semiconductor 703 is connected to wiring patterns 702a through bumps 705. *See supra* §§VIII.A, IX.B. Accordingly, Asahi-Dudderar's plurality of semiconductors 703 (the recited microcircuits) are connected to each other by means of bumps 705 (the recited conductors in the contact opening) and by wiring patterns 702a and 702b ("at least one of the conductive patterns" as recited). *See e.g.*, APPLE-1006, 13:7-9, 16:43-46, 17:59-61. Additionally, the combined system's circuit components 706 are connected to wiring patterns through a solder 707 or a conductive adhesive. *Id.*, 16:39-52.

[9] The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

195. Asahi-Dudderar renders claim [9] obvious for at least the same reasons as I previously discussed in the analysis of claim [24]. *Supra*, §VIII.A.

[10] The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

196. Asahi-Dudderar renders claim [10] obvious for at least the same reasons as I previously discussed in the analysis of claim [13]. *Supra*, §VIII.A. In particular, in the discussion of claim [13], I described that Asahi's electrically conducting inner via 704 maps to the feed-through between the wiring patterns 702a

on both surfaces of the module (the recited conductive patterns on the both sides of the insulating material layer). APPLE-1006, 15:51-17:44, FIG. 7; *see also id.*, Abstract, 1:32-39, 2:27-3:3 (“...any one of the first wiring patterns in the plurality of layers and the second wiring pattern[s] are connected electrically through an inner via”); 3:53-56, 4:19-5:62, FIGS. 1-10.

[11pre]-[11b] The circuit board of claim 1, wherein said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.

197. Asahi-Dudderar renders elements [11pre]-[11b] obvious for at least the same reasons as I previously discussed in the analyses of elements [8pre]-[8b]. *Supra*, §IX.B.

[12]-[27]

198. Asahi-Dudderar renders obvious claims [12]-[27] for at least the same reasons set forth above in Ground 1A. *Supra*, §VIII.A, analyses of claims [12]-[27].

[28] The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

199. The Asahi-Dudderar combination renders claim [28] obvious. For example, as I discussed above in the analysis of element [1d] in Ground 1B, the combined system includes metallization along the sidewalls of hole 712 in the electric insulation layer 701 for EMI shielding, in accordance with the EMI shield metallization 41 formed using standard PCB technique. *Supra*, §IX.B (analysis

of element [1d]), IX.A (Asahi-Dudderar combination). A POSITA would have understood from Asahi that forming metal layers on a standard PCB includes the use of a metal foil. *See e.g.*, APPLE-1006, 3:39-42 (metal layers on a wiring/circuit board typically made of “at least one selected from a metal foil, a lead frame, and a conductive resin composition”), 10:1-4 (“metal foils such as a copper foil and an aluminum foil, in addition to resin films...”).

200. I also note that the construction described by Asahi and Dudderar is similar to the '909 patent's description of metal foil such as “RCC (Resin Coated Copper) foil” of a similar thickness for the copper layer (“e.g., c. 5 μm ”) as part of a standard PCB. APPLE-1001, 5:54-59. This similarity is likely due to the fact that the use of such metal foil was conventional and well-known for a standard PCB, just as Dudderar suggests. APPLE-1014, 3:24-27 (“The portion 27” of the EMI shield metallization is conveniently the standard interlevel metal of multilevel PCB 16, and the edge metallization portion 27’ may also be part of a standard PCB”). Accordingly, a POSITA, in implementing the EMI shield metallization on the sidewalls of Asahi-Dudderar's cavity, would have found it obvious to use the same “standard PCB” processing, “as thick as desired... e.g. less than 4 μm ,” in accordance with Dudderar's teachings, thereby providing a metal foil, as claimed. APPLE-1014, 3:3-4, 3:24-27, 4:45-49.

[29] The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.

201. Asahi-Dudderar renders claim [29] obvious. For example, as I discussed above in the Ground 1B analyses of element [1d] and claim [28], the enhanced combined system has metal foil covering all four sidewalls of hole 712 to provide EMI shielding. *Supra*, §IX.B. A POSITA would have understood that semiconductor 703 is surrounded by the unbroken four sidewalls of hole 712 in a lateral direction of the circuit board, and would have further understood and found obvious that the metal foil covers the entirety of all four sidewalls of hole 712 to protect the semiconductor. Accordingly, a POSITA would have found it obvious to implement the metal foil in the Asahi-Dudderar combination as an unbroken metal foil that surrounds semiconductor 703 (the recited microcircuit) in a lateral direction of the circuit board to effectuate the metal foil's intended shielding objective of Dudderar. APPLE-1014, 4:45-50, 1:102-45, FIG. 1.

[30]-[33]

202. Asahi-Dudderar includes each element of claims [30]-[33] for at least the same reasons I discussed above in the analyses of claims [25] and [26] in Ground 1A and of elements [1pre]-[1e] in Ground 1B. *Supra*, §§VIII.A, IX.B.

X. GROUND 1C: THE ASAHI-JOSHI COMBINATION RENDERS CLAIMS 12-27 OBVIOUS

203. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a

POSITA would have plainly understood that the teachings of Asahi and Joshi render obvious claims 12-27.

A. The Predictable Combination of Asahi-Joshi

204. Based on my knowledge and experience in the field and my review of Asahi and Joshi, a POSITA would have been motivated to implement Asahi's component built-in module in accordance with Joshi's teaching to form bumps 705 using various plating techniques. As I have explained above with regard to elements [12c]-[12d] in Ground 1A, Asahi describes that the component built-in module utilizes bumps 705 on the semiconductor 703 to electrically connect semiconductor 703 with the wiring board substrate – connecting the semiconductor through the bumps' connection to the wiring patterns 702a on the wiring board. *Supra*, §§VIII.A, analyses of elements [12c]-[12d]; APPLE-1006, 16:39-66; *see also id.*, 8:9-10, 10:33-45, 11:47-54, 13:27-29, 14:25-27, 15:9-12, 17:59-61. Joshi provides a straightforward suggestion for forming bumps using multiple plating techniques that result in various benefits, including “improve[d] thermal characteristics of the interconnections,” “improved chip/carrier attachment,” “improved input/output characteristics from the chip to the carrier,” “reduction in the thermal resistance between the chip and the substrate,” and improved reliability of these interconnections. APPLE-1018, 2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34,

cl. 6. A POSITA would have been motivated to implement Asahi's bumps 705 with similar plating techniques to obtain these and other benefits, as Joshi teaches.

205. In the resulting combination of Asahi and Joshi, the bumps (e.g., bumps 705) are formed by first providing "a flash coat of conductive metal (e.g., copper)" on the first surface of the semiconductor (e.g., semiconductor 703), followed by another layer of "electroplat[ed] copper." APPLE-1006, 16:39-66; APPLE-1018, 3:1-3, 3:52-68, Cl. 6.

206. A POSITA would have been prompted to implement Asahi's bumps in the combined system in accordance with Joshi's suggestions for multiple layers of flash coat and electroplated copper. As I describe in more detail in the following paragraphs, multiple reasons confirm this analysis:

207. For example, Joshi expressly articulates multiple benefits of forming bumps with multiple layers of flash coat and electroplated copper, including to achieve "improve[d] thermal characteristics of the interconnections" (APPLE-1018, 2:13-14), "improved chip/carrier attachment" (*id.*, 2:16), "improved input/output characteristics from the chip to the carrier" (*id.*, 2:20-22), "reduction in the thermal resistance between the chip and the substrate" (*id.*, 3:25-26) and improved "reliability of these interconnections" (*id.*, 4:26-27), for example, each of which a POSITA would have been motivated to avail the Asahi module of by incorporating techniques taught by Joshi. APPLE-1018, Title, Abstract, 1:6-11,

2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34, Cl. 6. Indeed, to do so would have been the application of known techniques, including the multiple plating techniques suggested by Joshi for use with multi-layer conductors, to a known system of Asahi's module utilizing copper conductors, which was ready for improvement to yield predictable results. APPLE-1006, 20:52-59.

208. Moreover, a POSITA would have had a reasonable expectation of success based on the similarity of the systems and construction techniques described by Asahi and Joshi, and Joshi describes known plating techniques suitable for such applications.

209. Both Asahi and Joshi are analogous subject matter in the same field of endeavor and reasonably pertinent to common problems associated with semiconductor packaging and manufacturing, including for the reasons note above. APPLE-1006, Title, Abstract, 1:8-12, 3:44-46, 6:33-9:17, 9:18-11:25, 11:26-12:51, 15:50-17:44, 17:55-18:13; APPLE-1018, Abstract, 1:6-11, 2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34, cl. 6. In view of the similarities between Asahi and Joshi, a POSITA would have recognized that applying Joshi's suggested plating techniques to Asahi's system would have led to predictable results and to the express benefits articulated by Joshi, all while maintaining Asahi's functionality. *See* APPLE-1019, 2:4-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34. Accordingly, a POSITA would

have had a reasonable expectation of success in making the modifications based on the similarity of the systems in Asahi and Joshi.

B. Analysis of Asahi and Joshi with Respect to Claims 12-27

210. As shown in this section, the Asahi-Joshi combination, when predictably combined for at least the reasons described above, provides claims 12-27.

[12d]/[17d]/[19d]/[20d]/[27d]

211. Elements [12d], [17d], [19d], [20d], and [27d] each recite limitations related to copper that contains at least one of electrochemically deposited and chemically deposited copper. For example, the relevant portion of element [12d] recites “contact openings in the hardened insulating polymer layer and copper in the contact openings ... wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.”

212. Even if Asahi alone does not provide these limitations – which, as I explained above in Ground 1A, it does – the Asahi-Joshi combination renders these limitations obvious. *Supra*, §VIII.A.

213. As I have discussed above in the Joshi overview (§VII.D.) and Asahi-Joshi combination (§X.A.), the combined system includes bumps formed by first providing “a flash coat of conductive metal (e.g., copper)” on the first surface of semiconductor, and then forming another metal layer over the flash coat from

“electroplating copper” (the recited electrochemically deposited copper), in accordance with Joshi’s suggestions. APPLE-1018, Title, Abstract, 1:6-11, 2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34, Cl. 6. Again, a POSITA would have recognized that electroplating, such as electrolytic plating, is an electrochemical plating technique, and that electroless plating is a chemical plating technique. In electroplating, an electric current drives a chemical reaction to deposit a layer of metal onto a conductive surface. This process involves immersing the object to be plated (the cathode) and another conductor (the anode) in an electrolyte solution containing metal ions.

214. Accordingly, the Asahi-Joshi combination provides elements [12d], [17d], [19d], [20d], and [27d] for this independent reason, because the copper bumps in the Asahi-Joshi combination are electroplated (e.g., electrochemically deposited).

215. The combination of Asahi and Joshi additionally renders these elements obvious in a second manner. As a POSITA would have recognized, and found obvious, the “flash coat” technique described by Joshi may be performed according to one of two manners—either physically or chemically (e.g., performed by Physical Vapor Deposition (PVD), or Chemical Vapor or Bath Deposition (CVD or CBD)). APPLE-1034 (corroborating evidence), [0008]-[0009]. A POSITA would have appreciated that the selection between these limited number

of techniques for performing the flash coat step of Joshi's technique amounts to an obvious design choice. The two options of either physical or chemical flash coating were well-known and identified solutions by the Critical Date that would have been readily known to a POSITA, and a POSITA would have readily selected between these limited options to effectuate the layers of copper in accordance with Joshi's suggestions. APPLE-1034, [0008] (describing electroplating of copper in a partial additive or semi-additive plating process), [0009] (describing electroless plating of copper in which copper is chemically plated). Therefore, the Asahi-Joshi combination provides not only electrochemically deposited copper as explained above, but also provides chemically deposited copper that provides a first layer of the copper in the contact openings.

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

216. Asahi-Joshi renders obvious claim [24], even if the recited process of the product-by-process element is limiting, for at least the same reasons as I previously discussed in the analysis of element [12d] above. *Supra*, §X.B.

XI. GROUND 1D: THE ASAHI-DUDDERAR-JOSHI COMBINATION RENDERS CLAIMS 1-33 OBVIOUS

217. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a

POSITA would have plainly understood that the teachings of Asahi, Dudderar and Joshi render obvious claims 1-33.

A. The Predictable Combination of Asahi-Dudderar-Joshi

218. Even if the Asahi-Dudderar combination did not provide all elements of claims 1-33 – which, as I have explained above, it does – the predictable combination of Asahi-Dudderar-Joshi would provide the elements of claim 1-33. Based on my knowledge and experience in the field and my review of Asahi, Dudderar and Joshi, a POSITA would have been motivated by Joshi to further modify the Asahi-Dudderar combination (described above) to include Joshi’s suggested methods of plating the bumps, and would have made the combination with a reasonable expectation of success, for at least the same reasons articulated above in Grounds 1B and Grounds 1C, achieving each element of Claims 1-33.

Supra §§IX.B, X.B.

219. In the combination, the Asahi-Dudderar’s bumps 705 are integrated circuit bumps grown on the chip to provide connection between the chip and the substrate. *Supra*, §IX.A (Asahi-Dudderar combination). However, Asahi does not expressly articulate full implementation details of the specific materials and processes for forming the bumps. A POSITA would have looked to similar references, like Joshi, for additional details about how to provide the bumps described in Asahi. A POSITA would have found that Joshi provides a

straightforward example of such implementation details, as described above.

Supra, §§X.B, X.A (Asahi-Joshi Combination).

220. In the combination, a POSITA would have formed Asahi-Dudderar-Joshi's bumps 705 in a similar fashion, with a "flash coat" on the surface of semiconductor 703, followed by another copper layer from "electroplating copper," in accordance with Joshi and to achieve the benefits Joshi describes. *Supra*, §X.A (Asahi-Joshi Combination). For the reasons I explained above, the combination of Asahi-Dudderar-Joshi provides all elements of claims 1-33.

XII. GROUND 2A: CLAIMS 12-27 ARE OBVIOUS IN VIEW OF HAYASHI

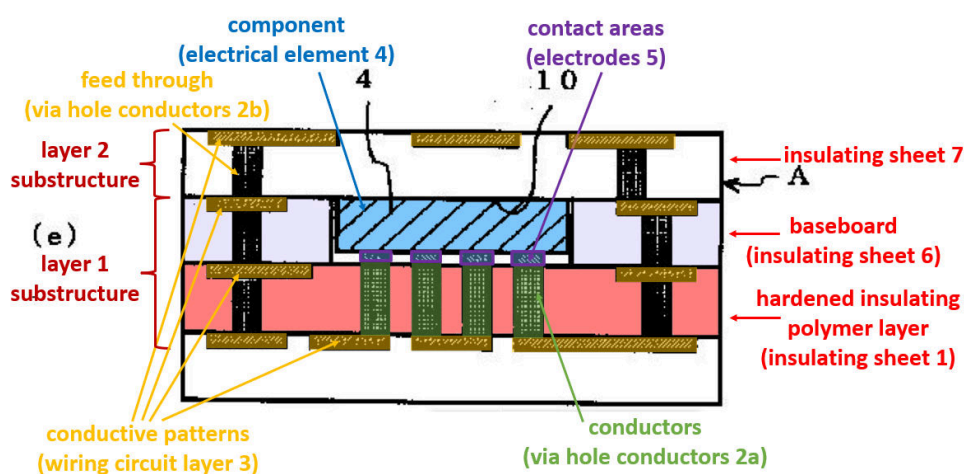
221. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art cited herein, claims 12-27 are rendered obvious by Hayashi.

A. Analysis of Hayashi with Respect to Claims 12-27

[12pre] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:

222. Hayashi discloses [12pre] in at least two manners. First, as illustrated below in annotated FIG. 1(e), Hayashi describes a first circuit board substructure (labeled "layer 1 substructure") provided by "insulating sheet 6," "insulating sheet 1," "wiring circuit layer 3" in these insulating sheets, "via hole conductors 2a," and "via-hole conductors 2b" through these layers. APPLE-1011, FIGS. 1(a)-(e); cl. 1,

[0001], [0009], [0015], [0016], [0017]. Hayashi also provides a second circuit board substructure, noted in annotated FIG. 1(e) below (as “layer 2 substructure”), which is provided by “insulating sheet 7,” “via-hole conductors 2b” through “insulating sheet 7,” and “top wiring circuit layer 3” on the surface of insulating sheet 7. APPLE-1011, FIGS. 1(a)-(e); cl. 1, [0001], [0009], [0015], [0016], [0017]. As illustrated below, the layer 2 circuit board substructure is on top of the layer 1 circuit board substructure. *Id.*, FIG. 1(e).



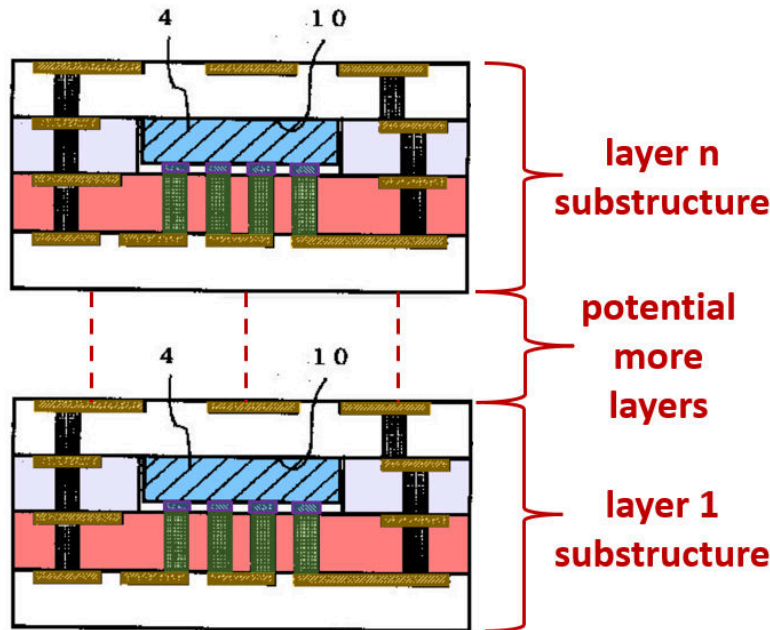
APPLE-1011, FIG. 1(e) (Annotated)

223. Hayashi also discloses [12pre] in a second manner, through its description of multiple insulating layers and multiple electrical components in different layers. APPLE-1011, [0004] (desire for “high-density mounting of a plurality of electrical elements”), [0007] (“the mounting density of the elements can be increased”), [0009], [0012], [0021], [0024], [0025], [0028], [0032], [0034] (“an electrical element mounted wiring board that can easily provide not only a

single but also a plurality of electrical elements inside the wiring board, thereby reducing the size of the wiring board and increasing the mounting density of the electrical elements can be provided”), [0036]-[0038], [0041], [0042], FIGS. 1(b)-(e).

224. For example, Hayashi describes “a plurality of electrical elements can be provided by forming a plurality of void portions in the same or different layers in a multilayer wiring substrate to stow and mount the electrical elements.”

APPLE-1011, [0032], [0034]. Hayashi thus describes that the module can include a multilayered configuration (the recited multi-layered circuit board) with multiple layers of substructures (the recited at least two circuit board substructures), each of which may contain one or more electrical elements. *Id.* In this express implementation, the multi-layered wiring board has similar substructures on top each other, each substructure having electrical elements such as semiconductors or memory chips embedded in insulating sheets. *Supra*, §VII.B. (Hayashi overview). I have annotated the below composite figure to illustrate this multi-layered circuit board configuration described by Hayashi.



Composite Based on APPLE-1011, FIG. 1(e) (Annotated)

225. Moreover, a POSITA would have found the use of multiple such layers obvious, in order to effectuate Hayashi's stated objectives, with a reasonable expectation of success in electrical connecting such layers using Hayashi's express techniques. *See e.g.*, APPLE-1011, [0004] (desire for "high-density mounting of a plurality of electrical elements"), [0007] ("the mounting density of the elements can be increased"), [0034] (multi-layered wiring board with multiple elements "reducing the size of the wiring board and increasing the mounting density of the electrical elements can be provided"). *Supra*, §VIII.A (Asahi ground), analysis of element [12pre] (discussion on the conventional use of multi-layered structures in component built-in devices and around corroborating prior art references).

226. As illustrated in the annotated composite FIG. 1(e) above, each substructure of Hayashi's multi-layered wiring board, such as the layer 1 substructure and layer n ($n \geq 2$) substructure (the recited "at least two circuit board substructures on top of each other") has the same or similar structure.

Accordingly, in the below discussions related to Hayashi's disclosure of the remaining elements of claim 12, according to Hayashi's second manner of disclosing the claim elements, I focus on the structure shown in FIG. 1(e) as the recited "at least one of said circuit board substructures."

227. Hayashi describes that in its wiring board including "an insulating substrate obtained by laminating a plurality of insulating layers containing at least a thermosetting resin," for example an "epoxy resin," the plurality of insulating layers make up a combined circuit board with each insulating layer itself constituting a circuit board. APPLE-1011, Cl. 1, [0001], [0009], [0015] (listing "epoxy resin" as one of example material for the thermosetting resin forming the insulating sheet), [0016] ("inorganic filler such as SiO_2 ," "A woven fabric, non-woven fabric composed of glass or aramid resin, etc. impregnated with one of the resins described above may also be used."), [0017], [0041].

228. I note that this disclosure is just like the '909 patent's description for its "baseboard 1 [] selected for the circuit-board manufacturing process," such as

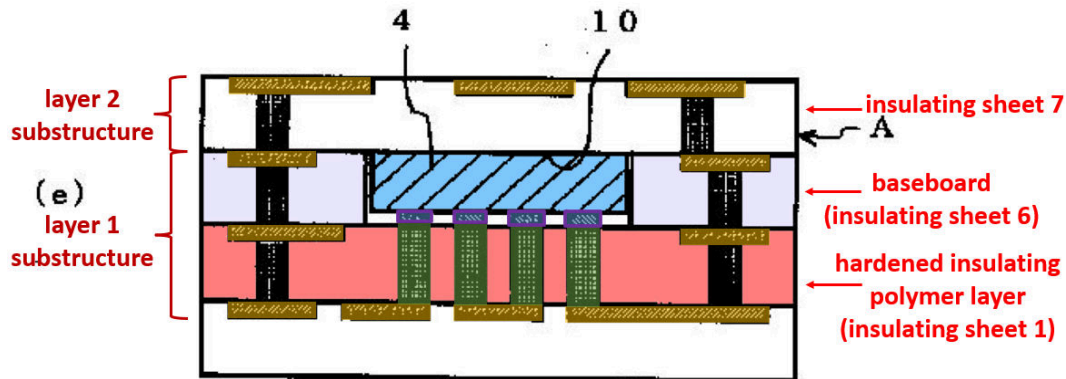
“a glass-fibre reinforced epoxy board, such as an FR4-type board,” “an organic board,” or “an inorganic board.” APPLE-1001, 3:46-55, cl. 9..

[12a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

229. Hayashi provides element [12a] under each of the two mappings discussed above with regard to element [12pre]. *Supra* §XII.A.

230. Consistent with the first mapping of element [12pre], Hayashi’s multilayered wiring board includes an insulating material layer including a baseboard (e.g., “insulating sheet 6”) and a hardened insulating polymer layer (e.g., “insulating sheet 1”). APPLE-1011, [0001] (“a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate”), [0028], [0039]; FIG. 1(a)-1(e); *supra*, §XII.A., analysis of element [12pre]. Hayashi describes that “an opening 9 for housing the electrical element 4 is formed in insulating sheet 6 and laminated directly above insulating sheet 1 so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7.” APPLE-1011, [0028], FIG. 1(e); *see also* [0001] (“a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate”), [0039] (“an opening slightly larger than the size of the electrical element was formed by punching an insulating sheet b, in which the via-hole conductors had been formed and on which the wiring circuit layer had been formed in the same manner as described above,

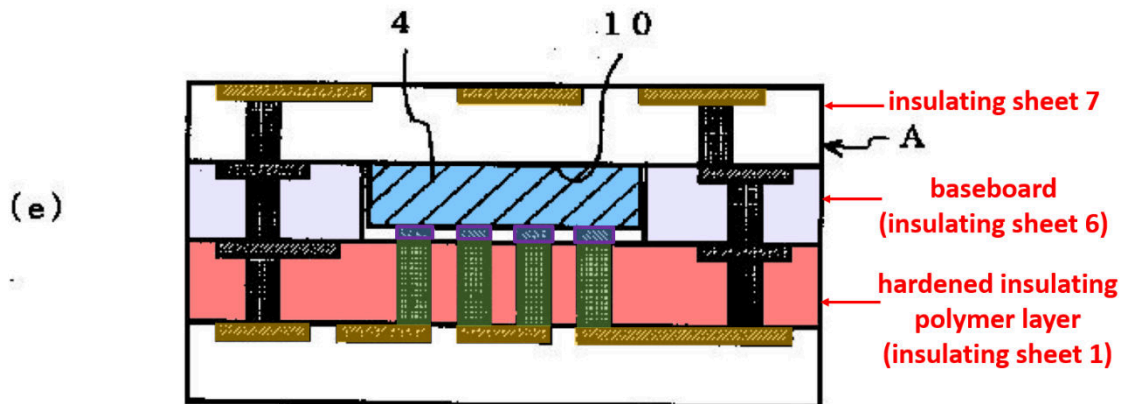
and the insulating sheets were laminated to the thickness of the electrical element.”). The annotated FIG. 1(e) below illustrates this configuration and mapping option.



APPLE-1011, FIG. 1(e) (Annotated)

231. Hayashi additionally provides [12a] in the second manner, consistent with the second mapping of [12pre]. *Supra* §XII.A. In particular, consistent with the second mapping, Hayashi’s “insulating sheet 1” provides the recited hardened insulating polymer layer, and the “insulating sheet 6,” alone or together with “insulating sheet 7,” provides the recited baseboard. Together, these layers (e.g., the insulating sheet 1 and insulating sheet 6 alone or with insulating sheet 7) provide the recited insulating material layer. APPLE-1011, FIG. 1(a), [0028] (“an opening 9 for housing the electrical element 4 is formed in insulating sheet 6 and laminated directly above insulating sheet 1 so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7.”), [0012], [0015], [0017], [0029]. The annotated FIG. 1(e) below illustrates this

configuration for any of the multiple substructure layers of Hayashi's multi-layered circuit board, according to the second mapping option that I previously discussed in the analysis of element [12pre]. *Supra* §XII.A.



APPLE-1011, FIG. 1(e) (Annotated)

232. Hayashi explains that the insulating sheets of the multilayer wiring board are made of insulating material such as “epoxy resin.” APPLE-1011, [0015] (“Note that the thermosetting resin forming the insulating sheet is not particularly limited as long as the thermosetting resin has electrical characteristics, heat resistance, and mechanical strength as an insulating material. For example, an aramid resin, phenol resin, epoxy resin, imide resin, fluororesin, phenylene ether resin, bismaleimide-triazine resin, urea resin, melamine resin, silicone resin, urethane resin, unsaturated polyester resin, or allyl resin, etc. can be used alone or in combination.”). As I explained above, based on my review of Hayashi and the ’909 patent, I note that Hayashi’s insulating sheets contain the same type of

material, such as “epoxy resin” that may be reinforced through impregnating a “woven fabric” or “non-woven fabric composed of glass,” as the ’909 patent’s description for its baseboard of the circuit board. *Supra*, §XII.A, analysis of element [12pre]; *see also* APPLE-1011, [0016] (“a filler can be compounded with an organic resin in the insulating sheet 1 described above to increase the strength of an insulating substrate or wiring substrate as a whole. An inorganic filler such as SiO₂, ... is preferably used as the filler compounded with the organic resin.”). A POSITA would have recognized that “SiO₂” is the chemical symbol for a type of glass. Accordingly, Hayashi’s insulating sheet 6 (alone or in combination with insulating sheet 7) provides the recited baseboard.

233. Hayashi’s insulating sheet 1 provides the hardened insulating polymer layer, as claimed. For example, Hayashi explains that “a soft (B-stage state) insulating sheet 1 containing a thermosetting resin with thermosetting temperature T₁ is formed and via-holes passing through in the thickness direction are formed in the insulating sheet 1.” APPLE-1011, [0012]. Hayashi describes that the insulating sheet 1 contains polymer, such as “epoxy resin.” *Id.*, [0015]. Hayashi further explains that insulating sheet 1 is hardened through a curing process, as the “laminate ... is heated at or above the thermosetting temperature T₁ of the thermosetting resin in the insulating sheet 1 to fully cure the insulating sheets 1, 6,

7.”. APPLE-1011, [0029]; *see also id.*, [0010], [0012], [0013], [0019], [0032], [0035], [0040], cls. 1, 2.

[12b] conductive patterns on both sides of the insulating material layer;

234. Hayashi provides element [12b] under each of the two mappings discussed above with regard to element [12pre]. *Supra* §XII.A.

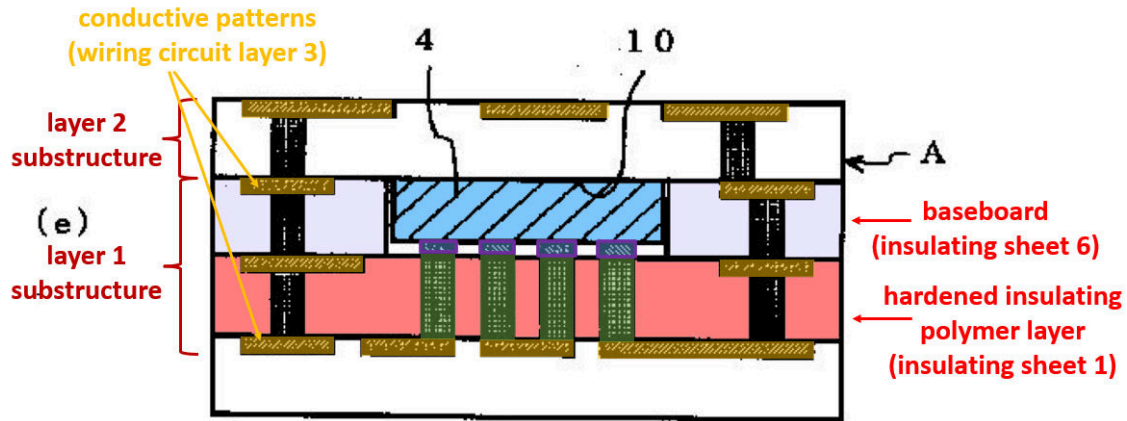
235. For example, Hayashi describes “wiring circuit layer 3” that can be provided on either or both sides of each insulating sheet 1, 6, 7, with these insulating sheets then laminated together resulting in the formation of the entire insulating substrate. APPLE-1011, FIG. 1, Cl. 1, [0009], [0012], [0021]. For example, Hayashi describes that “as shown in FIG. 1 (b), a wiring circuit layer 3 is formed on the front or back surface of the insulating sheet 1, as appropriate.” APPLE-1011, [0024]; *see also id.*, [0009] (“a wiring circuit layer formed on the surface and inside of the insulating substrate”). *Supra*, §VII.B. (Hayashi overview).

236. Wiring circuit layers 3 are patterned. *Id.*, [0024] (forming the wiring circuit layer 3 by “1) affixing metal foil to a surface of the insulating sheet 1 and performing etching to form a circuit pattern; 2) ... 3) affixing metal foil to a transfer film surface, etching the metal foil to form a circuit pattern, ...”), [0025], [0028], [0036] (“an adhesive was applied to a surface of a transfer sheet containing a polyethylene terephthalate (PET) resin, and copper foil with a thickness of 12 μm

and a surface roughness of 0.8 μm was affixed. A photoresist (dry film) was then applied, exposed to light and developed, and then immersed in a ferric chloride solution to etch away the non-patterned portion and form a wiring circuit layer. The resulting wiring circuit layer had a fine pattern with a line width of 20 μm and a spacing of 20 μm between wiring.”), [0037]-[0038], [0041], FIGS. 1(b)-(e).

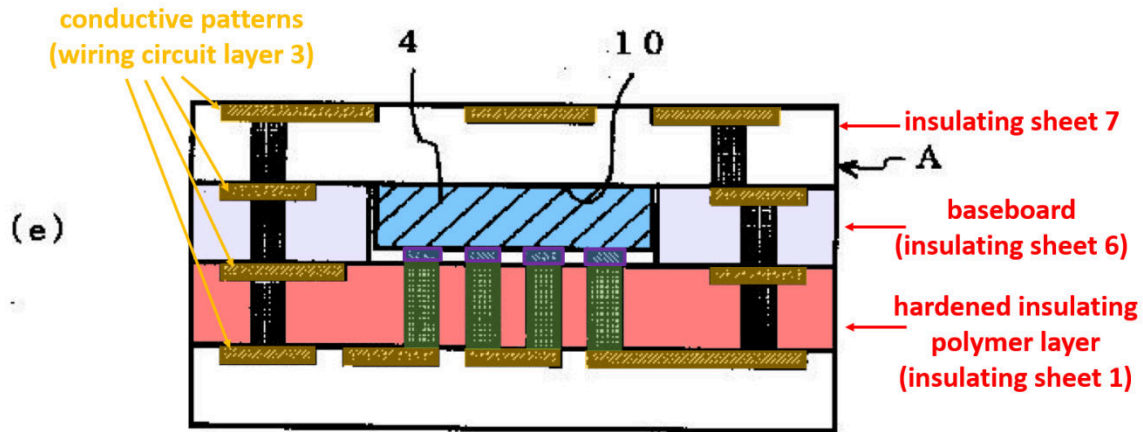
237. Accordingly, based on my review of Hayashi, the patterned wiring circuit layers 3 (the recited conductive patterns) are provided on both sides of the entire insulating substrate made of insulating sheets 1, 6, 7. Alternatively, when only insulating sheets 1 and 6 map to the recited insulating material layer, wiring circuit layers 3 are also on located both sides of this insulating material layer. APPLE-1011, FIG. 1(e).

238. To illustrate, I provide below annotated FIG. 1(e) showing how Hayashi provides [12b] in the first manner as I previously discussed in the analyses of elements [12pre] and [12a], with wiring circuit layers 3 located on both sides (e.g., on a top and a bottom side) of the insulating material layer comprised of insulating sheets 1 and 6, within the layer 1 circuit board substructure. *Supra*, §XII.A.



APPLE-1011, FIG. 1(e) (Annotated)

239. In another annotated FIG. 1(e) below, I illustrate how Hayashi also provides [12b] according to the second manner, focusing on one substructure layer (e.g., the layer 1 substructure) of the stack-up multilayered configuration that I previously discussed in the analyses of elements [12pre] and [12a]. *Supra*, §XII.A. As I explained above, in this configuration the wiring circuit layers 3 (the recited conductive patterns) are located on both sides of the insulating material layer composed of insulating sheets 1 and 6 alone or together with insulating sheet 7. APPLE-1011, FIG. 1.



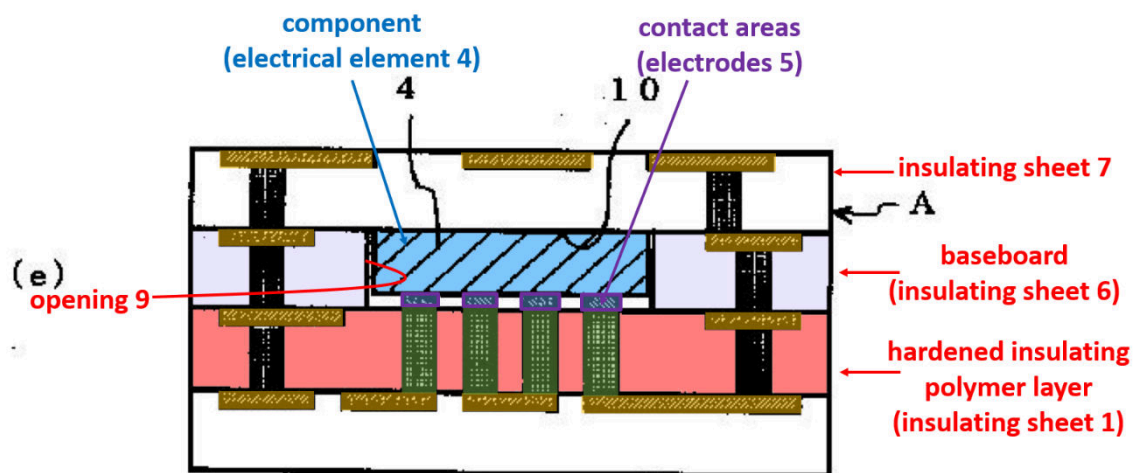
APPLE-1011, FIG. 1(e) (Annotated)

[12c] at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and

240. Hayashi provides element [12c]. Hayashi describes at least one microcircuit (e.g., “electrical element 4”) embedded in the insulating material layer (e.g., insulating sheets 1 and 6 in the first mapping, and insulating sheets 1 and 6 alone or in combination with insulating sheet 7 in the second mapping) in a hole in the baseboard (e.g., opening 9 in insulating sheet 6). For example, Hayashi describes an “electrical element 4,” such as a semiconductor element, embedded in an opening 9 of the wiring substrate, e.g., in insulating sheet 6. APPLE-1011, Title, cls. 1, 2, [0001]-[0003], [0005], [0007], [0026], [0027]-[0028] (“an opening 9 for housing the electrical element 4 is formed in insulating sheet 6 and laminated

directly above insulating sheet 1 so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7”), [0031] (“as shown in FIG. 1 (e), the electrical element 4 is housed and mounted in a hermetically sealed void 10 inside a multilayer wiring substrate A”), [0038] (“a silicon semiconductor memory chip” as an example of the electrical element), [0039] (“an opening slightly larger than the size of the electrical element was formed by punching an insulating sheet b”), [0040]-[0041] (“IC element” as an example), FIG. 1(e); *Supra*, §VII.B. (Hayashi overview).

241. Annotated FIG. 1(e) below shows this configuration, with electrical element 4 embedded in opening 9 within insulating sheet 6 (the recited baseboard) as part of the multilayer wiring board A.



APPLE-1011, FIG. 1(e) (Annotated)

242. A POSITA would have understood that “IC” (integrated circuit) elements, are a type of microcircuit, as microcircuits are miniaturized electronic

circuits that contain a network of interconnected semiconductor devices (e.g., transistors and diodes) and passive components (e.g., resistors, inductors, and capacitors), on a small substrate, and integrated circuits are essentially advanced microcircuits where all these components are fabricated onto a single semiconductor wafer.

243. Hayashi's electric element 4 (the recited microcircuit) has contact areas (e.g., "electrodes 5", depicted in FIG. 1(e) as contact pads) on a first surface, the first surface being against the hardened insulating polymer layer (e.g., "insulating sheet 1").

244. For example, Hayashi describes that "an electrical element 4 is mounted on the surface of the insulating sheet 1, and the electrodes 5 formed on the back surface of the electrical element 4 are brought into contact with the exposed portions on the end surfaces of the via-hole conductors 2a." APPLE-1011, [0026]; *see also*, [0030], [0038], FIGS. 1(c), 1(e). This "back surface" having "electrodes 5" (the recited contact areas) thereon for making electrical contacts thus provides the claimed first surface.

245. Alternatively, Hayashi provides the recited contact areas in a second manner through its disclosure of flat areas on the back surface of electrical element 4, from which electrodes 5 extend.

246. Based on my analysis of Hayashi, in the finished module, the first surface of the electrical element 4 is against the insulating sheet 1 (the recited hardened insulating polymer layer).

247. For example, although Figure 1(e) shows a gap or void between the first surface of the electrical element and insulating sheet 1 in a depicted cross-section, Hayashi explains that any gaps will be minimized to leave “almost no void.” APPLE-1011, FIG. 1(e), [0040]; *see also* [0032] (“it is preferable to make the thermosetting resin flow before curing to minimize a void with an insulating phase at the periphery of the electrical element 4 to improve reliability.”).

248. Hayashi further explains that “it is preferable to make the thermosetting resin [of the insulating sheets] flow before curing to minimize a gap with an insulating phase at the periphery of the electrical element 4 to improve reliability.” APPLE-1011, FIG. 1(e), [0032]. “The opening in the insulating sheet contracted due to the flow of resin caused by heating, and the insulating layer and the chip were bonded closely together, leaving almost no void between the chip and the insulating layer.” *Id.*, [0040].

249. Accordingly, a POSITA would have understood that in the resulting module, at least a portion of the first surface of the electrical element is in direct contact with the insulating sheet 1, due to the flow of the insulating layer resin, such that the first surface of the component is against the hardened insulating

polymer layer. In my opinion, a POSITA would understand that the plain language of element [12c] reciting “against” does not indicate that there is no gap anywhere between the first surface and the hardened insulating polymer layer.

250. Furthermore, based on my knowledge and experience in the field and my review of Hayashi, a POSITA would have found it obvious, based on Hayashi’s express preference to minimize a void between the first surface of electrical element 4 and a surface of insulating sheet 1 (the recited hardened insulating polymer layer), to flow the resin such that the first surface of the electrical element and the insulating sheet are in direct contact in the finished module. A POSITA would have been prompted, based on Hayashi’s suggestions, to achieve improved reliability and structural integrity due to two surfaces touching (thus against each other) at least in some places, without needing to eliminate all gaps completely across the entirety of the first surface.

251. A POSITA would have recognized that these benefits would result from contact in at least in some places without needing to eliminate all gaps completely across the entirety of the first surface of electrical element 4, or by providing contact completely across the entirety of the first surface. Contact between electrical element 4 and insulating sheet 1 would have predictably helped maintain electrical element 4 securely in place, which also promotes secured mechanical and electrical connection between electrodes 5 of electrical element 4

and the via-hole conductors in the insulating sheet 1 (discussed in more detail below for element [12d]).

252. Based on my knowledge and experience in the field, a POSITA would have had a reasonable expectation of success, especially because Hayashi expressly teaches the flow of resin for the purpose of minimizing potential void, and promoting contact, between the electrical component and insulating layer.

253. This analysis applies for both the first and second manners of satisfying two circuit board substructures as discussed in §XII.A, analysis of element [12pre]. In both mappings, electrical element 4 is embedded in insulating sheet 6 as I explained above.

[12d] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

254. Hayashi provides element [12d]. As discussed above, element [12d] recites what I understand to be a “product-by-process element” that is not limiting for purposes of determining invalidity. *Supra*, §VIII.A (explaining in element [12d] analysis that it is enough to show the presence of copper in the contact openings for purpose of invalidity).

255. Nonetheless, even if the recited process of the “product-by-process element” is found to be limiting on the claim, Hayashi renders obvious element

[12d]. Hayashi's electronic module has conductors (e.g., "via-hole conductors 2a") within the hardened insulating polymer layer (e.g., "insulating sheet 1") for forming electrical contacts between at least some of the conductive patterns (e.g., "wiring circuit layer 3") and at least some of the contact areas (e.g., "electrodes 5") of the component. For example, Hayashi describes that the "via-holes passing through in the thickness direction are formed in the insulating sheet 1," and "the via-holes that are connected to the electrodes of the electrical element are filled with an conductive paste while performing screen printing or suctioning to form via-hole conductors 2a for connecting the electrical element." APPLE-1011, [0012].

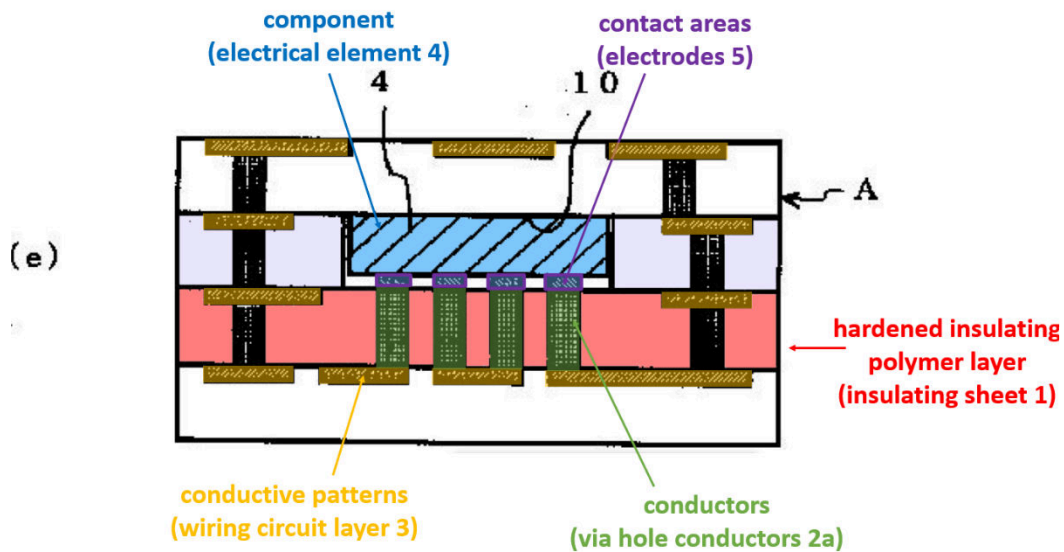
256. Accordingly, Hayashi discloses that via-hole conductors 2a are connected to the electrodes 5 of electrical element 4 and also connected with wiring circuit 3 (the recited conductive patterns), such that electrical element 4 is electrically connected to the wiring board. *Id.*, [0012], [0018] ("the via-hole conductors 2a connected to the electrodes of the electrical element"), [0026] ("the electrodes 5 formed on the back surface of the electrical element 4 are brought into contact with the exposed portions on the end surfaces of the via-hole conductors 2a"), [0030] ("the electrodes 5 of the electrical element 4 and the via-hole conductors 2a can be electrically connected"), [0031] ("a multilayer wiring

substrate can be fabricated that has electrical elements inside voids 10 electrically connected to via-hole conductors 2a”), [0038], [0041]-[0042], cls, 1 & 2, FIG. 1(e).

257. As discussed above, electrodes 5 (e.g., contact pads) provide the recited contact areas of electrical element 4; and, alternatively, the flat areas on the back surface of electrical element 4 from which electrodes 5 extend likewise independently provide the recited contact areas. *Supra*, §XII.A, analysis of element [12c]. For both manners in which Hayashi provides the recited contact areas, via-hole conductors 2a are in electrical contact with at least some of the contact areas of the electrical element 4, either in direct physical contact (first manner in which electrodes 5 provide the claimed contact areas), or in electrical contact through electrodes 5 (the second manner).

258. To be clear, the via-hole conductors 2a are also in electrical contact with the wiring circuit 3 (the recited at least some of the conductive patterns). *See e.g., id.*, FIG. 1, [0034] (“The manufacturing method of the present invention allows for the connection of electrical elements to a wiring substrate...”), [0041] (“After observing the area around the formation of the wiring circuit layers and via-hole conductors in the cross section for the resulting multilayer wiring board, it was found that the IC element and the via-hole conductors were in a proper connected state due to melting of the low melting point metal in the via-hole conductors. In conductivity testing of the wiring, no disconnected wiring was

observed.”), [0042]. The annotated figure below shows via hole conductors 2a within insulating sheet 1 (the recited hardened insulating polymer layer) for forming electrical contacts between wiring circuit layer 3 (the recited at least some of the conductive patterns) and electrodes 5 (the recited at least some of the contact areas) of electrical element 4.



APPLE-1011, FIG. 1(e) (Annotated)

259. Additionally, Hayashi describes that the via hole conductors 2a contain copper. For example, Hayashi describes that via hole for forming via-hole conductors 2a “are filled with an [*sic*] conductive paste” containing “a low melting point metal having low melting point T_2 , which is equal to or lower than thermosetting temperature T_1 of the thermosetting resin, and a high melting point metal having a melting point” higher than T_1 . APPLE-1011, [0012]. Hayashi further explains, “tin (Sn), zinc (Zn), bismuth (Bi), or an alloy thereof with silver

(Ag) or copper (Cu), etc. is preferred as the low melting point metal,” while

“[c]opper, silver, a copper-silver alloy, or any mixture thereof is preferably used as the high melting point metal.” APPLE-1011, [0018], [0020].

260. In more detail, Hayashi discloses, “conductive paste consisted of a metal component composed of 50 vol% copper powder with an average particle size of 5 μm plated with silver and 50 vol% Sn-Pb eutectic solder powder with an average particle size of 3 μm (melting point $T_2 = 183^\circ\text{C}$) serving as the low melting point metal[.]” *Id.*, [0035]. Based on Hayashi’s express teachings of the use of copper and copper powder plated with silver, a POSITA would have understood and found obvious the use of other core materials (metal or non-metal) plated with copper, formed with conventional plating techniques, such as electroless chemical plating. (the recited at least one of electrochemically deposited copper and chemically deposited copper). APPLE-1011, [0035] (describing the use of a conductive paste formed from copper powder plated with silver); APPLE-1017 (corroborating prior art), 12 (“the conductive particles can be, for example, particles of metals such as Au, Ag, Cu, or solder, and a conductive layer of Ni, Cu, Au, or solder is preferably provided on a spherical polymer core material such as polystyrene. A surface layer of Su [*sic*], Au, solder, etc. can also be formed on the surface of conductive particles.”). A POSITA would have understood that electroless chemical plating would have been preferred when plating a powder

since for a powder it is more difficult to make an electrical connection to each particle in the powder as required in electrochemical plating.

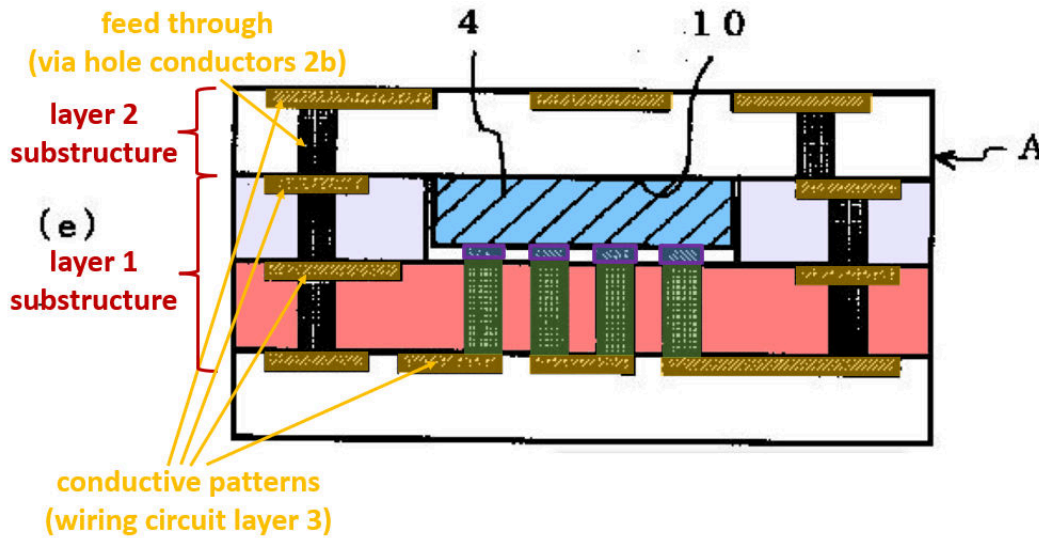
261. Indeed, a POSITA would have recognized and found obvious, from Hayashi's description, that copper-plated core materials would have similarly effectuated Hayashi's objectives for its conductive paste, especially because both copper and silver are identified design options by Hayashi for the metal component in the conductive paste, and Hayashi describes copper, silver, a copper-silver alloy, or any mixture thereof as equivalent alternatives. APPLE-1011, [0021] ("The via-hole conductors 2b that are not connected to the electrical element do not require a low melting point metal, and can be filled with a conductive paste containing a metal powder having a high melting point, such as ordinary copper, silver, or any alloy thereof"), [0035]. Moreover, a POSITA would have been prompted to utilize a copper-plated material to utilize a known composition readily available and facilitating low-cost manufacturing, and would have had a reasonable expectation of success in doing so in view of the known use of such materials in similar applications.

262. The above analysis applies for both the first and second manners of satisfying two circuit board substructures as I previously discussed in the analysis of element [12pre] (§XII.A.). I note that the connection structure between

electrodes 5 and bottom wiring circuit layer 3 is within insulating sheet 1 of both options.

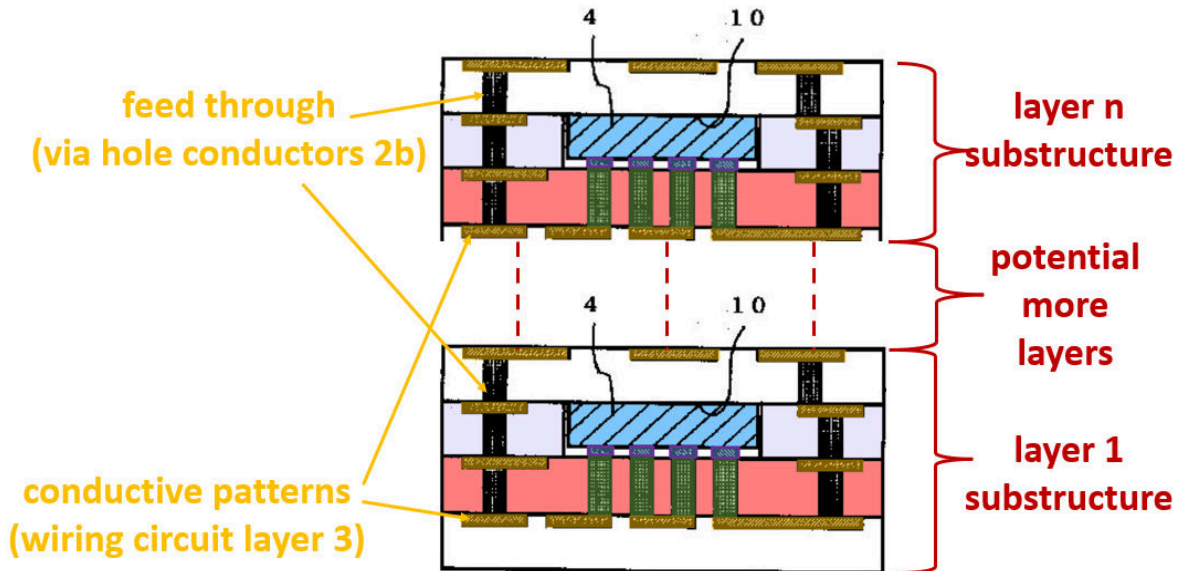
[13] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

263. Hayashi provides claim [13]. As I previously discussed in the analysis of element [12pre], Hayashi describes at least two circuit board substructures on top of each other, under at least two mappings. *Supra* §XII.A. Additionally, Hayashi discloses that the circuit board substructures are electrically connected to each other by “via-hole conductors 2b” formed on each of the laminated insulating sheets 1, 6, 7, 8 and in connection with wiring circuit layers 3 of the insulating sheets. APPLE-1011, [0012], [0028], FIGS. 1(a)-(e). In the below annotated figure showing layer 1 and 2 substructures on top of each other, the two substructures are electrically connected to each other by the via hole conductors 2b and the wiring circuit layers 3 of each insulating sheet in a first manner. *Supra*, §XII.A, analysis of element [12pre].



APPLE-1011, FIG. 1(e) (Annotated)

264. According to the second manner of forming a multilayered structure, as I discussed above in §XII.A, analysis of element [12pre], a POSITA would have understood and found obvious that when multiple substructure layers like in FIG. 1(e) are laminated on top of each other, the various substructures are electrically connected to each other through the “via-hole conductors 2b” and wiring circuit layers 3. APPLE-1011, [0032], [0034]. A POSITA would have understood that by connecting the substructures to one another through the via-hole conductors and wiring circuit layers, a multilayered functioning totality is formed, in accordance with Hayashi’s suggestions. APPLE-1011, [0032], [0034]. The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1011, FIG. 1(e) (Annotated)

[14] The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.

265. Hayashi renders obvious claim [14] for at least the same reasons as I previously discussed in the analysis of element [12pre]. *Supra*, §XII.A; APPLE-1011, [0032] (“a plurality of electrical elements can be provided ... in the same or different layers”), [0034]; *see also* §XII.A, analysis of element [12c] (electrical elements include microcircuits). As I have explained above, it was well-known by the Critical Date to embed a plurality of microcircuits in an insulating material layer or substrate. *See e.g.*, corroborating references APPLE-1008, [0044], [0045], [0047], [0053], [0054], FIGS. 1-7, 9-21; APPLE-1014, 1:15-16, 2:44-46, 4:66-5:3, FIGS. 1, 2.

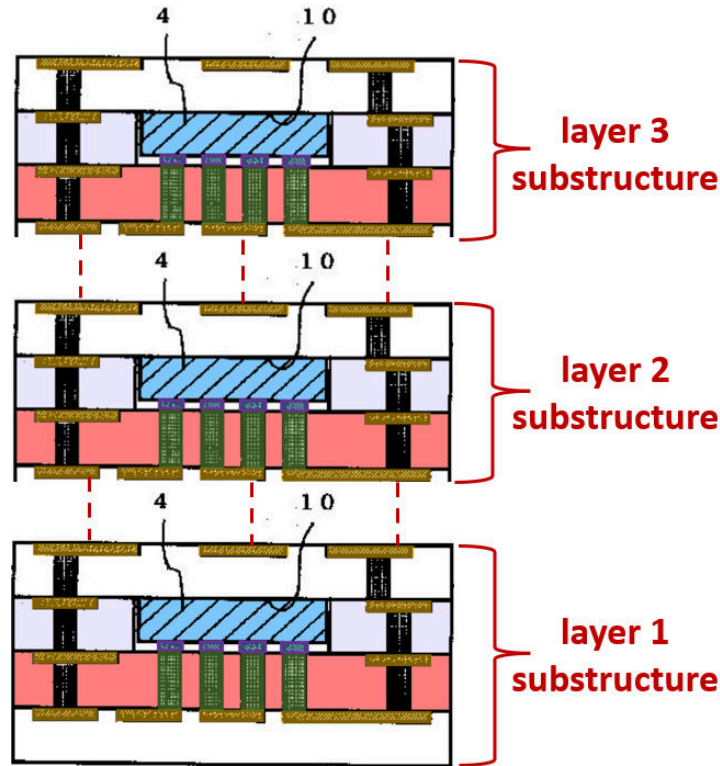
[15] The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.

266. Hayashi renders obvious claim [15] for at least the same reasons as I previously discussed in the analysis of element [12pre] (“second manner”). *Supra*, §XII.A; APPLE-1011, [0032] (“a plurality of electrical elements can be provided ... in the same or different layers”), [0034]; *see also supra*, §XII.A, analysis of element [12c]; APPLE-1011, [0038] (describing “silicon semiconductor memory chip[s]”).

[16] The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.

267. Hayashi renders obvious claim [16] for at least the same reasons as I previously discussed in the analysis of element [12pre]. *Supra*, §XII.A.

268. For example, below I provide a composite figure illustrating at least three similar circuit board substructures laminated on top of each other with potential other layers such as additional insulating sheets in between, with wiring circuit layers 3 and via hole conductors 2b on each substructure to electrically connect the substructures to each other, in accordance with Hayashi’s teachings, to achieve a high component density, compact configuration. *See supra*, §XII.A, analysis of claim [13] (discussion on how two circuit board substructures are electrically connected to each other).



Composite Based on APPLE-1011, FIG. 1(e) (Annotated)

[17pre]-[17d] The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise an insulating material layer including a baseboard and a hardened insulating polymer layer, conductive patterns on both sides of the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

269. Hayashi renders obvious the elements of claim [17] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d] (“second manner”). *Supra*, §XII.A.

[18] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.

270. Hayashi renders obvious claim [18] for at least the same reasons as I previously discussed in the analyses of claims [13] and [16]. *Supra*, §XII.A.

[19pre]-[19d] The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, conductive patterns on both sides of the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

271. Hayashi renders obvious the elements of claim [19] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d] and claim [18]. *Supra*, §XII.A.

[20pre]-[20d] The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, a conductive pattern on the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

272. Hayashi renders obvious the elements of claim [20] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d] (“second manner”) and claim [19]. *Supra*, §XII.A.

[21] The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.

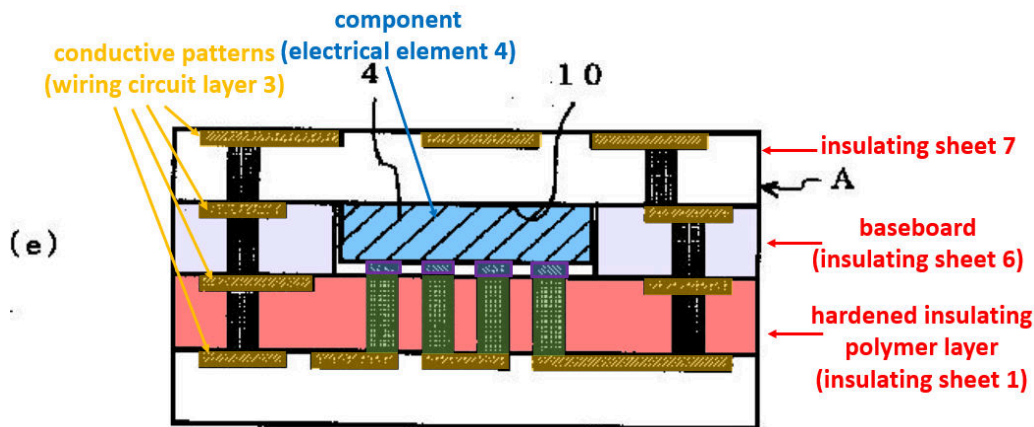
273. Hayashi renders obvious claim [21] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d] (*see* discussion of how insulating sheet 1 contains epoxy resin) and claim [20]. *Supra*, §XII.A.

[22] The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.

274. Hayashi renders obvious claim [22] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12a] (*see* discussion of how insulating sheets contain “epoxy resin” and a “woven fabric, non-woven fabric composed of glass”) and claim [20]. *Supra*, §XII.A.

[23] The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.

275. Hayashi renders obvious claim [23] for at least the same reasons as I previously discussed in the analyses of elements [12b]-[12c]. *Supra*, §XII.A; APPLE-1011, FIG. 1(e) (showing electrical element 4 located in between wiring circuit layers 3 on both sides of the insulating material layer composed of insulating sheets 1 and 6 (or 1, 6 and 7)).



APPLE-1011, FIG. 1(e) (Annotated)

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

276. Hayashi renders obvious claim [24], even if the recited processes of the “product-by-process element” are considered limiting to the claim for purposes of determining invalidity. *Supra*, §VIII.A (Asahi ground) (discussion related to the

requirements of the claim and it being enough to show recited copper layers for purpose of invalidity).

277. As I previously discussed in the analysis of element [12d] (*supra* §XII.A), a POSITA would have understood and found obvious to use a core plated with one or more layers of copper, as the metal component of conductive paste of via hole conductors 2a, using common plating techniques including electroless chemical plating (chemically deposited copper). APPLE-1011, [0021] (“The via-hole conductors 2b that are not connected to the electrical element do not require a low melting point metal, and can be filled with a conductive paste containing a metal powder having a high melting point, such as ordinary copper, silver, or any alloy thereof”), [0035]; *see also* APPLE-1017, (corroborating reference describing that “conductive particles can be, for example, particles of metals such as Au, Ag, Cu or solder, and a conductive layer of Ni, Cu, Au, or solder is preferably provided on a spherical polymer core material such as polystyrene [and a] surface layer of Su, Au, solder, etc. can also be formed on the surface of conductive particles.”).

278. Based on my knowledge and experience in the field and my review of Hayashi, a POSITA would have found it obvious, from Hayashi’s teachings of land areas over via hole conductors, to apply a second layer of copper on the via hole conductors by forming land areas over the via hole conductors. Hayashi expressly illustrates lands provided by wiring circuit layer 3 on both ends of via

hole conductors 2b. APPLE-1011, Figs. 1(b)-(e), [0024], [0028]. Similarly, Hayashi also illustrates conductor pads, also provided by wiring circuit layer 3, on the bottom ends of via hole conductors 2a. *Id.* A POSITA would have understood that the use of lands (and conductor pads) provided on via hole conductors was a common technique by the Critical Date, which was known to a POSITA to enhance the device by facilitating alignment and electrical connections between the vias and/or between the vias and component electrodes (e.g., Hayashi's electrodes 5). *See e.g.*, APPLE-1016 (corroborating prior art) [0011] ("The copper foil on the insulating substrate 6 is patterned into a shape with lands 17 on top of the connecting electrodes 7 and other regions as well as wiring 8 that is electrically connected to the semiconductor element 5.") [0012] ("lands 3 are formed on the connecting electrodes"), [0015] (wiring patterns and lands formed at the same time); APPLE-1027 (corroborating prior art), cl. 8 (forming lands on a surface of the second insulating layer that are connected conductively to the conductors in the via holes; and mounting an electronic component on the surface of the second insulating layer and conductively connecting terminal electrodes of the electronic component to the lands").

279. A POSITA would have found it obvious, based on Hayashi's teachings regarding the well-known technique, to form similar lands over the top ends of via hole conductors 2a, and would have predictably done so with a

reasonable expectation of success, especially because Hayashi expressly describes the use of such conducting structures and because they would have been readily implemented in connection with forming the wiring circuit layer 3, for example, facilitating efficient manufacturing. APPLE-1011, [0024] (“connecting pads”), [0028], FIG. 1.

280. Note that portions of Hayashi’s wiring circuit layer 3 already exist at the bottom of the via-hole conductors 2a as well as both ends of via-hole conductors 2b, and are not being added. APPLE-1011, [0028], FIG. 1. To be clear, Hayashi already describes “connecting pads” used to provide connection between the electrodes of the electrical element and the via-hole conductors 2a. *Id.*, [0024].

281. Further, Hayashi describes the lands on via hole conductors 2b (e.g., part of wiring circuit layer 3) are formed by copper “plating.” APPLE-1011, [0024] (“depositing a resist on a surface of the insulating sheet 1 surface and then performing plating”), [0025] (“copper” used for wiring circuit layer 3).

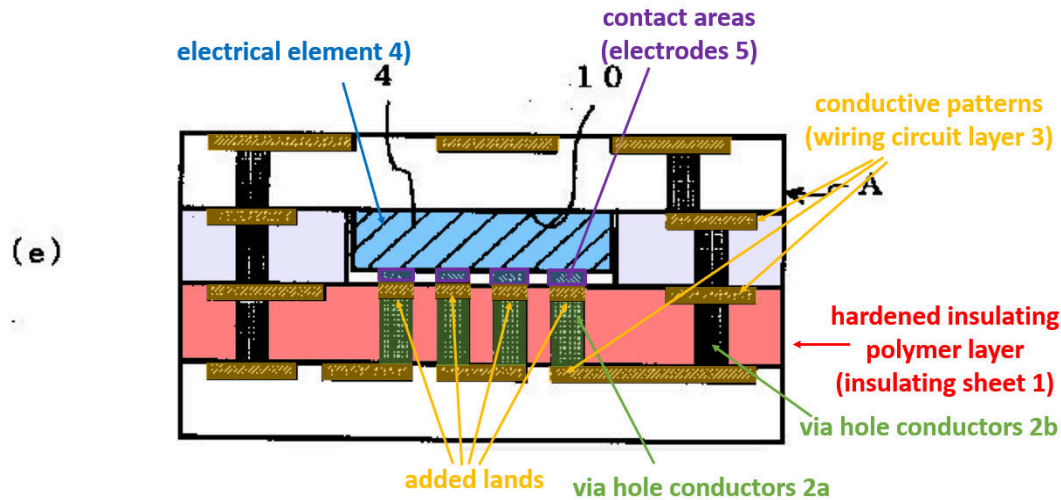
282. It would have been obvious to a POSITA to implement Hayashi’s plating suggestion according to well-known techniques, and, indeed, a POSITA would have been motivated to implement Hayashi’s express “plating” teaching using conventional techniques such as electrochemical plating or both electrochemical and electroless chemical plating. APPLE-1012, [0021] (corroborating prior art describing the use of both “[e]lectroless and electrolytic

copper plating” in forming wiring layers of a wiring substrate); APPLE-1004, [0033]-[0036] (corroborating prior art describing forming conductor circuit layers on a multilayer wiring substrate by a first layer of “electroless plated film” and a second layer of “electrolytic plated film”); APPLE-1005, [0030]-[0032] (corroborating prior art describing forming metal layers on an insulating substrate by “e-less plating, or the like” and metal-lining surfaces of substrate openings and vias “by e-less plating in combination with electrolytic plating, well known to those skilled in the art”). Again, a POSITA would have recognized that electrolytic plating is an electrochemical plating technique, and e-less or electroless plating is a chemical plating technique. In electrolytic plating, an electric current drives a chemical reaction to deposit a layer of metal onto a conductive surface. This process involves immersing the object to be plated (the cathode) and another conductor (the anode) in an electrolyte solution containing metal ions. Unlike electrolytic plating, electroless plating does not require an external electric current to deposit metal onto a surface. Instead, it relies on a chemical reaction that occurs between the plating solution and the object to be plated.

283. The annotated composite figure below illustrates the configuration of the resulting device, with additional lands (connecting pads) located at the top of the via-hole conductors 2a. APPLE-1011, [0024] (“connecting pads”), [0028], FIG. 1. These lands are formed using the same plating method by which the

existing wiring circuit layers 3 (including the existing portions below and in contact with via-hole conductors 2a as well as the portions in contact with both ends of via-hole conductors 2b) are formed, through electrochemical plating or a combination of electrochemical and electroless chemical plating (the recited electrochemically deposited copper), well known to those skilled in the art. In this modified device, the additional lands formed using electrochemical plating (the recited second layer of electrochemically deposited copper), or both electrochemical plating (the recited second layer of electrochemically deposited copper) and electroless plating (alternative mapping for the recited on the first layer of chemically deposited copper), are also in the contact openings and on the conductive paste containing chemically deposited copper (the recited on the first layer of chemically deposited copper). To be clear, the added copper lands together with copper-plated particles inside the via hole conductors 2a penetrate through insulating sheet 1 (the recited hardened insulating polymer layer), thus further providing the recited copper in the contact openings of element [12d], with the contact openings defined by the via hole conductors 2a and the lands over

them. *Supra*, §XII.A, analysis of element [12d].



Modified Based on APPLE-1011, FIG. 1(e) (Annotated)

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

284. Hayashi renders obvious claim [25]. Hayashi describes a metal foil (the recited metal plate) used in the formation of the patterned wiring circuit layers above and below the electrical element (the recited microcircuit). For example, Hayashi discloses the use of a metal foil for forming the patterned wiring circuit layers 3 on both sides of electrical element 4, such as a “copper foil with a thickness of 12 μm .” APPLE-1011, [0003], [0024], [0036], FIG. 1; *supra*, §XII.A, analysis of claim [23]. A POSITA would have found obvious that this “metal foil” provides a “metal plate.” Indeed, I note that the ’909 patent itself uses the terms “metal foil” and “metal plate” interchangeably, and describes forming conductive

pattern layers from a copper foil with a thickness of “e.g., c. 5 μm .” APPLE-1001, 9:11-29 (“a metal plate can be designed above the microcircuit, which is made in connection with the making of the circuit board’s conductive pattern. Similarly, a metal foil that is as complete as possible is made below the microcircuit.”); 4:40-59 (describing “a layer of copper (e.g., c. 5 μm)” which is “an RCC (Resin Coated Copper) foil” above the embedded microcircuit), 5:47-56, 8:44-9:41, FIGS. 1J, 4D.

285. To the extent a “metal foil” and “metal plate” differ in thickness, which the ’909 patent does not describe, the ’909 patent describes an exemplary thickness of “e.g., c. 5 μm ,” which is smaller than the Hayashi’s exemplary thickness of “12 μm ” for the copper foil. APPLE-1012 (corroborating prior art, describing metal foils with a thickness of more than “several 10 μm thick” after plating, used for forming wiring layers above and below embedded electronic components), [0017], [0021], [0025]. Accordingly, a POSITA would have found it to be an obvious design choice to select a metal foil or plate of a particular thickness for forming wiring circuit layers 3.

[26] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.

286. Hayashi renders obvious claim [26] for at least the same reasons as I previously discussed in the analyses of claims [23] and [25]. *Supra*, §XII.A.

[27pre]-[27d] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising: an insulating material layer including a baseboard and a hardened insulating polymer layer; conductive patterns on both sides of the insulating material layer; at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and

287. Hayashi renders obvious elements [27pre]-[27d] for at least the same reasons as I previously discussed in the analyses of elements [17pre]-[17d]. *Supra*, §XII.A.

[27e] at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.

288. Hayashi renders obvious element [27e] for at least the same reasons as I previously discussed in the analyses of claims [25] and [26]. *Supra*, §XII.A.

XIII. GROUND 2B: CLAIMS 1-33 ARE OBVIOUS IN VIEW OF THE HAYASHI-EIJI COMBINATION

289. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have plainly understood that the teachings of Hayashi and Eiji render claims 1-33 obvious.

A. The Predictable Combination of Hayashi and Eiji

290. Based on my knowledge and experience in the field and my review of Hayashi and Eiji, a POSITA would have been motivated to combine Hayashi and Eiji to use a shield layer on the sidewalls of the opening with the electrical element embedded therein, in accordance with Eiji, to make electronic components built into an insulating substrate “less susceptible to external electromagnetic waves, which can reduce the effects of noise generated by the circuits constituting these electronic components, and which can stabilize the electrical characteristics inside the wiring substrate[.]” APPLE-1011, [0028] (“an opening 9 for housing the electrical element 4 is formed in insulating sheet 6”), [0039] (“an opening slightly larger than the size of the electrical element”); APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

291. In the combined module of Hayashi in view of Eiji, the sidewalls of Hayashi’s opening 9 include “a shielding layer [] composed of a copper plating film that shields electromagnetic waves [] formed on an inner surface” of the opening 9 before housing electrical element 4 in a hermetically sealed void formed by the insulating sheets 1, 6 and 7, in accordance with Eiji’s teachings. APPLE-1011, [0028], [0039]; APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

292. Moreover, Eiji expressly describes forming metal layers on an insulating substrate through a combination of electroless plating (a chemical deposition of metal) and electrolytic plating (an electrochemical deposition of metal). *Supra*, §XII.A, analysis of claim [24]; APPLE-1012, [0021]-[0022]. This express teaching of Eiji further confirms that a POSITA would have found it obvious to implement both of these well-known plating techniques in forming the lands over the combined system's via hole conductors 2a, as I have described above in the analysis of claim [24] (§XII.A). As explained above, a POSITA would have understood that electroless plating and electrolytic plating were well-known techniques for depositing metal layers by the Critical Date and it would have been obvious to a POSITA to implement them in view of Eiji's teachings.

293. In the below annotated composite figure, I have illustrated the Hayashi-Eiji combination including the added electromagnetic interference (EMI) shield on the sidewalls of opening 9 and lands over the via hole conductors 2a, in accordance with Eiji, the figure also showing the existing wiring circuit layer 3 portions on the bottom ends of via hole conductors 2a and on both ends of via hole conductors 2b that Hayashi already discloses.

294. A POSITA would have been prompted to utilize EMI shielding in the electrical element mounted wiring board, in accordance with Eiji. As I describe in more detail in the following paragraphs, multiple reasons confirm this analysis:

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noise generated from circuits composed of these electronic components to the outside can be reduced”), [0007], [0009].

296. A POSITA would have appreciated that Hayashi already teaches providing an opening 9 in the insulating sheet to house electrical element 4. APPLE-1011, [0028], [0039]. A POSITA would have understood that it was well-known in the field of component built-in devices, such as the electrical element mounted wiring board device described in Hayashi, by the Critical Date, that electronic components built into an insulating substrate can be susceptible to external electromagnetic waves as well as noise generated by the circuits constituting these electronic components, as evidenced by Eiji. *See e.g.*, APPLE-1012, Abstract; *see also* APPLE-1014 (corroborating prior art), 1:42-45 (“As is known, EMI is disruptive to the proper operation of circuit components located near the source of the EMI. Accordingly, there is an identifiable need to reduce EMI.”), 1:10-41 (explaining that high frequency applications such as wireless applications and specialized computing devices are especially susceptible to EMI); APPLE-1016, [0022] (corroborating prior art describing “shielding effect” against EMI); APPLE-1015, 4:7-9, 5:24-36, 12:39-50 (corroborating prior art describing the use of a “shield layer” or “shield section” so that “noise does not penetrate to the electrical element contained inside the housing section of the multilayer substrate”).

297. A POSITA would have predictably looked towards other teachings such as Eiji for solutions. *See also* APPLE-1014, 4:44-49 (corroborating prior art disclosing “EMI shield metallization” “extend[ing] along the inside wall of cavity 17”). Eiji provides a known technique that would have been recognized to further “stabilize the electrical characteristics” of the system. APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

298. Second, combining Hayashi and Eiji would have been a common application of known techniques, such as forming an EMI shield layer, made of copper-plated film, on the inner surface of sidewalls of an opening that is provided in an insulating board for incorporating an electronic component, to a known electronic module system of Hayashi’s wiring board having an opening 9 in the insulating sheet to stow and mount electrical element 4. Based on my knowledge and experience in the field and my review of Hayashi and Eiji, a POSITA would have had a reasonable expectation of success modifying Hayashi with Eiji, because of the similarities between the systems. For example, both Hayashi and Eiji describe similar electronic modules involving embedding electronic components inside holes or openings of an insulation board. *E.g.*, APPLE-1011, Title, [0001]-[0003]; APPLE-1012, Abstract.

299. Based on my analysis, a POSITA would have recognized that applying Eiji's suggestions to Hayashi's electrical element mounted wiring board would not have significantly altered or hindered the functions performed by Hayashi's wiring board. Based on my knowledge and experience in the field, a POSITA would have found making the proposed modifications to be straightforward, since the modifications would have been implemented largely by adding a metal layer on the sidewalls of the cavity. Eiji already demonstrates this configuration to be successful. And the use of shield layers against EMI problems was known. *See e.g.*, APPLE-1014 (corroborating evidence to show the use of a "EMI metallization shield" along the inside walls of a cavity for accommodating electronic components to address EMI problems). Moreover, Hayashi and Eiji describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above.

B. Analysis of Hayashi and Eiji with Respect to Claims 1-33

300. As shown in this section, the Hayashi-Eiji combination, when predictably combined for at least the reasons described above, provides claims 1-33.

[1pre]-[1c] A circuit board, comprising: an insulating material layer including a baseboard and a hardened insulating polymer layer; conductive patterns on both sides of the insulating material layer; at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;

[1e] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

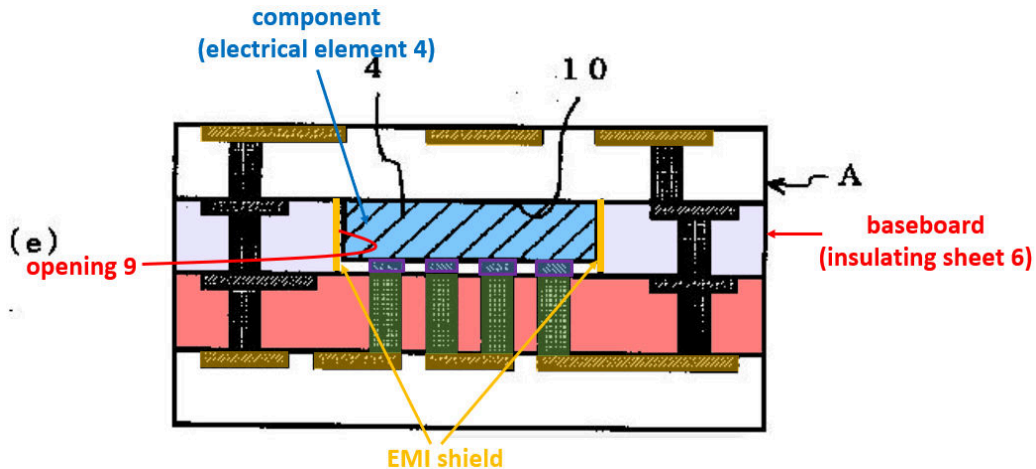
301. Hayashi-Eiji renders obvious elements [1pre]-[1c] and [1e] for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d]. *Supra* §XII.A. The mappings discussed for features of claim 12 apply to the same features recited in these elements of claim 1. I note that Hayashi-Eiji renders obvious independent claim 1 and its dependents without modification according to the “second manner” to utilize circuit board substructures on top of each other that is described with reference to my analysis of claims 12-27, because independent claim 1 and its dependents do not recite the multi-layered circuit board structure.

302. Additionally, for the element [1e], as I previously discussed in the analysis of claim [24] (XII.A, Hayashi ground) and the Hayashi-Eiji combination (XIII.A), the combination renders obvious element [1e], based on Eiji’s express disclosure of both electrochemically and chemically deposited copper in forming conductive wiring layers, which confirms that a POSITA would have found it

obvious to implement both of these well-known plating techniques in forming the lands over the combined system's via hole conductors 2a. APPLE-1012, [0021] ("Electroless and electrolytic copper plating" in forming wiring layers of a wiring substrate); *see also* [0017] (another express disclosure of using a combination of "electroless copper plating and electrolytic copper plating").

[1d] conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

303. Hayashi-Eiji provides element [1d]. The Hayashi-Eiji combination provides a conductive material (e.g., EMI shielding layer) on the sidewalls of the hole in the baseboard (e.g., the sidewalls of opening 9 in the insulating sheet 6). As I described above in §XIII.A (Hayashi-Eiji combination), a POSITA would have been motivated to enhance Hayashi, by adding a metal "shielding layer" on the four sidewalls of opening 9 in insulating sheet 6, in accordance with Eiji, to provide protection around electrical element 4 against "external electromagnetic wave" and "noise generated by the circuits constituting these electronic components," and "stabilize the electrical characteristics" of the system. *Supra* §XIII.A. The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1011, FIG. 1(e) (Annotated)

[2] The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

304. The Hayashi-Eiji combination renders claim [2] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre], [12a] (*see* discussion of how Hayashi’s insulating sheets, including insulating sheet 1 (the recited hardened insulating polymer layer), contain “epoxy resin”) and claim [21]. *Supra*, §XII.A.

[3]³ The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.

305. The Hayashi-Eiji combination renders claim [3] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre] and

³ As mentioned above, I find no support for the recited “the hardened

[12a]. *Supra*, §XII.A. In particular, as I described above, Hayashi's insulating sheets, including insulating sheet 1 (the recited hardened insulating polymer layer), contain "epoxy resin" and a "woven fabric, non-woven fabric composed of glass." APPLE-1011, FIG. 1(a), [0012], [0015], [0016], [0017], [0029].

[4] The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

306. The Hayashi-Eiji combination renders claim [4] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre] and [12a]. *Supra*, §XII.A. In particular, as I explained above, Hayashi's insulating sheets contain "epoxy resin" and a "woven fabric, non-woven fabric composed of glass," and Hayashi's insulating sheet 6, or alternatively 6 and 7 combined, corresponds to the recited baseboard. APPLE-1011, FIG. 1(a), [0012], [0015], [0016], [0017], [0029].

[5] The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.

307. The Hayashi-Eiji combination renders claim [5] obvious for at least the same reasons as I previously discussed in the analysis of claim [23]. *Supra*, §XII.A.

insulating polymer layer contains epoxy and glass fibres" limitation in the '909 patent's specification.

[6] The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.

308. Hayashi-Eiji renders obvious claim [6]. As I previously discussed in the analysis of element [12c] (§XII.A, Ground 2A), Hayashi discloses that “[t]he opening in the insulating sheet contracted due to the flow of resin [such as epoxy resin] caused by heating, and the insulating layer [composed of insulating sheets 1, 6, 7] and the chip were bonded closely together, leaving almost no void between the chip and the insulating layer ” APPLE-1011, [0040]. A POSITA would have understood and found obvious that the “flow of resin,” such as from insulating sheets 1 and 7, would fill in the gap in opening 9, including not only the vertical gap between the electrical element 4 and insulating sheet 1 but also lateral gaps around electrical element 4 from the sidewalls covered by the EMI shield layer of the Hayashi-Eiji device. APPLE-1011, [0032] (“it is preferable to make the thermosetting resin flow before curing to minimize a void with an insulating phase at the periphery of the electrical element 4 to improve reliability”), [0040], [0039] (“an opening slightly larger than the size of the electrical element was formed”), FIGS. 1(d)-(e). The insulating resin flowed into the gap in opening 9 provides the recited filler material in the hole. Consistent with this, Eiji also provides express teaching of a “resin 16, which is primarily epoxy resin,” to secure each component “at a predetermined location in the through-hole.” APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1, 3.

[7] The circuit board of claim 6, wherein the filler material contains epoxy.

309. The Hayashi-Eiji combination renders Claim [7] obvious for at least the same reasons as I previously discussed in the analysis of claim [6]. *Supra*, §XIII.B (describing that both Hayashi’s insulating sheets material flown into the gaps in the hole and Eiji’s resin 16 are options for the filler material, both contain epoxy).

[8pre]-[8b] The circuit board of claim 1, wherein said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

310. The Hayashi-Eiji combination renders claim [8] obvious for at least the same reasons as I previously discussed in the analyses of elements [12pre]-[12d], [1pre]-[1e], and claim [14] in Grounds 2A and 2B. *Supra*, §§XII.A and XIII.B. For example, Hayashi describes that when “a plurality of electrical elements” are provided “in the same ... layer[,]” these electrical elements are connected to each other through via hole conductors 2a (the recited conductors in the contact opening) for connecting to both the electrodes 5 on the first surface of each electrical element and the wiring circuit layers 3 (the recited at least one of the conductive patterns). APPLE-1011, [0032].

[9] The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

311. The Hayashi-Eiji combination renders claim [9] obvious for at least the same reasons as I previously discussed in the analysis of claim [24]. *Supra*, §XII.A. Additionally, as I also discussed in the Hayashi-Eiji combination, Eiji provides express teaching of “[e]lectroless and electrolytic copper plating” for forming wiring layers 26 and 27 on the upper and lower sides of embedded electronic components embedded in a cavity of an insulating substrate. APPLE-1012, [0021]-[0022]. A POSITA would have been prompted to implement the same plating techniques for plating Hayashi’s wiring circuit layer 3 and additional lands over the via hole conductors 2a. *Supra*, §XIII.A (Hayashi-Eiji combination).

[10] The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

312. The Hayashi-Eiji combination renders claim [10] obvious for at least the same reasons as I previously discussed in the analysis of claim 13 (*see* discussion of how Hayashi’s “via-hole conductors 2b” correspond to the recited feed-through). *Supra*, §XII.A.

[11pre]-[11b] The circuit board of claim 1, wherein said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.

313. The Hayashi-Eiji combination renders [11pre]-[11b] obvious for at least the same reasons as I previously discussed in the analysis of elements [8pre]-[8b]. *Supra*, §XIII.B.

[12]-[27]

314. The Hayashi-Eiji combination renders obvious these claims for at least the same reasons as I previously discussed for these claims under the Hayashi ground alone. *Supra*, §§XII.A, analyses of claims [12]-[27].

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

315. The Hayashi-Eiji combination provides claim [24]. For example, as discussed above in the Hayashi-Eiji combination, the combined system has lands formed over the via hole conductors 2a through a layer of electroless plating (the recited a first layer of chemically deposited copper) and a layer of electrolytic plating (the recited a second layer of electrochemically deposited copper) on the first layer of chemically deposited copper. *Supra*, §XIII.A (Hayashi-Eiji combination).

[28] The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

316. The Hayashi-Eiji combination provides claim [28]. As I previously discussed in the analysis of element [1d] (§XIII.B, Ground 2B), the enhanced Hayashi-Eiji device has a conductive metal film on the four sidewalls of opening 9 to provide EMI protection around electrical element 4, in accordance with Eiji's teaching of "shielding layer 10." APPLE-1012, [0012]. Eiji's shielding layer 10 is composed of a "copper plating film", which provides a metal foil, as claimed. I note that Eiji's construction for shielding layer 10 is like the '909 patent's description of the formation of a metal foil on the sidewalls of the hole, also by copper plating. APPLE-1012, Abstract, [0012], [0017]; *see also*, [0021], [0025], [0030], [0033], [0035]-[0036]; APPLE-1001, 3:61-4:9; 8:39-46.

[29] The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.

317. The Hayashi-Eiji combination renders claim [29] obvious. As I have discussed above in the analyses of element [1d] and claim [28] in Ground 2B, the enhanced Hayashi-Eiji device has metal foil covering all four sidewalls of opening 9 to provide EMI protection around electrical element 4. *Supra* §XIII.B. As electrical element 4 is surrounded by the unbroken four sidewalls of opening 9 in a lateral direction of the circuit board, a POSITA would have understood that the

metal foil covering all four sidewalls of opening 9 is an unbroken metal foil and surrounds electrical element 4 in a lateral direction of the circuit board.

[30]-[33]

318. The Hayashi-Eiji combination renders claims [30]-[33] obvious for at least the same reasons as I previously discussed in the analyses of claims [25] and [26] in Ground 2A and elements [1pre]-[1e] in Ground 2B. *Supra*, §§XII.A, XIII.B.

XIV. GROUND 2C: THE HAYASHI-WATANABE COMBINATION RENDERS CLAIMS 12-27 OBVIOUS

319. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have plainly understood that the teachings of Hayashi and Watanabe render claims 12-27 obvious.

A. The Predictable Combination of Hayashi and Watanabe

320. Based on my knowledge and experience in the field and my review of Hayashi and Watanabe, a POSITA would have been motivated to combine the teachings of Hayashi and Watanabe to implement Hayashi's conductive particles of the conductive paste in via hole conductors 2a with copper-plated polymer cores through chemical deposition, in accordance with Watanabe's suggestions.

APPLE-1011, [0012], [0018]-[0020], [0035]; APPLE-1017, 12, *see also* Title, Abstract, 1, 5, 14.

321. Hayashi's via hole conductors 2a for electrically connecting electrical element 4 (through connection with its electrodes 5) and the wiring board (through connection with wiring circuit layer 3 providing terminals on the substrate) are made of a "conductive paste contain[ing] a low melting point metal having low melting point T_2 , which is equal to or lower than thermosetting temperature T_1 of the thermosetting resin, and a high melting point metal having a melting point that is higher than the thermosetting temperature of the thermosetting resin." *Supra*, §XII.A, analysis of element [12d]. Additionally, Hayashi further discloses that the low melting point metal preferably contains copper among other metal options, with a specific example of copper powder plated with silver. APPLE-1011, [0012], [0018]-[0020], [0035] (This conductive paste consisted of a metal component composed of 50 vol% copper powder with an average particle size of 5 μm plated with silver and 50 vol% Sn-Pb eutectic solder powder with an average particle size of 3 μm (melting point $T_2 = 183^\circ\text{C}$) serving as the low melting point metal").

322. Watanabe describes the use of a "conductive adhesive" having conductive particles to make electrical connections between terminals (such as electrodes) on a semiconductor chip (e.g., an integrated circuit (IC) chip) and on an insulating substrate where the chip is mounted. APPLE-1017, Abstract, 1, 5, 14. Watanabe also describes that the conductive adhesive can include conductive

particles, and that “the conductive particles can be, for example, particles of metals such as Au, Ag, Cu or solder, and a conductive layer of Ni, Cu, Au, or solder is preferably provided on a spherical polymer core material such as polystyrene. A surface layer of Su, Au, solder, etc. can also be formed on the surface of conductive particles.” *Id.*, 12. I understand Watanabe’s reference to “Su” in this sentence to be a typo, and understand “Su” as “Cu” (referring to copper) in the context of the sentence, and there is no chemical element with the symbol “Su” in the periodic table.

323. Based on the suggestion of Watanabe, in the combined Hayashi-Watanabe system, the conductive particles of the conductive paste in Hayashi’s via hole conductors 2a are formed with a conductive layer of copper grown on a polymer core through a chemical deposition. APPLE-1017, 12, *see also* Title, Abstract, 1, 5, 14. *See also supra*, §XII.A, analysis of claim [24].

324. Combining Hayashi and Watanabe’s teachings in this way would have been obvious to a POSITA in view of Hayashi’s teachings regarding the use of metal-plated conductive particles and Watanabe’s description of implementation techniques for such particles. For example, Hayashi describes a “conductive paste” for via hole conductors 2a for electrically connecting electrical element 4 (through connection with its electrodes 5) and the wiring board (through connection with wiring circuit layer 3 providing terminals on the substrate), and

Hayashi describes various compositions, including copper. Although copper as a lower cost option (e.g., versus silver) is suggested, Hayashi does not provide exhaustive implementation details of copper-plated conductive particles. Based on my knowledge and experience in the field, and my review of Hayashi and Watanabe, a POSITA would have predictably looked to well-known techniques for forming conductive particles of a conductive paste for forming electrical connections between electrodes or electrode terminals of electrical elements and a mounting substrate. A POSITA would have found that Watanabe provides an example of suitable copper-plated polymer cores. APPLE-1017, Title, Abstract, 1, 5, 12, 14.

325. Based on my knowledge and experience in the field, a POSITA would have been further motivated to implement copper-plated polymer cores, in accordance with Watanabe's suggestions, for via hole conductors 2a to promote efficient manufacturing and reduced manufacturing and material costs (e.g., associated with a high silver content), while effectuating reliable electrical connection through the via hole conductors.

326. Additionally, combining Hayashi and Watanabe would have been a common application of known techniques such as forming conductive particles of a conductive paste through chemical deposition, suggested by Watanabe, to a known device of Hayashi's module that utilizes copper conductive paste. Based on

my knowledge and experience in the field and my review of Hayashi and Watanabe, a POSITA would have had a reasonable expectation of success modifying Hayashi with Watanabe, because of the similarities between the systems. For example, both Hayashi and Watanabe describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above, for example, they describe similar devices involving similar types of insulating substrate having conductor holes containing conductive particles therein for forming electrical connections between electrodes of a semiconductor chip and wiring layers on the substrate. *See e.g.*, APPLE-1011, Cl. 1, [0001], [0009], [0015], [0016]-[0017]; APPLE-1017, Abstract, 1, 5, 14.

327. Based on my analysis, a POSITA would have recognized that applying Watanabe's suggestions to Hayashi's electronic module would not have significantly altered or hindered the functions performed by Hayashi's electronic module. Moreover, based on my knowledge and experience in the field, a POSITA would have found making the proposed modifications to be straightforward, since the modifications would have been implemented largely by forming conductive particles through chemical copper plating on polymer cores. Watanabe already demonstrates this configuration to be successful.

B. Analysis of Hayashi and Watanabe with Respect to Claims

12-27

[12pre]-[12c], [13]-[16], [17pre]-[17c], [18], [19pre]-[19c], [20pre]-[20c], [21]-[23], [25]-[26], [27pre]-[27c], [27e]

328. The Hayashi-Watanabe combination renders obvious elements [12pre]-[12c], [17pre]-[17c], [19pre]-[19c], [20pre]-[20c], [27pre]-[27c], and [27e], and claims [13]-[16], [18], [21]-[23], and [25]-[26] for at least the same reasons as I previously discussed in the analyses of these elements and claims above under the Hayashi ground alone. *Supra*, §XII.A.

[12d]/[17d]/[19d]/[20d]/[27d]

329. Elements [12d], [17d], [19d], [20d], and [27d] recite the same or similar limitations. For example, element [12d] recites “contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.”

330. As I previously discussed in the analyses of element [12d] and claim [24] (§XII.A, Ground 2A), for example, Hayashi alone renders these elements obvious, even if the recited process of the “product-by-process element” is understood to be limiting to the claim for purposes of invalidity.

331. Even if Hayashi alone did not provide that the copper contains at least one of electrochemically deposited copper and chemically deposited copper –

which, as I explained above, it does – the combined system renders this limitation obvious. In particular, and as I described above in the Hayashi-Watanabe combination, copper-plated polymer cores are used as conductive particles of the conductive paste in the via hole conductors 2a described by Hayashi, in accordance with Watanabe. *Supra*, §§XIV.A (Hayashi-Watanabi combination), VII.F (Watanabe overview). As described above, in the combined system, the conductive layer of copper is grown on the polymer core, in accordance with Watanabe's suggestions, thereby disclosing the recited chemically deposited copper, in accordance with Watanabe's suggestions, and to predictably effectuate the copper-plated polymer cores. APPLE-1017, 12, 14; *supra*, §XII.A, analysis of element [12d]..

332. Additionally, the Hayashi-Watanabe combination renders obvious elements [12d], [17d], [19d], [20d], and [27d] in a second manner. As I previously discussed in the analysis of claim [24] (§XII.A), , a POSITA would have been motivated to form copper lands by electrochemical plating (the recited a second layer of electrochemically deposited copper), over the via hole conductors 2a containing copper-plated polymer cores (the recited on the first layer of chemically deposited copper), at the same time of forming the wiring circuit layer 3 on insulating sheet 1, in order to enhance alignment and robust connection with electrodes 5. For example, the added copper lands, taken together with copper-

plated particles inside the via hole conductors 2a, penetrate through insulating sheet 1, the recited hardened insulating polymer layer. The copper lands and copper-plated particles inside the via hole conductors 2a together accordingly provide an alternative mapping to the recited copper in the contact openings of element [12d], with the contact openings defined by the via hole conductors 2a and the lands over them. Because the lands are connected to the conductive particles (made of the copper-plated polymer cores) in the conductive paste in via hole conductors 2a to form electrical contacts, the interface between these two copper layers provides the recited second layer of electrochemically deposited copper on the first layer of chemically deposited copper. In the case where the lands themselves are formed through a combination of electroless and electrochemical plating, the lands alone then provide the recited first and second layers of copper. In this case, the copper of the copper-plated (through electroless chemical plating) conductive particles in the via hole conductors 2a provides yet another layer (a third layer of copper) of chemically deposited copper in contact with the plated lands.

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

333. The Hayashi-Watanabe combination renders obvious claim [24], even if the recited process of the “product-by-process element” is understood to be

limiting to the claim for purposes of determining invalidity, for at least the same reasons as I previously discussed in the analyses of element [12d] in Ground 2C and claim [24] in Ground 2B. *Supra*, §§XIV.B, XIII.B.

XV. GROUND 2D: THE HAYASHI-EIJI-WATANABE COMBINATION RENDERS CLAIMS 1-33 OBVIOUS

334. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have plainly understood that the teachings of Hayashi, Eiji and Watanabe render obvious claims 1-33.

A. The Predictable Combination of Hayashi-Eiji-Watanabe

335. Based on my knowledge and experience in this field and my review of Hayashi, Eiji, and Watanabe, a POSITA would have been motivated to implement the conductive particles of the conductive paste of Hayashi-Eiji's via hole conductors 2a with copper-plated polymer cores, in accordance with Watanabe's teaching, to reduce costs, as I have discussed in detail above. *Supra*, §XIII.A (Hayashi-Eiji Combination); §XIV.A (Hayashi-Watanabe Combination). The resulting Hayashi-Eiji-Watanabe includes each element of claim 1-33, for the reasons I've described in the combinations above, and the additional reasons noted below.

**B. Analysis of Hayashi, Eiji and Watanabe with Respect to
Claims 1-33**

[1pre]-[1d], [2]-[8], [10]-[33]

336. The Hayashi-Eiji-Watanabe combination provides elements [1pre]-[1d] and claims [2]-[8], [10]-[33] for at least the same reasons as I previously discussed in the analyses of these claims in Grounds 2A and 2B. *Supra*, §§XII.A, XIII.B, analyses of elements [1pre]-[1d] and claims [2]-[8], [10]-[33].

[1e] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

337. The Hayashi-Eiji-Watanabe combination renders obvious element [1e] for at least the same reasons as I previously discussed in the analyses of element [1e] in Ground 2B and element [12d] in Ground 2C. *Supra*, §§XIII.B, XIV.B.

[9] The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

338. The Hayashi-Eiji-Watanabe combination renders obvious claim [9] for at least the same reasons as I previously discussed in the analyses of claim [9] in Ground 2B and claim [24] in Ground 2C. *Supra*, §§XIII.B, XIV.B.

XVI. CONCLUSION

The findings and opinions set forth in this declaration are based on my work and examinations to date.

I may continue my examinations. I may also receive additional documentation and other factual evidence over the course of this IPR that will allow me to supplement and/or refine my opinions. I reserve the right to add to, alter, or delete my opinions and my declaration upon discovery of any additional information. I reserve the right to make such changes as may be deemed necessary.

In signing this declaration, I recognize that the declaration will be filed as evidence in an IPR before the PTAB. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

APPENDIX A

Dean P. Neikirk

Emeritus Professor, Emeritus Cullen Trust for Higher Education Professorship in Engineering
Department of Electrical and Computer Engineering
Cockrell School of Engineering
The University of Texas at Austin
Austin, TX 78712

Education:

Oklahoma State University (Physics and Mathematics; with Honors)	B.S.	1979
California Institute of Technology (Applied Physics)	M.S.	1981
California Institute of Technology (Applied Physics)	Ph.D.	1984

Professional Experience:

Assistant Professor, University of Texas at Austin, Jan. 1984 - Aug. 1988
Associate Professor, University of Texas at Austin, Sept. 1988- Aug. 1992
Full Professor, University of Texas at Austin, Sept. 1992-Jan. 2021
Associate Dean of Graduate Studies, Aug. 2014 – Jan. 2021
Emeritus Professor, Feb. 2021 - present

Honors and Awards:

- 1984 Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the areas of detectors and imaging arrays."
- Listed in the Second Edition of Who's Who in Frontiers of Science and Technology, 5th Edition of Who's Who in Technology Today, 1994 American Men & Women of Science; 1985 Outstanding Young Man of America, 1989 Outstanding Young Man of America; 7th Edition of Who's Who in Technology.
- 1984-85 Engineering Foundation Faculty Award, University of Texas at Austin Engineering Foundation Advisory Council.
- 1985-90 General Motors Foundation Centennial Teaching Fellowship, University of Texas at Austin.
- 1985-86 IBM Corporation Faculty Development Award
- 1986 National Science Foundation Presidential Young Investigator.

- 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, University of Texas at Austin.
- 1990-1992 Temple Foundation Endowed Faculty Fellowship (No. 1), University of Texas at Austin.
- 1992-present Cullen Trust for Higher Education Professorship in Engineering (No. 7), University of Texas.
- 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, University of Texas at Austin.
- 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, University of Texas at Austin.
- 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching
 - each year since 1956, Lockheed Martin and its predecessor, has sponsored an award for excellence in engineering teaching to reward one College of Engineering faculty member for exceptional teaching. This prestigious award is given to a faculty member dedicating time and energy in abundance to teaching undergraduate and graduate students. As a result, his or her work leaves a mark of excellence on the entire College of Engineering. Nominations for this award are made by The University of Texas at Austin engineering students and faculty. Final selection is made by a committee composed the five most recent faculty recipients of the award and the student presidents of the Student Engineering Council (SEC) and the Graduate Engineering Council (GEC).
- 2015 Civitatis Award: The University of Texas at Austin Civitatis Award was established in 1997 to recognize outstanding faculty citizenship. The Civitatis Award is conferred upon a member of the faculty in recognition of dedicated and meritorious service to the University above and beyond the regular expectations of teaching, research, and writing. The award is made by the President upon the recommendation of the Faculty Council Executive Committee. Prof. Neikirk was nominated for the award for his “extensive, effective and distinguished service record to his department, college and [the] University of Texas.”

Vita for Dean P. Neikirk:

Dean P. Neikirk was born in Oklahoma City, Oklahoma, on October 31, 1957. He received the B.S. degree (1979) in physics from Oklahoma State University, and the M.S. (1981) and Ph.D. (1984) degrees in applied physics from the California Institute of Technology. He joined the faculty of The University of Texas at Austin in 1984, and is currently a Professor in the Department of Electrical and Computer Engineering, holding the Cullen Trust for Higher Education Professorship in Engineering (No. 7). Dr. Neikirk developed the first monolithic, high resolution focal plane detector array for use at wavelengths between 0.1 mm and 1 mm, and in 1984 received the Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter

wave integrated circuits especially in the area of detectors and imaging arrays." He has also been named a 1986 National Science Foundation Presidential Young Investigator.

Dr. Neikirk's research interests concentrate on the fabrication and modeling of electromagnetic and micromachined sensors and actuators. His work also included projects involving integrated circuit processing and the high frequency properties of transmission lines. His work concentrated on the use of advanced fabrication techniques, including silicon micromachining, for new device and sensor development. Dr. Neikirk developed the teaching laboratory for semiconductor device fabrication at The University of Texas at Austin, and was an active member of The University of Texas at Austin Microelectronics Research Center. Recently Dr. Neikirk's research project related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between the University of Texas and LabNow, Inc. Dr. Neikirk has also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, the Secretary of the General Faculty at UT-Austin, and as an Associate Dean of the University of Texas at Austin Graduate School.

Professional Societies:

Senior Member, Institute of Electrical and Electronics Engineers

- Associate Editor for Solid State and VLSI Electronics, **IEEE Transactions on Education** (March 1991- Oct. 1994)

Commercialization of Technology:

Two companies have been founded based on technology developed by Dr. Neikirk's research group. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups.

From a University of Texas news release:

Firm commercializing University of Texas technology rounds up \$14 million venture capital investment (October 1, 2004)

AUSTIN, Texas—LabNow Inc. has received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors.

The money will be used to develop the company's technology and to launch its initial product, CD4Now™, a point-of-care diagnostic tool for HIV/AIDS patients.

The device, which is based on technology developed at The University of Texas at Austin, quickly and accurately analyzes complex fluids such as blood.

Patents

1. US Patent 5,080,870: "Sublimating and Cracking Apparatus," Jan. 14, 1992; Inventors: B. G. Streetman, T. J. Mattord, D. P. Neikirk
2. US Patent 5,408,107: "Semiconductor Device Having Multiple Current-Voltage Curves and Zero-Bias Memory," April 18, 1995;
Inventors: Dean P. Neikirk and Kiran Kumar Gullapalli
3. US Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," July 8, 2003;
Inventors: McDevitt; John T.; Anslyn; Eric V.; Shear; Jason B.; Neikirk; Dean P.
Assignee: Board of Regents, The University of Texas System (Austin, TX)
4. US Patent 6,602,702: "Detection system based on an analyte reactive particle," August 5, 2003
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)

Assignee: The University of Texas System (Austin, TX)

5. US Patent 6,649,403: "Method of preparing a sensor array," November 18, 2003
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
6. US Patent 6,680,206, "Sensor arrays for the measurement and identification of multiple analytes in solutions," January 20, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
7. US Patent 6,713,298, "Method and apparatus for the delivery of samples to a chemical sensor array, " March 30, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Travis, TX); Shear; Jason B. (Travis, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
8. US Patent 6,908,770, "Fluid based analysis of multiple analytes by a sensor array," June 21, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
9. US Patent 7,022,517, "Method and apparatus for the delivery of samples to a chemical sensor array," April 4, 2006, filed: July 14, 2000
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX); Borich; Damon V. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
10. US Patent 7,316,899, "Portable sensor array system," January 8, 2008, filed: January 31, 2001
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
11. US Patent 7,491,552, "Fluid based analysis of multiple analytes by a sensor array," February 17, 2009, filed: January 20, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
12. United States Patent 7,651,868, "Method and system for the analysis of saliva using a sensor array," January 26, 2010, Filed: December 13, 2004

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: The Board of Regents of The University of Texas System (Austin, TX)

13. United States Patent 8,101,431, "Integration of fluids and reagents into self-contained cartridges containing sensor elements and reagent delivery systems," January 24, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

14. United States Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements," January 31, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

15. United States Patent 8,257,967, "Method and system for the detection of cardiac risk factors," September 4, 2012, Filed: April 28, 2003

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

16. United States Patent 9,291,586, "Passive wireless self-resonant sensor," March 22, 2016, Filing Date: May 5, 2013

Inventors: Neikirk, Dean P. (Austin, TX, US), Pasupathy, Praveenkumar (Austin, TX, US), Zhang, Sheng (Austin, TX, US), Leonhardt, Brad (Austin, TX, US), Ekerdt, John G. (Austin, TX, US), Korgel, Brian A. (Austin, TX, US), Holmberg, Vincent C. (Seattle, WA, US), Shipman, Catherine D. (Reston, TX, US), Bogart, Timothy D. (Oxford, GB), Chockla, Aaron (Chicago, IL, US)

Assignee: Board of Regents, The University of Texas System (Austin, TX, US)

17. United States Patent 9,581,559, "Corrosion detection sensor embedded within a concrete structure with a diffusion layer placed over the sacrificial transducer," February 28, 2017, Filing Date: August 14, 2014

Inventors: Neikirk; Dean P. (Austin, TX), Wood; Sharon L. (Austin, TX), Pasupathy; Praveenkumar (Austin, TX), Yosef; Ali Abu (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

Publications:

A: Refereed archival journal publications

1. D. P. Neikirk and R. C. Powell, "Laser Time-Resolved Spectroscopy of Host-Sensitized Energy Transfer in $\text{Bi}_4\text{Ge}_3\text{O}_{12}:\text{Er}^{3+}$ Crystals," **J. Lumin.**, vol. 20, 1979, pp. 261-270.
2. R. C. Powell, D. P. Neikirk, J. M. Flaherty, and J. G. Gualtieri, "Lifetime Measurements, Infrared and Photoacoustic Spectroscopy of $\text{NdP}_5\text{O}_{14}$," **J. Phys. Chem. Solids**, vol. 41, 1980, pp. 345-350.
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D. Other Major Publications

V. Kesan and D. P. Neikirk, "Quantum Well Devices," **Microwaves and RF**, vol. 25, July 1986, pp. 93-97.

D. P. Neikirk, P. Cheung, M.S. Islam, and T. Itoh, "Optically Controlled Coplanar Waveguide Phase Shifters," **Microwave Journal**, Dec. 1989, pp. 77-88.

D. P. Neikirk, "Quantum Wells and Other Deep Subjects," **Discovery**, Vol. 11, No. 3, 1989, pp. 5-8.

S. M. Wentworth, J. M. Lewis, and D. P. Neikirk, "Antenna-Coupled Thermal Detectors of mm-Wave Radiation," **Microwave Journal**, Jan. 1993, pp. 94-103.

E. Book Chapter

D. B. Rutledge, D. P. Neikirk, and D. Kasilingam "Integrated- Circuit Antennas," in **Infrared and Millimeter Waves**, vol. 11, editor K.J. Button, 1984.

Nicolaos Christodoulides, Priya Dharshan, Jorge Wong, Pierre N. Floriano, Dean Neikirk and John T. McDevitt, "A Microchip-Based Assay for Interleukin-6," In: *Methods in Molecular Biology*, Volume 385: Microchip-Based Assay Systems, Humana Press, ISBN 978-1-58829-588-0 (Print) 978-1-59745-426-1 (Online), Copyright 2008, pages 131-144.

F. Technical Reports

C-K Tzuang, D. P. Neikirk, and T. Itoh, "Finite Element Analysis of Slow-Wave Schottky Contact Printed Lines," Microwave Laboratory Report No. 87-P-2, AFOSR Grant 86-0036, Feb., 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 87-P-3, AFOSR Grant 86-0036, Jan., 1987.

V. P. Kesan and D. P. Neikirk, "Quantum Well Devices," Electrical Engineering Research Laboratory Report No. 87-P-8, Joint Services Electronics Program Research Contract AFOSR F49620-86-C-0045, August 7, 1987.

Stuart M. Wentworth and D. P. Neikirk, "High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," Microwave Laboratory Report No. 87-P-7, August 26, 1987.

Stuart M. Wentworth and D. P. Neikirk, "Characterization of Tape Automated Bonding (TAB) Interconnects at High Frequency," Microwave Laboratory Report No. 87-P-9, October 23, 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 90-P-1, Final Technical Report for AFOSR Grant 86-0036, Feb., 1990.

A. Mortazawi, D. Neikirk, and T. Itoh, "Microwave and millimeter wave oscillators and planar power combining structures for QWITT and Gunn diodes," Microwave Laboratory Report No. 90-P-4, Technical Report for ARO Grant DAAL03-88-K-0005 and JSEP Grant F49620-89-0044, Aug., 1990.

Oral Presentations

A. Professional Society Presentation

D. B. Rutledge and D. P. Neikirk, "Imaging Antenna Arrays," Invited Keynote Speakers, Sixth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 7-12, 1981.

D. P. Neikirk and D. B. Rutledge, "Advances in Microbolometers," Invited Keynote Speakers, Eighth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 12-17, 1983.

D. P. Neikirk, "Optically Controlled Coplanar Waveguide Millimeter Wave Phase Shifter," Tenth International Conference on Infrared and Millimeter Waves, Lake Buena Vista, Fl., Dec. 9-13, 1985.

D. P. Neikirk, "Picosecond Response of an Optically Controlled Millimeterwave Phase Shifter," Second Topical Meeting on Picosecond Electronics and Optoelectronics, Jan., 1987.

D. P. Neikirk, "Influence of Transit Time Effects on the Optimum Design and Maximum Oscillation Frequency of Quantum Well Oscillators," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "Measurements of an Optically Controlled Coplanar Waveguide Phase-Shifter," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "High Frequency Characterization of Tape-Automated Bonding Interconnects," 5th Annual Texas Regional Symposium, International Society of Hybrid Manufacturing, April 11, 1988.

D. P. Neikirk, "Time Dependent Simulation of the Quantum Well Injection Transit Time Diode," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

D. P. Neikirk, "Experimental Performance of a Periodically Illuminated Optically Controlled Coplanar Waveguide Phase Shifter," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

B. Invited Lectures

1. D. P. Neikirk, "Exotic Heterojunction Devices for Microwave Circuits," NSF Workshop on Future Research Opportunities in Electromagnetics, Arlington, TX., January 29-31, 1986.

2. D. P. Neikirk, "Optical Control of a Monolithic Millimeter Phase Shifter," ARO Workshop on Fundamental Issues in Millimeter and Submillimeter Waves, Los Angeles, Ca., Sept. 15-16, 1986.

3. Dean P. Neikirk, "Quantum Well Oscillators for Millimeter Wave Applications," 1987 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Hilton Head Island, S.C., March 2-4, 1987.

4. S.M. Wentworth and D. P. Neikirk, "High Frequency Tape-Automated Bonding (TAB) Interconnect Characterization," IEEE 6th Annual VLSI and GaAs Packaging Workshop, Sept. 14-16, 1987.

5. D. P. Neikirk, "The quantum well injection transit time diode," Engineering Foundation Conference on Advanced Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec. 5-10, 1988.
6. D. P. Neikirk, ""The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," presented to the Microelectronics and Computer Technology Corporation, April 19, 1989.
7. Dean P. Neikirk, "Impedance measurements of quantum well diodes for millimeter wave applications," 1990 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), San Francisco, CA., Feb. 12-14, 1990.
8. Dean P. Neikirk, "Twin-slot multi-layer substrate-supported antennas and detectors for terahertz imaging," First International Symposium on Space Terahertz Technology, University of Michigan, Ann Arbor, Mich., March 5-6, 1990.
9. Dean P. Neikirk, "Microwave and Millimeterwave Oscillators using Quantum Well Diodes," Joint IEEE MTT/ED Dallas Chapter meeting, Sept. 27, 1990.
10. Dean P. Neikirk, "Quantum Transport Simulations of Resonant Tunneling Diodes," 1991 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Ft. Lauderdale, FL., Feb. 18-20, 1991.
11. Dean P. Neikirk, "The Application of Physics in Electrical Engineering (or is it Engineering in Physics?): Electromagnetics in Very High Frequency Semiconductor Devices," Physics Colloquium, Oklahoma State University, March 5, 1992.
12. D. P. Neikirk and B. G. Streetman, "MBE growth of multilayer heterostructures for photonic and high-speed electronic devices," Engineering Foundation Conference on High Speed Optoelectronic Devices and Circuits II, Banff, Alberta, Canada, Aug. 9-13, 1992.
13. L. T. Pillage, D. P. Neikirk, and R. Mercer, "Design automation techniques and algorithms for application specific electronic modules (ASEMs)," ARPA Electronic Packaging & Interconnect Principle Investigator Meeting, Marina del Ray, CA, Feb. 14-18, 1994.
14. D. P. Neikirk, "Micro-sensors - What happens when you make classical devices small?: Integrated Bolometric Radiation Detectors," Texas Instruments, Dallas, Texas, Oct. 20, 1994.
15. Dean P. Neikirk, "Micromachined sensors," Motorola Sensors Steering Committee, Albuquerque, New Mexico, March 28, 1995.
16. D. P. Neikirk, E. Tuncer, and B.-T. Lee, "The Use of Effective Internal Impedance Approximations in Lossy Transmission Line Modeling," *Progress in Electromagnetics*

Research Symposium PIERS 95, The University of Washington, Seattle, Washington, July 28, 1995.

17. D. P. Neikirk, M. S. Islam, and E. Tuncer, "Accurate Quasi-Static Modeling of Transmission Lines on Semiconducting Substrates," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.

18. D. P. Neikirk, "Impact of Finite Metal Conductivity on Inductance Extraction of Interconnects and Packages," Sematech meeting on Electrical Modeling Challenges Faced by Packaging Designers, Austin, Texas, Nov. 19, 1995.

19. D. P. Neikirk, "Micromachined Fabry-Perot Pressure Transducers," Hughes Research Laboratory, Malibu, California, Nov. 21, 1995.

20. D. P. Neikirk, "Classical Devices Made Small; or 'What's the big deal about little machines?'" , Manufacturing 2000, University of Texas at Austin, Feb. 23, 1996.

21. D. P. Neikirk, "Interconnect Inductance Modeling from DC to the Skin Effect Limit," Quad Designs, Camarillo, CA, July 10, 1996.

22. D. P. Neikirk, "Efficient Conductor Boundary Conditions in the dc to Skin Effect Limit," DARPA MAFET Program Review, Fairfax, VA, Oct. 27-31, 1997.

23. Micromachined Array-based Multi-analyte Chemical Sensors: Towards the Fabrication of an "Electronic Tongue" South, Texas Local Section of The Electrochemical Society Meeting, April 17, 1999.

24. D. P. Neikirk, "Resonant Chemical Surveillance Tags," IEEE Electron Device Chapter, Central Texas Section, September 25, 2008.

25. D.P. Neikirk, "Near Borehole Condition Sensing," Nanotechnology Conference and Trade Show - Nanotech 2009, Houston, TX May 3-7, 2009, Nanotech & Cleantech for Oil & Gas Session, (Session chair: Sean Murphy, Advanced Energy Consortium), May 5, 2009.

26. D.P. Neikirk, "Integrated Threshold Nanosensor Systems," Advanced Oil Consortium Microfabricated Sensors Workshop, Houston Research Center, Bureau of Economic Geology, University of Texas at Austin, September 8th-9th, 2010.

27. D. P. Neikirk, "Sensing systems for "harsh" environments," Engineering Challenges for Deepwater Drilling at the "U.S. Offshore Oil Exploration: Managing Risks to Move Forward," James A. Baker III Institute for Public Policy and PFC Energy, Rice University, Houston, TX, February 11, 2011.

C. Other Conference Presentations

Praveen Pasupathy, Mingxiang Zhuzhou, Shasi K. Munukutla, Dean P. Neikirk, and Sharon L. Wood, “Resonant Wireless Sensor Nets for Civil Infrastructure Health Monitoring,” 2009 National Science Foundation Division of Civil, Mechanical and Manufacturing Innovation (CMMI) Engineering Research and Innovation Conference, Honolulu, Hawaii, June 22-25, 2009.

Technical Consulting

Teltech Resource Network (1985-1993)
Ardex, Inc. (1986-88)
University and Polytechnic Grants Committee, Consultancy to examine Equipment Requirements for the Hong Kong University of Science and Technology, July, 1989
E. P. Hamilton Associates, (1987-90)
Burnett Company, Microwave Heating for Secondary Oil Recovery, July, 1990
Microelectronics and Computer Technology Corporation, June, 1990
Microelectronics and Computer Technology Corporation, Oct., 1994 - Sept., 1996
Baker-Hughes

University Committee Assignments

Departmental:

Graduate Student Financial Aid, Sept. 1984- Sept. 1987
Faculty Recruiting, Sept. 1984- Aug. 1985
Microelectronics Jr. Faculty Recruiting, Sept. 1985- Sept. 1987 (chairman)
ECE Safety Committee, Sept. 1985- Aug. 1993 (chairman, 1985-89)
ECE Electronics Shop Coordinating Committee, March 1986- Aug. 1993
Solid State Electronics Area Graduate Advisor, Aug. 1986- Aug. 89
ECE Space Allocation Committee, Sept. 1989-Aug. 1993 (chairman)
ECE Facilities Committee, Sept. 1993- Aug. 1996 (chairman)
ECE Areas Committee, Electromagnetics/Acoustics, Sept. 1993-present
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1995-Aug. 1995
ECE World Wide Web Home Page Committee, Sept. 1995-Aug. 1996
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1997-Aug. 1997
ECE Areas Committee, Materials and Quantum Electronics, Sept. 1993-present; chairman, Sept. 1996-present
Chair of ECE Graduate Studies Committee, May 1998-August 2006
ECE Chair's council, November 1999-2010
ECE Graduate Advisor, Sept. 1999- 2010
ECE Associate Chair, Sept. 2001-Dec. 2010
ECE peer Faculty Annual Review Committee, Sept. 2012-Aug. 2013

College:

Engineering Scholastic Appeals, Sept. 1984- Aug. 1985
Engineering Safety Committee, Sept. 1985- Aug. 1994 (chairman, Sept. 1989-Aug. 1994)

Aerospace Engineering Machine Shop, Sept. 1989-Aug. 1993
 College Annual Report Quality Team, Jan. 1994- Aug. 1994
 College Multimedia Committee, Sept. 1995-Aug. 2000
 Equal Opportunity in Engineering (EOE) Program, 1995-Dec. 1996
 Graduate Fellowship Review Committee, Sept. 2011-Aug. 2013

University:

Presidential Ad Hoc Committee on Research Infrastructure Enhancement, Jan. 1988 - Aug. 1994
 Research Safety Advisory Committee, Oct. 1991-present (chairman, Sept. 1996-1999)
 Ad Hoc Consultative Committee for the Selection of a Dean of the College of Engineering, Nov. 1995-May 1996
 Faculty Building Advisory Committee, Sept. 1995-Aug. 2000; Aug. 2003-Aug. 2004
 Ad Hoc Project Committee for Parking Garage # 4A, Sept. 1996-Aug. 2000
 Faculty Council, Sept. 1996-Aug. 2000; Sept. 2002 - Aug. 2004
 Faculty Advisory Committee on the Budget, Sept. 99 - Aug. 2000; Sept. 2008 – Aug. 2011 (vice chair Sept. 2009- Aug. 2010)
 Graduate Assembly, April 1997- Aug. 2000; Sept. 2001 - Aug. 2008
 Administrative sub-committee of GA, Sept. 1997-Aug. 1998; Sept. 2006-Aug. 2007
 Academic sub-committee of GA, Sept. 1998-Aug. 2000; Sept. 2001-Aug. 2006; Sept. 2007-Aug. 2008
 Chair, Graduate Assembly, 2004-2005
 Academy of Distinguished Teachers selection committee, academic year 1999-2000
 Outstanding Graduate Adviser selection committee, academic year 1999-2000
 Outstanding Graduate Coordinator selection committee, academic year 1999-2000
 Faculty Council, Sept. 2008 – Aug. 2012; Chair-elect Sept. 2009- Aug. 2010; Chair Sept. 2010- Aug. 2011; past chair: Sept. 2011-Aug. 2012
 Faculty Council Executive Committee, Sept. 2009 – Aug. 2012
 General Faculty Rules and Governance Committee, Sept. 2010 – Aug. 2015 (Chair, Sept. 2011 – Aug. 2013)
 Ad Hoc Consultative Committee for the Selection of a Dean of the Graduate School, Nov. 2012 – Sept. 2012
 Secretary of the General Faculty and Faculty Council, Sept. 2013 – Aug. 2015
 Committee on Undergraduate Degree Program review, Sept. 2013 – Aug. 2015
 Faculty Council Executive Committee, Sept. 2013 – Aug. 2015
 Faculty Committee on Committees, *ex officio* member, Sept. 2013 – Aug. 2015

UT System:

Task Force on Doctoral Programs and Post-Doctoral Experience, Spring-Fall 2006

University of Texas System Faculty Advisory Council, Sept. 2009- Aug. 2011

State of Texas:

Texas Higher Education Coordinating Board Graduate Education Advisory Committee (GEAC), September 1, 2015 - August 31, 2018.

Evidence of Teaching Effectiveness

Senior Design Projects:

Umer Yousafzai and Venuka Jayatilaka, Spring 1994

Chris Eiting and Sonny Gonzalez, Spring 1994

David Lee and David Onsongo, Fall 1996

Dave Pyle and Aruna Murthy, Spring 1999

Hitesh Mehta and Edward Zhu, Spring 1999, "Giving the electronic tongue a sense of good taste: image analysis tools and GUI"

Gus Espinosa and Donnie Garcia, Spring 1999, "Design and Implementation of a Computer Interfacing Circuit to Control LED's for use with a Chemical Sensor"

Natthanant Pon Skulkaew and Prem Nainani, Spring 2001, "PC-based data acquisition and wireless transmission system"

Matthew Andringa and Allen Hall, Spring 2001, "Non-Invasive RFID Weld Inspection"

Michael Amalfitano and Sapun Parekh, Spring 2002, "Output circuitry for a transmitter used in an Electronic Structural Surveillance system"

Kunal Patel and Jacy Little, Spring 2002, "Swept, high frequency oscillator to work in an Electronic Structural Surveillance (ESS) system"

Dong Pak, Spring 2002, "Automated image-processing software of an electronic chemical sensor"

Rajesh Nerlikar, Jonathan Solomon, Spring 2003, "Wireless Data Acquisition System for Bluetooth-enabled RFID Readers"

Nola Li, Judith Chen, Maria Huang, Fall 2003, "Design and build a tuning network for a swept frequency reader used in structural health analysis"

Tuenlap (Daniel) Chan, Imranul Islam, Derek Choi, Spring 2004, "Design and build an RFID Interrogator Receiver"

John McKee and Terence Man, Spring 2007, "Improved Corrosion Sensors"

Abdulaziz Beayeyz, Sravan Bhagavatula, Rahul Mitra, Shasi Munukutla, Spyder Spann, Fall 2009, "Portable Corrosion Detector"

Jonathan Pham, Po-Han Wu, Josh Schulte, Pritesh Solanki, Mesele Bedasa, Spring 2011- Fall 2011, "Multi-Sensor Robotics Platform"

Raymund Lee, Simon Chow, Connor Landy, Kevin Woo, and Anirudh Kashyap, Fall 2012-Spring 2013, "Variable Frequency RFID Tag and Reader"

Javier Chacon, Joshua Poncik, Joshua Orozco, Sebastian Salomon, Yongcong Zou, Fall 2013-Spring 2014, "Environmental Sensor Monitoring Network"

Organized Classes Taught:

EE 363M Introduction to Microwaves, Spring 1984, # 16455
EE 396K VLSI Fabrication Techniques, Fall 1984, # 16255
EE 379K Integrated Circuit Fabrication, Spring 1985, # 16055
EE 396K VLSI Fabrication Techniques, Fall 1985, # 16275
EE 379K Integrated Circuit Fabrication, Fall 1985, # 16070
EE 396K VLSI Fabrication Techniques, Spring 1986, # 17680
EE 379K Integrated Circuit Fabrication, Spring 1986, # 17450
EE 396K VLSI Fabrication Techniques, Fall 1986, # 15245
EE 379K Integrated Circuit Fabrication, Fall 1986, # 15020
EE 396K VLSI Fabrication Techniques, Spring 1987, # 15205
EE 379K Integrated Circuit Fabrication, Spring 1987, # 14970
EE 396K VLSI Fabrication Techniques, Fall 1987, # 15010
EE 440 Integrated Circuit Fabrication, Fall 1987, # 14545
EE 363M Introduction to Microwaves, Spring 1988, # 14535
EE 396K VLSI Fabrication Techniques, Spring 1988, # 14865
EE 440 Integrated Circuit Fabrication, Spring 1988, # 14390
EE 396K VLSI Fabrication Techniques, Fall 1988, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1988, # 14705
EE 363M Introduction to Microwaves, Spring 1989, # 14525
EE 396K VLSI Fabrication Techniques, Spring 1989, # 14855
EE 396K VLSI Fabrication Techniques, Fall 1989, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1989, # 14705
EE 363M Introduction to Microwaves, Spring 1990, # 14050
EE 396K VLSI Fabrication Techniques, Spring 1990, # 14355, 14360
EE 440 Integrated Circuit Fabrication, Spring 1990, # 13915, 13920
EE 396K VLSI Fabrication Techniques, Fall 1990, # 14630, 14635
EE 440 Integrated Circuit Fabrication, Fall 1990, # 14200, 14205
EE 363M Introduction to Microwaves, Spring 1991, # 14365
EE 396K VLSI Fabrication Techniques, Spring 1991, # 14660, 14665, 14670
EE 440 Integrated Circuit Fabrication, Spring 1991, # 14220, 14225, 14230
EE 396K VLSI Fabrication Techniques, Fall 1991, # 14865, 14860
EE 440 Integrated Circuit Fabrication, Fall 1991, # 14425, 14430
EE 363M Introduction to Microwaves, Spring 1992, # 14270
EE 396K VLSI Fabrication Techniques, Spring 1992, # 14545, 14550, 14555
EE 440 Integrated Circuit Fabrication, Spring 1992, # 14130, 14135
EE 396K VLSI Fabrication Techniques, Fall 1992, # 15095, 15100, 15105
EE 440 Integrated Circuit Fabrication, Fall 1992, # 14670, 14675
EE 397K Microwave Devices, Spring 1993, # 14805
EE 396K VLSI Fabrication Techniques, Fall 1993, # 14800, 14805, 14810
EE 440 Integrated Circuit Fabrication, Fall 1993, # 14385, 14390
EE 363M Introduction to Microwaves, Spring 1994, # 14370
EE 396K VLSI Fabrication Techniques, Fall 1994, # 14365

EE 440 Integrated Circuit Fabrication, Fall 1994, # 13870
 EE 397K Electromagnetics in Packaging, Spring 1995, # 14555
 EE 396K VLSI Fabrication Techniques, Fall 1995, # 14765
 EE 440 Integrated Circuit Fabrication, Fall 1995, # 14260
 EE 397K Electromagnetics in Packaging, Spring 1996, # 14695
 EE 382M Simulation Methods in CAD/VLSI, Spring 1996, # 14500
 EE 396K VLSI Fabrication Techniques, Fall 1996, # 14535
 EE 440 Integrated Circuit Fabrication, Fall 1996, # 14090
 EE 382M Simulation Methods in CAD/VLSI, Spring 1997, # 14325
 EE 363M Introduction to Microwaves, Spring 1997, # 14120
 EE 396K VLSI Fabrication Techniques, Fall 1997, # 15315
 EE 440 Integrated Circuit Fabrication, Fall 1997, # 14820
 EE 363M Introduction to Microwaves, Spring 1998, # 14530
 EE 397K Microwave Devices, Spring 1998, # 14950
 EE 396K VLSI Fabrication Techniques, Fall 1998, # 15475
 EE 440 Integrated Circuit Fabrication, Fall 1998, # 14965
 EE 363M Introduction to Microwaves, Spring 1999, # 14825
 EE 397K Microwave Devices, Spring 1999, # 15260
 EE 396K VLSI Fabrication Techniques, Fall 1999, # 15340
 EE 440 Integrated Circuit Fabrication, Fall 1999, # 14820
 EE 363M Introduction to Microwaves, Spring 2000, # 14755
 EE 396K VLSI Fabrication Techniques, Fall 2000, # 15600
 EE 440 Integrated Circuit Fabrication, Fall 2000, # 15100
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2001, #15170
 EE 396K VLSI Fabrication Techniques, Fall 2001, # 15725
 EE 440 Integrated Circuit Fabrication, Fall 2001, # 15230
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2002, #15330
 EE 396K VLSI Fabrication Techniques, Fall 2002, # 16050
 EE 440 Integrated Circuit Fabrication, Fall 2002, # 15485
 EE 397K Microwave Devices, Spring 2003, # 15110
 EE 396K VLSI Fabrication Techniques, Fall 2003, # 15580
 EE 440 Integrated Circuit Fabrication, Fall 2003, # 15095
 EE 325 Electromagnetic Engineering, Spring 2004, # 14345
 EE 396K VLSI Fabrication Techniques, Fall 2004, # 16250
 EE 440 Integrated Circuit Fabrication, Fall 2004, # 15715
 EE 396K 26-Microelectromechanical Systems, Spring 2005, # 15690
 EE 396K VLSI Fabrication Techniques, Fall 2005, # 16455
 EE 440 Integrated Circuit Fabrication, Fall 2005, # 15930
 EE 396K VLSI Fabrication Techniques, Fall 2006, # 17040
 EE 440 Integrated Circuit Fabrication, Fall 2006, # 16430
 EE 325 Electromagnetic Engineering, Spring 2007, # 15765
 EE 396K VLSI Fabrication Techniques, Fall 2007, # 17425
 EE 440 Integrated Circuit Fabrication, Fall 2007, # 16770
 EE 396K-26 Microelectromechanical Systems, Spring 2008, # 16815
 EE 396K VLSI Fabrication Techniques, Fall 2008, # 17380
 EE 325 Electromagnetic Engineering, Spring 2009, # 16000

EE 396K-24 Microwave Devices, Spring 2010, # 16975
 EE 396K VLSI Fabrication Techniques, Fall 2010, # 17075, 17080, 17085, 17090
 EE 440 Integrated Circuit Fabrication, Fall 2010, # 16540, 16545, 16550, 16555
 EE 396K VLSI Fabrication Techniques, Fall 2011, # 17295, 17300, 17305, 17310
 EE 440 Integrated Circuit Fabrication, Fall 2011# 16760, 16765, 16770, 16775
 EE 396K 26-Microelectromechanical Systems, Spring 2012, #17070
 EE 396K VLSI Fabrication Techniques, Fall 2012, # 17185, 17190, 17195, 17200
 EE 440 Integrated Circuit Fabrication, Fall 2012, # 16640, 16645, 16650, 16665
 EE 363M Introduction to Microwaves, Spring 2013, # 16605
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2013, # 17425, 17430, 17435, 17440
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2013, # 16790, 16795, 16800, 16805
 EE 396K-24 Microwave Devices. Spring 2014, #17440
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2014, #17525, 17530, 17535, 17540
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2014, #16960, 16965, 16970, 16975
 EE 363M Microwave and Radio Frequency Engineering, Spring 2015, #16355
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2015, #16965, 16970, 16975
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2015, #16480, 16485, 16490
 EE 363M Microwave and Radio Frequency Engineering, Spring 2016, #16550
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2016
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2016
 EE 396K 26-Microelectromechanical Systems, Spring 2017
 EE 363M Microwave and Radio Frequency Engineering, Spring 2018, #15890
 EE 363M Microwave and Radio Frequency Engineering, Spring 2019, #16625
 EE 363M Microwave and Radio Frequency Engineering, Spring 2020, #16695

Continuing Education Courses Taught

"Microelectronics Fabrication - Chemical Aspects," with Isaac Trachtenberg,
 Continuing Engineering Studies, College of Engineering, The University of
 Texas at Austin, June 1-4, 1987.
 "Integrated Circuit Process & Design," with M. R. Mercer, Motorola short course,
 Continuing Engineering Studies, College of Engineering, The University of

Texas at Austin:

- Aug.-Sept., 1987
- Nov.-Dec., 1987
- Nov.-Dec., 1988
- March-April, 1989
- Aug.-Sept., 1989
- Nov.-Dec., 1989
- Feb.-March, 1990
- April, 1990
- Aug., 1990

"Integrated Circuit Processing and Design," with L. T. Pillage, Advanced Micro Devices short course, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin:

- Oct.-Nov., 1990
- June-July, 1991

"Microelectronics Fabrication," for the Fellows of the Senior Service College Fellowship Program, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, yearly 1993-2003.