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Title: METHOD FOR EMBEDDING A COMPONENT IN A BASE

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,732,909 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 7,732,909
APPLE-1002	U.S. Patent No. 7,732,909 File History
APPLE-1003	Declaration of Dr. Dean Neikirk
APPLE-1004	Certified Translation of JP Application Publication 2001-339165A (“Sakamoto”)
APPLE-1005	U.S. Patent Application Publication No. 2002/0175402 (“McCormack”)
APPLE-1006	U.S. Patent No. 6,489,685 (“Asahi”)
APPLE-1007	U.S. Patent Application Publication No. 2001/0030059 (“Sugaya”)
APPLE-1008	U.S. Patent Application Publication No. 2002/0020898 (“Vu”)
APPLE-1009	RESERVED
APPLE-1010	RESERVED
APPLE-1011	Certified Translation of JP Patent No. 3207174 (“Hayashi”)
APPLE-1012	Certified Translation of JP Patent Application Publication No. 2002-016327 (“Eiji”)
APPLE-1013	U.S. Patent No. 6,335,571 (“Capote”)
APPLE-1014	U.S. Patent No. 6,297,551 (“Dudderar”)
APPLE-1015	U.S. Patent No. 6,404,052 (“Kurita”)
APPLE-1016	Certified Translation of JP Patent Application Publication No. 2001-068624A (“Imoto”)
APPLE-1017	Certified Translation of PCT Publication No. WO 00/09623 (“Watanabe”)

APPLE-1018	U.S. Patent No. 4,179,802 (“Joshi”)
APPLE-1019	U.S. Patent No. 5,608,262 (“Degani”)
APPLE-1020	U.S. Patent No. 5,321,210 (“Kimbara”)
APPLE-1021	U.S. Patent No. 5,146,674 (“Frankeny”)
APPLE-1022	JP Patent Application Publication No. 2001-339165A (“Sakamoto”)
APPLE-1023	JP Patent No. 3207174 (“Hayashi”)
APPLE-1024	JP Patent Application Publication No. 2002-016327 (“Eiji”)
APPLE-1025	JP Patent Application Publication No. 2001-068624A (“Imoto”)
APPLE-1026	PCT Publication No. WO 00/09623 (“Watanabe”)
APPLE-1027	Certified Translation of JP Patent Application Publication No. 2001-156457 (“Takayama”)
APPLE-1028	JP Patent Application Publication No. 2001-156457 (“Takayama”)
APPLE-1029	U.S. Patent No. 5,745,984 (“Cole”)
APPLE-1030	R. Aschenbrenner, A. Ostmann, U. Beutler, J. Simon and H. Reichl, “Electroless nickel/copper plating as a new bump metallization,” in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 18, no. 2, pp. 334-338, May 1995, doi: 10.1109/96.386270
APPLE-1031	W. W. Flack, Ha-Ai Nguyen, E. Capsuto and C. McEwen, “Characterization of a thick copper pillar bump process,” 2007 12th International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces, San Jose, CA, USA, 2007, pp. 208-213.
APPLE-1032	Xiang Dai, M. V. Brillhart, M. Roesch and P. S. Ho, “Adhesion and toughening mechanisms at underfill interfaces for flip-chip-on-organic-substrate packaging,” in

IEEE Transactions on Components and Packaging
Technologies, vol. 23, no. 1, pp. 117-127, March 2000

APPLE-1033

D. Suryanarayana, T. Y. Wu and J. A. Varcoe,
“Encapsulants used in flip-chip packages,” in IEEE
Transactions on Components, Hybrids, and Manufacturing
Technology, vol. 16, no. 8, pp. 858-862, Dec. 1993

APPLE-1034

U.S. Patent Application Publication No. 2001/0033889
 (“Bhatt”)

LISTING OF CLAIMS

Claim 1	
[1pre]	A circuit board, comprising:
[1a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[1b]	conductive patterns on both sides of the insulating material layer;
[1c]	at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;
[1d]	conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and
[1e]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 2	
[2]	The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.
Claim 3	
[3]	The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.
Claim 4	
[4]	The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

Claim 5	
[5]	The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.
Claim 6	
[6]	The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.
Claim 7	
[7]	The circuit board of claim 6, wherein the filler material contains epoxy.
Claim 8	
[8pre]	The circuit board of claim 1, wherein
[8a]	said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and
[8b]	the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.
Claim 9	
[9]	The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
Claim 10	
[10]	The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

Claim 11	
[11pre]	The circuit board of claim 1, wherein
[11a]	said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and
[11b]	said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.
Claim 12	
[12pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:
[12a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[12b]	conductive patterns on both sides of the insulating material layer;
[12c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and
[12d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 13	
[13]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

Claim 14	
[14]	The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.
Claim 15	
[15]	The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.
Claim 16	
[16]	The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.
Claim 17	
[17pre]	The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise
[17a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[17b]	conductive patterns on both sides of the insulating material layer,
[17c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[17d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

Claim 18	
[18]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.
Claim 19	
[19pre]	The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises
[19a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[19b]	conductive patterns on both sides of the insulating material layer,
[19c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[19d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 20	
[20pre]	The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises
[20a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[20b]	a conductive pattern on the insulating material layer,

[20c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[20d]	contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 21	
[21]	The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.
Claim 22	
[22]	The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.
Claim 23	
[23]	The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.
Claim 24	
[24]	The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

Claim 25	
[25]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.
Claim 26	
[26]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.
Claim 27	
[27pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising:
[27a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[27b]	conductive patterns on both sides of the insulating material layer;
[27c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and
[27d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and
[27e]	at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.
Claim 28	
[28]	The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

Claim 29	
[29]	The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.
Claim 30	
[30]	The circuit board of claim 1, comprising a metal plate above the microcircuit.
Claim 31	
[31]	The circuit board of claim 1, comprising a metal plate below the microcircuit.
Claim 32	
[32]	The circuit board of claim 1, comprising a metal plate above and below the microcircuit.
Claim 33	
[33]	The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

I. INTRODUCTION

Apple Inc. (“Apple”/“Petitioner”) petitions for IPR of claims 1-33 (“Challenged Claims”) of U.S. Patent No. 7,732,909 (“’909 patent”).

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR, as further supported by the Declaration of Dr. Neikirk (APPLE-1003).

Ground	Claims	§103 Basis
Ground 1A	12-27	Asahi
Ground 1B	1-33	Asahi-Dudderar
Ground 1C	12-27	Asahi-Joshi
Ground 1D	1-33	Asahi-Dudderar-Joshi
Ground 2A	12-27	Hayashi
Ground 2B	1-33	Hayashi-Eiji
Ground 2C	12-27	Hayashi-Watanabe
Ground 2D	1-33	Hayashi-Eiji-Watanabe

Each reference pre-dates the ’909 patent’s earliest possible priority date (January 31, 2002; “Critical Date”) and qualifies as prior art.

Reference	Date	Pre-AIA § Basis
Asahi(APPLE-1006)	Jan. 3, 2002 (filed)	§102(e)

Hayashi(APPLE-1011)	Sep. 10, 2001 (issued)	§102(a)/(b)
Dudderar(APPLE-1014)	Oct. 2, 2001 (issued)	§102(a)/(b)
Eiji(APPLE-1012)	Jan. 18, 2002 (published)	§102(a)/(b)
Joshi(APPLE-1018)	Dec. 25, 1979 (issued)	§102(b)
Watanabe(APPLE-1017)	Feb. 24, 2000 (published)	§102(b)

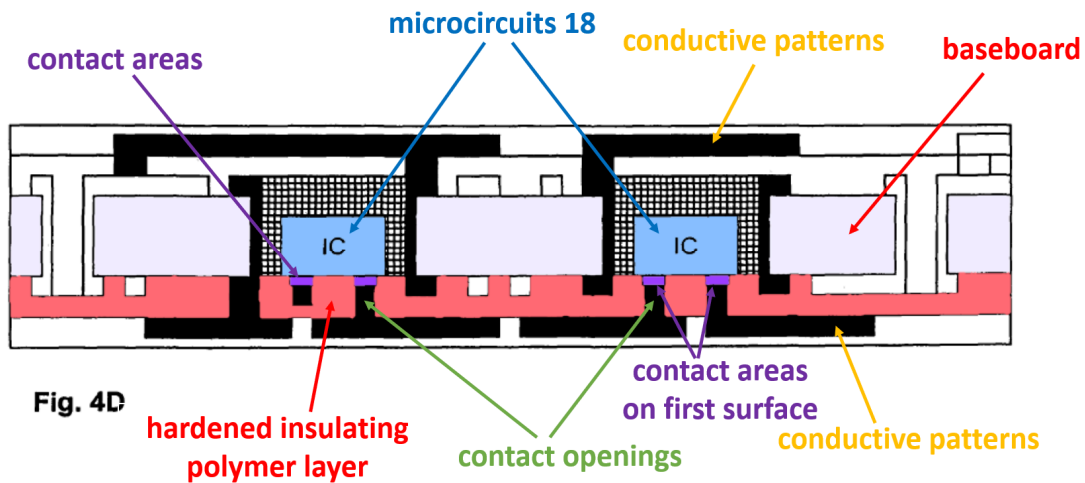
Hayashi (APPLE-1011), Eiji (APPLE-1012), and Watanabe (APPLE-1017) are certified English translations of JP3207174 (“Hayashi”/APPLE-1023), JP2002-016327 (“Eiji”/APPLE-1024), and WO00/09623 (“Watanabe”/APPLE-1026).

The combinations presented in the Grounds are directed to the prior art references (APPLE-1023, APPLE-1024, APPLE-1026), for which the translations are cited throughout to identify relevant aspects thereof.

III. THE '909 PATENT

A. Brief Description

The '909 patent recites an electronic module having electronic components embedded in a base. APPLE-1001, Title, Abstract. Figure 4D shows semiconductor components (microcircuits 18) embedded inside a baseboard and between two conductive pattern layers in which the components have contact areas on a first surface that is against a hardened insulating polymer layer. APPLE-1001, FIG. 4D and related descriptions, Cls. 1, 12; APPLE-1003, ¶61.



APPLE-1003, ¶61 (APPLE-1001, FIG. 4D (Annotated))

The '909 patent describes conductive material covering the sidewalls of the holes where microcircuits 18 are embedded, for protection from electromagnetic interference (EMI). *E.g.*, APPLE-1001, 3:61-4:9, 8:34-41, 8:64-66, Cl. 1. The '909 patent recites copper in the contact openings which “contains at least one of electrochemically deposited copper and chemically deposited copper.” *E.g., id.*, 6:21-25, Cls. 1, 12.¹ APPLE-1003, ¶62.

¹ “Electrochemically deposited copper” and “chemically deposited copper” are product-by-process elements that merely recite copper deposited by an electrochemical or chemical process. The recited processes have no patentable weight for purposes of determining unpatentability. *Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009) (“a product in the prior art made by a

While the '909 patent touts these routine aspects as “invention,” they were not innovative. Those of skills in the art were aware of the structure having electrical components embedded in a base-like circuit board to achieve miniaturization of electronic devices, and conductive material on the sidewalls of holes incorporating the components to achieve EMI protection. APPLE-1003, ¶¶67-338; *infra*, §VI.

B. Prosecution History Summary

During prosecution, a single substantive office action was issued, rejecting independent claim 1 and other claims as anticipated by Vu (2002/0020898), and claims 11 and 27 as unpatentable over Vu and Official Notice regarding chemical and electrochemical plating. APPLE-1002, 53-58. Pending claims 7, 26 and 29 were indicated as directed to allowable subject matter, with claims 7 and 26 each reciting “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit” and claim 29 reciting “a metal foil below at least one of the microcircuits.” *Id.*, 53-58, 100-104.

In response, applicant stated that “Claim 1 has been amended to incorporate the features of Claim 7, [and] Claim 14 has been amended to incorporate the

different process can anticipate a product-by-process claim, but an accused product made by a different process cannot infringe a product-by-process claim”).

features of Claim 26.” *Id.*, 43-45. Instead, however, the features of Claim 26 were **not actually introduced into independent claim 14**. Independent claim 14 (current claim 12) did not recite “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit.” APPLE-1001, Cl. 12. Following Applicant’s amendments that remarkably omitted the narrowing features Applicant purported to include in the claims, a notice of allowance was issued, ending prosecution prematurely, without reciting features purported to overcome the Vu rejection and without application of pertinent prior art discussed herein. APPLE-1002, 18-21.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the ’909 patent (a “POSITA”) would have had at least a Bachelor’s degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. APPLE-1003, ¶23.

V. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. The Board has repeatedly explained that “claim terms need only be construed to the

extent necessary to resolve the controversy,” and for purpose of the particular Grounds in this Petition, no formal construction is necessary because the prior art presented below satisfies the claims under any reasonable construction consistent with *Phillips. Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011)².

VI. DETAILED EXPLANATION OF GROUNDS

A. GROUND 1A – Asahi renders obvious Claims 12-27

1. Asahi³

Asahi describes a “component built-in module” where a semiconductor 703 and a circuit component 706 are embedded in electric insulation layer 701.

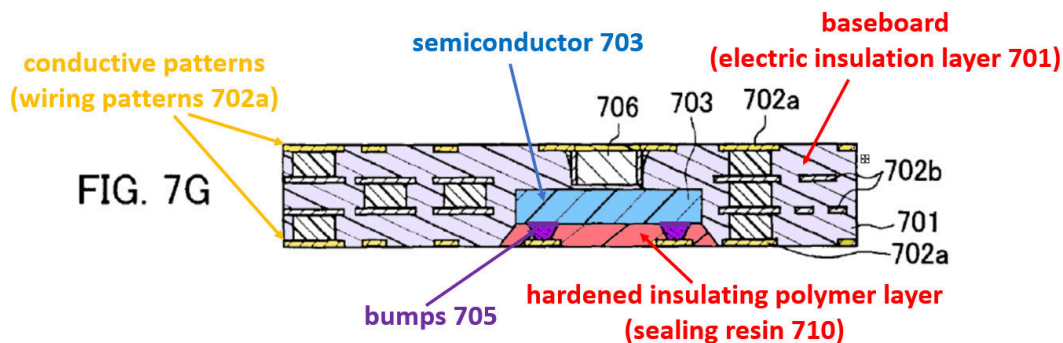
APPLE-1006, 15:50-17:44, FIG. 7; *see also*, Title, Abstract, 1:8-12, 3:44-46, 6:33-9:17, 9:18-11:25, 11:26-12:51, 17:55-18:13, FIG. 8. Wiring patterns (e.g., wiring

² Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

³ General descriptions provided for this and other references and combinations are incorporated into each subsection and mapping of the claims that includes citations to these references. All emphasis added unless otherwise indicated.

patterns 702a) made of “a metal foil” or a lead frame obtained by processing “a metal plate” are formed on both surfaces of the wiring board of the component built-in module. *Id.*, 7:23-65, FIG. 7; *see also*, 6:33-37, 8:66-9:4, 16:13-43, 17:35-36; APPLE-1003, ¶¶67-70. Bumps 705 (“bumps,” and in one example, “stud bumps”) on an active surface of the semiconductor provide connection between the semiconductor 703 and “wiring patterns 702a” on one surface of the module. *Id.*, FIG. 7, 16:39-66; *see also*, 8:9-10, 10:33-45, 11:47-54, 13:27-29, 14:25-27, 15:9-12, 17:59-61; APPLE-1003, ¶71.

Asahi describes “a sealing resin” is “injected between the semiconductor 703 and the wiring pattern 702a” to “prevent[] the semiconductor 703 from being damaged and improv[e] the reliability.” APPLE-1006, 16:52-62, FIG. 7; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13, FIG. 8. APPLE-1003, ¶¶72-73.



APPLE-1003, ¶68 (APPLE-1006, FIG. 7G (Annotated))

Asahi describes a multi-layered structure with electronic components, such as semiconductor bare chips, in each layer, to achieve “high density” and

“improved performance.” *E.g.*, APPLE-1006, 1:14-42, 3:44-49, 12:63-65, FIG. 4, FIGS. 7-10; APPLE-1003, ¶¶74-75.

2. Application to Challenged Claims

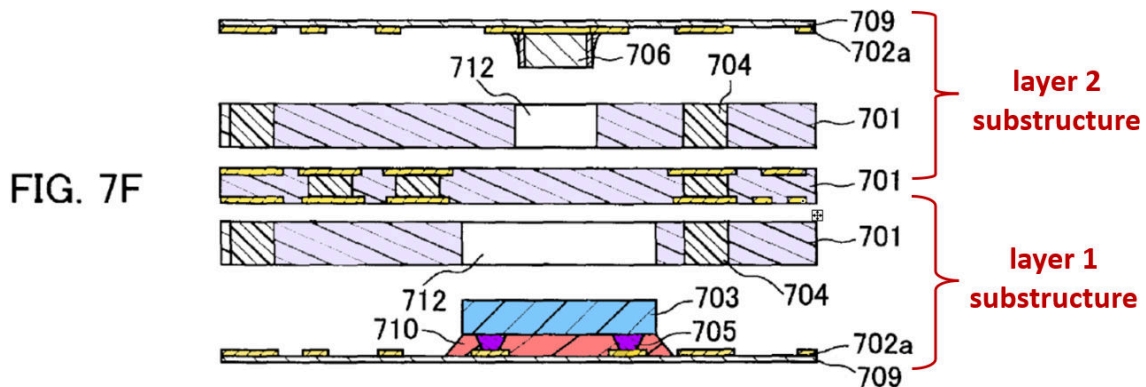
[12pre]

To the extent the preamble is limiting, Asahi provides [12pre]. APPLE-1003, ¶¶97-107. For example, Asahi describes an electronic component built-in module (*multi-layered circuit board*) that includes *at least two circuit board substructures* laminated *on top of each other*. APPLE-1006, FIGS. 4-10, 12:53-19:37; APPLE-1003, ¶97. *Supra*, VI.A.1.

Asahi describes the use of “generally used wiring board” such as “a glass-epoxy substrate” for its electric insulation layer to “reduc[e] the production cost.” APPLE-1006, 3:60-65; *see also id.*, 1:23-25, 3:11-38; 14:29-30, 15:62-16:2, Cls. 11, 21; APPLE-1006, 3:66-4:7 (“provided integrally”); APPLE-1003, ¶¶98-99. Asahi’s construction is thus just like the ’909 patent’s example circuit board material. APPLE-1001, 3:46-55 (“a glass-fibre reinforced epoxy board”).

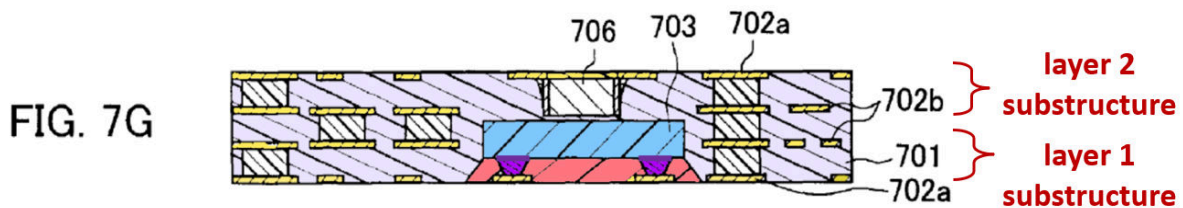
Figure 7F illustrates an example of this multi-layered structure, having at least two circuit board substructures, annotated as “layer 1 substructure” (i.e. substructure 1, which contains one or more layers) and “layer 2 substructure” (i.e. substructure 2, which contains one or more layers), positioned on top of each other before lamination to form a unified component built-in module. APPLE-1003,

¶100. Layer 1 substructure (*at least one of said circuit board substructures*) includes, among other things, semiconductor 703 mounted on wiring patterns 702a, and an electric insulation layer 701 having through hole 712 to receive semiconductor 703. Layer 2 substructure includes, among other things, component 706 mounted on another wiring patterns 702a, and an electric insulation layer 701 having through hole 712 to receive component 706. APPLE-1006, FIG. 7 (and related descriptions); *see also id.*, FIGS. 4-10 (and related descriptions of examples having additional layers laminated on top of each other); APPLE-1003, ¶¶100-107.



APPLE-1003, ¶100 (APPLE-1006, FIG. 7F (Annotated))

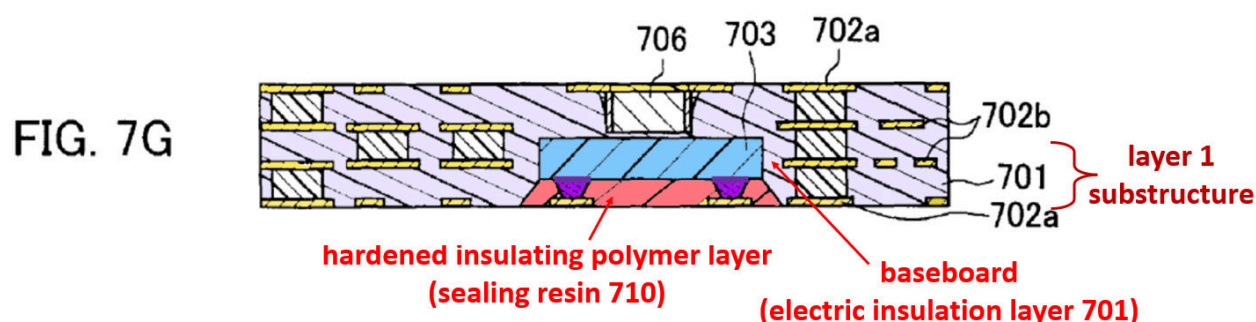
Figure 7G shows the multi-layered circuit board structure after lamination.



APPLE-1003, ¶101 (APPLE-1006, FIG. 7G (Annotated))

[12a]

Asahi's circuit board substructure (e.g., layer 1 substructure below) provides an *insulating material layer* including a *baseboard* (e.g., unified “electric insulation layer 701” of layer 1 substructure after lamination of various layers and components) and a *hardened insulating polymer layer* (e.g., “sealing resin 710”). APPLE-1006, FIG. 7, 3:66-4:7, 15:51-17:44; 16:52-62, FIGS. 7, 8; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13 *supra*, §VI.A.2, Analysis of [12pre]. APPLE-1003, ¶¶108-114.



APPLE-1003, ¶108 (APPLE-1006, FIG. 7G (Annotated))

Notably, the composition of Asahi's “electric insulation layer” is just like that of the baseboard 1 recited by the '909 patent. *Supra*, §VI.A.2, Analysis of [12pre]. APPLE-1003, ¶110.

Asahi describes “sealing resin 710” (*hardened insulating polymer layer*), includes “[a]n underfill resin used for ordinary flip chip bonding,” and “may be injected between the semiconductor 703 and the wiring pattern 702a” to “prevent[] the semiconductor 703 from being damaged and improv[e] the reliability.”

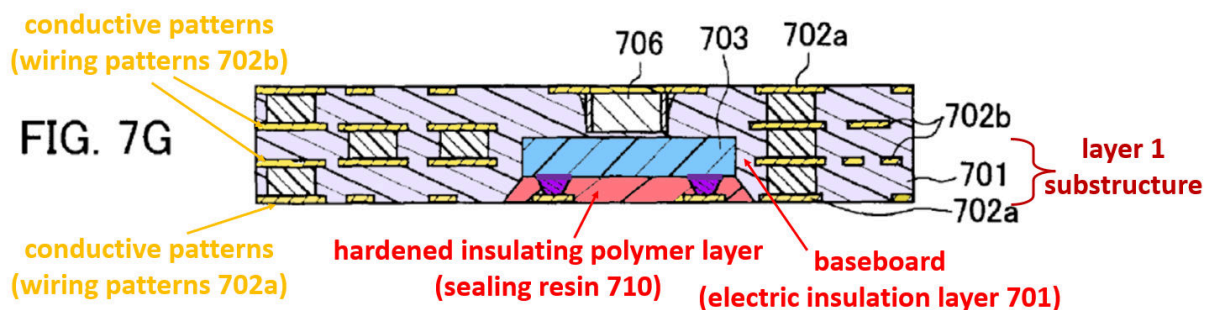
APPLE-1006, 16:52-62, FIGS. 7, 8; *see also id.*, 8:2-6, 10:45-53, 11:56-65, 17:55-18:13. To be clear, a POSITA would have recognized and found obvious that the underfill resin is a hardened insulating polymer, especially based on Asahi's express description of resin materials. APPLE-1003, ¶111. Asahi describes an electric insulation layer "made of a mixture of a filler and an insulating resin," and that the filler contains glass, e.g., "silica," and the insulating resin contains an "epoxy resin," for example. APPLE-1006, 3:11-38. Moreover, Asahi describes that "[b]y selecting an appropriate insulating resin material, it is possible to improve a heat resistance, an electric insulation, and high frequency characteristics." *Id.* A POSITA would have been motivated to utilize similar polymer material for the sealing resin to achieve similar desired characteristics. APPLE-1003, ¶¶112-113; *see also supra*, § VI.A.2, Analysis of [12pre] (electric insulation layer made of glass-epoxy containing "a reinforcing material such as a glass cloth or an unwoven fabric"). Additionally, a POSITA would have done so to further avoid stresses due to mismatch in "a heat conductivity, a coefficient of linear expansion, a dielectric constant, etc." between the sealing resin and the surrounding electric insulation layer. *Supra*, § VI.A.1; APPLE-1006, 3:14-16; APPLE-1003, ¶113 (citing APPLE-1013, 2:1-6).

The sealing resin is hardened, including through a curing process by heating of a suitable material "used for ordinary flip chip bonding," such that the

semiconductor embedded in the electric insulation layer and sealing resin “can be formed in a plate form,” and to effectuate Asahi’s objectives of the sealing resin. APPLE-1006, 10:62-67 (“cured by heating after pressing”); APPLE-1003, ¶114; *see also* APPLE-1001, 5:32-39.

[12b]

Asahi describes conductive wiring patterns 702a and 720b (*conductive patterns*) on both sides of the insulating material layer. APPLE-1003, ¶115. For example, Asahi describes conductive wiring patterns 702a at the lower side (on the lower surface of the component built-in module) and at least one layer of wiring patterns 702b on an upper side of the layer 1 substructure (*conductive patterns on both sides of the insulating material layer*). *Supra*, §VI.A.2, Analysis of Element [12a]; APPLE-1006, FIG. 7; APPLE-1003, ¶¶115-118.



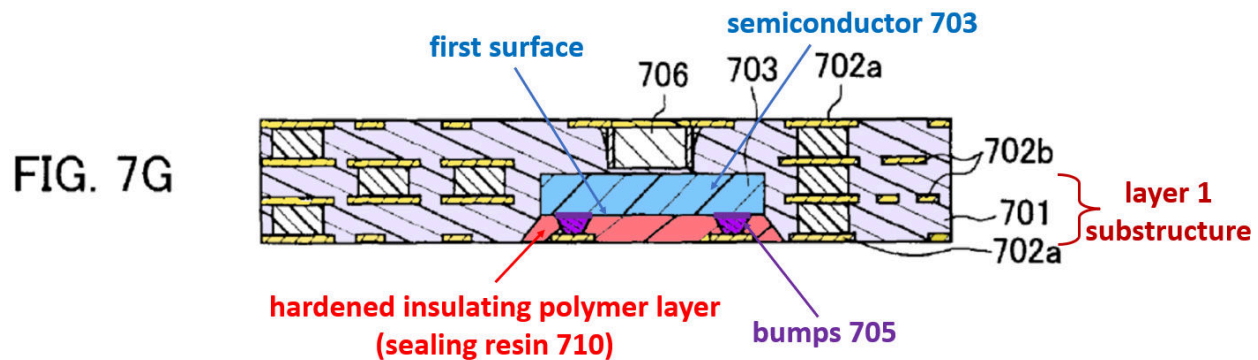
APPLE-1003, ¶117 (APPLE-1006, FIG. 7G (Annotated))

The wiring patterns, including wiring patterns 702a and 702b, are “made of a material having an electric conductivity.” APPLE-1006, 7:23-26. Thus, Asahi’s wiring patterns are *conductive patterns*. *See also* APPLE-1006, FIG. 7, 16:39-

17:44; APPLE-1003, ¶119.

[12c]

Asahi describes “semiconductor 703” (*at least one microcircuit*) that is *embedded in the insulating material layer* of the layer 1 circuit board substructure. *Supra*, §§VI.A.1, VI.A.2, Analysis of Element [12a]; APPLE-1006, FIG. 7, 3:44-46, 15:62-17:40 (“By pressing and heating, the semiconductor 703 ... [is] embedded in the electric insulation layers 701”), APPLE-1003, ¶120.



APPLE-1003, ¶120 (APPLE-1006, FIG. 7G (Annotated))

To be clear, a POSITA would have understood that semiconductors (e.g., semiconductor 703) in devices having “high density” circuitry such as “large scale integrated circuits (LSIs)” provide a microcircuit. APPLE-1006, 1:32-42; APPLE-1003, ¶121.

Semiconductor 703 has *a first surface* with *contact areas* thereon (e.g., semiconductor die’s pads on its active surface), where conductors such as bumps (e.g., bumps 705) are formed to provide electrical connections between the

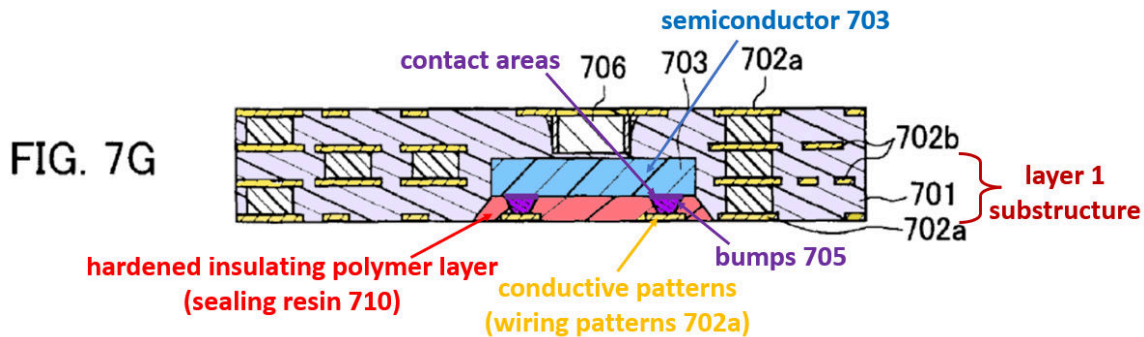
semiconductor 703 and wiring patterns 702a. APPLE-1006, 16:39-66 (“stud bumps” and “bumps”); *see also*, 8:9-10, 10:33-45, 11:47-54, 13:27-29, 14:25-27, 15:9-12, 17:59-61; APPLE-1003, ¶122.

The semiconductor 703 is inside the material layer in a hole (e.g., “hole 712” in electric insulation layer 701). APPLE-1006, 17:4-24; FIGs. 7F-7G. As shown in FIG. 7G above, *the first surface of* semiconductor 703 is *against* sealing resin 710 (*hardened insulating polymer layer*). *Supra*, §VI.A.2, Analysis of Element [12a]; APPLE-1006, FIG. 7, 16:39-66; APPLE-1003, ¶¶123-124.

[12d]

Asahi provides *contact openings* formed in the hardened sealing resin 710 (*hardened insulating polymer layer*) to accommodate bumps (e.g., bumps 705) or the like. APPLE-1003, ¶125. As discussed in §VI.A.2 (Analysis of Element [12c]), bumps form *electrical contacts* between *the contact areas of* semiconductor 703 (*microcircuit*) and wiring patterns 702a (*at least one of the conductive patterns*). APPLE-1006, FIG. 7E-7G (showing bumps 705 in connection with contact areas of semiconductor 703 and wiring patterns 702a); APPLE-1003, ¶125; *see also* APPLE-1006, 16:39-66, 8:9-10, 10:44-45 (“bump 205 and the conductive adhesive may be used in combination”), 11:47-54 (305 can be a conductive copper adhesive), 13:27-29 (“bumps 405”), 14:25-27 (“bumps 505”), 15:9-12 (“bumps 605”); APPLE-1003, ¶¶126-127. The electrical contacts

in the contact openings include “copper.” APPLE-1003, ¶128.



APPLE-1003, ¶125 (APPLE-1006, FIG. 7G (Annotated))

A POSITA would have recognized and found obvious, from Asahi’s description, that bumps for mounting semiconductor on the wiring patterns would have been beneficially made of *copper*, a conventional and widely used conductive material in flip chip bonding. APPLE-1003, ¶129. Asahi expressly describes benefits of high conductivity and low migration of copper in making electrical connections of its high-density component built-in module. *E.g.*, APPLE-1006, 8:19-35 (“Copper particularly is preferable since it has a high conductivity and migration of the same hardly occurs”). APPLE-1003, ¶129.

Even if Asahi did not expressly describe copper for bumps in the contact openings, a POSITA would have implemented copper as a conventional and suitable material choice to effectuate Asahi’s electrical contact objective, based on Asahi’s description. APPLE-1003, ¶130 (citing APPLE-1020, 10:15-21 (“copper bumps”)); APPLE-1021, 4:37-65 (“copper studs”); APPLE-1018, Title, Abstract,

1:6-11, 2:8-40, 3:1-3 (“copper studs”); APPLE-1030 (electroless copper plating in bump metallization); APPLE-1031 (copper plating bump)); *Intel Corporation v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. March 13, 2023).

Notably, claim 12 recites “electrochemically deposited” copper and “chemically deposited” copper, which are product-by-process elements that have no patentable weight for purposes of determining unpatentability. *Supra*, Fn. 1. Asahi describes copper in the contact openings, as claimed. That is enough.

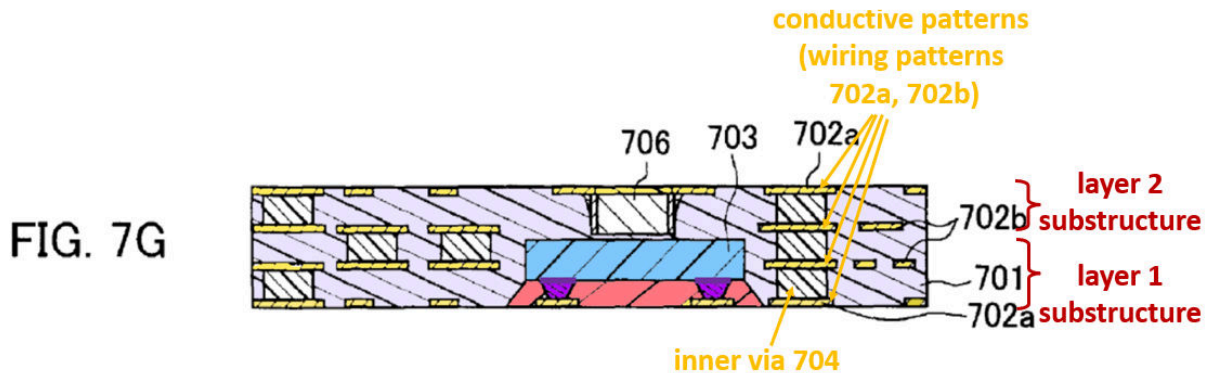
To be clear, even if the process recitations were considered limiting, Asahi renders Element [12d] obvious. APPLE-1003, ¶¶131-132. For example, a POSITA would have recognized, and found obvious, from Asahi’s description, that the copper contains at least one of electrochemically deposited copper and chemically deposited copper. APPLE-1003, ¶132. Asahi expressly describes plating surfaces of the wiring patterns so that “their corrosion resistance and electric conductivities can be improved.” APPLE-1006, 7:50-52; APPLE-1003, ¶132. Based on Asahi’s description, a POSITA would have been motivated to utilize plating techniques for forming bumps in the contact openings to achieve similar benefits of improved corrosion resistance and electric conductivities, with additional advantage of improved solderability for forming bumps 705. APPLE-1006, 16:39-66 (“stud bumps, and soldering”); APPLE-1003, ¶132. Moreover, given Asahi’s express disclosure of using copper (e.g., to avail the system of

copper's high conductivity), a POSITA would have readily implemented the copper bumps in the contact openings using chemical and/or electrochemical plating techniques that were well-known in the field before the Critical Date for forming chip or substrate bumps, including the use of multiple plating layers on top of each other, for the benefits described above. APPLE-1006, 8:19-35; APPLE-1003, ¶¶132-133 (citing APPLE-1020, 10:15-21 ("copper bumps ... formed by electroplating"); APPLE-1021, 4:37-65 ("copper studs" formed by electroplated copper); APPLE-1018, Title, Abstract, 1:6-11, 2:8-40, 3:1-3 ("copper studs ... formed by electroplating copper" over a "flash coat" of copper); APPLE-1030 (electroless copper plating in bump metallization); APPLE-1031 (copper plating bump)).

[13]

The *two circuit board substructures* of layer 1 substructure and layer 2 substructure *on top of each other are electrically connected to each other to form a multi-layered functioning totality* of Asahi's "component built-in module," as shown in Asahi's FIG. 7G. APPLE-1003, ¶134. For example, the substructures are electrically connected by inner via (e.g., via 708 filled with conductive paste 704) that connects wiring patterns 702a/702b of the respective substructures. APPLE-1006, 15:51-17:44, FIG. 7; *see also id.*, Abstract, 1:32-39, 2:27-3:3 ("...any one of the first wiring patterns in the plurality of layers and the second

wiring pattern[s] are connected electrically through an inner via”); 3:53-56, 4:19-5:62, FIGS, 1-10; cl. 1; APPLE-1003, ¶134.



APPLE-1003, ¶134 (APPLE-1006, FIG. 7G (Annotated))

[14]⁴

The duplication of the microcircuit has no patentable significance and would have been obvious to a POSITA in view of Asahi’s description. APPLE-1003, ¶136; *In re Harza*, 274F.2d 669, 671 (C.C.P.A. 1960). Claim 14 is unpatentable in view of Asahi for this independent reason.

Additionally, Asahi expressly describes “high-density component-mounting” that involves mounting a plurality of “semiconductors and circuit

⁴ Claim 14 is ambiguous as to whether the at least two microcircuits both require all elements recited in [12c], rendering claim 14 indefinite. Yet, unpatentability can be determined here, because the prior art expressly describes such features. APPLE-1003, ¶¶135-136.

components” to the wiring patterns 702a and 702b (e.g., within single layer 1 substructure). APPLE-1006, 17:41-44; *see also* 12:61-13:35 (“high density.”); *supra*, Analysis of [12c] (“microcircuit”); APPLE-1003, ¶137. A POSITA would have recognized and found obvious, from Asahi’s description, that each of the microcircuits (e.g., semiconductors) be mounted according to the arrangement and configuration consistent with Asahi’s description (e.g., of semiconductor 703) (*supra*, Analysis of [12c]-[12d]) and located within the first substructure layer (e.g., mounted to wiring patterns 702a), furthering Asahi’s high density mounting objectives. APPLE-1003, ¶¶137-139.

[15]

As discussed in §§VI.A.2, Analyses of Claims [13] and [14], Asahi’s layer 1 and layer 2 ***circuit board substructures each comprise*** a plurality of semiconductors and circuit components. APPLE-1006, 13:33-35, 14:5-10, 19:22-26, FIGS. 4, 10. A POSITA would have found obvious, from Asahi’s description, that such semiconductors and circuit components in “high density” circuitry devices such as “large scale integrated circuits (LSIs)” described by Asahi include ***at least one memory circuit***. APPLE-1003, ¶140 (citing APPLE-1011, [0038], APPLE-1008, [0040], [0055]). Indeed, such circuits were advantageously implemented to provide memory, and memory circuits were a common type of

integrated circuit used to store data in semiconductor devices used in computers, smartphones, embedded systems, and other electronic devices. *Id.*

[16]

Asahi expressly describes constructing a multi-layered circuit board module according to the techniques illustrated and described with reference to FIGS. 7A-7G to achieve a configuration having at least three circuit board substructures on top of each other (e.g., as shown in FIG. 4). §§VI.A.2, Analyses of Claims [12]-[14]; APPLE-1003, ¶141-142. Indeed, FIG. 4 illustrates an example three-layer structure with layers 1, 2 and 3 laminated (through wiring patterns 402a, 402b and inner vias 404). APPLE-1006, 17:41-44 (“other semiconductors and circuit components are mounted on the wiring patterns 702a on the surfaces, whereby a component built-in module shown in FIG. 4 is obtained.”); FIGS. 4, 7, 10 and related descriptions; APPLE-1003, ¶142.

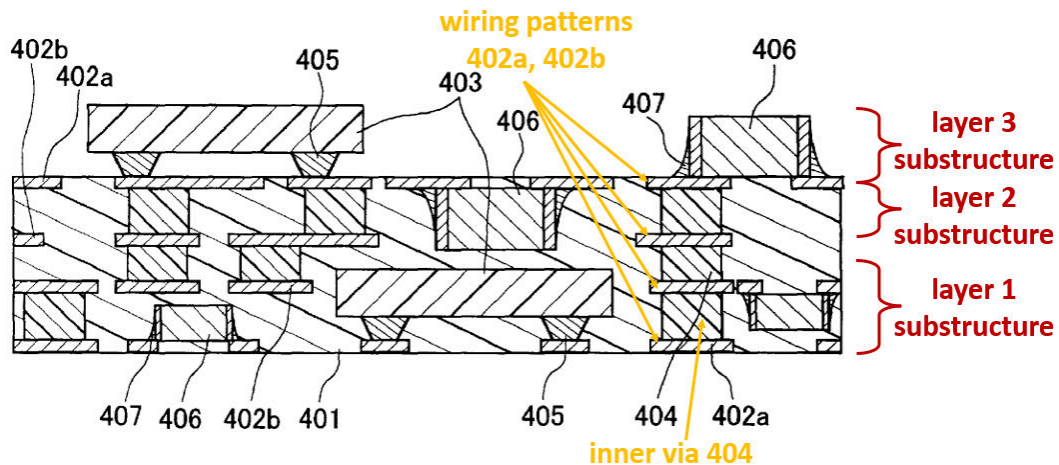


FIG. 4

APPLE-1003, ¶142 (APPLE-1006, FIG. 4 (Annotated))

A POSITA would have implemented the circuit board structure (e.g., including the configuration discussed above at [12pre]), to have a third substructure on top, in accordance with Asahi's teachings. APPLE-1003, ¶143; APPLE-1006, FIG. 4.

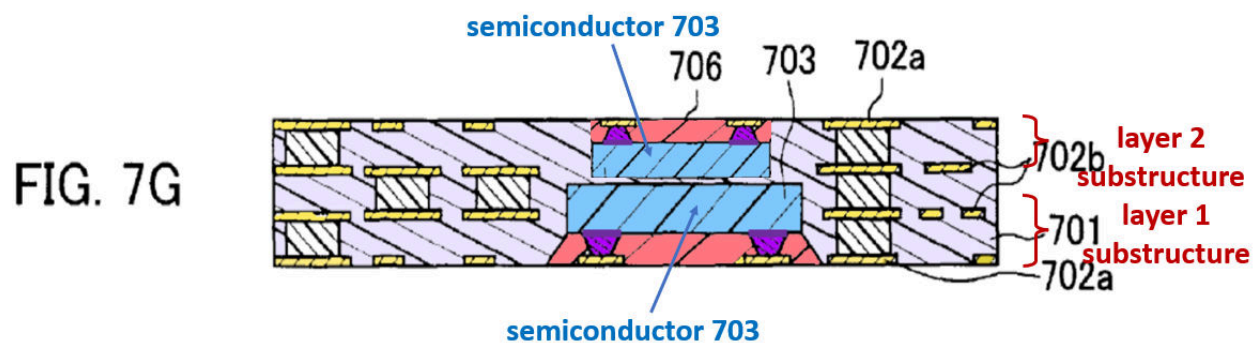
Even if Asahi did not expressly disclose the conventional feature recited by [16] (which it does), a POSITA would have been motivated, based on Asahi's description, to construct the module (e.g., including the configuration discussed above at [12pre]) to have at least three circuit board substructures on top of each other and electrically connected to each other to enhance the component density and functionality of the module, in accordance with Asahi's express objectives, and with a reasonable expectation of success based on Asahi's express techniques for implementing such multi-layer structures. APPLE-1003, ¶144.

[17pre]

To the extent the preamble is limiting, Asahi teaches [17pre]. *Supra*, §VI.A.2, Analysis of [12pre]; APPLE-1003, ¶145.

Asahi expressly describes mounting semiconductors and circuit components on both sides of wiring patterns 402a/702a, such that a component is mounted in each of two substructures. *Supra*, §VI.A.2, Analysis of Element [12a]; *see also* APPLE-1006, 19:1-37; APPLE-1003, ¶146. For example, Asahi describes a plurality of “semiconductors 403” and “circuit components 406” are “embedded in the electric insulation layer 401,” through mounting on wiring patterns 402a “on both sides.” APPLE-1006, 12:61-13:35, 14:5-10, 17:41-44, FIGS. 4, 10; APPLE-1003, ¶146. Accordingly, in one example, first and second substructure layers each include a semiconductor component mounted to conductive patterns. *Id.* For example, a first semiconductor is mounted to wiring pattern 402a/702a (e.g., at a bottom of the module) within the first substructure layer and a second semiconductor mounted to wiring pattern 402a/702a (e.g., at a top of the module) within the second substructure layer. APPLE-1003, ¶147. The semiconductors are each mounted according to Asahi’s descriptions, and thus utilize a hardened insulating polymer (e.g., “sealing resin 710”) in which the semiconductor is embedded. *Supra*, Analysis of [12c]; APPLE-1003, ¶148. Based on Asahi’s description, a POSITA would have found it obvious to implement the module to

include one semiconductor 703 embedded in layer 1 substructure and another semiconductor 703 (e.g., at the location of component 706) embedded in layer 2 substructure, with the two substructures having similar configuration, to achieve a high-density configuration having the functionality provided by multiple semiconductor components. *Id.*



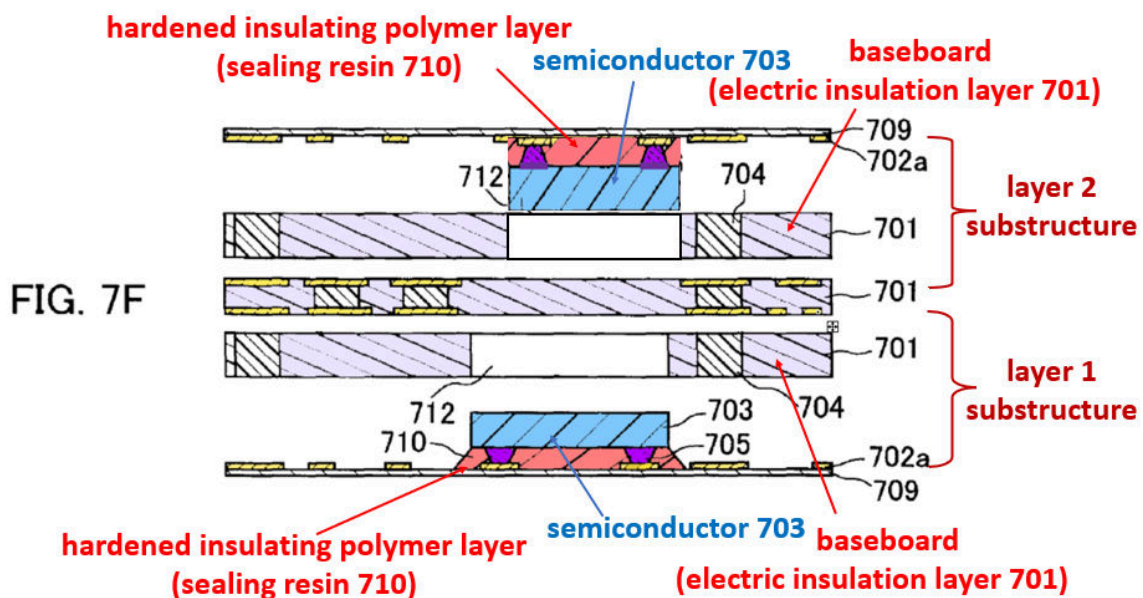
APPLE-1003, ¶147 (Modified FIG. 7G (Annotated))

[17a]

As discussed in §VI.A.2, Analysis of Element [12a], layer 1 circuit board substructure of Asahi's component built-in module comprises an insulating material layer composed of an electric insulation layer (*baseboard*) and a sealing resin layer (*hardened insulating polymer layer*). As discussed in §VI.A.2, Analysis of Element [17pre], Asahi's description provides for configurations in which a second circuit board substructure (layer 2 circuit board substructure shown below) has a similar configuration, also including an insulating material layer composed of an electric insulation layer (*baseboard*) and sealing resin layer

(*hardened insulating polymer layer*). APPLE-1003, ¶149.

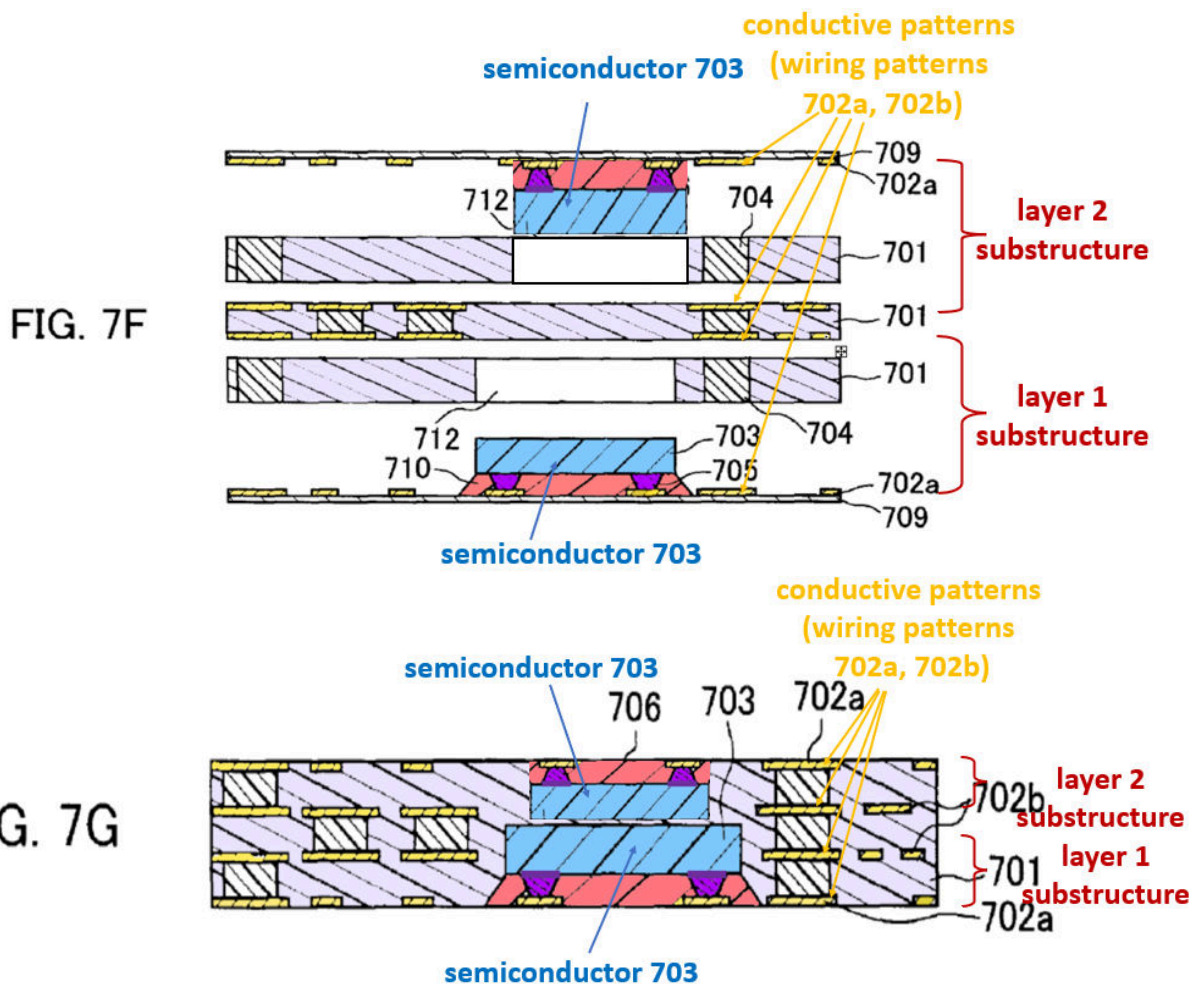
Consistent with Asahi's suggestions, the top insulation layer 701 has hole 712 to receive the semiconductor 703 of the layer 2 substructure, such that the top insulation layer 701 provides the baseboard of layer 2 substructure. Together with the sealing resin, this top insulation layer 701 provides the insulating material layer of the layer 2 substructure. APPLE-1003, ¶150. The bottom 701 layer includes hole 712 to receive the semiconductor 703 of the layer 1 substructure, and provides the claimed baseboard of the layer 1 substructure, and together with the sealing resin provide the insulating material layer of layer 1 substructure. APPLE-1003, ¶150; *supra*, § VI.A.2, Analysis of [12a].



APPLE-1003, ¶150 (Modified Based on APPLE-1006, FIG. 7F (Annotated))

[17b]

Asahi discloses Element [17b]. *Supra*, §VI.A.2, Analyses of Element [12b] and Elements [17pre]-[17a]; APPLE-1003, ¶151. Layer 1 and layer 2 substructures each comprises conductive wiring patterns 702b or 702a (*conductive patterns*) on the upper side of its insulating material layer, and conductive wiring patterns 702a or 702b (*conductive patterns*) on the lower side of its insulating material. APPLE-1003, ¶151.



APPLE-1003, ¶151 (Modified APPLE-1006, FIGS. 7F-7G (Annotated))

[17c]

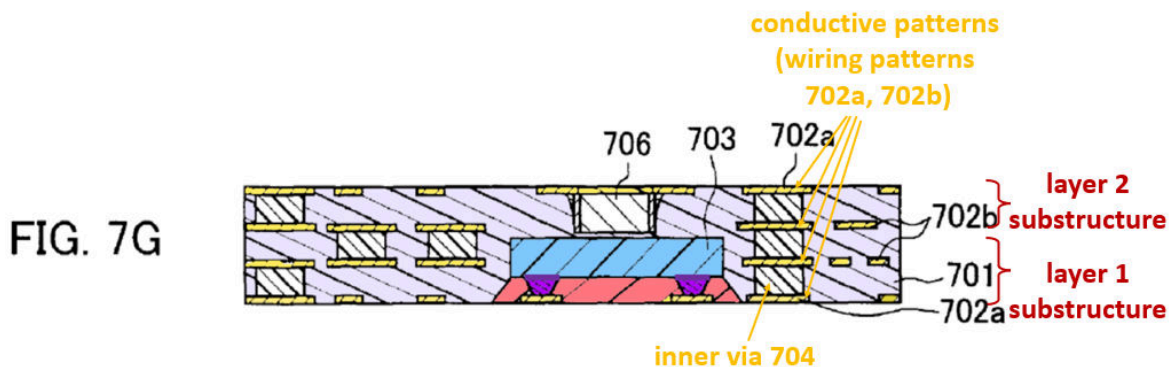
Supra, §§VI.A.2, Analyses of Element [12c] and Element [17pre]; APPLE-1003, ¶152.

[17d]

Supra, §§VI.A.2, Analyses of Element [12d] and Element [17pre]; APPLE-1003, ¶153.

[18]

The layer 1 substructure (*a first circuit board substructure*) and layer 2 substructure (*a second circuit board substructure*) are *electrically connected to each other to form a multi-layered functioning totality* through wiring patterns 702a, 702b and inner vias 704. APPLE-1003, ¶154; *supra*, §VI.A.2, Analysis of Claim [13];



APPLE-1003, ¶154 (APPLE-1006, FIG. 7G (Annotated))

[19pre]-[19d]

Supra, §§VI.A.2, Analyses of Elements [12pre]-[12d] and Claim [18];

APPLE-1003, ¶155.

[20pre]-[20d]

Supra, §§VI.A.2, Analyses of Elements [12pre]-[12d], [17pre]-[17d] and Claim [19]; APPLE-1003, ¶156.

[21]

Supra, §§VI.A.2, Analyses of Element [12a] (sealing resin contains “epoxy resin”) and Claim [20]; APPLE-1003, ¶157.

[22]

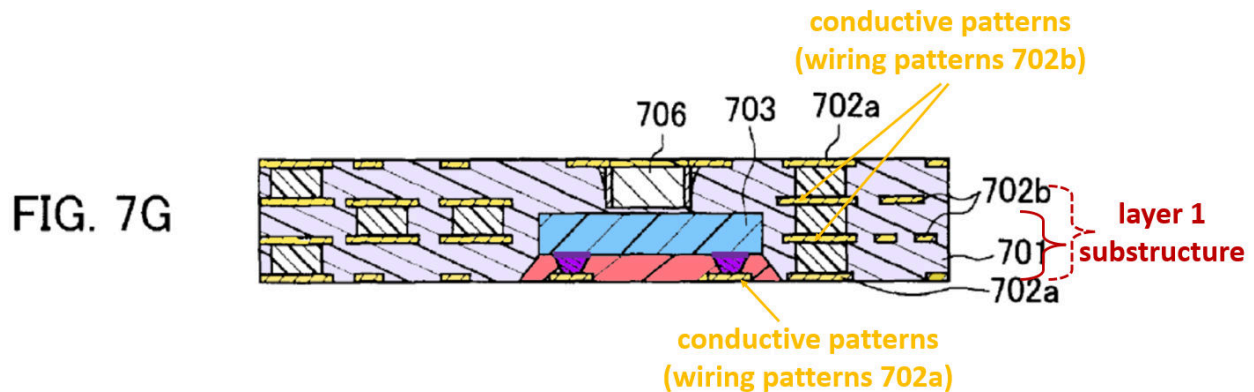
Supra, §§VI.A.2, Analyses of Element [12pre] (electric insulation layers being “a board form” containing “glass-epoxy,” “a reinforcing material such as a glass cloth or an unwoven fabric”) and Claim [20]; APPLE-1006, 3:60-65, 14:30, 16:1-2, cls. 11, 21; APPLE-1003, ¶158.

[23]

Supra, §§VI.A.2, Analyses of Claims [12], [18] and [19].

The annotated FIG. 7G below illustrates first and second alternative manners in which Asahi discloses Claim 23. According to the first manner (dashed bracket), the layer 1 substructure includes the wiring patterns 702b layer above the top surface of semiconductor 703, such that semiconductor 703 is **entirely** between at least this wiring patterns 702b layer and the wiring patterns 702a layer on the bottom surface of the layer 1 substructure. According to the second manner (solid

bracket), semiconductor 703 is at least partially between the lower patterns 702b layer and the wiring patterns 702a. Nothing in the plain language of the claim expressly recites that the component is “entirely” or “exclusively” between the conductive patterns. APPLE-1003, ¶¶159-161.



APPLE-1003, ¶161 (APPLE-1006, FIG. 7G (Annotated))

[24]

Like the [12d] analysis, Asahi provides two layers of copper (*a first layer of [] copper and a second layer of [] copper on the first layer of [] copper*), and thus discloses claim 24. *Supra*, §§VI.A.2, Analyses of [12pre]-[12d]; §III.A. (FN 1) (“product-by-process” elements); APPLE-1003, ¶162.

Even if the recited processes are limiting, Asahi provides claim 24, as discussed above in the Analysis of Element [12d] demonstrating *chemically deposited* and *electrochemically deposited copper* on top of each other *in the contact openings*, based on Asahi’s disclosure of plating and preference for copper as a high conductivity material for making electrical connections, as these are

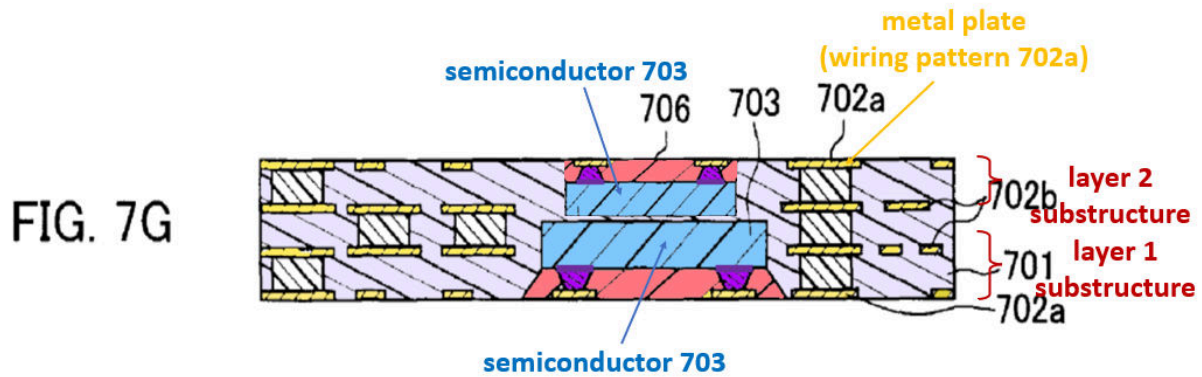
common plating techniques used for forming chip and substrate bumps in ordinary flip chip bonding, and utilize multiple plating layers.⁵ APPLE-1006, 7:50-52, 8:19-35; APPLE-1003, ¶163.

[25]

As discussed above in §VI.A.2, Analysis of Element [12b], Asahi discloses that wiring patterns, such as wiring patterns 402a/702a and 402b/702b, are made of “a metal foil” or “a lead frame obtained by processing a **metal plate**.” APPLE-1006, 7:23-26, 17:41-44; *see also, supra*, §§VI.A.2, Analyses of Claim [20], [19], [17], [12]; APPLE-1003, ¶164. Asahi explains that “the number of layers is not limited” for the inner wiring patterns 102b, and “a plurality of layers of inner wiring patterns 102b exist.” APPLE-1005, 9:4-10. Asahi thus discloses the *metal plate* that may be processed to form a wiring pattern. APPLE-1003, ¶164. For example, wiring patterns 702a of the layer 2 substructure represents the position of *a metal plate above* the embedded semiconductor of the layer 2 substructure.

⁵ Indeed, the patent examiner of the '909 Patent took Official Notice that “formation of plated Cu layers using both methods in formation of a seed layer and a bulk Cu layer was known prior to applicant’s invention.” APPLE-1002, 53-58.

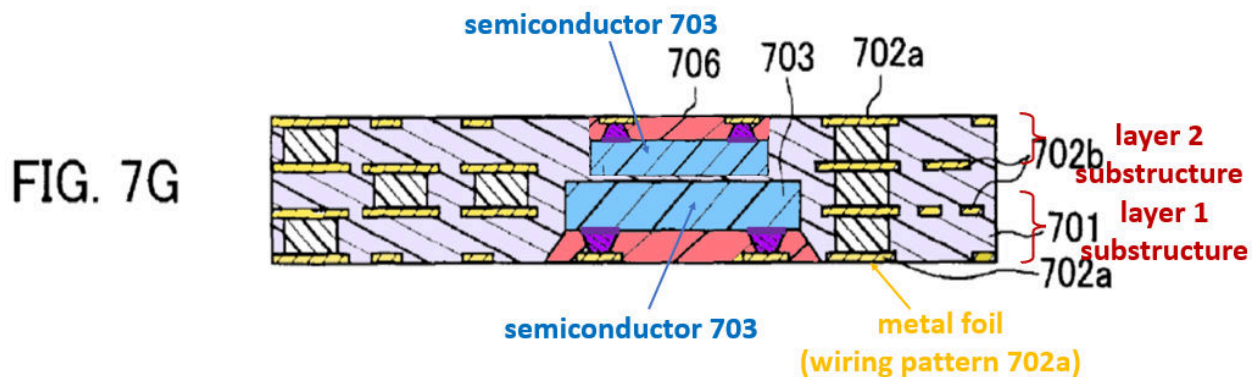
Supra, §§VI.A.2, Analyses of Claims [14]-[16] and Element [17pre]; APPLE-1003, ¶164.



APPLE-1003, ¶164 (Modified Based on APPLE-1006, FIG. 7G (Annotated)).

[26]

Wiring patterns 702a of the layer 1 substructure represents the position of a metal plate or *metal foil below* the embedded semiconductor 703 (*at least one of the microcircuits*) of layer 1 substructure. APPLE-1006, 3:39-41, 7:23-29, Cls. 5 & 18; APPLE-1003, ¶165; *see also supra*, §VI.A.2, Analyses of Claim [25].



APPLE-1003, ¶165 (Modified Based on APPLE-1006, FIG. 7G (Annotated))

[27pre]-[27d]

Supra, §§VI.A.2, Analyses of [17pre]-[17d]; APPLE-1003, ¶166.

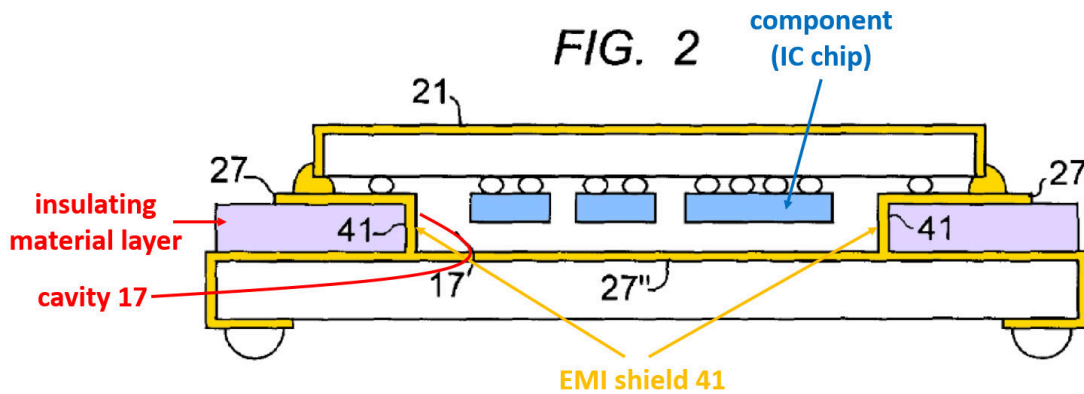
[27e]

Supra, §§VI.A.2, Analyses of Claim [25] (use of “metal foil” for wiring patterns, such as wiring patterns 702a) and Claim [26] (wiring patterns 702a of the layer 1 substructure below the embedded semiconductors 703 of layer 1 substructure); APPLE-1003, ¶167.

B. GROUND 1B – Asahi-Dudderar renders obvious Claims 1-33

1. Dudderar

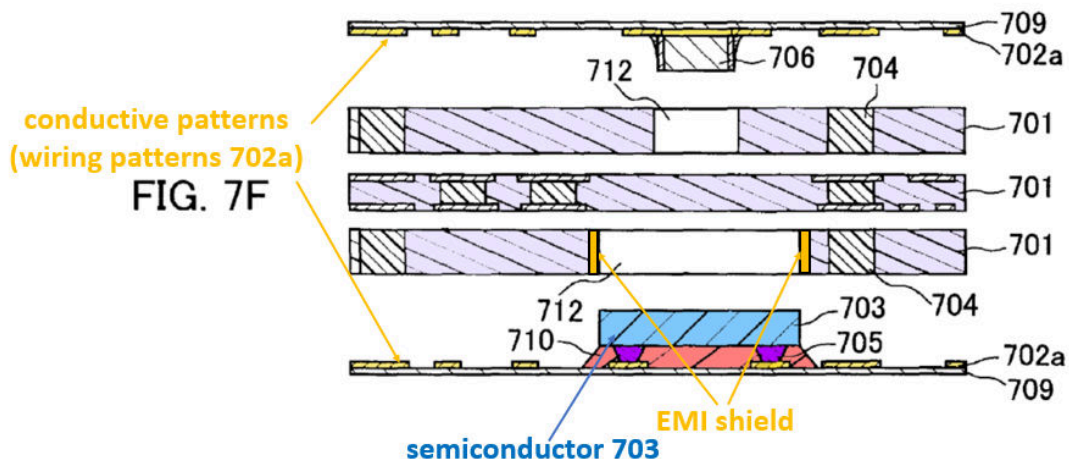
Dudderar describes embedding semiconductor components, such as integrated circuit chips, in a circuit board cavity and providing a grounded “EMI shield metallization” that surrounds the cavity and “extends along the inside wall of [the] cavity.” APPLE-1014, 1:10-63, 2:44-54, 2:63-3:4, 3:49-52, 4:45-52, 5:45-46, FIG. 2, Cl. 1; APPLE-1003, ¶¶81-84.



APPLE-1003, ¶84 (APPLE-1014, FIG.2 (Annotated))

2. Predictable Asahi-Dudderar Combination

A POSITA would have been motivated to enhance Asahi's circuit board through implementation of an EMI shield and copper metallization on the sidewalls of the cavity, in accordance with Dudderar's suggestions. APPLE-1003, ¶169. Doing so would have enhanced Asahi's device, and advanced Asahi's teachings of metal on the sides of a component, e.g., solder 707 on the sides of component 706. *E.g.*, APPLE-1006, 16:43-46, FIG. 7E; APPLE-1003, ¶¶169-170.



APPLE-1003, ¶169 (Composite Based on APPLE-1006, 7F (Annotated))

First, a POSITA would have been motivated to combine Asahi and Dudderar to predictably mitigate against “EMI problems” associated with integrated circuit packages, and to enhance protection of the component. APPLE-1014, 1:10-63 (“EMI is disruptive), 5:45-46; APPLE-1003, ¶171.

Second, a POSITA would have been prompted to combine Asahi and Dudderar, because doing so was the application of known techniques (forming an EMI shield that extends along the sidewalls of a cavity of circuit board for receiving IC chips) to a known device (Asahi’s device having a through hole 712 in a wiring board to receive semiconductor 703) ready for improvement to yield predictable results (benefits articulated above). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (“[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.”). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Asahi and Dudderar describe similar IC packages and apply metal on the sides of embedded components, and because the modifications would have been implemented largely by using conventional metallization for circuit boards extending it along the sidewalls of the cavity, for EMI shielding—a configuration Dudderar already demonstrated to be successful.

APPLE-1006, Title, Abstract, 3:44-46, 3:60-65, 6:33-46, 7:66-8:18, 15:62-67, 16:41-17:40, 17:55-18:13, FIG. 7; APPLE-1014, 2:43-54, FIG. 2; APPLE-1003, ¶¶172-174. Moreover, Asahi and Dudderar describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above. *Id.*

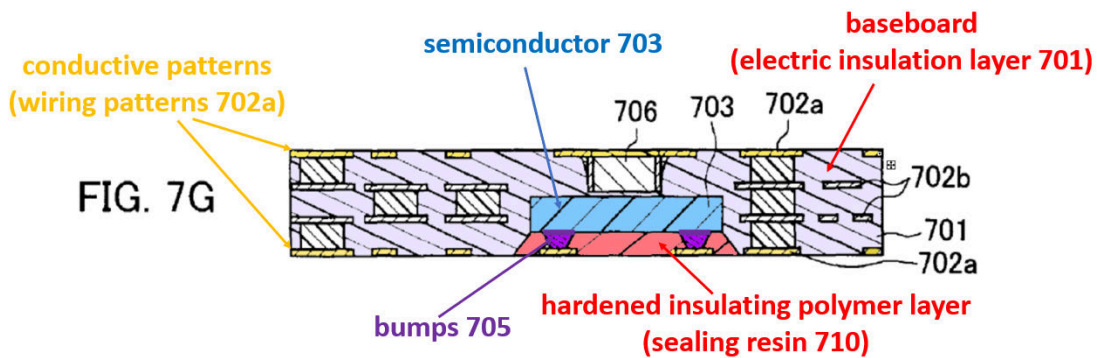
3. Application to Challenged Claims⁶

[1pre]-[1c], [1e]

The Asahi-Dudderar combination provides [1pre]-[1c] and [1e], as set forth above. *Supra*, Ground 1A Analysis of [12a]-[12c], [12d]; APPLE-1003, ¶176.

Asahi-Dudderar additionally provides claim 1 in a second manner. For example, the entire unified electric insulation layer 701 of the configuration in FIG. 7G (formed by laminating all three layers of 701 of FIG. 7F) provides a **baseboard** of [1a], and wiring patterns 702a on both surfaces of the entire module alternatively provide **conductive patterns on both sides of the insulating material layer** of [1b]. *Supra*, §VI.A.2; APPLE-1003, ¶177; *see also* APPLE-1006, FIGS. 3, 8 and related descriptions.

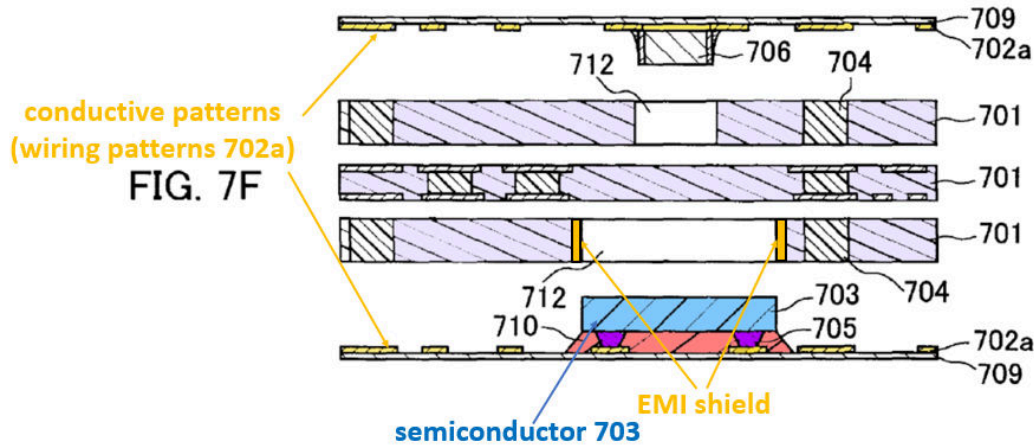
⁶Where Dudderar is not addressed in Ground 1B, the Ground 1A analysis applies fully here.



APPLE-1003, ¶177 (APPLE-1006, FIG. 7G (Annotated))

[1d]

The Asahi-Dudderar combination renders Element [1d] obvious. In the combined device (*supra*, §VI.B.2 (Asahi-Dudderar combination)), metallization (e.g., copper) is located along the sidewalls of hole 712 in the electric insulation layer 701 for EMI shielding (*conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit*), in accordance with Dudderar. APPLE-1003, ¶¶178-180; APPLE-1014, 3:24-27, 4:45-49; *see also id.*, 3:3-4; APPLE-1006, 5:47-49, 9:40-46, 10:18-25, 16:27-46, 17:25-34, 19:60-20:10.



APPLE-1003, ¶178 (Composite Based on APPLE-1006, FIG. 7F (Annotated))

[2]

Supra, §§VI.A.2, Analyses of Element [12a] (sealing resin contains “epoxy resin”) and Claim [21]; APPLE-1003, ¶181.

[3]⁷

Supra, §§VI.A.2, Analyses of Element [12pre] and Element [12a] (obvious for sealing resin to contain similar material, such as “glass-epoxy” or epoxy resins with glass fillers). Glass fibers was a common choice a POSITA would have found obvious to implement glass fillers in a resin, as it was a well-known economical solution in the field to provide effective structural properties and enhance module robustness. APPLE-1003, ¶182.

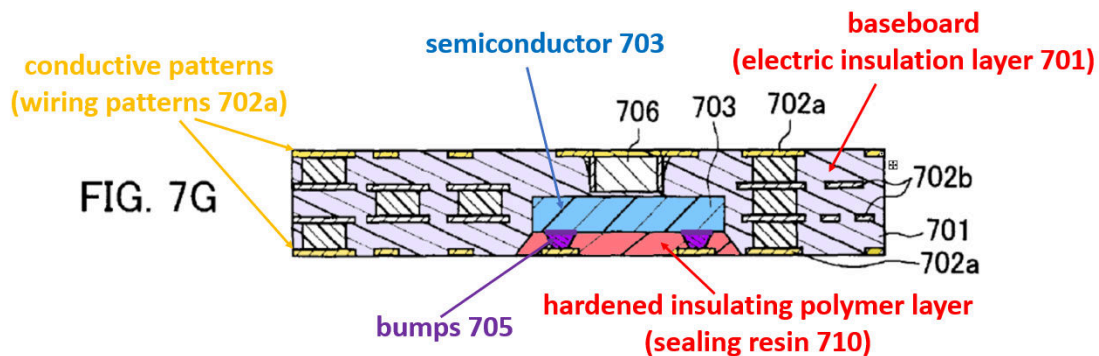
⁷ There is no support for the recited “the hardened insulating polymer layer contains epoxy and glass fibres” limitation in the ’909 patent specification.

[4]

Supra, §VI.A.2, Analyses of Claim [22]; APPLE-1003, ¶183.

[5]

Figure. 7G below, for example, shows semiconductor 703 (*microcircuit*) *located between* wiring patterns 702a (*conductive patterns*) *on both sides of the* unified *insulating material layer* composed of the unified electric insulation layer 701 (*baseboard*) and sealing resin 710 (*hardened insulating polymer layer*). APPLE-1003, ¶184; *see also* APPLE-1006, 11:26-12:51, 17:45-18:13; *supra*, §VI.A.2, Analyses of [12pre]-[12c], §VI.B.3, Analyses of [1pre]-[1c].



APPLE-1003, ¶184 (APPLE-1006, FIG. 7G (Annotated))

[6]

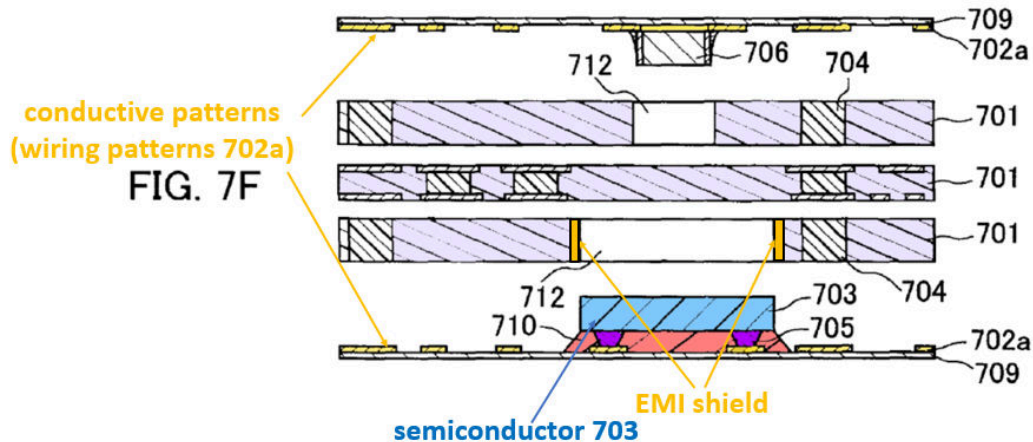
Dudderar incorporates by reference Degani, which describes filler material in the cavity in the printed wiring board, such as using “a compliant encapsulating material encompassing the [embedded] chips,” to “protect[] the chips, interconnections and adjacent surfaces of the substrate.” APPLE-1019, 3:4-56,

5:24-34 (“the cavity ... is filled with an encapsulating material... such as silicone gel”), 5:63-65 (“the cavity is filled by ... epoxy resin”), Cls. 2, 6; APPLE-1014, 2:15-18; *see also* APPLE-1006, 2:15-10; 16:59-62; APPLE-1003, ¶185.

A POSITA would have recognized and found obvious that in the manufacturing process of Asahi, carrier 709 temporarily secures semiconductor 703 in the hole 712 during lamination, and once carrier 709 is removed, there is a thin wiring layer 702a with sealing resin at the connection portion. APPLE-1006, 17:14-40, APPLE-1003, ¶186. Thus, consistent with Dudderar’s suggestions, to better *secure* each semiconductor 703 (*microcircuit*) in a predetermined position (*in place in the hole*), also g, a POSITA would have found obvious to fill hole 712 with *a filler material*. APPLE-1003, ¶186. Moreover, a POSITA would have predictably done so using a similar conformable encapsulating material of Dudderar before lamination, or by flowing the uncured resin of electric insulation layer 701 (e.g., the middle 701 layer of FIG. 7F, labeled as 701b for ease of reference) with decreased viscosity into the gap of hole 712 around semiconductor 703 during lamination “[b]y pressing and heating,” for example. APPLE-1006, APPLE-1006, 5:47-49, 9:40-46, 10:18-25, 16:27-35, 17:14-40, 19:60-20:10; APPLE-1003, ¶187. Indeed, the volume of electric insulation layer 701b would flow in these holes to fill in any gap during lamination, where the uncured 701 layers are pressed and fused together with heating, and semiconductor 703 and

circuit component 706 are pressed into the 701b layer from opposite directions.

APPLE-1006, 17:18-24; APPLE-1003, ¶¶188-189.



APPLE-1003, ¶189 (Composite Based on APPLE-1006, FIG. 7F (Annotated))

[7]

Supra, §VI.A.2, Analysis of [12pre] (insulation layer 701 contains epoxy resin), and §VI.B.3, Analysis of Claim 6; APPLE-1003, ¶190.

[8pre]

Supra, §VI.A.2, Analysis of Element [12pre] and § VI.B.3, Analysis of [1pre] and [1a]-[1e]; APPLE-1003, ¶191.

[8a]

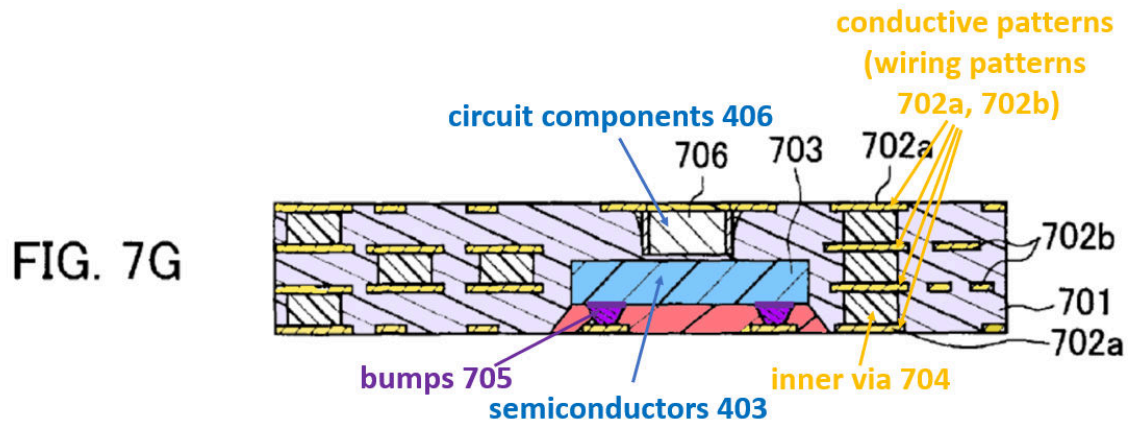
Supra, §§VI.A.2, Analyses of Claims [14]-[15]; APPLE-1003, ¶192.

[8b]

As discussed in §§VI.A.2, Analyses of Claims [13], [16], [18], the wiring patterns (e.g., 702a and 702b) of various layers of Asahi's component built-in

module are electrically connected through inner vias (e.g., inner vias 704).

APPLE-1003, ¶193.



APPLE-1003, ¶193 (APPLE-1006, FIG. 7G (Annotated))

Each semiconductor 703 is connected to wiring patterns 702a through bumps 705. *Supra*, §VI.A.2, Analysis of Element [12d] and § VI.B.3, Analysis of Element [1e]. Thus, the plurality of semiconductors 703 (*microcircuits*) (note that circuit components 706 are also connected to wiring patterns through a solder 707 or a conductive adhesive) ***are connected to each other, by means of*** bumps 705 (***conductors in the contact opening***) and wiring patterns 702a and 702b (***at least one of the conductive patterns***). *E.g.*, APPLE-1006, 13:7-9, 16:43-46, 16:39-52, 17:59-61; APPLE-1003, ¶194.

[9]

Supra, §VI.A.2, Analysis of Claim [24]; APPLE-1003, ¶195.

[10]

Supra, §VI.A.2, Analysis of Claim [13] (Asahi’s *electrically conducting* inner via 704 maps to the *feed-through between* the wiring patters 702a on both surfaces of the module (*the conductive patterns on the both sides of the insulating material layer*)); APPLE-1003, ¶196.

[11pre]-[11b]

Supra, §§VI.B.3, Analyses of [8pre]-[8b]; APPLE-1003, ¶197.

[12]-[27]

Asahi-Dudderar renders obvious these claims for at least the same reasons set forth above with respect to Asahi. *Supra*, §§VI.A.2, Analyses of Claims [12]-[27]; APPLE-1003, ¶198.

[28]

As discussed above in §VI.B.3, Analysis of [1d], the Asahi-Dudderar device has metallization along the sidewalls of hole 712 in the electric insulation layer 701 for EMI shielding, in accordance with the EMI shield metallization 41 formed using standard PCB technique. A POSITA would have understood from Asahi that forming metal layers on a standard PCB includes using a *metal foil*. E.g., APPLE-1006, 3:39-42 (“metal foil”), 10:1-4 (“metal foils”); APPLE-1003, ¶199. Indeed, the construction described by Asahi and Dudderar is like the ’909 patent’s description of metal foil such as “RCC (Resin Coated Copper) foil” of a similar thickness for the copper layer (“e.g., c. 5 μm ”) as part of a standard PCB. APPLE-

1001, 5:54-59; APPLE-1003, ¶200. Thus, for implementing the EMI shield metallization on the sidewalls of Asahi-Dudderar's cavity, a POSITA would have found it obvious to use "standard PCB" processing, "as thick as desired... e.g. less than 4 μm ," in accordance with Dudderar's teachings, thereby providing a *metal foil*, as claimed. APPLE-1014, 3:3-4, 3:24-27, 4:45-49; APPLE-1003, ¶200.

[29]

As discussed in §§VI.B.3, Analyses of Element [1d] and Claim [28], the Asahi-Dudderar device includes metal foil covering the four sidewalls of hole 712 to provide EMI shielding. As semiconductor 703 is surrounded by the unbroken four sidewalls of hole 712 in a lateral direction of the circuit board, a POSITA would have understood and found obvious that *the metal foil* cover the entirety of all four sidewalls of hole 712, and to thus implement as *an unbroken metal foil* that *surrounds* semiconductor 703 (*the microcircuit*) *in a lateral direction of the circuit board* to effectuate the shielding objective of Dudderar. APPLE-1003, ¶201.

[30]-[33]

Supra, §§ VI.A.2, Analysis of Claim [25] and [26], VI.B.3, Analysis of [1pre]-[1e]; APPLE-1003, ¶202.

C. GROUND 1C – Asahi-Joshi renders obvious Claims 12-27

Asahi renders obvious claims 12-27 for the reasons described above in

Ground 1A. But even if Asahi did not, the predictable Asahi-Joshi combination would do so based on Joshi's description of conventional plating techniques.⁸

1. Joshi

Joshi describes methods for connecting integrated circuit chips to a substrate or carrier, through copper studs formed on the chip or substrate using various plating methods with limited amount of solder, to achieve several express benefits (noted below). APPLE-1018, Title, Abstract, 1:6-11, 2:8-40, 3:1-3 ("copper studs ... are formed by electroplating copper"), 3:21-26, 3:52-68, 4:14-34, Cl. 6 ("electroplating copper in the stud areas"); APPLE-1003, ¶¶85-87.

2. Predictable Combination of Asahi and Joshi

Asahi's component built-in module utilizes bumps 705 on the semiconductor 703, to electrically connect semiconductor 703 with the wiring board substrate (e.g., through the bumps' connection to the wiring patterns 702a on the wiring board). *Supra*, §§VI.A.2, Analyses of Elements [12c]-[12d], FIG. 7; APPLE-1006, 16:39-66; *see also*, 8:9-10, 10:33-45, 11:47-54, 13:27-29, 14:25-27, 15:9-12, 17:59-61; APPLE-1003, ¶204. Joshi provides a straightforward suggestion for forming bumps using multiple plating techniques. APPLE-1018, 2:8-40, 3:1-3,

⁸ Where Joshi is not addressed in Ground 1C, the Ground 1A analysis applies fully here in Ground 1C.

3:21-26, 3:52-68, 4:14-34, Cl. 6.

In the resulting combination, bumps (e.g., bumps 705) are formed by first providing “a flash coat of conductive metal (e.g., copper)” on the first surface of the semiconductor (e.g., semiconductor 703), then another layer of “electroplat[ed] copper.” APPLE-1006, 16:39-66; APPLE-1018, 3:1-3, 3:52-68, Cl. 6; APPLE-1003, ¶204-205.

Multiple reasons would have prompted a POSITA to implement bumps in the combined system in accordance with Joshi’s suggestions for multiple layers of flash coat and electroplated copper. Joshi expressly articulates multiple benefits of such techniques, including to achieve “improve[d] thermal characteristics of the interconnections,” “improved chip/carrier attachment,” “improved input/output characteristics from the chip to the carrier,” “reduction in the thermal resistance between the chip and the substrate,” and improved “reliability of these interconnections,” for example, each of which a POSITA would have been motivated to avail the Asahi module of. APPLE-1018, Title, Abstract, 1:6-11, 2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34, Cl. 6; APPLE-1003, ¶¶206-207. Indeed, doing so would have been the application of known techniques (Joshi’s suggestions of multi-layer conductors using multiple plating techniques) to a known system (Asahi’s module that utilizes copper conductors) ready for improvement to yield predictable results. *KSR*, 550 U.S. at 417; APPLE-1006,

20:52-59. Moreover, a POSITA would have had a reasonable expectation of success based on the similarity of the systems and construction techniques described by Asahi and Joshi, and Joshi describes known plating techniques suitable for such applications. APPLE-1003, ¶¶208-209. Asahi and Joshi are analogous subject matter in the same field of endeavor and reasonably pertinent to common problems associated with semiconductor packaging and manufacturing, including for the reasons note above. *Id.*

3. Application to Challenged Claims

[12d]/[17d]/[19d]/[20d]/[27d]

Elements [12d], [17d], [19d], [20d], and [27d] recite limitations related to copper that contains at least one of electrochemically deposited and chemically deposited copper. Even if Asahi alone does not provide these limitations (which it does, *supra* § VI.A.2), the Asahi-Joshi combination renders them obvious. APPLE-1003, ¶¶210-212.

As discussed in §§VI.C.1 and VI.C.2, the Asahi-Joshi device includes bumps formed by first providing “a flash coat of conductive metal (e.g., copper)” on the first surface of semiconductor, then forming another metal layer over the flash coat from “electroplating copper” (*electrochemically deposited copper*), in accordance with Joshi’s suggestions. APPLE-1018, Title, Abstract, 1:6-11, 2:8-40, 3:1-3, 3:21-26, 3:52-68, 4:14-34, Cl. 6. To be clear, a POSITA would have

recognized that “electroplating copper” is electrochemical deposition of copper.

APPLE-1003, ¶213.

Accordingly, Asahi-Joshi provides Elements [12d], [17d], [19d], [20d], and [27d] for this independent reason. APPLE-1003, ¶214.

The combination additionally renders these elements obvious in a second manner. A POSITA would have recognized, and found obvious, that the “flash coat” described by Joshi be performed according to one of two manners—physically or chemically (e.g., Physical Vapor Deposition (PVD), or Chemical Vapor or Bath Deposition (CVD or CBD))—selection of which amounts to an obvious design choice. *KSR*, 550 U.S. at 421 (“a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions”). The two options of either physical or chemical flash coating were “identified, predictable solutions” by the Critical Date, and readily selected to effectuate the layers of copper in accordance with Joshi’s suggestions. APPLE-1003, ¶215 (citing APPLE-1034, [0008]-[0009]). Therefore, Asahi-Joshi also provides ***chemically deposited copper*** that provides a first layer of the copper in the contact openings. *Id.*

[24]

The Asahi-Joshi combination renders obvious Claim [24], even if the recited process of the product-by-process element is limiting. *Supra*, §VI.C.3, Ground 1C, Analysis of Element [12d]; APPLE-1003, ¶216.

D. GROUND 1D – Asahi-Dudderar-Joshi renders obvious Claims 1-33

1. Predictable Asahi-Dudderar-Joshi Combination

Even if the Asahi-Dudderar combination did not provide all elements of claims 1-33 (which it does), the predictable combination of Asahi-Dudderar-Joshi would do so. A POSITA would have been motivated by Joshi to further modify the Asahi-Dudderar combination, with a reasonable expectation of success, for the same reasons articulated above in Ground 1C, achieving each element of Claims 1-33. APPLE-1003, ¶¶217-220.

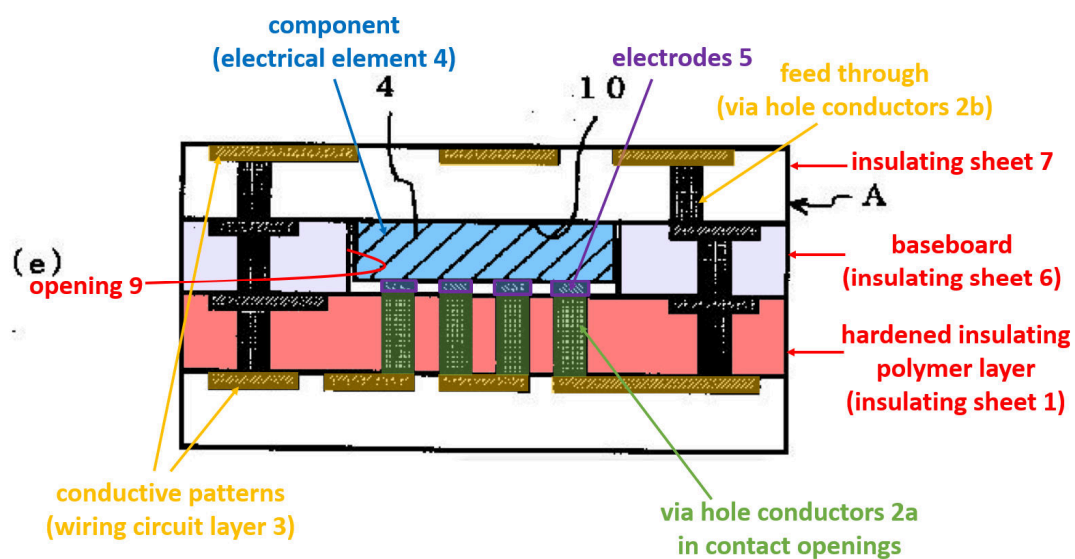
E. GROUND 2A – Hayashi renders obvious Claims 12-27

1. Hayashi

Hayashi describes “a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate, and to a manufacturing method for such a wiring substrate,” where examples of the electrical element include “a semiconductor element.” APPLE-1011, [0001]-[0003], *see also*, Title, Cls. 1, 2, [0007], [0027], [0038], [0041]; APPLE-1003, ¶¶76-77. Figure 1(e) below shows electrical element 4 stowed in an opening 9

formed in an insulating sheet 6 which is laminated directly above insulating sheet 1 and below insulating sheet 7, “so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7.”

APPLE-1011, [0028], [0039]-[0040]; APPLE-1003, ¶77. A “wiring circuit layer 3” as a “circuit pattern” is provided on both sides of and within the insulating layer composed of insulating sheets 1, 6, 7, these wiring circuit layers are interconnected through via hole conductors 2b in all the insulating sheets. APPLE-1011, Cl. 1, [0009], [0012], [0021], [0024], [0025], [0028], [0036]-[0038], [0041], FIGS. 1(b)-(e); APPLE-1003, ¶78. Electrical element 4 (through its electrodes 5) is connected to wiring circuit layer 3 through via holes conductors 2a in insulating sheet 1. APPLE-1011, [0008]- [0012], [0014], [0018], [0020], [0024], [0026], [0030], [0034], [0035], [0038], [0041], [0042], Cl. 1, 2; APPLE-1003, ¶78.



APPLE-1003, ¶77 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi's insulating sheet 1 contains a thermoset resin with via holes penetrating in a thickness direction formed in the insulating sheet 1. APPLE-1011, FIG. 1(a), [0012], [0015] (list of different polymers); APPLE-1003, ¶79. Insulating sheet 1, along with the other insulating sheets, is hardened through thermal curing. APPLE-1011, [0010], [0012], [0013], [0019], [0029], [0032], [0035], [0040], Cls. 1, 2; APPLE-1003, ¶79.

Hayashi describes that multiple layers of similar substructure of FIG. 1(e) are laminated on top of each other to increase mounting density, these substructures are electrically connected through via hole conductors 2b and the wiring circuit layers 3 provided in each insulating sheet. APPLE-1011, [0032]; *see also* [0004], [0007], [0009], [0012], [0021], [0024], [0025], [0028], [0034], [0036]-[0038], [0041], [0042], FIGS. 1(b)-(e); APPLE-1003, ¶80.

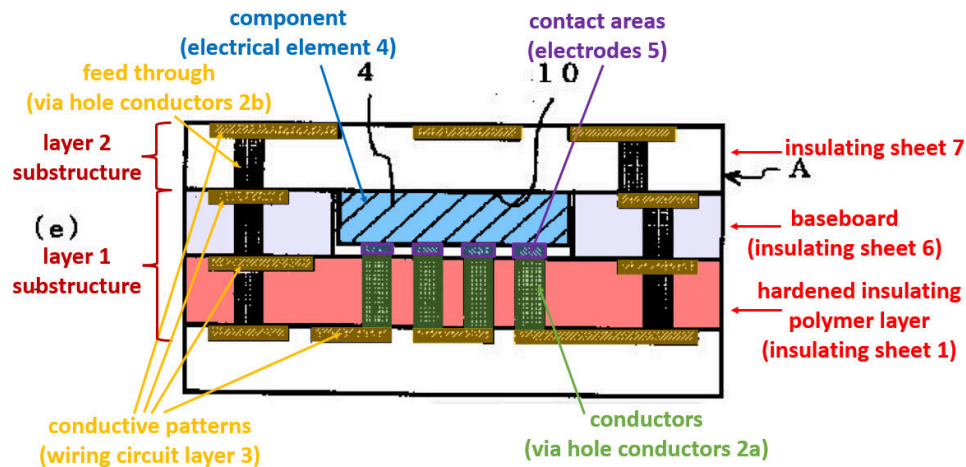
2. Application to Challenged Claims

[12pre]

To the extent the preamble is limiting, Hayashi discloses [12pre] in at least two manners.

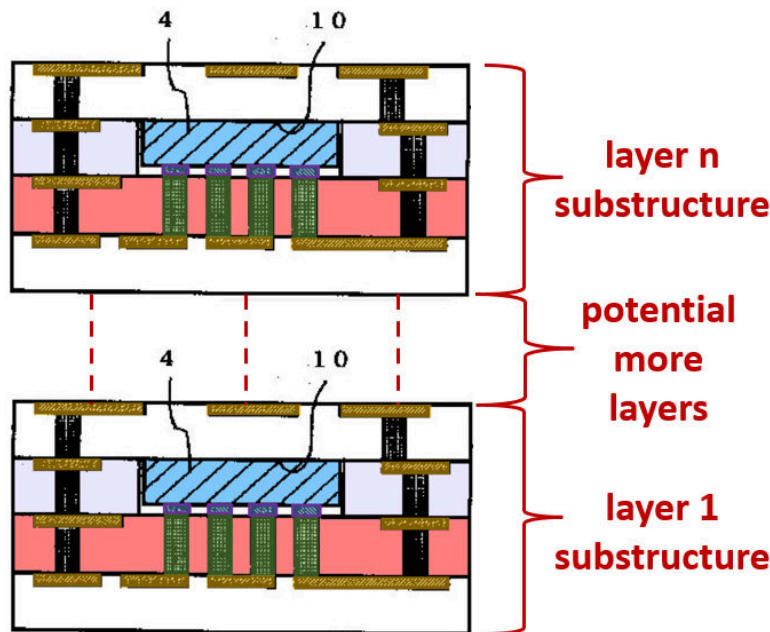
First, as illustrated in FIG. 1(e), Hayashi describes a first circuit board substructure provided by “insulating sheet 6,” “insulating sheet 1,” bottom “wiring circuit layer 3,” “via hole conductors 2a,” and “via-hole conductors 2b” through these layers, and a second circuit board substructure provided by “insulating sheet

7,” “via-hole conductors 2b” through “insulating sheet 7,” and “top wiring circuit layer 3.” APPLE-1011, FIGS. 1(a)-(e); cl. 1, [0001], [0009], [0015], [0016], [0017]; APPLE-1003, ¶222. The second circuit board substructure is on top of the first circuit board substructure. *Id.*, FIG. 1(e).



APPLE-1003, ¶222 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi also discloses [12pre] in a second manner, through its description of multiple insulating layers and multiple electrical components in different layers. APPLE-1003, ¶223. For example, Hayashi describes “a **plurality of electrical elements** can be provided by forming a plurality of void portions in the same or **different layers** in a multilayer wiring substrate to stow and mount the electrical elements.” APPLE-1011, [0032], [0034]; APPLE-1003, ¶¶223-224. In this express implementation, the multi-layered wiring board has similar **substructures on top each other**, each substructure having electrical elements such as semiconductors or memory chips embedded in insulating sheets. *Supra*, §VI.E.1.



APPLE-1003, ¶224 (Composite Based on APPLE-1011, FIG. 1(e) (Annotated)).

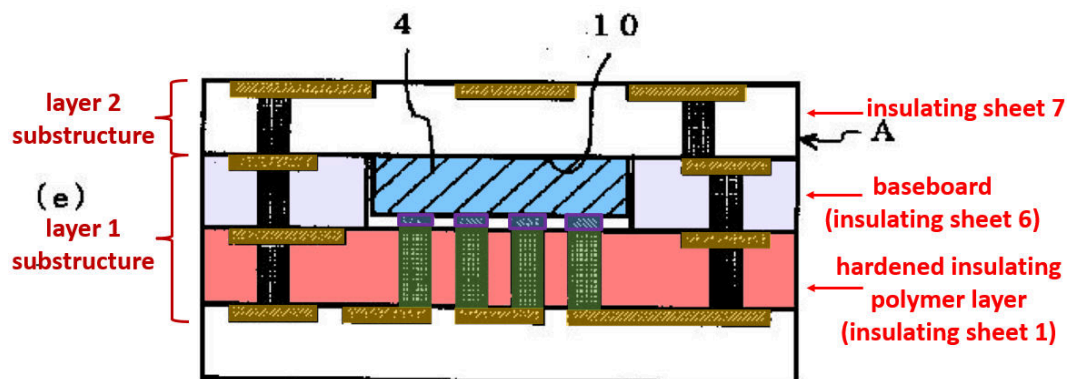
Moreover, a POSITA would have found the use of multiple such layers obvious, in order to effectuate Hayashi's stated objectives, with a reasonable expectation of success in electrically connecting such layers using Hayashi's express techniques. APPLE-1003, ¶225.

Each substructure of Hayashi's multi-layered wiring board, such as the layer 1 and layer n ($n \geq 2$) substructures (*at least two circuit board substructures on top of each other*) indicated in this composite figure, has the same or similar structure as shown in FIG. 1(e). Thus, subsequent discussions for the elements of Claim 12, according to Hayashi's second manner of disclosing the claim elements, focus on the structure shown in FIG. 1(e) as the recited *at least one of said circuit board substructures*. APPLE-1003, ¶226.

To be clear, Hayashi describes its wiring board includes “an insulating substrate obtained by laminating a plurality of insulating layers containing at least a thermosetting resin,” such as “epoxy resin,” constituting a combined circuit board with each insulating layer constituting a circuit board. APPLE-1011, Cl. 1, [0001], [0009], [0015] (“epoxy resin”), [0016], [0017]; The '909 patent recites the same type of material for its circuit board, such as “a glass-fibre reinforced epoxy board.” APPLE-1001, 3:46-55, Cl. 9; APPLE-1003, ¶¶227-228.

[12a]

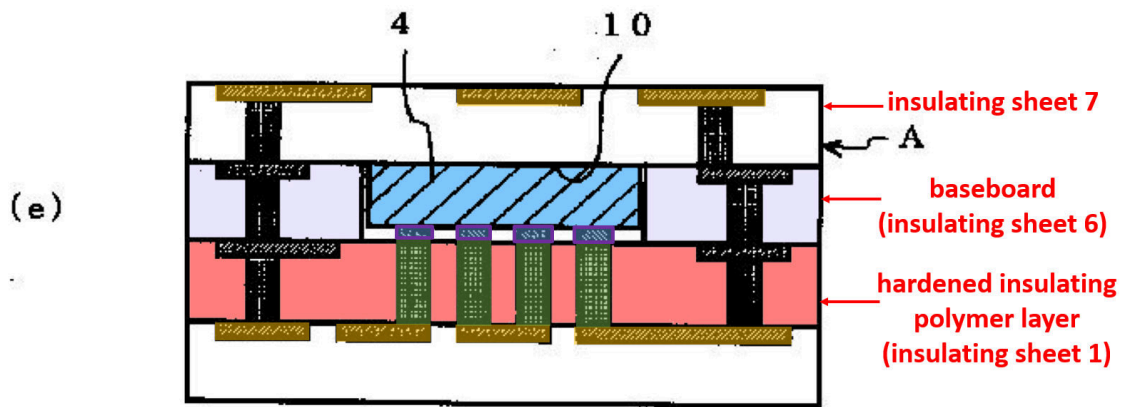
Hayashi describes an *insulating material layer* including *a baseboard* (e.g., “insulating sheet 6”) and *a hardened insulating polymer layer* (e.g., “insulating sheet 1”). APPLE-1011, FIG. 1(a)-1(e); APPLE-1003, ¶¶229-233; *supra*, Analysis of [12pre]. Thus, Hayashi provides [12a] in the first manner discussed above, as indicated in the below annotated FIG. 1(e). APPLE-1003, ¶¶229-230



APPLE-1003, ¶230 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi additionally provides [12a] in the second manner. In particular,

Hayashi's "insulating sheet 1" provides the *hardened insulating polymer layer*, and "insulating sheet 6," alone or together with "insulating sheet 7, provides the *baseboard*. Together, these layers provide the *insulating material layer*. *Supra*, §VI.E.2, Analysis of [12pre]; APPLE-1011, FIG. 1(a), [0012], [0015], [0017], [0029]; APPLE-1003, ¶231.



APPLE-1003, ¶231 (APPLE-1011, FIG. 1(e) (Annotated))

As discussed above, the insulating sheets contain the same type of material—such as “epoxy resin” that may be reinforced through impregnating a “woven fabric” or “non-woven fabric composed of glass”—as recited for the baseboard of the circuit board of the '909 patent. *Supra*, §VI.E.2, Analysis of [12pre]; *see also* APPLE-1011, [0016]. Thus, Hayashi's insulating sheet 6 (or combined with insulating sheet 7) provides a baseboard. APPLE-1003, ¶232.

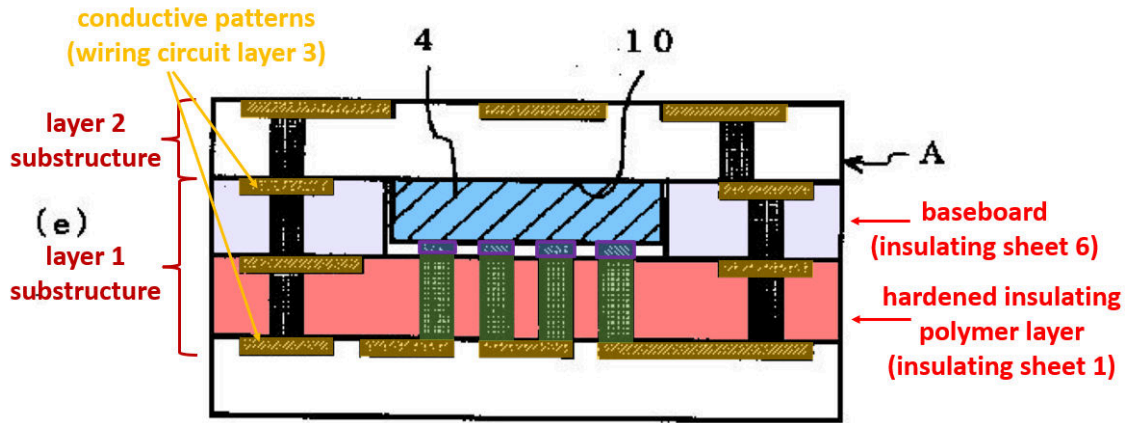
The insulating sheet 1 provides a *polymer* layer, such as “epoxy resin.” *Id.*, [0015]; APPLE-1003, ¶233. The “laminate ... is heated at or above the thermosetting temperature T_1 of the thermosetting resin in the insulating sheet 1 to

fully cure the insulating sheets 1, 6, 7,” indicating the insulating sheet 1 is *hardened*. APPLE-1011, [0029]; *see also id.*, [0010], [0012], [0013], [0019], [0032], [0035], [0040], Cls. 1, 2; APPLE-1003, ¶233.

[12b]

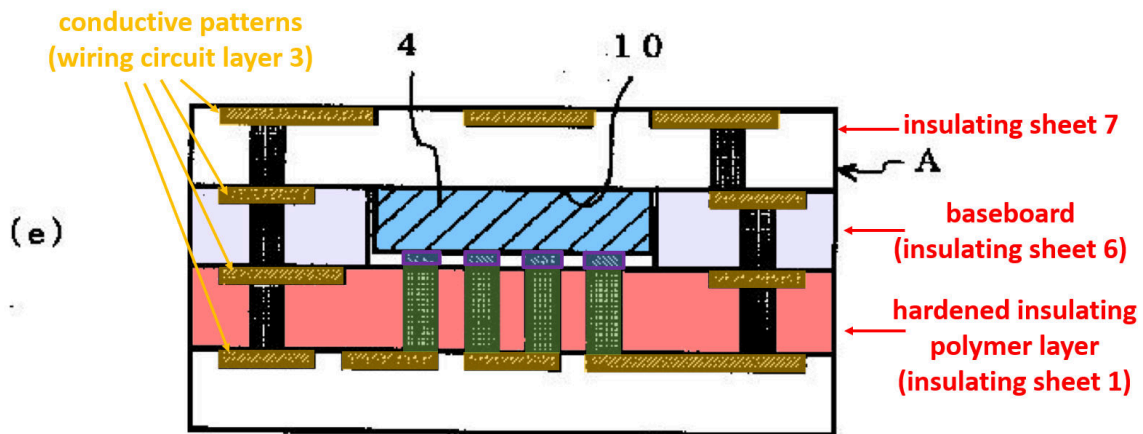
Hayashi discloses patterned “wiring circuit layer 3” that can be provided on either or both sides of each insulating sheet 1, 6, 7, with these insulating sheets laminated together resulting in the entire insulating substrate. APPLE-1011, FIG. 1, Cl. 1, [0009], [0012], [0021], [0024], [0025], [0028], [0036]-[0038], [0041], FIGS. 1(b)-(e); APPLE-1003, ¶¶234-236; *supra*, §VI.E.1. Thus, wiring circuit layers 3 (*conductive patterns*) are provided on both sides of the entire insulating substrate made of insulating sheets 1, 6, 7. Alternatively, when only insulating sheets 1 and 6 map to the recited insulating material layer, wiring circuit layers 3 are also on both sides of this insulating material layer. APPLE-1011, FIG. 1; APPLE-1003, ¶237.

Below annotated FIG. 1(e) illustrates how Hayashi provides [12b] in the first manner as discussed above, showing wiring circuit layers 3 on both sides of the insulating material layer comprised of insulating sheets 1 and 6. *Supra*, § VI.E.2, Analyses of [12pre]-[12a]; APPLE-1003, ¶238.



APPLE-1003, ¶238 (APPLE-1011, FIG. 1(e) (Annotated))

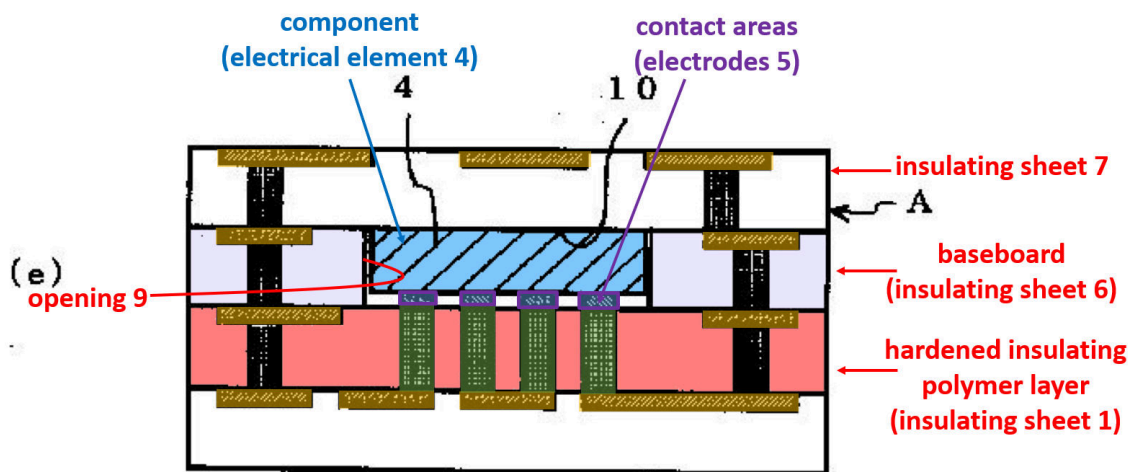
Hayashi also provides [12b] according to the second manner (annotated FIG. 1(e) below), focusing on the layer 1 substructure of the stack-up multilayered configuration. *Supra*, § VI.E.2, Analyses of [12pre]-[12a]; APPLE-1003, ¶239.



APPLE-1003, ¶239 (APPLE-1011, FIG. 1(e) (Annotated))

[12c]

Hayashi's "electrical element 4," such as a semiconductor element, embedded in an opening of the wiring substrate provides *at least one microcircuit embedded in the insulating material layer*. APPLE-1011, Title, Cls. 1, 2, [0001]-[0003], [0005], [0007], [0026], [0027]-[0028], [0031], [0038] ("a silicon semiconductor memory chip"), [0039]-[0041], FIG. 1(e); APPLE-1003, ¶240. *Supra*, §VI.E.1. Electrical element 4 is stowed in an opening 9 in an insulating sheet 6 (*a hole in the baseboard*). APPLE-1011, [0028], [0039]; APPLE-1003, ¶¶241-242.



APPLE-1003, ¶241 (APPLE-1011, FIG. 1(e) (Annotated))

Electric element 4 has "electrodes 5 formed on the back surface of the electrical element 4," where the electrodes 5 are depicted in FIG. 1(e) as contact pads that correspond to the recited *contact areas*, and the "back surface" of the electrical element 4 corresponds to the claimed *first surface*. APPLE-1011, [0026], [0030], [0038], FIGS. 1(c), 1(e); APPLE-1003, ¶¶243-244. Alternatively,

Hayashi provides the recited *contact areas*, in a second manner through its disclosure of flat areas on the back surface of electrical element 4, from which electrodes 5 extend. APPLE-1003, ¶245.

Although Figure 1(e) shows a gap between the first surface and insulating sheet 1 in a depicted cross-section, Hayashi expresses a preference that any gap will be minimized (e.g., leaving “almost no void”). APPLE-1011, FIG. 1(e), [0040], [0032]; APPLE-1003, ¶¶246-247. Hayashi explains that “it is preferable to make the thermosetting resin [of the insulating sheets] flow before curing to minimize a gap with an insulating phase at the periphery of the electrical element 4 to improve reliability.” APPLE-1011, FIG. 1(e), [0032]. “The opening in the insulating sheet contracted due to the flow of resin caused by heating, and the insulating layer and the chip were **bonded closely together**, leaving almost no void between the chip and the insulating layer.” *Id.*, [0040]. Notably, the claim language “*against*” does not recite that there is no gap **anywhere** between the first surface and the hardened insulating polymer layer. APPLE-1003, ¶248. To be clear, a POSITA would have understood that Hayashi teaches, and renders obvious, that it is preferable to minimize a void between the first surface of electrical element 4 and a surface of insulating sheet 1 (*the hardened insulating polymer layer*) for improved reliability, such that the two surfaces are touching (thus *against* each other) at least in some places, without needing to eliminate all

gaps completely across the entirety of the first surface. APPLE-1003, ¶¶249-252.

This analysis applies for both the first and second manners of satisfying two circuit board substructures as discussed in § VI.E.2, Analysis of [12pre]. APPLE-1003, ¶253. Electrical element 4 is embedded in insulating sheet 6 of both manners.

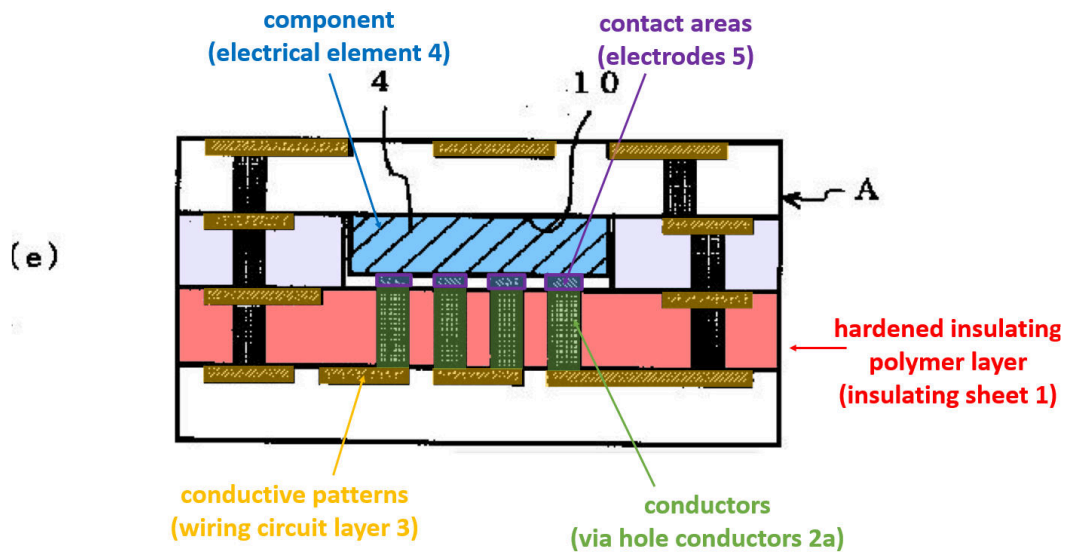
[12d]

As discussed above, Element [12d] recites product-by-process elements that are not limiting for purposes of determining invalidity. *Supra*, § III.A. (FN 1); §VI.A.2, Analysis of [12d] (Asahi ground); APPLE-1003, ¶254.

Even if the recited process of the product-by-process element is considered limiting, Hayashi renders obvious Element [12d].

Hayashi's "via-holes passing through in the thickness direction [] formed in the insulating sheet 1," to form "via-hole conductors 2a for connecting the electrical element," provide ***contact openings in the hardened insulating polymer layer***. APPLE-1011, [0012]; APPLE-1003, ¶255.

Hayashi discloses that via-hole conductors 2a is connected to the electrodes 5 of electrical element 4 and is also connected with wiring circuit 3 (***conductive patterns***), such that electrical element 4 is electrically connected to the wiring board. APPLE-1011, [0012], [0018], [0026], [0030], [0031], [0034], [0035], [0038], [0041]-[0042], Cls, 1 & 2, FIG. 1(e); APPLE-1003, ¶¶256-258.



APPLE-1003, ¶258 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi's via hole conductors 2a contain *copper*. APPLE-1003, ¶259.

Hayashi describes that via hole for forming via-hole conductors 2a “are filled with an [*sic*] conductive paste” containing “a low melting point metal having low melting point T_2 , which is equal to or lower than thermosetting temperature T_1 of the thermosetting resin, and a high melting point metal having a melting point” higher than T_1 . APPLE-1011, [0012]. Hayashi further explains, “tin (Sn), zinc (Zn), bismuth (Bi), or an alloy thereof with silver (Ag) or **copper** (Cu), etc. is preferred as the low melting point metal,” while “[**c**]**opper, silver, a copper-silver alloy, or any mixture thereof** is preferably used as the high melting point metal.” APPLE-1011, [0018], [0020].

In more detail, Hayashi discloses, “conductive paste consisted of a metal component composed of 50 vol% copper powder with an average particle size of 5

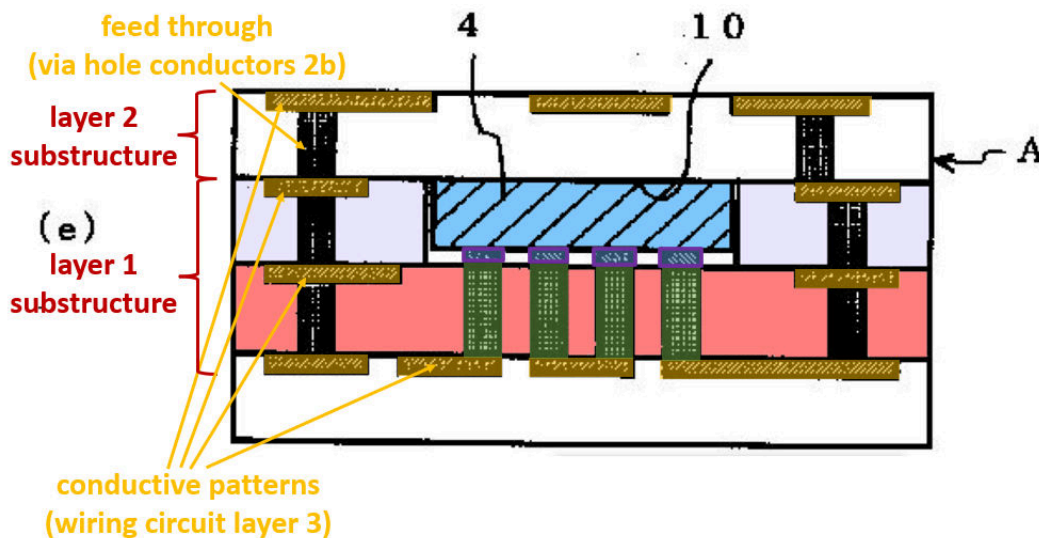
μm plated with silver and 50 vol% Sn-Pb eutectic solder powder with an average particle size of 3 μm (melting point $T_2 = 183^\circ\text{C}$) serving as the low melting point metal[.]” *Id.*, [0035]. Based on Hayashi’s express teachings, a POSITA would have understood and found obvious the use of other core materials (metal or non-metal) plated with copper, formed with conventional plating techniques, such as electroless chemical plating (*at least one of electrochemically deposited copper and chemically deposited copper*). APPLE-1003, ¶260 (citing APPLE-1017, 12). Indeed, a POSITA would have recognized and found obvious, from Hayashi’s description, that copper-plated core materials would have similarly effectuated Hayashi’s objectives for its conductive paste, especially because both copper and silver are identified design options by Hayashi for the metal component in the conductive paste, and Hayashi describes copper, silver, a copper-silver alloy, or any mixture thereof as equivalent alternatives. APPLE-1011, [0021], [0035]. *Intel*, 61 F.4th at 1381. Moreover, a POSITA would have been prompted to utilize a copper-plated material to utilize a known composition readily available and facilitating low-cost manufacturing, and would have had a reasonable expectation of success in doing so in view of the known use of such materials in similar applications. *Id.*; APPLE-1003, ¶261.

This analysis applies for both the first and second manners of satisfying two circuit board substructures as discussed in § VI.E.2, Analysis of [12pre], as the

connection structure between electrodes 5 and bottom wiring circuit layer 3 is within insulating sheet 1 of both options. APPLE-1003, ¶262.

[13]

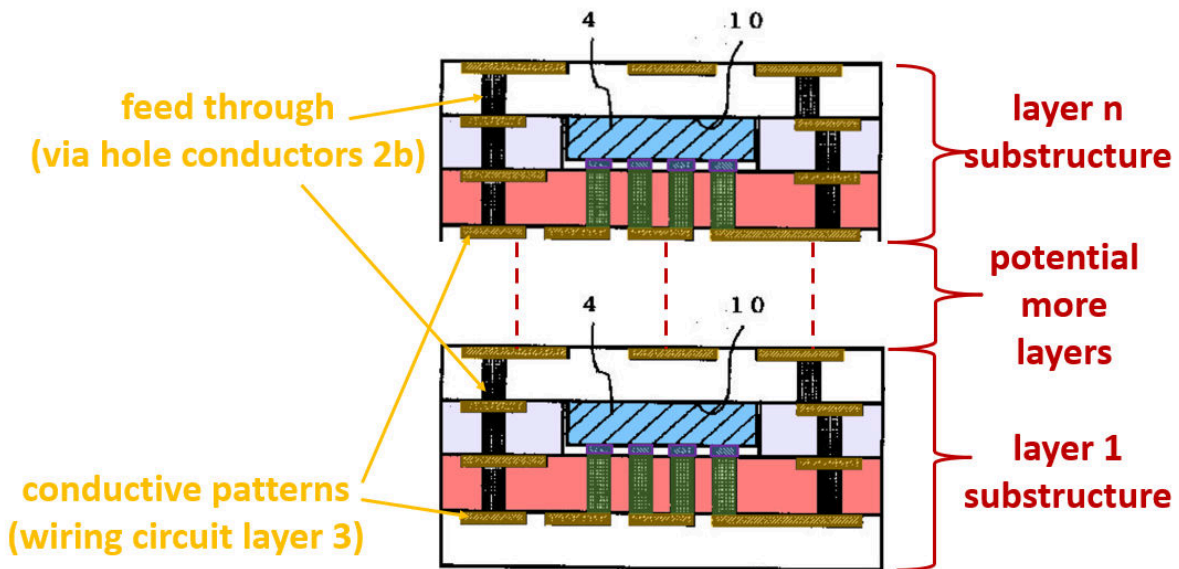
Hayashi discloses “via-hole conductors 2b” formed on each of the laminated insulating sheets 1, 6, 7, 8 and in connection with wiring circuit layers 3 of the insulating sheets. APPLE-1011, [0012], [0028], FIGS. 1(a)-(e); APPLE-1003, ¶263. Layer 1 and 2 substructures on top of each other are electrically connected to each other by the via hole conductors 2b and the wiring circuit layers 3 of each insulating sheet in a first manner. *Supra*, § VI.E.2, Analysis of [12pre].



APPLE-1003, ¶263 (APPLE-1011, FIG. 1(e) (Annotated))

According to the second manner of forming a multilayered structure, as discussed above in § VI.E.2, Analysis of [12pre], a POSITA would have understood and found obvious that when multiple layers of substructure like the

FIG. 1(e) are laminated on top of each other, the various substructures are electrically connected to each other through “via-hole conductors 2b” and wiring circuit layers 3 to form a multilayered functioning totality, in accordance with Hayashi’s suggestions. APPLE-1011, [0032], [0034]; APPLE-1003, ¶264.



APPLE-1003, ¶264 (Composite Based on APPLE-1011, FIG. 1(e) (Annotated))

[14]

Supra, §VI.E.2, Analysis of [12pre]; APPLE-1011, [0032] (“a plurality of electrical elements can be provided ... in **the same** or different **layers**”), [0034]; *supra*, §VI.E.2, Analysis of [12c] (electrical elements include microcircuits); APPLE-1003, ¶265.

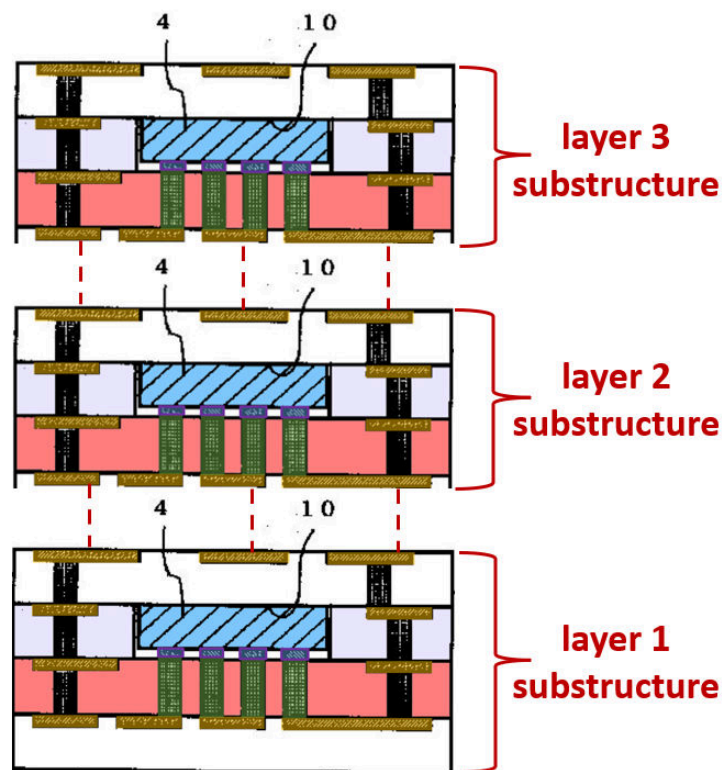
[15]

Supra, §VI.E.2, Analysis of [12pre] (“second manner”); APPLE-1011, [0032] (“a plurality of electrical elements can be provided ... in the same or

different layers”), [0034]. *Supra*, §VI.E.2, Analysis of [12c] (electrical elements include “silicon semiconductor *memory* chip[s]”). APPLE-1011, [0038]. APPLE-1003, ¶266.

[16]

In the resulting device, three similar circuit board substructures are laminated on top of each other with potential other layers such as additional insulating sheets in between with wiring circuit layers and via hole conductors 2b on them to electrically connect the substructures to each other, in accordance with Hayashi’s teachings, to achieve a high component density, compact configuration. APPLE-1003, ¶267-268; *supra*, §VI.E.2, Analysis of [12pre], Claim [13].



APPLE-1003, ¶268 (Composite Based on APPLE-1011, FIG. 1(e) (Annotated))

[17pre]-[17d]

Supra, §§VI.E.2, Analyses of [12pre]-[12d] (“second manner”); APPLE-1003, ¶269.

[18]

Supra, §§VI.E.2, Analyses of Claims [13] and [16]; APPLE-1003, ¶270.

[19pre]-[19d]

Supra, §§VI.E.2, Analyses of [12pre]-[12d], and Claim [18]; APPLE-1003, ¶271.

[20pre]-[20d]

Supra, §§VI.E.2, Analyses of [12pre]-[12d] (“second manner”), and Claim [19]; APPLE-1003, ¶272.

[21]

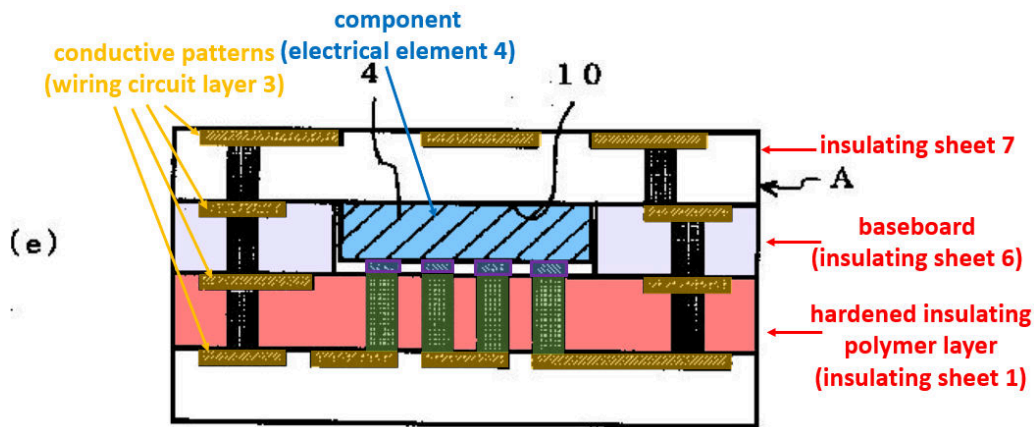
Supra, §§VI.E.2, Analyses of [12pre]-[12a] (insulating sheet 1 contains “epoxy resin”) and Claim [20]; APPLE-1003, ¶273.

[22]

Supra, §§VI.E.2, Analyses of [12pre]-[12a] (insulating sheets contain “epoxy resin” and a “woven fabric, non-woven fabric composed of glass”) and Claim [20]; APPLE-1003, ¶274.

[23]

Supra, §§VI.E.2, Analyses of [12b]-[12c]; APPLE-1011, FIG. 1(e) (showing electrical element 4 located in between wiring circuit layers 3 on both sides of the insulating material layer composed of insulating sheets 1 and 6 (or 1, 6 and 7)); APPLE-1003, ¶275.



APPLE-1003, ¶275 (APPLE-1011, FIG. 1(e) (Annotated))

[24]

Hayashi renders obvious Claim [24], even if the recited processes of the product-by-process element are considered limiting. *Supra*, §III.A. (FN 1), §VI.A.2, Analysis of Claim [24] (Asahi ground); APPLE-1003, ¶276. As discussed in §VI.E.2 (Ground 2A), Analyses of [12d], a POSITA would have understood and found obvious to use a core plated with one or more layers of copper, as the metal component of conductive paste of via hole conductors 2a, using common plating techniques including electroless chemical plating (chemically deposited copper). APPLE-1003, ¶277.

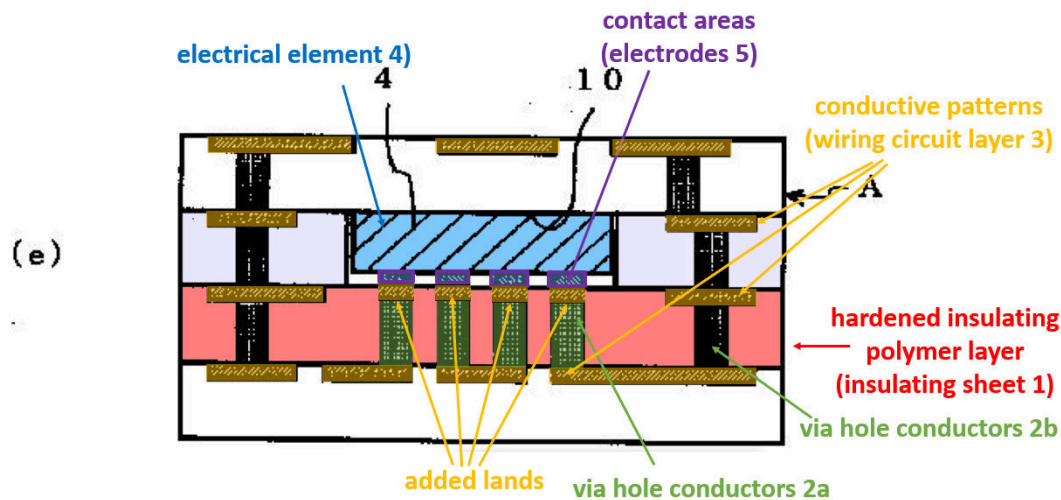
Additionally, a POSITA would have found it obvious, based on Hayashi's teachings of land areas over via hole conductors, to apply a second layer of copper on the via hole conductors by forming land areas over the via hole conductors. APPLE-1003, ¶278. Hayashi expressly illustrates lands provided by wiring circuit layer 3 on via hole conductors 2b (and similar conductor pads on the bottom ends of via hole conductors 2a), which was a common technique known to a POSITA to enhance the device by facilitating alignment and electrical connections between the vias and/or between the vias and component electrodes (e.g., Hayashi's electrodes 5). APPLE-1003, ¶278 (citing APPLE-1016; APPLE-1027). Based on Hayashi's teachings, a POSITA would have found it obvious to form similar lands over the top ends of via hole conductors 2a, and would have predictably done so with a reasonable expectation of success, especially because Hayashi expressly describes the use of such conducting structures and because they would have been readily implemented in connection with forming the wiring circuit layer 3, for example, facilitating efficient manufacturing. APPLE-1003, ¶279; APPLE-1011, [0024] ("connecting pads"), [0028], FIG. 1.

Hayashi describes the lands on via hole conductors 2b (e.g., part of wiring circuit layer 3) are formed by copper "plating." APPLE-1011, [0024] ("depositing a resist on a surface of the insulating sheet 1 surface and then performing plating"), [0025] ("copper" used for wiring circuit layer 3). A POSITA would have been

motivated to effectuate Hayashi's express "plating" teaching using conventional techniques, including electrochemical plating or both electrochemical and electroless chemical plating. APPLE-1003, ¶¶280-282.

In the resulting device, lands (connecting pads) are located at the top of the via-hole conductors 2a. The lands are formed using the same method of existing wiring circuit layer 3, for example (e.g., electrochemical plating, or both electrochemical and electroless chemical plating) (*electrochemically deposited copper*), including the portions below and in contact with via-hole conductors 2a (and the portions in contact with both ends of via-hole conductors 2b). In this modified device, the lands formed using electrochemical plating (*second layer of electrochemically deposited copper*), or both electrochemical plating (*second layer of electrochemically deposited copper*) and electroless plating (alternative mapping for *on the first layer of chemically deposited copper*), are also in the contact openings and on the conductive paste containing chemically deposited

copper (*on the first layer of chemically deposited copper*)⁹. APPLE-1003, ¶283.



APPLE-1003, ¶283 (Modified Based on APPLE-1011, FIG. 1(e) (Annotated))

[25]

Hayashi discloses the use of a metal foil for forming the patterned wiring circuit layers 3 above and below electrical element 4, with an exemplary “**copper foil with a thickness of 12 μm .**” APPLE-1011, [0003], [0024], [0036], FIG. 1; *supra*, §VI.E.2, Analysis of Claim [23]. A POSITA would have found obvious that this “metal foil” provides a “metal plate.” APPLE-1003, ¶284. Indeed, the

⁹ The added copper lands together with copper-plated particles inside the via hole conductors 2a penetrate through insulating sheet 1, the *hardened insulating polymer layer*, thus further providing the recited *copper in the contact openings* of Element [12d], with the *contact openings* defined by the via hole conductors 2a and the lands over them. *Supra*, §VI.E.2, Analysis of [12d]; APPLE-1003, ¶283.

'909 patent uses “metal foil” and “metal plate” interchangeably, and describes forming conductive pattern layers from a copper foil with a thickness of “e.g., c. 5 μm .” APPLE-1001, 9:11-29; 4:40-59, 5:47-56, 8:44-9:41, FIGS. 1J, 4D; APPLE-1003, ¶285.

[26]

Supra, §§VI.E.2, Analyses of Claims [23] and [25]; APPLE-1003, ¶286.

[27pre]-[27d]

Supra, §§VI.E.2, Analyses of [17pre]-[17d]; APPLE-1003, ¶287.

[27e]

Supra, §§VI.E.2, Analyses of Claims [25] and [26]; APPLE-1003, ¶288.

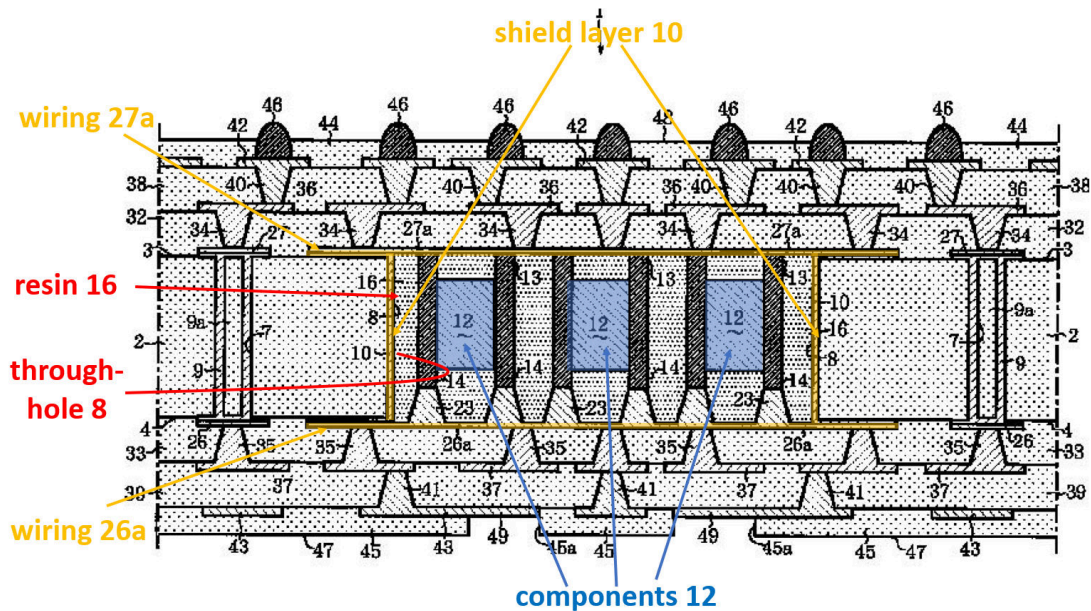
F. GROUND 2B – Hayashi-Eiji renders obvious Claims 1-33

1. Eiji

Eiji describes “a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded[.]” APPLE-1012, Abstract, FIG. 1; *see also*, [0001], [0005]-[0017], [0023], [0041]-[0042], Cls. 1, 6. APPLE-1003, ¶¶88-90.

Eiji also describes filling the through-hole with a resin (e.g., resin 16), “[i]n this way, electronic components are securely embedded in through-holes or

recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer.” *Id.*, [0007], [0010], [0019], cls. 2, 7, FIGS. 1, 3; *see also*, [0031]; APPLE-1003, ¶91.



APPLE-1003, ¶91 (APPLE-1012, FIG. 1 (Annotated))

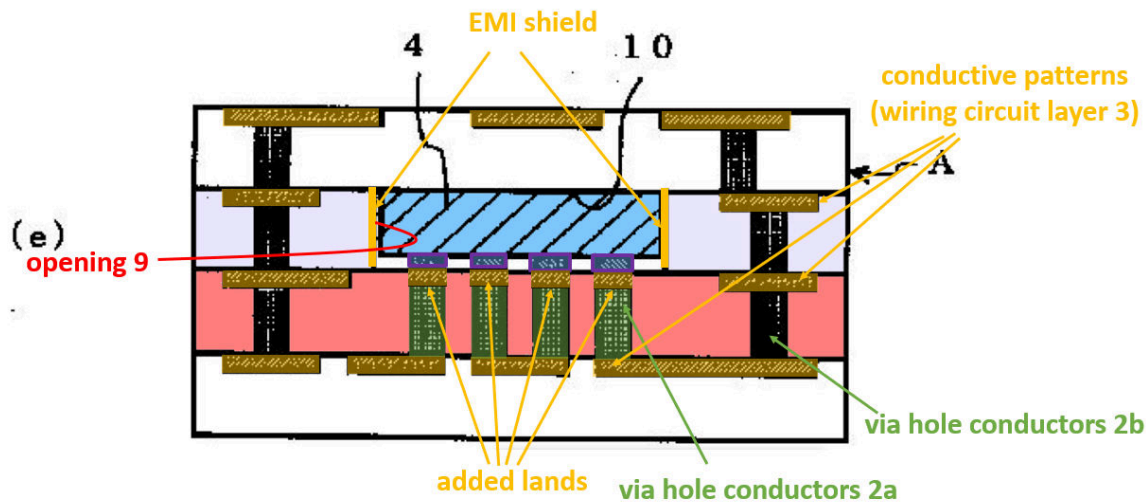
Eiji further describes wiring layers 26 and 27, “formed in the upper and lower openings to the through-hole 8.” *See e.g.*, APPLE-1012, [0011], [0023]. These metal layers are formed from “copper foil” with thickness of more than “several 10 μm thick.” *Id.*, [0017], [0021], [0025], FIGS. 1, 4; APPLE-1003, ¶91.

2. Predictable Combination of Hayashi and Eiji

A POSITA would have been motivated to combine Hayashi and Eiji to use a shield layer on the sidewalls of the opening with the electrical element embedded therein, in accordance with Eiji, to make electronic components built into an

insulating substrate “less susceptible to external electromagnetic waves, which can reduce the effects of noise generated by the circuits constituting these electronic components, and which can stabilize the electrical characteristics inside the wiring substrate[.]” APPLE-1011, [0028], [0039]; APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶290.

In the predictable combination, a “a shielding layer [] composed of a copper plating film that shields electromagnetic waves is formed on an inner surface” of the opening 9 before housing electrical element 4 in a hermetically sealed void formed by the insulating sheets 1, 6 and 7. APPLE-1011, [0028], [0039]; APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶291. Additionally, Eiji provides express disclosure of forming metal layers using both electroless plating and electrolytic plating on an insulating substrate, further confirming a POSITA would have found it obvious to implement both these plating techniques in forming the lands over the combined system’s via hole conductors 2a. *Supra*, §VI.E.2, Analysis of Claim [24]; APPLE-1012, [0021]-[0022]; APPLE-1003, ¶¶292-293.



APPLE-1003, ¶293 (Composite Based on APPLE-1011, FIG. 1(e) (Annotated))

Multiple reasons would have prompted a POSITA to combine Hayashi and Eiji. APPLE-1003, ¶294.

First, a POSITA would have been motivated to combine Hayashi and Eiji to provide protection against external electromagnetic waves, reduce influence by noise from circuits composed of the electronic components, and to stabilize electrical characteristics of the entire system. APPLE-1003, ¶295.

Hayashi already teaches providing an opening 9 in the insulating sheet to house electrical element 4. APPLE-1011, [0028], [0039]; APPLE-1003, ¶296. Additionally, it was well known in the field of component built-in devices, such as the electrical element mounted wiring board device described in Hayashi, by the Critical Date that electronic components built into an insulating substrate can be susceptible to external electromagnetic waves as well as noise generated by the

circuits constituting these electronic components, as evidenced by Eiji. APPLE-1012, Abstract; APPLE-1003, ¶296. Eiji provides a solution for these common problems that can “stabilize the electrical characteristics” of the system. APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶297.

Second, a POSITA would have been prompted to combine Hayashi and Eiji because doing so was the application of known techniques (forming a shield layer, made of copper-plated film, on the inner surface of sidewalls of an opening that is provided in an insulating board for incorporating an electronic component) to a known device (Hayashi’s wiring board having an opening 9 in the insulating sheet to stow and mount electrical element 4) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Hayashi and Eiji describe similar electronic modules involving embedding electronic components inside holes or openings of an insulation board, and because the modifications would have been implemented largely by adding a copper-plated layer on the sidewalls of the opening, in order to create interference protection around the electronic components—a configuration Eiji already demonstrates to be successful. APPLE-1003, ¶298-299. Hayashi and Eiji are analogous subject matter in the same field of endeavor and reasonably pertinent to

common problems associated with semiconductor packaging and manufacturing, including for the reasons note above. *Id.*

3. Application to Challenged Claims

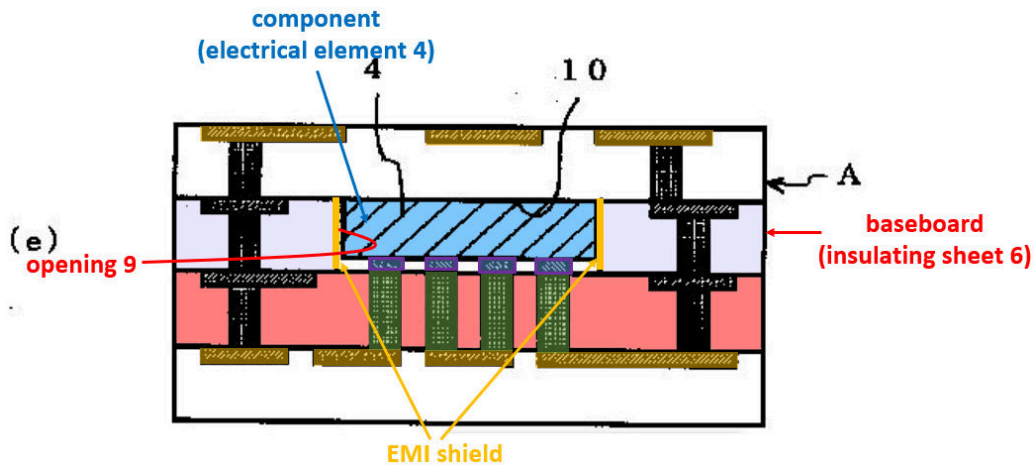
[1pre]-[1c], [1e]

The Hayashi-Eiji combination provides [1pre]-[1c] and [1e]. APPLE-1003, ¶¶301-302. The mappings discussed for features of Claim 12 apply to the same features recited in these elements of Claim 1.¹⁰ *Supra*, §§VI.E.2, Analyses of Elements [12pre]-[12d]; APPLE-1003, ¶¶301-302.

[1d]

In the Hayashi-Eiji combination a metal “shielding layer” is on the four sidewalls of opening 9 in insulating sheet 6. *Supra*, §VI.F.2; APPLE-1003, ¶303.

¹⁰ To be clear, Hayashi-Eiji renders obvious independent claim 1 and its dependent claims without modification according to the “second manner” to utilize multiple circuit board substructures on top of each other that is described with reference to claims 12-27. APPLE-1003, ¶301.



APPLE-1003, ¶303 (Composite Based on APPLE-1011, FIG. 1(e) (Annotated))

[1e]

Even if Hayashi alone did not render obvious [1e] (which it does, *supra*, Ground 2A, [12d]), Hayashi-Eiji renders it obvious. Additionally, the Hayashi-Eiji combination (§VI.F.2) renders obvious [1e] based on Eiji's express description of electrochemically and chemically deposited copper in forming conductive layers, which confirms that a POSITA would have found it obvious to implement both of these well-known plating techniques in forming the lands over the combined system's via hole conductors 2a. APPLE1012, [0021] ("Electroless and electrolytic copper plating" in forming wiring layers of a wiring substrate); *see also* [0017]; *supra*, § VI.E.2, analysis of claim [24]; APPLE-1003, ¶301-302.

[2]

The Hayashi-Eiji combination renders Claim [2] obvious. *Supra*, §§VI.E.2, Analyses of Elements [12pre], [12a] (Hayashi's insulating sheets, including

insulating sheet 1 (*hardened insulating polymer layer*), contain “epoxy resin”) and Claim [21]; APPLE-1003, ¶304.

[3]¹¹

The Hayashi-Eiji combination renders Claim [3] obvious. *Supra*, §§VI.E.2, Analyses of Element [12pre] (Hayashi’s insulating sheets, including insulating sheet 1 (*hardened insulating polymer layer*), contain “epoxy resin” and a “woven fabric, non-woven fabric composed of glass”) and Element [12a] (insulating sheet 1 corresponding to the recited *hardened insulating polymer layer*); APPLE-1003, ¶305.

[4]

The Hayashi-Eiji combination renders Claim [4] obvious. *Supra*, §§VI.E.2, Analyses of [12pre] (Hayashi’s insulating sheets contain “epoxy resin” and a “woven fabric, non-woven fabric composed of glass”) and Element [12a] (insulating sheet 6, or alternatively 6 and 7 combined, corresponds to the recited *baseboard*); APPLE-1003, ¶306.

[5]

The Hayashi-Eiji combination renders Claim [5] obvious. *Supra*, §VI.E.2,

¹¹ There is no support for “the hardened insulating polymer layer contains epoxy and glass fibres” limitation in the ’909 specification.

Analysis of Claim [23]; APPLE-1003, ¶307.

[6]

The Hayashi-Eiji combination renders Claim [6] obvious. APPLE-1003, ¶308. As discussed in §VI.E.2, Analysis of Element [12c], Hayashi discloses that “[t]he opening in the insulating sheet contracted due to the flow of resin [such as epoxy resin] caused by heating, and the insulating layer [composed of insulating sheets 1, 6, 7] and the chip were bonded closely together, leaving almost no void between the chip and the insulating layer” APPLE-1011, [0040]. A POSITA would have understood and found obvious that the “flow of resin,” such as from insulating sheets 1 and 7, would fill in the gap in opening 9, including a vertical gap between the electrical element 4 and insulating sheet 1 and lateral gaps around electrical element 4 from the sidewalls covered by the EMI shield layer of the Hayashi-Eiji device. APPLE-1011, [0032] (“minimize a void”), [0040], [0039], FIGS. 1(d)-(e); APPLE-1003, ¶308. The insulating resin flowed into the gap in opening 9 provides *filler material in the hole*. APPLE-1003, ¶308. This is also consistent with Eiji’s teaching of a “resin 16, which is primarily epoxy resin” to secure each component “at a predetermined location in the through-hole.” APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1,3; APPLE-1003, ¶308.

[7]

The Hayashi-Eiji combination renders Claim [7] obvious. *Supra*, §VI.F.3, Analysis of Claim [6] (both Hayashi’s insulating sheets and Eiji’s resin 16 as options for the filler material contain epoxy); APPLE-1003, ¶309.

[8pre]-[8b]

The Hayashi-Eiji combination renders Claim [8] obvious. APPLE-1003, ¶310. When “a plurality of electrical elements” are provided “in **the same ... layer**[,],” these electrical elements are connected to each other through via hole conductors 2a (*conductors in the contact opening*) for connecting to both the electrodes 5 (e.g., contact pads) on the first surface of each electrical element and the wiring circuit layers 3 (*at least one of the conductive patterns*). APPLE-1011, [0032]; *supra*, §§VI.E.2 and VI.F.3, Analyses of Claim [1], [12pre]-[12d] and Claim [14]; APPLE-1003, ¶310.

[9]

The Hayashi-Eiji combination renders Claim [9] obvious. *Supra*, §VI.E.2, Analysis of Claim [24]; §VI.F.2 (Hayashi-Eiji combination); APPLE-1003, ¶311.

[10]

The Hayashi-Eiji combination renders Claim [10] obvious. *Supra*, §VI.E.2, Analysis of Claim [13] (Hayashi’s “via-hole conductors 2b” correspond to the recited *feed-through*); APPLE-1003, ¶312.

[11pre]-[11b]

The Hayashi-Eiji combination renders [11pre]-[11b] obvious. *Supra*, §§VI.F.3, Analyses of [8pre]-[8b]; APPLE-1003, ¶313.

[12]-[27]

Hayashi-Eiji renders obvious these claims for at least the same reasons set forth above. *Supra*, §§VI.E.2, Analyses of Claims [12]-[27]; APPLE-1003, ¶314.

[24]

The combined system includes lands formed over the via hole conductors 2a through a layer of electroless plating (*a first layer of chemically deposited copper*) and a layer of electrolytic plating (*a second layer of electrochemically deposited copper*) on the first layer of chemically deposited copper. *Supra*, §VI.F.2 (Hayashi-Eiji combination); APPLE-1003, ¶315.

[28]

As discussed in §VI.F.3, Analysis of Element [1d], the Hayashi-Eiji device has a conductive metal film on the four sidewalls of opening 9 to provide EMI protection around electrical element 4, in accordance with Eiji's teaching of "shielding layer 10." *See also e.g.*, APPLE-1012, [0012]. Eiji's shielding layer 10 is composed of a "copper plating film," like the formation of a metal foil on the sidewalls of the hole by copper plating as disclosed in the '909 patent. APPLE-1012, Abstract, [0012], [0017]; *see also*, [0021], [0025], [0030], [0033], [0035]-[0036]; APPLE-1001, 3:61-4:9; 8:39-46; APPLE-1003, ¶316.

[29]

The Hayashi-Eiji combination renders Claim [29] obvious. APPLE-1003, ¶317. As discussed in §§VI.F.3, Analyses of Element [1d] and Claim [28], the enhanced Hayashi-Eiji device has metal foil covering all four sidewalls of opening 9 to provide EMI protection around electrical element 4. As electrical element 4 is surrounded by the unbroken four sidewalls of opening 9 in a lateral direction of the circuit board, a POSITA would have understood and been prompted to cover all four sidewalls of opening 9, providing an unbroken metal foil covering the four sidewalls that surrounds electrical element 4 in a lateral direction of the circuit board. APPLE-1003, ¶317.

[30]-[33]

The Hayashi-Eiji combination renders Claims [30]-[33] obvious. *Supra*, §VI.E.2, Analysis of Claims [25], [26]; §VI.F.3, Analysis of [1pre]-[1e]; APPLE-1003, ¶318.

G. GROUND 2C – Hayashi-Watanabe renders obvious Claims 12-27

1. Watanabe

Watanabe teaches the use of a “conductive adhesive” having conductive particles to make electrical connections between terminals (or electrodes) on a semiconductor chip (e.g., an integrated circuit (IC) chip) and on an insulating substrate where the chip is mounted. *E.g.*, APPLE-1017, Abstract, 1, 5, 14;

APPLE-1003, ¶¶92-93. Watanabe discloses example conductive particles including “particles of metals such as Au, Ag, Cu or solder, and a conductive layer of Ni, Cu, Au, or solder is preferably provided on a spherical polymer core material such as polystyrene. A surface layer of Su [*sic* for Cu]¹², Au, solder, etc. can also be formed on the surface of conductive particles.” APPLE-1017, 12; APPLE-1003, ¶¶94-95.

2. Predictable Combination of Hayashi and Watanabe

In the combined system, the conductive material of via hole conductors (e.g., Hayashi’s via hole conductors 2a) includes a conductive layer of copper grown on a polymer core through chemical deposition, in accordance with Watanabe’s suggestions. APPLE-1017, 12, *see also* Title, Abstract, 1, 5, 14; APPLE-1003, ¶320.

Hayashi describes a “conductive paste” for via hole conductors 2a for electrically connecting electrical element 4 (through connection with its electrodes 5) and the wiring board (through connection with wiring circuit layer 3 providing terminals on the substrate), and Hayashi describes various compositions, including

¹² There is no “Su” chemical element; when read in context of the preceding sentence, a POSITA would have understood as “Cu.” APPLE-1003, ¶¶95, 322.

copper. Although copper is suggested as a lower cost option (e.g., versus silver), Hayashi does not provide exhaustive implementation details of copper-plated conductive particles. *Id.*; APPLE-1003, ¶321. A POSITA would have predictably looked to well-known techniques for forming conductive particles of a conductive paste for forming electrical connections between electrodes (or terminals) of electrical elements and a mounting substrate. Watanabe provides an example of suitable copper-plated polymer cores. APPLE-1017, Title, Abstract, 1, 5, 12, 14; APPLE-1003, ¶¶322-323.

A POSITA would have been further motivated to implement copper-plated polymer cores, in accordance with Watanabe's suggestions, for via hole conductors 2a to promote efficient manufacturing and reduced manufacturing and material costs (e.g., associated with a high silver content), while effectuating reliable electrical connection. APPLE-1003, ¶324-325.

Moreover, a POSITA would have been prompted to combine Hayashi and Watanabe, because doing so was the application of known techniques (forming conductive particles of a conductive paste through chemical deposition) to a known device (Hayashi's module that utilizes copper conductive paste) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. 398, at 417. A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Hayashi and Watanabe describe

similar devices involving similar types of insulating substrate having conductor holes containing conductive particles therein for forming electrical connections between electrodes of a semiconductor chip and wiring layers on the substrate.

APPLE-1011, Cl. 1, [0001], [0009], [0015], [0016]-[0017]; APPLE-1017, Abstract, 1, 5, 14; APPLE-1003, ¶¶326-327. Hayashi and Watanabe are analogous subject matter in the same field of endeavor and reasonably pertinent to common problems associated with semiconductor packaging and manufacturing, including for the reasons note above. *Id.*

3. Application to Challenged Claims

[12pre]-[12c], [13]-[16], [17pre]-[17c], [18], [19pre]- [19c], [20pre]-[20c], [21]-[23], [25]-[26], [27pre]-[27c], [27e]

The Hayashi-Watanabe combination provides these claim elements. *Supra*, §VI.E.2; APPLE-1003, ¶328.

[12d]/[17d]/[19d]/[20d]/[27d]

Even if Hayashi alone did not provide that *the copper contains at least one of electrochemically deposited copper and chemically deposited copper* (which it does), the Hayashi-Watanabe combination renders this limitation obvious.

APPLE-1003, ¶¶329-331. In the Hayashi-Watanabe combination, copper-plated polymer cores are used as conductive particles of the conductive paste in the via hole conductors 2a described by Hayashi, in accordance with Watanabe. *Supra*, §§VI.G.1 & 2 (Watanabe and Hayashi-Watanabe combination). In the combined

system, the conductive layer of copper is grown on the polymer core, in accordance with Watanabe's suggestions, thereby providing ***chemically deposited copper***, in accordance with Watanabe's suggestions, and to predictably effectuate the copper-plated polymer cores. APPLE-1017, 12, 14; APPLE-1003, ¶331.

Hayashi-Watanabe additionally renders obvious Elements [12d], [17d], [19d], [20d], and [27d] in a second manner, through formation of copper lands by electrochemical plating (***a second layer of electrochemically deposited copper***), over the via hole conductors 2a containing copper-plated polymer cores (***on the first layer of chemically deposited copper***), at the same time of forming the wiring circuit layer 3 on insulating sheet 1, to enhance alignment and robust connection with electrodes 5.¹³ *Supra*, § VI.E.2 (Hayashi ground), Analysis of Claim [24]; APPLE-1003, ¶332.

[24]

¹³ The added copper lands together with copper-plated particles inside the via hole conductors 2a penetrate through insulating sheet 1, the ***hardened insulating polymer layer***, thus providing an alternative mapping to the recited ***copper in the contact openings*** of Element [12d], with the ***contact openings*** defined by the via hole conductors 2a and the lands over them. APPLE-1003, ¶332.

The Hayashi-Watanabe combination renders obvious Claim [24], even if the recited process of the product-by-process element is limiting. *Supra*, §VI.G.3, Analysis of Element [12d]; §VI.E.2, Analysis of Claim [24]; APPLE-1003, ¶333.

H. GROUND 2D – Hayashi-Eiji-Watanabe renders obvious Claims 1-33

1. Predictable Combination of Hayashi, Eiji and Watanabe

Even if the Hayashi-Eiji combination did not provide all element of claims 1-33 (which it does), the predictable combination of Hayashi-Eiji-Watanabe would do so. A POSITA would have been motivated to implement the conductive particles of the conductive paste of Hayashi-Eiji's via hole conductors 2a with copper-plated polymer cores, in accordance with Watanabe's teaching, to reduce cost, for the same reasons articulated above in Ground 2C, achieving each element of claims 1-33. *Supra*, §VI.F.2 (Hayashi-Eiji Combination); §VI.G.2 (Hayashi-Watanabe Combination); APPLE-1003, ¶335.

2. Application to Challenged Claims

[1pre]-[1d], [2]-[8], [10]-[33]

The Hayashi-Eiji-Watanabe combination provides Elements [1pre]-[1d] and Claims [2]-[8], [10]-[33]. *Supra*, §VI.E.2 and §VI.F.3; APPLE-1003, ¶336.

[1e]

The Hayashi-Eiji-Watanabe combination renders obvious Element [1e].
Supra, §VI.F.3 (Hayashi-Eiji), Analysis of Element [1e]; §VI.G.3 (Hayashi-Watanabe), Analysis of Element [12d]; APPLE-1003, ¶337.

[9]

The Hayashi-Eiji-Watanabe combination renders obvious Claim [9]. *Supra*, §VI.F.3 (Hayashi-Eiji), Analysis of Claim [9]; §VI.G.3 (Hayashi-Watanabe), Analysis of Claim [24]; APPLE-1003, ¶338.

VII. §325(D)

None of Asahi, Hayashi, Eiji, Joshi, Dudderar, or Watanabe were applied in a rejection during prosecution, and each is relied upon for disclosure of subject matter that is materially different than applied or set forth within references cited during prosecution. The Petition thus does not involve the same or substantially the same art or arguments previously presented, ending the *Advanced Bionics* inquiry in favor of institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

Here, while Asahi was cited on the face of the '909 patent, none of the above references was applied in a substantive office action, yet they are directly material to patentability.

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314

Essentially all of the *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written Decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors. Moreover, a Motion to Transfer to the Northern District of California remains pending. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while litigation remains in early stages. As noted above, Motions to Transfer remains pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds, outweighing any inefficiencies.

IX. FEES

Apple authorizes charge of fees to Deposit Account No. 06-1050.

X. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '909 patent. The '909 patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0192IP1@fr.com.

Respectfully submitted,

Dated: February 5, 2025

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,811 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 5, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 5, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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