

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title: METHOD FOR EMBEDDING A COMPONENT IN A BASE

DECLARATION OF DR. DEAN NEIKIRK

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 5, 2025

By: 

Dean Neikirk, Ph.D.

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I, Dr. Dean Neikirk, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of Apple (“Apple” or “Petitioner”). I understand that Apple is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 7,732,909 (“the ’909 patent”) (APPLE-1001). I have been asked to provide my independent analysis of the ’909 patent in light of the prior art publications cited below.

2. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’909 patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’909 patent.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

3. I have summarized in this section my educational background, career history, and other qualifications relevant to this matter. I have also included a current version of my curriculum vitae as Appendix A.

4. I am currently an emeritus Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin, holding the Emeritus Cullen Trust for Higher Education Professorship in Engineering. I

received a B.S. in Physics and Mathematics from Oklahoma State University in 1979, an M.S. in Applied Physics from the California Institute of Technology in 1981, and a Ph.D. in Applied Physics from the California Institute of Technology in 1984. Until January 2021, I was a tenured professor and endowed chair in the Cockrell School of Engineering at the University of Texas at Austin, where I have been a member of the engineering faculty since 1984. From 1992 to 2020 I held the Cullen Trust for Higher Education Professorship in Engineering at the University of Texas. From 2014 to 2020 I was the Associate Dean of Graduate Studies where I oversaw graduate student services for over 78 doctoral programs and 116 master's degree programs. I have also served as the Graduate Advisor of the Department of Electrical and Computer Engineering (ECE) at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, and the Secretary of the General Faculty at UT-Austin.

5. In 1985, I established the Microelectronics Fabrication Teaching Laboratory at The University of Texas at Austin, which continues to this day to provide undergraduate and graduate students with hands-on experience in IC fabrication. I have taught many courses in integrated-circuit fabrication, microwave devices, IC packaging, multi-chip modules, electromagnetics, computer aided design methods for circuit simulation, sensors of all sorts, and micro-

electromechanical systems. In recognition of my research and classroom teaching accomplishments, I received the 1984-85 Engineering Foundation Faculty Award from the University of Texas at Austin Engineering Foundation Advisory Council, the 1985-90 General Motors Foundation Centennial Teaching Fellowship, the 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, the 1990-1992 Temple Foundation Endowed Faculty Fellowship, the 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, the 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, and the 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching. In recognition of my service to the University of Texas at Austin I also received the 2015 University of Texas at Austin Civitatis Award.

6. My research over the last thirty-five years has concentrated heavily in the areas of optical systems, microelectronics, semiconductor devices, IC fabrication, device packaging, multi-chip modules, and new sensors. This research work has been funded by many agencies, focusing on the fabrication and modeling of semiconductor devices, electromagnetic devices and detectors, chemical sensors, temperature sensors, proximity sensors, and pressure sensors, as well as research on device packaging, the high frequency properties of transmission lines, RF devices, and infrared to terahertz detectors for use in focal plane imaging arrays.

My research related to the development of new chemical sensors (an “electronic taste” sensor) was selected for a commercialization venture between The University of Texas and two outside startup companies.

7. My early research was in the interaction of light with optically active materials, including color centers in crystals for use as light emitters. Each of my academic degrees involved significant studies in solid state physics, semiconductor devices, device packaging, electrical engineering, electronic systems, electromagnetics, optics, radio frequency systems, and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, and optical systems. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and quasioptical imaging antenna arrays, including research on integrated-circuit fabrication, semiconductor devices, integrated circuits, antennas, sensors, and IC packaging. I designed and fabricated the first monolithic integrated-circuit imaging antenna array for use at wavelengths in the far infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. For this work on the first high resolution focal plane antenna array for use at wavelengths between 0.1 mm and 1 mm I was awarded the 1984 Marconi International

Fellowship Young Scientist Award “for contributions to the development of millimeter wave integrated circuits especially in the area of detectors and imaging arrays.” In recognition of my early research efforts, I received the 1985–1986 IBM Corporation Faculty Development Award, and the 1986 National Science Foundation Presidential Young Investigator Award.

8. As represented by the publications listed in my CV, I have extensive experience with microelectronics, semiconductors, and IC fabrication.

9. I am a lifetime senior member of the Institute of Electrical and Electronics Engineers (IEEE) and served as Associate Editor for Solid State and VLSI Electronics, IEEE Transactions on Education from March 1991 through October 1994.

10. Through my work on electronic systems and innovations in other related fields, I have been named an inventor on 17 U.S. patents. These are summarized in my curriculum vitae.

11. I have also co-authored over 250 technical papers in international journals and conferences and presented over 30 invited lectures and professional society presentations. My publications have addressed technologies such as integrated circuits for antenna arrays, multilayer interconnection lines for highspeed digital integrated circuits, determining conductor loss in transmission lines, optical and electromagnetic devices for infrared detection, RF oscillator

circuits, memory-switching double-barrier quantum-well diodes circuits, RF and infrared detection circuits, and other topics related to semiconductor and IC fabrication.

12. A detailed list of my other professional activities, memberships, and speaking engagements is included in my CV, which is attached as Appendix A.

13. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '909 patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time. Based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the 2000s and specifically during the time of the alleged invention of the '909 patent. Indeed, I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

III. LEGAL PRINCIPLES

14. I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

A. Anticipation

15. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

16. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (the so-called critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Obviousness

17. I have been informed that a patent claim is invalid as "obvious" under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention ("POSITA"), taking into account (1) the scope and content of the prior art, (2) the

differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.

18. The '909 patent was filed May 4, 2007 as a continuation of Application No. 10/502,336 (now U.S. Pat. No. 7,294,529 (“the '529 patent”)), which claims priority to PCT/FI03/00065 filed January 28, 2003, and further to Finish Application No. 20020191 filed January 31, 2002. APPLE-1001, Cover, APPLE-1002, 74, 107. For purposes of my analysis here, I have applied a date of January 31, 2002 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than January 31, 2002.

19. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves,

the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the predictable combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

20. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. I have followed this approach in my analysis.

21. I have also been informed that, according to 35 U.S.C. § 112, a patent claim may lack written description if the specification and earlier-filed priority applications fail to describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application and that the patentee invented what is claimed. I understand that

even if a description would render obvious a claimed invention, such obviousness is not sufficient to satisfy the written description requirement for that claim. I have also been informed that a patent claim may be indefinite if, read in light of the specification and prosecution history, it fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

22. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have used the date of January 31, 2002 for reasons explained in ¶ 18 (above) and ¶¶ 24-25 (below). However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the early to mid-2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

23. A person of ordinary skill in the art at the time of the '909 patent (a "POSITA") would have had at least a Bachelor's degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. In view of the pertinent prior art discussed herein, my analysis would be the same applying a slightly higher or lower level of skill.

24. I have used January 31, 2002 as the point in time from which my analysis from the perspective of a POSITA is based, but my analysis would be similar even if the date was slightly earlier or later.

V. MATERIALS CONSIDERED

25. My analyses set forth in this declaration are based on my experience in the field of IC packaging and multi-chip modules. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the early- to mid-2000s and specifically during the time before the alleged priority date (January 31, 2002) for the '909 patent, and I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

26. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the critical date for the '909 patent; my own knowledge and experiences gained from my work experience in the field; and my experience in working with others, including teaching and advising others in the field. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- | | | |
|-----|------------|--|
| 27. | APPLE-1001 | U.S. Patent No. 7,732,909 (“the ’909 patent”) |
| 28. | APPLE-1002 | U.S. Patent No. 7,732,909 File History |
| 29. | APPLE-1004 | Certified Translation of JP Application Publication
2001-339165A (“Sakamoto”) |
| 30. | APPLE-1005 | U.S. Patent Application Publication No.
2002/0175402 (“McCormack”) |
| 31. | APPLE-1006 | U.S. Patent No. 6,489,685 (“Asahi”) |
| 32. | APPLE-1007 | U.S. Patent Application Publication No.
2001/0030059 (“Sugaya”) |
| 33. | APPLE-1008 | U.S. Patent Application Publication No.
2002/0020898 (“Vu”) |
| 34. | APPLE-1009 | RESERVED |
| 35. | APPLE-1010 | RESERVED |
| 36. | APPLE-1011 | Certified Translation of JP Patent No. 3207174
(“Hayashi”) |
| 37. | APPLE-1012 | Certified Translation of JP Patent Application
Publication No. 2002-016327 (“Eiji”) |
| 38. | APPLE-1013 | U.S. Patent No. 6,335,571 (“Capote”) |
| 39. | APPLE-1014 | U.S. Patent No. 6,297,551 (“Dudderar”) |
| 40. | APPLE-1015 | U.S. Patent No. 6,404,052 (“Kurita”) |

41. APPLE-1016 Certified Translation of JP Patent Application
Publication No. 2001-068624A (“Imoto”)
42. APPLE-1017 Certified Translation of PCT Publication No. WO
00/09623 (“Watanabe”)
43. APPLE-1018 U.S. Patent No. 4,179,802 (“Joshi”)
44. APPLE-1019 U.S. Patent No. 5,608,262 (“Degani”)
45. APPLE-1020 U.S. Patent No. 5,321,210 (“Kimbara”)
46. APPLE-1021 U.S. Patent No. 5,146,674 (“Frankeny”)
47. APPLE-1022 JP Patent Application Publication No. 2001-
339165A (“Sakamoto”)
48. APPLE-1023 JP Patent No. 3207174 (“Hayashi”)
49. APPLE-1024 JP Patent Application Publication No. 2002-
016327 (“Eiji”)
50. APPLE-1025 JP Patent Application Publication No. 2001-
068624A (“Imoto”)
51. APPLE-1026 PCT Publication No. WO 00/09623 (“Watanabe”)
52. APPLE-1027 Certified Translation of JP Patent Application
Publication No. 2001-156457 (“Takayama”)
53. APPLE-1028 JP Patent Application Publication No. 2001-
156457 (“Takayama”)

54. APPLE-1029 U.S. Patent No. 5,745,984 (“Cole”)
55. APPLE-1030 R. Aschenbrenner, A. Ostmann, U. Beutler, J. Simon and H. Reichl, “Electroless nickel/copper plating as a new bump metallization,” in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 18, no. 2, pp. 334-338, May 1995, doi: 10.1109/96.386270
56. APPLE-1031 W. W. Flack, Ha-Ai Nguyen, E. Capsuto and C. McEwen, “Characterization of a thick copper pillar bump process,” 2007 12th International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces, San Jose, CA, USA, 2007, pp. 208-213
57. APPLE-1032 Xiang Dai, M. V. Brillhart, M. Roesch and P. S. Ho, “Adhesion and toughening mechanisms at underfill interfaces for flip-chip-on-organic-substrate packaging,” in IEEE Transactions on Components and Packaging Technologies, vol. 23, no. 1, pp. 117-127, March 2000
58. APPLE-1033 D. Suryanarayana, T. Y. Wu and J. A. Varcoe, “Encapsulants used in flip-chip packages,” in IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 16, no. 8, pp. 858-862, Dec. 1993
59. APPLE-1034 U.S. Patent Application Publication No. 2001/0033889 (“Bhatt”)

60. This declaration refers to selected portions of the cited references for the sake of brevity. These references are examples. It should be understood that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties. Of course, I have also considered the claims of the '909 patent. The following table provides a quick sheet enumerating claim elements for ease of reference:

Claim Element	Language
[1pre]	A circuit board, comprising:
[1a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[1b]	conductive patterns on both sides of the insulating material layer;
[1c]	at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;
[1d]	conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

[1e]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[2]	The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.
[3]	The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.
[4]	The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.
[5]	The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.
[6]	The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.
[7]	The circuit board of claim 6, wherein the filler material contains epoxy.
[8pre]	The circuit board of claim 1, wherein
[8a]	said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and
[8b]	the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

[9]	The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
[10]	The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.
[11pre]	The circuit board of claim 1, wherein
[11a]	said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and
[11b]	said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.
[12pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:
[12a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[12b]	conductive patterns on both sides of the insulating material layer;
[12c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and
[12d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

[13]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.
[14]	The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.
[15]	The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.
[16]	The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.
[17pre]	The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise
[17a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[17b]	conductive patterns on both sides of the insulating material layer,
[17c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[17d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

[18]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.
[19pre]	The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises
[19a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[19b]	conductive patterns on both sides of the insulating material layer,
[19c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[19d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[20pre]	The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises
[20a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[20b]	a conductive pattern on the insulating material layer,
[20c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and

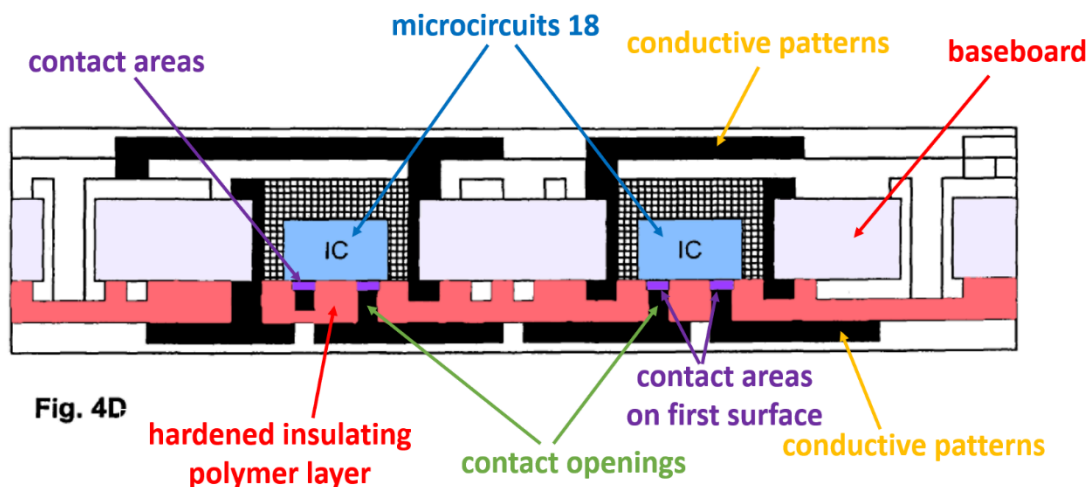
[20d]	contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
[21]	The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.
[22]	The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.
[23]	The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.
[24]	The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
[25]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.
[26]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.
[27pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising:
[27a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;

[27b]	conductive patterns on both sides of the insulating material layer;
[27c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and
[27d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and
[27e]	at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.
[28]	The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.
[29]	The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.
[30]	The circuit board of claim 1, comprising a metal plate above the microcircuit.
[31]	The circuit board of claim 1, comprising a metal plate below the microcircuit.
[32]	The circuit board of claim 1, comprising a metal plate above and below the microcircuit.
[33]	The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

VI. OVERVIEW OF THE '909 PATENT

A. Summary of the '909 Patent

61. The '909 patent relates to a method for embedding a component in a base, such as a circuit board, and an electronic module having electronic components embedded in a base. APPLE-1001, Title, Abstract. As illustrated the annotated FIG. 4D below, the electronic module includes a baseboard and a hardened insulating polymer layer, together forming an insulating material layer; conductive patterns on both sides of the insulating material layer; integrated circuit components (e.g., microcircuits 18) embedded inside the baseboard and between the two conductive pattern layers; each component having contact areas on a first surface; the first surface being against the hardened insulating polymer layer; contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the components and the conductive patterns on the lower side of the insulating material layer. APPLE-1001, FIG. 4D, cls. 1, 12.



APPLE-1001, FIG. 4D (Annotated)

62. The '909 patent additionally describes growing conductive material on the sidewalls of the holes where microcircuits 18 are embedded, in order to create protection against electromagnetic interference (EMI) around the microcircuits. *E.g.*, APPLE-1001, 3:61-4:9 (“In stage [1]C, metal is grown into the through holes made in stage B. ... The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallization can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. ... Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste.”), 8:34-41 (“The invention also permits electromagnetic protection to be made around the component embedded in the base. This is because the method of FIG. 1 can be modified in such a way that the holes 6 depicted in stage 1E can be made in connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components”), 8:64-66, cl. 1.

63. The '909 patent further describes copper in the contact openings containing “at least one of electrochemically deposited copper and chemically deposited copper.” *Id.*, cls. 1, 12, 6:21-25 (“the feed-throughs (holes 13) are first

of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 14 is increased by electrochemical deposition.”).

B. Prosecution History of the '909 patent

64. The '909 patent issued on June 8, 2010 from a continuation of application No. 10/502,336 (now U.S. Pat. No. 7,294,529 (“the '529 Patent”)), which claims priority to PCT/FI03/00065, filed January 28, 2003, which further claims priority to Finish application No. 20020191 filed January 31, 2002.

65. During prosecution, only a single office action was issued, rejecting then pending claims 1-6, 8-10, 12-25, 28, 30 and 31 under 35 U.S.C. §102(b) as being anticipated by Vu et al. (2002/0020898) (“Vu”). Then pending claims 11 and 27 under 35 U.S.C. § 103(a) were also rejected as being unpatentable over Vu, in view of an official notice stating, “formation of plated Cu layers using both [chemical and electrochemical] methods in formation of a seed layer and a bulk Cu layer was known prior to applicant’s invention.” APPLE-1002, 53-58.

Additionally, in the same office action, then pending claims 7, 26 and 29 were objected to but otherwise were considered allowable. Specifically, the original claims 7 and 26 each recite “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit,” and the original

claim 29 recites “a metal foil below at least one of the microcircuits.” *Id.*, 53-58, 100-104. In response to the office action, applicant amended the independent claims to incorporate the features of claims 7 and 26, and added new claim 32 to recite the features of claim 29. *Id.*, 43-45 (“Claim 1 has been amended to incorporate the features of Claim 7, Claim 14 has been amended to incorporate the features of Claim 26 (with Claims 7 and 26 consequently canceled). Further, new Claim 32 has been added to recite the features of Claim 29.”)

66. However, I note that the original independent claim 14 (now independent claim 12) was not correctly amended in response to the office action, as it failed to incorporate all the features of original claim 26 as the Applicant said it did. *Compare id.*, 36 *with id.*, 101-104. Particularly, current claim 12 does not recite “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit,” which was the allowable subject matter recited in the original claim 26. APPLE-1001, cl. 12. Thus, current claim 12 from the incorrectly amended original 14, and its dependent claims 13-25 for at least the same reason, fail to overcome the § 102(b) rejections based on Vu as decided in the office action. APPLE-1002, 53-58. A notice of allowance was subsequently issued with this error, which also ended prosecution prematurely without application of the more pertinent prior art such as McCormack, Sakamoto, Eiji, Sugaya and Imoto. APPLE-1002, 18-21. Based on my knowledge and

experience, and my review of the publications I discuss in more detail below, I do not agree that the '909 patent claims are patentable over the prior art. Those of skill in the art were aware of electronic modules that shared the same structural design and the known use of conductive material on the sidewalls of the holes for accommodating electronic components to achieve protection against electromagnetic interference (EMI).

VII. OVERVIEW OF THE CITED REFERENCES

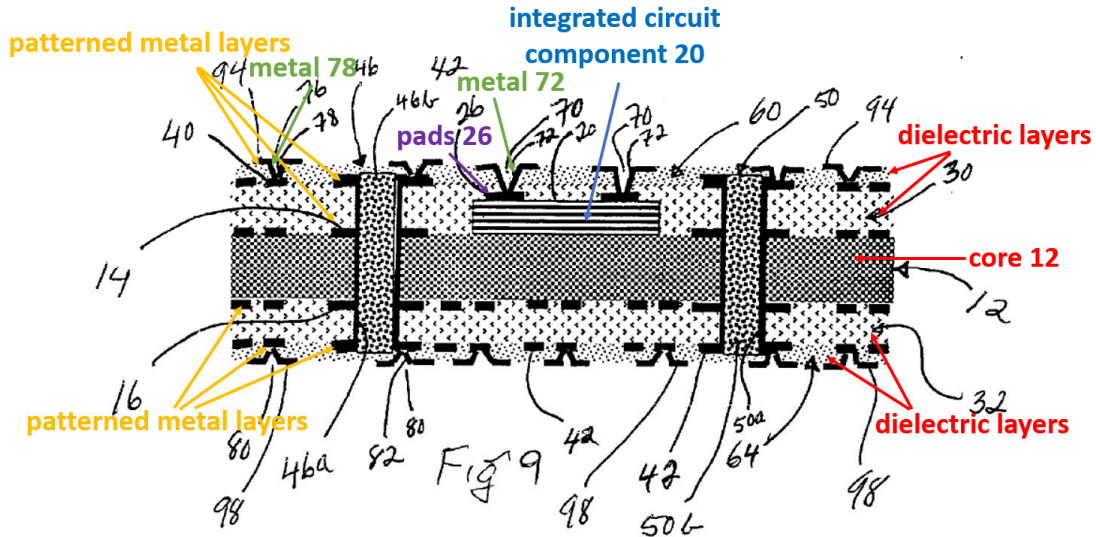
A. Overview of McCormack

67. U.S. Application Publication No. 2002/0175402 to McCormack et al. is titled “Structure and Method of Embedding Components in Multi-Layer Substrates.” APPLE-1005, Face. McCormack was filed on May 23, 2001 and was published on November 28, 2002. *Id.*

68. McCormack describes a circuit board having an embedded “integrated electronic component” and a method of producing such structure. APPLE-1005, Title, Abstract, cl. 1, [0009] (“a circuit board substrate having a first substrate surface and a second substrate surface”), [0026] (“a core 12 having opposed substrate surfaces”). McCormack describes that a prefabricated integrated circuit component 20 may be coupled to one or both surfaces of the circuit board substrate, or alternatively, one or both of the substrate surfaces “may have a cavity generally illustrated as 24” which “may be formed by any suitable means, such as

by milling, cutting or drilling” for receiving components such as “integrated circuit component 20.” *Id.*, [0028]-[0029]; *see also*, [0024]-[0025], FIGS. 9, 11-13.

69. The annotated FIG. 9 below shows a circuit component 20 mounted on an upper substrate surface of core substrate 12, and a dielectric layer (e.g., dielectric layer 30) on the substrate surface of core 12 and over the integrated circuit component 20. APPLE-1005, Abstract, [0029], [0030], Cl. 1, FIG. 9. McCormack describes optional additional dielectric layers (e.g., dielectric layers 60, 32, 64) on both the upper and lower sides of the core substrate 12, each dielectric layer and core 12 optionally have their own patterned metal layers that are electrically connected to each other through metal-lined openings (e.g., metal liners 72, 78 and 82 in openings 70, 76 and 80, respectively) and conductive feed-throughs (e.g., metal-lined vias 46, 50 and 18). APPLE-1005, Abstract, [0009] (“The method may also comprise...”), [0030] (“dielectric layers 30 and 32 may be respectively placed, flowed or laminated over the integrated circuit component 20, ... additional underfill, glop-top, or other adhesive/sealant materials may optionally be dispensed over the integrated circuit components 20 prior to any subsequent processing.”), [0031]-[0032], [0026].



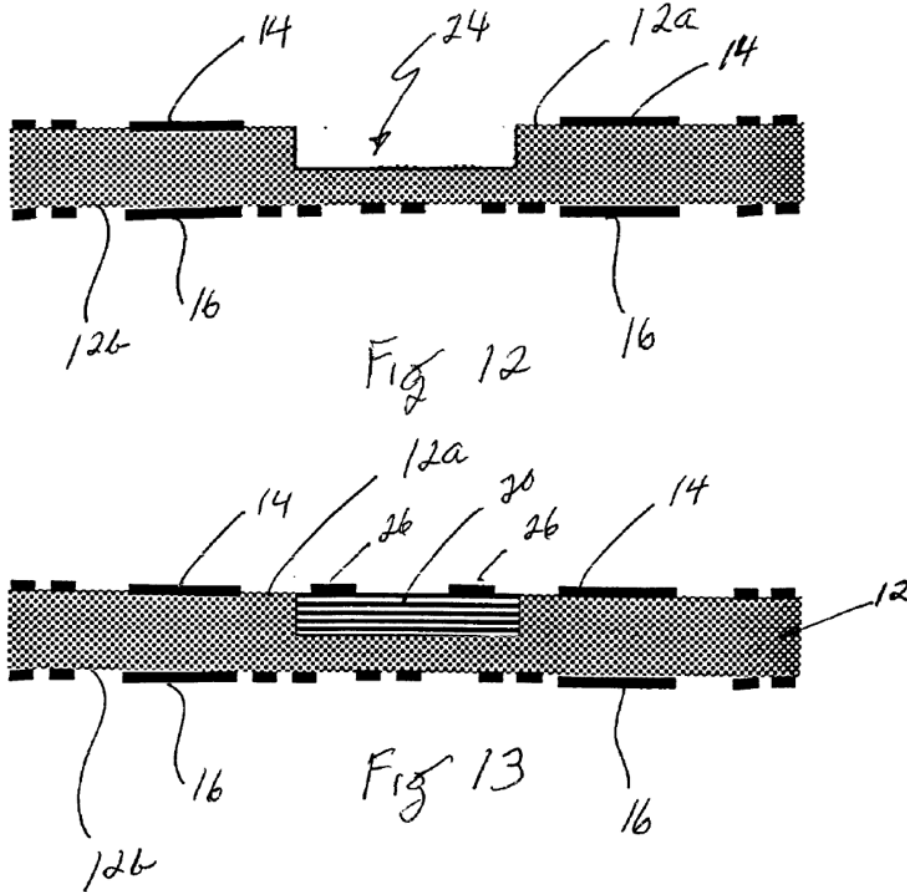
APPLE-1005, FIG. 9 (Annotated)

70. McCormack explains that suitable dielectric material for its dielectric layers and the core substrate includes “B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicones, well known to those skilled in the art.” *Id.*, [0033]. McCormack further describes that “[a] subsequent heating step may be preferably necessary to partially react the suitable material into a ‘B-stateable’ thermoplastic-like material, capable of reflowing and/or curing the material” of the dielectric layers and other materials, into a ternary matrix upon “additional exposure to heat and pressure.” *Id.*

71. To electrically connect the integrated circuit component 20 to the circuit board, “[a] pair of openings 70 is then formed (e.g., such as by laser drilling or the like)” through the dielectric layer(s) above the integrated circuit component, “to expose pads 26 of the integrated circuit component 20.” *Id.*, [0032].

McCormack further explains, “[o]penings 70 are then metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26.” *Id.*

72. McCormack describes an example method to embed components in its core substrate instead of on its surface(s), by providing “a cavity” beforehand in the core substrate 12 to dispose the integrated circuit component in the cavity. APPLE-1005, [0009]. McCormack’s FIGS. 12 and 13 illustrate this alternative embedding method, of disposing an integrated circuit component in a cavity 24 in the core substrate 12 instead of on a surface of the core 12, while sharing the same core substrate 12 of FIG. 2 and FIG. 9 and other common features indicated by the same numeral labels. *Id.*, [0024]-[0029] (describing common features of various preferred embodiments compatible with different methods for embedding the integrated circuit component 20, either on a surface of the core 12 or embedded in a cavity 24 in core 12), FIGS. 9, 12, 13. McCormack’s FIGS. 12 and 13 illustrating this alternative embedding method are reproduced below.



APPLE-1005, FIGS. 12, 13

B. Overview of Sakamoto

73. JP Application Publication No. 2001-339165A to Sakamoto et al. is titled “Multilayer Printed Wiring Board and Package Substrate.” APPLE-1004, Face. Sakamoto was filed on December 21, 2000 and published on December 7, 2001. *Id.*

74. Sakamoto describes “a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip.” APPLE-1004, [0001]; *see also*, Abstract, [0005]. For example, Sakamoto describes “providing an opening, through-hole, or counterbore in a resin insulating

substrate, incorporating an electronic component such as an IC chip in advance [.]”

Id., [0005]; *see also*, Abstract (“an IC chip 20 pre-embedded in a core substrate 30”), [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12.

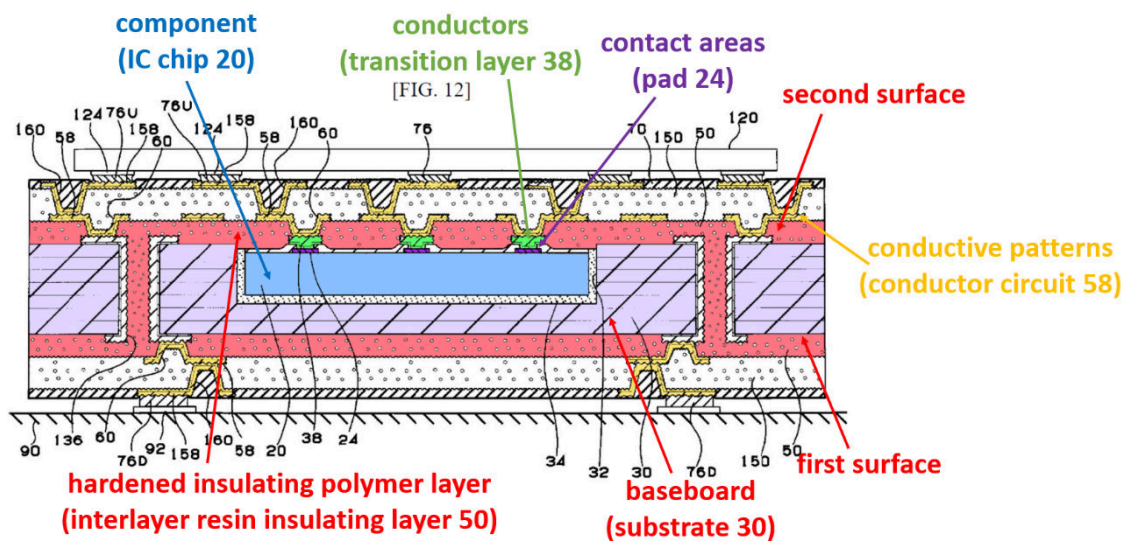
75. An “interlayer resin insulating layer 50” provided over the IC chip 20 and on a surface of substrate 30 contains polymer and is cured with the application of heat and pressure. *Id.*, [0030] (“A thermosetting cycloolefin resin sheet having a thickness of 30 to 50 μm is laminated on the substrate that has undergone the steps described above under vacuum at a pressure of 5 kg/cm^2 while raising the temperature to 50 to 150 $^{\circ}\text{C}$, resulting in an interlayer resin insulating layer 50...”), [0042] (“an epoxy resin can be used for the interlayer resin insulating layer 50 instead. This epoxy resin contains a poorly soluble resin, soluble particles, a curing agent, and other components.”), [0047] (listing examples of the soluble resin), [0057]-[0060], FIGS. 6, 10-12.

76. “Conductor circuit 58” is formed on the top surface of the interlayer resin insulating layer 50 and the inner wall surface of openings for via holes 60, which are formed through the interlayer resin insulating layer for connecting the electronic components and the conductive circuits. *Id.*, [0017], [0036].

“Conductor circuit 158” is “formed in interlayer resin insulating layer 150.” *Id.*, [0017], [0005]-[0007] (“providing a via on the IC chip pad by photoetching or laser to form a conductor circuit that is a conductor layer, and then repeatedly

forming the interlayer insulating layer and the conductor layer to provide a multilayer printed wiring board”).

77. Sakamoto further describes that “a transition layer 38” made of copper is provided on die pads 24 of the IC chip 20, to connect to via 60 in the interlayer resin insulating layer 50. *Id.*, Abstract (“by providing a transition layer 38 on the die pad 24 ... connectivity between and reliability of die pads 24 and via hole 60 can be improved”), [0018], [0020], [0028], [0031] (“a transition layer 38 made of copper on the die pads 24”), [0067], [0069], FIGS. 2, 6, 10, 12.



APPLE-1004, FIG. 12 (Annotated)

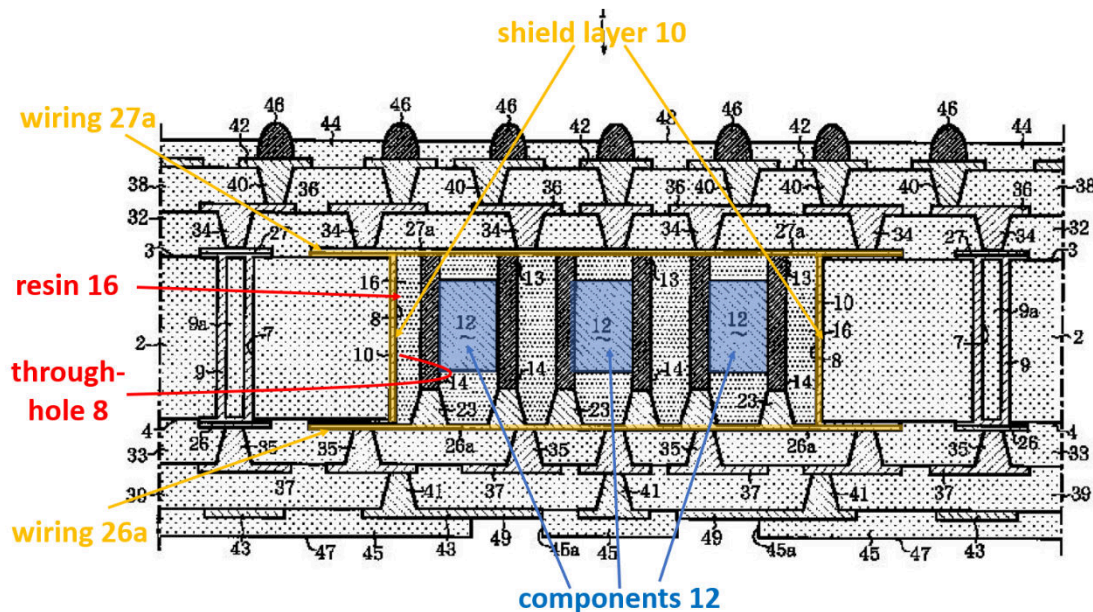
C. Overview of Eiji

78. JP Patent Application Publication No. 2002-016327 to Eiji et al. is titled “Wiring Substrate and Manufacturing Method Therefor.” APPLE-1012, Face. Eiji was filed April 23, 2001 and published January 18, 2002.

79. Eiji describes reducing EMI susceptibility of electronic components built into an insulating substrate, through a solution where “a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded[.]” *Id.*, Abstract, FIG. 1; *see also*, [0001], [0005], [0006] (“electronic components embedded in through-holes or recessed portions [of the insulating substrate] can be shielded from external electromagnetic waves, and noise generated from circuits composed of these electronic components to the outside can be reduced”), [0007], [0009], [0011]-[0012] (“an approximately 25 μm -thick shielding layer 10 is formed by copper plating on the inner surface of the outer circumference of the through-hole 8”), [0017] (“electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8 and through-holes 7 after applying catalyst metal nuclei for plating such as Pd”), [0041], cls. 1, 6.

80. Eiji gives examples of the electronic components including “active components such as low-noise amplifier (LNAs), transistors, semiconductor devices, and FETs, as well as SAW filters, LC filters, antenna switch modules, couplers, and diplexers, and any of the components listed above made into chip form.” *Id.*, [0006].

81. Eiji also describes filling the through-hole with a resin (e.g., resin 16), “[i]n this way, electronic components are securely embedded in through-holes or recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer.” *Id.*, [0007], [0010], [0019] (“after filling the through-hole 8 from the front surface 3 side with melted resin 16, which is primarily epoxy resin, curing is performed to hold the resin at about 100 °C for about 60 minutes. As a result, as shown in the figure, the resin 16 solidifies and each [electronic component] is embedded at a predetermined location in the through-hole 8 by the resin 16”), cls. 2, 7, FIGS. 1, 3; *see also*, [0031].



APPLE-1012, FIG. 1 (Annotated)

82. Eiji further describes wiring layers (e.g., wiring layers 26 and 27) that are “formed in the upper and lower openings to the through-hole 8.” *See e.g., Id.*,

[0011], [0023]. These metal layers are formed from “copper foil” with thickness of more than “several 10 μm thick” after plating. *Id.*, [0017] (26, 27 formed from “copper foil 5, 6 that is several 10 μm thick”), [0021] (“Electroless and electrolytic copper plating is applied to ... the copper foil 5, 6” to form even thicker metal layers); *see also* [0025] (“Shielding layers 60a and 60b, each about 25 μm thick”), FIGS. 1, 4.

D. Overview of Sugaya

83. U.S. Patent Application Publication No. 2001/0030059 to Sugaya et al. is titled “Circuit Component Built-in Module, Radio Device Having the Same, and Method for Producing the Same.” APPLE-1007, Face. Sugaya was filed December 15, 2000 and published October 18, 2001. *Id.*

84. Sugaya describes “[a] circuit component built-in module capable of mounting the circuit component” such as semiconductor chips “with high density.” APPLE-1007, Title, Abstract. Sugaya further describes stacking up multiple layers of similar modules to form a multi-layered structure, where “any number of layers [of similar configuration] can be formed depending on the design.” APPLE-1007, [0225] (“Although FIG. 9A shows the circuit component built-in module 900 having a three-layered structure, a structure having any number of layers can be formed depending on the design.”), FIG. 9A (reproduced below); *see also*, [0004] (“In recent years, with the demand for high performance and miniaturization of

FIG. 9A

APPLE-1007, FIG. 9A (Annotated)

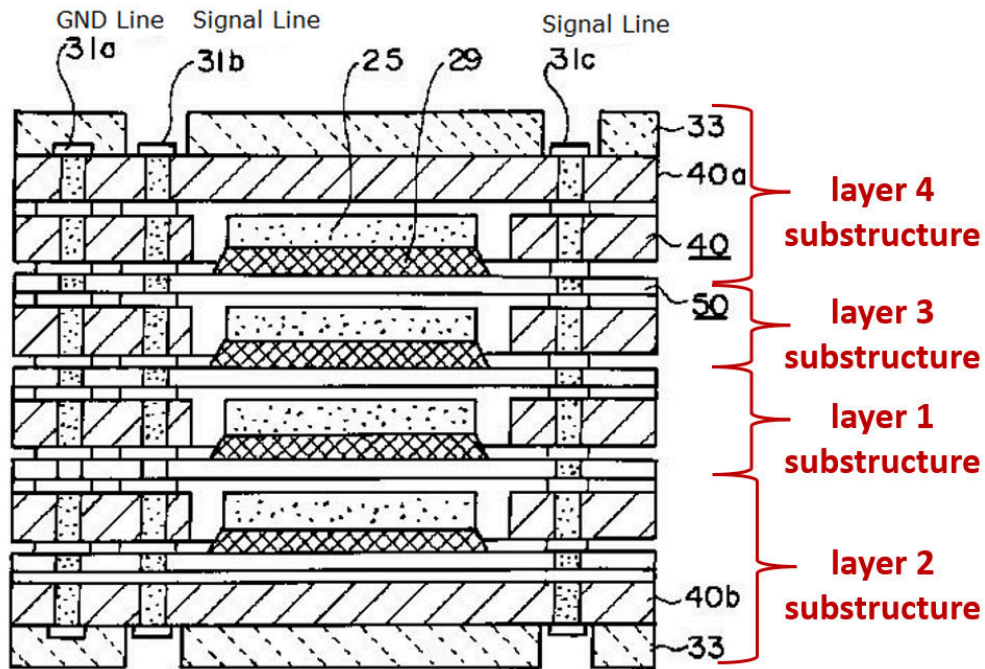
E. Overview of Imoto

85. JP Patent Application Publication No. 2001-068624A to Imoto is titled “Semiconductor Device and Semiconductor Device Manufacturing Method.” APPLE-1016, Face. Imoto was filed August 26, 1999 and published March 16, 2001. *Id.*

86. Imoto describes providing “a semiconductor device using a stacked package” with a semiconductor element 5 embedded in a chip cavity portion 12 of each of a plurality of stacked wiring substrates and electrically connected to the wiring. APPLE-1016, Abstract. Imoto thus teaches a stack-up multi-layered structure with each substructure layer having similar configurations. *Id.*, FIGS. 5-9 (and related descriptions).

87. Imoto makes clear in describing its first embodiment having four stacked semiconductor elements that, “the number of semiconductor elements to be stacked is not limited to the four in the present invention. Any number equal to or greater than two can be stacked.” *Id.*, [0010]; *see also*, cls, 1 (“a plurality of these stacks are stacked and integrated with the semiconductor element mounted on the wiring substrates completely housed inside the chip cavity portion”), 2, 8. The annotated FIG. 8 below shows layer 1 to layer 4 substructures stacked on top of each other.

[FIG. 8]



APPLE-1016, FIG. 8 (Annotated)

88. Imoto further describes that the multiple layers of these stacks are electrically connected to each other. *See e.g.*, cl. 8 (“forming vias that pass through the plurality of stacks while stacked, and forming connecting electrodes in these vias”), [0009], [0019], [0022] (“The connecting electrodes 31 connected to each semiconductor element 25 via wiring are formed inside the vias of the stack. The connecting electrodes 31 include connecting electrodes 31a that connect to the ground (GND) line, and connecting electrodes 31b, 31c that connect to signal lines”).

89. As also shown in FIG. 8 “metal film 33” formed on the conductive-via stacked substrates 40a, 40b in the upper and lower layers, “formed by sputtering or is metal foil,” “is electrically connected to the connecting electrodes 31a, which are connected to the ground line, and is not in contact with the connecting electrodes 31b, 31c that are connected to signal lines.” *Id.*, [0022]. Imoto explains that metal film 33 “has a shielding effect when connected to the ground line. This effect can be altered by adjusting the material used and the thickness of the metal film, or the material used and width of the connecting electrodes, as needed.” *Id.*

VIII. GROUND 1A: CLAIMS 12-21, 23-27 ARE OBVIOUS IN VIEW OF MCCORMACK

90. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art cited herein, claims 12-21 and 23-27 are rendered obvious by McCormack.

A. Analysis of McCormack with Respect to Claims 12-21, 23-27

[12pre] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:

91. McCormack provides [12pre]. McCormack discloses a multi-layered circuit board which includes at least two circuit board substructures on top of each other. For example, McCormack describes “a circuit apparatus and a method for embedding electronic components within multi-layer substrates, particularly

printed circuit boards.” *E.g.*, APPLE-1005, [0002]; *see also* Abstract, [0009]-[0012], [0029], FIGS. 9, 12, 13, cls. 1, 17, 35; *infra*, analysis of claims [13] and [17]. This is similar to the ’909 patent’s description. APPLE-1001, 1:63-67 (“The invention is based on embedding the semiconductor components, or at least some of them, in a base, such as a circuit board.”).

92. McCormack additionally describes “dielectric build-up” of multiple layers of its printed circuit board assembly such as in FIG. 9, “by means well known to those skilled in the art (e.g., post plating for stacked via build-up structures).” APPLE-1005, [0032]. Based on my knowledge and experience in the field, I note that the multi-layered structure through staking up multiple layers of circuit-board substructures on top of each other and mounting multiple electronic components in the same and different substructure layers, in accordance with McCormack’s suggestions, was a well-known common feature in the component built-in devices by the Critical Date, to achieve benefits such as high density, high performance, and short-distance wiring. A POSITA would have been motivated to stack multiple layers on top of each other in order to achieve known benefits of high-density, improved performance, reduced manufacturing cost, space saving, and short-distance wiring.

93. For example, Sugaya (U.S. application publication No. 2001/0030059, filed December 15, 2000), corroborates the POSITA’s knowledge of this known

configuration. Sugaya relates to a circuit component built-in module capable of mounting the circuit component with high density and having high heat releasing property and high reliability. APPLE-1007, Abstract, [0004] (“In recent years, with the demand for high performance and miniaturization of electronic equipment, high density, high performance and short-distance wiring of a circuit component have been desired increasingly. Accordingly, a wiring substrate capable of including a high density, high-performance and short-distance wiring circuit component has been demanded. The formation of a multi-layer circuit may be a solution to attain a higher-density wiring substrate.”), [0034] (“it is preferable in the configuration that the wiring substrate includes one or a plurality of circuit component built-in modules... it is possible to realize a highly reliable multilayer circuit component built-in module in which the circuit components are mounted with high density.”).

94. Sugaya describes an example circuit component built-in module having a three-layered structure. APPLE-1007, [0217], [0225] (“Although FIG. 9A shows the circuit component built-in module 900 having a three-layered structure, a structure having any number of layers can be formed depending on the design.”), FIG. 9A (reproduced below showing a three-layered structure with circuit components 908a, 908b and 908c embedded in the various substructure layers).

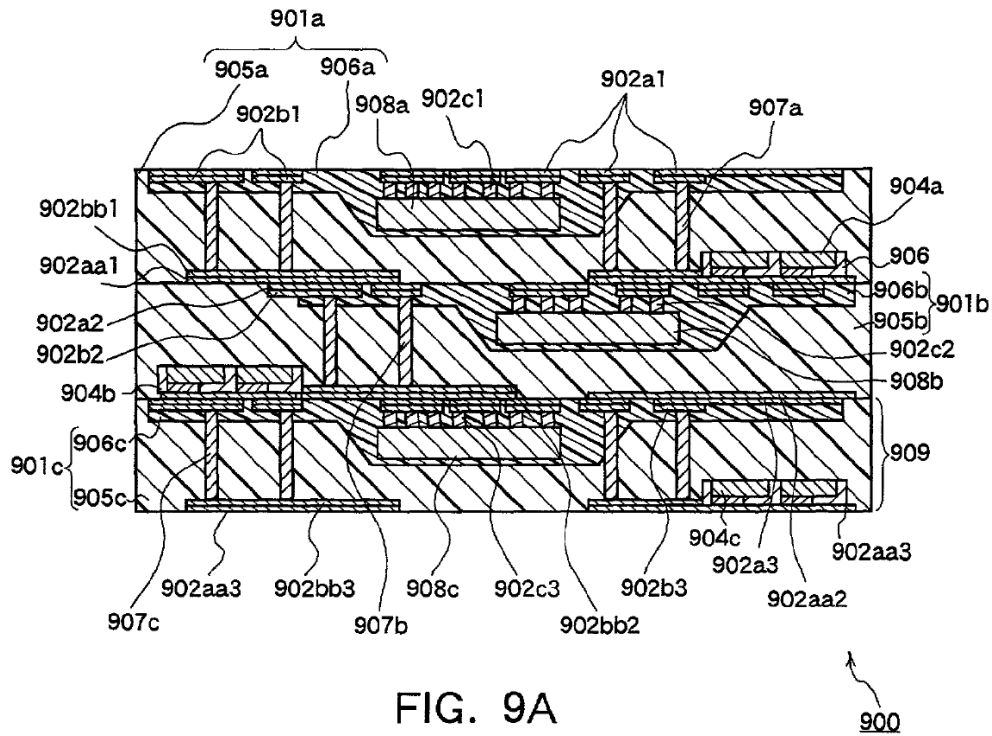


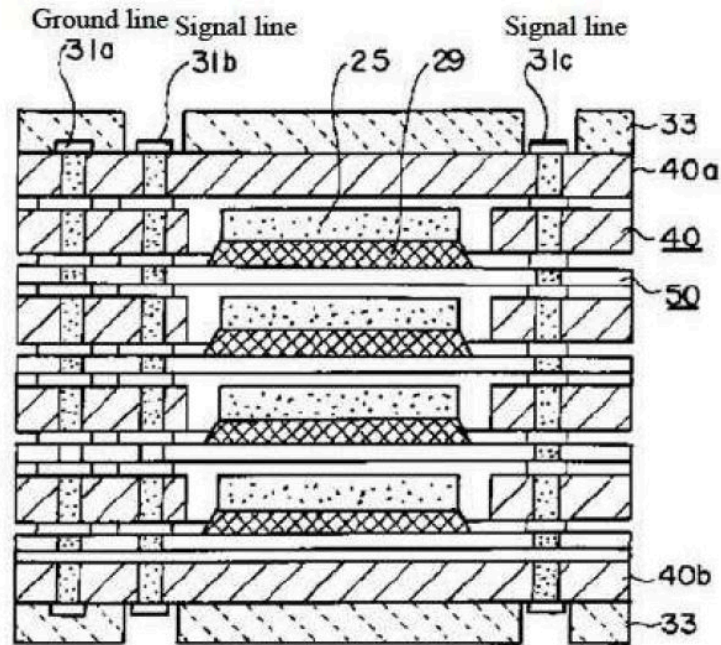
FIG. 9A

APPLE-1007, FIG. 9A

95. Another example as corroborating evidence of the POSITA's knowledge, prior art Imoto (JP patent application publication No. 2001-068624, published March 16, 2001) describes a semiconductor device having a multi-layered structure that includes any number of layers. *E.g.*, APPLE-1016, [0010] ("This embodiment is an example of four laminated semiconductor elements, but the number of semiconductor elements to be laminated is not limited to four, as in the present invention. Any required number of two or more can be laminated."), FIGS. 5-9; *see also* cls. 1, 2, 8 (reciting "a plurality of wiring substrates" and "plurality of conductive via insulating substrates"). FIG. 8 below shows a four-

layered structure with a semiconductor element 25 embedded in each substructure layer. *Id.*, [0021].

FIG. 8

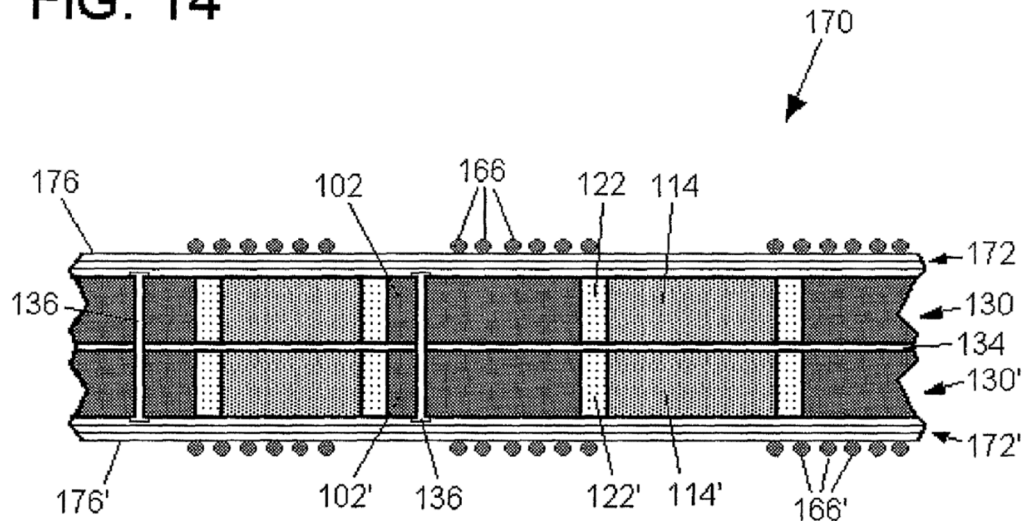


APPLE-1016, FIG. 8

96. Yet another prior art example as corroborating evidence is Vu (U.S. patent application publication No. 2002/0020898, filed on June 18, 2001 and published on February 21, 2002). APPLE-1008, Face. Vu describes microelectronic substrates with a plurality of microelectronic devices encapsulated in each microelectronic substrate core. *E.g.*, APPLE-1008, [0019]-[0027] (short descriptions of FIGS. 9-17 showing a “dual substrate assembly”), [0045]-[0057], FIGS. 9-17. For example, FIG. 14 reproduced below illustrates a plurality of

microelectronic devices 114 and 114' embedded in each of the two substrate layers (130 and 130') of a dual substrate assembly.

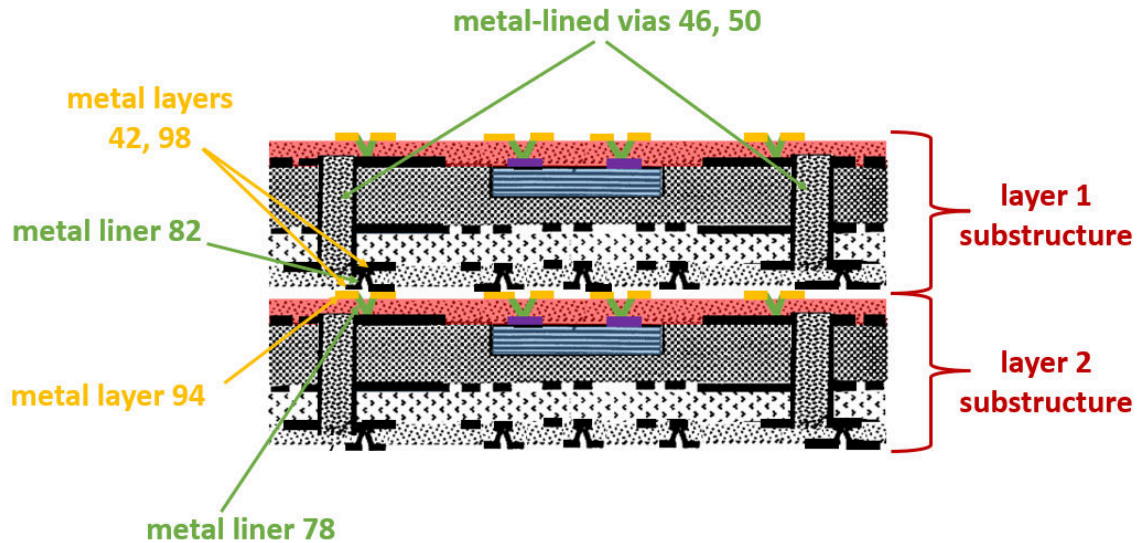
FIG. 14



APPLE-1008, FIG. 14

97. This was further highlighted during original prosecution, where the examiner concluded regarding this multi-layered feature, “it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and a second circuit board substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.” APPLE-1002, 107-110. The applicant did not dispute the examiner’s conclusion. APPLE-1002, *generally*. An example resulting stack-up of such a “multi-layered” structure is shown below, with two circuit board substructures annotated as “layer 1 substructure” (i.e. substructure 1, which contains one or more layers) and “layer 2

substructure” (i.e. substructure 2, which contains one or more layers). *See also*, *infra*, analysis of claims [13] and [17].



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[12a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

98. McCormack provides element [12a]. McCormack provides an insulating material layer including a baseboard (e.g., core substrate 12) and a hardened insulating polymer layer (e.g., dielectric layer above the core substrate). For example, McCormack’s “circuit board substrate” or “core substrate” 12 and one or more “dielectric layer[s]” above the core substrate 12, having integrated electronic components embedded therein, together provide an insulating material layer, as claimed. *See e.g.*, APPLE-1005, Abstract, [0009]-[0011], [0026], [0029], [0032]-[0033] (“Suitable dielectric material for the core 12 ... and/or dielectric layers 30, 32, 60 and 64 include B-stage polymeric compounds, such as

polyimides, epoxy resins, polyurethanes or silicones, well known to those skilled in the art. ...”), cls. 1, FIG. 9, 17, 35.

99. McCormack discloses element [1a] in a second manner, where optional additional dielectric layers below the core substrate 12, such as “dielectric layer 32,” or “dielectric layers 32 and 64,” along with the core substrate 12 and the dielectric layer(s) above the core substrate 12, collectively provide an insulating material layer.

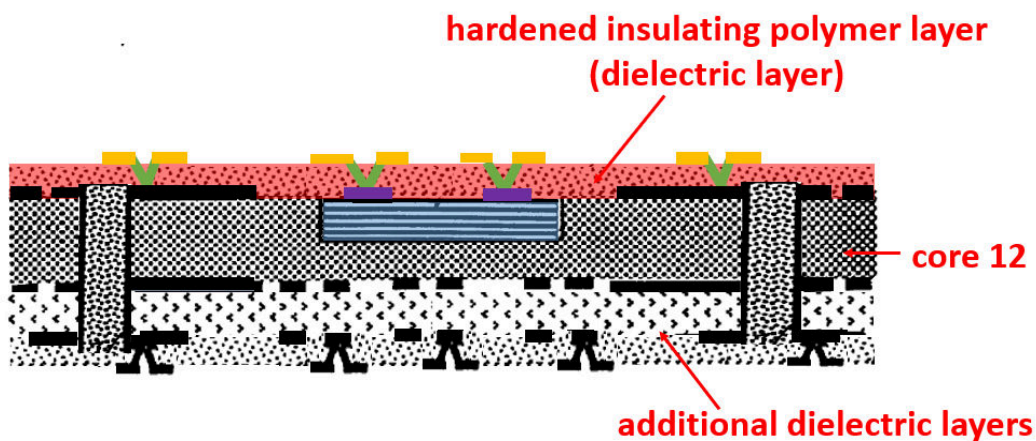
100. McCormack’s core substrate 12 (either by itself or together with dielectric layers 32, 64 below it) provides the recited baseboard. APPLE-1005, [0009], [0024]-[0026], FIGS. 12-13. McCormack describes that each of its dielectric layers, including the core substrate 12, are made of materials typical of a circuit board baseboard, such as epoxy. APPLE-1005, [0033] (listing a large variety of “[s]uitable dielectric material for the core 12 ... and/or dielectric layers 30, 32, 60 and 64 include B-stage polymeric compounds, such as polyimides, epoxy resins, ... thermosetting materials, such as high glass transition anhydride-cured epoxy composition. More particular suitable thermoset materials include, but are not limited to, one or more compounds selected from group consisting of epoxies and modified epoxies...”). The ’909 patent similarly describes its baseboard as “epoxy board,” an “organic board,” or “an inorganic board.” APPLE-1001, 3:48-57 (“The baseboard 1 can be, for example, a glass-fibre

reinforced epoxy board. ... A flexible and cheap organic board can thus be selected. ... Of course, an inorganic board can also be used.”).

101. Moreover, McCormack’s core substrate 12 is used to house an integrated electronic component (e.g., integrated circuit components 20). *See e.g.*, APPLE-1005, Abstract, [0009], cl. 1 (“A method for producing a circuit board having an integrated electronic component...”). I note that this construction is also like the ’909 patent’s description for its baseboard. *E.g.*, APPLE-1001, 2:22-26 (“With the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it.”), 3:23-33.

102. McCormack provides a hardened insulating polymer layer (e.g., dielectric layer above the core 12). For example, McCormack describes dielectric layer(s) (e.g., dielectric layers 30 and 60) “placed, flowed or laminated over the integrated circuit component 20” and over the upper surface of core 12. APPLE-1005, [0030]-[0032]. Based on my knowledge and experience in the field, and my review of McCormack, a POSITA would have found obvious from McCormack’s descriptions that one, two, or more than two dielectric layer(s) (along with their associated metal layer(s)) can be used above and/or below the core substrate 12, to provide an integrated electronic component in accordance with McCormack’s teachings. APPLE-1005, [0009] (“The method may also comprise...”), [0030]-[0032], [0035]. I note that, a POSITA would have been motivated to use a single

dielectric layer, for example, when implementing a circuit board having an embedded “integrated electronic component” in accordance with McCormack’s teachings, in order to provide a space-efficient design having reduced thickness (for a more compact design) and enhanced manufacturing efficiency, as it would involve fewer processing steps. I further note that a POSITA would have recognized that with the component positioned in a hole in the core substrate 12, a single dielectric layer effectively covers the component to provide a planar surface, without the need for an intermediate dielectric layer (e.g., before applying a second dielectric and a metal layer on the second dielectric). The annotated composite figure below illustrates the resulting configuration, with a single dielectric layer placed above the integrated circuit component 20 and the upper surface of the core substrate 12.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

103. McCormack’s dielectric layers are made of insulating material containing “polymeric compounds.” APPLE-1005, [0032]-[0033] (suitable

dielectric materials for dielectric layers “include B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicones, well known to those skilled in the art ... thermosetting materials, such as high glass transition anhydride-cured epoxy composition... high temperature thermoplastic materials ... and the like, and mixtures of any of the foregoing”).

104. McCormack further describes “curing” the dielectric layers upon “exposure to heat and pressure” at a “subsequent heating step.” *Id.*, [0033]. A POSITA would have recognized that the dielectric layers, including the dielectric layer above the core substrate 12, are thus hardened through this curing process. I note that this is consistent with the ’909 patent’s description of hardening a polymer layer through curing. APPLE-1001, 5:32-35 (“The polymer film 7 is hardened with the aid of curing. Curing generally comprises a heat treatment, but the process can also employ some treatment other than heat to harden the polymer.”). Alternatively, a thermoplastic with high glass transition temperature becomes rigid, thus hardened, when it cools from above to below its glass transition temperature.

105. I note that even if McCormack did not expressly describe the recited baseboard, which it does, a POSITA would have been prompted to utilize a glass fiber epoxy material. For example, a POSITA would have been motivated to use glass-fibre reinforced epoxy resin for McCormack’s core substrate 12, to facilitate

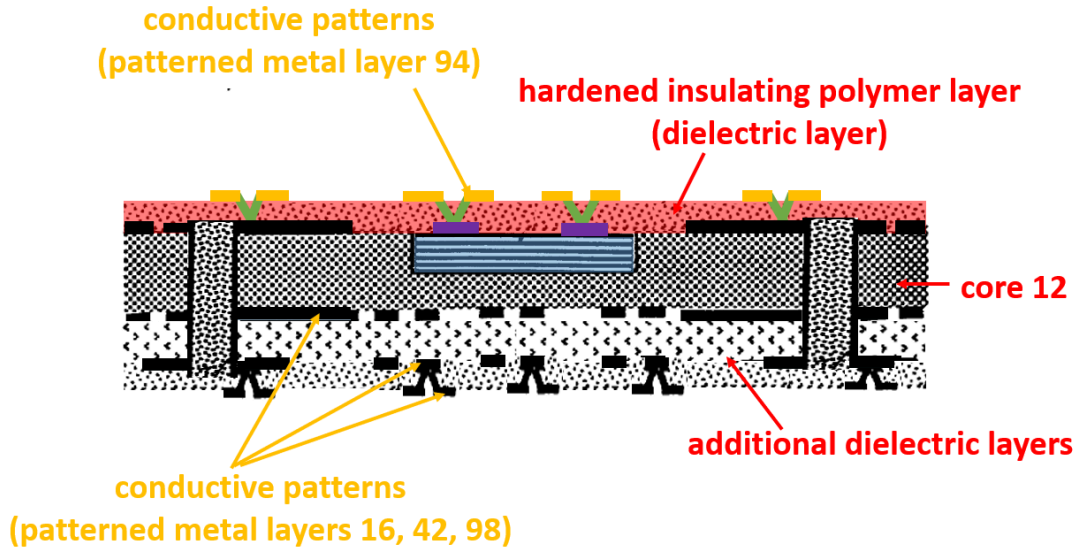
enhanced strength, as glass-fibre reinforced epoxy boards were both well-known in the art and known to have high strengths. APPLE-1004 (corroborating prior art), [0012] (suitable materials for a core substrate used to incorporate electronic components such as IC chips “include epoxy resins, BT resins, and phenol resins impregnating a reinforcing material such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin. However, any material generally used in printed wiring substrates can be used.”), [0023] (“an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as glass cloth has been impregnated with a resin such as an epoxy is used as the starting material”); APPLE-1006 (corroborating prior art), 3:59-64, 15:62-16:2 (“A component built-in module takes a board form, and the electric insulation layer... may be made of an insulating resin, a mixture of a filler and an insulating resin, or the like. It may contain a reinforcing material such as a glass cloth or an unwoven fabric.”), cls. 11, 21; APPLE-1011, [0015]-[0016] (corroborating). Such modification would have amounted to a simple substitution of one known element for another.

[12b] conductive patterns on both sides of the insulating material layer;

106. McCormack provides element [12b]. McCormack provides conductive patterns (e.g., metal layer 94 on the upper side and metal layer 16, 42, or 98 on the lower side) of the insulating material layer. For example, McCormack

describes a metal layer (e.g., metal layer 94) on the upper side of its circuit board, “disposed in” a dielectric layer, and a metal layer (e.g., “patterned metal layer 16”) on the lower side of the circuit board. APPLE-1005, [0032]; *see also* [0021], [0026] (“Metal layers 14 and 16 are optional, and may be any suitable conductive metal, such as copper.”). These metal layers are patterned. *Id.*, [0027] (“metal layers ... may be appropriately patterned with any suitable photoresist to respectively, selectively expose substrate surfaces... Patterning of the metal layers ... may be accomplished by etching to develop the desired patterned metal profile. ... such as by [a list of etching techniques]”), [0030]-[0031], FIGS, 7-9.

107. In the second manner that McCormack provides the claimed insulating material layer, as I previously discussed in the analysis of element [1a] (§VIII.A), in which the core substrate 12 and one or more dielectric layers above and below core substrate 12 in combination provide the recited insulating material layer, patterned metal layer 42 and/or patterned metal layer 98 also provides the recited conductive patterns on the lower side of the insulating material layer. The annotated composite figure below illustrates this configuration, with patterned metal layers 94, 16, 42, 98 on both sides of the insulating material layer.

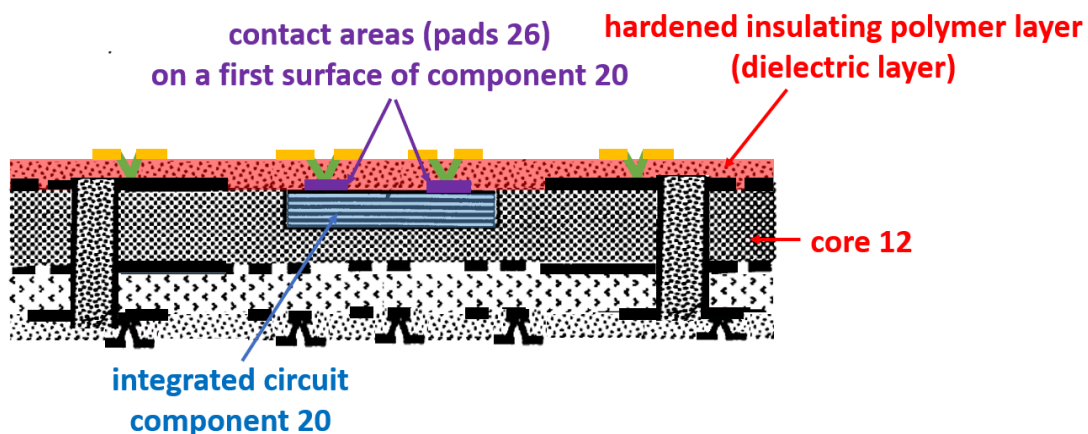


Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[12c] at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and

108. McCormack provides element [12c]. McCormack provides at least one microcircuit (e.g., “e.g., “at least one integrated electronic component” or “integrated circuit component” 20) embedded in the insulating material layer (e.g., embedded in “cavity 24” of the core substrate 12), the embedded microcircuit having contact areas (e.g., “conductor pads 26”) on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer (e.g., dielectric layer above core 12). For example, McCormack describes “at least one integrated electronic component” or “integrated circuit component” 20 embedded in a cavity in the core substrate. *See e.g.*, APPLE-1005, Abstract,

[0009], [0028] (“one or both of the substrate surfaces 12a and 12b may have a cavity generally illustrated as 24 in FIG. 12. ... The prefabricated, integrated circuit component 20 (e.g., resistors, capacitors, inductors, etc.) may be conveniently disposed in the cavity 24, as shown in FIG. 13.”). McCormack explains that integrated circuit component 20 has contact pads on its active surface (the recited first surface). *See e.g., id.*, [0021], [0029] (“The integrated circuit component 20 may include one or more conductor pads 26 and may be any suitable integrated circuit component 20...”), [0032], cls. 11, 25. As I previously discussed in the analyses of elements [12a] and [12b], the dielectric layer over the core substrate is also over the embedded integrated circuit component 20, thus, the first surface of the component is against the hardened insulating polymer layer. *See also*, APPLE-1005, [0030]-[0032]. The annotated composite figure below illustrates this configuration.



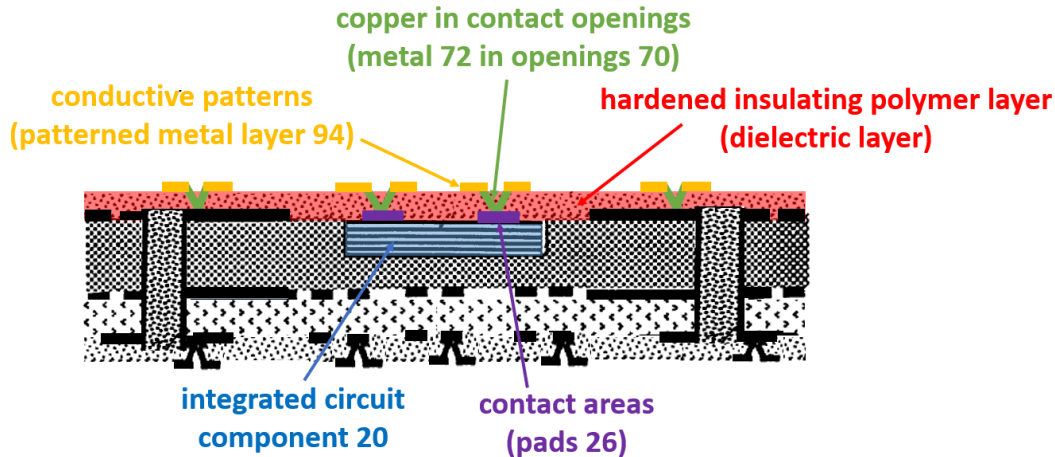
Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

109. Based on my knowledge and experience in the field, a POSITA would have understood that integrated circuit components are a type of microcircuit, as microcircuits are miniaturized electronic circuits that contain a network of interconnected semiconductor devices (e.g., transistors and diodes) and passive components (e.g., resistors, inductors, and capacitors), on a small substrate, and integrated circuits are essentially advanced microcircuits where all these components are fabricated onto a single semiconductor wafer.

[12d] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

110. McCormack provides element [12d]. McCormack's system includes contact openings in the hardened insulating polymer layer (e.g., dielectric layer over the component) and copper in the contact openings (e.g., "metal 72" made of copper in "openings 70") for forming electrical contacts between the contact areas (e.g., "pads 26") of the microcircuit and the at least one of the conductive patterns (e.g., metal layer 94), wherein the copper contains at least one of electrochemically deposited copper (e.g., "electrolytic plating") and chemically deposited copper (e.g., "e-less" plating). For example, McCormack describes forming "openings," such as by laser drilling or the like, through the dielectric layer(s) above the integrated circuit component, "to expose pads 26 of the integrated circuit

component 20.” APPLE-1005, [0032], FIG. 9. McCormack explains that “[o]penings 70 are then metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26.” *Id.*; *see also*, Abstract (“producing in the integrated electronic component assembly at least one via having a metal lining in contact with the metallic layer... At least one metal-lined opening is formed in the [dielectric layers above the component] to expose at least part of the integrated electronic component, and to couple the metal lining of the opening to the first integrated electronic component”), [0009]-[0011], [0021], cls. 1 (“a metal lining in said opening and coupled to the first integrated electronic component”), 12 (“at least one first pad in contact with said metal lining in said opening”), 17, 35, FIG. 9 (showing metal 72 connected with metal layer 94 and pads 26 on the component). Thus, metal lining 72 is electrically connected to conductor pads 26 (the recited contact areas) of the integrated circuit component 20 and metal layer 94 (the recited conductive patterns). *Id.* The annotated composite figure below illustrates this configuration, showing metal 72 in the openings 70 (in the dielectric layer above the integrated circuit component 20) connecting both the pads 26 on the component 20 and the patterned metal layer 94 on the dielectric layer above the component.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

111. Based on my analysis of McCormack, I note that even if McCormack's description did not indicate this, a POSITA would have predictably implemented the metal 72 to form electrical contacts between the pads of the component and the patterned metal layer on the dielectric layer that is over the component. Based on my knowledge and experience in the field, and my analysis of McCormack, a POSITA would have understood, and found obvious that when the integrated circuit component 20 is embedded in a cavity 24 in the core substrate 12 (as illustrated in e.g., FIGS. 12-13), and a single dielectric layer is provided above the core substrate 12 (and the embedded component), the metal 72 of openings 70 (the recited copper in the contact openings) likewise penetrates through that dielectric layer (thus in the recited hardened insulating polymer layer), in order to expose pads 26 of the component for forming electrical contacts between pads 26 (the recited contact areas) of the component and metal layer 94 (the recited at least one of the conductive patterns) on the dielectric layer over the

core substrate. I note that a POSITA would have been motivated to do so to achieve the objective of thereby electrically connecting the component with the metal layers of the circuit board, which McCormack expressly states. *See e.g.*, APPLE-1005, Abstract, [0032], FIG. 9, cl. 1

112. McCormack explains that metal lining 72 made of copper in the contact openings 70 (the recited copper in the contact openings) is accomplished “by the combination of e-less and electrolytic plating.” APPLE-1005, [0032]. A POSITA would have recognized that “electrolytic plating” is an electrochemical plating technique, and that “e-less” (short for electroless) plating is a chemical plating technique. In electrolytic plating, an electric current drives a chemical reaction to deposit a layer of metal onto a conductive surface. This process involves immersing the object to be plated (the cathode) and another conductor (the anode) in an electrolyte solution containing metal ions. Unlike electrolytic plating, e-less or electroless plating does not require an external electric current to deposit metal onto a surface. Instead, it relies on a chemical reaction that occurs between the plating solution and the object to be plated.

[13] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

113. McCormack renders obvious claim [13]. In the multi-layered structure illustrated above in the analysis of element [12pre] (§VIII.A), layer 1

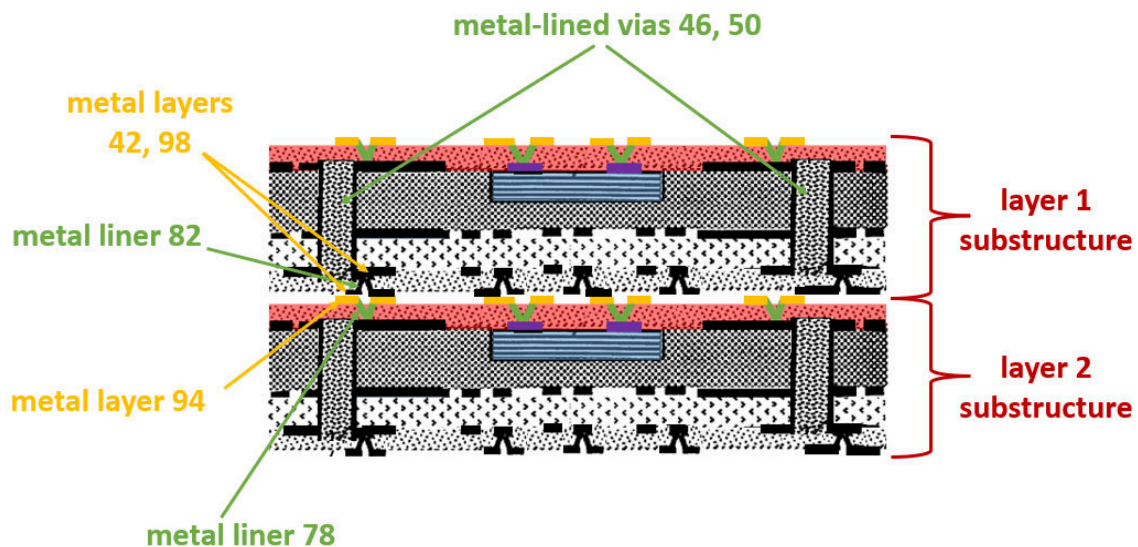
substructure and layer 2 substructure (the recited at least two circuit board substructures on top of each other) are electrically connected to each other to form a multi-layered functioning totality (e.g., through the metal layers on the surfaces of and within each substructure layer (e.g., metal layers 94, 98, 42, 14, 16, and 12c), metal lined openings (e.g., metal liners 78 and 82 of openings 76 and 80) and metal lined vias (e.g., vias 18, 46 and 50) of each substructure layer. For example, McCormack describes “metal-lined vias 46 and 50” functioning as conductive feed-throughs “formed by drilling openings through the entire FIG. 5 circuit board assembly,” these metal-lined vias provide electrical connection between the metal layers below the component (e.g., patterned metal layer 16, 42, or 98) and the metal layer above the component (e.g., patterned metal layer 94). APPLE-1005, [0031]. For example, the “openings pass[] through metal layers 40 and 42, through dielectric layers 30 and 32, through residual metal layers remaining from patterned metal layers 14 and 16, and through the core 12.” *Id.*, [0031] (“The opening for vias 46 and 50 are metal-lined (e.g., copper lined) with metal liners 46a and 50a by any suitable process, such as by e-less plating in combination with electrolytic plating, well known to those skilled in the art. Metal liners 46a and 50a are preferably respectively formed such as to be in electrical contact with residual metal layers remaining from patterned metal layers 14 and 16...”); *see also id.*, [0009] (“at least one via passing through the circuit board from the first substrate

surface to the second substrate surface”), [0018]-[0019] (“a pair of blind metal-lined vias”), [0020]-[0022], [0026] (core substrate assembly ... may also have one or more conducting-through vias, generally illustrated as 18 in FIG. 10”), FIGS. 6-10; *see also*, [0031] (additional electrical connection mechanisms such as “one or more metal-lined blind vias 54 and 58 ... in electrical contact with... metal layers 14 and 16”). A POSITA would have understood, and found obvious, that when a single dielectric layer is used above the core substrate, these metal-lined vias pass through metal layer 14 on the top surface of the core substrate, through the core substrate and dielectric layer 30, and through metal layer 16, in accordance with McCormack’s teachings.

114. Additionally, McCormack describes metal-lined openings within dielectric layers exposed to the surfaces of the circuit board, where the metal-lined vias do not pass through, to make electrical connections between metal layers on both sides of each of such dielectric layers. *See e.g., id.*, [0032] (“In addition to openings 70, a plurality of additional openings 76 and 80 may be respectively formed through respective dielectric layers 60 and 64, down to residual metal layers(s) remaining from patterned metal layers 40 and 42, respectively. Openings 76 and 80 are then metal-lined by any conventional process to respectively dispose metal liners 78 and 82 in openings 76 and 80. Subsequently metal layers 94 and 98 may be disposed in dielectric layers 60 and 64 and patterned, such that residual

metal layers 94 and 98 are respectively coupled to residual metal layers 40 and 42, respectively, by and through metal liners 78 and 82.”); *see also* Abstract, [0009]-[0011] (“At least one metal-lined blind via may be formed through the metallic layer, through the first dielectric layer and coupled to the metallic layer”), FIG. 9.

115. The annotated composite figure below illustrates the multi-layered structure configuration, where two circuit board substructures (layer 1 substructure and layer 2 substructure) are stacked on top of each other and electrically connected to each other.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[14] The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.

116. McCormack provides claim [14]. As I previously discussed in the analysis of claim [12] (§VIII.A), McCormack describes a stacked multilayer structure with one or more integrated circuit components (the recited microcircuits)

in the same and/or different substructures. APPLE-1005, [0029]-[0030], [0032]. I note that McCormack expressly describes the “circuit board having at least one integrated electronic component,” thereby disclosing at least two microcircuits inside the insulating material layer. *Id.*, *see also* [0010]-[0011], [0030] (“one or more of the integrated circuit components 20 have been suitable [*sic*] disposed where desired”), cls. 1, 11 (“a second integrated electronic component”), 17, 35, FIG. 11.

117. Furthermore, McCormack also incorporates by reference U.S. Patent No. 5,564,181 to Dineen, et al., teaching mounting “a plurality of electronic components” in “a plurality of holes” on a flat substrate. *Id.*, [0007] (“a method of fabricating a laminated substrate assembly chips-first multichip module including mounting a plurality of electronic components having a predetermined thickness to a flat substrate in a precise position and orientation”).

118. Even if McCormack did not expressly describe at least two integrated circuit components inside its dielectric layers (including core 12) of the circuit board assembly, based on my knowledge and experience in the field, a POSITA would have found this conventional configuration to be obvious based on McCormack’s suggestions.

119. For example, U.S. Patent No. 6,297,551 to Dudderar et al., titled “Integrated Circuit Packages with Improved EMI Characteristics,” filed September

22, 1999 and issued October 2, 2001, Vu (previously discussed in the analysis of [12pre]), and Eiji, all corroborate that it was a common practice and well known in the field to POSITA to embed a plurality of microcircuits in an insulating material layer/substrate. *See e.g.*, APPLE-1008, [0044], [0045], [0047], [0053], [0054], FIGS. 1-7, 9-21; APPLE-1014, 1:15-16, 2:44-46, 4:66-5:3, FIGS. 1, 2; APPLE-1012, Abstract (“a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded”), [0006] (“Note that the electronic components include, but are not limited to, passive components such as capacitors, inductors, filters, and resistors, and active components such as low-noise amplifiers (LNAs), transistors, semiconductor devices, and FETs, as well as SAW filters, LC filters, antenna switch modules, couplers, and diplexers, and any of the components listed above made into chip form. Different types of electronic components can be embedded together in the same through-hole or recessed portion.”), FIG. 1.

120. McCormack already describes use of multiple components. Based on my knowledge and experience in the field, a POSITA would have recognized the predictable benefits of positioning two or more components inside the insulating material layer to achieve the functionality of multiple components and/or to maintain a compact overall profile while doing so. Moreover, a POSITA would have had a reasonable expectation of success in doing so. This is especially true in

view of McCormack's express suggestion for incorporating multiple components, and implementation of multiple components in an insulating material layer was already known. Again, Dudderar, Vu, and Eiji, as corroborating prior art, already demonstrate this configuration to be successful. *See e.g.*, APPLE-1008, [0044], [0045], [0047], [0053], [0054], FIGS. 1-7, 9-21; APPLE-1014, 1:15-16, 2:44-46, 4:66-5:3, FIGS. 1, 2; APPLE-1012, Abstract, [0006], FIG. 1.

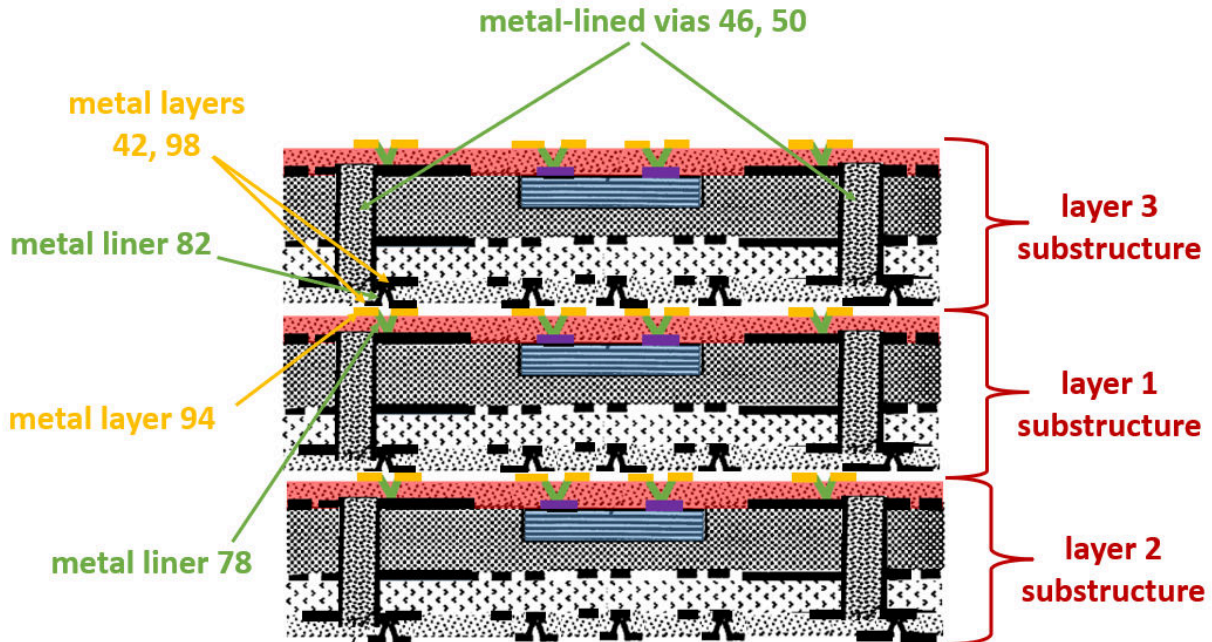
[15] The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.

121. McCormack provides claim [15]. As I previously discussed in the analyses of [12pre] and claim [14] (§VIII.A), McCormack describes a plurality of integrated circuit components electrically connected to each other in each circuit board substructure. Based on my knowledge and experience in the field and my review of McCormack, a POSITA would have understood and found obvious that such integrated circuit components of each substructure described by McCormack include at least one memory circuit, as memory circuit is a common type of integrated circuit used to store data in semiconductor devices used in computers, smartphones, embedded systems, and other electronic devices. APPLE-1011, [0038] (corroborating prior art, describing “a silicon semiconductor memory chip” as an example for electrical elements embedded in an insulating substrate), APPLE-1004 (corroborating prior art, describing “cache memory” as an example for “IC chip 120”), [0006], [0068], [0070]. I note that, based on my knowledge

and experience in the field and my review of McCormack, a POSITA would have been prompted to utility a semiconductor component that included a memory circuit, in order to impart memory functionality, if not already present. A POSITA would have recognized the predictable benefit of expanding the functionality and potential use cases of the resulting device by doing so.

[16] The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.

122. McCormack renders claim [16] obvious, for at least the same reasons as I previously discussed in the analysis of element [12pre] and claim [13]. The annotated composite figure below illustrates such a configuration with three similar circuit board substructures (e.g., layers 1-3) stacked on top of each other and electrically connected to each other, through the metal layers on the surfaces of each substructure layer, which are further connected through additional metal layers within each substructure, and metal-lined openings and metal-lined vias of each substructure.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

123. I note that, based on my knowledge and experience in the field, and my review of McCormack, adding one or more additional layer substructures amounted to duplication of parts, such as by duplicating a layer substructure and electrically connecting it on top of a lower substructure, using known techniques.

[17pre]-[17d] The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise an insulating material layer including a baseboard and a hardened insulating polymer layer, conductive patterns on both sides of the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

124. McCormack renders obvious elements [17pre]-[17d] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d].

Supra, §VIII.A. I note that the resulting device includes two substructures that each have similar features, as I discussed above.

[18] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.

125. McCormack renders obvious claim [18] for at least the same reasons as I discussed previously in the analyses of claims [13] and [16]. *Supra*, §VIII.A.

[19pre]-[19d] The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, conductive patterns on both sides of the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

126. McCormack renders obvious claim [19] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d] and claim [18]. *Supra*, §VIII.A.

[20pre]-[20d] The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises an insulating material layer including a baseboard and a hardened insulating polymer layer, a conductive pattern on the insulating material layer, at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts

between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

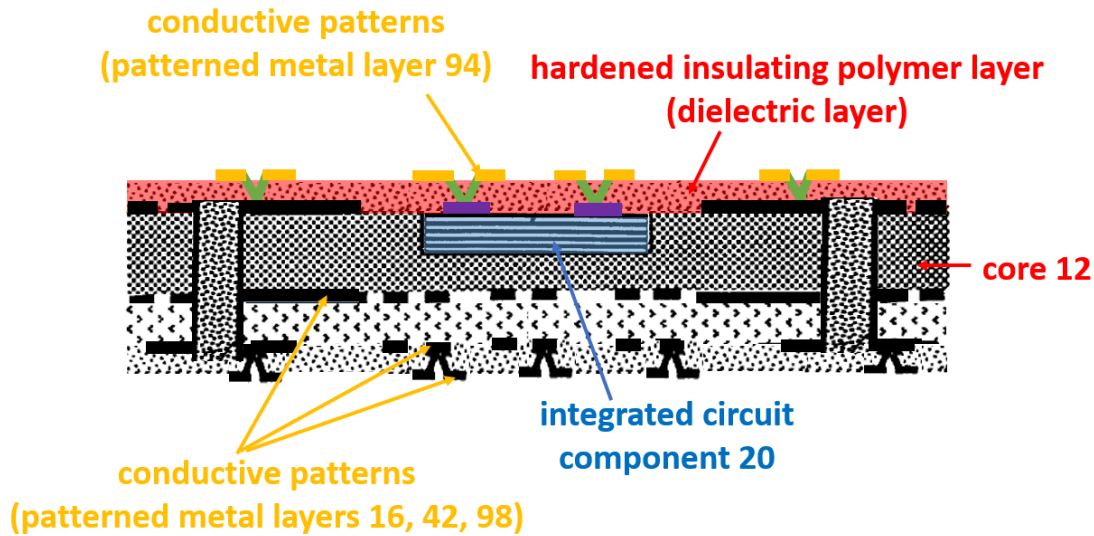
127. McCormack renders obvious claim [20] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d] and claim [19]. *Supra*, §VIII.A.

[21] The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.

128. McCormack renders claim [21] obvious for at least the same reasons as I discussed previously in the analyses of element [12a], regarding McCormack's dielectric layers containing "epoxy resins," and claim [20]. *Supra*, §VIII.A.

[23] The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.

129. McCormack renders claim [23] obvious for at least the same reasons as I discussed previously in the analyses of elements [12b]-[12c] (§VIII.A). The annotated composite figure below illustrates this configuration, with integrated circuit component 20 (the recited at least one microcircuit) positioned between patterned metal layer 94 and patterned metal layer 16 (and 42, 98) (the recited conductive patterns on both sides of the insulating material layer).



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

130. McCormack renders obvious claim [24]. As I previously discussed in the analysis of element [12d] (§VIII.A), metal liner 72 made of copper in the contact openings 70 (the recited copper in the contact openings) is accomplished “by the combination of e-less and electrolytic plating.” APPLE-1005, [0032]. The e-less plating layer provides the recited first layer of chemically deposited copper, and the electrolytic plating provides the recited second layer of electrochemically deposited copper on the first layer of chemically deposited copper. That is, a POSITA would have been prompted, based on McCormack’s description, to apply the copper layers such that the electrochemically deposited copper is applied to thicken the chemically deposited copper. This conventional technique is further

corroborated by Sakamoto. APPLE-1004, [0028]; *see also*, Abstract, [Claim 4], [0007], [0008] (“The transition layer is formed of two or more metal layers”), [0009], [0010], [0014] (“the transition layer can be thickened by electroplating”), [0015] (“When the transition layer is formed by a subtractive process, the metal film is thickened by electroless or electrolytic plating. Types of plating that can be formed include copper, nickel, gold, silver, zinc, and iron. Copper is preferably used from the standpoint of electrical properties, economy, and the fact that the conductor layer, which is a build-up formed later, is composed primarily of copper.”), [0018], [0020]-[0021], [0027] (“Plated film 36 may be formed on the metal film 33 by electroless plating (FIG. 2(B))... Copper is preferably used...”), [0028] (“electrolytic plated film [37] on the electroless plated film 36”), [0031] (“transition layer 38 made of copper”), [0035], [0067], [0069], [0070], [0071], FIG. 2 APPLE-1004 as corroboration). I additionally note that a POSITA would have recognized essentially two orders of e-less plating followed by electrolytic plating or electrolytic plating followed by e-less plating. E-less plating followed by electrolytic plating was a known, effective technique for forming copper conductors.

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

131. McCormack renders claim [25] obvious. For example, McCormack describes metal layer 94 (including the recited metal plate) above the embedded integrated circuit component, and metal layers 16, 42, 98 below the embedded integrated circuit component. APPLE-1005, [0026] (“Metal layers 14 and 16 are optional, and may be any suitable conductive metal, such as copper. The metal layers 14 and 16 may be respectively disposed on the surfaces 12a and 12b by any suitable means, such as by lamination, plating, sputtering or chemical vapor deposition (CVD).”), FIG. 9. Based on my review of McCormack, a POSITA would have understood, and found obvious, that McCormack’s other metal layers are formed on the dielectric layers with the same manufacturing process.

132. Based on my knowledge and experience in the field, a POSITA would have understood and found obvious that these metal layers are metal films on a substrate, including unpatterned portions that provide the metal plate(s) as claimed, to provide beneficial EMI shielding. APPLE-1004 (corroborating prior art), [0012] (“a double-sided copper-clad **lamin**ate... can also be used” to form conductive pattern layers on “[r]esin substrates for incorporating electronic components such as IC chips”), [0032]-[0037] (describing the formation of the conductor circuits made of an electroless plated film and an electrolytic **plated film**); APPLE-1012 (corroborating prior art), [0017] (describing forming wiring layers above and below embedded electronic components in an insulating

substrate, with EMI shielding effect, through lamination and plating, e.g., by electroless and electrolytic copper **plating** over “**copper foil** 5, 6 that is several 10 μm thick.”) [0013] (“insulating layers ... made of epoxy resin and wiring layers ... made of Cu are alternately **laminated** above the front surface 3 of the insulating substrate 2”), [0021]-[0022], FIG. 2(A)).

133. I note that this construction is like the '909 patent's description of forming its metal plates, where the specification appears to use the terms “metal plate,” “metal foil” and metal “film” interchangeably. APPLE-1001, 5:47-56 (“**[i]n stage J**, a polymer film [11] is formed on the first surface (1a) of the circuit board, followed by a thin metal coating 12 on top of the polymer film. In the example process, stage J is carried out by laminating a thin polymer film... on the surface of the circuit board, on top of which is **a layer of copper** (e.g., c. 5 μm). **Lamination** takes place with the aid of pressure and heat. ... the **film** is thus an RCC (Resin Coated **Copper**) **foil**.”), FIG. 1J, 8:44-9:15 (referring to FIG. 4, “... polymer and **metal foils** can be formed on the first surface of the circuit board **similarly to stage 1J**. ... In FIG. 4D, ... a **metal plate** can be designed above the microcircuit, which is made in connection with the making of the circuit board's conductive pattern. Similarly, **a metal foil** that is as complete as possible is made below the microcircuit.”). The '909 patent describes a similar process for forming a “metal foil” on the bottom side of the circuit board below the microcircuit at

Stage F, (FIG. 1F)). *Id.*, 4:40-59 (forming a metal coating 8 in the form of “a **layer of copper** (e.g., c. 5 μ m). **Lamination** takes place with the aid of pressure and heat. ... the **film** is thus an RCC (Resin Coated **Copper**) foil.”), 9:11-15 (“Similarly, a metal foil that is as complete as possible is made below the microcircuit.”).

[26] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.

134. McCormack renders obvious claim [26] for at least the same reasons as I previously discussed in the analyses of claims [23] and [25], at least one of McCormack’s metal layers 16, 42 and 98 below integrated circuit component 20 formed by “lamination” and “plating” of copper provides a metal foil, as claimed.

Supra, §VIII.A.

[27pre]-[27d] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising: an insulating material layer including a baseboard and a hardened insulating polymer layer; conductive patterns on both sides of the insulating material layer; at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and

135. McCormack renders obvious [27pre]-[27d] for at least the same reasons that I previously discussed for elements [17pre]-[17d]. *Supra*, §VIII.A.

[27e] at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.

136. McCormack renders obvious element [27e] for at least the same reasons that I previously discussed for claims [25] and [26]. *Supra*, §VIII.A.

IX. GROUND 1B: CLAIMS 1-33 ARE OBVIOUS IN VIEW OF THE MCCORMACK-EIJI COMBINATION

137. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have understood that the teachings of McCormack and Eiji render claims 1-33 obvious.

A. The Predictable Combination of McCormack and Eiji

138. Based on my knowledge and experience in the field and my review of McCormack and Eiji, a POSITA would have been motivated to implement a shield layer on the sidewalls of the cavity with the electronic component embedded therein, in accordance with Eiji, in McCormack's multilayer printed circuit board to achieve known benefits. For example, a POSITA would have done so based on Eiji's suggestions to make the electronic components built into an insulating substrate "less susceptible to external electromagnetic waves," to "reduce the effects of noise generated by the circuits constituting these electronic components," and/or to "stabilize the electrical characteristics" of the system, consistent with Sakamoto's objectives of higher functionality, high-speed operation and improved reliability. APPLE-1012, [Abstract]; *see also*, [0001], [0005]-[0007] ("the wiring

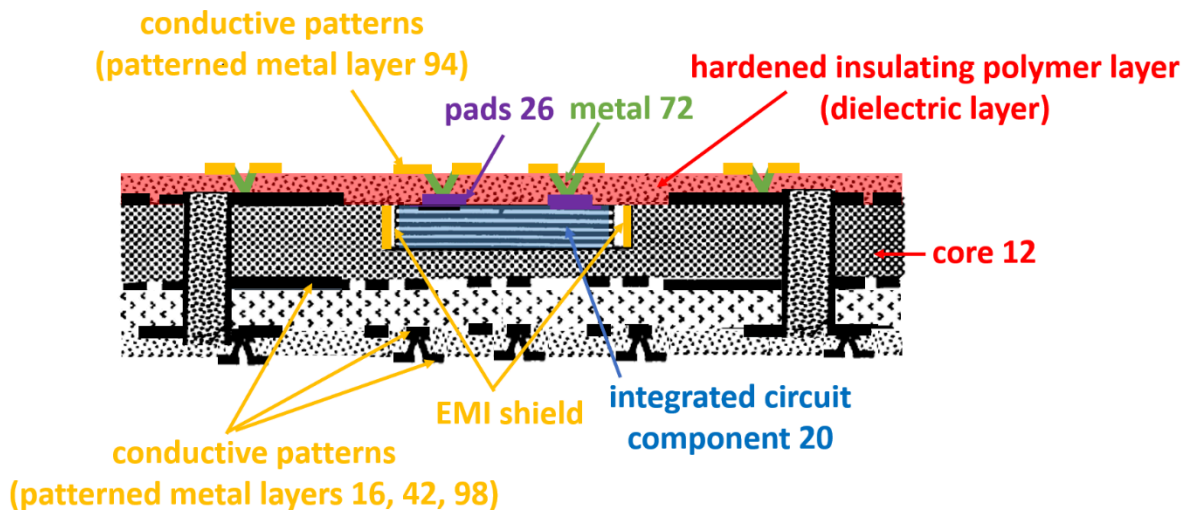
of the wiring layer at a position covering the opening to the through-hole or recessed portion in the insulating substrate also serves as the shielding layer”), [0009], [0011]-[0012] (“Wiring layers 26, 27, including wiring layers 26a and 27a which also serve as shielding layers, are formed in the upper and lower openings to the through-hole 8”), [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1; APPLE-1004, Abstract, [0006] (“components such as IC chips and capacitors with different functions can be mounted, and a multi-layer printed wiring substrate with higher functionality can be obtained.”), [0070]-[0071] (desire for “high-speed operation,” “higher functionality,” improved “connectivity between and reliability of the die pads and via holes,” shortened wiring length and reduced loop inductance).

139. In the combined module of McCormack in view of Eiji, an EMI shield layer composed of a copper plating film that shields electromagnetic waves (e.g., shielding layer 10) is formed on an inner surface of the cavity (e.g., cavity 24) in the core substrate (e.g., core 12), before inserting integrated circuit component (e.g., integrated circuit component 20), in accordance with Eiji’s teachings.

APPLE-1005, [0007], [0009], [0024]-[0025], [0028], FIGS. 12-13, cls. 11, 25-26; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

140. The resulting multilayer board implements McCormack’s suggestions of positioning the component in a cavity of the core substrate (e.g., cavity 24 of

core substrate 12), with an added electromagnetic interference (EMI) shield in the combined system, in accordance with Eiji. *E.g.*, APPLE-1005, [0030]-[0033] (additional dielectric layers of same or similar material and associated metal layers and vias are optional). The annotated composite figure below illustrates the configuration of the combined module.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

141. McCormack describes forming a cavity in the core 12 of the stack-up shown in FIG. 9. *See, e.g.*, APPLE-1005, [0028] (“one or both of the substrate surfaces 12a and 12b may have a cavity generally illustrated as 24 in FIG. 12”). Moreover, a POSITA would have recognized and found obvious that the circuit board having a cavity (e.g., as shown in McCormack’s FIG. 12) would have additional dielectric layer(s), such as any one or more of dielectric layers 30, 32, 60 and 64, or a combination thereof, along with their respective metal layers and vias therein, as already disclosed for the other embodiments such as in FIGS. 3-9 and

related descriptions, to effectuate McCormack's objectives and depending on the engineering and commercial needs. *E.g.*, APPLE-1005, [0009], [0030]-[0032] (following the descriptions of various embodiments of FIGS. 1-13, further describing that "[a]fter one or more of the integrated circuit components 20 have been suitable [sic] disposed where desired, dielectric layers 30 and 32 may be respectively placed, ... dielectric layers 60 and 64 are ... disposed").

142. McCormack describes an alternative embedding method as illustrated in FIGS. 12 and 13, where the integrated circuit component is disposed in cavity 24 in core 12, as opposed to on a surface of core 12 as shown in FIG. 9. Both embedding options develop from the same core substrate of FIG. 2 and thus sharing all other common features as indicated by the same numeral labels. *See e.g.*, APPLE-1005, [0009], [0024]-[0029], FIGS. 2, 9, 12, 13; *supra*, § VII.A., McCormack Overview.

143. A POSITA would have been prompted to utilize EMI shielding in the multilayer printed circuit board with embedded components, as well as to use a glass fiber epoxy (e.g., for core substrate 12/dielectric layers), in accordance with Eiji. As I describe in more detail in the following paragraphs, multiple reasons confirm this analysis:

144. First, a POSITA would have been motivated to combine McCormack and Eiji to alleviate the common and well-known problem of electromagnetic

interference caused by external electromagnetic waves, reduce influence by noise from circuits composed of various electronic components, and/or to stabilize electric characteristics of the entire system.

145. McCormack already teaches disposing an electronic component such as an integrated circuit component 20 in cavity 24 in core substrate 12. APPLE-1005, [0009] (“A cavity may be formed in the exposed portion of the second substrate surface, and a second integrated electronic component may be disposed in the cavity.”), [0024]-[0025], [0028] (“In another embodiment of the present invention one or both of the substrate surfaces ... may have a cavity generally illustrated as 24 in FIG. 12. The cavity 24 may be formed by any suitable means, such as by milling, cutting or drilling. The prefabricated, integrated circuit component 20 ... may be conveniently disposed in the cavity 24.”), FIGS. 12-13, cls. 11, 25-26. As I previously discussed under the McCormack ground, McCormack incorporates by reference Dineen, which teaches mounting “a plurality of electronic components” in “a plurality of holes” on a flat substrate. *Id.*, [0007]. *Supra*, §VIII.A.

146. McCormack similarly describes mounting multiple electronic components close to each other in the same circuit board assembly and in “high frequency applications.” APPLE-1005, [0006], [0008], [0034]; APPLE-1014, 1:10-28 (corroborating prior art Dudderar describing susceptibility of “high

frequency applications” to “EMI problems” such as “stray electromagnetic radiation”).

147. A POSITA would have recognized that, as were common problems with component built-in devices and high-density component mounting well known by the Critical Date, that electronic components incorporated into an insulating board can be easily affected by an external electromagnetic wave, and influenced by noise generated by a circuit composed of the electronic components, as evidenced by Eiji. APPLE-1012, [Abstract]; APPLE-1014 (corroborating prior art describing “EMI problems” “disruptive to the proper operation of circuit components located near the source of the EMI,” and a solution of “EMI metallization shield” including above, below and along the inside walls of a cavity for accommodating electronic components); APPLE-1016, [0022] (corroborating prior art describing “shielding effect” against EMI); APPLE-1015, 4:7-9, 5:24-36, 12:39-50 (corroborating prior art describing the use of a “shield layer” or “shield section” so that “noise does not penetrate to the electrical element contained inside the housing section of the multilayer substrate”); APPLE-1014, 1:10-28 (corroborating prior art describing susceptibility of “high frequency applications” to “EMI problems” such as “stray electromagnetic radiation”).

148. A POSITA would have predictably looked towards other teachings such as Eiji for solutions. *See also* APPLE-1014, 4:44-49 (corroborating prior art

disclosing “EMI shield metallization” “extend[ing] along the inside wall of cavity 17”). Eiji provides a known technique that would have been recognized to further “stabilize the electrical characteristics” of the system. APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

149. Second, a POSITA would have been motivated to combine McCormack and Eiji based on Eiji’s description of a glass epoxy material, in order to enhance the mechanical strength of the core/dielectric layers in the resulting device. Eiji describes composite materials of glass fibers with epoxy resin, which would have been recognized as beneficially utilized in McCormack’s device to enhance robustness of the construction. APPLE-1012, [0012], [0038], Abstract.

150. Third, combining McCormack and Eiji would have been a common application of known techniques (forming an EMI shield layer on the sidewalls of a through hole or cavity provided in an insulating substrate for incorporating an electronic component) to a known electronic module system (McCormack’s multilayer printed circuit board having a cavity 24 in core substrate 12 to accommodate an electronic component such as integrated circuit component 20 between wiring layers). Based on my knowledge and experience in the field and my review of McCormack and Eiji, a POSITA would have had a reasonable expectation of success modifying McCormack with Eiji, because of the similarities

between the systems. For example, both McCormack and Eiji describe multilayer wiring/circuit boards with electronic components embedded inside holes or cavities of an insulation substrate. APPLE-1005, Abstract; APPLE-1012, Abstract.

151. Based on my analysis, a POSITA would have recognized that applying Eiji's suggestions to McCormack's circuit board would not have significantly altered or hindered the functions performed by McCormack's circuit board. Moreover, based on my knowledge and experience in the field, a POSITA would have found making the proposed modifications to be straightforward, since the modifications would have been implemented largely by adding a metal layer on the sidewalls of the cavity. Eiji already demonstrates this configuration to be successful. And the use of shield layers against EMI problems was known. *See e.g.*, APPLE-1014 (corroborating evidence to show the use of a "EMI metallization shield" along the inside walls of a cavity for accommodating electronic components to address EMI problems).

152. I note that in addition to Eiji's teaching, McCormack also teaches "conventional" techniques of "metal lining" various via holes and openings in an insulating substrate, further leading a POSITA to this predictable configuration. APPLE-1005, [0031] ("opening for vias... are metal-lined (e.g., copper lined) with metal liners By any suitable process, such as by e-less plating in combination with electrolytic plating, well known to those skilled in the art"), [0032],

(“Openings ... are then metal-lined by any conventional process to respectively dispose metal liners ... in openings”), cl. 1. The reasons I’ve noted above further highlight that McCormack and Eiji are analogous art, in the same field of endeavor and pertinent to the types of problems associated with semiconductor packaging and manufacturing.

B. Analysis of McCormack and Eiji with Respect to Claims 1-33

153. As shown in this section, the McCormack-Eiji combination, when predictably combined for at least the reasons described above, renders obvious claims 1-33. To be clear, McCormack-Eiji renders obvious independent claim 1 and its dependent claims without modification to utilize multiple circuit board substructures on top of each other that is described with reference to claims 12-27.

[1pre]-[1c], [1e]

154. McCormack-Eiji renders obvious elements [1pre]-[1c] and [1e] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12c] and [12d]. *Supra*, §VIII.A.

[1a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

155. In addition to the reasons that I previously discussed under the McCormack ground alone, McCormack-Eiji satisfies it. For example, Eiji provides express teaching for use of glass fibers reinforced epoxy resin for an insulating substrate, as it describes, “the insulating substrate 2 can be made of glass

woven fabrics or composite materials of glass fibers and resins such as epoxy resin.” APPLE-1012, [0012], Abstract. Eiji further describes that “in addition to the glass-epoxy resin composite material described above, the insulating substrate 2 can be made of glass woven fabrics or composite materials of glass fibers and resins such as epoxy resin, polyimide resin, or BT resin having similar heat resistance, mechanical strength, flexibility, and ease of processing.” *Id.*, [0038].

156. Based on my knowledge and experience in the field, and my review of McCormack and Eiji, a POSITA would have been prompted to enhance the mechanical strength of McCormack’s core 12 and dielectric layers by using composite materials of glass fibers with epoxy resin, in accordance with Eiji’s teaching, as I discussed above. I note that this construction is just like the ’909 patent’s example for its own baseboard 1. APPLE-1001, 3:45-55 (“The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board...”).

157. I further note that a POSITA would have had a reasonable expectation of success in making this proposed modification. This is because McCormack and Eiji describe similar electronic devices, both using epoxy resin for an insulating substrate to house electronic components. It is also because the modification would have been implemented by substitution with a known material. Eiji already demonstrates this configuration to be successful.

[1d] conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

158. McCormack-Eiji renders obvious element [1d]. The McCormack-Eiji combination's integrated circuit component 20 is located in a hole (e.g., cavity 24) in the core substrate 12, which corresponds to the baseboard of the claimed insulating material layer. *Supra*, §IX.A. (McCormack-Eiji combination). Further, McCormack-Eiji includes a metal foil (e.g., a copper plating film), which is a conductive material, formed on the inner surface of and covering the sidewalls of the cavity 24, to provide a shielding layer against EMI, in accordance with Eiji's teachings. *Id.*

159. Based on my analysis of McCormack, Eiji and the '909 patent, I note that McCormack-Eiji's shielding layer material and configuration, in accordance with Eiji's teachings, is just like the '909 patent's description for growing its metal foil on the sidewalls of the holes by copper plating. *Compare* APPLE-1012, [0017] ("electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole") *with* APPLE-1001, 3:61-4:9 ("metal 4" "is grown into the through holes" at Stage C (FIG. 1C), by "coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method... The metal can thus be grown using a wet-chemical method, ... Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste."); *see also* APPLE-1012, Abstract, [0012]. Note that the '909 patent describes that the

same method for growing metal 4 is used for growing the metal foil covering the side walls of the holes to accommodate the electronic components. APPLE-1001, 8:39-46 (“the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components”).

160. I note that other references corroborate the use of a metal foil covering the sidewalls of a hole or cavity for embedding electronic components to provide EMI shielding. For example, U.S. Patent No. 6,297,551 to Dudderar et al., titled “Integrated Circuit Packages with Improved EMI Characteristics,” filed September 22, 1999 and issued October 2, 2001 (incorporating by reference U.S. Patent No. 5,608,262 to Degani et al, titled “Packaging Multi-Chip Modules without Wire-Bond Interconnection,” filed February 24, 1995 and issued March 4, 1997), describes metalizing sidewalls of a cavity to provide EMI shielding of semiconductors embedded in the cavity. APPLE-1014, 4:45-50 (“Here the EMI shield metallization extends along the inside wall of cavity 17 as shown at 41, and connects with the EMI cavity shield metallization 27” as in the arrangement of FIG. 1.).

161. I note that this is also consistent with McCormack’s own teaching of using “conventional process” to metal line various “openings” and “vias” in insulating boards such as “by e-less plating in combination with electrolytic

plating, well known to those skilled in the art.” APPLE-1005, [0031]-[0032];

supra, §IX.A (McCormack-Eiji combination).

[1e] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

162. In addition to the reasons I described under the McCormack ground alone, I note that Eiji also provides express teaching of “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate. APPLE-1012, [0017]. A POSITA would have been prompted to utilize these techniques with the combined device, including to implement the formation of copper metal lining in the openings, to avail the combined device of a known and effective technique for forming electrical contacts.

[2] The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

163. McCormack-Eiji renders claim [2] obvious for at least the same reasons that I previously discussed in the analysis of element [12a], McCormack’s dielectric layers contain “epoxy resins.” *Supra*, §VIII.A.

[3] The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.

164. McCormack-Eiji renders claim [3] obvious for at least the same reasons that I previously discussed in the analysis of element [1a] (§IX.B), a

POSITA would have been motivated to enhance the mechanical strength of McCormack-Eiji's core substrate 12 and dielectric layers, including the dielectric layer over core 12 and the embedded component (the recited hardened insulating polymer layer), by using composite materials of glass fibers with epoxy resin, in accordance with Eiji's teaching.

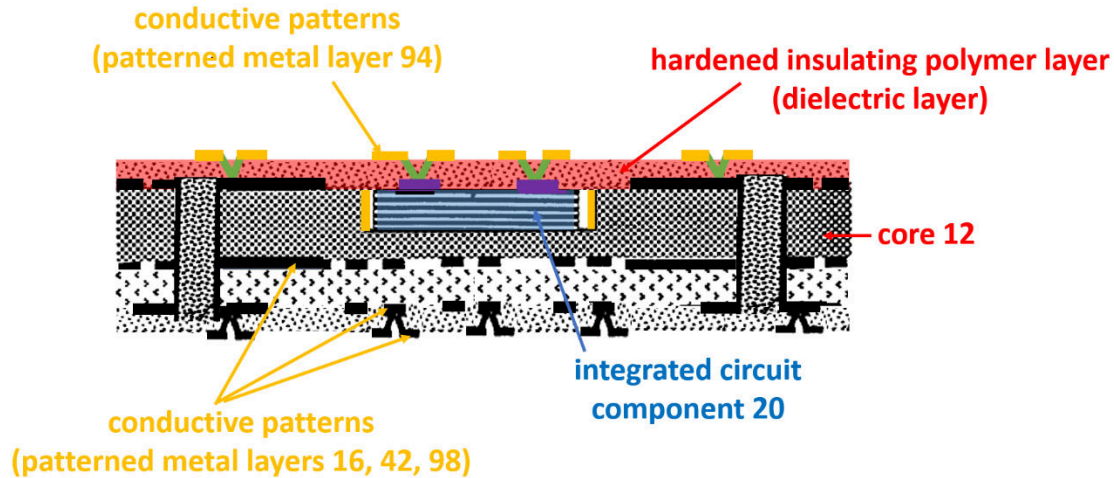
[4] The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

165. McCormack-Eiji renders obvious claim [4]. The McCormack-Eiji combination's baseboard (e.g., core substrate 12) is made of composite materials of glass fibers with epoxy resin. *Supra*, §IX.B, analysis of element [1a], §VIII.A, analyses of element [12a] and claim [22].

[5] The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.

166. McCormack-Eiji renders obvious claim [5]. McCormack-Eiji's integrated circuit component (the recited microcircuit) is located between metal layer 94 (the recited conductive patterns) on the upper side, and metal layer 16 (and metal layers 42, 98) (the recited conductive patterns) on the lower side, of the insulating material layer composed of the core substrate 12 (or further in combination with the additional dielectric layers 32, 64) (the recited baseboard) and the dielectric layer over the core substrate 12 (the recited hardened insulating polymer layer). *Supra*, §§VIII.A, analyses of elements [12pre]-[12c], IX.B,

analyses of elements [1pre]-[1c]. The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[6] The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.

167. McCormack-Eiji renders obvious claim [6]. The McCormack-Eiji circuit board includes a filler material in the hole (e.g., cavity 24), the filler material secures the integrated circuit component 20 in place in the hole. *Supra*, §VIII.A, analysis of element [12c]. For example, McCormack describes “a suitable adhesive” and “[a]dditional underfill, glop-top, or other adhesive/sealant materials” for securing the integrated circuit components “to a desired location,” and various “filler material” for filling metal-lined openings and vias in its insulating layers. APPLE-1005, [0029]-[0030], [0031] (“Dielectric materials ... conveniently provide filler material for the vias ... blind-via openings are ... subsequently filled with dielectric sputtering or by filler materials ... disposed by screen printing or lamination), [0032] (“Optionally the material for dielectric layers

... may form the filler materials”), [0033] (listing a variety of “[s]uitable dielectric material” for “filler material” including “epoxy resins” and the process of “curing” “filler material” along with other dielectric layers of the circuit board “upon additional exposure to heat and pressure”).

168. Based on my knowledge and experience in the field, a POSITA would have recognized and found obvious that the same type of adhesive, underfill, glop-top, or other adhesive/ sealant materials, and/or other filler material such as epoxy resins, is used to fill any gap in cavity 24 between the EMI shield and the component and secure the component in a desirable location in the cavity. *See e.g.*, APPLE-1005, [0006] (desire to secure embedded electronic components “in a precise position and orientation” in the holes).

169. Additionally, and consistent with McCormack’s teaching, Eiji also describes a “resin 16, which is primarily epoxy resin,” which is a filler material between the metal foil and the components to secure each component at “a predetermined location in the through-hole.” APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], cls. 2, 7, FIGS. 1, 3.

170. Degani, as I introduced previously as corroborating prior art, also provides corroborating evidence on the use of a filler material, as it describes filling the cavity with an encapsulating material, “such as an epoxy resin,” “which

protects the chips, interconnections between the chips and the substrate, interconnections between the substrate and the PWB, and surfaces of the substrate exposed within the cavity.” APPLE-1019, 2:24-26, 3:4-38, 3:54-56, 5:24-34, 5:63-65, cls. 2, 6. Vu, another prior art introduced earlier, similarly provides corroborating evidence by describing encapsulating material 122 in an opening of a substrate to secure electronic components disposed therein. APPLE-1008, [0037], [0042] (“The encapsulation material 122 secures the microelectronic device 114 within the microelectronic substrate core 102 and provides mechanical rigidity for the resulting structure...”).

[7] The circuit board of claim 6, wherein the filler material contains epoxy.

171. McCormack-Eiji renders obvious claim [7]. McCormack-Eiji’s filler material (e.g., either McCormack’s “filler materials” or Eiji’s “resin 16”) contains epoxy. *Supra*, §IX.B., analysis of claim [6].

[8pre] The circuit board of claim 1, wherein

172. McCormack-Eiji provides [8pre]. *Supra*, §IX.B., analysis of claim [1].

[8a] said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and

173. McCormack-Eiji renders obvious element [8a]. In addition to the reasons that I previously discussed for claim [14] (§VIII.A.), Eiji also describes

embedding multiple electronic components in the same substrate, a POSITA would have been prompted to embed multiple electronic components in the same substrate, in accordance with Eiji's suggestions, to provide enhanced functionality and high-density mounting. *See e.g.*, APPLE-1012, Abstract, [0006] (different types of electronic components can be embedded either in different or the same through-holes or recessed portions), FIGS. 1-7.

[8b] the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

174. McCormack-Eiji renders obvious element [8b]. For example, when several integrated circuit components (the recited microcircuits) are provided in the same substrate of the combined system, these integrated circuit components are connected to each other, for example, through metal 72 in openings 70 (the recited conductors in the contact opening) for connecting to both the pads 26 on the first surface of each integrated circuit component and metal layer 94 (the recited at least one of the conductive patterns). *Supra*, §§IX.B, analyses of elements [1e], [8a], VIII.A, analysis of element [12d].

[9] The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

175. McCormack-Eiji renders obvious claim [9]. As I previously discussed for elements [12d] (§VIII.A.) and [1e] (§IX.B.), metal 72 made of copper formed

in openings 70 (the recited copper in the contact openings) is formed by a “combination of e-less” plating (the recited first layer of chemically deposited copper) and “electrolytic plating” (the recited second layer of electrochemically deposited copper on the first layer of chemically deposited copper).

176. Moreover, Eiji similarly describes formation of conductors on the inner surfaces of through-holes in an insulating substrate through “electroless copper plating and electrolytic copper plating.” APPLE-1012, [0017].

[10] The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

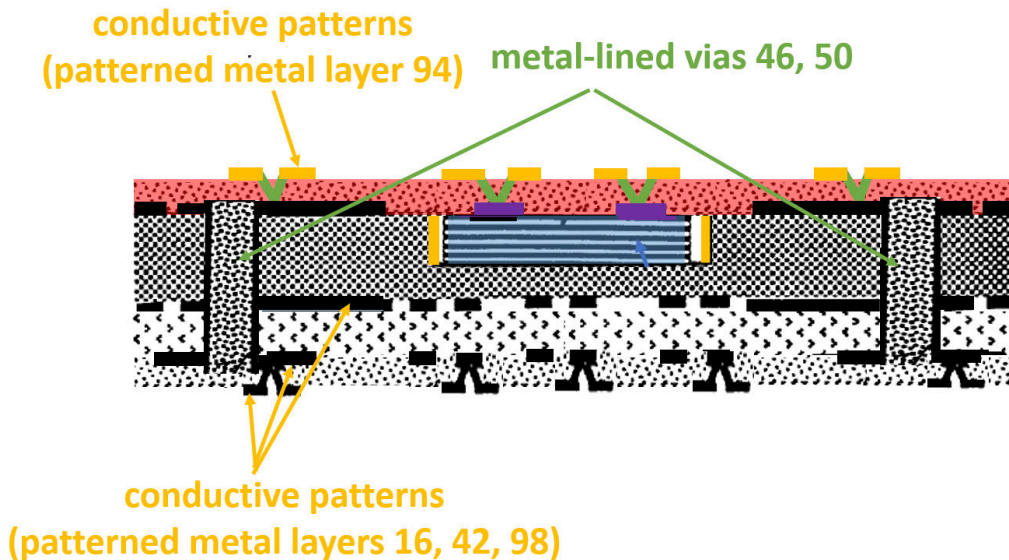
177. McCormack-Eiji renders obvious claim [10]. The McCormack-Eiji combination has an electrically conducting feed-through (e.g., metal-lined vias 46 and 50) between the conductive pattern layers (e.g., metal layers 94, 16, 42, 98) on both sides of the insulating material layer of the circuit board. For example, McCormack describes “metal-lined vias 46 and 50” functioning as conductive feed-throughs “formed by drilling openings through the entire FIG. 5 circuit board assembly,” these metal-lined vias provide electrical connection between the metal layer on the upper side (e.g., patterned metal layer 94) and metal layer(s) (e.g., patterned metal layer 16, 42, or 98) on the lower side of the circuit board. APPLE-1005, [0031].

178. For example, McCormack explains that the “openings pass[] through metal layers 40 and 42, through dielectric layers 30 and 32, through residual metal layers remaining from patterned metal layers 14 and 16, and through the core 12.” *Id.*, [0031]. A POSITA would have found obvious that when a single dielectric layer is used above the core substrate 12, the openings pass through dielectric layer 32 and the core 12, and through residual metal layers remaining from patterned metal layers 14 and 16. *Id.*

179. McCormack further explains that “[t]he opening for vias 46 and 50 are metal-lined (e.g., copper lined) with metal liners 46a and 50a by any suitable process, such as by e-less plating in combination with electrolytic plating, well known to those skilled in the art. Metal liners 46a and 50a are preferably respectively formed such as to be in electrical contact with residual metal layers remaining from patterned metal layers 14 and 16...” *Id.*; *see also id.*, [0009] (“at least one via passing through the circuit board from the first substrate surface to the second substrate surface”), [0018]-[0019] (“a pair of blind metal-lined vias”), [0020]-[0022], [0026] (core substrate assembly ... may also have one or more conducting-through vias, generally illustrated as 18 in FIG. 10”), FIGS. 6-10.

180. Based on my analysis of McCormack, a POSITA would have found obvious that when a single dielectric layer above the core is used in the combined module, metal layer 94 is coupled to residual metal layers 14, by and through metal

liners 78 in openings 76. *Id.*, [0032] (metal layer 98 is also coupled to metal layer 42 by and through metal liners 82 in openings 80), FIG. 9. The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

[11pre]-[11b]

181. The McCormack-Eiji combination renders obvious elements [11pre]-[11b] for at least the same reasons that I previously discussed in the analyses of elements [8pre]-[8b] (§IX.B.).

[12]-[21], [23]-[27]

182. The McCormack-Eiji combination renders obvious these claims for at least the same reasons that I previously discussed for these claims under the McCormack ground (§VIII.A) alone. Additionally, for elements [12d], [17d], [19d], [20d], [27d] and claim [24], which recite the same or similar features relating to chemically and/or electrochemically deposited copper in the contact

openings, Eiji also provides express teaching of “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate. APPLE-1012, [0017]. *Supra*, §IX.B., analysis of element [1e]. And for 12[a], the McCormack-Eiji device includes a baseboard made of a glass fiber epoxy. Here again, I note this construction is the same material construction recited by the '909 patent.

[12a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

183. The McCormack-Eiji combination provides a baseboard made of a glass fiber epoxy—the same material construction recited by the '909 patent, and thus renders obvious [12a]. *Supra*, §IX.B, analyses of element [1a] and claim [4].

[22] The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.

184. The McCormack-Eiji combination renders obvious claim [22] for at least the same reasons as I previously discussed for claim 4 (§IX.B.) and claim 20 (§VIII.A.).

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

185. McCormack-Eiji renders obvious claim [25]. In addition to what I previously discussed for claim [25] under the McCormack ground (§VIII.A.) alone, and consistent with McCormack’s teachings, a POSITA would have

predictably implemented the metal layers in accordance with Eiji's further suggestions. Eiji also describes metal wiring layers (e.g., 26, 27) formed above and below embedded electronic components in an insulating substrate through lamination of and plating over a "copper foil," e.g., by electroless and electrolytic copper plating over "copper foil 5, 6 that is several 10 μm thick." APPLE-1012, [0017], [0013] ("insulating layers ... made of epoxy resin and wiring layers ... made of Cu are alternately laminated above the front surface 3 of the insulating substrate 2"), [0021]-[0022], FIG. 2(A). I note that Eiji's wiring layers are each more than (due to plating on top of the copper foil) "several 10 μm thick," which is a substantial thickness compared with the '909 patent's metal coating of "e.g., c. 5 μm ." Although not required by the '909 patent's claims, Eiji also teaches connecting these wiring layers above and below the components to each other and to the shielding layer on the sidewalls of the hole for incorporating the components, all connected to a ground connection, to provide enhanced EMI shielding. APPLE-1012, Abstract, [0007]-[0008], [0010]-[0011], [0013]-[0014], [0021], [0023]-[0028], [0034]-[0036], cls, 3, 4, 5, FIGS. 1, 4.

186. Based on my analysis, I note that McCormack and Eiji combined provide at least as much detail as the '909 patent, which tersely recites a "metal plate" and "metal foil" without construction details, and separately describes materials like that described by McCormack, such as "a layer of copper" made of

“an RCC (Resin Coated Copper) foil” and “metal foil” through lamination, for forming its metal plates. APPLE-1001, 5:47-56, 8:44-9:41, 4:40-59; FIGS. 1J & 1F; *supra*, §VIII.A., analysis of claim [25].

187. I note that to the extent the '909 patent's description of forming a metal plate in connection with the making of the circuit board's conductive pattern requires growing a thicker metal film from its “metal coating 12” and/or “metal coating 8,” McCormack-Eiji also provides it. APPLE-1001, FIGS. 1F, 1J, 4C, 4D (with the structure corresponding to a metal plate above and below the embedded electronic components appearing thicker than the metal films in the same positions in FIG. 4C), 4:40-63, 5:47-6:4, 8:44-9:41. For example, each of McCormack-Eiji's conductive metal layers implemented in accordance with Eiji have a thickness more than “several 10 μm thick,” which is substantially thicker than the '909 patent's metal coating of “e.g., c. 5 μm .” APPLE-1012, [0017], [0021]-[0022].

[26]-[27]

188. McCormack-Eiji renders obvious claims [26] and [27]. In addition to the reasons that I previously discussed under the McCormack ground, at least one of the McCormack-Eiji combined system's metal layers 16, 42 and 98 below integrated circuit component 20, e.g., formed in accordance with Eiji (e.g., “copper

foil” that is more than “several 10 μm thick” after plating), is a metal foil. *Supra*, §VIII.A., Analysis of Claim [25].

[28] The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

189. McCormack-Eiji renders obvious claim [28]. As I previously discussed for element [1d], the combined system’s shield layer on the sidewalls of cavity 24 in the core substrate 12 (the recited baseboard) is “composed of a copper plating film” (the recited metal foil as the conductive material). *Supra*, §IX.B.

[29] The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.

190. McCormack-Eiji renders obvious claim [29]. Based on my knowledge and experience in the field, and my analysis of McCormack and Eiji, a POSITA would have been prompted to provide the metal foil on the sidewalls in the form of an unbroken metal foil that surrounds the microcircuit in a lateral direction of the circuit board, effectuating and enhancing the shielding objective of the metal foil. *Supra*, §IX.B, analyses of element [1d] and claim [28].

[30]-[32]

191. McCormack-Eiji renders obvious claims [30]-[31] for at least the same reasons that I previously discussed in the analysis of claim [25], the unpatterned portions of at least one of metal layers (e.g., metal layer 94) above integrated circuit component 20 provide a metal plate above the component, and the unpatterned portions of at least one of metal layers (e.g., metal layer 16, 42 or

98) below integrated circuit component 20, provide a metal plate below the component. *Supra*, §VIII.A, §IX.B.

[33] The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

192. The McCormack-Eiji combination renders obvious claim [33] for at least the same reasons that I previously discussed for claims [25] and [28]. *Supra*, §VIII.A, §IX.B.

X. GROUND 1C: CLAIMS 12-27 ARE OBVIOUS IN VIEW OF THE MCCORMACK-EIJI-SUGAYA COMBINATION

193. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have understood that the teachings of McCormack, Eiji and Sugaya render obvious claims 12-27. As I discuss in more detail below, Sugaya describes multi-layered circuit board structures, and thus provides additional express teachings relevant to the “multi-layered” elements of independent claim 12 and its dependent claims.

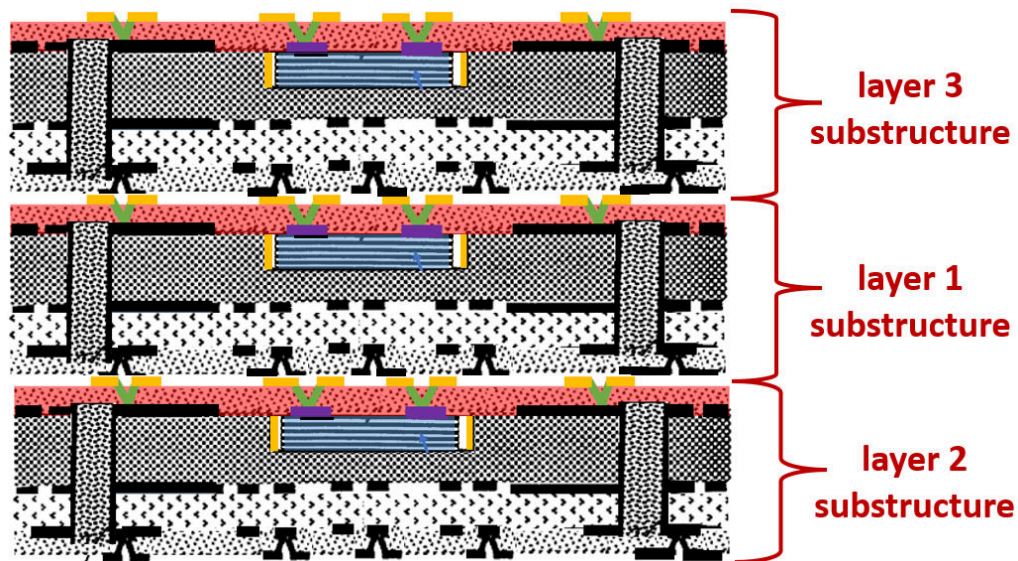
A. The Predictable Combination of McCormack, Eiji and Sugaya

194. Based on my knowledge and experience in the field and my review of McCormack, Eiji and Sugaya, a POSITA would have been motivated to combine the teachings of McCormack, Eiji and Sugaya provide a high-density, multi-layered structure with EMI shielding effect. Each of these references relate to a

component built-in module where circuit components are provided inside an insulating substrate. *See e.g.*, APPLE-1005, Abstract, [0002], [0029]-[0030]; APPLE-1012, [0023], FIGS. 1, 4; APPLE-1007, Title, Abstract. Sugaya also provides express disclosure on stacking up any number of layers of similar configuration to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1007, Abstract, [0004] (“In recent years, with the demand for high performance and miniaturization of electronic equipment, high density, high performance and short-distance wiring of a circuit component have been desired increasingly.”), [0225] (“Although FIG. 9A shows the circuit component built-in module 900 having a three-layered structure, a structure having any number of layers can be formed depending on the design.”), [0217], [0351], [0354], FIGS. 9A, 9B.

195. As I previously discussed for the McCormack-Eiji combination (§ IX.A.), a POSITA would have been motivated to utilize an EMI shield feature, in accordance with Eiji’s teachings, in a cavity in the core substrate described by McCormack, to provide a shielding effect. A POSITA would have been further motivated to stack up two or more layers of McCormack-Eiji’s circuit board, depending on the design, to form a multi-layered configuration, in accordance with Sugaya, to achieve high density mounting with EMI shielding. Adjacent layer substructures are electrically connected to each other to form a multi-layered

functioning totality, in accordance with Sugaya's suggestions. APPLE-1007, FIG. 9A, [0224]-[0229]. Below composite figure illustrates a three-layered configuration with each substructure layer having an integrated circuit component embedded in a cavity of its own core substrate, each cavity having metal foil on its sidewalls to provide EMI shielding.



Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated)

196. Moreover, Sugaya provides express description of “LSI, or the like” as examples for the components of its component built-in module. APPLE1007, [0092] (“a semiconductor device such as a transistor, an IC, an LSI, or the like, can be used”). The McCormack-Eiji-Sugaya combination also includes “LSI” (large-scale integration), which were typically used in components like microprocessors, where a single chip contains both processing logic and on-chip memory.

197. Based on my knowledge and experience in the field and my review of the references, a POSITA would have had a reasonable expectation of success in combining McCormack-Eiji with Sugaya. This is because McCormack, Eiji and Sugaya describe similar electronic devices composed of multilayer circuit board substrates with embedded semiconductor components. This is also because the modifications involve only implementation of well-known technologies. I note here again that McCormack, Eiji, and Sugaya related to the same field of endeavor and are directed to analogous subject matter, including disclosure pertinent to the construction of multi-layered circuit board configurations.

B. Analysis of McCormack, Eiji and Sugaya with Respect to Claims 12-27

198. As shown in this section, the McCormack-Eiji-Sugaya combination, when predictably combined for at least the reasons described above, provides claims 12-27.

[12]-[27]

199. The McCormack-Eiji-Sugaya combination renders obvious these claims for at least the same reasons that I previously discussed under the McCormack and McCormack-Eiji grounds (§VIII.A, §IX.B). In addition, with respect to the recited multi-layered feature, Sugaya provides express teaching of a stack-up multi-layered configuration. *Supra*, §VII.D, Sugaya Overview; APPLE-1007, [0225]; *see also*, [0004], [0217], [0226]-[0229], [0351], [0354], FIGS. 9A

(showing a three-layered structure), 9B. As I discussed in the McCormack-Eiji-Sugaya combination (§X.B), the combined system has a stack-up multi-layered configuration, in accordance with Sugaya. Each of the substructure layers (e.g., layers 1-3 in the composite figure above) has a similar or same configuration. The composite figure above illustrates this configuration, having three similar circuit board substructures stacked on top of each other. To be clear, each adjacent layer substructure is electrically connected with one another such that the resulting device provides a multi-layered functioning totality, in accordance with Sugaya's suggestions. APPLE-1007, FIG. 9A, [0224]-[0229].

200. Additionally regarding Claim [15], the McCormack-Eiji-Sugaya device includes a "memory circuit." For example, Sugaya describes semiconductor components such as "LSI, or the like." APPLE1007, [0092] ("a semiconductor device such as a transistor, an IC, an LSI, or the like, can be used"). LSI devices were commonly known to include memory, thereby providing a memory circuit. A POSITA would have been prompted to avail the resulting device of the advantages of an LSI device, including a memory circuit, to enhance the functionality of the device and expand the potential uses of the resulting device.

XI. GROUND 2A: CLAIMS 12-27 ARE OBVIOUS IN VIEW OF SAKAMOTO

201. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art cited herein, claims 12-27 are disclosed by Sakamoto.

A. Analysis of Sakamoto with Respect to Claims 12-27

[12pre] A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:

202. Sakamoto provides [12pre]. Sakamoto provides a multi-layered circuit board. First, Sakamoto provides a circuit board. For example, Sakamoto describes “a multilayer printed wiring substrate” comprising a “core substrate 30” in which IC chips (e.g., “IC chip 20”) and other “electronic components” are embedded. APPLE-1004, Title, Abstract, [Claim 1], [0001], [0005]-[0007], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12.

203. Sakamoto explains that suitable material for core substrate 30 used to incorporate electronic components such as IC chips “include epoxy resins, BT resins, and phenol resins impregnating a reinforcing material such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin. However, any material generally used in printed wiring substrates can be used.” *Id.*, [0012], [0020], [0023] (“an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as glass cloth has been impregnated with a resin such as an epoxy is used as the starting material”).

204. I note that this disclosure is just like the '909 patent's description for its "baseboard 1 [] selected for the circuit-board manufacturing process," such as "a glass-fibre reinforced epoxy board, such as an FR4-type board," "an organic board," or "an inorganic board." APPLE-1001, 3:46-55, cl. 9.

205. Sakamoto further provides a multi-layered circuit board which includes at least two circuit board substructures (e.g., a first circuit board substructure and second circuit board substructure) on top of each other. For example, Sakamoto describes connections with "external substrates such as motherboards and daughterboards," as well as mounting electronic components such as IC chips with different functions, thereby obtaining a multi-layer printed wiring substrate with higher functionality. APPLE-1004, [0006], [0011]. Sakamoto also describes an example of mounting IC chip 20, a cache memory 120, and a capacitor mounted both inside and on the surface of the wiring board and "arranged close to each other, enabling high-speed operation of the IC chip." *Id.*, [0068]-[0070].

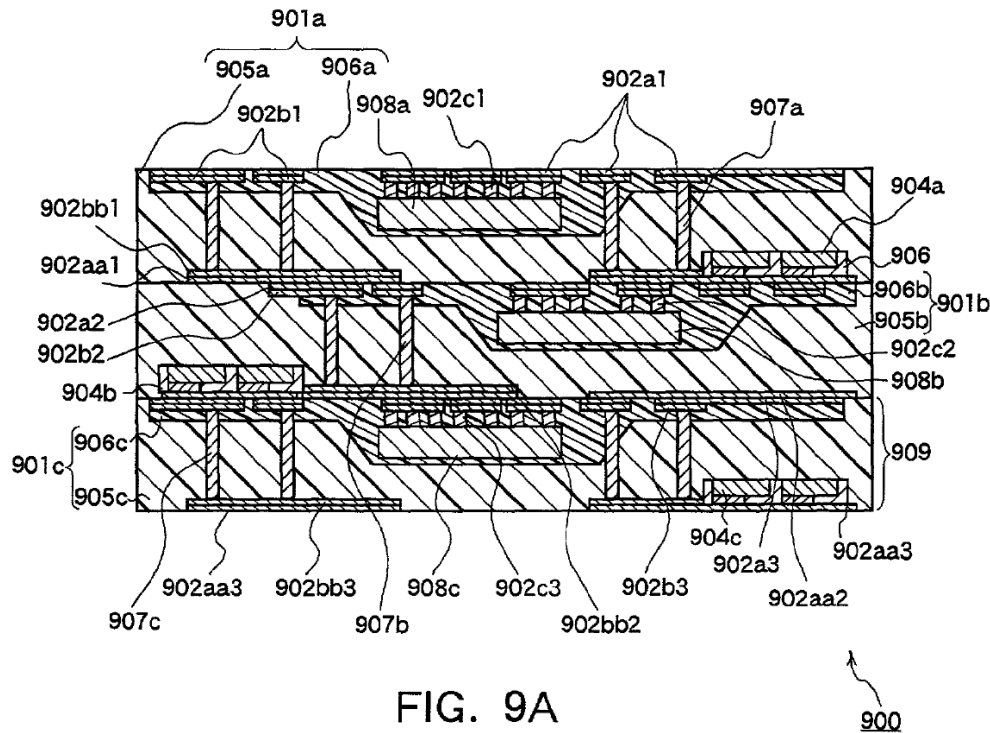
206. Based on my knowledge and experience in the field, I note that it was a common practice and well known in the field to stack multiple layers of circuit-board substructures on top of each other and mount a plurality of electronic components in the same as well as different such substructure layers to achieve

high-density, improved performance, reduced manufacturing cost, space saving, and short-distance wiring.

207. For example, Sugaya (U.S. application publication No. 2001/0030059, filed December 15, 2000), as corroborating prior art, relates to a circuit component built-in module capable of mounting the circuit component with high density and having high heat releasing property and high reliability. APPLE-1007, Abstract, [0004] (“In recent years, with the demand for high performance and miniaturization of electronic equipment, high density, high performance and short-distance wiring of a circuit component have been desired increasingly. Accordingly, a wiring substrate capable of including a high density, high-performance and short-distance wiring circuit component has been demanded. The formation of a multi-layer circuit may be a solution to attain a higher-density wiring substrate.”), [0034] (“it is preferable in the configuration that the wiring substrate includes one or a plurality of circuit component built-in modules... it is possible to realize a highly reliable multilayer circuit component built-in module in which the circuit components are mounted with high density.”).

208. Sugaya describes an example circuit component built-in module having a three-layered structure. APPLE-1007, [0217], [0225] (“Although FIG. 9A shows the circuit component built-in module 900 having a three-layered structure, a structure having any number of layers can be formed depending on the

design.”), FIG. 9A (reproduced below showing a three-layered structure with circuit components 908a, 908b and 908c embedded in the various substructure layers).

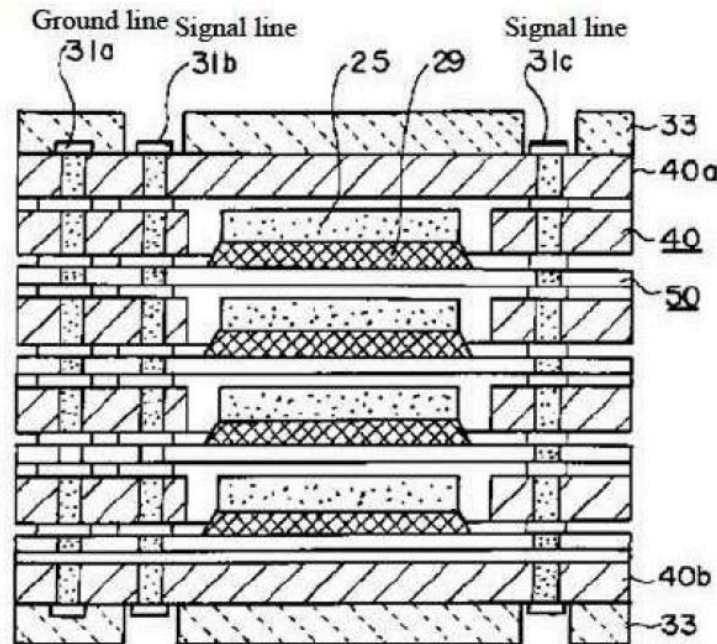


APPLE-1007, FIG. 9A

209. Another example as corroborating evidence, prior art Imoto (JP patent application publication No. 2001-068624, published March 16, 2001) describes a semiconductor device having a multi-layered structure that includes any number of layers. *E.g.*, APPLE-1016, [0010] (“This embodiment is an example of four laminated semiconductor elements, but the number of semiconductor elements to be laminated is not limited to four, as in the present invention. Any required number of two or more can be laminated.”), FIGS. 5-9; *see also* cls. 1, 2, 8

(reciting “a plurality of wiring substrates” and “plurality of conductive via insulating substrates”). FIG. 8 below shows a four-layered structure with a semiconductor element 25 embedded in each substructure layer. *Id.*, [0021].

FIG. 8

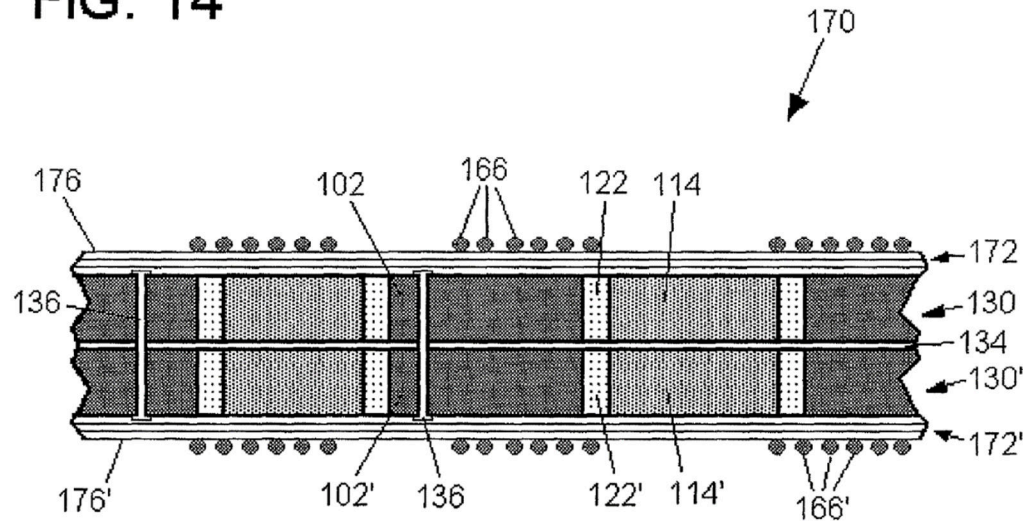


APPLE-1016, FIG. 8

210. Yet another prior art example as corroborating evidence is Vu (U.S. patent application publication No. 2002/0020898, filed on June 18, 2001 and published on February 21, 2002). Vu describes microelectronic substrates with a plurality of microelectronic devices encapsulated in each microelectronic substrate core. *E.g.*, APPLE-1008, [0019]-[0027] (short descriptions of FIGS. 9-17 showing a “dual substrate assembly”), [0045]-[0057], FIGS. 9-17. For example, FIG. 14 reproduced below illustrates a plurality of microelectronic devices 114 and 114’

embedded in each of the two substrate layers (130 and 130') of a dual substrate assembly.

FIG. 14



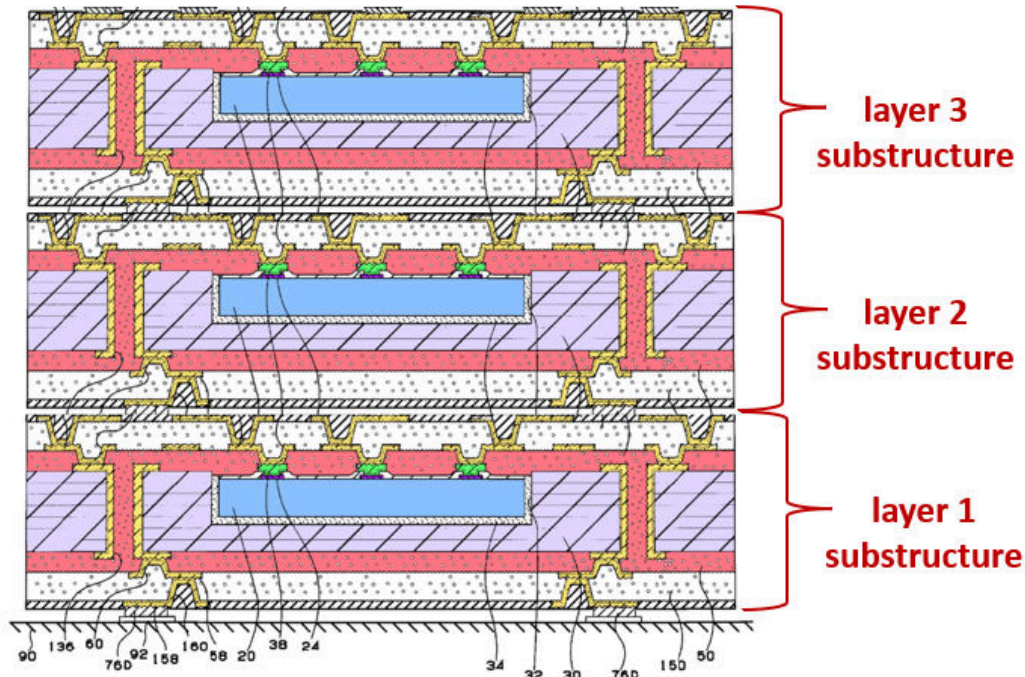
APPLE-1008, FIG. 14

211. This is consistent with the examiner's analysis and decision during the original prosecution, "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and a second circuit board substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art." APPLE-1002, 107-110 (citing *St. Regis Paper Co. v. Bemis Co.*, 193USPQ8). The applicant did not dispute this analysis in its response to the office action.

212. Based on my review of the references, a POSITA would have understood and found obvious that a plurality of Sakamoto's wiring boards are

beneficially stacked on top of each other, with the layers of these substructures mechanically and electrically connected to each other, through the vias (e.g., vias 60, 160) and through holes (e.g., through-holes 136) within each substructure layer and the connection mechanisms between substrates, to achieve the desired higher functionality, high-density, improved performance, reduced manufacturing cost, space saving, and short-distance wiring.

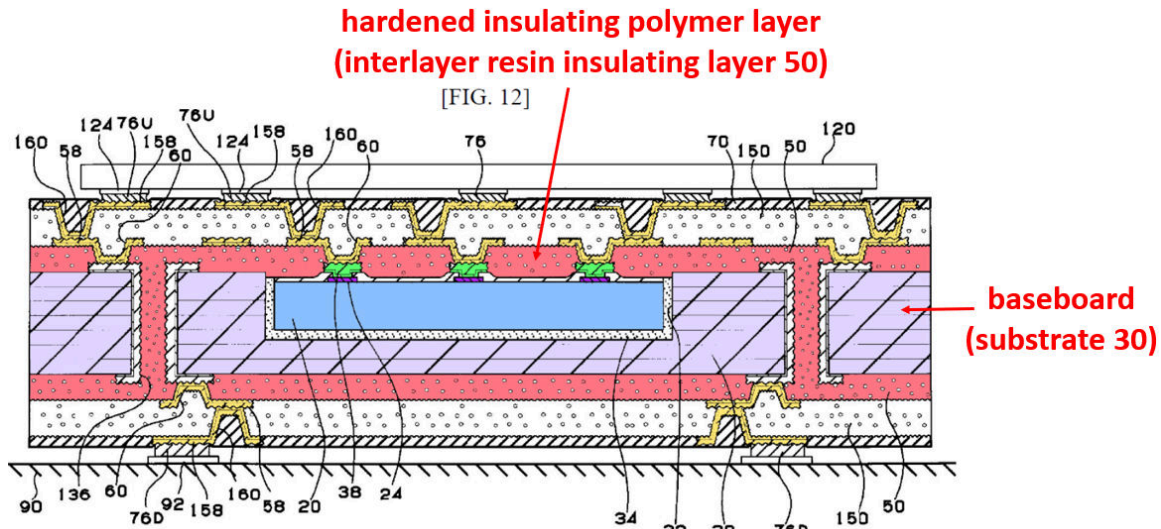
213. I note that this multi-layered configuration would have required only the same techniques already disclosed in Sakamoto for connecting to “external substrates” such as “motherboards and daughterboards,” including the use of “BGA, Solder bumps, and PGA (conductive connection pins),” among other common and routine mounting methods for high-density circuitry semiconductor devices. APPLE-1004, [0011], [0069], [0070]. The composite figure below based on Sakamoto’s FIG. 12 illustrates this multi-layered configuration with three similar substructure layers on top of each other, where layer 1 substructure and layer 2 substructure correspond to the claimed first circuit board substructure and second circuit board substructure, respectively.



Composite Based on APPLE-1004, FIG. 12 (Annotated)

[12a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

214. Sakamoto provides element [12a]. Sakamoto's circuit board has an insulating material layer including a baseboard (e.g., "substrate 30") and a hardened insulating polymer layer (e.g., "interlayer resin insulating layer 50"). For example, Sakamoto's "substrate 30" made of insulating material and "interlayer resin insulating layer 50" together provide an insulating material layer, as claimed. APPLE-1004, [0001], [0003], [0011], [0053], [0056]-[0057], [0078], FIG. 12. The annotated FIG. 12 below shows the combination of Sakamoto's substrate 30 and the interlayer resin insulating layer 50.



APPLE-1004, FIG. 12 (Annotated)

215. Sakamoto discloses element [1a] in a second manner, where Sakamoto's lower interlayer resin insulating layer 150 on the interlayer resin insulating layer 50, together with "substrate 30" and upper "interlayer resin insulating layer 50" likewise provide an insulating material layer, having a first side on the lower side of the lower interlayer resin insulating layer 150.

216. As I discussed previously in analysis of [12pre], Sakamoto's circuit board includes a baseboard (e.g., "substrate 30"). Further, Sakamoto's interlayer resin insulating layer 50 provides a hardened insulating polymer layer, as claimed. APPLE-1004, [0017], [0030], [0042]-[0043]. For example, Sakamoto describes example resins used for the interlayer resin insulating layer 50. *Id.*, [0030] (example material includes "thermosetting cycloolefin resin"), [0042] ("an epoxy resin can be used for the interlayer resin insulating layer 50 instead. This epoxy resin contains a poorly soluble resin, soluble particles, a curing agent, and other

components”), [0047] (“Specific examples of soluble resin particles include those composed of epoxy resins, phenol resins, polyimide resins, polyphenylene resins, polyolefin resins, and fluorine resins, and the particles may be composed of one of these resins or a mixture of two or more these resins.”), [0053]-[0060]. A POSITA would have recognized these examples as various polymers.

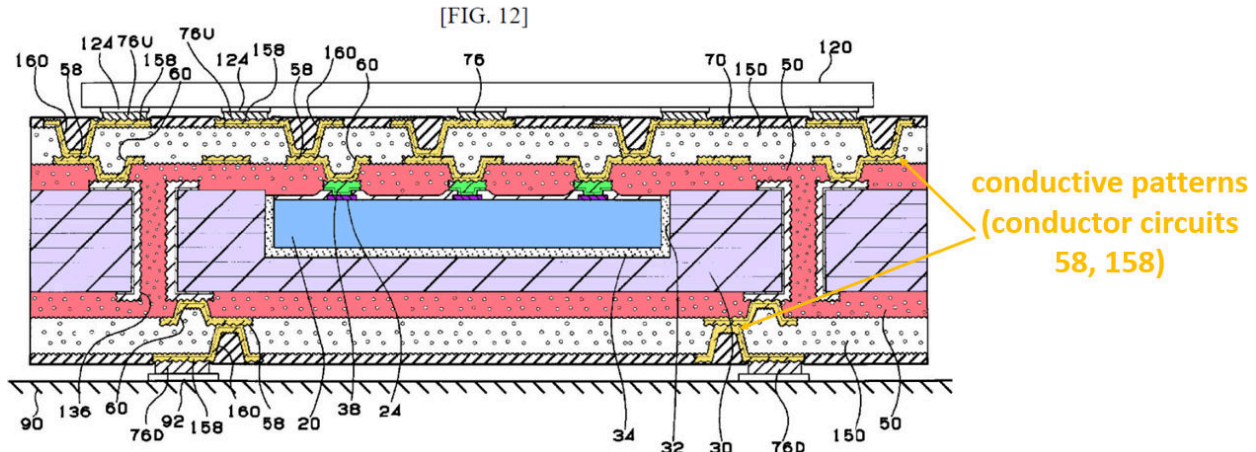
217. Sakamoto further describes that the epoxy resin of the interlayer resin insulating layers (including layers 50 and 150) contains “a curing agent,” and the wiring board goes through various heat treatments. *Id.*, [0042], [0053]; *see also*, [0054] (“heat cycle conditions”), [0058] (examples of “curing agents”), [0059] (“curing of the resin film” of the interlayer resin insulating layers). A POSITA would have understood and found it obvious that, interlayer resin insulating layers 50 and 150 are hardened through chemical and thermal curing. Thus, Sakamoto’s interlayer resin insulating layer 50 is a hardened insulating polymer layer.

[12b] conductive patterns on both sides of the insulating material layer;

218. Sakamoto provides element [12b]. Sakamoto’s circuit board has conductive patterns (e.g., “conductor circuit 58,” “conductor circuit 158”) on both sides of the insulating material layer (e.g., “substrate 30” and upper “interlayer resin insulating layer 50” together, and alternatively also including lower interlayer resin insulating layer 150 on the interlayer resin insulating layer 50). For example, Sakamoto describes a “conductor circuit 58” that is “formed in an interlayer resin

insulating layer 50,” and a “conductor circuit 158” that is “formed in interlayer resin insulating layer 150.” APPLE-1004, [0017]; *see also id.*, [0005]-[0007] (“providing a via on the IC chip pad by photoetching or laser to form a conductor circuit that is a conductor layer, and then repeatedly forming the interlayer insulating layer and the conductor layer to provide a multilayer printed wiring board”).

219. Sakamoto explains that these conductor circuit layers are made of “a double-sided copper-clad laminate” or made of an electroless plated film and an electrolytic plated film with a thickness of 16 μm . *Id.*, [0012] (“a double-sided copper-clad laminate... can also be used” for “[r]esin substrates for incorporating electronic components such as IC chips used in the present invention”), [0015], [0027]-[0028], [0032]-[0037] (describing the formation of the conductor circuit 58 made of an electroless plated film 52 and an electrolytic plated film 56, having a thickness of 16 μm , and repeating the same steps to form additional interlayer resin insulating layers 150 and conductor circuits 158 on top), [0062], FIGS. 4-6, 9-12. The conductor circuit layers 58 and 158 are patterned through photoetching or laser and thus provide the claimed conductive pattern layers. The annotated FIG. 12 below illustrates this configuration, with conductor circuits 58 and 158 (the recited conductive patterns) on both sides of the wiring board.

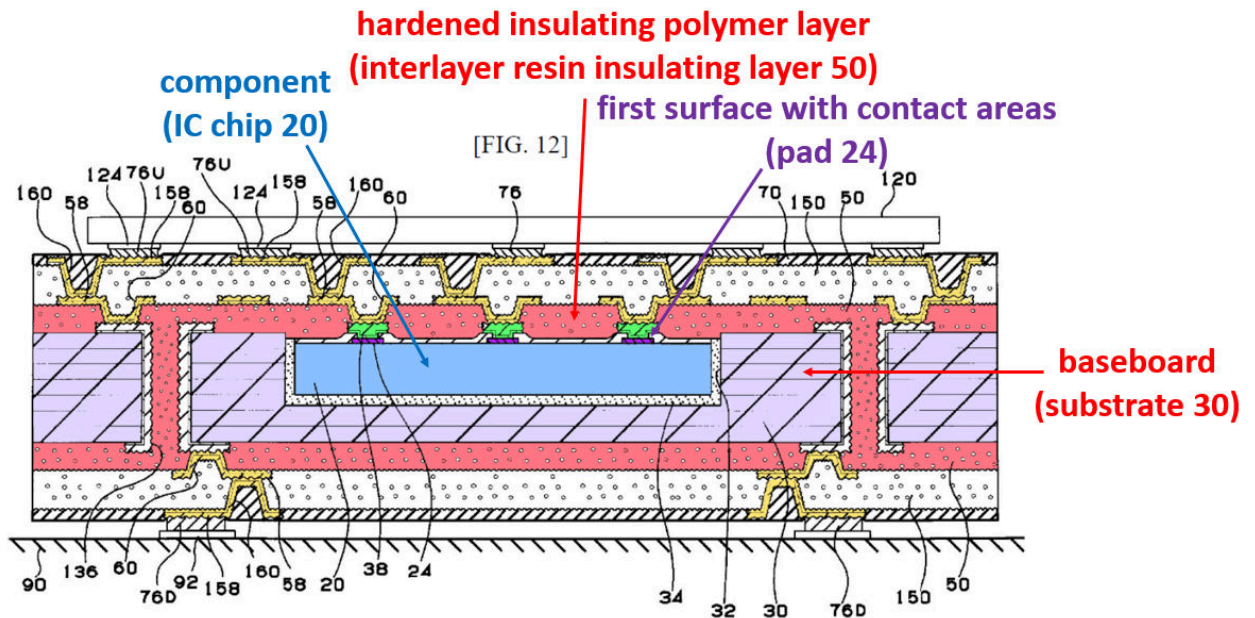


APPLE-1004, FIG. 12 (Annotated)

[12c] at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and

220. Sakamoto provides element [12c]. Sakamoto's circuit board has at least one microcircuit (e.g., "IC chip 20") embedded in the insulating material layer (e.g., in "substrate 30"), the embedded microcircuit having contact areas (e.g., "die pads 24") on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer (e.g., "interlayer resin insulating layer 50"), the at least one microcircuit being inside the insulating material layer in a hole in the baseboard (e.g., recessed portion 32 in core substrate 30) and having the first surface against the hardened insulating polymer layer. For example, as I previously discussed, for [12pre] and [12a], Sakamoto describes "an electronic component such as an IC chip" (e.g., "IC chip 20") (the recited microcircuit) embedded in an opening, through-hole, or counterbore (e.g., recessed

portion 32) in a resin insulating substrate (e.g., in substrate 30 as part of the recited insulating material layer). Again, integrated circuit (IC) chips are microcircuits. §VIII.A, analysis of element [12c]. The annotated FIG.12 below shows this configuration, with IC chip 20 (the recited microcircuit) inside substrate 30 (as part of the recited insulating material layer).



APPLE-1004, FIG. 12 (Annotated)

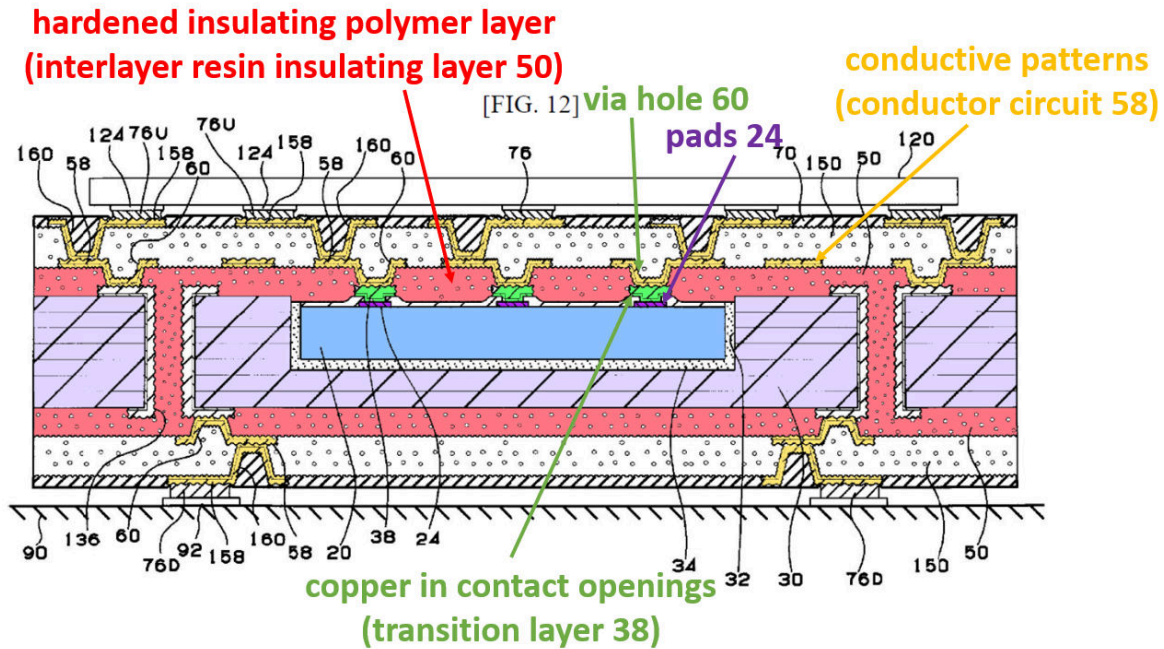
221. IC chip 20 has “die pads 24” on an active surface. APPLE-1004, Abstract, [0018] (“The IC chip 20 is covered with an IC protective film (passivation + polyimide) 22, and die pads 24 forming input/output terminals are provided in openings in the IC protective film 22.”), FIG. 12. The “die pads 24” thus correspond to the contact areas as claimed, and the active surface of the IC chip where the die pads are provided is the first surface as claimed.

222. Based on my knowledge and experience in the field, a POSITA would have found it obvious to omit the IC “protective film (passivation + polyimide) 22” that covers the active surface of the IC chip 20 and has openings for the die pads 24. APPLE-1004, [0018], FIG.12. A POSITA would have found it obvious, based on Sakamoto’s description, that the manufacturing process of the IC chip 20 and the module would have been simplified by omitting this protective film by reducing the number of manufacturing steps and material components. Indeed, a POSITS would have recognized that an additional protective film made of passivation and polyimide layer is not necessary, especially given that the interlayer resin insulating layer 50 grown on top of the first surface of the IC chip already provides the desired protection that a protective film provides. In the resulting device, the interlayer resin insulating layer 50 is in direct contact with and against the first surface of IC chip 20 (without including protective film 22).

[12d] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

223. Sakamoto provides element [12d]. Sakamoto’s circuit board includes contact openings in the hardened insulating polymer layer (e.g., “interlayer resin insulating layer 50”) and copper in the contact openings for forming electrical contacts between the contact areas (e.g., “die pads 24”) of the microcircuit (e.g.,

“IC chip 20”) and at least one of the conductive patterns (e.g., conductor circuits 58 and 158 on the second side of the wiring substrate), wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper. For example, Sakamoto describes that “vias are formed in the interlayer insulating layers, and electrical connections are established through the vias.” APPLE-1004, [Claim 1], [Claim 4]. Sakamoto describes “via holes 60,” which are formed in the interlayer resin insulating layers 50 and connected with die pads 24 of the IC chip either directly or through “transition layer 38.” APPLE-1004, Abstract, [0005]-[0007] (“providing vias on the IC chip pads using photoetching or a laser to form a conductor circuit that is a conductor layer”), [0008] (“via holes in interlayer resin insulating layers”), [0067] (“in the third embodiment, the vias 60 are connected directly to the pads 24 without providing a transition layer”), FIGS. 3-6, 9-12. I note that when transition layer 38 is used, it is also in the interlayer resin insulating layer 50 and thus defining an extended opening of the vias, as illustrated in the annotated FIG. 12 below. *Id.*



APPLE-1004, FIG. 12 (Annotated)

224. I note that portions of conductor circuit 58 extending into the via hole 60, either individually or together with and “transition layer 38” when it is used, provide the recited copper in the contact openings for forming electrical contacts between the contact areas (e.g., “die pads 24”) of the microcircuit and at least one of the conductive patterns (e.g., conductor circuits 58). More specifically, portions of conductor circuit 58 extend into the via hole 60, and the transition layer 38 is formed on the contact pads 24 (the recited contact areas) of the IC chip 20, as “an intermediate layer provided for direct connection of an IC chip, which is a semiconductor element, to [conductor circuit 58 of] a printed wiring substrate.” APPLE-1004, [0008].

225. The transition layer is formed of two or more metal layers and is larger than the die pads of the IC chips, such that “electrical connection and

alignment are improved, and via hole processing using a laser or photoetching can be performed without damaging the die pads. Therefore, reliable embedding, housing, storage, and connection of the IC chip to the printed wiring substrate becomes possible.” *Id.*; *see also*, Abstract (“by providing a transition layer 38 on the die pad 24 ... connectivity between and reliability of die pads 24 and via hole 60 can be improved”), [Claim 4], [0007], [0009]-[0010], [0071], FIGS. 3-6, 9-12.

226. Sakamoto also describes an embodiment (third embodiment) where “the vias 60 are connected directly to the pads 24 without providing a transition layer. Because the third embodiment can reduce the number of manufacturing steps compared to the first embodiment, it is less expensive.” *Id.*, [0067].

227. To be clear, these conductors (e.g., portions of conductor circuit 58 extending into via holes 60 and the “transition layer 38,” individually or collectively) are mechanically and electrically connected with the parts of the conductor circuit 58 outside the via hole 60 and on the top surface of the interlayer resin insulating layer 50, as well as with the die pads 24 of IC chip 20.

228. Sakamoto’s copper in the contact openings contains at least one of electrochemically deposited copper and chemically deposited copper. For example, Sakamoto discloses that transition layer 38 is made of copper and comprises at least an “electroless plated film 36” and an “electrolytic plated film 37,” providing a first layer of chemically deposited copper (electroless plating) and

a second layer of electrochemically deposited copper (electrolytic plated) on the first layer of chemically deposited copper. APPLE-1004, [0028]; *see also*, Abstract, [Claim 4], [0007], [0008] (“The transition layer is formed of two or more metal layers”), [0009], [0010], [0014] (“the transition layer can be thickened by electroplating”), [0015] (“When the transition layer is formed by a subtractive process, the metal film is thickened by electroless or electrolytic plating. Types of plating that can be formed include copper, nickel, gold, silver, zinc, and iron. Copper is preferably used from the standpoint of electrical properties, economy, and the fact that the conductor layer, which is a build-up formed later, is composed primarily of copper.”), [0018], [0020]-[0021], [0027] (“Plated film 36 may be formed on the metal film 33 by electroless plating (FIG. 2(B))... Copper is preferably used...”), [0028] (“electrolytic plated film [37] on the electroless plated film 36”), [0031] (“transition layer 38 made of copper”), [0035], [0067], [0069], [0070], [0071], FIG. 2

229. A POSITA would have recognized that “electroplating” such as “electrolytic plating” is an electrochemical plating technique, and that “electroless plating” is a chemical plating technique. In electroplating, an electric current drives a chemical reaction to deposit a layer of metal onto a conductive surface. This process involves immersing the object to be plated (the cathode) and another conductor (the anode) in an electrolyte solution containing metal ions. Unlike

electroplating, electroless plating does not require an external electric current to deposit metal onto a surface. Instead, it relies on a chemical reaction that occurs between the plating solution and the object to be plated.

230. As I previously discussed in the analyses of element [12b], conductor circuit 58 extending into vias 60 in direct contact with die pads 24 (e.g., where a transition layer 38 is not used) is also formed of an electroless plated film 52 (thus, providing the recited chemically deposited copper) and an electrolytic plated film 56 using copper (thus, providing the recited electrochemically deposited copper). APPLE-1004, [0032]-[0037], FIG. 4.

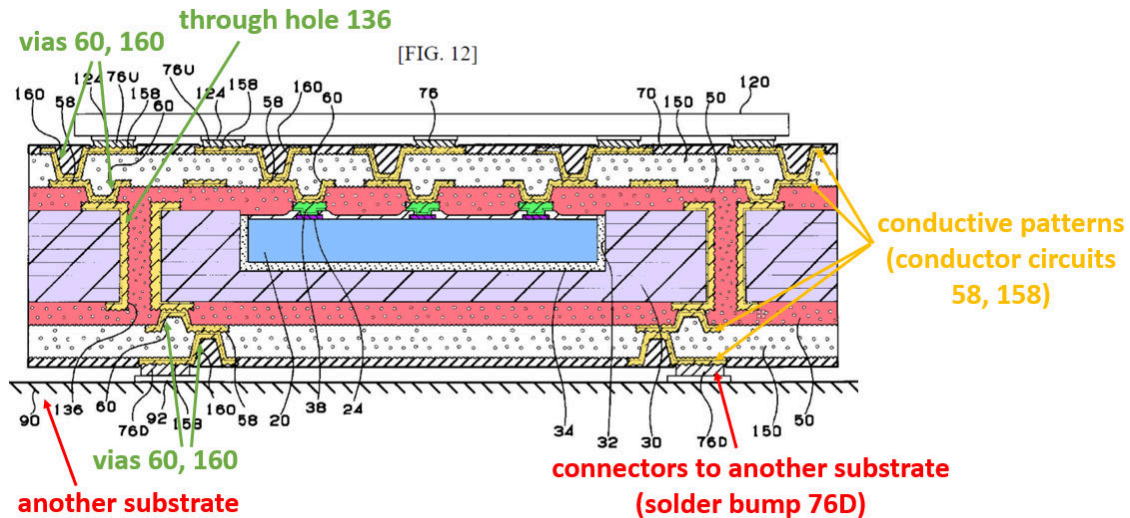
[13] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

231. Sakamoto provides claim [13]. In the multi-layered circuit board based on Sakamoto's teachings, as I previously discussed for claim [12], the at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality. For example, the substructure layers are mechanically and electrically connected to each other, through the vias (e.g., vias 60, 160) and through-holes (e.g., through-holes 136) within each substructure layer, as well as through the connection mechanisms between substrates already described by Sakamoto. *Supra*, §XI.A, analysis of [12pre].

232. For example, each circuit board substructure's conductive patterns (e.g., conductor circuits 58 and 158 on both sides of the wiring board) are electrically connected to each other, through vias 60, 160, and through-holes 136, which are metal-lined holes through substrate 30 and in electrical connection with conductor circuits 58 and 158 through the vias. *See e.g.*, APPLE-1004, [0069] (“The pads 24 of IC chip 20 and the pads 124 of IC chip 120 are connected by means of transition layers 38, vias 60, a conductor circuit 58, vias 160, another conductor circuit 158, and solder bumps 76U. Meanwhile, the pads 124 of IC chip 120 and the pads 92 of a daughterboard 90 are connected by means of solder bumps 76U, a conductor circuit 158, vias 160, another conductor circuit 58, vias 60, through-holes 136, vias 60, another conductor circuit 58, vias 160, another conductor circuit 158, and solder bumps 76U.”), FIG. 12

233. Additionally, Sakamoto describes mechanisms for connecting one wiring substrate to another wiring substrate (e.g., “external substrates” such as “motherboards and daughterboards”), including the use of “BGA, Solder bumps, and PGA (conductive connection pins),” among other common and routine mounting methods for high-density circuitry semiconductor devices. APPLE-1004, [0011], [0069] (describing electrical connections made between various mounted IC chips and with “a daughterboard 90,” through “solder bumps 76U” on the surfaces of the wiring board, as well as the conductor circuits, vias and

through-holes within each substructure wiring board), [0070], FIGS. 9-12. The annotated FIG. 12 below illustrates this configuration, with connection structures on the surfaces and within each circuit board substructure.



APPLE-1004, FIG. 12 (Annotated)

[14] The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.

234. Sakamoto provides claim [14]. Based on my knowledge and experience in the field, a POSITA would have understood from Sakamoto's text that Sakamoto either explicitly teaches or at least contemplates and suggests repeatedly incorporating at least two "electronic components such as IC chips" (the recited at least two microcircuits) some of which with different functions, inside the same resin substrate (the recited insulating material layer) for higher functionality, high-speed operation and shortened wiring length, among other benefits of a high-density circuitry. APPLE-1004, [0006] ("electronic components such as IC chips and capacitors with different functions can be mounted, and a

multi-layer printed wiring substrate with higher functionality can be obtained”),

[0012] (“Resin substrates used to incorporate electronic components such as IC chips used in the present invention...”), [0069], [0070] (“an IC chip 20 and a cache memory 120 can be arranged close to each other ..., enabling high-speed operation of the IC chip. by embedding an IC chip and placing an IC chip on the surface, electronic components such as IC chips with different functions can be mounted, thereby obtaining a multi-layer printed wiring substrate with higher functionality.

Although not shown, a capacitor can also be mounted on the surface. As a result, the IC chip 20, the cache memory 120, and the capacitor can be arranged close to each other, enabling high-speed operation of the IC chip.”), [0071] (“Compared to the conventional IC chip mounting methods, the wiring length running from an IC chip through a substrate to an external substrate can be shortened, and the loop inductance can be reduced.”); *supra*, § XI.A., analyses of claims [12] and [13].

Based on Sakamoto’s description, even if not expressly indicated (which it is), a POSITA would have been prompted to implement the device to have at least two electronic components or IC chips. Based on my knowledge and experience in the field, and my review of Sakamoto, a POSITA would have recognized that doing so would enhance the functionality of the device, and facilitate high-speed operation and shortened wiring length, along with other benefits associated with high-density circuitry.

235. Dudderar and Vu, as introduced previously, provide corroborating evidence that it was a common practice and well known in the field to embed a plurality of microcircuits in an insulating material layer/substrate. *See e.g.*, APPLE-1008, [0044], [0045], [0047], [0053], [0054], FIGS. 1-7, 9-21; APPLE-1014, 1:15-16, 2:44-46, 4:66-5:3, FIGS. 1, 2.

236. Eiji also provides corroborating evidence of embedding multiple electronic components within the same insulating substrate. *See e.g.*, APPLE-1012, Abstract (“a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded”), [0006] (“Note that the electronic components include, but are not limited to, passive components such as capacitors, inductors, filters, and resistors, and active components such as low-noise amplifiers (LNAs), transistors, semiconductor devices, and FETs, as well as SAW filters, LC filters, antenna switch modules, couplers, and diplexers, and any of the components listed above made into chip form. Different types of electronic components can be embedded together in the same through-hole or recessed portion.”), FIG. 1.

[15] The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.

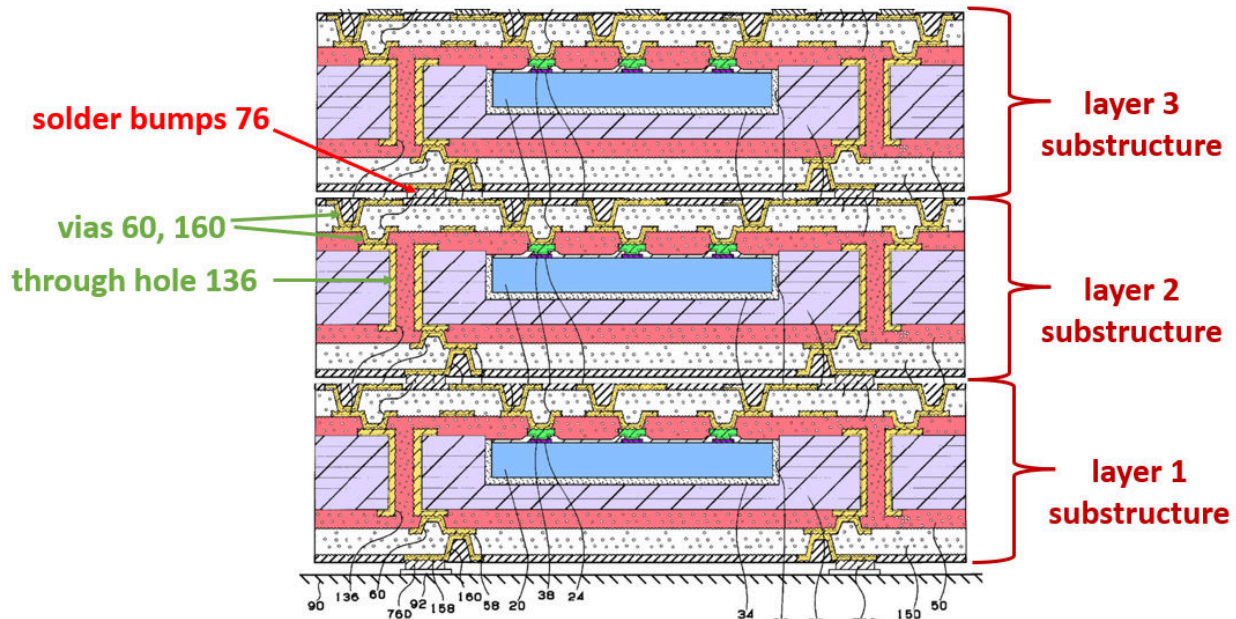
237. Sakamoto provides claim [15]. In the multi-layered circuit board, based on Sakamoto’s teachings as I discussed previously for claims [12] and [13], the at least two circuit board substructures each comprise at least one memory

circuit (e.g., “cache memory”). For example, Sakamoto expressly discloses “a cache memory” as an example, “in a specific example, an IC chip, cache memory, and capacitor can be arranged close to each other by embedding an IC chip with a calculating function as the built-in IC chip and mounting a cache memory and a capacitor on the surface layer.” APPLE-1004, [0006], [0068] (“a cache memory is the IC chip 120 mounted on the surface”), [0070]. I note that although Sakamoto describes the “cache memory” as “IC chip 120” mounted on a surface of the wiring board, based on my knowledge and experience in the field, a POSITA would have understood and found obvious that IC chip 120 (e.g., the “cache memory”), just like IC chip 20, is also embedded in an insulating material layer of each circuit board substructure of a multi-layered circuit board, in accordance with Sakamoto.

[16] The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.

238. Sakamoto provides claim [16]. In the multi-layered circuit board, in accordance with Sakamoto as I previously discussed for claim [12] and [13], at least three circuit board substructures are on top of each other and electrically connected to each other. The annotated composite figure below illustrates this configuration, with three similar circuit board substructures (labeled as layer 1 to layer 3 substructures) stacked on top of each other, also showing the connection mechanisms between two adjacent substructure layers, including the vias (e.g., vias

60, 160) and through-holes (e.g., through-holes 136) within each substructure layer, and connectors (e.g., “BGA, Solder bumps, and PGA (conductive connection pins)”) such as “solder bumps 76” between and electrically connecting neighboring substructure layers. *Supra*, §XI.A., analyses of claims [12] and [13].



Composite Based on APPLE-1004, FIG. 12 (Annotated)

[17pre]-[17d]

239. Sakamoto renders obvious elements [17pre]-[17d] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d].

Supra, §XI.A.

[18] The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.

240. Sakamoto renders obvious claim [18] for at least the same reasons as I discussed previously in the analyses of claims [13] and [16]. *Supra*, §XI.A.

[19pre]-[19d]

241. Sakamoto renders obvious claim [19] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d] and claim [18].

Supra, §XI.A.

[20pre]-[20d]

242. Sakamoto renders obvious claim [20] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12d] and claim [19].

Supra, §XI.A.

[21] The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.

243. Sakamoto renders obvious claim [21] for at least the same reasons as I discussed previously in the analysis of element [12a], Sakamoto's interlayer resin insulating layer 50 (the recited hardened insulating polymer layer) contains epoxy.

Supra, §XI.A.

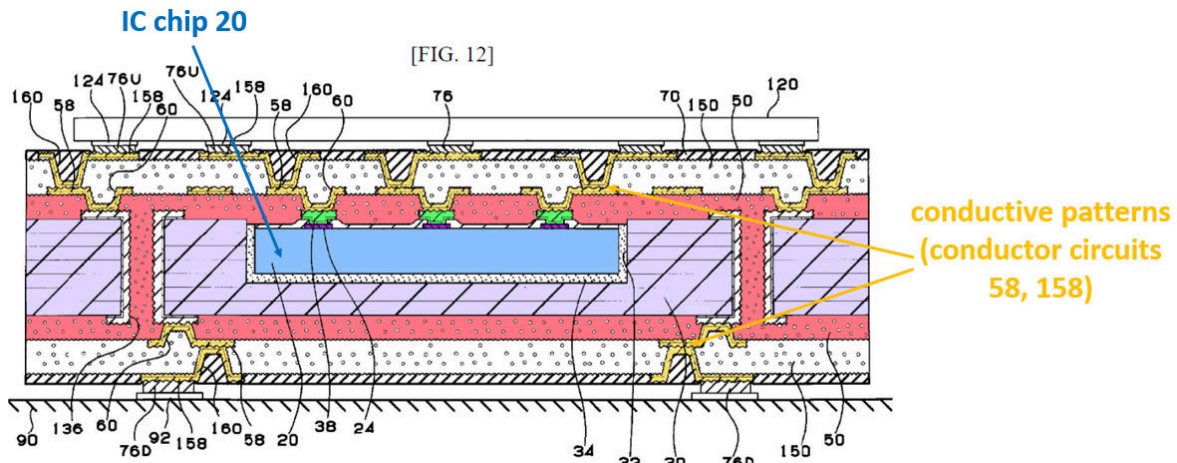
[22] The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.

244. Sakamoto renders obvious claim [22]. As I previously discussed for [12pre] and [12a], Sakamoto's substrate 30 (the recited baseboard) is made of "any material generally used in printed wiring substrates," such as "epoxy resins, BT

resins, and phenol resins impregnating a reinforcing material such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin.” *Id.*, [0012], [0020], [0023] (“an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as glass cloth has been impregnated with a resin such as an epoxy is used as the starting material”). Based on my knowledge and experience in the field, a POSITA would have found glass fibers as an obvious alternative for glass cloth as a reinforcing material for the “glass epoxy resin” of Sakamoto’s substrate 30. Indeed, glass fibers were well-known material commonly used to impregnate with insulating resins of a substrate to increase the strength of the substrate. For example, Eiji provides corroborating evidence of embedding electronic components in an insulating substrate that is made of “a glass-epoxy resin composite material.” APPLE-1012, [0012], Abstract. Eiji describes that “in addition to the glass-epoxy resin composite material described above, the insulating substrate 2 can be made of glass woven fabrics or composite materials of glass fibers and resins such as epoxy resin, polyimide resin, or BT resin having similar heat resistance, mechanical strength, flexibility, and ease of processing.” *Id.*, [0038].

[23] The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.

245. Sakamoto renders obvious claim [23]. *Supra*, §XI.A., analyses of elements [12b]-[12c]. The annotated composite figure below shows IC chip 20 (the recited microcircuit) between the conductor circuits 58, 158 (the recited conductive patterns) on both sides of the wiring board.



APPLE-1004, FIG. 12 (Annotated)

[24] The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

246. Sakamoto renders obvious claim [24]. As I previously discussed for element [12d], Sakamoto's transition layer 38 is made of copper and comprises at least an "electroless plated film 36" (the recited first layer of chemically deposited copper) and an "electrolytic plated film 37" (the recited second layer of electrochemically deposited copper on the first layer of chemically deposited copper). Additionally, Sakamoto's conductor circuit 58 extending into vias 60 in direct contact with die pads 24 (e.g., where a transition layer 38 is not used) is also

formed of an electroless plated film 52 (thus, providing the recited chemically deposited copper) and an electrolytic plated film 56 using copper (thus, providing the recited electrochemically deposited copper). *Supra*, §XI.A., analysis of element [12d].

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

247. Sakamoto renders obvious claim [25]. As I previously discussed for element [12b], Sakamoto describes forming its conductor layers on the both sides of its wiring substrate through various methods, including the use of “a double-sided copper-clad laminate,” and alternatively the formation of an electroless plated film and an electrolytic plated film “with a thickness of 16 μm .” APPLE-1004, [0012], [0007] (“form a conductive circuit that is a conductive layer”), [0032]-[0033] (“the substrate is immersed in an electroless plating solution to form an electroless plated film 52 on the surface of interlayer resin insulating layer 50”), [0034] (“electrolytic plating is performed under the conditions listed below to form an electrolytic plated film 56 with a thickness of 18 μm ”), [0035]-[0036] (“This forms a conductor circuit 58 and vias 60 with a thickness of 16 μm made of the electroless plated film 52 and electrolytic plated film 56.”), [0037] (forming conductor circuit 158 using the same method). *Supra*, §XI.A., analysis of element [12b]. These conductor layers have conductor circuits 58 and 158 and unpatterned

portions both above and below the integrated circuit component 20 (the recited at least one of the microcircuits), and a POSITA would have found it obvious to implement the unpatterned portions of the conductor layers to provide beneficial EMI shielding, thus providing a metal plate, as claimed. Again, as I previously discussed for claim [25] under the McCormack ground (§VIII.A.), Sakamoto's descriptions for its conductive layers are similar to the '909 patent descriptions for forming its "metal plate," metal "film," and "metal foil" (the '909 patent specification appears to use these terms interchangeably without distinction), from "a layer of copper (e.g., c. 5 μm)" such as "an RCC (Resin Coated Copper) foil," on both sides of the circuit board above and below the embedded electronic component.

248. I note that to the extent the '909 patent's description of forming a metal plate in connection with the making of the circuit board's conductive pattern requires growing a thicker metal film from its "metal coating 12" and/or "metal coating 8," Sakamoto also provides it. APPLE-1001, FIGS. 1F, 1J, 4C, 4D (with the structure corresponding to a metal plate above and below the embedded electronic components appearing thicker than the metal films in the same positions in FIG. 4C), 4:40-63, 5:47-6:4, 8:44-9:41. For example, each of Sakamoto's conductive layers "with a thickness of 16 μm ," is substantially thicker than the

'909 patent's metal coating or film of "e.g., c. 5 μm ." APPLE-1004, [0033]-

[0036].

[26] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.

249. Sakamoto provides claim [26]. As I previously discussed for element [12b] and claim [25], each of Sakamoto's conductive layers having conductor circuits 58 and 158, above and below the integrated circuit component 20 (the recited at least one of the microcircuits), provides a metal foil. *Supra*, §XI.A.

[27pre]-[27d]

250. Sakamoto renders obvious [27pre]-[27d] for at least the same reasons that I previously discussed for elements [17pre]-[17d]. *Supra*, §XI.A.

[27e]

251. Sakamoto renders obvious element [27e] for at least the same reasons that I previously discussed for claim [26]. *Supra*, §XI.A.

XII. GROUND 2B: CLAIMS 1-33 ARE OBVIOUS IN VIEW OF THE SAKAMOTO-EIJI COMBINATION

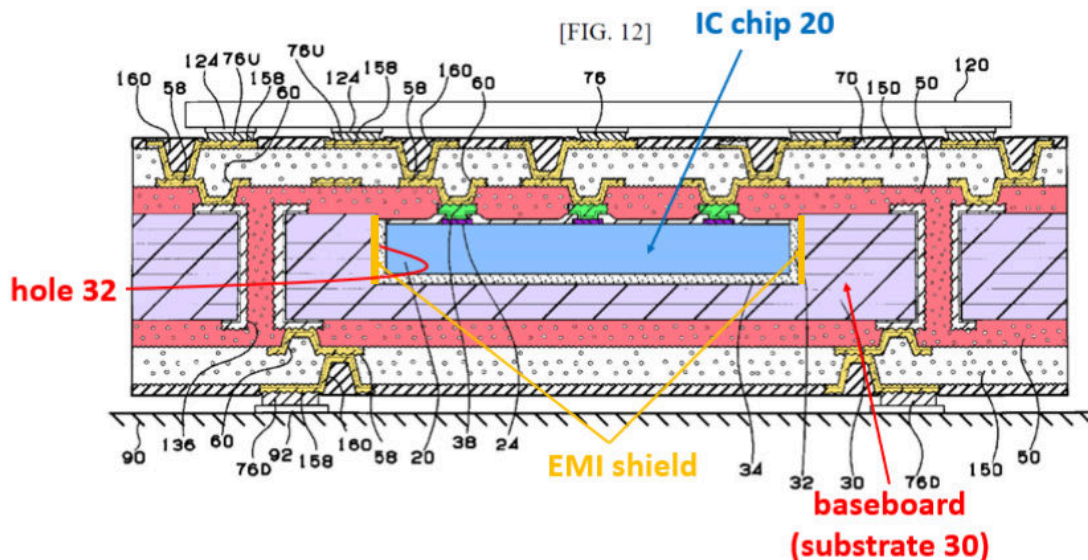
252. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have understood that the teachings of Sakamoto and Eiji render claims 1-33 obvious.

A. The Predictable Combination of Sakamoto and Eiji

253. Based on my knowledge and experience in the field and my review of Sakamoto and Eiji, a POSITA would have been motivated to implement a shield layer on the sidewalls of the hole that the electronic component is embedded in, in accordance with Eiji, in the multilayer printed wiring board in accordance with Sakamoto, to achieve known benefits. For example, Eiji provides suggestions to make the electronic components built into an insulating substrate “less susceptible to external electromagnetic waves,” to “reduce the effects of noise generated by the circuits constituting these electronic components,” and/or to “stabilize the electrical characteristics” of the system, consistent with Sakamoto’s objectives of higher functionality, high-speed operation and improved reliability. APPLE-1012, [Abstract]; *see also*, [0001], [0005]-[0007] (“the wiring of the wiring layer at a position covering the opening to the through-hole or recessed portion in the insulating substrate also serves as the shielding layer”), [0009], [0011]-[0012] (“Wiring layers 26, 27, including wiring layers 26a and 27a which also serve as shielding layers, are formed in the upper and lower openings to the through-hole 8”), [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1; APPLE-1004, Abstract, [0006] (“components such as IC chips and capacitors with different functions can be mounted, and a multi-layer printed wiring substrate with higher functionality can be obtained.”), [0070]-[0071] (desire for “high-speed operation,” “higher

functionality,” improved “connectivity between and reliability of the die pads and via holes,” shortened wiring length and reduced loop inductance).

254. In the combined Sakamoto-Eiji device, an EMI shield layer composed of a copper plating film that shields electromagnetic waves (e.g., shielding layer 10) is formed on an inner surface of the recessed portion in the core substrate (e.g., recessed portion or hole 32 in core substrate 30 shown in Sakamoto’s FIG. 12), before inserting IC chip, in accordance with Eiji’s teachings. APPLE-1004, [0005]-[0007], [0023]-[0025], [0066]; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.



Composite Based on APPLE-1004, FIG. 12 (Annotated)

255. A POSITA would have been prompted to utilize EMI shielding in the multilayer printed wiring substrate with embedded components, in accordance with

Eiji. As I describe in more detail in the following paragraphs, multiple reasons confirm this analysis:

256. First, a POSITA would have been motivated to combine Sakamoto and Eiji to alleviate the common and well-known problem of electromagnetic interference caused by external electromagnetic waves, reduce influence by noise from circuits composed of various electronic components, and/or to stabilize electric characteristics of the entire system.

257. Sakamoto already teaches incorporating an electronic component such as an IC chip 20 in an opening, through-hole, or counterbore (e.g., “recessed portion 32” or “through-hole” 32) in the core insulating substrate, and that multiple components can be included in close arrangement. APPLE-1004, [0066]; *see also*, [0005] (“providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance”), [0007], [0023]-[0025].

258. Sakamoto further describes “electronic components such as IC chips with different functions can be mounted,” including, as one example, an IC chip 20, a cache memory 120, and a capacitor mounted both inside and on the surface of the wiring board and “arranged close to each other, enabling high-speed operation of the IC chip.” *Id.*, [0006] (“electronic components such as IC chips and capacitors with different functions can be mounted, and a multi-layer printed

wiring substrate with higher functionality can be obtained. In a specific example, an IC chip, cache memory, and capacitor can be arranged close to each other by embedding an IC chip with a calculating function as the built-in IC chip and mounting a cache memory and a capacitor on the surface layer.”), [0011] (desire to “shorten wiring lengths and reduce loop inductance”), [0069]-[0071] (“the IC chip 20, the cache memory 120, and the capacitor can be arranged close to each other, enabling high-speed operation of the IC chip”).

259. A POSITA would have been motivated to mitigate against the problems due to external electromagnetic waves or noise generated by the circuits constituting the electronic components, especially where multiple components are arranged close to each other. APPLE-1012, Abstract; APPLE-1014 (corroborating prior art describing “EMI problems” “disruptive to the proper operation of circuit components located near the source of the EMI,” and a solution of “EMI metallization shield” including above, below and along the inside walls of a cavity for accommodating electronic components); APPLE-1016, [0022] (corroborating prior art describing “shielding effect” against EMI); APPLE-1015, 4:7-9, 5:24-36, 12:39-50 (corroborating prior art describing the use of a “shield layer” or “shield section” so that “noise does not penetrate to the electrical element contained inside the housing section of the multilayer substrate”). Eiji provides a known technique that would have been recognized to further “stabilize the electrical characteristics”

of the system. APPLE-1012, Abstract, [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], cls. 1, 6, FIG. 1.

260. Second, combining Sakamoto and Eiji would have been a common application of known techniques (forming an EMI shield layer on the sidewalls of a through hole or cavity provided in an insulating substrate for incorporating an electronic component) to a known electronic module system (Sakamoto's multilayer printed wiring board having an opening or recessed portion 32 in insulating substrate 30 to accommodate an electronic component such as IC chip 20 between wiring layers). Based on my knowledge and experience in the field and my review of Sakamoto and Eiji, a POSITA would have had a reasonable expectation of success modifying Sakamoto with Eiji, because of the similarities between the systems. For example, both Sakamoto and Eiji describe multilayer wiring boards with electronic components embedded inside holes of an insulation substrate. APPLE-1004, Abstract; APPLE-1012, Abstract.

261. Based on my analysis, a POSITA would have recognized that applying Eiji's suggestions to Sakamoto's electronic module would not have significantly altered or hindered the functions performed by Sakamoto's electronic module. Moreover, based on my knowledge and experience in the field, a POSITA would have found making the proposed modifications to be straightforward, since the modifications would have been implemented largely by

adding a metal layer on the sidewalls of the hole. Eiji already demonstrates this configuration to be successful. And the use of shield layers against EMI problems was known. *See e.g.*, APPLE-1014 (corroborating evidence to show the use of a “EMI metallization shield” above, below and along the inside walls of a cavity for accommodating electronic components to address EMI problems). I note that the above reasons further highlight that Sakamoto and Eiji are directed to analogous subject matter. They are in the same field of endeavor and pertinent to the problems addressed above that are encountered in semiconductor packaging and manufacturing.

B. Analysis of Sakamoto and Eiji with Respect to Claims 1-33

262. As shown in this section, the Sakamoto-Eiji combination, when predictably combined for at least the reasons described above, provides claims 1-33.

[1pre]-[1c]

263. Sakamoto-Eiji renders obvious elements [1pre]-[1c] for at least the same reasons as I discussed previously in the analyses of elements [12pre]-[12c]. *Supra*, §XI.A.

264. I note that the Sakamoto-Eiji provides each element of, and renders obvious, claims 1-11 and 28-33 even without modification to utilize multiple

circuit board substructures on top of each other that I describe with reference to claims 12-27.

[1a] an insulating material layer including a baseboard and a hardened insulating polymer layer;

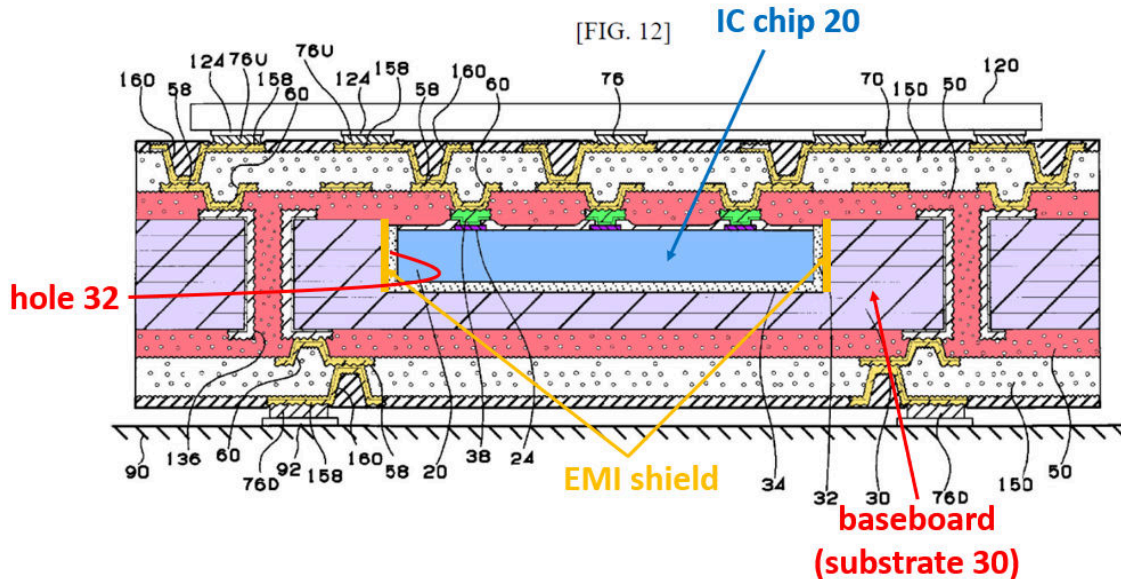
265. Sakamoto-Eiji provides element [1a]. Eiji provides express teaching for use of glass fibers reinforced epoxy resin for an insulating substrate, as it describes, “the insulating substrate 2 can be made of glass woven fabrics or composite materials of glass fibers and resins such as epoxy resin.” APPLE-1012, [0038], [0012]. *Supra*, §XI.A, analyses of element [12a] and claim [22].

[1d] conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and

266. Sakamoto-Eiji provides element [1d]. The Sakamoto-Eiji combination’s IC chip (e.g., IC chip 20) is located in a hole (e.g., recessed portion or through-hole 32) in the insulating substrate 30, which corresponds to the baseboard of the claimed insulating material layer. *Supra*, § XII.A. (Sakamoto-Eiji combination). Further, Sakamoto-Eiji includes a metal foil (e.g., a copper plating film), which is a conductive material, formed on the inner surface of and covering the sidewalls of the hole 32, to provide a shielding layer against EMI, in accordance with Eiji’s teachings. *Id.*

267. Based on my analysis of Sakamoto, Eiji and the ’909 patent, I note that Sakamoto-Eiji’s shielding layer material and configuration, in accordance with

Eiji's teachings, is just like the '909 patent's description for growing its metal foil on the sidewalls of the holes by copper plating. *Compare* APPLE-1012, [0017] ("electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole") *with* APPLE-1001, 3:61-4:9 ("metal 4" "is grown into the through holes" at Stage C (FIG. 1C), by "coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method... The metal can thus be grown using a wet-chemical method, ... Alternatively, the conductive layer 4 can be made, for example, by filling the through holes with an electrically conductive paste."); *see also* APPLE-1012, Abstract, [0012]. Note that the '909 patent describes that the same method for growing metal 4 is used for growing the metal foil covering the side walls of the holes to accommodate the electronic components. APPLE-1001, 8:39-46 ("the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components"). The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1004, FIG. 12 (Annotated)

268. Again, I note that other references corroborate the use of a metal foil covering the sidewalls of a hole or cavity for embedding electronic components to provide EMI shielding. *Supra*, §IX.B., analysis of element [1d] under the McCormack-Eiji ground.

[1e] contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

269. Sakamoto-Eiji provides element [1e]. Other than the reasons I described under the Sakamoto ground, I note that Eiji also provides express teaching of “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate. APPLE-1012, [0017]; *supra*, §XI.A, analysis of element [12d].

[2] The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

270. The Sakamoto-Eiji combination renders obvious claim [2], for at least the same reasons as I discussed previously in the analysis of element [12a], the interlayer resin insulating layer 50 contain “epoxy resin.” *Supra*, §XI.A.

[3] The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.

271. The Sakamoto-Eiji combination renders obvious claim [3]. For example, Sakamoto describes that “an epoxy resin can be used for the interlayer resin insulating layer 50” (the recited hardened insulating polymer layer). APPLE-1004, [0042]; *see also id.*, [0030] (interlayer resin insulating layer 50 is “laminated on the substrate” 30). As I previously discussed, substrate 30 (the recited baseboard) of the combined system contains glass-fiber reinforced epoxy. *Supra*, §XI.A., analysis of [12pre] and claim [22], §XII.B., analysis of element [1a]. Based on my knowledge and experience in the field and my review of Sakamoto and Eiji, a POSITA would have been prompted to similarly impregnate the epoxy resin of the interlayer resin insulating layer 50 with glass fibers, to achieve similar physical properties, such as thermal expansion coefficient, mechanical strength, flexibility, to those of the substrate 30, with the benefits of reduced mechanical stresses caused by mismatch of these physical properties during heat cycles and

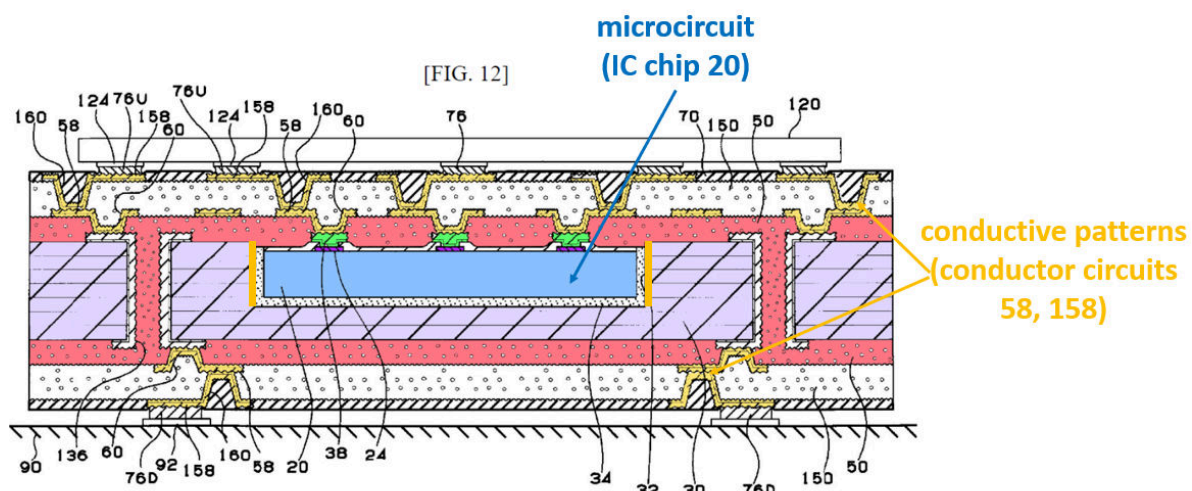
mechanical maneuvers during the manufacturing process, and enhanced reliability of the electronic device as a whole.

[4] The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

272. The Sakamoto-Eiji combination renders obvious claim [4]. As I previously discussed for elements [1a], [12pre] and claim [22], Sakamoto-Eiji's substrate 30 (the recited baseboard) contains glass fibers impregnated in epoxy resin. *Supra*, §XI.A., §XII.B.

[5] The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.

273. The Sakamoto-Eiji combination renders obvious claim [5]. The annotated composite figure below illustrates this configuration, with IC chip 20 (the recited microcircuit) located between conductor circuits 58, 158 on both sides of the wiring board. *Supra*, §XI.A., analyses of elements [12pre]-[12c], §XII.B., analyses of elements [1pre]-[1c].



Composite Based on APPLE-1004, FIG. 12 (Annotated)

[6] The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.

274. Sakamoto-Eiji provides claim [6]. The Sakamoto-Eiji combination includes a filler material in the hole between the metal foil and the component to secure IC chip 20 in place, in accordance with both Sakamoto's and Eiji's teachings. For example, Sakamoto describes "an adhesive material 34" applied to recessed portion or hole 32 before "IC chip 20 is placed on the adhesive material 34" in the recessed portion or hole. APPLE-1004, [0024] (application of "adhesive material 34" using a printer or potting). Based on my knowledge and experience in the field, a POSITA would have recognized that the "adhesive material 34" provides a filler material in the hole between the metal foil and the IC chip 20. Additionally, and consistent with Sakamoto's teaching, Eiji also describes a "resin 16, which is primarily epoxy resin," which is a filler material between the metal foil and the components to secure each component at "a predetermined location in the through-hole." APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], cls. 2, 7, FIGS. 1, 3.

275. One corroborating reference on the use of a filler material is Degani (introduced above), which describes filling the cavity with an encapsulating material, "such as an epoxy resin," "which protects the chips, interconnections between the chips and the substrate, interconnections between the substrate and the

PWB, and surfaces of the substrate exposed within the cavity.” APPLE-1019, 2:24-26, 3:4-56, 5:24-6:3, cls. 2, 6. Another corroborating reference is U.S. Patent Application Publication No. 2002/0020898 to Vu, et al., titled “Microelectronic Substrates with Integrated Devices”, filed June 18, 2001 and published February 21, 2002. APPLE-1008, Face. Vu describes encapsulating material 122 in an opening of a substrate to secure electronic components disposed therein. *Id.*, [0037], [0042] (“The encapsulation material 122 secures the microelectronic device 114 within the microelectronic substrate core 102 and provides mechanical rigidity for the resulting structure...”).

[7] The circuit board of claim 6, wherein the filler material contains epoxy.

276. Sakamoto-Eiji provides claim [7]. The Sakamoto-Eiji’s filler material in the hole contains epoxy. As I previously discussed for claim [6], at least Eiji’s “resin 16,” which is a filler material in a hole for securing electronic components in place in the hole contains “primarily epoxy resin.” *Supra*, §XII.B., analysis of claim [6]. Thus, Sakamoto-Eiji’s filler material, implemented in accordance with Eiji’s teaching of its “resin 16,” contains epoxy.

[8pre] The circuit board of claim 1, wherein

277. Sakamoto-Eiji provides [8pre]. *Supra*, §XII.B., analysis of claim [1].

[8a] said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and

278. Sakamoto-Eiji provides element [8a]. In addition to what I previously discussed for claim [14] (§XI.A.), Eiji also describes embedding multiple electronic components in the same substrate. *See e.g.*, APPLE-1012, Abstract, [0006] (different types of electronic components can be embedded either in different or the same through-holes or recessed portions), FIGS. 1-7.

[8b] the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.

279. The Sakamoto-Eiji combination renders obvious element [8b]. For example, when several electronic components such as IC chips (the recited microcircuits) are disposed in the same insulating substrate of the combined system, these IC chips are connected to each other through portions of conductor circuit 58 extending into via holes 60 and/or transition layer 38 (the recited conductors in the contact opening), depending on whether transition layer 38 is used, that are electrically connected to both the die pads 24 of each IC chip and conductor circuit 58 outside of via holes 60, also to conductor circuit 158. *Supra*, §XII.B., analyses of elements [1e] and [8a], §XI.A., analysis of element [12d].

[9] The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

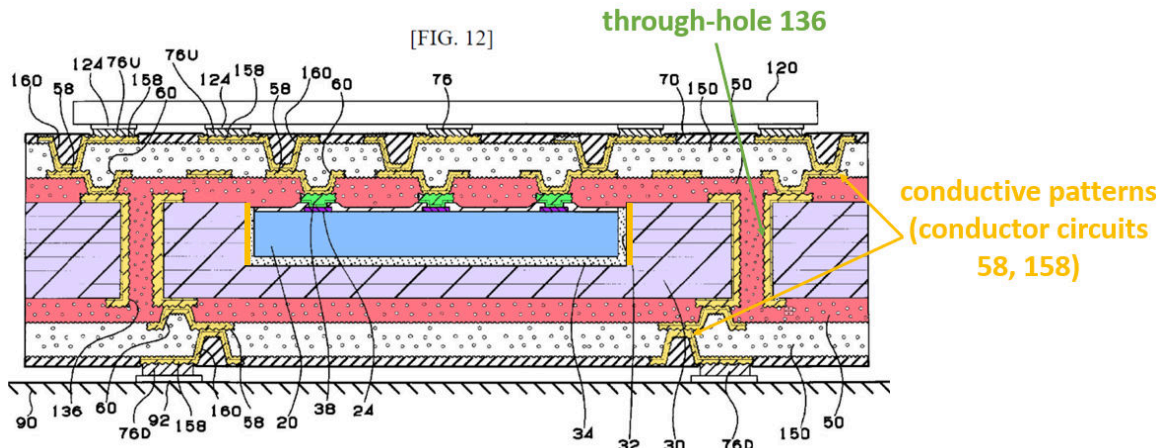
280. Sakamoto-Eiji provides claim [9]. As I previously discussed for elements [12d] (§XI.A.) and [1e] (§XII.B.), transition layer 38 made of copper as

part of the recited copper in the contact openings is composed of at least an “electroless plated film 36” (the recited first layer of chemically deposited copper) and an “electrolytic plated film 37” (the recited second layer of electrochemically deposited copper on the first layer of chemically deposited copper); additionally, conductor circuit 58 extending into vias 60 (also part of the recited copper in the contact openings) is also formed of an “electroless plated film 52” and an “electrolytic plated film 56 using copper.”

281. Moreover, Eiji similarly describes formation of conductors on the inner surfaces of through-holes in an insulating substrate through “electroless copper plating and electrolytic copper plating.” APPLE-1012, [0017].

[10] The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

282. Sakamoto-Eiji provides claim [10]. The combined system comprises an electrically conducting feed-through (e.g., metal-lined through-holes 136) between the conductive patterns (e.g., conductor circuits 58 and 158) on the both sides of the insulating material layer of the wiring board. *Supra*, §XII.B., analysis of claim [2]. The annotated composite figure below illustrates this configuration.



Composite Based on APPLE-1004, FIG. 12 (Annotated)

[11pre]-[11b]

283. The Sakamoto-Eiji combination renders obvious elements [11pre]-[11b] for at least the same reasons that I previously discussed in the analyses of elements [8pre]-[8b] (§XII.A.).

[12]-[27]

284. The Sakamoto-Eiji combination renders obvious these claims for at least the same reasons that I previously discussed for these claims under the Sakamoto ground (§XI.A.). Additionally, for elements [12d], [17d], [19d], [20d], [27d] and claim [24], which recite the same or similar features relating to chemically and/or electrochemically deposited copper in the contact openings, Eiji also provides express teaching of “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate. APPLE-1012, [0017]. *Supra*, §XII.B., analysis of element [1e].

[22] The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.

285. The Sakamoto-Eiji combination renders obvious claim [22]. *Supra*, §XII.B., analysis of claim [4], §XI.A., analysis of claim [20].

[25] The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.

286. Sakamoto-Eiji provides claim [25]. In addition to what I previously discussed for claim [25] under the Sakamoto ground (§XI.A.), and consistent with Sakamoto's teachings, Eiji also describes metal wiring layers (e.g., 26, 27) formed above and below embedded electronic components in an insulating substrate through lamination of and plating over a "copper foil," e.g., by electroless and electrolytic copper plating over "copper foil 5, 6 that is several 10 μm thick." APPLE-1012, [0017], [0013] ("insulating layers ... made of epoxy resin and wiring layers ... made of Cu are alternately laminated above the front surface 3 of the insulating substrate 2"), [0021]-[0022], FIG. 2(A). As I already noted under the McCormack-Eiji ground (§IX.B., analysis of claim [25]), Eiji's wiring layers are each more than (due to plating on top of the copper foil) "several 10 μm thick," which is a substantial thickness compared with the '909 patent's metal coating of "e.g., c. 5 μm ."

[26]-[27]

287. Sakamoto-Eiji provides claims [26] and [27]. As I previously discussed for these claims under the Sakamoto ground (§XI.A.), at least one of the combined system's conductor layers (e.g., conductor layers having conductor circuits 58 and 158) below IC chip 20 is also a metal foil, e.g., a plated film of "a thickness of 16 μm ." In addition, as I discussed for claim [25] (§XI.A and §XII.B), Eiji's also provides express teaching of laminated and plated "copper foil" that is more than "several 10 μm thick," for forming its wiring layers above and below the embedded electronic components.

[28] The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

288. Sakamoto-Eiji provides claim [28]. As I previously discussed for element [1d], the combined system's shield layer on the sidewalls of recessed portion or through-hole 32 in the core substrate 30 (the recited baseboard) is "composed of a copper plating film" (the recited metal foil as the conductive material). *Supra*, §XII.B.

[29] The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.

289. Sakamoto-Eiji renders obvious claim [29]. Based on my knowledge and experience in the field, and my analysis of Sakamoto and Eiji, a POSITA would have been prompted to provide the metal foil on the sidewalls in the form of an unbroken metal foil that surrounds the microcircuit in a lateral direction of the

circuit board, effectuating and enhancing the shielding objective of the metal foil.

Supra, §XII.B, analyses of element [1d] and claim [28].

[30]-[32]

290. Sakamoto-Eiji renders these claims obvious for at least the same reasons that I previously discussed for claim [25], at least one of the conductor layers (e.g., conductor layers having conductor circuits 58 and 158 and unpatterned portions) both above and below the embedded IC chip 20 includes a metal plate.

Supra, §XI.A, §XII.B.

[33] The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

291. The Sakamoto-Eiji combination renders obvious claim [33] for at least the same reasons that I previously discussed for claims [25] and [28]. *Supra*, §XI.A, §XII.B.

XIII. GROUND 2C: CLAIMS 12-27 ARE OBVIOUS IN VIEW OF THE SAKAMOTO-EIJI-IMOTO COMBINATION

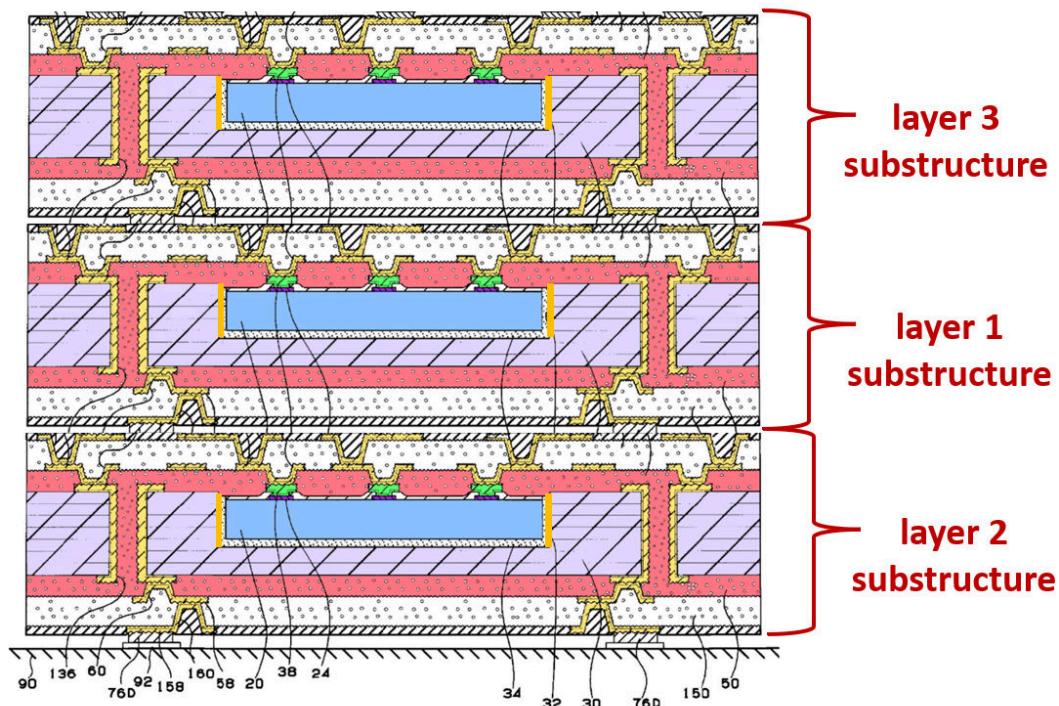
292. For the reasons I describe in detail below, and based on my review of the '909 patent and its file history, and the prior art references cited herein, a POSITA would have understood that the teachings of Sakamoto, Eiji and Imoto render obvious claims 12-27. As I discuss in more detail below, Imoto describes multi-layered circuit board structures, and thus provides additional express teachings relevant to the “multi-layered” elements of independent claim 12 and its dependent claims.

A. The Predictable Combination of Sakamoto, Eiji and Imoto

293. Based on my knowledge and experience in the field and my review of Sakamoto, Eiji and Imoto, a POSITA would have been motivated to combine the teachings of Sakamoto, Eiji and Imoto to provide a high-density, multi-layered structure with EMI shielding effect. Each of these references relate to multilayer wiring substrates with built-in semiconductor components. *See e.g.*, APPLE-1004, Abstract, [0001], [0005], [0017], [0020], [0023]-[0025], [0066]; APPLE-1012, [0023], FIGS. 1, 4; APPLE-1016, Abstract, [0004]-[0006]. Imoto also provides express disclosure on stacking up “[a]ny number equal to or greater than two” of layers of similar configuration, to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1016, [0002] (“Semiconductor devices are increasingly stacked to realize high-density mounting.”), [0010] (“This embodiment has four stacked semiconductor elements, but the number of semiconductor elements to be stacked is not limited to the four in the present invention. Any number equal to or greater than two can be stacked.”), cls.1, 2, 4, 8, FIGS. 5-9 (and related descriptions).

294. As I previously discussed for the Sakamoto-Eiji combination (§ XII.A.), a POSITA would have been motivated to utilize an EMI shield feature, in accordance with Eiji’s teachings, in a recessed portion or through hole in the core substrate described by Sakamoto, to provide a shielding effect. A POSITA would

have been further motivated to stack up two, three, or more layers of Sakamoto-Eiji's wiring board to form a multi-layered configuration, in accordance with Imoto, to achieve high density mounting with EMI shielding. Below composite figure illustrates a three-layered configuration with each substructure layer having an IC chip component embedded in a recessed portion of its own substrate, each recessed portion having metal foil on its sidewalls to provide EMI shielding.



Composite Based on APPLE-1004, FIG. 12 (Annotated)

295. Based on my knowledge and experience in the field and my review of the references, a POSITA would have had a reasonable expectation of success in combining Sakamoto-Eiji with Imoto. This is because Sakamoto, Eiji and Imoto describe similar electronic devices composed of multilayer wiring substrates with embedded semiconductor components. This is also because the modifications

involve only implementation of well-known technologies. And Sakamoto already teaches various mechanisms for connecting multiple substrates on top of each other, e.g., using “BGA, Solder bumps, and PGA (conductive connection pins).” APPLE-1004, [0011], [0069], [0070], FIGS. 9-12. I note here again that Sakamoto, Eiji, and Imoto relate to the same field of endeavor and are directed to analogous subject matter, including disclosure pertinent to the construction of multi-layered circuit board configurations.

B. Analysis of Sakamoto, Eiji and Imoto with Respect to Claims 12-27

[12]-[27]

296. The Sakamoto-Eiji-Imoto combination renders obvious these claims for at least the same reasons that I previously discussed under the Sakamoto and Sakamoto-Eiji grounds (§XI.A., §XII.B.). In addition, with respect to the recited multi-layered feature, Imoto provides express teaching of a multi-layered structure. *Supra*, §VII.E. (Imoto Overview). As I discussed in the Sakamoto-Eiji-Imoto combination (§XIII.A.) the Sakamoto-Eiji-Imoto combination has a stack-up multi-layered structure, in accordance with Imoto, that includes two, three, or more substructures. The composite figure above illustrates this configuration, having three similar circuit board substructures stacked on top of each other. As a result of this multi-layered configuration, the structures of the Sakamoto-Eiji-Imoto device provide each element of claim [12] through [27] in the same manner as

described above. Imoto further informs and motivates the multi-layered structure and electrical connections between each substructure.

XIV. CONCLUSION

The findings and opinions set forth in this declaration are based on my work and examinations to date.

I may continue my examinations. I may also receive additional documentation and other factual evidence over the course of this IPR that will allow me to supplement and/or refine my opinions. I reserve the right to add to, alter, or delete my opinions and my declaration upon discovery of any additional information. I reserve the right to make such changes as may be deemed necessary.

In signing this declaration, I recognize that the declaration will be filed as evidence in an IPR before the PTAB. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

APPENDIX A

Dean P. Neikirk

Emeritus Professor, Emeritus Cullen Trust for Higher Education Professorship in Engineering
Department of Electrical and Computer Engineering
Cockrell School of Engineering
The University of Texas at Austin
Austin, TX 78712

Education:

Oklahoma State University (Physics and Mathematics; with Honors)	B.S.	1979
California Institute of Technology (Applied Physics)	M.S.	1981
California Institute of Technology (Applied Physics)	Ph.D.	1984

Professional Experience:

Assistant Professor, University of Texas at Austin, Jan. 1984 - Aug. 1988
Associate Professor, University of Texas at Austin, Sept. 1988- Aug. 1992
Full Professor, University of Texas at Austin, Sept. 1992-Jan. 2021
Associate Dean of Graduate Studies, Aug. 2014 – Jan. 2021
Emeritus Professor, Feb. 2021 - present

Honors and Awards:

- 1984 Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the areas of detectors and imaging arrays."
- Listed in the Second Edition of Who's Who in Frontiers of Science and Technology, 5th Edition of Who's Who in Technology Today, 1994 American Men & Women of Science; 1985 Outstanding Young Man of America, 1989 Outstanding Young Man of America; 7th Edition of Who's Who in Technology.
- 1984-85 Engineering Foundation Faculty Award, University of Texas at Austin Engineering Foundation Advisory Council.
- 1985-90 General Motors Foundation Centennial Teaching Fellowship, University of Texas at Austin.
- 1985-86 IBM Corporation Faculty Development Award
- 1986 National Science Foundation Presidential Young Investigator.

- 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, University of Texas at Austin.
- 1990-1992 Temple Foundation Endowed Faculty Fellowship (No. 1), University of Texas at Austin.
- 1992-present Cullen Trust for Higher Education Professorship in Engineering (No. 7), University of Texas.
- 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, University of Texas at Austin.
- 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, University of Texas at Austin.
- 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching
 - each year since 1956, Lockheed Martin and its predecessor, has sponsored an award for excellence in engineering teaching to reward one College of Engineering faculty member for exceptional teaching. This prestigious award is given to a faculty member dedicating time and energy in abundance to teaching undergraduate and graduate students. As a result, his or her work leaves a mark of excellence on the entire College of Engineering. Nominations for this award are made by The University of Texas at Austin engineering students and faculty. Final selection is made by a committee composed the five most recent faculty recipients of the award and the student presidents of the Student Engineering Council (SEC) and the Graduate Engineering Council (GEC).
- 2015 Civitatis Award: The University of Texas at Austin Civitatis Award was established in 1997 to recognize outstanding faculty citizenship. The Civitatis Award is conferred upon a member of the faculty in recognition of dedicated and meritorious service to the University above and beyond the regular expectations of teaching, research, and writing. The award is made by the President upon the recommendation of the Faculty Council Executive Committee. Prof. Neikirk was nominated for the award for his “extensive, effective and distinguished service record to his department, college and [the] University of Texas.”

Vita for Dean P. Neikirk:

Dean P. Neikirk was born in Oklahoma City, Oklahoma, on October 31, 1957. He received the B.S. degree (1979) in physics from Oklahoma State University, and the M.S. (1981) and Ph.D. (1984) degrees in applied physics from the California Institute of Technology. He joined the faculty of The University of Texas at Austin in 1984, and is currently a Professor in the Department of Electrical and Computer Engineering, holding the Cullen Trust for Higher Education Professorship in Engineering (No. 7). Dr. Neikirk developed the first monolithic, high resolution focal plane detector array for use at wavelengths between 0.1 mm and 1 mm, and in 1984 received the Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter

wave integrated circuits especially in the area of detectors and imaging arrays." He has also been named a 1986 National Science Foundation Presidential Young Investigator.

Dr. Neikirk's research interests concentrate on the fabrication and modeling of electromagnetic and micromachined sensors and actuators. His work also included projects involving integrated circuit processing and the high frequency properties of transmission lines. His work concentrated on the use of advanced fabrication techniques, including silicon micromachining, for new device and sensor development. Dr. Neikirk developed the teaching laboratory for semiconductor device fabrication at The University of Texas at Austin, and was an active member of The University of Texas at Austin Microelectronics Research Center. Recently Dr. Neikirk's research project related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between the University of Texas and LabNow, Inc. Dr. Neikirk has also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, the Secretary of the General Faculty at UT-Austin, and as an Associate Dean of the University of Texas at Austin Graduate School.

Professional Societies:

Senior Member, Institute of Electrical and Electronics Engineers

- Associate Editor for Solid State and VLSI Electronics, **IEEE Transactions on Education** (March 1991- Oct. 1994)

Commercialization of Technology:

Two companies have been founded based on technology developed by Dr. Neikirk's research group. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups.

From a University of Texas news release:

Firm commercializing University of Texas technology rounds up \$14 million venture capital investment (October 1, 2004)

AUSTIN, Texas—LabNow Inc. has received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors.

The money will be used to develop the company's technology and to launch its initial product, CD4Now™, a point-of-care diagnostic tool for HIV/AIDS patients.

The device, which is based on technology developed at The University of Texas at Austin, quickly and accurately analyzes complex fluids such as blood.

Patents

1. US Patent 5,080,870: "Sublimating and Cracking Apparatus," Jan. 14, 1992; Inventors: B. G. Streetman, T. J. Mattord, D. P. Neikirk
2. US Patent 5,408,107: "Semiconductor Device Having Multiple Current-Voltage Curves and Zero-Bias Memory," April 18, 1995;
Inventors: Dean P. Neikirk and Kiran Kumar Gullapalli
3. US Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," July 8, 2003;
Inventors: McDevitt; John T.; Anslyn; Eric V.; Shear; Jason B.; Neikirk; Dean P.
Assignee: Board of Regents, The University of Texas System (Austin, TX)
4. US Patent 6,602,702: "Detection system based on an analyte reactive particle," August 5, 2003
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)

Assignee: The University of Texas System (Austin, TX)

5. US Patent 6,649,403: "Method of preparing a sensor array," November 18, 2003
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
6. US Patent 6,680,206, "Sensor arrays for the measurement and identification of multiple analytes in solutions," January 20, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
7. US Patent 6,713,298, "Method and apparatus for the delivery of samples to a chemical sensor array," March 30, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Travis, TX); Shear; Jason B. (Travis, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
8. US Patent 6,908,770, "Fluid based analysis of multiple analytes by a sensor array," June 21, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
9. US Patent 7,022,517, "Method and apparatus for the delivery of samples to a chemical sensor array," April 4, 2006, filed: July 14, 2000
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX); Borich; Damon V. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
10. US Patent 7,316,899, "Portable sensor array system," January 8, 2008, filed: January 31, 2001
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
11. US Patent 7,491,552, "Fluid based analysis of multiple analytes by a sensor array," February 17, 2009, filed: January 20, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
12. United States Patent 7,651,868, "Method and system for the analysis of saliva using a sensor array," January 26, 2010, Filed: December 13, 2004

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: The Board of Regents of The University of Texas System (Austin, TX)

13. United States Patent 8,101,431, "Integration of fluids and reagents into self-contained cartridges containing sensor elements and reagent delivery systems," January 24, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

14. United States Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements," January 31, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

15. United States Patent 8,257,967, "Method and system for the detection of cardiac risk factors," September 4, 2012, Filed: April 28, 2003

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

16. United States Patent 9,291,586, "Passive wireless self-resonant sensor," March 22, 2016, Filing Date: May 5, 2013

Inventors: Neikirk, Dean P. (Austin, TX, US), Pasupathy, Praveenkumar (Austin, TX, US), Zhang, Sheng (Austin, TX, US), Leonhardt, Brad (Austin, TX, US), Ekerdt, John G. (Austin, TX, US), Korgel, Brian A. (Austin, TX, US), Holmberg, Vincent C. (Seattle, WA, US), Shipman, Catherine D. (Reston, TX, US), Bogart, Timothy D. (Oxford, GB), Chockla, Aaron (Chicago, IL, US)

Assignee: Board of Regents, The University of Texas System (Austin, TX, US)

17. United States Patent 9,581,559, "Corrosion detection sensor embedded within a concrete structure with a diffusion layer placed over the sacrificial transducer," February 28, 2017, Filing Date: August 14, 2014

Inventors: Neikirk; Dean P. (Austin, TX), Wood; Sharon L. (Austin, TX), Pasupathy; Praveenkumar (Austin, TX), Yosef; Ali Abu (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

Publications:

A: Refereed archival journal publications

1. D. P. Neikirk and R. C. Powell, "Laser Time-Resolved Spectroscopy of Host-Sensitized Energy Transfer in $\text{Bi}_4\text{Ge}_3\text{O}_{12}:\text{Er}^{3+}$ Crystals," **J. Lumin.**, vol. 20, 1979, pp. 261-270.
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24. McCleskey, Shawn C.; Goodey, Adrian P.; Rodriguez, Marc D.; McDevitt, John T.; Anslyn, Eric V.; Neikirk, Dean P., "Development of a multi-component sensor array for the simultaneous detection of various analytes in solution," Abstracts of Papers, 222nd ACS National Meeting, Chicago, IL, United States, August 26-30, 2001.

D. Other Major Publications

V. Kesan and D. P. Neikirk, "Quantum Well Devices," **Microwaves and RF**, vol. 25, July 1986, pp. 93-97.

D. P. Neikirk, P. Cheung, M.S. Islam, and T. Itoh, "Optically Controlled Coplanar Waveguide Phase Shifters," **Microwave Journal**, Dec. 1989, pp. 77-88.

D. P. Neikirk, "Quantum Wells and Other Deep Subjects," **Discovery**, Vol. 11, No. 3, 1989, pp. 5-8.

S. M. Wentworth, J. M. Lewis, and D. P. Neikirk, "Antenna-Coupled Thermal Detectors of mm-Wave Radiation," **Microwave Journal**, Jan. 1993, pp. 94-103.

E. Book Chapter

D. B. Rutledge, D. P. Neikirk, and D. Kasilingam "Integrated- Circuit Antennas," in **Infrared and Millimeter Waves**, vol. 11, editor K.J. Button, 1984.

Nicolaos Christodoulides, Priya Dharshan, Jorge Wong, Pierre N. Floriano, Dean Neikirk and John T. McDevitt, "A Microchip-Based Assay for Interleukin-6," In: *Methods in Molecular Biology*, Volume 385: Microchip-Based Assay Systems, Humana Press, ISBN 978-1-58829-588-0 (Print) 978-1-59745-426-1 (Online), Copyright 2008, pages 131-144.

F. Technical Reports

C-K Tzuang, D. P. Neikirk, and T. Itoh, "Finite Element Analysis of Slow-Wave Schottky Contact Printed Lines," Microwave Laboratory Report No. 87-P-2, AFOSR Grant 86-0036, Feb., 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 87-P-3, AFOSR Grant 86-0036, Jan., 1987.

V. P. Kesan and D. P. Neikirk, "Quantum Well Devices," Electrical Engineering Research Laboratory Report No. 87-P-8, Joint Services Electronics Program Research Contract AFOSR F49620-86-C-0045, August 7, 1987.

Stuart M. Wentworth and D. P. Neikirk, "High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," Microwave Laboratory Report No. 87-P-7, August 26, 1987.

Stuart M. Wentworth and D. P. Neikirk, "Characterization of Tape Automated Bonding (TAB) Interconnects at High Frequency," Microwave Laboratory Report No. 87-P-9, October 23, 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 90-P-1, Final Technical Report for AFOSR Grant 86-0036, Feb., 1990.

A. Mortazawi, D. Neikirk, and T. Itoh, "Microwave and millimeter wave oscillators and planar power combining structures for QWITT and Gunn diodes," Microwave Laboratory Report No. 90-P-4, Technical Report for ARO Grant DAAL03-88-K-0005 and JSEP Grant F49620-89-0044, Aug., 1990.

Oral Presentations

A. Professional Society Presentation

D. B. Rutledge and D. P. Neikirk, "Imaging Antenna Arrays," Invited Keynote Speakers, Sixth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 7-12, 1981.

D. P. Neikirk and D. B. Rutledge, "Advances in Microbolometers," Invited Keynote Speakers, Eighth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 12-17, 1983.

D. P. Neikirk, "Optically Controlled Coplanar Waveguide Millimeter Wave Phase Shifter," Tenth International Conference on Infrared and Millimeter Waves, Lake Buena Vista, Fl., Dec. 9-13, 1985.

D. P. Neikirk, "Picosecond Response of an Optically Controlled Millimeterwave Phase Shifter," Second Topical Meeting on Picosecond Electronics and Optoelectronics, Jan., 1987.

D. P. Neikirk, "Influence of Transit Time Effects on the Optimum Design and Maximum Oscillation Frequency of Quantum Well Oscillators," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "Measurements of an Optically Controlled Coplanar Waveguide Phase-Shifter," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "High Frequency Characterization of Tape-Automated Bonding Interconnects," 5th Annual Texas Regional Symposium, International Society of Hybrid Manufacturing, April 11, 1988.

D. P. Neikirk, "Time Dependent Simulation of the Quantum Well Injection Transit Time Diode," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

D. P. Neikirk, "Experimental Performance of a Periodically Illuminated Optically Controlled Coplanar Waveguide Phase Shifter," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

B. Invited Lectures

1. D. P. Neikirk, "Exotic Heterojunction Devices for Microwave Circuits," NSF Workshop on Future Research Opportunities in Electromagnetics, Arlington, TX., January 29-31, 1986.

2. D. P. Neikirk, "Optical Control of a Monolithic Millimeter Phase Shifter," ARO Workshop on Fundamental Issues in Millimeter and Submillimeter Waves, Los Angeles, Ca., Sept. 15-16, 1986.

3. Dean P. Neikirk, "Quantum Well Oscillators for Millimeter Wave Applications," 1987 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Hilton Head Island, S.C., March 2-4, 1987.

4. S.M. Wentworth and D. P. Neikirk, "High Frequency Tape-Automated Bonding (TAB) Interconnect Characterization," IEEE 6th Annual VLSI and GaAs Packaging Workshop, Sept. 14-16, 1987.

5. D. P. Neikirk, "The quantum well injection transit time diode," Engineering Foundation Conference on Advanced Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec. 5-10, 1988.
6. D. P. Neikirk, ""The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," presented to the Microelectronics and Computer Technology Corporation, April 19, 1989.
7. Dean P. Neikirk, "Impedance measurements of quantum well diodes for millimeter wave applications," 1990 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), San Francisco, CA., Feb. 12-14, 1990.
8. Dean P. Neikirk, "Twin-slot multi-layer substrate-supported antennas and detectors for terahertz imaging," First International Symposium on Space Terahertz Technology, University of Michigan, Ann Arbor, Mich., March 5-6, 1990.
9. Dean P. Neikirk, "Microwave and Millimeterwave Oscillators using Quantum Well Diodes," Joint IEEE MTT/ED Dallas Chapter meeting, Sept. 27, 1990.
10. Dean P. Neikirk, "Quantum Transport Simulations of Resonant Tunneling Diodes," 1991 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Ft. Lauderdale, FL., Feb. 18-20, 1991.
11. Dean P. Neikirk, "The Application of Physics in Electrical Engineering (or is it Engineering in Physics?): Electromagnetics in Very High Frequency Semiconductor Devices," Physics Colloquium, Oklahoma State University, March 5, 1992.
12. D. P. Neikirk and B. G. Streetman, "MBE growth of multilayer heterostructures for photonic and high-speed electronic devices," Engineering Foundation Conference on High Speed Optoelectronic Devices and Circuits II, Banff, Alberta, Canada, Aug. 9-13, 1992.
13. L. T. Pillage, D. P. Neikirk, and R. Mercer, "Design automation techniques and algorithms for application specific electronic modules (ASEMs)," ARPA Electronic Packaging & Interconnect Principle Investigator Meeting, Marina del Ray, CA, Feb. 14-18, 1994.
14. D. P. Neikirk, "Micro-sensors - What happens when you make classical devices small?: Integrated Bolometric Radiation Detectors," Texas Instruments, Dallas, Texas, Oct. 20, 1994.
15. Dean P. Neikirk, "Micromachined sensors," Motorola Sensors Steering Committee, Albuquerque, New Mexico, March 28, 1995.
16. D. P. Neikirk, E. Tuncer, and B.-T. Lee, "The Use of Effective Internal Impedance Approximations in Lossy Transmission Line Modeling," *Progress in Electromagnetics*

Research Symposium PIERS 95, The University of Washington, Seattle, Washington, July 28, 1995.

17. D. P. Neikirk, M. S. Islam, and E. Tuncer, "Accurate Quasi-Static Modeling of Transmission Lines on Semiconducting Substrates," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.

18. D. P. Neikirk, "Impact of Finite Metal Conductivity on Inductance Extraction of Interconnects and Packages," Sematech meeting on Electrical Modeling Challenges Faced by Packaging Designers, Austin, Texas, Nov. 19, 1995.

19. D. P. Neikirk, "Micromachined Fabry-Perot Pressure Transducers," Hughes Research Laboratory, Malibu, California, Nov. 21, 1995.

20. D. P. Neikirk, "Classical Devices Made Small; or 'What's the big deal about little machines?'" , Manufacturing 2000, University of Texas at Austin, Feb. 23, 1996.

21. D. P. Neikirk, "Interconnect Inductance Modeling from DC to the Skin Effect Limit," Quad Designs, Camarillo, CA, July 10, 1996.

22. D. P. Neikirk, "Efficient Conductor Boundary Conditions in the dc to Skin Effect Limit," DARPA MAFET Program Review, Fairfax, VA, Oct. 27-31, 1997.

23. Micromachined Array-based Multi-analyte Chemical Sensors: Towards the Fabrication of an "Electronic Tongue" South, Texas Local Section of The Electrochemical Society Meeting, April 17, 1999.

24. D. P. Neikirk, "Resonant Chemical Surveillance Tags," IEEE Electron Device Chapter, Central Texas Section, September 25, 2008.

25. D.P. Neikirk, "Near Borehole Condition Sensing," Nanotechnology Conference and Trade Show - Nanotech 2009, Houston, TX May 3-7, 2009, Nanotech & Cleantech for Oil & Gas Session, (Session chair: Sean Murphy, Advanced Energy Consortium), May 5, 2009.

26. D.P. Neikirk, "Integrated Threshold Nanosensor Systems," Advanced Oil Consortium Microfabricated Sensors Workshop, Houston Research Center, Bureau of Economic Geology, University of Texas at Austin, September 8th-9th, 2010.

27. D. P. Neikirk, "Sensing systems for "harsh" environments," Engineering Challenges for Deepwater Drilling at the "U.S. Offshore Oil Exploration: Managing Risks to Move Forward," James A. Baker III Institute for Public Policy and PFC Energy, Rice University, Houston, TX, February 11, 2011.

C. Other Conference Presentations

Praveen Pasupathy, Mingxiang Zhuzhou, Shasi K. Munukutla, Dean P. Neikirk, and Sharon L. Wood, “Resonant Wireless Sensor Nets for Civil Infrastructure Health Monitoring,” 2009 National Science Foundation Division of Civil, Mechanical and Manufacturing Innovation (CMMI) Engineering Research and Innovation Conference, Honolulu, Hawaii, June 22-25, 2009.

Technical Consulting

Teltech Resource Network (1985-1993)
Ardex, Inc. (1986-88)
University and Polytechnic Grants Committee, Consultancy to examine Equipment Requirements for the Hong Kong University of Science and Technology, July, 1989
E. P. Hamilton Associates, (1987-90)
Burnett Company, Microwave Heating for Secondary Oil Recovery, July, 1990
Microelectronics and Computer Technology Corporation, June, 1990
Microelectronics and Computer Technology Corporation, Oct., 1994 - Sept., 1996
Baker-Hughes

University Committee Assignments

Departmental:

Graduate Student Financial Aid, Sept. 1984- Sept. 1987
Faculty Recruiting, Sept. 1984- Aug. 1985
Microelectronics Jr. Faculty Recruiting, Sept. 1985- Sept. 1987 (chairman)
ECE Safety Committee, Sept. 1985- Aug. 1993 (chairman, 1985-89)
ECE Electronics Shop Coordinating Committee, March 1986- Aug. 1993
Solid State Electronics Area Graduate Advisor, Aug. 1986- Aug. 89
ECE Space Allocation Committee, Sept. 1989-Aug. 1993 (chairman)
ECE Facilities Committee, Sept. 1993- Aug. 1996 (chairman)
ECE Areas Committee, Electromagnetics/Acoustics, Sept. 1993-present
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1995- Aug. 1995
ECE World Wide Web Home Page Committee, Sept. 1995-Aug. 1996
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1997- Aug. 1997
ECE Areas Committee, Materials and Quantum Electronics, Sept. 1993-present; chairman, Sept. 1996-present
Chair of ECE Graduate Studies Committee, May 1998-August 2006
ECE Chair's council, November 1999-2010
ECE Graduate Advisor, Sept. 1999- 2010
ECE Associate Chair, Sept. 2001-Dec. 2010
ECE peer Faculty Annual Review Committee, Sept. 2012-Aug. 2013

College:

Engineering Scholastic Appeals, Sept. 1984- Aug. 1985
Engineering Safety Committee, Sept. 1985- Aug. 1994 (chairman, Sept. 1989-Aug. 1994)

Aerospace Engineering Machine Shop, Sept. 1989-Aug. 1993
College Annual Report Quality Team, Jan. 1994- Aug. 1994
College Multimedia Committee, Sept. 1995-Aug. 2000
Equal Opportunity in Engineering (EOE) Program, 1995-Dec. 1996
Graduate Fellowship Review Committee, Sept. 2011-Aug. 2013

University:

Presidential Ad Hoc Committee on Research Infrastructure Enhancement, Jan. 1988 - Aug. 1994
Research Safety Advisory Committee, Oct. 1991-present (chairman, Sept. 1996-1999)
Ad Hoc Consultative Committee for the Selection of a Dean of the College of Engineering, Nov. 1995-May 1996
Faculty Building Advisory Committee, Sept. 1995-Aug. 2000; Aug. 2003-Aug. 2004
Ad Hoc Project Committee for Parking Garage # 4A, Sept. 1996-Aug. 2000
Faculty Council, Sept. 1996-Aug. 2000; Sept. 2002 - Aug. 2004
Faculty Advisory Committee on the Budget, Sept. 99 - Aug. 2000; Sept. 2008 – Aug. 2011 (vice chair Sept. 2009- Aug. 2010)
Graduate Assembly, April 1997- Aug. 2000; Sept. 2001 - Aug. 2008
Administrative sub-committee of GA, Sept. 1997-Aug. 1998; Sept. 2006-Aug. 2007
Academic sub-committee of GA, Sept. 1998-Aug. 2000; Sept. 2001-Aug. 2006; Sept. 2007-Aug. 2008
Chair, Graduate Assembly, 2004-2005
Academy of Distinguished Teachers selection committee, academic year 1999-2000
Outstanding Graduate Adviser selection committee, academic year 1999-2000
Outstanding Graduate Coordinator selection committee, academic year 1999-2000
Faculty Council, Sept. 2008 – Aug. 2012; Chair-elect Sept. 2009- Aug. 2010; Chair Sept. 2010- Aug. 2011; past chair: Sept. 2011-Aug. 2012
Faculty Council Executive Committee, Sept. 2009 – Aug. 2012
General Faculty Rules and Governance Committee, Sept. 2010 – Aug. 2015 (Chair, Sept. 2011 – Aug. 2013)
Ad Hoc Consultative Committee for the Selection of a Dean of the Graduate School, Nov. 2012 – Sept. 2012
Secretary of the General Faculty and Faculty Council, Sept. 2013 – Aug. 2015
Committee on Undergraduate Degree Program review, Sept. 2013 – Aug. 2015
Faculty Council Executive Committee, Sept. 2013 – Aug. 2015
Faculty Committee on Committees, *ex officio* member, Sept. 2013 – Aug. 2015

UT System:

Task Force on Doctoral Programs and Post-Doctoral Experience, Spring-Fall 2006

University of Texas System Faculty Advisory Council, Sept. 2009- Aug. 2011

State of Texas:

Texas Higher Education Coordinating Board Graduate Education Advisory Committee (GEAC), September 1, 2015 - August 31, 2018.

Evidence of Teaching Effectiveness

Senior Design Projects:

Umer Yousafzai and Venuka Jayatilaka, Spring 1994

Chris Eiting and Sonny Gonzalez, Spring 1994

David Lee and David Onsongo, Fall 1996

Dave Pyle and Aruna Murthy, Spring 1999

Hitesh Mehta and Edward Zhu, Spring 1999, "Giving the electronic tongue a sense of good taste: image analysis tools and GUI"

Gus Espinosa and Donnie Garcia, Spring 1999, "Design and Implementation of a Computer Interfacing Circuit to Control LED's for use with a Chemical Sensor"

Natthanant Pon Skulkaew and Prem Nainani, Spring 2001, "PC-based data acquisition and wireless transmission system"

Matthew Andringa and Allen Hall, Spring 2001, "Non-Invasive RFID Weld Inspection"

Michael Amalfitano and Sapun Parekh, Spring 2002, "Output circuitry for a transmitter used in an Electronic Structural Surveillance system"

Kunal Patel and Jacy Little, Spring 2002, "Swept, high frequency oscillator to work in an Electronic Structural Surveillance (ESS) system"

Dong Pak, Spring 2002, "Automated image-processing software of an electronic chemical sensor"

Rajesh Nerlikar, Jonathan Solomon, Spring 2003, "Wireless Data Acquisition System for Bluetooth-enabled RFID Readers"

Nola Li, Judith Chen, Maria Huang, Fall 2003, "Design and build a tuning network for a swept frequency reader used in structural health analysis"

Tuenlap (Daniel) Chan, Imranul Islam, Derek Choi, Spring 2004, "Design and build an RFID Interrogator Receiver"

John McKee and Terence Man, Spring 2007, "Improved Corrosion Sensors"

Abdulaziz Beayeyz, Sravan Bhagavatula, Rahul Mitra, Shasi Munukutla, Spyder Spann, Fall 2009, "Portable Corrosion Detector"

Jonathan Pham, Po-Han Wu, Josh Schulte, Pritesh Solanki, Mesele Bedasa, Spring 2011- Fall 2011, "Multi-Sensor Robotics Platform"

Raymund Lee, Simon Chow, Connor Landy, Kevin Woo, and Anirudh Kashyap, Fall 2012-Spring 2013, "Variable Frequency RFID Tag and Reader"

Javier Chacon, Joshua Poncik, Joshua Orozco, Sebastian Salomon, Yongcong Zou, Fall 2013-Spring 2014, "Environmental Sensor Monitoring Network"

Organized Classes Taught:

EE 363M Introduction to Microwaves, Spring 1984, # 16455
EE 396K VLSI Fabrication Techniques, Fall 1984, # 16255
EE 379K Integrated Circuit Fabrication, Spring 1985, # 16055
EE 396K VLSI Fabrication Techniques, Fall 1985, # 16275
EE 379K Integrated Circuit Fabrication, Fall 1985, # 16070
EE 396K VLSI Fabrication Techniques, Spring 1986, # 17680
EE 379K Integrated Circuit Fabrication, Spring 1986, # 17450
EE 396K VLSI Fabrication Techniques, Fall 1986, # 15245
EE 379K Integrated Circuit Fabrication, Fall 1986, # 15020
EE 396K VLSI Fabrication Techniques, Spring 1987, # 15205
EE 379K Integrated Circuit Fabrication, Spring 1987, # 14970
EE 396K VLSI Fabrication Techniques, Fall 1987, # 15010
EE 440 Integrated Circuit Fabrication, Fall 1987, # 14545
EE 363M Introduction to Microwaves, Spring 1988, # 14535
EE 396K VLSI Fabrication Techniques, Spring 1988, # 14865
EE 440 Integrated Circuit Fabrication, Spring 1988, # 14390
EE 396K VLSI Fabrication Techniques, Fall 1988, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1988, # 14705
EE 363M Introduction to Microwaves, Spring 1989, # 14525
EE 396K VLSI Fabrication Techniques, Spring 1989, # 14855
EE 396K VLSI Fabrication Techniques, Fall 1989, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1989, # 14705
EE 363M Introduction to Microwaves, Spring 1990, # 14050
EE 396K VLSI Fabrication Techniques, Spring 1990, # 14355, 14360
EE 440 Integrated Circuit Fabrication, Spring 1990, # 13915, 13920
EE 396K VLSI Fabrication Techniques, Fall 1990, # 14630, 14635
EE 440 Integrated Circuit Fabrication, Fall 1990, # 14200, 14205
EE 363M Introduction to Microwaves, Spring 1991, # 14365
EE 396K VLSI Fabrication Techniques, Spring 1991, # 14660, 14665, 14670
EE 440 Integrated Circuit Fabrication, Spring 1991, # 14220, 14225, 14230
EE 396K VLSI Fabrication Techniques, Fall 1991, # 14865, 14860
EE 440 Integrated Circuit Fabrication, Fall 1991, # 14425, 14430
EE 363M Introduction to Microwaves, Spring 1992, # 14270
EE 396K VLSI Fabrication Techniques, Spring 1992, # 14545, 14550, 14555
EE 440 Integrated Circuit Fabrication, Spring 1992, # 14130, 14135
EE 396K VLSI Fabrication Techniques, Fall 1992, # 15095, 15100, 15105
EE 440 Integrated Circuit Fabrication, Fall 1992, # 14670, 14675
EE 397K Microwave Devices, Spring 1993, # 14805
EE 396K VLSI Fabrication Techniques, Fall 1993, # 14800, 14805, 14810
EE 440 Integrated Circuit Fabrication, Fall 1993, # 14385, 14390
EE 363M Introduction to Microwaves, Spring 1994, # 14370
EE 396K VLSI Fabrication Techniques, Fall 1994, # 14365

EE 440 Integrated Circuit Fabrication, Fall 1994, # 13870
 EE 397K Electromagnetics in Packaging, Spring 1995, # 14555
 EE 396K VLSI Fabrication Techniques, Fall 1995, # 14765
 EE 440 Integrated Circuit Fabrication, Fall 1995, # 14260
 EE 397K Electromagnetics in Packaging, Spring 1996, # 14695
 EE 382M Simulation Methods in CAD/VLSI, Spring 1996, # 14500
 EE 396K VLSI Fabrication Techniques, Fall 1996, # 14535
 EE 440 Integrated Circuit Fabrication, Fall 1996, # 14090
 EE 382M Simulation Methods in CAD/VLSI, Spring 1997, # 14325
 EE 363M Introduction to Microwaves, Spring 1997, # 14120
 EE 396K VLSI Fabrication Techniques, Fall 1997, # 15315
 EE 440 Integrated Circuit Fabrication, Fall 1997, # 14820
 EE 363M Introduction to Microwaves, Spring 1998, # 14530
 EE 397K Microwave Devices, Spring 1998, # 14950
 EE 396K VLSI Fabrication Techniques, Fall 1998, # 15475
 EE 440 Integrated Circuit Fabrication, Fall 1998, # 14965
 EE 363M Introduction to Microwaves, Spring 1999, # 14825
 EE 397K Microwave Devices, Spring 1999, # 15260
 EE 396K VLSI Fabrication Techniques, Fall 1999, # 15340
 EE 440 Integrated Circuit Fabrication, Fall 1999, # 14820
 EE 363M Introduction to Microwaves, Spring 2000, # 14755
 EE 396K VLSI Fabrication Techniques, Fall 2000, # 15600
 EE 440 Integrated Circuit Fabrication, Fall 2000, # 15100
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2001, #15170
 EE 396K VLSI Fabrication Techniques, Fall 2001, # 15725
 EE 440 Integrated Circuit Fabrication, Fall 2001, # 15230
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2002, #15330
 EE 396K VLSI Fabrication Techniques, Fall 2002, # 16050
 EE 440 Integrated Circuit Fabrication, Fall 2002, # 15485
 EE 397K Microwave Devices, Spring 2003, # 15110
 EE 396K VLSI Fabrication Techniques, Fall 2003, # 15580
 EE 440 Integrated Circuit Fabrication, Fall 2003, # 15095
 EE 325 Electromagnetic Engineering, Spring 2004, # 14345
 EE 396K VLSI Fabrication Techniques, Fall 2004, # 16250
 EE 440 Integrated Circuit Fabrication, Fall 2004, # 15715
 EE 396K 26-Microelectromechanical Systems, Spring 2005, # 15690
 EE 396K VLSI Fabrication Techniques, Fall 2005, # 16455
 EE 440 Integrated Circuit Fabrication, Fall 2005, # 15930
 EE 396K VLSI Fabrication Techniques, Fall 2006, # 17040
 EE 440 Integrated Circuit Fabrication, Fall 2006, # 16430
 EE 325 Electromagnetic Engineering, Spring 2007, # 15765
 EE 396K VLSI Fabrication Techniques, Fall 2007, # 17425
 EE 440 Integrated Circuit Fabrication, Fall 2007, # 16770
 EE 396K-26 Microelectromechanical Systems, Spring 2008, # 16815
 EE 396K VLSI Fabrication Techniques, Fall 2008, # 17380
 EE 325 Electromagnetic Engineering, Spring 2009, # 16000

EE 396K-24 Microwave Devices, Spring 2010, # 16975
 EE 396K VLSI Fabrication Techniques, Fall 2010, # 17075, 17080, 17085, 17090
 EE 440 Integrated Circuit Fabrication, Fall 2010, # 16540, 16545, 16550, 16555
 EE 396K VLSI Fabrication Techniques, Fall 2011, # 17295, 17300, 17305, 17310
 EE 440 Integrated Circuit Fabrication, Fall 2011# 16760, 16765, 16770, 16775
 EE 396K 26-Microelectromechanical Systems, Spring 2012, #17070
 EE 396K VLSI Fabrication Techniques, Fall 2012, # 17185, 17190, 17195, 17200
 EE 440 Integrated Circuit Fabrication, Fall 2012, # 16640, 16645, 16650, 16665
 EE 363M Introduction to Microwaves, Spring 2013, # 16605
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2013, # 17425, 17430, 17435, 17440
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2013, # 16790, 16795, 16800, 16805
 EE 396K-24 Microwave Devices. Spring 2014, #17440
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2014, #17525, 17530, 17535, 17540
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2014, #16960, 16965, 16970, 16975
 EE 363M Microwave and Radio Frequency Engineering, Spring 2015, #16355
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2015, #16965, 16970, 16975
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2015, #16480, 16485, 16490
 EE 363M Microwave and Radio Frequency Engineering, Spring 2016, #16550
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2016
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2016
 EE 396K 26-Microelectromechanical Systems, Spring 2017
 EE 363M Microwave and Radio Frequency Engineering, Spring 2018, #15890
 EE 363M Microwave and Radio Frequency Engineering, Spring 2019, #16625
 EE 363M Microwave and Radio Frequency Engineering, Spring 2020, #16695

Continuing Education Courses Taught

"Microelectronics Fabrication - Chemical Aspects," with Isaac Trachtenberg,
 Continuing Engineering Studies, College of Engineering, The University of
 Texas at Austin, June 1-4, 1987.
 "Integrated Circuit Process & Design," with M. R. Mercer, Motorola short course,
 Continuing Engineering Studies, College of Engineering, The University of

Texas at Austin:

- Aug.-Sept., 1987
- Nov.-Dec., 1987
- Nov.-Dec., 1988
- March-April, 1989
- Aug.-Sept., 1989
- Nov.-Dec., 1989
- Feb.-March, 1990
- April, 1990
- Aug., 1990

"Integrated Circuit Processing and Design," with L. T. Pillage, Advanced Micro Devices short course, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin:

- Oct.-Nov., 1990
- June-July, 1991

"Microelectronics Fabrication," for the Fellows of the Senior Service College Fellowship Program, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, yearly 1993-2003.