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Title: METHOD FOR EMBEDDING A COMPONENT IN A BASE

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,732,909 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 7,732,909
APPLE-1002	U.S. Patent No. 7,732,909 File History
APPLE-1003	Declaration of Dr. Dean Neikirk
APPLE-1004	Certified Translation of JP Application Publication 2001-339165A (“Sakamoto”)
APPLE-1005	U.S. Patent Application Publication No. 2002/0175402 (“McCormack”)
APPLE-1006	U.S. Patent No. 6,489,685 (“Asahi”)
APPLE-1007	U.S. Patent Application Publication No. 2001/0030059 (“Sugaya”)
APPLE-1008	U.S. Patent Application Publication No. 2002/0020898 (“Vu”)
APPLE-1009	RESERVED
APPLE-1010	RESERVED
APPLE-1011	Certified Translation of JP Patent No. 3207174 (“Hayashi”)
APPLE-1012	Certified Translation of JP Patent Application Publication No. 2002-016327 (“Eiji”)
APPLE-1013	U.S. Patent No. 6,335,571 (“Capote”)
APPLE-1014	U.S. Patent No. 6,297,551 (“Dudderar”)
APPLE-1015	U.S. Patent No. 6,404,052 (“Kurita”)
APPLE-1016	Certified Translation of JP Patent Application Publication No. 2001-068624A (“Imoto”)
APPLE-1017	Certified Translation of PCT Publication No. WO 00/09623 (“Watanabe”)

APPLE-1018	U.S. Patent No. 4,179,802 (“Joshi”)
APPLE-1019	U.S. Patent No. 5,608,262 (“Degani”)
APPLE-1020	U.S. Patent No. 5,321,210 (“Kimbara”)
APPLE-1021	U.S. Patent No. 5,146,674 (“Frankeny”)
APPLE-1022	JP Patent Application Publication No. 2001-339165A (“Sakamoto”)
APPLE-1023	JP Patent No. 3207174 (“Hayashi”)
APPLE-1024	JP Patent Application Publication No. 2002-016327 (“Eiji”)
APPLE-1025	JP Patent Application Publication No. 2001-068624A (“Imoto”)
APPLE-1026	PCT Publication No. WO 00/09623 (“Watanabe”)
APPLE-1027	Certified Translation of JP Patent Application Publication No. 2001-156457 (“Takayama”)
APPLE-1028	JP Patent Application Publication No. 2001-156457 (“Takayama”)
APPLE-1029	U.S. Patent No. 5,745,984 (“Cole”)
APPLE-1030	R. Aschenbrenner, A. Ostmann, U. Beutler, J. Simon and H. Reichl, “Electroless nickel/copper plating as a new bump metallization,” in IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 18, no. 2, pp. 334-338, May 1995, doi: 10.1109/96.386270
APPLE-1031	W. W. Flack, Ha-Ai Nguyen, E. Capsuto and C. McEwen, “Characterization of a thick copper pillar bump process,” 2007 12th International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces, San Jose, CA, USA, 2007, pp. 208-213.
APPLE-1032	Xiang Dai, M. V. Brillhart, M. Roesch and P. S. Ho, “Adhesion and toughening mechanisms at underfill interfaces for flip-chip-on-organic-substrate packaging,” in

IEEE Transactions on Components and Packaging
Technologies, vol. 23, no. 1, pp. 117-127, March 2000

APPLE-1033

D. Suryanarayana, T. Y. Wu and J. A. Varcoe,
“Encapsulants used in flip-chip packages,” in IEEE
Transactions on Components, Hybrids, and Manufacturing
Technology, vol. 16, no. 8, pp. 858-862, Dec. 1993

APPLE-1034

U.S. Patent Application Publication No. 2001/0033889
 (“Bhatt”)

LISTING OF CLAIMS

Claim 1	
[1pre]	A circuit board, comprising:
[1a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[1b]	conductive patterns on both sides of the insulating material layer;
[1c]	at least one microcircuit comprising a first surface and having contact areas on the first surface, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer;
[1d]	conductive material on sidewalls of the hole in the baseboard, in order to create interference protection around the microcircuit; and
[1e]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 2	
[2]	The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.
Claim 3	
[3]	The circuit board of claim 2, wherein the hardened insulating polymer layer contains epoxy and glass fibres.
Claim 4	
[4]	The circuit board of claim 3, wherein the baseboard is a glass-fibre reinforced epoxy board.

Claim 5	
[5]	The circuit board of claim 1, wherein the microcircuit is located between said conductive patterns on both sides of the insulating material layer.
Claim 6	
[6]	The circuit board of claim 1, wherein the microcircuit is secured in place in the hole with a filler material in the hole.
Claim 7	
[7]	The circuit board of claim 6, wherein the filler material contains epoxy.
Claim 8	
[8pre]	The circuit board of claim 1, wherein
[8a]	said at least one microcircuit comprises several microcircuits inside the insulating material layer, the microcircuits comprising first surfaces and contact area on their first surfaces, the first surfaces of the microcircuits being against the hardened insulating polymer layer; and
[8b]	the microcircuits are connected to each other in order to form an operational totality by means of the conductors in the contact opening and at least one of the conductive patterns.
Claim 9	
[9]	The circuit board of claim 1, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.
Claim 10	
[10]	The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

Claim 11	
[11pre]	The circuit board of claim 1, wherein
[11a]	said at least one microcircuit comprises several microcircuits embedded in the insulating material layer, and
[11b]	said conductive patterns connect the embedded microcircuits to each other in order to form an operational totality.
Claim 12	
[12pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least one of said circuit board substructures comprising:
[12a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[12b]	conductive patterns on both sides of the insulating material layer;
[12c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, the at least one microcircuit being inside the insulating material layer in a hole in the baseboard and having the first surface against the hardened insulating polymer layer; and
[12d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 13	
[13]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other are electrically connected to each other to form a multi-layered functioning totality.

Claim 14	
[14]	The multi-layered circuit board of claim 13, wherein said at least one microcircuit comprises at least two microcircuits.
Claim 15	
[15]	The multi-layered circuit board of claim 13, wherein said at least two circuit board substructures each comprise at least one memory circuit.
Claim 16	
[16]	The multi-layered circuit board of claim 13, comprising at least three circuit board substructures on top of each other and electrically connected to each other.
Claim 17	
[17pre]	The multi-layered circuit board of claim 12, wherein at least two of said circuit board substructures each comprise
[17a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[17b]	conductive patterns on both sides of the insulating material layer,
[17c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[17d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.

Claim 18	
[18]	The multi-layered circuit board of claim 12, wherein said at least two circuit board substructures on top of each other comprises a first circuit board substructure and a second circuit board substructure, the first and second circuit board substructures being electrically connected to each other to form a multi-layered functioning totality.
Claim 19	
[19pre]	The multi-layered circuit board of claim 18, wherein said first circuit board substructure comprises
[19a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[19b]	conductive patterns on both sides of the insulating material layer,
[19c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[19d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 20	
[20pre]	The multi-layered circuit board of claim 19, wherein said second circuit board substructure comprises
[20a]	an insulating material layer including a baseboard and a hardened insulating polymer layer,
[20b]	a conductive pattern on the insulating material layer,

[20c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer, and
[20d]	contact opening in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the conductive pattern, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper.
Claim 21	
[21]	The multi-layered circuit board of claim 20, wherein the hardened insulating polymer layers of both the first and second circuit board substructures contain epoxy.
Claim 22	
[22]	The multi-layered circuit board of claim 20, wherein the baseboards of both the first and second circuit board substructures are glass-fibre reinforced epoxy boards.
Claim 23	
[23]	The multi-layered circuit board of claim 19, wherein the at least one microcircuit of the first circuit board substructure is located between said conductive patterns on both sides of the insulating material layer of the first circuit board substructure.
Claim 24	
[24]	The multi-layered circuit board of claim 12, wherein the copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper.

Claim 25	
[25]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal plate above at least one of the microcircuits.
Claim 26	
[26]	The multi-layered circuit board of claim 20, wherein at least one of said first and second circuit board substructures comprises a metal foil below at least one of the microcircuits.
Claim 27	
[27pre]	A multi-layered circuit board, which includes at least two circuit board substructures on top of each other, at least two of said circuit board substructures each comprising:
[27a]	an insulating material layer including a baseboard and a hardened insulating polymer layer;
[27b]	conductive patterns on both sides of the insulating material layer;
[27c]	at least one microcircuit embedded in the insulating material layer, the embedded microcircuit having contact areas on its first surface and the first surface of the microcircuit being against the hardened insulating polymer layer; and
[27d]	contact openings in the hardened insulating polymer layer and copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns, wherein the copper contains at least one of electrochemically deposited copper and chemically deposited copper, and
[27e]	at least one of said at least two circuit board substructures further comprises a metal foil below at least one of the microcircuits.
Claim 28	
[28]	The circuit board of claim 1, wherein all the sidewalls of the hole in the baseboard are covered by a metal foil as the conductive material.

Claim 29	
[29]	The circuit board of claim 28, wherein the metal foil is an unbroken metal foil and surrounds the microcircuit in a lateral direction of the circuit board.
Claim 30	
[30]	The circuit board of claim 1, comprising a metal plate above the microcircuit.
Claim 31	
[31]	The circuit board of claim 1, comprising a metal plate below the microcircuit.
Claim 32	
[32]	The circuit board of claim 1, comprising a metal plate above and below the microcircuit.
Claim 33	
[33]	The circuit board of claim 28, comprising a metal plate above and below the microcircuit.

I. INTRODUCTION

Apple Inc. (“Apple”/“Petitioner”) petitions for IPR of claims 1-33 (“Challenged Claims”) of U.S. Patent No. 7,732,909 (“the ’909 patent”).

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR, as further supported by the Declaration of Dr. Neikirk (APPLE-1003).

Ground	Claims	§103 Basis
Ground 1A	12-21, 23-27	McCormack
Ground 1B	1-33	McCormack-Eiji
Ground 1C	12-27	McCormack-Eiji-Sugaya
Ground 2A	12-27	Sakamoto
Ground 2B	1-33	Sakamoto-Eiji
Ground 2C	12-27	Sakamoto-Eiji-Imoto

Each reference pre-dates the ’909 patent’s earliest possible priority date (January 31, 2002; “Critical Date”) and qualifies as prior art.

Reference	Date	Pre-AIA Basis
Sakamoto(APPLE-1004)	Dec. 7, 2001 (published)	§§102(a)/(b)
McCormack(APPLE-1005)	May 23, 2001 (filed)	§102(e)

Eiji(APPLE-1012)	Jan. 18, 2002 (published)	§§102(a)/(b)
Imoto(APPLE-1016)	Mar. 16, 2001 (published)	§§102(a)/(b)
Sugaya(APPLE-1007)	Oct. 18, 2001 (published)	§§102(a)/(b)

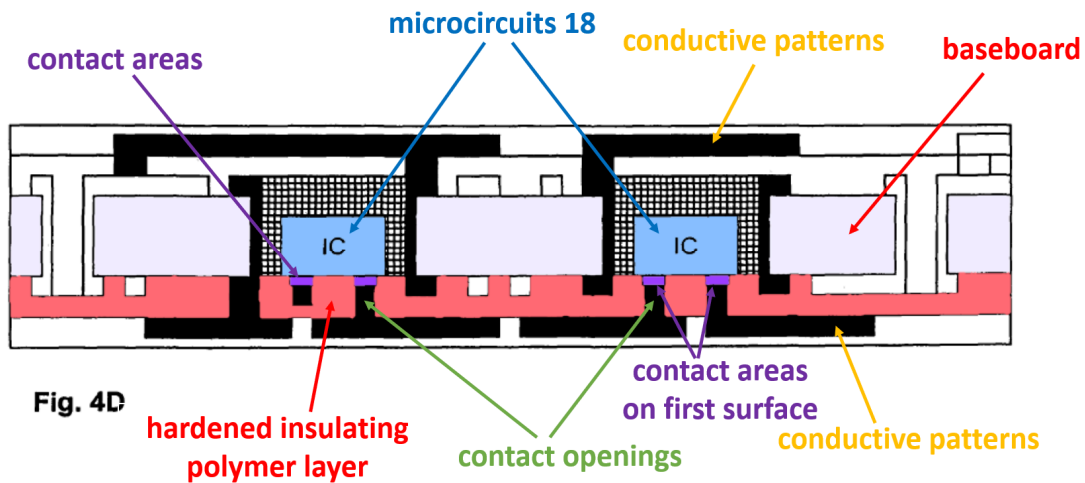
Sakamoto (APPLE-1004), Eiji (APPLE-1012), and Imoto (APPLE-1016) are certified English translations of JP2001-339165A (“Sakamoto”/APPLE-1022), JP2002-016327 (“Eiji”/APPLE-1024), and JP2001-068624A (“Imoto”/APPLE-1025). The Grounds are directed to the prior art references (APPLE-1004, APPLE-1012, APPLE-1016), for which the translations are cited throughout to identify relevant aspects thereof.

While a family member of Sugaya was cited on the face of the ’909 Patent, none of the above references were applied in a substantive office action.

III. ’909 PATENT

A. Brief Description

The ’909 patent recites an electronic module having electronic components embedded in a base. APPLE-1001, Title, Abstract. Figure 4D shows semiconductor components (microcircuits 18) embedded inside a baseboard and between two conductive pattern layers in which the components have contact areas on a first surface that is against a hardened insulating polymer layer. APPLE-1001, FIG. 4D and related descriptions, Cls. 1, 12; APPLE-1003, ¶¶61-63.



APPLE-1003, ¶61 (APPLE-1001, FIG. 4D (Annotated))

The '909 patent describes conductive material covering the sidewalls of the holes where microcircuits 18 are embedded, for protection from electromagnetic interference (EMI). *E.g.*, APPLE-1001, 3:61-4:9, 8:34-41, 8:64-66, Cl. 1. The '909 patent recites copper in the contact openings which “contains at least one of electrochemically deposited copper and chemically deposited copper.” *E.g., id.*, 6:21-25, Cls. 1, 12.¹

While the '909 patent touts these routine aspects as “invention,” they were

¹ “Electrochemically deposited copper” and “chemically deposited copper” are product-by-process elements that recite copper deposited by an electrochemical or chemical process. The recited processes have no patentable weight for purposes of determining unpatentability. *Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009).

not innovative. Those of skills in the art were aware of the structure having electrical components embedded in a base like circuit board to achieve miniaturization of electronic devices and using conductive material on the sidewalls of holes for incorporating the components to achieve EMI protection.

APPLE-1003, ¶¶67-294; *infra*, §VI.

B. Prosecution History Summary

During prosecution, a single substantive office action was issued, rejecting independent claim 1 and other claims as anticipated by Vu (2002/0020898), and claims 11 and 27 as unpatentable over Vu and Official Notice regarding chemical and electrochemical plating. APPLE-1002, 53-58. Pending claims 7, 26 and 29 were indicated as allowable, with claims 7 and 26 reciting “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit” and claim 29 reciting “a metal foil below at least one of the microcircuits.” *Id.*, 53-58, 100-104.

In response, applicant stated that “Claim 1 has been amended to incorporate the features of Claim 7,” and “Claim 14 has been amended to incorporate the features of Claim 26.” *Id.*, 43-45. Instead, however, the features of Claim 26 were **not actually introduced into independent claim 14**. Independent claim 14 (current claim 12) did not recite “conductive material on the sidewalls of the hole, in order to create interference protection around the microcircuit.” APPLE-1001,

Cl. 12. Following Applicant's amendments that remarkably omitted the narrowing features Applicant purported to include in the claims, a notice of allowance was issued, ending prosecution prematurely, without reciting features purported to overcome the Vu rejection and without application of pertinent prior art discussed herein. APPLE-1002, 18-21.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the '909 patent (a "POSITA") would have had at least a Bachelor's degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. APPLE-1003, ¶23.

V. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. The Board has repeatedly explained that "claim terms need only be construed to the extent necessary to resolve the controversy," and for purpose of the particular Grounds in this Petition, no formal construction is necessary because the prior art presented below satisfies the claims under any reasonable construction consistent with *Phillips*. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed.

Cir. 2011)².

VI. DETAILED EXPLANATION OF GROUNDS

A. GROUND 1A – McCormack renders obvious claims 12-21, 23-27

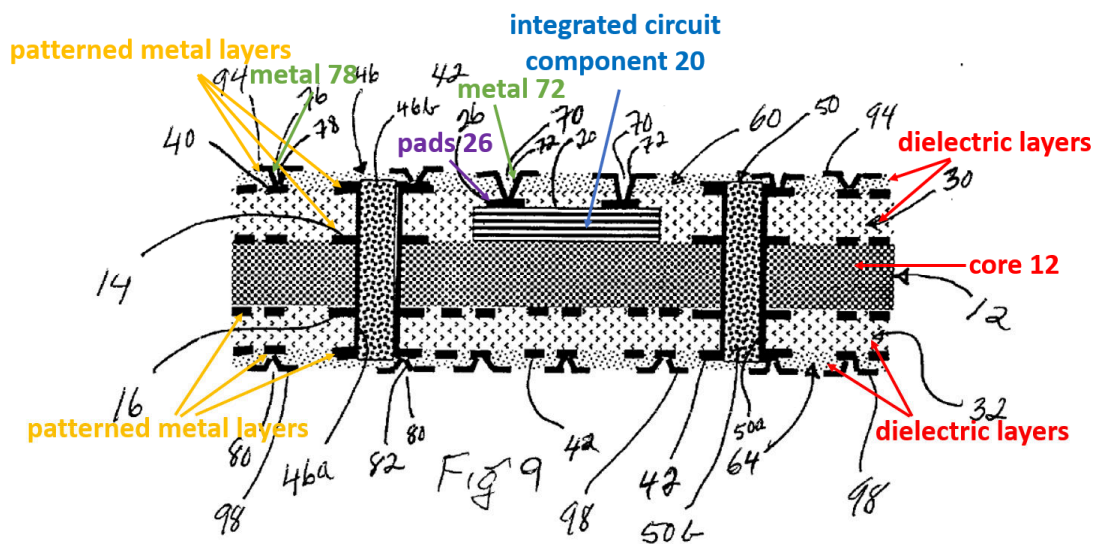
1. McCormack³

McCormack describes a circuit board having an embedded “integrated electronic component” and a method of producing such structure. APPLE-1005, Title, Abstract, [0009], [0024]-[0026], [0028]-[0029], Cl. 1, FIGS. 9, 11-13; APPLE-1003, ¶¶67-68. As shown in Figure 9, a circuit component 20 is mounted on an upper substrate surface of core substrate 12, and a dielectric layer (e.g., dielectric layer 30) is on the substrate surface of core 12 and over the integrated circuit component 20. APPLE-1005, Abstract, [0029], [0030], Cl. 1, FIG. 9. McCormack describes optional additional dielectric layers (e.g., dielectric layers

² Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

³ General descriptions provided for this and other references and combinations are incorporated into each subsection and mapping of the claims that includes citations to these references. All emphasis added unless otherwise indicated.

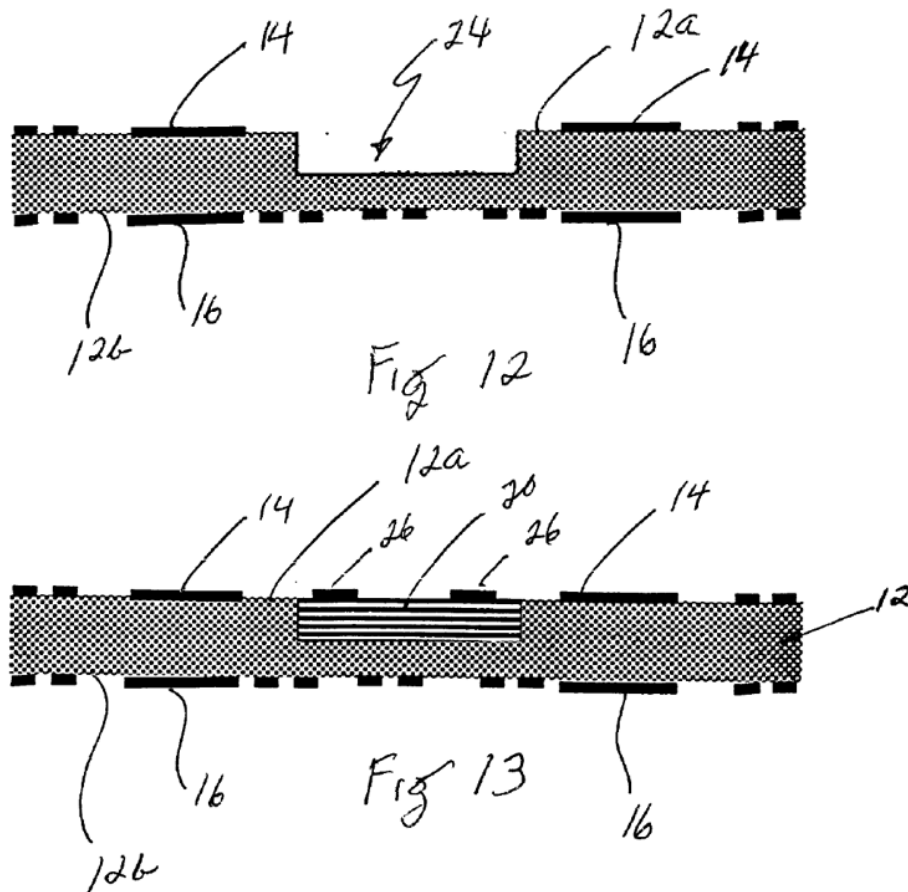
60, 32, 64) on both the upper and lower sides of the core substrate 12, with patterned metal layers on each of the dielectric layers and the core substrate that are interconnected through metal-lined openings (e.g., metal liners 72, 78 and 82 in openings 70, 76 and 80, respectively) and conductive feed-throughs (e.g., metal-lined vias 46, 50 and 18). APPLE-1005, Abstract, [0009] (“may also comprise”), [0030]-[0032], [0026]. McCormack further describes that openings 70 are formed through the dielectric layer(s) above the integrated circuit component, “to expose pads 26 of the integrated circuit component 20,” and openings 70 are then “metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26.” *Id.*, [0032]. APPLE-1003, ¶¶69-71.



APPLE-1003, ¶69 (APPLE-1005, FIG. 9 (Annotated))

McCormack discloses an example technique to embed components in its substrate, with “a cavity” provided beforehand in the core substrate 12 where the

integrated circuit component is disposed. APPLE-1005, [0009], [0024]- [0025] (indicating FIGS. 12 and 13 depict an alternative embedding method, disposing an IC component in a cavity in the core substrate instead of on a surface, while sharing the same core substrate of FIG. 2 and FIG. 9), [0026]-[0029], FIGS. 12, 13; APPLE-1003, ¶72.



APPLE-1003, ¶72 (APPLE-1005, FIGS. 12, 13)

2. Application to Challenged Claims

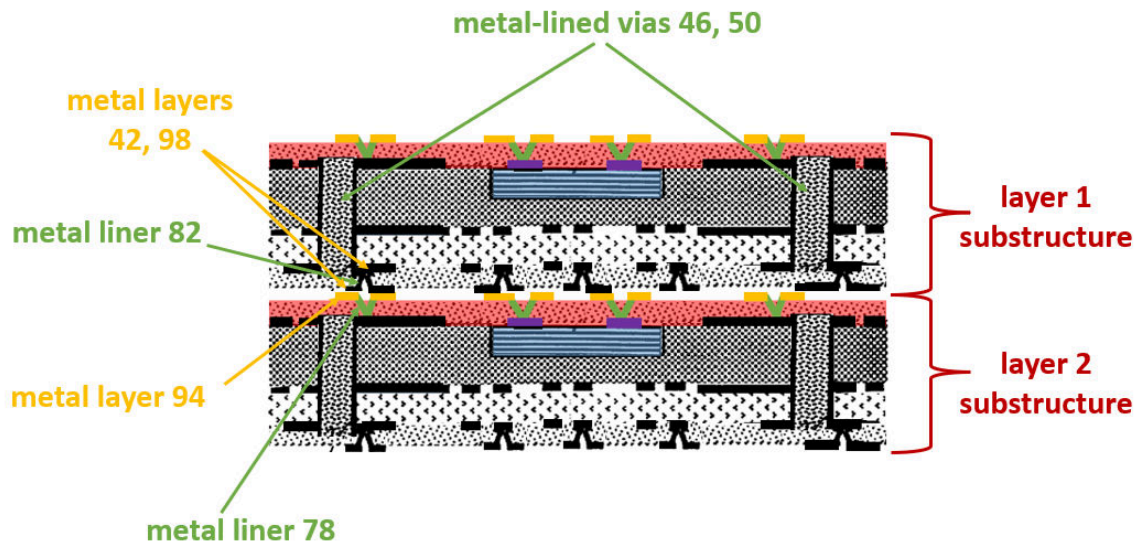
[12pre]

To the extent the preamble is limiting, McCormack provides [12pre].

APPLE-1003, ¶¶91-97. For example, McCormack describes “a circuit apparatus and a method for embedding electronic components within multi-layer substrates, particularly printed **circuit boards**.” APPLE-1005, [0002]; *see also* Abstract, [0009]-[0012], [0029], FIGS. 9, 12, 13, Cls. 1, 17, 35; *infra*, Analysis of [13], [17]. APPLE-1001, 1:63-67; APPLE-1003, ¶91. McCormack additionally describes “dielectric build-up” of multiple layers of its printed circuit board assembly such as in FIG. 9, “by means well known to those skilled in the art (e.g., post plating for stacked via build-up structures).” APPLE-1005, [0032]; APPLE-1003, ¶92.

To be clear, stacking multiple layers of circuit-board substructures on top of each other and mounting a plurality of electronic components in the same and different such layers, in accordance with McCormack’s teachings, to form a “multi-layered” structure was common practice and well known in the field. A POSITA would have been motivated to stack multiple layers on top of each other in order to achieve known benefits of high-density, improved performance, reduced manufacturing cost, space saving, and short-distance wiring. APPLE-1003, ¶¶92-96. The well-known nature of multi-layer structures and associated benefits, was highlighted during original prosecution, in which applicant did not dispute the examiner’s conclusion that “it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and a second circuit board substructure on top of each other,

since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.” APPLE-1002, 107-110; APPLE-1003, ¶97. An example resulting stack-up of such a “multi-layered” structure is shown below, with two circuit board substructures annotated as “layer 1 substructure” (i.e. substructure 1, which contains one or more layers) and “layer 2 substructure” (i.e. substructure 2, which contains one or more layers). *See also, infra*, Analysis of [13], [17].



APPLE-1003, ¶97 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))
[12a]

McCormack discloses Element [12a]. APPLE-1003, ¶¶98-105. For example, McCormack’s “circuit board substrate” or “core substrate” 12 and one or more “dielectric layer[s]” (e.g., above the core substrate) having integrated electronic components embedded therein collectively provide *an insulating material layer*. APPLE-1005, Abstract, [0009]-[0011], [0026], [0029], [0032]-

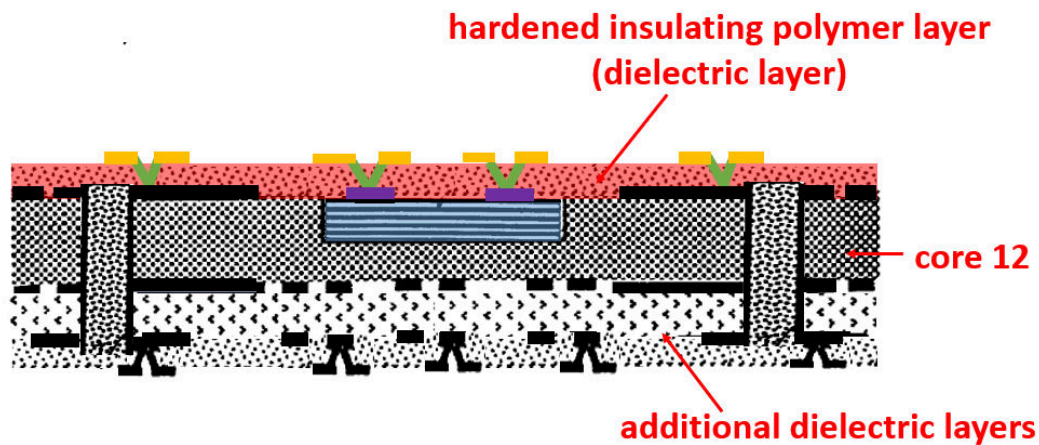
[0033] (“Suitable dielectric material for the core 12 ... and/or dielectric layers 30, 32, 60 and 64 include B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicones, well known to those skilled in the art. ...”), Cls. 1, FIG. 9, 17, 35; APPLE-1003, ¶98. Additionally, McCormack provides Element [1a] in a second manner in which dielectric layers below the core substrate (e.g., “dielectric layer 32,” or “dielectric layers 32 and 64”) together with core substrate 12 and the dielectric layer(s) above the core substrate 12, collectively provide an insulating material layer as claimed. APPLE-1003, ¶99.

Core substrate 12 (either by itself or together with dielectric layers 32, 64 below it) provides a **baseboard**. APPLE-1005, [0009], [0024]-[0026], FIGS. 12-13; APPLE-1003, ¶100. McCormack describes example material for core 12, including “epoxy resins” or other materials, which is cured with heat and pressure. APPLE-1005, [0033] (listing a variety of materials for the dielectric layers and core). This is like the ’909 patent’s description of its baseboard. APPLE-1001, 3:48-57 (“a glass-fibre reinforced epoxy board”). Additionally, core 12 is used to house an integrated electronic component (McCormack’s integrated circuit components 20), like the ’909 patent’s baseboard. *Compare e.g.*, APPLE-1001, 2:22-26, 3:23-33 *with e.g.*, APPLE-1005, Abstract, [0009], Cl. 1; APPLE-1003, ¶¶100-101, 105.

McCormack discloses a **hardened insulating polymer layer** provided by a

“dielectric layer” over the upper surface of core 12. APPLE-1003, ¶102. For example, McCormack describes dielectric layer(s) (e.g., dielectric layers 30 and 60) “placed, flowed or laminated over the integrated circuit component 20” and over the upper surface of core 12. APPLE-1005, [0030]-[0032]. A POSITA would have found obvious from McCormack’s descriptions that one, two, or more than two dielectric layer(s) (along with associated metal layer(s)) can be used above and/or below the core substrate 12, to provide an integrated electronic component in accordance with McCormack’s teachings. APPLE-1005, [0009] (“may also comprise”), [0030]-[0032], [0035]; APPLE-1003, ¶102. A POSITA would have been motivated to use a single dielectric layer, for example, when implementing a circuit board having an embedded “integrated electronic component” in accordance with McCormack’s teachings, in order to provide a space-efficient design having reduced thickness and enhanced manufacturing efficiency (e.g., by including fewer processing steps). Moreover, a POSITA would have recognized that, with the component positioned in a hole in core 12, a single dielectric advantageously covers the component to provide a planar surface without use of an intermediate dielectric (e.g., as depicted before applying a second dielectric and a metal layer on the second dielectric). APPLE-1003, ¶102. In the resulting configuration, a single dielectric layer is disposed over the integrated circuit component 20 and the upper surface of core 12, which provides *a hardened*

insulating polymer layer as claimed. APPLE-1003, ¶102.



APPLE-1003, ¶102 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

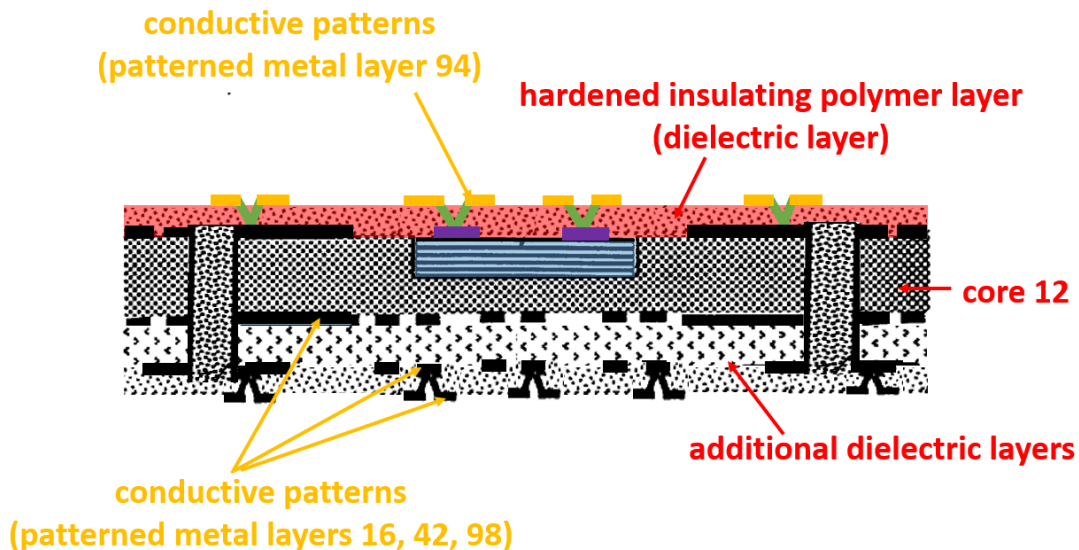
To be clear, the dielectric material described by McCormack is an *insulating* material and includes *polymer*. APPLE-1005, [0033] (“B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicons . . . thermosetting materials, such as high glass transition anhydride-cured epoxy composition . . . high temperature thermoplastic materials”). APPLE-1003, ¶103. The dielectric layer is “cur[ed]” at “a subsequent heating step” “upon additional exposure to heat and pressure,” indicating it is a *hardened* layer. *Id.*, [0033]; APPLE-1003, ¶104; APPLE-1001, 5:32-35.

[12b]

For example, McCormack describes a metal layer (e.g., metal layer 94) on the upper side of the circuit board, that is “disposed in” a dielectric layer and “patterned,” and a metal layer (e.g., “patterned metal layer 16”) on the lower side

of the circuit board (*conductive patterns on both sides of the insulating material layer*). APPLE-1005, [0032]; *see also* [0021], [0026] (“Metal layers 14 and 16 are optional, and may be any suitable conductive metal, such as copper.”), [0027] (“Patterning of the metal layers ... may be accomplished by etching to develop the desired patterned metal profile.”), [0030]-[0031], FIGS. 7-9; APPLE-1003, ¶106.

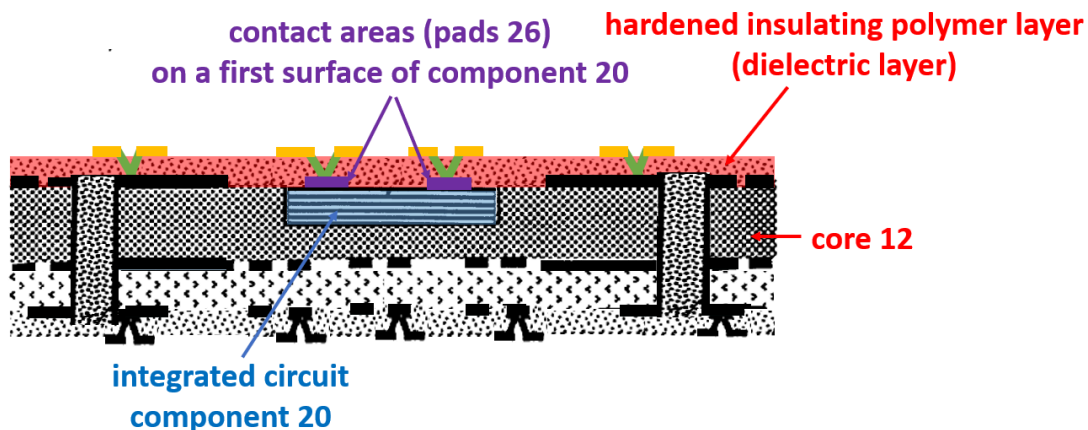
In the second manner that McCormack provides the claimed insulating material layer (in which core substrate 12 and one or more dielectric layers above and below core substrate 12 collectively provide an insulating material layer (Analysis of [1a])), patterned metal layer 42 and/or patterned metal layer 98 provides the recited *conductive patterns* on the lower side of the insulating material layer. APPLE-1003, ¶107.



APPLE-1003, ¶107 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

[12c]

McCormack describes *at least one microcircuit* (e.g., “at least one integrated electronic component” or “integrated circuit component” 20) in cavity 24 of core 12 (*being inside the insulating material layer in a hole in the baseboard*), the integrated circuit component *having contact areas* (e.g., “conductor pads 26”) *on its first surface*. APPLE-1005, Abstract, [0009], [0028], [0029] (“The integrated circuit component 20 may include one or more conductor pads 26 ...”), Cls. 11, 25; APPLE-1003, ¶108. The *first surface* of the component is *against the hardened insulating polymer layer* (e.g., dielectric layer over integrated circuit component 20). *See also*, APPLE-1005, [0030]-[0032]; *supra*, §VI.A.2, Analyses of [12a]-[12b]; APPLE-1003, ¶108.



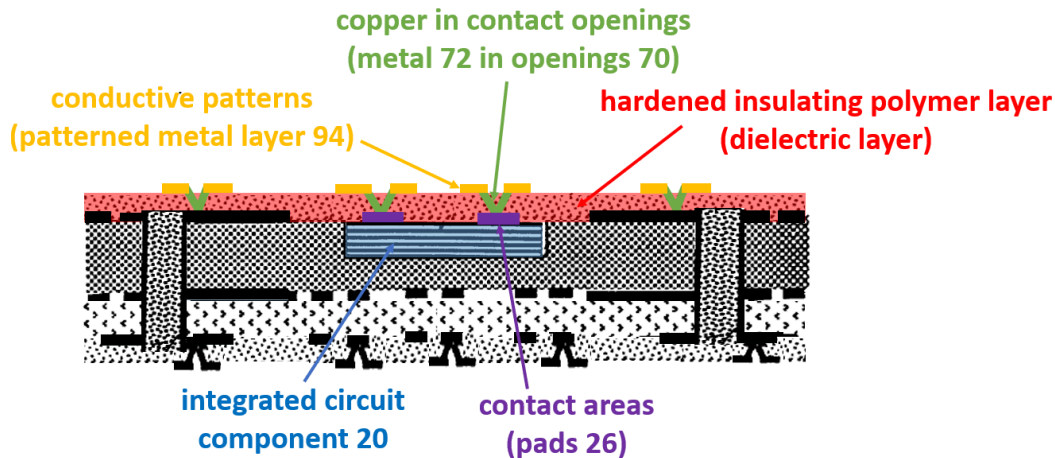
APPLE-1003, ¶108 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

A POSITA would have understood that integrated circuit components are a type of *microcircuit* because an integrated circuit component is a miniaturized

electronic circuit that contain a network of interconnected semiconductor devices (e.g., transistors and diodes) and passive components (e.g., resistors, inductors, and capacitors), on a small substrate (e.g., fabricated onto a single semiconductor wafer). APPLE-1003, ¶109.

[12d]

McCormack describes **contact openings** (e.g., “openings 70”) in the **hardened insulating polymer layer** (e.g., dielectric layer over the component), and **copper in the contact openings** (e.g., “metal 72” made of copper). APPLE-1005, [0032], FIG. 9. McCormack describes forming “openings,” such as by laser drilling or the like, through the dielectric layer(s) above the integrated circuit component, “to expose pads 26 of the integrated circuit component 20.” *Id.* “Openings 70 are then metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26.” *Id.*; *see also*, Abstract (“metal-lined opening”), [0009]-[0011], [0021], Cls. 1, 12 (“at least one first pad in contact with said metal lining in said opening”), 17, 35, FIG. 9. The metal 72 thus forms electrical contacts between the pads of the component and the patterned metal layer above. *Id.*; APPLE-1003, ¶110.



APPLE-1003, ¶110 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

To be clear, even if not revealed to a POSITA by the description offered by McCormack (which it is), a POSITA would have predictably implemented the metal 72 in accordance with McCormack's teachings to form electrical contacts between the pads of the component and the patterned metal layer on the dielectric layer that is over the component. APPLE-1003, ¶111. Indeed, based on McCormack's description, a POSITA would have understood, and found obvious, that when the component is buried in a cavity in the core substrate 12 (e.g., FIGS. 12-13) and a single dielectric layer is provided above the core substrate, the metal 72 of openings 70 (*copper in the contact openings*) likewise penetrates through that dielectric layer (*in the hardened insulating polymer layer*), in order to expose pads 26 of the component *for forming electrical contacts between* pads 26 (*contact areas*) and metal layer 94 (*at least one of the conductive patterns*). A

POSITA would have done so to effectuate McCormack's expressly stated objective of thereby electrically connecting the component with the metal layers of the circuit board. APPLE-1005, Abstract, [0032], FIG. 9, Cl. 1; APPLE-1003, ¶111.

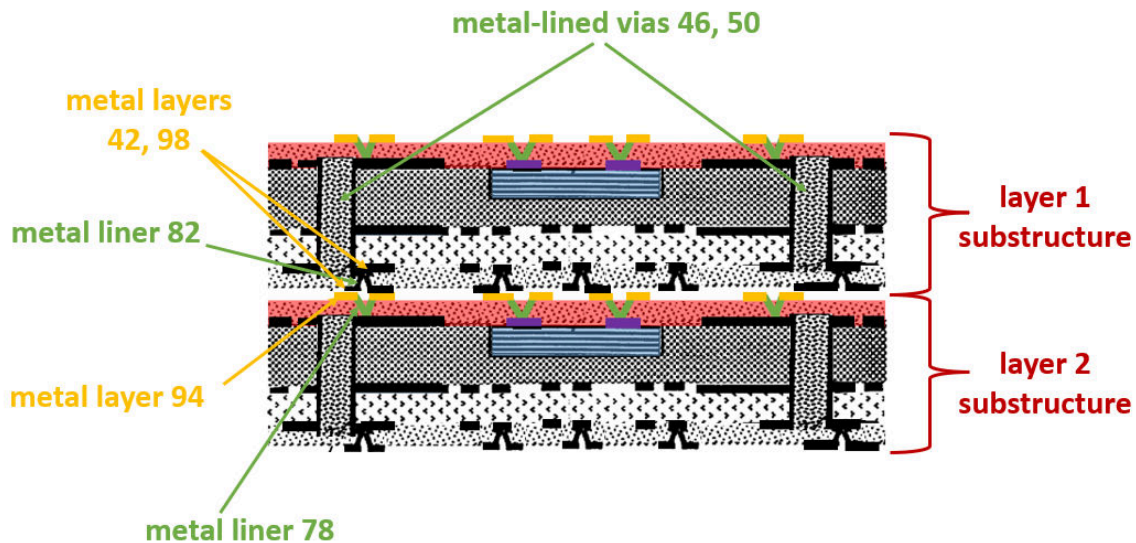
As noted in §III.A., recitation of “electrochemically deposited” and “chemically deposited” copper is a product-by-process element, and thus not limiting for purpose of invalidity. McCormack describes copper, as claimed. That is enough. Even if the process recitations were considered limiting, McCormack provides it. The formation of metal 72 lining openings 70 is accomplished “by the combination of e-less and electrolytic plating.” APPLE-1005, [0032]. A POSITA would have understood that “e-less” (electroless) chemical plating of copper provides *chemically deposited copper*, and “electrolytic plating” of copper provide *electrochemically deposited copper*. APPLE-1003, ¶112.

[13]

McCormack discloses conductive feed-throughs including “metal-lined vias 46 and 50 formed by drilling openings through the entire FIG. 5 circuit board assembly,” which provide electrical connection between the metal layers above and below the embedded component (e.g., patterned metal layer 94 and patterned metal layer 16, 42, or 98). APPLE-1005, [0031]; *see also id.*, [0009], [0018]-[0019], [0020]-[0022], [0026], FIGS. 6-10; APPLE-1003, ¶113.

McCormack further describes metal-lined openings within dielectric layers where the metal-lined vias do not pass through, to make electrical connections between metal layers on both sides of each of such dielectric layers. *See e.g., id.*, [0032]; *see also* Abstract, [0009]-[0011], FIG. 9. APPLE-1003, ¶114.

In the multi-layered structure illustrated below, a POSITA would have understood, and found obvious, that layer 1 substructure and layer 2 substructure (*two circuit board substructures on top of each other*) are electrically connected to each other to form a multi-layered functioning totality, through the metal layers on the surfaces (e.g., metal layers 94, 98) of the adjacent substructure layers. *Supra*, §VI.A.2, Analyses of [12pre]-[12b]; APPLE-1003, ¶115.



APPLE-1003, ¶115 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

[14]

McCormack describes a stacked multilayer structure with one or more

integrated circuit components (*at least two microcircuits*) in the same and/or different substructures. APPLE-1005, [0029]-[0030], [0032]. Indeed, McCormack, expressly indicates the “circuit board having **at least one** integrated electronic component,” thereby disclosing at least two microcircuits inside the insulating material layer. *Id.*, see also [0010]-[0011], [0030] (“**one or more** of the integrated circuit components 20 have been suitable [*sic*] disposed where desired”), Cls. 1, 11 (“a **second** integrated electronic component”), 17, 35, FIG. 11; APPLE-1003, ¶¶116-117; see also APPLE-1005, [0007] (“Dineen, et al.”).

Even if McCormack did not expressly describe several integrated circuit components inside its dielectric layers (including core 12) of the circuit board assembly, a POSITA would have found this conventional configuration to be obvious based on McCormack’s suggestions. APPLE-1003, ¶¶118-119. As discussed above, McCormack describes use of multiple components. A POSITA would have been prompted to do so based on predictable benefits of positioning several components inside the insulating material layer to achieve the functionality of multiple components and/or to maintain a compact overall profile while doing so. APPLE-1003, ¶120. A POSITA would have had a reasonable expectation of success in doing so, especially in view of McCormack’s express suggestion for multiple integrated circuit components, and the known implementation of multiple components inside an insulating material layer. APPLE-1003, ¶120. *Supra*,

§VI.A.2, Analysis of [1c].

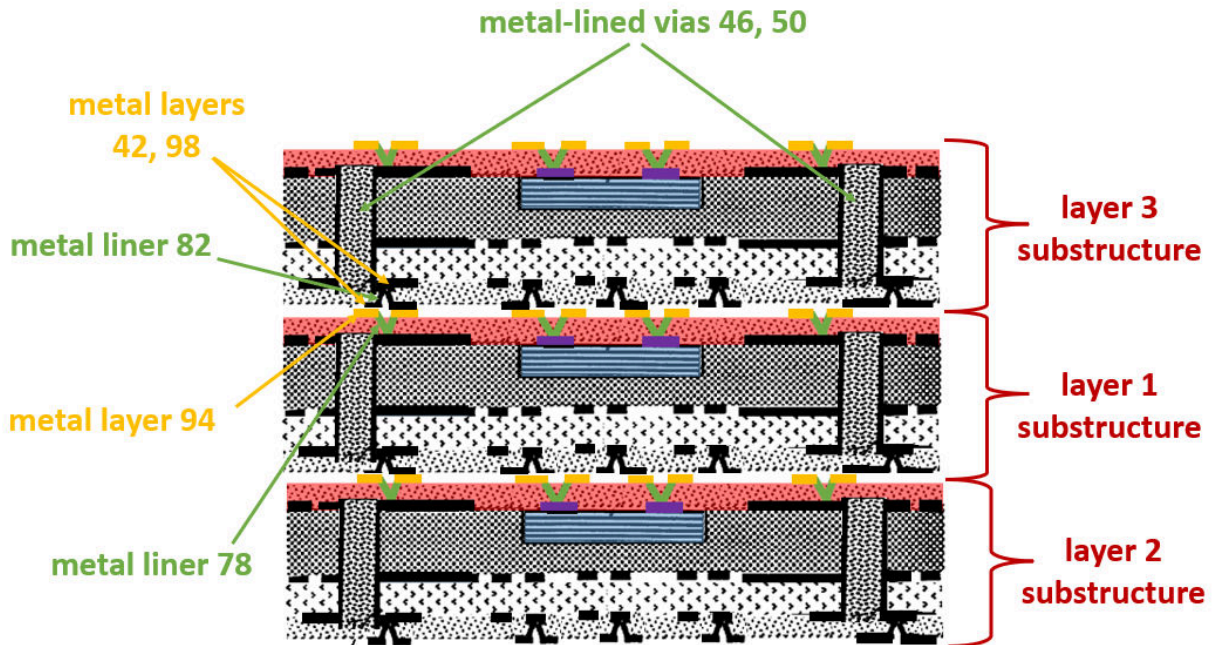
[15]

As discussed above, McCormack describes a plurality of integrated circuit components electrically connected to each other in each circuit board substructure. *Supra*, §VI.A.2, Analyses of Element [12pre] and Claim [14]; APPLE-1003, ¶121. A POSITA would have understood and found obvious that such integrated circuit components of each substructure described by McCormack include ***at least one memory circuit***—a common type of integrated circuit used to store data in semiconductor devices used in computers, smartphones, embedded systems, and other electronic devices. APPLE-1003, ¶121. Moreover, a POSITA would have been motivated to do so to enhance the circuit board structure by imparting memory functionality, thereby expanding the potential uses and applications of the resulting device. *Id.*

[16]

McCormack renders obvious the use of additional circuit board structures in a multi-layered circuit board, and such structure amounted to duplication of parts. *Supra*, Analysis of [12pre]; APPLE-1003. In the resulting structure, three similar circuit board substructures are laminated on top of each other and electrically connected to each other through the patterned metal layers and metal-lined

openings and metal-lined vias on each of the substructures. APPLE-1003, ¶¶122-123; *supra*, §VI.A.2, Analysis of Claim [13].



APPLE-1003, ¶122 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

[17pre]-[17d]

The resulting device includes two substructures having similar features, including the features described above, and thus renders obvious [17pre]-[17d].

Supra, §§VI.A.2, Analyses of [12pre]-[12d]; APPLE-1003, ¶124.

[18]

Supra, §§VI.A.2, Analyses of Claims [13] and [16]; APPLE-1003, ¶125.

[19pre]-[19d]

Supra, §§VI.A.2, Analyses of [12pre]-[12d] and Claim [18]; APPLE-1003, ¶126.

[20pre]-[20d]

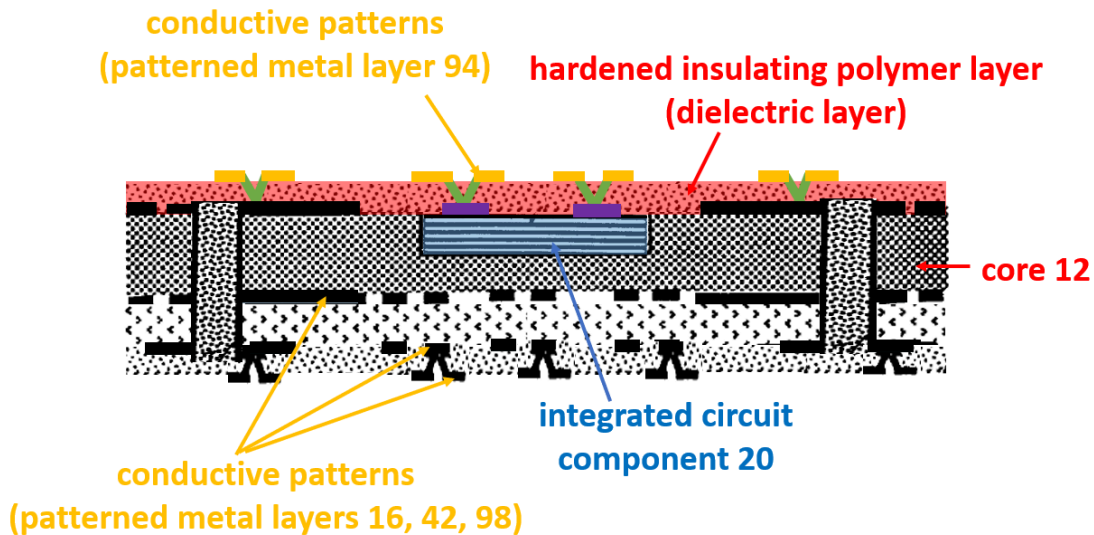
Supra, §§VI.A.2, Analyses of [12pre]-[12d] and Claim [19]; APPLE-1003, ¶127.

[21]

Supra, §§VI.A.3, Analyses of Element [12a] (McCormack’s dielectric layers contain “epoxy resins”) and Claim [20]; APPLE-1003, ¶128.

[23]

Supra, §§VI.A.2, Analyses of [12b]-[12c]. The resulting device in accordance with McCormack’s teachings includes integrated circuit component 20 **(at least one microcircuit) between** patterned metal layer 94 and patterned metal layer 16 (and 42, 98) **(conductive patterns) on both sides of the insulating material layer**. APPLE-1003, ¶129.



APPLE-1003, ¶129 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

[24]

As discussed above, metal 72 made of copper formed in openings 70 (*copper in the contact openings*) is formed by a “combination of e-less and electrolytic plating,” which provides *a first layer of chemically deposited copper* (through e-less plating) *and a second layer of electrochemically deposited copper* (through electrolytic plating) *on the first layer of chemically deposited copper*. *Supra*, §VI.A.2, Analysis of [12d]; APPLE-1003, ¶130. Indeed, a POSITA would have found it obvious, from McCormack, to apply the copper layers in a sequence in which the electrochemically deposited copper is applied to thicken the chemically deposited copper. *Id.*; APPLE-1003, ¶130. Moreover, a POSITA would have recognized, from McCormack, the finite options of e-less plating followed by electrolytic plating or vice versa, and would have selected e-less

plating followed by electrolytic plating as a known, effective technique for forming copper conductors. *Id.*

[25]

McCormack describes that “metal layers ... may be any suitable conductive material, such as copper. ... disposed ... by any suitable means, such as by lamination, plating, sputtering or chemical vapor deposition (CVD).” APPLE-1005, [0026]; FIG. 9. A POSITA would have understood and found obvious that these metal layers are metal films on a substrate, unpatterned portions of which providing the *metal plates* as claimed, to provide beneficial EMI shielding. APPLE-1003, ¶¶131-132.

This is just like the '909 patent's description of forming its metal plates (also referred to as “metal foil” and “film” in the specification). APPLE-1001, 5:47-56, FIG. 1J, 8:44-9:15; *see also id.*, 4:40-59 (describing a similar process for forming a metal coating 8 in the form of “**a layer of copper** (e.g., c. 5 μm). **Lamination** takes place with the aid of pressure and heat. ... the **film** is thus an RCC (Resin Coated **Copper**) **foil**,” on the bottom side of the circuit board below the microcircuit at Stage F, (FIG. 1F)); *see also* APPLE-1001, 9:11-13. APPLE-1003, ¶133.

[26]

Supra, §VI.A.2, Analyses of Claims [23], [25] (at least one of McCormack's

metal layers 16, 42 and 98 below integrated circuit component 20 (*below at least one of the microcircuits*) formed by “lamination” and “plating” of copper provides a *metal foil*). APPLE-1003, ¶134.

[27pre]-[27d]

Supra, §§VI.A.2, Analyses of [17pre]-[17d]; APPLE-1003, ¶135.

[27e]

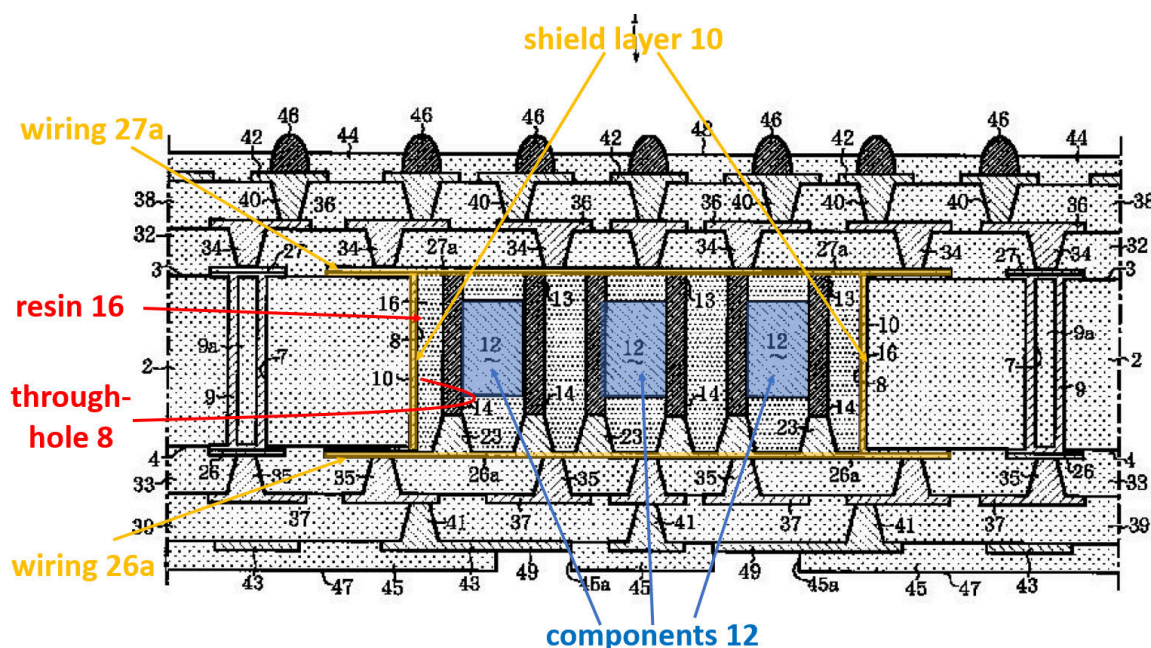
Supra, §§VI.A.2, Analyses of Claims [25] and [26]; APPLE-1003, ¶136.

**B. GROUND 1B – McCormack and Eiji render obvious
Claims 1-33**

1. Eiji

Eiji describes “a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded[.]” APPLE-1012, Abstract, FIG. 1; *see also*, [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6; APPLE-1003, ¶¶78-80.

Eiji also describes filling the through-hole with a resin (e.g., resin 16), “[i]n this way, electronic components are securely embedded in through-holes or recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer.” *Id.*, [0007], [0010], [0019], cls. 2, 7, FIGS. 1, 3; *see also*, [0031]; APPLE-1003, ¶81.



APPLE-1003, ¶81 (APPLE-1012, FIG. 1 (Annotated))

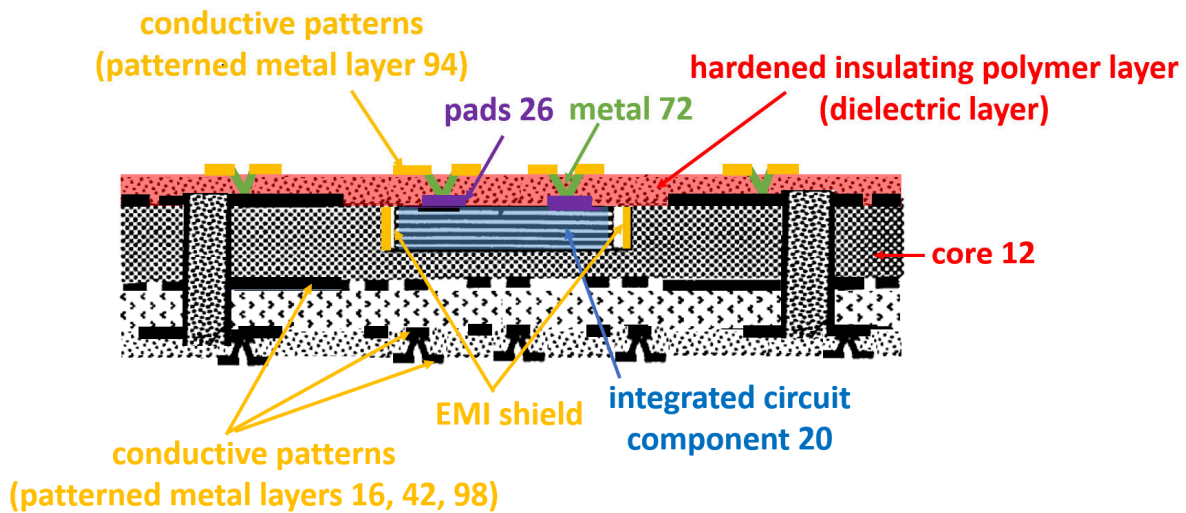
Eiji further describes wiring layers 26 and 27, “formed in the upper and lower openings to the through-hole 8.” *See e.g.*, APPLE-1012, [0011], [0023]. These metal layers are formed from “copper foil” with thickness of more than “several 10 μm thick.” *Id.*, [0017] (26, 27 formed from “copper foil 5, 6 that is several 10 μm thick”), [0021] (“Electroless and electrolytic copper plating is applied to ... the copper foil 5, 6” to form even thicker metal layers); *see also* [0025] (“Shielding layers 60a and 60b, each about 25 μm thick”), FIGS. 1, 4; APPLE-1003, ¶82.

2. Predictable Combination of McCormack and Eiji

A POSITA would have been motivated to enhance the McCormack

multilayer printed circuit board through implementation of Eiji's teachings of a shield layer on the sidewalls of the cavity in which an electronic component is embedded, to make the electronic components built into an insulating substrate "less susceptible to external electromagnetic waves," to "reduce the effects of noise generated by the circuits constituting these electronic components," and to "stabilize the electrical characteristics" of the system, for example. APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶138.

In the predictable combination, a shielding layer (e.g., Eiji's "shielding layer 10" composed of a copper plating film) that shields electromagnetic waves is formed on an inner surface of a cavity in the core (e.g. McCormack's "cavity 24" in the core 12), before disposing integrated circuit component 20 therein, in accordance with Eiji's teachings. APPLE-1005, [0009], [0024]-[0025], [0028], FIGS. 12-13, Cls. 11, 25-26; *see also id.*, [0007]; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶¶139-142.



APPLE-1003, ¶140 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

Additionally, a POSITA would have been motivated to implement the combination by utilizing a glass fiber epoxy (e.g., for core substrate 12 and/or dielectric layers), in accordance with Eiji's suggestions. APPLE-1012, [0012], [0038], Abstract; APPLE-1003, ¶143.

Multiple reasons would have prompted a POSITA to utilize an EMI shield feature in accordance with Eiji in a substrate cavity described by McCormack. APPLE-1003, ¶143.

First, a POSITA would have been motivated to combine McCormack and Eiji to provide protection against external electromagnetic waves, reduce influence by noise from circuits composed of various electronic components, and to stabilize electric characteristics of the entire system. APPLE-1003, ¶144.

McCormack already teaches providing a hole or cavity, such as "cavity 24"

in core substrate 12 for accommodating an electronic component such as an integrated circuit component 20. APPLE-1005, [0009], [0024]-[0025], [0028], FIGS. 12-13, Cls. 11, 25-26; *see also id.*, [0007] (incorporating by reference “Dineen”); APPLE-1003, ¶145. McCormack also discloses mounting multiple electronic components close to each other in the same circuit board assembly and in “high frequency applications.” APPLE-1005, [0006], [0008], [0034]; APPLE-1003, ¶146. A POSITA would have recognized that electronic components incorporated into an insulating board can be easily affected by an external electromagnetic wave, and influenced by noise generated by a circuit composed of the electronic components, as evidenced by Eiji. APPLE-1012, [Abstract]; APPLE-1003, ¶147. A POSITA would have predictably looked towards other teachings such as Eiji for solutions. APPLE-1003, ¶148. Eiji provides a solution for these common problems that can “stabilize the electrical characteristics” of the system. APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶148.

Second, a POSITA would have been motivated to combine Eiji with McCormack to enhance the mechanical strength of McCormack’s core 12 and dielectric layers. APPLE-1003, ¶149. In particular, Eiji describes composite materials of glass fibers with epoxy resin, which a POSITA would have been prompted to utilize in McCormack to enhance robustness of the construction. *Id.*;

APPLE-1012, [0012], [0038], Abstract.

Third, a POSITA would have been prompted to combine McCormack and Eiji because doing so was the application of known techniques (forming a shield layer on the inner surface of sidewalls of a through hole or cavity provided in an insulating board for incorporating an electronic component)⁴ to a known device (McCormack’s multilayer printed circuit board having a hole or cavity 24 in core substrate 12 to accommodate an electronic component such as integrated circuit component 20) ready for improvement to yield predictable results (benefits articulated above). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (“[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.”). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that McCormack and Eiji describe similar circuit boards with electronic

⁴ McCormack also teaches “conventional” techniques of “metal lining” various via holes and openings in an insulating board, further leading a POSITA to this predictable configuration. APPLE-1005, [0031] (“opening for vias... are metal-lined (e.g., copper lined) with metal liners”), [0032], Cl. 1; APPLE-1003, ¶152.

components embedded inside holes/cavities of an insulation board, and because the modifications would have been implemented largely by adding a metal layer on the sidewalls of the hole/cavity, in order to create interference protection around the electronic components, and use of epoxy resin for an insulating substrate—options Eiji already demonstrates to be successful. APPLE-1003, ¶¶150-152. Moreover, McCormack and Eiji describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above. *Id.*

3. Application to Challenged Claims

***[1pre]-[1c]*⁵**

The McCormack-Eiji combination provides [1pre]-[1c], as set forth above. *Supra*, Analysis of [12pre]-[12c]; APPLE-1003, ¶154.

[1a]

To the extent McCormack’s description regarding suitable materials for its

⁵ To be clear, McCormack-Eiji renders obvious independent claim 1 and its dependent claims without modification to utilize multiple circuit board substructures on top of each other that is described with reference to claims 12-27. APPLE-1003, ¶153.

dielectric layers and core were not considered to provide the claimed baseboard, McCormack-Eiji renders it obvious. APPLE-1003, ¶¶155-157. In the combination, “a glass-epoxy resin composite material” is used for the insulating substrate, resulting in a baseboard construction just like the ’909 patent’s example. APPLE-1012, [0012], [0038], Abstract; APPLE-1001, 3:45-55 (“glass-fibre reinforced epoxy board...”).

[1d]

The McCormack-Eiji combination renders obvious Element [1d]. As discussed in §VI.B.2 (McCormack-Eiji combination), the combined system includes an integrated circuit component 20 (*microcircuit*) located in a cavity 24 in an insulating board (*the hole in the baseboard*). APPLE-1003, ¶158. A shield layer “composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of” cavity 24 (*conductive material on sidewalls of the hole*). *Id.*

The shielding layer material and configuration of the combined system, in accordance with Eiji’s teaching, is just like the formation mechanism disclosed in the ’909 patent for growing the metal foil on the sidewalls of the holes by copper plating. APPLE-1012, [Abstract], [0012]; *compare id.*, [0017] (“electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8”) *with* APPLE-1001, 3:61-4:9 (“coating the holes with a thin

layer of chemical copper and then continuing the coating using an electrochemical copper-growing method...”), 8:39-46; APPLE-1003, ¶¶159-161; *see also* APPLE-1005, [0031]-[0032]; *supra*, §VI.A.2.

[1e]

Even if McCormack alone did not render obvious [1e] (which it does, *supra*, XI.3, [12d]), McCormack-Eiji renders it obvious. Eiji describes “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate—techniques a POSITA would have beneficially utilized to implement the formation of copper metal lining in the openings. APPLE-1012, [0017]; APPLE-1003, ¶162.

[2]

Supra, §VI.A.2, Analysis of [12a] (McCormack’s dielectric layers contain “epoxy resins”); APPLE-1003, ¶163.

[3]

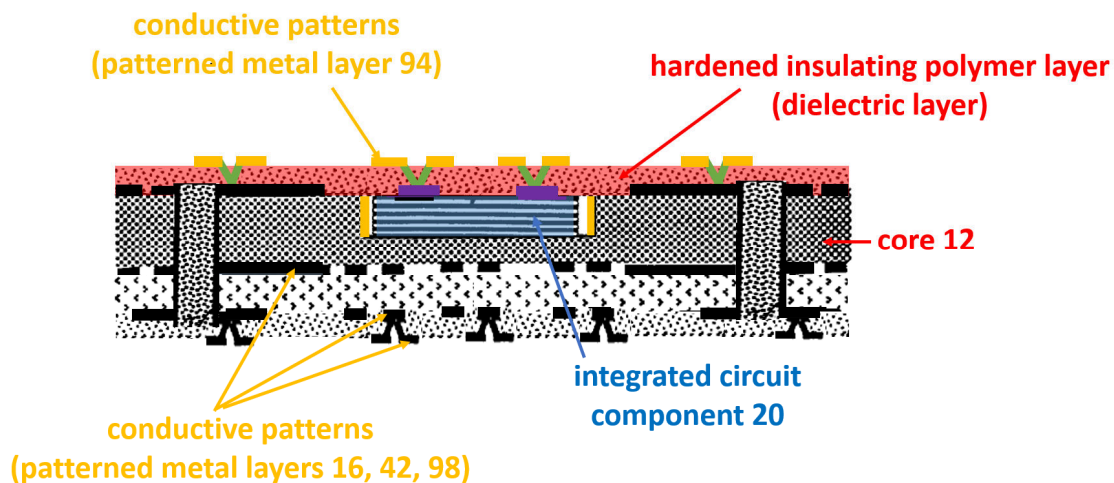
McCormack-Eiji discloses Claim [3]. McCormack-Eiji’s core 12 and dielectric layers, including the dielectric layer over core 12 and the embedded component (*the hardened insulating polymer layer*), include composite materials of *glass fibers* with *epoxy* resin, in accordance with Eiji’s teaching. *Supra*, §VI.B.3, Analysis of [1a]; APPLE-1003, ¶164.

[4]

McCormack-Eiji renders obvious Claim [4]. *Supra* §VI.B.3, Analysis of [1a] (McCormack-Eiji's core 12 (**baseboard**) is made of composite materials of **glass fibers** with **epoxy** resin); APPLE-1003, ¶165.

[5]

McCormack-Eiji renders obvious Claim [5]. The combination's "integrated electronic component"/ "integrated circuit component 20" (**microcircuit**) is **located between** metal layer 94 and metal layer 16 (and 42, 98) (**conductive patterns**) **on both sides of the insulating material layer** composed of the core 12 (**baseboard**) and the dielectric layer over core 12. *Supra*, §§VI.A.2, Analyses of [12pre]-[12c], §§VI.B.3, Analyses of [1pre]-[1c]; APPLE-1003, ¶166.



APPLE-1003, ¶166 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

[6]

As discussed above, McCormack-Eiji's integrated circuit component 20 (*microcircuit*) is disposed in cavity 24 (*in the hole*). *Supra*, §VI.A.2, Analysis of [12c]. Further, McCormack teaches "a suitable adhesive" and "[a]dditional underfill, glop-top, or other adhesive/sealant materials" for securing the integrated circuit components "to a desired location," and various "filler material" for filling metal-lined openings and vias in its insulating layers. APPLE-1005, [0029]-[0030], [0031], [0032], [0033]; APPLE-1003, ¶167. A POSITA would have recognized and found obvious that the same type of adhesive, underfill, glop-top, or other adhesive/sealant materials, and/or other filler material such as epoxy resins, is used to fill any gap in cavity 24 between the EMI shield and the component and secure the component in a desirable location (*secured in place*) in the cavity (*in the hole with a filler material in the hole*). *E.g.*, APPLE-1005, [0006]; APPLE-1003, ¶168. A POSITA would have been further prompted to implement the combination in this manner in view of Eiji's teaching of a "resin 16, which is primarily epoxy resin," to secure each component at "a predetermined location in the through-hole." APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1, 3; APPLE-1003, ¶169-170.

[7]

Supra, §VI.B.3, Analysis of Claim 6 (both McCormack's "filler materials" and Eiji's "resin 16" contain *epoxy* resin). APPLE-1003, ¶171.

[8pre]

Supra, §VI.B.3, Analysis of Claim [1]. APPLE-1003, ¶172.

[8a]

McCormack-Eiji renders [8a] obvious. *Supra*, §VI.A.2, Analysis of Claim [14]; APPLE-1003, ¶173.

Additionally, a POSITA would have been prompted to embed multiple electronic components in the same substrate, in accordance with Eiji's suggestions, to provide enhanced functionality and high-density mounting. *See e.g.*, APPLE-1012, Abstract, [0006], FIGS. 1-7; APPLE-1003, ¶173.

[8b]

McCormack-Eiji renders [8b] obvious. APPLE-1003, ¶174. For example, when several integrated circuit components (*microcircuits*) are provided in the same substrate of the combined system, these integrated circuit components are connected to each other through metal 72 in openings 70 (*conductors in the contact opening*) for connecting to both the pads 26 on the first surface of each integrated circuit component and metal layer 94 (*at least one of the conductive patterns*). *Supra*, §§VI.B.3, Analyses of [1e], [8a], §VI.A.2, Analysis of [12d]; APPLE-1003, ¶174.

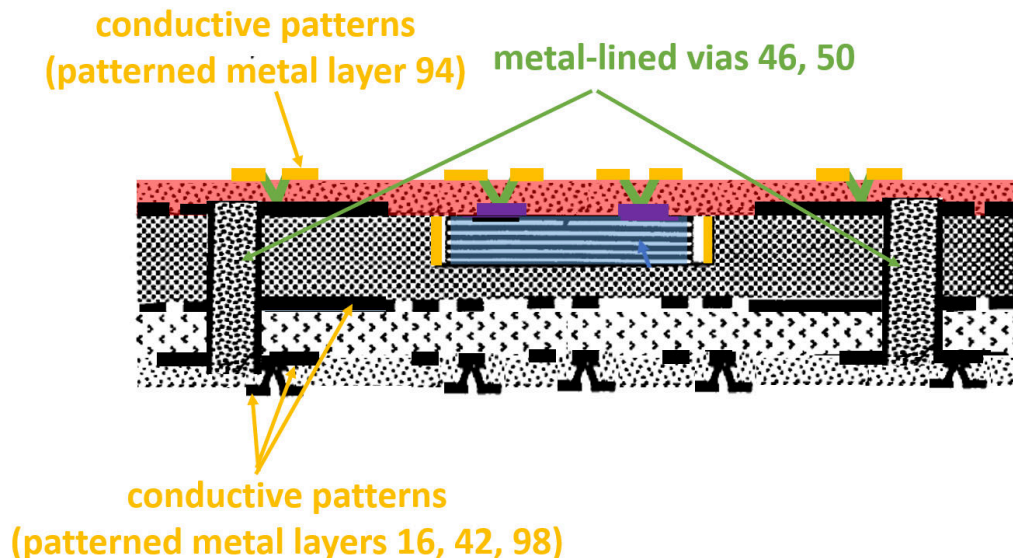
[9]

McCormack-Eiji renders Claim [9] obvious. As discussed above, metal 72 made of copper formed in openings 70 (*copper in the contact openings*) is formed by a “combination of e-less and electrolytic plating,” which provides *a first layer of chemically deposited copper* (through e-less plating) *and a second layer of electrochemically deposited copper* (through electrolytic plating) *on the first layer of chemically deposited copper*. *Supra*, §VI.B.3, Analysis of [1e] and §VI.A.2, Analysis of [12d], [24]; APPLE-1003, ¶175. Additionally, a POSITA would have further implemented the combination in this manner, based on Eiji’s express teaching of “electroless copper plating and electrolytic copper plating” that are “performed on the inner surfaces of” through-holes in an insulating substrate. APPLE-1012, [0017]; *supra*, §VI.B.3, Analysis of [1e]; APPLE-1003, ¶176.

[10]

For example, McCormack discloses *electrically conducting feed-throughs* including “metal-lined vias 46 and 50 formed by drilling openings through the entire FIG. 5 circuit board assembly,” that provide electrical connection *between the conductive patterns on the both sides of the insulating material layer* (e.g., patterned metal layer 94 on the upper side and patterned metal layer 16, 42, or 98 on the lower side). APPLE-1005, [0031]. A POSITA would have found obvious that when a single dielectric layer is used above core 12, the openings pass through

dielectric layer 32 and the core 12, and through residual metal layers remaining from patterned metal layers 14 and 16 *Id.*, [0031] (“The opening for vias 46 and 50 are metal-lined (e.g., copper lined) with metal liners 46a and 50a by any suitable process, such as by e-less plating in combination with electrolytic plating, well known to those skilled in the art. Metal liners 46a and 50a are preferably respectively formed such as to be in electrical contact with residual metal layers remaining from patterned metal layers 14 and 16...”); *see also id.*, [0009], [0018]-[0019], [0020]-[0022], [0026], FIGS. 6-10. Moreover, a POSITA would have found obvious that when a single dielectric layer above the core is used, metal layer 94 is coupled to residual metal layers 14, by and through metal liners 78 in openings 76. *Id.*, [0032] (metal layer 98 is also coupled to metal layer 42 by and through metal liners 82 in openings 80), FIG. 9. APPLE-1003, ¶¶177-180.



APPLE-1003, ¶180 (Composite Based on APPLE-1005, FIGS. 9 & 12)

(Annotated))

[11pre]-[11b]

McCormack-Eiji renders [11pre]-[11b] obvious. *Supra*, §§VI.B.3, Analyses of [8pre]-[8b]; APPLE-1003, ¶181.

[12]-[21], [23]-[27]

McCormack-Eiji renders these claims obvious for at least the same reasons set forth above. *Supra*, §§VI.A.2, [12]-[21], [23]-[27]; §VI.B.3, Analysis of [1e] (reciting similar features relating to chemically and/or electrochemically deposited copper as [12d], [17d], [19d], [20d], [24], [27d]); APPLE-1003, ¶182.

[12a]

McCormack-Eiji provides a baseboard made of a glass fiber epoxy—the same material construction recited by the '909 patent, and thus renders obvious [12a]. *Supra*, §VI.B.3, Analysis of [1a], Claim [4]; APPLE-1003, ¶183.

[22]

McCormack-Eiji renders obvious Claim [22]. *Supra*, §VI.B.3, Analysis of [1a], Claim [4], VI.A.2, Analysis of Claim [20]; APPLE-1003, ¶184.

[25]

McCormack-Eiji additionally renders obvious Claim [25] based on Eiji's further teachings for forming thick metal layers (e.g., 26, 27) above and below embedded electronic components in an insulating substrate through **lamination** of

a metal foil and **plating** on top, e.g., by electroless and electrolytic copper plating over “copper foil 5, 6 that is several 10 μm thick.” APPLE-1012, [0017], [0013], [0021]-[0022], FIG. 2(A). Although not required by the ’909 patent’s claims, Eiji also teaches connecting these wiring layers above and below the components to each other and to the shielding layer on the sidewalls of the hole for incorporating the components, all connected to a ground connection, to provide enhanced EMI shielding. APPLE-1012, Abstract, [0007]-[0008], [0010]-[0011], [0013]-[0014], [0021], [0023]-[0028], [0034]-[0036], Cls. 3, 4, 5, FIGS. 1, 4. APPLE-1003, ¶185.

Notably, McCormack and Eiji combined provide at least as much detail as the ’909 patent, which tersely recites a “metal plate” and “metal foil” without extensive construction details, and separately describes materials like that described by McCormack, such as “a layer of copper” made of “an RCC (Resin Coated Copper) foil” and “metal foil” through lamination, for forming its metal plates. APPLE-1001, 5:47-56, 8:44-9:41, 4:40-59; FIGS. 1J & 1F; *supra*, §VI.A.2, Analysis of Claim [25]; APPLE-1003, ¶186; *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994) (“[T]hat appellant did not provide the type of detail in his specification that he now argues is necessary in prior art references supports the Board’s finding that one skilled in the art would have known how to implement the features of the references.”).

To the extent the ’909 patent’s description of forming a metal plate in

connection with the making of the circuit board's conductive pattern requires growing a thicker metal film from its "metal coating 12" and/or "metal coating 8," McCormack-Eiji discloses it. APPLE-1001, FIGS. 1F, 1J, 4C, 4D, 4:40-63, 5:47-6:4, 8:44-9:41; APPLE-1003, ¶187. For example, McCormack-Eiji's conductive metal layers implemented in accordance with Eiji have a substantial thickness more than "several 10 μm thick," compared with the '909 patent's metal coating of "e.g., c. 5 μm ." APPLE-1012, [0017], [0021]-[0022]; APPLE-1003, ¶187.

[26]-[27]

McCormack-Eiji additionally renders obvious claims [26]-[27] based on Eiji's further teachings. For example, at least one of McCormack-Eiji's metal layers 16, 42 and 98 below integrated circuit component 20 (*below at least one of the microcircuits*), e.g., formed in accordance with Eiji (e.g., "copper foil" that is more than "several 10 μm thick") is *a metal foil*. *Supra*, §VI.B.3, Analysis of Claim [25]; APPLE-1003, ¶188.

[28]

Supra, §VI.B.3, Analysis of [1d] (McCormack-Eiji's shield layer on the sidewalls of cavity 24 in core 12 (*sidewalls of the hole in the baseboard*) is "composed of a copper plating film" (*covered by a metal foil as the conductive material*)); APPLE-1003, ¶189.

[29]

The McCormack-Eiji device has a metal foil covering all sidewalls to provide EMI protection around the semiconductor component. *Supra*, §VI.B.3, Analysis of [1d], [28]. As the component is surrounded by unbroken four sidewalls of the opening in lateral directions, a POSITA would have been prompted to cover all four sidewalls, providing an unbroken metal foil that surrounds the microcircuit in a lateral direction of the circuit board, and effectuating and enhancing the shielding objective of the metal foil. APPLE-1003, ¶190.

[30]-[32]

Supra, §§VI.B.3, Analyses of Claims [1], [25], §VI.A.2, [25] (the unpatterned portions of at least one of metal layers (e.g., metal layer 94) above integrated circuit component 20, and unpatterned portions of at least one of metal layers (e.g., metal layer 16, 42 or 98) below integrated circuit component 20, each provide a *metal plate*); APPLE-1003, ¶191.

[33]

Supra, §§VI.A.2, Analyses of Claims [25], VI.B.3, [25], [28]; APPLE-1003, ¶192.

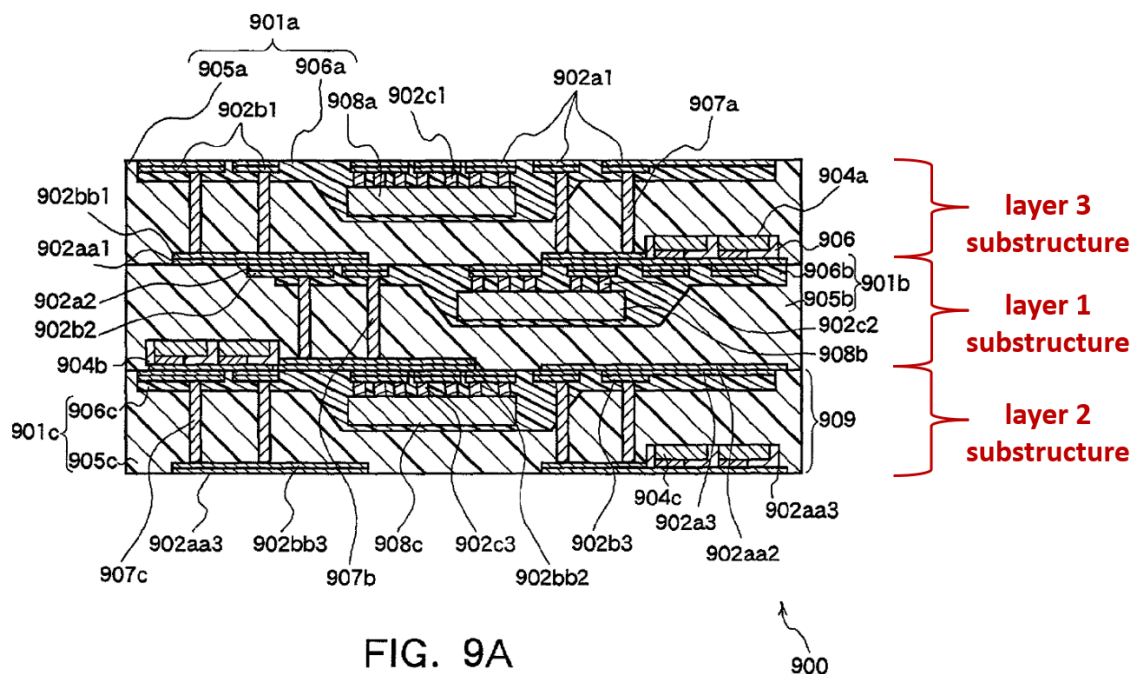
C. GROUND 1C – McCormack, Eiji and Sugaya render obvious Claims 12-27

Sugaya provides further express teachings of multi-layered circuit boards, further informing the “multi-layered” elements of independent claim 12 and its

dependent claims. APPLE-1003, ¶193. Thus, Ground 1C provides an additional manner in which the prior art renders obvious claims 12-27. *Id.*

1. Sugaya

Sugaya describes a “circuit component built-in module” with embedded circuit components such as semiconductor chips. APPLE-1007, Title, Abstract, FIG. 1A, [0013], [0015], [0020]-[0021], [0086], [0092]. Sugaya further describes stacking up multiple layers of similar modules to form a multi-layered structure, where “any number of layers [of similar configuration] can be formed depending on the design.” APPLE-1007, [0225]; *see also*, [0004], [0217], [0226]-[0229], [0351], [0354], FIGS. 9A (reproduced below showing a three-layered structure), 9B; APPLE-1003, ¶83-84.



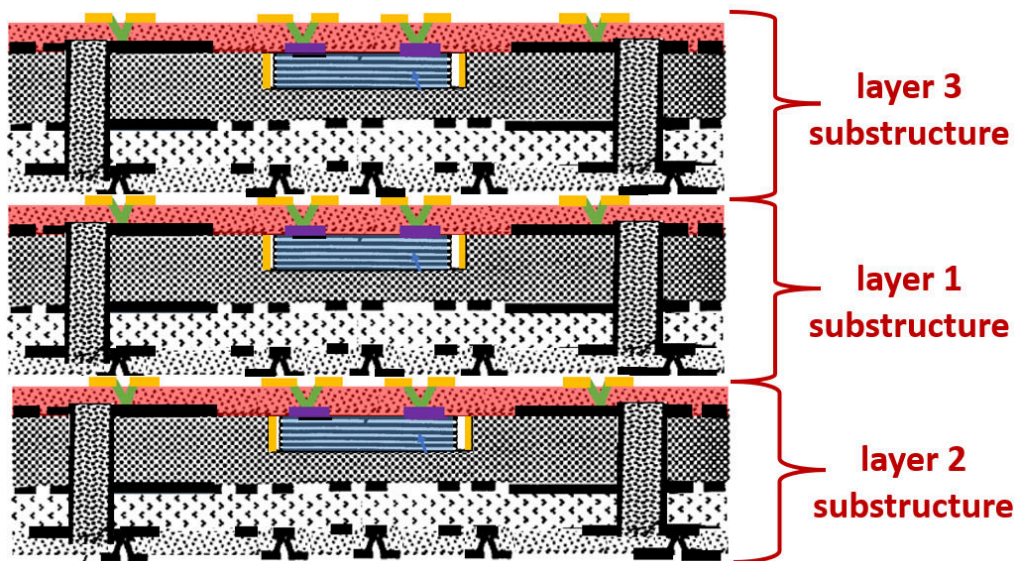
APPLE-1003, ¶84 (APPLE-1007, FIG. 9A (Annotated))

2. Predictable Combination of McCormack, Eiji and Sugaya

A POSITA would have been motivated to combine the teachings of McCormack, Eiji and Sugaya to provide a high-density, multi-layered structure with EMI shielding effect. APPLE-1003, ¶194. Each relates to a component built-in module where circuit components are provided inside an insulating substrate, thus relating to the same field of endeavor and directed to analogous subject matter. *See e.g.*, APPLE-1005, Abstract, [0002], [0029]-[0030]; APPLE-1012, [0023], FIGS. 1, 4; APPLE-1007, Title, Abstract. Sugaya expressly describes stacking up any number of layers of similar configuration to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1007, Abstract, [0004] (“high density, high performance and short-distance wiring of a circuit component have been desired increasingly.”), [0225], [0217], [0351], [0354], FIGS. 9A, 9B; APPLE-1003, ¶194.

A POSITA would have been motivated to utilize an EMI shield feature in accordance with Eiji in a cavity in the core substrate described by McCormack, and to stack up any number of layers of similar configuration, depending on the design, to form a multi-layered structure in accordance with Sugaya’s express suggestions, to achieve high density mounting and EMI shielding. APPLE-1003,

¶195; *supra*, §VI.C.2 (McCormack-Eiji combination). The resulting combination includes a three-layered structure, for example, with each substructure having an integrated circuit component embedded in a cavity of a core substrate, each cavity having EMI shield on its sidewalls. Adjacent layer substructures are electrically connected to each other to form a multi-layered functioning totality, in accordance with Sugaya's suggestions. APPLE-1007, FIG. 9A, [0224]-[0229]; APPLE-1003, ¶195.



APPLE-1003, ¶195 (Composite Based on APPLE-1005, FIGS. 9 & 12
(Annotated))

Additionally, Sugaya provides express description of “LSI, or the like” as examples for the components of its component built-in module. APPLE1007, [0092] (“a semiconductor device such as a transistor, an IC, an LSI, or the like, can

be used”). The McCormack-Eiji-Sugaya combination also includes “LSI” (large-scale integration), which were typically used in components like microprocessors, where a single chip contains both processing logic and on-chip memory. APPLE-1003, ¶196.

A POSITA would have had a reasonable expectation of success in making the proposed modifications given that McCormack, Eiji and Sugaya describe similar circuit component built-in modules, and because the modifications involve only implementation of well-known technologies. APPLE-1003, ¶197.

3. Application to Challenged Claims

[12]-[27]

McCormack-Eiji-Sugaya renders obvious claims 12-27 for the reasons described above in Ground 1A and Ground 1B. But even if McCormack-Eiji did not, the predictable McCormack-Eiji-Sugaya combination would do so.⁶ In accordance with Sugaya’s suggestions of a multi-layered structure, the McCormack-Eiji-Sugaya combination includes a stack-up multi-layered structure, shown in the composite figure above, for example, in which each of the layer 1-3

⁶ Where Sugaya is not addressed in Ground 1C, the Ground 1A and Ground 1B analysis applies fully here in Ground 1C.

substructures have similar configuration/construction. APPLE-1003, ¶199; *supra*, §VI.C.2 (McCormack-Eiji-Sugaya combination); §VI.A.3, Analysis of [12]-[27]. The structures of the McCormack-Eiji-Sugaya thus disclose each element of [12]-[27] in the same manner as set forth in Grounds 1A and 1B, with Sugaya further informing and motivating the multi-layered structure and construction. *Id.*

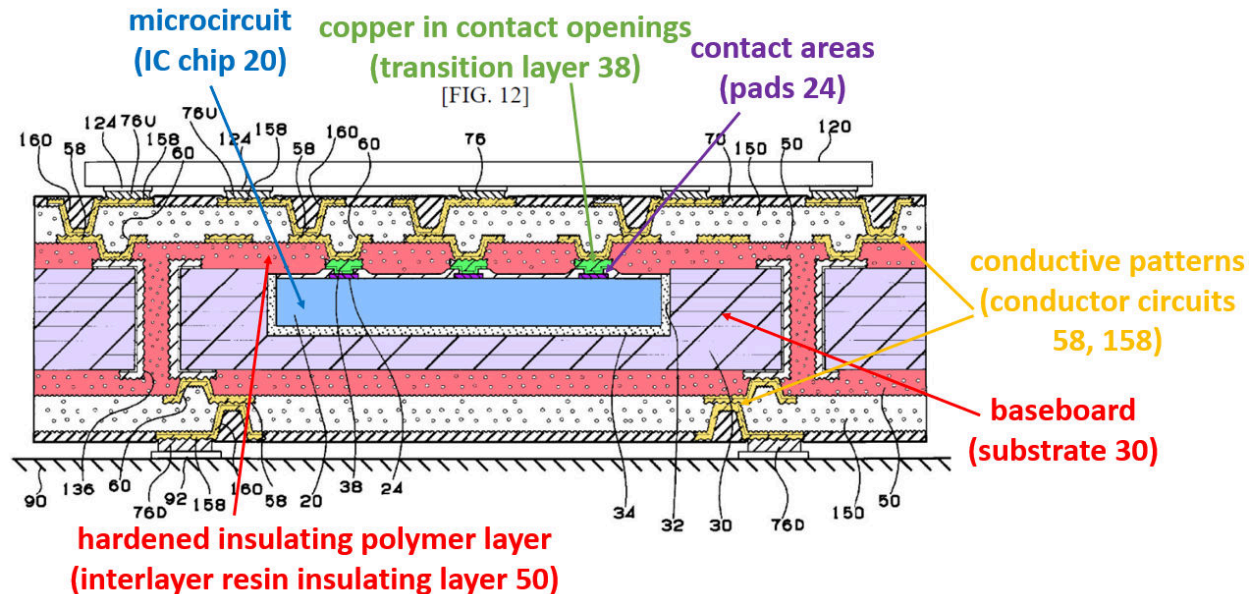
Additionally for Claim [15], McCormack-Eiji-Sugaya provides at least one memory circuit, in accordance with Sugaya's teaching regarding "LSI," a known circuit type that includes a memory circuit. *Supra*, §VI.C.1 (Sugaya). APPLE-1003, ¶200.

D. GROUND 2A – Sakamoto renders obvious claims 12-27

1. Sakamoto

Sakamoto describes "a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip." APPLE-1004, [0001]; *see also*, Abstract ("an IC chip 20 pre-embedded in a core substrate 30"), [0005], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. An "interlayer resin insulating layer 50" provided over the IC chip 20 and on a surface of substrate 30 contains polymer and is cured with the application of heat and pressure. *Id.*, [0030], [0042], [0047], [0057]-[0060]; APPLE-1003, ¶73-75. "Conductor circuit 58" is formed on the top surface of the interlayer resin insulating layer 50 and the inner wall surface of openings for via holes 60, which

are formed through the interlayer resin insulating layer for connecting the electronic components and the conductive circuits. APPLE-1004, [0017], [0036]; APPLE-1003, ¶76. Sakamoto further describes that “a transition layer 38” made of copper is provided on a die pad 24 of the IC chip 20, to connect to via 60 in the interlayer resin insulating layer 50. *Id.*, Abstract, [0018], [0020], [0028], [0031], [0067], [0069]; APPLE-1003, ¶77.



APPLE-1003, ¶77 (APPLE-1004, FIG. 12 (Annotated))

2. Application to Challenged Claims

[12pre]

If the preamble is deemed limiting, Sakamoto discloses it. APPLE-1003, ¶¶202-213. For example, Sakamoto describes “a multilayer printed wiring substrate” comprising a “core substrate 30” in which IC chips (e.g., “IC chip 20”)

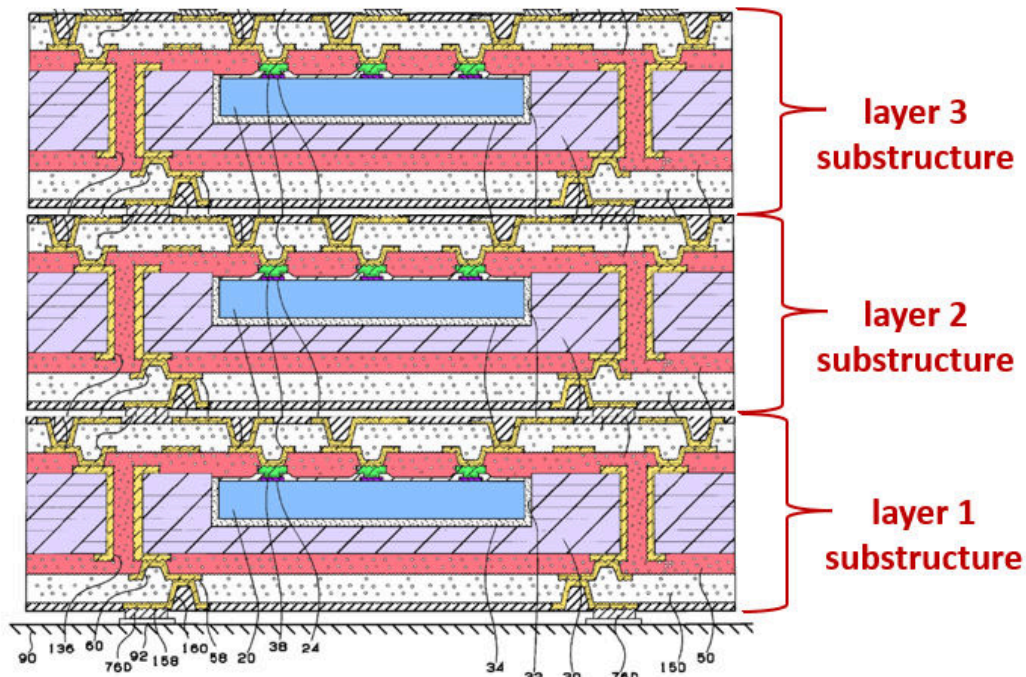
and other “electronic components” are embedded. APPLE-1004, Title, Abstract, [Claim 1], [0001], [0005]-[0007], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. Substrate 30 is made of “any material generally used in printed wiring substrates,” such as “epoxy resins, BT resins, and phenol resins impregnating a reinforcing material such as **glass epoxy** resin or a core material, or a pre-preg laminate impregnated with an epoxy resin .” *Id.*, [0012], [0020], [0023]; APPLE-1003, ¶¶202-203. Sakamoto’s disclosure of suitable material for substrate 30 is thus just like the ’909 patent’s description for its “baseboard 1 [] selected for the circuit-board manufacturing process,” such as “a glass-fibre reinforced epoxy board.” APPLE-1001, 3:46-55, Cl. 9, APPLE-1003, ¶204.

Sakamoto renders obvious a “multi-layered circuit board, which includes at least two circuit board substructures on top of each other.” APPLE-1003, ¶¶205-211. Moreover, stacking multiple layers of circuit-board substructures on top of each other and mounting a plurality of electronic components in the same as well as different such layers to achieve high-density, improved performance, and short-distance wiring was common practice and well known in the field, and amounts to a mere duplication of parts. APPLE-1003, ¶¶205-211. *Supra*, §VI.A.2 (McCormack ground), Analysis of [12pre].

A POSITA would have understood and found obvious that a plurality of Sakamoto’s wiring substrates (including two, three, or more) are beneficially

stacked on top of each other, with the layers of these substructures mechanically and electrically connected to each other, through vias (e.g., vias 60, 160) and through holes (e.g., through-holes 136) within each layer and the connection mechanisms between substrates, all of which Sakamoto already teaches, to achieve “higher functionality” while efficiently manufacturing the multi-layer structure, and other benefits articulated above. APPLE-1003, ¶212; *infra*, §VI.D.2, Analysis of Claim [13].

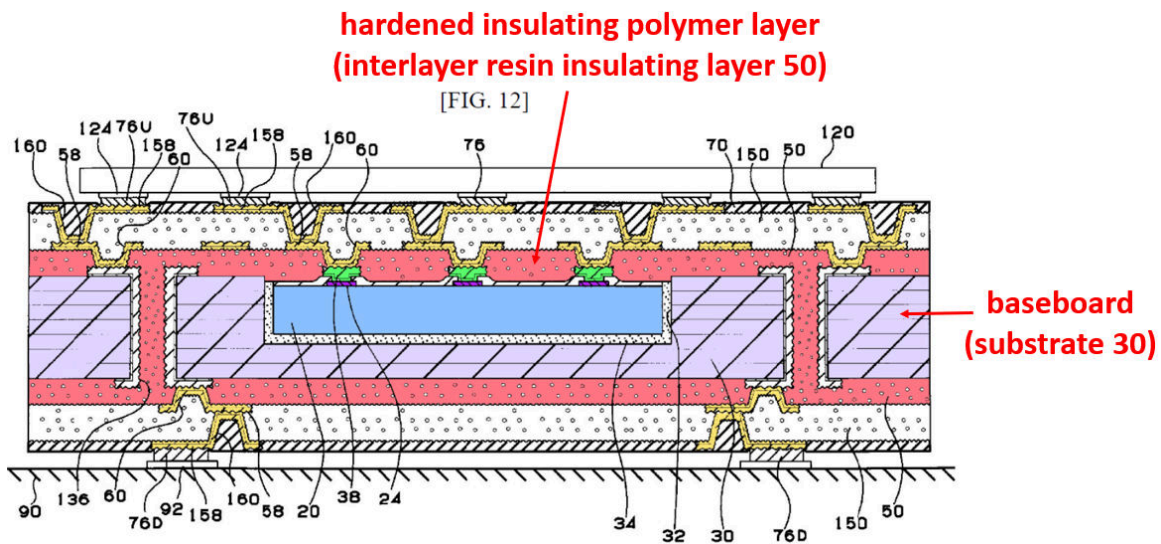
This multi-layered configuration would have been implemented, including electrically connecting the respective substructures to provide a multi-layered functioning totality, using techniques already disclosed in Sakamoto for connecting to “external substrates” such as “motherboards and daughterboards,” including the use of “BGA, Solder bumps, and PGA (conductive connection pins),” among other common and routine mounting methods for high-density circuitry semiconductor devices. APPLE-1004, [0011], [0069], [0070]; APPLE-1003, ¶213. In accordance with Sakamoto’s suggestions, the multi-layered structure includes three similar substructure layers (*at least two circuit board substructures on top of each other*).



APPLE-1003, ¶213 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[12a]

Sakamoto discloses Element [12a]. APPLE-1003, ¶¶214-217. For example, Sakamoto's "substrate 30" made of insulating material and "interlayer resin insulating layer 50" together provide an *insulating material layer*. APPLE-1004, [0001], [0003], [0011], [0053], [0056]-[0057], [0078], FIG. 12; APPLE-1003, ¶214.



APPLE-1003, ¶214 (APPLE-1004, FIG. 12 (Annotated))

To be clear, Sakamoto’s lower interlayer resin insulating layer 150 on the interlayer resin insulating layer 50, together with “substrate 30” and upper “interlayer resin insulating layer 50” likewise provide an *insulating material layer*, and thus Sakamoto discloses [1a] in this second manner. APPLE-1003, ¶215.

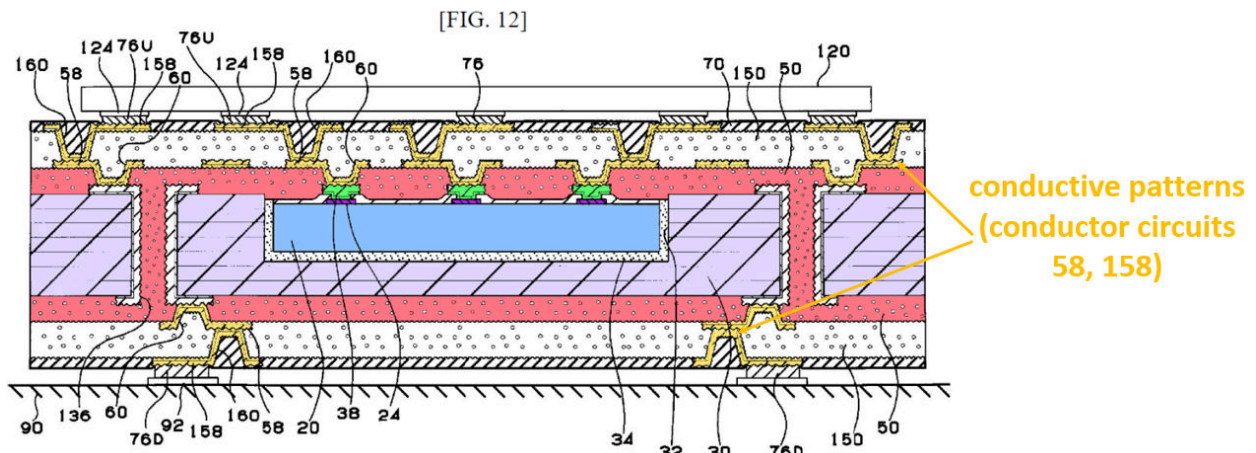
Sakamoto’s “substrate 30” provides a *baseboard* as claimed. *Supra*, §VI.D.2, Analysis of [12pre]. Further, a POSITA would have understood and found obvious that Sakamoto’s interlayer resin insulating layer 50 is a *hardened insulating polymer layer*. APPLE-1003, ¶216; APPLE-1004, [0017], [0030], [0042]-[0043]. For example, Sakamoto describes various resins used for the interlayer resin insulating layer 50, which a POSITA would have recognized as *polymers*. APPLE-1003, ¶216; APPLE-1004, [0030], [0042] (“an **epoxy resin** can be used”), [0047], [0053]-[0060]. Additionally, a POSITA would have understood

and found obvious that interlayer resin insulating layers 50 and 150 are **hardened** through chemical and thermal curing. APPLE-1004, [0042] (“This epoxy resin [of the interlayer resin insulating layers] contains ... a curing agent...”), [0053] (“various heat treatments”), [0054] (“heat cycle conditions”), [0058] (examples of “curing agents”), [0059] (“curing of the resin film” of the interlayer resin insulating layers); APPLE-1003, ¶217.

[12b]

Sakamoto renders obvious [12b]. APPLE-1003, ¶¶218-219. For example, Sakamoto describes a “conductor circuit 58” that is “formed in an interlayer resin insulating layer 50,” and a “conductor circuit 158” that is “formed in interlayer resin insulating layer 150.” APPLE-1004, [0017]; *see also id.*, [0005]-[0007], [0012], [0015], [0027]-[0028], [0032]-[0037] (describing the formation of the conductor circuits made of an electroless plated film and an electrolytic plated film), [0062], FIGS. 4- 6, 9-12; APPLE-1003, ¶¶218-219.

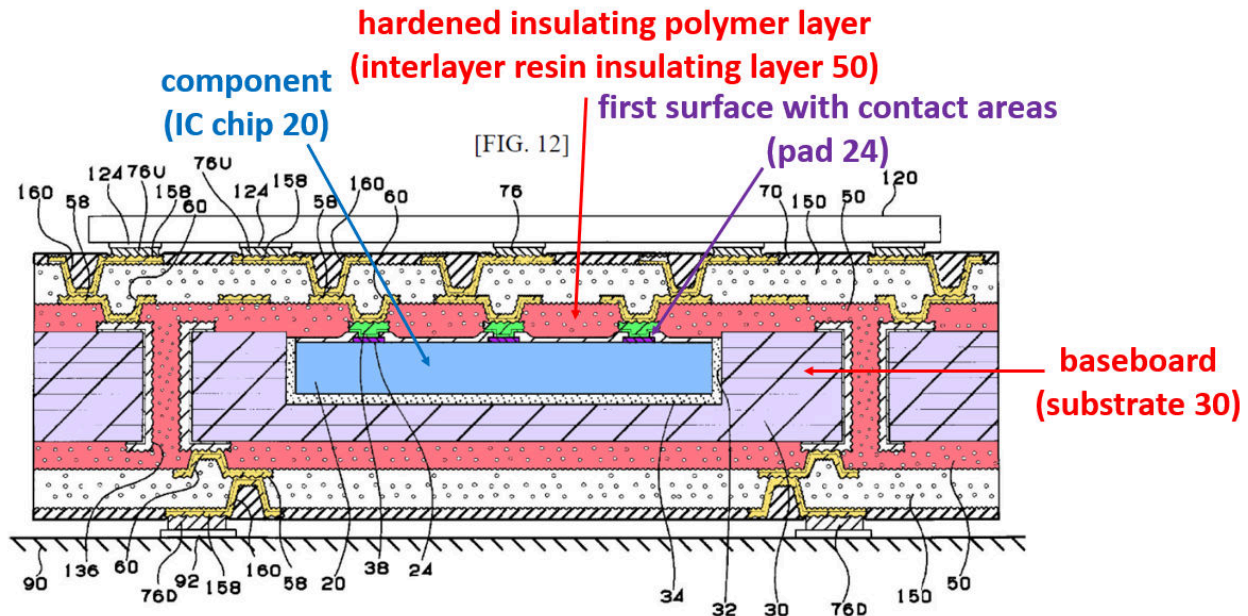
The conductor circuit layers 58 and 158 arranged on both sides of the wiring board (***on both sides of the insulating material layer***) are patterned through photoetching or laser and provide ***conductive patterns*** as claimed. APPLE-1003, ¶219.



APPLE-1003, ¶219 (APPLE-1004, FIG. 12 (Annotated))

[12c]

Sakamoto renders obvious Element [12c]. APPLE-1003, ¶¶220-222. For example, Sakamoto describes “an electronic component such as an IC chip” (e.g., “IC chip 20”) (*at least one microcircuit*) *embedded* in an opening, through-hole, or counterbore in a resin insulating substrate (e.g., in substrate 30 as part of *the insulating material layer*). *Supra*, §VI.D.2, Analyses of [12pre]-[12a]; §VI.A.2, Analysis of [12c] (IC chips are microcircuits); APPLE-1003, ¶220.



APPLE-1003, ¶220 (APPLE-1004, FIG. 12 (Annotated))

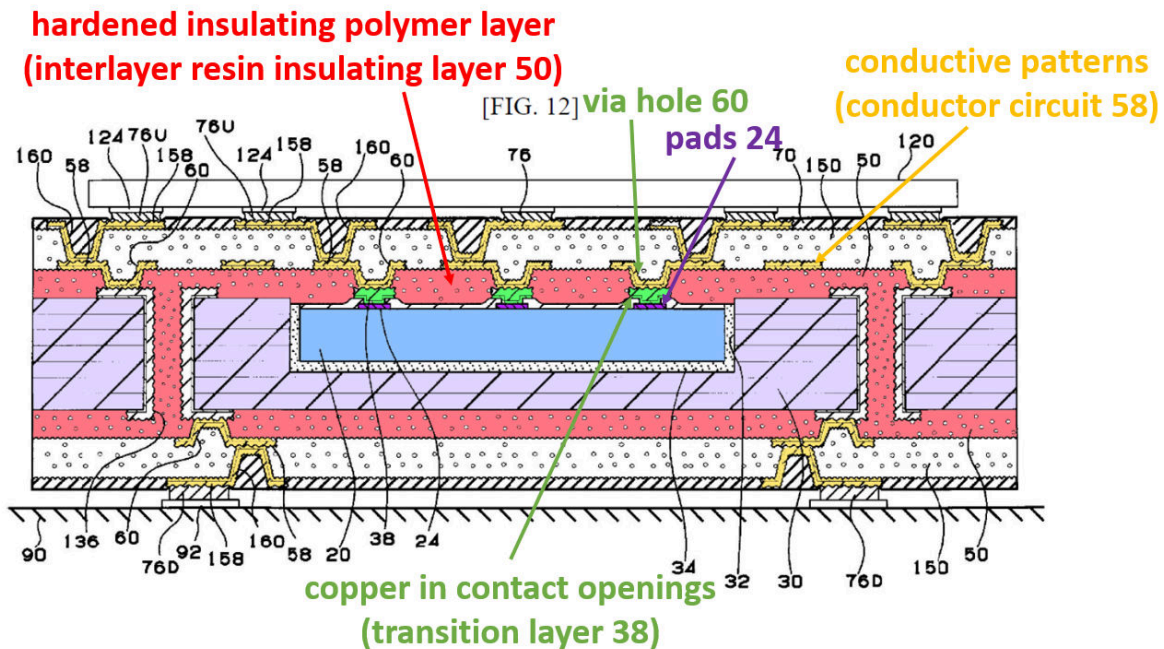
Sakamoto further describes that IC chip 20 has “die pads 24” (*contact areas*) on a surface (*first surface*). APPLE-1004, Abstract, [0018], FIG. 12; APPLE-1003, ¶221.

A POSITA would have found it obvious to omit the IC “protective film (passivation + polyimide) 22” that covers the active surface of the IC chip 20 and has openings for the die pads 24. APPLE-1004, [0018], FIG.12. Based on Sakamoto’s description, a POSITA would have recognized that the manufacturing process of the IC chip 20 and the module would have been advantageously simplified by omitting this protective film by reducing the number of manufacturing steps and material components. APPLE-1003, ¶222. Indeed, a POSITA would have recognized that an additional protective film made of

passivation and polyimide layer is not required, especially given that the interlayer resin insulating layer 50 grown on top of the first surface of the IC chip provides protection that a protective film provides. APPLE-1003, ¶222. In the resulting device, the interlayer resin insulating layer 50 is *against* the first surface of IC chip 20 (without including protective film 22). APPLE-1003, ¶222.

[12d]

Sakamoto discloses Element [12d]. APPLE-1003, ¶¶223-230. For example, Sakamoto describes that “vias are formed in the interlayer insulating layers, and electrical connections are established through the vias” (*contact openings in the hardened insulating polymer layer*). APPLE-1004, [Claim 1], [Claim 4]. For example, “via holes 60” are formed in the interlayer resin insulating layers 50 and connected with die pads 24 of the IC chip either directly or through “transition layer 38” (also in the interlayer resin insulating layer 50 and defining an extended opening of the vias). APPLE-1004, Abstract, [0005]-[0007] (“providing vias on the IC chip pads using photoetching or a laser to form a conductor circuit that is a conductor layer”), [0008] (“via holes in interlayer resin insulating layers”), [0067] (“in the third embodiment, the vias 60 are connected directly to the pads 24 without providing a transition layer”), FIGS. 3-6, 9-12; APPLE-1003, ¶223.



APPLE-1003, ¶223 (APPLE-1004, FIG. 12 (Annotated))

Portions of the conductor circuit extending into the via hole and the “transition layer 38” made of copper, individually or collectively, provide *copper in the contact openings for forming electrical contacts between the contact areas of the microcircuit and at least one of the conductive patterns*. APPLE-1003, ¶224. Indeed, portions of conductor circuit (e.g., as shown by Sakamoto’s 58) extend into the via hole 60, and the transition layer 38 is formed on the contact pads 24 (*contact areas*) of the IC chip 20, for “direct connection of an IC chip, which is a semiconductor element, to [conductor circuit 58 of] a printed wiring substrate,” such that “the via can be reliably connected to the die pad, improving reliability.” APPLE-1004, [0008]-[0010]; *see also*, Abstract (“by providing a transition layer 38 on the die pad 24 ... connectivity between and reliability of die

pads 24 and via hole 60 can be improved”), [Claim 4], [0007], [0009]-[0010], [0067], [0071], FIGS. 3-6, 9-12; APPLE-1003, ¶¶224-226. To be clear, these conductors are mechanically and electrically connected with the parts of the conductor circuit 58 outside the via hole 60 and on the top surface of the interlayer resin insulating layer 50, as well as with pads 24 on the IC chip component. APPLE-1003, ¶227.

As noted in §III.A., recitation of “electrochemically deposited” and “chemically deposited” copper is a product-by-process element, and thus not limiting for purpose of invalidity. Sakamoto describes copper, as claimed. That is enough.

To be clear, even if the process recitations were considered limiting, Sakamoto renders [12d] obvious. APPLE-1003, ¶228-230. Sakamoto discloses that transition layer 38 made of copper is composed of at least an “electroless plated film 36” (*chemically deposited copper*) and an “electrolytic plated film 37” (*electrochemically deposited copper*), providing a first layer of chemically deposited copper (electroless plating) and a second layer of electrochemically deposited copper (electrolytic plated) on the first layer of chemically deposited copper. APPLE-1004, [0028]; *see also*, Abstract, [Claim 4], [0007], [0008] (“The transition layer is formed of two or more metal layers”), [0009], [0010], [0014] (“the transition layer can be thickened by **electroplating**”), [0015] (“When the

transition layer is formed by a subtractive process, the metal film is thickened by **electroless or electrolytic plating**. Types of plating that can be formed include copper, nickel, gold, silver, zinc, and iron. **Copper is preferably used**”), [0018], [0020]-[0021], [0027] (“Plated film 36 may be formed on the metal film 33 by **electroless plating** (FIG. 2(B))... **Copper is preferably used...**”), [0028] (“**electrolytic plated film [37] on the electroless plated film 36**”), [0031] (“transition layer 38 made of **copper**”), [0035], [0067], [0069], [0070], [0071], FIG. 2; APPLE-1003, ¶¶228-229.

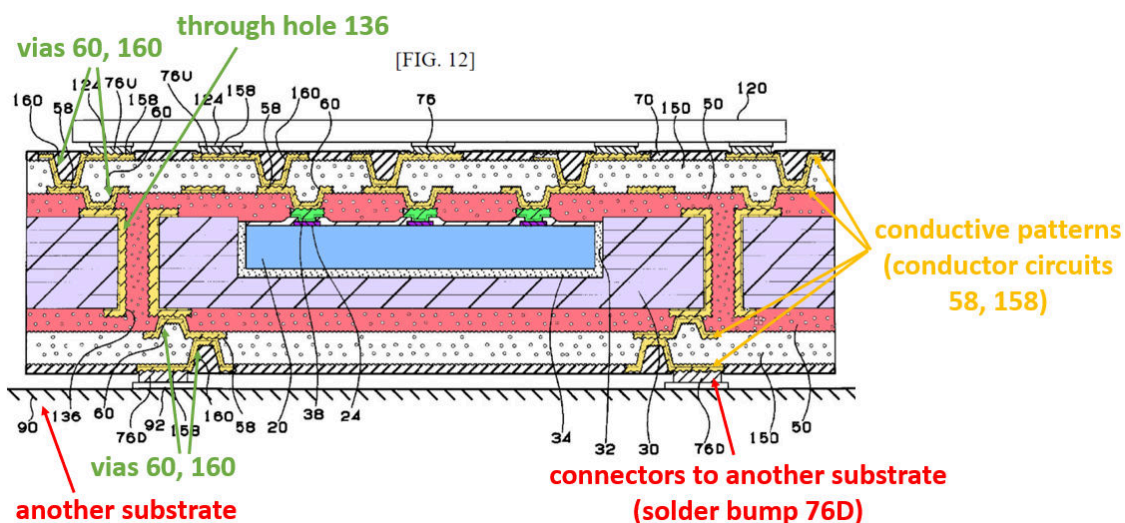
To be clear, conductor circuit 58 extending into vias 60 in direct contact with die pads 24 (e.g., where a transition layer 38 is not used) is also formed of an electroless plated film 52 and an electrolytic plated film 56 using copper. APPLE-1004, [0032]-[0037], FIG. 4; *supra*, §VI.D.4, analysis of [12b]; APPLE-1003, ¶230.

[13]

Sakamoto renders obvious Claim [13]. APPLE-1003, ¶¶231-233. As discussed above, substructure layers of Sakamoto’s multi-layered circuit board system are mechanically and electrically connected to each other, through the vias (e.g., vias 60, 160) and through-holes (e.g., through-holes 136) within each layer, as well as the connection mechanisms between substrates to form a multi-layered functioning totality. *Supra*, §VI.D.2, Analysis of [12pre]. For example, each

circuit board substructure's conductive patterns (e.g., conductor circuits 58 and 158 on both sides of the wiring board) are electrically connected to each other, through vias 60, 160, and through-holes 136, which are metal-lined holes through substrate 30 and in electrical connection with conductor circuits 58 and 158 through the vias. *E.g.*, APPLE-1004, [0069], FIG. 12; APPLE-1003, ¶¶231-232.

Sakamoto also describes mechanisms for connecting one wiring substrate to another wiring substrate (e.g., “external substrates” such as “motherboards and daughterboards”), including the use of “BGA, Solder bumps, and PGA (conductive connection pins),” among other common and routine mounting methods for high-density circuitry semiconductor devices. APPLE-1004, [0011], [0069], [0070], FIGS. 9-12. Below annotated FIG. 12 shows these connection structures of one substructure. APPLE-1003, ¶233.



APPLE-1003, ¶233 (APPLE-1004, FIG. 12 (Annotated))

[14]

Sakamoto renders obvious Claim [14]. APPLE-1003, ¶¶234-236. For example, a POSITA would have understood from Sakamoto's text that Sakamoto explicitly teaches, or at least contemplates and suggests, repeatedly incorporating at least two "electronic components such as IC chips" (*at least two microcircuits*) some of which having different functions, inside the same resin substrate (*the insulating material layer*). APPLE-1004, [0006] ("electronic components such as IC chips and capacitors with different functions can be mounted, and a multi-layer printed wiring substrate with higher functionality can be obtained"), [0012] ("Resin substrates used to incorporate electronic components such as IC chips used in the present invention..."), [0069], [0070], [0071]; *supra*, §§VI.D.2, Analyses of Claims [12], [13]; APPLE-1003, ¶¶234-236. Moreover, a POSITA would have been motivated to implement the device to have at least two electronic components/IC chips, in order to facilitate higher functionality, high-speed operation and shortened wiring length, among other benefits of a high-density circuitry, in accordance with Sakamoto's teachings. *Id.*

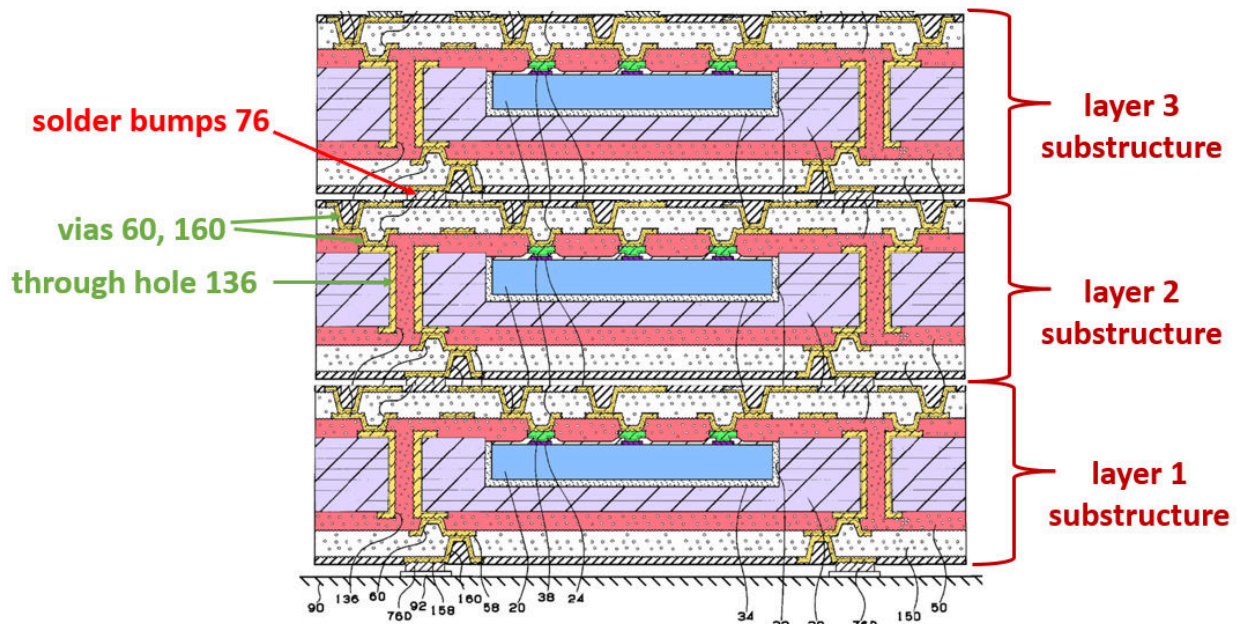
[15]

Sakamoto renders obvious Claim [15]. APPLE-1003, ¶237. For example, Sakamoto expressly discloses "cache memory" as an example, "in a specific example, an IC chip, cache memory, and capacitor can be arranged close to each

other by embedding an IC chip with a calculating function as the built-in IC chip and mounting a cache memory and a capacitor on the surface layer.” APPLE-1004, [0006], [0068] (“a cache memory is the IC chip 120 mounted on the surface”), [0070]. A POSITA would have understood and found obvious that IC chip 120, just like IC chip 20, is beneficially embedded in an insulating material layer of each circuit board substructure, effectuating its functionality in the multi-layer circuit board structure. APPLE-1003, ¶237; *supra*, Analysis of [14].

[16]

Sakamoto renders obvious Claim [16]. APPLE-1003, ¶238. *Supra*, §VI.D.2, Analysis of [12pre]. Sakamoto renders obvious ***three*** similar ***circuit board substructures*** stacked ***on top of each other and electrically connected to each other*** through the vias (e.g., vias 60, 160) and through-holes (e.g., through-holes 136) within each layer, as well as the connection mechanisms (e.g., “BGA, Solder bumps, and PGA (conductive connection pins)”). APPLE-1003, ¶238; *supra*, §VI.D.2, Analysis of Claim [12pre], [13].



APPLE-1003, ¶238 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[17pre]-[17d]

Supra, §§VI.D.2, Analyses of [12pre]-[12d]; APPLE-1003, ¶239.

[18]

Supra, §§VI.D.2, Analyses of Claims [13] and [16]; APPLE-1003, ¶240.

[19pre]-[19d]

Supra, §§VI.D.2, Analyses of [12pre]-[12d] and Claim [18]; APPLE-1003, ¶241.

[20pre]-[20d]

Supra, §§VI.D.2, Analyses of [12pre]-[12d] and Claim [19]; APPLE-1003, ¶242.

[21]

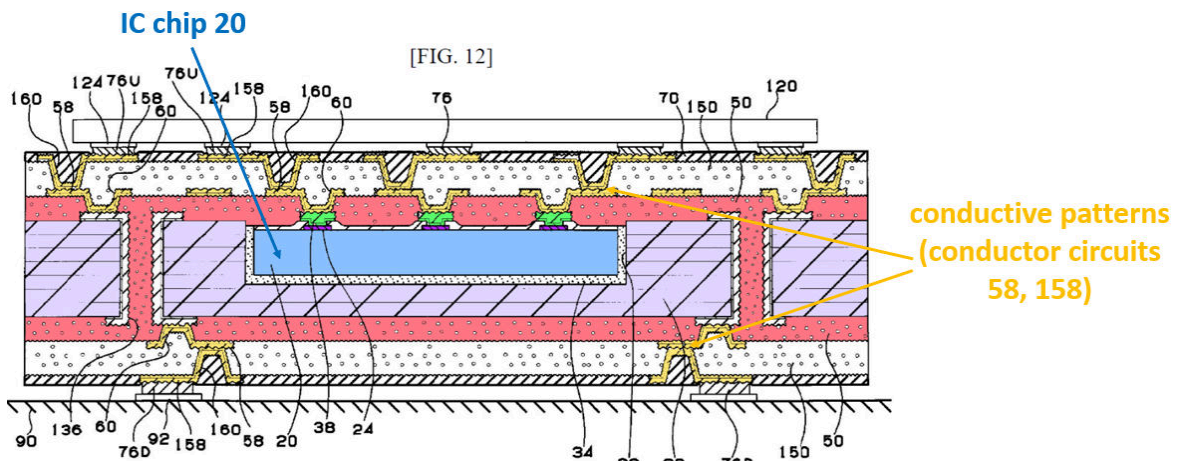
Supra, §VI.D.2, Analysis of [12a] (Sakamoto's interlayer resin insulating layer 50 (***hardened insulating polymer layer***) contains ***epoxy***); APPLE-1003, ¶243.

[22]

As discussed above for [12pre] and [12a], Sakamoto's substrate 30 (***baseboard***) is made of a glass epoxy, such as a glass-fiber reinforced epoxy board. *See also*, APPLE-1004, [0012], [0020], [0023]; APPLE-1003, ¶244. To be clear, a POSITA would have been prompted to utilize **glass fibers** as an obvious alternative for glass cloth as a reinforcing material for the "glass epoxy resin" of Sakamoto's substrate 30, as glass fibers were well-known material commonly used to impregnate with insulating resins of a substrate to increase the strength of the substrate. APPLE-1003, ¶244.

[23]

Supra, §§VI.D.2, Analyses of [12b]-[12c]. In the resulting multi-layer device, IC chip 20 (***at least one microcircuit***) is located ***between*** the conductor circuits 58, 158 (***conductive patterns***) ***on both sides of the insulating material layer***. APPLE-1003, ¶245.



APPLE-1003, ¶245 (APPLE-1004, FIG. 12 (Annotated))

[24]

Portions of Sakamoto's conductor circuit 58 extending into the via hole and the "transition layer 38", individually or collectively, provide the recited *copper in the contact openings contains a first layer of chemically deposited copper and a second layer of electrochemically deposited copper on the first layer of chemically deposited copper*); APPLE-1003, ¶246; *supra*, §VI.D.2, Analysis of [12d].

[25]

As discussed above, Sakamoto describes various methods for forming its conductor layers on the both sides of its wiring substrate, either using "a **double-sided copper-clad laminate**" or an electroless plated film and an electrolytic **plated film** (e.g., "with a thickness of 16 μm "). APPLE-1004, [0012], [0007] ("form a conductive circuit that is a conductive layer"), [0032]-[0033] ("the

substrate is immersed in an electroless plating solution to form an electroless plated **film** 52 on the surface of interlayer resin insulating layer 50”), [0034] (“form an electrolytic plated **film** 56 with a thickness of 18 μm ”), [0035]-[0036] (“This forms a conductor circuit 58 and vias 60 with a thickness of 16 μm made of the electroless plated film 52 and electrolytic plated film 56.”), [0037] (forming conductor circuit 158 using the same method). *Supra*, §VI.D.2, Analysis of [12b]. APPLE-1003, ¶247.

These conductor layers having conductor circuits 58 and 158 and unpatterned portions both *above* and below the integrated circuit component 20 (*at least one of the microcircuits*), and a POSITA would have found it obvious to implement the unpatterned portions of the conductor layers to provide beneficial EMI shielding, providing *a metal plate*. *Supra*, §VI.A.2 (McCormack ground), Analysis of Claim [25] (discussion of similarity to the ’909 patent descriptions of “metal plate,” metal “film,” and “metal foil” (terms used interchangeably in the ’909 patent specification), using “**a layer of copper** (e.g., c. 5 μm)” such as “an RCC (Resin Coated **Copper**) foil” on both sides of the circuit board above and below the embedded electronic component); *see also* APPLE-1001, 9:11-13; APPLE-1003, ¶247.

To the extent the ’909 patent’s description of forming a metal plate in connection with the making of the circuit board’s conductive pattern requires

growing a thicker metal film from its “metal coating 12” and/or “metal coating 8,” Sakamoto satisfies it. APPLE-1001, FIGS. 1F, 1J, 4C, 4D, 4:40-63, 5:47-6:4, 8:44-9:41; APPLE-1003, ¶248. For example, Sakamoto’s conductor layers each have a substantial thickness “of 16 μm ,” compared with the ’909 patent’s metal coating of “e.g., c. 5 μm .” APPLE-1004, [0033]-[0036]; APPLE-1003, ¶248.

[26]

Sakamoto’s conductor layers having conductor circuits 58 and 158 both above and *below* the integrated circuit component 20 (*at least one of the microcircuits*) each provide *a metal foil*. *Supra*, §VI.D.2, Analysis of [12b] and Claim [25]; APPLE-1003, ¶249.

[27pre]-[27d]

Supra, §§VI.D.2, Analyses of [17pre]-[17d]; APPLE-1003, ¶250.

[27e]

Supra, §VI.D.2, Analysis of Claim [26]; APPLE-1003, ¶251.

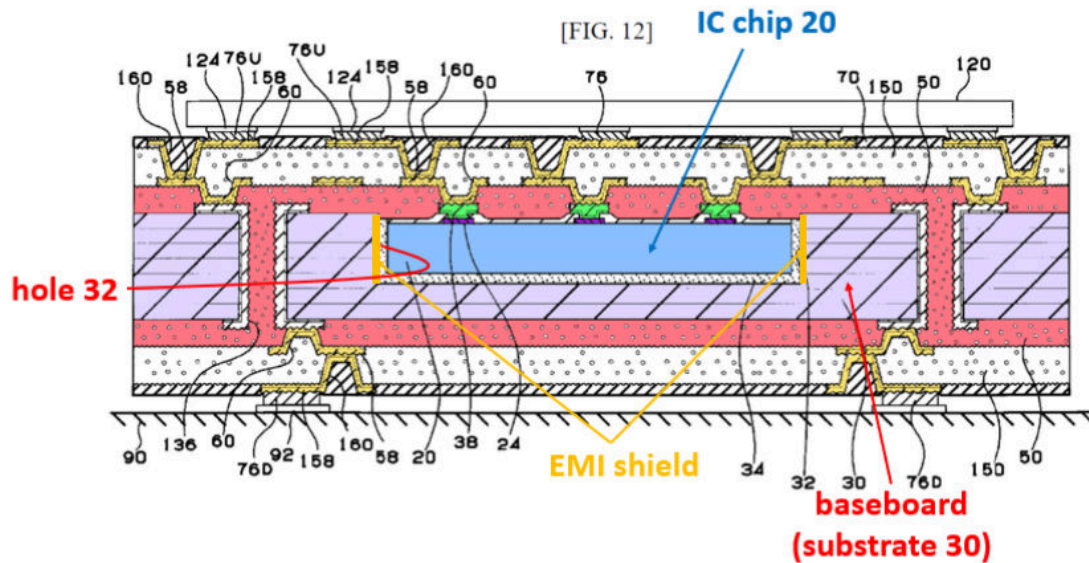
E. GROUND 2B – Sakamoto and Eiji render obvious Claims 1-33

1. Predictable Combination of Sakamoto and Eiji

A POSITA would have been motivated to implement a shield layer on the sidewalls of the hole with the electronic component embedded therein, in accordance with Eiji, in Sakamoto’s multilayer printed wiring board to achieve known benefits. APPLE-1003, ¶253. For example, a POSITA would have done so

based on Eiji's suggestions to make the electronic components built into an insulating substrate "less susceptible to external electromagnetic waves," to "reduce the effects of noise generated by the circuits constituting these electronic components," and/or to "stabilize the electrical characteristics" of the system, consistent with Sakamoto's objectives of higher functionality, high-speed operation and improved reliability. APPLE-1012, [Abstract]; *see also*, [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1004, Abstract, [0006], [0070]-[0071]; APPLE-1003, ¶253.

In the predictable combination, a shielding layer composed of a copper plating film that shields electromagnetic waves (e.g., shielding layer 10) is formed on an inner surface of the recessed portion in the core substrate (e.g., recessed portion 32 in core substrate 30), before inserting IC chip, in accordance with Eiji's suggestions. APPLE-1004, [0005]-[0007], [0023]-[0025], [0066]; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶254.



APPLE-1003, ¶254 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

Multiple reasons would have prompted a POSITA to utilize EMI shielding, in accordance with Eiji's suggestions, in the multilayer printed wiring substrate. APPLE-1003, ¶255.

First, a POSITA would have been motivated to combine Sakamoto and Eiji to provide protection against external electromagnetic waves, reduce influence by noise from circuits composed of various electronic components, and/or to stabilize electric characteristics of the entire system. APPLE-1003, ¶256.

Sakamoto already teaches accommodating an electronic component such as an IC chip 20 in a space (e.g., "recessed portion 32") in the core substrate, and that multiple components can be included in close arrangement. APPLE-1004, [0066]; *see also*, [0005]-[0007], [0011], [0023]-[0025], [0069]-[0071]; APPLE-1003, ¶¶257-258. A POSITA would have been motivated to mitigate against external

electromagnetic waves or noise generated by circuit components, especially where multiple components are used in close proximity. APPLE-1012, [Abstract]; APPLE-1003, ¶259. Eiji provides a known technique that would have been recognized to further “stabilize the electrical characteristics” of the system. APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶259.

Second, a POSITA would have been prompted to combine Sakamoto and Eiji because doing so was the application of known techniques (forming a shield layer on the inner surface of sidewalls of a through hole provided in an insulating board for incorporating an electronic component) to a known device (Sakamoto’s multilayer printed wiring board having an opening or recessed portion 32 in insulating substrate 30 to accommodate an electronic component such as IC chip 20 between wiring layers) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Sakamoto and Eiji describe similar wiring boards with electronic components embedded inside holes of an insulation board, and because the modifications would have been implemented largely by adding a metal layer on the sidewalls of the hole, in order to create interference protection—a configuration Eiji already demonstrates to be successful. APPLE-1003, ¶260-261. Moreover, Sakamoto and

Eiji describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems discussed above associated with semiconductor packaging and manufacturing. *Id.*

2. Application to Challenged Claims

[1pre]-[1c]⁷

The Sakamoto-Eiji combination provides [1pre]-[1c], as set forth above.

Supra, §VI.D.2, Analysis of [12pre]-[12c]; APPLE-1003, ¶263.

[1a]

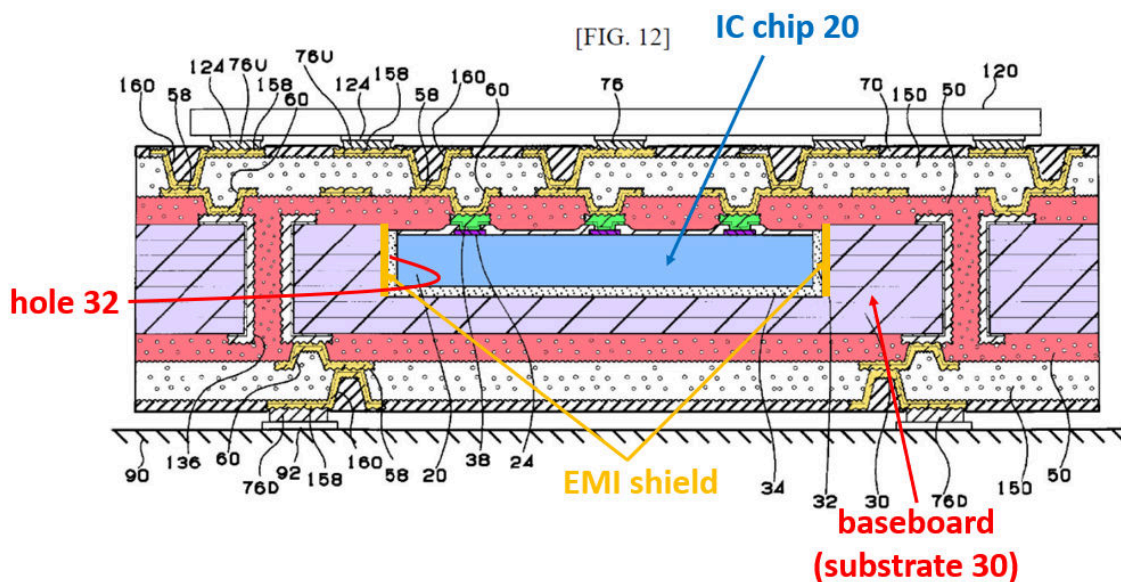
Supra, §VI.D.2, Analysis of [12a], [22]; *see also* APPLE-1012, [0038] (“glass fibers and resins such as epoxy resin.”); [0012]; APPLE-1003, ¶265. .

[1d]

The Sakamoto-Eiji combination renders obvious [1d]. As discussed in §VI.E.1 (Sakamoto-Eiji combination), the combined system includes an IC chip (***microcircuit***) located in a recess (e.g., recessed portion 32) in the insulating substrate 30 (***the hole in the baseboard***). APPLE-1003, ¶266. A shield layer

⁷ To be clear, Sakamoto-Eiji renders obvious independent claim 1 and its dependent claims even without modification to utilize multiple circuit board substructures on top of each other that is described with reference to claims 12-27. APPLE-1003, ¶264.

composed, for example, of a copper plating film that shields electromagnetic waves is formed on an inner surface of the hole and provides **conductive material on sidewalls of the hole**, as claimed. *Supra*, §VI.E.1; APPLE-1003, ¶266. The shielding layer material and configuration of the combined system, in accordance with Eiji's teaching, is just like the formation mechanism disclosed in the '909 patent for growing the conductive material on the sidewalls of the holes, by copper plating. APPLE-1012, [Abstract], [0012]; *compare id.*, [0017] ("electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8") *with* APPLE-1001, 3:61-4:9, 8:39-46; APPLE-1003, ¶¶267-268.



APPLE-1003, ¶267 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[1e]

Supra, §VI.D.2, Analysis of [12d]. Additionally, Sakamoto-Eiji renders

obvious [1e], based on Eiji's further express teaching of "electroless copper plating and electrolytic copper plating" that are "performed on the inner surfaces of" through-holes in an insulating substrate. APPLE-1012, [0017]; APPLE-1003, ¶269.

[2]

Supra, §VI.D.2, Analysis of [12a] (interlayer resin insulating layer 50 contain "epoxy resin"); APPLE-1003, ¶270.

[3]

Sakamoto-Eiji renders obvious Claim [3]. For example, Sakamoto describes that "an epoxy resin can be used for the interlayer resin insulating layer 50" (*hardened insulating polymer layer*). APPLE-1004, [0042]. Sakamoto also describes that the interlayer resin insulating layer 50 is "laminated on the substrate" 30. *Id.*, [0030]. As discussed above, Sakamoto-Eiji's substrate 30 (*baseboard*) contains glass-fiber reinforced epoxy. *Supra*, §§VI.D.2, Analyses of [12pre] and Claim [22], §VI.E.2, Analysis of [1a]. A POSITA would have been prompted to similarly impregnate the epoxy resin of the interlayer resin insulating layer 50 with glass fibers (*contains epoxy and glass fibres*), to achieve similar thermal expansion coefficient, mechanical strength, flexibility, among other relevant physical properties to those of the substrate 30, to reduce mechanical stresses caused by mismatch of these physical properties during heat cycles and

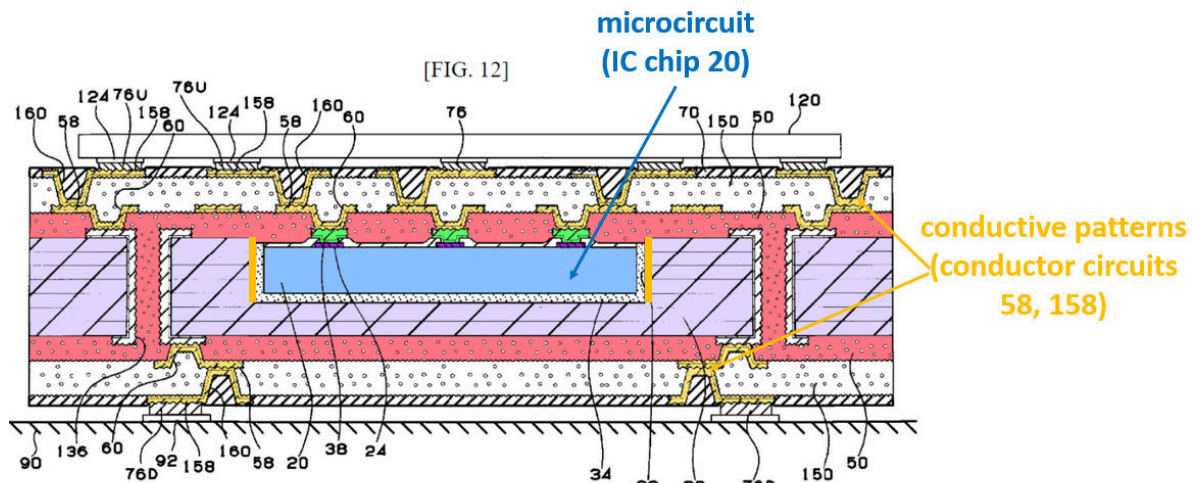
mechanical maneuvers during the manufacturing process, and ultimately enhance the reliability of the entire wiring board system. APPLE-1003, ¶271.

[4]

Supra, §§VI.D.2, Analyses of [12pre] and Claim [22], and §VI.E.2, Analysis of [1a] (Sakamoto-Eiji's substrate 30 (**baseboard**) contains glass fibers impregnated in epoxy resin (**glass-fibre reinforced epoxy board**); APPLE-1003, ¶272.

[5]

In the Sakamoto-Eiji combination, the IC chip 20 (**microcircuit**) is *located between* conductor circuits 58 (and 158) (**conductive patterns**) *on both sides of the insulating material layer*. *Supra*, §§VI.D.2, Analyses of [12pre]-[12c], §§VI.E.2, Analyses of [1pre]-[1c]; APPLE-1003, ¶273.



APPLE-1003, ¶273 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[6]

Sakamoto-Eiji renders obvious Claim [6]. For example, Sakamoto teaches “an adhesive material 34” applied to recessed portion 32 before “IC chip 20 is placed on the adhesive material 34” in the recessed portion. APPLE-1004, [0024]. The “adhesive material” provides *a filler material in the hole* between the metal foil and the IC chip 20 (*microcircuit*) to secure IC chip 20 in place. APPLE-1003, ¶274. This is also consistent with, and further informed by, Eiji’s teaching of a “resin 16, which is primarily epoxy resin” to secure each component at “a predetermined location in the through-hole.” APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1, 3; APPLE-1003, ¶275.

[7]

Supra, §VI.E.2, Analysis of Claim [6] (at least Eiji’s “resin 16” contains “primarily epoxy resin,” and the filler material of the combined system, implemented in accordance with Eiji’s teaching, contains epoxy); APPLE-1003, ¶276.

[8pre]

Supra, §VI.E.2, Analysis of Claim [1]. APPLE-1003, ¶277.

[8a]

Sakamoto-Eiji renders [8a] obvious. *Supra*, §VI.D.2, Analysis of Claim [14]; APPLE-1003, ¶278.

Additionally, Sakamoto-Eiji renders obvious [8a] based on Eiji's description of embedding multiple electronic components in the same substrate. *See e.g.*, APPLE-1012, Abstract, [0006], FIGS. 1-7; APPLE-1003, ¶278.

[8b]

Sakamoto-Eiji renders [8b] obvious. APPLE-1003, ¶279. For example, when several electronic components such as IC chips (*microcircuits*) are provided in the same substrate of the combined system, these components are connected to each other through portions of conductor circuit 58 extending into via holes 60 and/or transition layer 38 (*conductors in the contact opening*) for connecting to both the pads 24 on the first surface of each component and conductor circuit 58 (and 158) (*at least one of the conductive patterns*). *Supra*, §§VI.E.2, Analyses of [1e], [8a], §VI.D.2, Analysis of [12d]; APPLE-1003, ¶279.

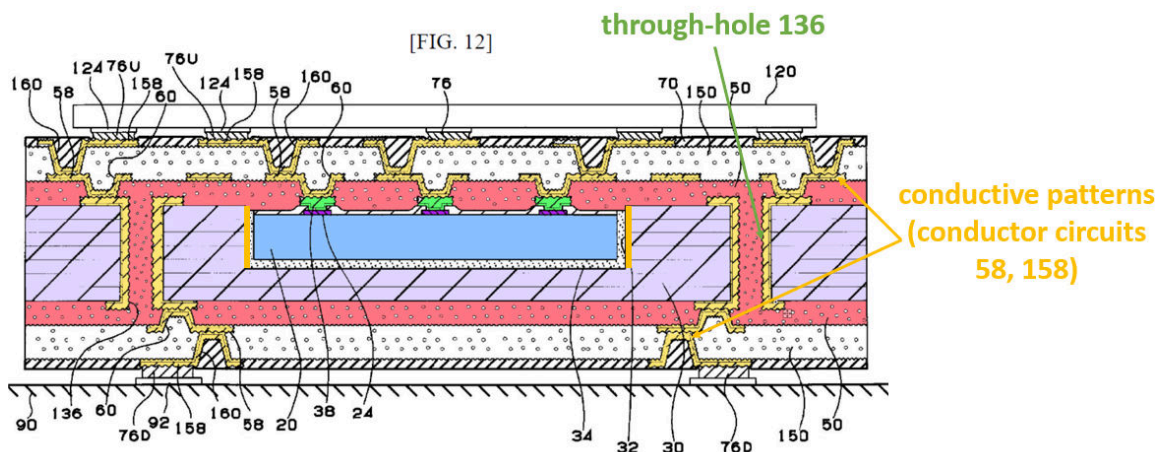
[9]

Sakamoto-Eiji renders obvious Claim [9]. *Supra*, §VI.E.2, Analysis of [1e], §VI.D.2, Analysis of [12d] (transition layer 38 made of copper as part of the *copper in the contact openings* is composed of at least an “electroless plated film 36” (*a first layer of chemically deposited copper*) and an “electrolytic plated film 37” (*a second layer of electrochemically deposited copper on the first layer of chemically deposited copper*); conductor circuit 58 extending into vias 60 (also part of the *copper in the contact openings*) is likewise formed of an electroless

plated film 52 and an electrolytic plated film 56 using copper), Analysis of [24]; APPLE-1003, ¶280. The Sakamoto-Eiji combination further renders obvious claim 9 based on Eiji's express teaching for "electroless copper plating and electrolytic copper plating" that are "performed on the inner surfaces of" through-holes in an insulating substrate. APPLE-1012, [0017]; *supra*, §VI.E.2, Analysis of [1e]; APPLE-1003, ¶281.

[10]

Sakamoto-Eiji renders obvious Claim [10]. For example, metal-lined through-holes 136 provide *an electrically conducting feed-through between the conductive patterns* (provided by conductor circuits 58 and 158) *on the both sides of the insulating material layer* of the wiring board. *Supra*, §VI.A.4, Analysis of Claim [2]; APPLE-1003, ¶282.



APPLE-1003, ¶282 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[11pre]-[11b]

Supra, §§VI.E.2, Analyses of [8pre]-[8b]; APPLE-1003, ¶283.

[12]-[27]

Sakamoto-Eiji renders these claims obvious for at least the same reasons set forth above. *Supra*, §§VI.D.2, Analyses of Claims [12]-[27] and §VI.E.2, Analysis of [1e] (reciting similar features relating to chemically and/or electrochemically deposited copper as [12d], [17d], [19d], [20d], [24], [27d]); APPLE-1003, ¶284.

[22]

Sakamoto-Eiji additionally renders obvious Claim [22] based on Eiji's further teachings. *Supra*, §VI.E.2, Analysis of Claim [4], VI.D.2, Analysis of Claim [20]; APPLE-1003, ¶285.

[25]

Sakamoto-Eiji additionally renders obvious Claim [25] based on Eiji's further teachings of forming metal wiring layers (e.g., 26, 27) above and below embedded electronic components in an insulating substrate through **lamination** of and **plating** over a "copper foil," e.g., by electroless and electrolytic copper plating over "copper foil 5, 6 that is several 10 μm thick." APPLE-1012, [0017], [0013], [0021]-[0022], FIG. 2(A); APPLE-1003, ¶286. Again, Eiji's wiring layers are of substantial thickness of more than (due to plating on top of the copper foil) "several 10 μm thick," compared with the '909 patent's metal coating of "e.g., c. 5 μm ." *Supra*, §VI.B.2 (McCormack-Eiji ground), Analysis of Claim [25]; APPLE-1003, ¶286.

[26]-[27]

Sakamoto-Eiji additionally renders obvious Claim [26]-[27] based on Eiji's further teachings. For example, at least one of Sakamoto-Eiji's conductor layers (e.g., conductor layers having conductor circuits 58 and 158) below IC chip 20 (*below at least one of the microcircuits*) is *a metal foil*, e.g., Sakamoto's plated film of "a thickness of 16 μm ," or formed in accordance with Eiji's express teaching of laminated and plated "copper foil" that is more than "several 10 μm thick." *Supra*, §VI.D.2, Analysis of Claim [25], §VI.E.2, Analysis of Claim [25]; APPLE-1003, ¶287.

[28]

Sakamoto-Eiji renders obvious Claim [28]. *Supra*, §VI.E.2, Analysis of [1d] (Sakamoto-Eiji's shield layer on the sidewalls of hole or recessed portion 32 in substrate 30 (*sidewalls of the hole in the baseboard*) is "composed of a copper plating film" (*covered by a metal foil as the conductive material*)); APPLE-1003, ¶288.

[29]

The Sakamoto-Eiji device has a metal foil covering all sidewalls to provide EMI protection around the semiconductor component. *Supra*, §VI.E.2, Analysis of [1d], [28]. As the component is surrounded by unbroken four sidewalls of the opening in lateral directions, a POSITA would have been prompted to cover all

four sidewalls, providing an unbroken metal foil that surrounds the microcircuit in a lateral direction of the circuit board, and effectuating and enhancing the shielding objective of the metal foil. APPLE-1003, ¶289.

[30]-[32]

Sakamoto-Eiji renders obvious Claim [30]-[32]. *Supra*, §§VI.D.2, Analyses of Claims [25]; VI.E.2, [1], [25]; APPLE-1003, ¶290.

[33]

Sakamoto-Eiji renders obvious Claim [33]. *Supra*, §§VI.D.2, Analyses of Claims [25]; VI.E.2, [25], [28]; APPLE-1003, ¶291.

F. GROUND 2C – Sakamoto, Eiji and Imoto render obvious Claims 12-27

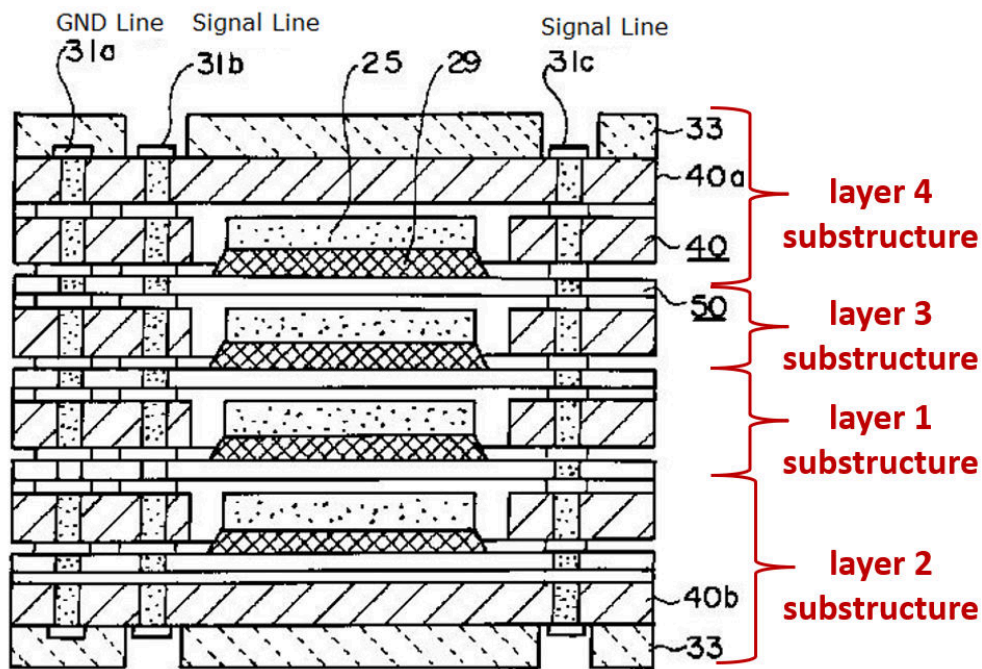
Imoto provides further express teachings of a “stacked” multi-layered circuit board, further informing the “multi-layered” elements of independent claim 12 and its dependent claims. APPLE-1003, ¶292. Thus, Ground 2C provides an additional manner in which the prior art renders obvious claims 12-27. *Id.*

1. Imoto

Imoto describes a semiconductor device using a “stacked package” with a semiconductor element embedded in a chip cavity portion of each of a plurality of stacked wiring substrates and electrically connected to the wiring. APPLE-1016, Abstract. Imoto thus teaches a stack-up multi-layered structure with each substructure layer having similar configurations. *Id.*, FIGS. 5-9 (and related

descriptions), [0010] (“Any number equal to or greater than two can be stacked.”),
Cls, 1, 2, 8. APPLE-1003, ¶¶85-89.

[FIG. 8]



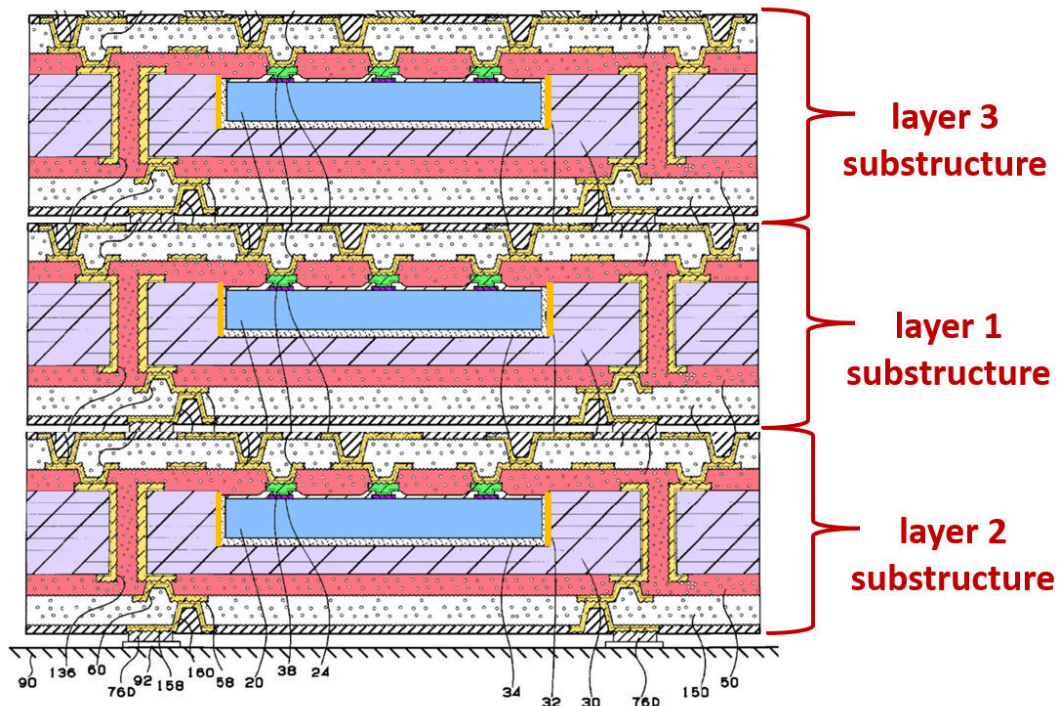
APPLE-1003, ¶87 (APPLE-1016, FIG. 8 (Annotated))

2. Predictable Combination of Sakamoto, Eiji and Imoto

A POSITA would have been motivated to combine the teachings of Sakamoto, Eiji and Imoto to provide a high-density, multi-layered structure with EMI shielding effect. APPLE-1003, ¶293. Each relates to multilayer wiring substrates with built-in semiconductor components. *See e.g.*, APPLE-1004, Abstract, [0001], [0005], [0017], [0020], [0023]-[0025], [0066]; APPLE-1012, [0023], FIGS. 1, 4; APPLE-1016, Abstract, [0004]-[0006]. Imoto describes stacking up “[a]ny number equal to or greater than two” of layers of similar

configuration, to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1016, [0002], [0010], Cls.1, 2, 4, 8, FIGS. 5-9 (and related descriptions). APPLE-1003, ¶293.

A POSITA would have been motivated to utilize an EMI shield feature in accordance with Eiji in a recessed portion in the core substrate described by Sakamoto, and to stack up two, three, or more layers of similar configuration to form a multi-layered structure in accordance with Imoto to achieve high density mounting and EMI shielding. APPLE-1003, ¶294; *supra*, §VI.A.3 (Sakamoto-Eiji combination). Each substructure has an IC chip component embedded in a recessed portion of a substrate, and each recessed portion has EMI shield on its sidewalls.



APPLE-1003, ¶294 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

A POSITA would have had a reasonable expectation of success in making the proposed modification given that Sakamoto, Eiji and Imoto describe similar multilayer wiring substrates with built-in semiconductor components, and because the modifications involve implementation of well-known technologies. APPLE-1003, ¶295. The references relate to the same field of endeavor and are directed to analogous subject matter that inform construction of multi-layered configurations. *Id.*

3. Application to Challenged Claims

[12]-[27]

Sakamoto-Eiji renders obvious claims 12-27 for the reasons described above

in Grounds 2A and 2B. But even if Sakamoto-Eiji did not, the predictable Sakamoto-Eiji-Imoto combination would do so.⁸ In accordance with Imoto's express teachings of a multi-layered structure, the Sakamoto-Eiji-Imoto combination includes a stack-up multi-layered structure, such as including three substructures as shown in the composite figure above, each of the layer 1-3 substructures having similar configuration. APPLE-1003, ¶296; *supra*, §VI.F.2 (Sakamoto-Eiji-Imoto combination). The structures of Sakamoto-Eiji-Imoto thus disclose each element of [12]-[27] in the same manner as set forth in Grounds 2A and 2B, with Imoto further informing and motivating the multi-layered structure and electrical connection between each substructure. *Id.*

VII. The *Advanced Bionics* Test Favors Institution—§325(D)

None of McCormack, Sakamoto, Eiji, or Imoto were applied in a rejection during prosecution, and each is relied upon for disclosure of subject matter that is materially different than applied or set forth within references cited during prosecution. The Petition thus does not involve the same or substantially the same art or arguments previously presented, ending the *Advanced Bionics* inquiry in

⁸ Where Imoto is not addressed in Ground 2C, the Ground 2A and Ground 2B analysis applies fully here in Ground 2C.

favor of institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

While a family member of Sugaya was cited on the face of the '909 patent, none of the other references were applied in a substantive office action, which demonstrate the unpatentability of the prior art.

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314

Essentially all of the *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written Decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors. Moreover, a Motion to Transfer to the Northern District of California remains pending. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while litigation remains in early stages. As noted above, Motions to

Transfer remains pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds, outweighing any inefficiencies.

IX. FEES

Apple authorizes charge of fees to Deposit Account No. 06-1050.

X. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '909 patent. The '909 patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0192IP2@fr.com.

Respectfully submitted,

Dated: February 5, 2025

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,804 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 5, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 5, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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