

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS
AMERICA, INC.; and SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
Petitioner,

v.

IMBERATEK LLC,
Patent Owner.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Before DONNA M. PRAISS, JON B. TORNQUIST, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Settlement Prior to Institution of Trial
37 C.F.R. § 42.74

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

With our authorization, Petitioner, Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC, and Patent Owner, ImberaTek LLC, filed a Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases. Paper 8 (“Joint Motions”).¹ In their Joint Motions, the parties contend that dismissal is appropriate as the *inter partes* reviews (“IPRs”) are in their early stages and the parties “have settled all disputes” related to the involved patents. *Id.* at 1–2.

With their Joint Motions, the parties filed (1) a copy of a Settlement and Patent License Agreement that the parties represent “resolves the disputes in the above-captioned *inter partes*” reviews, (2) a Confirmatory Letter from Patent Owner to Petitioner acknowledging and confirming certain facts and rights related to the Settlement and Patent License Agreement, and (3) a Joint Request to treat the settlement documents as business confidential information, to be kept separate from the files of the above-captioned patents. Ex. 1022 (“Settlement and Patent License Agreement”); Ex. 1023 (“Confirmatory Letter”); Paper 9 (“Joint Request”).

“There are strong policy reasons to favor settlement between the parties to a proceeding,” and “[t]he Board expects that a proceeding will terminate after the filing of a settlement agreement, unless the Board has already decided the merits of the proceeding.” Patent Trial and Appeal

¹ We cite to papers and exhibits filed in IPR2022-01597. Similar papers and exhibits were filed in each of the above-captioned cases.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Board Consolidated Trial Practice Guide November 2019, at 86 (citing 35 U.S.C. §§ 317(a), 327). The above-captioned IPRs are at an early stage, with the Board not yet reaching the merits of the petitions or issuing institution decisions. Thus, we find it is appropriate to dismiss the petitions and terminate the proceedings in each of the above-captioned IPRs.

We also find it appropriate to treat the settlement documents as business confidential information, to be kept separate from the files of the involved patents.

Accordingly, it is

ORDERED that the Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases is *granted*;

FURTHER ORDERED that the parties' Joint Request that the settlement documents (Exs. 1022, 1023) be treated as business confidential information and kept separate from the files of the involved patents is *granted*; and

FUTHER ORDERED that the proceedings in the above-captioned IPRs are *terminated*.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

FOR PETITIONER:

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv233	DATE FILED 6/24/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF ImberaTek LLC		DEPENDANT SAMSUNG ELECTRONICS CO., LTD, et al
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,609,527	10/27/2009	ImberaTek LLC
2 8,222,723	7/17/2012	ImberaTek LLC
3 8,368,201	2/5/2013	ImberaTek LLC
4 7,989,944	8/2/2011	ImberaTek LLC
5 8,238,113	8/7/2012	ImberaTek LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 10/31/2022	INCLUDED BY ☒ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 11,071,207	7/20/2021	ImberaTek LLC
2 7,732,909	6/8/2010	ImberaTek LLC
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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PLAINTIFF ImberaTek LLC		DEPENDANT SAMSUNG ELECTRONICS CO., LTD, SAMSUNG ELECTRONICS AMERICA, Inc., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,107,324	8/15/2015	ImberaTek LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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2 8,222,723	7/17/2012	ImberaTek LLC
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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5967120

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	7732909	
Patent Number:	7989944	
Patent Number:	7609527	
Patent Number:	8817485	
Patent Number:	8034658	
Patent Number:	8222723	
Patent Number:	8487194	
Patent Number:	9232658	
Patent Number:	8351214	
Patent Number:	8455994	
Patent Number:	8368201	
Patent Number:	9622354	
Patent Number:	9691724	
Patent Number:	9107324	
Patent Number:	10231335	
Patent Number:	10085345	
Patent Number:	10010019	
Patent Number:	10085347	
Patent Number:	9324647	
Patent Number:	9883587	

Property Type	Number
Patent Number:	9674948
Patent Number:	9820375
Patent Number:	10470346
Application Number:	14580257
Application Number:	15355096
Application Number:	16104979

CORRESPONDENCE DATA

Fax Number: (703)643-9789
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Email: yoon@capitoliplaw.com
Correspondent Name: YEASUN YOON
Address Line 1: 20319 KIAWAH ISLAND DR
Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER:	PA01GETOIMBERATEK02
NAME OF SUBMITTER:	YEASUN YOON
SIGNATURE:	/yoon/
DATE SIGNED:	02/18/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7
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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this "**Assignment**") is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company ("**Assignor**"), in favor of **ImberaTek, LLC**, a Delaware limited liability company ("**Assignee**").

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the "**Patent Sale Agreement**"); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the "**Patents**").

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

Name: Patrick K. Patnode

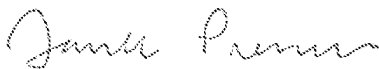
Title: Authorized SIGNATORY

Acknowledgement:

State of New York)

ss.

County of Schenectady)


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8022402
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRPI0307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A 1, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A 1, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1 , US10010019B2, US2018352689A 1	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15/937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	08/02/2011	7989944	0365-0601PUS3	8440

2292 7590 07/13/2011
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 843 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Risto Tuominen, Helsinki, FINLAND;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$0	\$0	\$1510	\$0	06/28/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
DIALLO, MAMADOU L	2895	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 Birch, Stewart, Kolasch & Birch, LLP
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Imbera Electronics Oy

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Espoo, Finland

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account Number 02-2448 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☒ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature _____
 Typed or printed name Michael K. Mutter

Date June 27, 2011
 Registration No. 29,680

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MS Issue Fee
PATENT
0365-0601PUS3

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	Risto Tuominen	Conf.:	8440
Appl. No.:	11/878,557	Group:	2895
Filed:	July 25, 2007	Examiner:	Mamadou L Diallo
For:	METHOD FOR EMBEDDING A COMPONENT IN A BASE		

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

MS Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant is appreciative of the Notice of Allowance papers dated March 28, 2011. Applicant offers the following comments regarding these documents.

In the Reasons for Allowance, the Examiner listed (pages 2-3 of the Notice of Allowability) portions of independent claims 1, 15 and 32 in connection with claim language which does not appear in each of these claims. Thus, Applicant would like to point out that claim 1 recites:

“a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.”

Cet

Applicant would also like to point out that claim 15 recites:

“a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,
a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers”

Finally, claim 32 recites:

“a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface,
a filler material in the hole between the metal foil and the microcircuit,
a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and
contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.”

Applicant respectfully notes that invention is defined by all of the allowed claims, which stand upon their own recitations, and limitations should not be imputed to any of the claims based upon the statement of Reasons for Allowance. Moreover, Applicant respectfully reserves his right to argue alternative interpretations and additional patentable distinctions of the claimed invention over any alleged prior art, should that need ever arise, and do not necessarily agree with any characterization of the invention and/or advantages thereof expressed by the Examiner.

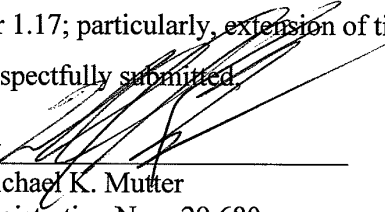
If the Examiner has any questions concerning this application, the Examiner is requested to contact Corina E. Tanasa, Registration No. 64,042, at telephone number (703) 208-4003, located in the Washington, DC area.

Application No. 11/878,557

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: June 27, 2011

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29,680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road

Suite 100 East

P.O. Box 747

Falls Church, Virginia 22040-0747

(703) 205-8000

Attorney for Applicant

cef

Electronic Acknowledgement Receipt	
EFS ID:	10396687
Application Number:	11878557
International Application Number:	
Confirmation Number:	8440
Title of Invention:	METHOD FOR EMBEDDING A COMPONENT IN A BASE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Michael Keith Mutter/Ruth Calendine
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0601PUS3
Receipt Date:	27-JUN-2011
Filing Date:	25-JUL-2007
Time Stamp:	17:42:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2011062ISSUEFEE.PDF	214187	yes	4
			62601e903660f482041c6ed023d850f6e719a47f		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Issue Fee Payment (PTO-85B)	1	1
	Request for Corrected Notice of Allowance	2	4
Warnings:			
Information:			
Total Files Size (in bytes):		214187	
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$0	\$0	\$1510	\$0	06/28/2011
EXAMINER	ART UNIT	CLASS-SUBCLASS	Adjustment date: 06/28/2011 HBLANC01 12/08/2010 INTEFSW 00003634 022448 11878557 01 FC:1501 1510.00 CR			
DIALLO, MAMADOUL	2895	257-774000				

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

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(2) the name of a single firm (having at least one registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
- 1 Birch, Stewart, Kolasch & Birch, LLP
HBLANC01 00000022 022448 11878557
01 FC:1501 3 1510.00 DA

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(A) NAME OF ASSIGNEE

Imbera Electronics Oy

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Espoo, Finland

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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☐ Publication Fee (No small entity discount permitted)
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(e)(2).

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Authorized Signature _____

Typed or printed name Michael K. Mutter

Date June 27, 2011

Registration No. 29,680

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NOTICE OF ALLOWANCE AND FEE(S) DUE

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

DIALLO, MAMADOU L

ART UNIT

PAPER NUMBER

2895

DATE MAILED: 03/28/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$0	\$0	\$1510	\$0	06/28/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

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EXAMINER	ART UNIT	CLASS-SUBCLASS
DIALLO, MAMADOUL	2895	257-774000

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2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

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- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature _____

Date _____

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Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440
2292 7590 03/28/2011 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			EXAMINER DIALLO, MAMADOU L	
			ART UNIT 2895	PAPER NUMBER

DATE MAILED: 03/28/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 843 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 843 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	11/878,557	TUOMINEN, RISTO	
	Examiner	Art Unit	
	MAMADOU DIALLO	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the remarks filed on 06/17/2010.

2. ☒ The allowed claim(s) is/are 1-36.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/502336.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>01/04/2011</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 01/04/2011 has been entered.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 01/04/2011 is being considered by the examiner.

Allowable Subject Matter

Claims 1, 15 and 32 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest, singularly or in combination, at least the limitations of the independent claim 1, 15, and 32 including "a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface, a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer,

and contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.”

Because no reference alone, nor is there any motivation to combine the details over the prior art to create such limitations in these independent claims, the claims are deemed patentable over the prior art.

Claims 2-14, 16-31 and 32-36 are also allowed as being directly or indirectly dependent of the allowed base claim(s).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAMADOU DIALLO whose telephone number is (571)270-5449. The examiner can normally be reached on 9:30- 6:30 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. D./
Examiner, Art Unit 2895

/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895

<i>Index of Claims</i> 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	02/27/2010	08/19/2010						
1	1	✓	=						
2	2	✓	=						
3	3	✓	=						
4	4	✓	=						
5	5	✓	=						
6	6	✓	=						
7	7	✓	=						
8	8	✓	=						
11	9	✓	=						
12	10	✓	=						
9	11	✓	=						
13	12	✓	=						
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14	14	✓	=						
15	15	✓	=						
16	16	✓	=						
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27	27	✓	=						
28	28	✓	=						
29	29	✓	=						
30	30	✓	=						
31	31	✓	=						
32	32	✓	=						
33	33	✓	=						
34	34	✓	=						
35	35	✓	=						
36	36	✓	=						

Issue Classification 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

ORIGINAL						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
257		687				H	0	1	L	21 / 52 (2006.01.01)									
CROSS REFERENCE(S)						H	0	1	L	21 / 60 (2006.01.01)									
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
257	774	E23.005	E21.503	678	684														

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	33	33										
2	2	18	18	34	34										
3	3	19	19	35	35										
4	4	20	20	36	36										
5	5	21	21												
6	6	22	22												
7	7	23	23												
8	8	24	24												
11	9	25	25												
12	10	26	26												
9	11	27	27												
13	12	28	28												
10	13	29	29												
14	14	30	30												
15	15	31	31												
16	16	32	32												

/MAMADOU DIALLO/ Examiner.Art Unit 2895 (Assistant Examiner)	03/14/2011 (Date)	Total Claims Allowed: 36	
/N DREW RICHARDS/ Supervisory Patent Examiner.Art Unit 2895 (Primary Examiner)	03/15/2011 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4D

Search Notes 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

SEARCHED			
Class	Subclass	Date	Examiner
257	793,774,700,	2/27/2010	MD
257	257/e23.005,e23.126,e23.128,e23.182,e21.5,e21.503,e21.505,e21.511	8/19/2010	MD
438	107,118,126	8/19/2010	MD

SEARCH NOTES			
Search Notes		Date	Examiner
updated search		3/15/2011	MD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see attached interference search	8/19/2010	MD
	see attached updated interference search	3/15/2011	MD

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Receipt date: 01/04/2011

11878557 - GAU: 2895

PTO/SB/085 (07-03)

Approved for use through 07/31/2012. OMB 0851-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO				Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	11/878,557-Conf. #8440	
				Filing Date	July 25, 2007	
				First Named Inventor	Risto TUOMINEN	
				Art Unit	2895	
				Examiner Name	M. L. Diallo	
Sheet	1	of	1	Attorney Docket Number	0365-0601PUS3	
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	AA*	US-6,607,943-B1	08-19-2003	Kinsman		
	AB*	US-5,102,829	04-07-1992	Cohn		
	AC*	US-5,227,338	07-13-1993	Kryzaniwsky		
	AD*	US-5,970,321	10-19-1999	Hively		
	AE*	US-6,015,722	01-18-2000	Banks et al.		
	AF*	US-6,100,108	08-08-2000	Mizuno et al.		
	AG*	US-20010054756	12-27-2001	Isaak		
	AH*	US-2002/0020898-A1	02-21-2002	Vu et al.		
	AI*	US-20020063342	05-30-2002	Blackshear		
	AJ*	US-20020127770	09-12-2002	Vaiyapuri		
	AK*	US-6,495,394	12-17-2002	Nakata et al.		
	AL*	US-6,521,530	02-18-2003	Peters et al.		
	AM*	US-5,305,670-A1	04-26-1994	Mowatt et al.		
	AN*	US-5,943,216	08-24-1999	Schmidt		
	AO*	US-6,131,269-A	10-17-2000	Lee et al.		
	AP*	US-6,324,067	11-27-2001	Nishiyama		
	AQ*	US-2003/0090883-A1	05-15-2003	Asahi et al.		
	AR*	US-4,246,595	01-20-1981	Noyori et al.		
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.	Foreign Patent Document Country Code ³ / Number ⁴ / Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	Fig. 1*
NON PATENT LITERATURE DOCUMENTS						
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ⁶
Examiner Signature	/Mamadou Diallo/				Date Considered	03/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

³Applicant's unique citation designation number (optional). ⁵Applicant is to place a check mark here if English language Translation is attached.

let

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D./

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"US 20080036093"	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/02/26 10:40
S2	25	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "4246595" "5162613" "5208188" "5216806" "5637919" "6038133" "6154366" "6271469" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596"). PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:44
S3	28	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "5162613" "5208188" "5216806" "5248852" "5497033" "5637919" "6038133" "6154366" "6271469" "6284564" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596"). PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:46
S4	25089	circuit board with (components or chip) with (in or inside)	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:03
S5	67	circuit board with (components or chip) with (in or inside)with insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:04

S6	18	electronic with embed\$4 with printed circuit same insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:09
S7	424	electronic with embed\$4 with printed circuit	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:10
S8	2	("20050048759" "20060068332").PN. OR ("7653991").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:20
S9	16	("20020071256" "20020118523" "20030000737" "3857683" "5243320" "5683928" "6021050" "6225570" "6288905" "6356455" "6717071" "6757178" "6806428" "6876091").PN. OR ("7190592").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:22
S10	1	"20020132096"	US-PGPUB; USPAT	ADJ	ON	2010/02/26 14:37
S11	1	("20070018203").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/01 14:19
S12	24	("20010054758" "20020020898" "20020063342" "20020127770" "5102829" "5227338" "5970321" "6015722" "6100108" "6495394" "6521530" "6607943"). PN.	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:30
S13	5434	((438/107,118,126) or (2571/e23.005,e23.126, e23.128,e23.182,e21.5, e21.503,e21.505,e21.511)). CCLS.	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:41
S14	52	((438/107,118,126) or (2571/e23.005,e23.126, e23.128,e23.182,e21.5, e21.503,e21.505,e21.511)). CCLS. and (hardened with insulating)	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:42
S15	133	((438/107,118,126) or (257/ e23.005,e23.126,e23.128, e23.182,e21.5,e21.503, e21.505,e21.511)).CCLS. and (hardened with insulating)	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:44

S17	18	("20010054758" "20020020898" "20020053342" "20020127770" "20030090883" "4246595" "5102829" "5227338" "5306670" "5943216" "5970321" "6015722" "6100108" "6131269" "6324067" "6495394" "6521530" "6607943").PN.	US-PGPUB; USPAT	ADJ	ON	2011/02/14 15:09
S18	18	("20010054758" "20020020898" "20020053342" "20020127770" "20030090883" "4246595" "5102829" "5227338" "5306670" "5943216" "5970321" "6015722" "6100108" "6131269" "6324067" "6495394" "6521530" "6607943").PN.	US-PGPUB; USPAT	ADJ	ON	2011/03/14 11:38

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	6	insulat\$5 same harden \$5 same polymer same open\$5 same metal same contact	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/03/15 16:03
L3	13	insulat\$5 with metal with plate with second with inside with conductive	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/03/15 16:06
S16	6	insulat\$5 same harden \$5 same polymer same open\$5 same metal same electrical	US-PGPUB; USPAT; UPAD	ADJ	ON	2010/08/19 13:05

3/ 15/ 2011 4:07:41 PM**C:\ Documents and Settings\ mdiallo\ My Documents\ EAST\ Workspaces\ 11878557.wsp**

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PATENT WITHDRAWAL NOTICE

DATE WITHDRAWN

1/5/11

WITHDRAWAL NUMBER

18898

The following application has been **WITHDRAWN** from the

Tuesday, January 18, 2011 issue.

SERIAL NO.

11/878,557

PATENT NUMBER

7,872,342

DRAWINGS

012

CLASS

257/774

TITLE

METHOD FOR EMBEDDING A COMPONENT IN A BASE

NAME AND ADDRESS

RISTO TUOMINEN
HELSINKI, FINLAND

REASON FOR WITHDRAWAL

Office of Petitions granted applicant's request to withdraw patent from issue.

APPROVED

/Kimberly Terrell/, Manager

Patent Publication Branch
Office of Data Management



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
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Alexandria, VA 22313-1450
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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH VA 22040-0747

MAILED

JAN 05 2011

OFFICE OF PETITIONS

In re Application of :
Riston Tuominen :
Application No. 11/878,557 : **DECISION GRANTING PETITION**
Filed: July 25, 2007 : **UNDER 37 CFR 1.313(c)(2)**
Attorney Docket No. 0365-0601PUS3 :

This is a decision on the petition under 37 CFR 1.313(c)(2), filed, January 4, 2011 to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED**.

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid on December 7, 2010 cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.¹

Telephone inquiries should be directed to Terri Johnson at (571) 272-2991.

This application is being referred to Technology Center AU 2895 for processing of the request for continued examination under 37 CFR 1.114 and for consideration of the concurrently filed information disclosure statement.

/Terri Johnson/
Terri Johnson
Petitions Examiner
Office of Petitions

¹ *The request to apply the issue fee to the new Notice may be satisfied by completing and returning the new Part B – Fee(s) Transmittal Form (along with any balance due at the time of submission). Petitioner is advised that the Issue Fee Transmittal Form must be completed and timely submitted to avoid abandonment of the application.*



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Date : January 5, 2011
TO : Director, Office of Data Management
FROM : Office of Petitions
SUBJECT : Withdrawal from Issue of **Application No. 11/878,557**

Applicant(s) : Risto Tuominen
Application No. : 11/878,557
Filed : July 25, 2007

The above-identified application has been assigned Patent No. 7,872,342 and an issue date of January 18, 2011.

It is hereby directed that this application be withdrawn from issue at the request of the applicant. Do not refund the issue fee.

The following erratum should be published in the Official Gazette if the above-identified application is published in the OG of January 18, 2011:

"All reference to Patent No. 7,872,342 to Risto Tuominen of Finland for METHOD FOR EMBEDDING A COMPONENT IN A BASE appearing in the Official Gazette of January 18, 2011 should be deleted since no patent was granted."

/Terri Johnson/
Terri Johnson
Petitions Examiner
Office of Petitions

cc: Paul Harrison
Deneise Boyd
Mary Louise McAskill
Niomi Farmer
Mary E. Johnson (Cookie)
Brad Harris
Kim Terrell
Lamont Fletcher

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request
for
Continued Examination (RCE)
TransmittalAddress to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	11/878,557
Filing Date	July 25, 2007
First Named Inventor	Risto TUOMINEN
Art Unit	2895
Examiner Name	M. L. Diallo
Attorney Docket Number	0385-0601PUS3

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

- a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
- i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ii. ☐ Other _____
- b. ☒ Enclosed
- i. ☐ Amendment/Reply
- ii. ☐ Affidavit(s)/ Declaration(s)
- iii. ☒ Information Disclosure Statement (IDS)
- iv. ☐ Other _____

2. **Miscellaneous**

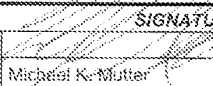
- Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a
- a. ☐ period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(f) required)
- b. ☐ Other _____

3. **Fees**

- The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
- The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 02-2448
- a. ☒ RCE fee required under 37 CFR 1.17(e)
- i. ☒ RCE fee required under 37 CFR 1.17(e)
- ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
- iii. ☐ Other _____
- b. ☐ Check in the amount of \$ _____ enclosed
- c. ☐ Payment by credit card (Form PTO-2038 enclosed).

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	January 4, 2011
Name (Print/Type)	Michael K. Mutter	Registration No.	29,680

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature		Date	
Name (Print/Type)			

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Risto TUOMINEN

Appl. No.:

11/878,557

Confirmation No.: 8440

Filed:

July 25, 2007

Art Unit:

2895

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner:

M. L. Diallo

**PETITION TO WITHDRAW APPLICATION FROM
ISSUE PURSUANT TO 37 C.F.R. § 1.313(c)**

MS 313(c)

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

Applicant hereby petitions the Commissioner to withdraw the above-identified application from Issue. The Issue Fee in this application was timely paid on December 7, 2010.

It is requested that the above-mentioned application be withdrawn from Issue for the following reason:

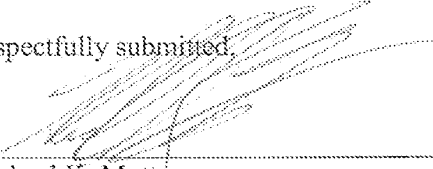
- ☐ Unpatentability of one or more claims. Submitted herewith is an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable (37 C.F.R. § 1.313(c)(1));
- ☒ Consideration of a Request for Continued Examination under 37 C.F.R. § 1.114 (37 C.F.R. § 1.313(c)(2)); or

☐ Express abandonment of the application (37 C.F.R. § 1.313(c)(3)).

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: January 4, 2011

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29,680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road, Suite 100 East

P.O. Box 747

Falls Church, VA 22040-0747

703-205-8000



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FEE **Under 37 CFR 1.17(f), (g) & (h)** **TRANSMITTAL**

(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	11/878,557	Conf. No.	8440
Filing Date	July 25, 2007		
First Named Inventor	Risto TUOMINEN		
Art Unit	2885		
Examiner Name	M. L. Diallo		
Attorney Docket Number	0385-0601PUS3		

Enclosed is a petition filed under 37 CFR 1.313 that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of \$ 130.00 is enclosed.

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. For transmittal of processing fees under 37 CFR 1.17(f), see form PTO/SB/17L.

Payment of Fees (small entity amounts are NOT available for the petition fees)

☒ The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 02-2448:

☒ petition fee under 37 CFR 1.17(f), (g) or (h) ☒ any deficiency of fees and credit of any overpayments

☐ Check in the amount of \$ _____ is enclosed.

☐ Payment by credit card (Form PTO-2038 or equivalent enclosed). Do not provide credit card information on this form.

Petition Fees under 37 CFR 1.17(f): Fee \$400 Fee Code 1462

For petitions filed under:

- § 1.36(a) - for revocation of a power of attorney by fewer than all applicants
- § 1.53(e) - to accord a filing date.
- § 1.57(a) - to accord a filing date.
- § 1.182 - for decision on a question not specifically provided for.
- § 1.183 - to suspend the rules.
- § 1.378(e) - for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
- § 1.741(b) - to accord a filing date to an application under § 1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee \$200 Fee Code 1463

For petitions filed under:

- § 1.12 - for access to an assignment record.
- § 1.14 - for access to an application.
- § 1.47 - for filing by other than all the inventors or a person not the inventor.
- § 1.59 - for expungement of information.
- § 1.103(a) - to suspend action in an application.
- § 1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
- § 1.295 - for review of refusal to publish a statutory invention registration.
- § 1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
- § 1.377 - for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
- § 1.550(c) - for patent owner requests for extension of time in *ex parte* reexamination proceedings.
- § 1.956 - for patent owner requests for extension of time in *inter partes* reexamination proceedings.
- § 5.12 - for expedited handling of a foreign filing license.
- § 5.15 - for changing the scope of a license.
- § 5.25 - for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee \$130 Fee Code 1464

For petitions filed under:

- § 1.19(g) - to request documents in a form other than that provided in this part.
- § 1.84 - for accepting color drawings or photographs.
- § 1.91 - for entry of a model or exhibit.
- § 1.102(d) - to make an application special.
- § 1.138(c) - to expressly abandon an application to avoid publication.
- § 1.313 - to withdraw an application from issue.
- § 1.314 - to defer issuance of a patent.

Michael K. Mutter

Signature

Typed or printed name

January 4, 2011

Date

29,680

Registration No., if applicable

This collection of information is required by 37 CFR 1.17. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No.: 0365-0601PUS3
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Risto TUOMINEN

Application No.: 11/878,557

Confirmation No.: 8440

Filed: July 25, 2007

Art Unit: 2895

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner: Mamadou L.
Diallo

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the attached PTO/SB/08.

II. COPIES

☒ a. Copies of foreign patent documents, non-patent literature and other information.

☐ b. REFERENCES PREVIOUSLY CITED OR SUBMITTED: Copies of any information not provided can be found in one or more of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Application No. and U.S. Filing Date

10/502,336 filed September 23, 2004

III. CONCISE EXPLANATION OF THE RELEVANCE/OTHER INFORMATION

☐ a. NON-ENGLISH LANGUAGE DOCUMENTS: A concise explanation of the relevance of all non-English language patents, publications, or other information listed is as follows:

☐ b. ENGLISH LANGUAGE SEARCH REPORT OR FOREIGN PATENT OFFICE COMMUNICATION: An English language version of the search report or Foreign Patent Office communication that indicates the degree of relevance is attached.

☒ c. OTHER: The following additional information is provided.

Some references submitted herein were cited by the Examiner in US Appl. No. 11/797,609 (now US Patent 7,732,909) which is a continuation of US Appl. No. 10/502,336 (now US patent 7,294,529), wherein US Appl. No. 10/502,336 is also the parent of the present application.

Three references submitted herein (US 4,246,595, US 5,943,216 and US 6,324,067) were cited in a European application which belongs to the family of applications including the present application, US Appl. No. 11/797,609 and US Appl. No. 10/502,336 .

A Response filed in the above-mentioned European application and which discusses US 4,246,595, US 5,943,216 and US 6,324,067 is also submitted herein.

IV. STATEMENT UNDER 37 C.F.R. § 1.97(e)

The undersigned hereby states that:

☐ a. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than 30 days prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ b. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ c. No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.

☐ d. Some of the items of information in the IDS were cited in a communication from a foreign patent office. Such items were first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office. As to the remaining items of information, to the knowledge of the person signing the certification after making reasonable inquiry, such remaining items were not known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

V. FEES

☒ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application or Request for Continued Examination. No fee is required.

☐ b. This Information Disclosure Statement is being filed within three months of the filing date of an application. No fee is required.

☐ c. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits. No fee is required. If a first Office Action on the merits has issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) above. If no statement has been made, charge our deposit account for the required fee.

☐ d. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action or before the mailing date of a Notice of Allowance (see 37 C.F.R. § 1.97(c)(1)).

☐ No statement. The fee as required by 37 C.F.R. § 1.17(p) is provided.

or

☐ See the above statement. No fee is required.

☐ e. This Information Disclosure Statement is being filed after the mailing date of a Final Office Action or after the mailing date of a Notice of Allowance (see 37 C.F.R. § 1.97(d)), see the statement above. The fee as required by 37 C.F.R. § 1.17(p) is provided.

VI. PAYMENT OF FEES

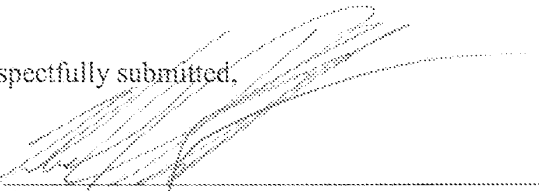
☐ The required fee is listed on the attached Fee Transmittal.

☒ No fee is required.

If the Examiner has any questions concerning this IDS, please contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the USPTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

Dated: January 4, 2011

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29,680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road, Suite 100 East

P.O. Box 747

Falls Church, VA 22040-0747

703-205-8000

Attachment(s):

- ☒ PTO/SB/08
- ☒ Document(s)
- ☐ Foreign Patent Office Communication
- ☐ Foreign Search Report
- ☐ Fee
- ☐ Other:

et

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known Application Number: 11/878,557-Conf. #8440 Filing Date: July 25, 2007 First Named Inventor: Risto TUOMINEN Art Unit: 2895 Examiner Name: M. L. Diallo Attorney Docket Number: 0365-0601PUS3	
Sheet	1	of	1		
U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA*	US-6,607,943-B1	08-19-2003	Kinsman	
	AB*	US-5,102,829	04-07-1992	Cohn	
	AC*	US-5,227,338	07-13-1993	Kryzaniwsky	
	AD*	US-5,970,321	10-19-1999	Hively	
	AE*	US-6,015,722	01-18-2000	Banks et al.	
	AF*	US-6,100,108	08-08-2000	Mizuno et al.	
	AG*	US-20010054758	12-27-2001	Isaak	
	AH*	US-2002/0020898-A1	02-21-2002	Vu et al.	
	AI*	US-20020063342	05-30-2002	Blackshear	
	AJ*	US-20020127770	09-12-2002	Vaiyapuri	
	AK*	US-6,495,394	12-17-2002	Nakata et al.	
	AL*	US-6,521,530	02-18-2003	Peters et al.	
	AM*	US-5,305,670-A1	04-26-1994	Mowatt et al.	
	AN*	US-5,943,216	08-24-1999	Schmidt	
	AO*	US-6,131,259-A	10-17-2000	Lee et al.	
	AP*	US-6,324,067	11-27-2001	Nishiyama	
	AQ*	US-2003/0090883-A1	05-15-2003	Asahi et al.	
	AR*	US-4,246,595	01-20-1981	Noyori et al.	
FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No.	Foreign Patent Document Country Code ³ / Number ⁴ / Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
Examiner Signature				Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 806. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

³Applicant's unique citation designation number (optional). ⁵Applicant is to place a check mark here if English language translation is attached.

let

Electronic Patent Application Fee Transmittal				
Application Number:		11878557		
Filing Date:		25-Jul-2007		
Title of Invention:		METHOD FOR EMBEDDING A COMPONENT IN A BASE		
First Named Inventor/Applicant Name:		Risto Tuominen		
Filer:		Michael Keith Mutter/Patti Young		
Attorney Docket Number:		0365-0601PUS3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Petition fee- 37 CFR 1.17(h) (Group III)	1464	1	130	130
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				940

Electronic Acknowledgement Receipt	
EFS ID:	9159887
Application Number:	11878557
International Application Number:	
Confirmation Number:	8440
Title of Invention:	METHOD FOR EMBEDDING A COMPONENT IN A BASE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Michael Keith Mutter/Patti Young
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0601PUS3
Receipt Date:	04-JAN-2011
Filing Date:	25-JUL-2007
Time Stamp:	14:42:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 940
RAM confirmation Number	851
Deposit Account	022448
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20110104RCEPetWD.pdf	3032680	yes	5
			8baa5ccf477500941f13367233d4842d133b0f27		
	Multipart Description/PDF files in .zip description				
	Document Description		Start		End
	Miscellaneous Incoming Letter		1		1
	Request for Continued Examination (RCE)		2		2
	Petition to Withdraw from Issue		3		4
	Miscellaneous Incoming Letter		5		5
Warnings:					
Information:					
2		20110104IDS.pdf	2719933	yes	6
			0c197e09d66c33835da3d81b785495759b22bcd6		
	Multipart Description/PDF files in .zip description				
	Document Description		Start		End
	Transmittal Letter		1		5
	Information Disclosure Statement (IDS) Filed (SB/08)		6		6
Warnings:					
Information:					
3	NPL Documents	EPReference.pdf	2941734	no	7
			c3542c86fda7ff1542e0df433ec1ecb1ddcb5560		
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	32334	no	2
			a241933879aa02b2adcfcc2425a33b19f0b0a1814		
Warnings:					
Information:					
Total Files Size (in bytes):			8726681		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Effective on 12/02/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2009		Complete if Known Application Number: 11/878,557 Conf. No.: 8440 Filing Date: July 25, 2007 First Named Inventor: Risto TUOMINEN Examiner Name: M. L. Diallo Art Unit: 2895 Attorney Docket No.: 0365-0601PUS3	
☐ Applicant claims small entity status. See 37 CFR 1.27			
TOTAL AMOUNT OF PAYMENT (\$) 940.00			

METHOD OF PAYMENT (check all that apply)

☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2538.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

Total Claims **Extra Claims** **Fee (\$)** **Fee Paid (\$)**
 _____ - 20 or HP = _____ x _____ = 0.00
 HP = highest number of total claims paid for, if greater than 20.

Indep. Claims **Extra Claims** **Fee (\$)** **Fee Paid (\$)**
 _____ - 3 or HP = _____ x _____ = 0.00
 HP = highest number of independent claims paid for, if greater than 3.

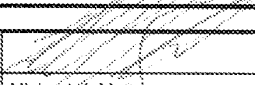
3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
_____ - 100 = _____	_____ / 50 = _____	_____ (round up to a whole number) x _____	_____	0.00

4. OTHER FEE(S)

	Fees Paid (\$)
Non-English Specification, \$130 fee (no small entity discount)	
Other (e.g., late filing surcharge), 1464 - Petition Fee: \$130 / 1801 - RCE Filing Fee: \$810	940.00

SUBMITTED BY		Registration No. 29680	Telephone 703-205-8000
Signature		(Attorney/Agent)	
Name (Print/Type)	Michael K. Mutter	Date	January 4, 2011

This collection of information is required by 37 CFR 1.126. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing this form, call 1-800-PTO-9199 and select option 2.

cef



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	01/18/2011	7872342	0365-0601PUS3	8440

2292 7590 12/28/2010
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 715 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Risto Tuominen, Helsinki, FINLAND;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use block 1 for any change of address)

2292 7390 10/07/2010

BIRCH STEWART KOLASCH & BIRCH, LLP
 PO BOX 747
 FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	G365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPL. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE PAID
nonprovisional	NO	\$1510	\$300	\$0	\$1810	12/07/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
DIALLO, MAMADOU L.	2895	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Birch, Stewart, Kolasch & Birch, LLP

2.

3.

3. ASSIGNED NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Imbera Electronics Oy

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Espoo, Finland

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies:

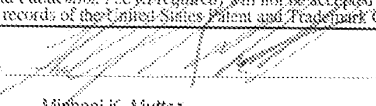
4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number G2-2448 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature: 

Date: December 7, 2010

Typed or printed name: Michael K. Mutter

Registration No.: 29,680

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		11878557		
Filing Date:		25-Jul-2007		
Title of Invention:		METHOD FOR EMBEDDING A COMPONENT IN A BASE		
First Named Inventor/Applicant Name:		Risto Tuominen		
Filer:		Michael Keith Mutter/Patti Young		
Attorney Docket Number:		0365-0601PUS3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt	
EFS ID:	8984993
Application Number:	11878557
International Application Number:	
Confirmation Number:	8440
Title of Invention:	METHOD FOR EMBEDDING A COMPONENT IN A BASE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Michael Keith Mutter/Patti Young
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0601PUS3
Receipt Date:	07-DEC-2010
Filing Date:	25-JUL-2007
Time Stamp:	16:53:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1810
RAM confirmation Number	3634
Deposit Account	022448
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20101207IssueFee.pdf	2855603 b1f372bfbffa299b32c8dd5e56ec4e3f03c9ba28	yes	5
Multipart Description/PDF files in .zip description					
	Document Description	Start	End		
	Miscellaneous Incoming Letter	1	4		
	Issue Fee Payment (PTO-85B)	5	5		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32061 caeb6fc150c75fdc2929922322f56a63152fe0f5	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2887664		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

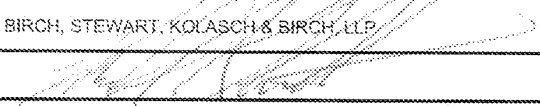
Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/R21 (07-09)
Approved for use through 07/31/2012. OMB 0851-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	11/878,557	Conf. No.: 8440
	Filing Date	July 25, 2007	
	First Named Inventor	Risto TUOMINEN	
	Art Unit	2895	
	Examiner Name	M. L. Diallo	
Total Number of Pages in This Submission	Attorney Docket Number	0365-0601PUS3	

ENCLOSURES (Check all that apply)		
☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ Alter Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Issue Fee Transmittal and Comments on Statement of Reasons for Allowance
Remarks		
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm Name	BIRCH, STEWART, KOLASCH & BIRCH, LLP	
Signature		
Printed name	Michael K. Mutter	
Date	December 7, 2010	Reg. No. 29,580

CERTIFICATE OF TRANSMISSION/MAILING		
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:		
Signature		
Typed or printed name		Date

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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MS Issue Fee
PATENT
0365-0601PUS3

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant:	Risto Tuominen	Conf.:	8440
Appl. No.:	11/878,557	Group:	2895
Filed:	July 25, 2007	Examiner:	Mamadou L Diallo
For:	METHOD FOR EMBEDDING A COMPONENT IN A BASE		

MS Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The comments attached herewith do not cause substantial interference and delay in the patent issue process and therefore cannot be considered a “failure to engage in reasonable efforts” to conclude processing or examination of the application. Accordingly, the submission of said comments must not result in a reduction of the patent term adjustment of 538 days pursuant to 37 C.F.R. § 1.704(c)(10). See O.G. 26 June 2001, lines 38-53.

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Applicant is appreciative of the Notice of Allowance papers dated September 7, 2010. Applicant offers the following comments regarding these documents.

In the Reasons for Allowance, the Examiner listed (page 3 of the Notice of Allowability) independent claims 1, 15 and 32 in connection with claim language which does not appear in each of these claims. Thus, Applicant would like to point out that claim 1 recites:

“a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the

second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.”

Applicant would also like to point out that claim 15 recites:

“a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers”

Finally, claim 32 recites:

“a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface,

a filler material in the hole between the metal foil and the microcircuit,

a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.”

Applicant respectfully notes that invention is defined by all of the allowed claims, which stand upon their own recitations, and limitations should not be imputed to any of the claims based upon the statement of Reasons for Allowance. Moreover, Applicant respectfully reserves his right to argue alternative interpretations and additional patentable distinctions of the claimed invention over any alleged prior art, should that need ever arise, and do not necessarily agree with any characterization of the invention and/or advantages thereof expressed by the Examiner.

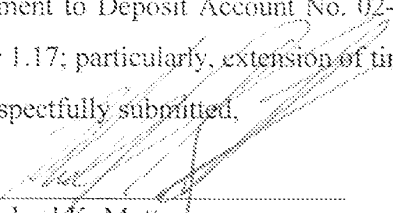
If the Examiner has any questions concerning this application, the Examiner is requested to contact Corina E. Tanasa, Registration No. 64,042, at telephone number (703) 208-4003, located in the Washington, DC area.

Application No. 11/878,557

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: December 7, 2010

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29,680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road

Suite 100 East

P.O. Box 747

Falls Church, Virginia 22040-0747

(703) 205-8000

Attorney for Applicant



UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

2292 7590 09/07/2010

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

DIALLO, MAMADOUL

ART UNIT

PAPER NUMBER

2895

DATE MAILED: 09/07/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	12/07/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 09/07/2010

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440

TITLE OF INVENTION: METHOD FOR EMBEDDING A COMPONENT IN A BASE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	12/07/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
DIALLO, MAMADOU L	2895	257-774000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440
2292	7590	09/07/2010	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			DIALLO, MAMADOU L	
			ART UNIT	PAPER NUMBER
			2895	
DATE MAILED: 09/07/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 538 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 538 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Corina Tanasa on August 27, 2010.

The application has been amended as follows:

Claim 1, line 14(last line of the claim), delete all and replace with -- least one second conductive pattern layer or layers. --;

Claim 14, line 2, after "conductive" delete "patterns" and replace with – pattern layers --;

Claim 15, line 16(last line of the claim), delete all and replace with – least one second conductive pattern layer or layers.--;

Claim 20, line 13(last line of the claim), delete all and replace with – least one second conductive pattern layer or layers.--;

Claim 21, line 15(last line of the claim), delete all and replace with – least one second conductive pattern layer or layers.-- and,

Claim 32,line 17(last line of the claim), delete all and replace with – least one second conductive pattern layer or layers. -- .

Remarks

The above changes have been made to clarify the connections by the thru conductors to the second conductive pattern layer or layers.

Allowable Subject Matter

Claims 1, 15 and 32 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest, singularly or in combination, at least the limitations of the independent claim 1, 15, and 32 including "a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface, a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern."

Because no reference alone, nor is there any motivation to combine the details over the prior art to create such limitations in these independent claims, the claims are deemed patentable over the prior art.

Claims 2-14, 16-31 and 32-36 are also allowed as being directly or indirectly dependent of the allowed base claim(s).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAMADOU DIALLO whose telephone number is (571)270-5449. The examiner can normally be reached on 9:30- 6:30 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. D./
Examiner, Art Unit 2895

/Matthew S. Smith/
Supervisory Patent Examiner, Art
Unit 2823

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"US 20080036093"	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/02/26 10:40
S2	25	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "4246595" "5162613" "5208188" "5216806" "5637919" "6038133" "6154366" "6271469" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596"). PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:44
S3	28	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "5162613" "5208188" "5216806" "5248852" "5497033" "5637919" "6038133" "6154366" "6271469" "6284564" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596"). PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:46
S4	25089	circuit board with (components or chip) with (in or inside)	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:03
S5	67	circuit board with (components or chip) with (in or inside)with insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:04

S6	18	electronic with embed\$4 with printed circuit same insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:09
S7	424	electronic with embed\$4 with printed circuit	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:10
S8	2	("20050048759" "20060068332").PN. OR ("7653991").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:20
S9	16	("20020071256" "20020118523" "20030000737" "3857683" "5243320" "5683928" "6021050" "6225570" "6288905" "6356455" "6717071" "6757178" "6806428" "6876091").PN. OR ("7190592").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:22
S10	1	"20020132096"	US-PGPUB; USPAT	ADJ	ON	2010/02/26 14:37
S11	1	("20070018203").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/01 14:19
S12	24	("20010054758" "20020020898" "20020063342" "20020127770" "5102829" "5227338" "5970321" "6015722" "6100108" "6495394" "6521530" "6607943"). PN.	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:30
S13	5434	((438/107,118,126) or (2571/e23.005,e23.126, e23.128,e23.182,e21.5, e21.503,e21.505,e21.511)). CCLS.	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:41
S14	52	((438/107,118,126) or (2571/e23.005,e23.126, e23.128,e23.182,e21.5, e21.503,e21.505,e21.511)). CCLS. and (hardened with insulating)	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:42
S15	133	((438/107,118,126) or (257/ e23.005,e23.126,e23.128, e23.182,e21.5,e21.503, e21.505,e21.511)).CCLS. and (hardened with insulating)	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/08/19 11:44

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L1	6	insulat\$5 same harden\$5 same polymer same open \$5 same metal same electrical	US-PGPUB; USPAT; UPAD	ADJ	ON	2010/08/19 13:05
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8/ 19/ 2010 1:12:56 PM**C:\ Documents and Settings\ mdiallo\ My Documents\ EAST\ Workspaces\ 11878557.wsp**

Search Notes 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

SEARCHED			
Class	Subclass	Date	Examiner
257	793,774,700,	2/27/2010	MD
257	257/e23.005,e23.126,e23.128,e23.182,e21.5,e21.503,e21.505,e21.511	8/19/2010	MD
438	107,118,126	8/19/2010	MD

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see attached interference search	8/19/2010	MD

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Issue Classification 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
257		687				H	0	1	L	21 / 52 (2006.0)								
CROSS REFERENCE(S)						H	0	1	L	21 / 60 (2006.0)								
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
257	774	E23.005	E21.503	678	684													

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	33	33										
2	2	18	18	34	34										
3	3	19	19	35	35										
4	4	20	20	36	36										
5	5	21	21												
6	6	22	22												
7	7	23	23												
8	8	24	24												
11	9	25	25												
12	10	26	26												
9	11	27	27												
13	12	28	28												
10	13	29	29												
14	14	30	30												
15	15	31	31												
16	16	32	32												

/MAMADOU DIALLO/ Examiner.Art Unit 2895 (Assistant Examiner)	08/19/2010 (Date)	Total Claims Allowed: 36	
/Matthew S Smith/ Supervisory Patent Examiner.Art Unit 2823 (Primary Examiner)	08/26/2010 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4D

<i>Index of Claims</i> 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	02/27/2010	08/19/2010												
1	1	✓	=												
2	2	✓	=												
3	3	✓	=												
4	4	✓	=												
5	5	✓	=												
6	6	✓	=												
7	7	✓	=												
8	8	✓	=												
11	9	✓	=												
12	10	✓	=												
9	11	✓	=												
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31	31	✓	=												
32	32	✓	=												
33	33	✓	=												
34	34	✓	=												
35	35	✓	=												
36	36	✓	=												

Docket No.: 0365-0601PUS3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto Tuominen.

Application No.: 11/878,557

Confirmation No.: 8440

Filed: July 25, 2007

Art Unit: 2895

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner: Mamadou L Diallo

REPLY UNDER 37 C.F.R. § 1.111

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated March 17, 2010 please amend the above-identified U.S. patent application as follows:

A Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Original) A circuit board comprising
an insulating material layer having a first side and a second side,
at least one first conductive pattern layer on the first side of the insulating material layer,
at least one of the first conductive pattern layers defining a first metal plate,
at least one second conductive pattern layer on the second side of the insulating material
layer, at least one of the second conductive pattern layers defining a second metal plate,
a component inside the insulating material layer and between the first and second metal
plates, the component having a first surface facing towards the second metal plate, and contact
areas on the first surface,
a hardened insulating polymer layer between the first surface of the component and at
least one conductive pattern of said at least one second conductive pattern layer, and
contact openings in the hardened insulating polymer layer and conductors in the contact
openings for forming electrical contacts between the contact areas of the component and the at
least one conductive pattern.
2. (Original) The circuit board of claim 1, wherein the first and second metal plates are
electrically connected to each other.
3. (Original) The circuit board of claim 1, wherein the first and second metal plates are
electrically connected to an earth connection of the circuit board.
4. (Original) The circuit board of claim 1, wherein the component is located in a hole in
the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of
the hole and a filler material in the hole between the metal foil and the component.
5. (Original) The circuit board of claim 4, wherein the metal foil is electrically connected

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to at least one of the first and second metal plates.

6. (Original) The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

7. (Original) The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that

the side-surfaces of the component face towards the metal foil,
the first surface of the component face towards the second metal plate, and
the second surface of the component face towards the first metal plate.

8. (Original) The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

9. (Original) The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

10. (Currently Amended) The circuit board ~~boar~~ of claim 1, wherein the hardened insulating polymer layer contains epoxy.

11. (Original) The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

12. (Original) The circuit board of claim 1, wherein the component is a microcircuit.

13. (Original) The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole

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and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.

14. (Original) The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

15. (Original) A multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises

- an insulating material layer having a first side and a second side,
- at least one first conductive pattern layer on the first side of the insulating material layer,
- at least one of the conductive pattern layers defining a first metal plate,
- at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
- a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,
- a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
- contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

16. (Original) The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.

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17. (Original) The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.

18. (Currently Amended) The multi-layered ~~multi-layered~~ circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.

19. (Original) The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

20. (Original) The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises

an insulating material layer having a first side and a second side,

at least one first conductive pattern layer on the first side of the insulating material layer,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

a component inside the insulating material layer and having a first surface facing towards the second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

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21. (Original) The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises

- an insulating material layer having a first side and a second side,
- at least one first conductive pattern layer on the first side of the insulating material layer,
- at least one of the first conductive pattern layers defining a first metal plate,
- at least one second conductive pattern layer on the second side of the insulating material layer,

- a component inside the insulating material layer, the component having first surface and a second surface on the opposite sides of the component and contact areas on the first surface, the second surface facing towards the first metal plate,

- a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

- contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

22. (Original) The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.

23. (Original) The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.

24. (Original) The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.

25. (Original) The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.

26. (Original) The multi-layered circuit board of claim 15, wherein the first and second

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metal plates are electrically connected to each other.

27. (Original) The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.

28. (Original) The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.

29. (Original) The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

30. (Original) The multi-layered circuit board of claim 15, wherein the component is a microcircuit.

31. (Original) The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.

32. (Original) An electronic module comprising
an insulating material layer having a first side and a second side,
at least one first conductive pattern layer on the first side of the insulating material layer,
at least one of the first conductive pattern layers defining a first metal plate,
at least one second conductive pattern layer on the second side of the insulating material layer,
at least one of the second conductive pattern layers defining a second metal plate,
a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates,
a metal foil covering the sidewalls of the hole,

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a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface,

a filler material in the hole between the metal foil and the microcircuit,

a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one conductive pattern.

33. (Original) The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.

34. (Original) The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.

35. (Original) The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.

36. (Original) The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.

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REMARKS

Claims 1-36 are currently pending in the application; with claims 1, 15 and 32 being independent. Claims 1-36 were pending prior to the Office Action.

Claims 10 and 18 have been amended only for clarification (to correct two typos), without narrowing their scope. The amendments to claims 10 and 18 were not made to overcome any statutory rejection.

The Examiner is respectfully requested to reconsider the rejections in view of the remarks set forth herein. Applicant respectfully requests favorable consideration thereof in light of the comments contained herein, and earnestly seeks timely allowance of the pending claims.

Claim Rejections – 35 USC §102 and §103

The Examiner rejected claims 1-36 under 35 U.S.C. § 102(b) as being anticipated, or, in the alternative, under 35 U.S.C. § 103(a) as being made obvious by US 2002/0132096 ("Takeuchi et al.").

These rejections are respectfully traversed.

To establish a *prima facie* case of anticipation or obviousness, the Examiner has the burden of meeting the basic criterion that the prior art must teach or suggest all of the claim limitations. Regarding this basic criterion, the Applicant submits that Takeuchi does not disclose or suggest all features of each of the independent claims 1, 15 and 32, as explained in detail below.

Takeuchi describes a wiring board in which electronic components are embedded by use of an embedding resin having a dielectric constant of less than or equal to about 5. The embedding resin preferably contains carbon black in an amount of less than or equal to about 1.4 mass %, and preferably contains at least a thermosetting resin and at least one inorganic filler (Abstract).

In the Office Action, the Examiner alleges that Figs. 12-13 and 19-24 of Takeuchi illustrate a circuit board as recited in the independent claims, and that layers 700 and 240 are first and second metal plates.

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Applicant submits that the Examiner's description of layer 240 is not accurate. Element 240 in the figures of Takeuchi is not a metal layer but a *solder resist layer* (see paragraph [0085]). The term solder resist does not mean that the layer is made of solder but refers to the function of the resist layer in the later defined step of forming the solder bumps (see e.g. paragraph [0086]). Paragraph [0085] explicitly states that:

"A dry film, which is to serve as a solder resist layer, is laminated on the outermost surface of the wiring substrate, and a mounting pattern of a semiconductor element is formed on the dry film through exposure and development, to thereby form a solder resist layer 210."

Thus, the element 240 is a layer of photo-definable polymer, so-called photo-resist, and is not made of metal.

Takeuchi discloses copper layers 200 and 700. However, none of the discussed embodiments (Figs. 12-13, 19-24) of Takeuchi fulfils all the features of claim 1 in which the recited circuit board comprises:

"at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface."

Only figures 24 and 25 of Takeuchi depict final products having conductive pattern layers on a first side of an insulating material layer and on a second side of the insulating material layer. However, these products do not have a component between the first and second metal plates and having a first surface facing towards the second metal plate.

The Examiner appears to think that Fig. 22 of Takeuchi, for instance, discloses a component 130 between the first and second metal plates 700. However, Fig. 22 shows only an intermediate phase of the manufacturing process and not the final product (see the description of Figs. 13-24 at paragraphs [0032]-[0043] which explain that these figures represent intermediate

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steps in the manufacturing of the wiring board of Fig. 25), therefore not qualifying as a circuit board within the meaning of claim 1. Specifically, this intermediate product fails to possess the following features of claim 1:

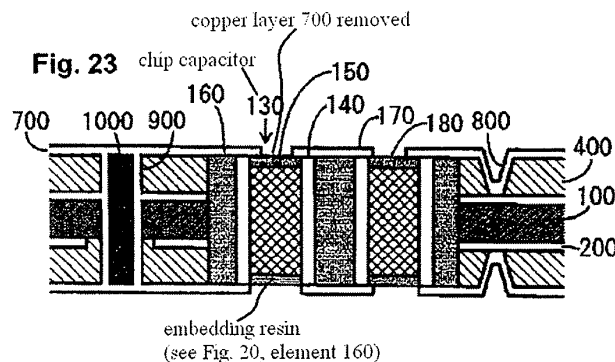
“at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate, [...]

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.”

In Fig. 23 of Takeuchi, the intermediate product is shown after patterning of the copper layers. After this process step, Takeuchi et al. does not any more disclose the wiring layers 700 to have metal plates. As explained at paragraph [0084], a resist layer is used in Fig. 22 to form a predetermined wiring pattern as shown in Fig. 23 (reproduced below for Examiner's convenience), whereby the copper layer 700 has been removed from the area above and below the chip capacitors 130 (which the Examiner considers to be the claimed components). The patterning of the copper layers (for example, of copper foil 200) is described by reference to Fig. 13 and paragraph [0075].



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Applicant also notes that in Figs. 24 and 25 layers 700 *cannot be continuous films* (i.e., Figs. 24 and 25 cannot be modified to have a continuous film 700), because if the layers 700 were continuous films extending over the capacitors 130, the electrodes 140 of the capacitors 130 would be short-circuited via the layers 700 and the through hole conductor 900.

Therefore, with respect to claim 1, Takeuchi fails to teach or suggest a final circuit board comprising:

- “at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
- at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
- a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface.”

Applicant points out that, per MPEP § 2131, “a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). For anticipation, “The identical invention must be shown in as complete detail as is contained in the ... claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). MPEP § 2131.02.

Takeuchi does not, expressly or inherently, disclose each and every element as set forth in claim 1. Thus, Takeuchi does not anticipate claim 1. Takeuchi also does not make claim 1 obvious because Takeuchi does not teach or suggest all of the claim limitations.

In addition, the circuit board of claim 1 can be used as a protective shield against electromagnetic interference. Takeuchi cannot achieve the advantages of the claimed circuit board, since Takeuchi fails to disclose or suggest a structure that can be used as a protective shield against electromagnetic interference.

With respect to independent claim 15, Takeuchi fails to teach or suggest, at least:

“A multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises [...]

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at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the conductive pattern layers defining a first metal plate,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface.”

With respect to independent claim 32, Takeuchi fails to disclose or suggest an electronic module comprising “at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate” and “at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate.” Takeuchi also fails to teach or suggest an electronic module comprising a microcircuit inside a hole which has sidewalls that are covered by a metal foil. In addition, Takeuchi fails to teach or suggest a microcircuit inside a hole and having a first surface facing towards the second metal plate, and contact areas on the first surface.

The electronic module of claim 32 can be used as a protective shield against electromagnetic interference. Takeuchi fails to disclose or suggest a structure that can be used as a protective shield against electromagnetic interference.

Furthermore, the circuit boards of claims 1 and 15 and the electronic module 32 cannot be made obvious by Takeuchi, as it would not be obvious to modify the process of Takeuchi such that isolated features present in the intermediate phases of the described process and serving their planned purpose would suddenly, with absolutely no motivation in Takeuchi, be shifted to another place in the final product. Furthermore, Takeuchi completely fails to disclose the interference protection around the embedded components.

For all of the above reasons, taken alone or in combination, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. §102 and §103 rejections of claims 1, 15 and 32. Claims 1-14 depend from claim 1 and are allowable at least by virtue of their dependency. Claims 16-31 depend from claim 15 and are allowable at least by virtue of their

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dependency. Claims 33-36 depend from claim 32 and are allowable at least by virtue of their dependency.

CONCLUSION

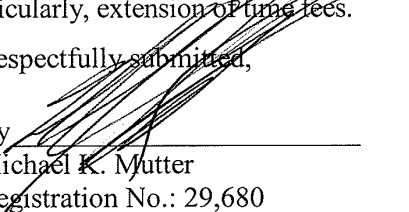
In view of the above remarks, this application appears to be in condition for allowance and the Examiner is, therefore, requested to reexamine the application and pass the claims to issue.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Corina E. Tanasa, Registration No. 64,042, at telephone number (703) 208-4003, located in the Washington, DC area, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: June 17, 2010

Respectfully submitted,

By 
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af

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Electronic Acknowledgement Receipt	
EFS ID:	7839500
Application Number:	11878557
International Application Number:	
Confirmation Number:	8440
Title of Invention:	Method for embedding a component in a base
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Michael Keith Mutter/Ruth Calendine
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0601PUS3
Receipt Date:	17-JUN-2010
Filing Date:	25-JUL-2007
Time Stamp:	17:45:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20100617AMENDMENT.PDF	715991 924644c1018a696dc5bbc119a0446a6bbb db4b86	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Claims	3	9
	Applicant Arguments/Remarks Made in an Amendment	10	15
Warnings:			
Information:			
Total Files Size (in bytes):		715991	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

AMENDMENT TRANSMITTAL LETTER				Docket No. 0365-0601PUS3	
Application No. 11/878,557 - Conf. #8440	Filing Date July 25, 2007	Examiner M. L. Diallo	Art Unit 2895		
Applicant(s): Risto TUOMINEN					
Invention: METHOD FOR EMBEDDING A COMPONENT IN A BASE					
Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-145 Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.					
CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	36	- 36 =	0	x 52.00	0.00
Independent Claims	3	- 3 =	0	x 220.00	0.00
Multiple Dependent Claims (check if applicable) ☐					0.00
Other fee (please specify):					0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00
☐ Large Entity ☐ Small Entity ☐ No additional fee is required for this amendment. ☐ Please charge Deposit Account No. <u>02-2448</u> in the amount of \$ _____. A duplicate copy of this sheet is enclosed. ☐ A check in the amount of \$ _____ is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☒ The Director is hereby authorized to charge and credit Deposit Account No. <u>02-2448</u> as described below. ☒ Credit any overpayment ☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.					
 Michael K. Mutter Attorney Reg. No.: 29,680				Dated: <u>June 17, 2010</u>	
BIRCH, STEWART, KOLASCH & BIRCH, LLP 8110 Gatehouse Road, Suite 100 East P.O. Box 747 Falls Church, VA 22040-0747 United States 703-205-8000					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/878,557		Filing Date 07/25/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR	X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =			X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR OTHER THAN SMALL ENTITY	
AMENDMENT	06/17/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 36	Minus	** 36	= 0	X \$ =		OR	X \$52=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/KAREN T. WASHINGTON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3	8440
2292 7590 03/17/2010 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			EXAMINER DIALLO, MAMADOUL	
			ART UNIT 2895	PAPER NUMBER
			NOTIFICATION DATE 03/17/2010	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.		Applicant(s)	
	11/878,557		TUOMINEN, RISTO	
	Examiner		Art Unit	
	MAMADOU DIALLO		2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 25 July 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-36 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>07/25/2007</u> .	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 07/25/2007 is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-36 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Takeuchi et al, US Patent Publication No.2002/013096 A1.

Pertaining to claim 1, Takeuchi teaches a circuit board comprising an insulating material layer[100] having a first side and a second side, at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate (see fig.12-13 and 19-24), at least one second conductive pattern layer on the second side of the insulating material layer,

at least one of the second conductive pattern layers defining a second metal plate (see fig.12-13 and 19-24), a component[130] inside the insulating material layer and between the first and second metal plates (see fig.19), the component having a first surface facing towards the second metal plate, and contact areas on the first surface, a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern(see figs.24-25).

Pertaining to claim 2, Takeuchi teaches the circuit board of claim 1, wherein the first and second metal plates [700,240] are electrically connected to each other.

Pertaining to claim 3, Takeuchi teaches the circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board (circuit board property)

Pertaining to claim 4, Takeuchi teaches The circuit board of claim 1, wherein the component [130] is located in a hole in the insulating material layer[100], and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material[160] in the hole between the metal foil and the component(see fig.22).

Pertaining to claim 5, Takeuchi teaches the circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.

Pertaining to claim 6, Takeuchi teaches the circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board (circuit board property).

Pertaining to claim 7, Takeuchi teaches The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate(see figs.1-24).

Pertaining to claim 8, Takeuchi teaches the circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer (see para [0094]).

Pertaining to claim 9, Takeuchi teaches The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper(see Para[0032; 0078-0079]).

Pertaining to claim 10, Takeuchi teaches the circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy (see para [0016, 0076]).

Pertaining to claim 11, Takeuchi teaches the circuit board of claim 8, wherein the baseboard is a glass-fiber reinforced epoxy board (see para [0045 and 0076]).

Pertaining to claim 12, Takeuchi teaches the circuit board of claim 1, wherein the component is a microcircuit [130]).

Pertaining to claim 13, Takeuchi teaches The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component (see figs.20).

Pertaining to claim 14, Takeuchi teaches The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material • layer(see fig.14,19).

Pertaining to claim 15-17 Takeuchi teaches A multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises an insulating material layer[100] having a first side and a second side, at least one first conductive pattern layer on the first side of the insulating material layer[200], at least one of the conductive pattern layers[700],240] defining a first metal plate, at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate, a component [130] inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface, a hardened insulating polymer layer[190] between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and contact openings in the hardened

Art Unit: 2895

insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern(see figs 24-25) wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.

Takeuchi does not teach a first circuit board substructure and second circuit board substructure on top of each other, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.

However It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and second circuit board substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art .St.Regis Paper Co.v.Bemis Co., 193USPQ8.

Pertaining to claim 18 Takeuchi teaches the multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component [130] embedded in the insulating material layer.

Pertaining to claim 19, Takeuchi teaches The multi-layered circuit board of claim 15, but did not teach wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit

such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

However It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and second circuit board substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art .St.Regis Paper Co.v.Bemis Co., 193USPQ8.

Pertaining to claim 20, Takeuchi teaches The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises an insulating material layer having a first side and a second side, at least one first conductive pattern layer on the first side of the insulating material layer, at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate, a component [130] inside the insulating material layer [100] and having a first surface facing towards the second metal plate, and contact areas on the first surface, a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern(see fig.25).

Pertaining to claim 21, Takeuchi teaches The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises an insulating material layer [100] having a first side and a second side, at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate, at least one second conductive pattern layer on the second side of the insulating material layer, a component inside the insulating material layer, the component [130] having first surface and a second surface on the opposite sides of the component and contact areas on the first surface, the second surface facing towards the first metal plate, a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component [130] and the at least one conductive pattern (see fig.25).

Pertaining to claim 22-24 Takeuchi teaches The multi-layered circuit board of claim 15, but does not teach the circuit comprising a third circuit board substructure on top of the first and second circuit board substructures, wherein the first circuit board substructure is between the second and third circuit board substructures or wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.

However It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and second circuit

board substructure and a third substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art .St.Regis Paper Co.v.Bemis Co., 193USPQ8.

Pertaining to claim 25-26, Takeuchi teaches the multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other (see fig.25).

Pertaining to claim 27, Takeuchi teaches The multi-layered circuit board of claim 15, wherein the component[130] is located in a hole in the insulating material layer[100], and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component(see fig.18-25).

Pertaining to claim 28, Takeuchi teaches the multi-layered circuit board of claim 15, wherein the metal foil [200] is electronically connected to at least one of the first and second metal plates.

Pertaining to claim 29, Takeuchi teaches the multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper (see para [0079]).

Pertaining to claim 30, Takeuchi teaches the multi-layered circuit board of claim 15, wherein the component [130] is a microcircuit.

Pertaining to claim 31, Takeuchi teaches the multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits [130] inside the insulating material layer (see fig.19).

Pertaining to claim 32, Takeuchi teaches An electronic module comprising an insulating material layer [100] having a first side and a second side, at least one first conductive pattern [200] layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate, at least one second conductive pattern [700 or 240] layer on the second side of the insulating material layer[100] , at least one of the second conductive pattern layers defining a second metal plate, a hole[110] having sidewalls defined in the insulating material layer and located between the first and second metal plates, a metal foil covering the sidewalls of the hole, a microcircuit [130] inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface, a filler material [160] in the hole between the metal foil and the microcircuit,[130] a hardened insulating polymer [190] layer between the first surface of the microcircuit [130] and at least one conductive pattern [240] of said at least one second conductive pattern layer, and contact openings (see fig.25) in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit[130] and the at least one conductive pattern.

Pertaining to claim 33, Takeuchi teaches the electronic module of claim 32, wherein the first and second metal plates [200,700 and 240] are electronically connected to each other.

Pertaining to claim 34, Takeuchi teaches the electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module (circuit board property).

Pertaining to claim 35, Takeuchi teaches The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal [700,240] plates(see fig.25).

Pertaining to claim 36, Takeuchi teaches the electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module (see fig 25 and circuit board property to have ground connection).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAMADOU DIALLO whose telephone number is (571)270-5449. The examiner can normally be reached on 9:30- 6:30 Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571)272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2895

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2895

/M. D./
Examiner, Art Unit 2895

Notice of References Cited	Application/Control No. 11/878,557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO	
	Examiner MAMADOU DIALLO	Art Unit 2895	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0132096 A1	09-2002	Takeuchi et al.	428/210
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

SEARCHED			
Class	Subclass	Date	Examiner
257	793,774,700	2/27/2010	MD

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	02/27/2010								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
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	33	✓								
	34	✓								
	35	✓								
	36	✓								

<i>Index of Claims</i> 	Application/Control No. 11878557	Applicant(s)/Patent Under Reexamination TUOMINEN, RISTO
	Examiner MAMADOU DIALLO	Art Unit 2895

✓	Rejected
=	Allowed

-	Cancelled
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A	Appeal
O	Objected



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BIB DATA SHEET

CONFIRMATION NO. 8440

SERIAL NUMBER 11/878,557	FILING or 371(c) DATE 07/25/2007 RULE	CLASS 438	GROUP ART UNIT 2895	ATTORNEY DOCKET NO. 0365-0601PUS3		
APPLICANTS Risto Tuominen, Helsinki, FINLAND; ** CONTINUING DATA ***** This application is a CON of 10/502,336 09/23/2004 PAT 7,294,529 ** FOREIGN APPLICATIONS ***** FINLAND 20020191 01/31/2002 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/14/2007						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /MAMADOU L DIALLO/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 12	TOTAL CLAIMS 36	INDEPENDENT CLAIMS 3
ADDRESS BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747 UNITED STATES						
TITLE Method for embedding a component in a base						
FILING FEE RECEIVED 1800	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
			☐ Credit			

Receipt date: 07/25/2007

11878557 - GAU: 2895

Used in Lieu of PTO/SB/08A/B
(Based on PTO 04-07 version)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	NEW
				Filing Date	July 25, 2007
				First Named Inventor	Risto TUOMINEN
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	0365-0601PUS3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
	BA	JP-2002-016327-A	01-18-2002		

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Examiner Signature	/Mamadou Diallo/	Date Considered	02/26/2010
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Birch, Stewart, Kolasch & Birch, LLP

MKM/STW/ta

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Receipt date: 07/25/2007

11878557 - GAU: 2895

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(Based on PTO 04-07 version)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	NEW
				Filing Date	July 25, 2007
				First Named Inventor	Risto TUOMINEN
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	0365-0601PUS3

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Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	PATENT ABSTRACTS OF JAPAN, vol. 2002, no 05, May 3, 2002.	

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Examiner Signature	/Mamadou Diallo/	Date Considered	02/26/2010
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Birch, Stewart, Kolasch & Birch, LLP

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"US 20080036093"	US-PGPUB; USPAT; USOCR; DERWENT	ADJ	ON	2010/02/26 10:40
S2	25	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "4246595" "5162613" "5208188" "5216806" "5637919" "6038133" "6154366" "6271469" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596").PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:44
S3	28	("20020117743" "20020185303" "20030068852" "20030100142" "20030137045" "20040266067" "20050285244" "20060105500" "4246595" "5162613" "5208188" "5216806" "5248852" "5497033" "5637919" "6038133" "6154366" "6271469" "6284564" "6292366" "6475877" "6489685" "6537848" "6538210" "6607943" "6710458" "6790712" "6979596"). PN.	US-PGPUB; USPAT	ADJ	ON	2010/02/26 11:46

S4	25089	circuit board with (components or chip) with (in or inside)	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:03
S5	67	circuit board with (components or chip) with (in or inside)with insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:04
S6	18	electronic with embed \$4 with printed circuit same insulator	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:09
S7	424	electronic with embed \$4 with printed circuit	US-PGPUB; USPAT	ADJ	ON	2010/02/26 12:10
S8	2	("20050048759" "20060068332").PN. OR ("7653991").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:20
S9	16	("20020071256" "20020118523" "20030000737" "3857683" "5243320" "5683928" "6021050" "6225570" "6288905" "6356455" "6717071" "6757178" "6806428" "6876091").PN. OR ("7190592").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/02/26 12:22
S10	1	"20020132096"	US-PGPUB; USPAT	ADJ	ON	2010/02/26 14:37

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3

CONFIRMATION NO. 8440

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA22040-0747

Title: Method for embedding a component in a base

Publication No. US-2008-0036093-A1

Publication Date: 02/14/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Pre-Grant Publication Division, 703-605-4283



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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/878,557	07/25/2007	Risto Tuominen	0365-0601PUS3

CONFIRMATION NO. 8440

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA22040-0747

Date Mailed: 11/30/2007

NOTICE OF NEW OR REVISED PROJECTED PUBLICATION DATE

The above-identified application has a new or revised projected publication date. The current projected publication date for this application is 02/14/2008. If this is a new projected publication date (there was no previous projected publication date), the application has been cleared by Licensing & Review or a secrecy order has been rescinded and the application is now in the publication queue.

If this is a revised projected publication date (one that is different from a previously communicated projected publication date), the publication date has been revised due to processing delays in the USPTO or the abandonment and subsequent revival of an application. The application is anticipated to be published on a date that is more than six weeks different from the originally-projected publication date.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/878,557	07/25/2007	2823	1800	0365-0601PUS3	36	3

CONFIRMATION NO. 8440

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA22040-0747

FILING RECEIPT

Date Mailed: 08/15/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Risto Tuominen, Helsinki, FINLAND;

Power of Attorney: The patent practitioners associated with Customer Number 02292

Domestic Priority data as claimed by applicant

This application is a CON of 10/502,336 09/23/2004

Foreign Applications

FINLAND 20020191 01/31/2002

If Required, Foreign Filing License Granted: 08/14/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/878,557**

Projected Publication Date: 11/22/2007

Non-Publication Request: No

Early Publication Request: No

Title

Method for embedding a component in a base

Preliminary Class

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to

espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Docket No.: 0365-0601PUS3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto TUOMINEN

Application No.: NEW

Confirmation No.: N/A

Filed: July 25, 2007

Art Unit: N/A

For: METHOD FOR EMBEDDING A
COMPONENT IN A BASE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION WITH CONTINUATION-IN-PART OR RULE 1.53 (B))
CONTINUATION OR DIVISIONAL APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. **LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION**

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO-SB08(s), attached hereto.

II. **COPIES**

☐ a. Copies of cited U.S. patents and patent application publications are not included.
Copies of foreign patent documents and non-patent literature are included.

Application No.:

Docket No.: 0365-0601PUS3

☐ b. Some or all of the documents listed on the PTO-SB08 are not enclosed because they were cited in the International Search Report and copies should already be in the PTO file. If copies are needed, please contact the undersigned.

☒ c. REFERENCES PREVIOUSLY CITED OR SUBMITTED - Pursuant to 37 C.F.R. §1.98(d), consideration of information listed on the PTO-SB08 form(s) is requested since any patents, publications, or other information which are listed on the PTO-SB08 form(s) but for which copies are not enclosed herewith, were previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Appl. No(s) and U.S. Filing Date

10/502,336 filed September 23, 2004

III. CONCISE EXPLANATION OF THE RELEVANCE

(check at least one box)

☐ a. DOCUMENTS IN THE ENGLISH LANGUAGE - The patents, publications, or other information listed on the attached PTO SB08 are in the English language and therefore, do not require a statement of relevancy.

☐ b. DOCUMENTS NOT IN THE ENGLISH LANGUAGE - A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

☐ c. ENGLISH LANGUAGE SEARCH REPORT - An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

☐ d. OTHER - The following additional information is provided for the Examiner's consideration.

Application No.:

Docket No.: 0365-0601PUS3

IV. FEES (check one box)

☐ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

☒ b. This Information Disclosure Statement is being filed concurrent with the filing of a continuation-in-part, continuation, or divisional patent application; therefore, no fee is required.

☐ c. This Information Disclosure Statement is being filed within three months of the filing date of a national application (37 C.F.R. § 1.97(b)(1)). No fee or statement is required. *(This section is not to be used with RCE's.)*

☐ d. This Information Disclosure Statement is being filed within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or statement is required.

☐ e. This Information Disclosure Statement is being filed concurrently with the filing of a Request for Continued Examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.

☐ f. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or statement is required. In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) below, or, if no statement has been made, charge our deposit account for the fee as required by 37 C.F.R. § 1.17(p).

☐ g. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action under 37 C.F.R. § 1.113 (See 37 C.F.R. § 1.97(c)(1)) or before the mailing date of a Notice of Allowance under 37 C.F.R. § 1.311 (See 37 C.F.R. § 1.97(c)(2)).

☐ No statement; therefore, a fee as required by 37 C.F.R. § 1.17(p) is attached.

or

Application No.:

Docket No.: 0365-0601PUS3

☐ See the statement below. No fee is required.

V. STATEMENT UNDER 37 C.F.R. § 1.97(e)

(check only one box)

The undersigned hereby states that:

☐ a. **Each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than 30 days prior to the filing of this IDS; or**

☐ b. Each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS; or

☐ c. No item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.

☐ d. Some of the items of information were cited in a communication from a foreign Patent Office. As to this information, the undersigned states that each item of information contained in the IDS was first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby states that no item of this remaining information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application and, to the best of my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

VI. PAYMENT OF FEES (check one box)

Application No.:

Docket No.: 0365-0601PUS3

☐ The required fee is listed on the attached Fee Transmittal.

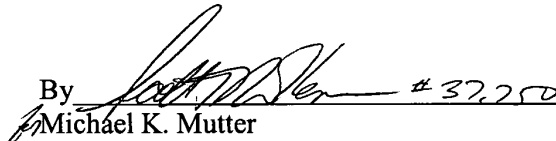
☒ No fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to our Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Dated: July 25, 2007

Respectfully submitted,

By  #37,250
Michael K. Mutter
Registration No.: 29,680
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

Attachment(s):

☒ PTO/SB/08

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	NEW
				Filing Date	July 25, 2007
				First Named Inventor	Risto TUOMINEN
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	1	of	2	Attorney Docket Number	0365-0601PUS3

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	US-4,246,595-A1	01-20-1981	Noyori et al.	
	AB*	US-2003/0068852-A1	04-10-2003	Towle et al.	
	AC*	US-2003/0137045-A1	07-24-2003	Sugaya et al.	
	AD*	US-6,038,133-A	03-14-2000	Nakatani et al.	
	AE*	US-6,154,366-A	11-28-2000	Ma et al.	
	AF*	US-6,271,469-B1	08-07-2001	Ma et al.	
	AG*	US-6,292,366-B1	09-18-2001	Platt	
	AH*	US-6,475,877-B1	11-05-2002	Saia et al.	
	AI*	US-6,489,685-B2	12-03-2002	Asahi et al.	
	AJ*	US-6,538,210-B2	03-25-2003	Sugaya et al.	
	AK*	US-2002/0117743-A1	08-29-2002	Nakatani et al.	
	AL*	US-2002/0185303-A1	12-12-2002	Takeuchi et al.	
	AM*	US-2006/0105500-A1	05-18-2006	Chang	
	AN*	US-5,216,806-A	06-08-1993	Lam	
	AO*	US-5,637,919-A	06-10-1997	Grabbe	
	AP*	US-2003/0100142-A1	05-29-2003	Shin et al.	
	AQ*	US-2004/0266067-A1	12-30-2004	Bai	
	AR*	US-2005/0285244-A1	12-29-2005	Chen	
	AS*	US-5,162,613-A	11-10-1992	Schoenthaler	
	AT*	US-5,208,188-A	05-04-1993	Newman	
	AU*	US-6,537,848-B2	03-25-2003	Camenforte et al.	
	AV*	US-6,607,943-B1	08-19-2003	Kinsman	
	AW*	US-6,710,458-B2	03-23-2004	Seko et al.	
	AX*	US-6,790,712-B2	09-14-2004	Bai et al.	
	AY*	US-6,979,596-B2	12-27-2005	Corisis et al.	
	AZ*	US-6,284,564-B1	09-04-2001	Balch et al.	
	AA1*	US-5,497,033-A	03-05-1996	Fillion et al.	
	AB1*	US-5,248,852-A	09-28-1993	Kumagai	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)			
	BA	JP-2002-016327-A	01-18-2002		

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
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Birch, Stewart, Kolasch & Birch, LLP

MKM/STW/ta

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	NEW
				Filing Date	July 25, 2007
				First Named Inventor	Risto TUOMINEN
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	0365-0601PUS3

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	PATENT ABSTRACTS OF JAPAN, vol. 2002, no 05, May 3, 2002.	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

Birch, Stewart, Kolasch & Birch, LLP

MKM/STW/ta

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 11878557			
Substitute for Form PTO-875									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	\$150	N/A	\$300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	\$250	N/A	\$500			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	\$100	N/A	\$200			
TOTAL CLAIMS (37 CFR 1.16(j))	36	minus 20 = 16	x \$25 =		x \$50 =	800			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 =	x \$100 =		x \$200 =				
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).		\$125		\$250				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180 =		+360 =				
			TOTAL		TOTAL	1800			
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(j))	Minus	**	=	x \$25 =	x \$50 =	x \$200 =		
	Independent (37 CFR 1.16(h))	Minus	***	=	x \$100 =	x \$200 =	x \$200 =		
	Application Size Fee (37 CFR 1.16(s))			\$125		\$250			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			+180 =		+360 =			
			TOTAL		TOTAL				
			ADD'L FEE		ADD'L FEE				
15 32									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(j))	Minus	**	=	x \$25 =	x \$50 =	x \$200 =		
	Independent (37 CFR 1.16(h))	Minus	***	=	x \$100 =	x \$200 =	x \$200 =		
	Application Size Fee (37 CFR 1.16(s))			\$125		\$250			
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			+180 =		+360 =			
			TOTAL		TOTAL				
			ADD'L FEE		ADD'L FEE				

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION SERIAL NO. _____

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET**

07/26/2007 SZEWDIE1 00000014 022448 11878557

01 FC:1011	300.00 DA
02 FC:1111	500.00 DA
03 FC:1311	200.00 DA
04 FC:1202	800.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002-489-267/69033

15992 U.S. PTO
072507

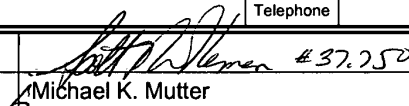
U.S. PTO
11/878557
07/25/2007

Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL (ONLY FOR NEW NONPROVISIONAL APPLICATIONS UNDER 37 CFR 1.53(B))		Attorney Docket No. 0365-0601PUS3 First Inventor Risto TUOMINEN Title METHOD FOR EMBEDDING A COMPONENT IN A BASE Express Mail Label No.	
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APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.		ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	
1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing) See 37 CFR 1.27. 2. ☐ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages <u>25</u>] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>12</u>] 5. Oath or Declaration [Total Sheets <u>2</u>] a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☐ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. - c. are required) a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies		ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee 10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney (when there is an assignee) 11. ☐ English Translation Document (if applicable) 12. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 13. ☐ Preliminary Amendment 14. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other:	

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: <u>10/502,336</u> Prior application information: Examiner <u>Matthew S. Smith</u> Art Unit: <u>2823</u>			
19. CORRESPONDENCE ADDRESS			
☒ The address associated with Customer Number: <u>02292</u> OR ☐ Correspondence address below			
Name: _____			
Address: _____			
City	State	Zip Code	
Country	Telephone	Email Address	
Signature: 		Date	July 25, 2007
Name (Print/Type): Michael K. Mutter		Registration No. (Attorney/Agent)	29,680

15992 U.S. PTO
072507

PTO/SB/17 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2007		Complete if Known <table border="1"> <tr> <td>Application Number</td> <td>NEW</td> </tr> <tr> <td>Filing Date</td> <td>July 25, 2007</td> </tr> <tr> <td>First Named Inventor</td> <td>Risto TUOMINEN</td> </tr> <tr> <td>Examiner Name</td> <td>Not Yet Assigned</td> </tr> <tr> <td>Art Unit</td> <td>N/A</td> </tr> <tr> <td>Attorney Docket No.</td> <td>0365-0601PUS3</td> </tr> </table>		Application Number	NEW	Filing Date	July 25, 2007	First Named Inventor	Risto TUOMINEN	Examiner Name	Not Yet Assigned	Art Unit	N/A	Attorney Docket No.	0365-0601PUS3
Application Number	NEW														
Filing Date	July 25, 2007														
First Named Inventor	Risto TUOMINEN														
Examiner Name	Not Yet Assigned														
Art Unit	N/A														
Attorney Docket No.	0365-0601PUS3														
☐ Applicant claims small entity status. See 37 CFR 1.27															
TOTAL AMOUNT OF PAYMENT	(\$)	1,800.00													

METHOD OF PAYMENT (check all that apply)

☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: Birch, Stewart, Kolasch & Birch,

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	1,000.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims **Extra Claims** **Fee (\$)** **Fee Paid (\$)**
 36 - 20 = 16 x 50.00 = 800.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims **Extra Claims** **Fee (\$)** **Fee Paid (\$)**
 3 - 3 = x =

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

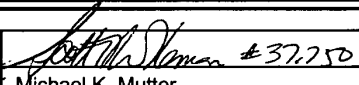
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
37	- 100 =	/50 =	(round up to a whole number) x	=

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): _____

SUBMITTED BY			
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METHOD FOR EMBEDDING A COMPONENT IN A BASE

[0001] This application is a Continuation of co-pending Application No. 10/502,336, filed on September 23, 2004, the entire contents of which are hereby incorporated by reference and for which priority is claimed under 35 U.S.C. § 120.

[0002] The present invention relates to a method for embedding one or more components in a base.

[0003] The bases that are processed using the methods to which the present invention relates are used as bases for electrical components, typically semiconductor components and particularly microcircuits, in electronic products. The task of the base is to provide a mechanical attachment base for the components and the necessary electrical connections to the other components on the base and outside the base. The base can be a circuit board, so that the method that is the object of the invention is closely related to circuit-board manufacturing technology. The base can also be some other base, for example, a base used for packaging a component or components, or the base of an entire functional module.

[0004] Circuit-board manufacturing technologies differ from microcircuit manufacture in, among other things, the fact that the substrate used in microcircuit manufacturing technologies is a semiconductor material, whereas the base material of a circuit board is an insulator. Microcircuit manufacturing technologies are also typically considerably more expensive than circuit-board manufacturing technologies.

[0005] Circuit-board manufacturing technologies differ from packaging techniques in that packaging techniques are intended to form a package around a semiconductor component, which will facilitate its handling. The surface of a package of a semiconductor component has contact parts, typically protrusions, which allow the packaged component to be easily installed on a circuit board. A semiconductor package also contains conductors, through which voltage can be connected to the actual

semiconductor, connecting the protruding contact parts outside the package to the contact areas on the surface of the semiconductor component.

[0006] However, the packages of components manufactured using conventional technologies take up a considerable amount of space. The miniaturization of electronic devices has led to an attempt to eliminate the packaging of semiconductor components. For this purpose, the so-called flip-chip technology for instance, has been developed, in which a semiconductor component without a package is assembled directly onto the surface of the circuit board. There are, however, many difficulties in flip-chip technology. For example, problems can arise with the reliability of connections, especially in applications in which mechanical stresses arise between the circuit board and the semiconductor component. Mechanical stresses must be evened by adding a suitable underfill between the chip and the circuit board. This procedure slows down the process and increases manufacturing costs. Stresses arise particularly in applications in which a flexible circuit board is used and the circuit board is flexed strongly.

[0007] Object of the invention is to create a method, by means of which unpacked microcircuits can be embedded to a base reliably but economically.

[0008] The invention is based on embedding the semiconductor components, or at least some of them, in a base, such as a circuit board, during the manufacture of the board, whereby part of the base structure is, as it were, manufactured around the semiconductor components. According to the invention, feed-throughs for semiconductor components are made in the base in such a way that the holes extend between the first and second surfaces of the base. After the holes have been made, a polymer film is spread over the second surface of the base structure in such a way that the polymer film also covers the feed-throughs made for the semiconductor components, from the second side of the base structure. Before the hardening of the polymer film, or after partial hardening, the semiconductor components are placed, from the direction of the first side of the base, in the holes that have been made. The semiconductor components are pressed against the polymer film so that they adhere to the polymer film. After this, the final hardening of the polymer film is carried out. According to the

invention, a conductive pattern is made in the base, before a component is placed in the holes, and the component is placed in the hole in such a way that the component is aligned in relation to the conductive patterns made on the baseboard.

[0009] More specifically, the method according to the invention is characterized by what is stated in the characterizing portion of Claim 1.

[0010] Considerable advantages are gained with the aid of the invention. This is because, with the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it. The invention also makes it possible to manufacture a small and reliable component package around a component.

[0011] The invention also permits a large number of embodiments, which provide significant additional advantages.

[0012] For example, with the aid of preferred embodiments of the invention, the component's packaging stage, the circuit board's manufacturing stage, and the assembly and contact-making stage of the semiconductor components can be combined to form a single totality. The combination of the various process stages brings important logistic benefits and permits the manufacture of a smaller and more reliable electronic module. There is the further advantage that such a manufacturing method can largely exploit circuit board manufacturing and assembly technologies that are in general use.

[0013] According to a preferred embodiment of the invention, the totality of the composite process is simpler than, for example, using flip-chip technology to manufacture a circuit board and attach the components to the circuit board. By means of such preferred embodiments, the following advantages over the conventional solution are obtained:

- Soldering is not required to form contacts with the components, instead an electrical contact can be manufactured by growing conductors on top of the contact areas of a semiconductor component. This means that there

is no need to use molten metal to connect the components, so that compounds are not formed between metals. Compounds between metals are generally brittle, so that reliability is improved compared to connections made by soldering. Particularly in small connections, the brittleness of the metal compounds in the connections causes great problems. According to a preferred embodiment, it is possible to achieve clearly smaller structures in a solderless solution than in soldered solutions. The solderless contact-making method also has the advantage that high temperatures are not required to form contacts. A lower process temperature permits greater choice when selecting other materials of the circuit board, the component package, or the electronics module. In the method, the temperature of the circuit board, the component, and the conductive layer directly connected to the component can be kept in the range 20 - 85°C. Higher temperatures, for example, of about 150°C, may be needed only when curing (polymerizing) the polymer films used. However, the temperature of the baseboard and the components can be kept under 200°C during the entire process. If the method employs polymer films that are hardened in other ways than due to the effect of a high temperature, for example, chemically, or by electromagnetic radiation, the temperature of the baseboard and the components can, in a preferred embodiment, be kept under 100°C during the entire process.

- Because the use of the method permits the manufacture of smaller structures, the components can be spaced more closely. The conductors between the components can then also be shorter while the electrical properties of the electronic circuit improve, for example, by reducing losses, interference, and delay times.
- The method also permits the manufacture of three-dimensional structures, as the bases and the components embedded in the bases can be assembled on top of each other.

- In the method, it is also possible to reduce the interfaces between different metals.
- The method permits a lead-free process.

[0014] The invention also permits other preferred embodiments. In connection with the invention, flexible circuit boards, for instance, can be used. Further, the process permits circuit boards to be assembled on top of each other.

[0015] With the aid of the invention, it is also possible to manufacture extremely thin structures, in which the semiconductor components are, despite its thinness, entirely protected within a base, such as a circuit board.

[0016] Because the semiconductor components can be placed entirely inside the circuit board, the joints between the circuit board and the semiconductor components are mechanically durable and reliable.

[0017] In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

[0018] Figure 1 shows a series of cross-sections of one process according to the invention.

[0019] Figure 2 shows a series of cross-sections of a second process according to the invention.

[0020] Figure 3 shows a schematic diagram of one possible contact-forming method.

[0021] Figure 4 shows a series of cross-sections of a third process according to the invention.

[0022] The series of illustrations shown in Figure 1 show one possible process according to the invention. In the following, the process of Figure 1 is examined in stages:

[0023] Stage A (Figure 1A):

[0024] In stage A, a suitable baseboard 1 is selected for the circuit-board manufacturing process. The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, such as an FR4-type board. In the example process, the baseboard 1 can thus be an organic board, as the example process does not require high temperatures. A flexible and cheap organic board can thus be selected for the baseboard 1. Typically a board that is already coated with a conductive material 2, usually copper, is selected for the baseboard 1. Of course, an inorganic board can also be used.

[0025] Stage B (Figure 1B):

[0026] In stage B, through holes 3 are made in the baseboard for electrical contacts. The holes 3 can be made, for example, with some known method used in circuit-board manufacture, such as mechanical drilling.

[0027] Stage C (Figure 1C):

[0028] In stage C, metal is grown into the through holes made in stage B. In the example process, the metal 4 is also grown on top of the circuit board, thus also increasing the thickness of the conductive layer 2.

[0029] The conductive material 4 to be grown is copper, or some other material with sufficient electrical conductivity. Copper metallizing can take place by coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method. Chemical copper is used in the example, as it will also surface on top of a polymer and act as an electrical conductor in electrochemical coating. The metal can thus be grown using a wet-chemical method, so that the growth is cheap. Alternatively, the conductive layer 4 can be made, for example,

by filling the through holes with an electrically conductive paste.

[0030] Stage D (Figure 1D):

[0031] In stage D, the conductive layer on the surface of the circuit board is patterned. This can be done by utilizing generally known circuit-board manufacturing methods. The patterning of the conductive layer is aligned, for example, on the holes made in stage B.

[0032] The manufacture of the conductor pattern can take place, for example, by laminating, on the surface of the metal 4, a photolithographic polymer film, on which the desired conductive pattern is formed by directing light through a patterned mask. After exposure, the polymer film is developed, when the desired areas are removed from it and the copper 4 under the polymer is revealed. Next, the copper revealed under the film is etched away, leaving the desired conductive pattern. The polymer acts as a so-called etching mask and openings 5, at the foot of which the baseboard of the circuit board is revealed, are formed in the metal layer 4. After this, the polymer film is also removed from on top of the copper 4.

[0033] Stage E (Figure 1E):

[0034] In stage E, holes 6 are made in the baseboard for the microcircuits. The holes extend through the entire baseboard, from the first surface 1a to the second surface 1b. The holes may be made, for example, mechanically milling by means of a milling machine. The holes 6 can also be made, for example, by stamping. The holes 6 are aligned relative to the conductive patterns 4 of the circuit board. The holes 3 made during stage B can also be used to aid alignment, but then too the alignment is relative to the conductive patterns 4, as the conductive patterns 4 have a specific position in relation to the holes 3.

[0035] Stage F (Figure 1F):

[0036] In stage F, a polymer film 7 forming an electrical insulation is made on the second surface 1b of the baseboard and over the holes 6. The polymer film 7 is made in such a way that it is sufficiently rigid to retain the main features of its shape, but, however, not hardened, so that components can be attached by pressing them into the film. The polymer film should also be sufficiently rigid to be able to hold the components pressed into the film essentially immovable in relation to the base, during the following process stages.

[0037] The polymer film made in Stage F can be, for example, a pre-preg-type film.

[0038] If desired, a metal coating 8 can also be made on top of the polymer film 7 in stage F.

[0039] In the example process, stage F is carried out by laminating a thin polymer film (e.g., c. 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil. The lamination must then be carried out to be uncompleted, so that the polymer is not completely hardened. This is achieved by setting the laminating temperature sufficiently low and/or by shortening the duration of the heat treatment.

[0040] Stage G (Figure 1G):

[0041] In stage G, the microcircuits 18 are assembled in the holes 6, from the side of the first surface 1a of the baseboard. Assembly can take place using a precision assembly machine, the microcircuits 18 being aligned relative to the conductive patterns of the circuit board. As in stage E, the holes made in stage B can be used to aid alignment.

[0042] The microcircuits 18 are assembled in such a way that they adhere to polymer film 7 in the 'bottoms' of the holes 6. The most suitable way to carry out assembly is to use such a force that the microcircuits 18 push slightly inside the polymer film 7, so that

the microcircuits are made to remain in place better. It is also advantageous to the process, if the microcircuits being assembled have contact protrusions 9, which penetrate inside the polymer film 7.

[0043] Figure 3 shows an interesting alternative embodiment, in which the contact protrusions 9 of the microcircuits are so long that they extend right through the polymer film 7 to the metal coating 8. In that case, there is no need to make holes in the polymer film 7 (Stage K) for making contacts in the microcircuits, as the holes are formed in connection with the assembly of the components. In addition, the metallizing stage (Stage L) of the holes can be simplified, as the contact protrusions 9 automatically form conductor columns through the polymer film 7. In the embodiment of Figure 3, the contact protrusions can also be given a sharp shape, so that their penetration ability improves. If the contact protrusions 9 are sufficiently long and sharp, they can also penetrate the metal coating 8 and in principle form an electrical contact between the microcircuit 18 and the metal coating 8.

[0044] Stage H (not shown):

[0045] In stage H, the polymer film 7 is hardened with the aid of curing. Curing generally comprises a heat treatment, but the process can also employ some treatment other than heat to harden the polymer. If desired, stage H can also be omitted, particularly in connection with polymers cured by heat treatment. However, hardening the polymer at this stage prevents the microcircuit from moving relative to the base during stage I.

[0046] Stage I (Figure 1I):

[0047] In stage I, the microcircuits are secured to the baseboard of the circuit board by filling the holes made for the microcircuits with a filler material 10. In the example process, this stage is carried out by spreading casting epoxy into the holes from the first surface (1a) of the circuit board and on top of the microcircuits. The epoxy is smoothed with a spatula and hardened by curing in an autoclave. At the same time, the polymer

film 7 is also hardened, if the process does not include stage H.

[0048] Stage J (Figure 1J):

[0049] In stage J, a polymer film 11 is formed on the first surface (1a) of the circuit board, followed by a thin metal coating 12 on top of the polymer film.

[0050] In the example process, stage J is carried out by laminating a thin polymer film (e.g., c. 40 μm) on the surface of the circuit board, on top of which is a layer of copper (e.g., c. 5 μm). Lamination takes place with the aid of pressure and heat. In the example process, the film is thus an RCC (Resin Coated Copper) foil.

[0051] The polymer film can also be made by, for example, spreading polymer in a liquid form on the circuit board. Thus lamination is not essential in stage J. What is essential is that an insulating layer, typically a polymer film, is made on the circuit board, which contains the embedded components, particularly embedded microcircuits. The polymer film itself can be, according to the embodiment, a filled or unfilled polymer film. The polymer film can also be coated with metal, but this is not essential, as the conductive surface can also be made later, on top of a polymer layer that is already attached to the circuit board.

[0052] Stage J makes it possible to use conventional manufacturing methods and work stages used in circuit board manufacture in the example process and nevertheless to be able to bury microcircuits and other components inside the circuit board.

[0053] Stage K (Figure 1K)

[0054] In stage K, holes 13 are made in the polymer films 7 and 11 (and at the same time in the conductive foils 8 and 12), through which it is possible to create contacts with the conductive patterns and feed-throughs (conductive material 4) of the circuit board and with the microcircuits.

[0055] The holes 13 can be made, for example, using a laser, or some other suitable method. The conductive patterns made in stage D, or the through holes made in stage B can be used for alignment.

[0056] Stage L (Figure 1L):

[0057] Stage L corresponds to stage C. In stage L, a conductive layer 14 is made in the holes 13 and on the surfaces of the circuit board.

[0058] In the example process, the feed-throughs (holes 13) are first of all cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized by first forming a catalysing SnPd surface on the polymer and after that depositing a thin layer (about 2 Fm) of chemical copper onto the surface. The thickness of the copper 14 is increased by electrochemical deposition.

[0059] Alternatively, the feed-throughs can be filled with an electrically conductive paste or made using some other suitable micro-via metallizing method.

[0060] Stage M (Figure 1M):

[0061] In stage M, a conductive pattern is formed in the same way as in stage D.

[0062] Stages N and O (Figures 1N and 1O):

[0063] In stages N and O, a photolithographic polymer 14 is spread on the surface of the circuit board and the desired pattern is formed in the polymer 14 (in a manner similar to that in stages D and M). The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

[0064] Stage P (Figure 1P):

[0065] In stage P, the connection areas of the polymer film pattern formed in the previous stage are coated 16. The coating 16 can be made with, for example, a Ni/Au coating, or an OSP (organic surface protection).

[0066] The example of Figure 1 depicts one process, which can be used to exploit our invention. Our invention is thus in no way restricted to the process described above, but instead the invention covers a large group of different process and their end products, to the full extent of the Claims and allowing for equivalency interpretations. In particular, the invention is in no way restricted to the layout shown in the example, instead it will be obvious to one versed in the art that the processes according to our invention can be used to manufacture many kinds of circuit boards, which differ greatly from the examples disclosed here. Thus, the microcircuits and connections of the figures are only shown to illustrate the manufacturing process.

[0067] A great many changes can thus be made to the process of the example disclosed above, without nevertheless deviating from the idea according to the invention. The changes can relate to the manufacturing techniques depicted in the various stages, or, for example, to the mutual sequence of the stages. For example, stage B can equally well be carried out after stage D, i.e. the procedure can be to align the drill on the pattern, instead of aligning the pattern on the drilled holes. Correspondingly, the order of stages D and E can also be reversed. The component holes 6 are then made before the conductive patterns are formed. In that case, the conductive pattern is aligned relative to the holes 6 (and also the holes 3). Irrespective of the order in which stages B, D, and E are carried out, the polymer film 7 to be made in stage F covers the holes 6 and the conductive pattern formed on the second surface 1b of the baseboard.

[0068] Stages that are felt to be required can also be added to the process of the example disclosed above. For example, a foil that protects the surface of the circuit board during the casting taking place in stage H can be laminated onto the first side (1a) of the circuit board. Such a protective foil is manufactured so that it covers all the other areas except for the holes 6. The protective foil keeps the surface of the circuit board clean when the

casting epoxy is spread with the spatula. The protective foil can be made in a suitable stage before stage I and removed from the surface of the circuit board immediately after the casting.

[0069] With the aid of the method, it is also possible to manufacture component packets to be attached to the circuit board. Such packets can also include several semiconductor components, which are connected electrically to each other.

[0070] The method can also be used to manufacture entire electrical modules. The process shown in Figure 1 can also be applied in such a way that the conductive structure is made only on the second side (1b) of the circuit board, to which the contact surfaces of the microcircuit are oriented.

[0071] The method makes it possible to manufacture, for example, circuit boards or electrical modules, in which the thickness of the baseboard used is in the range 50 - 200 microns and the thickness of the microcircuit and microcircuits is in the range 50 - 150 microns. The pitch of the conductors can vary, for example, in the range 50 - 250 microns while the diameter of the micro-feed-throughs can be, for example, 15 - 50 microns. Thus, the total thickness of a single board in a one-layer construction will be about 100 - 300 microns.

[0072] The invention can also be applied in such a way that circuit boards are assembled on top of each other, thus forming a multi-layer circuit structure, in which there are several circuit boards manufactured according to Figure 1 set on top of each other and connected electrically to each other. The circuit boards set on top of each other can also be circuit boards in which the conductive structure is formed only on the second side 1b of the circuit board, but which nevertheless include feed throughs, through which an electrical contact can also be formed to the microcircuits from the first side of the circuit board. Figure 2 shows one such process.

[0073] Figure 2 shows the connection of circuit boards to each other. In the following, the process is described in stages.

[0074] Stage 2A (Figure 2A):

[0075] Stage 2A depicts the circuit boards being set on top of each other. The lowest circuit board can be obtained, for example, after stage J of a modified process of Figure 1. In this case, the process of Figure 1 is then modified by omitting stage 1C.

[0076] The middle and upper circuit boards in turn can be obtained after stage M of a modified process of Figure 1, for instance. In this case, the process of Figure 1 is modified by omitting stage 1C and performing stages J, K, and L on only the second side (1b) of the circuit board.

[0077] In addition to the circuit boards, Figure 2A also shows pre-preg epoxy layers 21 placed between the circuit boards.

[0078] Stage 2B (Figure 2B):

[0079] In stage 2B, the circuit boards are laminated together with the aid of pre-preg epoxy layers 21. In addition, a metal-coated polymer film 22 is made on the upper surface of the circuit board. The process corresponds to stage J of the process of Figure 1. In the example process, a metal-coated polymer film 22 is already on the under surface of the circuit board.

[0080] Stage 2C (Figure 2C):

[0081] In stage 2C, holes 23, for the formation of contacts, are drilled in the circuit board.

[0082] After Stage 2C, the process can be continued for example as follows:

[0083] Stage 2D:

[0084] In stage 2D, conductive material is grown on top of the circuit board and in the through holes 23, in the same way as in stage 1C.

[0085] Stage 2E:

[0086] In stage 2E, the conductive layer on the surface of the circuit board is patterned in the same way as in stage 1D.

[0087] Stage 2F:

[0088] In stage 2F, a photolithographic polymer is spread on the surfaces of the circuit board and the desired pattern is formed in the polymer in the same way as in stages 1N and 1O. The exposed polymer film is developed, but the polymer film pattern remaining on the circuit board is not removed.

[0089] Stage 2G:

[0090] In stage 2G, the connection areas of the polymer film pattern formed in the previous stage are metallized in the same way as in stage 1P.

[0091] On the basis of the example of Figure 2, it is obvious that the method can also be used to manufacture many kinds of three-dimensional circuit structures. For example, the method can be used in such a way that several memory circuits are placed on top of each other, thus forming a packet containing several memory circuits, in which the memory circuits are connected to each other to form an operational totality. Such a packet can be termed a three-dimensional multichip module. The chips in such modules can be selected freely and the contacts between the chips can be easily made according to the selected circuits.

[0092] The invention also permits electromagnetic protection to be made around the component embedded in the base. This is because the method of Figure 1 can be

modified in such a way that the holes 6 depicted in stage 1E can be made in connection with the making of the holes 3 carried out in stage 1B. In that case, the conductive layer 4 to be made in stage 1C will also cover the side walls of the holes 6 made for the components. Figure 4A shows a cross-section of the base structure as it is after stage 1F in the process modified in the aforesaid manner.

[0093] After the intermediate stage shown in Figure 4A, the process can be continued by assembling the microcircuits in a similar way to stage 1G, the polymer film being hardened as in stage 1H, and the microcircuits being attached similarly to stage 1I. After this, polymer and metal foils can be formed on the first surface of the circuit board similarly to stage 1J. Figure 4B shows an example cross-section of the base structure after these process stages.

[0094] After the intermediate stage shown in Figure 4B, the process can be continued by making holes, similar to those of stage 1K, in the polymer film, for making contacts. After this, a conductive layer is made in the holes and on the surfaces of the board similarly to stage 1L. Figure 4C shows an example cross-section of the base structure after these process stages. For reasons of clarity, the conductive layer made similarly to stage 1L in the holes and on the board surfaces is highlighted in black.

[0095] After the intermediate stage shown in Figure 4C, the process can be continued by patterning a conductive layer on the surfaces of the board as in stage 1M and by coating the surfaces of the board as in stage 1N. After these stages, the microcircuits are surrounded by a nearly unbroken metal foil, which forms an effective protection against interference caused by electromagnetic interaction. This construction is shown in Figure 4D. After the intermediate stage shown in Figure 4D, stages corresponding to stages 1O and 1P are carried out, in which a protective foil and connections are made on the surface of the circuit board.

[0096] In Figure 4D, the cross-sections of the metal layers protecting the microcircuits are highlighted in black. In addition, the background of the microcircuits is highlighted with cross-hatching. The cross-hatching is intended to be a reminder that all the sides of

a hole made for a microcircuit are covered by a metal foil. Thus the microcircuit is surrounded laterally with an unbroken metal foil. In addition to this, a metal plate can be designed above the microcircuit, which is made in connection with the making of the circuit board's conductive pattern. Similarly, a metal foil that is as complete as possible is made below the microcircuit. The making of contacts below the microcircuit means that small gaps must be made in the metal foil, as shown in Figure 4D, for instance. These gaps can, however, be made so narrow laterally, or, correspondingly, so thin vertically, that they do not weaken the protective effect obtained against electromagnetic interference.

[0097] When examining the example of Figure 4D, it must also be taken into account that the final structure also contains parts extending at right angles to the plane shown in the figure. Such a structure extending at right angles is shown by the conductor connected to the contact bump on the left-hand side of the left-hand microcircuit of Figure 4D, which runs towards the viewer from between the metal foil surrounding the microcircuit laterally and the conductive layers below the microcircuit.

[0098] The solution shown by Figure 4D thus provides the microcircuit with excellent protection against electromagnetic interference. As the protection is made immediately around the microcircuit, the construction also protects against mutual interference arising between the components contained in the circuit board. Most of the electromagnetic protective structure can also be earthed, as the metal foil surrounding the microcircuits laterally can be connected electrically to the metal plate above the circuit. The connections of the circuit board, can, in turn, be designed in such a way that the metal plate is earthed through the conductive structure of the circuit board.

Claims:

1. A circuit board comprising
 - an insulating material layer having a first side and a second side,
 - at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
 - at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
 - a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,
 - a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
 - contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.
2. The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.
3. The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.
4. The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.
5. The circuit board of claim 4, wherein the metal foil is electrically connected to

at least one of the first and second metal plates.

6. The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.

7. The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that

the side-surfaces of the component face towards the metal foil,
the first surface of the component face towards the second metal plate, and
the second surface of the component face towards the first metal plate.

8. The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.

9. The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

10. The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.

11. The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

12. The circuit board of claim 1, wherein the component is a microcircuit.

13. The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.

14. The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive patterns on the both sides of the insulating material layer.

15. A multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other, wherein at least the first circuit board substructure comprises

an insulating material layer having a first side and a second side,

at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the conductive pattern layers defining a first metal plate,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

16. The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.

17. The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer.

18. The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.

19. The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

20. The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises

an insulating material layer having a first side and a second side,

at least one first conductive pattern layer on the first side of the insulating material layer,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

a component inside the insulating material layer and having a first surface facing towards the second metal plate, and contact areas on the first surface,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

21. The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises

an insulating material layer having a first side and a second side,

at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,

at least one second conductive pattern layer on the second side of the insulating material layer,

a component inside the insulating material layer, the component having first surface and a second surface on the opposite sides of the component and contact areas on the first surface, the second surface facing towards the first metal plate,

a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one conductive pattern.

22. The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.

23. The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.

24. The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.

25. The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.

26. The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.

27. The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.

28. The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.

29. The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.

30. The multi-layered circuit board of claim 15, wherein the component is a microcircuit.

31. The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer.

32. An electronic module comprising
 an insulating material layer having a first side and a second side,
 at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,

at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates,

a metal foil covering the sidewalls of the hole,

a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface,

a filler material in the hole between the metal foil and the microcircuit,

a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer, and

contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the

microcircuit and the at least one conductive pattern.

33. The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.

34. The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.

35. The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.

36. The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.

Abstract of the Disclosure

A method, in which the semiconductor components forming part of an electronic circuit, or at least some of them, are embedded in a base, such as a circuit board, during the manufacture of the base, when part of the base structure is, as it were, manufactured around the semiconductor components. Through-holes for the semiconductor components are made in the base, in such a way that the holes extend between the first and second surface of the base. After the making of the holes, a polymer film is spread over the second surface of the base structure, in such a way that the polymer film also covers the through-holes made for the semiconductor components from the side of the second surface of the base structure. Before the hardening, or after the partial hardening of the polymer film, the semiconductor components are placed in the holes made in the base, from the direction of the first surface of the base. The semiconductor components are pressed against the polymer film in such a way that they adhere to the polymer film.

PLEASE NOTE:
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FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: ➡

Method for embedding a component in a base

the specifications of which is attached hereto. If not attached hereto, the application is identified by the attorney docket number as set forth above and/or the following:

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Attached: ➡

the specification was filed on _____ as
United States Application Number _____;
and amended on _____ (if applicable); and/or
the specification was filed on January 28, 2003 as PCT
International Application Number PCT/FI03/00065; and was
amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority
Information:
(if appropriate) ➡

Prior Foreign Application(s)

(Number)	(Country)	(Month / Day / Year Filed)	Priority Claimed
<u>20020191</u>	<u>Finland</u>	<u>01/31/2002</u>	☒ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No
_____	_____	_____	☐ Yes ☐ No

Insert Provisional
Application(s): ➡
(if any)

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
_____	_____
_____	_____

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed more than 12 months (6 months for designs) Prior to the Filing Date of this Application:

Insert Requested
Information:
(if appropriate) ➡

Country	Application Number	Date of Filing (Month / Day / Year)
_____	_____	_____
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s), including for continuation-in-part application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S.
Application(s): ➡
(if any)

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
_____	_____	_____
_____	_____	_____

I hereby appoint the practitioners at **CUSTOMER NO. 02292** as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or **CUSTOMER NO. 02292**

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Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full Name of First or
Sole Inventor:
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Insert Date This
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Insert Residence
Insert Citizenship

Insert Mailing
Address

Full Name of Second
Inventor, if any:

see above

Full Name of Third
Inventor, if any

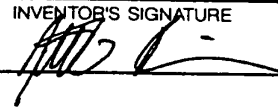
see above

Full Name of Fourth
Inventor, if any

see above

Full Name of Fifth
Inventor, if any

see above

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GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
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GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
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GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
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MAILING ADDRESS (Complete Street Address including City, State & Country)			

* DATE OF SIGNATURE

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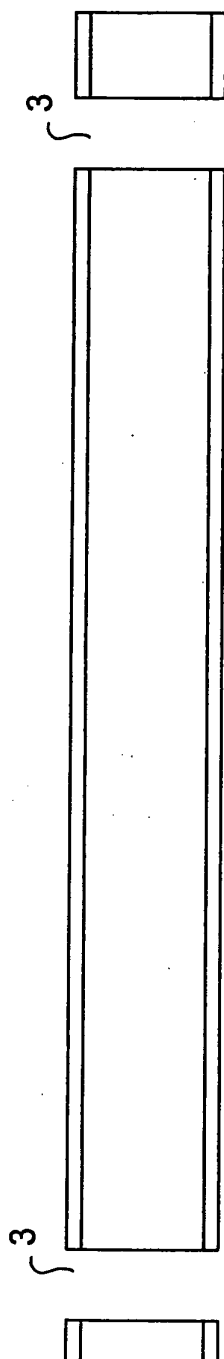
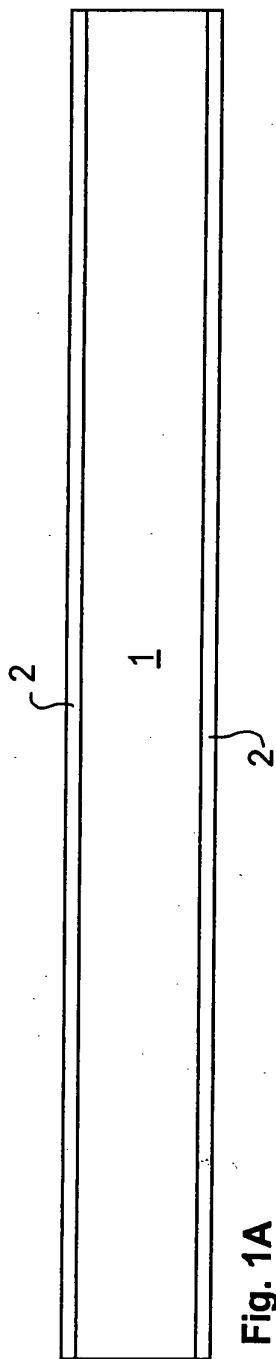


Fig. 1B

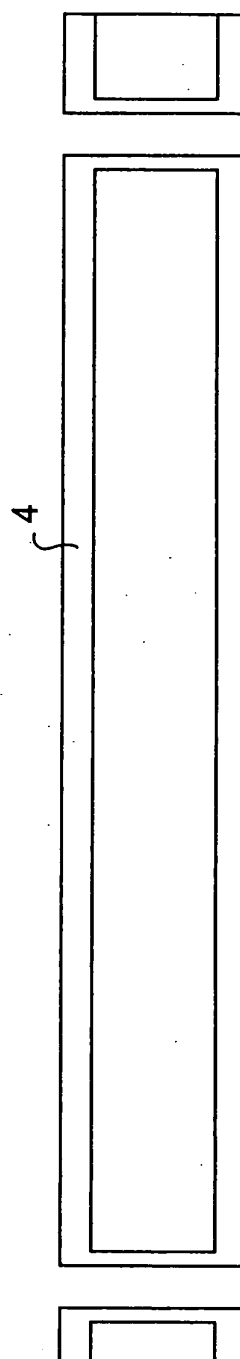


Fig. 1C

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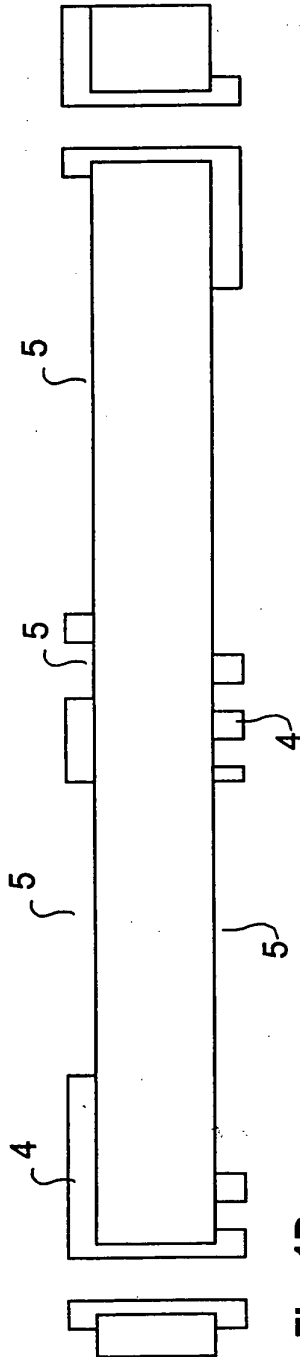


Fig. 1D

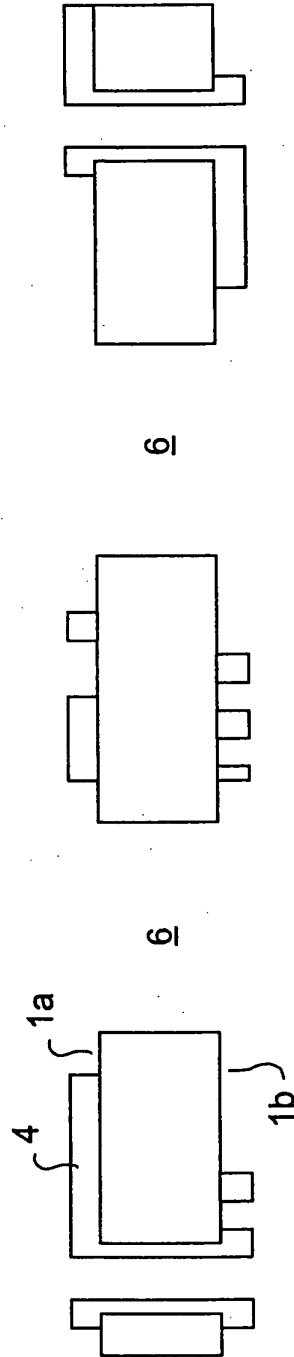


Fig. 1E

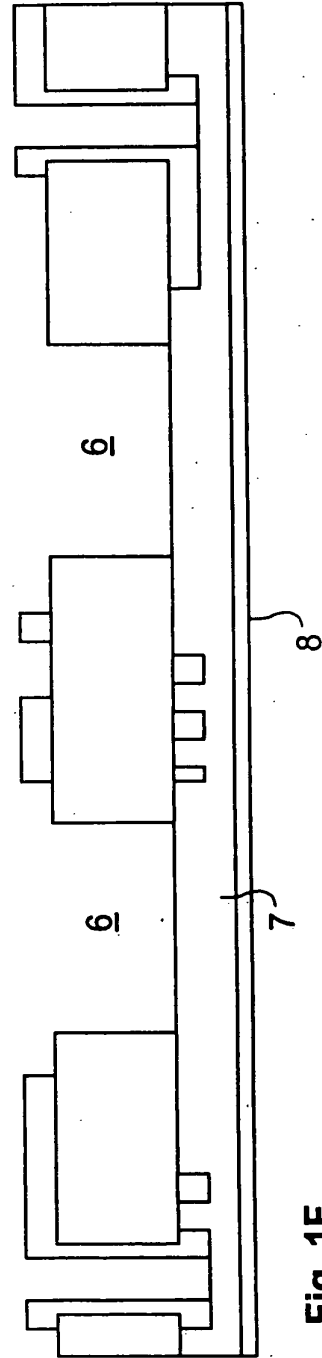


Fig. 1F

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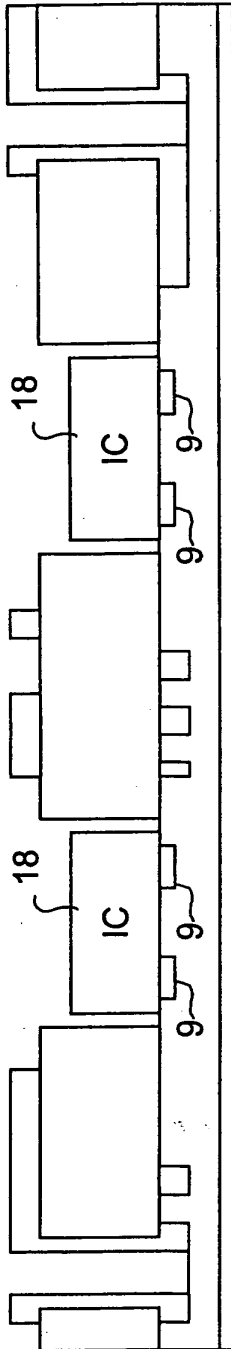


Fig. 1G

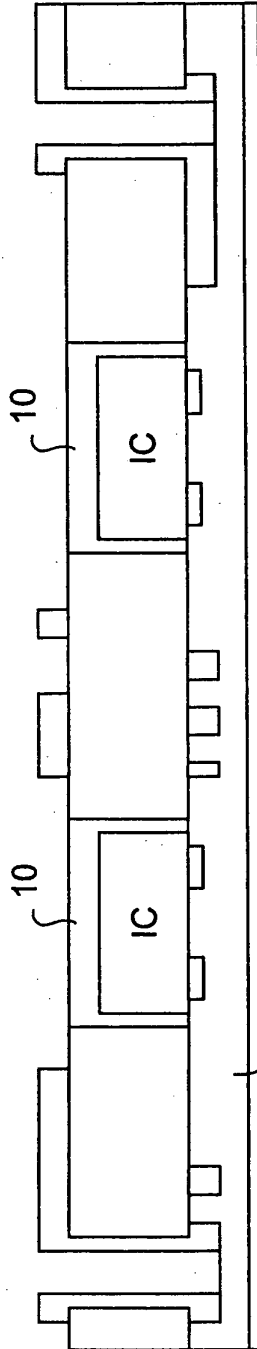


Fig. 1I

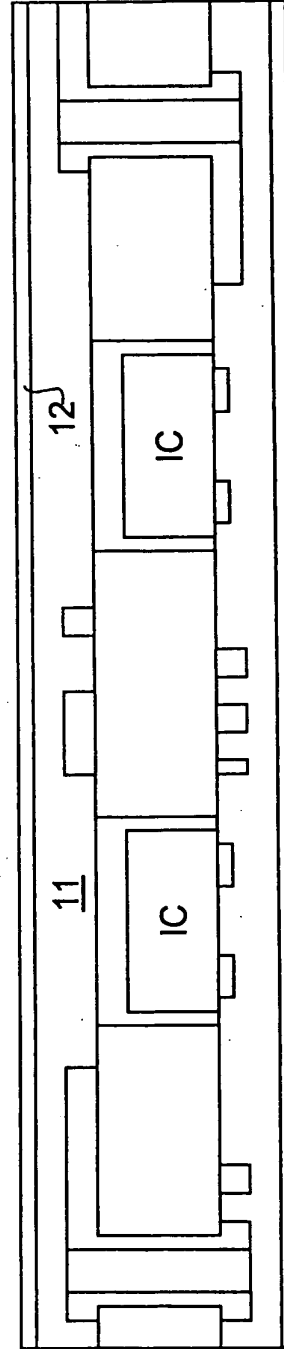
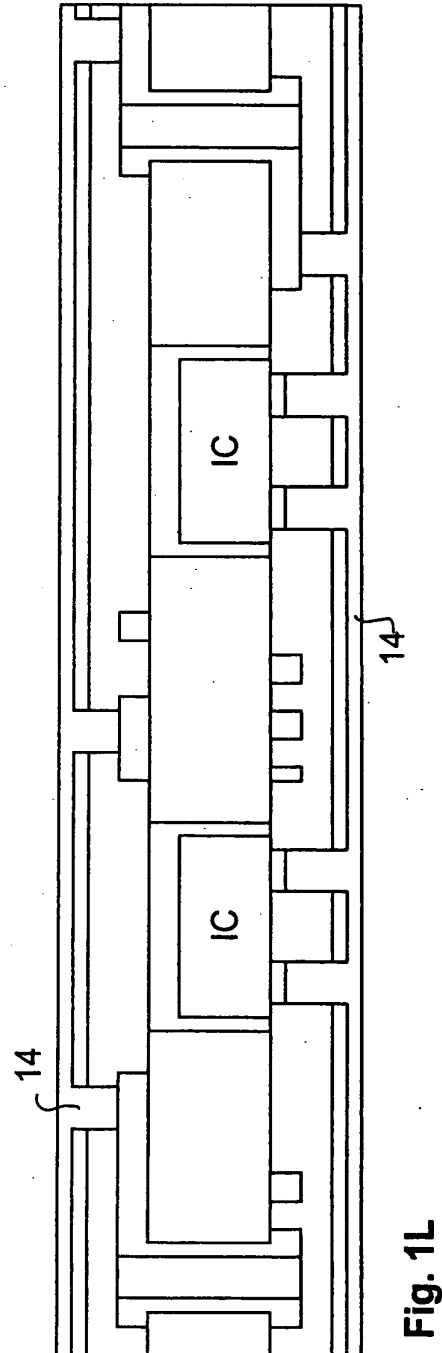
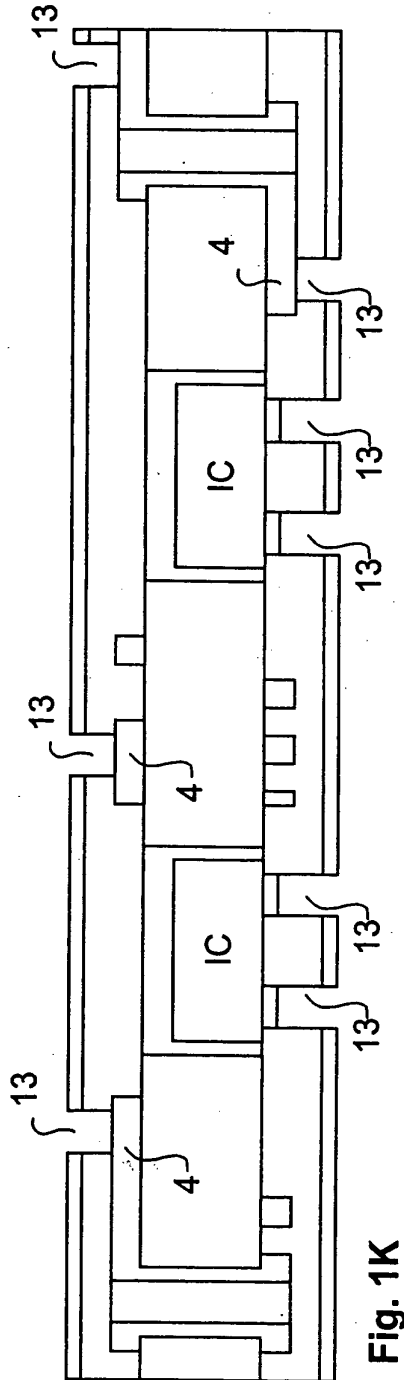


Fig. 1J

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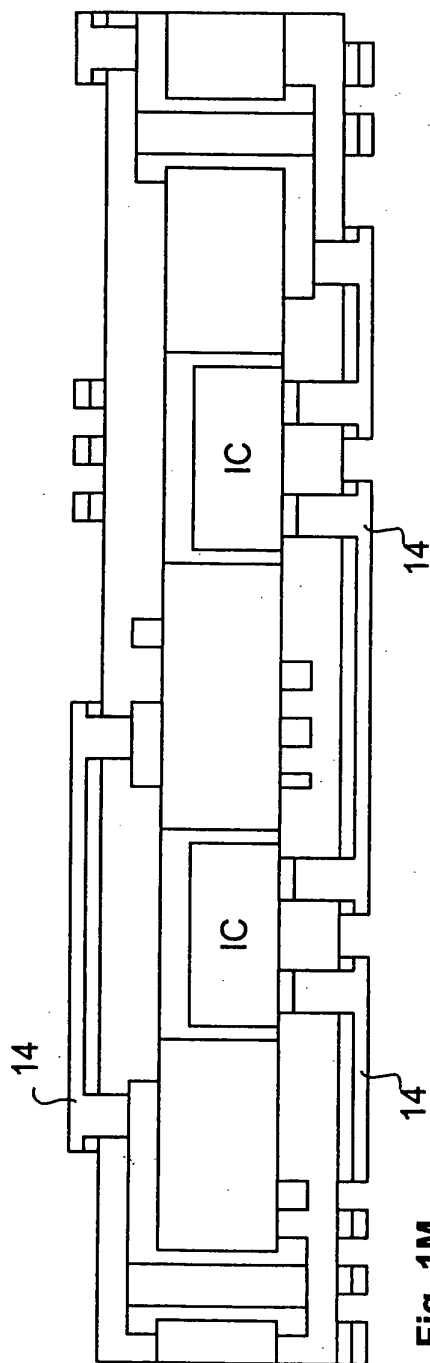


Fig. 1M

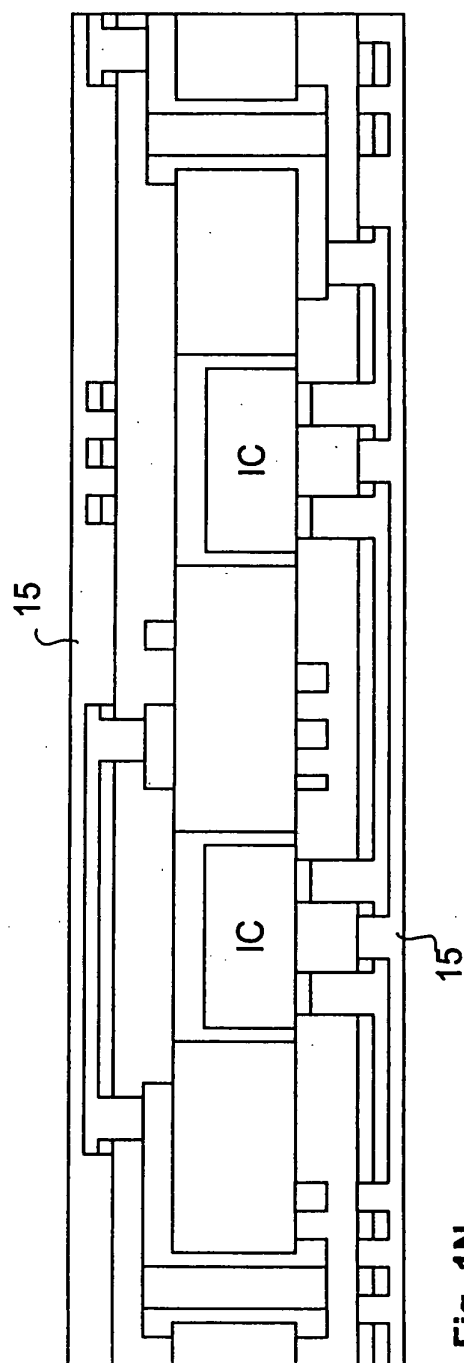


Fig. 1N

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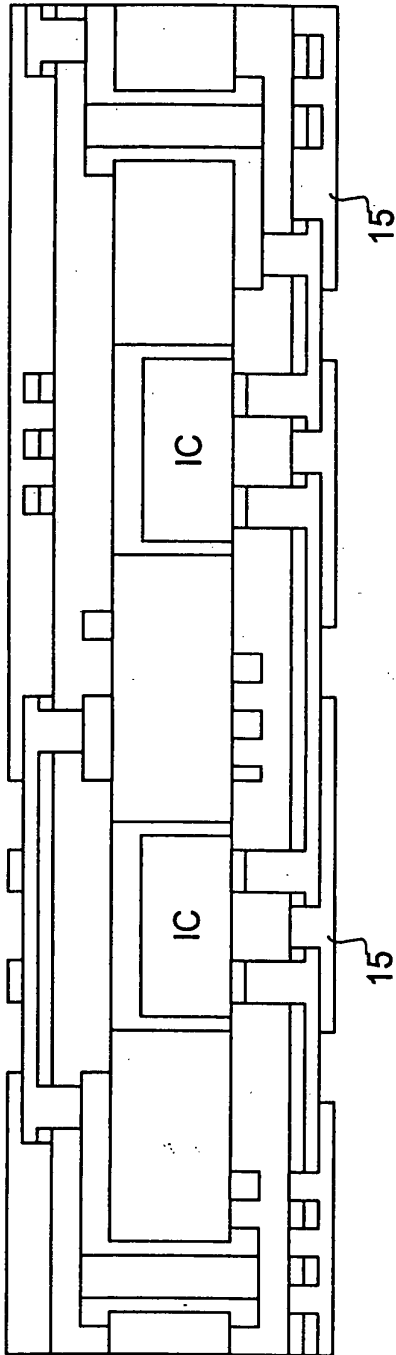


Fig. 10

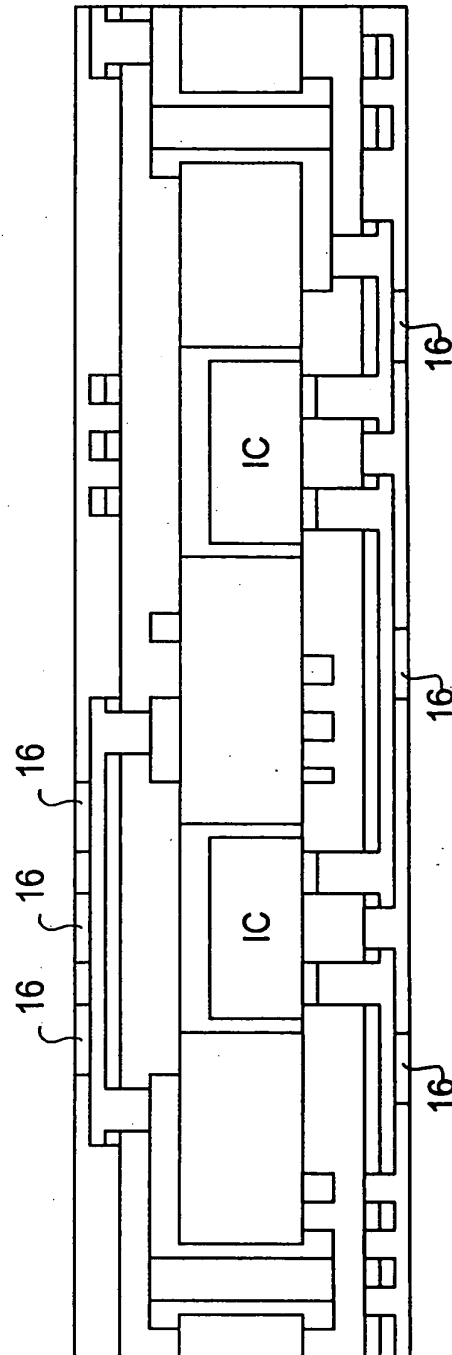


Fig. 1P

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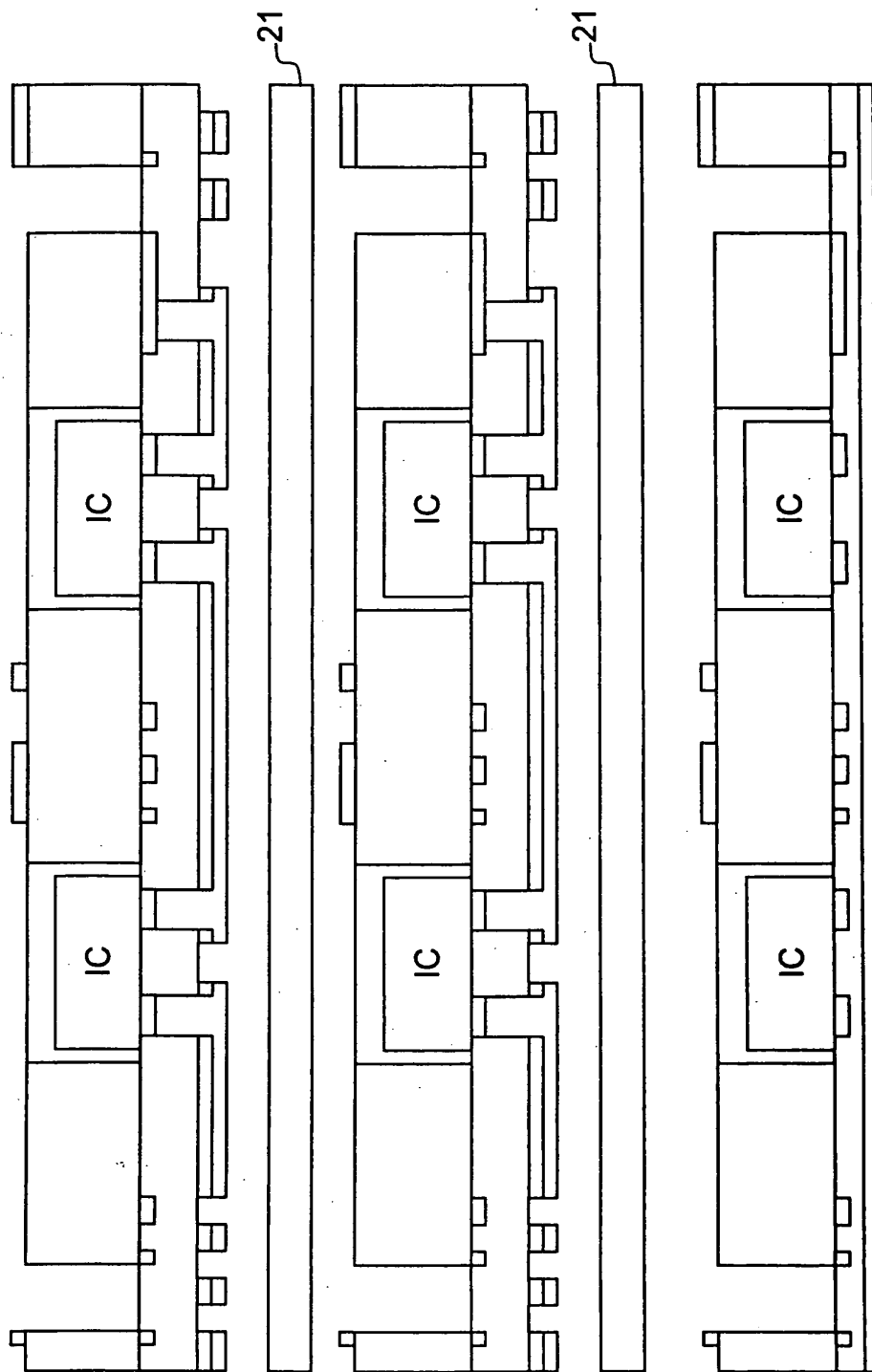


Fig. 2A

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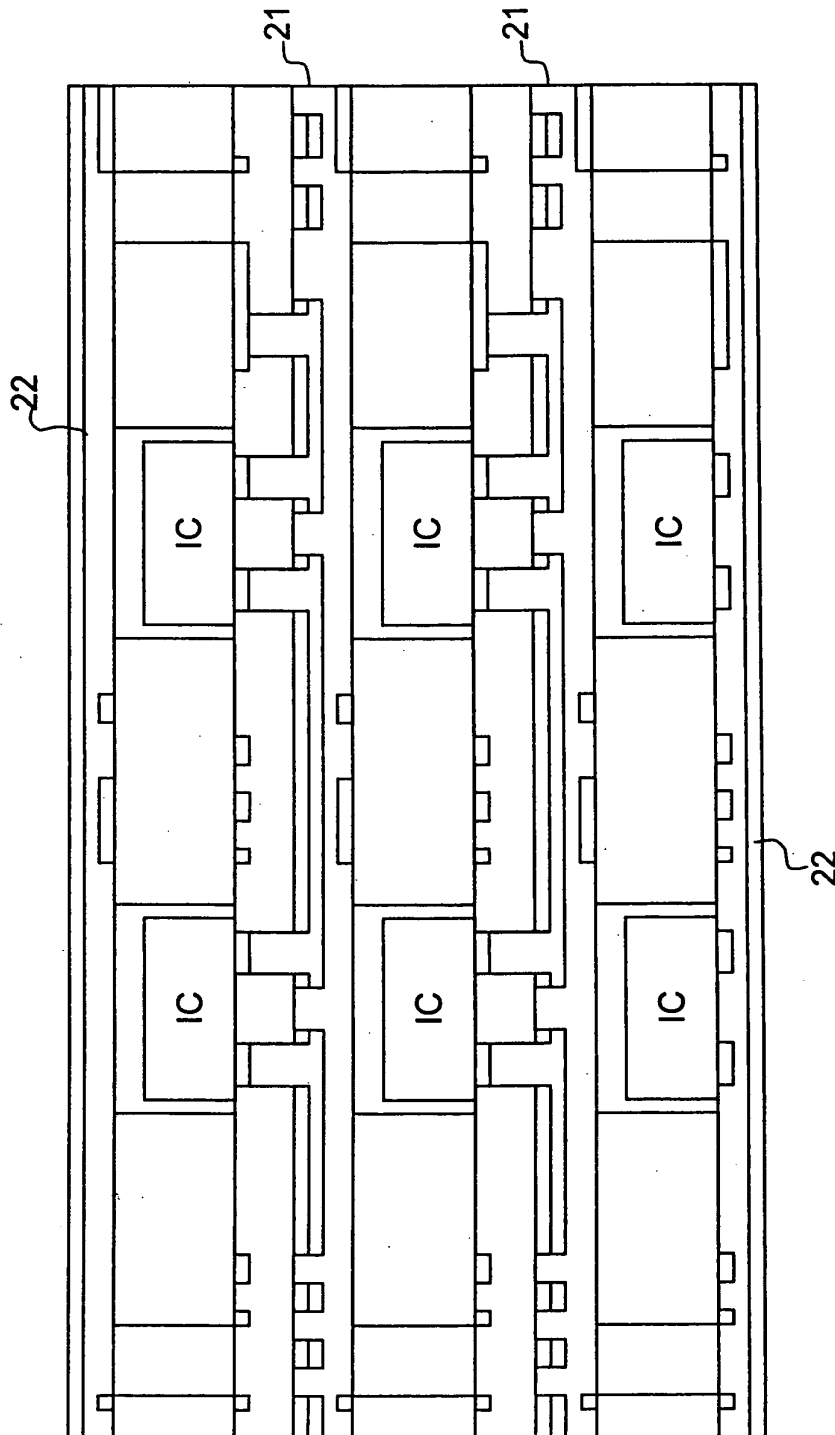


Fig. 2B

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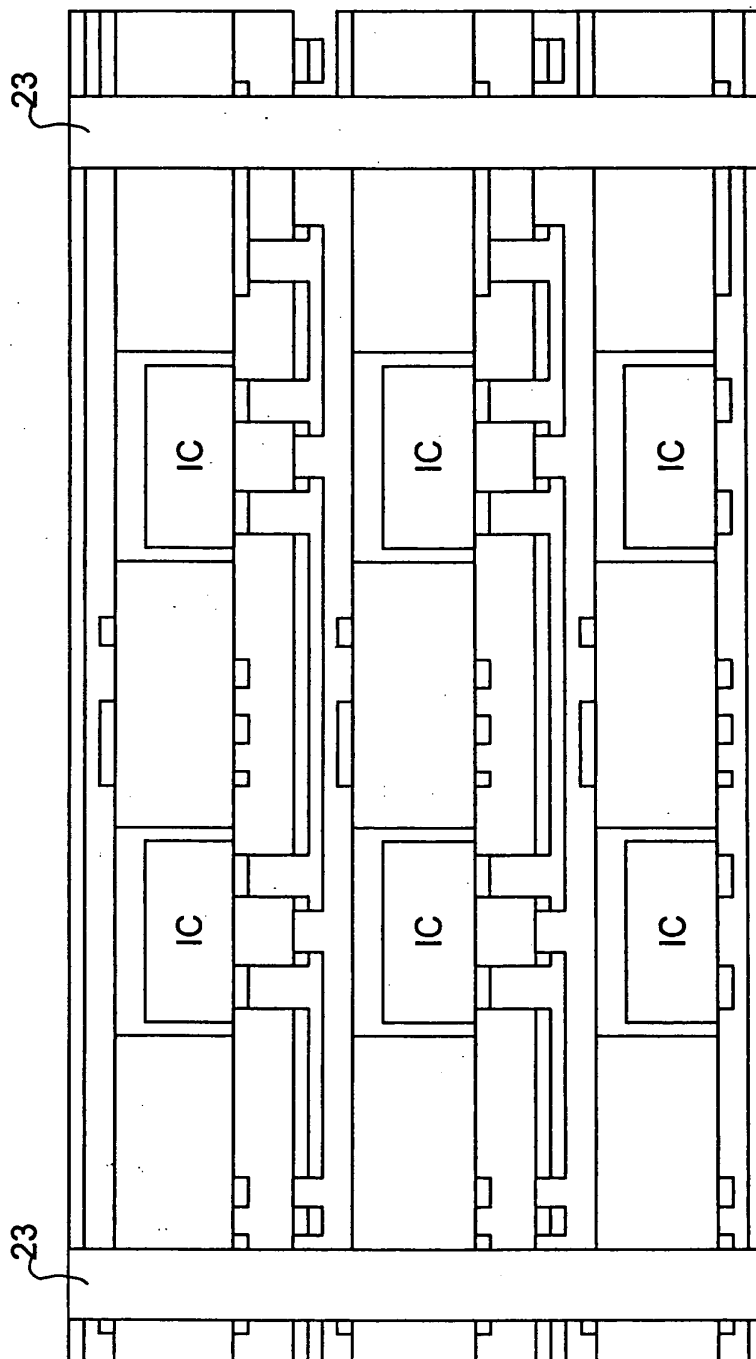


Fig. 2C

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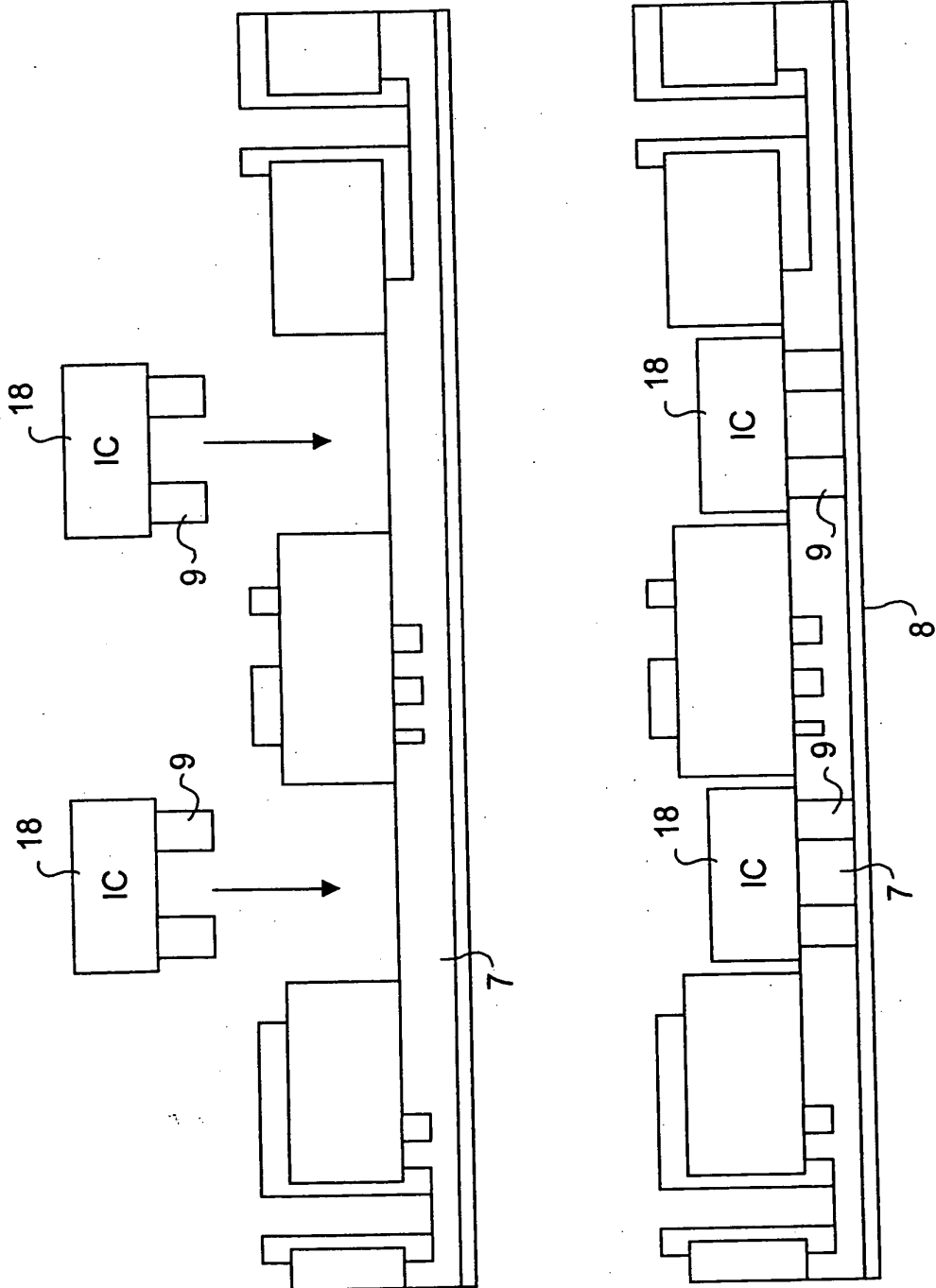
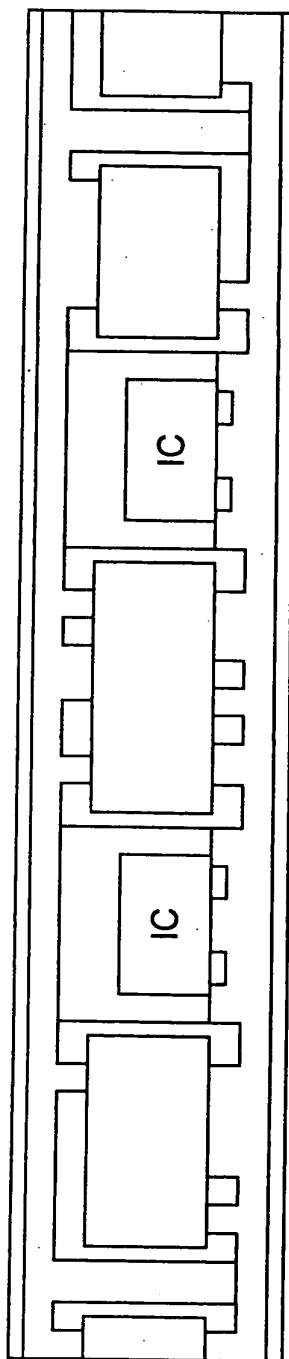
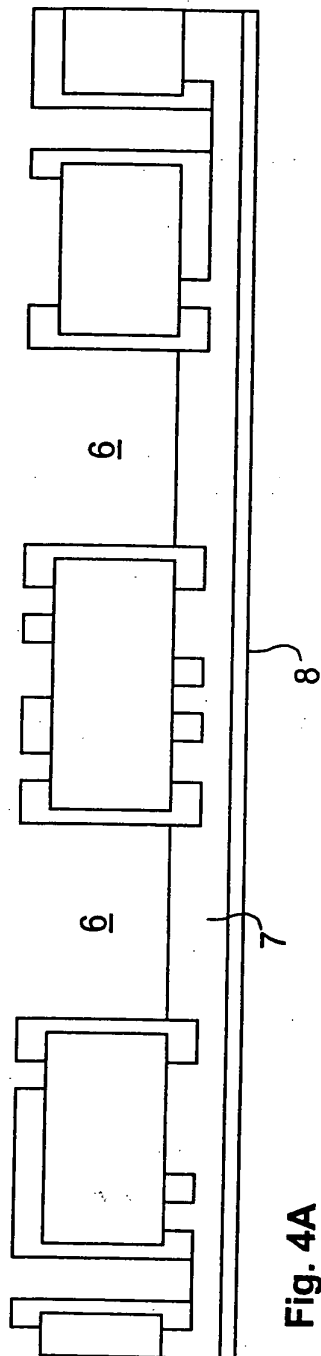


Fig. 3

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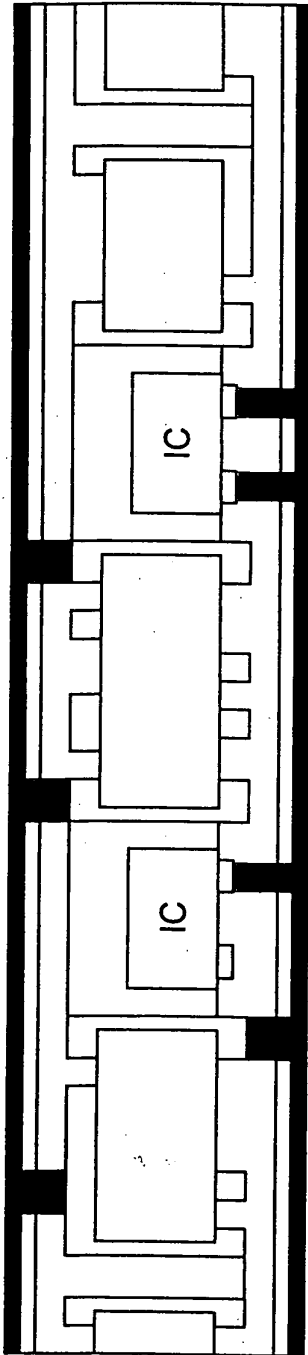


Fig. 4C

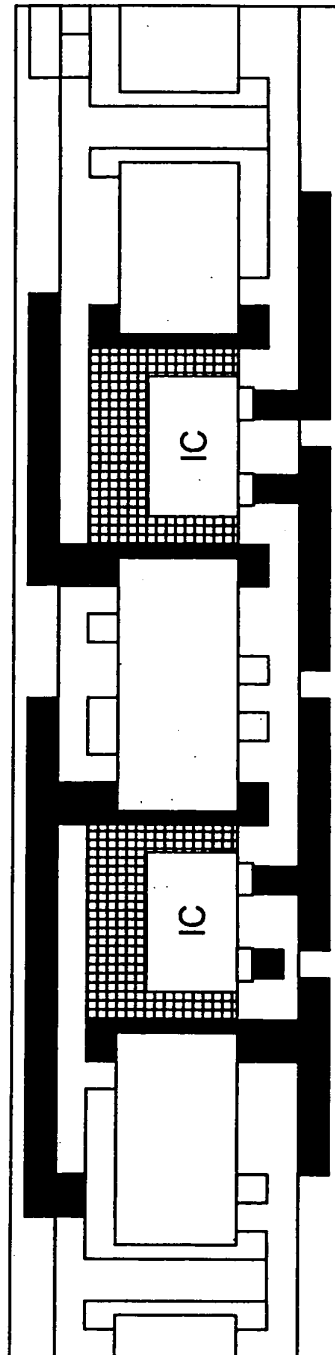


Fig. 4D