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Frank McGee

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 (71) [Applicant]
 [Identification Number] 000000158
 [Name] Ibiden Co., Ltd.
 [Address] 2-1, Kanda-cho, Ogaki-shi, Gifu-ken
 (72) [Inventor]
 [Name] Hajime SAKAMOTO
 [Address] Ibiden Co., Ltd., 1-1, Kanda-cho, Ogaki-shi, Gifu-ken
 (72) [Inventor]
 [Name] Sunao SUGIYAMA
 [Address] Ibiden Co., Ltd., 1-1, Kanda-cho, Ogaki-shi, Gifu-ken
 (74) [Agent]
 [Identification Number] 100095795
 [Attorney]
 [Name] Akihito TAGE (and 1 other)

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[Claims]

[Claim 1]

A multilayer printed wiring substrate having an interlayer insulating layer and a conductor layer repeatedly formed on a substrate, vias are formed in the interlayer insulating layers, and electrical connections are established through the vias, the multilayer printed wiring substrate characterized in that an electronic component is built into the substrate.

[Claim 2]

The multilayer printed wiring substrate according to claim 1, wherein an electronic component is mounted on the surface.

[Claim 3]

The multilayer printed wiring substrate according to claim 1 or claim 2, wherein the substrate is provided with terminals for establishing a connection with an external substrate.

[Claim 4]

A multilayer printed wiring substrate having an interlayer insulating layer and a conductor layer repeatedly formed on a substrate, vias are formed in the interlayer insulating layers, and electrical connections are established through the vias, the multilayer printed wiring substrate characterized in that an electronic component is built into the substrate, and a transition layer is formed on the die pads of the electronic component to connect the electronic component to vias in the lowermost interlayer insulating layer.

[Claim 5]

The multilayer printed wiring substrate according to any of claims 1 to 4, wherein the substrate is a package substrate.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a build-up multilayer printed wiring substrate, and more specifically to a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip.

[0002]

[Prior Art]

IC chips have been electrically connected to printed wiring substrates using mounting methods such as the wire bonding, TAB, and flip chip methods. In the wire bonding method, an IC chip is die-bonded to a printed wiring substrate using adhesive, the pads of the printed wiring substrate are connected to the pads of the IC chip using wire such as gold

wire, and a sealing resin, such as thermosetting resin or thermoplastic resin, is applied to protect the IC chip and wires. In the TAB method, bumps on an IC chip and pads on a printed wiring substrate are connected all at once to wires called leads by solder, etc., and then sealed in a resin. In the flip chip method, an IC chip to the pad portions of a printed wiring substrate are connected via bumps and the gap between the chip and the bumps is filled with a resin.

[0003]

[Problem to Be Solved by the Invention]

However, in each of these mounting methods, an electrical connection is established between the IC chip and the printed wiring substrates via lead components (wires, leads, bumps). Each of these lead components is prone to disconnection and corrosion, which can lead to loss of connection with the IC chip or cause a malfunction. Also, in each of these mounting methods, the IC chip is sealed with a thermoplastic resin such as epoxy resin in order to protect the chip. However, if air pockets are trapped when filled with a resin, the trapped air pockets can become a starting point for the destruction of lead components, corrosion of IC pads, and loss of reliability. When sealing using thermoplastic resin, resin-loading plungers and molds have to be created for each component, and a thermosetting resin has to be selected that takes into consideration the materials in the lead component, solder resists, etc., so that the resin can be used in a wide range of applications, leading to higher costs for each component.

[0004]

In view of these circumstances, it is an object of the present invention to provide a multilayer printed wiring substrate that can be electrically connected directly to an IC chip without a lead component.

[0005]

[Means for Solving the Problem]

As a result of extensive research, the present inventors propose a structure that can establish an electrical connection with an IC chip using a leadless, bumpless process without the use of a sealing resin, by providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance, applying an interlayer insulating layer, providing vias on the IC chip pads using photoetching or a laser to form a conductor circuit that is a conductor layer, and then repeatedly forming interlayer insulating layers and conductor layers to provide a multilayer printed wiring substrate.

[0006]

The present inventors also propose a structure in which an electronic component such as an IC chip or a capacitor is mounted on the surface of the multilayer printed wiring substrate obtained by providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance, applying an interlayer insulating layer, providing vias on the IC chip pads using photoetching or a laser to form a conductor circuit that is a conductor layer, and then repeatedly forming interlayer insulating layers and conductor layers. As a result, a leadless, bumpless electrical connection can be made with an IC chip without using a sealing resin. In addition, electronic

components such as IC chips and capacitors with different functions can be mounted, and a multi-layer printed wiring substrate with higher functionality can be obtained. In a specific example, an IC chip, cache memory, and capacitor can be arranged close to each other by embedding an IC chip with a calculating function as the built-in IC chip and mounting a cache memory and a capacitor on the surface layer.

[0007]

As a result of extensive research, the present inventors also propose providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance, and providing a transition layer consisting of a conductor layer on the pads of the IC chip. An electrical connection with an IC chip can be realized in a leadless and bumpless manner without using a sealing resin by laminating an interlayer insulating layer on top of the transition layer, providing vias in the transition layer using photoetching or a laser to form a conductive circuit that is a conductive layer, and then repeatedly forming interlayer insulating layers and conductor layers to form a multilayer printed wiring substrate. Because the transition layer is formed in the IC chip portion and the IC chip portion is flattened, the upper interlayer insulating layer is also flattened and the film thickness made uniform. The transition layer also enables shape stability to be maintained during the formation of the vias in the upper layer.

[0008]

The transition layer defined in the present invention will now be described. Transition layer refers to an intermediate layer provided for direct connection of an IC chip, which is a semiconductor element, to a printed wiring substrate without using a conventional IC chip mounting technology. The transition layer is formed of two or more metal layers and is made larger than the die pads of the IC chip, which is as a semiconductor element. As a result, electrical connection and alignment are improved, and via hole processing using a laser or photoetching can be performed without damaging the die pads. Therefore, reliable embedding, housing, storage, and connection of the IC chip to the printed wiring substrate becomes possible. A metal, which is a conductor layer of a printed wiring substrate, can be directly formed on the transition layer. Examples of conductor layers include via holes in interlayer resin insulating layers and through-holes in substrates.

[0009]

The reason for providing the transition layer on the pads of the IC chip is as follows. First, if the die pads are fine and small in size, alignment becomes difficult when forming vias, so a transition layer is provided to facilitate alignment. By providing a transition layer, a buildup layer can be stably formed even at a die pad pitch of 150 μm or less and a pad size of 20 μm or less. If vias in the interlayer insulating layer are formed by photoetching while the die pads do not have a transition layer, and if the diameter of the vias are larger than the diameter of the die pads, the polyimide layer, which is the protective layer on the die pad surface, will be dissolved or damaged during de-smearing, which is performed to remove residue at the bottom of the vias and to roughen the surface of the interlayer insulating layer. Meanwhile, when a laser is used, if the via diameter is larger than the die pad diameter, the die pads, passivation layer, and polyimide layer (protective film for the IC) are destroyed by the laser. If the pads of the IC chip are very small and the via diameter is larger than the size of the die pads, alignment in the photoetching or laser method becomes difficult, and connection failures may occur between the die pads and the vias.

[0010]

In contrast, by providing a transition layer on the die pads, the vias can be reliably connected to the die pads, even when the die pad pitch is 150 μm or less and the pad size is 20 μm or less, thus improving reliability. Furthermore, by interposing a transition layer with a larger diameter on the pads of the IC chip, the die pads can be immersed in an acid or an etchant or subjected to annealing during post-processing such as de-smearing and plating with no risk of dissolving or damaging the protective films (passivation, polyimide layer) on the IC.

[0011]

While various functions are realized by a multilayer printed wiring substrate, in some cases, BGA, solder bumps, and PGA (conductive connection pins) can be used to connect with external substrates such as motherboards and daughterboards in order to function as a package substrate of a semiconductor device. This configuration can also shorten wiring lengths and reduce loop inductance compared to connection using a conventional mounting method.

[0012]

Resin substrates used to incorporate electronic components such as IC chips in the present invention include epoxy resins, BT resins, and phenol resins impregnating a reinforcing material such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin. However, any material generally used in printed wiring substrates can be used. A double-sided copper-clad laminate, a single-sided board, a resin board with no metal film, or a resin film can also be used.

[0013]

Physical vapor deposition such as vapor deposition or sputtering is performed on the entire surface of the core substrate in which the IC chip is incorporated to form a conductive metal film on the entire surface. The metal is preferably one or more layers of a metal such as tin, chromium, titanium, nickel, zinc, cobalt, gold, or copper. The thickness is preferably 0.001 to 2.0 μm . A thickness of 0.01 to 1.0 μm is especially preferred.

[0014]

When forming the transition layer by a semi-additive process, a dry film resist can be formed on the metal film applied the IC chip and the core substrate to remove the portion corresponding to the transition layer, and the transition layer can then be thickened by electroplating. Afterwards, the resist can be removed and an etchant applied to form a similar transition layer on top of the IC chip pads.

[0015]

When the transition layer is formed by a subtractive process, the metal film is thickened by electroless or electrolytic plating. Types of plating that can be formed include copper, nickel, gold, silver, zinc, and iron. Copper is preferably used from the standpoint of electrical properties, economy, and the fact that the conductor layer, which is a build-up formed later, is composed primarily of copper. The thickness is preferably in the range of 1 to 20 μm . If the thickness is any greater, undercutting may occur during etching and a gap appears between the formed transition layer, the vias, and the interface. Next, an etching resist is formed, exposed, and developed, and then etching is performed to expose the metal on the

portions other than the transition layer, in order to form a transition layer on the pads of the IC chip.

[0016]

[Embodiments of the Invention]

Embodiments of the present invention will now be described with reference to the appended drawings. First, the configuration of the multilayer printed wiring substrate in the first embodiment of the present invention will be described with reference to FIG. 6, which is a cross-section of the multilayer printed wiring substrate 10.

[0017]

As shown in FIG. 6, the multilayer printed wiring substrate 10 includes a core substrate 30 housing an IC chip 20, an interlayer resin insulating layer 50, and another interlayer resin insulating layer 150. Vias 60 and a conductor circuit 58 are formed in an interlayer resin insulating layer 50, and vias 160 and a conductor circuit 158 are formed in interlayer resin insulating layer 150.

[0018]

The IC chip 20 is covered with an IC protective film (passivation + polyimide) 22, and die pads 24 forming input/output terminals are provided in openings in the IC protective film 22. A die transition layer 38 is formed on the pads 24.

[0019]

A solder resist layer 70 is provided on the interlayer resin insulating layer 150. The conductive circuit 158 under the openings 71 in the solder resist layer 70 are provided with solder bumps 76 or conductive connection pins (not shown) for connecting to an external substrate such as a daughterboard or motherboard (not shown).

[0020]

In the multilayer printed wiring substrate 10 of the present embodiment, the IC chip 20 is incorporated into the core substrate 30 beforehand, and a transition layer 38 is provided on the pads 24 of the IC chip 20. This simplifies alignment when forming the vias, and a buildup layer can be stably formed even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less. If vias in the interlayer insulating layer are formed by photoetching without a transition layer formed on the die pads, and the diameter of the vias are greater than the diameter of the die pads, the polyimide layer serving as a protective layer of the die pad surface is dissolved or damaged during de-smearing, which is performed to remove residue at the bottom of the vias and to roughen the surface of the interlayer insulating layer. When a laser is used, if the via diameter is greater than the die pad diameter, the die pads, passivation layer, and polyimide layer (protective film on the IC) are destroyed by the laser. If the pads of the IC chip are very small and the via diameter is greater than the die pad size, alignment for the photoetching or laser processing becomes difficult, and connection failures may occur between the die pad and the vias.

[0021]

In contrast, by providing a transition layer on the die pads, the vias can be reliably connected to the die pads, even when the die pad pitch is 150 μm or less and the pad size is 20 μm or less, thus improving reliability. Furthermore, by interposing a transition layer with a larger diameter on the pads of the IC chip, the die pads can be immersed in an acid or an etchant or subjected to annealing during post-processing such as de-smearing and plating with no risk of dissolving or damaging the protective films (passivation, polyimide layer) on the IC.

[0022]

Next, the method for manufacturing the multilayer printed wiring substrate described above with reference to FIG. 6 will be explained with reference to FIG. 1 to FIG. 5.

[0023]

(1) First, an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as glass cloth has been impregnated with a resin such as an epoxy is used as the starting material (see FIG. 1 (A)). Next, a recessed portion 32 for housing an IC chip is formed on one side of the core substrate 30 by counterbore processing (see FIG. 1 (B)). Here, the recessed portion is provided using counterbore processing, but a core substrate with a housing portion can be formed by stacking an insulating resin substrate with an opening on an insulating resin substrate without an opening.

[0024]

(2) Afterwards, an adhesive material 34 is applied to the recessed portion 32 using a printer. At this time, potting may also be performed. Next, the IC chip 20 is placed on the adhesive material 34 (see FIG. 1 (C)).

[0025]

(3) Then, pressure is applied to the upper surface of the IC chip 20 to store the chip completely inside the recessed portion 32 (see FIG. 1 (D)). In this way, the core substrate 30 becomes smooth.

[0026]

(4) Afterward, physical vapor deposition such as vapor deposition or sputtering is performed on the entire surface of the core substrate 30 housing the IC chip 20 to form a conductive metal film 33 on the entire surface (FIG. 2 (A)). The metal is preferably one or more layers of a metal such as tin, chromium, titanium, nickel, zinc, cobalt, gold, or copper. The thickness is preferably 0.001 to 2.0 μm . A thickness of 0.01 to 1.0 μm is especially preferable. The metal is preferably nickel, chromium, or titanium. This is because these metals do not allow moisture to penetrate from the interface, and the metal adhesion is excellent. The thickness of chromium should be set so that cracks do not occur in the sputtered layer and sufficient adhesion to the sputtered copper layer can be obtained.

[0027]

Plated film 36 may be formed on the metal film 33 by electroless plating (FIG. 2 (B)). Types of plating that can be formed include nickel, copper, gold, and silver. Copper is preferably used from the standpoint of electrical properties, economy, and the fact that the conductor layer, which is a build-up to be formed later, is primarily copper. The thickness of the plated

film should be in a range of 0.01 to 5 μm . A thickness of 0.1 to 3 μm is especially preferable. Preferred combinations of the first thin film layer and second thin film layer include chromium-copper, chromium-nickel, titanium-copper, and titanium-nickel. These combinations are superior to other combinations in terms of bondability with metals and electrical conductivity.

[0028]

(5) Afterward, a resist is applied or photosensitive film is laminated. This is exposed and developed to form a plating resist 35 in order to form openings above the pads of the IC chip, and an electrolytic plated film 37 is formed (FIG. 2 (C)). The thickness of the electrolytic plated film 37 is preferably about 1 to 20 μm . The film can be formed of nickel, copper, gold, silver, zinc, or iron. After removing the plating resist 35, the electroless plated film 36 and the metal film 33 underneath the plating resist 35 are removed by etching to form a transition layer 38 on the pads 24 of the IC chip (FIG. 2(D)). Here, the transition layer is formed by a plating resist. However, a transition layer may be formed on the pads of the IC chip by uniformly forming electrolytic plated film on the electroless plated film 36, and then forming an etching resist, which is exposed and developed to form portions other than the transition layer to expose and etch the metal. In this case, the thickness of the electroplated film should be in a range of 1 to 20 μm . This is because if the thickness is greater, undercutting may occur during etching, and a gap may occur at the interface between the formed transition layer and the vias.

[0029]

(6) Next, an etchant is sprayed onto the substrate to etch the surface of the transition layer 38 and form a roughened surface 38a (see FIG. 3 (A)). A roughened surface can also be formed using electroless plating or oxidation-reduction treatment.

[0030]

(7) A thermosetting cycloolefin resin sheet having a thickness of 30 to 50 μm is laminated on the substrate that has undergone the steps described above under vacuum at a pressure of 5 kg/cm^2 while raising the temperature to 50 to 150°C, resulting in an interlayer resin insulating layer 50 made of a cycloolefin resin (see FIG. 3 (B)). The degree of vacuum during the vacuum pressure bonding is 10 mmHg. Alternatively, the insulating layer may be formed by applying a liquid insulating resin using spin coating.

[0031]

(8) Next, via openings 48 are formed in the interlayer resin insulating layer 50 using a CO_2 gas laser (see FIG. 3 (C)). Chromic acid is used to remove the resin residue in the openings 48. Here, alignment during via formation is simplified and the vias on the die pads 24 are positively connected, thus improving connectivity and reliability between pads and vias, by providing a transition layer 38 made of copper on the die pads 24. Afterward, a buildup layer can be stably formed. By interposing a larger diameter transition layer on the pads of the IC chip, the protective film (passivation, polyimide layer) 22 on the die pads 24 of the IC is no longer at risk of dissolution or damage by immersion in an acid or an etchant or annealing during post-processing such as plating or de-smearing performed to remove the residue at the bottom of the vias and roughen the surface of the interlayer resin insulating layer. Here, permanganic acid can be used for resin residue removal, and oxygen plasma can be used for de-smearing.

[0032]

(9) Next, the surface of the interlayer resin insulating layer 50 is roughened to form a roughened surface 50a (see FIG. 3 (D)). Note that this roughening step can be omitted.

[0033]

(10) Next, after applying a palladium catalyst to the surface of the interlayer resin insulating layer 50, the substrate is immersed in an electroless plating solution to form an electroless plated film 52 on the surface of interlayer resin insulating layer 50 (FIG. 4 (A)).

[0034]

(11) A commercially available photosensitive dry film is then affixed to the processed substrate 30, and a chrome glass mask is placed on top, which is exposed at 40 mJ/cm² and developed with 0.8% sodium carbonate to provide a plating resist 54 with a thickness of 25 μm. Next, electrolytic plating is performed under the conditions listed below to form an electrolytic plated film 56 with a thickness of 18 μm (see FIG. 4 (B)). The additive in the electrolytic plating aqueous solution is Capracid HL from Atotech Japan.

[0035]

[Electroplating aqueous solution]

Sulfuric acid	2.24 mol/L
Copper sulfate	0.26 mol/L
Additive (Capalacid HL from Atotech Japan)	19.5 mL/L

[Electroplating conditions]

Current density	1 A/dm ²
Time	65 min.
Temperature	22 ± 2°C

[0036]

(12) After removing the plating resist 54 with 5% NaOH, the electroless plated film 52 under the plating resist is dissolved and removed by etching using a mixed solution of nitric acid, sulfuric acid, and hydrogen peroxide. This forms a conductor circuit 58 and vias 60 with a thickness of 16 μm made of the electroless plated film 52 and electrolytic plated film 56. Roughened surfaces 58a, 60a are then formed using an etchant containing a dicopper complex and an organic acid (FIG. 4 (C)).

[0037]

(13) Next, steps (8) to (13) are repeated to form additional interlayer resin insulating layers 150 and conductor circuits 158 (including vias 160) on top (see FIG. 5 (A)).

[0038]

(14) Next, 46.67 parts by weight of a photosensitive oligomer (molecular weight 4,000) with photosensitivity imparted by acrylation of 50% of the epoxy groups in a cresol novolac epoxy resin (from Nippon Kayaku) dissolved in diethylene glycol dimethyl ether (DMDG) to a

concentration of 60 wt%; 15 parts by weight of a 80 wt% bisphenol A-type epoxy resin (Epicoat 1001 from Yuka Shell) dissolved in methyl ethyl ketone; 1.6 parts by weight of an imidazole curing agent (2E4MZ-CN from Shikoku Kasei); 3 parts by weight of a polyfunctional acrylic monomer (R604 from Kyoei Chemical); 1.5 parts by weight of a similarly polyvalent acrylic monomer (DPE6A from Kyoei Chemical); and 0.71 parts by weight of a dispersion antifoaming agent (S-65 from San Nopco) are placed in a container, and then stirred and mixed to prepare a mixed composition, to which 2.0 parts by weight of benzophenone (from Kanto Chemical) serving as a photopolymer initiator and 0.2 parts by weight of Michler's ketone (from Kanto Chemical) serving as a photosensitizer are added to obtain a solder resist composition (organic resin insulating material) with a viscosity adjusted to 2.0 Pa·s at 25°C. The viscosity is measured using a B-type viscometer (DVL- B from Tokyo Keiki) using rotor No. 4 at 60 rpm and rotor No. 3 at 6 rpm.

[0039]

(15) Next, the solder resist composition is applied to a thickness of 20 μm on the substrate 30, and dried at 70°C for 20 minutes and at 70 C for 30 minutes. A 5 mm-thick patterned photomask is brought into close contact with the solder resist layer 70, exposed to ultraviolet rays of 1000 mJ/cm², and developed with a DMTG solution to form openings 71 with a land diameter of 620 μm and an opening diameter of 460 μm . (See FIG. 5 (B)).

[0040]

(16) Next, the substrate on which the solder resist layer (organic resin insulating layer) 70 has been formed is coated with nickel chloride (2.3×10^{-1} mol/L), sodium hypophosphate (2.8×10^{-1} mol/L), and sodium citrate (1.6×10^{-1} mol/L) in an electroless nickel plating solution with a pH of 4.5 for 20 minutes to form a 5 μm -thick nickel plating layer 72 in the openings 71. The substrate is then immersed in an electroless plating solution containing potassium gold cyanide (7.6×10^{-3} mol/L), ammonium chloride (1.9×10^{-1} mol/L), sodium citrate (1.2×10^{-1} mol/L), and sodium hypophosphite (1.7×10^{-1} mol/L) at 80°C for 7.5 minutes to form a gold plating layer 74 with a thickness of 0.03 μm on the nickel plating layer 72, and solder pads 75 on the conductor circuit 158 (see FIG. 5 (C)).

[0041]

(17) Afterward, solder paste is printed in the openings 71 of the solder resist layer 70 and reflowed at 200°C to form solder bumps 76. As a result, a multilayer printed wiring substrate 10 containing the IC chip 20 and having solder bumps 76 can be obtained (see FIG. 6). Conductive connection pins may also be provided by printing solder paste.

[0042]

In the embodiment described above, thermosetting cycloolefin resin sheets are used for the interlayer resin insulating layers 50, 150. However, an epoxy resin can be used for the interlayer resin insulating layer 50 instead. This epoxy resin contains a poorly soluble resin, soluble particles, a curing agent, and other components. Each component will now be described.

[0043]

The epoxy resin that can be used in the manufacturing method of the present invention is composed of particles that are soluble in acids or oxidizing agents ("soluble particles" below) dispersed in a resin that is poorly soluble in acids or oxidizing agents ("poorly soluble resin")

below). The terms "poorly soluble" and "soluble" used in the present invention refer to materials that have a relatively high dissolution rate when immersed in a solution containing a given acid or oxidizing agent over a given period of time. For the sake of convenience, those with a relatively slow dissolution rate are referred to as "poorly soluble."

[0044]

Examples of soluble particles include resin particles soluble in acids or oxidants ("soluble resin particles" below), inorganic particles soluble in acids or oxidants ("soluble inorganic particles" below), and metal particles soluble in acids or oxidants ("soluble metal particles" below). These soluble particles may be used alone or in combinations of two or more.

[0045]

The shape of the soluble particles is not particularly limited, which may be spherical, crushed, etc. However, it is desirable that the soluble particles have a uniform shape. This is because a roughened surface with uniform roughness can be formed.

[0046]

The average particle diameter of the soluble particles is preferably 0.1 to 10 μm . Particles with two or more particle sizes within this range may be included. In other words, this particle size range includes, for example, soluble particles with an average particle size of 0.1 to 0.5 μm and soluble particles with an average particle size of 1 to 3 μm . As a result, a more complicated roughened surface can be formed, facilitating excellent adhesiveness to the conductive circuit. In the present invention, the particle diameter of the soluble particles is the length of the longest portion of the soluble particles.

[0047]

Examples of soluble resin particles include, but are not limited to, those composed of thermosetting resins and thermoplastic resins, and those having a faster dissolution rate than the poorly soluble resin when immersed in a solution composed of an acid or an oxidizing agent. Specific examples of soluble resin particles include those composed of epoxy resins, phenol resins, polyimide resins, polyphenylene resins, polyolefin resins, and fluorine resins, and the particles may be composed of one of these resins or a mixture of two or more of these resins.

[0048]

Resin particles composed of rubber can also be used as the soluble resin particles. Examples of rubbers include polybutadiene rubber, modified polybutadiene rubbers such as epoxy-modified, urethane-modified, and (meth)acrylonitrile-modified rubbers, and carboxyl group-containing (meth)acrylonitrile-butadiene rubber. The use of rubber makes the soluble resin particles more soluble in acids or oxidizing agents. In other words, when the soluble resin particles are dissolved in acid, an acid other than a strong acid can be used, and when the soluble resin particles are dissolved using an oxidizing agent, a permanganate with relatively low oxidizing capability may be used. Even when chromic acid is used, dissolving can be performed at a low concentration. As a result, no acid or oxidizing agent remains on the resin surface and, as described below, when a catalyst such as palladium chloride is applied to the roughened surface, there is no risk of the catalyst not being applied or the catalyst not being oxidized.

[0049]

Examples of soluble inorganic particles include particles made of at least one type selected from the group consisting of aluminum compounds, calcium compounds, potassium compounds, magnesium compounds, and silicon compounds.

[0050]

Examples of aluminum compounds include alumina, and aluminum hydroxide. Examples of calcium compounds include calcium carbonate and calcium hydroxide. An example of a potassium compounds is potassium carbonate. Examples of magnesium compounds include magnesite, dolomite, and basic magnesium carbonate, and examples of silicon compounds include silica and zeolite. These may be used alone or in combinations of two or more.

[0051]

Examples of soluble metal particles include particles made of at least one type selected from the group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, calcium, and silicon. These soluble metal particles may be coated with a resin to ensure insulating properties.

[0052]

When two or more types of soluble particles are mixed together and used, a combination of resin particles and inorganic particles is preferred as the combination of the two types of soluble particles mixed together. This is because both soluble types of particles have low conductivity, ensuring that the resin film has insulating properties, and thermal expansion can be easily adjusted with a poorly soluble resin, keeping delamination from occurring between the interlayer resin insulating layers and the conductor circuits.

[0053]

The poorly soluble resin is not particularly limited as long as it can maintain the shape of the roughened surface when a roughened surface is formed on the interlayer resin insulating layer using an acid or an oxidizing agent. Examples include resins, thermoplastic resins, and composites thereof. Photosensitive resins obtained by imparting photosensitivity to these resins may also be used. By using a photosensitive resin, the interlayer resin insulating layer can be exposed and developed to form openings for the vias. Among these examples, those containing a thermosetting resin are preferred. This is because the shape of the roughened surface can be maintained even when exposed to a plating solution or various heat treatments.

[0054]

Specific examples of poorly soluble resins include epoxy resins, phenolic resins, phenoxy resins, polyimide resins, polyphenylene resins, polyolefin resins, and fluorine resins. These resins may be used alone or in combinations of two or more. A thermosetting resin, a thermoplastic resin, or a composite thereof may be used. An epoxy resin having two or more epoxy groups per molecule is more preferred. This is because in addition to being able to form a roughened surface, it provides excellent heat resistance so that stress concentration does not occur in the metal layer even under heat cycle conditions, and delamination of the metal layer is less likely to occur.

[0055]

Examples of epoxy resins include cresol novolak-type epoxy resins, bisphenol A-type epoxy resins, bisphenol F-type epoxy resins, phenol novolac type epoxy resins, alkylphenol novolak-type epoxy resins, bisphenol F-type epoxy resins, naphthalene-type epoxy resins, dicyclopentadiene-type epoxy resins, epoxidized condensates of phenols and aromatic aldehydes with phenolic hydroxyl groups, triglycidyl isocyanurate, and alicyclic epoxy resins. These may be used alone or in combinations of two or more. As a result, these provide excellent heat resistance.

[0056]

In the resin film used in the present invention, the soluble particles are preferably dispersed almost uniformly in the poorly soluble resin. This is because a roughened surface with uniform roughness can be formed, and even if vias or through-holes are formed in the resin film, the adhesion of the metal layer of the conductive circuit formed thereupon can be ensured. Also, a resin film containing soluble particles only in the surface layer forming the roughened surface may be used. As a result, the portions other than the surface layer of the resin film are not exposed to the acid or the oxidizing agent, and insulation between the conductor circuits via the interlayer resin insulating layers is reliably maintained.

[0057]

In the resin film, the amount of the soluble particles dispersed in the poorly soluble resin is preferably 3 to 40 wt% of the resin film. If the amount of soluble particles is less than 3 wt%, it may not be possible to form a roughened surface with the desired unevenness. If the amount exceeds 40 wt%, the soluble particles are dissolved by acid or oxidation deep in the resin film, making it difficult to maintain insulation between conductor circuits via an interlayer resin insulating layer made of this resin film, and making short circuits more likely.

[0058]

In addition the soluble particles and poorly soluble resins mentioned above, the resin film preferably contains a curing agent, etc. Examples of curing agents include imidazole-based curing agents, amine-based curing agents, guanidine-based curing agents, epoxy adducts of these curing agents, microencapsulated products of these curing agents, triphenylphosphine, and organic phosphine compounds such as tetraphenylphosphonium-tetraphenylborate.

[0059]

The amount of the curing agent is preferably 0.05 to 10 wt% relative to the weight of the resin film. If the amount added is less than 0.05 wt%, curing of the resin film becomes insufficient, and penetration of the acid or oxidizing agent into the resin film increases, potentially impairing the insulating properties of the resin film. However, if the amount exceeds 10 wt%, the excessive amount of curing agent may modify the composition of the resin, which may lead to a decrease in reliability.

[0060]

Examples of other components that can be added include fillers such as inorganic compounds and resins that do not affect the formation of the roughened surface. Examples

of inorganic compounds include silica, alumina, and dolomite, and examples of resins include polyimide resins, polyacrylic resins, polyamideimide resins, polyphenylene resins, melanin resins, and olefin resins. By including these fillers, the performance of the multilayer printed wiring substrate can be improved by matching the coefficient of thermal expansion and improving heat resistance and chemical resistance.

[0061]

The resin film may also contain a solvent. Examples of solvents include ketones such as acetone, methyl ethyl ketone and cyclohexanone, ethyl acetate, butyl acetate, cellosolve acetate, and aromatic hydrocarbons such as toluene and xylene. These may be used alone or in combinations of two or more. However, the resulting interlayer resin insulating layer melts and is carbonized when a temperature of 350°C or higher is applied.

[0062]

After the resin film has been attached, a laser is used to open vias in the interlayer resin insulating layer. Afterward, the interlayer resin insulating layer is immersed in an acid or an oxidizing agent to form a roughened layer. A strong acid such as sulfuric acid, phosphoric acid, hydrochloric acid, or formic acid can be used as the acid, and chromic acid, chromic sulfuric acid, or permanganate can be used as the oxidizing agent. In this way, a roughened layer is formed on the surface of the interlayer resin insulating layer by dissolving or dislodging soluble particles. After applying a catalyst such as Pb to the interlayer resin insulating layer on which a roughened surface has been formed, electroless plating is performed. A resist is applied to the electroless plated film, which is then exposed to light and developed to form unformed portions in the plating resist. Electroplating is applied to the unformed portions to remove the resist, and the electroless plated film on the interlayer resin insulating layer is removed by etching to form vias and a conductor circuit.

[0063]

FIG. 7 (A) is a perspective view of the multilayer printed wiring substrate in the first embodiment and FIG. 7 (B) is an enlarged explanatory view of the multilayer printed wiring substrate. Solder bumps (a ball grid array) 76 are arranged in a houndstooth pattern over the entire surface of the multilayer printed wiring substrate 10 in the first embodiment. In the first embodiment, the wiring length from the IC chip 20 can be shortened by forming solder bumps 76 on the IC chip 20 as well.

[0064]

FIG. 8 (A) is a perspective view of the multilayer printed wiring substrate 10 in a modified example of the first embodiment and FIG. 8 (B) is an enlarged explanatory view of the multilayer printed wiring substrate 10. Solder bumps (a ball grid array) 76 are arranged in a houndstooth pattern on the surface of the multilayer printed wiring substrate 10 of the modified example excluding the rectangular top of the IC chip 20. The solder bumps 76 in this modified example are less susceptible to thermal and electromagnetic influences from the IC chip by avoiding the top of the IC chip 20.

[0065]

A multilayer printed wiring substrate in another modified example of the first embodiment of the present invention will now be described with reference to FIG. 9. In the first embodiment described above, a ball grid array (BGA) is provided. The second embodiment

is substantially the same as the first embodiment, but has a pin grid array (PGA) in which connections are made via conductive connection pins 96 as shown in FIG. 9.

[0066]

Next, a multilayer printed wiring substrate in a second embodiment of the invention will be described with reference to FIG. 10. In the first embodiment, the IC chip is housed in a recessed portion 32 provided in the core substrate 30 by performing counterboring. In contrast, in the second embodiment, the IC chip 20 is housed in a through-hole 32 formed in the core substrate 30. In the second embodiment, the IC chip 20 can be efficiently cooled because a heat sink can be attached directly to the back side of the IC chip 20.

[0067]

Next, a multilayer printed wiring substrate in a third embodiment of the invention will be described with reference to FIG. 11. In the first embodiment described above, the transition layer 38 is formed on the pads 24 of the IC chip 20 and vias 60 in the interlayer resin insulating layer 50 are connected to the transition layer 38. In contrast, in the third embodiment, the vias 60 are connected directly to the pads 24 without providing a transition layer. Because the third embodiment can reduce the number of manufacturing steps compared to the first embodiment, it is less expensive.

[0068]

Next, a multilayer printed wiring substrate in a fourth embodiment of the invention will be described with reference to FIG. 12. In the first embodiment described above, an IC chip is housed in the multilayer printed wiring substrate. In contrast, in the fourth embodiment, an IC chip 20 is housed in the multilayer printed wiring substrate and another IC chip 120 is mounted on the surface of the substrate. Here, a computational CPU is the IC chip 20 housed inside, and a cache memory is the IC chip 120 mounted on the surface.

[0069]

The pads 24 of IC chip 20 and the pads 124 of IC chip 120 are connected by means of transition layers 38, vias 60, a conductor circuit 58, vias 160, another conductor circuit 158, and solder bumps 76U.

Meanwhile, the pads 124 of IC chip 120 and the pads 92 of a daughterboard 90 are connected by means of solder bumps 76U, a conductor circuit 158, vias 160, another conductor circuit 58, vias 60, through-holes 136, vias 60, another conductor circuit 58, vias 160, another conductor circuit 158, and solder bumps 76U.

[0070]

In the fourth embodiment, an IC chip 20 and a cache memory 120 can be arranged close to each other while the low-yield cache memory 120 is manufactured separately from the IC chip 20 for the CPU, enabling high-speed operation of the IC chip. In the fourth embodiment, by embedding an IC chip and placing an IC chip on the surface, electronic components such as IC chips with different functions can be mounted, thereby obtaining a multi-layer printed wiring substrate with higher functionality. Although not shown, a capacitor can also be mounted on the surface. As a result, the IC chip 20, the cache memory 120, and the capacitor can be arranged close to each other, enabling high-speed operation of the IC chip.

[0071]

[Effect of the Invention]

The structure of the present invention can be used to establish a connection between an IC chip and a printed wiring substrate without a lead component. As a result, resin sealing becomes unnecessary. Also, by providing a transition layer on the die pads, buildup layers can be stacked even when the die pads have a fine pitch (150 μm) and/or a small size (20 μm or less), and connectivity between and reliability of the die pads and via holes can be improved. Compared to the conventional IC chip mounting methods, the wiring length running from an IC chip through a substrate to an external substrate can be shortened, and the loop inductance can be reduced.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 (A), (B), (C), and (D) are diagrams showing manufacturing steps for the multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 2]

FIG. 2 (A), (B), (C), and (D) are diagrams showing manufacturing steps for the multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 3]

FIG. 3 (A), (B), (C), and (D) are diagrams showing manufacturing steps for the multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 4]

FIG. 4 (A), (B), and (C) are diagrams showing manufacturing steps for the multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 5]

FIG. 5 (A), (B), and (C) are diagrams showing manufacturing steps for the multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 6]

FIG. 6 is a cross-sectional view of a multilayer printed wiring substrate in the first embodiment of the present invention.

[FIG. 7]

FIG. 7 (A) is a perspective view of the multilayer printed wiring substrate in the first embodiment and FIG. 7 (B) is an enlarged explanatory view of the multilayer printed wiring substrate.

[FIG. 8]

FIG. 8 (A) is a perspective view of the multilayer printed wiring substrate in a modified example of the first embodiment and FIG. 8 (B) is an enlarged explanatory view of the multilayer printed wiring substrate.

[FIG. 9]

FIG. 9 is a cross-sectional view of a multilayer printed wiring substrate in a modified example of the first embodiment of the present invention.

[FIG. 10]

FIG. 10 is a cross-sectional view of a multilayer printed wiring substrate in the second embodiment of the present invention.

[FIG. 11]

FIG. 11 is a cross-sectional view of a multilayer printed wiring substrate in the third embodiment of the present invention.

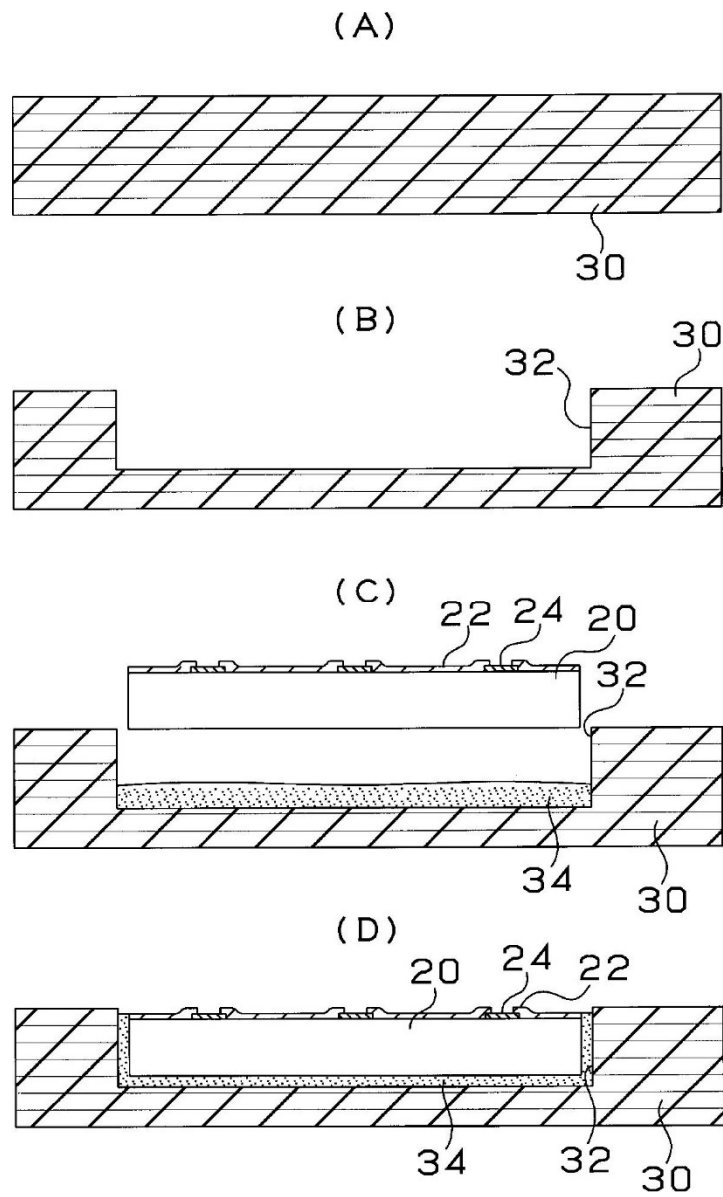
[FIG. 12]

FIG. 12 is a cross-sectional view of the multilayer printed wiring substrate in the fourth embodiment of the present invention.

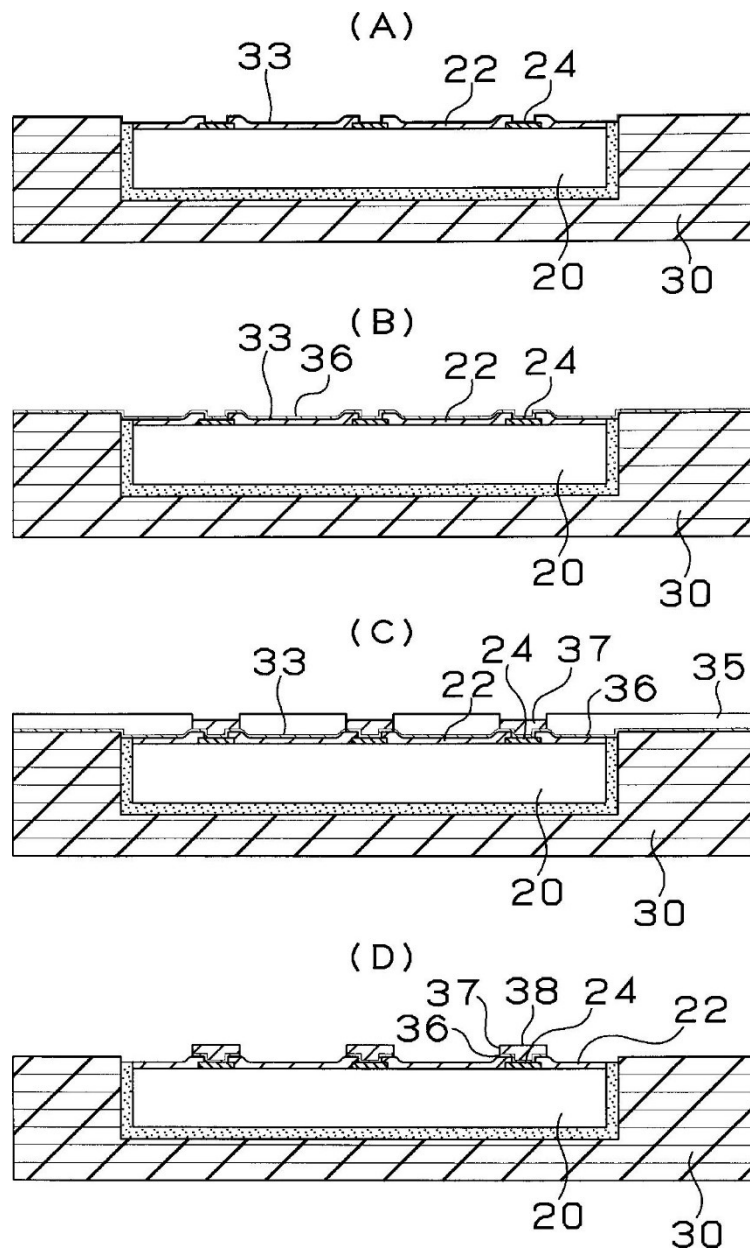
[Reference Numbers]

20: IC chip (electronic component)
 24: Pad
 30: Core substrate
 32: Recessed portion
 36: Resin layer
 38: Transition layer
 50: Interlayer resin insulating layer
 58: Conductor circuit
 60: Via
 70: Solder resist layer
 76: Solder bump (terminal)
 90: Daughter board (external substrate)
 96: Conductive connection pins (terminals)
 97: Conductive adhesive
 120: IC chip (electronic component)
 150: Interlayer resin insulating layer
 158: Conductor circuit
 160: Via

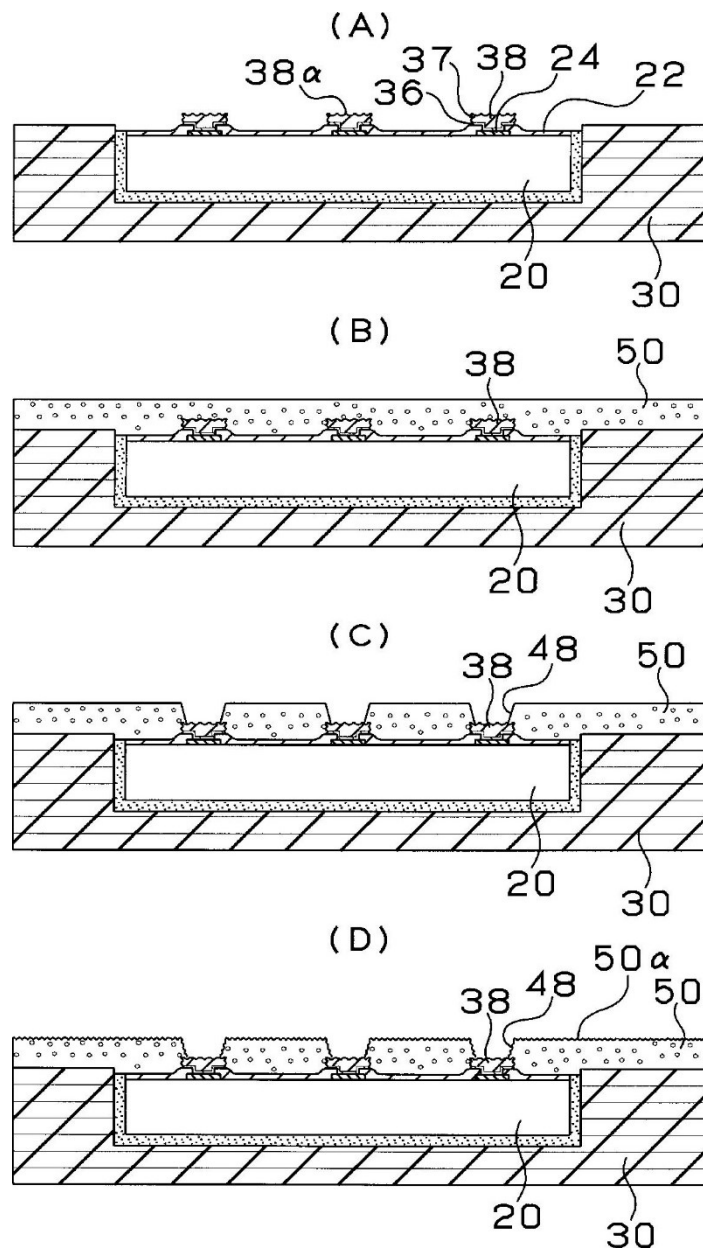
[FIG. 1]



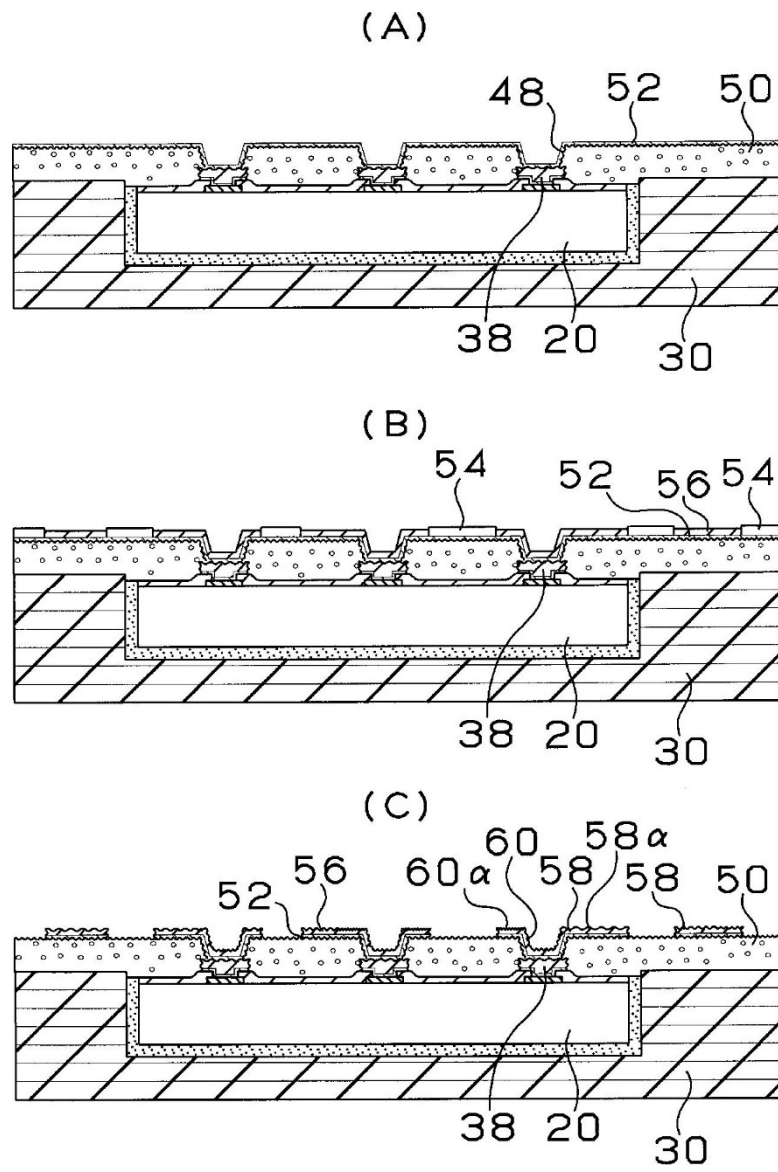
[FIG. 2]



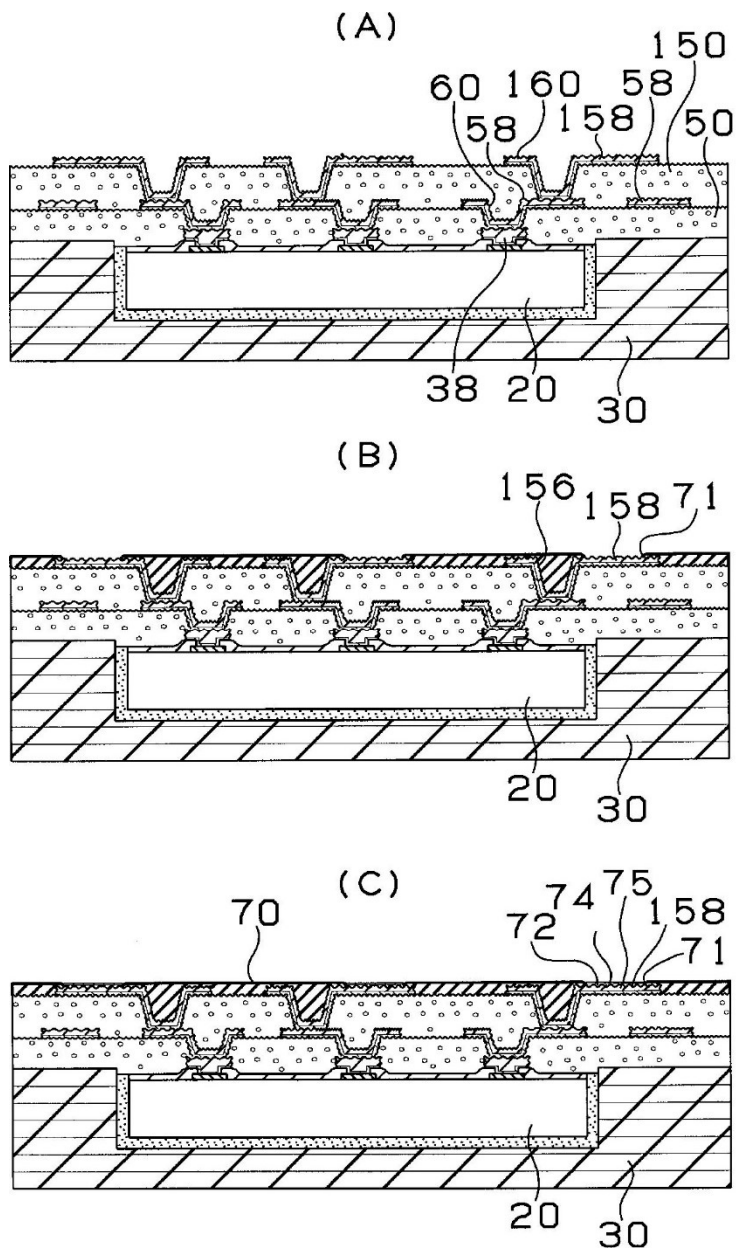
[FIG. 3]



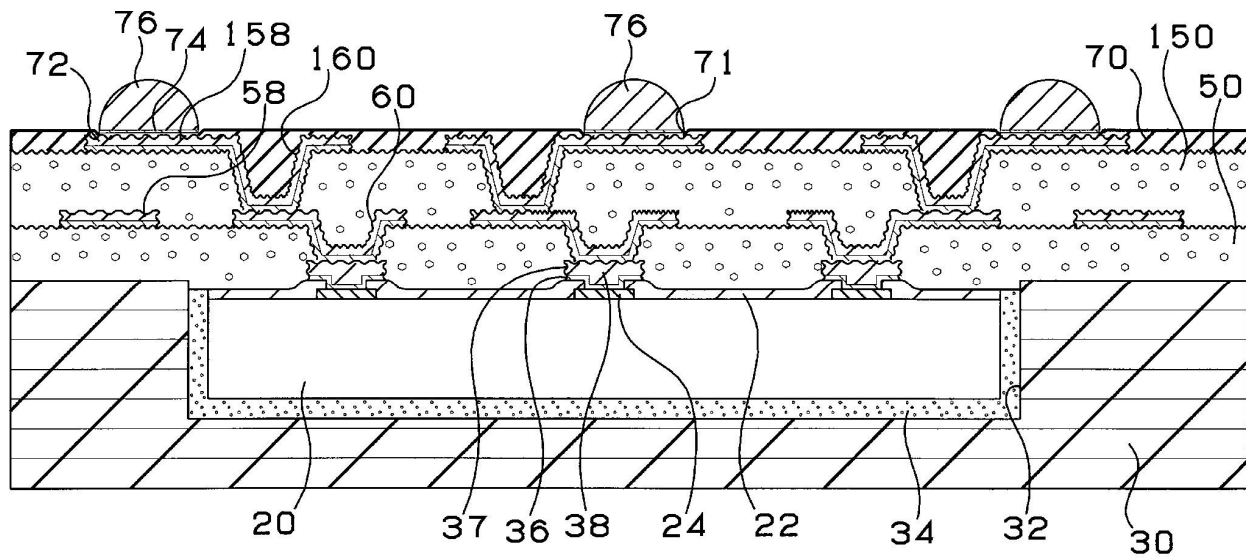
[FIG. 4]



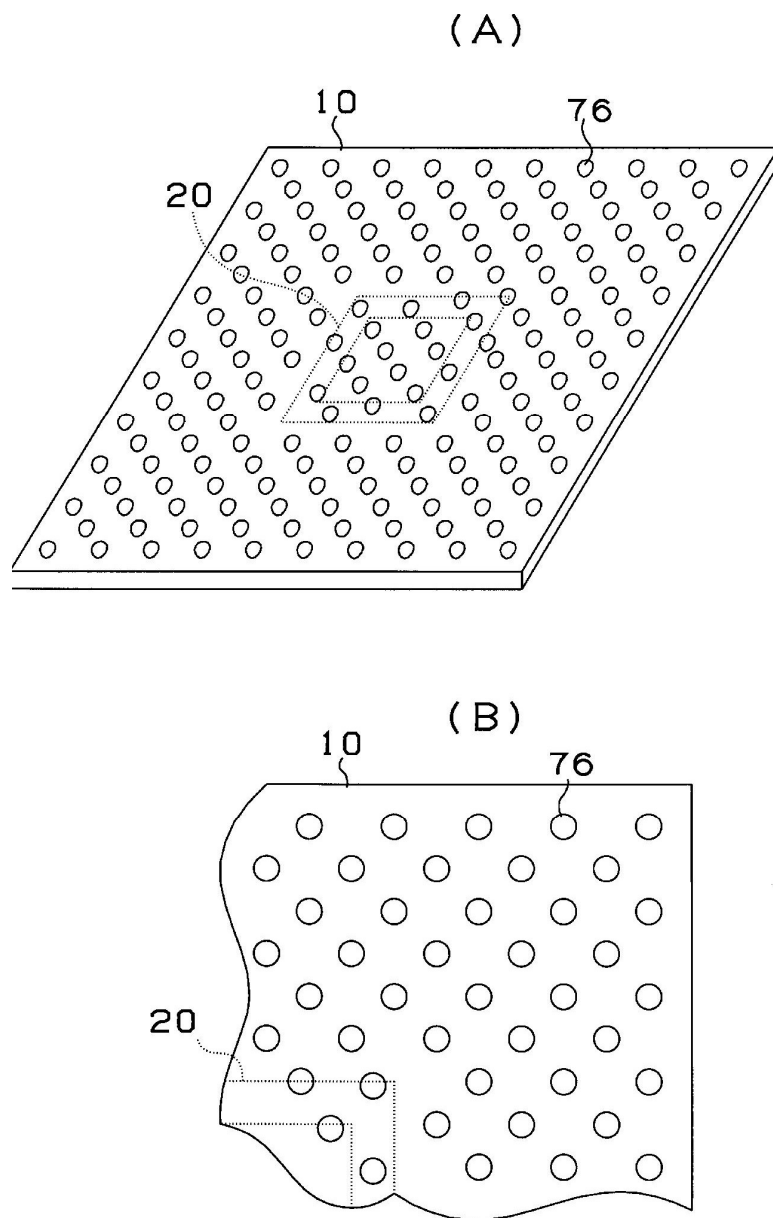
[FIG. 5]



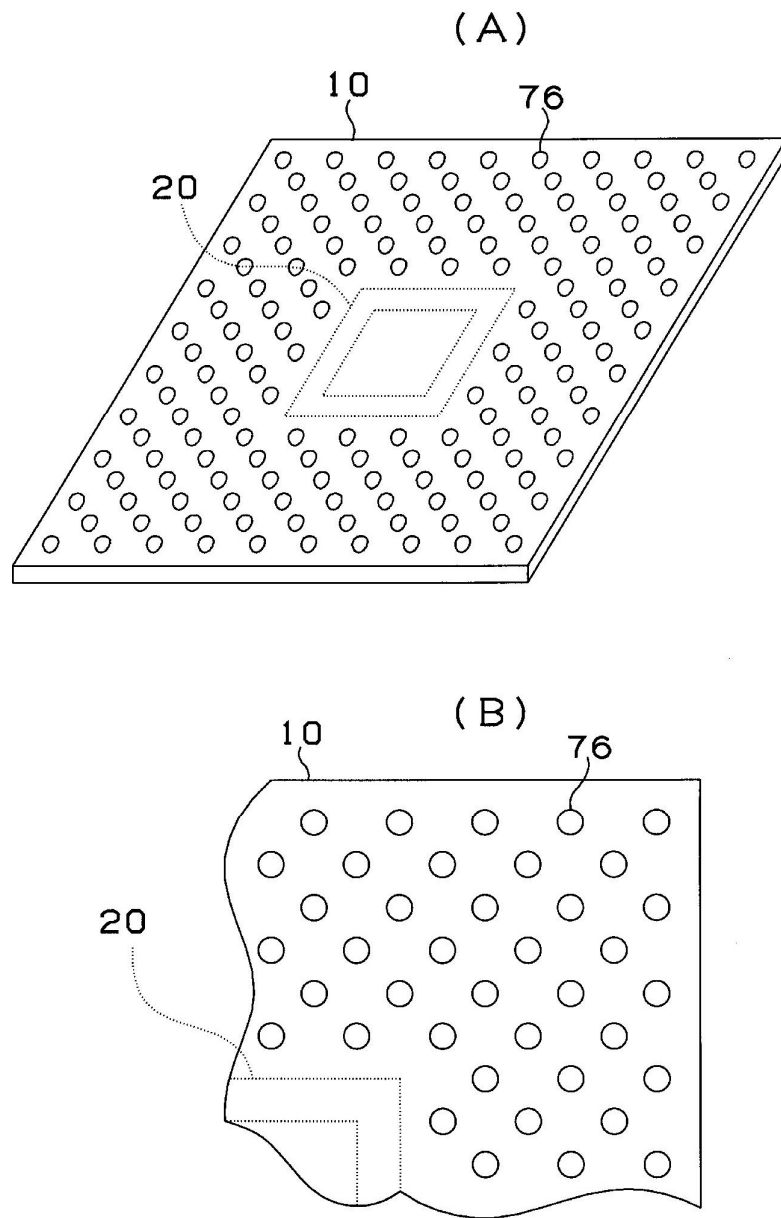
[FIG. 6]



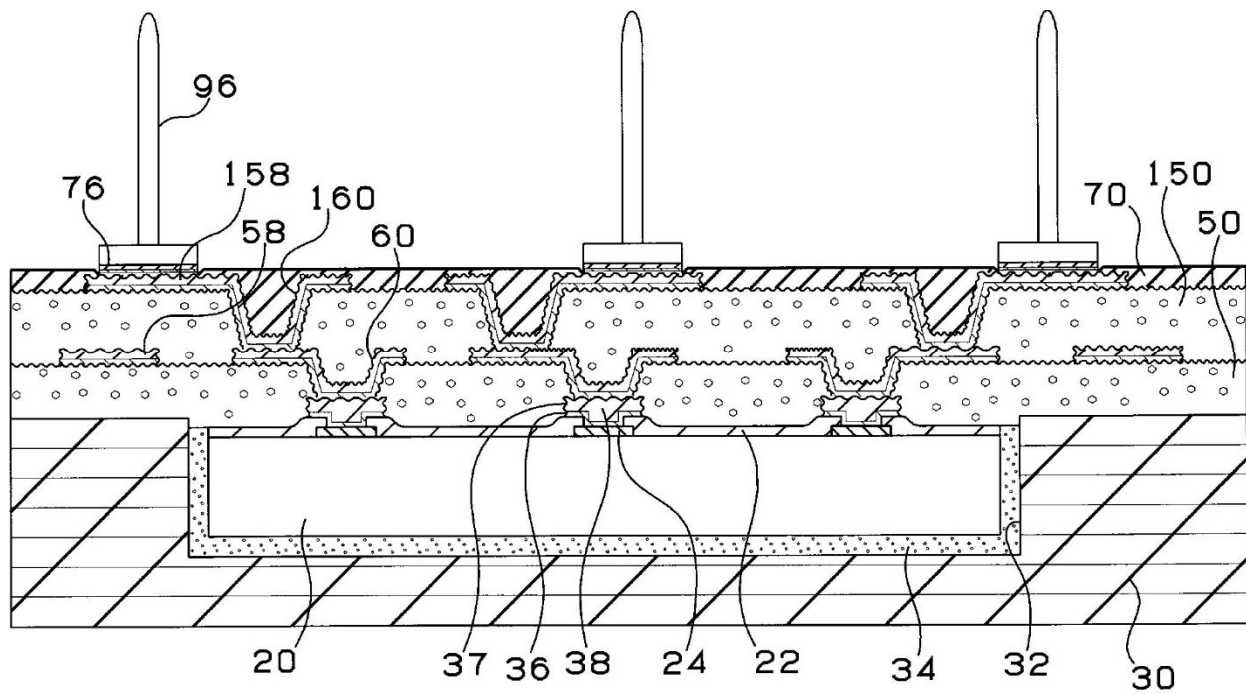
[FIG. 7]



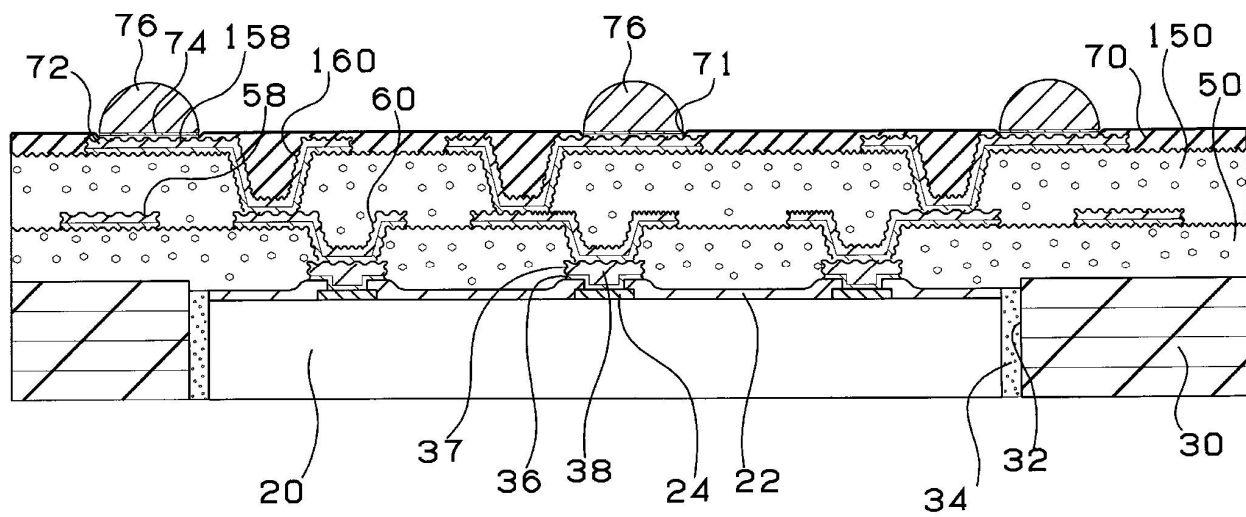
[FIG. 8]



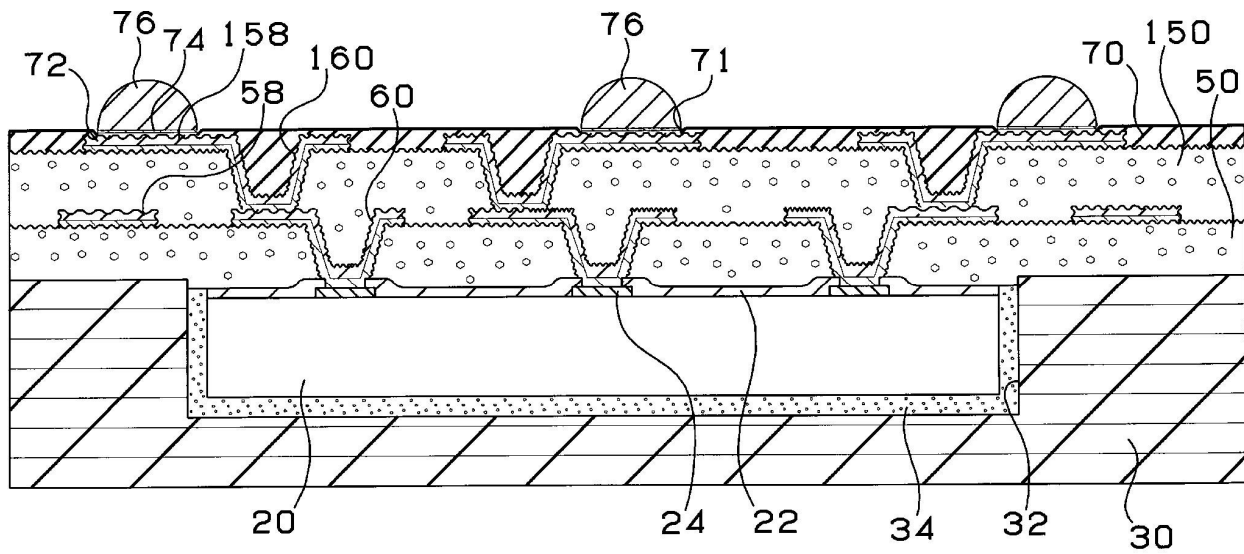
[FIG. 9]



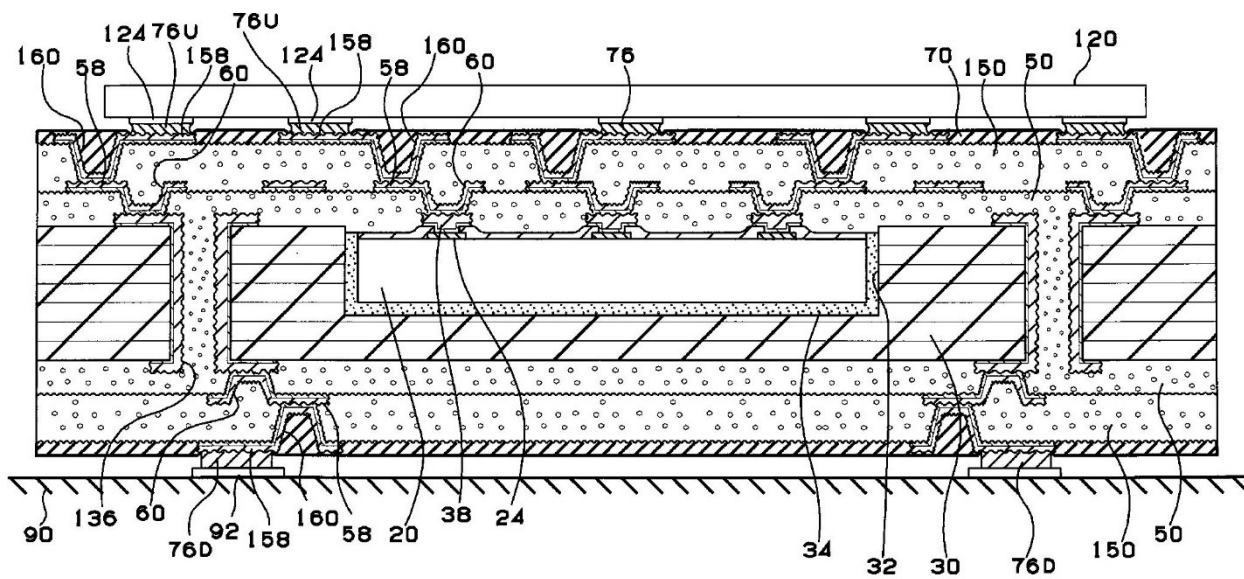
[FIG. 10]



[FIG. 11]



[FIG. 12]



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(51) [Int.Cl.⁷]

[FI] H01L 23/12 F

(72) [Inventor]

[Name] WANG Dongdong

[Address] Ibiden Co., Ltd., Ogaki Kita Plant, 1-1, Kitagata, Ibigawa-cho, Ibi-gun, Gifu-ken

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