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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

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(71) Applicant 000004547
NGK Spark Plug Co., Ltd.
14-18, Takatsujicho, Mizuho-ku, Nagoya-shi, Aichi-ken

(72) Inventor
Eiji KODERA
NGK Spark Plug Co., Ltd., 14-18, Takatsujicho, Mizuho-ku, Nagoya-shi, Aichi-ken

(72) Inventor
Koju OGAWA
NGK Spark Plug Co., Ltd., 14-18, Takatsujicho, Mizuho-ku, Nagoya-shi, Aichi-ken

(74) Agent 100098615
Manabu SUZUKI

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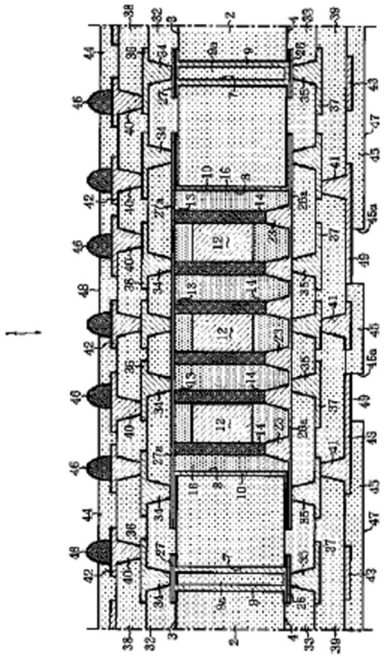
(54) [Title of the Invention]
Wiring Substrate and Manufacturing Method Therefor

(57) [Abstract]
[Problem] To provide a wiring substrate in which the electronic components built into an insulating substrate are less susceptible to external electromagnetic waves, which can reduce the effects of noise generated by the circuits constituting these electronic components, and which can stabilize the electrical characteristics inside the wiring substrate and conductivity with the wiring layers and IC chips mounted on the first main surface, and to provide a method for manufacturing such a wiring substrate.
[Solution] Provided is a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded, in which a chip capacitor (electronic component) 12 inserted into the through-hole 8 is secured via a resin 16 and thereby built-into the insulating substrate 2, and in which wiring layers 26, 27, etc. electrically connected to the electrodes 13, 14 of the capacitor 12 are formed on the upper and lower sides of the insulating substrate 2.



[Claims]

[Claim 1] A wiring substrate characterized in that a shielding layer is formed an the inner surface of a through-hole or recessed portion in an insulating substrate in which an electronic component has been embedded.

[Claim 2] The wiring substrate according to claim 1, wherein the electronic component is embedded in the through-hole or recessed portion via a resin.

[Claim 3] The wiring substrate according to claim 1 or 2, wherein a shielding layer is also formed in an opening to the through-hole or recessed portion.

[Claim 4] The wiring substrate according to claim 2 or 3, wherein a wiring layer that is connected electrically to the electrodes of the embedded electronic component is formed on at least one of the top and bottom of the insulating substrate.

[Claim 5] The wiring substrate according to claim 4, wherein the wiring of the wiring layer at a position covering the opening to the through-hole or recessed portion in the insulating substrate also serves as the shielding layer.

[Claim 6] A method for manufacturing a wiring substrate, the method comprising the steps of: forming a through-hole or recessed portion in an insulating substrate for embedding an electronic component; and forming a shielding layer on the inner surface of the through-hole or recessed portion by plating.

[Claim 7] The method for manufacturing the wiring substrate according to claim 6, the method comprising the steps of: inserting an electronic component into the through-hole or recessed portion after the step of forming the shielding layer; and filling the through-hole or recessed portion into which the electronic component has been inserted with a resin and solidifying the resin.

[Claim 8] The method for manufacturing the wiring substrate according to claim 7, the method further comprising the step of: forming a wiring layer that is electrically connected to the electrodes of the embedded electronic component on at least one of the top and bottom of the insulating substrate after the step of filling with and solidifying the resin.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention] The present invention relates to a wiring substrate in which an electronic component has been fixed to and embedded in an insulating substrate, and to a method for manufacturing the same.

[0002]

[Prior Art]

In response to the increasing size reduction in wiring substrates and the increasing density of wiring in wiring substrates in recent years, a wiring substrate has been proposed in which electronic components are embedded inside an insulating substrate in addition to mounting electronic components such as IC chips on the first main surface of the wiring substrate. For example, in the wiring substrate 100 shown in FIG. 8(A), a chip capacitor (electronic component) 103 is inserted into a through-hole 102 passing through an insulating substrate 101, and electrodes 104 at both ends of the capacitor are connected to a land 107 formed between the substrate 101 and an adjacent insulating layer 106 via solder 108. The capacitor 103 is then secured and embedded by filling the through-hole 102 with a resin 109. Internal electrodes 105 are provided inside this capacitor 103.

[0003] In the wiring substrate 110 shown in FIG. 8(B), one opening to the through-hole 112 passing through the insulating substrate 111 is pre-filled with an adhesive temporary securing film not shown in the figure, and the through-hole 112 is filled with a resin 119 and the resin is solidified with the chip capacitor (electronic component) 113 with internal electrodes 115 affixed to the temporary securing film. Afterward, the temporary securing film is removed. In this wiring substrate 110, electrodes 114 located at both ends of the capacitor 113 are connected via solder 118 to lands 117, 117 previously provided between the insulating substrate 111 and an adjacent insulating layer 116.

[0004] However, in the wiring substrate 100 in FIG. 8(A), because the through-hole 102 with the embedded capacitor 103 is surrounded by the insulating substrate 101 and an insulating layer 106 via a resin 109, radio waves and magnetic fields ("electromagnetic waves" below) from the outside can easily cause malfunctions, and the electrical characteristics inside the wiring substrate 100 can become unstable. Also, in the wiring substrate 110 in FIG. 8(B), because the through-hole 112 with the embedded chip capacitor 113 is surrounded by the insulating substrate 111 and an insulating layer 116 via a resin 119, malfunctions can easily occur, and the electrical characteristics inside the wiring substrate 100 can become unstable. Furthermore, when an electronic component that is switched at high frequencies is embedded in the through-hole 102, 112, noise from the power supply system leaks to the outside. This may adversely affect IC chips mounted on the surface of the wiring substrate 100, 110, or IC chips mounted on

other wiring substrates of a motherboard on which the wiring substrate 100, 110 itself has been mounted.

[0005]

[Problem to Be Solved by the Invention] It is an object of the present invention to solve the problems associated with the prior art described above by reducing the effect of noise generated by circuits composed of electronic components embedded in insulating substrates, while also making them less susceptible to external electromagnetic waves. It is another object of the present invention to provide a wiring substrate that can stabilize the electrical characteristics inside the wiring substrate and the electrical connection between the wiring layer and electronic components, such as IC chips, mounted on the first main surface.

[0006]

[Means for Solving the Problem] In order to solve the problems described above, the present invention was conceived in which a shielding function for electromagnetic shielding is provided on the inner surface of a through-hole or recessed portion that contains an electronic component. In other words, the wiring substrate of the present invention (claim 1) is characterized in that a shielding layer is formed an the inner surface of a through-hole or recessed portion in an insulating substrate in which an electronic component has been embedded. The wiring substrate can be a wiring substrate with a shielding layer formed on the inner surface of a through-hole or recessed portion in which an electronic component has been embedded in the insulating substrate. Because the through-hole or recessed portion is surrounded by a shielding layer, electronic components embedded in through-holes or recessed portions can be shielded from external electromagnetic waves, and noise generated from circuits composed of these electronic components to the outside can be reduced. This allows the electronic components and the IC chips mounted on the first main surface to operate properly and also stabilizes internal electrical characteristics, such as reducing crosstalk noise in the wiring substrate. Note that the electronic components include, but are not limited to, passive components such as capacitors, inductors, filters, and resistors, and active components such as low-noise amplifiers (LNAs), transistors, semiconductor devices, and FETs, as well as SAW filters, LC filters, antenna switch modules, couplers, and diplexers, and any of the components listed above made into chip form. Different types of electronic components can be embedded together in the same through-hole or recessed portion.

[0007] The present invention also encompasses a wiring substrate (claim 2), wherein the electronic component is embedded in the through-hole or recessed portion via a resin. In this way, electronic components are securely embedded in through-holes or recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer. This enables the electronic components embedded on the insulating substrate of the wiring substrate to operate properly and reliably. At the same time, the noise generated by the circuits composed of the embedded electronic components can be shielded, preventing or reducing adverse effects on the IC chips and other components mounted on the wiring substrate. The present invention also encompasses a wiring substrate (claim 3), wherein a shielding layer is also formed in an opening to the through-hole or recessed portion. In this way, electronic components embedded in an insulating substrate are surrounded by a shielding layer (ground layer or power layer), enabling the electronic components to operate more precisely and reliably while shielding them from any noise that may occur.

[0008] The present invention also encompasses a wiring substrate (claim 4), wherein a wiring layer that is connected electrically to the electrodes of the embedded electronic component is formed on at least one of the top and bottom of the insulating substrate. In this way, a wiring substrate can be reliably provided that can stably maintain an electrical connection between electronic components and a wiring layer, as well as with IC chips mounted on the first main surface of the wiring substrate and the motherboard on the second main surface of the wiring substrate via the wiring layer. The present invention also encompasses a wiring substrate (claim 5), wherein the wiring of the wiring layer at a position covering the opening to the through-hole or recessed portion in the insulating substrate also serves as the shielding layer. Thus, in addition to establishing electrical connections between the electronic components and the IC chips, etc., the wiring layer itself can shield electronic components without the need for a dedicated shielding layer. This helps respond to the demand for smaller and higher density wiring substrates.

[0009] The present invention is also a method for manufacturing a wiring substrate (claim 6), the method comprising the steps of: forming a through-hole or recessed portion in an insulating substrate for embedding an electronic component; and forming a shielding layer on the inner surface of the through-hole or

recessed portion by plating. In this way, a wiring substrate can be easily and reliably provided in which electronic components embedded in through-holes or recessed portions can be shielded from external electromagnetic waves in fewer steps, and the noise generated by the circuits composed of these electronic components can be kept from leaking into the board and beyond.

[0010] The present invention also encompasses a method for manufacturing a wiring substrate (claim 7), the method comprising the steps of: inserting an electronic component into the through-hole or recessed portion after the step of forming the shielding layer; and filling the through-hole or recessed portion into which the electronic component has been inserted with a resin and solidifying the resin. In this way, a wiring substrate can be reliably provided in which electronic components embedded in the through-holes or recessed portions can be shielded from external electromagnetic waves while also being insulated, and in which leakage of noise generated by circuits composed of these electronic components can be prevented. The present invention also encompasses a method for manufacturing a wiring substrate (claim 8), the method further comprising the step of: forming a wiring layer that is electrically connected to the electrodes of the embedded electronic component on at least one of the top and bottom of the insulating substrate after the step of filling with and solidifying the resin. In this way, a wiring substrate can be reliably provided that can stably maintain an electrical connection between electronic components and a wiring layer, as well as with IC chips mounted on the first main surface of the wiring substrate and the motherboard on the second main surface of the wiring substrate via the wiring layer. In addition, because the shielding layer can be formed at the same time as the wiring layer connected electrically to the electronic components, the number of manufacturing steps can be reduced and costs can be cut.

[0011]

[Embodiments of the Invention] Preferred embodiments of the present invention will now be described with reference to the drawings. FIG. 1 is a cross-sectional view of the main portion of a 40 mm x 40 mm wiring substrate 1 of the present invention (claims 3 to 5). As shown in FIG. 1, the wiring substrate 1 includes an insulating substrate (core substrate) 2 and a shielding layer 10 formed on the inner surface of a through-hole 8 that passes from the front surface 3 of the insulating substrate 2 to the back surface 4. This board also has a plurality of chip capacitors (electronic components) 12 built into the through-hole 8 via a resin 16. Wiring layers 26, 27, including wiring layers 26a and 27a which also serve as shielding layers, are formed in the upper and lower openings to the through-hole 8. The wiring layers 26, 27 are used as ground layers or power layers.

[0012] The insulating substrate 2 is an approximately 0.8 mm-thick substrate that is square when viewed from above, and is made of, for example, a glass-epoxy resin composite material. A 12 mm x 12 mm through-hole 8, which is square when viewed from above, is formed in the center of the substrate using the punching process. Also, as shown in FIG. 1, through-holes 7, 7 are formed in the insulating substrate 2 on both sides of the through-hole 8, and a through-hole conductor 9 and filling resin 9a are formed inside these through-holes. In addition, an approximately 25 μm-thick shielding layer 10 is formed by copper plating on the inner surface of the outer circumference of the through-hole 8. This shielding layer will be described later. The chip capacitors 12 embedded in the through-hole 8 via a resin 16 have electrodes 13, 14 made of Cu on their upper and lower ends, and can be, for example, ceramic capacitors consisting of alternating dielectric layers composed of mainly barium titanate and Ni layers. The size of the chip capacitors 12 is 3.2 mm × 1.6 mm × 0.7 mm.

[0013] As shown in FIG. 1, at the upper and lower openings to the through-hole 8, wiring layers 26, 27, including wiring 26a, 27a connected electrically to the electrodes 13, 14 of the chip capacitors 12 and serving as a shielding layer, are formed along the front and back surfaces 3, 4 of the insulating substrate 2. In addition, via conductors (filled vias) 23 are formed in the wiring 26a on the back surface 4 that are connected to each electrode 14 of the capacitor 12. Also, as shown in FIG. 1, insulating layers 32, 38, 44 made of epoxy resin and wiring layers 36, 42 made of Cu are alternately laminated above the front surface 3 of the insulating substrate 2, and via conductors (filled vias) 34, 40 forming connections between wiring layers 27, 36 and between wiring layers 36, 42 are formed in the insulating layers 32, 38. A plurality of solder bumps 46 are formed at predetermined locations in the uppermost wiring layer 42 that pass through the insulating layer (solder resist layer) 44 and protrude higher than the first main surface 48. Each bump 46 is connected to an IC chip, not shown, which is mounted on the first main surface 48.

[0014] Also, as shown in FIG. 1, insulating layers 33, 39, 45 made of the same resin as above and wiring layers 37, 43 are alternately laminated below the back surface 4 of the

insulating substrate 2, and via conductors (filled vias) 35, 41 are formed in the insulating layers 33, 39 to connect wiring layers 26 and 37 and wiring layers 37 and 43. A portion of the wiring layer 43 is exposed inside the openings 45a, 45a provided in the second main surface 47 under the lowermost insulating layer (solder resist layer) 45, and connection terminals 49 are formed on the surface from Ni and Au plating. These connection terminals 49 are used to establish a connection with a wiring substrate, such as a motherboard, not shown, on which the wiring substrate 1 itself has been mounted. In addition, the wiring layers 26, 27 sandwiching the insulating substrate 2 between them are connected electrically to each other via each chip capacitor 12 and through-hole conductor 9.

[0015] In the wiring substrate 1 described above, each chip capacitor (electronic component) 12 is embedded in the through-hole 8 with a shielding layer 10 formed on the inner surface by being secured to a resin 16, as shown in FIG. 1, and the uppermost and lowermost openings of the through-hole 8 are also covered by the wiring 26a, 27a in the wiring layers 26, 27 while connecting electrically with the electrodes 14, 13 of each capacitor 12. As a result, each chip capacitor 12 is reliably shielded from external electromagnetic waves, so that it can function as it should without malfunctioning, can be connected electrically to the wiring layers 26, 27, etc., and can be electrically connected with IC chips mounted on the first main surface 48 and mother board on the second main surface 47 stably via these layers.

[0016] Therefore, in the wiring substrate 1, the chip capacitors (electronic components) 12 operate normally and the electrical characteristics are improved and stabilized, such as reducing crosstalk noise inside the wiring substrate 1. In addition, noise generated when the capacitors 12 perform switching at high frequencies can be kept from affecting IC chips mounted on the first main surface 48 and IC chips mounted on other wiring substrates on the motherboard on which the wiring substrate 1 itself has been mounted. In the embodiment described above, a single insulating layer (core substrate 2) is used as the insulating substrate 2, but the present invention is not limited to this embodiment. In other embodiments, a plurality of insulating layers (including a core substrate) are stacked, or a plurality of insulating layers are stacked and a wiring layer is formed between them. In addition, the plurality of insulating layers mentioned above may be made of one or more materials.

[0017] FIG. 2 and FIG. 3 relate to a method for manufacturing the wiring substrate 1 shown in FIG. 1 above. As shown in FIG. 2(A), the front and back surfaces 3, 4 of an insulating substrate 2 that is about 0.8 mm thick are covered beforehand with copper foil 5, 6 that is several 10 μm thick. As shown in FIG. 2(B), a 12 mm x 12 mm through-hole 8 is formed by punching out the approximate center of the insulating substrate, and through-holes 7, 7 are opened on both sides of this. Next, electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8 and through-holes 7 after applying catalyst metal nuclei for plating such as Pd. As a result, as shown in FIG. 2(C), a wiring substrate 11 is obtained in which a shielding layer 10 consisting of a 25 μm-thick copper plating layer is formed on the inner surfaces of through-hole 8, and a through-hole conductor 9 is formed on the inner surfaces of through-holes 7. This wiring substrate 11 corresponds to claim 1 of the present invention. As shown in Figure 2(D), a filling resin 9a is applied inside the cylindrical through-hole conductors 9.

[0018] Next, as shown in FIG. 2(E), tape 15 with the adhesive side facing the through-hole 8 is affixed to the back surface 4 of the insulating substrate 2 to close the opening on the back surface 4 side of the through-hole 8. The tape 15 is affixed across the entire back surface 4 as shown in the figure to close all the through-holes 8, 8, etc. in an assembly (panel) of insulating substrates including the insulating substrates 2, 2. As shown in FIG. 2(E), a plurality of chip capacitors 12 are then inserted into the through-hole 8 and affixed at predetermined positions on the adhesive side of the tape 15. The insertion work can be performed, for example, by a chip mounter. These capacitors 12 have electrodes 14, 13 protruding on the upper and lower ends, and the end face of the electrode 13 on the lower end is affixed to the adhesive surface of the tape 15.

[0019] As shown in FIG. 3(A), after filling the through-hole 8 from the front surface 3 side with melted resin 16, which is primarily epoxy resin, curing is performed to hold the resin at about 100°C for about 60 minutes. As a result, as shown in the figure, the resin 16 solidifies and each capacitor 12 is embedded at a predetermined location in the through-hole 8 by the resin 16, except for the end faces of its electrode 13. As shown in FIG. 3(A), the surface 17 of the solidified resin 16 is curved and raised, burying the electrode 14 of each capacitor 12. Meanwhile, the back surface 18 of the resin 16 is flat and conforms to the tape 15, exposing the end faces of the electrode 14 of each capacitor 12. At this stage, the location of each capacitor 12 embedded in the resin 16 and the presence

of short circuits are inspected. The curing process described above removes air bubbles from the resin 16 and makes the resin 16 dense. The tape 15 has the heat resistance to withstand the curing process.

[0020] Next, as shown in FIG. 3(B), after the tape 15 is peeled off, and the surface 17 of the resin 16 is buffed, for example, with the insulating substrate 2 secured. As a result, a wiring substrate 20 is obtained in which the surface 19 of the newly formed resin 16 is flush with the copper foil 5 on the surface 3 of the insulating substrate 2, as shown in the figure. This wiring substrate 20 corresponds to claim 2 of the present invention. Next, as shown in FIG. 3(C), a laser L is emitted vertically from the surface 19 side of the resin 16. The emission position of the laser L is set so as to be directly above the electrode 14 at the top end of each capacitor 12. As a result, a trapezoidal-shaped via hole 22 with an inner diameter of about 100 μm is formed directly above each of the electrodes 14, as shown in the figure, and the end faces of the 14 electrodes are exposed at the bottom. A CO_2, YAG, or excimer laser can be used as the laser L.

[0021] Electroless and electrolytic copper plating is applied to the front and back surfaces 19, 18 of the resin 16 and to the copper foil 5, 6 by applying the catalyst metal nuclei in each via hole 22 and on the front and back surfaces 19, 18 of the resin. As a result, as shown in FIG. 3(D), a copper plating layer 24 including via conductors 23 is formed on the front surface 3 side of the insulating substrate 2, and a flat copper plating layer 25 is formed on the back surface 4 side. Each via conductor 23 is connected to the electrode 14 of each capacitor 12, and the copper plating layer 25 is connected to the electrode 13 of each capacitor 12.

[0022] In this state, a layer of photosensitive resin, not shown in the figure, is formed over the copper plating layer 24 and under the copper plating layer 25, and exposure and development are performed in a predetermined pattern to form photoresists. After etching the copper plating layers 24 and 25 via the gaps in the resists, the resists are peeled off. As a result, as shown in FIG. 3(E), a wiring layer 26 including wiring 26a with a via conductor 23 is formed to cover the through-hole 8 and the resin 16 on the front surface 3 side of the insulating substrate 2, and a wiring layer 27 including flat wiring 27a is formed in the same manner as described above on the back surface side 4. The result is the wiring substrate 28 corresponding to claim 3 of the present invention.

[0023] Along with the shielding layer 10, this wiring 26a, 27a, serves as a shielding layer to shield each capacitor 12 from external electromagnetic waves. As shown in FIG. 3(E), wiring layers 26 and 27 are also formed on both end faces of the left and right through-hole conductors 9. In this way, the wiring layers 26, 27 are connected electrically to each other via the respective capacitors 12 and also via the through-hole conductors 9. With the front and back surfaces of the wiring substrate 28 reversed, insulating layers 32, 33, etc., wiring layers 36, 37, etc., via conductors 34, 35, etc., and solder bumps (flip chip bumps) 46 are formed above and below the wiring layers 27, 26 using any build-up technique known in the art. This results in the wiring substrate 1 with the multilayer structure shown in FIG. 1. Build-up techniques include, but are not limited to, laminating film or liquid resin insulating layers, opening via holes by photolithography or laser processing, and forming via conductors and wiring layers by semi-additive, fully-additive, or subtractive methods.

[0024] FIG. 4 is a cross-sectional view of the main portion in a wiring substrate 50 of the present invention (claims 3-5), which has the same size and different form as the wiring substrate 1 described above. As shown in FIG. 4, the wiring substrate 50 includes an insulating substrate (core substrate) 52, a recessed portion 58 opening on the front surface 53 side of the insulating substrate 52, and shielding layers 60a, 60b formed on the inner surface of the recessed portion 58. The wiring substrate also has a plurality of chip capacitors (electronic components) 62 embedded in the recessed portion 58 via a resin 64, and a wiring layer 72 including wiring 72a, which also serves as a shielding layer, formed at the opening to the recessed portion 58. The wiring layer 72 is used as a ground layer or a power layer. The insulating substrate 52 is the same size and made of the same material as the insulating substrate 2 described above, and its center is router cut to form a 12 mm x 12 mm recessed portion 58 that is square when viewed from above. As shown in FIG. 4, through-holes 57, 57 pass through the insulating substrate 52 on both sides of the recessed portion 58, and are filled with a through-hole conductor 59 and a filling resin 59a.

[0025] Shielding layers 60a and 60b, each about 25 μm thick, are formed by copper plating on the inner surfaces of the circumferential surfaces and bottom surface of the recessed portion 58. The chip capacitors 62, that are embedded in the recessed portion 58 via a resin 64, have Cu electrodes 63 protruding only from

the upper end, but are otherwise the same as the capacitors 12 described above. As shown in FIG. 4, a wiring layer 72 including wiring 72a that establishes an electrical connection with the electrodes 63 of each chip capacitor 62 and that also serves as a shielding layer, is formed along the front surface 53 of the insulating substrate 52 at the opening above the recessed portion 58. Via conductors (filled vias) 69 are formed in the wiring 72a to connect with each electrode 63 of the chip capacitors 62.

[0026] Also, as shown in FIG. 4, insulating layers 76, 82, 88 made of epoxy resin and wiring layers 80, 86 made of Cu are alternately stacked above the front surface 53 of the insulating substrate 52, and via conductors (filled vias) 78, 84 that connect the wiring layers 72, 80, 86 are formed in the insulating layers 76, 82. A plurality of solder bumps 92 are formed at predetermined locations in the uppermost wiring layer 86, passing through the insulating layer (solder resist layer) 88 and protruding higher than the first main surface 90. Each bump 92 is connected to an IC chip, not shown, that is mounted on the first main surface 90.

[0027] In addition, as shown in FIG. 4, insulating layers 77, 83, 89 made of the same resin as above and wiring layers 73, 81, 87 are alternately stacked below the back surface 54 of the insulating substrate 52, and via conductors (filled vias) 79, 85 are formed in the insulating layers 77, 83 to connect the wiring layers 73, 81, 87. A portion of the wiring layer 87 is exposed in the openings 93, 93 provided on the second main surface 91 under the lowermost insulating layer (solder resist layer) 89, and connection terminals 94 are formed by Ni and Au plating film on the exposed surfaces. These connection terminals 94 are also used to connect to a printed wiring substrate, such as a motherboard, not shown, on which the wiring substrate 50 itself has been mounted. The wiring layers 72, 73 sandwiching the insulating substrate 52 are connected by way of through-hole conductors 59.

[0028] In the wiring substrate 50 described above, as shown in FIG. 4, each chip capacitor (electronic component) 62 is adhered to the resin 64 and embedded in a recessed portion 58 in which shielding layers 60a, 60b have been formed on the inner surface, the opening in the recessed portion 58 is covered by the wiring 72a in the wiring layer 72, and the wiring 72a is connected electrically to the electrodes 63. Because of this, each chip capacitor 62 is reliably shielded from external electromagnetic waves. It can perform its intended function without malfunctioning, is connected electrically with the wiring layer 72, etc., and is stably connected electrically with IC chips mounted on the first main surface 90 and the motherboard on the second main surface 91 via this layer.

[0029] Therefore, in the wiring substrate 50, the embedded chip capacitors 62 operate normally, and electrical characteristics are also improved and stabilized, such as the ability to reduce internal crosstalk noise. In addition, noise generated by the circuit composed of the capacitors 62 can be kept from leaking from the recessed portion 58, thereby preventing adverse effects on the IC chips and other components. In the embodiment described above, a single insulating layer (core substrate 52) is used as the insulating substrate 52, but the present invention is not limited to this embodiment. In other embodiments, a plurality of insulating layers (including a core substrate) are stacked, or a plurality of insulating layers are stacked and a wiring layer is formed between them. A through-hole may be formed in a portion of the plurality of insulating layers to form the recessed portion 58 when laminated with other insulating layers. In addition, the plurality of insulating layers mentioned above may be made of one or more materials. In the embodiment described above, the opening in the recessed portion 58 opens on the side with solder bumps 92 for mounting IC chips, etc., but the present invention is not limited to this embodiment. The opening in the recessed portion 58 may also open on the side of the connection terminals 94 used to connect to the motherboard, etc.

[0030] FIG. 5 and FIG. 6 relate to the method for manufacturing the wiring substrate 50 shown in FIG. 4 above. As shown in FIG. 5(A), the front and back surfaces 53, 54 of the same insulating substrate 52 described above are covered with copper foil 55, 56 several tens of μm thick. As shown in FIG. 5(B), the center of the insulating substrate 52 is router cut to form a recessed portion 58 that opens on the front surface 53 side, and through-holes 57, 57 are opened on both sides of the recessed portion. Next, copper plating is applied to the inner surfaces of the recessed portions 58 and through-holes 57 in the same manner as described above. As a result, a wiring substrate 61 is obtained, as shown in FIG. 5(C), in which shielding layers 60a, 60b consisting of a 25 μm thick copper plating layer are formed on the walls (inner surfaces) and bottom (inner surface) of the recessed portion 8, and through-hole conductors 59 are formed on the inner surface of the through-holes 57. This wiring substrate 61 also corresponds to claim 1 of the present invention.

[0031] As shown in FIG. 5(D), a filler resin 59a fills the interior of the through-hole conductors 59. The through-hole conductors 59 and shielding layers 60a, 60b are continuous with the copper foil 55, 56. Next, as shown in FIG. 5(E), a plurality of chip capacitors 62 are inserted into the recessed portion 58 and placed at predetermined positions on the shielding layer 60b. These capacitors 62 have electrodes 63 protruding only from the top end. The top surface of each electrode 63 is lower than the surface of the copper foil 55. As shown in FIG. 6(A), the same melted resin 64 described above is used to fill the recessed portion 58 from the front surface 53 side, and this is followed by the same curing process described above. As a result, each capacitor 62 is embedded in place in the recessed portion 58 by the resin 64 as the resin 64 solidifies, as shown in the figure. As shown in FIG. 6(A), the surface 65 of the solidified resin 64 is raised to bury the electrodes 63 of each capacitor 62.

[0032] Next, the surface 65 of the resin 64 is buffed, for example, with the insulating substrate 52 secured. In this way, as shown in FIG. 6(B), a wiring substrate 67 can be obtained in which the surface 66 of the newly formed resin 64 is flush with the copper foil 55 on the front surface 53 of the insulating substrate 52. This wiring substrate 20 also corresponds to claim 2 of the present invention. As shown in FIG. 6(C), the same laser L described above is vertically emitted from the surface 66 side of the resin 64, directly above the electrodes 63 at the top end of each capacitor 62. As a result, as shown in the figure, via holes 68 with an inner diameter of about 100 μm and a trapezoidal cross section are formed directly above each of the electrodes 63, exposing the top surface of the electrodes 63 at the bottom of the via holes.

[0033] Next, the same catalyst metal nuclei as described above are deposited in each of the via holes 68 and on the surface 66 of the resin 64, and the same copper plating as described above is applied to the surface 66 and on the copper foils 55, 56. As a result, as shown in FIG. 6(D), a copper plating layer 70 containing via conductors 69 is formed on the front surface 53 side of the insulating substrate 52, and a flat copper plating layer 71 is formed on the back surface 54 side. Each via conductor 69 is connected to the electrodes 63 of the capacitors 62. In this state, a layer of photosensitive resin, not shown in the figure, is formed over the copper plating layer 70 and under the copper plating layer 71, and exposure and development are performed in a predetermined pattern to form photoresists. After etching the copper plating layers 70 and 71 via the gaps in the resists, the resists are peeled off.

[0034] As a result, as shown in FIG. 6(E), a wiring layer 72 including wiring 72a covering the recessed portion 58 and the resin 64 and having via conductors 69 is formed on the front surface 53 of the insulating substrate 52, and a wiring layer 73 is formed on the back surface 4. This results in a wiring substrate 75 corresponding to claim 3 of the present invention. Along with shielding layers 60a and 60b, the wiring 72a serves as a shielding layer to shield each capacitor 62 from external electromagnetic waves. As shown in FIG. 6(E), wiring layers 72, 73 are also formed on both end faces of the left and right through-hole conductors 59, so that the wiring layers 72, 73 are connected electrically to each other via the through-hole conductors 59. Then, by forming insulating layers 76, 77, etc., wiring layers 80, 81, etc., via conductors 78, 79, etc., and solder bumps (flip chip bumps) 92, etc. above and below the wiring layers 72, 73 in wiring substrate 75 using any of the build-up technologies mentioned above, the wiring substrate 50 with the multilayer structure shown in FIG. 4 above can be obtained.

[0035] FIG. 7(A) is a cross-sectional view corresponding to FIG. 3(B) above. Each chip capacitor 12, which is embedded inside the through-hole 8 in the insulating substrate 2, has the end faces of the top and bottom electrodes 14, 13 exposed on the front and back surfaces 19, 18 of the resin 16. The same copper plating layers as described above are formed on the front and back surfaces 19, 18 and on the copper foil 5, 6 of the insulating substrate 2 to form etching resists, and etching is then performed in the same manner as described above. As shown in FIG. 7(B), this enables a wiring substrate 97 to be obtained that has wiring layers 95, 96 on the front and back surfaces 3 and 4, including wiring layers 95a, 96a that connect to the electrodes 14 , 13 of each capacitor 12. The wiring 95a, 96a, together with the shielding layer 10 on the inner surface of the through-hole 8, also serves as a shielding layer to shield each capacitor 12. In addition, because the electrodes 14, 13 of each capacitor 12 can be directly connected to the wiring 95a, 96a on the wiring substrate 97, the number of manufacturing steps is reduced, and the electrical connection established between the capacitors 12 and the wiring layer 95, etc., is more stable than that of the wiring substrate 28 using via conductors 23 described above.

[0036] FIG. 7(C) is a cross-sectional view corresponding to FIG. 6(B) above, in which each of the chip capacitors 62 embedded in the recessed 58 of the insulating substrate 52 has

the end faces of the top electrodes 63 exposed on the surface 66 of the resin 64. The same copper plating layer as described above is formed on the surface 66 of the resin and on the copper foil 55, 56 of the insulating substrate 52, and etching resists are formed before performing etching in the manner described above. In this way, as shown in FIG. 7(D), a wiring substrate 99 can be obtained that has a wiring layer 98 including wiring 98a that connects to the electrodes 63 of each capacitor 62 on the front surface 53 side and a wiring layer 73 on the back surface 54 side. The wiring 98a, together with the shielding layers 60a, 60b on the inner surface of the recessed portion 58, serves as a shielding layer to shield each capacitor 62. Because the electrodes 63 of each capacitor 62 are directly connected to the wiring 98a in the wiring substrate 99, the number of manufacturing steps is reduced, and the electrical connection established between the capacitors 62 and the wiring layer 98, etc., is more stable than that of the wiring substrate 75 using via conductors 69 described above.

[0037] The present invention is not limited to the embodiments described above. For example, a single electronic component may be embedded in a through-hole 8 or recessed portion 58. Conversely, a plurality of through-holes 8 or recessed portions 58 may be formed in a single product (insulating substrate 2, 52) in a panel of multiple units containing a plurality of insulating substrates 2, 52. Electronic components such as the capacitors 62 with electrodes 63 described above can be embedded at the top end only inside a through-hole 8 in the insulating substrate 2. In addition, a plurality of chip electronic components can be made into a single unit with pre-bonded chip electronic components side-by-side, which can then be inserted into and embedded in a through-hole 8 or recessed portion 58. In addition to the chip capacitors 12 described above, chip electronic components include passive components such as inductors, resistors, and filters in chip form, as well as active components such as transistors, memories, and low-noise amplifiers (LNAs). It is also possible to embed electronic components of different types in the same through-hole or recessed portion.

[0038] Also, in addition to the glass-epoxy resin composite material described above, the insulating substrate 2 can be made of glass woven fabrics or composite materials of glass fibers and resins such as epoxy resin, polyimide resin, or BT resin having similar heat resistance, mechanical strength, flexibility, and ease of processing. Alternatively, composites of organic fibers such as polyimide fibers and resins, and resin-resin composites in which a resin such as an epoxy resin is impregnated with a fluorinated resin having a three-dimensional network structure, such as PTFE having continuous pores, can also be used. In addition to the copper plating described above, the shielding layers 10, 60a, 60b and wiring layers 26, 72, etc. can be made of Ni, Ni-Au, etc., or can be formed by applying a conductive resin instead of using metal plating. In addition, the via conductors 34, etc., are not limited to filled vias in which via holes are filled, but can also be cylindrical bodies that conform to via holes.

[0039] In addition to those whose main component is the epoxy resin described above, the insulating layers 32, 76, etc. can be made of resin composites in which a polyimide resin, BT resin, PPE resin, or fluorinated resin with a three-dimensional network structure with continuous pores, such as PTFE, is impregnated with epoxy resin or other resin with similar heat resistance, pattern formability, etc. The insulating layers can also be formed by applying a liquid resin with a roll coater, or by thermo-compression bonding of an insulating film. In addition to the flip chip bumps (solder bumps) 46, 92 mentioned above, flip chip pads, wire bonding pads, or pads for TAB connection may be used as connection terminals with IC chips mounted on the first main surfaces 48, 90 of the wiring substrates 1, 50. Although the capacitors 12, 62 above use a high-k dielectric ceramic with $BaTiO_3$ as the main component, ones whose main component is $PbTiO_3$, $PbZrO_3$, TiO_2, $SrTiO_3$, $CaTiO_3$, $MgTiO_3$, $KNbO_3$, $NaTiO_3$, $KTaO_3$, $PbTaO_3$, $(Na_{1/2}Bi_{1/2})TiO_3$, $Pb(Mg_{1/2}W_{1/2})O_3$, or $(K_{1/2}Bi_{1/2})TiO_3$ may also be used.

[0040] Although Cu is the main material of the electrodes 13, etc. of the capacitors 12, etc. above, Pt, Ag, Ag-Pt, Ag-Pd, Pd, Au, and Ni, etc., which are compatible with electronic components, can also be used. In addition, the capacitors 12 of the electronic components above may be capacitors that are a composite with a dielectric layer consisting mainly of a high dielectric ceramic, an electrode layer consisting of Ag-Pd, etc., and a via conductor or wiring layer consisting of a resin, Cu plating, Ni plating, etc. A plurality of mounting areas may also be formed on the first main surfaces 48, 90 of the wiring substrates 1, 50, and an a plurality of IC chips may be mounted individually in each area.

[0041]

[Effects of the Invention] In the wiring substrate according to the present invention (claim 1) described above, a through-hole or recessed portion is surrounded by a shielding layer. As a result, an electronic component embedded in

the through-hole can be shielded from external electromagnetic waves, and noise from the circuit composed of the electronic component is less likely to leak into and out from the wiring substrate. This enables the electronic component and IC chips to operate normally and also stabilizes electrical characteristics, such as reducing crosstalk noise in the wiring substrate. In the wiring substrate according to claim 3, the electronic component embedded in the insulating substrate is surrounded by a shielding layer around its entire perimeter. As a result, the electronic component itself, IC chips mounted on the wiring substrate, and IC chips mounted on other wiring substrates connected electrically via a motherboard can operate more precisely and reliably. In addition to the above, the wiring substrate according to claims 4 and 5 can stably establish an electrical connection not only between the embedded electronic component and the wiring layer, but also between a IC chip mounted on the surface of the wiring substrate and the motherboard on the second main surface via this wiring layer.

[0042] Meanwhile, the method for manufacturing a wiring substrate according to the present invention (claim 6) can easily and reliably provide, in fewer steps, a wiring substrate in which electronic components embedded in through-holes or recessed portions can be shielded from external electromagnetic waves, and the noise generated by the circuits composed of these electronic components can be kept from leaking into the board and beyond. The method for manufacturing a wiring substrate in claim 7 can reliably provide a wiring substrate in which electronic components embedded in through-holes or recessed portions are shielded from external electromagnetic waves while insulating them, and noise generated by circuits composed of the electronic components does not leak. In addition to the above, the method for manufacturing a wiring substrate in claim 8 can reliably provide a wiring substrate that can stably maintain an electrical connection between an embedded electronic component and the wiring layer, as well as an electrical connection with IC chips mounted on the first main surface of the wiring substrate and the motherboard on the second main surface via the wiring layer.

[Brief Description of the Drawings]

[FIG. 1] FIG. 1 is a cross-sectional view showing the main portion of the wiring substrate of the present invention.

[FIG. 2] FIG. 2 (A) to (E) show steps performed to manufacture the wiring substrate shown in FIG. 1.

[FIG. 3] FIG. 3 (A) to (E) show the manufacturing steps following FIG. 2 (E).

[FIG. 4] FIG. 4 is a cross-sectional view showing the main portion of the wiring substrate in another embodiment of the present invention.

[FIG. 5] FIG. 5 (A) to (E) show steps performed to manufacture the wiring substrate shown in FIG. 4.

[FIG. 6] FIG. 6 (A) to (E) show the manufacturing steps following FIG. 5 (E).

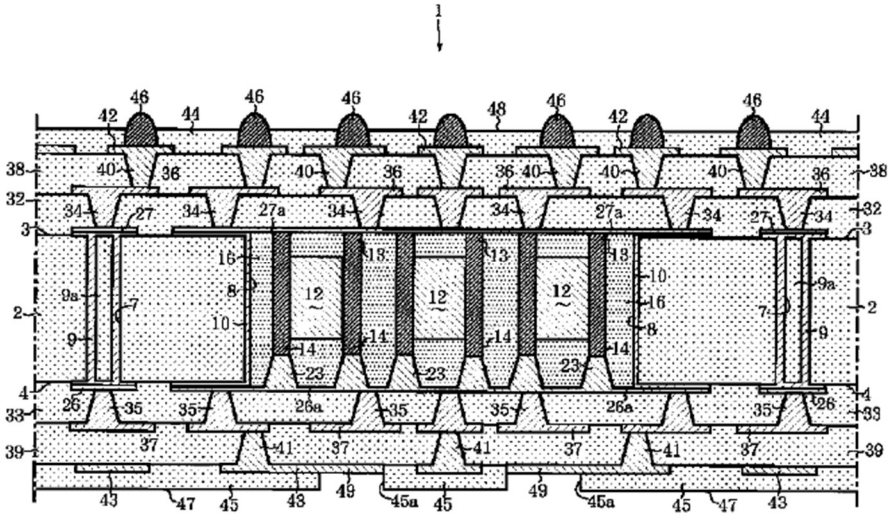
[FIG. 7] FIG. 7 (A) to (D) show steps performed to manufacture the wiring substrate in a modified embodiment of the present invention.

[FIG. 8] FIG. 8 (A) and (B) are cross-sectional views showing wiring substrates of the prior art.

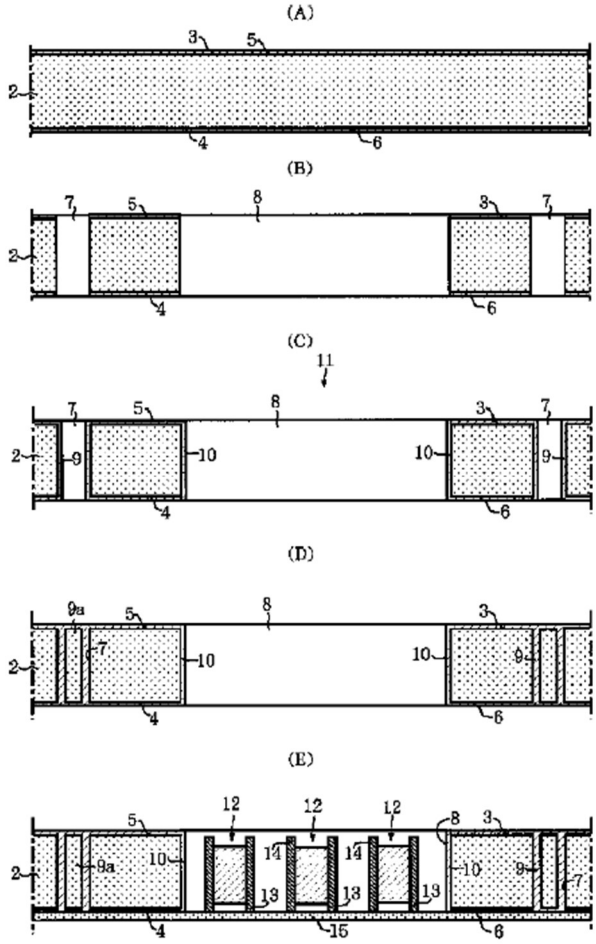
[Key to the Drawings]

1, 11, 20, 28, 50, 61, 67, 75, 97, 99: Wiring Substrate
2, 52: Insulating substrate
8: Through-hole
10, 60a, 60b: Shielding layer
12, 62: Chip capacitor (electronic component)
13, 14, 63: Electrode
16, 64: Resin
26, 27, 36, 37, 42, 43, 72, 73, 80, 81, 86, 87, 95, 96, 98: Wiring layer
26a, 27a, 72a, 95a, 96a, 98a: Wiring (and shielding layer)

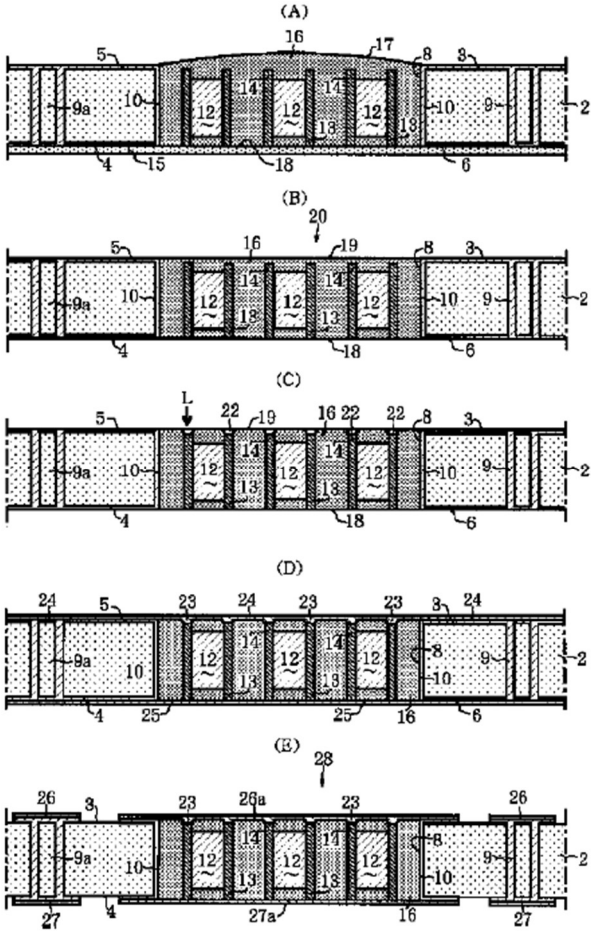
[FIG. 1]



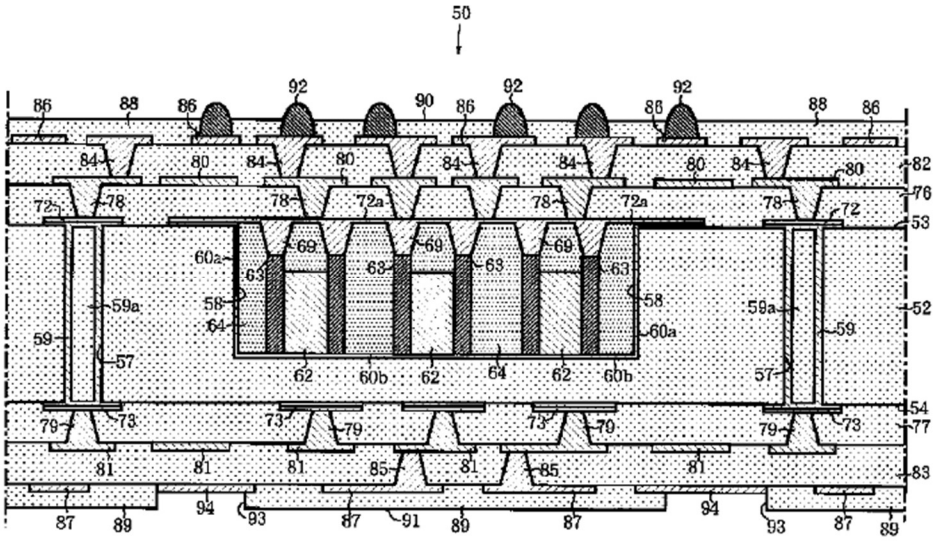
[FIG. 2]



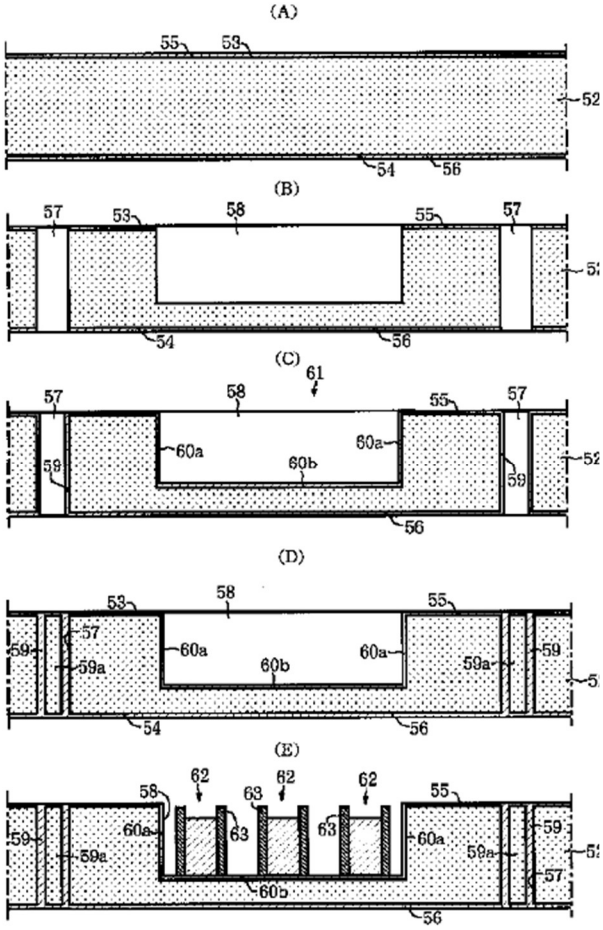
[FIG. 3]



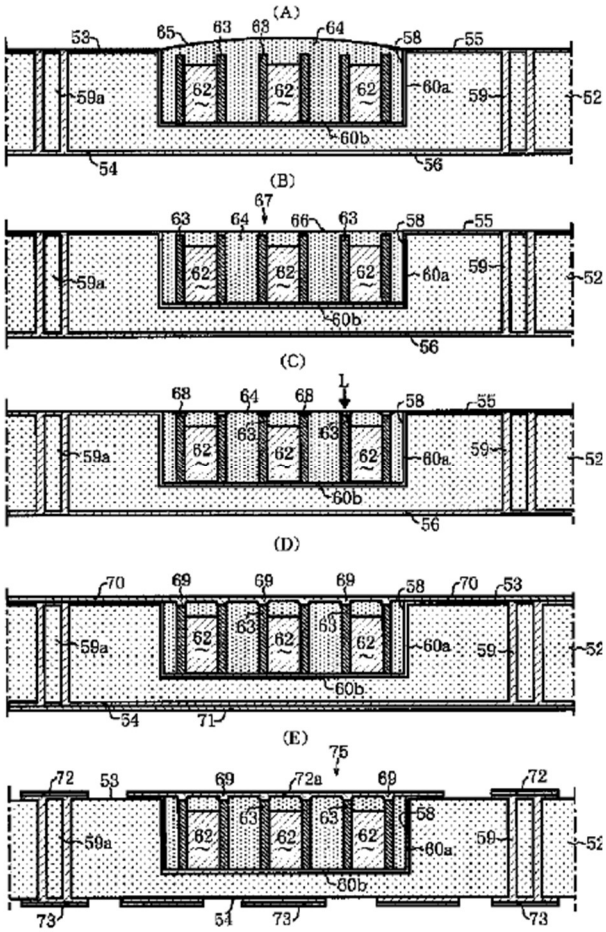
[FIG. 4]



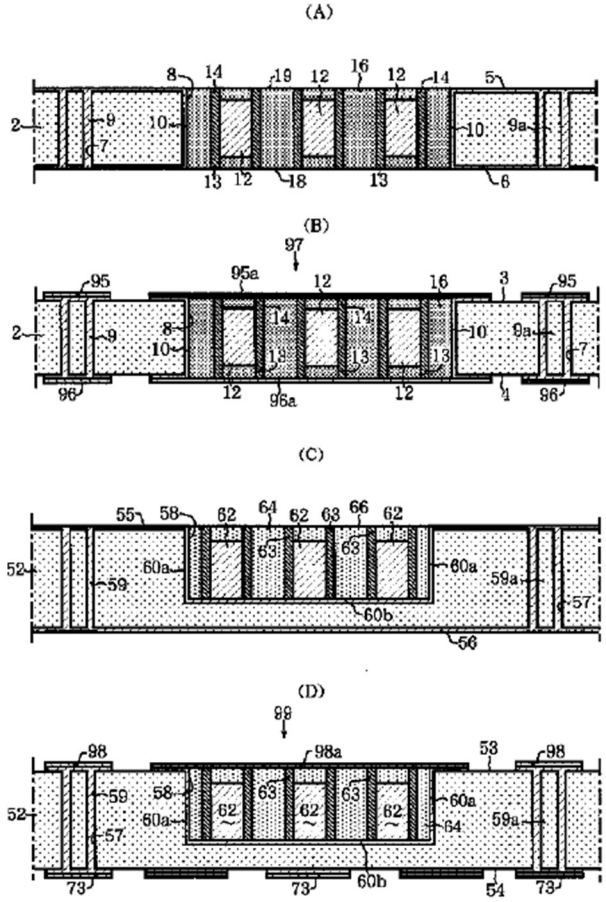
[FIG. 5]



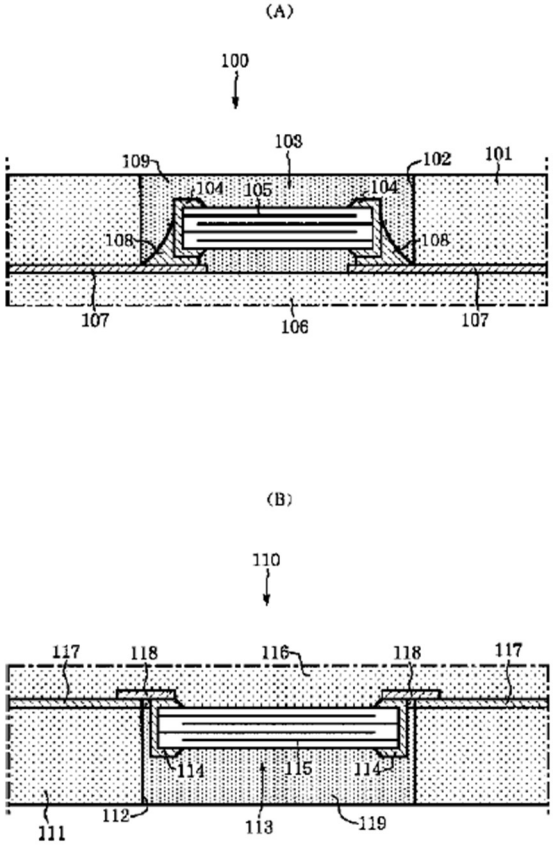
[FIG. 6]



[FIG. 7]



[FIG. 8]



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