IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Tuominen	
U.S. Patent No.:	7,989,944	Attorney Docket No. 50095-0193IP1
Issue Date:	Aug. 2, 2011	
Appl. Serial No.:	11/878,557	
Filing Date:	Jul. 25, 2007	
Title:	METHOD FOR EMBEDDING A COMPONENT IN A BASE	

Mail Stop Patent Board
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 7,989,944 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

TABLE OF CONTENTS

I. INTRODUCTION 1

II. REQUIREMENTS UNDER 37 C.F.R. § 42.104 1
- **A.** Standing Under 37 C.F.R. § 42.104(a) 1
- **B.** Challenge Under 37 C.F.R. § 42.104(b) 1

III. SUMMARY OF THE '944 PATENT 2
- **A.** Brief Description 2
- **B.** Summary of the Prosecution History of the '944 patent 4

IV. LEVEL OF ORDINARY SKILL 5

V. CLAIM CONSTRUCTION 5

VI. DETAILED EXPLANATION OF GROUNDS 6
- **A.** GROUND 1A – Sakamoto-Eiji Renders Obvious Claims 1-36 6
  - 1. Sakamoto 6
  - 2. Eiji 7
  - 3. Predictable Combination of Sakamoto and Eiji 9
  - 4. Application to Challenged Claims 13
- **B.** GROUND 1B – Sakamoto-Eiji-Imoto renders obvious Claims 15-31 45
  - 1. Imoto 45
  - 2. Predictable Combination of Sakamoto, Eiji and Imoto 46
  - 3. Application to Challenged Claims 49
- **C.** GROUND 2A – McCormack and Eiji renders obvious Claims 1-36 50
  - 1. McCormack 50
  - 2. Predictable Combination of McCormack and Eiji 52
  - 3. Application to Challenged Claims 56
- **D.** GROUND 2B – McCormack, Eiji and Sugaya render obvious Claims 15-31 84
  - 1. Sugaya 84
  - 2. Predictable Combination of McCormack, Eiji and Sugaya 85
  - 3. Application to Challenged Claims 87

VII. The *Advanced Bionics* Test Favors Institution—§325(D) 88

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314 89

IX. FEES 90

X. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1) 91

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1).....91
B. Related Matters Under 37 C.F.R. § 42.8(b)(2).....91
C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3).....91
D. Service Information 92

LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 7,989,944
APPLE-1002	U.S. Patent No. 7,989,944 File History
APPLE-1003	Declaration of Dr. Dean Neikirk
APPLE-1004	Certified Translation of JP Patent Application Publication No. 2001-339165A ("Sakamoto")
APPLE-1005	U.S. Patent Application Publication No. 2002/0175402 ("McCormack")
APPLE-1006	U.S. Patent No. 6,489,685 ("Asahi")
APPLE-1007	U.S. Patent Application Publication No. 2001/0030059 ("Sugaya")
APPLE-1008	U.S. Patent Application Publication No. 2002/0020898 ("Vu")
APPLE-1009	U.S. Patent No. 7,294,529 ("the '529 Patent")
APPLE-1010	RESERVED
APPLE-1011	Certified Translation of JP Patent No. 3207174 ("Hayashi")
APPLE-1012	Certified Translation of JP Patent Application Publication No. 2002-016327 ("Eiji")
APPLE-1013	U.S. Patent No. 6,335,571 ("Capote")
APPLE-1014	U.S. Patent No. 6,297,551 ("Dudderar")
APPLE-1015	U.S. Patent No. 6,404,052 ("Kurita")
APPLE-1016	Certified Translation of JP Patent Application Publication No. 2001-068624A ("Imoto")
APPLE-1017	Certified Translation of PCT Publication No. WO00/09623 ("Watanabe")

APPLE-1018	U.S. Patent No. 4,179,802 ("Joshi")
APPLE-1019	U.S. Patent No. 5,608,262 ("Degani")
APPLE-1020	U.S. Patent No. 5,321,210 ("Kimbara")
APPLE-1021	U.S. Patent No. 5,146,674 ("Frankeny")
APPLE-1022	JP Patent Application Publication No. 2001-339165A ("Sakamoto")
APPLE-1023	JP Patent No. 3207174 ("Hayashi")
APPLE-1024	JP Patent Application Publication No. 2002-016327 ("Eiji")
APPLE-1025	JP Patent Application Publication No. 2001-068624A ("Imoto")
APPLE-1026	PCT Publication No. WO00/09623 ("Watanabe")
APPLE-1027	RESERVED
APPLE-1028	RESERVED
APPLE-1029	U.S. Patent No. 5,745,984 ("Cole")
APPLE-1030	RESERVED
APPLE-1031	RESERVED
APPLE-1032	RESERVED
APPLE-1033	RESERVED
APPLE-1034	RESERVED
APPLE-1035	RESERVED
APPLE-1036	U.S. Patent No. 5,880,938 ("Johnsen")

LISTING OF CLAIMS

Claim 1	
[1pre]	A circuit board comprising
[1a]	an insulating material layer having a first side and a second side,
[1b]	at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
[1c]	at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
[1d]	a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,
[1e]	a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
[1f]	contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.
Claim 2	
[2]	The circuit board of claim 1, wherein the first and second metal plates are electrically connected to each other.

Claim 3	
[3]	The circuit board of claim 1, wherein the first and second metal plates are electrically connected to an earth connection of the circuit board.
Claim 4	
[4]	The circuit board of claim 1, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.
Claim 5	
[5]	The circuit board of claim 4, wherein the metal foil is electrically connected to at least one of the first and second metal plates.
Claim 6	
[6]	The circuit board of claim 4, wherein the metal foil is electronically connected to an earth connection of the circuit board.
Claim 7	
[7]	The circuit board of claim 4, wherein the component has a second surface opposite to the first surface and side-surfaces between the first and second surfaces, and wherein the first and second metal plates and the metal foil form an electromagnetic interference shield around the component such that the side-surfaces of the component face towards the metal foil, the first surface of the component face towards the second metal plate, and the second surface of the component face towards the first metal plate.
Claim 8	
[8]	The circuit board of claim 1, wherein the insulating material layer includes a baseboard and the hardened insulating polymer layer.
Claim 9	
[9]	The circuit board of claim 8, wherein the baseboard is a glass-fibre reinforced epoxy board.

Claim 10	
[10]	The circuit board of claim 8, wherein the component is located in a hole in the baseboard; and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, wherein the metal foil creates an interference protection structure around the component.
Claim 11	
[11]	The circuit board of claim 1, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.
Claim 12	
[12]	The circuit board of claim 1, wherein the hardened insulating polymer layer contains epoxy.
Claim 13	
[13]	The circuit board of claim 1, wherein the component is a microcircuit.
Claim 14	
[14]	The circuit board of claim 1, comprising an electrically conducting feed-through between the conductive pattern layers on the both sides of the insulating material layer.
Claim 15	
[15pre]	A multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other,
[15a]	wherein at least the first circuit board substructure comprises an insulating material layer having a first side and a second side,
[15b]	at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the conductive pattern layers defining a first metal plate,
[15c]	at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

15[d]	a component inside the insulating material layer and between the first and second metal plates, the component having a first surface facing towards the second metal plate, and contact areas on the first surface,
15[e]	a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
15[f]	contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.
Claim 16	
[16]	The multi-layered circuit board of claim 15, wherein said first circuit board substructure and said second circuit board substructure are electrically connected to each other to form a multi-layered functioning totality.
Claim 17	
[17]	The multi-layered circuit board of claim 16, wherein said second circuit board substructure comprises an insulating material layer and at least one conductive pattern layer in the insulating material layer
Claim 18	
[18]	The multi-layered circuit board of claim 17, wherein said second circuit board substructure includes a component embedded in the insulating material layer.
Claim 19	
[19]	The multi-layered circuit board of claim 15, wherein said first circuit board substructure comprises a first microcircuit and said second circuit board substructure comprises a second microcircuit such that the first and second microcircuits are on top of each other and at least one of the first and second metal plates is located between said first and second microcircuits.

Claim 20	
[20pre]	The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises
[20a]	an insulating material layer having a first side and a second side,
[20b]	at least one first conductive pattern layer on the first side of the insulating material layer,
[20c]	at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,
[20d]	a component inside the insulating material layer and having a first surface facing towards the second metal plate, and contact areas on the first surface,
[20e]	a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
[20f]	contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.
Claim 21	
[21pre]	The multi-layered circuit board of claim 15, wherein said second circuit board substructure comprises
[21a]	an insulating material layer having a first side and a second side,
[21b]	at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
[21c]	at least one second conductive pattern layer on the second side of the insulating material layer,

[21d]	a component inside the insulating material layer, the component having first surface and a second surface on the opposite sides of the component and contact areas on the first surface, the second surface facing towards the first metal plate,
[21e]	a hardened insulating polymer layer between the first surface of the component and at least one conductive pattern of said at least one second conductive pattern layer, and
[21f]	contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers.
Claim 22	
[22]	The multi-layered circuit board of claim 15, comprising a third circuit board substructure on top of the first and second circuit board substructures.
Claim 23	
[23]	The multi-layered circuit board of claim 22, wherein the first circuit board substructure is between the second and third circuit board substructures.
Claim 24	
[24]	The multi-layered circuit board of claim 22, wherein each of the first, second and third circuit board substructures includes an embedded microcircuit.
Claim 25	
[25]	The multi-layered circuit board of claim 15, wherein the first and second metal plates are electronically connected to each other.
Claim 26	
[26]	The multi-layered circuit board of claim 15, wherein the first and second metal plates are electrically connected to each other.

Claim 27	
[27]	The multi-layered circuit board of claim 15, wherein the component is located in a hole in the insulating material layer, and the circuit board comprises metal foil covering the sidewalls of the hole and a filler material in the hole between the metal foil and the component.
Claim 28	
[28]	The multi-layered circuit board of claim 15, wherein the metal foil is electronically connected to at least one of the first and second metal plates.
Claim 29	
[29]	The multi-layered circuit board of claim 15, wherein the conductors in the contact openings contain at least one of electrochemically deposited copper and chemically deposited copper.
Claim 30	
[30]	The multi-layered circuit board of claim 15, wherein the component is a microcircuit.
Claim 31	
[31]	The multi-layered circuit board of claim 15, wherein the first circuit board substructure comprises at least two microcircuits inside the insulating material layer
Claim 32	
[32pre]	An electronic module comprising
[32a]	an insulating material layer having a first side and a second side,
[32b]	at least one first conductive pattern layer on the first side of the insulating material layer, at least one of the first conductive pattern layers defining a first metal plate,
[32c]	at least one second conductive pattern layer on the second side of the insulating material layer, at least one of the second conductive pattern layers defining a second metal plate,

[32d]	a hole having sidewalls defined in the insulating material layer and located between the first and second metal plates,
[32e]	a metal foil covering the sidewalls of the hole,
[32f]	a microcircuit inside the hole and having a first surface facing towards the second metal plate, and contact areas on the first surface,
[32g]	a filler material in the hole between the metal foil and the microcircuit,
[32h]	a hardened insulating polymer layer between the first surface of the microcircuit and at least one conductive pattern of said at least one second conductive pattern layer,
[32i]	contact openings in the hardened insulating polymer layer and conductors in the contact openings for forming electrical contacts between the contact areas of the microcircuit and the at least one second conductive pattern layer or layers.
Claim 33	
[33]	The electronic module of claim 32, wherein the first and second metal plates are electronically connected to each other.
Claim 34	
[34]	The electronic module of claim 32, wherein the first and second metal plates are electrically connected to an earth connection of the electronic module.
Claim 35	
[35]	The electronic module of claim 32, wherein the metal foil is electronically connected to at least one of the first and second metal plates.
Claim 36	
[36]	The electronic module of claim 32, wherein the metal foil and the first and second metal plates are electronically connected to an earth connection of the electronic module.

I. INTRODUCTION

Apple Inc. ("Apple" or "Petitioner") petitions for IPR of claims 1-36 ("Challenged Claims") of U.S. Patent No. 7,989,944 ("the '944 patent").

II. REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. § 42.104(b)

Petitioner requests IPR based on the following grounds, further supported by the Declaration of Dr. Neikirk (APPLE-1003).

Ground	Claims	§103 Basis
Ground 1A	1-36	Sakamoto-Eiji
Ground 1B	15-31	Sakamoto-Eiji-Imoto
Ground 2A	1-36	McCormack-Eiji
Ground 2B	15-31	McCormack-Eiji-Sugaya

Although priority entitlement is not conceded, each reference pre-dates the '944 patent's earliest possible priority date (January 31, 2002; "Critical Date").

Reference	Date	Pre-AIA Status
Sakamoto(APPLE-1004)	Dec. 7, 2001 (published)	§§102(a)/(b)
McCormack(APPLE-1005)	May 23, 2001 (filed)	§102(e)
Eiji(APPLE-1012)	Jan. 18, 2002 (published)	§§102(a)/(b)
Imoto(APPLE-1016)	Mar. 16, 2001 (published)	§§102(a)/(b)

Sugaya(APPLE-1007)	Oct. 18, 2001 (published)	§§102(a)/(b)

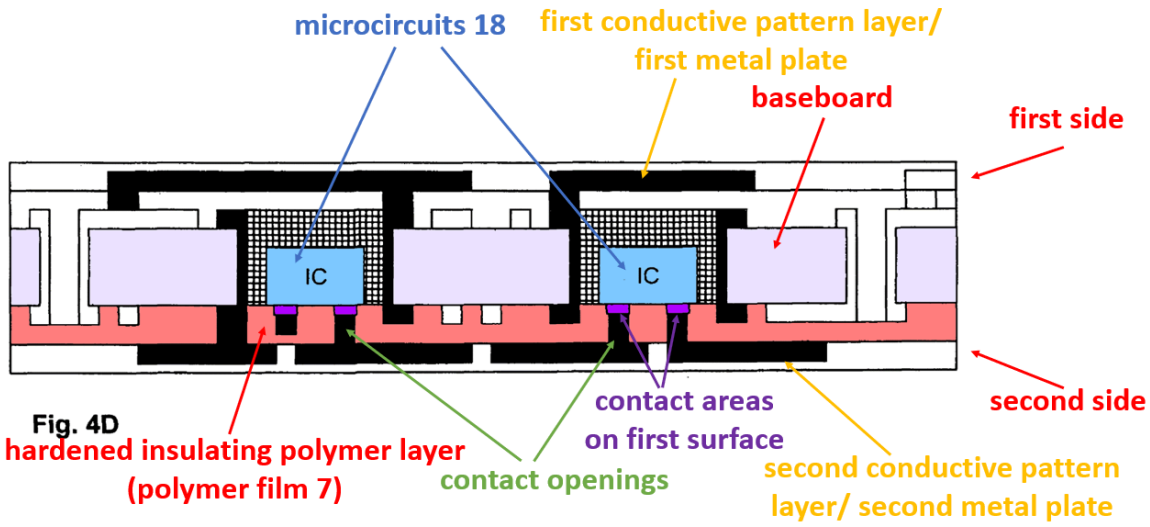
Sakamoto (APPLE-1004), Eiji (APPLE-1012), and Imoto (APPLE-1016) are certified English translations of JP2001-339165A ("Sakamoto"/APPLE-1022), JP2002-016327 ("Eiji"/APPLE-1024), and JP2001-068624A ("Imoto"/APPLE-1025). The Grounds are directed to the prior art references (e.g. APPLE-1022, APPLE-1024, APPLE-1025), for which the translations are cited throughout the petition to identify relevant aspects thereof.

III. SUMMARY OF THE '944 PATENT

A. Brief Description

The '944 patent recites a method for embedding a component in a base and an electronic module having electronic components embedded in a base. APPLE-1001, Title, Abstract. In particular, the annotated Figure 4D below shows integrated circuit components (microcircuits 18) embedded inside a baseboard and between a first and a second conductive pattern layers (each defining a metal plate) on a first and a second side, respectively, of an insulating material layer composed of the baseboard and a hardened insulating polymer layer; each component having contact areas on a first surface of the component; the hardened insulating polymer layer positioned between the first surface and the second conductive pattern layer; contact openings in the hardened insulating polymer layer and conductors in the

contact openings for forming electrical contacts between the contact areas of the components and the second conductive pattern layer. APPLE-1001, FIG. 4D (and related descriptions), Cl. 1; APPLE-1003, ¶63.



APPLE-1001, FIG. 4D (Annotated)

The ’944 patent describes a “metal foil” (or “conductive material”) covering the sidewalls of the holes where microcircuits 18 are embedded, for protection from electromagnetic interference (EMI). *E.g.*, APPLE-1001, 3:61-4:9, 8:34-41, 64-66, Cls. 4, 10, 27, 32; APPLE-1003, ¶64. The ’944 patent also describes a “metal foil” below microcircuits 18 and a “metal plate” above. APPLE-1001, 9:10-20. The ’944 patent describes copper in the contact openings which “contains at least one of electrochemically deposited copper and chemically deposited

copper."[1] *E.g.*, APPLE-1001, Cls. 11, 29, 6:21-25; APPLE-1003, ¶65.

While the '944 patent touts these routine aspects as "invention," POSITAs were aware of the structure having electrical components embedded in a base like circuit board to achieve miniaturization of electronic devices and high density circuitry. APPLE-1003, ¶¶70-303; *infra*, §VI.

B. Summary of the Prosecution History of the '944 patent

Only a single office action was issued, rejecting all pending claims as anticipated and obvious over Takeuchi (US2002/0132096). APPLE-1002, 101-113. In response, applicant argued that Takeuchi is lacking the metal plates as claimed, and that "Takeuchi fails to disclose or suggest a structure that can be used as a protective shield against electromagnetic interference" and "completely fails to disclose the interference protection around the embedded components." APPLE-1002, 91-96. A notice of allowance followed, ending prosecution prematurely and

[1] "Electrochemically deposited copper" and "chemically deposited copper" are product-by-process elements that merely reference to copper deposited either by an electrochemical process or a chemical process. APPLE-1003, ¶66. It has been well established that the recited process in such a product-by-process element has no patentable weight in view of the prior art. *See Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009) ("different process can anticipate"). .

without application of the more pertinent prior art such as Sakamoto, McCormack, Eiji, Imoto and Sugaya that are discussed in this Petition. *Id.*, 26-33.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the '944 patent (a "POSITA") would have had at least a Bachelor's degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. APPLE-1003, ¶23.

V. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. The Board has repeatedly explained that "claim terms need only be construed to the extent necessary to resolve the controversy," and for purpose of the particular Grounds in this Petition, no formal construction is necessary because the prior art presented below satisfies the claims under any reasonable construction consistent with *Phillips*. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed.

Cir. 2011).[2]

VI. DETAILED EXPLANATION OF GROUNDS

A. GROUND 1A – Sakamoto-Eiji Renders Obvious Claims 1-36

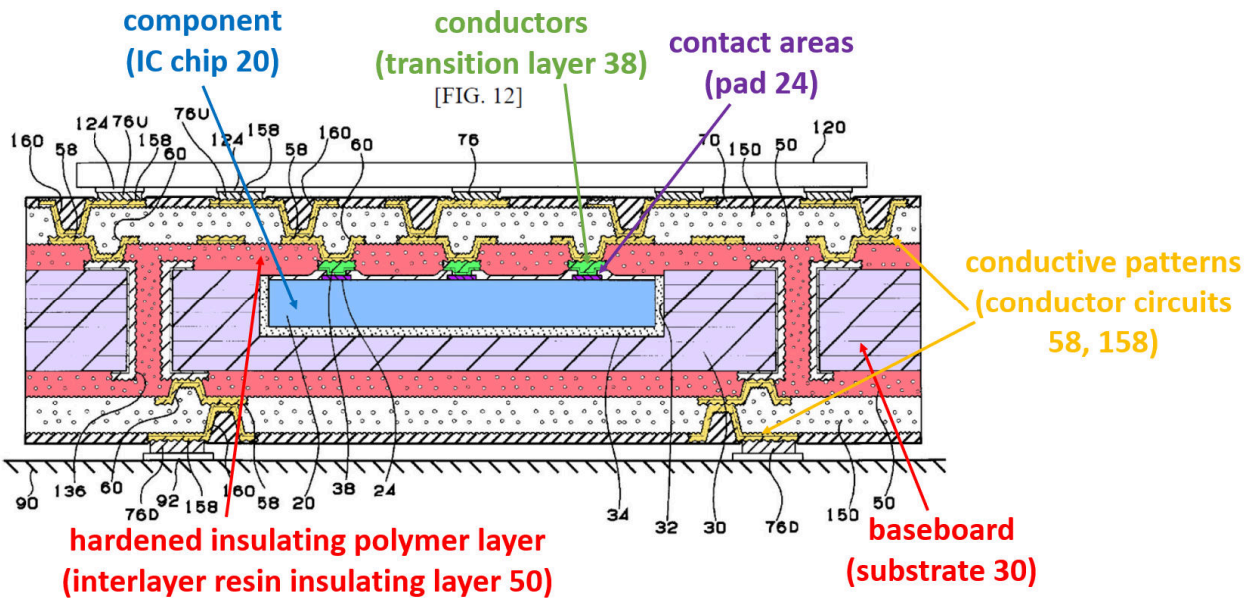
1. Sakamoto[3]

Sakamoto describes "a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip." APPLE-1004, [0001]; *see also*, Abstract, [0005], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. An "interlayer resin insulating layer 50" provided over the IC chip 20 and on a surface of substrate 30 contains polymer and is cured with the application of heat and pressure. *Id.*, [0030], [0042], [0047], [0057]-[0060]; APPLE-1003, ¶¶70-72. "Conductor circuit 58" is formed on the interlayer resin insulating layer 50 and the inner wall surface of openings for via holes 60. APPLE-1004, [0017], [0036];

[2] Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

[3] General descriptions provided for this and other references and combinations are incorporated into each subsection and mapping of the claims that includes citations to these references. All emphasis is added unless otherwise indicated.

APPLE-1003, ¶73. A "transition layer 38" made of copper is provided on a die pad 24 of the IC chip 20, to connect to via 60 in the interlayer resin insulating layer 50. *Id.*, Abstract, [0018], [0020], [0028], [0031], [0067], [0069]; APPLE-1003, ¶74.

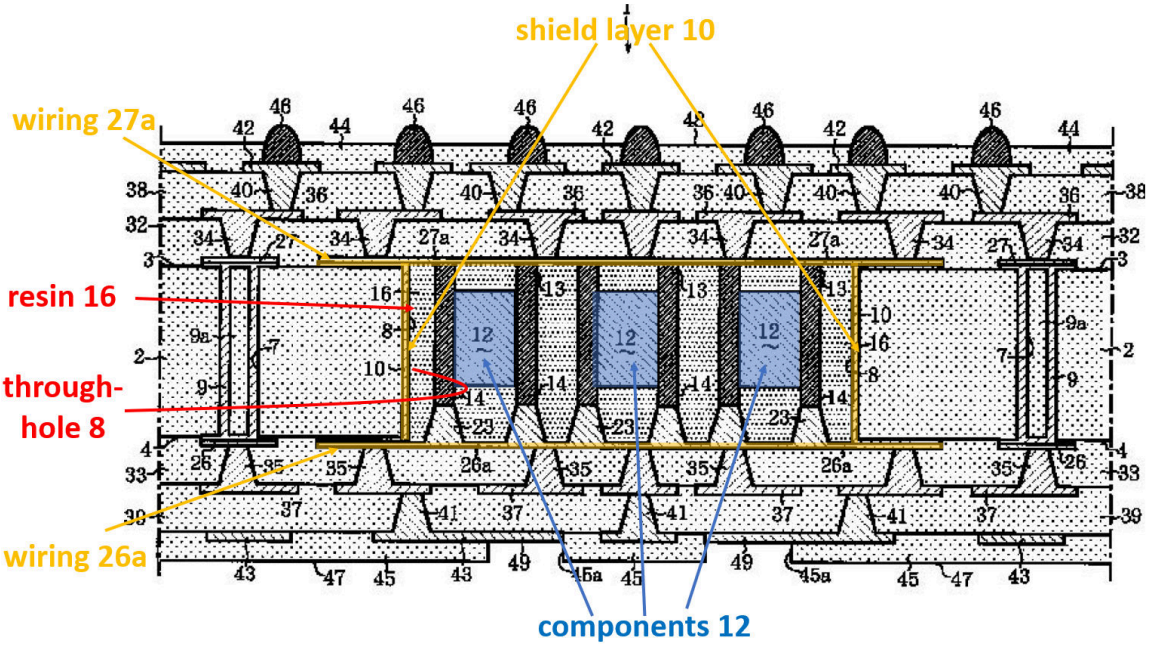


APPLE-1003, ¶74 (APPLE-1004, FIG. 12 (Annotated))

2. Eiji

Eiji describes "a wiring substrate 1 in which a shielding layer 10 composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of a through-hole 8 provided in an insulating substrate (core substrate) 2 in which electronic components 12 are embedded[.]" APPLE-1012, Abstract, FIG. 1; *see also*, [0001], [0005], [0006]-[0007], [0009], [0011]-[0012], [0017], [0041], Cls. 1, 6; APPLE-1003, ¶¶81-83.

Eiji describes filling the through-hole with a resin (e.g., resin 16) such that "electronic components are securely embedded in through-holes or recessed portions while being surrounded and insulated by a resin, in addition to being shielded from external electromagnetic waves by the shielding layer." *Id.*, [0007], [0010], [0019], cls. 2, 7, FIGS. 1, 3; *see also*, [0031]; APPLE-1003, ¶84.



APPLE-1003, ¶84 (APPLE-1012, FIG. 1 (Annotated))

Beyond shielding layer 10, Eiji further describes wiring layers 26 and 27, "including wiring layers 26a and 27a which also serve as shielding layers." *See e.g.*, APPLE-1012, [0011], [0023], [0025]; *see also*, Abstract, [0007], [0008], [0010], [0013]-[0014], [0017] (26, 27 formed from "copper foil 5, 6 that is several 10 μm thick"), [0021] ("Electroless and electrolytic copper plating is applied to … the copper foil 5, 6" to form even thicker metal layers), [0024]-[0028], [0034]-

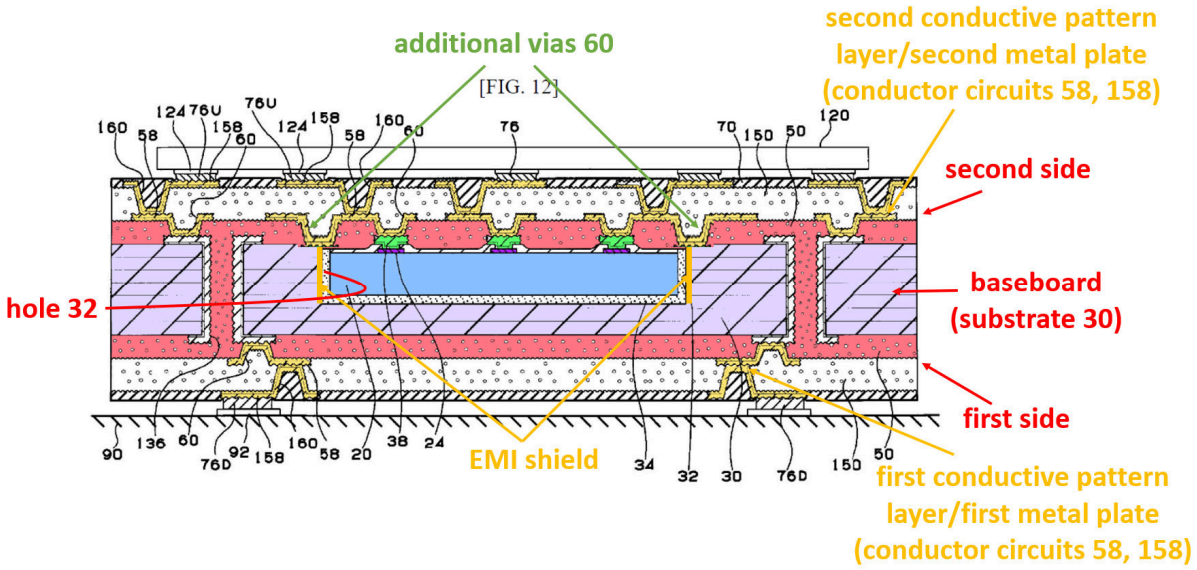
[0036], Cls, 3, 4, 5, FIGS. 1, 4; APPLE-1003, ¶85.

3. Predictable Combination of Sakamoto and Eiji

A POSITA would have been motivated to implement a shield layer on the sidewalls of the hole with the electronic component embedded therein, in accordance with Eiji[4], in Sakamoto's multilayer printed wiring board to achieve known benefits. APPLE-1003, ¶95. For example, a POSITA would have done so based on Eiji's suggestions to make the electronic components built into an insulating substrate "less susceptible to external electromagnetic waves," to "reduce the effects of noise generated by the circuits constituting these electronic components," and/or to "stabilize the electrical characteristics" of the system, consistent with Sakamoto's objectives of higher functionality, high-speed operation and improved reliability. APPLE-1012, [Abstract]; *see also*, [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1004, Abstract, [0006], [0070]-[0071]; APPLE-1003, ¶95.

[4] Unlike Takeuchi, in that Eiji's shielding layer 10 in the through-hole for accommodating electronic components, and layers 26 and 27 on both sides of the components, are in the finished module and provide structure for EMI shielding. APPLE-1003, ¶95.

In the predictable combination, a shielding layer composed of a copper plating film that shields electromagnetic waves (e.g., shielding layer 10) is formed on an inner surface of the recessed portion in the core substrate (e.g., recessed portion 32 in core substrate 30), before inserting IC chip, in accordance with Eiji's suggestions. APPLE-1004, [0005]-[0007], [0023]-[0025], [0066]; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶96. Additionally, at least one of the conductive circuit layers (e.g., Sakamoto's 58 and 158) above the IC chip and at least one of the conductive circuit layers (e.g., Sakamoto's 58 and 158) below the IC chip, implemented in accordance with Eiji's suggestions to provide EMI shielding, have portions electrically connected to each other and to the copper film on the sidewalls of hole 32 through additional vias (e.g., vias 60 already taught by Sakamoto), and connected to the ground to provide enhanced shielding effect, in accordance with Eiji's teachings. APPLE-1012, Abstract, [0008], [0010]-[0011], [0013]-[0014], [0021], [0023]-[0028], [0034]-[0036], Cls, 4, 5, FIGS. 1, 4; APPLE-1003, ¶97.



APPLE-1003, ¶97 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

Multiple reasons would have prompted a POSITA to utilize EMI shielding, in accordance with Eiji's suggestions, in the multilayer printed wiring substrate. APPLE-1003, ¶98.

First, a POSITA would have been motivated to combine Sakamoto and Eiji to provide protection against external electromagnetic waves, reduce influence by noise from circuits composed of various electronic components, and/or to stabilize electric characteristics of the entire system. APPLE-1003, ¶99.

Sakamoto already teaches accommodating an electronic component such as an IC chip 20 in a space (e.g., "recessed portion 32") in the core substrate, and that multiple components can be included in close arrangement. APPLE-1004, [0066]; *see also*, [0005]-[0007], [0011], [0023]-[0025], [0069]-[0071]; *see also*, ; APPLE-1003, ¶100. A POSITA would have been motivated to mitigate against external

electromagnetic waves or noise generated by circuit components, especially where multiple components are used in close proximity. APPLE-1012, [Abstract]; APPLE-1003, ¶101. Eiji provides a known technique that would have been recognized to further "stabilize the electrical characteristics" of the system. APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012] [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶101-102. Moreover, a POSITA would have been motivated, based on Eiji's suggestions, to enhance the shielding effect by implementing conductor circuits 58, 158 to have the structure and configuration that provides EMI shielding (e.g., above and below the component) in accordance with Eiji. *Id.*

Second, a POSITA would have been prompted to combine Sakamoto and Eiji because doing so was the application of known techniques (forming a shield layer on the inner surface of sidewalls of a through hole provided in an insulating board for incorporating an electronic component and grounding wiring layers above and/or below the embedded component for additional shielding effect) to a known device (Sakamoto's multilayer printed wiring board having an opening or recessed portion 32 in insulating substrate 30 to accommodate an electronic component such as IC chip 20 between wiring layers) ready for improvement to yield predictable results (benefits articulated above). *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) ("[W]hen a patent 'simply arranges old elements with

each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious."). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Sakamoto and Eiji describe similar wiring boards with electronic components embedded inside holes of an insulation board, and because the modifications would have been implemented largely by adding a metal layer on the sidewalls of the hole and grounding wiring layers above and/or below the components, in order to create interference protection around the electronic components—a configuration Eiji already demonstrates to be successful. APPLE-1003, ¶¶103-104. Sakamoto and Eiji describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems discussed above associated with semiconductor packaging and manufacturing. *Id*.

4. Application to Challenged Claims

[1pre]

If the preamble is deemed limiting, Sakamoto-Eiji teaches a ***circuit board***. APPLE-1003, ¶¶106-108. For example, Sakamoto describes "a multilayer printed wiring substrate" comprising a "core substrate 30" in which IC chips (e.g., "IC chip 20") and other "electronic components" are embedded. APPLE-1004, Title,

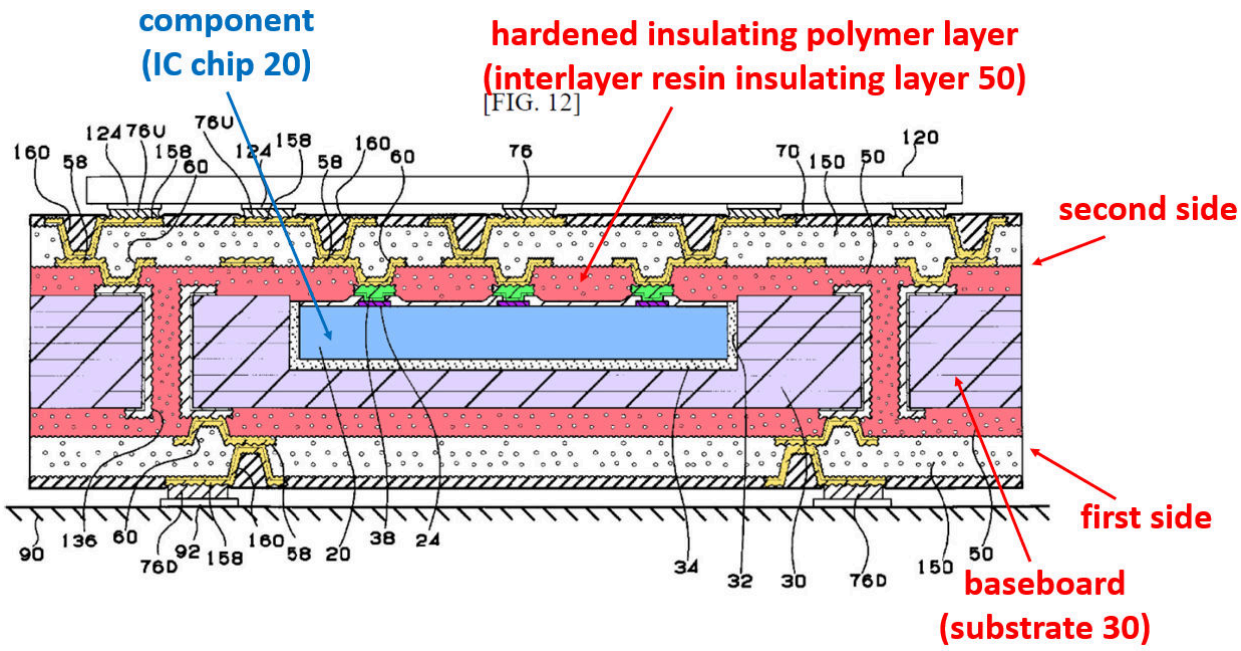
Abstract, [Claim 1], [0001], [0005]-[0007], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. Substrate 30 is made of "any material generally used in printed wiring substrates," such as "epoxy resins, BT resins, and phenol resins impregnating a reinforcing material such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin." *Id*., [0012], [0020], [0023] ("an insulating resin substrate (core substrate) 30 laminated with a pre-preg in which a core material such as **glass cloth** has been impregnated with a resin such as an epoxy is used as the starting material"); APPLE-1003, ¶¶106-107. Sakamoto's disclosure of suitable material for substrate 30 is thus just like the '944 patent's description for its "baseboard 1 [] selected for the circuit-board manufacturing process," such as "a glass-fibre reinforced epoxy board." APPLE-1001, 3:46-55, Cl. 9; APPLE-1003, ¶108.

Accordingly, through Sakamoto's disclosure of "wiring substrate" comprising "substrate 30" to incorporate IC chips, Sakamoto-Eiji provides [1pre].

[1a]

Sakamoto's "substrate 30" made of insulating material and "interlayer resin insulating layer 50" together provide an ***insulating material layer***. APPLE-1004, [0001], [0003], [0011], [0053], [0056]-[0057], [0078], FIG. 12; APPLE-1003, ¶109. The combination of Sakamoto's substrate 30 and the interlayer resin

insulating layer 50 has a lower side (***first side***) and an upper side (***second side***). APPLE-1003, ¶109.



APPLE-1003, ¶109 (APPLE-1004, FIG. 12 (Annotated))

To be clear, Sakamoto's interlayer resin insulating layer 150 on the interlayer resin insulating layer 50, together with "substrate 30" and "interlayer resin insulating layer 50" likewise provide an ***insulating material layer***, having a first side (and second side) on the lower (and upper) side of the lower interlayer resin insulating layer 150, and thus Sakamoto-Eiji discloses [1a] in this second manner. APPLE-1003, ¶110.

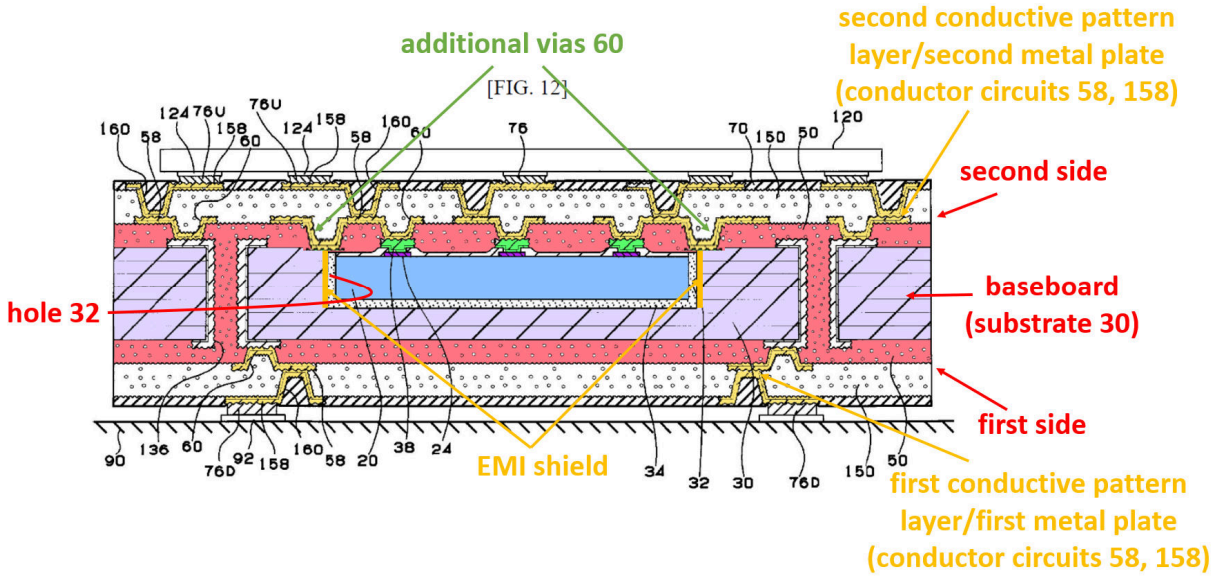
[1b]-[1c]

Sakamoto-Eiji renders obvious Elements [1b]-[1c]. APPLE-1003, ¶¶111-120. For example, Sakamoto describes a "conductor circuit 58" that is "formed in

an interlayer resin insulating layer 50," and a "conductor circuit 158" that is "formed in interlayer resin insulating layer 150." APPLE-1004, [0017]; *see also id.*, [0005]-[0007], [0012], [0015], [0027]-[0028], [0032]-[0037] (describing the formation of the conductor circuits made of an electroless plated film and an electrolytic plated film), [0062], FIGS, 4-6, 9-12; APPLE-1012, Abstract, [0007], [0008], [0010]-[0011], [0013]-[0014], [0021], [0023]-[0028], [0034]-[0036]; APPLE-1003, ¶¶111-113.

The conductor circuit layers 58 and 158 are patterned through photoetching or laser and provide ***conductive pattern layers***. APPLE-1003, ¶111.

Sakamoto's patterned conductor circuit layers 58 and 158 are arranged on both sides of the wiring board, with a portion of the conductor circuit layers 58 (and/or 158) (***at least one first conductive pattern layer***) on the lower side (***first side***) and another portion of the conductor circuit layers 58 (and/or 158) (***at least one second conductive pattern layer***) on the upper side (***second side***). *Supra*, §VI.A.4, Analysis of Element [1a]; APPLE-1003, ¶112-114.



APPLE-1003, ¶116 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

In the combined system, at least one of the conductive circuit layers 58 and 158 on the first side of the substrate are implemented in accordance with Eiji's wiring layer 26 or 27, which serves as ***the first conductive pattern layer defining a first metal plate***, and at least one of the conductive circuit layers 58 and 158 on the second side of the substrate are implemented in accordance with Eiji's wiring layer 26 or 27, which serves as ***the second conductive pattern layer defining a second metal plate***. *Supra*, §§VI.A.3 (Sakamoto-Eiji combination); *infra*, §VI.A.4, Analysis of Claim [5]; APPLE-1003, ¶115-116. They are electrically connected to each other (e.g., through additional vias 60) and to the EMI shield on the sidewalls of hole 32, and grounded to provide enhanced shielding effect, in accordance with Eiji's teachings. *Id.*

Further, Sakamoto describes the formation of conductive circuit layers 58 and 158 by first forming an electroless plated film 52 "on the surface of interlayer resin insulating layer 50" by immersing the entire substrate in an electroless plating solution, then forming an electrolytic plated film 56 on top of film 52, together forming "a conductor circuit 58 and vias 60 with a thickness of 16 μm made of the electroless plated film 52 and electrolytic plated film 56," and next forming additional interlayer resin insulating layers 150 and conductor circuits 158 (including vias 160) on top by repeating the same steps. APPLE-1004, [0032]-[0037]; APPLE-1003, ¶117.

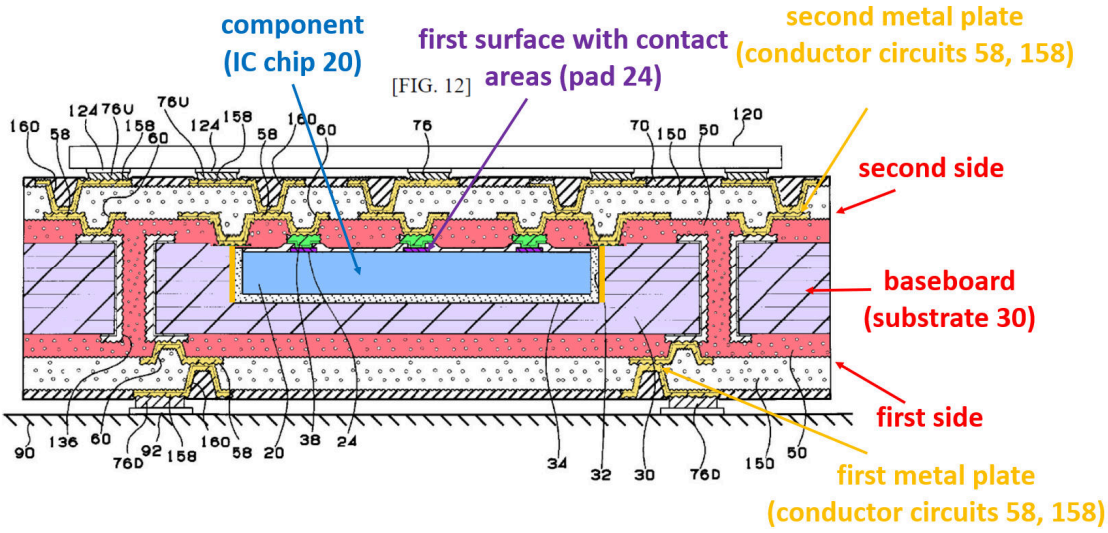
This is just like the '944 patent's disclosure of the metal plates, where "[i]n stage J, a polymer film [11] is formed on the first surface (1a) of the circuit board, followed by a thin metal coating 12 on top of the polymer film. In the example process, stage J is carried out by laminating a thin polymer film… on the surface of the circuit board, on top of which is **a layer of copper (e.g., c. 5 μm)**." APPLE-1001, 5:47-56, FIG. 1J, 8:44-9:41; *see also id.*, 4:40-59 (describing a similar process for forming a metal coating 8 in the form of "a layer of copper (e.g., c. 5 μm)" on the bottom side of the circuit board below the microcircuit at Stage F, (FIG. 1F)); APPLE-1003, ¶¶118-119.

To the extent the '944 patent's description of forming a metal plate in connection with the making of the circuit board's conductive pattern requires

growing a thicker metal film from its "metal coating 12" and/or "metal coating 8," which it does not, Sakamoto-Eiji satisfies it. APPLE-1001, FIGS. 1F, 1J, 4C, 4D, 4:40-63, 5:47-6:4, 8:44-9:41; APPLE-1003, ¶120. Sakamoto-Eiji's conductive circuit layers 58 and 158 have a substantial thickness (e.g., "16 μm"). APPLE-1004, [0032]-[0037]; APPLE-1001, 5:51-56 ("e.g., c. 5 μm"); *see also* APPLE-1012, [0017] (Eiji describing layers 26, 27 above and below embedded electronic components formed from "copper foil 5, 6 that is several 10 μm thick"), [0021] (plating over copper foil 5, 6 to form even thicker metal layers), [0022], [0025]; APPLE-1003, ¶120.

[1d]

Sakamoto-Eiji renders obvious Element [1d]. APPLE-1003, ¶¶121-122. In particular, Sakamoto's "IC chip 20" (***component***) is embedded inside substrate 30 of the wiring board (part of ***the insulating material layer***). *Supra*, §VI.A.2, Analyses of [1pre]-[1a]. IC chip 20 is located between conductor circuits 58 (and circuits 158) on respective sides of the substrate (***between the first and second metal plates***). *Supra*, §§VI.A.4, Analyses of Elements [1b]-[1c], FIG. 12; APPLE-1003, ¶121.



APPLE-1003, ¶121 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

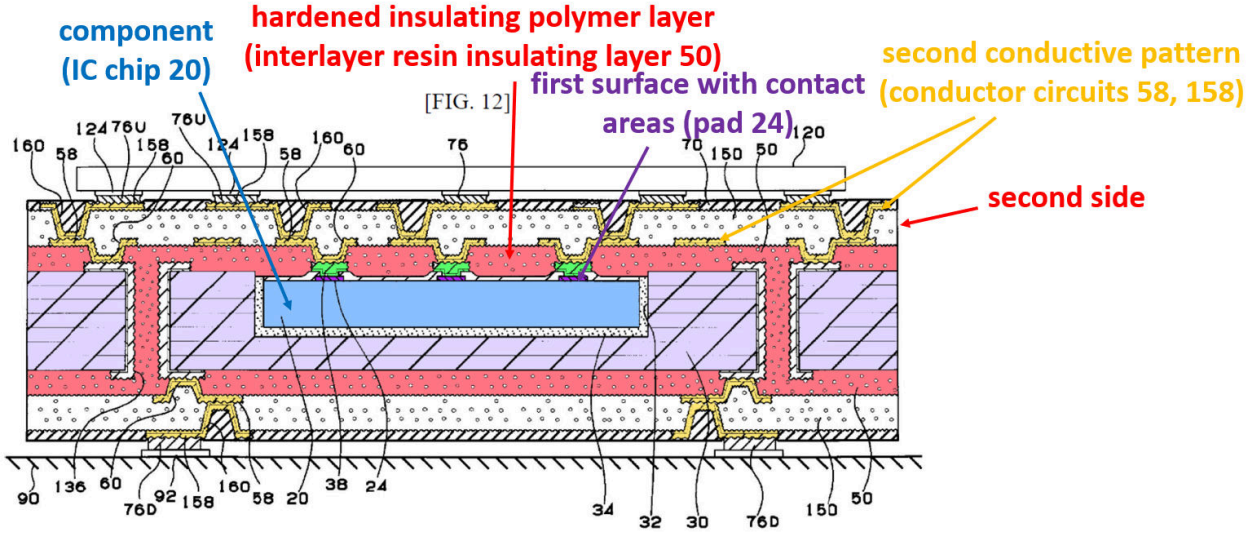
Sakamoto further describes that IC chip 20 has "die pads 24" (***contact areas***) on a surface (***first surface***) facing towards the conductor circuits 58 and 158 on the second side of the wiring board. APPLE-1004, Abstract, [0018], FIG. 12; APPLE-1003, ¶122.

Accordingly, through at least disclosure of "IC chip 20," Sakamoto provides Element [1d].

[1e]

Sakamoto-Eiji provides ***a hardened insulating polymer layer*** (e.g., Sakamoto's interlayer resin insulating layer 50). APPLE-1003, ¶¶123-126; APPLE-1004, [0017], [0030], [0042]-[0043]. For example, Sakamoto describes resins used for the interlayer resin insulating layer 50 that are ***polymer***s. APPLE-1003, ¶123; APPLE-1004, [0030] ("thermosetting cycloolefin resin"), [0042]

("epoxy resin"), [0047], [0053]-[0060]. Further, a POSITA would have understood and found it obvious, based on Sakamoto's description, that interlayer resin insulating layers 50 and 150 are ***hardened*** through chemical and thermal curing. APPLE-1004, [0042] ("curing agent"), [0053] ("heat treatments"), [0054] ("heat cycle conditions"), [0058] (examples of "curing agents"), [0059] ("curing of the resin film"); APPLE-1003, ¶124.



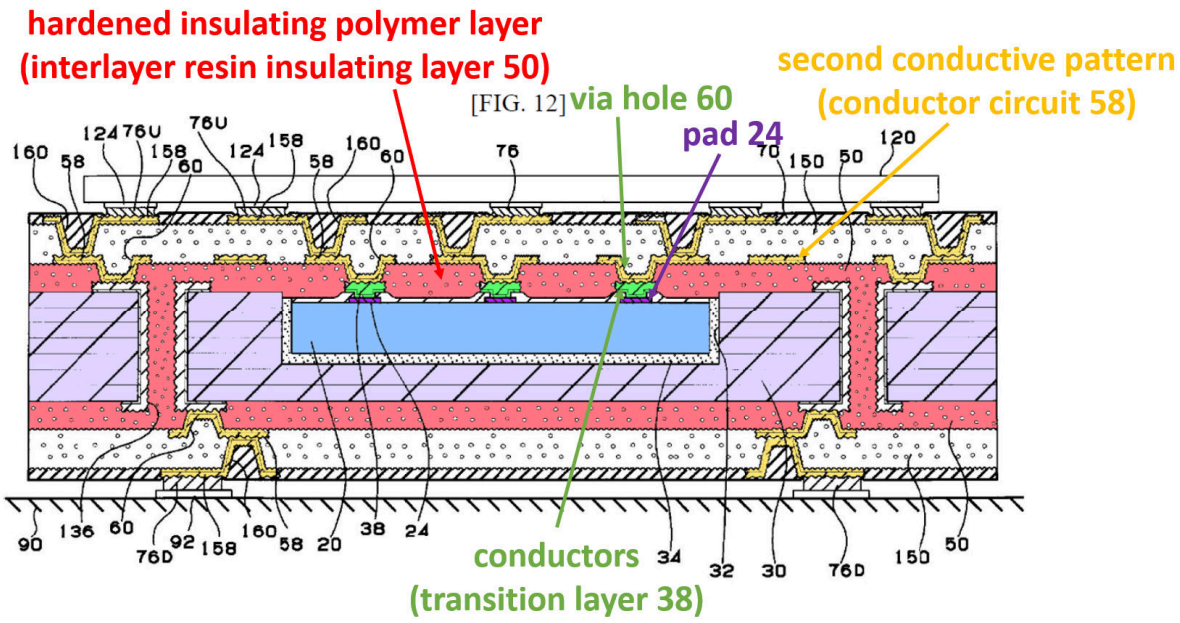
APPLE-1003, ¶124 (APPLE-1004, FIG. 12 (Annotated))

In Sakamoto-Eiji, the interlayer resin insulating layer 50 is ***between the first surface of*** IC chip 20 (***component***) and conductor circuits 58 and 158 on the second side of the wiring substrate (***at least one conductive pattern of said at least one second conductive pattern layer***). APPLE-1003, ¶125; APPLE-1004, [0030]-[0037]; *see also*, [0017]. Notably, dependent claim 8 recites that the "insulating material layer includes a baseboard and the hardened insulating polymer layer,"

indicating that the ***insulating material layer*** of claim 1 (e.g., "substrate 30" and "interlayer resin insulating layer 50," and one or more other layers) encompasses a ***baseboard*** and ***hardened insulating polymer layer*** (e.g., interlayer resin insulating layer 50 between the component and conductor circuits 58 and 158 on the second side of the wiring substrate). APPLE-1003, ¶126; *supra*, Analysis of [1a]; *infra*, Analysis of Claim 8.

[1f]

Sakamoto-Eiji discloses Element [1f]. APPLE-1003, ¶¶127-131. For example, Sakamoto describes that "vias are formed in the interlayer insulating layers, and electrical connections are established through the vias" (***contact openings in the hardened insulating polymer layer***). APPLE-1004, [Claim 1], [Claim 4]. For example, "via holes 60" are formed in the interlayer resin insulating layers 50 and connected with die pads 24 of the IC chip either directly or through "transition layer 38" (also in the interlayer resin insulating layer 50 and defining an extended opening of the vias). APPLE-1004, Abstract, [0005]-[0007] ("providing vias on the IC chip pads using photoetching or a laser to form a conductor circuit that is a conductor layer"), [0008] ("via holes in interlayer resin insulating layers"), [0067] ("in the third embodiment, the vias 60 are connected directly to the pads 24 without providing a transition layer"), FIGS. 3-6, 9-12; APPLE-1003, ¶127.



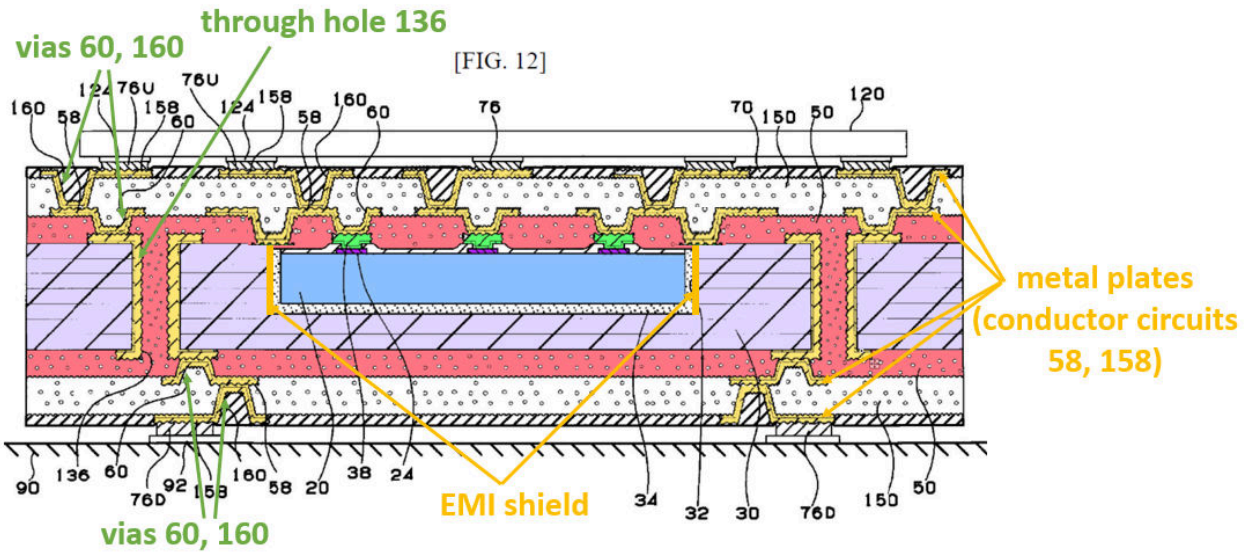
APPLE-1003, ¶127 (APPLE-1004, FIG. 12 (Annotated))

Portions of the conductor circuit extending into the via hole and the "transition layer 38," individually or collectively, provide ***conductors in the contact openings for forming electrical contacts between the contact areas of the component and the at least one second conductive pattern layer or layers***. APPLE-1003, ¶¶128-131. Indeed, in the combined system, portions of conductor circuit (e.g., as shown by Sakamoto's 58) extend into the via hole 60, and the transition layer 38 is formed on the contact pads 24 (***contact areas***) of the IC chip 20, for "direct connection of an IC chip, which is a semiconductor element, to [conductor circuit 58 of] a printed wiring substrate," such that "the via can be reliably connected to the die pad, improving reliability." APPLE-1004, [0008]-[0010]; *see also*, Abstract ("by providing a transition layer 38 on the die pad 24 … connectivity between and reliability of die pads 24 and via hole 60 can be

improved"), [Claim 4], [0007], [0009]-[0010], [0067], [0071], FIGS. 3-6, 9-12; APPLE-1003, ¶¶128-130. To be clear, these conductors are mechanically and electrically connected with the parts of the conductor circuit 58 outside the via hole 60 and on the top surface of the interlayer resin insulating layer 50, as well as with pads 24 on the IC chip component. APPLE-1003, ¶131.

[2]

As discussed in §§VI.A.4, Analyses of Elements [1b]-[1c], Sakamoto-Eiji's metal plates (e.g., conductor circuits 58 and 158 on both sides of the wiring board) are ***electrically connected to each other***, through vias 60, 160, and through holes 136, which are metal-lined holes through substrate 30 and in electrical connection with conductor circuits 58 and 158 through the vias. *E.g.*, APPLE-1004, [0069] (describing an electrical connection path including "a conductor circuit 158, vias 160, another conductor circuit 58, vias 60, through-holes 136, vias 60, another conductor circuit 58, vias 160, another conductor circuit 158"), FIG. 12; APPLE-1003, ¶132.



APPLE-1003, ¶132 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[3][5]

In the combined system, conductor circuits 58 and 158 (conductive pattern layers defining the ***metal plates***) of the wiring substrate (***circuit board***) with embedded electronic components are connected to ground to provide enhanced shielding effect and disclosing [3]. *Supra*, §§VI.A.3 (Sakamoto-Eiji combination), VI.A.4, Analyses of [1b]-[1c] and Claim [2]; APPLE-1003, ¶133. A POSITA would have found it obvious that Sakamoto-Eiji's ground connection be

[5] Claim 3 recites an "earth connection of the circuit board," which amounts to a non-limiting statement of use. Nonetheless, even if considered to be limiting, it is disclosed by Sakamoto-Eiji.

implemented to provide ***an earth connection.*** There are only two possibilities: earth the ground connection or not. The well-known benefits of facilitating enhanced EMI shielding when electrically connected to an earth connection would have prompted a POSITA to utilize an earth connection. APPLE-1003, ¶133.

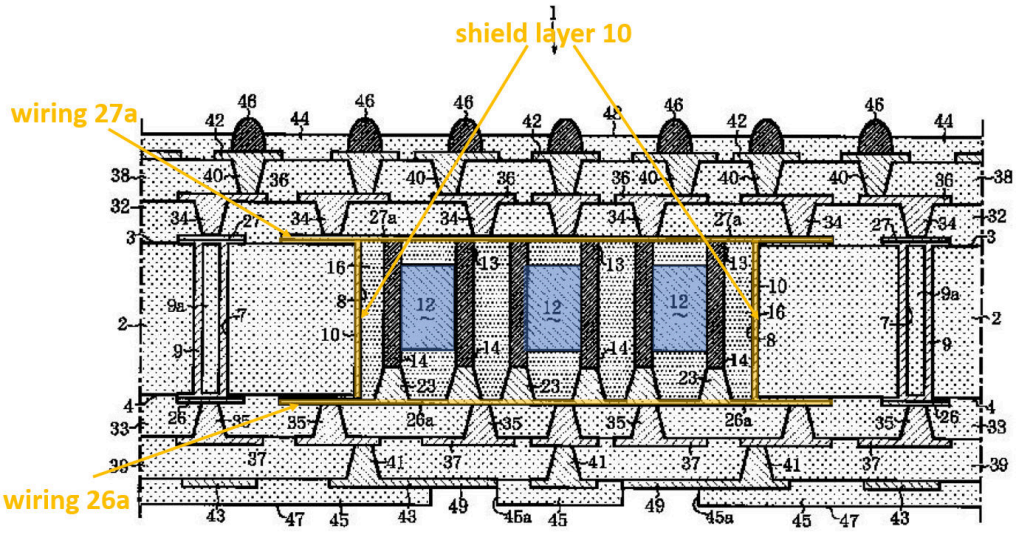
[4]

As discussed in §VI.A.3 (Sakamoto-Eiji combination), the combined system includes an IC chip (***component***) located in a recess (e.g., recessed portion 32) in the insulating substrate 30 (***baseboard*** of the ***insulating material layer***). APPLE-1003, ¶134. A shield layer composed, for example, of a copper plating film that shields electromagnetic waves is formed on an inner surface of the hole and provides a ***metal foil covering the sidewalls of the hole***, as claimed. *Supra*, §VI.A.3; APPLE-1003, ¶134. The shielding layer material and configuration of the combined system, in accordance with Eiji's teaching, is just like the formation mechanism disclosed in the '944 patent for growing the ***metal foil on the sidewalls of the holes*** by copper plating. APPLE-1012, [Abstract], [0012]; *compare id.*, [0017] ("electroless copper plating and electrolytic copper plating are performed on the inner surfaces of through-hole 8") *with* APPLE-1001, 3:61-4:9 ("metal 4" "is grown into the through holes" at Stage C (FIG. 1C), by "coating the holes with a thin layer of chemical copper and then continuing the coating using an electrochemical copper-growing method…"), 8:39-46; APPLE-1003, ¶135-136.

The combined system includes filler material in the hole between the metal foil and the component. For example, Sakamoto describes "an adhesive material 34" applied to recessed portion 32 before "IC chip 20 is placed on the adhesive material 34" in the recessed portion. APPLE-1004, [0024]. A POSITA would have recognized that the "adhesive material" provides ***a filler material in the hole between the metal foil and the*** IC chip 20 (***component***). APPLE-1003, ¶137. This is also consistent with, and further rendered obvious, based on Eiji's teaching of a "resin 16, which is primarily epoxy resin" to secure each component at "a predetermined location in the through-hole." APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1, 3; APPLE-1003, ¶¶137-138.

[5]

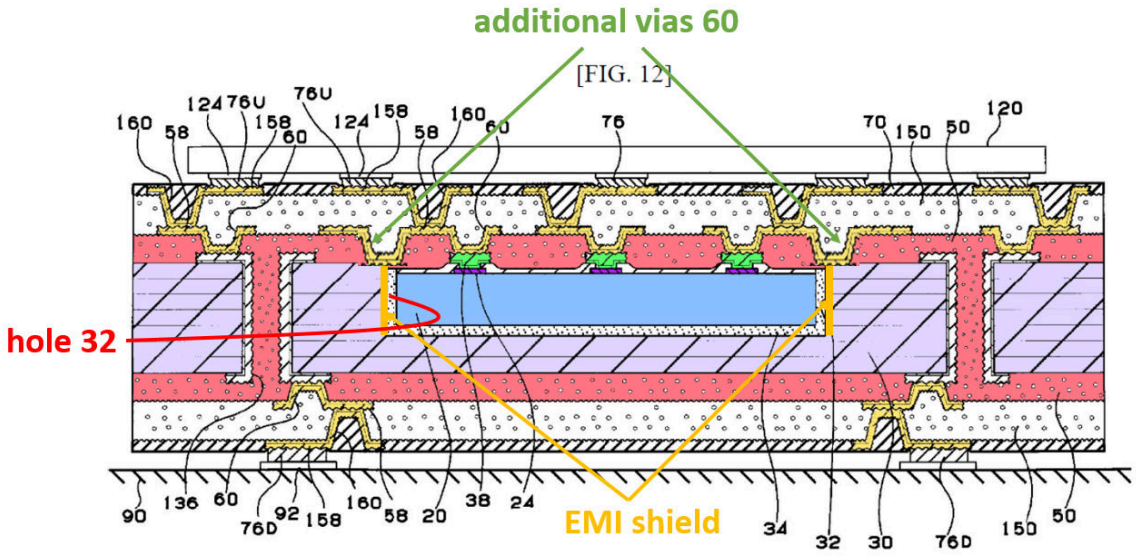
For example, Eiji describes a shield layer connected to a "ground layer or power layer" to provide more accurate and reliable operation of the electronic components and more reliable EMI shielding. APPLE-1012, [0007]. Eiji teaches connecting shielding layer 10 covering the sidewalls of hole with wiring layers 26a and 27a in the upper and lower openings of the through holes 8, which also serve as shield layers, and the wiring layers 26, 27 are used as ground layers or power layers. *Id.*, [0007], [0011], [0013], [0015], [0023], FIG. 1; APPLE-1003, ¶139.



APPLE-1003, ¶139 (APPLE-1012, FIG. 1 (Annotated))

A POSITA would have been prompted and found obvious to implement this connection (***electrically connected***) for the shield layer (***metal foil***) of the Sakamoto-Eiji system with the conductive circuits 58 and 158 (conductive pattern layers defining ***metal plates***) in the upper and lower sides of the wiring substrate, in accordance with Eiji, such as through additional vias in the insulating substrate (e.g., in the interlayer resin insulating layer 50) using the suggested techniques for forming the existing vias, to achieve the benefits of more accurate and reliable operation of the electronic components and more reliable EMI shielding. APPLE-1003, ¶¶140-142; *supra*, §VI.A.4, Analysis of Claim [2] (conductive circuits 58 and 158 on both sides of the wiring substrate are also electrically connected through conducting feed-throughs 136), §VI.A.3 (Sakamoto-Eiji combination). In the resulting combination, additional vias 60 connect the shield layer in the hole

with conductor circuits in the upper and lower sides of the wiring board, for example.



APPLE-1003, ¶142 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

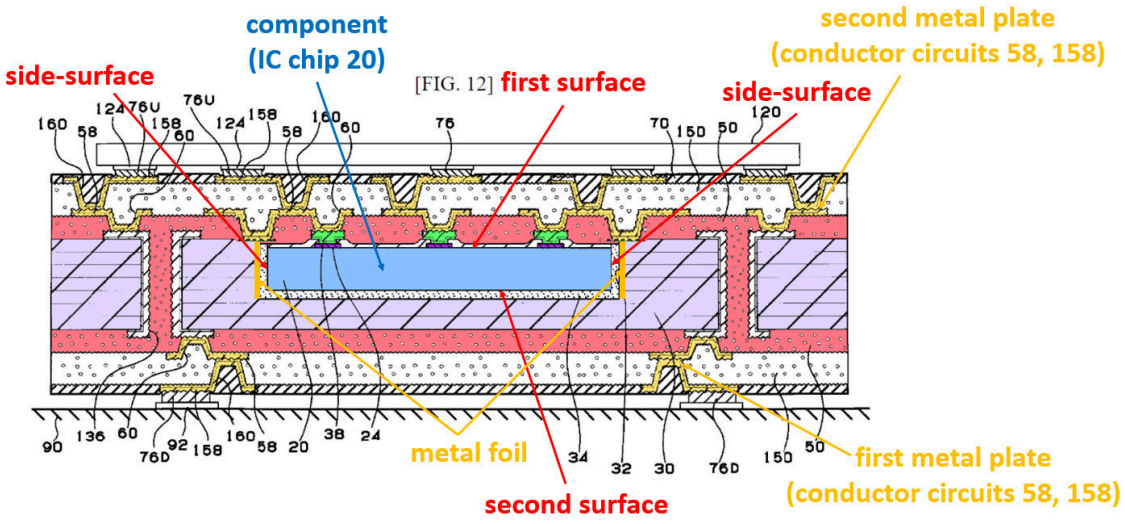
[6]

As discussed above, Eiji discloses that shielding layer 10 covering the sidewalls of the hole for incorporating electronic components is connected to a "ground layer," which "enabl[es] the electronic components to operate more precisely and reliably while shielding them from any noise that may occur." APPLE-1012, FIG. 1, [0007]; *supra*, §VI.A.4, Analysis of Claim [5]. A POSITA would have been prompted and found obvious to implement this ground connection (***an earth connection***) for the shield layer (***metal foil***) of the Sakamoto-Eiji system, in accordance with Eiji to advance express benefits of more accurate

and reliable operation of the electronic components and more reliable EMI shielding. APPLE-1003, ¶144; *supra*, §§VI.A.3 (Sakamoto-Eiji combination), VI.A.4, Analyses of [1b]-[1c] and Claims [3] (obvious to earth a ground connection) & [5].

[7]

As discussed above, in the combined system, the metal plates and the metal foil covering the sidewalls of the through-hole or recessed portion 32 are electrically connected and grounded, forming an electromagnetic interference shield around IC chip 20 (***component***), such that the side-surfaces of IC chip 20 face towards the metal foil, the first surface of IC chip 20 face towards the conductor circuits on the top side of the wiring substrate (***second metal plate***) and the second surface opposite to the first surface of IC chip 20 ***face towards*** the conductor circuits on the bottom side of the wiring substrate (***first metal plate***). *Supra*, §§VI.A.3 (Sakamoto-Eiji combination), VI.A.4, Analyses of [1b]-[1c] and Claim [5]; APPLE-1003, ¶145.



APPLE-1003, ¶145 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[8]

The Sakamoto-Eiji's insulating material layer includes a baseboard (e.g., "substrate 30") and the hardened insulating polymer layer (e.g., "interlayer resin insulating layer 50"). *Supra*, Analysis of [1pre], [1e]; APPLE-1003, ¶146.

Even if Sakamoto's description of materials for its core substrate 30 were considered not to provide a baseboard as recited (which it does), the Sakamoto-Eiji combination renders it obvious. APPLE-1003, ¶146. For example, Eiji describes "a glass-epoxy resin composite material" for its insulating substrate where electronic components are embedded. APPLE-1012, [0012], [0038] ("glass woven fabrics or composite materials of **glass fibers** and resins such as **epoxy resin**"), Abstract. A POSITA would have been motivated to facilitate enhanced mechanical strength of Sakamoto's substrate 30 by using composite materials of

glass fibers with epoxy resin, in accordance with Eiji's teaching, and would have had a reasonable expectation of success in doing so. APPLE-1003, ¶¶147-148. The resulting baseboard has a construction just like the '944 patent's example. APPLE-1001, 3:45-55.

[9]

See, *supra*, §VI.A.4, Analysis of Claim [8] (describing composite materials of glass fibers with epoxy resin); APPLE-1003, ¶149.

[10]

In the Sakamoto-Eiji combination, the component is located in a hole (e.g., recessed portion 32) in the baseboard, and the circuit board comprises conductive material on the sidewalls of the hole and a filler material in the hole between the metal foil and the component, in accordance with Eiji. *Supra*, §VI.A.4, Analysis of Claim [4]. The metal foil (e.g., layer "composed of a copper plating film" covering the sidewalls of through-hole 32) creates an interference protection structure around the component. APPLE-1012, Abstract, FIG. 1; *see also*, [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0041], Cls. 1, 6; APPLE-1003, ¶150.

[11]

As noted in §III.A., recitation of "electrochemically deposited" and "chemically deposited" copper is a product-by-process element, and thus not

limiting for purpose of invalidity. Sakamoto describes copper, as claimed. That is enough.

To be clear, even if the process recitations were considered limiting, Sakamoto-Eiji renders obvious Claim [11]. APPLE-1003, ¶151-153. As discussed in §VI.A.4, Analysis of Element [1f], Sakamoto-Eiji's "transition layer 38" in the vias on the IC chip pads provide ***conductors in the contact openings***. Sakamoto describes that transition layer 38 made of copper is composed of at least an "electroless plated film 36" and an "electrolytic plated film 37." APPLE-1004, [0028]; *see also*, Abstract, [Claim 4], [0007], [0008], [0009], [0010], [0014] ("thickened by **electroplating**"), [0015] ("thickened by **electroless or electrolytic plating**," and "[**c**]**opper is preferably used**"), [0018], [0020]-[0021], [0027], [0028], [0031], [0035], [0067], [0069], [0070], [0071], FIG. 2; APPLE-1003, ¶151. "Electroplating" such as "electrolytic plating" provides an electrochemical plating technique (***electrochemically deposited copper***), and "electroless plating" provides a chemical plating technique (***chemically deposited copper***), as recited by claim 11. APPLE-1003, ¶152.

To be clear, conductor circuit 58 extending into vias 60 in direct contact with die pads 24 (e.g., where a transition layer 38 is not used) is also formed of an electroless plated film 52 and an electrolytic plated film 56 using copper. APPLE-1004, [0032]-[0037], FIG. 4; *supra*, §§VI.A.4, analyses of [1b]-[1c], [1f]; APPLE-

1003, ¶153.

[12]

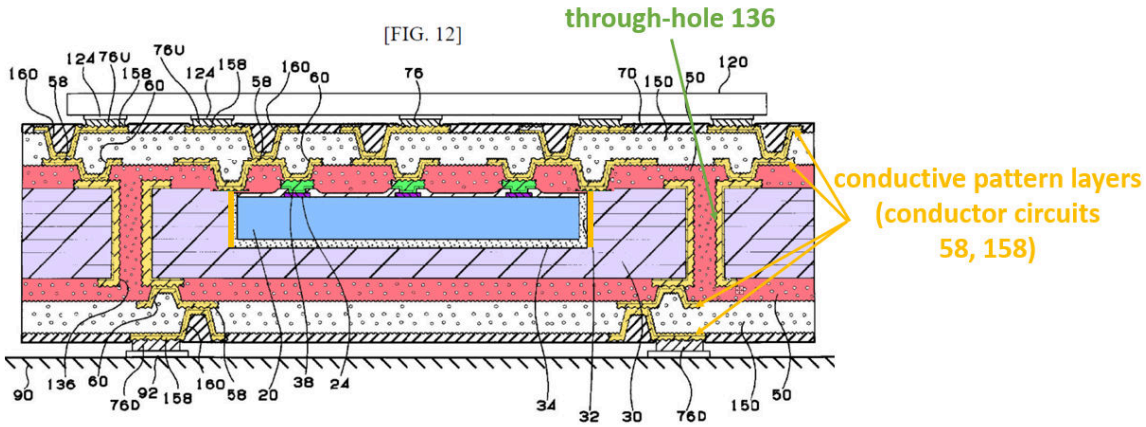
As discussed with respect to [1e], "interlayer resin insulating layer 50" (***hardened insulating polymer layer***) contains "***epoxy*** resin." APPLE-1003, ¶154; *supra*, §VI.A.4, Analysis of [1e].

[13]

For example, Sakamoto describes the electric component includes an "IC chip" in substrate 30. *E.g.*, APPLE-1004, [0006]-[0007]; *see also*, Abstract, [Claim 1], [Claim 4], [0001], [0012], [0070]; *supra*, §§VI.A.4, Analyses of [1pre], [1d]; APPLE-1003, ¶155. A POSITA would have understood that "IC chips"—integrated circuit chips—are a type of ***microcircuit***. An IC chip is a miniaturized electronic circuit that contain a network of interconnected semiconductor devices (e.g., transistors and diodes) and passive components (e.g., resistors, inductors, and capacitors), on a small substrate (e.g., fabricated onto a single semiconductor wafer). APPLE-1003, ¶155.

[14]

For example, metal-lined through-holes 136 provide ***an electrically conducting feed-through between the conductive pattern layers*** (e.g., conductor circuits 58 and 158) ***on the both sides of the insulating material layer*** of the wiring board. *Supra*, §VI.A.4, Analysis of Claim [2]; APPLE-1003, ¶156.



APPLE-1003, ¶156 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[15pre]

Sakamoto-Eiji renders obvious Claim [15]. APPLE-1003, ¶¶157-166. Claim 15 recites identical limitations of the ***at least the first circuit board substructure*** of a ***multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other*** as those recited in Claim 1 for ***a circuit board***. *Compare* APPLE-1001, Cl. 1 *with id.*, Cl. 15. These same limitations of Claim 15 are rendered obvious by Sakamoto-Eiji for at least the same reasons provided in §§VI.A.4, Analyses of [1pre]-[1f].

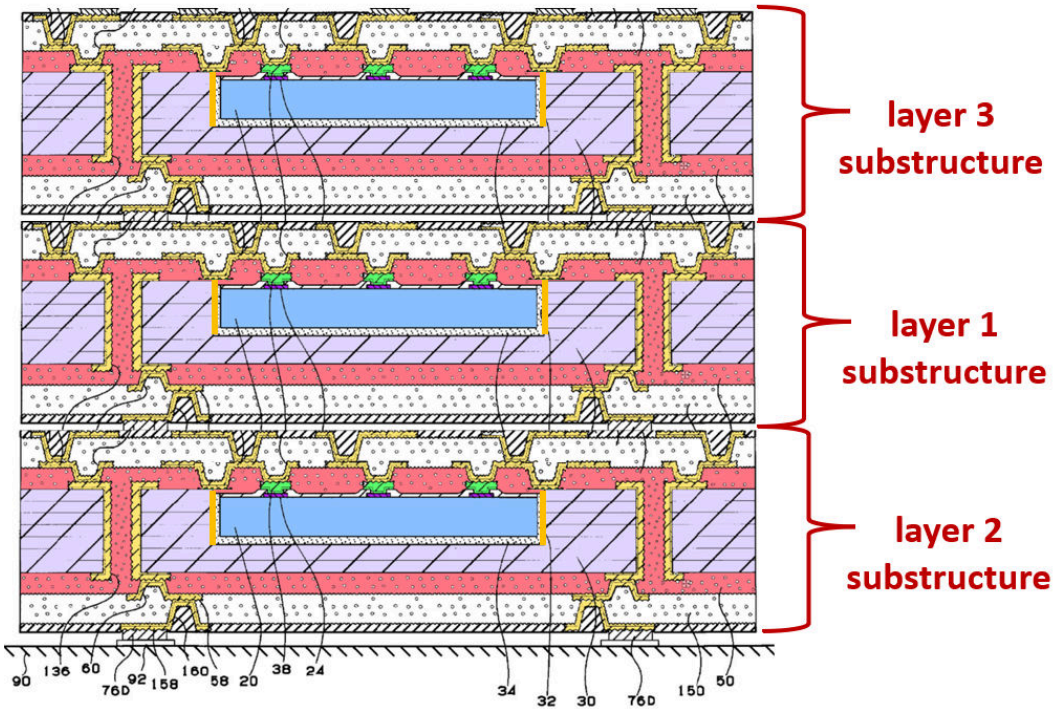
To the extent the preamble of Claim 15 is limiting, Sakamoto-Eiji also renders it obvious. APPLE-1003, ¶¶157-166. Sakamoto describes connections with "external substrates such as motherboards and daughterboards," as well as mounting electronic components such as IC chips with different functions, thereby obtaining a multi-layer printed wiring substrate with higher functionality. APPLE-1004, [0006], [0011]; *see also*, [0068]-[0070]; APPLE-1003, ¶158. Indeed,

stacking multiple layers of circuit-board substructures on top of each other and mounting a plurality of electronic components in the same as well as different such layers to achieve high-density, improved performance, reduced manufacturing cost, space saving, and short-distance wiring was common practice and well known in the field. APPLE-1003, ¶¶159-163. This is further highlighted by the analysis during original prosecution, which was not disputed by applicant—"it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a first circuit board substructure and a second circuit board substructure on top of each other, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art." APPLE-1002, 107-110; APPLE-1003, ¶164.

A POSITA would have understood and found obvious that a plurality of Sakamoto-Eiji's wiring substrates are beneficially stacked on top of each other, with the layers of these substructures mechanically and electrically connected to each other, through the vias (e.g., vias 60, 160) and through holes (e.g., through-holes 136) within each layer and the connection mechanisms between substrates, to achieve desirable "higher functionality" and the other benefits articulated above. APPLE-1003, ¶165; *supra*, §VI.A.4, Analysis of Claim [2].

The multi-layered configuration would have required only the same known techniques (e.g., already evident in Sakamoto) for connecting to "external

substrates" such as "motherboards and daughterboards," including the use of "BGA, Solder bumps, and PGA (conductive connection pins)," among other common and routine mounting methods for high-density circuitry semiconductor devices. APPLE-1004, [0011], [0069]-[0070]; APPLE-1003, ¶166. The resulting device, e.g., based on Sakamoto's FIG. 12, includes a multi-layered configuration having three similar substructure layers, including "layer 1 substructure" (i.e. substructure 1, which contains one or more layers), "layer 2 substructure" (i.e. substructure 2, which contains one or more layers) (***a first circuit board substructure and second circuit board substructure on top of each other***) and "layer 3 substructure" (i.e. substructure 3, which contains one or more layers).



APPLE-1003, ¶166 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[15a]-[15f]

Supra, §§VI.A.4, Analyses of [1a]-[1f]; APPLE-1003, ¶167.

[16]

Supra, §VI.A.4, Analysis of Claim [15] (Analysis of [15pre]); APPLE-1003, ¶168.

[17]

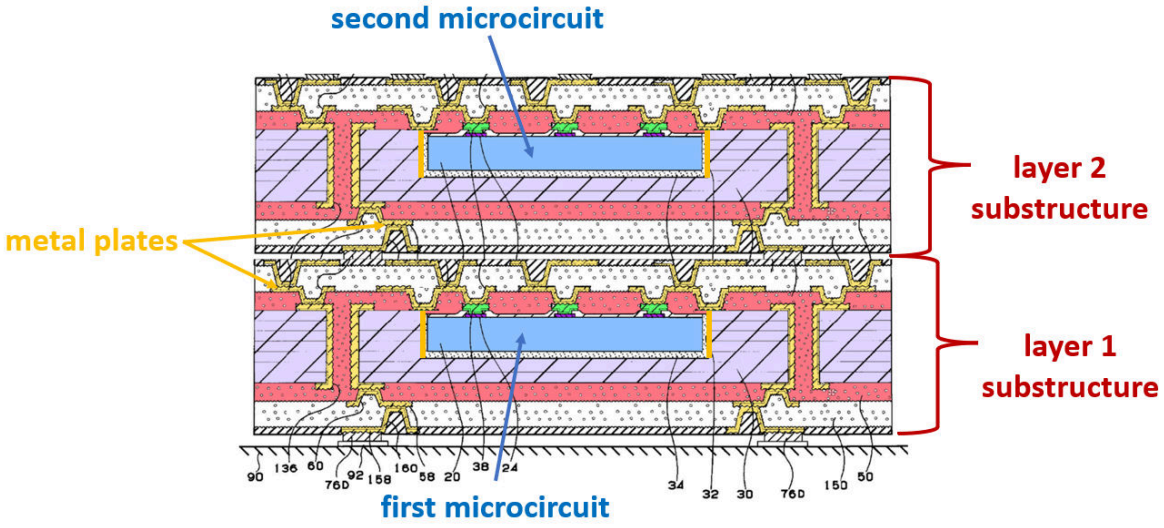
Supra, §§VI.A.4, Analysis of Claim [15] (each of layer 1 and layer 2 substructures, as the ***first*** and ***second circuit board substructure*** respectively, of the exemplary ***multi-layered circuit board*** have the same or similar configuration); Analysis of Claim [16], Analyses of [1a]-1b]; APPLE-1003, ¶169.

[18]

Supra, §§VI.A.4, Analyses of Claims [15], [17], Analysis of [1d]; APPLE-1003, ¶170.

[19]

Supra, §§VI.A.4, Analyses of Claims [1], [13] (Sakamoto's IC chips are microcircuits), and [15] (the embedded IC chip 20 of layer 1 substructure and IC chip 20 of the layer 2 substructure ***are on top of each other*** by virtue of layer 1 and layer 2 substructures being on top of each other, and some of the conductor circuits 58 and 158 of each layer, as the ***metal plates***, are in ***between*** the two IC chips as the ***said first and second microcircuits***); APPLE-1003, ¶171.



APPLE-1003, ¶171 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[20]

Supra, §§VI.A.4, Analyses of Claims [1], [15]; APPLE-1003, ¶¶172-173.

[20pre]

Sakamoto-Eiji satisfies [20pre] even if it is limiting. Element [20pre] recites the ***second circuit board substructure*** to also comprise features demonstrated by the first circuit board substructure with reference to [15a]-[15f]. As discussed in §VI.A.4, Analysis of [15pre], the first and second circuit board substructures (e.g., layer 1 substructure and layer 2 substructure, respectively, in the composite figures therein) have similar substructure configurations that also satisfy the recited features in [20a]-[20f]. *See also*, §§VI.A.4, Analyses of [1a]-[1f]; APPLE-1003, ¶172.

[20a]-[20f]

Supra, §§VI.A.4, Analyses of [1a]-[1f] and [15a]-[15f]; APPLE-1003, ¶173.

[21]

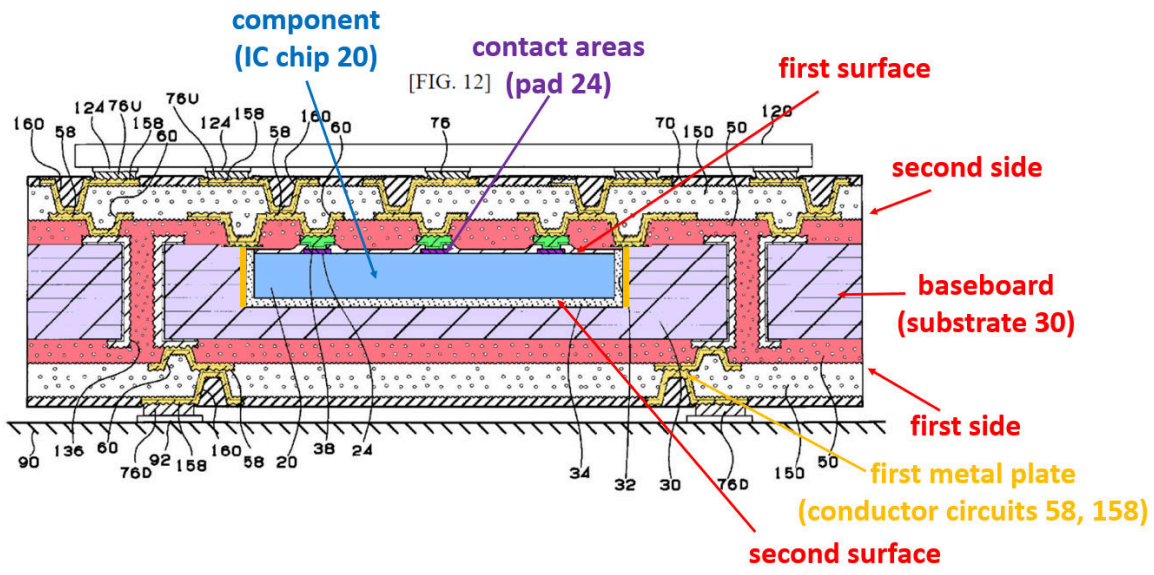
Supra, §§VI.A.4, Analyses of Claims [15], [20]; APPLE-1003, ¶¶174-175.

[21pre]-[21c], [21e]-[21f]

Supra, §§VI.A.4, Analyses of [15pre]-[15c], [15e]-[15f], [1pre]-[1c], [1e]-[1f]; APPLE-1003, ¶174.

[21d]

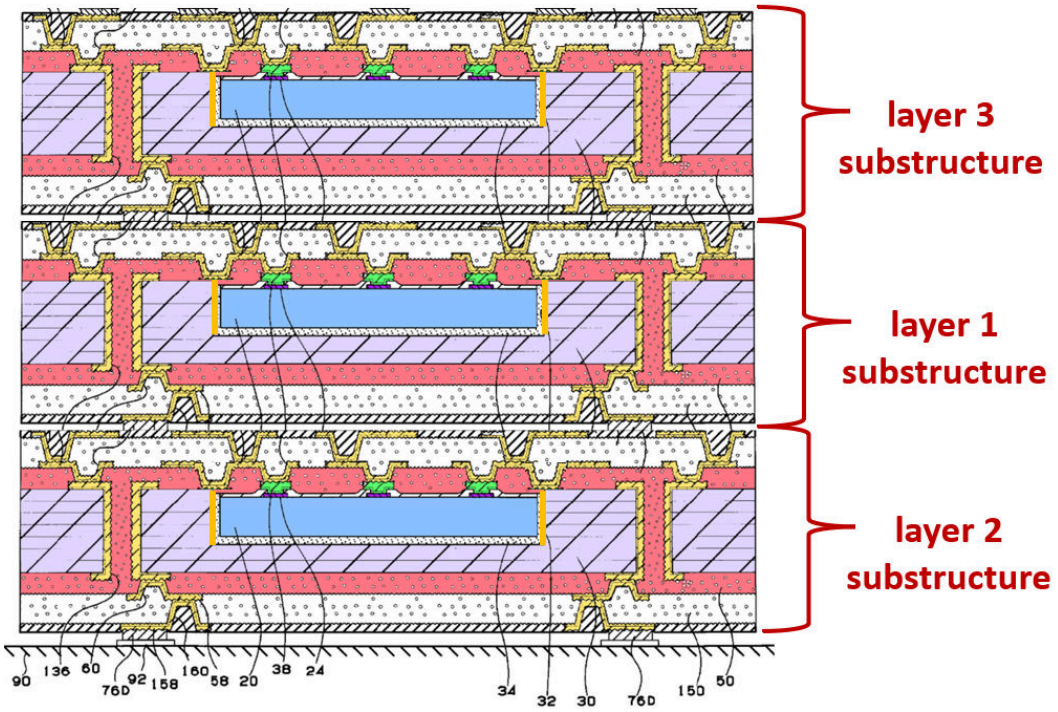
In the Sakamoto-Eiji device, the "IC chip" (***component***) has ***a first surface*** (with ***contact areas*** thereon) ***and a second surface on the opposite sides of the*** chip ***component***, ***the second surface facing towards the*** conductor circuits 58 and 158 on the first side of the insulating material layer (***first metal plate***). *Supra*, §§VI.A.4, Analyses of [15d], [1d]; APPLE-1003, ¶175.



APPLE-1003, ¶175 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[22]

Supra, §VI.A.4, Analysis of Claim [15]; APPLE-1003, ¶176. The Sakamoto-Eiji device includes a multi-layered configuration with three layers of same or similar substructures, with layer 3 substructure on top of layer 1 and layer 2 substructures.



APPLE-1003, ¶176 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

[23]

Supra, §VI.A.4, Analysis of Claim [22] (layer 1 substructure as ***the first circuit board substructure is between*** layer 2 substructure and layer 3 substructure as ***the second and third circuit board substructures***); APPLE-1003, ¶177.

[24]

Supra, §§VI.A.4, Analyses of Claims [22] and [13] (each of the layer 1, 2, and 3 substructures contain an IC chip 20 as ***an embedded microcircuit***); APPLE-1003, ¶178.

[25]-[26]

As discussed previously, (*supra*, §§VI.A.4, Analyses of Claims [2], [15] and [16]), the first and second metal plates are electrically connected[6] to each other. APPLE-1003, ¶179.

[27]

Supra, §VI.A.4, Analysis of Claim [4]; APPLE-1003, ¶180.

[28][7]

[6] And are likewise "electronically connected," as recited in claim 25. APPLE-1003, ¶179.

[7] Claim 28 lacks antecedent basis as it depends on claim 15 which does not recite "metal foil." Even if claim 28 is meant to depend on claim 27 instead,

Supra, §VI.A.4, Analyses of Claims [5], [27]; APPLE-1003, ¶181.

[29]

Supra, §§VI.A.4, Analyses of Claims [11], [15]; APPLE-1003, ¶182.

[30]

Supra, §§VI.A.4, Analyses of Claims [13], [15]; APPLE-1003, ¶183.

[31]

For example, a POSITA would have understood from Sakamoto's description that Sakamoto explicitly teaches, or at least would have prompted a POSITA, to implement the combined device by repeatedly incorporating at least two "electronic components such as IC chips" (***at least two microcircuits***) some of which with different functions, inside the same resin substrate (***the insulating material layer***) for higher functionality, high-speed operation and shortened wiring length, among other benefits of a high-density circuitry. APPLE-1004, [0006] (higher functionality"), [0012], [0069]-[0071]; *supra*, §§VI.A.4, Analyses of Claims [1], [13], [15] and [22]; APPLE-1003, ¶184. Moreover, the conventional structure would have been predictably implemented based on Eiji's further teachings of embedding multiple electronic components within the same insulating substrate, to achieve known benefits noted above. *See e.g.*, APPLE-1012,

---

Sakamoto-Eiji renders it obvious. APPLE-1003, ¶181.

Abstract, [0006] (different types of electronic components can be embedded either in different or the same through-holes or recessed portions), FIG. 1. APPLE-1003, ¶¶185-186

[32]

The Sakamoto-Eiji combination renders obvious Claim [32]. APPLE-1003, ¶¶187-188. Claim 32 recites the same or similar features as recited in Claims 1, 4 and 13 combined, as indicated in the table below. *Supra*, §§VI.A.4, Analyses of Claims [1], [4], [13]; APPLE-1003, ¶187.

[32a]	[1a]
[32b]	[1b]
[32c]	[1c]
[32d]	[1d], [4]
[32e]	[4]
[32f]	[1d], [13]
[32g]	[4]
[32h]	[1e]
[32i]	[1f]

Regarding the preamble [32pre], Sakamoto-Eiji's wiring board having semiconductor components embedded in a base provides ***an electronic module***. Indeed, the resulting structure is similar to that described in the '944 patent itself.

APPLE-1001, Title, Abstract; *supra*, §VI.A.4, Analysis of Claim [1]; APPLE-1003, ¶188.

[33]

Supra, §§VI.A.3 (Sakamoto-Eiji combination), VI.A.4, Analyses of [1b]-[1c], Claims [2], [25]/[26], [32]; APPLE-1003, ¶189.

[34]

Supra, §§VI.A.3 (Sakamoto-Eiji combination), VI.A.4, Analyses of [1b]-[1c], Claims [3], [32]; APPLE-1003, ¶190.

[35]

Supra, §§VI.A.4, Analyses of Claims [5], [32]; APPLE-1003, ¶191.

[36]

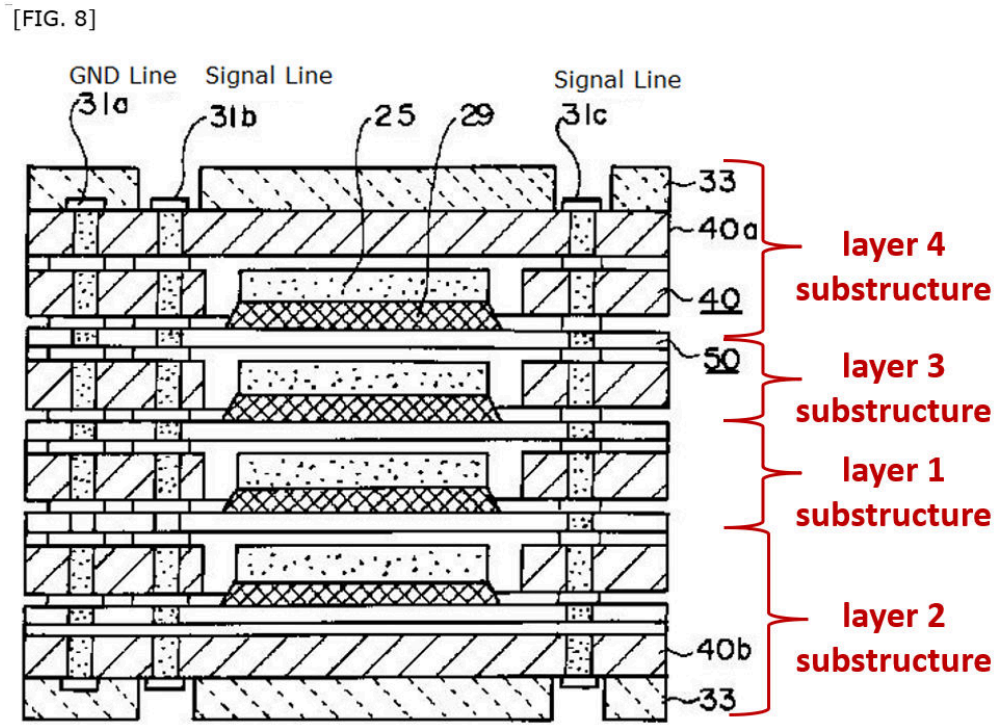
Supra, §§VI.A.4, Analyses of Claim [3], [5], [6] and [32]; APPLE-1003, ¶192.

B. GROUND 1B – Sakamoto-Eiji-Imoto renders obvious Claims 15-31

1. Imoto

Imoto describes a semiconductor device using a "stacked package" with a semiconductor element embedded in a chip cavity portion of each of a plurality of stacked wiring substrates and electrically connected to the wiring. APPLE-1016, Abstract. Imoto thus teaches a stack-up multi-layered structure with each

substructure layer having similar configurations. *Id.*, FIGS. 5-9 (and related descriptions), [0010] ("Any number equal to or greater than two can be stacked."), Cls, 1 ("a plurality of these stacks are stacked and integrated with the semiconductor element mounted on the wiring substrates completely housed inside the chip cavity portion"), 2, 8; APPLE-1003, ¶¶86-90.



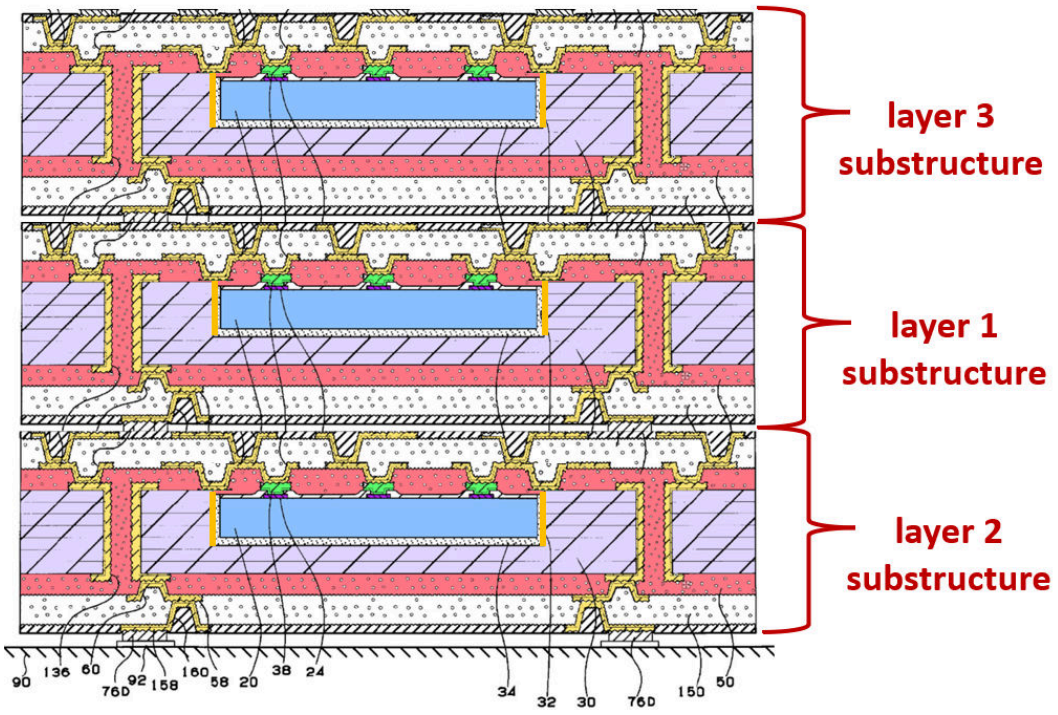
APPLE-1003, ¶88 (APPLE-1016, FIG. 8 (Annotated))

2. Predictable Combination of Sakamoto, Eiji and Imoto

A POSITA would have been motivated to combine the teachings of Sakamoto, Eiji and Imoto to provide a high-density, multi-layered structure with EMI shielding effect. APPLE-1003, ¶193. Each relates to multilayer wiring substrates with built-in semiconductor components. *See e.g.*, APPLE-1004,

Abstract, APPLE-1012, Abstract, FIGS. 1, 4; APPLE-1016, Abstract, [0004]-[0006]. Imoto describes stacking up "[a]ny number equal to or greater than two" of layers of similar configuration, to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1016, [0002] ("high-density mounting."), [0010], Cls.1, 2, 4, 8, FIGS. 5-9 (and related descriptions). APPLE-1003, ¶193.

The resulting device includes a multi-layered structure (e.g. three-layered structure) with each substructure having an IC chip component embedded in a recessed portion of a substrate, each recessed portion having EMI shield on its sidewalls. APPLE-1003, ¶194.



APPLE-1003, ¶194 (Composite Based on APPLE-1004, FIG. 12 (Annotated))

First, a POSITA would have been motivated to stack up any number of layers of similar configuration to form a multi-layered structure in accordance with Imoto, in order to achieve high density mounting. APPLE-1003, ¶¶193-194; *supra*, §VI.A.3 (Sakamoto-Eiji combination); APPLE-1016, [0004]-[0006], [0017], [0020], [0023]-[0025], [0066]. Such a configuration would have enhanced the resulting device by providing enhanced functionality associated with additional layers/components, while providing shielding of respective components in accordance with Eiji, advancing express objectives of the references. *Id.*

Second, a POSITA would have been prompted to combine Imoto with Sakamoto and Eiji because doing so was the application of known techniques (stacking up multiple layers of similar configuration to form a multi-layered structure) to a conventional device (Sakamoto and Eiji's multilayer device) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success in making the proposed modification given that Sakamoto, Eiji and Imoto describe similar multilayer wiring substrates with built-in semiconductor components, and because the modifications involve implementation of well-known technologies demonstrated to be effective by Imoto. APPLE-1003, ¶¶195-196. The references relate to the same field of endeavor and are directed to analogous subject matter that inform construction of multi-layered configurations. *Id.*

3. Application to Challenged Claims

[15]-[31]

As discussed above in §§VI.A.4, Analyses of Claims [15]-[31], Sakamoto-Eiji already renders these claims obvious. The claims are additionally rendered obvious to a POSITA, for at least the same known benefits and reasons, based on the express teaching of Imoto of a multi-layered structure. APPLE-1003, ¶¶197-198. The Sakamoto-Eiji-Imoto combination has a stack-up multi-layered structure, such as shown in the composite figure above, in which each of the layer 1-3 substructures have similar configuration. APPLE-1003, ¶198; *supra*, §VI.B.2 (Sakamoto-Eiji-Imoto combination).

[16]

In addition to Sakamoto's teachings of mechanically and electrically connecting substructures through vias (e.g., vias 60, 160) and through holes (e.g., through-holes 136), as well as mechanism for connecting with external substrates, claim 16 is further rendered obvious in view of Imoto's description of electrically connecting the substructure layers through metal films 33, connecting electrodes 31a, 31b, and 31c inside the vias of the stack. *See e.g.*, APPLE-1016, Abstract, Cls. 1, 2, 4, 8, [0004]-[0006], [0022], FIG. 8; *supra*, §VI.A.4, Analysis of Claim [16]; APPLE-1003, ¶199. In the resulting Sakamoto-Eiji-Imoto device, the circuit

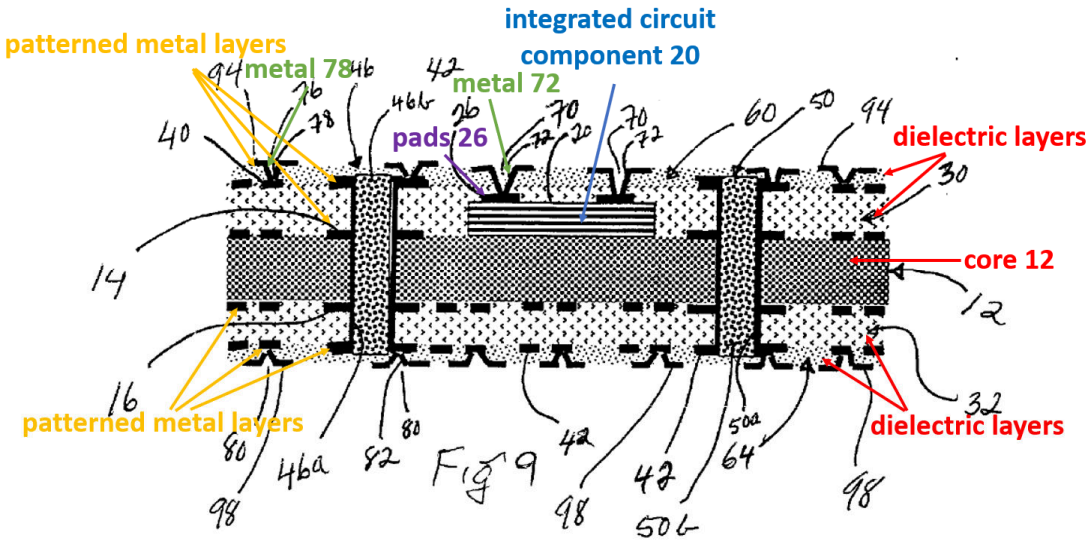
board substructures are electrically connected to each other to form a multi-layered functioning totality. *Id.*

C. GROUND 2A – McCormack and Eiji renders obvious Claims 1-36

1. McCormack

McCormack describes a circuit board having an embedded "integrated electronic component" and a method of producing such structure. APPLE-1005, Title, Abstract, [0009], [0024]-[0026], [0028]-[0029], Cl. 1, FIGS. 9, 11-13; APPLE-1003, ¶75-76. As shown in Figure 9, a circuit component 20 is mounted on an upper substrate surface of core substrate 12, and a dielectric layer (e.g., dielectric layer 30) is on the substrate surface of core 12 and over the integrated circuit component 20. APPLE-1005, Abstract, [0029]-[0030], Cl. 1, FIG. 9; APPLE-1003, ¶77. McCormack's "dielectric layer[] 60," disposed over a patterned metal layer 40 on the dielectric layer 30, is positioned between the component 20 and a "metal layer[] 94" which is disposed over dielectric layer 60 and "patterned." APPLE-1005, [0032]. This dielectric layer 60 contains "polymeric compounds" and is "cur[ed]" at "a subsequent heating step." *Id.*, [0033]; APPLE-1003, ¶78. "A pair of openings 70 is … formed … through dielectric layer 60, … to expose pads 26 [on the integrated circuit component 20]",

and openings 70 are then "metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26." *Id.*, [0032]; APPLE-1003, ¶79.



APPLE-1003, ¶79 (APPLE-1005, FIG. 9 (Annotated))

McCormack discloses an example technique to embed components in its substrate, with "a cavity" provided beforehand in the core substrate 12 where the integrated circuit component is disposed. APPLE-1005, [0009], [0024]- [0025] (indicating FIGS. 12 and 13 as showing an alternative embedding method, of disposing an integrated circuit component in a cavity in the core substrate instead of on a surface of the core, while sharing the same core substrate of FIG. 2 and FIG. 9 and the other common features indicated by the same numeral labels), [0026]-[0029], FIGS. 12, 13; APPLE-1003, ¶80.

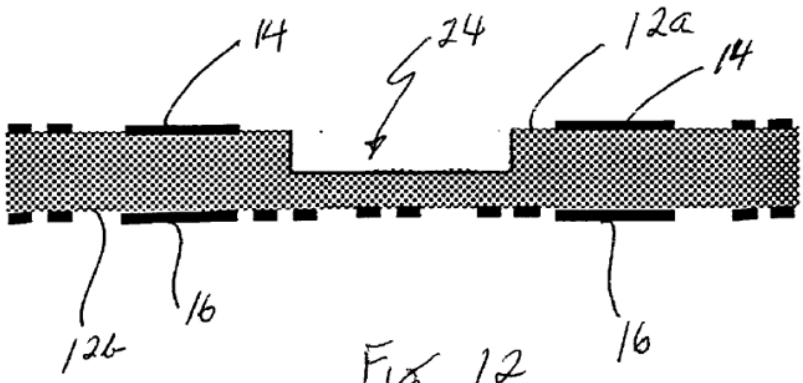


Fig 12

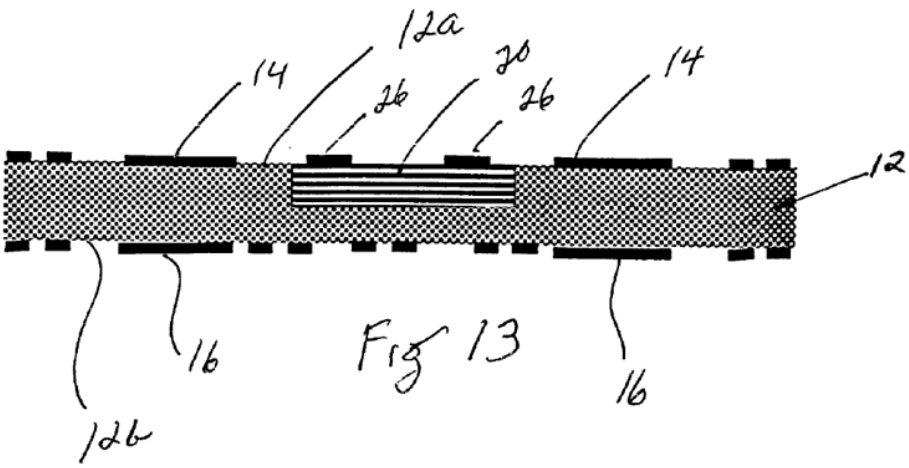


Fig 13

APPLE-1003, ¶80 (APPLE-1005, FIGS. 12, 13)

2. Predictable Combination of McCormack and Eiji

A POSITA would have been motivated to enhance the McCormack multilayer printed circuit board through implementation of Eiji's teachings of a shield layer on the sidewalls of the cavity in which an electronic component is embedded, to make the electronic components built into an insulating substrate "less susceptible to external electromagnetic waves," to "reduce the effects of noise generated by the circuits constituting these electronic components," and to "stabilize the electrical characteristics" of the system, for example. APPLE-1012,

[Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶200.

In the predictable combination, a shielding layer (e.g., Eiji's "shielding layer 10" composed of a copper plating film) that shields electromagnetic waves is formed on an inner surface of a cavity in the core (e.g. McCormack's "cavity 24" in the core 12), before disposing integrated circuit component 20 therein, in accordance with Eiji's teachings. APPLE-1005, [0009], [0024]-[0025], [0028], FIGS. 12-13, Cls. 11, 25-26; *see also id.*, [0007]; APPLE-1012, [Abstract], [0001], [0005]-[0007], [0009], [0011]-[0012], [0017], [0023], [0041]-[0042], Cls. 1, 6, FIG. 1; APPLE-1003, ¶¶201-204.

Further, a POSITA would have been motivated to implement the combination by utilizing a glass fiber epoxy (e.g., for core substrate 12), in accordance with Eiji's suggestions, for enhanced strength. APPLE-1012, [0012], [0038], Abstract; APPLE-1003, ¶205.

Additionally, in the McCormack-Eiji combination, at least one of the metal layers above the component (e.g., metal layers 94, 40) and at least one of the metal layers below the component (e.g., metal layers 16, 42, 98) are electrically connected to each other and to the copper film on the sidewalls of cavity 24 through vias and through-holes (e.g., vias and metal-lined openings already taught by McCormack), and connected to the ground to provide enhanced shielding

effect, in accordance with Eiji's teachings. APPLE-1012, Abstract, [0007]-[0008], [0010]-[0011], [0013]-[0014], [0021], [0023]-[0028], [0034]-[0036], Cls, 3, 4, 5, FIGS. 1, 4; APPLE-1003, ¶206.

Multiple reasons would have prompted a POSITA to utilize an EMI shield feature in accordance with Eiji in a substrate cavity described by McCormack. APPLE-1003, ¶207.

First, a POSITA would have been motivated to combine McCormack and Eiji to provide protection against external electromagnetic wave, reduce influence by noise from circuits composed of various electronic components, and to stabilize electric characteristics of the entire system. APPLE-1003, ¶208.

McCormack already teaches accommodating an electronic component in a core substrate, and mounting multiple electronic components close to each other. APPLE-1005, [0006]-[0009], [0024]-[0025], [0028] ("one or both of the substrate surfaces … may have a cavity generally illustrated as 24 in FIG. 12."), [0034], FIGS. 12-13, Cls. 11, 25-26; *see also id.*, [0007] (incorporating by reference "Dineen"); APPLE-1003, ¶209-210. A POSITA would have recognized that such electronic components can be affected by external electromagnetic waves, or influenced by internal noise, as evidenced by Eiji. APPLE-1012, [Abstract]; APPLE-1003, ¶211. Eiji provides a suitable and known solution for these common problems that can "stabilize the electrical characteristics" of the system. APPLE-

1012, [Abstract], [0001], [0005]-[0012], [0017], [0023], [0041]-[0042], FIG. 1; APPLE-1003, ¶212.

Second, a POSITA would have been motivated to combine Eiji with McCormack to enhance the mechanical strength of McCormack's core substrate 12. APPLE-1003, ¶213. In particular, Eiji describes composite materials of glass fibers with epoxy resin, which a POSITA would have been prompted to utilize in McCormack to enhance robustness of the construction. *Id.*; APPLE-1012, [0012], [0038], Abstract.

Third, a POSITA would have been prompted to combine McCormack and Eiji because doing so was the application of known techniques (forming a shield layer on the inner surface of sidewalls of a through hole or cavity provided in an insulating board for incorporating an electronic component) to a known device (McCormack's multilayer printed circuit board having a hole or cavity 24 in core substrate 12 to accommodate an electronic component such as integrated circuit component 20) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success in making the proposed modifications given that McCormack and Eiji describe similar circuit boards with electronic components embedded inside holes/cavities of an insulation board, and because the modifications would have been implemented largely by adding a metal layer on the

sidewalls of the hole/cavity, in order to create interference protection around the electronic components, and use of glass-fiber impregnated epoxy resin for an insulating substrate—options Eiji already demonstrates to be successful. APPLE-1003, ¶¶214-216. Moreover, for similar reasons, McCormack and Eiji describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing addressed here. *Id.*

3. Application to Challenged Claims

[1pre]

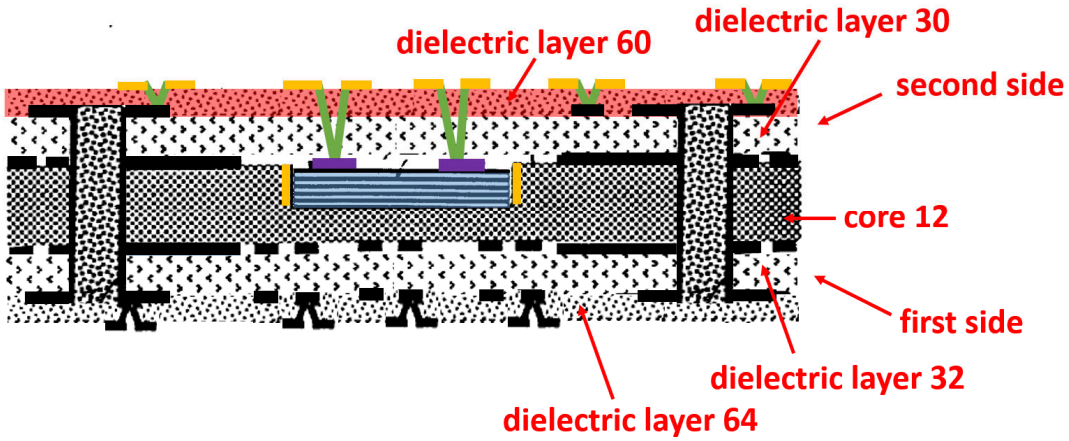
If the preamble is deemed limiting, McCormack-Eiji teaches [1pre]. APPLE-1003, ¶218. For example, McCormack discloses "a circuit apparatus and a method for embedding electronic components within multi-layer substrates, particularly printed **circuit boards**." *E.g.*, APPLE-1005, [0002], [0009]-[0012], Cls. 1, 17, 35; APPLE-1003, ¶218.

Accordingly, through McCormack's disclosure of a "circuit board," the combination provides [1pre].

[1a]

McCormack-Eiji discloses Element [1a]. APPLE-1003, ¶¶219-220. For example, the combination of McCormack-Eiji's "circuit board substrate" or "core

substrate" 12 and one or more dielectric layers (such as "dielectric layer 30" and "dielectric layer 60") having integrated electronic components embedded therein collectively provide ***an insulating material layer having a first*** (lower) ***side and a second*** (upper) ***side***. *E.g.*, APPLE-1005, Abstract, [0009]-[0011], [0026], [0029], [0032]-[0033] ("Suitable dielectric material for the core 12 … and/or dielectric layers 30, 32, 60 and 64 include B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicons, well known to those skilled in the art. …"), Cls. 1, FIG. 9, 17, 35; APPLE-1003, ¶219. Additionally, McCormack provides Element [1a] in a second manner in which "dielectric layer 32," or "dielectric layers 32 and 64," together with "circuit board substrate" 12 and "dielectric layer 30" and "dielectric layer 60," collectively provide ***an insulating material layer*** as claimed. APPLE-1003, ¶220.

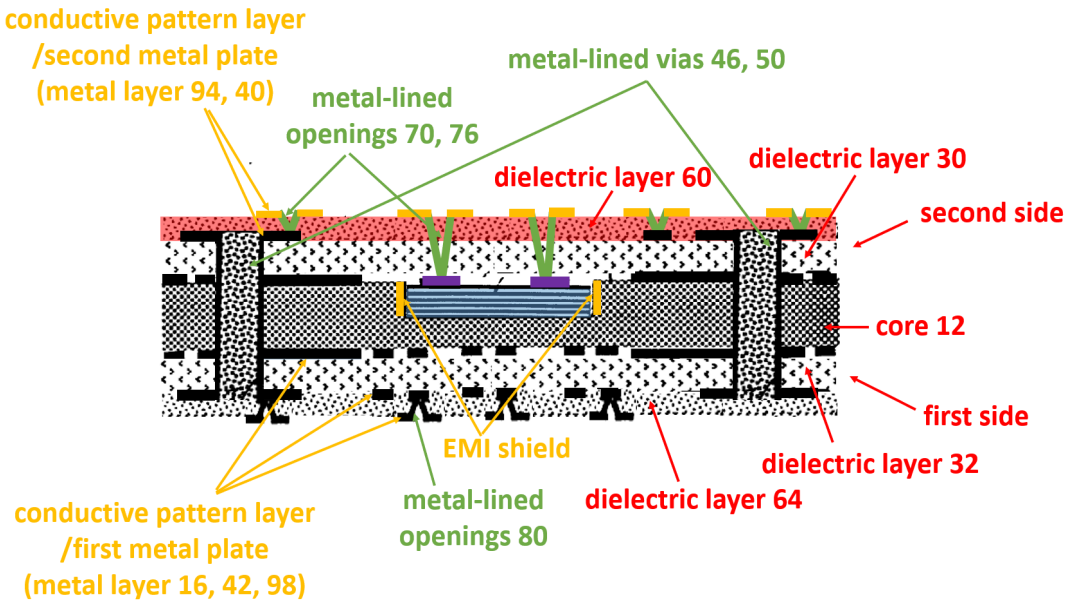


APPLE-1003, ¶220 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[1b]-[1c]

McCormack-Eiji discloses Elements [1b] and [1c]. APPLE-1003, ¶¶221-228. For example, McCormack describes "metal layers" 94 and 40 on the upper (second) side of the circuit board (***at least one second conductive pattern layer on the second side of the insulating material layer***) and "patterned metal layer 16" on the lower (first) side of the circuit board (***at least one first conductive pattern layer on the first side of the insulating material layer***). APPLE-1005, [0026] ("Metal layers 14 and 16 are optional, and may be any suitable conductive metal, such as copper."), [0027] ("metal layers … may be appropriately patterned with any suitable photoresist to respectively, selectively expose substrate surfaces… Patterning of the metal layers … may be accomplished by etching to develop the desired patterned metal profile. … such as by [a list of etching techniques]"), [0030]-[0032], FIGS, 7-9; *see also id.*, [0021]; APPLE-1003, ¶221.

In the second manner that McCormack-Eiji provides the claimed insulating material layer, as discussed above (Analysis of [1a]), circuit board substrate 12 and dielectric layers 30, 60, and 32 (collectively or further including dielectric layer 64) likewise provide an insulating material layer, in which the patterned metal layer 42 or the patterned metal layer 98 on the lower (first) side of the circuit board provides the ***at least one first conductive pattern layer***. APPLE-1003, ¶222.



APPLE-1003, ¶222 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

To be clear, a POSITA would have understood and found obvious that McCormack-Eiji's metal layer 16 (e.g., or 42 and 98) serves as ***the first conductive pattern layer defining a first metal plate***, and metal layer 94 or 40 serves as ***the second conductive pattern layer defining a second metal plate***. APPLE-1003, ¶223; *supra*, §VI.C.2 (McCormack-Eiji combination). As discussed above, in the combined system, at least one of the metal layers 94 and 40 and at least one of the metal layers 16, 42, 98 are electrically connected to each other (e.g., through metal-lined vias 46, 50 and openings 70, 78, 80) and to the EMI shield on the sidewalls of cavity 24, and are grounded to provide enhanced shielding effect, in accordance with Eiji's teachings. *Supra*, §VI.C.2 (McCormack-Eiji combination); APPLE-1001, 8:44-9:41 (describing the metal plates of FIG. 4D are connected

with the metal foil surrounding the microcircuits laterally and are earthed, "thus provides the microcircuit with excellent protection against electromagnetic interference"); *infra*, §VI.C.3, Analysis of Claim [5]; APPLE-1003, ¶¶224-225. Further, McCormack describes that "metal layers … may be any suitable conductive material, such as copper. … disposed … by any suitable means, such as by lamination, plating, sputtering or chemical vapor deposition (CVD)." APPLE-1005, [0026]; FIG. 9; APPLE-1003, ¶226.

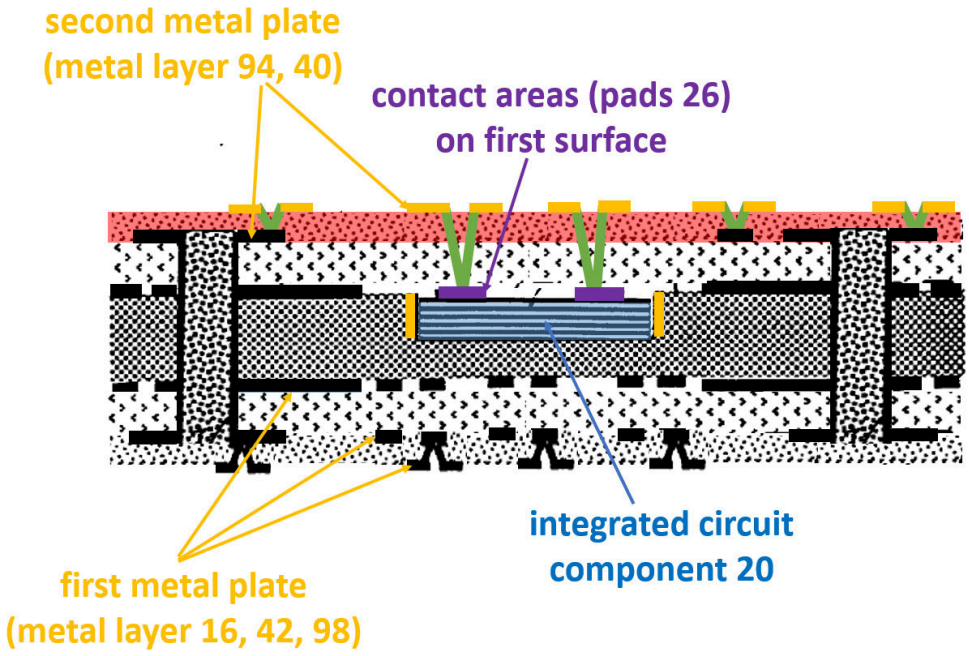
To be clear, McCormack-Eiji's conductive metal layers implemented in accordance with Eiji have a substantial thickness more than "several 10 μm thick," compared with the '944 patent's metal coating of "e.g., c. 5 μm." APPLE-1012, [0017], [0021]-[0022], [0025]; APPLE-1001, FIGS. 1F, 1J, 4C, 4D, 4:40-63, 5:47-6:4, 8:44-9:41; APPLE-1003, ¶227.

Notably, McCormack and Eiji combined provide at least as much detail as the '944 patent, which tersely recites a "metal plate" (also referred to as "metal foil" and "film" in the specification) without construction details, and separately describes materials like that described by McCormack, such as "a layer of copper" made of "an RCC (Resin Coated Copper) foil" and "metal foil", for forming its metal plates. APPLE-1001, 5:47-56, 8:44-9:41, 4:40-59; FIGS. 1J & 1F; APPLE-1003, ¶228; *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994) ("[T]hat appellant did not provide the type of detail in his specification that he now argues is

necessary in prior art references supports the Board's finding that one skilled in the art would have known how to implement the features of the references."); *see also* §VI.A.4 (Sakamoto-Eiji ground), Analysis of Element [1b]-[1c].

[1d]

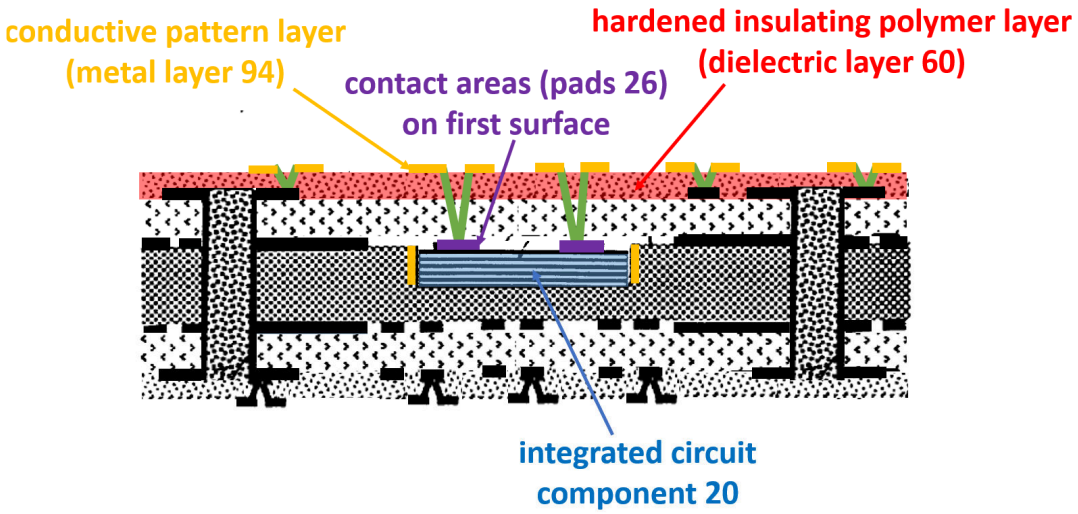
McCormack-Eiji renders obvious Element [1d]. APPLE-1003, ¶229. For example, the combination's "integrated electronic component"/ "integrated circuit component 20" embedded in the dielectric materials of the circuit board provides ***a component inside the insulating material layer***. *E.g.*, APPLE-1005, Abstract, [0009]-[0011], [0021], [0028]-[0033], FIG. 9; APPLE-1003, ¶229. McCormack further discloses that integrated circuit component 20 has "conductor pads 26" (***contact areas***) on its active surface (***first surface***). APPLE-1005, [0021], [0029], [0032]. Integrated circuit component 20 is between a second metal plate (e.g., metal layer 94 (and 40) and first metal plate (e.g., metal layer 16 (and metal layer 42, 98), each implemented as described above in the McCormack-Eiji combination), having its ***first surface facing towards*** metal layer 94 (and 40) (***second metal plate***). APPLE-1003, ¶229.



APPLE-1003, ¶229 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[1e]

McCormack-Eiji discloses Element [1e]. APPLE-1003, ¶230-232. For example, the combination's dielectric layer 60 provides ***a hardened insulating polymer layer***. The dielectric layers contain "polymeric compounds" and are "cur[ed]" at a "subsequent heating step" with "exposure to heat and pressure" such that it is ***hardened***. APPLE-1005, [0032]-[0033]; APPLE-1003, ¶230-231. The composite figure below shows dielectric layer 60 located ***between the first surface*** (having conductor pads 26 thereon) of the integrated circuit component 20 and metal layer 94 (***at least one conductive pattern of said at least one second conductive pattern layer***). *See also*, §VI.C.3, Analysis of [1a].



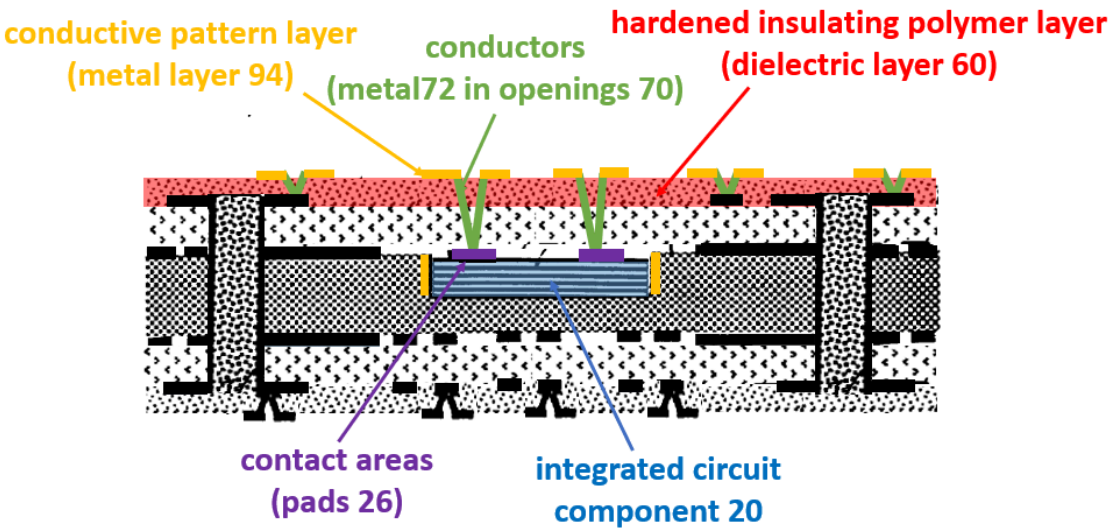
APPLE-1003, ¶231 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

As discussed above, the ***insulating material layer*** of claim 1 (e.g., dielectric layers 30 and 60 together with circuit board substrate 12 and one or more other layers) encompasses a ***baseboard*** and ***hardened insulating polymer layer*** (e.g., dielectric layer 60). APPLE-1003, ¶232; *supra*, Analysis of [1a]; *infra*, Analysis of Claim 8.

[1f]

McCormack-Eiji discloses Element [1f]. APPLE-1003, ¶233. For example, McCormack describes "openings 70" formed through dielectric layer 60 (***hardened insulating polymer layer***) and dielectric layer 30, to "expose pads 26" (***contact areas***), "[o]penings 70 are then metal-lined with a suitable metal (e.g., copper) 72 into ***electrical contacts*** with pads 26." APPLE-1005, [0032] (metal lining accomplished "by the combination of e-less and electrolytic plating"); *see also*,

Abstract ("metal-lined opening"), [0009]-[0011], [0021], Cls. 1 ("a metal lining in said opening and coupled to the first integrated electronic component"), 12 ("at least one first pad in contact with said metal lining in said opening"), 17, 35, FIG. 9 (showing metal 72 connected with metal layer 94). "Openings 70" thus provide ***contact openings***, and "metal lining 72" provide ***conductors in the contact openings for forming electrical contacts between*** conductor pads 26 (***contact areas***) of the integrated circuit component 20 and metal layer 94 (***at least one second conductive pattern layer or layers***). APPLE-1003, ¶233.



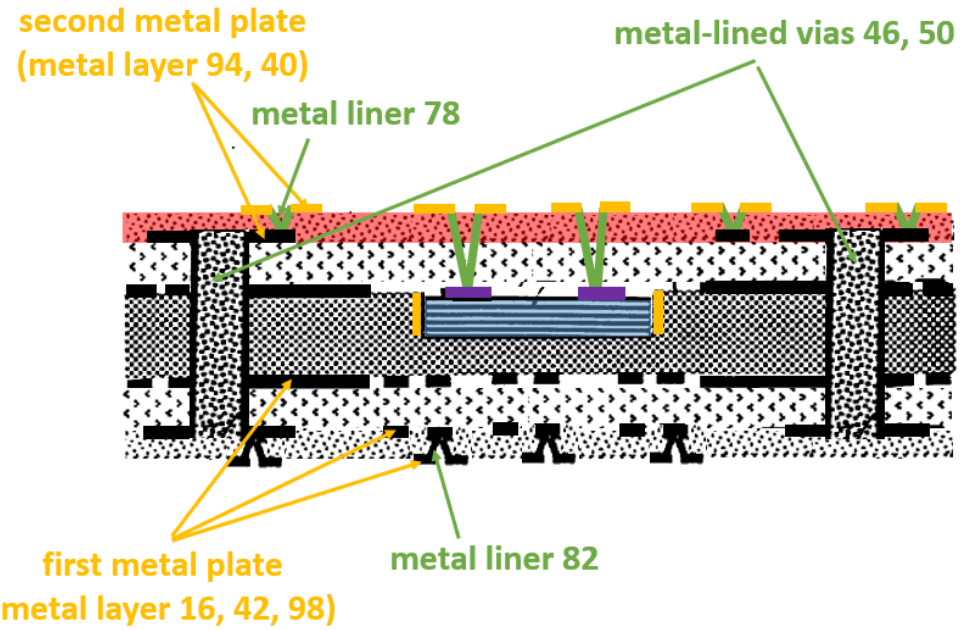
APPLE-1003, ¶233 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[2]

For example, McCormack discloses conductive feed-throughs including "metal-lined vias 46 and 50 formed by drilling openings through the entire FIG. 5

circuit board assembly," that provide electrical connection between the first and second metal plates (e.g., patterned metal layer 94 or 40 and patterned metal layer 16, 42, or 98). APPLE-1005, [0031]. For example, the "openings pass[] through metal layers 40 and 42, through dielectric layers 30 and 32, through residual metal layers remaining from patterned metal layers 14 and 16, and through the core 12." *Id.*, [0031]; *see also id.*, [0009], [0018]-[0019], [0020]-[0022], [0026], FIGS. 6-10. McCormack further explains that "residual metal layers 94 and 98 are respectively coupled to residual metal layers 40 and 42, respectively, by and through metal liners 78 and 82" in openings 76 and 80, respectively. *Id.*, [0032]; *see also* Abstract, [0009]-[0011], FIG. 9. APPLE-1003, ¶¶234-235.

Thus, metal layer 94 (or 40) (conductive pattern layer defining the ***second metal plate***) and metal layer 16 (or metal layer 42 or 98) (conductive pattern layer defining the ***first metal plate***) ***are electrically connected to each other***, through a conductive path of metal layer 94-metal liner 78-metal layer 40-vias 46 and 50-metal layer 42-metal liner 82-metal layer 98. *See also* APPLE-1005, [0031]; APPLE-1003, ¶236.



APPLE-1003, ¶236 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[3][8]

Supra, §§VI.A.2 (Eiji overview), VI.C.2 (McCormack-Eiji combination), VI.C.3, Analyses of [1b]-[1c] and Claim [2], VI.A.4 (Sakamoto-Eiji ground), Analysis of Claim [3] (obvious to earth a ground connection); APPLE-1003, ¶¶237-238 (citing Cole, Jr., incorporated by reference in McCormack); APPLE-1029, 7:14-26; APPLE-1005, [0004], [0006].

[4]

[8] Claim 3 recites an "earth connection of the circuit board," which amounts to a non-limiting statement of use. Even if considered to be limiting, it is disclosed as set forth here.

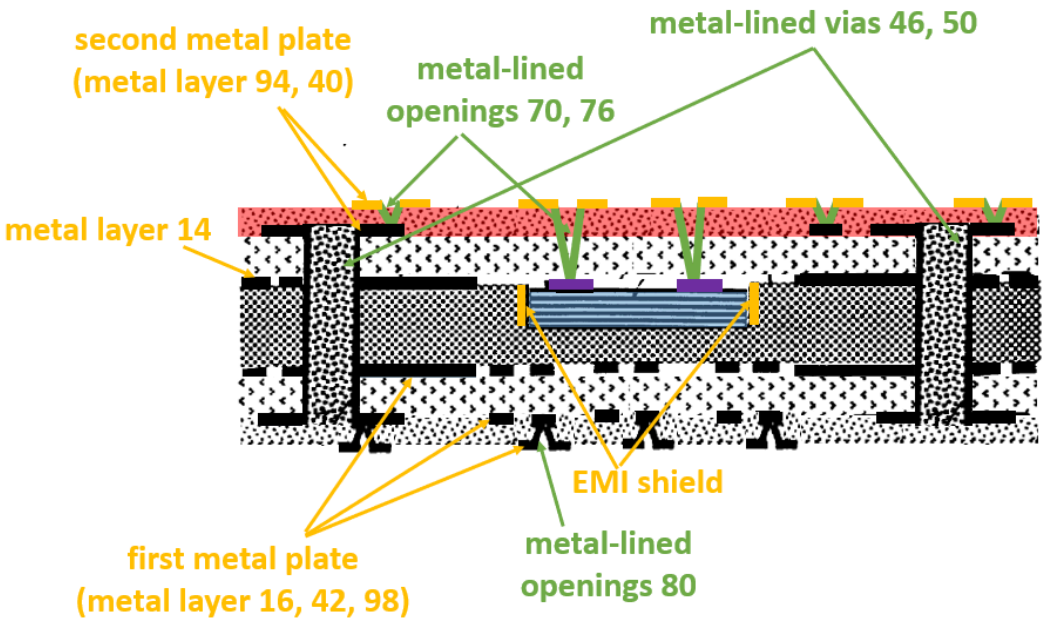
As discussed in §VI.C.2 (McCormack-Eiji combination), the combined system has integrated circuit component 20 (***component***) located in a cavity 24 in an insulating board (***in a hole in the insulating material layer***), and a shield layer "composed of a copper plating film that shields electromagnetic waves is formed on an inner surface of" cavity 24 (***metal foil covering the sidewalls of the hole***). *Supra*, §VI.C.2; APPLE-1003, ¶¶239-242. *See also supra*, §VI.A.4, Analysis of Claim [4] (Sakamoto-Eiji ground); APPLE-1005, [0031]-[0032]; *supra*, §VI.C.2.

McCormack further teaches "a suitable adhesive" and "[a]dditional underfill, glop-top, or other adhesive/sealant materials" for securing the integrated circuit components "to a desired location," and various "filler material" for filling metal-lined openings and vias in its insulating layers. APPLE-1005, [0029] -[0033]; APPLE-1003, ¶243. A POSITA would have been prompted to use such adhesive, underfill, glop-top, or other adhesive/sealant materials, and/or other filler material such as epoxy resins, to fill any gap in cavity 24 between the EMI shield and the component to enhance securement of the component in a desirable location in the cavity (***a filler material in the hole between the metal foil and the component***). *E.g.*, APPLE-1005, [0006] (desire to secure embedded electronic components "in a precise position and orientation" in the holes); APPLE-1003, ¶243. A POSITA would have been further motivated to do so based on Eiji's teaching of a "resin 16, which is primarily epoxy resin," to secure each component at "a predetermined

location in the through-hole." APPLE-1012, [0019]; *see also*, [0007], [0010], [0031], Cls. 2, 7, FIGS. 1, 3; APPLE-1003, ¶¶244-245.

[5]

As discussed above in §VI.A.4, Analysis of Claim [5] (Sakamoto-Eiji ground), Eiji teaches a shield layer connected to the conductive wiring layers on both the lower and upper sides of its wiring board used as ground layers or power layers. A POSITA would have been prompted and found obvious to implement this connection for McCormack-Eiji's shield layer (***metal foil***) with its metal layers (e.g., metal layers 94, 40, 16, 42, 98) (conductive pattern layers defining ***the first and second metal plates***) on both sides of its circuit board, in accordance with Eiji, such as through metal layer 14, and additional vias in the insulating dielectric layers if necessary, using the same technique for forming the existing vias and openings (like existing metal-lined openings 70, 76 and 80, also "metal-lined vias" like vias 46 and 50), to achieve the same benefits of more accurate and reliable operation of the electronic components and more reliable EMI shielding as taught by Eiji. APPLE-1003, ¶¶246-248; *supra*, §§VI.C.2 (McCormack-Eiji combination); VI.C.3, Analyses of Claims [2], [4]. APPLE-1005, [0026], [0032], FIGS, 9, 12.



APPLE-1003, ¶248 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

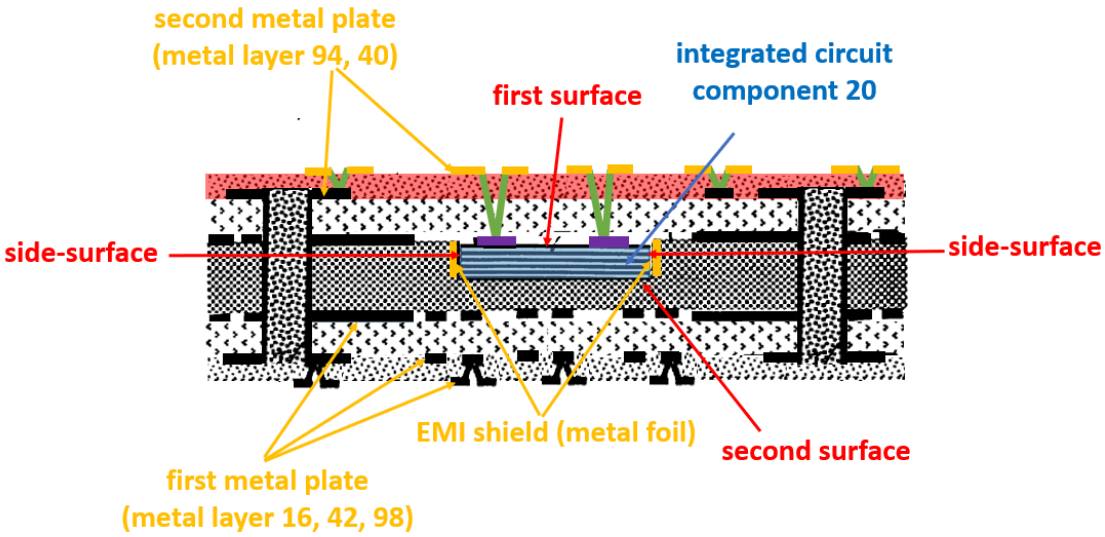
[6]

Supra, §§VI.C.3, Analyses of Claims [3], [5]. As discussed above, Eiji discloses that shielding layer 10 covering the sidewalls of the hole for incorporating electronic components is connected to a "ground layer," which "enabl[es] the electronic components to operate more precisely and reliably while shielding them from any noise that may occur." APPLE-1012, FIG. 1, [0007]; APPLE-1003, ¶¶249. A POSITA would have been prompted and found obvious to implement this ground connection (***earth connection***) for the shield layer (***metal foil***) of the McCormack-Eiji system, in accordance with Eiji, such as through additional vias in the insulating layers, to achieve the same benefits of more

accurate and reliable operation of the electronic components and more reliable EMI shielding. APPLE-1003, ¶250.

[7]

Supra, §§VI.C.2 (McCormack-Eiji combination), VI.C.3, Analyses of [1b]-[1c] and Claim [5] (in the combined system, the metal layers such as metal layers 16 and 94, as ***the first and second metal plates***, ***and the metal foil*** covering the sidewalls of cavity 24 ***form an electromagnetic interference shield around*** integrated circuit component 20 (***the component***), ***such that the side-surfaces of*** integrated circuit component 20 (***the component***) ***face towards the metal foil, the first surface of*** integrated circuit component 20 (***the component***) ***face towards*** the metal layer on the upper side of the circuit board (***the second metal plate***), ***and the second surface*** opposite to the first surface ***of*** integrated circuit component 20 (***the component***) ***face towards*** the metal layer on the lower side of the circuit board (***the first metal plate***)); APPLE-1003, ¶251.



APPLE-1003, ¶251 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[8]

As discussed in §§VI.C.3, Analyses of [1a] and [1e], the combined system's "circuit board substrate" 12 along with "dielectric layer 30" and "dielectric layer 60" (or further including additional dielectric layers 32, 64) is an ***insulating material layer***, in which "dielectric layer 60" is a ***hardened insulating polymer layer***, and core substrate 12 (or further in combination with the dielectric layers30, 32, 64) provides a ***baseboard*** as claimed. APPLE-1003, ¶252.

To be clear, each of these dielectric layers, including the core 12, are made of materials typical of a circuit board baseboard, such as epoxy. *Compare* APPLE-1005, [0033] *with* APPLE-1001, 45-55 (the '944 patent describing its baseboard as "epoxy board," an "organic board," or "an inorganic board"); APPLE-1003, ¶252.

To the extent McCormack's description regarding the suitable materials for its dielectric layers and core were not considered to provide the claimed baseboard, McCormack-Eiji renders it obvious. APPLE-1003, ¶253. In the combination, "a glass-epoxy resin composite material" is used for the core substrate, resulting in a baseboard construction just like the '944 patent's example. APPLE-1012, [0012], [0038], Abstract; APPLE-1001, 3:45-55 ("glass-fibre reinforced epoxy board…"). §VI.C.2 (McCormack-Eiji Combination); APPLE-1003, ¶¶253-255.

[9]

Supra §§VI.C.2 (McCormack-Eiji combination), VI.C.3, Analysis of Claim [8] (the McCormack-Eiji combination's core substrate having electronic components embedded therein is made of composite materials of glass fibers with epoxy resin). APPLE-1003, ¶256.

[10]

Supra, §VI.C.3, Analysis of Claim [4] (the shield layer "composed of a copper plating film" covering the sidewalls of cavity 24 is a ***conductive material***); APPLE-1003, ¶257.

[11]

McCormack-Eiji discloses Claim [11], even if the recited process of the product-by-process element is limiting. *Supra*, §§III.A. (FN 1); VI.C.3, Analysis

of [1f] (metal lining 72 made of copper in the contact openings 70 is accomplished "by the combination of e-less and electrolytic plating"); APPLE-1003, ¶¶258-259.

[12]

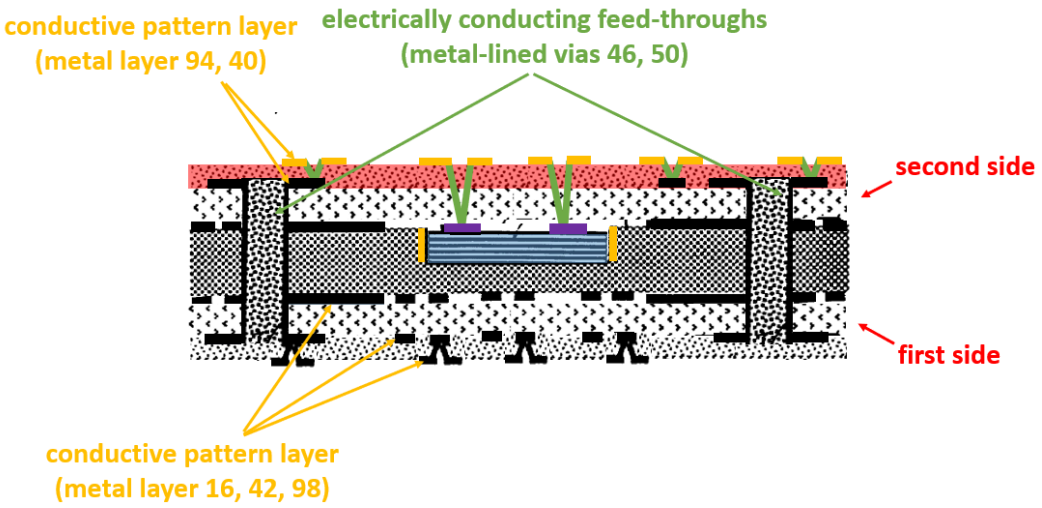
Supra, §§VI.C.3, Analyses of [1a] & [1e] (dielectric layer 60 contains "epoxy resins"); APPLE-1003, ¶260.

[13]

Supra, §VI.C.3, Analysis of [1d]. McCormack-Eiji's "integrated electronic component" or "integrated circuit component 20" is a ***microcircuit***. APPLE-1003, ¶261.

[14]

Supra, §VI.C.3, Analysis of Claim [2] ("metal-lined vias 46 and 50" are each ***an electrically conducting feed-through*** between metal layers, the recited ***conductive pattern layers***, ***on the both sides of the insulating material layer*** of the circuit board); APPLE-1003, ¶262.



APPLE-1003, ¶262 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

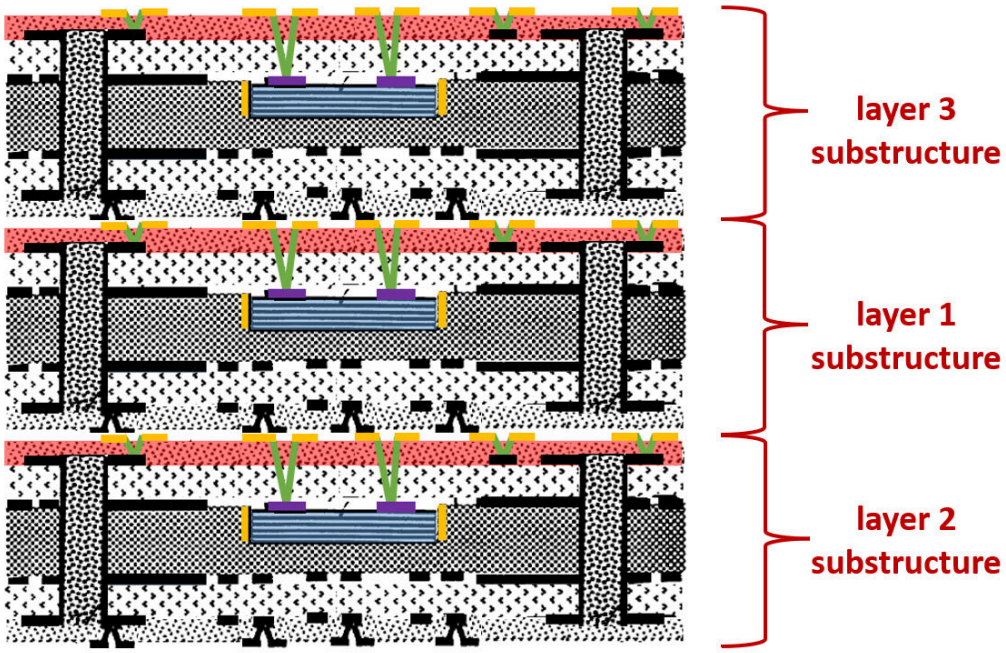
[15]

APPLE-1003, ¶¶263-269. Claim 15 recites identical limitations for its "at least the first circuit board substructure" of a "multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other" as those recited in Claim 1 for a circuit board. *Compare* APPLE-1001, Cl. 1 *with id.*, Cl. 15. Thus, these same limitations of Claim 15 are rendered obvious by McCormack-Eiji for at least the same reasons provided in §§VI.C.3, Analyses of [1pre]-[1f].

[15pre]

Again, regarding the preamble of Claim 15 relating to the recited "multi-layered circuit board comprising a first circuit board substructure and second circuit board substructure on top of each other," it amounts to routine duplication

of parts. APPLE-1003, ¶264 (citing APPLE-1002, 107-110). Additionally, to the extent it is limiting, McCormack-Eiji renders it obvious. APPLE-1003, ¶265. For example, McCormack describes "dielectric build-up" of multiple layers of its printed circuit board assembly such as in FIG. 9, "by means well known to those skilled in the art (e.g., post plating for stacked via build-up structures)." APPLE-1005, [0032]; APPLE-1003, ¶265. Below composite figure illustrates this ***multi-layered circuit board*** configuration with three layers (layers 1-3) of the same or similar substructures (e.g., layer 1 and layer 2 substructures corresponding to the claimed ***a first circuit board substructure and second circuit board substructure***), each substructure comprising each recited element of Claim 15. APPLE-1003, ¶265; §§VI.C.3, Analyses of [1pre]-[1f].



APPLE-1003, ¶265 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

Indeed, stacking multiple layers of circuit-board substructures on top of each other and mounting a plurality of electronic components in the same as well as different such layers to achieve high-density, improved performance, and short-distance wiring was common practice and well known in the field. APPLE-1003, ¶¶266-268.

[15a]-[15f]

Supra, §VI.C.3, Analyses of [1a]-[1f]; APPLE-1003, ¶269.

[16]

In the multi-layered structure illustrated above, layer 1 substructure (***first circuit board substructure***) and layer 2 substructure (***second circuit board substructure***) ***are electrically connected to each other to form a multi-layered functioning totality***, through the metal layers on the surfaces of and within each substructure layer such as metal layers 94, 98, 40, 42, 14, 16, and 12c, vias with metal liners such as metal liners 78 and 82 of openings 76 and 80, and conducting-through vias such as vias 18, 46 and 50 of each substructure layer. *Supra*, §§VI.C.3, Analyses of Claims [15] and [2]; APPLE-1003, ¶270.

[17]

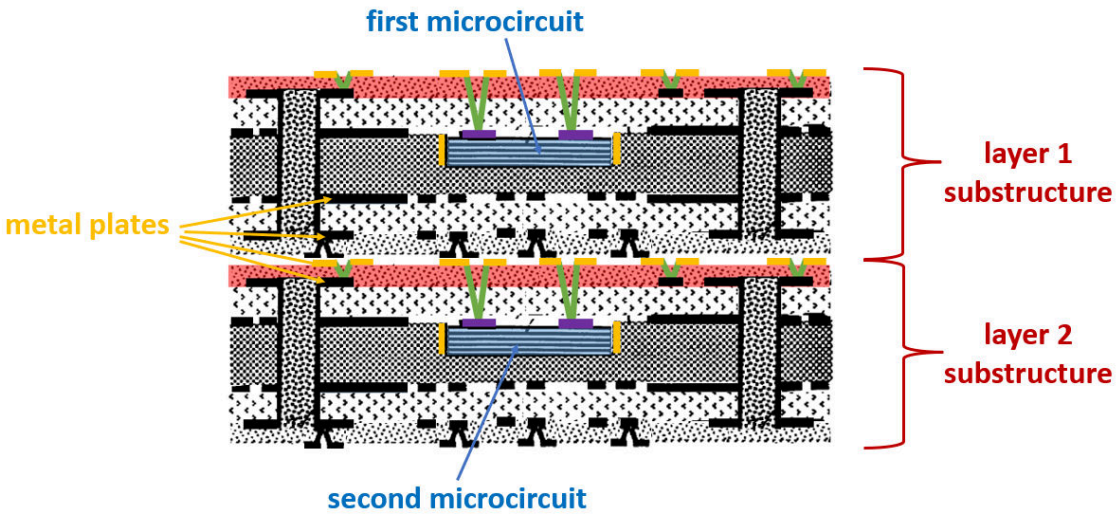
Supra, §§VI.C.3, Analyses of Claims [15] (each of layer 1 and layer 2 substructures, as the ***first*** and ***second circuit board substructure*** respectively, of the exemplary ***multi-layered circuit board*** have the same or similar configuration), [16], and Elements [1a]-1b]; APPLE-1003, ¶271.

[18]

Supra, §§VI.C.3, Analyses of Claims [15], [17], Analysis of [1d]; APPLE-1003, ¶272.

[19]

Supra, §§VI.C.3, Analyses of Claims [1], [13] (integrated circuit components are ***microcircuits***), and [15]. In the exemplary multi-layered circuit board (below), the ***first and second microcircuits*** of the layer 1 and layer 2 substructures ***are on top of each other*** by virtue of layer 1 and layer 2 substructures being on top of each other. Moreover, ***at least one of the first and second metal plates*** defined by conductive pattern layers, such as metal layers 16, 42 and 98 of layer 1 substructure, and metal layers 94 and 40 of layer 2 substructure, ***is located between said first and second microcircuits***. APPLE-1003, ¶273; *supra*, §VI.C.3, Analysis of Claim [15].



APPLE-1003, ¶273 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[20]

Supra, §§VI.C.3, Analyses of Claims [1], [15]; APPLE-1003, ¶¶274-275.

[20pre]

Element [20pre] recites the ***second circuit board substructure*** to also comprise the same or similar features as recited in [15a]-[15f] for at least the first circuit board substructure. As discussed in §VI.C.3, Analysis of [15pre], the first and second circuit board substructures (indicated as layer 1 substructure and layer 2 substructure, respectively, in the composite figures therein) have similar substructure configurations that also satisfy the recited features in [20a]-[20f]. *See also*, §§VI.C.3, Analyses of [1a]-[1f]; APPLE-1003, ¶274.

[20a]-[20f]

Supra, §§VI.C.3, Analyses of [1a]-[1f] and [15a]-[15f]; APPLE-1003, ¶275.

[21]

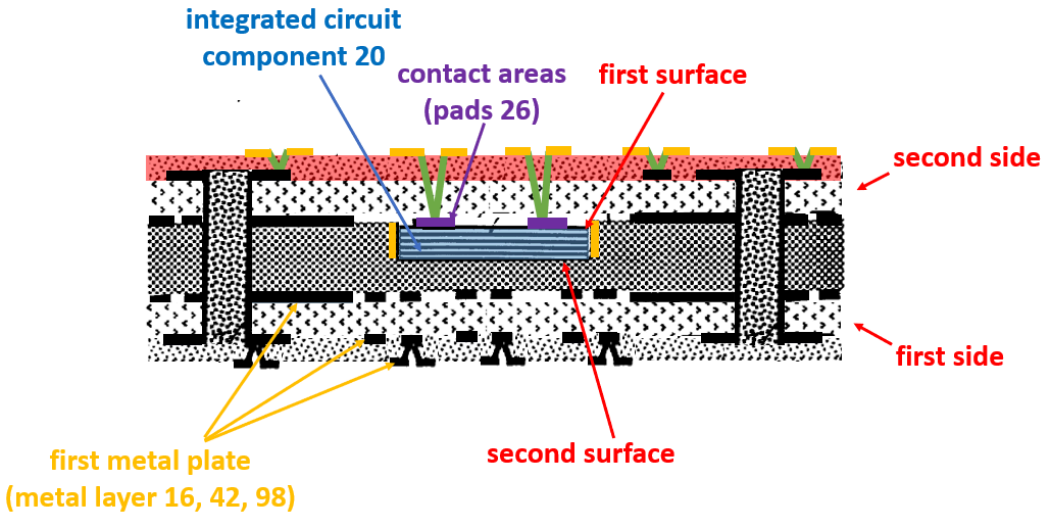
Supra, §§VI.C.3, Analyses of Claims [1], [15], [20]; APPLE-1003, ¶¶276-277.

[21pre]-[21c], [21e]-[21f]

Supra, §§VI.C.3, Analyses of [15pre]-[15c], [15e]-[15f], [1pre]-[1c], [1e]-[1f]; APPLE-1003, ¶276.

[21d]

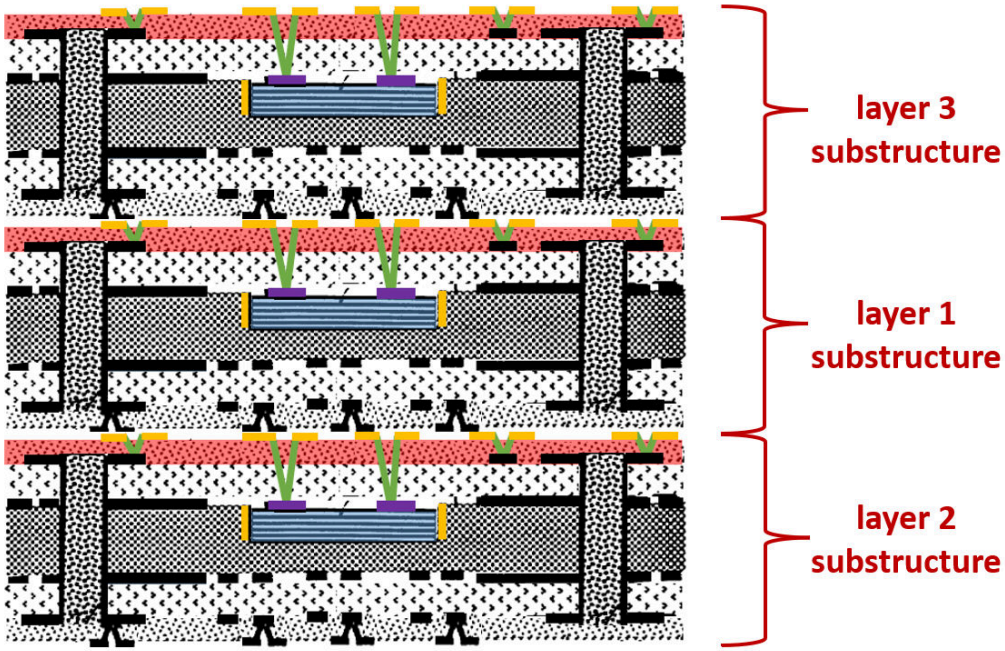
The composite figure below shows that "integrated circuit component 20" has ***a first surface*** (with ***contact areas*** thereon) ***and a second surface on the opposite sides of the*** IC chip ***component***, ***the second surface facing towards the*** metal layers 16, 42 and 98 on the first side of the insulating material layer (***first metal plate***). *Supra*, §§VI.C.3, Analyses of [15d], [1d]; APPLE-1003, ¶277.



APPLE-1003, ¶277 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[22]

Supra, §VI.C.3, Analysis of Claim [15]; APPLE-1003, ¶278. Below composite figure illustrates a multi-layered configuration with three layers of same or similar substructures, with layer 3 substructure on top of layer 1 and layer 2 substructures (***a third circuit board substructure on top of the first and second circuit board substructures***).



APPLE-1003, ¶278 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

[23]

Supra, §VI.C.3, Analysis of Claim [22] (layer 1 substructure as ***the first circuit board substructure is between*** layer 2 and layer 3 substructures as ***the second and third circuit board substructures***); APPLE-1003, ¶279.

[24]

Supra, §§VI.C.3, Analyses of Claims [22] and [13]; APPLE-1003, ¶280.

[25]-[26]

As discussed previously (*supra*, §§VI.C.3, Analyses of Claims [2], [15] and [16]), the first and second metal plates are electrically connected[9] to each other. APPLE-1003, ¶281.

[27]

Supra, §VI.C.3, Analysis of Claim [4]; APPLE-1003, ¶282.

[28][10]

[9] And are likewise "electronically connected," as recited in claim 25. APPLE-1003, ¶281.

[10] Claim 28 lacks antecedent basis as it depends on claim 15 which does not recite "metal foil." Even if claim 28 is meant to depend on claim 27 instead, McCormack-Eiji renders it obvious. APPLE-1003, ¶283.

Supra, §§VI.C.3, Analyses of Claims [5], [27]; APPLE-1003, ¶283.

[29]

Supra, §§VI.C.3, Analyses of Claims [11], [15]; APPLE-1003, ¶284.

[30]

Supra, §§VI.C.3, Analyses of Claims [13], [15]; APPLE-1003, ¶285.

[31]

APPLE-1003, ¶¶286-291. As discussed above in §§VI.C.3, Analyses of Claims [1], [13], [15] and [22], McCormack describes a stacked multilayer structure with one or more integrated circuit components (***microcircuits***) in the same and/or different substructures. APPLE-1005, [0029]-[0030], [0032]. Indeed, McCormack, expressly indicates the "circuit board having **at least one** integrated electronic component," thereby disclosing at least two microcircuits inside the insulating material layer. *Id.*, *see also* [0010]-[0011], [0030] ("**one or more** of the integrated circuit components 20 have been suitable [*sic*] disposed where desired"), Cls. 1, 11 ("a **second** integrated electronic component"), 17, 35, FIG. 11; APPLE-1003, ¶¶286-287; *see also* APPLE-1005, [0007] (incorporating by reference "Dineen" teaching "mounting **a plurality of electronic components**").

Even if McCormack did not expressly describe at least two integrated circuit components inside its dielectric layers (including core 12) of the circuit board

assembly, a POSITA would have found this conventional configuration to be obvious based on McCormack's suggestions. APPLE-1003, ¶¶288-289. As discussed above, McCormack describes use of multiple components. A POSITA would have recognized the predictable benefits of positioning two components inside the insulating material layer to achieve the functionality of two components and/or to maintain a compact overall profile while doing so. Moreover, a POSITA would have had a reasonable expectation of success in doing so, especially in view of McCormack's express suggestion for multiple components, and the known implementation of multiple components in an insulating material layer. APPLE-1003, ¶290. Consistently, Eiji also describes embedding multiple electronic components in the same substrate. *See e.g.*, APPLE-1012, Abstract, [0006], FIG. 1. APPLE-1003, ¶291.

[32]

Supra, §VI.A.4, Analysis of Claim [32] (Sakamoto-Eiji ground) (element correspondence between Claim 32 and Claims 1, 4 and 13; §§VI.C.3, Analyses of Claims [1], [4], [13]; APPLE-1003, ¶292.

Regarding preamble [32 Pre] reciting an electronic module instead of a circuit board, McCormack-Eiji's "electronic circuit board" having semiconductor components embedded in a base is a similar device as described in the '944 patent,

and thus is ***an electronic module***. *E.g.*, APPLE-1005, [0012]; APPLE-1001, Title, Abstract; *supra*, §VI.C.3, Analysis of Claim [1]; APPLE-1003, ¶293.

[33]

Supra, §§VI.C.2 (McCormack-Eiji combination), VI.C.3, Analyses of [1b]-[1c], Claims [2], [25]/[26] and [32]; APPLE-1003, ¶294.

[34]

Supra, §§VI.C.2 (McCormack-Eiji combination), VI.C.3, Analyses of [1b]-[1c], Claims [3] and [32]; APPLE-1003, ¶295.

[35]

Supra, §§VI.C.3, Analysis of Claims [5], [32]; APPLE-1003, ¶296.

[36]

Supra, §§VI.C.3, Analyses of Claims [3], [5], [6] and [32]; APPLE-1003, ¶297.

D. GROUND 2B – McCormack, Eiji and Sugaya render obvious Claims 15-31

1. Sugaya

Sugaya describes a "circuit component built-in module" with embedded circuit components such as semiconductor chips. APPLE-1007, Title, Abstract, FIG. 1A, [0013], [0015], [0020]-[0021], [0086], [0092]. Sugaya further describes

stacking up multiple layers of similar modules to form a multi-layered structure, where "any number of layers [of similar configuration] can be formed depending on the design." APPLE-1007, [0225]; *see also*, [0004], [0217], [0351], [0354], FIGS. 9A (reproduced below showing a three-layered structure), 9B; APPLE-1003, ¶¶91-93.

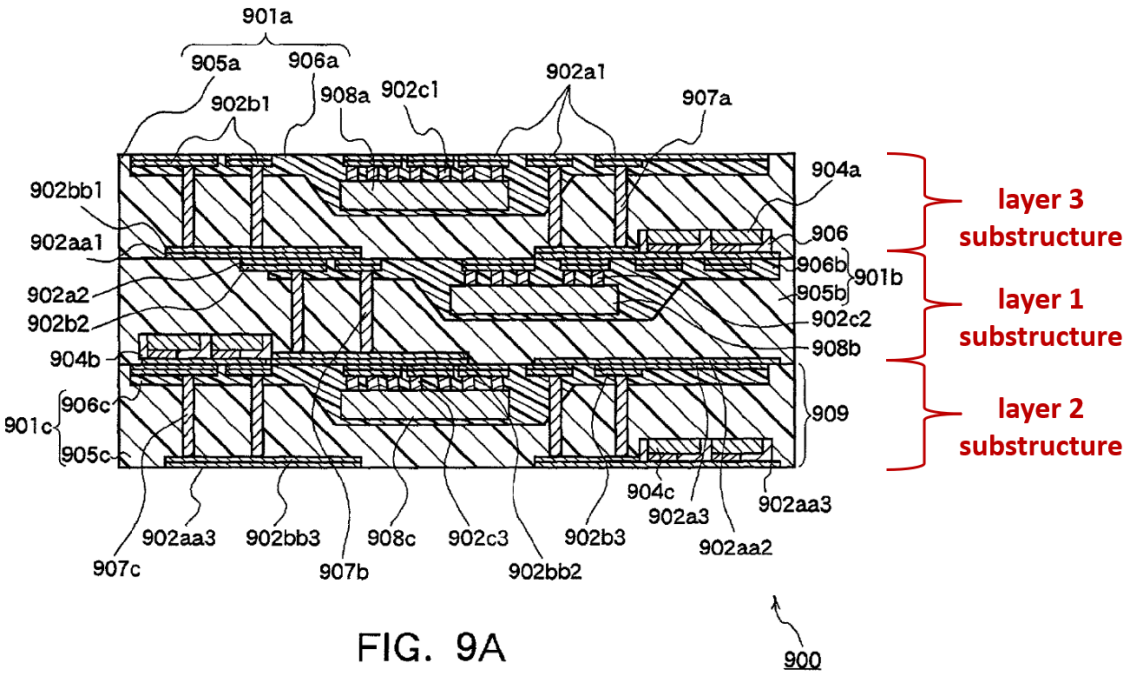


FIG. 9A

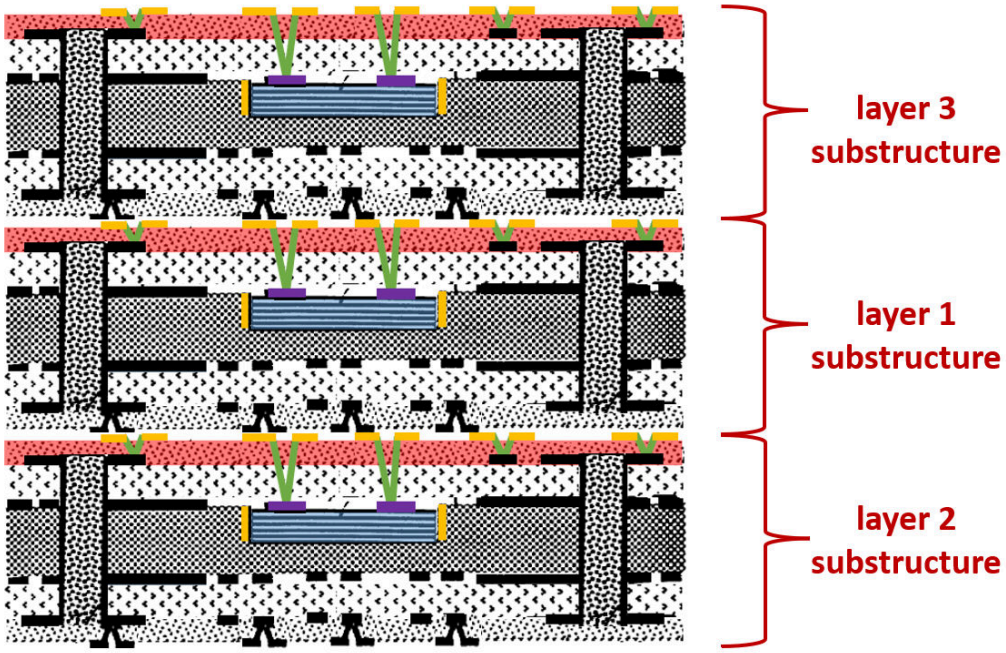
APPLE-1003, ¶92 (APPLE-1007, FIG. 9A (Annotated))

2. Predictable Combination of McCormack, Eiji and Sugaya

A POSITA would have been motivated to combine the teachings of McCormack, Eiji and Sugaya to provide a high-density, multi-layered structure with EMI shielding effect. APPLE-1003, ¶298. Each relates to a component built-in module where circuit components are provided inside an insulating substrate,

relating to the same field of endeavor and directed to analogous subject matter. *See e.g.*, APPLE-1005, Abstract, [0002], [0029]-[0030]; APPLE-1012, [0023], FIGS. 1, 4; APPLE-1007, Title, Abstract. Sugaya expressly describes stacking up any number of layers of similar configuration to form a multi-layered structure with the substructure layers electrically connected to each other, for high density mounting. APPLE-1007, Abstract, [0004] ("In recent years, with the demand for high performance and miniaturization of electronic equipment, high density, high performance and short-distance wiring of a circuit component have been desired increasingly."), [0225], [0217], [0351], [0354], FIGS. 9A, 9B; APPLE-1003, ¶298.

A POSITA would have been motivated to utilize an EMI shield feature in accordance with Eiji in a cavity in the core substrate described by McCormack, and to stack up any number of layers of similar configuration, depending on the design, to form a multi-layered structure in accordance with Sugaya's express suggestions, to achieve high density mounting and EMI shielding. APPLE-1003, ¶299; *supra*, §VI.C.2 (McCormack-Eiji combination). Below composite figure illustrates a three-layered structure with each substructure having an integrated circuit component embedded in a cavity of a core substrate, each cavity having EMI shield on its sidewalls. APPLE-1003, ¶299.



APPLE-1003, ¶299 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

A POSITA would have had a reasonable expectation of success in making the proposed modifications given that McCormack, Eiji and Sugaya describe similar circuit component built-in modules, and because the modifications involve only implementation of well-known technologies. APPLE-1003, ¶300.

3. Application to Challenged Claims

[15]-[31]

As discussed above in §§VI.C.3, Analyses of Claims [15]-[31], McCormack in view of Eiji already renders these claims obvious. For at least the same reasons, and with the additional express teaching of Sugaya of a multi-layered structure, the McCormack-Eiji-Sugaya combination has a stack-up multi-layered structure, such

as shown in the composite figure above, each of the layer 1-3 substructures having similar configuration. APPLE-1003, ¶¶301-302; *supra*, §VI.D.2 (McCormack-Eiji-Sugaya combination).

[16]

Additionally for Claim [16], other than McCormack's teachings of mechanically and electrically connecting substructures through metal layers, metal lined openings, and metal lined vias as conductive feed-throughs of each substructure layer, Sugaya similarly describes electrically connecting substructure layers of a multi-layered structure to each other through "inner via conductors" and wiring patterns of each layer, for high density mounting. *See e.g.*, APPLE-1007, Abstract, [0016], [0019], [0047], [0217], [0227], FIGS. 9A-B; *supra*, §VI.C.3, Analysis of [16]; APPLE-1003, ¶303.

VII. The *Advanced Bionics* Test Favors Institution—§325(D)

None of Sakamoto, McCormack, Eiji, or Imoto were applied in a rejection during prosecution, and each is relied upon for disclosure of subject matter that is materially different than applied or set forth within references cited during prosecution. The Petition thus does not involve the same or substantially the same art or arguments previously presented, ending the *Advanced Bionics* inquiry in

favor of institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

While a family member of Sugaya was cited on the face of the '944 patent, none of the other references were applied in a substantive office action, which demonstrate the unpatentability of the prior art.

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314

Essentially all of the *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written Decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors. Moreover, a Motion to Transfer to the Northern District of California remains pending. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while litigation remains in early stages. As noted above, Motions to

Transfer remains pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds, outweighing any inefficiencies.

IX. FEES

Apple authorizes charge of fees to Deposit Account No. 06-1050.

X. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '944 patent. The '944 patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.* 1-24-cv-00129 (WDTX), filed February 5, 2024; *ImberaTek LLC v. Samsung Electronics Co., Ltd. et al* 2-22-cv-00233 (EDTX), filed June 24, 2022; and *Samsung Electronics Co., Ltd. et al v. ImberaTek LLC* IPR2023-00044 (PTAB), filed October 12, 2022.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
W. Karl Renner, Reg. No. 41,265 Fish & Richardson P.C. 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR50095-0193IP1@fr.com	Craig Deutsch, Reg. No. 69,264 Charlene Thrower, Reg. No. 79,289 Fish & Richardson P.C. 60 South Sixth Street Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR50095-0193IP1@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0193IP1@fr.com.

Respectfully submitted,

Dated: February 6, 2025

/W. Karl Renner/

W. Karl Renner, Reg. No. 41,265
Craig Deutsch, Reg. No. 69,264
Charlene Thrower, Reg. No. 79,289
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2025-00578)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,799 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 6, 2025

/W. Karl Renner/

W. Karl Renner, Reg. No. 41,265
Craig Deutsch, Reg. No. 69,264
Charlene Thrower, Reg. No. 79,289
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2025-00578)

Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

BIRCH STEWART KOLASCH & BIRCH, LLP
2600 Park Tower Drive
Suite 600
Vienna, VA 22180-7371
(703) 205-8000

/Crena Pacheco/
Crena Pacheco
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
pacheco@fr.com