

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv233	DATE FILED 6/24/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, et al
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,609,527	10/27/2009	ImberaTek LLC
2 8,222,723	7/17/2012	ImberaTek LLC
3 8,368,201	2/5/2013	ImberaTek LLC
4 7,989,944	8/2/2011	ImberaTek LLC
5 8,238,113	8/7/2012	ImberaTek LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 10/31/2022	INCLUDED BY ☒ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 11,071,207	7/20/2021	ImberaTek LLC
2 7,732,909	6/8/2010	ImberaTek LLC
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, SAMSUNG ELECTRONICS AMERICA, Inc., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,107,324	8/15/2015	ImberaTek LLC
2		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5967120

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	7732909	
Patent Number:	7989944	
Patent Number:	7609527	
Patent Number:	8817485	
Patent Number:	8034658	
Patent Number:	8222723	
Patent Number:	8487194	
Patent Number:	9232658	
Patent Number:	8351214	
Patent Number:	8455994	
Patent Number:	8368201	
Patent Number:	9622354	
Patent Number:	9691724	
Patent Number:	9107324	
Patent Number:	10231335	
Patent Number:	10085345	
Patent Number:	10010019	
Patent Number:	10085347	
Patent Number:	9324647	
Patent Number:	9883587	

Property Type	Number
Patent Number:	9674948
Patent Number:	9820375
Patent Number:	10470346
Application Number:	14580257
Application Number:	15355096
Application Number:	16104979

CORRESPONDENCE DATA

Fax Number: (703)643-9789

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4349062975

Email: yoon@capitoliplaw.com

Correspondent Name: YEASUN YOON

Address Line 1: 20319 KIAWAH ISLAND DR

Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER:	PA01GETOIMBERATEK02
NAME OF SUBMITTER:	YEASUN YOON
SIGNATURE:	/yoon/
DATE SIGNED:	02/18/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7

source=imbera assignment#page1.tif

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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this “**Assignment**”) is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company (“**Assignor**”), in favor of **ImberaTek, LLC**, a Delaware limited liability company (“**Assignee**”).

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the “**Patent Sale Agreement**”); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the “**Patents**”).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

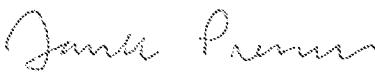
Name: PATRICK K. PATNODE

Title: AUTHORIZED SIGNATORY

Acknowledgement:

State of New York)
County of Schenectady)

ss.


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8024403
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRPI0307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A I, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A I, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1 , US10010019B2, US2018352689A I	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15'937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	07/17/2012	8222723	0365-0652PUS3	6266
2292	7590	06/27/2012		
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747				

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 186 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Risto Tuominen, Espoo, FINLAND;
Petteri Palm, Helsinki, FINLAND;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 03/19/2012
BIRCH STEWART KOLASCH & BIRCH, LLP
PO BOX 747
FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3	6266

TITLE OF INVENTION: ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/19/2012
EXAMINER		ART UNIT	CLASS-SUBCLASS			
WILLIAMS, ALEXANDER O		2826	257-686000			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Birch, Stewart, Kolasch
 2 & Birch, LLP
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

IMBERA ELECTRONICS OY

ESPOO, FINLAND

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2448 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Typed or printed name

Michael K. Mutter

Date

Registration No.

JUN 18 2012

29680

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:	12699628			
Filing Date:	03-Feb-2010			
Title of Invention:	ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER			
First Named Inventor/Applicant Name:	Risto Tuominen			
Filer:	Michael Keith Mutter/Letitia Alexander			
Attorney Docket Number:	0365-0652PUS3			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	13041710
Application Number:	12699628
International Application Number:	
Confirmation Number:	6266
Title of Invention:	ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	2292
Filer:	Michael Keith Mutter/Letitia Alexander
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0652PUS3
Receipt Date:	18-JUN-2012
Filing Date:	03-FEB-2010
Time Stamp:	16:40:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$2040
RAM confirmation Number	3746
Deposit Account	022448
Authorized User	MUTTER,MICHAEL K.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20120618ISSUEFEE.PDF	106393	no	1
			f978c5810b72fe3a8d920c7d3bb343c17954efdb		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	32166	no	2
			fa2685436eb533916259df443eb0b7ab3070b861		

Warnings:

Information:

Total Files Size (in bytes): 138559

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

2292 7590 03/19/2012
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 03/19/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3	6266

TITLE OF INVENTION: ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/19/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 03/19/2012
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3	6266

TITLE OF INVENTION: ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1740	\$300	\$0	\$2040	06/19/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
WILLIAMS, ALEXANDER O	2826	257-686000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3	6266

2292 7590 03/19/2012
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 03/19/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 186 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 186 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/699,628	TUOMINEN ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Amendment filed 3/2/2012.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 9, 11, 12, 14 and 16-20; renumbered 1, 2, 3, 4, and 5-9 respectively.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in **ABANDONMENT** of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date ____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____.
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/Alexander O Williams/ Primary Examiner, Art Unit 2826	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"12699628"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:12
L2	6	"10550023"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:18
L3	2	"7663215".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:21
L4	70	Tuominen with Risto	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:48
L5	44	Palm with Petteri	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:49
L6	87	Imbera with Electronics	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:50
L7	76	4 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:50
L8	52	6 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:51
L9	8412	257/686	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L10	378	257/e23.085	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L11	142	257/e23.178	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L12	78	257/e25.011	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L13	80	257/e23.105	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L14	413	257/e21.705	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L15	7277	257/777	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:52
L16	7181	257/723	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:53
L17	9305	257/778	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:53
L18	4622	257/692	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:53
L19	6495	257/773	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:53
L20	8061	257/774	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/03/11 19:53

3/ 11/ 2012 8:02:14 PM

C:\Users\awilliams\Documents\EAST\Workspaces\12326269.wsp

Issue Classification 	Application/Control No. 12699628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner A O WILLIAMS	Art Unit 2826

ORIGINAL						INTERNATIONAL CLASSIFICATION									
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED				
257		686				H	0	1	L	23 / 02 (2006.01.01)					
CROSS REFERENCE(S)						H	0	1	K	3 / 10 (2006.01.01)					
						H	0	1	L	23 / 48 (2006.01.01)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					H	0	5	K	3 / 34 (2006.01.01)					
257	E23.085	E23.178	E25.011	E23.105	E21.705	H	0	1	L	21 / 00 (2006.01.01)					
257	777	723	778	692	773										
257	774														

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	6	17												
	2	7	18												
	3	8	19												
	4	9	20												
	5														
	6														
	7														
	8														
1	9														
	10														
2	11														
3	12														
	13														
4	14														
	15														
5	16														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 9	
/A O WILLIAMS/ Primary Examiner. Art Unit 2826 (Primary Examiner) _____ (Date) _____		3/11/12 O.G. Print Claim(s)	O.G. Print Figure 11

Search Notes 	Application/Control No. 12699628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner A O WILLIAMS	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	686,e23.085,e23.178,e25.011,e23.105,e21.705,777,723,778,692,773,774	3/11/12	AW

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	3/11/12	AW
checked 10/550023	10/28/11	AW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	686,e23.085,e23.178,e25.011,e21.705,777,723,778,692,773,774	3/11/12	AW

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BIB DATA SHEET

CONFIRMATION NO. 6266

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/699,628	02/03/2010	257	2826	0365-0652PUS3		
APPLICANTS Risto Tuominen, Espoo, FINLAND; Petteri Palm, Helsinki, FINLAND; ** CONTINUING DATA ***** This application is a CIP of 10/550,023 09/23/2005 PAT 7,663,215 which is a 371 of PCT/FI2004/000195 03/31/2004 ** FOREIGN APPLICATIONS ***** FINLAND 20030493 04/01/2003 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/18/2010						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/A O WILLIAMS/</u> Examiner's Signature		☒ Met after Allowance AW Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 8	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747 UNITED STATES						
TITLE ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN LAYER						
FILING FEE RECEIVED 1220	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

<i>Index of Claims</i> 	Application/Control No. 12699628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner A O WILLIAMS	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	10/28/2011	03/11/2012												
	1	✓	-												
	2	✓	-												
	3	✓	-												
	4	✓	-												
	5	✓	-												
	6	✓	-												
	7	✓	-												
	8	✓	-												
1	9	O	=												
	10	✓	-												
2	11	O	=												
3	12	O	=												
	13	✓	-												
4	14	O	=												
	15	✓	-												
5	16	✓	=												
6	17	✓	=												
7	18	✓	=												
8	19	✓	=												
9	20	✓	=												

Docket No.: 0365-0652PUS3
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Risto TUOMINEN et al.

Application No.: 12/699,628

Confirmation No.: 6266

Filed: February 03, 2010

Art Unit: 2826

For: AN ELECTRONIC MODULE HAVING A
CONDUCTIVE PATTERN LAYER (As
Amended)

Examiner: Alexander O. Williams

AMENDMENT UNDER 37 C.F.R. § 1.111

MS AMENDMENT

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Commissioner:

INTRODUCTORY COMMENTS

In reply to the Office Action dated November 03, 2011, the following amendments and remarks are respectfully submitted in connection with the above-identified application.

Amendments to the Specification begin on page 2.

Amendments to the Abstract of the Disclosure begin on page 3.

Amendments to the Claims begin on page 4.

Remarks begin on page 7.

AMENDMENTS TO THE SPECIFICATION

Please amend the title of the invention as follows:

AN ELECTRONIC MODULE HAVING A CONDUCTIVE PATTERN LAYER

Before Paragraph [0001] of the Specification, please insert the following heading:

Background

Before Paragraph [0010] of the Specification, please insert the following heading:

Summary

Before Paragraph [0029] of the Specification, please insert the following heading:

Brief Description of the Drawings

Before Paragraph [0035] of the Specification, please insert the following heading:

Detailed Description

AMENDMENTS TO THE ABSTRACT OF THE DISCLOSURE

Please replace the Abstract of the Disclosure with the following Abstract:

An electronic module including a conductive-pattern layer; an insulating-material layer supporting the conductive-pattern layer; and at least one component inside the insulating-material layer is disclosed. The component includes a first surface and contact zones on the first surface. The electronic module further includes a first hardened adhesive layer on the first surface of the component; a second hardened adhesive layer in contact with the conductive-pattern layer and the first hardened adhesive layer; holes in the first and second hardened adhesive layer at the locations of the contact zones; and conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer.

AMENDMENTS TO THE CLAIMS

1. – 8. (Cancelled)

9. (Currently Amended) An electronic module, comprising:
a conductive-pattern layer;
an insulating-material layer supporting the conductive-pattern layer;
at least one component inside the insulating-material layer, the at least one
component comprising a first surface and contact zones on the first surface;
a first hardened adhesive layer on the first surface of the at least one component;
a second hardened adhesive layer in contact with the conductive-pattern layer and
the first hardened adhesive layer;
holes in the first and second hardened adhesive layer at the locations of the
contact zones; and
conductive material in the holes and in electrical connection with the contact
zones of the component and the conductive-pattern layer.~~The electronic module of claim 8,~~
wherein the first hardened adhesive layer has a first composition and the second hardened
adhesive layer has a second composition different from the first composition.

10. (Cancelled).

11. (Original) The electronic module of claim 9, wherein the second hardened
adhesive layer covers the conductive-pattern layer such that the insulating-material layer
supports the conductive-pattern layer via said second hardened adhesive layer.

12. (Currently Amended) The electronic module of claim ~~[[8]]~~9, wherein the first and
second hardened adhesive layers are local and present at the location of the component such that
the insulating-material layer directly supports the conductive-pattern layer.

13. (Cancelled)

14. (Currently Amended) An electronic module, comprising:
at least one semiconductor component comprising a first surface and a set of
contact zones on the first surface;
a first hardened adhesive layer on the first surface;
a second hardened adhesive layer at least on the first hardened adhesive layer;
contact elements made of metal on the set of contact zones, the contact elements
extending through the first and second hardened adhesive layers;
conductors in contact with the contact elements and forming a conductive-pattern
layer; and
an insulating-material layer around the at least one semiconductor component~~The~~
~~electronic module of claim 13,~~

wherein the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition.

15. (Cancelled).

16. (Currently Amended) The electronic module of claim ~~[[13]]~~14, wherein the at least one semiconductor component comprises at least one microcircuit.

17. (Currently Amended) The electronic module of claim ~~[[13]]~~14, wherein the area of the first hardened adhesive layer is equal to the area of the first surface of the at least one semiconductor component.

18. (Currently Amended) The electronic module of claim ~~[[13]]~~14, wherein the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer.

19. (Currently Amended) The electronic module of claim ~~[[13]]~~14, wherein the contact elements comprise a first layer of metal and at least one second layer of metal.

20. (Currently Amended) The electronic module of claim ~~[[13]]~~14, wherein the contact elements are in metallurgical contact with the respective contact zones and the respective conductors.

REMARKS

Claims 9, 11, 12, 14, and 16 - 20 are now present in this application. Claims 9 and 14 are independent. Claims 1 – 8, 10, 13, and 15 have been canceled, claims 9, 12, 14, and 16 - 20 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Title of the Invention

Applicant(s) have amended the Title of the Invention in order to better reflect the subject matter claimed.

Objection to the Abstract of the Disclosure

The Examiner has objected to the Abstract of the Disclosure because of the use of legal phraseology. In order to overcome this objection, Applicant(s) have amended the Abstract of the Disclosure to delete the legal phraseology. Accordingly, reconsideration and withdrawal of this objection are respectfully requested.

Specification Objections

The Examiner has objected to the specification because of several informalities. In order to overcome this objection, Applicant(s) have amended the specification in order to correct the deficiencies pointed out by the Examiner. Reconsideration and withdrawal of this objection are respectfully requested.

Claim Amendments

Applicant(s) have amended the claims in order to secure subject matter indicated as allowable. No other changes in claim scope or substance are made or intended hereby.

Rejections under 35 U.S.C. § 103 - Mowatt

Claims 1-8, 10, 13 and 15-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mowatt et al. (U.S. Patent No. 5,306,670) [hereinafter "Mowatt"]. Claims 1 – 8, 10, and 15 are cancelled and the dependencies of remaining claims are adjusted so that they now depend from allowable subject matter, rendering this rejection moot.

Allowable Subject Matter

The Examiner states that claims 9, 11, 12 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have so re-written these claims or adjusted their dependency so that they now depend from allowable subject matter.

Conclusion

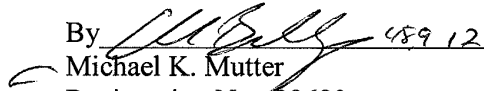
All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant(s) therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Naphtali Y. Matlis, Registration No. 61592, at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: March 2, 2012

Respectfully submitted,

By  489 12
Michael K. Mutter
Registration No. 29680
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road, Suite 100 East
P.O. Box 747
Falls Church, VA 22040-0747
703-205-8000

Electronic Acknowledgement Receipt

EFS ID:	12216848
Application Number:	12699628
International Application Number:	
Confirmation Number:	6266
Title of Invention:	ELECTRIC MODULE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	2292
Filer:	Chad J. Billings/Ruth Calendine
Filer Authorized By:	Chad J. Billings
Attorney Docket Number:	0365-0652PUS3
Receipt Date:	02-MAR-2012
Filing Date:	03-FEB-2010
Time Stamp:	18:08:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20120302AMENDMENT.PDF	324294 7988da0f26b7bfd3d7d05901de398a2697562370	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Specification	3	3
	Abstract	4	4
	Claims	5	9
Warnings:			
Information:			
Total Files Size (in bytes):		324294	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

AMENDMENT TRANSMITTAL LETTER				Docket No. 0365-0652PUS3	
Application No. 12/699,628 - Conf. #6266		Filing Date February 03, 2010		Examiner Alexander O. Williams	
Art Unit 2826					
Applicant(s): Risto TUOMINEN et al.					
Invention: AN ELECTRONIC MODULE HAVING A CONDUCTIVE PATTERN LAYER					
MS AMENDMENT Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450					
Transmitted herewith is an amendment in the above-identified application.					
The fee has been calculated and is transmitted as shown below.					
CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	9	- 20 =	0	x 60	0.00
Independent Claims	2	- 3 =	0	x 250	0.00
Multiple Dependent Claims (check if applicable) ☐				450	0.00
Other fee (please specify):					0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00
☒ Large Entity ☐ Small Entity					
☒ No additional fee is required for this amendment.					
☐ Please charge Deposit Account No. <u>02-2448</u> in the amount of \$ <u>0.00</u> . A duplicate copy of this sheet is enclosed.					
☐ A check in the amount of \$ <u>0.00</u> is enclosed.					
☐ Payment by credit card. Form PTO-2038 is attached.					
☒ The Director is hereby authorized to charge and credit Deposit Account No. <u>02-2448</u> as described below.					
☒ Credit any overpayment.					
☒ Charge any additional filing or application processing fees required under 37 C.F.R. §§ 1.16 and 1.17.					
Michael K. Mutter Attorney Reg. No.: 29680				Dated: <u>March 2, 2012</u>	
BIRCH, STEWART, KOLASCH & BIRCH, LLP 8110 Gatehouse Road, Suite 100 East P.O. Box 747 Falls Church, VA 22040-0747 703-205-8000					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/699,628		Filing Date 02/03/2010		☐ To be Mailed				
APPLICATION AS FILED – PART I													
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY					
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A				N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR		X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =				X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
					TOTAL				TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.													
APPLICATION AS AMENDED – PART II													
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	03/02/2012		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))		* 9	Minus	** 20	= 0		X \$ =		OR		X \$60=	0
	Independent (37 CFR 1.16(h))		* 2	Minus	*** 3	= 0		X \$ =		OR		X \$250=	0
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	0		
AMENDMENT	Total (37 CFR 1.16(i))		*	Minus	**	=		X \$ =		OR		X \$ =	
	Independent (37 CFR 1.16(h))		*	Minus	***	=		X \$ =		OR		X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
						TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE			
	* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

Legal Instrument Examiner:
/JONYA SMALLS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3	6266
2292 7590 11/03/2011 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			EXAMINER WILLIAMS, ALEXANDER O	
			ART UNIT 2826	PAPER NUMBER
			NOTIFICATION DATE 11/03/2011	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Application/Control Number: 12/699,628

Page 2

Art Unit: 2826

Serial Number: 12/699628 Attorney's Docket #: 0365-0652PUS3

Filing Date: 2/3/2010;

Applicant: Tuomonen et al.

Examiner: Alexander Williams

DETAILED ACTION

Applicant's Pre-Amendment filed 2/3/2010 has been acknowledged.

Priority

This application is a CIP of 10/550023 filed 9/23/2005 now U.S. Patent # 7,663,215 which is a 371 of PCT/FI2004/000195 filed 3/31/2004.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the

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patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

- (1) if a machine or apparatus, its organization and operation;
- (2) if an article, its method of making;
- (3) if a chemical compound, its identity and use;
- (4) if a mixture, its ingredients;
- (5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The

Art Unit: 2826

abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.

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- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A
“Sequence Listing” is required on paper if the application discloses a
nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if
the required “Sequence Listing” is not submitted as an electronic
document on compact disc).

The disclosure is objected to because of the following informalities: Applicant's related application information should be updated.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

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consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a first hardened adhesive layer and a second hardened adhesive layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1-8, 10, 13 and 15-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mowatt et al. (U.S. Patent # 5,306,670).

With regards to claim 1, Mowatt et al. (figures 3, 4 and 7) show an electronic module, comprising: a conductive-pattern layer **130**; at least one component **56** comprising contact zones facing the conductive-pattern layer; a hardened adhesive **126** between the component and the conductive-pattern layer, the hardened adhesive

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comprising a first hardened adhesive layer (**lower portion of 126**) in contact with the component **56** and a second hardened adhesive layer (**upper portion of 126**) in contact with the conductive-pattern layer **130**; conductive-material **44** formations penetrating the hardened adhesive between the conductive-pattern layer and the contact zones of the component; and an insulating-material layer **10** around the component on the conductive-pattern layer and conforming to the shape of the component (**see abstract; column 4, line 62 – column 6, lines 47**).

With regards to claim 2, Mowatt et al. show wherein the first hardened adhesive layer (**lower portion of 126**) is in contact with the second hardened adhesive layer (**upper portion of 126**).

With regards to claim 3, Mowatt et al. show wherein the second hardened adhesive layer (**lower portion of 126 directly above 56**) has a first area in contact with the first hardened adhesive layer (**upper portion of 126 and end portion of right side of 126**) and a second area around the first area in contact (**in contact thru 12**) with the insulating-material layer **10**.

With regards to claim 4, Mowatt et al. show wherein the at least one component **56** comprises at least one semiconductor component; the semiconductor component has a first surface facing the conductive-pattern layer **130**; the contact zones **44** are located on the first surface; and the first surface is against the first hardened adhesive layer (**upper portion of 126**).

With regards to claim 5, Mowatt et al. show wherein the first hardened adhesive layer (**upper portion of 126**) covers the first surface outside the contact zones **44**.

With regards to claim 6, Mowatt et al. show wherein a surface area of the first hardened adhesive layer (**upper portion of 126**) is equal to a surface area of the first surface of the component **56**.

With regards to claim 7, Mowatt et al. show wherein a surface area of the second hardened adhesive layer (**lower portion of 126**) is greater than the surface area of the first hardened adhesive layer (**upper portion of 126**).

With regards to claim 8, Mowatt et al. (figures 3, 4 and 7) show an electronic module, comprising: a conductive-pattern layer **130**; an insulating-material layer **10** supporting the conductive-pattern layer; at least one component **56** inside the insulating-material layer **10**, the at least one component comprising a first surface and contact zones on the first surface; a first hardened adhesive layer (**lower portion of 126**) on the first surface of the at least one component **56**; a second hardened adhesive layer (**upper portion of 126**) in contact with the conductive-pattern layer **130** and the first hardened adhesive layer (**lower portion of 126**); holes **44** in the first and second hardened adhesive layer **126** at the locations of the contact zones **44**; and conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer (**see abstract; column 4, line 62 – column 6, lines 47**).

With regards to claim 10, Mowatt et al. show wherein the first hardened adhesive layer and the second hardened adhesive layer have a common composition **126**.

With regards to claim 13, Mowatt et al. (figures 3, 4 and 7) show an electronic module, comprising: at least one semiconductor component **56** comprising a first surface and a set of contact zones on the first surface; a first hardened adhesive layer (**lower portion of 126**) on the first surface; a second hardened adhesive layer (**upper portion of 126**) at least on the first hardened adhesive layer; contact elements made of metal **44** on the set of contact zones, the contact elements extending through the first and second hardened adhesive layers; conductors **44** in contact with the contact elements and forming a conductive-pattern layer **130**; and an insulating-material layer **10** around the at least one semiconductor component **56** (**see abstract; column 4, line 62 – column 6, lines 47**).

With regards to claim 15, Mowatt et al. show wherein the first hardened adhesive layer and the second hardened adhesive layer have a common composition **126**.

With regards to claim 16, Mowatt et al. show wherein the at least one semiconductor component **56** comprises at least one microcircuit.

With regards to claim 17, Mowatt et al. show wherein the area of the first hardened adhesive layer is **(lower portion of 126)** equal to the area of the first surface of the at least one semiconductor component **56**.

With regards to claim 18, Mowatt et al. show wherein the area of the first hardened adhesive layer **(lower portion or 126 being greater than upper portion)** is greater than the area of the second hardened adhesive layer **(upper portion of 126 being smaller than lower portion of 126)**.

With regards to claim 19, Mowatt et al. show wherein the contact elements **44** comprise a first layer of metal and at least one second layer of metal.

With regards to claim 20, Mowatts et al. show wherein the contact elements **44** are in metallurgical contact with the respective contact zones and the respective conductors.

Therefore, it would have been obvious to one of ordinary skill in the art to use the first hardened adhesive layer and the second hardened adhesive layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Allowable Subject Matter

Claims 9, 11, 12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: As to dependent claims 9, 11, 12 and 14, the prior art of record fails to show the combination recited in any of the claims. In particular, the prior art of record fails to show or collectively teach the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition in claims 9 and 14; and the insulating material layer directly supports the conductive pattern layer in claim 12.

The listed references are cited as of interest to this application, but not applied at this time.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571)272-1924. The examiner can normally be reached on 7:00 Am -5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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10/31/2011
/Alexander O Williams/
Primary Examiner, Art Unit 2826

Notice of References Cited	Application/Control No. 12/699,628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.	
	Examiner Alexander O. Williams	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,294,529 B2	11-2007	Tuominen, Risto	438/107
*	B	US-7,609,527 B2	10-2009	Tuominen et al.	361/761
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"12699628"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/28 07:36
L2	2	"7663215".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/28 07:37
L3	2	"5306670".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/10/28 07:50

10/ 28/ 2011 9:23:48 AM**C:\ Users\ awilliams\ Documents\ EAST\ Workspaces\ 12326269.wsp**

Search Notes 	Application/Control No. 12699628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner A O WILLIAMS	Art Unit 2826

SEARCHED			
Class	Subclass	Date	Examiner
257	686,e23.085,e23.178,e25.011,e23.105,e21.705,777,723,778,692,773,774	10/28/11	AW

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	10/28/11	AW
checked 10/550023	10/28/11	AW

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Receipt date: 02/03/2010

12699628 - GAU: 2826

PTO/SB/08a (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known		
				Application Number	NEW 12699628	
Sheet		1	of	2	Attorney Docket Number	0365-0652PUS3
					Filing Date	02-03-10
					First Named Inventor	Risto Tuominen
					Art Unit	Not Yet Assigned 2826
					Examiner Name	Not Yet Assigned /Alexander Williams/

U.S. PATENT DOCUMENTS					
Examiner initial *	Cite No. 1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	1	US-2002/0117743-A1	08-29-2002	Nakatani et al.	
	2	US-2003/0068852-A1	04-10-2003	Towle et al.	
	3	US-2003/0159852-A1	08-28-2003	Nakamura	
	4	US-4,246,595-A1	01-20-1981	Noyori et al.	
	5	US-4,746,392	05-24-1988	Hoppe	
	6	US-5,248,852-A	09-28-1993	Kumagai	
	7	US-5,306,670-A1	04-26-1994	Mowatt et al.	
	8	US-5,353,195-A	10-04-1994	Fillion et al.	
	9	US-5,355,102-A	10-11-1994	Kornrumpf et al.	
	10	US-5,497,033-A	03-05-1996	Fillion et al.	
	11	US-5,552,633-A	09-03-1996	Sharma	
	12	US-6,038,133-A	03-14-2000	Nakatani et al.	
	13	US-6,154,366-A	11-28-2000	Ma et al.	
	14	US-6,271,469-B1	08-07-2001	Ma et al.	
	15	US-6,284,564-B1	09-04-2001	Balch et al.	
	16	US-6,396,148-B1	05-28-2002	Eichelberger et al.	
	17	US-6,475,877-B1	11-05-2002	Saia et al.	
	18	US-6,701,614-B2	03-09-2004	DING et al.	
	19	US-6,713,859-B1	03-30-2004	Ma	
	20	US-6,783,077-B1	08-31-2004	Fannasch	

FOREIGN PATENT DOCUMENTS							
Examiner Initial *	Cite No. 1	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country ³ Code	Number ⁴ Kind Code (if known) ⁵				
	21	WO	03/065778-A1	08-07-2003			
	22	JP	2001-053447-A	02-23-2001			

Examiner Signature	/Alexander Williams/	Date Considered	10/28/2011
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include of this form with next communication to applicant.

1. Applicant's unique citation designation number (optional) 2. See Kinds codes of USPTO patent Documents, at www.uspto.gov or MPEP 901.04.

3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3.) 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

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12699628 - GAU: 2826

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	NEW 12699628
				Filing Date	02-03-10
				First Named Inventor	Risto Tuominen
				Art Unit	Not Yet Assigned 2826
				Examiner Name	Not Yet Assigned /Alexander Williams/
				Attorney Docket Number	0365-0652PUS3
Sheet	2	of	2		

[illegible][illegible]

Examiner Signature	/Alexander Williams/	Date Considered	10/28/2011
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<i>Index of Claims</i> 	Application/Control No. 12699628	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner A O WILLIAMS	Art Unit 2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	10/28/2011									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
	7	✓									
	8	✓									
	9	O									
	10	✓									
	11	O									
	12	O									
	13	✓									
	14	O									
	15	✓									
	16	✓									
	17	✓									
	18	✓									
	19	✓									
	20	✓									



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/699,628	02/03/2010	Risto Tuominen	0365-0652PUS3

CONFIRMATION NO. 6266

2292

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

PUBLICATION NOTICE



OC000000043019430

Title:ELECTRIC MODULE

Publication No.US-2010-0202114-A1

Publication Date:08/12/2010

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/699,628	02/03/2010	1795	1220	0365-0652PUS3	20	3

CONFIRMATION NO. 6266

UPDATED FILING RECEIPT



OC000000041416312

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

Date Mailed: 05/05/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Risto Tuominen, Espoo, FINLAND;
Petteri Palm, Helsinki, FINLAND;

Assignment For Published Patent Application

Imbera Electronics Oy, Espoo, FINLAND

Power of Attorney: The patent practitioners associated with Customer Number 02292

Domestic Priority data as claimed by applicant

This application is a CIP of 10/550,023 09/23/2005 PAT 7,663,215
which is a 371 of PCT/FI2004/000195 03/31/2004

Foreign Applications

FINLAND 20030493 04/01/2003

If Required, Foreign Filing License Granted: 02/18/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/699,628**

Projected Publication Date: 08/12/2010

Non-Publication Request: No

Early Publication Request: No

Title

ELECTRIC MODULE

Preliminary Class

430

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Docket No.: 0365-0652PUS3
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Risto TUOMINEN et al.et al

Application No.: 12/699,628

Confirmation No.: 6266

Filed: February 03, 2010

Art Unit: Not Yet Assigned

For: AN ELECTRONIC MODULE

Examiner: Not Yet Assigned

**SUBMISSION OF ADDITIONAL DOCUMENTS AND/OR
FEES FOR COMPLETION OF FILING REQUIREMENTS**

MS MISSING PARTS

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

The following documents are submitted in connection with the above-identified application:

- ☒ The Notice to File Missing Parts of Non-provisional Application.
- ☐ The Notification of Missing Requirements (371 Formalities Letter).
- ☐ The Notice to File Missing Parts of Provisional Application.
- ☐ The Notice to File Missing Parts of Reissue Application.
- ☐ The Notice to File Corrected Application Papers.
- ☐ The Notice of Omitted Items.
- ☐ The Notice of Incomplete Application Papers.

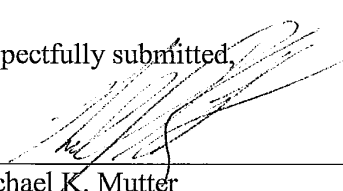
- ☒ Executed Declaration and Power of Attorney.
- ☒ The undersigned hereby declares that "Attorney Docket No. 0365-0652PUS3" on page of the attached Declaration corresponds to Application No. 12/699,628, filed February 3, 2010 entitled "AN ELECTRONIC MODULE."
- ☐ Attached is an accurate English language translation of the above-identified application that was filed in a foreign language, which should be used as the copy for examination purposes.
- ☐ Assent of Assignee and Statement under 37 C.F.R. 3.73(b) establishing ownership.
- ☐ Preliminary Amendment.
- ☐ Substitute specification that complies with 37 C.F.R. § 1.52. The substitute specification does not contain new matter.
- ☐ Substitute Sequence Listing (paper and electronic copy).
- ☐ The attached sheet(s) of drawing(s), including Figure(s) , should be substituted for the corresponding sheet(s) of drawing(s) on file.
- ☐ Corrected Provisional Application Cover Sheet identifying the city and state or city and foreign country of the residence of each inventor.
- ☐ Supplemental Application Data Sheet (ADS).
- ☐ Claims small entity status under 37 C.F.R. § 1.27.
- ☐ Petition for Extension of Time.
- ☒ Fee transmittal listing the required fees.
- ☐ All filing requirements were met in a previous submission on . Copies of previously submitted documents are readily available in PAIR.

☐ Other:

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: April 23, 2010

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road, Suite 100 East

P.O. Box 747

Falls Church, VA 22040-0747

703-205-8000

Attachments



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/699,628	02/03/2010	Risto TUOMINEN	0365-0652PUS3

CONFIRMATION NO. 6266

FORMALITIES LETTER



2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

Date Mailed: 02/23/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$1220 for a non-small entity

- \$330 Statutory basic filing fee.
- \$130 Surcharge.
- The application search fee has not been paid. Applicant must submit \$540 to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$220 to complete the examination fee for a non-small entity.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/masfaw/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING

BIRCH, STEWART, KOLASCH & BIRCH, LLP

P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT AND DESIGN APPLICATIONS

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: Method for manufacturing an electronic module and an electronic module

Fill in Appropriate the specification of which is attached hereto. If not attached hereto, the application is identified by the attorney docket number as set forth above and/or the following:

Information - The specification was filed on February 3, 2010 as
For Use Without United States Application Number 12/699,628;
Specification and amended on _____ (if applicable) and/or
Attached: the specification was filed on _____ as PCT
International Application Number _____; and was
amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)	Priority Foreign Application(s)	Priority Claimed
<u>20030493</u> (Number)	<u>Finland</u> (Country)	<u>April 1, 2003</u> (Month/Day/Year Filed)
		☒ Yes ☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)
		☐ Yes ☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)
		☐ Yes ☐ No
<u> </u> (Number)	<u> </u> (Country)	<u> </u> (Month/Day/Year Filed)
		☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

Insert Provisional Application(s): (if any)	(Application Number)	(Filing Date)
	<u> </u>	<u> </u>
	<u> </u>	<u> </u>

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Insert Requested Information: (if appropriate)	Country	Application Number	Date of Filing (Month/Day/Year)
	<u> </u>	<u> </u>	<u> </u>
	<u> </u>	<u> </u>	<u> </u>

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s), including for continuation-in-part application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S. Application(s): (if any)	(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
	<u>10/550,023</u>	<u>Sept. 23, 2005</u>	<u>patented</u>
	<u> </u>	<u> </u>	<u> </u>
	<u> </u>	<u> </u>	<u> </u>

I hereby appoint the practitioners at CUSTOMER NO. 02292 as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the United States Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

CUSTOMER NO. 02292 (BIRCH, STEWART, KOLASCH & BIRCH, LLP)

Telephone: (703) 205-8000

Facsimile: (703) 205-8050

PLEASE NOTE:
YOU MUST
COMPLETE
THE
FOLLOWING:

Full Name of First
or Sole Inventor:
Insert Name of
Inventor →
Insert Date This
Document is Signed

Insert Residence
Insert Citizenship →

Insert Post Office
Address →

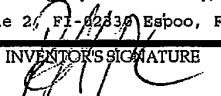
Full Name of Second
Inventor, if any:
see above

Full Name of Third
Inventor, if any:
see above

Full Name of Fourth
Inventor, if any:
see above

Full Name of Fifth
Inventor, if any:
see above

Full Name of Sixth
Inventor, if any:
see above

GIVEN NAME/FAMILY NAME Risto Tuominen		INVENTOR'S SIGNATURE 	DATE* 2010/03/18
Residence (City, State & Country) Espoo, Finland		CITIZENSHIP Finnish	
MAILING ADDRESS (Complete Street Address including City, State & Country) c/o Imbera Electronics Oy, Ruukintie 2, FI-02830 Espoo, Finland			
GIVEN NAME/FAMILY NAME Petteri Palm		INVENTOR'S SIGNATURE 	DATE* 2010/03/22
Residence (City, State & Country) Helsinki, Finland		CITIZENSHIP Finnish	
MAILING ADDRESS (Complete Street Address including City, State & Country) Alkutie 47 as. 1, FI-00660 Helsinki, Finland			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME/FAMILY NAME		INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
MAILING ADDRESS (Complete Street Address including City, State & Country)			

Electronic Patent Application Fee Transmittal				
Application Number:		12699628		
Filing Date:		03-Feb-2010		
Title of Invention:		ELECTRIC MODULE		
First Named Inventor/Applicant Name:		Risto TUOMINEN		
Filer:		Michael Keith Mutter		
Attorney Docket Number:		0365-0652PUS3		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1220

Electronic Acknowledgement Receipt	
EFS ID:	7480787
Application Number:	12699628
International Application Number:	
Confirmation Number:	6266
Title of Invention:	ELECTRIC MODULE
First Named Inventor/Applicant Name:	Risto TUOMINEN
Customer Number:	02292
Filer:	Michael Keith Mutter/Crystal Boyer/smt
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0652PUS3
Receipt Date:	23-APR-2010
Filing Date:	03-FEB-2010
Time Stamp:	19:13:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1220
RAM confirmation Number	5358
Deposit Account	022448
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Perfect.pdf	339224	yes	8
			e4d180c34feafa73db74e1259740b1136f03959e		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Miscellaneous Incoming Letter	1	1		
	Applicant Response to Pre-Exam Formalities Notice	2	6		
	Oath or Declaration filed	7	8		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	36523	no	2
			8f74425e9c7b7d4d327d478ebdb55c2e77ed64ee		
Warnings:					
Information:					
Total Files Size (in bytes):			375747		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2009		Complete if Known	
☐ Applicant claims small entity status. See 37 CFR 1.27		Application Number 12/699,628	Conf. No.: 6266
TOTAL AMOUNT OF PAYMENT (\$) 1,220.00		Filing Date February 3, 2010	First Named Inventor Risto TUOMINEN
		Examiner Name Not Yet Assigned	Art Unit Not Yet Assigned
		Attorney Docket No. 0365-0652PUS3	

METHOD OF PAYMENT (check all that apply)

☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: _____

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	<u>Small Entity</u> Fee (\$)	Fee (\$)	<u>Small Entity</u> Fee (\$)	Fee (\$)	<u>Small Entity</u> Fee (\$)	
Utility	330	165	540	270	220	110	1,090.00
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	<u>Small Entity</u> Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

Total Claims 20 - 20 or HP = 0 x = 0.00
 Extra Claims Fee (\$): 0
 Fee Paid (\$) 0.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims 3 - 3 or HP = 0 x = 0.00
 Extra Claims Fee (\$): 0
 Fee Paid (\$) 0.00

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

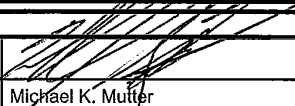
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
32	0	0	0	0.00

32 - 100 = 0 / 50 = 0 (round up to a whole number) x = 0.00

4. OTHER FEE(S)

Description	Fee (\$)	Fees Paid (\$)
Non-English Specification, \$130 fee (no small entity discount)	0.00	0.00
Other (e.g., late filing surcharge): 105T Surcharge-Late oath or declaration	130.00	130.00

SUBMITTED BY			
Signature		Registration No. 29680 (Attorney/Agent)	Telephone 703-205-8000
Name (Print/Type)	Michael K. Muller	Date	April 23, 2010

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/699,628	02/03/2010	Risto TUOMINEN	0365-0652PUS3

CONFIRMATION NO. 6266

FORMALITIES LETTER



OC000000040175746

Date Mailed: 02/23/2010

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is \$1220 for a non-small entity

- \$330 Statutory basic filing fee.
- \$130 Surcharge.
- The application search fee has not been paid. Applicant must submit \$540 to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$220 to complete the examination fee for a non-small entity.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/masfaw/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/699,628	02/03/2010	1795	0.00	0365-0652PUS3	20	3

CONFIRMATION NO. 6266

2292

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

FILING RECEIPT



OC000000040175745*

Date Mailed: 02/23/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Risto TUOMINEN, Helsinki, FINLAND;
Petteri Palm, Helsinki, FINLAND;

Assignment For Published Patent Application

Imbera Electronics Oy, Espoo, FINLAND

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 10/550,023 09/23/2005 PAT 7,663,215
which is a 371 of PCT/FI2004/000195 03/31/2004

Foreign Applications

FINLAND 20030493 04/01/2003

If Required, Foreign Filing License Granted: 02/18/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/699,628**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

ELECTRIC MODULE

Preliminary Class

430

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">Attorney Docket No.</td> <td style="padding: 2px;">0365-0652PUS3</td> </tr> <tr> <td style="padding: 2px;">First Inventor</td> <td style="padding: 2px;">Risto TUOMINEN</td> </tr> <tr> <td style="padding: 2px;">Title</td> <td style="padding: 2px;">AN ELECTRONIC MODULE</td> </tr> <tr> <td style="padding: 2px;">Express Mail Label No.</td> <td style="padding: 2px;"></td> </tr> </table>	Attorney Docket No.	0365-0652PUS3	First Inventor	Risto TUOMINEN	Title	AN ELECTRONIC MODULE	Express Mail Label No.	
Attorney Docket No.	0365-0652PUS3								
First Inventor	Risto TUOMINEN								
Title	AN ELECTRONIC MODULE								
Express Mail Label No.									

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450
--	--

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) 2. ☐ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages <u>24</u>] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>8</u>] 5. Oath or Declaration [Total Sheets _____] a. ☐ Newly executed (original or copy) b. ☐ A copy from a prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 18 completed)</i> i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☒ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (<i>Appendix</i>) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, items a. – c. are required)</i> a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet (PTO-1595) & document(s)) Name of Assignee _____ 10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney <i>(when there is an assignee)</i> 11. ☐ English Translation Document <i>(if applicable)</i> 12. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of foreign patent documents, publications, & other information 13. ☒ Preliminary Amendment 14. ☐ Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> 15. ☐ Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 16. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other: _____
--	---

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation
 ☐ Divisional
 ☒ Continuation-in-part (CIP)
 of prior application No.: 10/550,023

Prior application information:
 Examiner Not Yet Assigned
 Art Unit: Not Yet Assigned

19. CORRESPONDENCE ADDRESS

☐ The address associated with Customer Number: 02292
 OR
☐ Correspondence address below

Name				
Address				
City	State	Zip Code		
Country	Telephone	Email		

Signature	Date
Name (Print/Type) <u>Michael K. Mutter</u>	<u>February 3, 2010</u> Registration No. (Attorney/Agent) <u>29680</u>

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).**FEE TRANSMITTAL**
For FY 2009☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$) 0.00**Complete if Known**

Application Number	NEW	Conf. No.:
Filing Date	2/3/2010	
First Named Inventor	Risto TUOMINEN	
Examiner Name	Not Yet Assigned	
Art Unit	Not Yet Assigned	
Attorney Docket No.	0365-0652PUS3	

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit Card ☐ Money Order ☒ None ☐ Other (please identify): _____☐ Deposit Account Deposit Account Number: _____ Deposit Account Name: _____

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below☐ Charge fee(s) indicated below, **except for the filing fee**☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17☐ Credit any overpayments**WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**FEE CALCULATION****1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES**Fee Description**

Each claim over 20 (including Reissues)

Fee (\$)	Small Entity Fee (\$)
----------	-----------------------

52 26

Each independent claim over 3 (including Reissues)

220 110

Multiple dependent claims

390 195

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
20	- 20 or HP = 0	x	= 0.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
- 3 or HP = 0	x	= 0.00	

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
33	- 100 = 0	/ 50 = 0	(round up to a whole number) x	= 0.00

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Fees Paid (\$)

Other (e.g., late filing surcharge)

SUBMITTED BY

Signature	Registration No. 29680 (Attorney/Agent)	Telephone 703-205-8000
Name (Print/Type) Michael K. Mutter	Date February 3, 2010	

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Data Sheet

Application Information

Application Type::	Regular
Subject Matter::	Continuation-In-Part
Suggested Group Art Unit::	N/A
CD-ROM or CD-R?::	None
Sequence submission?::	None
Computer Readable Form (CRF)?::	No
Title::	AN ELECTRONIC MODULE
Attorney Docket Number::	0365-0652PUS3
Request for Early Publication?::	No
Request for Non-Publication?::	No
Total Drawing Sheets::	8
Small Entity?::	No
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

Applicant Information

Applicant Authority Type::	Inventor
Primary Citizenship Country::	Finland
Status::	Full Capacity
Given Name::	Risto
Family Name::	TUOMINEN
City of Residence::	Helsinki
Country of Residence::	Finland
Street of mailing address::	Vainoelankatu 17 B 18
City of mailing address::	Helsinki
Country of mailing address::	Finland
Postal or Zip Code of mailing address::	FI-00610

Applicant Authority Type:: Inventor
 Primary Citizenship Country:: Finland
 Status:: Full Capacity
 Given Name:: Petteri
 Family Name:: PALM
 City of Residence:: Helsinki
 Country of Residence:: Finland
 Street of mailing address:: Alkutie 47 as. 1
 City of mailing address:: Helsinki
 Country of mailing address:: Finland
 Postal or Zip Code of mailing address:: FI-00660

Correspondence Information

Correspondence Customer Number:: 02292

Representative Information

Representative Customer Number:: 02292

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application is a	Continuation-in-part of	10/550,023	9/23/2005
10/550,023 is a	National Stage of	PCT/FI2004/000195	3/31/2004

Foreign Priority Information

Country::	Application number::	Filing Date::	Priority Claimed::
Finland	20030493	04/01/2003	Yes

Assignee Information

Assignee name::	Imbera Electronics Oy
Street of mailing address::	P.O. Box 74
City of mailing address::	Espoo
Country of mailing address::	Finland
Postal or Zip Code of mailing address::	FI-02151

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Risto TUOMINEN et al.

Application No.: NEW

Confirmation No.: Not Yet Assigned

Filed: February 3, 2010

Art Unit: Not Yet Assigned

For: AN ELECTRONIC MODULE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the attached PTO/SB/08.

II. COPIES

☐ a. Copies of foreign patent documents, non-patent literature and other information.

☒ b. REFERENCES PREVIOUSLY CITED OR SUBMITTED: Copies of any information not provided can be found in one or more of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Application No. and U.S. Filing Date

10/550,023 filed September 23, 2005

III. CONCISE EXPLANATION OF THE RELEVANCE/OTHER INFORMATION

☐ a. NON-ENGLISH LANGUAGE DOCUMENTS: A concise explanation of the relevance of all non-English language patents, publications, or other information listed is as follows:

☐ b. ENGLISH LANGUAGE SEARCH REPORT OR FOREIGN PATENT OFFICE COMMUNICATION: An English language version of the search report or Foreign Patent Office communication that indicates the degree of relevance is attached.

☐ c. OTHER: The following additional information is provided.

IV. STATEMENT UNDER 37 C.F.R. § 1.97(e)

The undersigned hereby states that:

☐ a. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than **30 days** prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ b. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than **three months** prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ c. No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.

☐ d. Some of the items of information in the IDS were cited in a communication from a foreign patent office. Such items were first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office. As to the remaining items of information, to the knowledge of the person signing the certification after making reasonable inquiry, such remaining items were not known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

V. FEES

☒ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application or Request for Continued Examination. No fee is required.

☐ b. This Information Disclosure Statement is being filed within three months of the filing date of an application. No fee is required.

☐ c. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits. No fee is required. If a first Office Action on the merits has issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) above. If no statement has been made, charge our deposit account for the required fee.

☐ d. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action or before the mailing date of a Notice of Allowance (see 37 C.F.R. § 1.97(c)(1)).

☐ No statement. The fee as required by 37 C.F.R. § 1.17(p) is provided.

or

☐ See the above statement. No fee is required.

☐ e. This Information Disclosure Statement is being filed after the mailing date of a Final Office Action or after the mailing date of a Notice of Allowance (see 37 C.F.R. § 1.97(d)), see the statement above. The fee as required by 37 C.F.R. § 1.17(p) is provided.

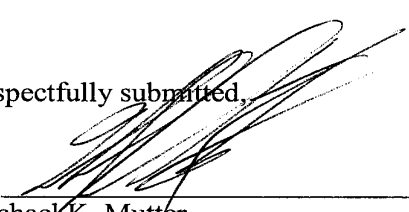
VI. PAYMENT OF FEES

☐ The required fee is listed on the attached Fee Transmittal.

☒ No fee is required.

Dated: February 3, 2010

Respectfully submitted,

By 

Michael K. Mutter

Registration No.: 29680

BIRCH, STEWART, KOLASCH & BIRCH, LLP

8110 Gatehouse Road, Suite 100 East

P.O. Box 747

Falls Church, VA 22040-0747

703-205-8000

Attachment(s):

- ☒ PTO/SB/08
- ☐ Document(s)
- ☐ Foreign Patent Office Communication
- ☐ Foreign Search Report
- ☐ Fee
- ☐ Other:

Under the Paperwork reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known		
				Application Number	NEW	
Sheet		1	of	2	Attorney Docket Number	0365-0652PUS3

U.S. PATENT DOCUMENTS						
Examiner initial *	Cite No. 1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number - Kind Code ² (if known)				
	1	US-2002/0117743-A1	08-29-2002	Nakatani et al.		
	2	US-2003/0068852-A1	04-10-2003	Towle et al.		
	3	US-2003/0159852-A1	08-28-2003	Nakamura		
	4	US-4,246,595-A1	01-20-1981	Noyori et al.		
	5	US-4,746,392	05-24-1988	Hoppe		
	6	US-5,248,852-A	09-28-1993	Kumagai		
	7	US-5,306,670-A1	04-26-1994	Mowatt et al.		
	8	US-5,353,195-A	10-04-1994	Fillion et al.		
	9	US-5,355,102-A	10-11-1994	Kornrumpf et al.		
	10	US-5,497,033-A	03-05-1996	Fillion et al.		
	11	US-5,552,633-A	09-03-1996	Sharma		
	12	US-6,038,133-A	03-14-2000	Nakatani et al.		
	13	US-6,154,366-A	11-28-2000	Ma et al.		
	14	US-6,271,469-B1	08-07-2001	Ma et al.		
	15	US-6,284,564-B1	09-04-2001	Balch et al.		
	16	US-6,396,148-B1	05-28-2002	Eichelberger et al.		
	17	US-6,475,877-B1	11-05-2002	Saia et al.		
	18	US-6,701,614-B2	03-09-2004	DING et al.		
	19	US-6,713,859-B1	03-30-2004	Ma		
	20	US-6,783,077-B1	08-31-2004	Fannasch		

FOREIGN PATENT DOCUMENTS							
Examiner Initial *	Cite No. 1	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country ³ Code	Number ⁴ Kind Code (if known) ⁵				
	21	WO	03/065778-A1	08-07-2003			
	22	JP	2001-053447-A	02-23-2001			

Examiner Signature	Date Considered
--------------------	-----------------

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include of this form with next communication to applicant.

1. Applicant's unique citation designation number (optional) 2. See Kinds codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04.

3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3.) 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.

Under the Paperwork reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	NEW
				Filing Date	02-03-10
				First Named Inventor	Risto Tuominen
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	0365-0652PUS3

[illegible][illegible]

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include of this form with next communication to applicant.

1. Applicant's unique citation designation number (optional) 2. See Kinds codes of USPTO patent Documents, at www.uspto.gov or MPEP 901.04.

3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3.) 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.3.16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.

Docket No.: 0365-0652PUS3
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Risto TUOMINEN et al.

Application No.: NEW

Confirmation No.: Not Yet Assigned

Filed: February 3, 2010

Art Unit: Not Yet Assigned

For: AN ELECTRONIC MODULE

Examiner: Not Yet Assigned

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination on the merits, please amend the above-identified U.S. patent application as follows:

Amendments to the Specification begin on page 2.

Remarks begin on page 3.

AMENDMENTS TO THE SPECIFICATION

Before line 1 of the specification (after the Title), please insert the following new header and paragraph:

Cross Reference to Related Applications:

This application is a Continuation-In-Part of co-pending U.S. Application No. 10/550,023 filed on September 23, 2005, which is the National Stage application of PCT International Application No. PCT/FI2004/000195 filed on March 31, 2004, which claims the benefit of and to Patent Application No. 20030493 filed in Finland, on April 1, 2003. The entire contents of all of the above applications is hereby incorporated by reference.

REMARKS

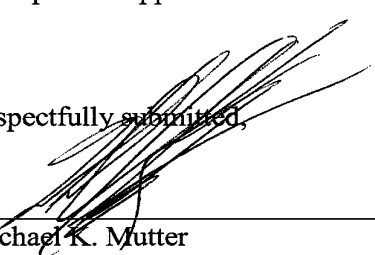
The Specification has been amended to make cross-reference to the related applications.
Claims 1-20 are pending in this application.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Michael K. Mutter, Registration No. 29,680 at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

Dated: February 3, 2010

Respectfully submitted,

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Attachment(s)

An Electronic Module

The present invention relates to an electronic modules.

5 In particular, the invention relates to an electronic module, which includes one or more components embedded in an installation base. The electronic module can be a module like a circuit board, which includes several components, which are connected to each other electrically, through conducting structures manufactured in the module. The components can be passive components, microcircuits, semiconductor components, or
10 other similar components. Components that are typically connected to a circuit board form one group of components. Another important group of components are components that are typically packaged for connection to a circuit board. The electronic modules to which the invention relates can, of course, also include other types of components.

15 The installation base can be of a type similar to the bases that are generally used in the electronics industry as installation bases for electrical components. The task of the base is to provide components with a mechanical attachment base and the necessary electrical connections to both components that are on the base and those that are outside the base. The installation base can be a circuit board, in which case the construction and method to
20 which the invention relates are closely related to the manufacturing technology of circuit boards. The installation base may also be some other base, for example, a base used in the packaging of a component or components, or a base for an entire functional module.

The manufacturing techniques used for circuit boards differ from those used for
25 microcircuits in, among other things, the fact that the installation base in microcircuit manufacturing techniques, i.e. the substrate, is of a semiconductor material, whereas the base material of an installation base for circuit boards is some form of insulating material. The manufacturing techniques for microcircuits are also typically considerably more expensive than the manufacturing techniques for circuit boards.

30 The constructions and manufacturing techniques for the cases and packages of components, and particularly semiconductor components differ from the construction and manufacture of circuit boards, in that component packaging is primarily intended to form

a casing around the component, which will protect the component mechanically and facilitate the handling of the component. On the surface of the component, there are connector parts, typically protrusions, which allow the packaged component to be easily set in the correct position on the circuit board and the desired connections to be made to it. In addition, inside the component case, there are conductors, which connect the connector parts outside the case to connection zones on the surface of the actual component, and through which the component can be connected as desired to its surroundings.

However, component cases manufactured using conventional technology demand a considerable amount of space. As electronic devices have grown smaller, there has been a trend to eliminate component cases, which take up space, are not essential, and create unnecessary costs. Various constructions and methods have been developed to solve this problem.

One known solution is flip-chip (FC) technology, in which non-packaged semiconductor components are installed and connected directly to the surface of the circuit board. However, flip-chip technology has many weaknesses and difficulties. For example, the reliability of the connections can be a problem, especially in applications, in which mechanical stresses arise between the circuit board and the semiconductor component. In an attempt to avoid mechanical stresses, a suitable elastic underfill, which equalizes mechanical stresses, is added between the semiconductor component and the circuit board. This procedural stage slows down the manufacturing process and increases costs. Even the thermal expansion caused by the normal operation of a device may cause mechanical stresses large enough to compromise the long-term reliability of an FC structure.

US patent publication 4 246 595 discloses one solution, in which recesses are formed in the installation base for the components. The bottoms of the recesses are bordered by a two-layered insulation layer, in which holes are made for the connections of the component. The layer of the insulation layer that lies against the components is made of an adhesive. After this, the components are embedded in the recesses with their connection zones facing the bottom of the recess, electrical contacts being formed to the

components through the holes in the insulation layer. If it is wished to make the structure mechanically durable, the component must also be attached to an installation base, so that the method is quite complicated. It is extremely difficult to use a complicated method, which demands several different materials and process stages, to profitably
5 manufacture cheap products. In other ways too, the method does not correspond to the technology used nowadays (the patent dates from 1981).

JP application publication 2001-53 447 discloses a second solution, in which a recess is made for the component in an installation base. The component is placed in the recess,
10 with the component's contact zones facing towards the surface of the installation base. Next, an insulation layer is made on the surface of the installation base and over the component. Contact openings for the component are made in the insulation layer and electrical contacts are made to the component, through the contact openings. In this method, considerable accuracy is demanded in manufacturing the recess and setting the
15 component in the recess, so that the component will be correctly positioned, to ensure the success of the feed-throughs, relative to the width and thickness of the installation board.

The invention is intended to create a relatively simple and economical method for manufacturing electronic modules, with the aid of which a mechanically durable
20 construction can be achieved.

The invention is based on the component being glued to the surface of a conductive layer, from which conductive layer conductive patterns are later formed. After the gluing of the component, an insulating-material layer, which surrounds the component attached
25 to the conductive layer, is formed on, or attached to the surface of the conductive layer. After the gluing of the component, feed-throughs are also made, through which electrical contacts can be formed between the conductive layer and the conductive zones of the component. After this, conductive patterns are formed from the conductive layer, to which the component is glued.

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Considerable advantages are gained with the aid of the invention. This because it is possible, with the aid of the invention, to manufacture mechanically durable electronic modules, which include unpackaged components embedded in an installation base.

The invention permits a quite simple manufacturing method, in which relatively few different materials are required. For this reason, the invention has embodiments, with the aid of which electronic modules can be manufactured at low cost. For example, in the technique disclosed in US patent publication 4 246 595, (the references are to figure 8 of the patent) a support layer 24, an insulating layer 16, and an adhesion layer 17 are required. In addition, a fourth insulating material (not shown in the embodiment of figure 8), i.e. filler with the aid of which the component is attached to the support layer 24, is also required, in order to create a mechanically sturdy attachment. In the solution of the JP application publication 2001-53 447 too, a corresponding attachment that entirely surrounds the component requires about 3 - 4 separate insulating materials, or insulating layers (publication figures 2 and 4).

Unlike the reference publications, our invention has embodiments, in which the component can be entirely surrounded using 2 - 3 insulating materials, or insulating layers. This because the contact surface of the component is glued to a conductive layer, so that, in preferred embodiments, the adhesive attaches the component essentially over the entire area of its contact surface. Elsewhere, in such an embodiment, the component is attached with the aid of an insulating-material layer, which acts as the base material for the electronic module being formed. The insulating-material layer is formed after the gluing of the component, so that in preferred embodiments it can be made around the component to conform to the shape of the component. In such embodiments, it is possible to achieve a comprehensive attachment of the component with the aid of an adhesive layer and a base-material layer formed from 1 - 2 insulating-material sheets.

In the embodiments of the invention, it is thus possible to manufacture a circuit board, inside which components are embedded. The invention also has embodiments, with the aid of which a small and reliable component package can be manufactured around a component, as part of the circuit board. In such an embodiment, the manufacturing process is simpler and cheaper than manufacturing methods in which separate packaged components are installed and connected to the surface of the circuit board. The manufacturing method can also be applied to use the method to manufacture Reel-to-Reel products. Thin and cheap circuit-board products containing components can be

made by using the methods according to the preferred embodiments.

The invention also permits many other preferred embodiments, which can be used to obtain significant additional advantages. With the aid of such embodiments, a component's packaging stage, the circuit board's manufacturing stage, and the assembly and connecting stage of the components, for example, can be combined to form a single totality. The combination of the separate process stages brings significant logistical advantages and permits the manufacture of small and reliable electronic modules. A further additional advantage is that such an electronic-module manufacturing method can mostly utilize known circuit-board manufacturing and assembly techniques.

The composite process according to the embodiment referred to above is, as a totality, simpler than manufacturing a circuit board and attaching a component to the circuit board using, for example, the flip-chip technique. By using such preferred embodiments, the following advantages are obtained, compared to other manufacturing methods:

- Soldering is not needed in the connections of the components, instead an electrical connection between the connection zones on the surface of the component and the metal film of the installation base is created by a via-method. This means that the connection of a component does not need metal being maintained molten for a long time with its associated high temperature. Thus, the construction is made more reliable than soldered connections. The brittleness of the metal alloys creates large problems particularly in small connections. In a solderless solution according to a preferred embodiment, it is possible to achieve clearly smaller constructions than in soldered solutions.

- As smaller structures can be manufactured using the method, the components can be placed closer together. Thus, the conductors between the components also become shorter and the characteristics of the electronic circuits improve. For example, losses, interferences, and transit-time delays can be significantly reduced.

- The method permits a lead-free manufacturing process, which is environmentally

friendly.

-When using a solderless manufacturing process, fewer undesirable intermetallics also arise, thus improving the long-term reliability of the construction.

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-The method also permits three-dimensional structures to be manufactured, as the installation bases and the components embedded in them can be stacked on top of each other.

10 The invention also permits other preferred embodiments. For instance, flexible circuit boards can be used in connection with the invention. Further, in embodiments, in which the temperature of the installation base can be kept low during the entire process, organic manufacturing materials can be used comprehensively.

15 With the aid of embodiments, it is also possible to manufacture extremely thin structures, in which, despite the thinness of the structure, the components are entirely protected inside their installation base, such as a circuit board.

In embodiments, in which the components are located entirely inside the installation
20 base, the connections between the circuit board and the components will be mechanically durable and reliable.

The embodiments also permit the design of electronic-module manufacturing processes requiring relatively few process stages. Embodiments with fewer process stages
25 correspondingly also require fewer process devices and various manufacturing methods. With the aid of such embodiments, it is also possible in many cases to cut manufacturing costs compared to more complicated processes.

30 The number of conductive-pattern layers of the electronic module can also be chosen according to the embodiment. For example, there can be one or two conductive-pattern layers. Additional conductive-pattern layers can be manufactured on top of these, in the manner known in the circuit-board industry. A total module can thus incorporate, for example, three, four, or five conductive-pattern layers. The very simplest embodiments

have only one conductive-pattern layer and indeed one conductor layer. In some embodiments, each of the conductor layers contained in the electronic module can be exploited when forming conductive patterns.

5 In embodiments, in which the conductor layer connected to a component is patterned only after the connection of the component, the conductor layer can include conductor patterns even at the location of the component. A corresponding advantage can also be achieved in embodiments, in which the electronic module is equipped with a second conductive-pattern layer, which is located on the opposite surface of the base material of
10 the module (on the opposite surface of the insulation material layer relative to the conductive-pattern layer connected to the component). The second conductor layer can thus also include conductive patterns at the location of the component. The placing of conductive patterns in the conductor layers at the location of the component will permit a more efficient use of space in the module and a denser structure.

15 In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

Figures 1 - 10 show a series of cross-sections of some examples of manufacturing methods according to the invention and schematic cross-sectional diagrams of some
20 electronic modules according to the invention.

Figure 11 shows a cross-sectional view of one electronic module according to the invention, which includes several installation bases on top of each other.

25 Figure 12 shows two adhesive layers according to an embodiment.

Figure 13 shows a cross-section of a module with two-layer adhesive according to an embodiment.

30 Figure 14 shows a cross-section of a module with two-layer adhesive according to another embodiment.

In the methods of the examples, manufacturing starts from a conductive layer 4, which

can be, for example, a metal layer. One suitable manufacturing material for the conductive layer 4 is copper film (Cu). If the conductive film 4 selected for the process is very thin, or the conductive film is not mechanically durable for other reasons, it is recommended that the conductive film 4 be supported with the aid of a support layer 12.

5 This procedure can be used, for example, in such a way that the process is started from the manufacture of the support layer 12. This support layer 12 can be, for example, an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer. An unpatterned conductive layer 4 can be made on the second surface of the support layer 12, for example, by using some manufacturing

10 method well known in the circuit-board industry. The conductive layer can be manufactured, for example, by laminating a copper film (Cu) on the surface of the support layer 12. Alternatively, it is possible to proceed by making the support layer 12 on the surface of the conductive layer 4. The conductive film 4 can also be a surfaced metal film, or some other film including several layers, or several materials.

15 Later in the process, conductive patterns are made from the conductive layer 4. The conductive patterns must then be aligned relative to the components 6. The alignment is most easily performed with the aid of suitable alignment marks, at least some of which can be made already in this stage of the process. Several different methods are available for creating the actual alignment marks. One possible method is to make small through-

20 holes 3 in the conductive layer 4, in the vicinity of the installation areas of the components 6. The same through-holes 3 can also be used to align the components 6 and the insulating-material layer 1. There should preferably be at least two through-holes 3, for the alignment to be carried out accurately.

25 The components 6 are attached to the surface of the conductive layer 4 with the aid of an adhesive. For gluing, an adhesive layer 5 is spread on the attachment surface of the conductive layer 4, or on the attachment surface of the component 6, or on both. Thus, a first layer of adhesive can be formed on the surface of the component 6 and a second layer of adhesive can be formed on the surface of the conductive layer 4. After this, the

30 components 6 can be aligned to the positions planned for the components 6, with the aid of alignment holes 3, or other alignment marks. Alternatively, it is possible to proceed by first gluing the components to the conductive layer 4, positioned relative to each other, and after this making the alignment marks aligned relative to the components. The term

attachment surface of the component 6 refers to that surface, which faces the conductive layer 4. The attachment surface of the component 6 includes the contact zones, by means of which an electrical contact can be formed with the component. Thus, the contact zones can be, for example, flat areas on the surface of the component 6, or more usually contact
 5 protrusions protruding from the surface of the component 6. There are generally at least two contact zones or protrusions in the component 6. In complex microcircuits, there can be a greater number of contact zones.

10 In many embodiments, it is preferable to spread so much adhesive on the attachment surface, or attachment surfaces, that the adhesive entirely fills the space remaining between the components 6 and the conductive layer 4. A separate filler is then not required. The filling of the space between the components 6 and the conductive layer 4 reinforces the mechanical connection between the component 6 and the conductive layer 4, thus achieving a structure that is mechanically more durable. The comprehensive and
 15 unbroken adhesive layer also supports the conductive patterns 14 to be formed later from the conducting layer 4 and protects the structure during later process stages.

The term adhesive refers to a material, by means of which the components can be attached to the conductive layer. One property of the adhesive is that the adhesive can be
 20 spread on the surface of the conductive layer, and/or of the component in a relatively fluid form, or otherwise in a form that will conform to the shape of the surface. Another property of the adhesive is that, after spreading, the adhesive hardens, or can be hardened, at least partly, so that the adhesive will be able to hold the component in place (relative to the conductive layer), at least until the component is secured to the structure
 25 in some other manner. A third property of the adhesive is its adhesive ability, i.e. its ability to stick to the surface being glued.

The term gluing refers to the attachment of the component and conductive layer to each other with the aid of an adhesive. Thus, in gluing, an adhesive is brought between the
 30 component and the conductive layer and the component is placed in a suitable position relative to the conductive layer, in which the adhesive is in contact with the component and the conductive layer and at least partly fills the space between the component and the conductive layer. After this, the adhesive is allowed (at least partly) to harden, or the

adhesive is actively hardened (at least partly), so that the component sticks to the conductive layer with the aid of the adhesive. In some embodiments, the contact protrusions of the component may, during gluing, extend through the adhesive layer to make contact with the conductive layer.

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The adhesive used in the embodiments is typically a thermally hardening epoxy, for example an NCA (non-conductive adhesive). The adhesive is selected to ensure that the adhesive used will have sufficient adhesion to the conductive film, the circuit board, and the component. One preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material during the process. The adhesive selected should also preferably have a short hardening time, preferably of a few seconds at most. Within this time, the adhesive should harden at least partly, to such an extent that the adhesive is able to hold the component in position. Final hardening can take clearly more time and the final hardening can be planned to take place in connection with later process stages. The adhesive should also withstand the process temperatures used, for example, heating to a temperature in the range 100 - 265 °C a few times, and other stresses in the manufacturing process, for example, chemical and mechanical stress. The electrical conductivity of the adhesive is preferably in the same order as that of the insulating materials.

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In an embodiment using a first layer of adhesive formed on the surface of the component 6 and a second layer of adhesive formed on the surface of the conductive layer 4, the compositions of the adhesive in the first layer and second layer may be different to each other. Of course, it is also possible that the adhesive is the same in both of the adhesive layers.

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In an embodiment using two layers of adhesive it is possible to select the first adhesive such that it has a good adhesion to the surface of the component 6 and the second adhesive such that it has a good adhesion to the surface of the conductive layer 4. It is also possible to select the adhesives based on their other properties such as spreading properties, thermal conductivity, thermal expansion coefficient, mechanical strength, price etc. Therefore, using two different layers of adhesive having two different

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compositions may help in achieving the desired properties of the hardened adhesive between the component and the conductor-layer. It is also possible that one of the adhesives is applied in the form of an adhesive sheet and the other is spread in fluid form. Of course, both of the adhesives can be applied in any suitable form, including adhesive
 5 sheet and paste or liquid.

It is also possible that the first and second layers of adhesive are different in size and thickness. For example, the surface area of the second adhesive layer can be greater than the surface area of the first adhesive layer. The second adhesive layer can even extend to
 10 the sides of module. Thus, the surface area of the second adhesive layer can be as great as the surface area of the whole module. The first adhesive layer is preferably local and present only at the location of the component. Of course, also the second adhesive layer can be local as well.

15 A suitable insulating-material layer 1 is selected as the base material of the electronic module, for example, the circuit board. Using a suitable method, recesses, or through-holes are made in the insulating-material layer 1, according to the size and mutual positions of the components 6 to be attached to the conductive layer 4. The recesses or through-holes can also be made to be slightly larger than the components 6, in which
 20 case the alignment of the insulating layer 1 relative to the conductive layer 4 will not be so critical. If an insulating-material layer 1, in which through-holes are made for the components 6, is used in the process, certain advantages can be achieved by using, in addition, a separate insulating-material layer 11, in which holes are not made. Such an insulating-material layer 11 can be located on top of the insulating-material layer 1 to
 25 cover the through-holes made for the components.

If it is desired to make a second conductive layer in the electronic module, this can be made, for example, on the surface of the insulating-material layer 1. In embodiments, in which a second conductive layer 11 is used, the conductive layer can be made on the
 30 surface of this second conductive layer 11. If desired, conductive patterns 19 can be made from a second conductive layer 9. The conductive layer 9 can be made, for example, in a corresponding manner to the conductive film 4. The manufacture of a second conductive film 9 is not, however, necessary in simple embodiments and when

manufacturing simple electronic modules. A second conductive film 9 can, however, be exploited in many ways, such as additional space for conductive patterns and to protect the components 6 and the entire module against electromagnetic radiation (EMC shielding). With the aid of a second conductive film 9 the structure can be reinforced and warping of the installation base, for example, can be reduced.

Feed-throughs, through which electrical contacts can be formed between the contact zones of the components 6 and the conductive layer 4, are made in the electronic module. Holes 17 are made in the conductive layer 4 for the feed-throughs, at the positions of the contact zones (in the figures, the contact protrusions 7) of the components 6. Holes 3, or other available alignment marks can be utilized in the alignment. The holes 17 are made in such a way that they also penetrate through the adhesive layer that has been left on top of the contact zones, or contact protrusions 7. The holes 17 thus extend to the material of the contact protrusions 7 or other contact zones. The holes 17 can be made, for example, by drilling with a laser device, or by using some other suitable method. After this, conductive material is introduced to the hole 17, so that an electrical contact is formed between the components 6 and the conductive layer 4.

The manufacturing processes according to the examples can be implemented using manufacturing methods, which are generally known to those versed in the art of manufacturing circuit boards.

In the following, the stages of the method shown in Figures 1 - 8 are examined in greater detail.

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Stage A (Figure1):

In stage A, a suitable conductive layer 4 is selected as the initial material of the process. A layered sheet, in which the conductive layer 4 is located on the surface of a support base 12, can also be selected as the initial material. The layered sheet can be manufactured, for example, in such a way that a suitable support base 12 is taken for processing, and a suitable conductive film for forming the conductive layer 4 is attached to the surface of this support base 12.

The support base 12 can be made of, for example, an electrically conductive material, such as aluminium (Al), or an insulating material, such as polymer. The conductive layer 4 can be formed, for example, by attaching a thin metal film to the second surface of the support base 12, for example, by laminating it from copper (Cu). The metal film can be
 5 attached to the support base, for example, using an adhesive layer, which is spread on the surface of the support base 12 or metal film prior to the lamination of the metal layer. At this stage, there need not be any patterns in the metal film.

In the example of Figure 1, holes 3 are made penetrating the support base 12 and the
 10 conductive layer 4, for alignment during the installation and connection of the components 6. Two through-holes 3, for example, can be manufactured for each component 6 to be installed. The holes 3 can be made using some suitable method, for example, mechanically by milling, impact, drilling, or with the aid of a laser. However, it is not essential to make through-holes 3, instead some other suitable alignment markings
 15 can be used to align the components. In the embodiment shown in Figure 1, the through-holes 3 used to align the components extend through both the support base 12 and the conductive film 4. This has the advantage that the same alignment marks (through-holes 3) can be used for aligning on both sides of the installation base.

20 Stage A can also be performed in the same way in embodiments in which a self-supporting conductive layer 4 is used and from which thus totally lacks a support layer 12.

Stage B (Figure 2):

25 In stage B, an adhesive layer 5 is spread on those areas of the conductive layer 4, to which the components 6 will be attached. These areas can be termed attachment areas. The adhesive layers 5 can be aligned, for example, with the aid of the through-holes 3. The thickness of the adhesive layer is selected so that the adhesive suitably fills the space
 30 between the component 6 and the conductive layer 4, when the component 6 is pressed onto the adhesive layer 5. If the component 6 includes contact protrusions 7, it would be good for the thickness of the adhesive layer 5 to be greater, for example about 1.5 - 10 times, the height of the contact protrusions 7, so that the space between the component 6

and the conductive layer 4 will be properly filled. The surface area of the adhesive layer 5 formed for the component 6 can also be slightly larger than the corresponding surface area of the component 6, which will also help to avoid the risk of inadequate filling.

- 5 Stage B can be modified in such a way that the adhesive layer 5 is spread on the attachment surfaces of the components 6, instead of on the attachment areas of the conductive layer 4. This can be carried out, for example, by dipping the component in adhesive, prior to setting it in place in electronic module. It is also possible to proceed by spreading the adhesive on both the attachment areas of the conductive layer 4 and on the
10 attachment surfaces of the components 6. Such modifications are further described below with reference to Figures 12 to 14.

- The adhesive being used is thus a electrical insulator, so that electrical contacts are not formed in the actual adhesive layer 5, between the contact zones (contact protrusions 7 in
15 the example) of the component 6.

Stage C (Figure 3):

- In stage C, the component 6 is set in place in the electronic module. This can be done, for
20 example, by pressing the components 6 into the adhesive layer 5, with the aid of an assembly machine. In the assembly stage, the through-holes 3 made for alignment, or other available alignment marks, are used to align the components 6.

- The components 6 can be glued individually, or in suitable groups. The typical procedure
25 is for the conductive layer, which can be termed the bottom of the installation base, to be brought to a suitable position relative to the assembly machine, and after this the component 6 is aligned and pressed onto the bottom of the installation base, which is held stationary during the aligning and attaching.

Stage D (Figure 4):

In stage D, an insulating-material layer 1, in which there are pre-formed recesses 2 or recesses for the components 6 to be glued to the conductive layer 4, is placed on top of

the conductive layer 4. The insulating-material layer 1 can be made from a suitable polymer base, in which recesses or cavities according to the size and position of the components 6 are made using some suitable method. The polymer made can be, for example, a pre-preg base known and widely used in the circuit-board industry, which is made from a glass-fibre mat and so-called b-state epoxy. It is best to perform stage D only once the adhesive layer 5 has been hardened, or it has otherwise hardened sufficiently for the components 6 to remain in place during the placing of the insulating-material layer 1.

When manufacturing a very simple electronic module, the insulating-material layer 1 can be attached to the conductive layer 4 in connection with stage D and the process continued with the patterning of the conductive layer 4.

Stage E (Figure 5):

In stage E, an unpatterned insulating-material layer 11 is placed on top of the insulating-material layer 1 and on top of it a conductive layer 9. Like the insulating-material layer 1, the insulating-material layer 11 can be made from a suitable polymer film, for example, the aforesaid pre-preg base. The conductive layer 9 can, in turn, be, for example, a copper film, or some other film suitable for the purpose.

Stage F (Figure 6):

In stage F, the layers 1, 11, and 9 are pressed with the aid of heat and pressure in such a way that the polymer (in the layers 1 and 11) forms a unified and tight layer between the conductive layer 4 and 9 around the components 6. The use of this procedure makes the second conductive layer 9 quite smooth and even.

When manufacturing simple electronic modules and those including a single conductive-pattern layer 14, stage E can even be totally omitted, or the layers 1 and 11 can be laminated to the construction, without a conductive layer 9.

Stage G (Figure 7):

In stage G, the support base 12 is detached or otherwise removed from the construction. Removal can take place, for example, mechanically or by etching. Stage G can naturally be omitted from embodiments that do not employ a support base 12.

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Stage H (Figure 8):

In stage H, holes 17 are made for the feed-throughs. The holes 17 are made through the conductive layer 4 and the adhesive layer 5, in such a way that the material of the contact protrusions 7, or other contact zones of the components 6 is exposed. The holes 17 can be made, for example, by drilling with a laser. The holes 17 can be aligned, for example, with the aid of holes 3.

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Stage I (Figure 9):

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In stage I, conductive material 18 is grown into the holes 17 made in stage H. In the example process, the conductive material is grown at the same time also elsewhere on top of the base, so that the thickness of the conductive layers 4 and 9 also increases.

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The conductive material 18 being grown can be, for example, copper, or some other sufficiently electrically conductive material. The choice of conductive material 18 should take into account the ability of the material to form an electrical contact with the contact protrusions 7 of the component 6. In one example process, the conductive material is mainly copper. Copper-metallizing can be performed by surfacing the holes 17 with a thin layer of chemical copper and then continuing the surfacing using an electrochemical copper-growing method. Chemical copper is used, for example, because it also forms a surface on top of the adhesive and acts as an electrical conductor in electrochemical surfacing. The growth of the metal can thus be performed using a wet-chemical method, in which case the growing will be cheap.

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In the example process, the holes 17 of the feed-throughs are first cleaned using a three-stage desmear treatment. After this, the feed-throughs are metallized in such a way that an SnPd coating catalysing the polymer is first formed, after which a thin layer (about 2

μm) is deposited on the surface. The thickness of the copper is increased using electrochemical deposition.

Stage I is intended to form an electrical contact between the component 6 and the conductive layer 4. In stage I, it is therefore not essential to increase the thickness of the conductive layers 4 and 9, instead the process can equally well be planned in such a way that in stage I the holes 17 are only filled with a suitable material. The conductive layer 18 can be made, for example, by filling the holes 17 with an electrically conductive paste, or by using some other metallizing method suitable for micro-vias.

In the later figures, the conductive layer 18 is shown with the conductive layers 4 and 9 merged.

Stage J (Figure 10):

In stage J, the desired conductive patterns 14 and 19 are formed from the conductive layers 4 and 9 on the surface of the base. If only a single conductive layer 4 is used in the embodiment, the patterns are formed on only one side of the base. It is also possible to proceed in such a way that the conductive patterns are only formed from the conductive layer 4, even though a second layer 9 is also used in the embodiment. In such an embodiment, the unpatterned conductive layer 9 can act, for example, as a mechanically supporting or protective layer of the electronic module, or as a protection against electromagnetic radiation.

The conductive patterns 14 can be made, for instance, by removing the conductive material of the conductive layer 4 from outside of the conductive patterns. The conductive material can be removed, for example, using one of the patterning and etching methods that are widely used and well known in the circuit-board industry.

After stage J, the electronic module includes a component 6, or several components 6 and conductive patterns 14 and 19 (in some embodiments only conductive patterns 14), with the aid of which the component or components 6 can be connected to an external circuit, or to each other. The conditions for manufacturing a functional totality then exist already.

The process can thus be designed in such a way that the electronic module is already finished after stage J and figure 10 shows one example of a possible electronic module that can be manufactured using the example methods. If it is wished, the process can also continue after stage J, for example, by surfacing the electronic module with a protective substance, or by making additional conductive patterns on the first and/or second surface of the electronic module.

Figure 11

Figure 11 shows a multi-layered electronic module, which includes three bases 1 laminated on top of each other, together with their components 6, and a total of six conductive-pattern layers 14 and 19. The bases 1 are attached to each other with the aid of intermediate layers 32. The intermediate layer 32 can be, for example, a pre-preg epoxy layer, which is laminated between the installation bases 1. After this, holes running through the module are drilled in the electronic module, in order to form contacts. The contacts are formed with the aid of a conductive layer 31 grown in the holes. With the aid of the conductors 31 running through the electronic module, the various conductive-pattern layers 14 and 19 of the installation bases 1 can be suitably connected to each other, thus forming a multi-layered functioning totality.

On the basis of the example of Figure 11, it is clear that the method can also be used to manufacture many different kinds of three-dimensional circuit structures. The method can be used, for example, in such a way that several memory circuits are placed on top of each other, thus forming a package containing several memory circuits, in which the memory circuits are connected to each other to form a single functional totality. Such packages can be termed three-dimensional multichip modules. In modules of this kind, the chips can be selected freely and the contacts between the various chips can be easily manufactured according to the selected circuits.

The sub-modules (bases 1 with their components 6 and conductors 14 and 19) of a multi-layered electronic module can be manufactured, for example, using one of the electronic-module manufacturing methods described above. Some of the sub-modules to be connection to the layered construction can, of course, be quite as easily manufactured

using some other method suitable for the purpose.

Figures 12 to 14 show embodiments wherein the adhesive 5 is divided into two different layers, a first adhesive layer 51 and a second adhesive layer 52. According to Figure 12, the first adhesive layer 51 is applied on the surface of the component 6 and the second adhesive layer 52 is applied on the surface of the conductor layer 4. After this, the process is continued for example as described above, and the resultant electronic module is shown in Figure 13. In the embodiment of Figure 12, the second adhesive layer 52 covers the whole surface of the conductor layer 4, and therefore also the surface of all the conductors 14 in the resultant module of Figure 13. Figure 14 shows an electronic module, wherein the second adhesive layer 52 is local. The thickness of the first adhesive layer 51 can be for example 10–30 micrometers, such as 15–20 micrometers. The thickness of the second adhesive layer 51 can be for example 5–20 micrometers, such as 10–15 micrometers. Of course, other thicknesses can also be used when appropriate.

The examples of Figures 1–14 show some possible processes, with the aid of which our invention can be exploited. Our invention is not, however, restricted to only the processes disclosed above, but instead the invention also encompasses various other processes and their end products, taking into account the full scope of the Claims and the interpretation of their equivalences. The invention is also not restricted to only the constructions and method described by the examples, it being instead obvious to one versed in the art that various applications of our invention can be used to manufacture a wide range of different electronic modules and circuit boards, which differ greatly from the examples described above. Thus, the components and wiring of the figures are shown only with the intention of illustrating the manufacturing process. Thus many alterations to and deviations from the processes of the examples shown above can be made, while nevertheless remaining within the basic idea according to the invention. The alterations can relate, for example, to the manufacturing techniques described in the different stages, or to the mutual sequence of the process stages.

With the aid of the method, it is also possible to manufacture component packages for connection to a circuit board. Such packages can also include several components that are connected electrically to each other.

The method can also be used to manufacture total electrical modules. The module can also be a circuit board, to the outer surface of which components can be attached, in the same way as to a conventional circuit board.

Claims:

1. An electronic module, comprising:
 - a conductive-pattern layer;
 - 5 at least one component comprising contact zones facing the conductive-pattern layer;
 - a hardened adhesive between the component and the conductive-pattern layer, the hardened adhesive comprising a first hardened adhesive layer in contact with the component and a second hardened adhesive layer in contact with the conductive-pattern
 - 10 layer;
 - conductive-material formations penetrating the hardened adhesive between the conductive-pattern layer and the contact zones of the component; and
 - an insulating-material layer around the component on the conductive-pattern layer and conforming to the shape of the component.
 - 15
2. The electronic module of claim 1, wherein the first hardened adhesive layer is in contact with the second hardened adhesive layer.
3. The electronic module of claim 2, wherein the second hardened adhesive layer has a
 - 20 first area in contact with the first hardened adhesive layer and a second area around the first area in contact with the insulating-material layer.
4. The electronic module of claim 1, wherein
 - the at least one component comprises at least one semiconductor component;
 - 25 the semiconductor component has a first surface facing the conductive-pattern layer;
 - the contact zones are located on the first surface; and
 - the first surface is against the first hardened adhesive layer.
- 30 5. The electronic module of claim 4, wherein the first hardened adhesive layer covers the first surface outside the contact zones.
6. The electronic module of claim 4, wherein a surface area of the first hardened adhesive

layer is equal to a surface area of the first surface of the component.

7. The electronic module of claim 6, wherein a surface area of the second hardened adhesive layer is greater than the surface area of the first hardened adhesive layer.

5

8. An electronic module, comprising:

a conductive-pattern layer;

an insulating-material layer supporting the conductive-pattern layer;

at least one component inside the insulating-material layer, the at least one

10 component comprising a first surface and contact zones on the first surface;

a first hardened adhesive layer on the first surface of the at least one component;

a second hardened adhesive layer in contact with the conductive-pattern layer and the first hardened adhesive layer;

holes in the first and second hardened adhesive layer at the locations of the

15 contact zones; and

conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer.

9. The electronic module of claim 8, wherein the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition.

20

10. The electronic module of claim 8, wherein the first hardened adhesive layer and the second hardened adhesive layer have a common composition.

25

11. The electronic module of claim 9, wherein the second hardened adhesive layer covers the conductive-pattern layer such that the insulating-material layer supports the conductive-pattern layer via said second hardened adhesive layer.

30

12. The electronic module of claim 8, wherein the first and second hardened adhesive layers are local and present at the location of the component such that the insulating-material layer directly supports the conductive-pattern layer.

13. An electronic module, comprising:
- at least one semiconductor component comprising a first surface and a set of contact zones on the first surface;
 - a first hardened adhesive layer on the first surface;
 - 5 a second hardened adhesive layer at least on the first hardened adhesive layer;
 - contact elements made of metal on the set of contact zones, the contact elements extending through the first and second hardened adhesive layers;
 - conductors in contact with the contact elements and forming a conductive-pattern layer; and
 - 10 an insulating-material layer around the at least one semiconductor component.
14. The electronic module of claim 13, wherein the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition.
- 15
15. The electronic module of claim 13, wherein the first hardened adhesive layer and the second hardened adhesive layer have a common composition.
16. The electronic module of claim 13, wherein the at least one semiconductor
- 20 component comprises at least one microcircuit.
17. The electronic module of claim 13, wherein the area of the first hardened adhesive layer is equal to the area of the first surface of the at least one semiconductor component.
- 25
18. The electronic module of claim 13, wherein the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer.
19. The electronic module of claim 13, wherein the contact elements comprise a first layer of metal and at least one second layer of metal.
- 30
20. The electronic module of claim 13, wherein the contact elements are in metallurgical contact with the respective contact zones and the respective conductors.

Abstract:

An electronic module, comprising: a conductive-pattern layer; an insulating-material layer supporting the conductive-pattern layer; at least one component inside the insulating-material layer, the at least one component comprising a first surface and contact zones on the first surface; a first hardened adhesive layer on the first surface of the at least one component; a second hardened adhesive layer in contact with the conductive-pattern layer and the first hardened adhesive layer; holes in the first and second hardened adhesive layer at the locations of the contact zones; and conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer.

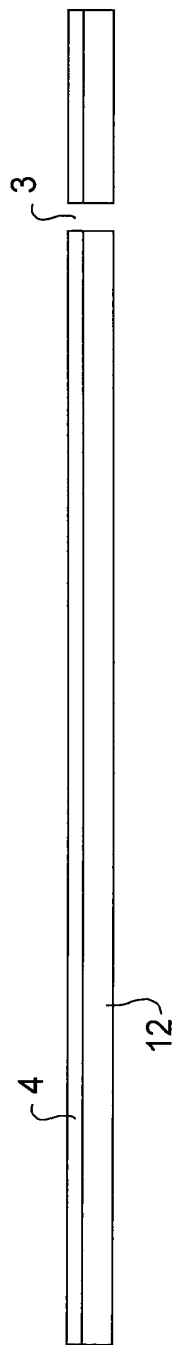


Fig. 1

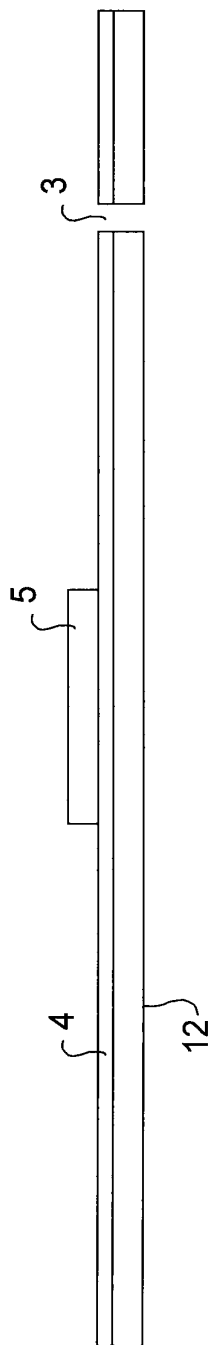


Fig. 2

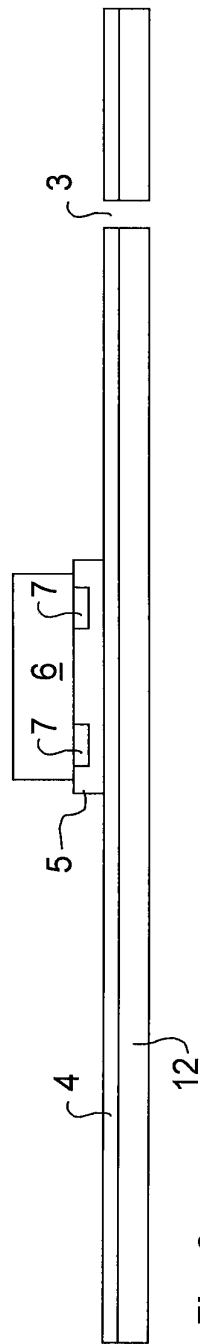


Fig. 3

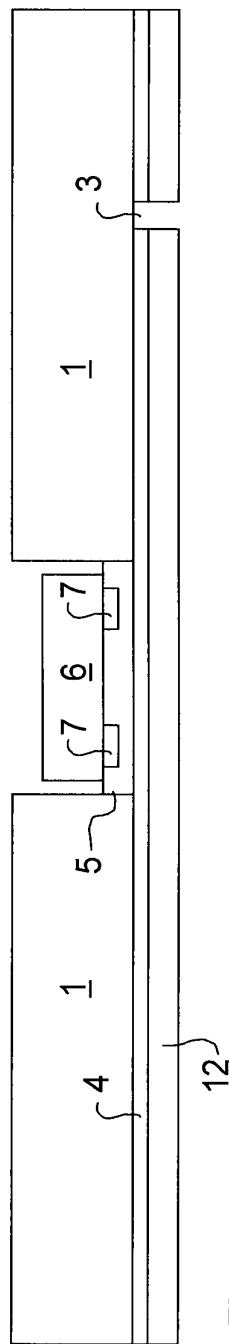


Fig. 4

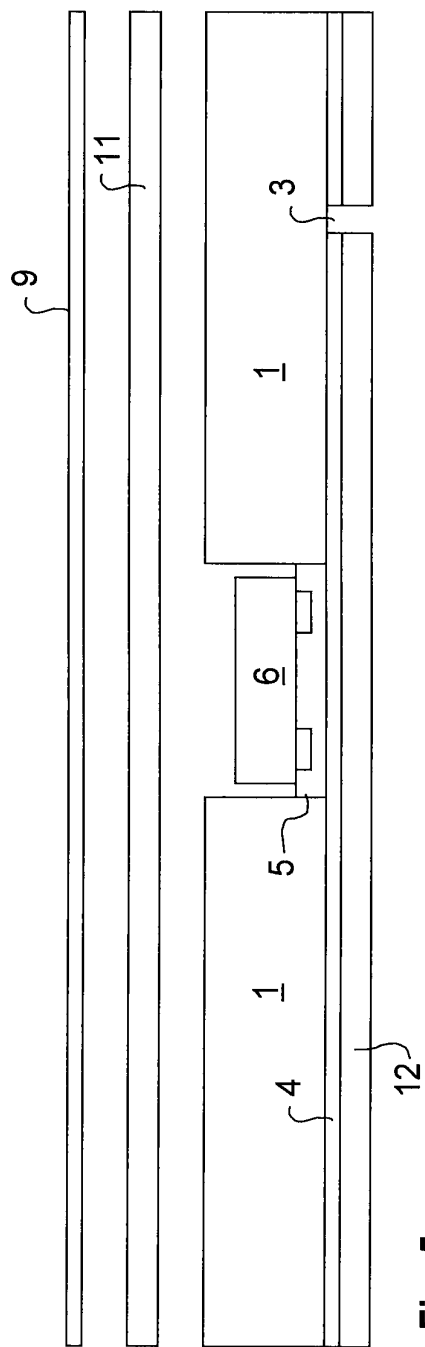


Fig. 5

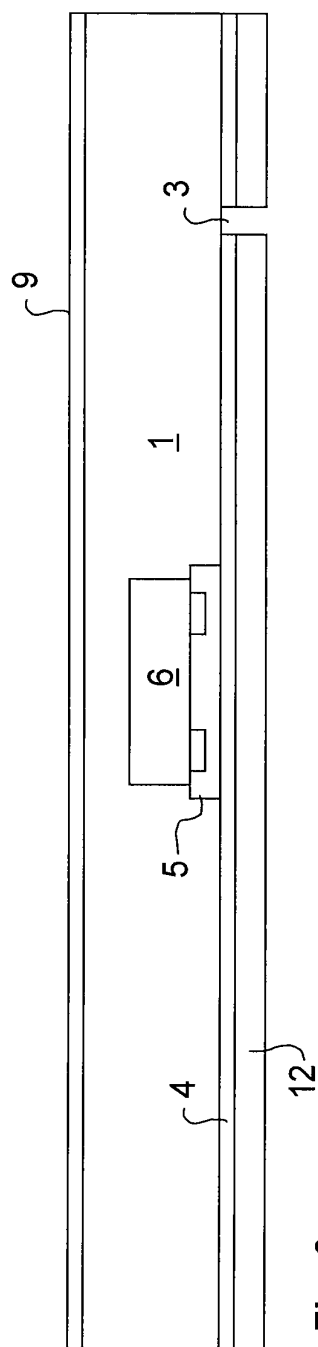


Fig. 6

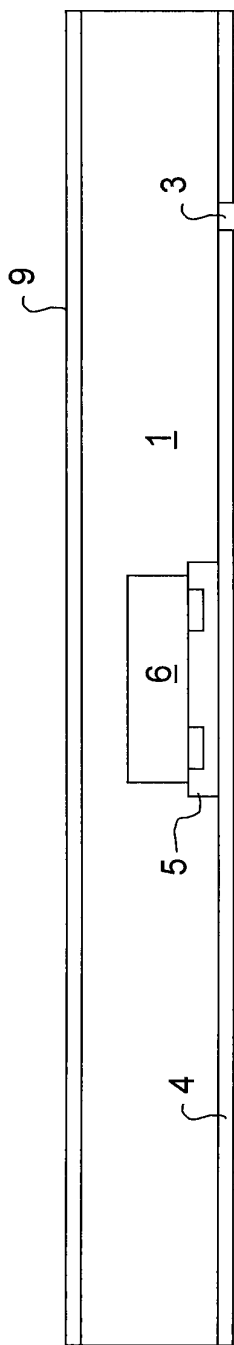


Fig. 7

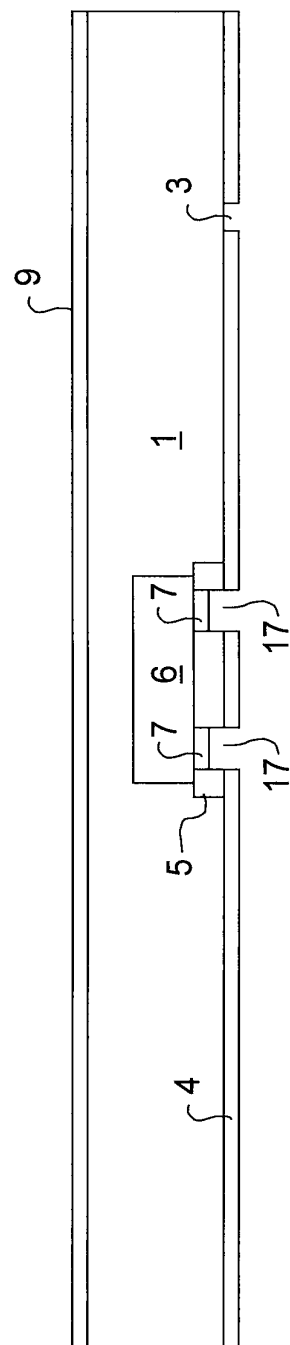


Fig. 8

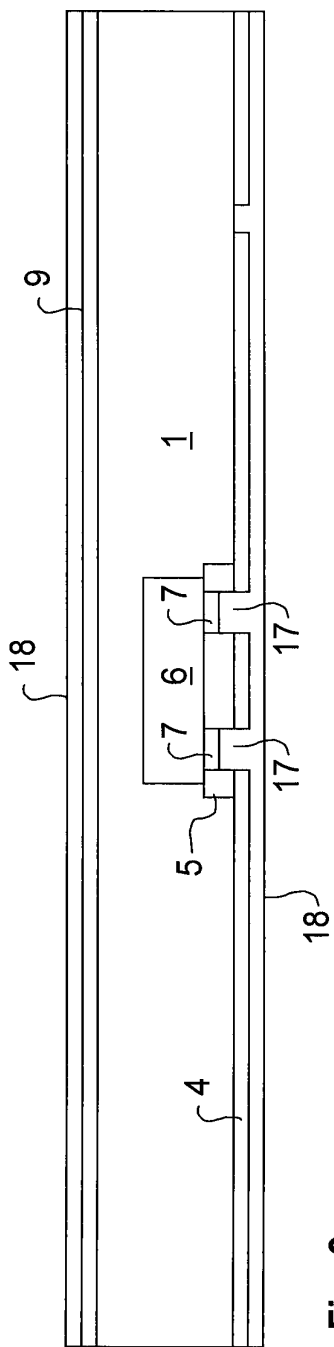


Fig. 9

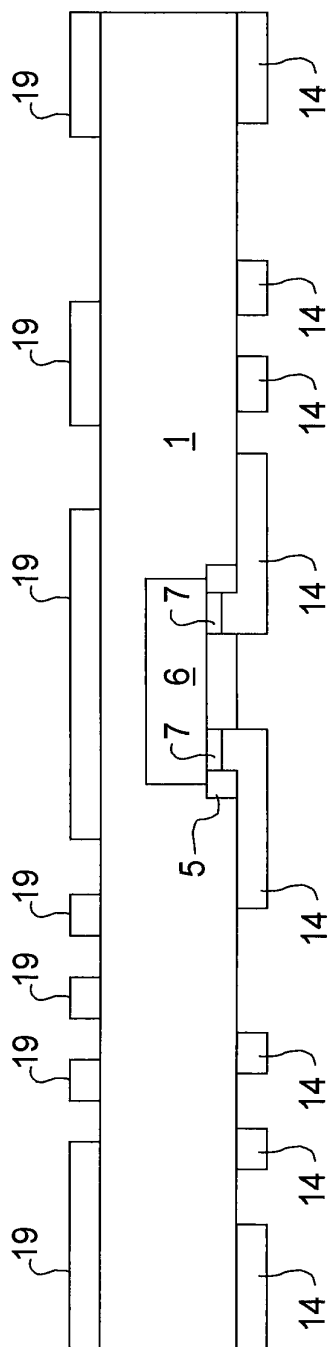


Fig. 10

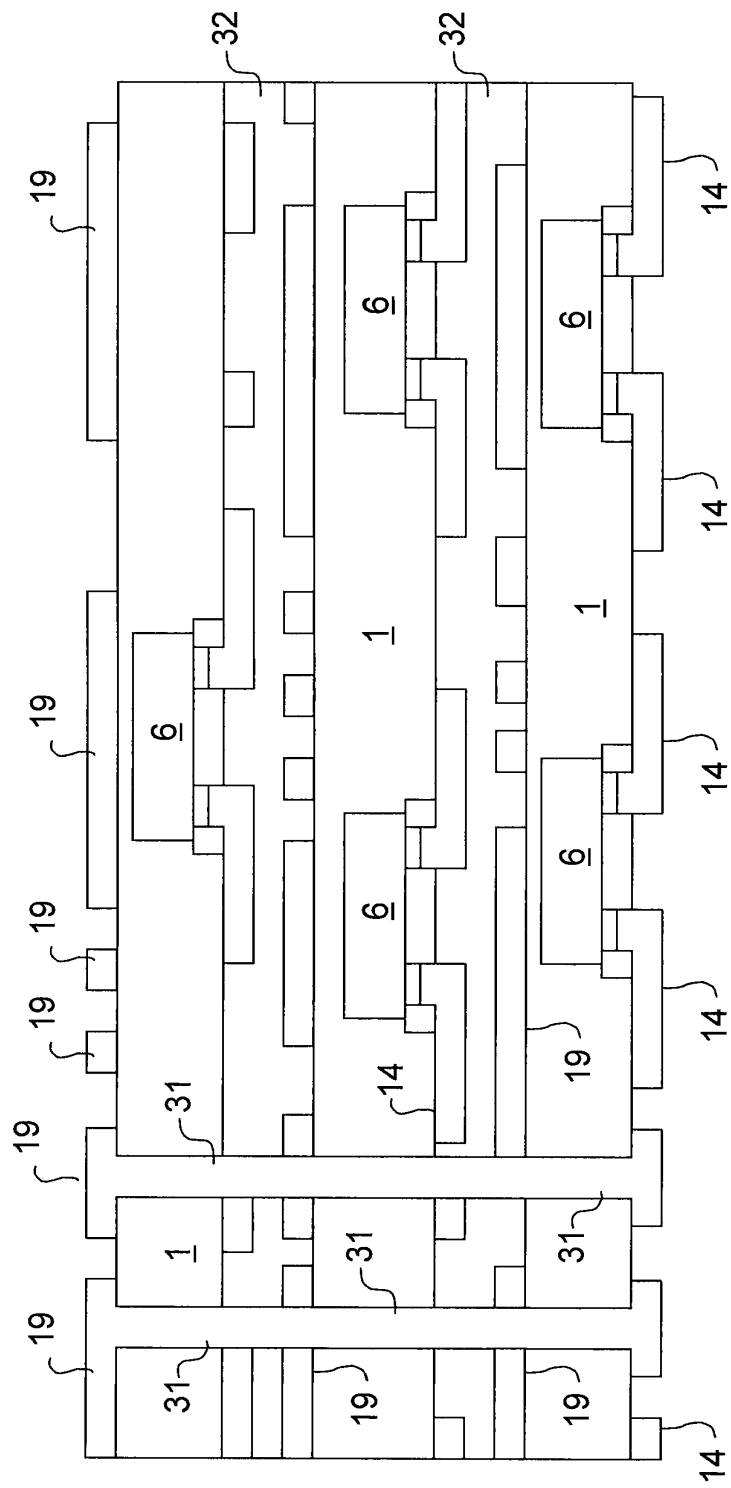


Fig. 11

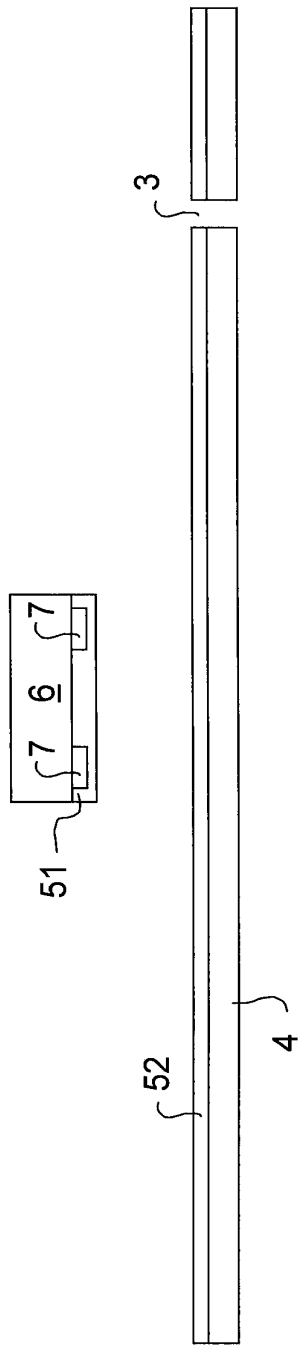


Fig. 12

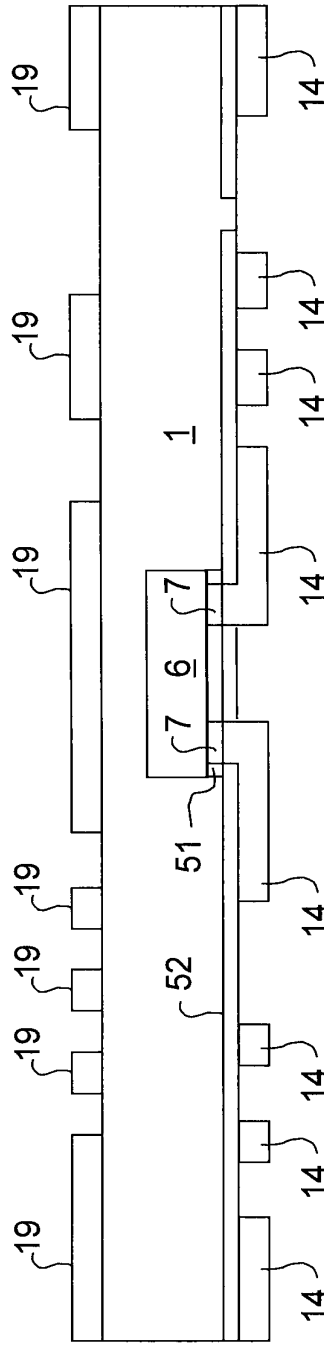


Fig. 13

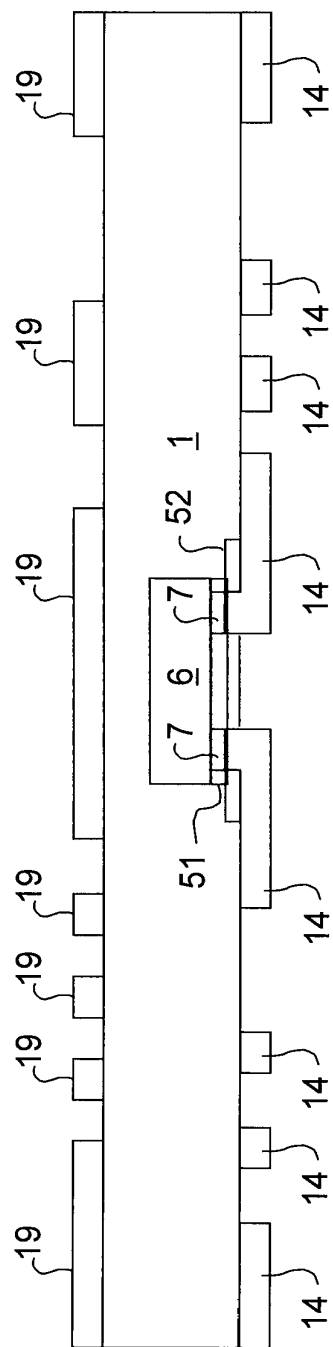


Fig. 14

Electronic Acknowledgement Receipt	
EFS ID:	6943561
Application Number:	12699628
International Application Number:	
Confirmation Number:	6266
Title of Invention:	AN ELECTRIC MODULE
First Named Inventor/Applicant Name:	Risto TUOMINEN
Customer Number:	02292
Filer:	Michael Keith Mutter/Hannah White
Filer Authorized By:	Michael Keith Mutter
Attorney Docket Number:	0365-0652PUS3
Receipt Date:	03-FEB-2010
Filing Date:	
Time Stamp:	17:25:19
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20100203_CIPAPPLICATION.pdf	1737625 25b73bc5e9f426f4dcf6608ee8c047f4a6211c57	yes	46

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal of New Application	1	1
	Miscellaneous Incoming Letter	2	2
	Application Data Sheet	3	5
	Transmittal Letter	6	9
	Information Disclosure Statement (IDS) Filed (SB/08)	10	11
	Preliminary Amendment	12	12
	Specification	13	13
	Applicant Arguments/Remarks Made in an Amendment	14	14
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	Claims	35	37
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