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Issue Date: July 17, 2012
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Title: ELECTRIC MODULE HAVING A CONDUCTIVE PATTERN
LAYER

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 8,222,723 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 8,222,723
APPLE-1002	U.S. Patent No. 8,222,723 File History
APPLE-1003	Declaration of Dr. Dean Neikirk
APPLE-1004	U.S. Patent Application Publication No. 2006/0278967 ("Tuominen967Pub")
APPLE-1005	U.S. Patent No. 6,335,571 ("Capote")
APPLE-1006	PCT Publication No. WO 00/09623 ("Watanabe")
APPLE-1007	Certified Translation of PCT Publication No. WO 00/09623 ("Watanabe")
APPLE-1008	RESERVED
APPLE-1009	RESERVED
APPLE-1010	U.S. Patent Application Publication No. 2001/0030059 ("Sugaya")
APPLE-1011	U.S. Patent Application Publication No. 2002/0175402 ("McCormack")
APPLE-1012	U.S. Patent No. 6,489,685 ("Asahi")
APPLE-1013	U.S. Patent No. 4,179,802 ("Joshi")

LISTING OF CLAIMS

Claim 1	
[1 Pre]	An electronic module, comprising:
[1a]	a conductive-pattern layer;
[1b]	an insulating-material layer supporting the conductive-pattern layer;
[1c]	at least one component inside the insulating-material layer, the at least one component comprising a first surface and contact zones on the first surface;
[1d]	a first hardened adhesive layer on the first surface of the at least one component;
[1e]	a second hardened adhesive layer in contact with the conductive-pattern layer and the first hardened adhesive layer;
[1f]	holes in the first and second hardened adhesive layer at the locations of the contact zones; and
[1g]	conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer,
[1h]	wherein the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition.
Claim 2	
[2]	The electronic module of claim 1, wherein the second hardened adhesive layer covers the conductive-pattern layer such that the insulating-material layer supports the conductive-pattern layer via said second hardened adhesive layer.

Claim 3	
[3]	The electronic module of claim 1, wherein the first and second hardened adhesive layers are local and present at the location of the component such that the insulating-material layer directly supports the conductive-pattern layer.
Claim 4	
[4 Pre]	An electronic module, comprising:
[4a]	at least one semiconductor component comprising a first surface and a set of contact zones on the first surface;
[4b]	a first hardened adhesive layer on the first surface;
[4c]	a second hardened adhesive layer at least on the first hardened adhesive layer;
[4d]	contact elements made of metal on the set of contact zones, the contact elements extending through the first and second hardened adhesive layers;
[4e]	conductors in contact with the contact elements and forming a conductive-pattern layer; and
[4f]	an insulating-material layer around the at least one semiconductor component,
[4g]	wherein the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition.
Claim 5	
[5]	The electronic module of claim 4, wherein the at least one semiconductor component comprises at least one microcircuit.

Claim 6	
[6]	The electronic module of claim 4, wherein the area of the first hardened adhesive layer is equal to the area of the first surface of the at least one semiconductor component.
Claim 7	
[7]	The electronic module of claim 4, wherein the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer.
Claim 8	
[8]	The electronic module of claim 4, wherein the contact elements comprise a first layer of metal and at least one second layer of metal.
Claim 9	
[9]	The electronic module of claim 4, wherein the contact elements are in metallurgical contact with the respective contact zones and the respective conductors.

I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for IPR of claims 1-9 (“Challenged Claims”) of U.S. Patent No. 8,222,723 (“the ’723 patent”).

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR based on the following grounds, as further explained in this Petition and supported by the Declaration of Dr. Dean Neikirk (APPLE-1003).

Ground	Patent Claims	Basis
1A	1-9	§103 – Tuominen967Pub-Capote
1B	1-9	§103 – Tuominen967Pub
2	1-9	§103 – Asahi-Capote

The ’723 Patent was filed on Feb. 3, 2010, and is a Continuation-In-Part (CIP) of U.S. application No. 10/550,023 (the ’023 Application), filed on Sep. 23, 2005, which is the National Stage application of PCT International Application No. PCT/FI2004/000195 (the PCT Application), filed on Mar. 31, 2004, which claims priority to Finish Patent Application No. 20030493 (the Finnish Application), filed on Apr. 1, 2003. APPLE-1001, 1:7-12. As discussed below in Section III.C., the

'723 patent is not entitled to a priority date any earlier than its filing date of February 3, 2010, because all claims are limited to new matter described first in the CIP. Tuominen967Pub is thus prior art under § 102(b).

Capote and Asahi are prior art regardless of whether the '723 Patent's earliest possible priority date (Apr. 1, 2003) or the actual filing date (February 3, 2010, *infra* § III.C) is applied.

Reference	Date	Prior Art Under
Tuominen967Pub (APPLE-1004)	Dec. 14, 2006 (Published)	Pre-AIA § 102(b)
Capote (APPLE-1005)	Jan. 1, 2002 (Issued)	Pre-AIA § 102(b)
Asahi (APPLE-1012)	Dec. 3, 2002 (Issued)	Pre-AIA § 102(a)/(b)

None of the above references were applied in a rejection during prosecution.

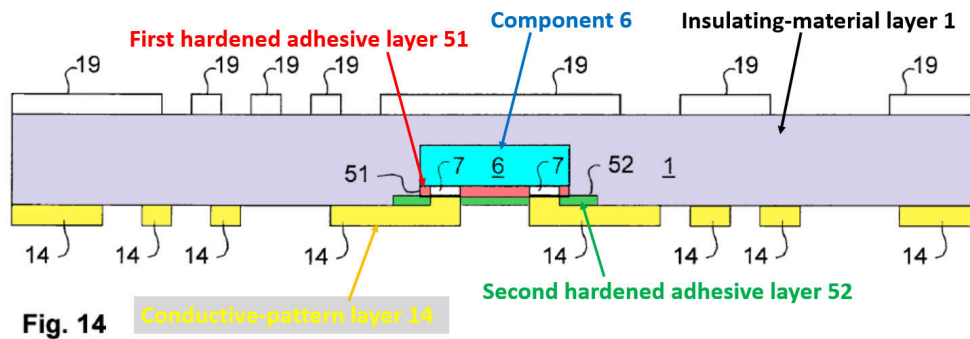
III. SUMMARY OF THE '723 PATENT

A. Brief Description

The '723 patent relates to an “electronic module.” APPLE-1001, Abstract, 1:18. In particular, the '723 patent describes “one or more components embedded in an installation base.” APPLE-1001, 1:19-21. The electronic module recited by the claims includes a conductive-pattern layer 14; an insulating-material layer 1; at least one component 6 inside the insulating-material layer and having a first surface and contact zones on the first surface; a first hardened adhesive layer 51 on the first surface of the component; and a second hardened adhesive layer 52 in

contact with the conductive-pattern layer and the first hardened adhesive layer.

APPLE-1001, Abstract, Cls. 1, 4, FIGS. 12-14. The electronic module further includes holes in the first and second hardened adhesive layers at the locations of the contact zones, with conductive material in the holes electrically connecting the contact zones of the component and the conductive-pattern layer. *Id.* The first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition. APPLE-1001, 7:14-30, cls. 1, 4.



APPLE-1003, ¶38 (APPLE-1001, FIG. 14 (Annotated))

According to the '723 patent, “using two different layers of adhesive having two different compositions may help in achieving the desired properties of the hardened adhesive between the component and the conductor-layer,” such that the first adhesive “has a good adhesion to the surface of the component 6” and the second adhesive “has a good adhesion to the surface of the conductive layer 4 [from which conductive-patterns 14 are formed].” APPLE-1001, 6:31-32, 7:14-30,

10:32-37 (conductive layer 4 thickened by growing “conductive material 18”).

While the ’723 patent touts these routine aspects as “invention,” they were not innovative. Those of skills in the art were aware of the use of two different adhesive layers, in combination with the other recitations of the claims, to achieve known benefits. APPLE-1003, ¶¶38-39; *infra*, § VI.

B. Summary of the Prosecution History of the ’723 Patent

The ’723 Patent issued on July 17, 2012 from a continuation-in-part filed on February 3, 2010. *See* APPLE-1002.

During prosecution, only a single office action was issued, rejecting pending claims 1-8, 10, 13, and 15-20 under 35 U.S.C. § 103(a) as unpatentable over Mowatt et al. (U.S. Patent No. 5,306,670). APPLE-1002, 46-57. The examiner indicated that claims 9, 11, 12 and 14 would be allowable if rewritten in independent form including all limitations of their respective base and intervening claims. *Id.*, 55. The reason for allowance regarding claims 9 and 14 stated, “the prior art of record fails to show or collectively teach **the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition**[.]” *Id.*, 56¹.

In response to this office action, applicant canceled pending claims 1-8, 10,

¹ All emphasis added unless otherwise noted.

13 and 15, and rewrote claims 9 and 14 as independent claims. *Id.*, 37-38. A notice of allowance followed, ending prosecution prematurely and without application of the more pertinent prior art such as Tuominen967Pub, Capote, and Asahi. *Id.*, 24-28. Although the '723 Patent claims priority as CIP to Tuominen967Pub (publication of the '023 Application), Tuominen967Pub is prior art under pre-AIA 35 U.S.C. § 102(b). *Infra*, § III.C. Tuominen967Pub was not applied as such in the prosecution history. APPLE-1002, 46-57. APPLE-1003, ¶¶40-42.

C. Priority Date

The '723 patent is not entitled to its alleged priority date of April 1, 2003, because the independent claims 1 and 4 recite new matter first described in the continuation-in-part application filed Feb. 3, 2010. In particular, the claims of the '723 patent recite that “the first hardened adhesive layer has a first composition and the second hardened adhesive layer has *a second composition different from the first composition.*” This limitation is not supported by the '023 Application, the PCT Application, or the Finnish Application. APPLE-1002, 108-109, 120-121; APPLE-1001, 7:14-30, Cls. 1, 4; APPLE-1003, ¶43.

Tuominen967Pub describes spreading adhesive “on both” the attachment surface of the conductive layer and on the attachment surface of the component. APPLE-1004, [0036]. Tuominen967Pub does not, however, describe the relative composition of the potential two adhesive layers. APPLE-1004, [0036]-[0040].

Tuominen⁹⁶⁷Pub points out that “[t]he adhesive is selected to ensure that the adhesive used will have sufficient adhesion to the conductive film, the circuit board, and the component[,]” and that “[o]ne preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material during the process.” *Id.*, [0040].

In contrast, the CIP, filed on February 3, 2010, adds the following paragraphs *for the first time*:

In an embodiment using a first layer of adhesive formed on the surface of the component 6 and a second layer of adhesive formed on the surface of the conductive layer 4, the **compositions of the adhesive in the first layer and second layer may be different to each other**. Of course, it is also possible that the adhesive is the same in both of the adhesive layers.

In an embodiment using two layers of adhesive it is possible to select the first adhesive such that it has a good adhesion to the surface of the component 6 and the second adhesive such that it has a good adhesion to the surface of the conductive layer 4. It is also possible to select the adhesives based on their other properties such as spreading properties, thermal conductivity, thermal expansion coefficient, mechanical strength, price etc. Therefore, **using two different layers of adhesive having two different compositions** may help in achieving the desired properties of the hardened adhesive between the component and the conductor-layer. It is also possible that one of the adhesives is applied in the form of an adhesive sheet and the other is spread in fluid form. Of course, both of the adhesives can be applied in any suitable form, including adhesive sheet and paste or liquid.

APPLE-1002, 108-109; APPLE-1001, 7:14-30.

The above added paragraphs provide the earliest and only written description of the limitation of the two hardened adhesive layers having *different* compositions. The examiner identified this feature as allowable during the prosecution history (originally recited in the pending dependent Claims 9 and 14 of the CIP and which were later rewritten in independent form and issued as Claims 1 and 4 in the '723 Patent), but it was simply not supported by the priority applications. APPLE-1002, 37-38, 46-57; *supra*, § III.B.

Thus, the only written description supporting the limitation that “the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition” is new matter added in the CIP filed on February 3, 2010, not disclosed in any of the earlier priority documents. Accordingly, the earliest priority date for each claim of the '723 Patent is the filing date of the CIP, February 3, 2010 (“Critical Date”). APPLE-1003, ¶¶43-46.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the '723 Patent (a “POSITA”) would have had at least a Bachelor’s degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute

for experience. APPLE-1003, ¶¶23-24.

V. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. The Board has repeatedly explained that “claim terms need only be construed to the extent necessary to resolve the controversy,” and for purpose of the particular Grounds in this Petition, no formal construction is necessary because the prior art presented below satisfies the claims under any reasonable construction consistent with *Phillips*. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011)².

VI. DETAILED EXPLANATION OF GROUNDS

As detailed below, this request shows a reasonable likelihood that the Petitioner will prevail with respect to the Challenged Claims of the ’723 patent.

A. GROUND 1A – Tuominen967Pub and Capote render obvious Claims 1-9

² Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

1. Tuominen967Pub³

Tuominen967Pub is the publication of the application to which the '723 Patent claims priority as a continuation-in-part. As such, Tuominen967Pub describes each element of the claims of the '723 patent, in the same language of the '723 patent, with the exception of the “different” composition feature that was first introduced in the continuation-in-part.

In particular, Tuominen967Pub describes “an electronic module” having “one or more components embedded in an installation base.” APPLE-1004, Title, Abstract, [0002]. Tuominen967Pub’s electronic module comprises an “insulating-material layer 1” where “component 6” is embedded. *Id.*, Abstract, FIG. 10 (below), [0002], [0036], [0043]; APPLE-1003, ¶48. Component 6 is adhered to the surface of a conductive layer 4, from which “conductive patterns 14” are later formed. *Id.*, Abstract, [0037]; APPLE-1003, ¶48. Tuominen967Pub uses hardened adhesive 5 to adhere component 6 to the conductive-pattern layer 14. *Id.*, Abstract, [0036], [0037], [0038], [0052], [0053], Cl. 3. Component 6 and the

³ General descriptions provided for this and other references and combinations are incorporated into each subsection and mapping of the claims that includes citations to these references. All emphasis is added unless otherwise indicated.

conductive-pattern layer 14 are connected electrically, through conductive material 18 in holes extending through the hardened adhesive at the locations of contact zones on the component; in some embodiments, “protrusions 7” on the component 6 extend into the holes for making electrical connection with the conductive-pattern layer 14. *Id.*, [0036], [0037], [0039] (“the contact protrusions of the component may, during gluing, extend through the adhesive layer to make contact with the conductive layer [from which conductive patterns 14 are formed]”), [0043] (“holes 17 thus extend to the material of the contact protrusions 7”), [0069]-[0074]; APPLE-1003, ¶49.

Notably, while Tuominen967Pub does not describe different adhesive compositions, Tuominen967Pub describes two layers of an adhesive. For example, Tuominen967Pub describes that “an adhesive layer 5 is spread on the attachment surface of the conductive layer 4 [from which conductive patterns 14 are formed], or on the attachment surface of the component 6, or **on both**.” *Id.*, [0036], [0037] (describing spreading adhesive on “attachment **surfaces**”), [0053] (“It is also possible to proceed by spreading the adhesive on **both the attachment areas**.”), [0038] (“the adhesive hardens”); APPLE-1003, ¶50. When two layers of adhesive are used (not illustrated in the figures), one on the conductive layer 4 and the other on the attachment surface of the component 6, “the adhesive layers are pressed against each other.” *Id.*, Cl. 3; APPLE-1003, ¶50.

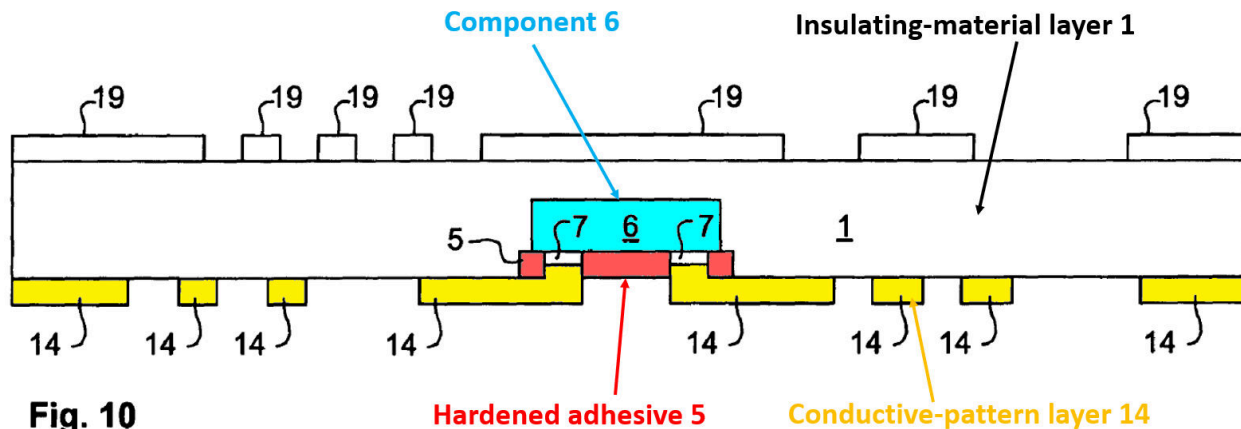


Fig. 10

APPLE-1003, ¶48 (APPLE-1004, FIG. 10 (Annotated))

Tuominen967Pub notes that “[e]ven the thermal expansion caused by the normal operation of a device may cause mechanical stresses large enough to compromise the long-term reliability of an FC [(flip-chip)] structure.” APPLE-1004, [0007]; APPLE-1003, ¶51. Tuominen967Pub indicates that “[o]ne preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material [including the component, the conductive layer, the substrate, and protrusions on the component] during the process.” APPLE-1004, [0040]; APPLE-1003, ¶52.

2. Capote

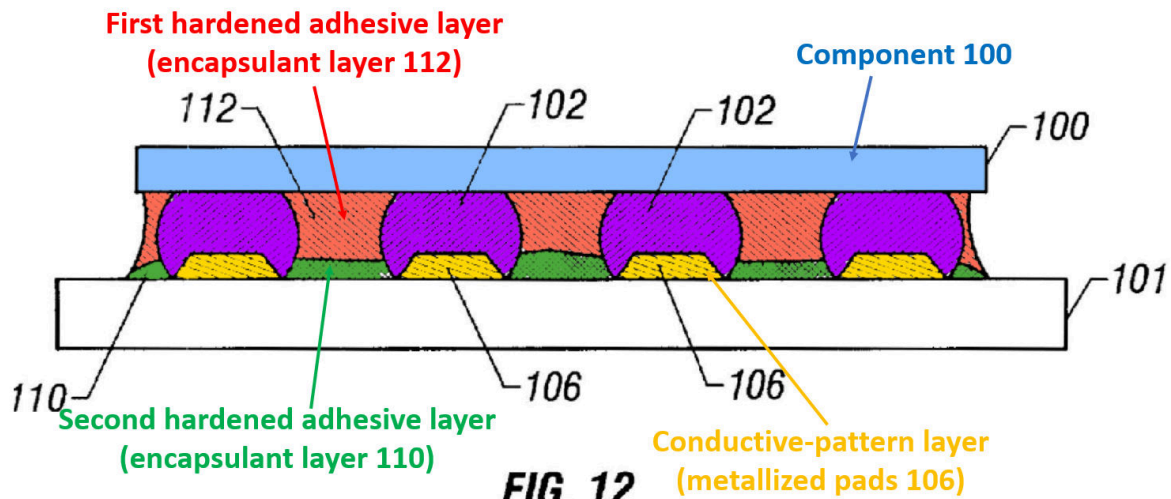
Capote describes an electrical component assembly having an integrated circuit chip mechanically and electrically attached to metallized pads on a substrate using a “multilayer encapsulant” that includes at least two adhesives having

different compositions. APPLE-1005, Title, Abstract, FIG. 12, 3:31-32 (“underfill encapsulating adhesive”), 4:18-6:29, 8:61-9:32, 9:63-67; APPLE-1003, ¶¶53-54.

Capote discusses an “obstacle” to flip-chip technology when applied to “polymer printed circuit substrates (i.e., circuit boards)” of “unacceptably poor reliability of the solder joints due to the **mismatch of the coefficients of thermal expansion** of the (i) chip . . . , (ii) the polymer substrate . . . , and (iii) the solder joint.” APPLE-1005, 1:26-59; APPLE-1003, ¶55. To overcome this obstacle and achieve “superior structural integrity,” Capote describes multiple embodiments of this “multilayer encapsulant” having the structure of at least two hardened adhesive layers with different compositions. *E.g.*, APPLE-1005, Abstract, 4:18-48, Examples 1-6; APPLE-1003, ¶55.

Like Tuominen967Pub, Capote describes “coating the active surface of the integrated circuit chip having separate discrete solder bumps thereon with a first encapsulant layer,” “coating the printed circuit substrate with a second encapsulant layer,” “placing the coated integrated circuit chip on the coated substrate whereby the first and second encapsulant layers are in contact with each other and thereafter causing the solder bumps to penetrate into the second encapsulant layer,” “curing the first and second encapsulant layers,” and “simultaneously reflowing the solder bumps to electrically connect the contacts of the integrated circuit chip to the pads of the substrate.” APPLE-1005, 4:49-5:9; *see also id.*, 4:33-34 (“a substrate

having a substrate surface with a plurality of contacts thereon”), 5:65-6:2, 7:19-25, 8:21-25 (“adhesive strength of the encapsulant”), 8:51-60 (“A preferred composition is directed to fluxing adhesive compositions... the thermally curable adhesive composition... ”), 8:61-9:32, FIG. 12 (showing first portion encapsulant layer 112 on the active surface of the IC chip 100 and second portion encapsulant layer 110 on the substrate 101 with metallized pads 106); APPLE-1003, ¶¶56-58.



APPLE-1003, ¶58 (APPLE-1005, FIG. 12 (Annotated))

Capote describes that “the encapsulant layers exhibit a gradient in thermal expansion and modulus between the substrate and the chip,” such that “in an ideal configuration, the encapsulant layer applied to the chip should have an expansion coefficient and modulus that are nearer to those of the chip and the encapsulant layer applied to the substrate should have an expansion coefficient and modulus that are nearer to those of the substrate.” APPLE-1005, 8:1-9; APPLE-1003, ¶59.

Capote explains that “[o]verall, the composite expansion coefficient for the entire encapsulant should be comparable to the expansion coefficient of the solder... to minimize stress on the solder.” APPLE-1005, 8:9-12; APPLE-1003, ¶¶59-60.

3. Predictable Combination of Tuominen967Pub and Capote

A POSITA would have been motivated to implement Tuominen967Pub’s adhesive layer 5 in accordance with Capote’s teaching of using different compositions for two hardened adhesive layers, to enhance reliability and to reduce potential problems associated with “thermal expansion mismatch” (i.e., a difference in coefficient of thermal expansion) between a component and its surrounding material. APPLE-1005, 2:14-16; *see also* APPLE-1004, [0007] (describing reliability problems associated with “thermal expansion”), [0010] (goal to achieve “a mechanically durable construction”), [0014], [0027], [0037], [0040], [0059]; APPLE-1003, ¶67 (citing APPLE-1007, 1-2). A POSITA would have combined Capote with Tuominen967Pub to facilitate secure bonding of the chip and the installation base, and reliable connections between different materials, consistent with Tuominen967Pub and Capote’s objectives. APPLE-1003, ¶68.

In the predictable combination, the first hardened adhesive layer and the second hardened adhesive layer (e.g., of adhesive 5 described by Tuominen967Pub) have different compositions, in accordance with Capote’s

suggestion to use two different material compositions. *E.g.*, APPLE-1005, 4:18-6:29, 8:61-9:32, 9:63-67, 12:3-47; APPLE-1004, [0036], [0037], [0053]; APPLE-1003, ¶69. In particular, a POSITA would have found it obvious to use two adhesives having “different physical properties as measured by their thermal expansion coefficients and elastic moduli”), in accordance with Capote’s teachings, to achieve “superior structural integrity,” among other benefits. APPLE-1005, 4:18-30; APPLE-1004, [0010] (describing similar objective of “a mechanically durable construction”); APPLE-1003, ¶69.

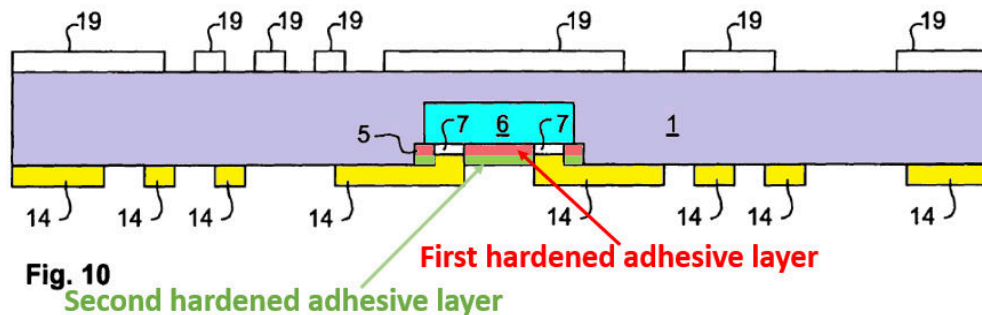


Fig. 10
Second hardened adhesive layer

APPLE-1003, ¶69 (Composite based on APPLE-1004, FIG. 10 (Annotated))

Multiple reasons would have prompted a POSITA to implement Tuominen967Pub’s adhesive (e.g., adhesive 5) in accordance with Capote’s use of different compositions for two or more adhesive layers. APPLE-1003, ¶70.

First, a POSITA would have been motivated to combine Tuominen967Pub and Capote to alleviate a common and well-known problem of reduced connection reliability associated with thermal expansion mismatch and to achieve the benefits of durable construction and superior structural integrity, consistent with

Tuominen967Pub and Capote's objectives. APPLE-1005, 4:18-30 (objective of "superior structural integrity"); APPLE-1004, [0010] (desire to achieve "a mechanically durable construction"); APPLE-1003, ¶71. For example, Tuominen967Pub emphasizes that "[e]ven the thermal expansion caused by the normal operation of a device may cause mechanical stresses large enough to compromise the long-term reliability of an FC structure." APPLE-1004, [0007]; APPLE-1003, ¶71. To address similar problems for an embedded structure, Tuominen967Pub explains that "[o]ne preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material during the process." APPLE-1004, [0040]; APPLE-1003, ¶72. This is useful when layers of similar structure are stacked on top of each other to form a multi-layered structure, as shown in Tuominen967Pub's Figure 11, because stress caused by thermal expansion mismatch between the embedded components 6 and surrounding material can accumulate through the multiple layers and compromise structural integrity. APPLE-1004, [0081] ("intermediate layer 32 can be, for example, a pre-preg epoxy layer, which is laminated between the installation bases 1"); APPLE-1003, ¶72.

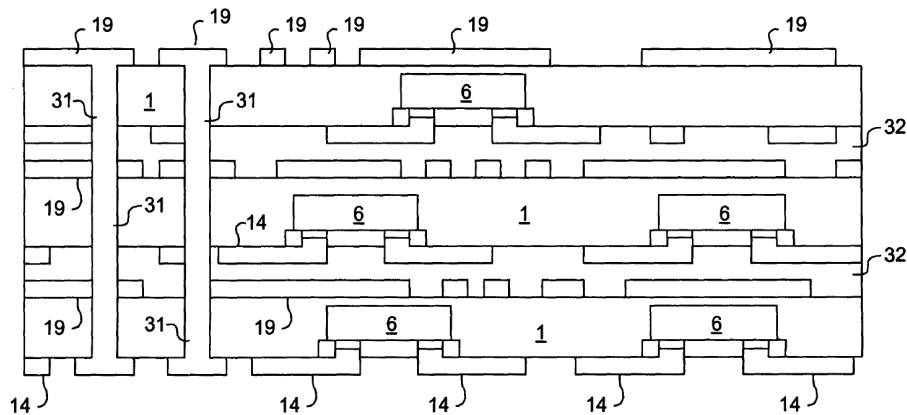


Fig. 11

APPLE-1003, ¶72 (APPLE-1004, FIG. 11)

Similarly, Capote expresses potential structural reliability issues caused by “thermal expansion mismatch between the chip and the substrate,” and describes as a solution the use of “two or more layers” of encapsulant having “different physical properties as measured by their thermal expansion coefficients and elastic moduli.” APPLE-1005, 1:26-4:15, 4:18-30; *see also id.*, 2:11-16 (“For the underfill encapsulant to be effective, it is important that it adheres well to the chip 100 and the substrate 101”); APPLE-1003, ¶73. Capote teaches “the encapsulant layer applied to the chip should have an expansion coefficient and modulus that are nearer to those of the chip and the encapsulant layer applied to the substrate should have an expansion coefficient and modulus that are nearer to those of the substrate.” APPLE-1005, 8:1-9; APPLE-1003, ¶73.

Tuominen967Pub already describes spreading adhesive 5 “on both” the attachment surface of the conductive layer 4 [from which conductive patterns 14

are formed] and the attachment surface of the component 6. APPLE-1004, [0036], *see also id.*, [0037] (describing spreading adhesive on “attachment **surfaces**”), [0053] (“It is also possible to proceed by spreading the adhesive on **both the attachment areas.**”); Cl. 3 (“the adhesive layers are pressed against each other”); APPLE-1003, ¶74. Tuominen967Pub teaches that “[t]he adhesive is selected to ensure that the adhesive used will have sufficient adhesion to the conductive film, the circuit board, and the component.” APPLE-1004, [0040]. Tuominen967Pub further emphasizes “[o]ne preferred property of the adhesive is a **suitable coefficient of thermal expansion**, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material[.]” APPLE-1004, [0040] (emphasis added); APPLE-1003, ¶74. Capote provides a straightforward suggestion for implementing the layers of Tuominen967Pub’s adhesive using first and second layers of different composition to achieve secure adhesion, reliable connection, and overall structural integrity. APPLE-1003, ¶¶75-76.

A POSITA would have recognized the benefits of using two different adhesives especially because Capote plainly describes addressing the same types of problems caused by thermal expansion mismatch when electrically and mechanically connecting components, such as semiconductor chips, to a substrate with conductors. *E.g.*, APPLE-1005, 1:21-4:15; APPLE-1003, ¶77. A POSTA

would also have recognized this because Capote's specific solution, of using different compositions in two or more adhesive layers "exhibit[ing] a **gradient in thermal expansion and modulus**" between the chips and surrounding material such as the substrate and conductive layer, and also "comparable to the expansion coefficient of the solder," furthers Tuominen967Pub's teaching of using adhesives with "**suitable coefficient of thermal expansion**, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material." APPLE-1005, 8:1-9 (emphasis added), 4:49-5:9, FIG. 12, Examples 1-6 (providing multiple example embodiments for specific adhesive compositions and application methods); APPLE-1004, [0040] (emphasis added), [0039] ("the contact protrusions of the component may ... extend through the adhesive layer to make contact with the conductive layer," indicating that contact protrusions are part of the "surrounding material," like the solder in Capote), [0043] ("holes 17 thus extend to the material of the contact protrusions 7"); APPLE-1003, ¶77.

Second, a POSITA would have been prompted to combine Tuominen967Pub and Capote because doing so was the application of known techniques (use of two or more adhesive layers having different compositions and thus different physical properties including thermal expansion coefficients and modulus in accordance with Capote's suggestions) to a known device

(Tuominen967Pub’s electronic module having a component adhered to the surface of a conductive layer of a circuit board) ready for improvement to yield predictable results (benefits articulated above). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (“[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.”). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Tuominen967Pub and Capote describe similar electronic module assemblies involving use of adhesive layers to adhere components (e.g., semiconductor chips) to a substrate and secure their mechanical and electrical connections, and because the modifications would have been implemented largely by using different compositions with different thermal expansion coefficients and modulus for the two adhesive layers—a configuration Capote already demonstrates to be successful. APPLE-1003, ¶¶78-79. Indeed, for similar reasons, Tuominen967Pub and Capote describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above. *Id.*

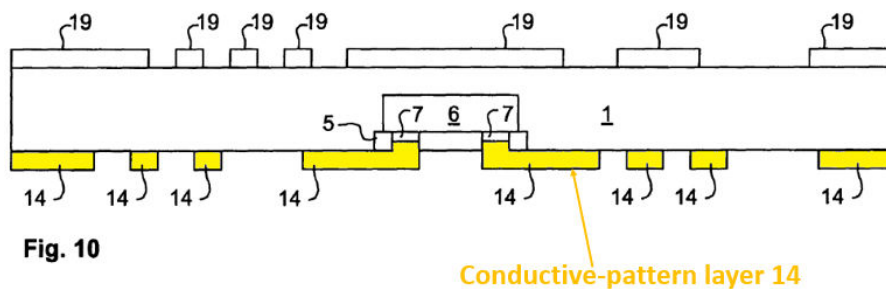
4. Application to Challenged Claims

[1pre]

If the preamble is deemed limiting, Tuominen967Pub-Capote teaches [1pre].
APPLE-1003, ¶81. For example, Tuominen967Pub describes “an electronic module and a method for manufacturing an electronic module.” APPLE-1004, Title, Abstract; APPLE-1003, ¶81.

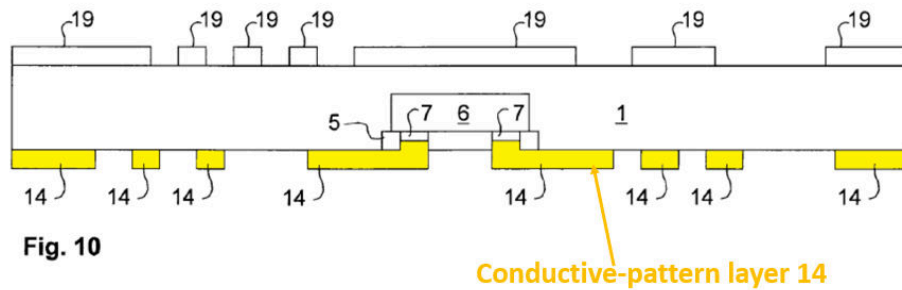
[1a]

Tuominen967Pub-Capote teaches Element [1a]. APPLE-1003, ¶¶82-83. For example, Tuominen967Pub describes “conductive patterns 14” that are made from a conductive layer 4. APPLE-1004, Abstract, [0011], [0029] (“The number of conductive-pattern layers of the electronic module can also be chosen according to the embodiment. ... each of the conductor layers contained in the electronic module can be exploited when forming conductive patterns”), [0030], [0035], [0037], [0077]-[0079], FIG. 10 (below); APPLE-1003, ¶82.



APPLE-1003, ¶82 (Tuominen967Pub, APPLE-1004, FIG. 10 (Annotated))

Tuominen967Pub’s description of “conductive patterns 14,” and example shown in FIG. 10, is the same as the ’723 patent itself:



APPLE-1003, ¶83 ('723 patent, APPLE-1001, FIG. 10 (Annotated))

[1b]

Tuominen967Pub-Capote teaches Element [1b]. APPLE-1003, ¶¶84-85. For example, Tuominen967Pub describes “an insulating-material layer 1” that is “formed on, or attached to the surface of the conductive layer [from which the conductive-pattern layer is later formed].” APPLE-1004, Abstract, [0035], [0041] (“A suitable insulating material layer 1 is selected as the base material of the electronic module”), [0042], [0059] (“The insulating-material layer 1 can be made from a suitable polymer base, in which recesses or cavities according to the size and position of the components 6 are made using some suitable method. The polymer made can be, for example, a pre-preg base known and widely used in the circuit-board industry, which is made from a glass-fibre mat and so-called b-stage epoxy.”), [0060], Cl. 1 (“making an insulating-material layer, which surrounds the component glued to the conductive layer, on the first surface of the conductive layer”), FIGS. 4-11; APPLE-1003, ¶84.

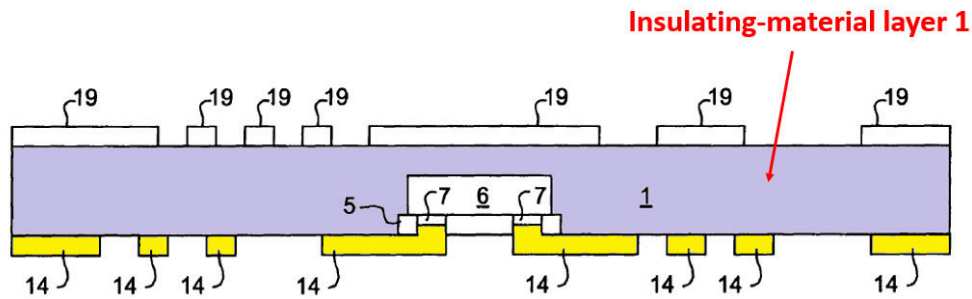


Fig. 10

APPLE-1003, ¶84 (APPLE-1004, FIG. 10 (Annotated))

The conductive-pattern layer (e.g., “conductive-pattern layer 14”) is on the insulating-material layer (e.g., “insulating-material layer 1”) such that the insulating-material layer supports the conductive-pattern layer. APPLE-1003, ¶84.

Here again, Tuominen967Pub’s description is the same as the ’723 patent itself:

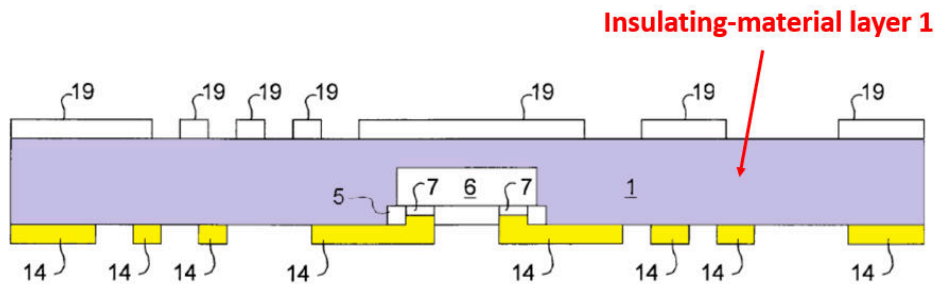


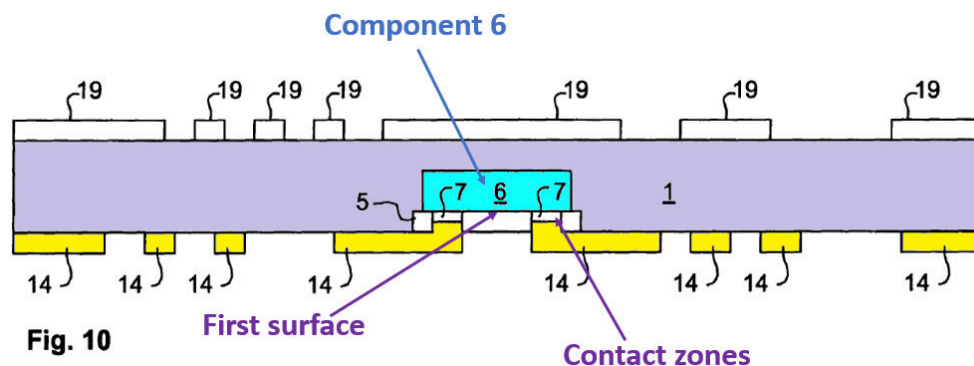
Fig. 10

APPLE-1003, ¶85 (APPLE-1001, FIG. 10 (Annotated))

[1c]

Tuominen967Pub-Capote teaches Element [1c]. APPLE-1003, ¶¶86-89. As shown in annotated Figure 10 below, Tuominen967Pub describes a “component 6”

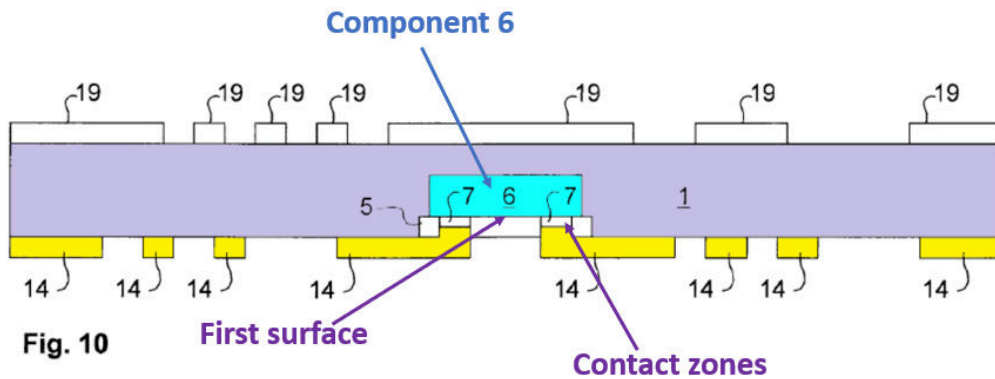
that is “surround[ed]” by the insulating-material layer 1. APPLE-1004, Abstract, [0002] (the components can be “semiconductor components”), [0035]-[0037], [0041]-[0043], [0052]-[0059], [0069], [0079]-[0081], FIGS. 3-11; APPLE-1003, ¶¶86-87. Tuominen967Pub explains that “component 6” has a *first surface* (e.g., provided by the “contact surface”) facing the conductive layer 4. APPLE-1004, [0016], [0036]. The contact surface includes “contact zones” for forming electrical contact with the component, and “the contact zones can be, for example, flat areas on the surface of the component 6, or more usually contact protrusions protruding from the surface of the component 6.” APPLE-1004, [0036]; *see also id.*, [0009], [0043], [0054], [0069], Cls. 1, 19, FIG. 10; APPLE-1003, ¶88.



APPLE-1003, ¶88 (APPLE-1004, FIG. 10 (Annotated))

Tuominen967Pub’s description of these features is the same as the

’723 patent:



APPLE-1003, ¶89 (APPLE-1001, FIG. 10 (Annotated))

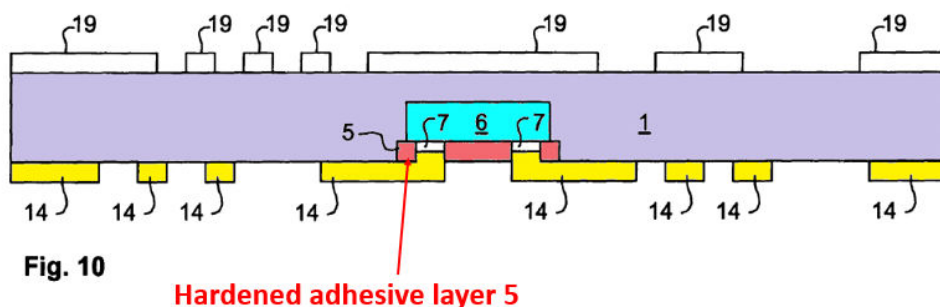
[1d]

Tuominen967Pub-Capote teaches Element [1d]. APPLE-1003, ¶¶90-91.

For example, Tuominen967Pub describes spreading adhesive layers 5 on “the attachment surface of the conductive layer 4 [from which conductive patterns 14 are formed], or **on the attachment surface of the component 6**, or on both.”

APPLE-1004, [0036]; *see also id.*, [0016], [0037], [0052]-[0056], [0059], Cls. 2, 3

(“when gluing the component[,], **adhesive layers are spread on the contact surface of the component** and the first surface of the conductive layer, and the adhesive layers are pressed against each other.”), 4, 5, 19, FIGS. 2-11; APPLE-1003, ¶90.



APPLE-1003, ¶90 (APPLE-1004, FIG. 10 (Annotated))

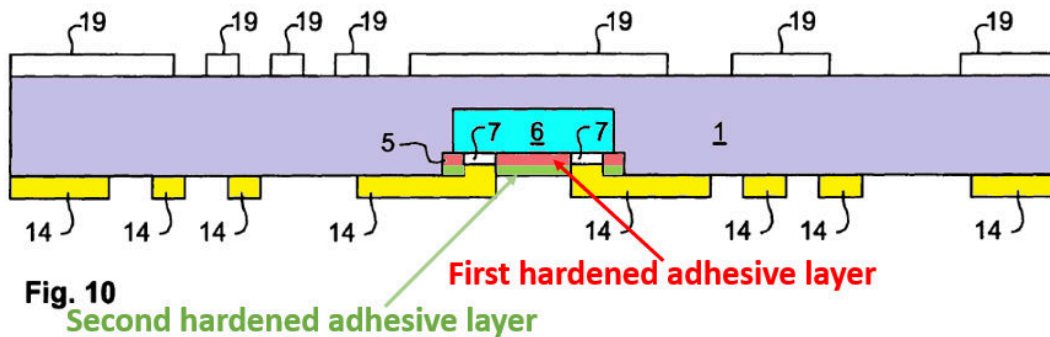
Tuominen967Pub also describes that adhesive layer 5 is “hardened.”

APPLE-1004, Cl. 19 (“a **hardened** adhesive layer in the hole or recess in the insulating-material layer, between the component and the conductive layer”); [0038] (“Another property of the adhesive is that, after spreading, the adhesive **hardens, or can be hardened**”), [0039]-[0040], [0059], Cl. 19; APPLE-1005, 4:18-30, 4:49-5:23, 7:1-35; 8:1-35, 8:61-9:32, 9:33-67. APPLE-1003, ¶91. In the combined system, the adhesive layer on the first surface of the component would have had a composition different than the second adhesive layer, in accordance with Capote. *Supra*, §VI.A.3 (Tuominen967Pub-Capote combination); *infra*, Analysis of [1h]; APPLE-1003, ¶91.

[1e]

Tuominen967Pub-Capote teaches Element [1e]. APPLE-1003, ¶¶92-93. For example, Tuominen967Pub describes spreading adhesive layers 5 on “**the attachment surface of the conductive layer 4** [from which conductive patterns 14 are formed], or on the attachment surface of the component 6, or on both.” APPLE-1004, [0036]; *see also id.*, [0016], [0037], [0052]-[0056], [0059]; Cls. 2, 3 (“when gluing the component[,], **adhesive layers** are spread on the contact surface of the component and the **first surface of the conductive layer**, and the adhesive layers are **pressed against each other.**”), 4, 5, 19, FIGS. 2-11; APPLE-1003, ¶92.

In the Tuominen967Pub-Capote combination, first and second hardened adhesive layers are located between the component and the conductive patterns (e.g., conductive-patterns 14).



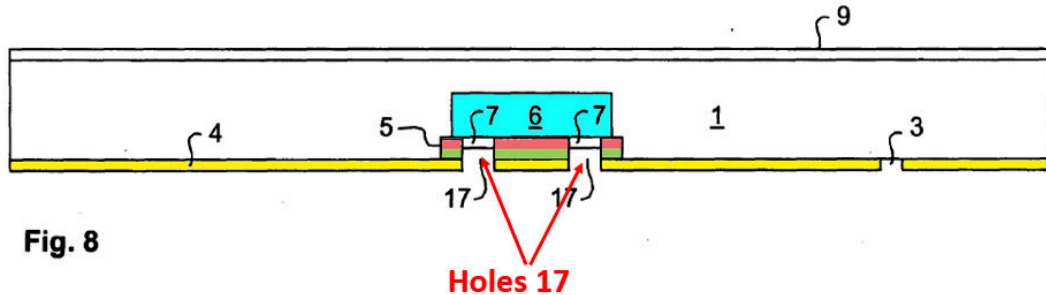
APPLE-1003, ¶92 (APPLE-1004, FIG. 10 (Annotated to show first and second hardened adhesive layers))

Furthermore, as discussed above in §VI.A.4, Analysis of Element [1d], Tuominen967Pub describes that adhesive layers 5 are “hardened.” APPLE-1004, Cl. 19, [0038]-[0040], [0059]; APPLE-1003, ¶93. Additionally, in the combined system, the second hardened adhesive layer would have had a composition in accordance with Capote. *Supra*, §VI.A.3 (Tuominen967Pub-Capote combination); *infra*, §VI.A.4, Analysis of [1h]; APPLE-1003, ¶93.

[1f]

The Tuominen967Pub-Capote combination provides Element [1f]. APPLE-1003, ¶¶94-96. Tuominen967Pub describes that “**holes 17** are made **through** the conductive layer 4 and **the adhesive layer 5**, in such a way that the material of the contact protrusions 7, or other contact zones of the components 6 is exposed.”

APPLE-1004, [0069], FIG. 8; APPLE-1003, ¶94. “**Holes 17** are made in the conductive layer 4 [from which conductive patterns 14 are formed] ..., **at the positions of the contact zones** (in the figures, the contact protrusions 7) of the components 6,” for feed-throughs “through which electrical contacts can be formed between the contact zones of the components 6 and the conductive layer 4.”
APPLE-1004, [0043]; *see also id.*, [0069]-[0074], FIG. 8; APPLE-1003, ¶94.

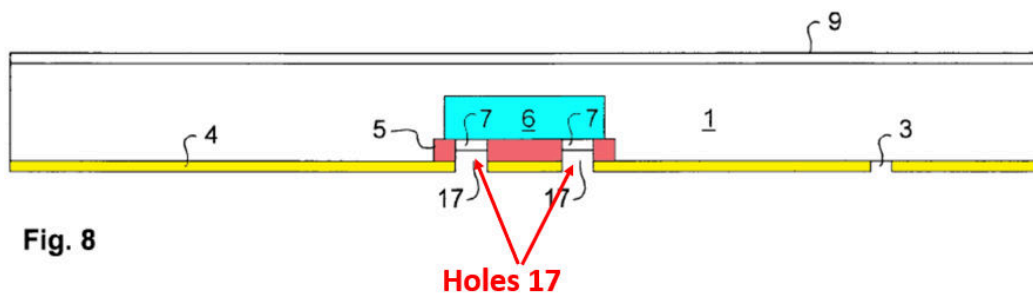


APPLE-1003, ¶94 (APPLE-1004, FIG. 8 (Annotated to show first and second hardened adhesive layers))

The holes extend through the first and second hardened adhesive layer, consistent with Tuominen967Pub’s teachings. Indeed, a POSITA would have understood and found obvious that when adhesive layer 5 is formed by pressing two adhesive layers together, one spread on the contact surface of the component (*first hardened adhesive layer*) and the other spread on the attachment surface of the conductive layer (*second hardened adhesive layer*), holes 17 would extend through both the first and second hardened adhesive layers at the locations of the contact zones, consistent with Tuominen967Pub’s teachings of the holes extending

through the hardened adhesive layer 5, so that electrical contacts can be formed between the contact zones of the components and the conductive layer. APPLE-1004, [0043], [0069]; APPLE-1003, ¶95; *supra*, §VI.A.4, Analyses of Elements [1d] and [1e].

Tuominen967Pub's description of these features is the same as the '723 patent:

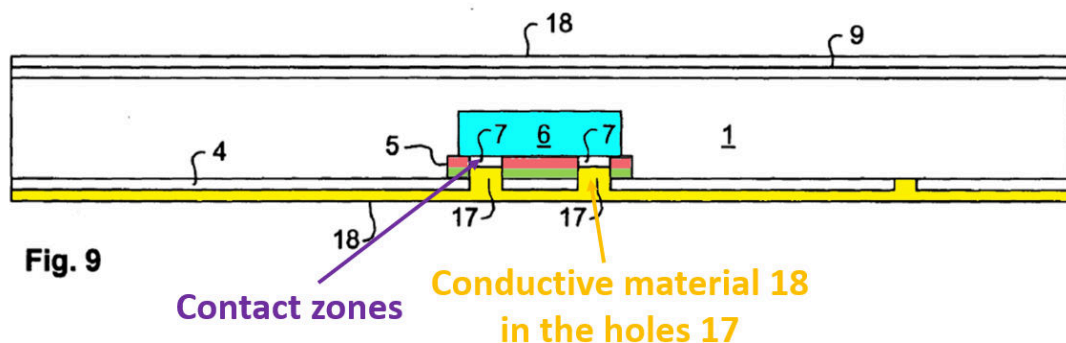


APPLE-1003, ¶96 (APPLE-1001, FIG. 8 (Annotated))

[1g]

Tuominen967Pub-Capote teaches Element [1g]. APPLE-1003, ¶¶97-98. For example, Tuominen967Pub describes that “holes 17 thus extend to the material of the contact protrusions 7 or other contact zones [of the component 6]” and that “conductive material is introduced to the hole 17, so that an electrical contact is formed between the components 6 and the conductive layer 4 [from which conductive patterns 14 are formed].” APPLE-1004, [0043], [0071] (“**conductive material 18** is grown into the holes 17”), [0072] (“The conductive material 18

being grown can be, for example, copper, or some other sufficiently electrically conductive material.”), [0073]-[0074], Cls. 1 (“making feed-throughs for connecting the contact zones of the component electrically to the conductive layer, and making conductive patterns from the conductive layer”), 19 (“conductive-material formations penetrating the adhesive layer, for forming an electrical contact between the conductive-pattern layer and the contact zones of the component”); APPLE-1003, ¶¶97-98. To be clear, Tuominen967Pub’s description here mirrors that of the ’723 patent as to these features. Compare APPLE-1004, [0071]-[0074] with APPLE-1001, 10:33-67.



APPLE-1003, ¶97 (Composite Based on APPLE-1004, FIG. 9 (Annotated to show first and second hardened adhesive layers))

[1h]

The Tuominen967Pub-Capote combination renders Element [1h] obvious. APPLE-1003, ¶¶99-103. As discussed above, Tuominen967Pub-Capote has first and a second hardened adhesive layers. *Supra*, §§VI.A.4, Analyses of Elements [1d] and [1e]. In the combined system, the first hardened adhesive layer and the

second hardened adhesive layer are different compositions “exhibit[ing] a gradient in thermal expansion and modulus between the substrate and the chip” and comparable to the expansion coefficient of the conductive material connecting the chip and the substrate, in accordance with Capote’s teachings, to enhance the structure and reliability (as discussed above), furthering Tuominen967Pub and Capote’s objectives. APPLE-1005, 8:1-12; *see also id.*, 2:14-16, 4:18-30, 8:61-9:32, 9:63-67; APPLE-1004, [0007], [0010], [0040]; APPLE-1003, ¶¶99-101; *supra*, §VI.A.3 (Tuominen967Pub-Capote combination).

For example, the first hardened adhesive layer is spread on the contact surface of the component and has a composition with an expansion coefficient and modulus that are nearer to those of the component, and the second hardened adhesive layer is spread on the attachment surface of the conductive-pattern layer and has a composition with an expansion coefficient and modulus that are nearer to those of the conductive film and substrate, in accordance with both Tuominen967Pub’s and Capote’s teachings. APPLE-1004, [0040] (teaching use of adhesives with “suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material”), [0036], [0037], [0052], [0053]; APPLE-1005, 4:18-30, 4:49-5:9, 8:1-12, 8:61-9:32, 9:63-67, FIG. 12; *supra*, §VI.A.3 (Tuominen967Pub-Capote combination); APPLE-1003, ¶102.

As shown below, the Tuominen967Pub-Capote combination includes two different adhesives to form a composite adhesive layer 5, with the first hardened adhesive layer having one composition on the contact surface of the component, and the second hardened adhesive layer having a different composition on the attachment surface of the conductive layer. APPLE-1003, ¶103.

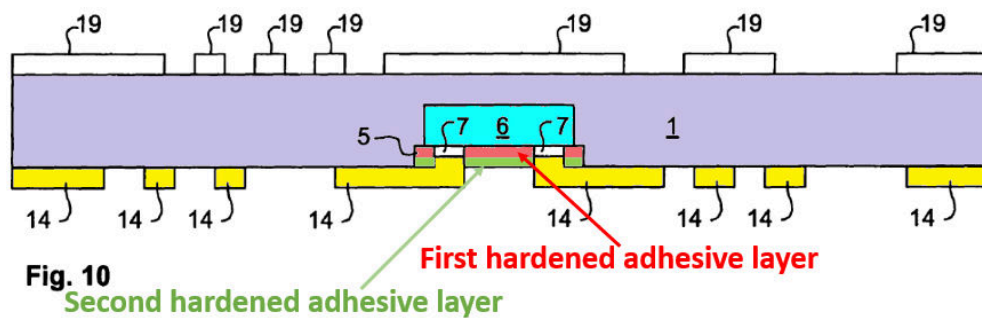
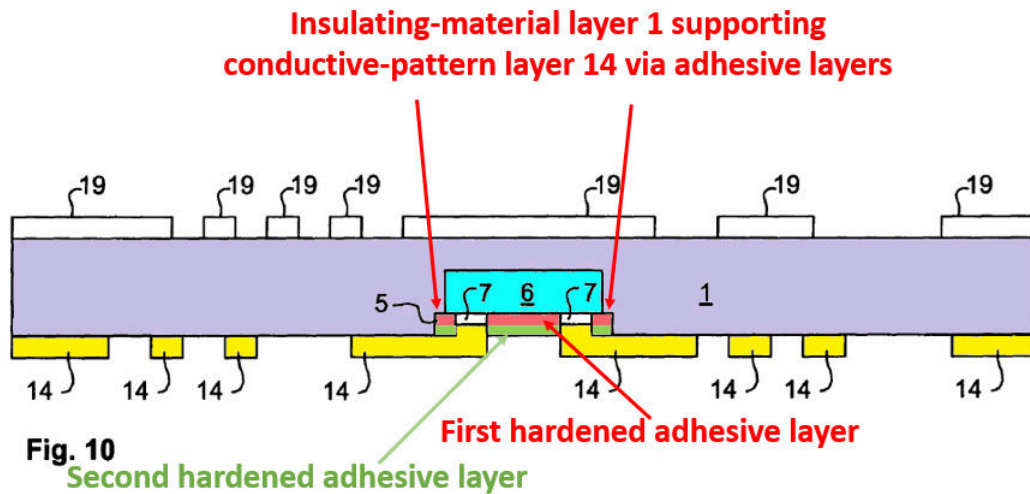


Fig. 10
APPLE-1003, ¶103 (APPLE-1004, FIG. 10 (Annotated to show first and second hardened adhesive layers))

[2]

The Tuominen967Pub-Capote combination renders Claim [2] obvious. APPLE-1003, ¶104. For example, Tuominen967Pub describes that “the adhesive entirely fills the space remaining between the components 6 and the conductive layer 4,” and that the “adhesive layer also supports the conductive patterns 14 to be formed later from the conducting layer 4.” APPLE-1004, [0037]. As shown in the annotated composite figure below, the second hardened adhesive layer is located between the conductive-pattern layer and insulating-material layer 1, such that insulating-material layer 1 supports conductive-pattern layer 14 via said second

hardened adhesive layer. APPLE-1003, ¶104; *supra*, §VI.A.4, Analysis of Element [1e].



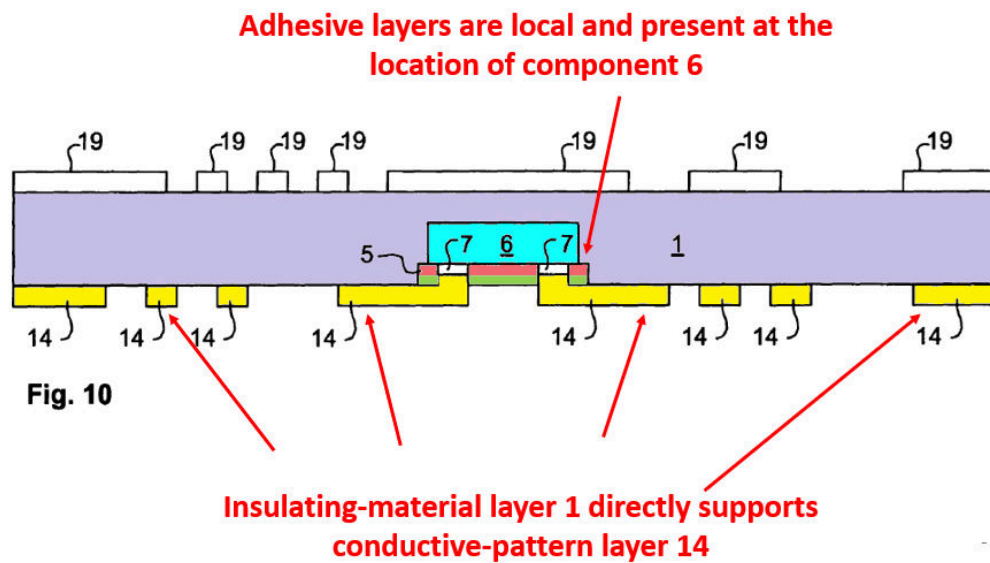
APPLE-1003, ¶104 (APPLE-1004, FIG. 10 (Annotated to show first and second hardened adhesive layers))

[3]

The Tuominen967Pub-Capote combination renders Claim [2] obvious.

APPLE-1003, ¶105. As shown in the annotated figure below, Tuominen967Pub describes adhesive (e.g., first and second hardened adhesive layers) are local and present at the location of component 6 such that insulating-material layer 1 directly supports conductive-pattern layer 14 (e.g., outside the location of component 6). APPLE-1004, [0059] (“In stage D, an insulating-material layer 1, in which there are pre-formed recesses 2 or recesses for the components 6 to be glued to the conductive layer 4, is **placed on top of the conductive layer 4** [from which conductive-pattern layer 14 is later formed]”), FIGS. 4-11; APPLE-1003, ¶105. In

the Tuominen967Pub-Capote combination, the adhesive includes first and second hardened adhesive compositions, in accordance with Capote's suggestions, which are local and present at the location of the component, in accordance with Tuominen967Pub's description (e.g., of adhesive 5). *Id.*



APPLE-1003, ¶105 (APPLE-1004, FIG. 10 (Annotated to show first and second hardened adhesive layers))

[4pre]

Tuominen967Pub-Capote teaches [4pre], to the extent the preamble is limiting. *See* §VI.A.4, Analysis of [1pre]; APPLE-1003, ¶106.

[4a]

See §VI.A.4, Analysis of [1c]; APPLE-1003, ¶107; APPLE-1004, [0002] (“semiconductor components”).

[4b]

See §VI.A.4, Analysis of [1d]; APPLE-1003, ¶108.

[4c]

See §VI.A.4, Analysis of [1e]; APPLE-1003, ¶109.

[4d]

For example, Tuominen967Pub describes that the contact zones on attachment surface of the component 6 are “flat areas on the surface of the component 6, or more usually contact protrusions protruding from the surface of the component 6.” APPLE-1004, [0036]. Tuominen967Pub further describes that “holes 17 are made in such a way that they also penetrate through the adhesive layer that has been left on top of the contact zones, or contact protrusions 7 ... [and] extend to the material of the contact protrusions 7 or other contact zones.” APPLE-1004, [0043]. Further, “conductive material is introduced to the hole 17” for forming electrical contact between the components 6 and the conductive layer 4. *Id.* The conductive material grown into the holes 17 is, for example, “copper.” *Id.*, [0071], [0072] (also disclosing copper-metallization methods, “by surfacing the holes 17 with a thin layer of chemical copper and then continuing the surfacing using an electrochemical copper-growing method. ...”); APPLE-1003, ¶¶110-111.

Tuominen967Pub’s conductive material in holes 17, alone or together with contact protrusions 7, provide the claimed *contact elements*. APPLE-1003, ¶¶111-115. To be clear, Tuominen967Pub’s description describes the ’723 Patent’s

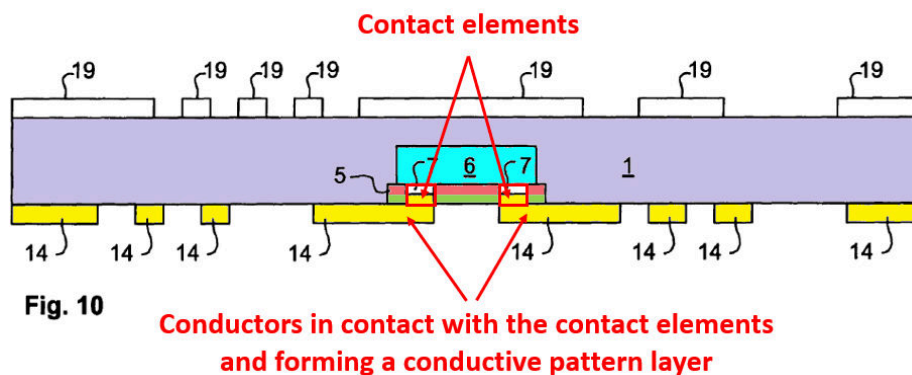
example embodiment verbatim. *Compare* APPLE-1004, [0071]-[0074] *with* APPLE-1001, 10:33-67. For example, in Tuominen967Pub's example in which the contact zones are "flat areas" on the surface of the component 6, the metal (e.g., copper layers) in holes 17 provide the claimed "contact elements made of metal" on the set of contact zones. APPLE-1004, [0036]; APPLE-1003, ¶112. The contact elements are grown inside holes 17 so that an electrical contact is formed between the component and the conductive layer, and thus "penetrate through the adhesive layer" and "extend to the material of the contact zones." APPLE-1003, ¶113; *supra*, §§VI.A.4, Analyses of Elements [1d] ("a first hardened adhesive layer on the first surface of the at least one component"), [1e] ("a second hardened adhesive layer in contact with the conductive-pattern layer and the first hardened adhesive layer"), and [1f] ("holes in the first and second hardened adhesive layer at the locations of the contact zones").

In Tuominen967Pub's example in which contact protrusions 7 are included, if contact protrusions 7 are considered to be on top of the contact zones ("flat areas" on the surface of component 6), then the conductive material (e.g., copper) in holes 17 and the contact protrusions 7 together provide the claimed contact elements. APPLE-1004, [0036], [0043]; APPLE-1003, ¶113. Alternatively, if contact protrusions 7 themselves are considered to provide contact zones, the conductive material (e.g., copper layers) in holes 17 provide the claimed "contact

elements.” APPLE-1004, [0036], [0043]; *supra*, §VI.A.4, Analysis of Element [1g]; APPLE-1003, ¶114. Tuominen967Pub explains that when the component 6 includes contact protrusions 7, the thickness of the adhesive layer 5 is “greater, for example about 1.5-10 times, the height of the contact protrusions 7.” APPLE-1004, [0052]. Accordingly, the conductive material (such as layers of copper) in holes 17 extends through both the second hardened adhesive layer (on the attachment surface of the conductive layer) and the first hardened adhesive layer. *Id.*, [0043] (“penetrate through the **adhesive layer** that has been **left on top of** the contact zones, or **contact protrusions 7**”); *supra*, §VI.A.4, Analysis of Element [1g]; APPLE-1003, ¶¶114-115.

[4e]

See §VI.A.4, Analysis of Element [1a]; APPLE-1003, ¶116. The ’723 Patent and Tuominen967Pub refer to conductive-pattern layers 14 and 19 also as “conductors 14 and 19.” Compare APPLE-1001, 11:62, 12:11 with APPLE-1004, [0083].



APPLE-1003, ¶116 (Composite Based on APPLE-1004, FIG. 10 (Annotated to show first and second hardened adhesive layers))

[4f]

See §VI.A.4, Analyses of Element [1b] (“an insulating-material layer”) & [1c] (“at least one component inside the insulating-material layer”); APPLE-1003, ¶117.

[4g]

See §VI.A.4, Analysis of Element [1h]; APPLE-1003, ¶118.

[5]

The Tuominen967Pub-Capote combination provides Claim [5]. APPLE-1003, ¶119. For example, Tuominen967Pub teaches that the components are “microcircuits.” APPLE-1004, [0002], [0036].

[6]⁴

The Tuominen967Pub-Capote combination provides Claim [6]. APPLE-1003, ¶¶120-121. For example, Tuominen967Pub describes that “the contact surface of the component is glued to a conductive layer, so that, in preferred

⁴ The “area of the first hardened adhesive layer is equal to the area of the first surface” is ambiguous and renders claim 6 indefinite. Yet, unpatentability of claim 6 can be determined here, because the prior art expressly describes such features. APPLE-1003, ¶120.

embodiments, the adhesive attaches the component essentially **over the entire area of its contact surface.**” APPLE-1004, [0016], [0053] (“adhesive layer 5 is spread on the attachment surfaces of the components 6,” and the spreading “can be carried out, for example, by dipping the component in adhesive”); APPLE-1001, 3:27-30; 9:18-27. A POSITA would have understood that by dipping the component in the adhesive, the resulting adhesive “spread on” the component would cover, and have an area equal to, the entire area of the contact surface of the component. APPLE-1003, ¶¶120-121.

*[7]*⁵

The Tuominen967Pub-Capote combination renders Claim [7] obvious. APPLE-1003, ¶¶122-126. Tuominen967Pub describes that “[f]or gluing, an adhesive layer 5 is spread on the attachment surface of the conductive layer 4 [from which conductive patterns 14 are formed], or on the attachment surface of the component 6, or on both.” APPLE-1004, [0036]. Tuominen967Pub further explains, “[i]n many embodiments, it is preferable to spread so much adhesive on

⁵ The “area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer” is ambiguous and renders claim 7 indefinite. Yet, unpatentability of claim 7 can be determined here, because the prior art expressly describes such features. APPLE-1003, ¶122.

the attachment surface, or attachment surfaces, that the adhesive entirely fills the space remaining between the components 6 and the conductive layer 4.” *Id.*, [0037]. In one example, Tuominen967Pub describes that “the adhesive layer 5 is spread on the attachment surfaces of the components 6 [alone], instead of on the attachment areas of the conductive layer 4,” while “[i]t is also possible to proceed by spreading the adhesive on both the attachment areas of the conductive layer 4 and on the attachment surfaces of the components 6.” *Id.*, [0053]. APPLE-1003, ¶123.

A POSITA would have found obvious, from Tuominen967Pub’s description of spreading adhesive only on the attachment surface of the component as well as only on the attachment areas of the conductive layer, design options for the relative areas of the adhesive spread on the two attachment surfaces. In particular, a POSITA would have found obvious from Tuominen967Pub’s description a design choice involving only three discrete possibilities in which the area of the adhesive spread on the attachment surface of the component is either (1) greater than, (2) less than, or (3) equal to, the area of the adhesive spread on the attachment surface of the conductive layer. APPLE-1003, ¶124. A POSITA would have been motivated to apply any of the above design choices, for example, to accommodate different sizes of openings or holes that are on the attachment surface of the component or on the attachment surface of the conductive layer, or to balance a

secure adhesion between the component and the conductive layer with savings on the total amount of adhesive used. APPLE-1003, ¶125. Indeed, Tuominen967Pub describes spreading adhesive on the conductive layer such that “the surface of the conductive layer is essentially free of adhesive outside of the connection zones of the components.” APPLE-1004, Cl. 4. At least in some configurations, “the connection zones” would have been understood to be smaller than the attachment surface of the components, and thus, the area of the first adhesive layer is greater than the area of the second adhesive layer (i.e., option (1) above). APPLE-1003, ¶125.

To be clear, a POSITA would have had a reasonable expectation of success in implementing the design choices, including a design in which the area of the first adhesive layer is greater than the area of the second adhesive layer. APPLE-1003, ¶126. Tuominen967Pub describes options are achieve bonding, including by spreading adhesive on the attachment surface of the component alone, and thus a POSITA would have recognized that applying adhesive that would contact a smaller area of the attachment surface of the conductive layer would also be expected to achieve sufficient adhesion. *Id.*

[8]

The Tuominen967Pub-Capote combination renders Claim [8] obvious. APPLE-1003, ¶¶127-128. For example, Tuominen967Pub describes that the

conductive material 18 being grown into the holes 17 can be copper, and “[c]opper metallizing can be performed by surfacing the holes 17 with **a thin layer of chemical copper** and then **continuing the surfacing using an electrochemical copper-growing method.**” APPLE-1004, [0071], [0072] (emphasis added), [0073] (“the holes 17 of the feed-throughs are first cleaned ... After this, the feed-throughs are metallized in such a way that an SnPd coating catalysing [*sic*] the polymer is first formed, after which a thin layer (about 2 μm) is deposited on the surface. The thickness of the copper is increased using electrochemical deposition.”) Thus, Tuominen967Pub teaches contact elements comprising a first layer of chemically deposited copper and at least one second layer of electrochemically deposited copper. APPLE-1003, ¶127; *supra*, §VI.A.4, Analyses of Elements [1g] and [4d].

Further, Tuominen967Pub also describes contact protrusions 7, which may form another layer of the claimed “contact elements.” *Supra*, §VI.A.4, Analysis of Element [4d]; APPLE-1003, ¶128. A POSITA would have understood and found obvious that contact protrusions on electronic components be metal, because metals are widely used to form contact protrusions and Tuominen967Pub itself recognizes that connections of a component—such as component 6, to which contact protrusions 7 protrude from for making connections with other elements of the electronic module system—are “metal.” APPLE-1004, [0020] (describing that

the connection of a component does not need “**metal** being maintained molten for a long time” as an advantage of the disclosed examples). APPLE-1003, ¶128.

[9]

The Tuominen967Pub-Capote combination renders Claim [9] obvious. APPLE-1003, ¶¶129-130. For example, Tuominen967Pub describes that the conductive material 18 (the recited contact elements) being grown into the holes 17 is copper, and “[c]opper metallizing can be performed by surfacing the holes 17 with a **thin layer of chemical copper** and then **continuing the surfacing using an electrochemical copper-growing method.**” *Supra*, §VI.A.4, Analysis of Element [4d] (“contact elements made of metal...”); APPLE-1004, [0071], [0072] (emphasis added), [0073], [0074] (description of “**some other metallizing method**” used to fill holes 17 with conductive material). APPLE-1003, ¶129. A POSITA would have understood and found obvious that Tuominen967Pub’s contacts are metallurgical contacts because they are formed by metal-on-metal contacts, specifically though “electrochemical copper-growing” or otherwise “metallizing” metal over existing metal structures (i.e., the contact zones and conductors) previously formed through a different process. *E.g.*, APPLE-1004, [0034]-[0035] (conductors of the conductive-patterns 14 in contact with the contact elements are formed from conductive layer 4 which can be made from a “copper film”), [0036] (contact zones in contact with the contact elements can be “more

usually contact protrusions protruding from the surface of the component 6”); APPLE-1003, ¶130. Again, like discussed in Section VI.A.4, Analysis of [4d], Tuominen967Pub’s description describes the ’723 Patent’s example embodiment verbatim here. *Compare* APPLE-1004, [0034]-[0036] *with* APPLE-1001, 5:29-62, 6:13-21.

B. GROUND 1B – Tuominen967Pub renders obvious Claims 1-9

Claims 1-9 are additionally rendered obvious based on Tuominen967Pub itself. Tuominen967Pub fails to describe the use of different adhesive compositions, and thus does not provide written description support for claim 1 of the ’723 patent. APPLE-1003, ¶131. Yet, a POSITA would have found the use of different adhesive compositions obvious. *Id.*

1. Application to Challenged Claims

[1pre]-[1g], [4pre]-[4f]

Tuominen967Pub teaches Elements [1pre]-[1g], [4pre]-[4f]. *See* §§VI.A.4, Analyses of [1pre]-[1g], [4pre]-[4f]; APPLE-1003, ¶132.

[1h]/[4g]

As discussed above in sections VI.A.4, Analyses of [1d] and [1e], Tuominen967Pub teaches application of two adhesive layers, the first layer applied on the attachment surface of component 6 and the second layer applied on the attachment surface of conductive layer 4. APPLE-1003, ¶¶133-134. Although

Tuominen967Pub does not describe different compositions for the two layers of adhesive and fails to demonstrate possession of this feature (and thus fails to provide written description support for this feature under §112), a POSITA would have understood the use of adhesives of different compositions to be obvious.

Lockwood v. Am. Airlines, Inc., 107 F.3d 1565, 1571-1572 (Fed. Cir. 1997)

(“Entitlement to a filing date does not extend to subject matter which is not disclosed, but would be obvious over what is expressly disclosed. It extends only to that which is disclosed.”); *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998) (“A disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations.”). APPLE-1003, ¶134.

A POSITA would have been motivated to modify Tuominen967Pub’s structure to use multiple different compositions. APPLE-1003, ¶135.

Tuominen967Pub describes an objective to achieve “a mechanically durable construction” (APPLE-1004, [0010]), and describes that “[e]ven the thermal expansion caused by the normal operation of a device may cause mechanical stresses large enough to compromise the long-term reliability of an FC structure.” APPLE-1004, [0007]; APPLE-1003, ¶135. Moreover, Tuominen967Pub describes a solution to address such problems—“[o]ne preferred property of the adhesive is a

suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too greatly from the thermal expansion of the surrounding material during the process.”⁶ APPLE-1004, [0040]; APPLE-1003, ¶¶136-137. A POSITA would have found obvious that such considerations are useful when layers of substructures comprising different materials are stacked on top of each other to form a multi-layered structure, as shown in Tuominen967Pub’s Figure 11, because stress caused by thermal expansion mismatch between the embedded components 6 and surrounding material (including substrate 1, conductive-pattern layer 14, conductive elements connecting the components 6 and conductive-pattern layer 14, and intermediate layers 32) can accumulate through the multiple layers and compromise the structural integrity of the whole system. APPLE-1004, [0081] (“intermediate layer 32 can be, for example, a pre-preg epoxy layer, which is laminated between the installation bases 1”); APPLE-1003, ¶138.

Based on Tuominen967Pub’s suggestion of selecting an adhesive based on coefficient of thermal expansion relative to surrounding material, and the use of

⁶ To be clear, the ’723 patent itself does not describe example formulations for the adhesive compositions, beyond mentioning “[t]he adhesive used in the embodiments is typically a thermally hardening epoxy, for example an NCA (non-conductive adhesive).” EX1001, 6:60-62.

two “layers” of adhesive, a POSITA would have been motivated to try layers of different compositions. APPLE-1003, ¶139. In particular, a POSITA would have been prompted to select a first adhesive having a coefficient of thermal expansion relative to the material (e.g., component) it adheres to, and to select a second adhesive having a coefficient of thermal expansion relative to the material it adheres to (e.g., conductive-pattern layer).

Accordingly, through disclosure of two layers of hardened adhesive and the existence of identified, predictable solutions, and a known design need, Tuominen967Pub renders obvious Elements [1h] and [4g].

[2]/[3], [5]/[9]

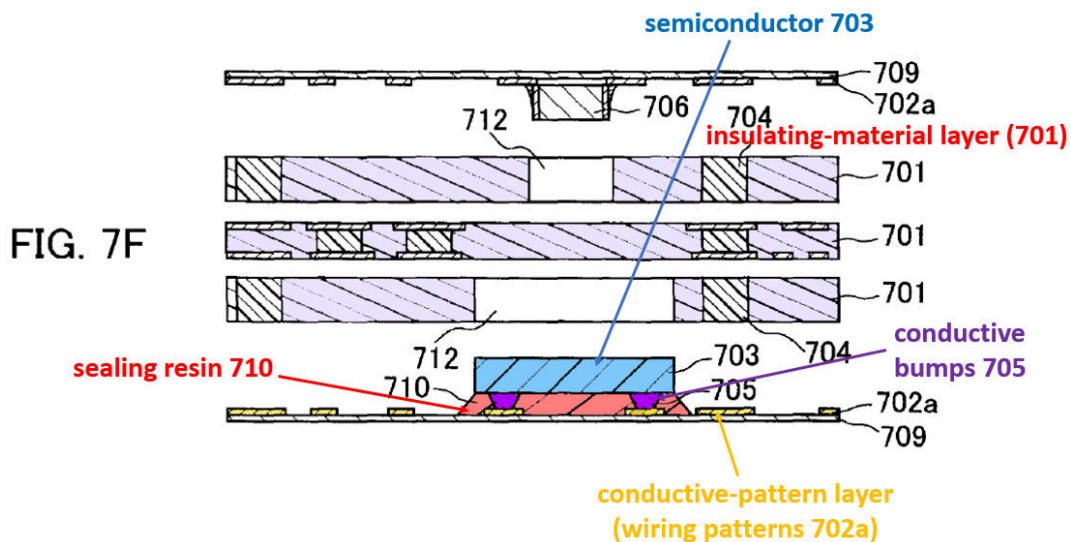
Tuominen967Pub renders dependent claims 2-3 and 5-9 obvious for the reasons set forth above, without reference to Capote. *See*, §VI.A.4, Ground 1A, Analyses of Claims 2-3, 5-9. APPLE-1003, ¶140.

C. GROUND 2 – Asahi and Capote render obvious Claims 1-9

1. Asahi

Asahi describes a “component built-in module” in which “a semiconductor 703” is embedded in an “electric insulation layer 701.” APPLE-1012, Title, Abstract, 15:62-67, 16:41-17:40, FIG. 7 (FIG. 7F). “Stud bumps 705” are used on an active surface of the semiconductor to form connections between semiconductor 703 and “wiring patterns 702a” on a surface of the insulation layer 701. *Id.*, FIG.

7, 16:36-53. Asahi likewise describes mounting processes such as “soldering” and “flip chip bonding” can be used. *Id.*, 16:65-66; APPLE-1003, ¶¶61-63. Asahi describes the use of “a sealing resin 710,” which can be “[a]n underfill resin used for ordinary flip chip bonding,” to “prevent a gap from being formed between the semiconductor 703 and the wiring patterns 702a,” so as to “prevent[] the semiconductor 703 from being damaged and improv[e] the reliability”. APPLE-1012, 16:52-62, FIG. 7; *see also id.*, 10:45-53, FIG. 8. Further, Asahi describes that “[b]y heating after pressing, the electric insulation layers 701 are cured” upon making the electric connection. *Id.*, 5:35-46, 17:33-34; *see also* 15:65-67 (“the electric insulation layer 701 may be made of an insulating resin, a mixture of a filler and an insulating resin, or the like”); APPLE-1003, ¶¶64-65.



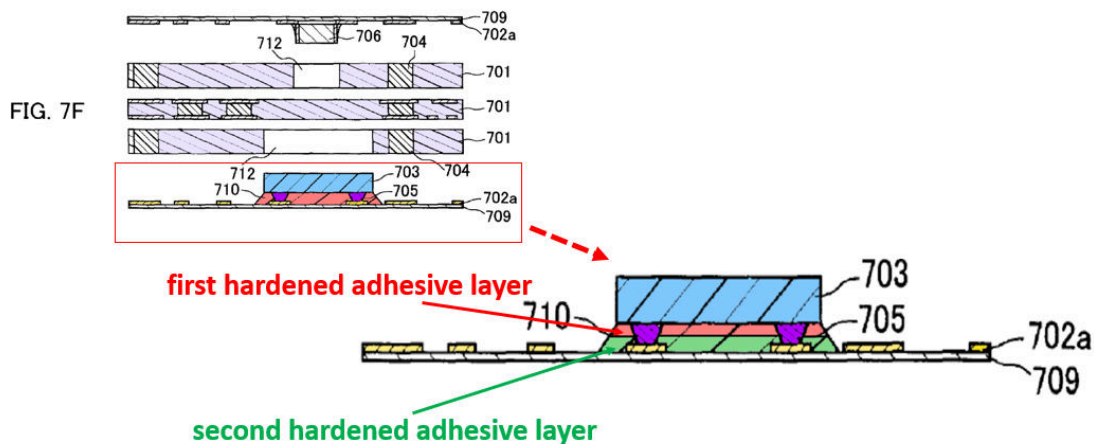
APPLE-1003, ¶62 (APPLE-1012, FIG. 7F (Annotated))

2. Predictable Combination of Asahi and Capote

A POSITA would have been motivated to implement an adhesive sealing resin (e.g., Asahi's sealing resin 710) in accordance with Capote's teaching of different compositions for at least two hardened adhesive layers, to enhance system performance and reliability (e.g., reduce or eliminate "solder joint fatigue" and other "principal disadvantages" associated with conventional underfilling processes). APPLE-1005, 1:37-4:30; APPLE-1012, 2:24-26 (desiring "high reliability" especially in "high-density component-mounting"), 16:47-66 (goals of "preventing the semiconductor 703 from being damaged and improving the reliability" in mounting methods such as "soldering" and "flip chip bonding"); APPLE-1003, ¶142.

In the predictable combination, a "sealing resin" which Asahi describes as "[a]n underfill resin used for ordinary flip chip bonding," is implemented using a "multilayer underfill encapsulant" having an adhesive composition that "allows the layers to have different physical properties as measured by their thermal expansion coefficients and elastic moduli," in accordance with Capote. APPLE-1012, 16:47-66; APPLE-1005, 4:18-30; *see also id.*, 3:31 ("underfill encapsulating adhesive"), 8:47-60 ("fluxing adhesive compositions" and "thermally curable adhesive composition"); APPLE-1003, ¶143. In the combined system (an example of which is illustrated in the composite figure below), first and second hardened adhesive layers that "exhibit a gradient in thermal expansion and modulus" are used

between the wiring patterns on the carrier and the semiconductor chip. APPLE-1005, 8:1-12 (“the encapsulant layer applied to the chip should have an expansion coefficient and modulus that are nearer to those of the chip and the encapsulant layer applied to the substrate should have an expansion coefficient and modulus that are nearer to those of the substrate”); APPLE-1003, ¶144.



APPLE-1003, ¶144 (APPLE-1012, FIG. 7F (Annotated to show first and second hardened adhesive layers))

Multiple reasons would have prompted a POSITA to implement a multi-layer sealing resin (e.g., Asahi's sealing resin 710) in accordance with Capote's teachings of different compositions for such layers. APPLE-1003, ¶145.

First, a POSITA would have been motivated to combine Asahi and Capote to address potential disadvantages associated with conventional flip chip technologies and underfill processes in semiconductor flip-chip packages. *E.g.*, APPLE-1012, 16:47-66; APPLE-1005, 1:37-4:15 (obstacle to flip-chip technology

such as poor reliability of the solder joints due to the mismatch of the coefficients of thermal expansion of the chip, the substrate, and the solder joint; and other “principal disadvantages” associated with conventional underfilling processes of flip-chip packages); APPLE-1003, ¶146.

Second, Asahi does not recite exhaustive implementation details of the specific material used for its sealing resin, other than “an underfill resin used for ordinary flip chip bonding.” *E.g.*, APPLE-1012, 16:58-59. A POSITA would have predictably looked towards other teachings, such as Capote, which provides a straightforward example for implementing an underfill resin using two layers of different adhesive compositions. Asahi already describes an embodiment in FIG. 7 using a flip-chip bonding to mount semiconductor 703 on wiring patterns on a carrier and using a sealing resin 710 such as “underfill resin used for ordinary flip chip bonding” to prevent a gap between the semiconductor 703 and wiring patterns 702a. APPLE-1012, 16:47-66 (disclosing stub bumps and solder flip-chip); APPLE-1003, ¶147. A POSITA would have predictably looked to Capote, which provides a known technique for implementing a sealing resin using two layers of different compositions, and enhancing Asahi’s stated reliability objectives. APPLE-1003, ¶147. Indeed, Asahi identifies thermal expansion as a consideration in material selection for some parts of its module, without offering implementation details as to the sealing resin. APPLE-1012, 3:12-16; 6:39-46. A POSITA would

have further been prompted because Capote also describes an underfilling process for flip-chip packages to prevent an “air gap between the chip and the substrate.” APPLE-1005, 2:1-4; APPLE-1003, ¶147-148.

Third, a POSITA would have been prompted to combine Asahi and Capote to enhance Asahi’s module and manufacturing process with benefits associated with Capote’s suggestions to “pre-apply” the first and second compositions. Capote discloses advantages of pre-application of the two or more layers of underfill encapsulants with different compositions having different physical properties. APPLE-1005, 2:48-3:38, 4:10-15. APPLE-1003, ¶149. Capote describes techniques for providing two layers of hardened adhesive with different compositions that facilitate express benefits of “among other advantages, simple chip placement followed by reflow without labor intensive underfill steps,” “a solder bumped chip or substrate with an encapsulant pre-attached, with the encapsulant performing a mechanical function and the solder performing an electrical function,” “a low-cost method for applying the solder bumps to a flip chip or flip chip substrate by creating holes in a pre-coated encapsulant,” and “a pre-coated chip encapsulant of two or more layers, with each layer performing a distinct function.” APPLE-1005, 6:19-29; *see also* 3:18-38; APPLE-1003, ¶149.

Fourth, a POSITA would have been prompted to combine Asahi and Capote because doing so was the application of known techniques (use of two or

more adhesive layers having different compositions and different physical properties including thermal expansion coefficients and modulus, using a pre-application technique) to a known device (Asahi's electronic module having a semiconductor mounted on the surface of a conductive layer) ready for improvement to yield predictable results (benefits articulated above). *KSR*, 550 U.S. at 417 (2007). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Asahi and Capote describe similar electronic module assemblies involving mounting semiconductors on a conductive pattern (e.g., through flip chip packaging) and the use of resin type hardened adhesive materials between the chip and conductive pattern to secure their mechanical and electrical connections. APPLE-1003, ¶150. Moreover, the modifications would have been implemented largely by using a pre-application using different compositions with different thermal expansion coefficients and modulus for the two adhesive layers—a configuration Capote already demonstrates to be successful. APPLE-1003, ¶151. For similar reasons, Asahi and Capote describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing addressed here. *Id.*

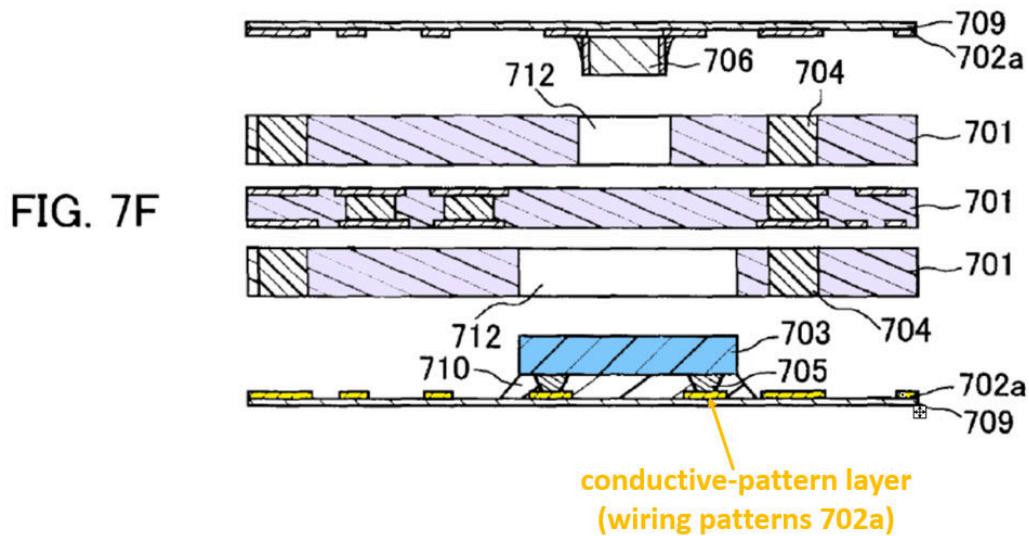
3. Application to Challenged Claims

[1pre]

If the preamble is deemed limiting, the Asahi-Capote combination provides an electronic module. APPLE-1003, ¶152. For example, Asahi describes a “component built-in module” where at least one electronic component is embedded in an electric insulation layer. APPLE-1012, Title, Abstract, 15:62-67, 16:41-17:40, 17:6-9 (“holes 712 are formed for incorporating the circuit component 706 and the semiconductor 703”), FIG. 7; *see also* APPLE-1005, Title (“semiconductor flip-chip package”), Abstract, 4:19-6:29 (“the invention is directed to an electrical component assembly,” “electrical components such as flip-chips”, having an “integrated circuit chip”); APPLE-1003, ¶152.

[1a]

The Asahi-Capote combination provides Element [1a]. APPLE-1003, ¶153. For example, Asahi describes a conductive-pattern layer (e.g., “wiring patterns 702a”). The “wiring patterns 702a” are provided on a “carrier 709,” and a semiconductor 703 is provided on the wiring patterns 702a. APPLE-1012, 16:39-43, FIG. 7F; *see also* APPLE-1005, 4:33-34, 9:9-15 (“solder pads 106” on a substrate), FIG. 12; APPLE-1003, ¶153.



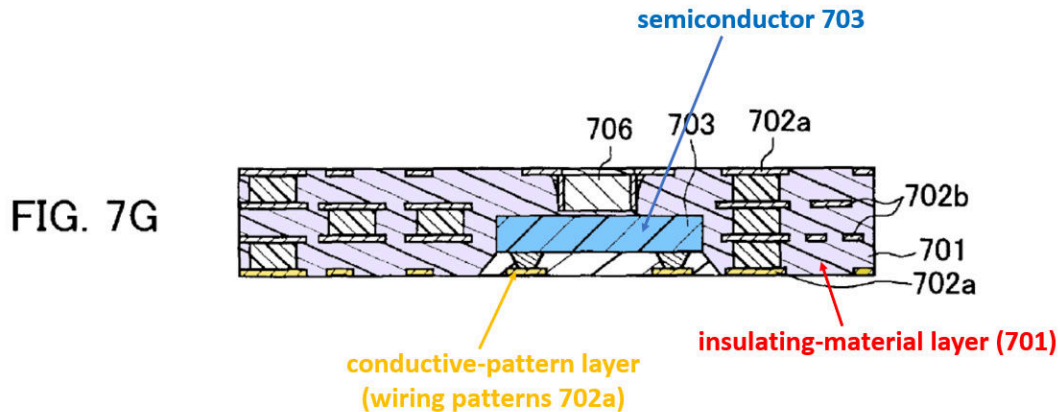
APPLE-1003, ¶153 (APPLE-1012, FIG. 7F (Annotated))

Accordingly, through at least Asahi’s “wiring patterns 702a,” Asahi-Capote provides Element [1a].

[1b]

The Asahi-Capote combination includes an insulating-material layer (e.g., Asahi’s “electric insulating layer 701” having embedded electronic components). APPLE-1012, 15:62-16:43; APPLE-1003, ¶154. Asahi’s electric insulating layer 701 supports the wiring patterns 702a (conductive-pattern layer), when the semiconductor 703 is embedded in the electric insulation layers 701. *Supra*, §VI.C.3, Analysis of Element [1a]; APPLE-1012, 17:25-36 (“By heating after pressing, the electric insulation layers 701 are cured. After curing, the carriers 709 are removed, thereby providing a component built-in module that has the wiring

patterns 702a on surfaces thereof”); FIG. 7G (showing electric insulation layer 701 supporting wiring patterns 702a); APPLE-1003, ¶154.



APPLE-1003, 154 (APPLE-1012, FIG. 7G (Annotated))

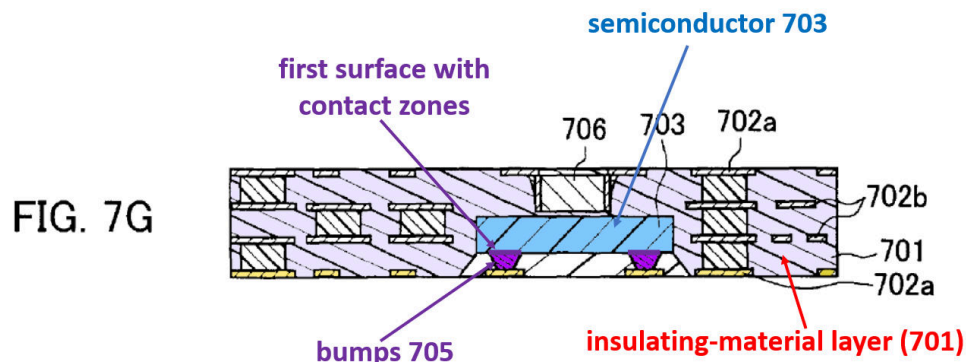
Accordingly, through Asahi’s disclosure of “electric insulating layer 701” and its relationship with “wiring patterns 702a,” Asahi-Capote provides Element [1b].

[1c]

The Asahi-Capote combination provides Element [1c]. APPLE-1003, ¶¶155-157. As discussed above in Section VI.C.3, Analyses of Elements [1a] and [1b], Asahi describes at least one component (e.g., “semiconductor 703”) inside the insulating material layer (e.g., “electric insulating layer 701”). APPLE-1012, 15:62-17:40 (“By pressing and heating, the semiconductor 703 ... [is] embedded in the electric insulation layers 701”), FIG. 7G; APPLE-1003, ¶155.

Semiconductor 703 has a first surface with contact zones (e.g., the semiconductor die's pads on its active surface) thereon. Contact elements, such as “stud bumps 705,” formed at the contact zones provide connections between the semiconductor and wiring patterns. APPLE-1012, 16:47-66 (“Usable as a method for mounting the semiconductor 703, are flip chip bonding utilizing ACF, NCF, a non-conductive particle paste (NCP), gold-gold junction, or stud bumps, and soldering of a real-chip-size-package (R-CSP). In the present embodiment, stud bumps 705 are used.”); APPLE-1003, ¶156.

To be clear, Capote similarly describes “an integrated circuit chip [100] having an active surface with a plurality of contacts thereon wherein the substrate surface faces the active surface.” *E.g.*, APPLE-1005, 4:35-37; APPLE-1003, ¶157. Even if not expressly provided by Asahi, a POSITA would have recognized, and found obvious, that the first surface of the component include contact zones, effectuating electrical connection with the semiconductor component, in accordance with Asahi and Capote's teachings. *Id.*



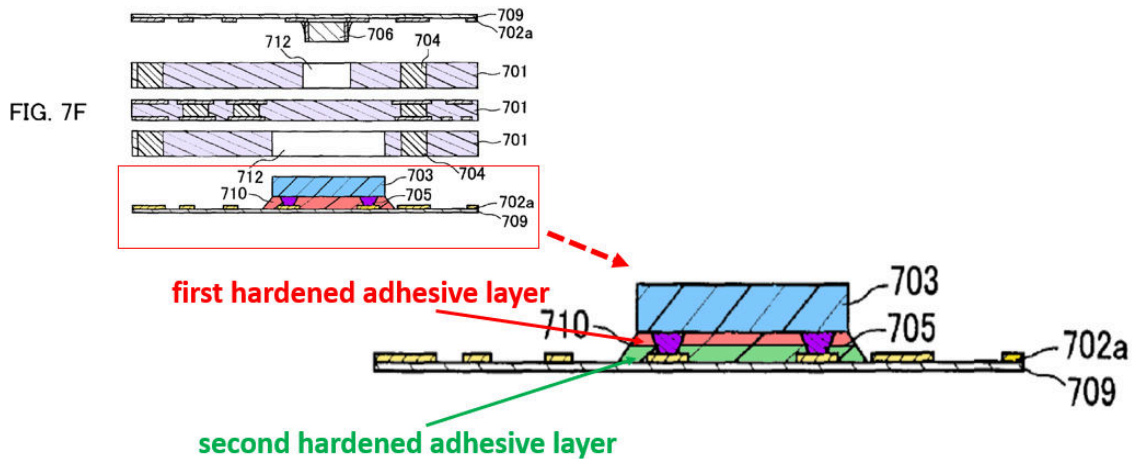
APPLE-1003, ¶157 (APPLE-1012, FIG. 7G (Annotated))

Accordingly, the Asahi-Capote combination provides Element [1c].

[1d]

The Asahi-Capote combination provides Element [1d]. APPLE-1003, ¶¶158-161. As discussed above in Section VI.C.1, Asahi describes “a sealing resin 710,” which can be “[a]n underfill resin used for ordinary flip chip bonding,” to “prevent a gap from being formed between the semiconductor 703 and the wiring patterns 702a,” and “prevent[] the semiconductor 703 from being damaged and improv[e] the reliability.” APPLE-1012, 16:52-62, FIG. 7; *see also id.*, 10:45-53, FIG. 8; APPLE-1003, ¶158. In the predictable Asahi-Capote combination, the sealing resin is implemented with multiple layers having different compositions, in accordance with Capote’s suggestions. *Supra*, §VI.C.2; APPLE-1003, ¶158.

As illustrated in the composite figure below, in the combined system, the sealing resin layer includes a two-layer underfill encapsulant having a first hardened adhesive layer on the first surface of the semiconductor (e.g., semiconductor 703) and a second hardened adhesive layer in contact with wiring patterns and the first hardened adhesive layer. *Supra*, §VI.C.2; APPLE-1005, 4:18-6:18; *see also* APPLE-1005, 8:1-12; APPLE-1003, ¶159.



APPLE-1003, ¶159 (Composite Based on APPLE-1012, FIG. 7F (Annotated to show first and second hardened adhesive layers))

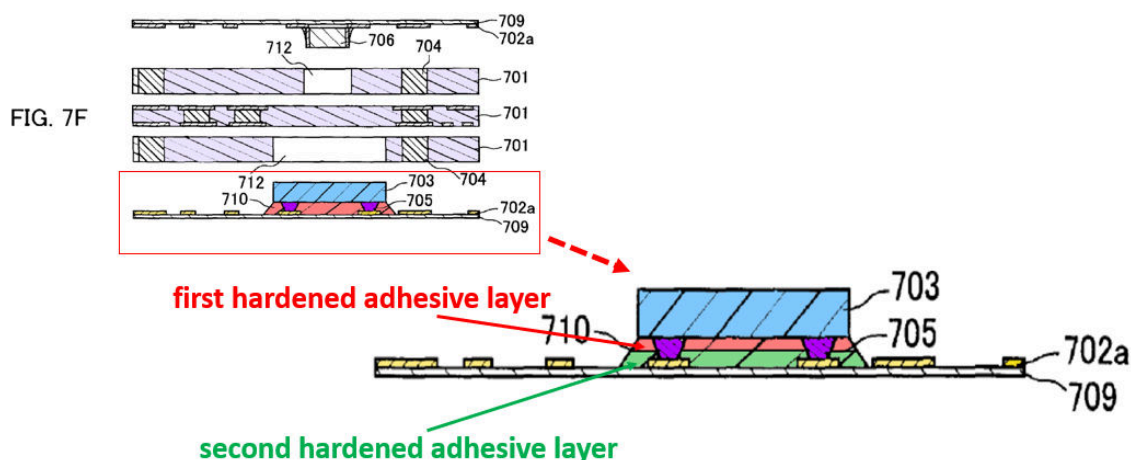
To be clear, the first layer is an “adhesive,” as suggested by Capote. *See e.g.*, APPLE-1005, 3:31 (“underfill encapsulating adhesive”), 8:15-25 (“the adhesive strength of the encapsulant” referring to the first encapsulate layer), 8:47-60 (“A preferred composition [of the second encapsulant layer] is directed to fluxing adhesive compositions ... Generally, depending upon the intended end use, the thermally curable adhesive composition comprises ...”); *supra*, §VI.A.2 (Capote overview); APPLE-1003, ¶160. Capote further describes that the first and second layers are “hardened” such as through “curing.” APPLE-1005, 4:52-6:18; APPLE-1003, ¶160. Thus, the combination’s first layer provides a first hardened adhesive layer on the first surface of semiconductor 703, and the second portion encapsulant provides a second hardened adhesive layer in contact with wiring patterns 702a (the conductive-pattern layer) and the first portion encapsulant (first hardened adhesive layer). APPLE-1003, ¶161.

Accordingly, the Asahi-Capote combination provides Element [1d].

[1e]

The Asahi-Capote combination provides Element [1e]. *Supra*, §VI.C.3, Analysis of Element [1d]; APPLE-1003, ¶¶158-161.

As described above, the combined system includes a two-layer underfill encapsulant having a first hardened adhesive layer on the first surface of the semiconductor (e.g., semiconductor 703) and a second hardened adhesive layer in contact with wiring patterns and the first hardened adhesive layer. *Supra*, §VI.C.2; APPLE-1005, 4:18-6:18; *see also* APPLE-1005, 8:1-12; APPLE-1003, ¶159. The second portion encapsulant provides a second hardened adhesive layer in contact with wiring patterns 702a (the conductive-pattern layer) and the first portion encapsulant (first hardened adhesive layer). APPLE-1003, ¶¶159-161.

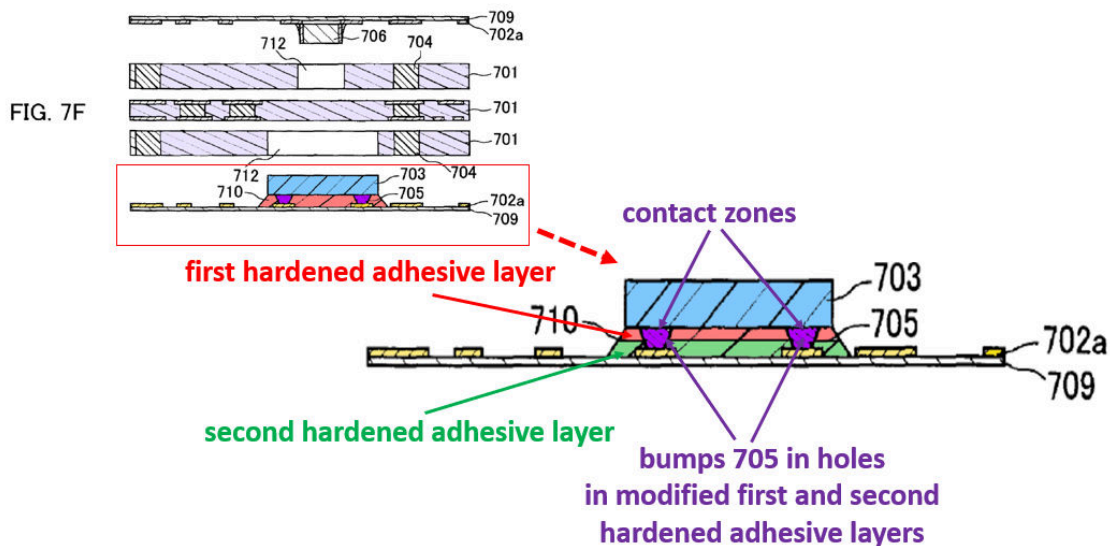


APPLE-1003, ¶159 (Composite Based on APPLE-1012, FIG. 7F (Annotated to show first and second hardened adhesive layers))

Accordingly, the Asahi-Capote combination provides Element [1e].

[1f]

The Asahi-Capote combination provides Element [1f]. APPLE-1003, ¶162. For example, the combined system includes holes in the first and second hardened adhesive layers at the locations of the contact zones on semiconductor 703 to accommodate stud bumps 705 extending from the contact zones. *Supra*, §VI.C.3, Analyses of Elements [1c]-[1e]; APPLE-1003, ¶162.



APPLE-1003, ¶162 (Composite Based on APPLE-1012, FIG. 7F (Annotated to show first and second hardened adhesive layers))

Both Asahi and Capote describe holes in the first and second hardened adhesive layers at the location of contact zones. Asahi describes the sealing resin 710 has holes at the locations of the contact zones of semiconductor 703 to accommodate stud bumps 705 formed on the contact zones, and the combined system would have likewise included a similar hole configuration when adhesive layers of two different compositions are used. APPLE-1012, 16:39-62, FIG. 7;

APPLE-1003, ¶162. Indeed, Capote's multilayer underfill encapsulant also has holes to accommodate or form solder bumps on an active surface of a chip.

APPLE-1005, 4:31-6:18 (disclosing various method embodiments for forming this structure), 6:25-27 ("a low-cost method for applying the solder bumps to a flip chip or flip chip substrate by creating holes in a pre-coated encapsulant"); APPLE-1003, ¶162.

[1g]

The Asahi-Capote combination provides Element [1g]. APPLE-1003, ¶¶163-164. As discussed above, the combined system uses conductive material such as "gold-gold junction, or stud bumps, and soldering" in the holes through the first and second hardened adhesive layers and in electrical connection with the contact zones of semiconductor 703 and wiring patterns 702a (the claimed conductive-pattern layer). *Supra*, §§VI.C.3, Analyses of Elements [1a], [1c] and [1f]; APPLE-1012, 16:39-66 (describing methods for mounting semiconductor 703 on wiring patterns 702a, thus forming mechanical and electrical connections, including "flip chip bonding," "gold-gold junction, or stud bumps... it is possible to apply different mounting processes (for instance, the soldering and the flip chip bonding"); FIG. 7E-7G (showing bumps 705 in connection with contact zones of semiconductor 703 and wiring patterns 702a); *see also* APPLE-1005, 1:32-35 ("solder bumps situated between the semiconductor chip and the substrate [in]

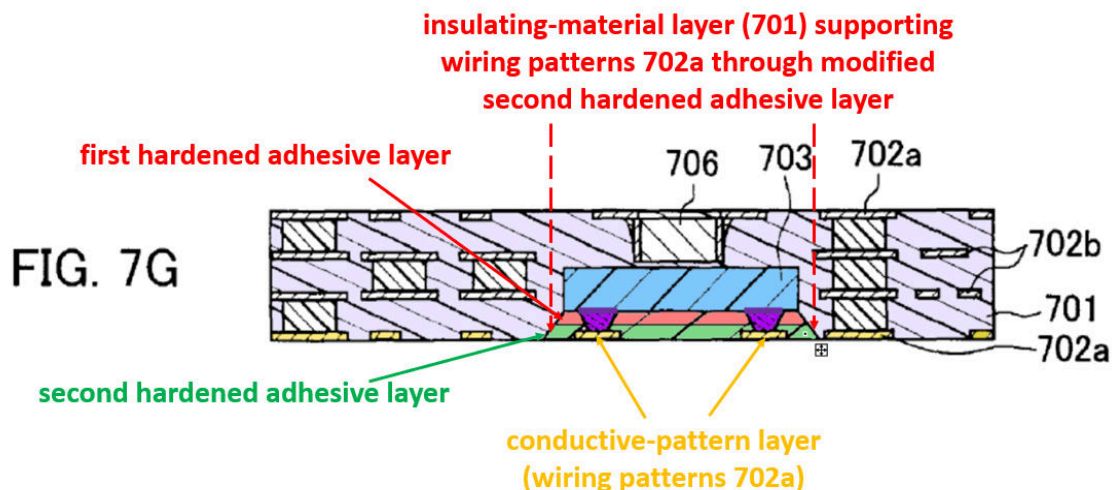
mechanical and electrical connections between the chip and substrate”), 11:29-30, 12:36-39, FIG. 12 (showing a similar structure with solder 102 in electrical connection with contact zones of chip 100 and metallization pads 106 on substrate 101); APPLE-1003, ¶¶163-164.

[1h]

Asahi-Capote renders Element [1h] obvious. *See* §VI.C.3, Analysis of Element [1d]; APPLE-1003, ¶165.

[2]

In the combined system, the second hardened adhesive layer covers wiring patterns 702a (*conductive-pattern layer*). The electric insulation layer 701 (*insulating-material layer*) supports portions of wiring patterns 702a via the second hardened adhesive layer. APPLE-1003, ¶166.



APPLE-1003, ¶166 (Composite Based on APPLE-1012, FIG. 7G (Annotated to show first and second hardened adhesive layers))

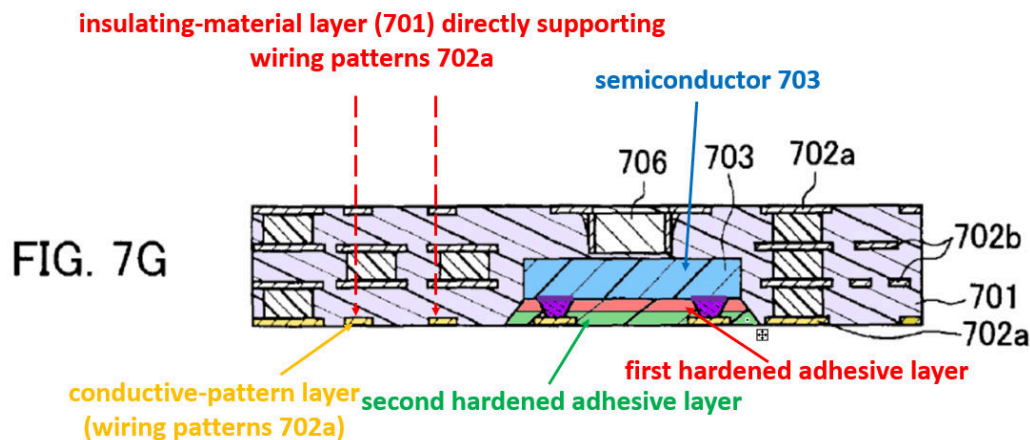
The portions of wiring patterns 702a contact the second hardened adhesive

layer such that they are supported by the electrical insulation layer via the second hardened adhesive layer. APPLE-1003, 166.

To be clear, Asahi illustrates the sealing resin's (e.g., sealing resin 710) bottom surface in contact with wiring patterns 702a has a greater area than that of its top surface in contact with semiconductor 703, such that the electric insulation layer 701 (insulating-material layer) supports portions of wiring patterns 702a via the sealing resin layer. APPLE-1012, FIG. 7G; APPLE-1003, ¶167.

[3]

The first and second hardened adhesive layers of the combined device are local and present at the location of semiconductor 703, consistent with the positioning described by Asahi and Capote. APPLE-1012, FIG. 7; 17:34-36; APPLE-1003, ¶168.



APPLE-1003, ¶168 (Composite Based on APPLE-1012, FIG. 7G (Annotated to show first and second hardened adhesive layers))

The electric insulation layer 701 (*insulating-material layer*) directly supports wiring patterns 702a (*conductive-pattern layer*) at locations outside of the hardened adhesive layers, as illustrated in FIG. 7G of Asahi, for example. *Id.*

[4pre]

To the extent the preamble is limiting, Asahi-Capote provides an electronic module. *See* §VI.C.3, Analysis of [1pre]; APPLE-1003, ¶169.

[4a]

See §VI.C.3, Analysis of [1c]; APPLE-1003, ¶170.

[4b]

See §VI.C.3, Analysis of [1d]; APPLE-1003, ¶171.

[4c]

See §VI.C.3, Analysis of [1e]; APPLE-1003, ¶171.

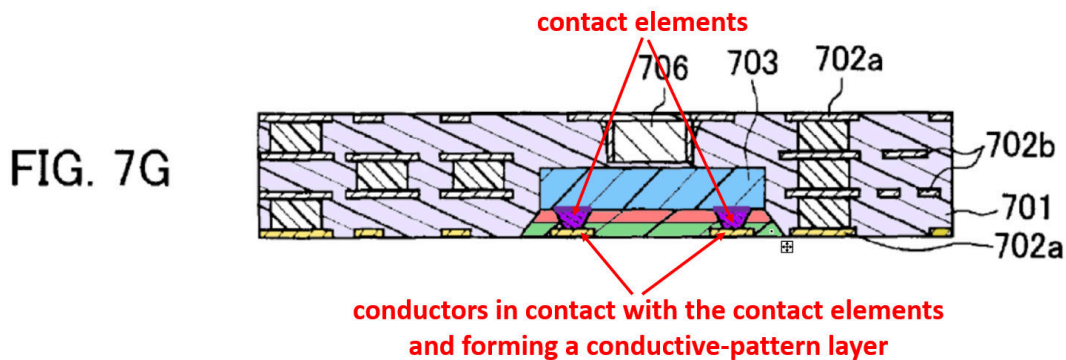
[4d]

As discussed above in Section VI.C.3, Analysis of [1g], conductive material such as “gold-gold junction, or stud bumps, and soldering” are in the holes extending through the modified first and second hardened adhesive layers and in mechanical and electrical connection with the contact zones of semiconductor 703. APPLE-1012, 16:39-66. Asahi expressly describes contact elements made of metal on the set of contact zones (e.g., “gold-gold junction”). Additionally, a POSITA would have recognized and found obvious that “stud bumps, and

soldering” described by Asahi for used in semiconductor packaging and flip-chip technology are made of metal, as metal is a known conductor suitable to effectuate the express objective of providing electrical connection through the hardened adhesive layers. APPLE-1003, ¶172.

[4e]

See §§VI.C.3, Analyses of [1a] (conductive-pattern layer), [1g] (conductive material in the holes and in electrical connection with the contact zones of the component and the conductive-pattern layer) and [4d] (contact elements). For example, Asahi describes “wiring patterns 702a” that include conductors arranged in patterns to form a conductive-pattern layer. APPLE-1012, 16:39-43, FIG. 7; APPLE-1003, ¶173. This is just like the example provided in the ’723 Patent for the recited conductors forming the conductive-pattern layer. APPLE-1001, 11:62 (referring to conductive-pattern layer 14 also as “conductors 14”), 12:11. The annotated figure below shows conductors on wiring patterns 702a in contact with conductor elements, the conductors arranged in patterns, thus forming a conductive-pattern layer.



APPLE-1003, ¶173 (Composite Based on APPLE-1012, FIG. 7G (Annotated to show first and second hardened adhesive layers))

[4f]

See §§VI.C.3, Analyses of [1b] (insulating-material layer) and [1c] (at least one component inside the insulating-material layer); APPLE-1003, ¶174.

[4g]

See §VI.C.3, Analysis of Element [1h]; APPLE-1003, ¶175.

[5]

In the Asahi-Capote combination, the at least one semiconductor component (e.g., Asahi’s “semiconductor element”) comprises at least one microcircuit.

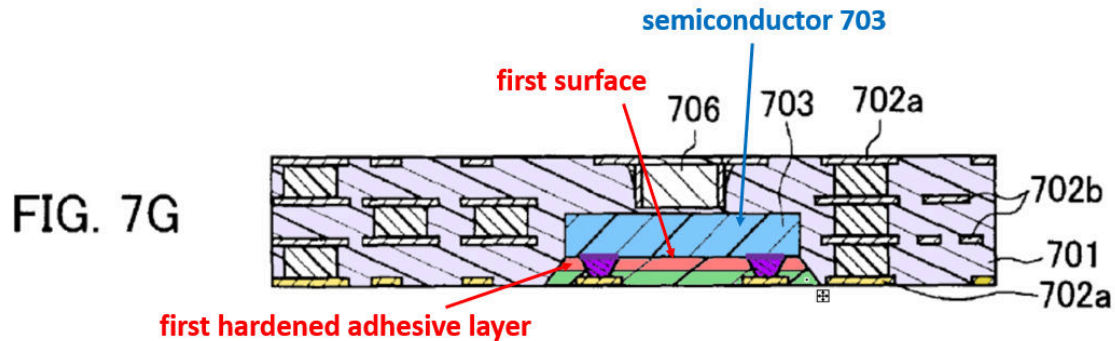
APPLE-1003, ¶176. For example, Asahi describes that “a semiconductor element such as an ... integrated circuit (IC), or an LSI [large scale integrated circuit] can be used,” thereby providing a microcircuit. APPLE-1012, 7:66-8:1. To be clear, a POSITA would have understood and found obvious from Asahi that such ICs or LSIs provide microcircuits; *see also e.g.*, APPLE-1005, 4:35 (“integrated circuit

chip”); APPLE-1003, ¶176 (explaining an integrated circuit is a conventional example of a microcircuit).

[6]⁷

For example, in the combined system, the top surface area of the modified first hardened adhesive layer extends to the edges of the first surface of the semiconductor component such that the top surface area is equal to the area of the first surface of semiconductor 703. *E.g.*, APPLE-1005, 9:43-48 (“The first portion encapsulating material [112] is first uniformly spread in liquid form across the surface of the chip 100 and between the solder bumps 108 covering the remainder of the chip 100, but leaving the tips of the solder bumps uncoated, then it is subsequently hardened.”); *see also*, 9:2-6; APPLE-1012, 10:45-53, 16:52-62 (“prevent a gap from being formed between the semiconductor 703 and the wiring patterns 702a,”), FIGS. 7-8. APPLE-1003, ¶¶177-178.

⁷ The “area of the first hardened adhesive layer is equal to the area of the first surface” is ambiguous and renders claim 6 indefinite. Yet, unpatentability of claim 6 can be determined here, because the prior art expressly describes such features. APPLE-1003, ¶177.



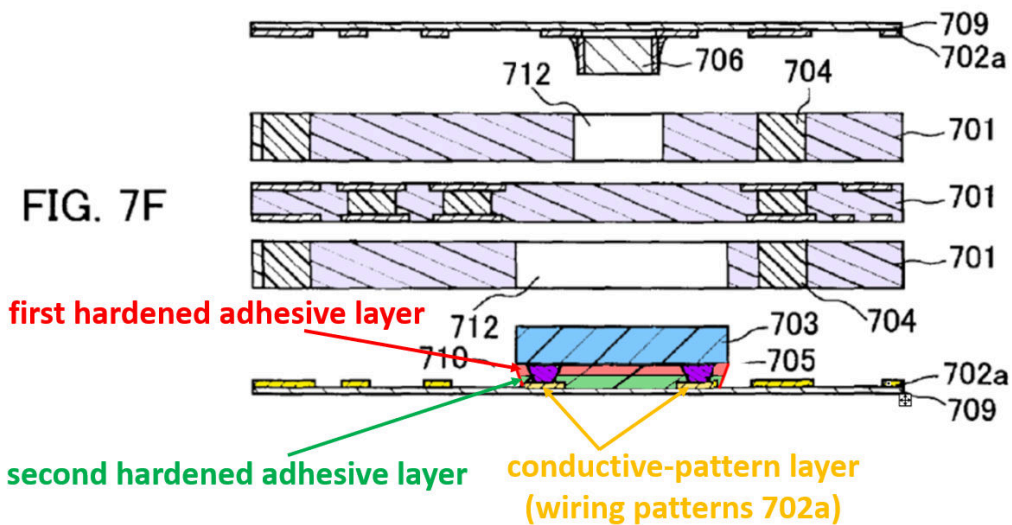
APPLE-1003, ¶178 (Composite Based on APPLE-1012, FIG. 7G
(Annotated to show first and second hardened adhesive layers))

[7]⁸

A POSITA would have found it obvious to implement the area of the first hardened adhesive layer to be greater than the area of the second hardened adhesive layer, based on Asahi and Capote's teachings regarding the relative size and positioning of the semiconductor 703 and conductive pattern portions 702 and pre-application of the two adhesive layers. For example, a POSITA would have recognized from Asahi (e.g., as shown in FIG. 7F) that the conductive pattern portions in contact with the contact elements (e.g., bumps 705) are inset from perimeter edges of the semiconductor component. A POSITA would have been

⁸ The "the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer" is ambiguous and renders claim 7 indefinite. Yet, unpatentability of claim 7 can be determined here, because the prior art expressly describes such features. APPLE-1003, ¶179.

prompted to pre-apply the first hardened adhesive layer to cover the entire first surface of the component and pre-apply the second hardened adhesive to extend to a width of the conductive pattern, to provide robust adhesion while reducing the material usage of the second adhesive. APPLE-1003, ¶180. In the resulting configuration, the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer. Moreover, Capote provides examples in which the first hardened adhesive layer has a width at least as great as the second hardened adhesive layer, further confirming that a POSITA would have readily implemented this predictable configuration. *See, e.g.*, APPLE-1005, FIGS. 26-27 (FIGS. 26 and 27 illustrate an embodiment where an encapsulant layer 39 coated on the chip 10 has a greater area than another encapsulant layer 37 coated on the substrate 20), 11:25-32. APPLE-1003, ¶181.



APPLE-1003, ¶180 (Composite Based on APPLE-1012, FIG. 7F (Annotated to show first and second hardened adhesive layers))

Additionally, a POSITA would have recognized and found obvious from Asahi and Capote that the area of the first hardened adhesive layer is greater than the area of the second hardened adhesive layer due to the presence of conductive pattern layer portions in the second hardened adhesive layer. APPLE-1003, ¶182. For example, while the contact elements are present through the hardened adhesive layers at discrete locations (e.g., extending from the contact zones of the semiconductor component), the conductors of the conductive-pattern layer may extend laterally across portions of the second hardened adhesive layer. *Id.*

The Asahi-Capote combination additionally renders claim 7 obvious because the relative areas of the first and second hardened adhesive layers amount to an obvious design choice. APPLE-1003, ¶183. For example, as discussed previously, Asahi describes sealing resin 710 between the semiconductor 703 and wiring pattern 702a to prevent a gap from being formed. APPLE-1012, 16:52-62; APPLE-1003, ¶183. A POSITA would have understood from Asahi and Capote (neither of which expressly exclude relative areas of the respective adhesive layers) that there are only three discrete possibilities for the relative areas of the first and second hardened adhesive layers: The first hardened adhesive layer coated on semiconductor 703 is: (1) greater than, (2) less than, or (3) equal to, the area of the second hardened adhesive layer coated on wiring patterns 702a. *Supra*, §VI.C.3, Analysis of Element [1d]; APPLE-1005, 4:30-6:8, APPLE-1003, ¶183. A

POSITA would have recognized and found obvious, in at least some scenarios, to implement the area of the first hardened adhesive layer to be greater than the area of the second hardened adhesive layer to accommodate different sizes and distances of contact zones on the active surface of the semiconductor 703 or the various patterns of conductors on the wiring patterns 702a, or to balance a secure adhesion and adequate protection of the semiconductor and wiring patterns with reduced adhesive material usage. APPLE-1003, ¶183; *KSR*, 550 U.S. at 421 (“obvious to try” when there are a “finite number” of identified, predictable solutions).

To be clear, the Asahi-Capote teachings actually provide more detail on the Claim 7 limitations than the '723 patent itself, which tersely mentions it is “possible that the first and second layers of adhesive are different in size and thickness,” and describes an example of a configuration opposite to claim 7 in which the “surface area of the second adhesive layer can be greater than the surface area of the first adhesive layer.” APPLE-1001, 7:35-44; *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994) (“[T]hat appellant did not provide the type of detail in his specification that he now argues is necessary in prior art references supports the Board’s finding that one skilled in the art would have known how to implement the features of the references.”).

[8]

For example, as discussed in Section VI.C.3, Analysis of Element [4d], Asahi describes that contact elements used to mount semiconductor 703 on the wiring patterns 702a include a “gold-gold junction” where “junction” indicates at least two layers of gold that come into contact with each other, thus providing the claimed a first layer of metal and at least one second layer of metal. APPLE-1003, ¶184. Additionally, Asahi describes use of “stud bumps, and soldering.” *Id.* A POSITA would have understood and found obvious that stud bumps used in semiconductor packaging and flip-chip technology often have plating layers over a metal core for enhanced electrical conductivity and signal integrity, as well as improved reliability and lifespan of the solder bumps, providing a first layer of metal and at least one second layer of metal and furthering Asahi and Capote’s electrical connection objective. APPLE-1003, ¶184.

[9]

For example, as discussed in Section VI.C.3, Analysis of Element [4d], the contact elements of the combined system include “gold-gold junction, or stud bumps, and soldering” using “flip chip bonding” to form contacts with the metal conductors formed on wiring patterns 702a (e.g., a metal foil laminated on the electric insulation layer 701, with its surface plated). APPLE-1012, 3:39-44 (“wiring patterns preferably are made of at least one selected from a metal foil, a

lead frame, and a conductive resin composition”), 7:50-52 (“by plating surfaces of the wiring patterns 102a and 102b, their corrosion resistance and electric conductivities can be improved”), Cls. 5, 18; APPLE-1003, ¶185. Contact elements formed using “gold-gold junction” provides a metal-on-metal contact with the contact zones of the component (such as gold-plated copper pads commonly used on semiconductor dies) such that the contact elements are in metallurgical contact with the respective contact zones and the respective conductors. APPLE-1012, 16:47-51; APPLE-1003, ¶185. Alternatively, when contact elements are formed by stud bumps, they are typically metal and thus also form metal-on-metal contact (metallurgical contact) with the contact zones and conductors. *Supra*, §VI.C.3, Analysis of Claim [8]; APPLE-1003, ¶185.

Similarly, Capote describes contacts of solder bumps formed over existing metal structure of “a matching pattern of solderable gold-plated copper pads, consisting of approximately 0.8 mm thick BT resin/glass laminate with approximately 30 microns of copper foil.” APPLE-1005, 12:20-24, 11:66-12:3 (“a bumped semiconductor chip, part FBT-250 available from Flip Chip Technologies”); *see also id.*, 5:7-9 (“reflowing the solder bumps to electrically connect the contacts of the integrated circuit chip to the pads of the substrate”), 5:33-36, 5:58-60, 6:16-18, 6:22, 12:36-45; APPLE-1003, ¶186. These metal-touching-metal contacts between the contact elements and the conductors of the

wiring patterns and between the contact elements and the contact zones of the component provide metallurgical contact. APPLE-1003, ¶187.

VII. §325(D)

The references of Grounds 1A-2 were not applied in a rejection during prosecution. This Petition thus does not involve the same or substantially the same art or arguments previously presented, ending the *Advanced Bionics* inquiry in favor of institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-9 (P.T.A.B. February 13, 2020) (precedential).

To be clear, regarding the first prong in the *Advanced Bionics* analysis, the Board held when neither the combination of references nor similar prior art had been examined, the prosecution history lacks overlapping arguments. *Godbersen-Smith Constr. Co., D/B/A/ Gomaco Corp., v. Guntert & Zimmerman Const. Div., Inc.* IPR2021-00050, Paper 24 at 19-21 (PTAB May 7, 2021). As the first prong is unmet, the Board does not need to proceed to the second prong. *Id.* at 21.

Tuominen967Pub, although a publication of the '023 Application to which the '723 Patent claims priority as a continuation-in-part, was never considered as prior art or applied in a rejection. Likewise, Asahi and Capote were not before the Examiner. The Petition presents these references in a manner that is not cumulative with the references cited during prosecution. Indeed, the only

reference applied by the examiner, *Mowatt*, does not describe electronic modules with two hardened adhesive layers as claimed by the '723 Patent, which the examiner acknowledged. APPLE-1002, 56. Each Ground of the Petition thus presents never-considered references that disclose the very features that formed the Examiner's stated reasons for allowance. *SHDS, Inc., et al. v. Truinject Corp.*, IPR2020-00935, Paper 12 at 9-12 (PTAB Nov. 17, 2020) (declining to deny institution under 325(d) where "the noted limitation is the very one that, in the Examiner's view, placed the claims . . . into a condition for allowance.").

The Board need not reach part 2 of the *Advanced Bionics* framework because part 1 is not satisfied. Even if the Board were to reach the second part, original examination involved multiple material errors in failing to properly evaluate the faulty priority claim of the '723 patent and failing to consider the relevant disclosures of Tuominen967Pub, Asahi, and Capote.

Here, the examiner erred by failing to recognize Tuominen967Pub as prior art. As discussed above (Section III.C), Tuominen967Pub does not provide written description support for the limitation that "the first hardened adhesive layer has a first composition and the second hardened adhesive layer has a second composition different from the first composition," which was first recited in the continuation-in-part application that led to the '723 patent.

The Petition relies on disclosures of Tuominen967Pub that are not reflected in the Examiner's analysis during prosecution, both alone and in combination with Capote. Additionally, the Petition relies on Asahi in combination with Capote. None of these pertinent disclosures were properly considered, especially in view of the testimony evidence set forth herein.

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314

Essentially all of the *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written Decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors. Moreover, a Motion to Transfer to the Northern District of California remains pending. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while litigation remains in early stages. Motion to Transfer remains

pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds, outweighing any inefficiencies borne of parallel litigation.

IX. FEES

Petitioner authorizes the USPTO to charge any necessary fees to Deposit Account No. 06-1050.

X. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple Inc. is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the '723 Patent. The '723 Patent is the subject of *ImberaTek LLC v. Apple Inc.* 1-24-cv-00129 (WDTX), filed February 5, 2024, *ImberaTek LLC v. Samsung Electronics Co., Ltd. et al* 2-22-cv-00233 (EDTX), filed June 24, 2022; and *Samsung Electronics Co., Ltd. et al v. ImberaTek LLC* IPR2023-00044 (PTAB), filed October 12, 2022.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0194IP1@fr.com.

Respectfully submitted,

Dated: February 5, 2025

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(Control No. IPR2025-00580)

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,680 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 5, 2025

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Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 5, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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