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Title:	METHOD FOR EMBEDDING A COMPONENT IN A BASE	

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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 8,368,201 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 8,368,201 ("the '201 Patent")
APPLE-1002	U.S. Patent No. 8,368,201 File History
APPLE-1003	Declaration of Dr. Dean Neikirk
APPLE-1004	Certified Translation of JP Application Publication 2001-339165A ("Sakamoto")
APPLE-1005	U.S. Patent Application Publication No. 2002/0175402 ("McCormack")
APPLE-1006	U.S. Patent No. 6,489,685 ("Asahi")
APPLE-1007	U.S. Patent Application Publication No. 2001/0030059 ("Sugaya")
APPLE-1008	U.S. Patent No. 7,989,944 ("the '944 Patent")
APPLE-1009	U.S. Patent No. 7,294,529 ("the '529 Patent")
APPLE-1010	U.S. Patent No. 8,222,723 ("the '723 Patent")
APPLE-1011	Certified Translation of JP Patent No. 3207174 ("Hayashi")
APPLE-1012	Certified Translation of JP Patent Application Publication No. 2002-016327 ("Eiji")
APPLE-1013	U.S. Patent No. 6,335,571 ("Capote")
APPLE-1014	U.S. Patent No. 6,297,551 ("Dudderar")
APPLE-1015	U.S. Patent No. 6,404,052 ("Kurita")
APPLE-1016	Certified Translation of JP Patent Application Publication No. 2001-068624A ("Imoto")
APPLE-1017	Certified Translation of PCT Publication No. WO 00/09623 ("Watanabe")

APPLE-1018	U.S. Patent No. 4,179,802 ("Joshi")
APPLE-1019	U.S. Patent No. 5,608,262 ("Degani")
APPLE-1020	U.S. Patent No. 5,321,210 ("Kimbara")
APPLE-1021	U.S. Patent No. 5,146,674 ("Frankeny")
APPLE-1022	JP Patent Application Publication No. 2001-339165A ("Sakamoto")
APPLE-1023	JP Patent No. 3207174 ("Hayashi")
APPLE-1024	JP Patent Application Publication No. 2002-016327 ("Eiji")
APPLE-1025	JP Patent Application Publication No. 2001-068624A ("Imoto")
APPLE-1026	PCT Publication No. WO00/09623 ("Watanabe")
APPLE-1027	Certified Translation of JP Patent Application Publication No. 2001-156457 ("Takayama")
APPLE-1028	JP Patent Application Publication No. 2001-156457 ("Takayama")

LISTING OF CLAIMS

Claim 1	
[1pre]	An electronic module, comprising
[1a]	a baseboard having a first surface and a second surface;
[1b]	a hardened insulating polymer layer on the second surface of the baseboard;
[1c]	at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;
[1d]	conductive patterns on the hardened insulting polymer layer; and
[1e]	conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

I. INTRODUCTION

Apple Inc. ("Apple" or "Petitioner") petitions for IPR of claim 1 ("Challenged Claim") of U.S. Patent No. 8,368,201 ("the '201 Patent").

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Petitioner certifies that IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. § 42.104(b) and Relief Requested

Petitioner requests IPR based on the following grounds, as further explained in this Petition and supported by the Declaration of Dr. Neikirk (APPLE-1003).

Ground	'201 Patent Claims	Basis
1	1	§102 and §103 – Hayashi
2A	1	§102 and §103 – Takayama
2B	1	§103 – Takayama-Hayashi
3A	1	§103 – McCormack
3B	1	§103 – McCormack-Sakamoto
4	1	§102 and §103 – Sakamoto
5A	1	§102 and §103 – Asahi
5B	1	§103 – Asahi-Sakamoto
6	1	§102 and §103 – Sugaya

Each reference pre-dates the '201 Patent's earliest possible priority date (January 31, 2002; "Critical Date") and qualifies as prior art.

Reference	Date	Pre-AIA Status
Sakamoto (APPLE-1004)	Dec. 7, 2001 (published)	§102(b)
McCormack (APPLE-1005)	May 23, 2001 (filed)	§102(e)
Asahi (APPLE-1006)	Jan. 3, 2002 (filed)	§102(e)
Sugaya (APPLE-1007)	Oct. 18, 2001 (published)/Dec. 15, 2000 (filed)	§§102(a)/(b)/(e)
Hayashi (APPLE-1011)	Sep. 10, 2001(published)	§§102(a)/(b)
Takayama (APPLE-1027)	Jun. 8, 2001 (published)	§102(a)/(b)

Sakamoto (APPLE-1004), Hayashi (APPLE-1011), and Takayama (APPLE-1027) are certified English translations of JP2001-339165A ("Sakamoto"/APPLE-1022), JP3207174 ("Hayashi"/APPLE-1023), and JP2001-156457 ("Takayama" APPLE-1028). The Grounds are directed to the prior art references (APPLE-1022, APPLE-1023, APPLE-1028), for which the translations are cited throughout to identify relevant aspects thereof.

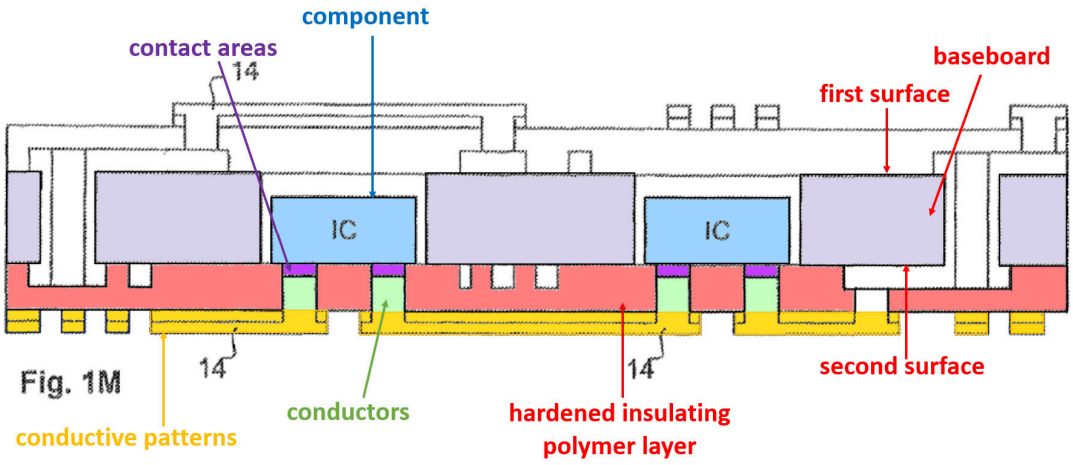
While Asahi and a family member of Sugaya were cited on the face of the '201 patent, none of the above references were applied in a substantive office action.

III. SUMMARY OF THE '201 PATENT

A. Brief Description

The '201 Patent recites a method for embedding semiconductor components in a base, such as a circuit board. APPLE-1001, Abstract, 1:11-12. The '201

Patent includes a single claim broadly directed to an "electronic module." APPLE-1001, Abstract, Cl. 1. As shown in the annotated Figure 1M below, the electronic module includes a baseboard having a first surface and a second surface; one or more components embedded in the baseboard and having contact areas on its contact surface; a hardened insulating polymer layer on the second surface of the baseboard, with the component's contact surface against this hardened insulating polymer layer; conductive patterns on the hardened insulating polymer layer; and conductors within the hardened insulating polymer layer for forming electrical contacts between the conductive patterns and the components. APPLE-1001, FIG. 1M, Cl. 1.



APPLE-1001, FIG. 1M (Annotated)

While the '201 Patent touts these routine aspects as "invention," they were not innovative. Those of skills in the art were aware of the structure having electrical components embedded in a base like circuit board to achieve

miniaturization of electronic devices, which were described in such references as McCormack, Sakamoto, Hayashi, Takayama, Asahi and Sugaya. APPLE-1003, ¶¶60-220; *infra*, §VI.

B. Prosecution History Summary

The Examiner issued a notice of allowance without a single prior art rejection against the claims, and without any substantive discussion of the prior art. APPLE-1002, 29-36. Notably, the Examiner's statement of reasons for allowance indicated that the "prior art of record does not teach or suggest, singularly or in combination, at least the limitations of independent claim 1," reciting the entirety of the elements of claim 1. *Id.*, 34-35. These features, however, were known to a POSITA, and the claims allowed without application of pertinent prior art discussed herein.

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the '201 Patent (a "POSITA") would have had at least a Bachelor's degree in electrical engineering, material science, applied physics, or a related technical field, and at least 3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent; additional education could substitute for experience. APPLE-1003, ¶23.

V. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. The Board has repeatedly explained that "claim terms need only be construed to the extent necessary to resolve the controversy," and for purpose of the particular Grounds in this Petition, no formal construction is necessary because the prior art presented below satisfies the claims under any reasonable construction consistent with *Phillips*. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011)[1].

VI. DETAILED EXPLANATION OF GROUNDS

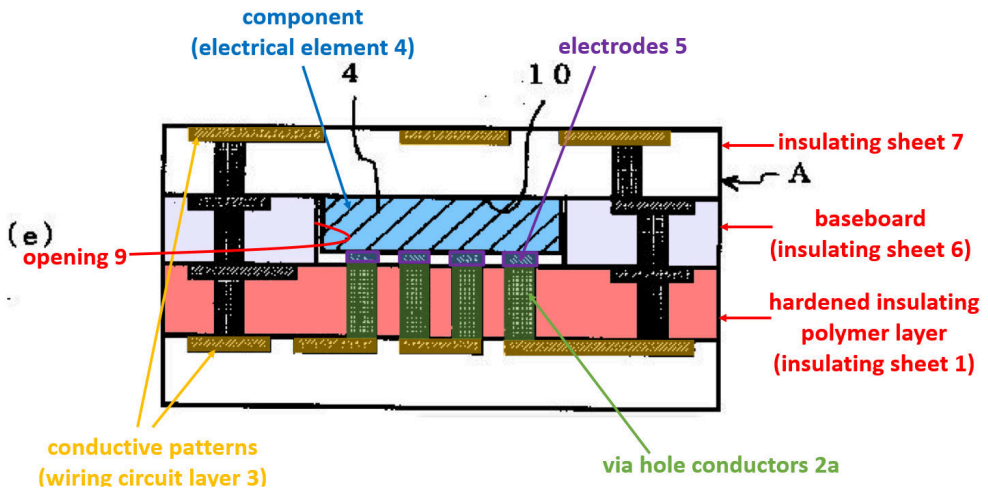
A. GROUND 1 – Hayashi anticipates or renders obvious Claim 1

1. Hayashi[2]

[1] Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

[2] General descriptions provided for this and other references and combinations are incorporated into each subsection and mapping of the claims that includes citations to these references. All emphasis is added unless otherwise indicated.

Hayashi describes "a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate, and to a manufacturing method for such a wiring substrate," where examples of the electrical element include "a semiconductor element." APPLE-1011, [0001]-[0003], *see also id.*, Title, Cls. 1, 2, [0007], [0027], [0038], [0041], FIG. 1(e) (reproduced below); APPLE-1003, ¶60. Figure 1(e) below shows electrical element 4 stowed away in an opening 9 formed in an insulating sheet 6 which is laminated directly above insulating sheet 1 and below insulating sheet 7, "so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7." APPLE-1011, [0028], [0039]-[0040], FIGS. 1(d)-(e); APPLE-1003, ¶61. A "wiring circuit layer 3" as a "circuit pattern" is provided on both sides of and within a portion of the board composed of insulating sheets 1, 6, 7. APPLE-1011, [0024]-[0025]; *see also*, Cl. 1, [0009], [0012], [0028], [0036]-[0038], [0041], FIGS. 1(b)-(e) (showing multiple conductive patterns of wiring circuit layer 3 on both sides of insulating sheets 1, 6 and 7, respectively); APPLE-1003, ¶62. Electrical element 4 (through its electrodes 5) is connected to wiring circuit layer 3 through via hole conductors 2a within insulating sheet 1. APPLE-1011, [0008]- [0012], [0014], [0018], [0020], [0024], [0026], [0030], [0035], [0038], [0041], Cl. 1, 2; APPLE-1003, ¶62.



APPLE-1003, ¶61 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi's insulating sheet 1 contains a thermoset resin with a curing temperature T_1 with via holes penetrating in a thickness direction formed in the insulating sheet 1, and such thermoset resin has heat resistance and mechanical strength. APPLE-1011, FIG. 1(a), [0012], [0015] (list of different polymers); APPLE-1003, ¶63. Insulating sheet 1 is hardened through thermal curing. APPLE-1011, [0010], [0012], [0013], [0019], [0029], [0032], [0035], [0040], Cls. 1, 2; APPLE-1003, ¶63.

2. Application to Challenged Claim

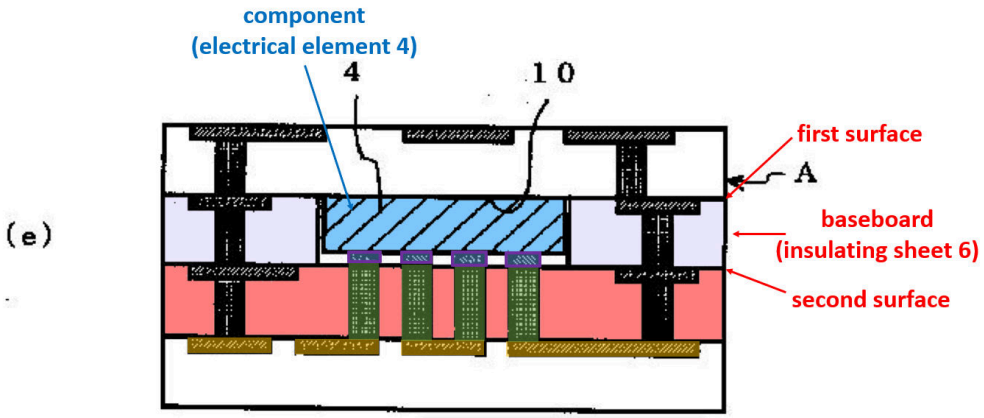
Element [1pre] An electronic module, comprising

If the preamble is deemed limiting, Hayashi teaches [1pre]. APPLE-1003, ¶95. For example, Hayashi discloses "a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate," and

describes a "semiconductor element" as an example of the electrical element. APPLE-1011, [0001], [0007]. Hayashi's electrical element mounted wiring board provides an electronic module. APPLE-1003, ¶95. Indeed, it is just like the '201 Patent's description of an electronic module with electrical components embedded within a base. APPLE-1001, Abstract 1:11-24, 1:63-67; APPLE-1003, ¶95.

Element [1a] a baseboard having a first surface and a second surface;

Hayashi discloses Element [1a]. APPLE-1003, ¶¶96-99. For example, Hayashi describes that "an opening 9 for housing the electrical element 4 is formed in insulating sheet 6 and laminated directly above insulating sheet 1 so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7." APPLE-1011, [0028], FIG. 1(e).



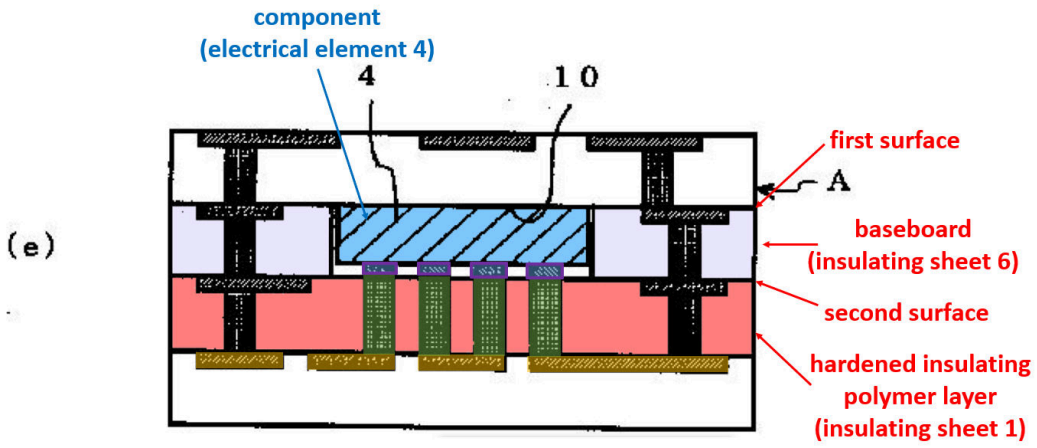
APPLE-1003, ¶96 (APPLE-1011, FIG. 1(e) (Annotated))

Figure 1(e) shows insulating sheet 6 (***baseboard***) ***having a first surface and a second surface***. *Id.*; *see also id.*, [0001] ("a wiring substrate with a mounted

electrical element, in which the electrical element is built into an insulating substrate"), [0039]. Insulating sheet 6 with embedded electrical element 4 as part of the multilayer wiring board is made of insulating material such as "epoxy resin," and "[a] woven fabric, non-woven fabric composed of glass or aramid resin, etc. impregnated with one of the resins described above may also be used." APPLE-1011, [0015]-[0016]. This is just like the baseboard described in the '201 Patent. *Compare* APPLE-1011, [0015]-[0016] *with* APPLE-1001, 3:48-57 ("The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board, …"); 2:22-26 ("a circuit board can be manufactured with the semiconductor components embedded inside it"); APPLE-1003, ¶¶97-99.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Hayashi discloses Element [1b]. APPLE-1003, ¶¶100-102. For example, Hayashi's "insulating sheet 1" provides a ***hardened insulating polymer layer***. APPLE-1003, ¶100. Figure 1(e) illustrates ***hardened insulating polymer layer*** (e.g., insulating sheet 1) ***on the second surface of*** the ***baseboard*** (e.g., insulating sheet 6). *Supra*, §VI.A.2, Analysis of Element [1a]; APPLE-1003, ¶100.



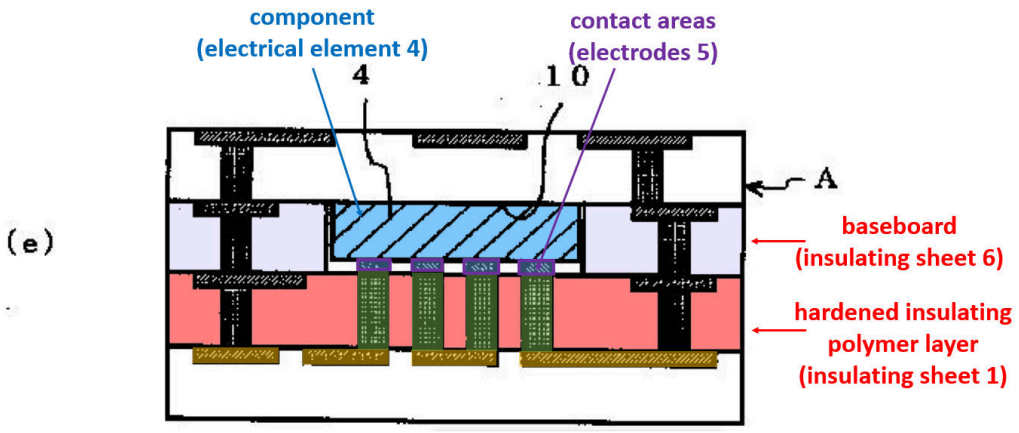
APPLE-1003, ¶100 (APPLE-1011, FIG. 1(e) (Annotated))

A POSITA would have recognized, from Hayashi's description, that insulating sheet provides a ***polymer*** layer. APPLE-1003, ¶101. Hayashi explains that "first, as shown in FIG. 1 (a), a soft (B-stage state) insulating sheet 1 containing a thermosetting resin with thermosetting temperature T_1 is formed and via-holes passing through in the thickness direction are formed in the insulating sheet 1." APPLE-1011, [0012]. Hayashi further explains, "the thermoset resin forming the insulating sheet [1] is not particularly limited as long as the thermoset resin has electrical characteristics, heat resistance, and mechanical strength as an insulating material." *Id.*, [0015].

Additionally, the insulating sheet 1 is ***hardened*** through curing. APPLE-1011, [0029]; *see also id.*, [0010], [0012], [0013], [0019], [0032], [0035], [0040] ("hardening process"), Cls. 1, 2; APPLE-1001, 5:32-35; APPLE-1003, ¶102.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

Hayashi discloses Element [1c]. APPLE-1003, ¶¶103-109. For example, Hayashi's "electrical element 4" provides ***at least one component within the baseboard***. APPLE-1011, [0026] ("an electrical element 4 is mounted on the surface of the insulating sheet 1, and the electrodes 5 formed on the back surface of the electrical element 4 are brought into contact with the exposed portions on the end surfaces of the via-hole conductors 2a"); *see also*, Title, Cls. 1, 2, [0001] ("a wiring substrate with a mounted electrical element, in which the electrical element is built into an insulating substrate"), [0002]-[0003], [0005], [0007], [0027]-[0028], [0038]-[0041], FIG. 1(e); APPLE-1003, ¶103. Hayashi describes that the electrical element 4 is stowed in an opening 9 "formed in insulating sheet 6 and laminated directly above insulating sheet 1, so that electrical element 4 can be housed and mounted in a hermetically sealed void formed by insulating sheets 1, 6, 7." APPLE-1011, [0028], [0031], [0039], FIG. 1(e) (showing electrical element 4 embedded within insulating sheet 6 as part of the multilayer wiring board A); APPLE-1003, ¶104.



APPLE-1003, ¶104 (APPLE-1011, FIG. 1(e) (Annotated))

Hayashi further describes "electrodes 5 formed on the back surface of the electrical element 4", depicted in FIG. 1(e) as contacts pads of the electrical element 4, that provide ***contact areas on a first surface of the component***. APPLE-1011, [0026], [0030], [0038], FIGS. 1(c), 1(e); APPLE-1003, ¶105.

In the finished module, the first surface of the electrical element (***component***) is against the insulating sheet (***hardened insulating polymer layer***). For example, although FIG. 1(e) shows a gap between the first surface of the electrical component and the insulating sheet, Hayashi explains that gaps will be minimized to leave "almost no void." APPLE-1011, FIG. 1(e), [0040], [0032]; APPLE-1003, ¶105. Specifically, Hayashi explains that "it is preferable to make the thermosetting resin [of the insulating sheets] flow before curing to minimize a void with an insulating phase at the periphery of the electrical element 4 to improve reliability." APPLE-1011, FIG. 1(e), [0032]. Hayashi further explains,

"[t]he opening in the insulating sheet contracted due to the flow of resin caused by heating, and the insulating layer and the chip were **bonded closely together**, leaving almost no void between the chip and the insulating layer." *Id.*, [0040]. Accordingly, in the resulting module, the insulating sheet 1 contacts at least a portion of the first surface of the electrical component due to the flow of the insulating layer resin, such that the first surface of the component is against the hardened insulating polymer layer. Indeed, nothing in the plain language of the claim recites that there is no gap anywhere between the first surface and the hardened insulating polymer layer. APPLE-1003, ¶¶105-106.

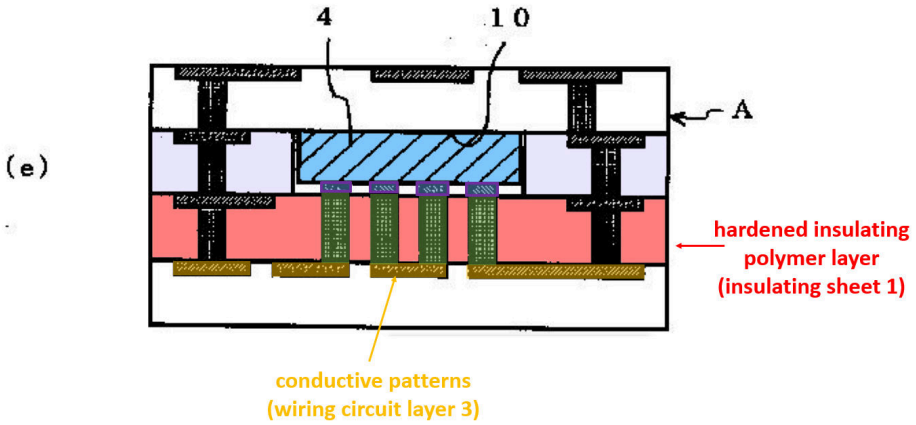
Additionally, a POSITA would have found it obvious, based on Hayashi's express preference to minimize (e.g., to the point of partial or complete elimination) a void between the first surface of electrical element 4 and a surface of insulating sheet 1 (***the hardened insulating polymer layer***), to flow the resin such that the first surface of the electrical element and the insulating sheet are in direct contact in the finished module. APPLE-1003, ¶107. A POSITA would have been prompted, based on Hayashi's suggestions, to achieve improved reliability and structural integrity due to two surfaces touching. *Id.* Indeed, a POSITA would have recognized that these benefits would result from contact in at least in some places without eliminating all gaps completely across the entirety of the first surface, or by providing contact completely across the entirety of the first surface.

Id. Contact between the component and insulating layer would have predictably helped maintain the component securely in place, promoting secure electrical contact. *Id.* Moreover, a POSITA would have had a reasonable expectation of success, especially because Hayashi expressly teaches the flow of resin for the purpose of minimizing potential void, and promoting contact, between the electrical component and insulating layer. APPLE-1003, ¶¶108-109.

Accordingly, through disclosure of "electrical element 4" with electrodes 5 (e.g., contact pads) on its back surface, Hayashi discloses Element [1c].

Element [1d] conductive patterns on the hardened insulting polymer layer; and

Hayashi discloses Element [1d]. APPLE-1003, ¶¶110-112. Hayashi describes a "wiring circuit layer 3" that is "formed on the front or back surface of the insulating sheet 1." APPLE-1011, [0024]; *see also id.*, [0009], [0036] ("The resulting wiring circuit layer had **a fine pattern** with a line width of 20 μm and a spacing of 20 μm between wiring."), [0038], FIG. 1(e), Cl. 1. Hayashi further explains that the wiring circuit layer 3 is formed by "affixing **metal foil** to a surface of the insulating sheet 1 and performing etching to form **a circuit pattern**" or "affixing **metal foil** to a transfer film surface, etching the metal foil to form **a circuit pattern**, and then transferring the circuit pattern formed of metal foil onto a sheet of the insulating sheet 1 surface." APPLE-1011, [0024].



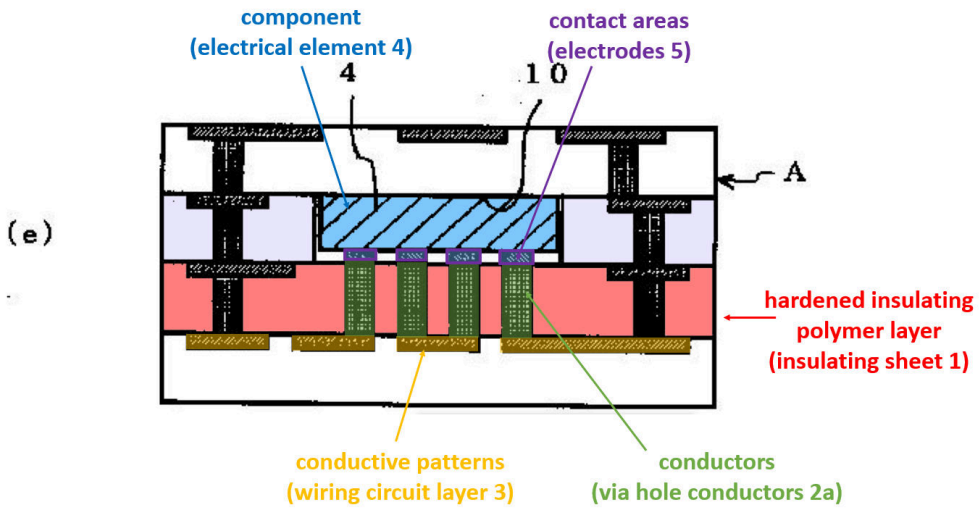
APPLE-1003, ¶112 (APPLE-1011, FIG. 1(e) (Annotated))

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

Hayashi discloses Element [1e]. APPLE-1003, ¶¶113-115. For example, Hayashi's "via-hole conductors 2a" provide ***conductors within the hardened insulating polymer layer***. APPLE-1003, ¶¶113-115. Hayashi describes that "via-holes passing through in the thickness direction are formed in the insulating sheet 1," and "the via-holes that are connected to the electrodes of the electrical element are filled with an conductive paste while performing screen printing or suctioning to form via-hole conductors 2a for connecting the electrical element." APPLE-1011, [0012].

Further, Hayashi describes that via hole conductor 2a is electrically connected to the electrode 5 of electrical element 4. APPLE-1011, [0012], [0018] ("the via-hole conductors 2a connected to the electrodes of the electrical element"),

[0026] ("the electrodes 5 formed on the back surface of the electrical element 4 are brought into contact with the exposed portions on the end surfaces of the via-hole conductors 2a"), [0030], [0031], [0038], Cls, 1 & 2, FIG. 1; *see also* [0034] ("The manufacturing method of the present invention allows for the connection of electrical elements to a wiring substrate…"), [0041]-[0042]. Figure 1(e) showing via hole conductors 2a ***within*** insulating sheet 1 ***for forming electrical contacts between*** wiring circuit layer 3 ***and at least some of the contact areas of*** electrical element 4. APPLE-1003, ¶114-115.



APPLE-1003, ¶115 (APPLE-1011, FIG. 1(e) (Annotated))

B. GROUND 2A – Takayama anticipates or renders obvious Claim 1

1. Takayama

Takayama describes "[a] method for manufacturing an electronic circuit device with a multilayer circuit board and a chip-type electronic component having

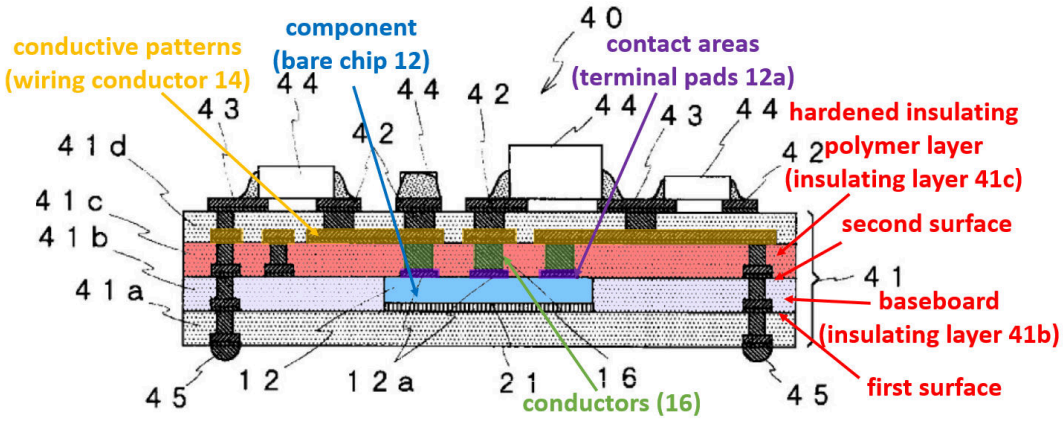
terminal pads on a main surface[.]" APPLE-1027, Cl. 1. The chip-shaped electronic components of Takayama's electronic circuit device are "embedded inside [the] multilayer circuit board." *See e.g.*, *id.*, [0008], [0019]-[0021] ("bare chips of semiconductor integrated circuit elements have been embedded"), [0023] ("a bare chip 12 of a semiconductor integrated circuit is embedded inside a multilayer circuit board 11"); *see also* Abstract, [0006], FIGS. 1-17. APPLE-1003, ¶¶64-66.

Figure 17 below illustrates bare chip 12 with terminal pads 12a embedded in an insulating layer 41b, and "[p]olyimide or some other resin may be used in the insulating layer[.]" APPLE-1027, [0029]. Note that FIG. 17's layer 41b formed using the same process of forming layer 23 (11b) of FIG. 3 is done to a depth that does not cover the component. *Id.*, [0051], FIGS. 3, 17; APPLE-1003, ¶67. The insulating layer 41b has a first surface against layer 41a and a second surface against layer 41c. *Id.*, FIG. 17.

Insulating layer 41c provided on the insulating layer 41b plays the same role as the spin coated layer in embodiment 1 coating the active surface of the bare chip 12 (e.g., "to a thickness of 20 μm") and is an "epoxy-based photosensitive resin," "[p]olyimide or some other resin." *Id.*, [0029], [0051]. The insulating layers are "cured" after drying. *Id.*, [0030]. Wiring conductors 14 are formed on the surface

of insulating layer 41c with a wiring pattern. *Id.*, [0032]-[0037], FIG. 17. Via holes are formed in the insulating layer on the terminal pads 12a of the bare chip 12 and are filled with conductor 16 by a copper plating process. *Id.*, Abstract, [0008], [0012], [0025], [0045], [0053], FIG. 17, Cl. 1. APPLE-1003, ¶¶68-71.

FIG. 17



APPLE-1003, ¶66 (APPLE-1027, FIG. 17 (Annotated))

2. Application to Challenged Claim

Element [1pre] An electronic module, comprising

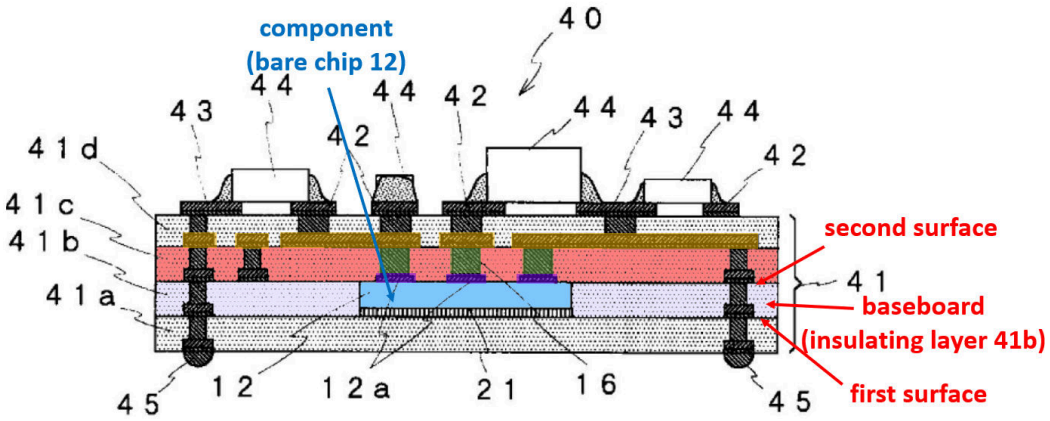
If the preamble is deemed limiting, Takayama teaches [1pre]. APPLE-1003, ¶117. For example, Takayama describes "an electronic circuit device with a multilayer circuit board and a chip-type electronic component having terminal pads on a main surface[.]" APPLE-1027, Cl. 1, Abstract, [0023] ("an electronic circuit device in which a bare chip 12 of a semiconductor integrated circuit is embedded inside a multilayer circuit board 11"). A POSITA would have recognized that

Takayama's electronic circuit having semiconductor chips embedded in a multilayer circuit board is an electronic module. APPLE-1003, ¶117. Indeed, it is just like the '201 Patent's description of an electronic module with semiconductor components embedded within a circuit board. APPLE-1001, Abstract 1:11-24, 1:63-67; APPLE-1003, ¶117.

Element [1a] a baseboard having a first surface and a second surface;

Takayama discloses Element [1a]. APPLE-1003, ¶¶118-122. For example, Takayama describes insulating layer 41b with bare chip 12 embedded therein. APPLE-1027, FIG. 17; *see also* Abstract, [0008], [0019]-[0021], [0023], [0029] [0051] ("multilayer circuit board 41 with four insulating layers 41a-41d"). As shown in FIG. 17, insulating layer 41b is thin enough to not cover the active surface of the bare chip 12. Insulating layer 41b has a material like layer 23 of the first embodiment, e.g., "[p]olyimide or some other resin …as long as it is resistant to the plating solution," and is applied using spin deposition, like layer 23. APPLE-1027, [0029], [0051]; APPLE-1003, ¶¶118-119. Annotated FIG. 17 below illustrates bare chip 12 embedded in insulating layer 41b, which has a first surface against layer 41a and a second surface against layer 41c.

FIG. 17



APPLE-1003, ¶119 (APPLE-1027, FIG. 17 (Annotated))

Insulating layer 41b housing a semiconductor chip is made of "[p]olyimide or some other resin," which is just like the '201 Patent's ***baseboard***. *Compare* APPLE-1001, 2:22-26 ("With the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it."), 3:23-33, 3:48-57 ("an organic board" or "an inorganic board" for baseboard 1) *with e.g.,* APPLE-1027, Abstract, [0021] ("bare chips of semiconductor integrated circuit elements have been embedded"), [0023], [0029] ("[p]olyimide or some other resin"), FIG. 17. APPLE-1003, ¶120.

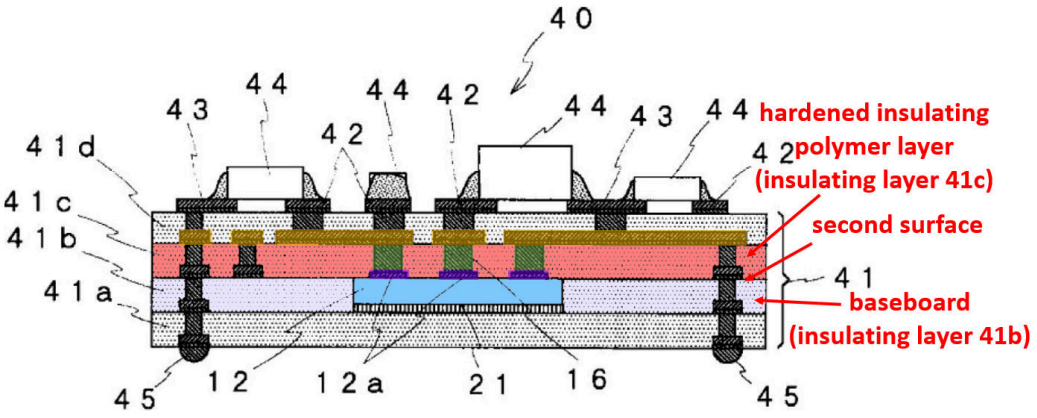
To the extent Takayama is considered not to expressly disclose the claimed baseboard (which it does), a POSITA would have found [1a] obvious based on Takayama's description. APPLE-1003, ¶121. A POSITA would have been motivated to use glass-fibre reinforced epoxy resin for Takayama's insulating layer 41b, which was a known material suitable for use as a baseboard layer. APPLE-

1003, ¶121. Indeed, a POSITA would have recognized use of such a material to achieve a desired strength utilizing a well-known baseboard material. Such modification would have amounted to a simple substitution of one known element for another. APPLE-1003, ¶¶121-122; *Intel Corporation v. PACT XPP Schweiz AG*, 61 F.4th at 1381.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Takayama discloses Element [1b]. For example, Takayama's insulating layer 41c provides a ***hardened insulating polymer layer***. APPLE-1003, ¶¶123-124; APPLE-1027, FIG. 1.

FIG. 17



APPLE-1003, ¶123 (APPLE-1027, FIG. 17 (Annotated))

Takayama describes that insulating layer 41c in FIG. 17 is an "epoxy-based photosensitive resin" spin-coated to cover the top of the bare chip to a thickness of 20 μm, and "[p]olyimide or some other resin may be used in the insulating

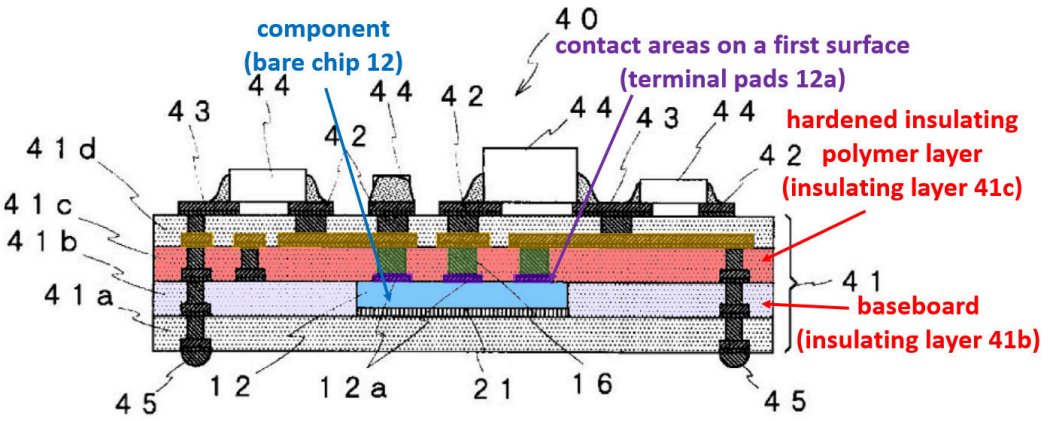
layer[.]" APPLE-1027, [0029]; *supra*, §VI.B.1. A POSITA would have recognized that an epoxy-based resin or polyimide is a polymer. APPLE-1003, ¶123.

Takayama further describes curing of the resin (e.g., of insulating layer 41c) after drying. APPLE-1027, [0029]-[0030] ("after the photosensitive resin [] has dried, the photosensitive resin [] is exposed, developed, and cured"). A POSITA would have understood that the process of drying and curing the resin results in a hardened insulating layer, which is like the '201 Patent's description for its hardened insulating polymer layer. APPLE-1001, 5:32-35; APPLE-1003, ¶124.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

Takayama discloses Element [1c]. For example, Takayama's "bare chip 12" provides ***at least one component***. APPLE-1003, ¶125; APPLE-1027, Abstract, FIGS. 1-17 (and related descriptions). Takayama describes bare chip 12 as "a semiconductor integrated circuit," like the component recited by the '201 Patent. *See e.g.*, APPLE-1027, Abstract, [0023], [0005]-[0006], Cl. 9; APPLE-1001, Abstract ("semiconductor components forming part of an electronic circuit, or at least some of them, are embedded in a base"). Annotated FIG. 17 below shows bare chip 12 embedded within insulating layer 41b.

FIG. 17



APPLE-1003, ¶125 (APPLE-1027, FIG. 17 (Annotated))

Bare chip 12 has "terminal pads 12a" on its active surface (***contact areas on a first surface***). APPLE-1027, [0025] ("The bare chip 12 has a rectangular plate shape and a plurality of terminal pads 12a made of copper (Cu) arranged in a grid pattern on one of the main surfaces (the top surface in FIG. 1)."). Takayama explains that terminal pads 12a are in contact with conductors 16. *Id.* ("Each of these terminal pads 12a is conductively connected to … conductors 16 and wiring conductors 14 in via holes 15."); APPLE-1003, ¶126.

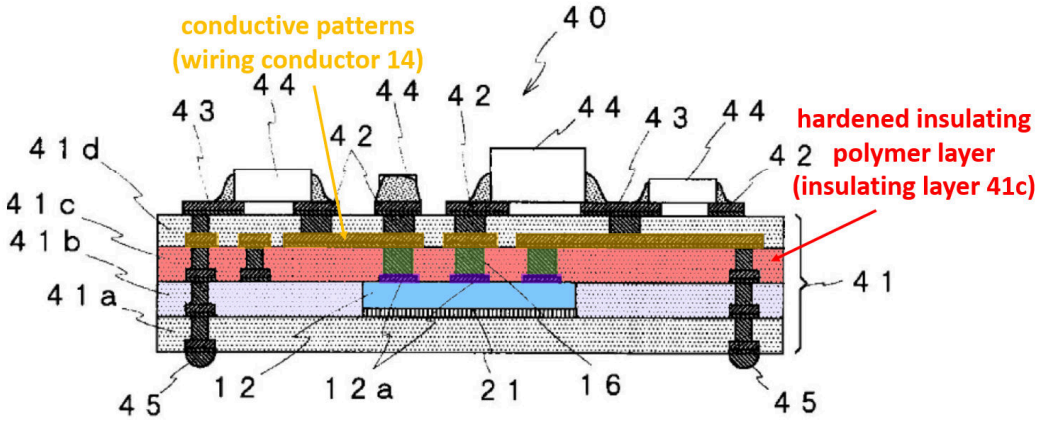
The ***first surface*** of bare chip 12 with terminal pads 12a thereon is ***against*** insulating layer 41c, as shown in FIG. 17, for example. APPLE-1027, FIG. 17; [0029]; APPLE-1003, ¶127.

Element [1d] conductive patterns on the hardened insulting polymer layer; and

Takayama discloses Element [1d]. APPLE-1003, ¶¶128-129. For example, Takayama's "electronic circuit device 40" includes ***conductive patterns*** (e.g.,

"wiring conductors") formed on the ***hardened insulating polymer layer*** (e.g., "insulating layer 41c"). APPLE-1027, Abstract ("wiring conductors 14 are formed on the top surface of the insulating layer [covering the active surface of bare chip 12]"), [0029], [0032]. APPLE-1003, ¶128.

FIG. 17



APPLE-1003, ¶128 (APPLE-1027, FIG. 17 (Annotated))

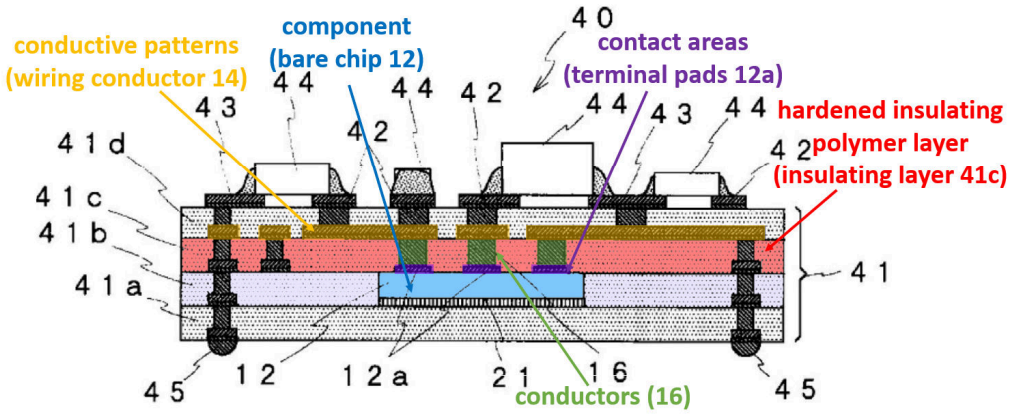
A POSITA would have recognized, and found obvious from Takayama's description, that the wiring conductor is made of copper (***conductive***) and forms a ***pattern***. *Id.*, [0016], [0032]-[0037] ("wiring pattern openings"), [0041] ("Cu wiring conductors 14"); APPLE-1003, ¶129.

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

Takayama discloses Element [1e]. APPLE-1003, ¶¶130-131. For example, Takayama describes a "conductor 16" that is electrically connected to terminal pads 12a and formed in insulating layer (e.g., insulating layer 41c), by forming via

hole 15 in the insulating layer and filling the via hole with a conductor by a Cu plating process. APPLE-1027, Abstract ("the via holes 15 are filled with a conductor 16 to establish a conductive connection with the terminal pads 12a"), [0045]; *see also* [0007]-[0008], [0012], [0024]-[0025], [0030]-[0031], [0041], [0047], Cls. 1, 2, 3, 4, 6; APPLE-1003, ¶130.

FIG. 17



APPLE-1003, ¶130 (APPLE-1027, FIG. 17 (Annotated))

Conductor 16 forms ***electrical contacts between*** the wiring conductors (***at least some of the conductive patterns***) on the insulating layer 41c and terminal pads 12a (***at least some of the contact areas of the component***). APPLE-1027, [0025] ("Each of these terminal pads 12a is conductively connected to … via conductors 16 and wiring conductors 14 in via holes 15."), [0053] ("a buildup system in which chip-type electronic components are embedded inside multilayer circuit boards, via holes are formed on the terminal pads of the chip-type electronic component and filled with conductors to connect the terminal pads and conductors,

and wiring conductors are formed to connect to the conductors. In this way, the electrical connection between the terminal pads, the conductors, and the wiring conductors can be improved, and short-circuits between terminal pads become less likely even when pitch between terminal pads is narrower."), FIG. 17; *see also* [0008]-[0009], [0012], [0045], Cls. 1, 2, 3, 4, 6. APPLE-1003, ¶131.

C. GROUND 2B – Takayama and Hayashi render obvious Claim 1

1. Predictable Combination of Takayama and Hayashi

A POSITA would have been motivated to combine the teachings of Takayama and Hayashi to utilize a glass-reinforced epoxy resin for insulating layer 41b. APPLE-1003, ¶132. Both Takayama and Hayashi relate to embedding semiconductor components inside an insulating substrate formed by a plurality of insulating layers. *See e.g.*, APPLE-1011, [Claim 1], [0001]-[0003]; APPLE-1027, [0008], [0019]-[0024], [0051]. Both also describe resin materials for the multiple insulating layers. APPLE-1011, [0015]-[0016]; APPLE-1027, [0029], [0051]. Hayashi further describes that, "[a] woven fabric, non-woven fabric composed of glass or aramid resin, etc. impregnated with one of the resins described above [e.g., epoxy resin] may also be used," providing a known material for a baseboard layer. APPLE-1011, [0015]-[0016]. APPLE-1003, ¶132.

A POSITA would have been motivated to apply this teaching of Hayashi to

Takayama by impregnating a glass material with epoxy resin for its insulating layer 41b, for example. APPLE-1003, ¶¶132-133. Hayashi recognizes the benefits of glass impregnated with epoxy resin, in "increase[ing] the strength of an insulating substrate or wiring substrate as a whole." APPLE-1011, [0016]. A POSITA would have recognized that impregnating glass fibers with epoxy resin for Takayama's insulating layer 41b would promote increased strength of its multilayer circuit board (e.g., as a whole). APPLE-1003, ¶133.

A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Takayama and Hayashi describe similar devices involving use of resin material in an insulating layer for housing semiconductor components, and because the modification would have been implemented by impregnating epoxy resin with glass—a configuration Hayashi already demonstrates to be successful. APPLE-1003, ¶134. Moreover, Hayashi and Takayama describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing, including for the reasons noted above. *Id.*

2. Application to Challenged Claim

Elements [1pre], [1b]-[1e]

See, supra, Ground 2A, Analysis of Elements [1pre], [1b]-[1e]; APPLE-1003, ¶135.

Element [1a]

As discussed above (Ground 2A), Takayama alone already anticipates or renders obvious Element [1a]. *Supra*, § VI.B.2, Analysis of [1a]. To the extent Takayama is considered not to expressly provide Element [1a], Takayama in view of Hayashi renders Element [1a] obvious. APPLE-1003, ¶136. As discussed in §VI.C.1 (Takayama-Hayashi combination), the combined system's insulating layer 41b having bare chip 12 embedded therein is made of epoxy resin impregnated with glass, in accordance with Hayashi's suggestions, which is just like the '201 Patent's description for its baseboard. APPLE-1001, 3:49-57 ("a glass-fibre reinforced epoxy board").

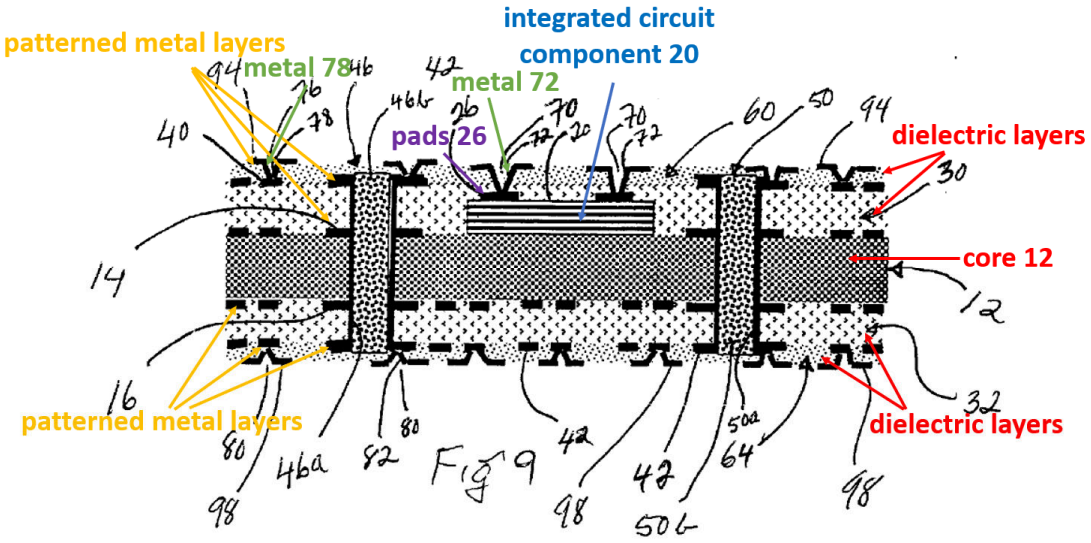
Accordingly, the Takayama-Hayashi combination provides Element [1a].

D. GROUND 3A – McCormack renders obvious Claim 1

1. McCormack

McCormack describes a circuit board having an embedded "integrated electronic component" ("integrated circuit component 20") and a method of producing such structure. APPLE-1005, Title, Abstract, [0009], [0026], [0029], Cl. 1; APPLE-1003, ¶¶72-73. As shown in Figure 9, a circuit component 20 is mounted on an upper substrate surface of core substrate 12, and a dielectric layer (e.g., dielectric layer 30) is on the substrate surface of core 12 and over the integrated circuit component 20. APPLE-1005, Abstract, [0029], [0030], Cl. 1,

FIG. 9. APPLE-1003, ¶74. As shown in FIG. 9, McCormack describes optional additional dielectric layers (e.g., dielectric layers 60, 32, 64) on both the upper and lower sides of the core substrate 12, with patterned metal layers on each of the dielectric layers and the core substrate that are interconnected through metal-lined openings (e.g., metal liners 72, 78 and 82 in openings 70, 76 and 80, respectively) and conductive feed-throughs (e.g., metal-lined vias 46, 50 and 18). APPLE-1005, Abstract, [0009] ("may also comprise"), [0030]-[0032], [0026]. The dielectric layers contain "polymeric compounds" and are "cur[ed]" at "a subsequent heating step." *Id.*, [0033]. APPLE-1003, ¶75. McCormack further describes that openings 70 are formed through the dielectric layer(s) above the integrated circuit component, "to expose pads 26 of the integrated circuit component 20," and openings 70 are then "metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26." *Id.*, [0032]. APPLE-1003, ¶76.



APPLE-1003, ¶76 (APPLE-1005, FIG. 9 (Annotated))

McCormack discloses an example technique to embed components in its substrate, with "a cavity" provided beforehand in the core substrate 12 to dispose the integrated circuit component in the cavity. APPLE-1005, [0009], [0024]-[0025], [0026]-[0029] (describing common features of various preferred embodiments compatible with different methods for embedding the integrated circuit component 20, either on a surface of the core 12 or embedded in a cavity 24 in core 12), FIGS. 12, 13 (reproduced below); APPLE-1003, ¶77.

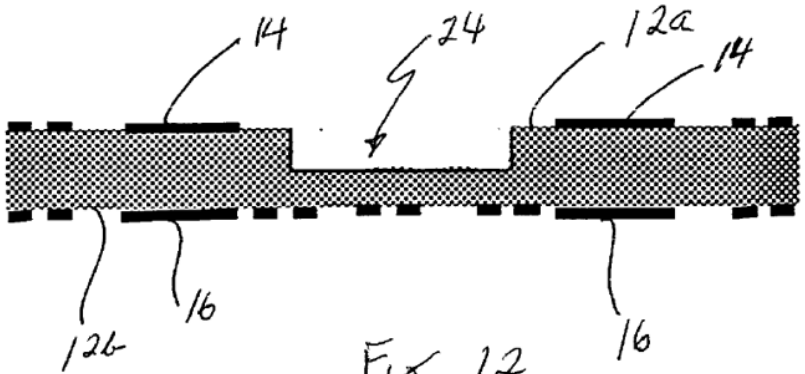


Fig 12

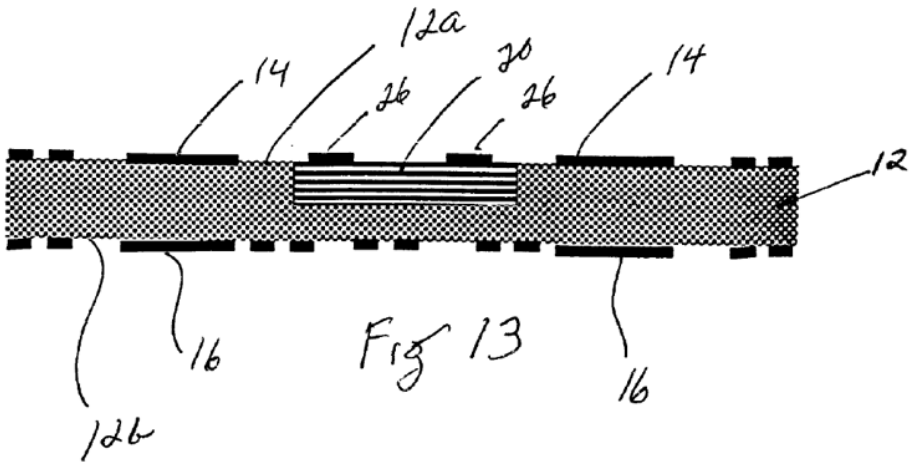


Fig 13

APPLE-1003, ¶77 (APPLE-1005, FIGS. 12, 13)

2. Application to Challenged Claim

Element [1pre] An electronic module, comprising

If the preamble is deemed limiting, McCormack teaches [1pre]. APPLE-1003, ¶138. For example, McCormack describes a circuit board having an integrated electronic component 20 embedded in a circuit board substrate. APPLE-1005, Abstract, [0009], [0029], Cl. 1, FIGS. 9, 12, 13; APPLE-1001, 1:63-67; APPLE-1003, ¶138.

Element [1a] a baseboard having a first surface and a second surface;

McCormack discloses Element [1a]. APPLE-1003, ¶¶139-144. In particular, McCormack's "core substrate" 12 provides a baseboard as claimed. APPLE-1005, [0009], [0024]-[0026], FIGS. 12-13. The core substrate has a first surface and a second surface. APPLE-1003, ¶139; *Infra*, Analysis of Element [1b] (Composite Based on APPLE-1005, FIGS. 9 & 12).

McCormack describes example materials for core 12, such as "B-stage polymetric compounds such as polyimides, epoxy resins, polyurethanes or silicons, well known to those skilled in the art," which is cured with heat and pressure. APPLE-1005, [0033]. This is consistent with the '201 Patent's description of its baseboard. APPLE-1001, 3:48-57 ("The baseboard 1 can be, for example, a glass-fibre reinforced epoxy board. … A flexible and cheap organic board can thus be

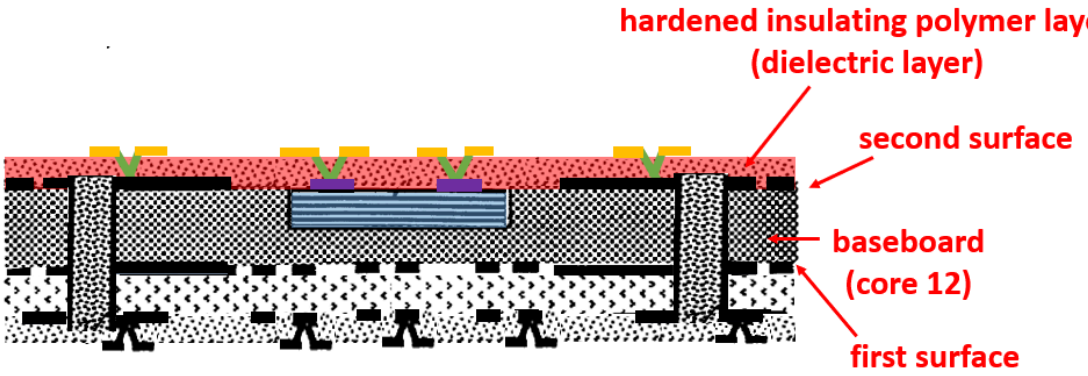
selected. … Of course, an inorganic board can also be used."). APPLE-1003, ¶140. Additionally, core 12 is used to house an integrated electronic component (McCormack's integrated circuit components 20), as is the '201 Patent's baseboard. *Compare e.g.,* APPLE-1001, 2:22-26 ("With the aid of the invention, a circuit board can be manufactured with the semiconductor components embedded inside it."), 3:23-33 *with e.g.,* APPLE-1005, Abstract, [0009], Cl. 1 ("A method for producing a circuit board having an integrated electronic component…"). APPLE-1003, ¶141.

Even if McCormack did not expressly describe the claimed baseboard (which it does), McCormack renders this element obvious. APPLE-1003, ¶142. A POSITA would have been motivated to use glass-fibre reinforced epoxy resin for McCormack's core 12, to facilitate enhanced strength, as glass-fibre reinforced epoxy boards were both well-known in the art and known to have high strengths. APPLE-1003, ¶¶142-143. Such modification would have amounted to a simple substitution of one known element for another. APPLE-1003, ¶144.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

McCormack discloses Element [1b]. APPLE-1003, ¶¶145-151. For example, McCormack describes dielectric layer(s) (e.g., dielectric layers 30 and 60) "placed, flowed or laminated over the integrated circuit component 20" and

over the upper surface of core 12. APPLE-1005, [0030]-[0032]. A POSITA would have found obvious from McCormack's descriptions that one, two, or more than two dielectric layer(s) (along with associated metal layer(s)) can be used above and/or below the core substrate 12, to provide an integrated electronic component in accordance with McCormack's teachings. APPLE-1005, [0009], [0030]-[0032], [0035]; APPLE-1003, ¶145-146. Indeed, a POSITA would have been motivated to use a single dielectric layer, for example, to provide a space-efficient design having reduced thickness and enhanced manufacturing efficiency (e.g., by including fewer processing steps). Moreover, a POSITA would have recognized that with the component positioned in a hole in core 12, a single dielectric effectively covers the component without use of an intermediate dielectric to provide a planar surface (e.g., before applying a second dielectric and a metal layer on the second dielectric). APPLE-1003, ¶147. In the resulting configuration, a single dielectric layer is disposed over the integrated circuit component 20 and the second (upper) surface of core 12, which provides ***a hardened insulating polymer layer on the second surface of*** core 12 (baseboard). APPLE-1003, ¶148; *supra*, §VI.D.2, Analysis of Element [1a].



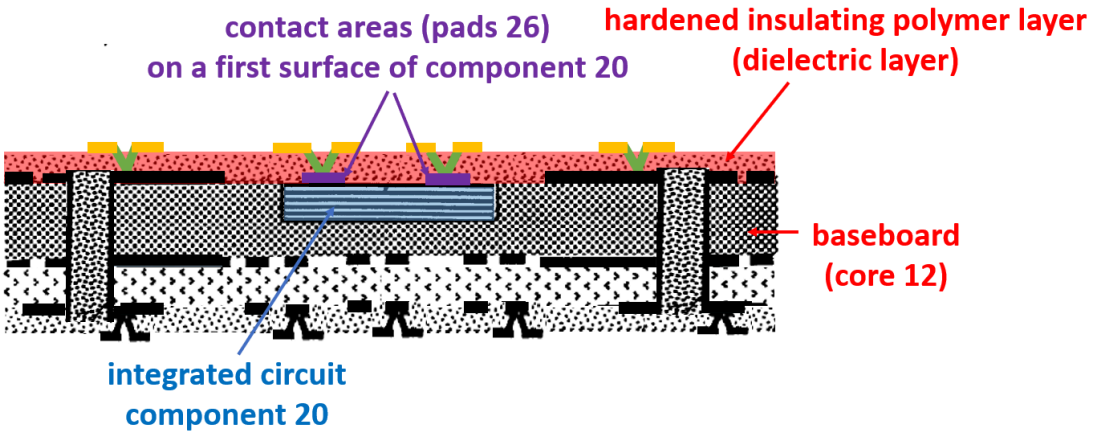
APPLE-1003, ¶148 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

The dielectric material described by McCormack is an insulating material. APPLE-1003, ¶149. Moreover, McCormack describes that dielectric material for dielectric layers include polymer: "B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicons, well known to those skilled in the art … thermosetting materials, such as high glass transition anhydride-cured epoxy composition… high temperature thermoplastic materials … and the like, and mixtures of any of the foregoing." APPLE-1005, [0033]; APPLE-1003, ¶149.

The dielectric layers are "cur[ed]" at "a subsequent heating step" "upon additional exposure to heat and pressure." *Id.*, [0033]; APPLE-1003, ¶150. A POSITA would have understood that the process of curing the resin with heat and pressure results in a ***hardened*** layer, and alternatively, a thermoplastic with high glass transition temperature becomes rigid, thus hardened, when it cools from above to below its glass transition temperature. APPLE-1003, ¶151; APPLE-1001, 5:32-35.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

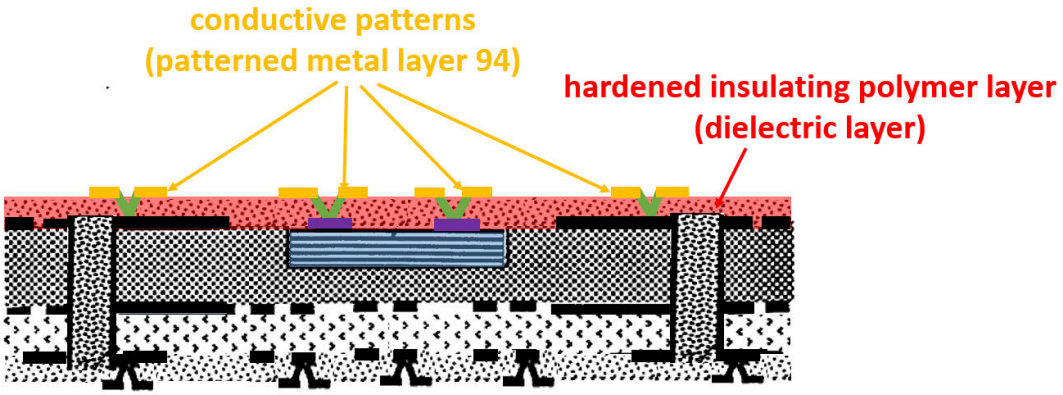
McCormack discloses Element [1c]. APPLE-1003, ¶152. For example, McCormack describes ***at least one component*** (e.g., "at least one integrated electronic component [20]") ***within the baseboard*** (e.g., a cavity of core 12) and having ***contact areas*** (e.g., "conductor pads 26") on a first surface of the component. APPLE-1005, Abstract, [0009], [0028] ("one or both of the substrate surfaces 12a and 12b may have a cavity generally illustrated as 24 in FIG. 12. … The prefabricated, integrated circuit component 20 (e.g., resistors, capacitors, inductors, etc.) may be conveniently disposed in the cavity 24, as shown in FIG. 13."), [0029] ("The integrated circuit component 20 may include one or more conductor pads 26 and may be any suitable integrated circuit component 20…"), Cls. 11, 25; APPLE-1003, ¶152. The first surface of the component is ***against*** the ***hardened insulating polymer layer*** (e.g., dielectric layer over integrated circuit component 20). *See also*, APPLE-1005, [0030]-[0032]; *supra*, §VI.D.2, Analyses of Elements [1a] and [1b]; APPLE-1003, ¶152.



APPLE-1003, ¶152 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

Element [1d] conductive patterns on the hardened insulting polymer layer; and

McCormack discloses Element [1d]. APPLE-1003, ¶¶153-154. For example, McCormack describes a metal layer (e.g., metal layer 94) that is "disposed in" the dielectric layer and is "patterned." APPLE-1005, [0032]; *see also* [0027] (explaining how "[p]atterning" of the metal layers may be performed "to develop the desired patterned metal profile"), FIG. 9 (showing patterned metal layer 94 on dielectric layer 60); *supra*, §VI.D.2, Analysis of Element [1b]. As illustrated below, McCormack provides ***conductive patterns*** (e.g., patterned metal layer 94) ***on*** the ***hardened insulating polymer layer*** (e.g., dielectric layer over the embedded component). APPLE-1003, ¶¶153-154.



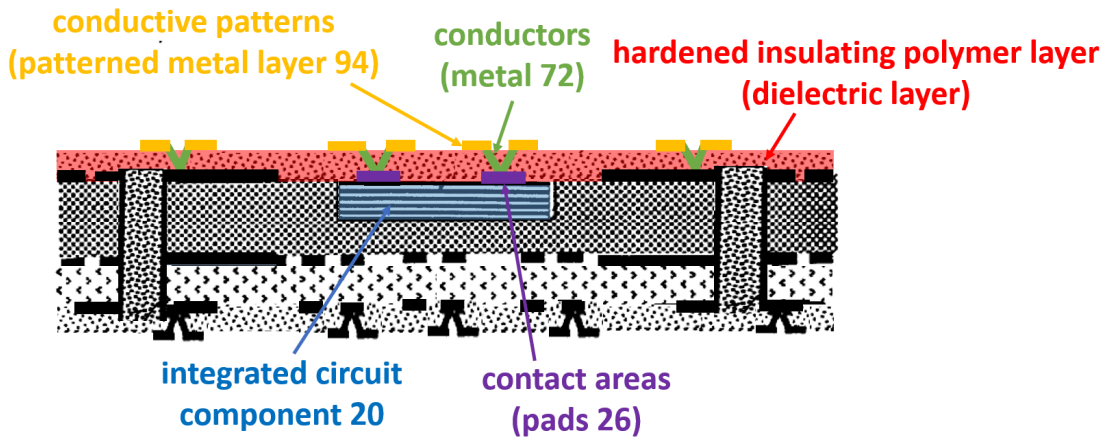
APPLE-1003, ¶154 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

McCormack discloses Element [1e]. APPLE-1003, ¶¶155-157. For example, McCormack describes ***conductors*** (e.g., metal 72) ***within the hardened insulating polymer layer*** (e.g., dielectric layer over the component). APPLE-1005, [0021], [0032], FIG. 9. For example, McCormack describes forming "metal-lined openings," such as first forming openings (e.g., "openings 70") by laser drilling or the like, through the dielectric layer(s) above the integrated circuit component, "to expose pads 26 of the integrated circuit component 20." *Id*. "Openings 70 are then metal-lined with a suitable metal (e.g., copper) 72 into electrical contact with pads 26." *Id*. APPLE-1003, ¶155.

To be clear, even if not revealed to a POSITA by the description offered by

McCormack (which it is), a POSITA would have predictably implemented the metal 72 in accordance with McCormack's teachings to form electrical contacts between the pads of the component and the patterned metal layer on the dielectric layer that is over the component. APPLE-1003, ¶156. Indeed, based on McCormack's description, a POSITA would have understood, and found obvious, that when the component is buried in a cavity in the core substrate 12 (e.g., FIGS. 12-13) and a single dielectric layer is provided above the core substrate, the metal 72 (***conductors***) of openings 70 likewise penetrates through that dielectric layer (***within the hardened insulating polymer layer***), in order to expose pads 26 of the component ***for forming electrical contacts between*** metal layer 94 (***at least some of the conductive patterns***) and pads 26 (***contact areas***). Doing so effectuates McCormack's expressly stated objective of thereby electrically connecting the component with the metal layers of the circuit board. APPLE-1005, Abstract, [0021],[0032], FIG. 9, Cl. 1; APPLE-1003, ¶157.



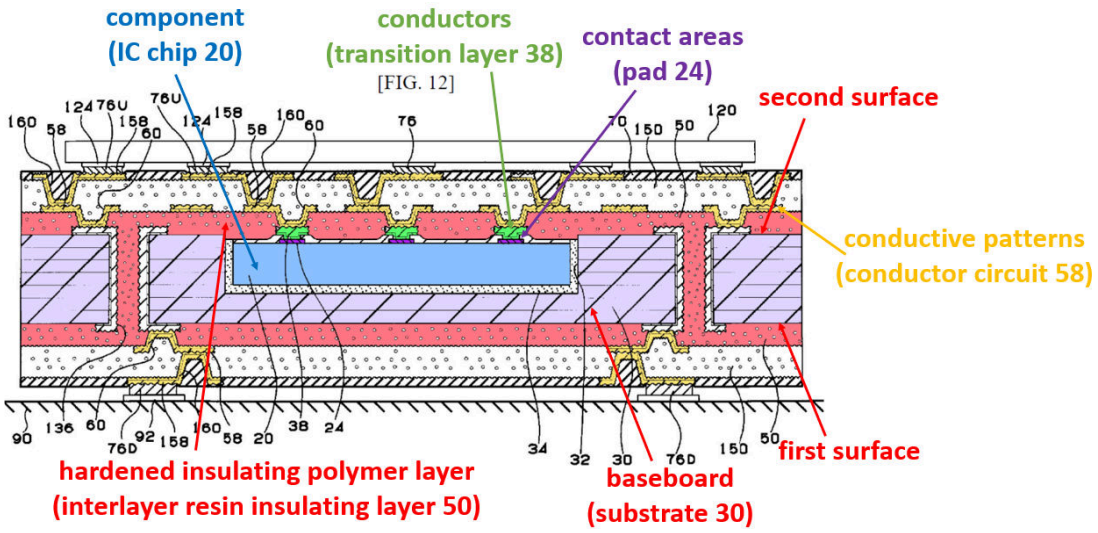
APPLE-1003, ¶157 (Composite Based on APPLE-1005, FIGS. 9 & 12 (Annotated))

E. GROUND 3B – McCormack and Sakamoto render obvious Claim 1

1. Sakamoto

Sakamoto describes "a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip." APPLE-1004, [0001]; *see also*, Abstract, [0005]. Sakamoto describes "providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance [.]" *Id.*, [0005]; *see also*, Abstract ("an IC chip 20 pre-embedded in a core substrate 30"), [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. Sakamoto further describes "impregnating a reinforcing material such as glass epoxy resin," such as impregnating a core material such as glass cloth with an epoxy resin, as a core substrate. APPLE-1004, [0012], [0023]. An "interlayer resin insulating layer 50" provided over the IC chip 20 and on a surface of substrate 30 contains polymer and is cured with the application of heat and pressure. *Id.*, [0030], [0042], [0047], [0057]-[0060]. "Conductor circuit 58" is formed on the top surface of the interlayer resin insulating layer 50 and the inner wall surface of openings for via holes 60, which are formed through the interlayer resin insulating layer for connecting the

electronic components and the conductive circuits. *Id.*, [0017], [0036]. Sakamoto further describes that "a transition layer 38" made of copper is provided on a die pad 24 of the IC chip 20, to connect to via 60 in the interlayer resin insulating layer 50. *Id.*, Abstract, [0018], [0020], [0028], [0031] ("a transition layer 38 made of copper on the die pads 24"), [0067], [0069]; APPLE-1003, ¶¶78-82.



APPLE-1003, ¶82 (APPLE-1004, FIG. 12 (Annotated))

2. Predictable Combination of McCormack and Sakamoto

A POSITA would have been motivated to combine the teachings of McCormack and Sakamoto to impregnate a core material such as glass cloth with an epoxy resin, for the core substrate. APPLE-1003, ¶159. Both McCormack and Sakamoto relate to embedding semiconductor components within multi-layer substrates (e.g., in a cavity or opening in a core substrate). *See e.g.*, APPLE-1004,

Abstract, [0001], [0005], Cl. 1, FIGS. 6, 10-12; APPLE-1005, Title, Abstract, [0002], [0009], [0026], [0029]-[0030], Cl. 1. Both also describe using epoxy resins for the core substrate for housing the semiconductor components. *See e.g.*, APPLE-1004, [0012], [0020], [0023]; APPLE-1005, [0009], [0024]-[0026], FIGS. 12-13. Sakamoto further describes "impregnating a reinforcing material such as glass epoxy resin," such as impregnating a core material such as glass cloth with an epoxy resin, for its core substrate. APPLE-1004, [0012], [0023]. APPLE-1003, ¶159.

In the combined system, the core substrate is formed by impregnating glass cloth, for example, with an epoxy resin. APPLE-1003, ¶160.

A POSITA would have been motivated to combine McCormack and Sakamoto based on Sakamoto's express recognition of the benefits of glass cloth impregnated with a resin as a "reinforcing material." APPLE-1004, [0012]. A POSITA would have recognized, from Sakamoto's teachings, that impregnating glass cloth or similar materials with an epoxy resin in a core substrate (e.g., McCormack's core substrate 12) would promote enhanced strength and thereby facilitated more reliable chip packages less likely to break or malfunction due to various mechanical stresses. APPLE-1003, ¶160.

A POSITA would have had a reasonable expectation of success in making the proposed modifications given that McCormack and Sakamoto describe similar

devices involving use of epoxy resin core substrates for housing semiconductor components, and because the modifications would have been implemented by impregnating the epoxy resin with glass cloth—a configuration Sakamoto already demonstrates to be successful. APPLE-1003, ¶¶161-162. Moreover, for reasons similar to those described above, McCormack and Sakamoto describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing. *Id.*

3. Application to Challenged Claim

Elements [1pre], [1b]-[1e]

McCormack-Sakamoto provides these elements. *See, supra,* Ground 3A, Analyses of Elements [1pre], [1b]-[1e]; APPLE-1003, ¶163.

Element [1a]

As discussed above under Ground 3A, McCormack alone either anticipates or renders obvious Element [1a]. *Supra*, § VI.D.2, Analysis of [1a]. To the extent McCormack alone is considered not to provide Element [1a], McCormack in view of Sakamoto renders Element [1a] obvious. APPLE-1003, ¶164. As discussed in § VI.E.2 (McCormack-Sakamoto combination), the combined system's core 12 with integrated circuit component 20 incorporated therein is made of glass-cloth impregnated epoxy resin, which is just like the '201 Patent's description for its baseboard. APPLE-1001, 3:49-57 ("a glass-fibre reinforced epoxy board").

Accordingly, the McCormack-Sakamoto combination provides Element [1a].

F. GROUND 4 – Sakamoto anticipates or renders obvious Claim 1

1. Application to Challenged Claim

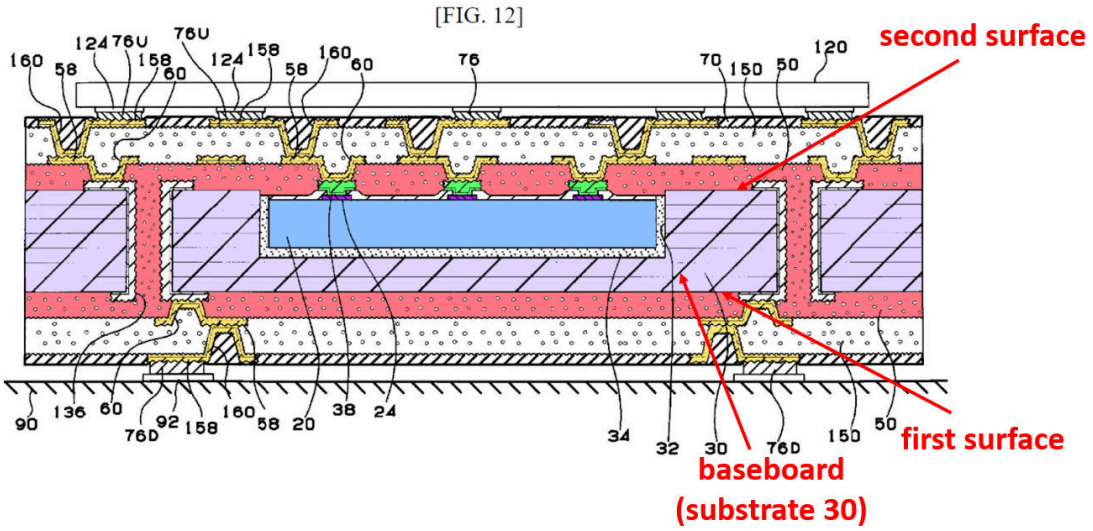
Element [1pre] An electronic module, comprising

If the preamble is deemed limiting, Sakamoto teaches [1pre]. APPLE-1003, ¶166. For example, Sakamoto describes "a multilayer printed wiring substrate and a package substrate with a built-in electronic component such as an IC chip," thereby providing ***an electronic module***. APPLE-1004, [0001]; *see also*, Abstract, [0005], [0008], [0011]; APPLE-1001, 1:63-67; APPLE-1003, ¶166.

Element [1a] a baseboard having a first surface and a second surface;

Sakamoto discloses Element [1a]. APPLE-1003, ¶¶167-168. For example, Sakamoto describes a "core substrate 30" where an IC chip is incorporated in advance. APPLE-1004, Abstract; *see also*, [0005] ("providing an opening, through-hole, or counterbore in a resin insulating substrate, incorporating an electronic component such as an IC chip in advance[.]"), [0006]-[0007], [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12. Sakamoto further explains that the resin substrates for incorporating electronic components such as IC chips "include epoxy resins, BT resins, and phenol resins impregnating a reinforcing material

such as glass epoxy resin or a core material, or a pre-preg laminate impregnated with an epoxy resin. However, any material generally used in printed wiring substrates can be used." *Id.*, [0012]; *see also*, [0020], [0023]. This is just like the '201 Patent's description for its "baseboard 1," such as "a glass-fibre reinforced epoxy board." *Compare* APPLE-1004, [0012], [0023] *with* APPLE-1001, 3:49-57. Thus, a POSITA would have recognized that Sakamoto's substrate 30 is a ***baseboard***. APPLE-1003, ¶¶167-168. The annotated FIG. 12 below illustrates substrate 30, which provides a ***baseboard having a first surface and a second surface***. APPLE-1003, ¶168.

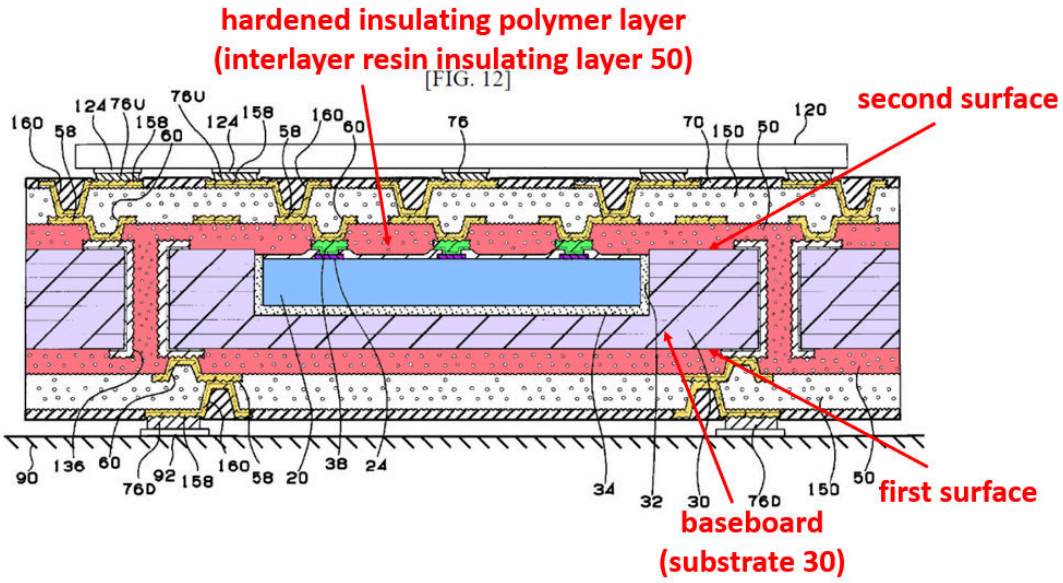


APPLE-1003, ¶168 (APPLE-1004, FIG. 12 (Annotated))

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Sakamoto discloses Element [1b]. APPLE-1003, ¶¶169-170. In particular, Sakamoto describes an "interlayer resin insulating layer 50" provided over the IC

chip 20 and on the second surface of substrate 30 (***baseboard***). APPLE-1004, [0017], [0030], FIGS. 6, 10-12. APPLE-1003, ¶169.



APPLE-1003, ¶169 (APPLE-1004, FIG. 12 (Annotated))

As illustrated in FIG. 12, the "interlayer resin insulating layer 50" is on the second surface of substrate 30 such that it directly contacts the second surface of substrate 30. APPLE-1003, ¶169.

Interlayer resin insulating layer 50 contains ***polymer*** and is cured (thus ***hardened***) with the application of heat and pressure. *E.g., id.*, [0030] ("A thermosetting cycloolefin resin sheet having a thickness of 30 to 50 μm is laminated on the substrate that has undergone the steps described above under vacuum at a pressure of 5 kg/cm^2 while raising the temperature to 50 to 150 °C, resulting in an interlayer resin insulating layer 50…"), [0042] ("an epoxy resin can be used for the interlayer resin insulating layer 50 instead. This epoxy resin

contains a poorly soluble resin, soluble particles, a curing agent, and other components."), [0047] ("Specific examples of soluble resin particles include those composed of epoxy resins, phenol resins, polyimide resins, polyphenylene resins, polyolefin resins, and fluorine resins, and the particles may be composed of one of these resins or a mixture of two or more these resins."), [0053]-[0060]; APPLE-1003, ¶170; APPLE-1001, 5:32-35.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

Sakamoto discloses Element [1c]. APPLE-1003, ¶171-173. For example, Sakamoto describes "an electronic component such as an IC chip" (***at least one component***) in an opening, through-hole, or counterbore in a resin insulating substrate (***within the baseboard***). APPLE-1004, [0005]; *see also*, Abstract ("an IC chip 20 pre-embedded in a core substrate 30"), [0017], [0020], [0023]-[0025], [0066], FIGS. 6, 10-12; APPLE-1003, ¶171.

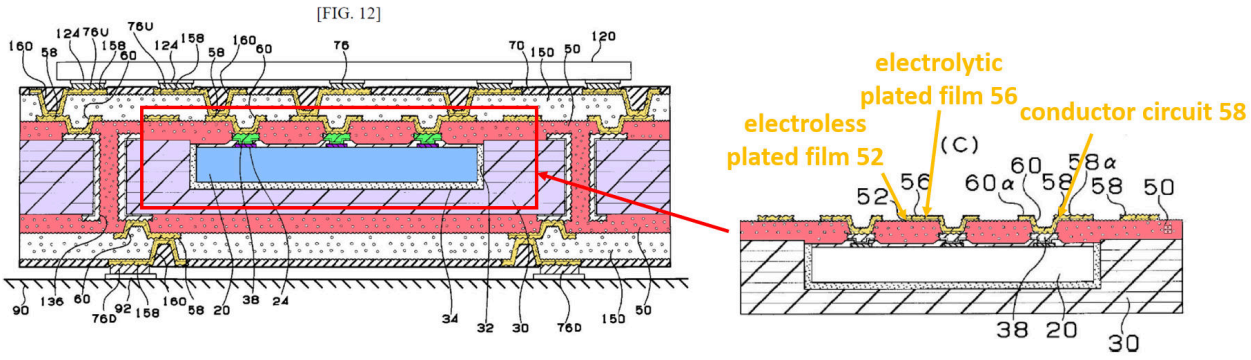
IC chip 20 has die pads 24 (***contact areas***) on its active surface (***a first surface***). *E.g.*, APPLE-1004, Abstract, [0008], [0018] ("die pads 24 forming input/output terminals"), FIG. 12. APPLE-1003, ¶172.

In the resulting device, the interlayer resin insulating layer 50 is ***against*** the surface of IC chip 20 (without including protective film 22). APPLE-1003, ¶173. Indeed, a POSITA would have found it obvious to omit the IC "protective film

(passivation + polyimide) 22" that covers the active surface of the IC chip 20 and has openings for the die pads 24 (and that is illustrated in Sakamoto's FIG. 12). APPLE-1004, [0018]. Based on Sakamoto's description, a POSITA would have recognized that the manufacturing process of the IC chip 20 and the module would have been advantageously simplified by omitting this protective film by reducing the number of manufacturing steps and material components. APPLE-1003, ¶173. Indeed, a POSITA would have recognized that an additional protective film made of passivation and polyimide layer is not required, especially given that the interlayer resin insulating layer 50 grown on top of the first surface of the IC chip provides protection that a protective film provides. APPLE-1003, ¶173. In the resulting device, the interlayer resin insulating layer 50 is ***against*** the first surface of IC chip 20 (without including protective film 22). APPLE-1003, ¶173.

Element [1d] conductive patterns on the hardened insulting polymer layer; and

Sakamoto discloses Element [1d]. APPLE-1003, ¶¶174-175. Sakamoto's "conductor circuit 58" (***conductive patterns***) is formed on the surface of the interlayer resin insulating layer 50 (***hardened insulating polymer layer***) and extends into via holes 60. APPLE-1004, [0017], [0032]-[0036] (describing the formation of the conductor circuits 58 and via 60 made of an electroless plated film 52, on the surface of the interlayer resin insulating layer 50, and an electrolytic plated film 56), FIGS. 4(A)-(C), 6, 10-12; APPLE-1003, ¶174.



APPLE-1003, ¶174 (APPLE-1004, FIGS. 12 & 4(C) (Annotated))

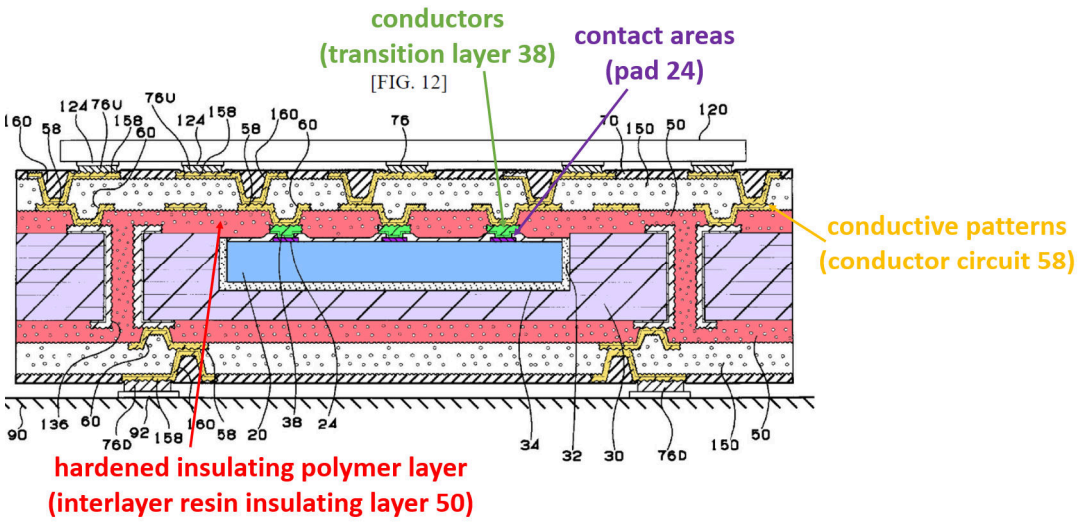
Sakamoto additionally provides [1d] in a second manner. For example, the portions of conductor circuit 58 outside the via holes 60 and on top of the interlayer resin insulating layer 50 alone provide the claimed ***conductive patterns***. APPLE-1003, ¶175; *infra*, §VI.F.1, Analysis of Element [1e].

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

Sakamoto discloses Element [1e]. APPLE-1003, ¶¶176-178. For example, Sakamoto discloses a "transition layer 38" formed on the die pads 24 of the IC chip 20 to electrically connect the IC chip and portions of the conductor circuit 58 in via holes 60. APPLE-1004, Abstract, [0008], [0014]-[0015], [0018], [0020], [0027]-[0028], [0031], [0067] ("the transition layer 38 is formed on the pads 24 of the IC chip 20 and vias 60 in the interlayer resin insulating layer 50 are connected to the transition layer 38"), FIG. 2. The "transition layer 38" provides ***conductors within the hardened insulating polymer layer***, as claimed. Indeed, Sakamoto's

configuration is just like the '201 patent, which describes electrical contact formed "by growing conductors on top of the contact areas of a semiconductor component." APPLE-1001, 2:45-48; *see also* APPLE-1004, [0008], FIGS, 6, 10-12; APPLE-1004, [0067], [0069] (describing a conductive path including "transition layers 38, vias 60, a conductor circuit 58" as part of the connection path between the pads 24 of the IC chip 20 and the pads 124 of another IC chip 120); APPLE-1003, ¶¶176-177.

Annotated FIG. 12 below illustrates transition layer 38 (***conductors***) ***within*** interlayer resin insulating layer 50 (***the hardened insulating polymer layer***) in ***electrical contacts between*** conductor circuit 58 through via 60 (***at least some of the conductive patterns***) ***and*** die pads 24 of the IC chip (***at least some of the contact areas of the component***). APPLE-1003, ¶177.



APPLE-1003, ¶177 (APPLE-1004, FIG. 12 (Annotated))

Sakamoto provides [1e] in a second manner. For example, the parts of the

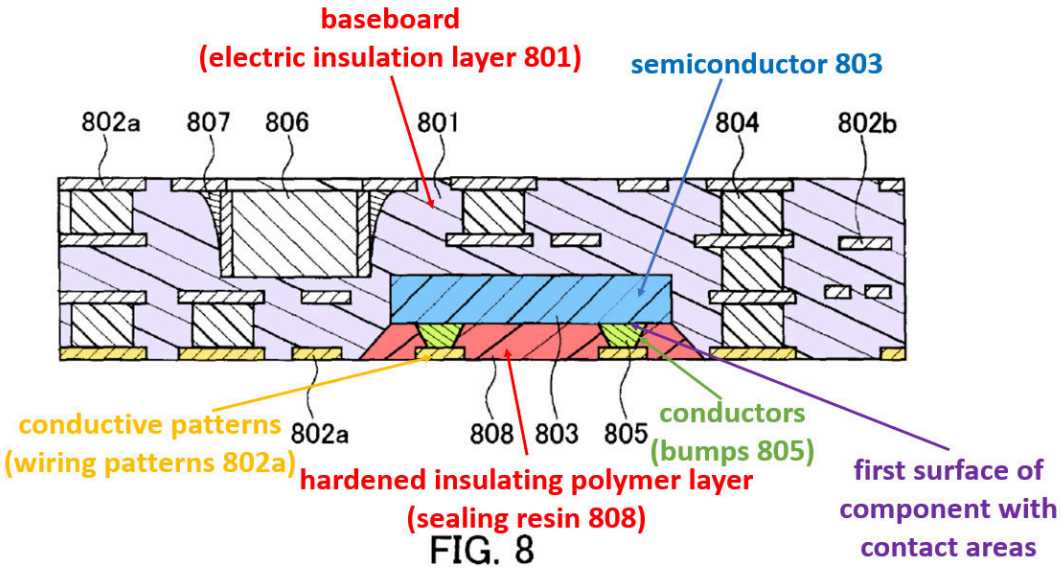
conductor circuit 58 extending into the via holes 60 provide the claimed ***conductors within*** interlayer resin insulating layer 50 (***the hardened insulating polymer layer***). APPLE-1004, [0067]; APPLE-1003, ¶178. These conductors are connected with the parts of the conductor circuit 58 outside the via holes and on top of the interlayer resin insulating layer 50 (***conductive patterns***) as well as pads 24 (***contact areas***) on the component, thus ***forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component***. APPLE-1003, ¶178; *supra*, §VI.F.1, Analysis of Element [1d].

G. GROUND 5A – Asahi anticipates or renders obvious Claim 1

1. Asahi

Asahi describes "a component built-in module in which an electronic component such as a semiconductor and/or a circuit component is provided inside an electric insulation layer." APPLE-1006, 1:7-10; *see also id.*, Title, Abstract. As shown in FIG. 8, "the component built-in module includes an electric insulation layer 801, wiring patterns 802a and 802b, a semiconductor 803 as an electronic component…" *Id.*, 17:55-18:13 *see also* 6:33-9:17, 9:18-11:25, 11:26-12:51, 15:50-17:44, FIG. 7. Bumps 805 are formed on a surface of semiconductor 803 to provide connection between semiconductor 803 and "wiring patterns 802a" on a surface of the electric insulation layer 801. *Id.*, FIG. 8, 17:55-61; APPLE-1003,

¶¶83-87. Asahi discloses "a sealing resin 808" that "may be injected between the semiconductor [803] and the wiring pattern [802a]." APPLE-1006, 17:55-18:13, FIG. 8; *see also id.*, 8:2-10, 10:45-53, 11:54-63, 16:52-62, FIG. 7. The electric insulation layer "is made of a mixture of a filler and an insulating resin" which contains polymer. *Id.*, 3:11-38. Further, Asahi describes that "[i]n the case where a thermosetting resin is used as an insulating resin, the thermosetting resin in the electric insulation layer [] is cured by heating after pressing, whereby the electric insulation layer [] in which the semiconductor [] is embedded can be formed in a plate form." *Id.*, 10:62-67; *see also*, 5:35-46, 15:65-67, 17:33-34. APPLE-1003, ¶88-89.



APPLE-1003, ¶84 (APPLE-1006, FIG. 8 (Annotated))

2. Application to Challenged Claim

Element [1pre] An electronic module, comprising

If the preamble is deemed limiting, Asahi teaches [1pre]. APPLE-1003, ¶180. For example, Asahi describes "a component built-in module in which an electronic component such as a semiconductor and/or a circuit component is provided inside an electric insulation layer." APPLE-1006, 1:7-10; *see also id.*, 6:33-9:17, 9:18-11:25, 11:26-12:51, 15:50-17:44, 17:45-18:13, FIGS. 7, 8. A POSITA would have understood Asahi's component built-in module with embedded electronic components to be an electronic module. APPLE-1001, 1:63-67; APPLE-1003, ¶180.

Element [1a] a baseboard having a first surface and a second surface;

Asahi discloses Element [1a]. APPLE-1003, ¶¶181-183. Asahi's "electric insulation layer" provides a baseboard. APPLE-1006, Abstract, 6:33-9:17, 9:18-11:25, 11:26-12:51, 15:50-17:44, 17:55-18:13, FIGS. 7, 8; APPLE-1003, ¶181. As shown in the annotated Figure 8 below, "electric insulation layer 801" has a first surface and a second surface, and has embedded electronic components therein.

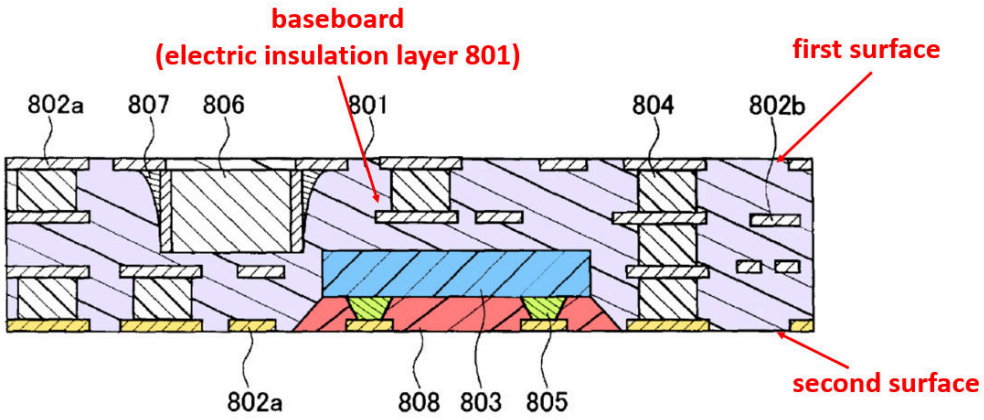


FIG. 8

APPLE-1003, ¶181 (APPLE-1006, FIG. 8 (Annotated))

Asahi also describes the use of "generally used wiring board" such as "a glass-epoxy substrate" for its electric insulation layer to "reduc[e] the production cost." APPLE-1006, 3:60-65; *see also id.*, 1:23-25, 3:11-38; 14:29-30, 15:62-16:2 ("A component built-in module takes a board form, and the electric insulation layer… may contain **a reinforcing material such as a glass cloth or an unwoven fabric**"), Cls. 11, 21; APPLE-1003, ¶182. Asahi further explains that "in each of the first and second component built-in modules [of a multi-layered circuit board], the electric insulation layer in contact with the electronic component and the electric insulation layer in contact with the first inner via preferably are provided integrally[,]" such that "the two electric insulation layers have a common composition and are continuous seamlessly," with benefits of electric insulation layers being "provided continuously without a boundary, thereby improving the

reliability." APPLE-1006, 3:66-4:7; APPLE-1003, ¶182. This is just like the description of "baseboard 1" in the '201 Patent. APPLE-1001, 3:49-57, 2:22-26. Thus, a POSITA would have recognized that Asahi's electric insulation layer is a baseboard. APPLE-1003, ¶183.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Asahi discloses Element [1b]. APPLE-1003, ¶¶184-189. For example, Asahi describes that junction portions between the semiconductor and the wiring patterns are protected with "a sealing resin" to prevent a gap from being formed between the semiconductor and the wiring patterns, to prevent the semiconductor from being damaged, and to improve reliability. APPLE-1006, 8:2-6, 10:45-54, 11:56-65, 16:52-62, 17:62-62; FIGS. 7, 8; *supra*, § VI.C.2, Analysis of Element [1a]; APPLE-1003, ¶184.

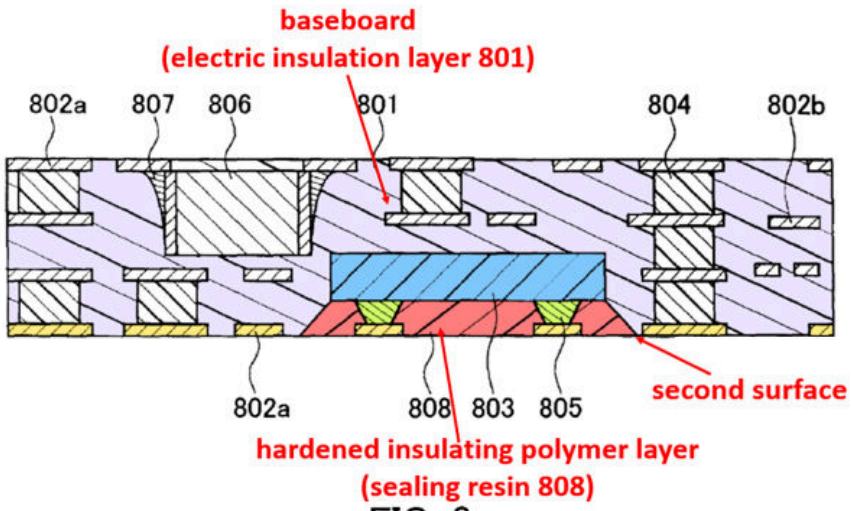


FIG. 8

APPLE-1003, ¶184 (APPLE-1006, FIG. 8 (Annotated))

As shown in FIG. 8, for example, electric insulation layer 801 includes a second surface that sealing resin 808 is in contact with such that the sealing resin 808 is on the second surface of the electric insulation layer 801. APPLE-1003, ¶184. Asahi describes wiring patterns as "on a surface" of an electric insulation layer even though part of the wiring patterns is inside of that electric insulation layer. *See e.g.*, 4:35-37 ("the another wiring pattern is provided on a surface of another electric insulation layer"), 4:50-51, 5:11-13, 5:54-57, 10:54-56 ("the electric insulation layer 201 shown in FIG. 2D on which the wiring patterns 202a and 202b are provided"), 14:42-44, 16:19-20 ("As shown in FIG. 7D, the carriers 709 are removed after pressing, so that the electric insulation layer 701 provided with the wiring patterns 702b on both of its surfaces"), 17:35-40 ("providing a component built-in module that has the wiring patterns 702a on surfaces thereof"), 18:47-52 ("an electric insulation layer having wiring patterns on both surfaces thereof"), 19:24-25, 20:13-15. Similarly, a POSITA would have recognized that, sealing resin 808, with a side exposed to the outside of the built-in component module, is ***on the second surface of the*** electric insulation layer 801 (***baseboard***). APPLE-1003, ¶185; APPLE-1012, 7:58-63.

Asahi explains that "[a]n underfill resin used for ordinary flip chip bonding can be used as the sealing resin." APPLE-1006, 10:45-54, 11:56-65, 16:52-62. A

POSITA would have understood and found obvious that Asahi's underfill resin used for ordinary flip chip bonding includes polymer material and is hardened after curing, e.g., with heat. APPLE-1003, ¶186 (citing APPLE-1007, [0021], [0024], [0038], [0041], [0060], [0093]).

Moreover, a POSITA would have recognized and found obvious that the underfill resin is a hardened insulating polymer based on Asahi's express description of resin materials. APPLE-1003, ¶187. For example, Asahi describes an electric insulation layer "made of a mixture of a filler and an insulating resin," and "the insulating resin preferably contains at least one selected from an epoxy resin, a phenol resin, a fluorocarbon resin, a cyanate resin, a polytetrafluoroethylene (PTFE) resin, a poly(phenylene oxide)(PPO) resin, and a polyphenylether (PPE) resin." APPLE-1006, 3:11-38. Moreover, Asahi describes that "[b]y selecting an appropriate insulating resin material, it is possible to improve a heat resistance, an electric insulation, and high frequency characteristics." *Id.* A POSITA would have been motivated to utilize similar polymer material for the sealing resin to achieve similar desired characteristics. APPLE-1003, ¶187. Additionally, a POSITA would have done so to further avoid stresses due to mismatch in "a heat conductivity, a coefficient of linear expansion, a dielectric constant, etc." between the sealing resin and the surrounding electric insulation layer. *Supra*, § VI.G.1; APPLE-1006, 3:14-16; APPLE-1003, ¶188.

In addition, Asahi describes that such materials are "cured by heating after pressing, whereby the electric insulation layer 201 in which the semiconductor 203 is embedded can be formed in a plate form." APPLE-1006, 10:62-67; *see also id.*, 5:35-39 ("in each of the first and second methods, the electric insulation layer is cured upon making the electric connection"). A POSITA would have recognized, and at least found obvious, from Asahi's description that the sealing resin is likewise hardened, including through a curing process by heating of a suitable material "used for ordinary flip chip bonding," such that the semiconductor embedded in the electric insulation layer and sealing resin "can be formed in a plate form," and to effectuate Asahi's objectives of the sealing resin. APPLE-1006, 10:62-67; APPLE-1003, ¶189; *see also* APPLE-1001, 5:32-35.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

Asahi teaches Element [1c]. APPLE-1003, ¶¶190-191. For example, Asahi discloses "an electronic component such as a semiconductor and/or a circuit component" provided inside an electric insulation layer (***baseboard***). *E.g.*, APPLE-1006, 1:7-11, 17:55-63 ("semiconductor 803"), FIG. 8; *supra*, § VI.G.2, Analysis of Element [1a]; APPLE-1003, ¶190. Semiconductor 803 has flat ***contact areas*** (e.g., the semiconductor die's pads on its active surface) on an active surface (***first surface***). Asahi describes use of "a conductive adhesive, an anisotropic

conductive film (ACF), etc. is used in the case of flip chip bonding," or a "bump 805" to achieve electrical connection between the semiconductor 803 and wiring patterns 802a. APPLE-1006, 8:6-10; *see also id.*, 10:35-45 ("bump 205" and a "conductive adhesive" may be used as alternatives and "formed on the semiconductor 203 side" or "used in combination"), 17:59-61; APPLE-1003, ¶191.

Figure 8 illustrates semiconductor 803 (***at least one component***) within electric insulation layer 801 (***baseboard***), flat contact areas on the first surface of semiconductor 803 where bumps 805 are formed, and this ***first surface*** being ***against*** the sealing resin 808 (***hardened insulating polymer layer***); *supra*, § VI.G.2, Analyses of Elements [1a], [1b]; APPLE-1003, ¶191.

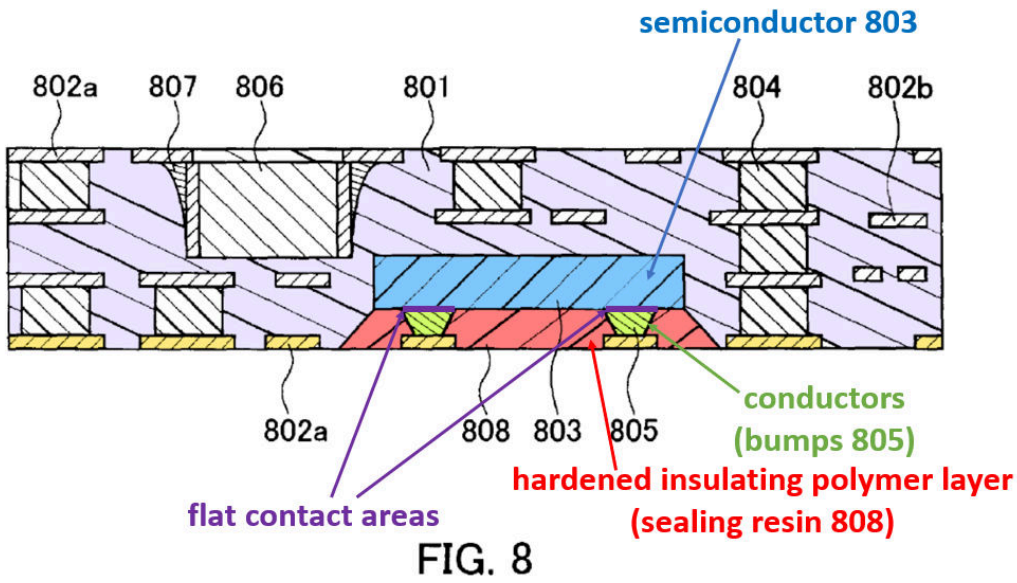


FIG. 8

APPLE-1003, ¶191 (APPLE-1006, FIG. 8 (Annotated))

Element [1d] conductive patterns on the hardened insulting polymer layer; and

Asahi discloses Element [1d]. APPLE-1003, ¶192. For example, Asahi discloses "first wiring patterns in a plurality of layers that are laminated with the electric insulation layer being interposed therebetween," where at least one electronic component embedded in the electric insulation layer is mounted on. APPLE-1006, Abstract, 1:67-2:3. In the example Eighth Embodiment, "wiring patterns 802a" are provided on the surfaces of the module shown in FIG. 8. APPLE-1006, 17:55-63. Asahi explains that semiconductor 803 is connected via bumps 805 with the wiring patterns 802a. *Id*. The "wiring patterns" in electrical connection with various components and conductive vias are made of conductive material(s) and have "patterns," thus are ***conductive patterns***. *Id.*, 3:39-43; APPLE-1003, ¶192.

Asahi further describes that "[j]unction portions between the semiconductor 803 and the wiring patterns 802a are protected with a sealing resin 808." APPLE-1006, 17:55-63, FIG. 8. Thus, wiring patterns 802a (***conductive patterns***) are ***on*** sealing resin 808 (***the hardened insulating polymer layer***). APPLE-1003, ¶193; *see also* APPLE-1006, 8:2-6, 10:45-54, 11:56-65, 16:52-62, FIGS. 7, 8; *supra*, §VI.G.2, Analysis of Element [1b]. The annotated Figure 8 below shows wiring patterns 802a on the sealing resin 808.

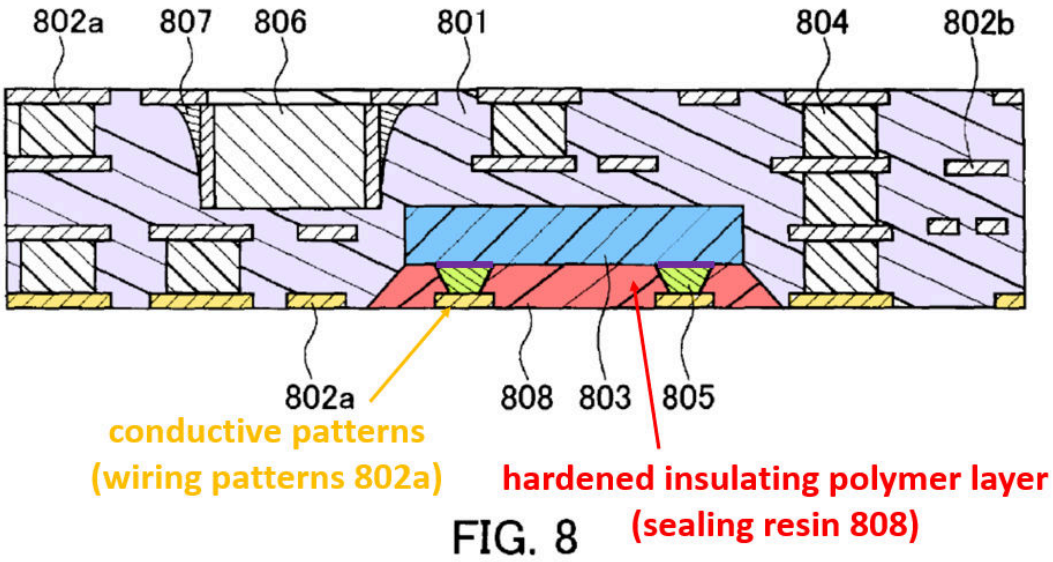


FIG. 8

APPLE-1003, ¶193 (APPLE-1006, FIG. 8 (Annotated))

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

Asahi discloses Element [1e]. APPLE-1003, ¶194-195. As discussed above in §VI.G.2, Analysis of Element [1c], Asahi describes that "a conductive adhesive, an anisotropic conductive film (ACF), etc. is used in the case of flip chip bonding[,]" or "a bump" (***conductors***) can be formed on the semiconductor side to achieve connection between the contact areas on the semiconductor and the first wiring patterns (***forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component***). APPLE-1006, 8:6-10; *see also, id.*, 10:35-45 ("bump" and a "conductive adhesive" may be "used in combination"), 17:59-63; APPLE-1003, ¶194.

Also discussed above in §§ VI.G.2, Analyses of Elements [1b] and [1d], junction portions between the semiconductor 803 and the wiring patterns 802a are protected with a "sealing resin 808." APPLE-1006, 17:62-63; *see also id.*, 8:2-6 ("The semiconductor element may be embedded in a manner such that the semiconductor element, or at least a part of the semiconductor element and connecting portions of the same with the wiring patterns 102a and 102b, is sealed with a sealing resin."), 10:45-54, 11:56-65, 16:52-62, FIGS. 7, 8. Thus, ***conductors*** in the form of "a conductive adhesive, an anisotropic conductive film (ACF)" or "bump" are positioned ***within*** the sealing resin (***the hardened insulating polymer layer***). The annotated FIG. 8 below shows bump 805 within sealing resin 808 and in connection with the contact areas on the component and portions of wiring patterns 802a, the claimed conductive patterns. APPLE-1006, 17:55-63 (semiconductor 803 is connected via bumps 805 with the wiring patterns 802a). APPLE-1003, ¶195.

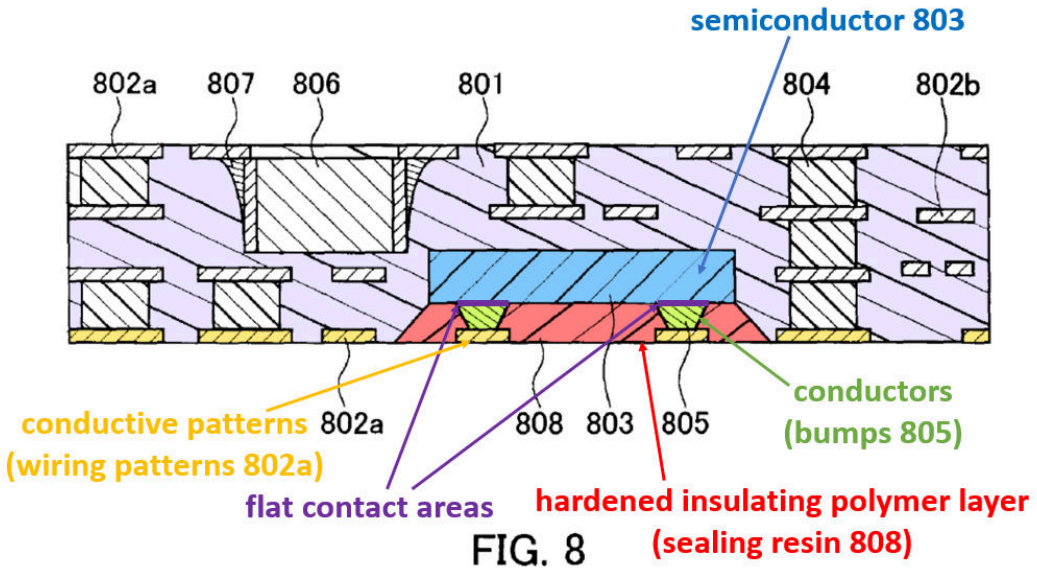


FIG. 8

APPLE-1003, ¶195 (APPLE-1006, FIG. 8 (Annotated))

H. GROUND 5B – Asahi and Sakamoto render obvious Claim 1

1. Predictable Combination of Asahi and Sakamoto

A POSITA would have been motivated to combine Asahi and Sakamoto to utilize a suitable material for Asahi's "sealing resin," in accordance with Sakamoto's teaching, to prevent a gap from being formed between the semiconductor and the wiring patterns, protect the semiconductor from damages, and achieve improved reliability. APPLE-1006, 8:2-10, 10:45-54, 11:54-65, 16:52-62, FIGS. 7, 8; APPLE-1004, [0018]; APPLE-1003, ¶197.

In the predictable combination, the sealing resin (e.g., sealing resin 808) is made of a hardened insulating polymer material, in accordance with Sakamoto's detailed teachings for its interlayer resin insulating layer. APPLE-1006, 8:2-10,

10:45-54, 11:54-65, 16:52-62; APPLE-1004, [0030], [0042], [0047], [0053]-[0060]; *supra*, § VI.F.1, Analysis of Element [1b]; *supra*, § VI.G.2, Analysis of Element [1b]; APPLE-1003, ¶198. In particular, Asahi-Sakamoto's sealing resin would be made of ***polymer*** with similar compositions of Sakamoto's "interlayer resin insulating layer 50," and is ***hardened*** through the application of heat and/or pressure, in accordance with both Sakamoto's and Asahi's teachings. *Supra*, § VI.F.1, Analysis of Element [1b]; *supra*, § VI.G.2, Analysis of Element [1b]; APPLE-1003, ¶198.

Multiple reasons would have prompted a POSITA to implement Asahi's sealing resin in accordance with Sakamoto's material suggestions (e.g., used for Sakamoto's interlayer resin insulating layer 50). APPLE-1003, ¶199.

First, a POSITA would have been motivated to combine Asahi and Sakamoto to further enhance connection reliability and prevent damage to the electronic component. *E.g.*, APPLE-1006, 16:52-62 (sealing resin "prevent[s] a gap from being formed between the semiconductor and the wiring patterns… An effect of preventing the semiconductor from being damaged and improving the reliability can be expected with the use of the sealing resin"); 17:62-63; APPLE-1004, [0018] (expressing similar goals of preventing the electronic component from damages, excellent insulation properties and connection reliability); APPLE-1003, ¶200.

Asahi's describes use of an "underfill resin used for ordinary flip chip bonding" as the sealing resin, but does not expressly articulate all implementation details. A POSITA thus would have predictably looked toward other teachings such as Sakamoto for implementation details, to achieve the desired functionality such as protection of the electronic component and improved connection reliability. APPLE-1006, 10:51-53, 11:62-63, 16:58-59; APPLE-1003, ¶201.

A POSITA would have recognized such benefits especially because Sakamoto describes enhancing reliability of embedding electronic components in a substrate with electrical connections to patterned wiring on the substrate. *Supra*, §§ VI.B.1, VI.G.1; APPLE-1003, ¶202. A POSITA would also have recognized this because of the additional benefits taught by Sakamoto, such as "ensuring that the resin film has insulating properties, and thermal expansion can be easily adjusted with a poorly soluble resin, keeping delamination from occurring between the interlayer resin insulating layers and the conductor circuits." APPLE-1004, [0052], [0060]"; APPLE-1003, ¶202.

Second, a POSITA would have been prompted to combine Asahi and Sakamoto because doing so was the application of known techniques (material used for Sakamoto's interlayer resin insulating layer) to a known device (Asahi's sealing resin) ready for improvement to yield predictable results (benefits articulated above). *KSR Int'l Co. v. Teleflex Inc*., 550 U.S. 398, 417 (2007)

("[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious."); *see also Intel Corporation v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. March 13, 2023) (reversing Board and finding that Petitioner "just had to show that [secondary reference's feature] was a 'suitable option' to replace [primary reference's feature]," and not that it was an "'improvement' in the categorical sense"). A POSITA would have had a reasonable expectation of success in making the proposed modifications given that Asahi and Sakamoto describe similar electronic modules involving use of curable insulating material between components (e.g., semiconductor chips) and wiring patterns to secure their mechanical and electrical connections, and because the modifications would have been implemented largely by using a hardened insulating polymer material for such insulating material—a configuration Sakamoto already demonstrates to be successful. APPLE-1003, ¶¶203-204. Moreover, for reasons similar to those described above, Asahi and Sakamoto describe analogous subject matter in the same field of endeavor and reasonably pertinent to the problems associated with semiconductor packaging and manufacturing addressed here. *Id*

2. Application to Challenged Claims

Elements [1pre]-[1a], [1c]-[1e];

Asahi-Sakamoto renders these elements obvious. *See, supra,* Ground 5A, Analysis of Elements [1pre]-[1a], [1c]-[1e]; APPLE-1003, ¶205.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Asahi in view of Sakamoto renders Element [1b] obvious. APPLE-1003, ¶206. As discussed above in §VI.F.1, Analysis of Element [1b], Sakamoto's interlayer resin insulating layer is made of ***polymer***, and is ***hardened*** through various methods such as "vacuum pressure bonding" with heat or using a curing agent. APPLE-1004, [0030], [0042], [0058]-[0059], [0060]; APPLE-1003, ¶206. The Asahi-Sakamoto combination implements sealing resin with the same material, in accordance with Sakamoto's teaching for its interlayer resin insulating layer. *Supra*, § VI.H.1; APPLE-1003, ¶206. Thus, the resulting combination's sealing resin is a ***hardened insulating polymer layer***. APPLE-1003, ¶206.

Furthermore, as discussed above in § VI.G.2, Analysis of Element [1b], Asahi's sealing resin is on the second surface of the electric insulation layer (***baseboard***). APPLE-1003, ¶206.

I. GROUND 6 – Sugaya anticipates or renders obvious Claim 1

1. Sugaya

Sugaya describes a "circuit component built-in module" with an embedded "circuit component 103a" such as a semiconductor chip. APPLE-1007, Title, Abstract, FIG. 1A, [0013], [0015], [0020]-[0021], [0086], [0092]; APPLE-1003, ¶¶90-91. Circuit component 103a is buried in an "insulating substrate 101 made of a first mixture 105 and a second mixture 106" and having "wiring patterns 102a and 102b formed on one principal surface and another principal surface of the insulating substrate 101[.]" APPLE-1007, Abstract, [0013] ("a first mixture [105] forming a region excluding the second mixture [106] in the insulating substrate [101]"), [0084], FIG. 1A; APPLE-1003, ¶91.

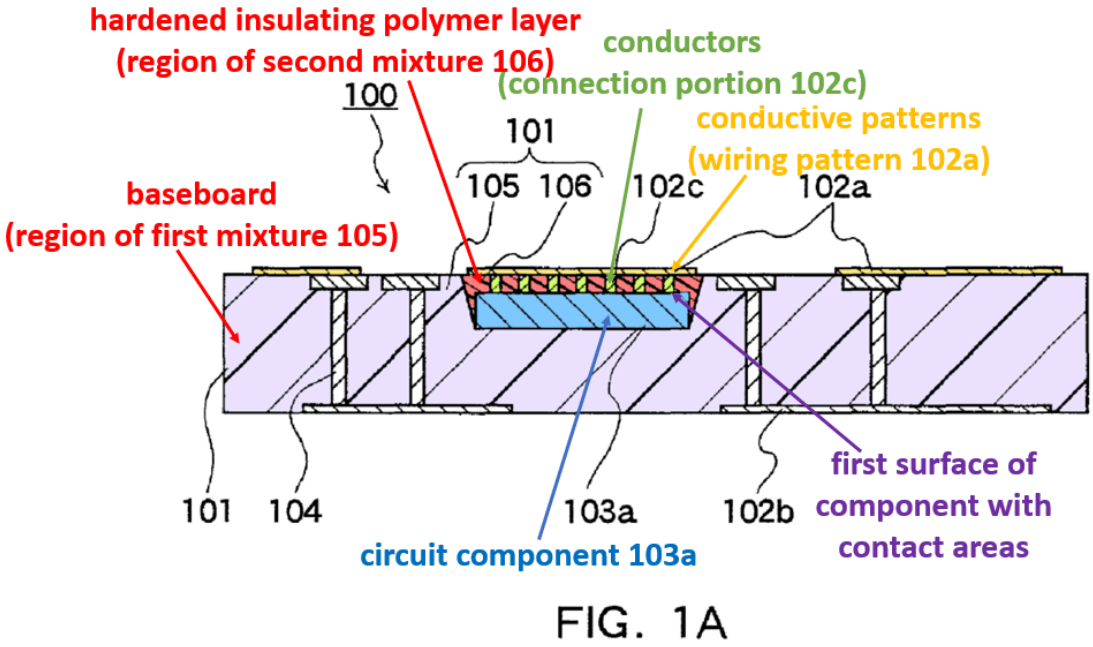


FIG. 1A

APPLE-1003, ¶91 (APPLE-1007, FIG. 1A (Annotated))

The "second mixture 106" contains polymer, is between the first wiring pattern [102a] and the circuit component [103a] and is cured, thus hardened.

APPLE-1007, [0013] ("a mixture of an inorganic filler and a thermosetting resin; …the mixture includes a second mixture"), [0024] ("the thermosetting resin includes" a list containing polymer), [0038], [0041] ("curing the second mixture"), [0060]; APPLE-1003, ¶92.

"[C]onnection portion" 102c between the wiring pattern 102a and the component 103a can be conductive adhesive and/or a gold bump within the second mixture 106 for forming electrical contacts between at least some of the wiring pattern 102a and at least some of the contact areas of the component (e.g., flat areas on the component where conductive adhesive or bumps may be formed). APPLE-1007, Abstract ("circuit component 103a electrically connected to the wiring pattern 102a"), [0013], [0109] ("A semiconductor chip 204 is electrically connected to the copper foil wiring pattern 211 via a conductive adhesive 212."), [0110] ("Instead of the conductive adhesive 212, a gold bump produced by a gold wire bonding or a solder bump may be formed on the side of the semiconductor chip 204 beforehand. … the solder bump also can be used together with the conductive adhesive"), [0191], FIG. 1A; APPLE-1003, ¶93.

2. Application to Challenged Claim

Element [1pre] An electronic module, comprising

If the preamble is deemed limiting, Sugaya teaches [1pre]. APPLE-1003, ¶208. For example, Sugaya describes a "circuit component built-in module" with

an embedded "circuit component" such as a semiconductor chip. APPLE-1007, Title, Abstract, FIG. 1A, [0013], [0015], [0086], [0092]. A POSITA would have recognized that Sugaya's circuit component built-in module is an electronic module. APPLE-1003, ¶208.

Element [1a] a baseboard having a first surface and a second surface;

Sugaya discloses Element [1a]. APPLE-1003, ¶¶209-211. In particular, Sugaya describes an "insulating substrate 101" comprising a region formed by "a first mixture 105" (***baseboard***) and a region formed by "a second mixture 106," with a circuit component buried in the first mixture 105 and wiring pattern formed on at least one principal surface of the insulating substrate. APPLE-1007, Abstract, [0013], FIG. 1A (showing the region of first mixture 105 ***having a first surface and a second surface***); APPLE-1003, ¶209. Sugaya explains that the second mixture 106 sealing at least a connection portion between wiring pattern 102a and a circuit component 103a, and the first mixture 105 forming a region excluding the second mixture 106. APPLE-1007, [0013], [0084]; APPLE-1003, ¶209.

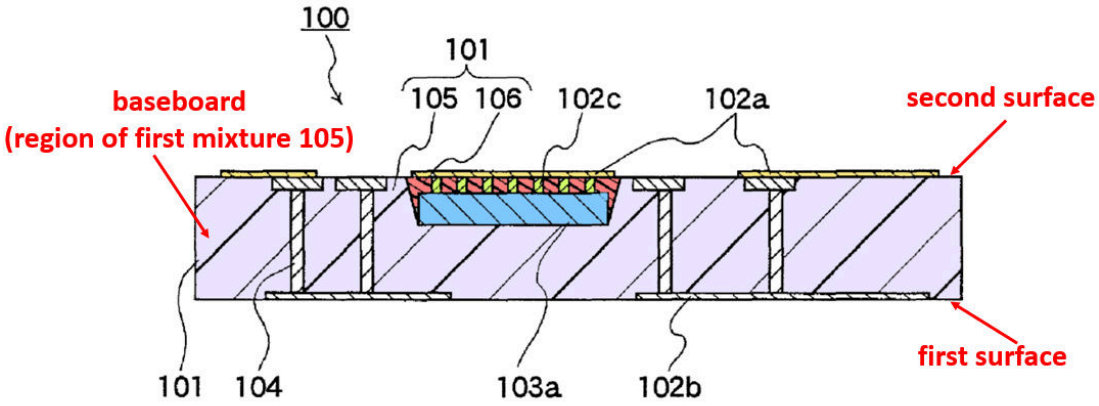


FIG. 1A

APPLE-1003, ¶209 (APPLE-1007, FIG. 1A (Annotated))

Sugaya's first mixture 105 includes "a mixture of an inorganic filler and a thermosetting resin" ([0013], [0085]), the inorganic filler includes glass (e.g., "SiO_2, (in particular, amorphous SiO_2)," and the thermosetting resin "includes at least one resin selected from the group consisting of an epoxy resin, a phenol resin, a cyanate resin and a polyphenylene ether resin because these resins are excellent in thermal resistance or insulating property." APPLE-1007, [0023]-[0024]; *see also e.g.*, [0022], [0023] (describing inorganic filler, including glass, "SiO_2, (in particular, amorphous SiO_2)"), [0040], [0085], [0088], [0089] ("An epoxy resin is particularly desirable because of its high heat resistance."), [0096]-[0097], [0269], [0287]. Sugaya's construction is like that of the '201 patent, which likewise describes a baseboard that is an insulating board for burying electronic components with conductive patterns on its surfaces, and similarly made of a "glass-fibre

reinforced epoxy board." APPLE-1001, 2:22-26, 3:49-57. A POSITA would know that glass fibers are an inorganic filler. APPLE-1003, ¶¶210-211.

Element [1b] a hardened insulating polymer layer on the second surface of the baseboard;

Sugaya discloses Element [1b]. APPLE-1003, ¶¶212-213. For example, Sugaya describes a "second mixture 106" between wiring pattern 102a (portions of which on the second surface of the baseboard) and the circuit component 103a. APPLE-1007, Abstract, [0041], [0084]-[0085], FIG. 1A; APPLE-1003, ¶212.

The "second mixture 106" contains polymer and is cured into a hardened layer. APPLE-1007, [0013] ("a mixture of an inorganic filler and a thermosetting resin; …the mixture includes a second mixture"), [0024] ("the thermosetting resin includes at least one resin selected from the group consisting of an epoxy resin, a phenol resin, a cyanate resin and a polyphenylene ether resin" – a list containing polymer), [0038], [0041] ("curing the second mixture"), [0060], [0085], [0089]; APPLE-1003, ¶213. A POSITA would have recognized that the thermosetting resin material of the second mixture contains polymer, and after curing with heat, the region formed by second mixture 106 becomes a ***hardened insulating polymer layer***. APPLE-1003, ¶213.

Figure 1A shows the region of second mixture 106 (***hardened insulating polymer layer***) ***on the second surface of the*** region of first mixture 105

(***baseboard***). APPLE-1007, [0013]; *supra*, §VI.I.2, Analysis of Element [1a]; APPLE-1003, ¶213.

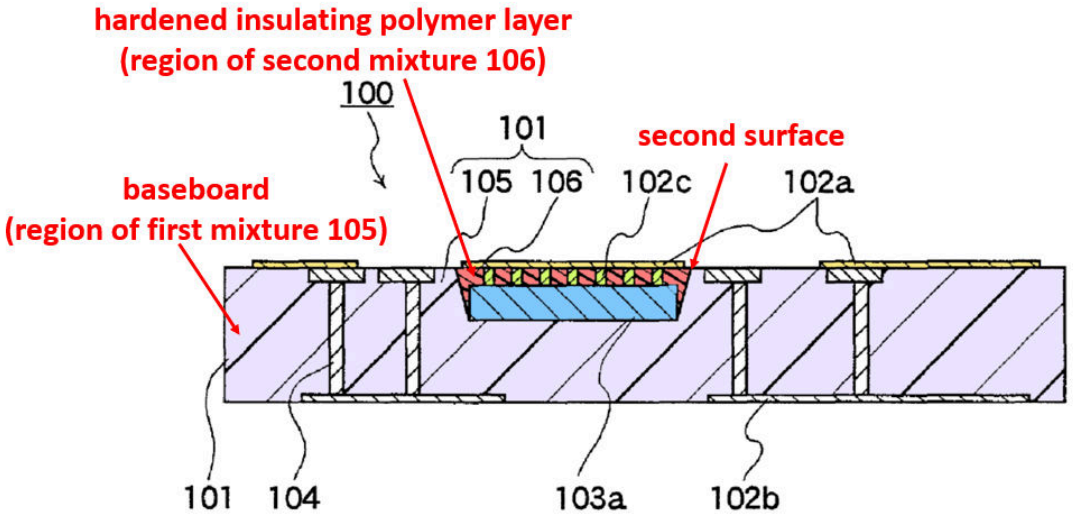


FIG. 1A

APPLE-1003, ¶213 (APPLE-1007, FIG. 1A (Annotated))

To be clear, as shown in FIG. 1A, for example, the region of first mixture 105 includes a second surface that the region of second mixture 106 is in contact with, such that the region of second mixture 106 is on the second surface of the region of first mixture 105. APPLE-1003, ¶213.

Element [1c] at least one component within the baseboard, the component having contact areas on a first surface of the component, said first surface of the component being against the hardened insulating polymer layer;

Sugaya teaches Element [1c]. APPLE-1003, ¶¶214-216. For example, Sugaya discloses a "circuit component 103a" such as a semiconductor chip placed "in an internal portion [inside the region of first mixture 105] of the insulating

substrate 101" (***at least one component within the baseboard***). APPLE-1007, Abstract; *see also e.g.*, Title, [0013], [0015] ("a circuit component built-in module preferably integrates a semiconductor device"), [0086], [0092], FIG. 1A; APPLE-1003, ¶¶214-215.

Sugaya explains that "conductive adhesive 212" (e.g., FIG. 2A) and/or "a gold bump produced by a gold wire bonding or a solder bump may be formed on the side of the semiconductor chip" to form a connection portion between the wiring pattern and the circuit component. APPLE-1007, [0110], [0013], [0021], [0191], FIG. 1A; APPLE-1003, ¶216. A POSITA would have understood that the semiconductor chip has flat areas on a side where such conductive adhesive and/or connection bumps are formed, and these flat areas on the side of the semiconductor chip provide ***contact areas on a first surface of the component***. APPLE-1003, ¶216.

Figure 1A shows circuit component 103a within the region of first mixture 105 (***baseboard***), and the first surface of component 103a with flat contact areas to form connection portion 102c ***being against*** the region of second mixture 106 (***the hardened insulating polymer layer***). APPLE-1007, [0013] ("a second mixture … seals at least a connection portion between the wiring pattern [102a] and the circuit component [103a]"), [0014], [0038], [0041]; *supra*, §§ VI.I.2, Analyses of Elements [1a], [1b]; APPLE-1003, ¶216.

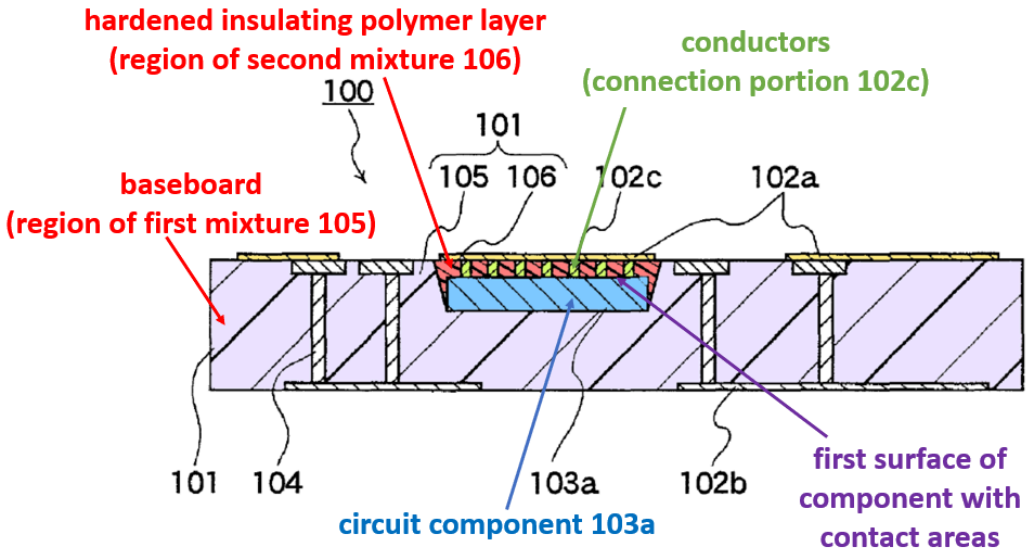


FIG. 1A

APPLE-1003, ¶216 (APPLE-1007, FIG. 1A (Annotated))

Element [1d] conductive patterns on the hardened insulting polymer layer; and

Sugaya discloses Element [1d]. APPLE-1003, ¶¶217-218. For example, Sugaya describes "wiring pattern 102a" formed on the region of second mixture 106 (***hardened insulating polymer layer***). APPLE-1007, Abstract ("wiring patterns 102a and 102b formed on one principal surface and another principal surface of the insulating substrate 101, a circuit component 103a **electrically connected** to the wiring pattern 102a and sealed with the second mixture 106 in an internal portion of the insulating substrate 101"), [0013]; APPLE-1003, ¶217. A POSITA would have recognized that Sugaya's wiring patterns are ***conductive patterns*** to form electrical connections. *See also e.g.*, APPLE-1007, [0016], [0025], ("the wiring pattern includes copper"), [0026]. The annotated Figure 1A below shows wiring pattern 102a (***conductive patterns***) on the region of second

mixture 106 (***hardened insulating polymer layer***). *Supra*, §VI.I.2, Analysis of Element [1b]; APPLE-1003, ¶218.

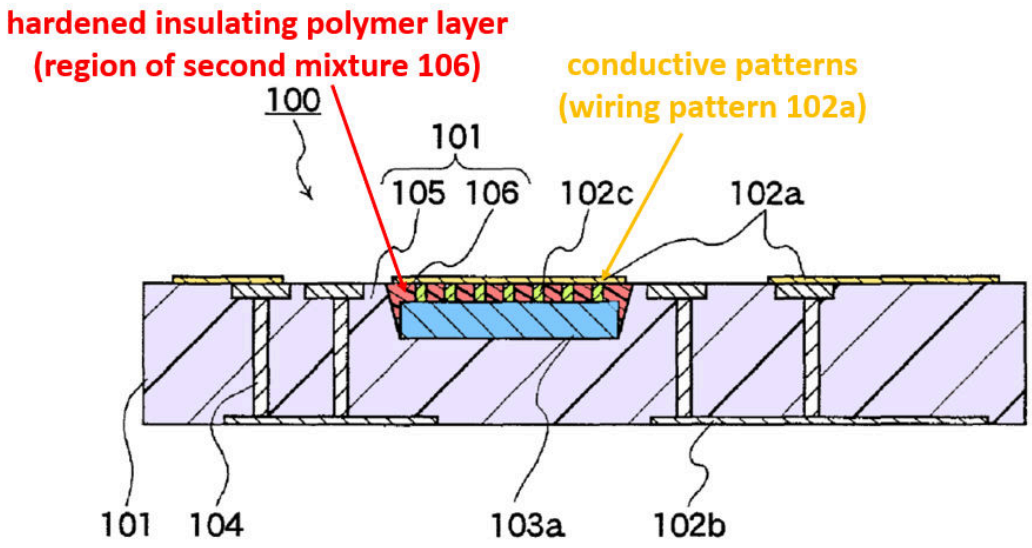


FIG. 1A

APPLE-1003, ¶218 (APPLE-1007, FIG. 1A (Annotated))

Element [1e] conductors within the hardened insulating polymer layer for forming electrical contacts between at least some of the conductive patterns and at least some of the contact areas of the component.

Sugaya discloses Element [1e]. APPLE-1003, ¶¶219-220. As discussed above in §VI.I.2, Analysis of Element [1c], Sugaya explains that "conductive adhesive 212" (e.g., FIG. 2A) and/or "a gold bump produced by a gold wire bonding or a solder bump" can be "formed on the side of the semiconductor chip" to form a connection portion between the wiring pattern and the circuit component. APPLE-1007, [0110]; *see also id.*, [0013], [0191], FIG. 1A; APPLE-1003, ¶219.

Also discussed above in §VI.I.2, Analysis of Element [1b], Sugaya's "second mixture 106" (forming the ***hardened insulating polymer layer***) is injected into the connection portion between wiring pattern102a and the circuit component 103a and cured to seal the connection portion and the side part of wiring pattern 102a and the circuit component 103a. APPLE-1007, Abstract, [0013], [0041], [0024], [0060]; APPLE-1003, ¶220. The annotated Figure 1A below shows connection portion 102c (***conductors***) within the region of second mixture 106 (***hardened insulating polymer layer***) for forming electrical contacts between portions of wiring pattern 102a (***conductive patterns***) and the ***contact areas*** of the component 103a. APPLE-1003, ¶220.

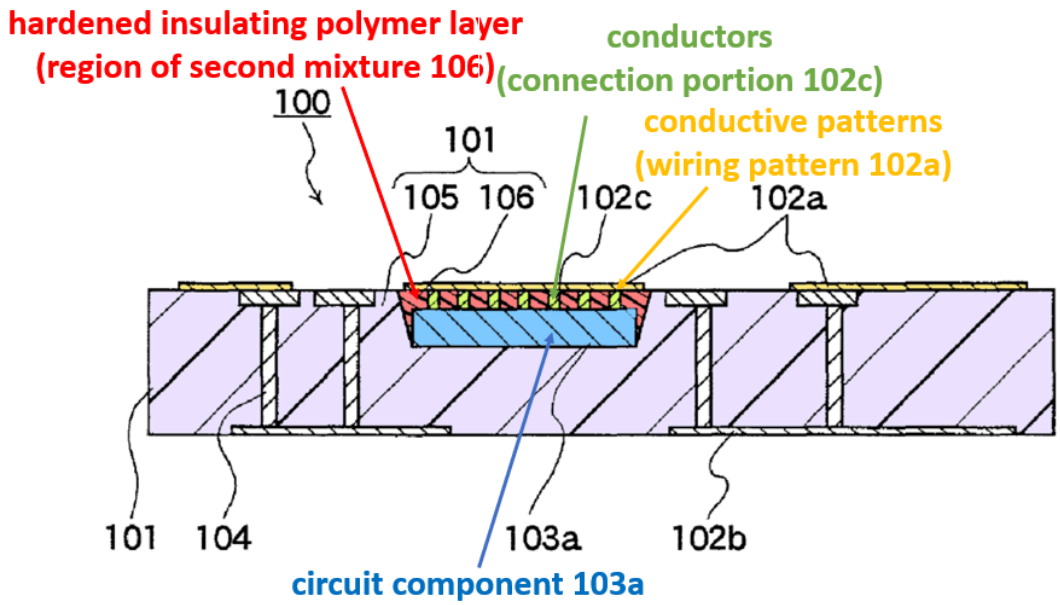


FIG. 1A

APPLE-1003, ¶220 (APPLE-1007, FIG. 1A (Annotated))

VII. THE BOARD SHOULD NOT EXERCISE ITS DISCRETION UNDER 325(D) TO DENY HEARING THESE INVALIDITY ISSUES FOR THE FIRST TIME IN THIS PETITION

In considering its discretion under §325(d), "the Board uses the following two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

Here, while Asahi and a family member of Sugaya were cited on the face of the '201 patent, none of the above references were applied in a substantive office action, yet they are directly material to patentability. Even assuming the first prong were met, the second *Advanced Bionics* prong makes clear that institution should not be denied under 325(d) because it was material error to overlook Asahi and Sugaya. *See Advanced Bionics*, IPR2019-01469, Paper 6 at 8, 9, n.10; *see also Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential).

Here, the examiner erred by overlooking the clear and unambiguous teachings of Asahi and Sugaya, because as explained in detail in Section VI.C,

Asahi in combination with other prior art at least renders obvious all of the challenged claims, and as explained in Section VI.E, Sugaya anticipates or renders obvious all of the challenged claims. *Advanced Bionics*, IPR2019-01468, Paper 6 at 10; *see also*, *Dish Network et al. v. Sound View Innovations, LLC*, IPR2020-01041, Paper 13 at 21 (PTAB Jan. 19, 2021).

In sum, the clear and unambiguous disclosures of Asahi and Sugaya set out in detail in this petition, which demonstrate the obviousness of the challenged claims, substantially outweigh the significance of Asahi and a family member of Sugaya being cited on the face of the '201 Patent. The record is otherwise silent regarding Asahi and Sugaya. In view of the foregoing, the Board should not exercise its discretion under § 325(d) to deny institution.

VIII. The *Fintiv* Factors Weigh in Favor of Institution – 35 U.S.C. § 314

Essentially all of the *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written

Decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors. Moreover, a Motion to Transfer to the Northern District of California remains pending. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while litigation remains in early stages. As noted above, Motions to Transfer remains pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds, outweighing any inefficiencies.

IX. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the Patent and Trademark Office to charge any fees to Deposit Account No. 06-1050.

X. CONCLUSION

Petitioner respectfully requests institution of IPR.

XI. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or petitions for inter partes review for the ’201 Patent. The ’201 Patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024; *Samsung Electronics Co., Ltd. et al v. ImberaTek LLC*, IPR2022-01597 (PTAB), filed September 30, 2022, *ImberaTek LLC v. Samsung Electronics Co., Ltd. et al.*, 2-22-cv-00233 (EDTX), filed June 24, 2022.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0196IP1@fr.com.

Respectfully submitted,

Dated: February 6, 2025

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(Control No. IPR2025-00581)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,673 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 6, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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