

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS
AMERICA, INC.; and SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
Petitioner,

v.

IMBERATEK LLC,
Patent Owner.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Before DONNA M. PRAISS, JON B. TORNQUIST, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Settlement Prior to Institution of Trial
37 C.F.R. § 42.74

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

With our authorization, Petitioner, Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC, and Patent Owner, ImberaTek LLC, filed a Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases. Paper 8 (“Joint Motions”).¹ In their Joint Motions, the parties contend that dismissal is appropriate as the *inter partes* reviews (“IPRs”) are in their early stages and the parties “have settled all disputes” related to the involved patents. *Id.* at 1–2.

With their Joint Motions, the parties filed (1) a copy of a Settlement and Patent License Agreement that the parties represent “resolves the disputes in the above-captioned *inter partes*” reviews, (2) a Confirmatory Letter from Patent Owner to Petitioner acknowledging and confirming certain facts and rights related to the Settlement and Patent License Agreement, and (3) a Joint Request to treat the settlement documents as business confidential information, to be kept separate from the files of the above-captioned patents. Ex. 1022 (“Settlement and Patent License Agreement”); Ex. 1023 (“Confirmatory Letter”); Paper 9 (“Joint Request”).

“There are strong policy reasons to favor settlement between the parties to a proceeding,” and “[t]he Board expects that a proceeding will terminate after the filing of a settlement agreement, unless the Board has already decided the merits of the proceeding.” Patent Trial and Appeal

¹ We cite to papers and exhibits filed in IPR2022-01597. Similar papers and exhibits were filed in each of the above-captioned cases.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Board Consolidated Trial Practice Guide November 2019, at 86 (citing 35 U.S.C. §§ 317(a), 327). The above-captioned IPRs are at an early stage, with the Board not yet reaching the merits of the petitions or issuing institution decisions. Thus, we find it is appropriate to dismiss the petitions and terminate the proceedings in each of the above-captioned IPRs.

We also find it appropriate to treat the settlement documents as business confidential information, to be kept separate from the files of the involved patents.

Accordingly, it is

ORDERED that the Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases is *granted*;

FURTHER ORDERED that the parties' Joint Request that the settlement documents (Exs. 1022, 1023) be treated as business confidential information and kept separate from the files of the involved patents is *granted*; and

FUTHER ORDERED that the proceedings in the above-captioned IPRs are *terminated*.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

FOR PETITIONER:

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv233	DATE FILED 6/24/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, et al
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,609,527	10/27/2009	ImberaTek LLC
2 8,222,723	7/17/2012	ImberaTek LLC
3 8,368,201	2/5/2013	ImberaTek LLC
4 7,989,944	8/2/2011	ImberaTek LLC
5 8,238,113	8/7/2012	ImberaTek LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 10/31/2022	INCLUDED BY ☒ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 11,071,207	7/20/2021	ImberaTek LLC
2 7,732,909	6/8/2010	ImberaTek LLC
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,107,324	8/15/2015	ImberaTek LLC
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

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2 8,222,723	7/17/2012	ImberaTek LLC
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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5967120

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	7732909	
Patent Number:	7989944	
Patent Number:	7609527	
Patent Number:	8817485	
Patent Number:	8034658	
Patent Number:	8222723	
Patent Number:	8487194	
Patent Number:	9232658	
Patent Number:	8351214	
Patent Number:	8455994	
Patent Number:	8368201	
Patent Number:	9622354	
Patent Number:	9691724	
Patent Number:	9107324	
Patent Number:	10231335	
Patent Number:	10085345	
Patent Number:	10010019	
Patent Number:	10085347	
Patent Number:	9324647	
Patent Number:	9883587	

Property Type	Number
Patent Number:	9674948
Patent Number:	9820375
Patent Number:	10470346
Application Number:	14580257
Application Number:	15355096
Application Number:	16104979

CORRESPONDENCE DATA

Fax Number: (703)643-9789

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Email: yoon@capitoliplaw.com

Correspondent Name: YEASUN YOON

Address Line 1: 20319 KIAWAH ISLAND DR

Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER:	PA01GETOIMBERATEK02
NAME OF SUBMITTER:	YEASUN YOON
SIGNATURE:	/yoon/
DATE SIGNED:	02/18/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7

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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this “**Assignment**”) is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company (“**Assignor**”), in favor of **ImberaTek, LLC**, a Delaware limited liability company (“**Assignee**”).

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the “**Patent Sale Agreement**”); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the “**Patents**”).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

Name: PATRICK K. PATNODE

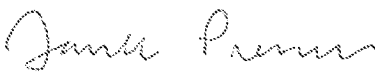
Title: AUTHORIZED SIGNATORY

Acknowledgement:

State of New York)

ss.

County of Schenectady)


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8024403
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRPI0307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A I, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A I, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1 , US10010019B2, US2018352689A I	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15'937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	08/11/2015	9107324	IMB 22 US CON	1010
95002	7590	07/22/2015		

Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Petteri Palm, Helsinki, FINLAND;
Risto Tuominen, Helsinki, FINLAND;
Antti Iihola, Helsinki, FINLAND;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON	1010
95002	7590	07/02/2015	EXAMINER	
Seppo Laine Oy Joshua P. Wert Itamerenkatu 3B Helsinki, FI00180 FINLAND			NORRIS, JEREMY C	
			ART UNIT	PAPER NUMBER
			2847	
			MAIL DATE	DELIVERY MODE
			07/02/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Corrected Notice of Allowability	Application No. 14/231,758	Applicant(s) PALM ET AL.	
	Examiner JEREMY C. NORRIS	Art Unit 2847	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Notice of Allowance filed 3-31-2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
 a) ☒ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 12/990,785.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	5. ☒ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____
--	---

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

18 (currently amended). The circuit module of claim ~~[[18]]~~17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

20 (currently amended). The circuit module of claim ~~[[18]]~~19, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 1-20 are allowed.

Response to Amendment

The preceding Examiner's Amendment is provided to clear up claim dependency.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY C. NORRIS whose telephone number is (571)272-1932. The examiner can normally be reached on Mon, Wed, Fri 10am-6pm; Tues, Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy J. Thompson can be reached on 571-272-2342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JEREMY C. NORRIS
Primary Examiner
Art Unit 2847

/JEREMY C. NORRIS/
Primary Examiner, Art Unit 2847

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

95002 7590 03/31/2015
 Seppo Laine Oy
 Joshua P. Wert
 Itamerenkatu 3B
 Helsinki, FI00180
 FINLAND

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
 I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON	1010

TITLE OF INVENTION: CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/30/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
NORRIS, JEREMY C	2847	257-762800

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Seppo Laine Oy
 2.
 3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

GE Embedded Electronics Oy

Helsinki (FI)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first resupply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Joshua P. Wert Reg. No. 65880/

Date 2015-06-25

Typed or printed name Joshua P. Wert

Registration No. 65880

Electronic Patent Application Fee Transmittal				
Application Number:		14231758		
Filing Date:		01-Apr-2014		
Title of Invention:		CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
First Named Inventor/Applicant Name:		Petteri Palm		
Filer:		Joshua Paul Wert/Ross Worrell		
Attorney Docket Number:		IMB 22 US CON		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	22734591
Application Number:	14231758
International Application Number:	
Confirmation Number:	1010
Title of Invention:	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert/Ross Worrell
Filer Authorized By:	Joshua Paul Wert
Attorney Docket Number:	IMB 22 US CON
Receipt Date:	25-JUN-2015
Filing Date:	01-APR-2014
Time Stamp:	07:27:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	23867
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IMB22USCON_2015-06-25_Issue_fee.pdf	163513 35a1d189292ad5d9c20b9ff3a6355a5eee6c a4b9	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32483 17306c9e81668e8c2277eb92382562718ad 0a71c	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			195996		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

95002 7590 03/31/2015
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

EXAMINER

NORRIS, JEREMY C

ART UNIT

PAPER NUMBER

2847

DATE MAILED: 03/31/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON	1010

TITLE OF INVENTION: CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/30/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

95002 7590 03/31/2015
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON	1010

TITLE OF INVENTION: CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	06/30/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
NORRIS, JEREMY C	2847	257-762000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON	1010

95002	7590	03/31/2015
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Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

EXAMINER
NORRIS, JEREMY C

ART UNIT	PAPER NUMBER
2847	

DATE MAILED: 03/31/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<i>Notice Requiring Inventor's Oath or Declaration</i>	Application No. 14/231,758	Applicant(s) Petteri Palm	
	Examiner NORRIS, JEREMY C	Art Unit 2847	

This notice is an attachment to the Notice of Allowability (PTOL-37), or the Notice of Allowability For A Design Application (PTOL-37D).

An inventor's oath or declaration in compliance with 37 CFR 1.63 or 1.64 executed by or with respect to each inventor has not yet been submitted.

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor (for any inventor for which a compliant oath, declaration, or substitute statement has not yet been submitted) **MUST** be filed no later than the date on which the issue fee is paid. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application.

A properly executed inventor's oath to declaration has not been received for the following inventor(s):

If applicant previously filed one or more oaths, declarations, or substitute statements, applicant may have received an informational notice regarding deficiencies therein.

The following deficiencies are noted:

INFORMAL ACTION PROBLEMS

A new inventor's oath or declaration that identifies this application (e.g., by Application Number and filing date) is required. The inventor's oath or declaration does not comply with 37 CFR 1.63 in that it:

- does not state that the above-identified application was made or authorized to be made by the person executing the oath or declaration: **Petteri Palm, Risto Tuominen** , and **Antti Iihola**.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/231,758	Applicant(s) PALM ET AL.	
	Examiner JEREMY C. NORRIS	Art Unit 2847	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Declaration filed 05/20/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 12/990,785.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d). The certified copy has been filed in parent Application No. 12/990,785, filed on 11/03/2010.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance: Claim 1 states the limitation "contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal, a contact surface area (Acont 1) between the intermediate layer and the contact terminal being less than a surface area (Apad) of the contact terminal." This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art. Claim 17 states the limitation "a contact surface area (Acont 1) between the intermediate layer and the contact terminal being less than a surface area (Apad) of the contact terminal". This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art. Claim 19 states the limitation "a contact surface area (Acont

1) between the intermediate layer and the contact terminal being less than a surface area (Apad) of the contact terminal. This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,396,148,

US 2006/0056152 A1,

US 2004/0246690 A1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY C. NORRIS whose telephone number is (571)272-1932. The examiner can normally be reached on Mon, Wed, Fri 10am-6pm; Tues, Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy J. Thompson can be reached on 571-272-2342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JEREMY C. NORRIS
Primary Examiner
Art Unit 2847

/JEREMY C. NORRIS/
Primary Examiner, Art Unit 2847

Notice of References Cited	Application/Control No. 14/231,758	Applicant(s)/Patent Under Reexamination PALM ET AL.	
	Examiner JEREMY C. NORRIS	Art Unit 2847	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,396,148	05-2002	Eichelberger et al.	257/758
*	B	US-2006/0056152	03-2006	Li et al.	361/697
*	C	US-2004/0246690	12-2004	Nakamura et al.	361/763
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 14231758	Applicant(s)/Patent Under Reexamination PALM ET AL.
	Examiner JEREMY C NORRIS	Art Unit 2847

CPC- SEARCHED		
Symbol	Date	Examiner
h05k 1/188	3-13-15	jcsn
h01l 24/19, 24/24	3-13-15	jcsn

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
reviewed file wrapper of 12/990,785	3-16-15	jcsn

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
h01l	24/19, 24/24	3-13-15	jcsn
h05k	1/188	3-13-15	jcsn

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Issue Classification 	Application/Control No. 14231758	Applicant(s)/Patent Under Reexamination PALM ET AL.	
	Examiner JEREMY C NORRIS	Art Unit 2847	

CPC					
Symbol				Type	Version
H05K	1		188	F	2013-01-01
Y10T	29		4913	A	2015-01-15
Y10T	29		49117	A	2015-01-15
H01L	21		486	A	2013-01-01
H01L	23		5384	I	2013-01-01
H01L	23		5389	I	2013-01-01
H01L	24		24	I	2013-01-01
H01L	24		82	I	2013-01-01
H01L	2221		68359	A	2013-01-01
H01L	2224		13144	A	2013-01-01
H01L	2224		13147	A	2013-01-01
H01L	2224		24227	A	2013-01-01
H01L	2924		01005	A	2013-01-01
H01L	2924		01013	A	2013-01-01
H01L	2924		0102	A	2013-01-01
H01L	2924		01027	A	2013-01-01
H01L	2924		01029	A	2013-01-01
H01L	2924		0103	A	2013-01-01
H01L	2924		01033	A	2013-01-01
H01L	2924		01074	A	2013-01-01
H01L	2924		01075	A	2013-01-01
H01L	2924		01078	A	2013-01-01
H01L	2924		01079	A	2013-01-01
H01L	2924		01082	A	2013-01-01
H01L	2924		14	A	2013-01-01
H01L	2924		1433	A	2013-01-01
H01L	2924		15153	A	2013-01-01
H01L	2924		1517	A	2013-01-01
H05K	3		305	A	2013-01-01
H05K	2201		0355	A	2013-01-01
H05K	2201		09509	A	2013-01-01
NONE (Assistant Examiner) _____ (Date) _____ /JEREMY C NORRIS/ Primary Examiner, Art Unit 2847 (Primary Examiner) _____ (Date) _____				Total Claims Allowed: 20 O.G. Print Claim(s) O.G. Print Figure 1 9	

Issue Classification 	Application/Control No. 14231758	Applicant(s)/Patent Under Reexamination PALM ET AL.	
	Examiner JEREMY C NORRIS	Art Unit 2847	

H05K	2201	0969	A	2013-01-01
H05K	2201	10674	A	2013-01-01
H05K	2203	063	A	2013-01-01
H01L	24	19	I	2013-01-01
H01L	2924	01006	A	2013-01-01
H01L	2924	01023	A	2013-01-01
H01L	2924	01024	A	2013-01-01
H01L	2924	01047	A	2013-01-01
H01L	2224	24137	A	2013-01-01
H01L	2224	04105	A	2013-01-01
H01L	2224	12105	A	2013-01-01
H01L	2224	92144	A	2013-01-01
H01L	23	49866	I	2013-01-01
H01L	2924	12041	A	2013-01-01
H01L	2924	1461	A	2013-01-01
H01L	2224	0401	A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
H01L		2924	/	1517	A	1	1	2013-01-01
H01L		2924	/	15153	A	1	2	2013-01-01
H01L		2224	/	24227	A	2	1	2013-01-01
H01L		2924	/	1517	A	2	2	2013-01-01
H01L		2924	/	12041	A	3	1	2013-01-01
H01L		2924	/	00	A	3	2	2013-01-01
H01L		2924	/	1461	A	4	1	2013-01-01
H01L		2924	/	00	A	4	2	2013-01-01

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 20	
/JEREMY C NORRIS/ Primary Examiner, Art Unit 2847 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 9

Issue Classification 	Application/Control No. 14231758	Applicant(s)/Patent Under Reexamination PALM ET AL.	
	Examiner JEREMY C NORRIS	Art Unit 2847	

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED									
						H	0	5	K	1 / 18 (2006.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 20	
/JEREMY C NORRIS/ Primary Examiner.Art Unit 2847 (Primary Examiner) _____ (Date) _____		03/23/2015 O.G. Print Claim(s) 1	O.G. Print Figure 9



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 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1010

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/231,758	04/01/2014	257	2847	IMB 22 US CON		
APPLICANTS INVENTORS Petteri Palm, Helsinki, FINLAND; Risto Tuominen, Helsinki, FINLAND; Antti Iihola, Helsinki, FINLAND; ** CONTINUING DATA ***** This application is a CON of 12/990,785 11/03/2010 PAT 8699233 * which is a 371 of PCT/FI09/50383 05/11/2009 (*)Data provided by applicant is not consistent with PTO records. ** FOREIGN APPLICATIONS ***** FINLAND 20085443 05/12/2008 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/22/2014						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/JEREMY C NORRIS/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 15	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Seppo Laine Oy Joshua P. Wert Itamerenkatu 3B Helsinki, FI00180 FINLAND						
TITLE Circuit module and method of manufacturing the same						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON

CONFIRMATION NO. 1010

PUBLICATION NOTICE



OC000000069925493

95002
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Title:Circuit module and method of manufacturing the same

Publication No.US-2014-0210090-A1

Publication Date:07/31/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 14/231,758 Confirmation No. : 1010
Applicant : GE Embedded Electronics Oy
Filed : 2014-04-01
TC/AU : Not Yet Assigned
Examiner : Not Yet Assigned

Attorney Docket No. : IMB 22 US CON

M/S Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION FILED UNDER 37 CFR 1.63(d)

Sir:

In response to the INFORMATIONAL NOTICE TO APPLICANT mailed April 22, 2014, a copy of a previously executed declaration is attached herein in accordance with 37 CFR 1.63(d). The present declaration was filed in the parent application 12/990,785 on March 11, 2010. Should there be any problems with the acceptance of the present declaration, the Office is respectfully requested to call the undersigned at 571-480-8372 in order to expedite the pre-examination formalities process.

Respectfully submitted,

/ Joshua P. Wert Reg. No. 65880/

Joshua P. Wert
Reg. No. 65880
Seppo Laine Oy
Itämerenkatu 3 B
FIN-00180 Helsinki, Finland
Tel. (US) +1 571-480-8372

May 20, 2014

Seppo Laine Oy

JPW / rw

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of
Invention

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☒ The attached application, or
☐ Application No. _____ filed on _____
☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Petteri Palmi Date: 29.10.2010

Signature: [Signature] Citizen of: FI

Inventor two: Risto Tuominen Date: 6.10.2010

Signature: [Signature] Citizen of: FI

☒ Additional inventors or a legal representative are being named on 1 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9198 and select option 2.

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
	Page <u>2</u> of <u>2</u>

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Anttl		Iihola	
Inventor's Signature 		Date <u>Oct. 28 2010</u>	
Residence: City	State	Country	FI Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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Electronic Acknowledgement Receipt	
EFS ID:	19072825
Application Number:	14231758
International Application Number:	
Confirmation Number:	1010
Title of Invention:	Circuit module and method of manufacturing the same
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert/Ross Worrell
Filer Authorized By:	Joshua Paul Wert
Attorney Docket Number:	IMB 22 US CON
Receipt Date:	20-MAY-2014
Filing Date:	01-APR-2014
Time Stamp:	07:45:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IMB22USCON_2014-05-20_Response_NOMP.pdf	229286 ebc352255196f9066703cae4b010438cd9584444	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Applicant Response to Pre-Exam Formalities Notice	1	1
	Oath or Declaration filed	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		229286	
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/231,758			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 80 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 420 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
				TOTAL		TOTAL	1600		
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
		TOTAL ADD'L FEE				TOTAL ADD'L FEE			
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)		
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	x =	=		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	x =	=		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
		TOTAL ADD'L FEE				TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									



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APPLICATION NUMBER	FILING or 371 (c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/231,758	04/01/2014	2811	1600	IMB 22 US CON	20	3

CONFIRMATION NO. 1010

FILING RECEIPT



OC000000067946827*

95002
Seppo Laine Oy
Joshua P. Wert
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Helsinki, FI00180
FINLAND

Date Mailed: 04/22/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Petteri Palm, Helsinki, FINLAND;
Risto Tuominen, Helsinki, FINLAND;
Antti Iihola, Helsinki, FINLAND;

Applicant(s)

Petteri Palm, Helsinki, FINLAND;
Risto Tuominen, Helsinki, FINLAND;
Antti Iihola, Helsinki, FINLAND;

Assignment For Published Patent Application

GE EMBEDDED ELECTRONICS OY, Helsinki, FINLAND

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/990,785 11/03/2010 PAT 8699233 *
which is a 371 of PCT/FI09/50383 05/11/2009
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
FINLAND 20085443 05/12/2008 No Access Code Provided

If Required, Foreign Filing License Granted: 04/22/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/231,758**

Projected Publication Date: 07/31/2014

Non-Publication Request: No

Early Publication Request: No
Title

Circuit module and method of manufacturing the same

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/231,758	04/01/2014	Petteri Palm	IMB 22 US CON

CONFIRMATION NO. 1010

95002

Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

NOTICE



Date Mailed: 04/22/2014

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

A new inventor's oath or declaration that identifies this application (e.g., by Application Number and filing date) is required. The inventor's oath or declaration does not comply with 37 CFR 1.63 in that it:

- does not state that the above-identified application was made or authorized to be made by the person executing the oath or declaration.

Petteri Palm
Risto Tuominen
Antti Iihola

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	<i>Attorney Docket No.</i>	IMB 22 US CON
	<i>First Inventor</i>	PALM, Petteri
	<i>Title</i>	Circuit module and method of manufa
	<i>Express Mail Label No.</i>	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450
1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) 2. ☐ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages <u>47</u>] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>15</u>] 5. Oath or Declaration [Total Sheets <u>3</u>] a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☒ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee _____ 10. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney 11. ☐ English Translation Document (if applicable) 12. ☐ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 13. ☐ Preliminary Amendment 14. ☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. ☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other: _____
18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: <u>12/990,785</u> Prior application information: Examiner <u>NORRIS, JEREMY C</u> Art Unit: <u>2835</u>	

19. CORRESPONDENCE ADDRESS					
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Country		Telephone		Email	
Signature		/Joshua P. Wert Reg. No. 65880/		Date 2014-04-01	
Name (Print/Type)		Joshua P. Wert		Registration No. (Attorney/Agent) 65880	

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Technical Field

5 The present invention relates to circuit modules, which comprise an insulator layer and, inside the insulator layer, at least one component, which comprises contact areas. In addition, the circuit modules comprise conductors on the surface of the insulator layer, through which a component can be connected to become part of a circuit outside the component. For creating electrical contacts, the circuit modules comprise contact
10 elements between the contact areas of the component and the conductors.

The invention also relates to methods for manufacturing the aforementioned circuit modules.

15 Background Art

In the background art, several different ways are described, by means of which circuit modules containing components located inside an insulator material can be manufactured. The background art also discloses several solutions for manufacturing
20 electrical contacts to the contact terminals of a component, by means of contact elements, and methods for manufacturing a conductor-pattern layer connected to the contact elements.

When evaluating circuit modules and manufacturing methods, attention can be paid, for
25 example, to the circuit module's properties achieved by the method, for example, its price, mechanical durability, and the thickness (thinness) that can be achieved. Depending on the applications, significant factors can also be the quality and durability of the electrical contacts and the reliability and quality of the electrical properties of the whole module. Significant properties to be examined in terms of manufacturing can also
30 be, for example, the reliability, yield, efficiency, price, and environmental friendliness of the manufacturing methods to be used. The practicability of the manufacturing method is also affected by the availability of raw materials and the ability of the method to place

different types of component in a circuit module.

All in all, the requirements set for manufacturing methods and circuit modules are thus very diverse and vary according to the application. This being the case, there is still a
 5 need in the sector to develop new circuit-module structures and manufacturing methods, which can offer new or improved properties, or combinations of properties.

One line of development has been the placing of components inside the electronics module in a bumpless form, i.e. without growing bumps of top of the contact areas of the
 10 component. Cost benefits can then be gained, as the components need no longer be transported during manufacture to a separate production plant to make the bumps.

The applicant's own patent and application publications disclose manufacturing techniques, which can also be used in connection with bump-free components. The
 15 techniques described are particularly suitable for components, in which the material of the contact areas is copper. Of the applicant's own publications, those that can be referred to as most closely relating to the invention are the international patent application publications WO 2004/089048, WO 2005/027602, WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217, and
 20 WO 2007/107630.

However, at present copper is quite little used as a conductor material in semiconductor processes. The most common conductor material is aluminium. In circuit-board manufacture, on the other hand, copper is the principal material for conductors. Copper
 25 conductors of a circuit module can be grown directly on top of aluminium contact areas, but the contact between copper and aluminium is brittle, so that a module of this kind is not optimal in applications, in which mechanical stress acts on the circuit module.

An improved possibility to use contact areas of aluminium or contact areas containing
 30 aluminium would mean that, in circuit modules and manufacturing methods, normal semiconductor circuits in a bumpless form could be used immediately after the semiconductor manufacturing processes and the passivation of the surface. As

aluminium is the conductor material most widely used in the semiconductor industry, good compatibility between the contact element of the circuit module and aluminium would also ensure that suitable semiconductor circuits would be abundantly and economically available. Attempts to develop such manufacturing methods have indeed
 5 already been made for several decades in the field of component packaging technology. In component packaging solutions of this kind, the goal has been a technique, by means of which a relatively small component package could be manufactured around a component, to which a circuit board could then be attached later. Unlike packaging technology, the goal of the manufacturing techniques of the circuit module to which the
 10 present invention relates is the ability to manufacture the entire circuit board in the same process, so as to completely eliminate the packaging stage of the separate component. Of course, this does not exclude the possibility of using the manufacturing method of the circuit module to manufacture only a component package.

15 The patent US 4 246 595, Noyori et al., discloses a method, in which the contact areas of a component are brought into contact with an insulator sheet, in which V-shaped openings have been made. First of all, a layer of titanium (Ti) or chromium (Cr) is grown on the surfaces of the openings and the aluminium contact areas. This intermediate metal layer is intended to prevent the copper from diffusing into the
 20 aluminium and the semiconductor component, as well as to improve the adhesion between the copper and the aluminium. In addition, the intermediate layer acts as an electrical conductor later during electrochemical growing (electroplating), so that the intermediate metal layer will reliably cover also the side walls of the openings. The growing of the titanium or chromium layer requires the use of the sputtering technique,
 25 for which reason the openings must also have a clear V shape. Sputtering is expensive when used on large surfaces (on circuit modules) while additionally the open V shape reduces the available conducting density. Contract structures of a corresponding type are also disclosed in patents US 4 783 695 and US 4 894 115, Eichelberger et al., and in patent US 5 353 195, Fillion et al.

30 Later, in patent US 6 396 148, Eichelberger et al., an attempt is made to solve the problems relating to sputtering, by forming the intermediate metal layer by growing a

layer of nickel on the surface of the aluminium contact areas. According to the patent, the growing of the nickel is performed by means of a chemical growing method (electroless plating). Yet another layer, which also covers the side walls of the openings made in the insulating material for the contacts, is growing on top of the nickel layer by means of a chemical growing method. In the method, the components are attached first by their side and rear surfaces to the insulator layer and, after this, a photo-patternable polymer is spread on the front surface of the component and on top of the contact areas. The polymer is patterned by exposing it to light and developing it, to form openings for the contacts.

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One possibility is to grow bumps on the surface of the conductors of the circuit-board part of the circuit module and attach the component to the conductors by a flip-chip mounting technique, for example, by ultrasound bonding. Such a method is disclosed in the applicant's own international patent application WO 2006/134220. Problems relating to both production and the quality of the contacts are associated with methods using flip-chip methods.

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Disclosure of Invention

The object of the invention is to develop a new contact-element structure envisaging the utilization of bumpless components, as well as a circuit module and manufacturing technique using such a structure.

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According to an aspect of the invention, a bumpless component is used in the circuit module, the material of the contact areas of which being of a different metal, or metal alloy to the conductors of the conductor layer of the circuit module. The contact areas of the component and the conductors of the circuit module are connected to each other with the aid of contact elements, which contain an intermediate layer, which contains a third metal or metal alloy, which differs from the material of the contact areas and conductors, on the surface of the material of the contact area. In addition, the contact surface area between the intermediate layer of each contact element and the contact area of the component is smaller than the surface area of the contact area.

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According to another aspect of the invention, a manufacturing method is created in order to manufacture the circuit module described above, in which the component is attached to a conductor foil or conductor-pattern layer with the aid of a polymer layer and contact elements are made through the polymer layer. When making the contact elements, contact holes are made in the polymer layer on top of the contact areas, at the locations of the contact areas. The contact holes are dimensioned in such a way that the contact surface area between each contact hole and the corresponding contact area is smaller than the total surface area of the contact area. After this, the contact holes are filled with a conductor material, in such a way that filling is started by coating the surface of the contact areas with an intermediate layer, for example, by using one or more chemical metal-growing methods.

Thus, a new type of circuit module and manufacturing method is obtained, which can offer some advantages in terms of the applications of some circuit modules.

In addition, the invention has numerous special embodiments, which provide additional advantages.

In one embodiment, components are used in the circuit module, the material of the contact areas of which contains aluminium and the contact elements comprise a layer containing zinc on the surface of these contact areas containing aluminium. In addition, the contact elements are manufactured in such a way that the contact surface area between the layer containing zinc and the contact area is smaller than the total surface area of the actual contact area.

A layer containing zinc has been observed to be useful in terms of the quality of the electrical contact, as coating a layer containing zinc on the surface of an aluminium contact area prevents the re-oxidation of the aluminium surface and permits the creation of good adhesion between the aluminium and the next layer. In addition, the layer containing zinc improves the mechanical durability against lateral stress of the contact formed through the interface between the aluminium and the intermediate layer of other

metal.

We have observed that extremely good mechanical durability is achieved by using a double zincate process, in which the blank containing the components is subjected to the zincate process at least twice. Thus a more even and denser layer of zinc is made to grow on top of the aluminium contact surfaces. After a single zincate treatment, there is zinc on only some areas of the contact surfaces, or else the layer is porous, therefore a double zincate process is used in the preferred embodiment.

The possibility to use contact elements that are narrower than the contact area can, for its part, provide advantages, for example, by allowing the conductors connected to the contact elements to also be made narrow, especially in embodiments, in which the contact element is essentially of even width vertically, or only narrows moderately towards the component.

In an embodiment of the manufacturing process, in which contact openings are made in the conductor foil of the conductor-pattern layer prior to attaching the component, the component can be attached aligned relative to the contact openings while, in addition, the contact holes needed for the manufacture of the contact elements can be made through these contact openings, by using the material of the conductor foil or conductor-pattern layer as a mask. In such an embodiment, an advantage is obtained in the case of the alignment between the contact elements and the contact areas. In addition, an advantage is obtained in terms of the manufacture of the contact holes, because the holes can be opened using a CO₂ laser, for example.

In an embodiment, in which the contact holes are opened using a laser, the contact holes can be opened one component or component-group at a time, and thus the first intermediate layer can be manufactured first through the contact holes, on top of the contact areas of the first components, and then later the second intermediate layer can be manufactured through the contact holes opened later, on top of the contact areas of the second components. Thus, components, the materials of the contact areas of which differ from each other and are incompatible with the growth processes of the same

intermediate layer, can be fitted in the same process.

In the embodiments, it is also possible to attach the components to the conductors by means of mutually differing polymer layers. Thus the properties of the insulation
 5 between the component and the conductor can be arranged to also be suitable for different mechanical and electrical requirements.

Brief Description of Drawings

10 Figures 1 - 8 show the intermediate stages of a circuit module when using a manufacturing method according to one embodiment.

Figure 9 shows one example of a circuit module according to one embodiment.

15 Figures 10 - 17 show the intermediate stages of a circuit module when using a manufacturing method according to a second embodiment.

Figures 18 - 23 show the intermediate stages of a circuit module when using a manufacturing method according to a third embodiment.

20 Figure 24 shows one intermediate stage of a circuit module when using a manufacturing method according to a fourth embodiment.

25 Figure 25 shows one possible example of a contact hole and its dimensions made for a contact element of a circuit module.

Figure 26 shows examples of possible contact holes.

30 Figure 27 shows some embodiments of intermediate layers manufactured in the contact hole of Figure 26.

Figure 28 shows one contact-element structure.

Figure 29 shows a second contact-element structure.

Figure 30 shows a third contact-element structure.

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Figure 31 shows a fourth contact-element structure.

Figure 32 shows a fifth contact-element structure.

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Figure 33 shows a sixth contact-element structure.

Modes for Carrying Out the Invention

15 Figures 1 - 9 show one exemplary application of the manufacturing method according to one embodiment. In this embodiment, manufacture begins from a conductor foil 12, which of metal, for example. A suitable conductor foil 12 is, for example, a copper film, the thickness of which is in the range 1 - 70 μm , typically in the range 3 - 12 μm . Instead of a bare conductor foil 12, it is also possible to use as the base material a layered sheet, which comprises a conductor foil 12 and an insulator layer 13, which is shown by a broken line in Figure 1, on the surface of this. In the embodiments described in the following, it is possible to use such a layered sheet 12, 13, in place of the conductor foil 12.

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25 Differing from what is shown in Figure 1, it is also possible to use a layered sheet, which comprises a support membrane on the second surface of the conductor foil 12. The support membrane is on the opposite surface of the conductor foil relative to the components to be attached to the conductor foil. If the layered sheet also comprises an insulator layer 13, the support membrane will then be on the opposite side of the conductor foil to the insulator membrane 13. The support membrane can be used, for example, to improve the mechanical stiffness and ease of handling at the start of the manufacturing process of the conductor foil 12, or the layered sheet 12, 13. The support membrane is, however, intended to be removed at a later stage in the process. It is also

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possible to proceed by starting manufacture from a support membrane while a conductor foil 12, which is patterned or unpatterned, is made on the surface of this. The process examples and stages described in the application example can also be performed correspondingly when using a support membrane, though this is not stated separately. In the description hereinafter, however, reference will be made to a support membrane only when calling attention to something particularly noteworthy in the case of an embodiment using a support membrane. The actual support membrane can be, for example, of an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer. The thickness of the support membrane can be, for example, 25 - 400 μm . The thickness of the support membrane is typically in the range 35 - 105 μm .

Next, contact openings 8 are made in the conductor foil 12, which are located on the conductor foil 12 in such a way that they are placed at the positions of the contact terminals of the components being placed in the module being manufactured. Thus, an individual contact opening 8 is made in the conductor foil 12 for each contact terminal of the component. In this embodiment, the contact openings 8 can be manufactured with the aid of a UV laser. The contact openings 8 can also be manufactured, for example, mechanically by drilling, milling, or etching. In an embodiment using a support membrane, the contact openings 8 are preferably made from the direction of the opposite surface, in such a way that they penetrate the conductor foil 12 completely. However, the contact openings need not penetrate the sheet, instead the method can equally well also be designed in such a way that the contact openings 8 only extend as far as the surface of the material of the support membrane, or form recesses in the material of the support membrane, without, however, passing entirely through it. Also, the contact openings need not pass entirely through the conductor foil, if a thick conductor foil is used, which is thinned by etching in a later stage.

In the embodiment of Figure 1, the contact openings 8 are manufactured in such a way that the size of a contact opening 8 is less than the contact surface area of the contact material to be placed at the opening 8. The contact opening is typically circular in shape, though other shapes too can be used. The shape and size of the contact opening 8 are

selected in such a way that the contact surface of the contact terminal can cover the contact opening 8 entirely.

5 According to Figure 2, manufacture is continued by spreading adhesive layers 5 on the surface of the conductor foil 12, in the connection areas of the components. The adhesive layers will then also cover the contact openings 8. Alternatively, the adhesive 5 can be spread on the surface of the components. The adhesive can also be spread on the surface of both the component and the conductor foil 12. Typically, the adhesive is spread locally, so that the adhesive layers 5 will be located only in the connection areas
10 of the components.

The term adhesive refers to a material, by means of which the components can be attached to the conductor foil 12 or insulator layer 13 that acts as a base. One property of the adhesive is that the adhesive can be spread on the surface to be glued in a relatively
15 fluid form, or one that otherwise conforms to the surface shapes, for example, in the form of a film. A second property of the adhesive is that, after spreading, the adhesive hardens, or can be hardened, at least partly, in such a way that the adhesive is able to hold the component in place (relative to the conductor foil 12) at least until the component is secured to the construction in some other way. A third property of the
20 adhesive is an adhesive capability, i.e. an ability to stick to the surfaces being glued.

The term gluing, for its part, refers to the attachment of pieces to be glued to each other with the aid of an adhesive. In the embodiments, the adhesive is brought between the component and the conductor foil 12 or insulator layer 13 acting as a base and the
25 component is placed in a suitable position relative to the base, in which the adhesive is in contact with the component and the base and at least partly fills the space between the component and the base. After this, the adhesive is allowed (at least partly) to harden, or the adhesive is (at least partly) actively hardened, so that the component attaches to its base with the aid of the adhesive. In some embodiments, the contact protrusions of the
30 component may protrude during gluing through the adhesive layer to come into contact with the base.

The adhesive used in the embodiments is typically an epoxy-based adhesive, for example a heat-cured epoxy adhesive. The adhesive is selected in such a way that the adhesive to be used will have sufficient adhesion to the base and the component. One preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too much from the thermal expansion of the surrounding material during the process. It would also be preferable for the adhesive selected to have a short hardening time, preferably of a few seconds at most. Within this time, it would be good for adhesive to harden at least partly, so that the adhesive can hold the component in place. Final hardening can take a clearly longer time and can even be planned to take place in connection with later process stages. In addition, the stresses caused by the later process stages, such as thermal, chemical, or mechanical stress, are taken into account when selecting the adhesive. The electrical conductivity of the adhesive will be preferably in the order of the electrical conductivity of the insulator materials.

Next, components 6 and 16, which comprise contact terminals 7 and 17, are taken. Both components 6 and 16 are semiconductor components, for example, processors, memory chips, or other microcircuits. The contact terminals of the component 6 are contact areas 7, which are located essentially on the level of the surface of the component. Such contact areas 7 of the component 6 are created at the semiconductor factory during the manufacturing process of the semiconductor component. The contact area 7 typically forms the surface of a conductor pattern on the metal used in the process. The metal used in the manufacturing process of semiconductor components is typically aluminium, though other metals, metal alloys, or other conductor materials can also be used. For example, the use of copper has become common in semiconductor-component manufacturing processes.

The contact terminals of the component 16 are contact bumps 7, which protrude from the level of the surface of the component. Such contact bumps 17 are manufactured in a bump-making process after the manufacture of the semiconductor component 16, typically in a separate factory. The contact bump 17 can contain one or more metals, metal alloys, or other conductor materials. Typically, the outer surface of the contact

bump 17, i.e. the contact surface, is made from copper or gold.

The components 6 and 16 are aligned relative to the contact openings 8, in such a way that each contact terminal 7, 17 comes next to the corresponding contact opening 8, and is pressed against the adhesive layer 5. After this, the adhesive is at least partly hardened, so as to prevent, or minimize the relative movement of the components 6, 16 and the conductor foil 12 after alignment. In alignment and gluing, the aim is to position the contact opening 8 to be in the centre of the corresponding contact terminal 7, 17.

After this, insulator sheets 11, in which openings are made for the components 6, 16, as well as a unified insulator sheet 10, which is of unhardened or pre-hardened polymer, are laminated on top of the conductor foil 12. During lamination, the insulator sheets 10, 11 are melted together and form a unified insulator layer 1 around the components 6, 16. In the embodiment of Figure 2, the insulator sheets 11 are fibre mats impregnated with polymer, or sheets containing pre-hardened polymer and reinforced with a fibre material. The polymer can be, for example, epoxy and the fibre reinforcement can be, for example, glass-fibre mat. A typical example of a suitable insulating-sheet 11 material is an FR4-type glass-fibre reinforced epoxy sheet. Other reinforcement and polymer material combinations can be used, of course. When using several insulator sheets 11, the sheets can also differ mutually.

In Figures 2 and 3, the fibre material is shown by wavy shading 19. In the figures hereinafter, the fibre material 19 is not shown, but these structures too include fibre material 19. The fibre material 19 contained in the insulator sheet 11 or the insulator sheets 11 acts as a reinforcement, which provides the electronic module being manufactured with mechanical strength. According to the example of Figure 2, holes 4 are made in the insulator sheets 11 at the locations of the components 6, 16. The insulator sheets 11 are perforated particularly to make openings for components in the fibre material 19 contained in the insulator sheets 11. Without perforation, the components would press against the fibre-material layers 19 during lamination. The unperforated insulator sheet 10, on the other hand, can be fibre-reinforced or unreinforced, depending on the embodiment.

The insulator sheets 10, 11 are typically selected in such a way that they contain enough fluid polymer for the polymer flowing in the lamination stage to be sufficient to fill the holes 4 made in the insulator sheets 11 for the component 6, 16, around the components.

5 The structure shown in Figure 3 is then obtained, in which the insulator layer 1 contains a tight polymer layer, which contains one or more reinforcements of a fibre material 19. The polymer layer is bound tightly to the fibre layer 19 while the tight polymer layer also attaches the components 6, 16 to the surfaces, so that a tight, unified, and mechanically strong insulator layer is formed, which contains the components 6, 16, and
10 which is, in addition, reinforced with fibre material 19.

In the example of Figure 2, a unified insulator sheet 10 is used, though the insulator sheet 10 can also be omitted from the structure. In that case, the insulator sheet 11 or insulator sheets 11 are selected in such a way that they themselves already contain
15 sufficient fluid polymer to fill the holes 4 in the insulator sheets 11 around the components 6, 16. However, it is typically easier to ensure the filling of the holes 4 by using a separate insulator sheet 10.

A conductor foil 14, which is preferably of a material that is similar to, and equally as
20 thick as the conductor foil 12, is also laminated with the insulator sheets 10, 11 into a single structure. Thus, the insulator layer 1 and the components 6, 16 remains between the corresponding conductor foils 12 and 14. Figure 3 shows this intermediate stage of the module manufacture. In the intermediate stage of Figure 3, there is adhesive on the contact surface of the contact terminals 7, 17 and typically also in the contact openings
25 18. In the stage shown in Figure 4, this adhesive is removed and contact holes 18, which extend to the contact surfaces of the contact terminals 7, 17 are formed at the positions of the contact openings 8.

With reference to Figure 3, it can be further stated that the structure can also be
30 manufactured in such a way that a unified layer of fibre material 19 runs between the components 6, 16 and the conductor foil 14. Such a construction can be used when the thickness of the components 6, 16 is sufficiently less than the thickness of the insulator

layer 1. The structure can be manufactured, for example, in such a way that a unified insulator sheet 10, which contains the fibre material 19 of the layer, can be laminated onto the structure.

5 If a support membrane is used in the embodiment on the surface of the conductor foil 12, as depicted in connection with the description of Figure 1, it is most suitable to remove the support membrane after the lamination, i.e. between the intermediate stages shown in Figures 3 and 4.

10 After lamination and the removal of the possible support layer, the adhesive layer, which has been created in the contact openings 8 and between the contact openings 8 and the contact terminals 7, 17, is removed. In the embodiment of the figures, the removal of the adhesive is implemented by the laser-ablation method, using a CO₂ laser. The ability of a CO₂ laser to vaporize organic insulating substances, such as epoxy-base adhesive, is
 15 good, but its ability to vaporize copper or other metals is poor, so that the conductor foil 12 can be used as mask for making the contact holes 18. Thus, it is possible to manufacture contact holes 18, the diameter of which is less than the diameter of the beam of the CO₂ laser. This property creates a significant advantage, as the minimum diameter of the beam of a CO₂ laser is typically in the order of 75 µm, which is too large
 20 when considering the manufacture of precise electronic module structures. A UV laser, on the other hand, can typically be used to manufacture clearly more precise structures. The minimum diameter of the beam of a UV laser can be, for example 25 µm, but a UV laser is not, on the other hand, suitable for removing adhesive from the contact openings 8 and from between the contact openings 8 and the contact terminals 7, 17.

25 Thus, the use of a conductor mask permits the manufacture of very precisely limited and precisely positioned contact holes 18 in an insulator material, such as the adhesive 5 using in the embodiment. In addition, the use of a CO₂ laser permits the cleaning of the contact surfaces of the contact terminals 7, 17 in the same process stage, without any
 30 significant danger of destroying or damaging the contact terminals 7, 17. In the embodiment, the conductor foil 12 is of copper while the contact terminals 7, 17 of the component are also of metal, so that they are not sensitive to the beam of the CO₂ laser,

so that the process can be designed in such a way that the contact surfaces of the contact terminals 7, 17 will be sure to be cleaned sufficiently well. Thus, the advantage of the method described is that contact openings 8 can be made in the conductor foil 12 very precisely with the aid of a UV laser and, after this, the contact openings can be used as a mask for the making of the contact holes 18 by means of a CO₂ laser that is less precise, but safer for the structure.

If the contact holes 8 of the conductor foil 12 were to be manufactured only in this process stage, the method used for machining the metal of the conductor foil 12, for example, a UV laser, would more easily damage also the contact terminals 7, 17, because the energy required to penetrate the conductor foil 12 is significantly greater than the energy required to penetrate the adhesive or other insulation between the contact terminals 7, 17 and the conductor foil 12. In such a manufacturing method, it would be challenging to stop the drilling at precisely the correct depth. In addition, aligning the drilling would be more difficult, due to the deformations arising during lamination and for the reason that the contact terminals 7, 17 of the components cannot be seen through the solid metal film. The use of contact holes 8 pre-manufactured in the conductor foil 12 provides significant advantages, both in the alignment of the components 7, 17 and in the manufacture of the contact holes 18.

In Figure 5, an intermediate layer 2, which is of a suitable conductor material, is made in the contact holes 18. The intermediate layer 2 is manufactured using a suitable chemical conductor-material growing method (electroless plating). The intermediate layer 2 can also consist of a layer of two or more different materials, which are manufactured correspondingly using two or more methods. One purpose of the intermediate layer 2 is to form a conductor membrane for the side walls of the contact holes 18, which connects the contact terminals 7, 17 and the conductor foil 12 to each other. A second purpose of the intermediate layer 2 is to provide a material adapter between the material of the of the contact terminals 7, 17 and the conductor-pattern material to be connected to them. Such a material adapter can be required, for example, in order to ensure the quality of the mechanical or electrical contact and durability, for example, when the material of the conductor-pattern layers of the circuit module is copper and the material of the contact

terminals 7, 17 is something other than copper (Cu), for example aluminium (Al).

When manufacturing the intermediate layer 2, a suitable chemical growing method is used, because by means of such a method the conductor material can also be grown on the vertical surfaces of the contact holes 18, unlike when using sputtering, for example. An electrochemical method (electroplating) cannot be used in this stage, because the side walls of the contact holes 18 are not conducting. Alternatively, V-shaped-opening contact holes can be used and the intermediate layer 2 made by sputtering. Sputterable materials suitable for this purpose are, for example, titanium-wolfram (TiW) and chromium (Cr). A layer of nickel (Ni) and gold (Au) can also be grown on top of the TiW or Cr layer. In the example of Figure 5, nickel grown by a chemical method is used as the intermediate layer 2 in the example of Figure 5, however, so that the intermediate layer 2 will grow at the same time also on the surfaces of the conductor foils 12 and 14. Another example of the intermediate layer 2 is a layer containing zinc, manufactured on the surface of the contact terminals 7, 17, on top of which a layer of nickel (Ni) can further be manufactured. More alternatives that are possible are depicted in connection with the description of Figures 26 - 33.

In this embodiment, after the manufacture of the intermediate layer 2, manufacture is continued by spreading resist layers 3, typically photoresist layers, on both surfaces of the module. The resist layers 3 are patterned with the aid of a conductor-pattern mask by exposure and development, in such a way that the resist 3 is removed from the desired parts of the conductor patterns of the conductor-pattern layers. This intermediate stage is shown in Figure 6. After this, the module is taken to an electrochemical bath and voltage is led to the intermediate layers 2 of the module. The desired conductors of the conductor-pattern layer are then grown in the openings of the resist layers 3. The conductor material also grows in the contact holes 18, forming a conductor core to the contact elements, as can be seen from Figure 7. In the example of Figure 7, the conductors 22, 24 are electrochemically grown copper. Finally, thin etching-mask layers are grown on the surface of the conductors 22, 24. A layer of tin (Sn), for example, can act as the etching mask.

- Next, the resist layers 3 are removed, when, in the embodiment of the figures, the intermediate layer 2 is revealed from under the removed resist. The revealed part of the intermediate layer 2 is removed, for example, by etching, the same procedure being use for the parts of the conductor foils 12 and 14 revealed outer the conductors 22 and 24.
- 5 The etching-mask layer then protects the outermost surfaces of the conductors 22 and 24 from the effects of the etching. An electronic module, which contains two components 6 and 16 connected electrically to conductors 22, comprising two conductor-pattern layers (conductors 22 and 24), and shown in Figure 8, is then obtained.
- 10 In the example of Figures 6 and 7, the conductors 22 and 24 are grown directly into their correct shape in the openings made in the resist layer 3. However, the conductors 22 and 24 can also be manufactured in another way, both in this example and in the examples described hereinafter. One alternative way of manufacture is to grow a unified layer of conductor material over the surfaces of the entire module blank and to pattern the
- 15 conductor layer later by means of a lithography method, in order to form the conductors 22 and 24. Described in greater detail, it is possible to proceed, for example, in such a way that, continuing from the intermediate stage of Figure 5, copper is grown on the surfaces of both intermediate layers 2 by means of an electrochemical method. In that case, the contact holes 18 too are filled with copper. After this, resist layers are spread
- 20 on top of the copper layers, the resists are patterned, and the excess parts of copper, or the intermediate layer 2 and the conductor foils 12 and 14 are etched. After this, the resist mask is removed. Using either manufacturing method, the result is the structure shown in Figure 8.
- 25 Figure 8 can show an already finished simple circuit module, but manufacture is usually continued by manufacturing additional insulator and conductor layers on the surfaces of the circuit module, which are connected electrically with the aid of vias to the structure shown in Figure 8. In addition, it should be noted that vias can be manufactured in the module too of Figure 8, which connect the conductors 22 to the conductors 24. Such vias
- 30 can be manufactured in a corresponding manner to, and in the same process stages as described above in the manufacture of the contact elements.

The module of Figure 8 can be further refined in the manner shown in Figure 9, in such a way that the surfaces of the module are protect by protecting layers 20. In addition, in the example of Figure 9, external contact elements, which comprise bases 21 made on top of the conductor patterns 22, 24 and contact balls 23 made on their surfaces, are manufactured in the module.

Figures 10 - 16 show a manufacturing method according to a second embodiment, up to a stage corresponding to the intermediate stage shown in Figure 5. Manufacture can be continued from the intermediate stage of Figure 16, for example, as shown by Figures 6 - 9, or suitably also in an alternative manner, in which the material of the conductors 22 and 24 is first of all grown over the entire surface and after that patterned to form conductors 22 and 24. The technical features and parameters presented in connection with the description of Figures 1 - 5 can also be applied in the process stages shown in Figures 10 - 16, so that there is no need to repeat all the details of the manufacturing process and their advantages in the following embodiment. On the other hand, the essential differences between the embodiments shown by Figures 1 - 9 and Figures 10 - 16 are brought out in the following.

In the embodiment of Figures 10 - 16, manufacture starts, as in Figure 1, from a conductor foil 12, in which contact openings 8 are made. After this, a spacer 15 is attached to the future attachment point of the component 6 on the surface of the conductor foil 12. The spacer 15 is of a suitable insulating material, for example, of pre-hardened adhesive or some other polymer, which has sufficient adhesion with the surface of the conductor foil 12. The spacer 15 can also be of hardened polymer, in which case it can be attached to the surface of the conductor foil 12, for example with the aid of separate adhesive.

A spacer 15 can be used for many different reasons. One use of a spacer is to increase the insulating thickness between the component 6 and the conductor foil 12. The need to increase the insulating thickness can be imposed, for example, by the requirements set by the electrical operation of the circuit module or the component 6. In that case, with the aid of the spacer 15 it is possible to set the properties of the insulation between the

component 6 and the conductor foil 12 as desired. The properties selected can be, for example, a desired specific resistance and spark-over resistance, which can be influenced by the selection of the material of the spacer 15 and the adhesive 5. The spacer can also be used to prevent a short-circuit between the component and the conductor foil 12. Such a use will come into question especially in embodiments in which the surface of the component 6 is pressed very close to the conductor foil, when a risk arises of unintended electrical contacts being formed between the conductor structures on the surface of the component and the conductor foil. A spacer can also be used to weaken the capacitive connection between the internal circuit elements of the component 6 and conductors 22 running next to the location of the component 6.

In addition to, or instead of a spacer 15, it is possible to use for the same purpose an insulator layer 13 entirely covering the surface of the conductor foil 12, as described in connection with Figure 1.

In the examples of Figures 10 - 16, a spacer 15 is used in connection with a bumpless component 6, but the contact terminals of a component 16 with bumps must be made to extend closer to the surface of the conductor foil 12, so that a sufficient insulating gap can be ensured between the opposite surface of the component 16 and the conductor foil 14. In the embodiment, spacers 15 selected component-specifically can be placed in the circuit module, in order to optimize the electrical and/or mechanical properties of the circuit-board module. The same module can thus also contain different kinds of spacers 15 and thus spacers 15 can also be used in series production, in order to make components 6, 16 coming from different sources and with different properties to each other compatible with the circuit-board manufacturing process being used. One example of a mechanical property requiring optimization is the thickness of the insulator layer 1 (and at the same time of the entire module), which can be reduced with the aid of suitable selected spacers 15, which can be seen, for example, in Figure 12.

According to Figure 11, manufacture is continued by spreading adhesive layers 5 on the surfaces of the conductor foil 12 and the spacer 15 in the connection areas of the components. The components 6 and 16 are aligned relative to the contact openings 8 and

glued in place. After that, in the example of Figure 11, insulator sheets 10, 11 and a conductor foil 14 are laminated on top of the conductor foil 12. Next, photo-resist layers 30, which are patterned in such a way that openings larger than the contact openings 8 are created at the positions of the contact openings 8, are spread on the surface of the conductor foils 12 and 14, or a coating is made electrophoretically on top of the entire conductor layer. This photo-resist layer 30 is used to limit the growth of an intermediate-layer material grown using a non-selective method to the contact holes and the immediate surroundings of the contact openings 8. Such a procedure can also be used in connection with the example described above, nor, on the other hand, is it essential in the examples of Figures 10 - 16. Figure 12 shows the module after these stages. The contact terminals 7 of the component 6 are covered by both a spacer 15 and adhesive 5. There is adhesive on the surface of the contact bumps 17 of the component 16 and in the corresponding contact openings 8.

In the stage shown in Figure 13, contact holes 18 are made at the positions of the contact openings 8 of the component 6. The contact holes are opened through the spacer 15 and the adhesive layer 5, as far as the contact surfaces of the contact terminals 7. In the embodiment of the figure, the opening of the contact holes 8 is implemented by the laser-ablation method, using a CO₂ laser, as described in connection with Figure 4. In the embodiment of Figures 10 - 16, the important fact is that contact holes are not opened at this stage of the position of the contact terminals 17 of the second component 16.

In the stage shown in Figure 14, an intermediate layer 2, which is of a suitable material, is made in the contact holes 18 of the component 6. The conductor material of the intermediate layer 2 is selected on the basis of the material of the contact terminals 7 of the component 6 and manufactured using a suitable chemical conductor-material growing method. In the example of the figure, the material of the contact terminals 7 of the component is aluminium and the material of the intermediate layer 2 is mainly a metal alloy containing zinc. The principles described in connection with Figure 5 above are applied to the growing of the intermediate layer. Unlike the example of Figure 5, in the case of Figure 14, it is, however, also possible to proceed in such a way that in this

stage the intermediate layer 2 is grown with the aid of a selective method only on the surface of the contact terminals 7, i.e. on the bottom of the contact holes 18 and not on the edges of the contact holes 18. In this embodiment, the intermediate layer 2 coming on the edges of the contact holes 18 is grown later in connection with the growing of the intermediate layer relating to the contact bumps 17 of the component 16. The embodiment using a selective growing method has the advantage that the intermediate layer 2 does not grow on top of the adhesive layer covering the contact bumps 17 of the component 16.

Manufacture is continued in the stage shown in Figure 15 by manufacturing contact holes 28 at the positions of the contact openings 8 of the second component 16. After this, the module according to Figure 16 is subjected to a suitable chemical conductor-material growing method. In the example of Figure 15, the growing method is non-selective and the conductor material grows on all the free surfaces of the module and thus also in the contact holes 18 of component 6 and in the contact holes 28 of component 16. However, the photo-resist layer 30 protects the surfaces of the module, so that the intermediate layer 2 grows only in the contact holes 18 and 28 and in their surroundings. After this, the photo-resist and the conductor material that may have grown on its surface is removed. Such an embodiment using a photo-resist layer 30 can be useful, for example, when nickel or some other metal differing from copper is grown in the openings of the photo-resist layer, for example, using a non-selective method. The conductors 22 and 24 can then be manufactured to consist of solely a copper layer.

In other embodiments, suitably selected selective growing methods can also be used and the conductor material is grown only on the surfaces of the contact bumps 17 of the component 16, correspondingly as described above in connection with Figure 14. In any case, at this stage the intermediate layer 2 is grown at least on the surfaces of the contact bumps 17 of the component 16 and on the surfaces of the side walls of the contact holes 28 and, in addition, if desired also on the surface of the intermediate layer 2 connected to the contact terminals 17 of the component 6 and/or on the surfaces of the side walls of the contact holes 18 of the component 6.

If the example of Figures 10 - 16 were to be implemented without the use of a photo-resist 30, in the example of Figure 16 the material of the surface of the contact bumps 17 of the component 16 could suitably also be copper and the material of intermediate layer 2 to be grown of the surface of the contact bumps 17 would then be copper manufactured suitably using a chemical growing method.

After the manufacture of the intermediate layer 2, in this embodiment manufacture can be continued, for example, in the manner stated in connection with the description of Figures 6 - 9, by manufacturing conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28.

Another alternative is to coat copper on both conducting surfaces of the module, after the removal of the photo-resist layer 30. After this, the copper layers can be patterned to form conductors 22 and 24, when the structure shown in Figure 17 will be obtained, in which the conductors 22 and 24 are formed of the first and second copper layers in the surroundings of the contact elements, as well as of an intermediate layer 2, which is of nickel for example, between them. Elsewhere, the conductors 22 and 24 are formed of a first and second copper layer, between which is the interface to be analysed. Once the structure of Figure 17 has been manufactured, it is possible, if desired, to continue in some manner described in connection with any of the previous examples.

Figure 18 - 23 show a manufacturing method according to a third embodiment, which is a variation of the embodiment shown in Figures 10 - 16. From the intermediate stage of Figure 23, manufacture can be continued, for example, in the manner shown in Figures 6 - 9. The technical features and parameters presented in connection with the description of Figures 1 - 5 and 10 - 16 can thus also be applied in the process stages shown in Figures 18 - 23, so that all the details and their advantages of the manufacturing process need not be unnecessarily repeated in the following embodiment. However, in the following the essential difference between the embodiments shown in Figures 10 - 16 and Figures 18 - 23 is presented.

In the embodiment of Figures 18 - 23, manufacture is commenced, as in the case of

Figure 10, from a conductor foil 12, in which contact openings 8 are made. After this, spacers 15 are attached to the surface of the conductor foil 12, to the future attachment points of the components 6 and 26. The spacers 15 of the components 6 and 26 can be mutually identical or selected component specifically, for example, in such a way that the spacer 15 of the component 6 is of a different material and/or thickness to the spacer 15 of the component 26.

According to Figure 18, manufacture is continued by spreading adhesive layers 5 on the connection areas of the components and by laminating insulator sheets 10, 11 and a conductor foil 14 to the blank, exactly as described in connection with Figure 11. Figure 19 show the module after these stages.

In the stage shown in Figure 19, contact holes 18 are made at the positions of the contact openings 8 of the component 6, as described in connection with Figure 13. At this stage, contact holes are not yet opened at the positions of the contact terminals 27 of the component 26.

The stage shown in Figure 21 corresponds completely to the method stage described in connection with Figure 14. In this embodiment, an intermediate layer 2, which is of two layers, is manufactured in the contact holes 18 of the component 6. In the example of the figure, the material of the contact terminals 7 of the component is aluminium. The two-layer intermediate layer 2 of the example comprises first a grown layer containing zinc and after this a grown nickel-aluminium layer. The nickel-aluminium layer is grown by means of a chemical method and is used to seal the layer containing zinc.

Manufacture is continued in the stage shown in Figure 22, by making contact holes 28 at the positions of the contact openings 8 of the second component 26. After this, according to Figure 23 the module is subjected to a suitable chemical conductor-material growing method. This stage corresponds to the method stage described in connection with Figure 16. In the example of Figure 23, the material of the surface of the contact terminals 27 of the component 26 is copper and the material of the intermediate layer 2 grown of the surface of the contact terminals is also copper.

Figure 24, for its part, shows a modification of the embodiment of Figures 18 - 23, in which, after the stage shown by Figure 22, a first intermediate layer is grown on top of the contact terminals 27 of the component 26, by means of a selective growing method and, after his, the growing of the intermediate layer 2 is continued using a non-selective method. In the example of Figure 24, the material on the surface of the contact terminals 27 of the component 26 is gold and the material of the intermediate layer 2 grown on the surface of the contact terminals 27 is nickel.

10 In the embodiments of these Figures 18 - 24, after the manufacture of the intermediate layers 2 it is possible to continue, for example, by making conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28, for example, by means of the manner stated in connection with the description of Figures 6 - 9.

15 Figure 25 shows in greater detail the shape of the contact hole and correspondingly also the shape of the contact element to be manufactured in this opening. The example of Figure 25 shows one possible shape, which can be achieved when using the embodiments described above. The shape can be affected with the aid of the shape of the contact openings 8 to be made in the conductor foil 12, the properties of the insulation between the conductor foil 12 and the component, and the operating parameters of the CO₂ laser. The contact hole of Figure 25 is rotationally symmetrical and the cross-section shown in the figure is taken through the central axis of the contact hole, i.e. it shows the widest possible cross-section. In Figure 25, the size and shape of the contact hole are determined with the aid of the following parameters:

- greatest width W_{MAX} , from which the greatest cross-sectional area A_{MAX} can be calculated,
- 30 - the width W_{CONT} of the contact between the contact element and the contact surface 7 of the component 6, from which the contact surface-area $A_{CONT 1}$ between the contact element and the contact surface of the component can be calculated, and

- the width W_{HOLE} of the contact opening, from which the contact surface-area $A_{CONT\ 2}$ between the contact element and the conductor of the conductor-pattern layer can be calculated.

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The figure also shows the width W_{PAD} of the contact surface of the component, from which the surface area A_{PAD} of the contact surface can be calculated, if the shape of the contact surface is known. The contact surface 7 can be, for example, square in shape and, when W_{PAD} represents the width of a side, the surface area of the contact surface is obtained as: $A_{PAD} = W_{PAD} \times W_{PAD}$. Of course, the surface areas can also be determined with the aid of surface-area measurement, which can be more practical if the surface area to be determined is of an irregular shape.

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In the figure, the contact surface 7 is surrounded by a passivation layer 9 made on the surface of the component 6. In that case, the surface area A_{PAD} refers precisely to the surface area free to form a contact, i.e. the surface area of the surface that is revealed in the opening made in the passivation layer 9. In addition, the figure shows the distance H of the distance between the conductor foil 12 and the contact surface 7, which corresponds to the depth of the contact hole and is thus the height of the contact element to be made in the contact hole. Because the contact hole is filled entirely with conductor material, the other dimensions too of the contact hole correspond to the dimensions of the contact element and the parameters W_{MAX} and W_{HOLE} can also be used to refer to the corresponding dimensions of the contact element.

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The following presents some typical parameters in connection with the embodiments described above:

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$H = 1 - 50\ \mu\text{m}$, usually $5 - 30\ \mu\text{m}$;

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$W_{PAD} = 20 - 1000\ \mu\text{m}$, usually $50 - 200\ \mu\text{m}$, and most usually about $100\ \mu\text{m}$; and

$W_{HOLE} = 5 - 500\ \mu\text{m}$, usually $20 - 75\ \mu\text{m}$, and most usually about $30 - 50\ \mu\text{m}$.

In addition, generally $W_{HOLE} \geq H$, which represents the reliable filling of the contact hole. The contact hole 18 is intended to be manufactured in such a way that the side walls of the hole would be vertical. In other words, the goal is a contact hole, the width and shape of which remains constant over the whole distance H between the conductor foil 12 and the contact surface 7, i.e. the contact hole would have the shape of the contact opening 8 over all of this distance. A shape that narrows towards the contact surface 7 is also good. In practice, when using the laser process described above the contact hole can, however, become widening towards the contact surface 7, or first widening and then narrowing, so that the contact hole is widest somewhere between the conductor foil 12 and the contact surface 7. Figure 25 shows a contact hole of this kind. Such a non-optimal shape is not problematic, provided the widening is not too great and the filling of the hole succeeds well.

Of the dimension values of the widths referred to above, the width W_{PAD} of the contact surface 7 of the component is determined through the selection of the component. If necessary, W_{PAD} can be measured separately from each straight line that runs through the centre point of the contact surface 7. This definition may be required when examining the dimension values referred to above and their ratios, if the shape of the contact surface 7 or of the contact opening 8 is irregular. In the most usual cases, the contact surface is, however, square, in which case the width of the side of the square can generally be used as the width W_{PAD} of the contact surface 7.

The width W_{HOLE} of the contact opening 8 is a parameter, which is selected when planning the manufacturing process. One parameter to be taken into account when selecting the width of the contact opening 8 is the width of the contact surface 7 of the component being used. The width of the contact opening 8 is selected in such a way that the contact hole to be made through the contact opening will meet the contact area 7 of the component over its entire cross-sectional area at the component end, and will not miss the contact area, for example, on the surface of the passivation layer. If the contact opening is circular in shape, with width W_{HOLE} of the contact opening is the diameter measured through the centre point of the circle. If, on the other hand, the contact opening

is irregular I shape, W_{HOLE} can, if necessary, be measured separately along each straight line that runs through the centre point of the contact opening 8. In the case of an irregular shape, when comparing the width W_{HOLE} of the contact opening with the width W_{PAD} of the contact surface, the comparison can always be made separately for each pair
 5 of widths measured through parallel straight lines. If necessary, the widths W_{HOLE} and W_{PAD} can also be compared in a corresponding manner to the other parameters described.

The ratios of the parameters described above can also be applied in connection with the
 10 contact bumps 17, in which case the surface area and width of the contact area will be replaced by the surface area and width of the contact bump and the distance H will be measured to the surface of the contact bump.

The shape of the contact hole can be influenced with the air of the laser parameters,
 15 which are selected according to the hole parameters and the properties of the insulation to be removed. The manufacturing result is, of course, also affected by the laser device being used. The suitability of the selected parameters for the process is indeed examined with the aid of a pilot manufacturing batch and, if necessary, the parameters are altered so that the desired result will be achieved.

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In general, it is sensible in the manufacturing method to try to achieve a contact-hole shape, in which

$W_{CONT} = 0.5 - 1.5$ times W_{HOLE} , preferably $0.7 - 1.2$ times W_{HOLE} , and most preferably 0.8
 25 $- 1.0$ times W_{HOLE} , however, in such a way that $W_{CONT} < W_{PAD}$; and

$W_{MAX} =$ at most $100 \mu\text{m}$, preferably at most $30 \mu\text{m}$, and most preferably at most $10 \mu\text{m}$ larger than whichever of the parameters W_{HOLE} and W_{CONT} is greater. Presented relatively, the objective would be for $W_{MAX} =$ at most 40% , preferably at most 20% , and
 30 most preferably at most 10% greater than whichever of the parameters W_{HOLE} and W_{CONT} is greater.

In the most optimal shape of a contact element, W_{MAX} is essentially as large as W_{HOLE} and, in addition, W_{CONT} is 0 - 20 % smaller than W_{MAX} .

5 In the most typical embodiments, the contact surface 7 has a square shape and the contact opening 8 is circular in shape. In that case, $A_{CONT\ 1}$ is typically 10 - 75 % of the surface area A_{PAD} . $A_{CONT\ 1}$ and $A_{CONT\ 2}$ are typically mutually approximately of equal size, for example, with an accuracy of ± 20 %.

10 Figure 26 shows examples of other possible shapes of the contact holes 18. Figure 27, for its part, shows examples of intermediate layers 2 manufactured in such contact holes. In the examples of Figures 26 and 27, the component to be attached is bumpless. As can be seen from Figure 27, the intermediate layers 2 do not extend at all on top of the passivation layer 9 of the component, but instead are in contact only with the contact surface 7 of the component. With the aid of this feature, it is possible to see even from
15 the finished electronic module whether the component embedded in the electronic module has bumps or is bumpless. The bumps grown on the contact surface 7 of the component in the bump-creation processes always fill the entire contact surface 7 and always also spread slightly on top of the passivation layer 9. If, on the other hand, bumpless components are used in the embodiments described above, the intermediate
20 layer 2 and the contact element grow only into the contact hole 18, when in the finished electronic module the intermediate layer 2 will not extend on top of the component's passivation layer 9 and part of the contact surface 7 of the component will always remain free of the intermediate layer 2 (the edges of the contact surface 7) when the alignment and manufacture of the contact hole 8 have succeeded. Also in a possible
25 contact-hole 18 alignment-error situation, in which the contact opening 8 is not completely aligned with the contact surface 7, at least part of the edge areas of the contact surface 7 and of the passivation layer surrounding the edge area will be free of the intermediate layer 2.

30 If a bumpless component is manufactured by a semiconductor process using copper conductors, the contact area 7 is copper. In that case, the intermediate layer can be manufactured directly from chemically grown copper, which forms a conductor

surfacing also on the side walls of the contact hole 18. After this, the contact holes 18 can be filled and the thickness of the conductor layer increased using an electrochemical copper-growing method.

5 At the moment of writing of the present application, the most commonly used conductor material in semiconductor processes is, however, aluminium. Thus, the most common material of the contact area 7 of bumpless components too is aluminium and it is preferable to use an intermediate layer, with one or more layers manufactured from different materials, between the aluminium contact area and the copper conductors of the
10 electronics module. In the following, reference is made to a few possible intermediate-layer constructions:

Intermediate-layer construction 1

15 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the side walls of the contact hole 18. A layer of nickel, which does not grow at all or only poorly on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical
20 method on the surface of the nickel. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 2

25 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of copper is grown by a chemical method on the surface of the layer containing zinc. The copper grown by a chemical
30 growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 3

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of nickel-aluminium, which does not grow on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical method on the surface of the nickel-aluminium. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 4

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. A layer of nickel-aluminium is grown by a chemical method on the surface of the layer containing zinc. A layer of nickel is grown by a chemical method on the surface of the nickel-aluminium and a layer of copper is grown by a chemical method on the surface of the nickel.

Intermediate-layer construction 5

First of all, a layer containing zinc is grown on the surface of the aluminium contact layer 7. A layer of nickel is grown by a chemical method on the surface of the layer containing zinc.

Intermediate-layer construction 6

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, which grown nickel layer alone forms the intermediate layer 2.

Intermediate-layer construction 7

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, and a layer of copper is grown by a chemical method on the surface of the nickel.

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In the above examples of intermediate-layer constructions, the layer containing zinc contains, for example, about 80 % zinc, about 16 % copper, about 2 - 3 % nickel, and about 2 - 3 % iron. This is only one possible example of alloy ratios suitable for the application, so that the alloy ratios can, of course, vary according to the applications. In the above examples of intermediate constructions, the thickness of the layer containing zinc is less than 1 μm , usually as a single layer about 0.1 μm and as several layers, for example 0.3 - 0.4 μm . At its thinnest, the layer containing zinc can be about 5 - 10 nm after manufacture. When growing a layer containing nickel or nickel-aluminium on top of the layer containing zinc, at least some of the zinc atoms dissolve and are replaced with nickel atoms. In the finished circuit module, it can be possible for the layer containing zinc to be observable as mainly a concentration profile of zinc in the interface between the aluminium and the material of the next layer. The layer containing zinc need not necessarily be precisely limited in the final product, because the zinc can diffuse to the adjacent material layers, particularly in stages of the manufacturing process using higher temperatures.

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In one preferred embodiment, the layer containing zinc is grown by a double zincate process. With a single zincate process, the zinc forms a non-uniform and uneven surface on top of the aluminium. The adhesion of a nickel layer grown on top of such a surface is weaker and is less suitable for use with small micro-via openings. The quality of the grown zinc surface can be significantly improved by using a double zincate process. Typically, in such a process, after the first zincate treatment, the layer containing zinc is stripped using nitric acid (HNO_3), after which a second layer containing zinc is coated. By means of the double zincate process, a tight and uniform layer containing zinc is obtained on the surface of the component's aluminium junction interface.

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The thickness of the nickel-aluminium layer, for its part, can be, for example, 0.2 - 2

μm. The thickness of the nickel layer, on the other hand, can be, for example 0.5 - 20 μm, typically 2 - 10 μm. The layer thicknesses too are only examples of the possible layer thicknesses and other layer thicknesses can also be used.

- 5 In the embodiments, the electrochemically grown copper layer can have a thickness of, for example, 5 - 30 μm, typically 10 - 20 μm. The copper layer grown by a chemical growing method, for its part, is generally manufactured to be clearly thinner, and its thickness in the embodiments is, for example, 0.1 - 2 μm, typically 200 - 800 nm.
- 10 In the manufacturing methods described above, it is, of course, also possible to use intermediate-layer constructions and materials, for example tin, other than those referred to above. It is also possible to grow a nickel layer directly on the surface of the aluminium, for example, by alkali etching and flushing the surface after this with propan-2-ol and immediately after this coating with propan-2-ol at boiling point in a
- 15 warm chemical nickel bath. In addition, the surface of the layer containing zinc could also be coated with chromium and gold on the surface of the nickel.

Figure 28 shows yet another possible contact structure, in which it is possible to use components, the contact area of which is pre-equipped with base-metallurgical layers, though bumps as such are not made. Figure 29 shows one possible corresponding contact structure, implemented with a bumpless component.

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Figure 28 shows a passivation layer 9 on the surface of the component, in which there is an opening at the position of the contact area 7 of the component. There is a polymer layer 25 of the surface of the passivation layer 9. The polymer layer 25 can consist of one or more polymer layers. The material of the polymer layer 25 can contain, for example, an insulator layer 13 depicted in connection with Figure 1, adhesive 5 depicted in connection with Figure 2, and/or a spacer depicted in connection with Figure 11. The base metallurgy, which in this case comprises two layers, is made on the surface of the contact area 7 of the component. The first base-metallurgy layer 26 is a layer of, for example, chromium (Cr) or titanium-wolfram (TiW) manufactured by sputtering. The second base-metallurgy layer 27 is a layer of, for example, nickel (Ni), copper (Cu), or

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gold (Au), manufactured by sputtering. The actual bump comprises further a gold or copper layer, for example, grown chemically or electrochemically, on the surface of the second base-metallurgy layer 27.

5 In the example of Figure 28, the component is attached by a polymer layer 25 to a conductor foil 12, in which contact openings 8 have been made as depicted in the methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the second base-metallurgy layer 27, are made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is
10 made using one or more chemical growing methods, in a corresponding manner to that depicted in the methods described above. In the example of Figure 28, the intermediate layer 2 is of copper grown using a chemical growing method. On top of this intermediate layer a layer 32 of copper is grown using an electrochemical growing method. The electrochemically grown copper also forms the conductor core 29 of the contact element.
15 It can be seen from Figure 28 that the conductor foil 12, the intermediate layer 2, and the copper layer 32 together form the material of the conductor 22. In the example, the conductor foil 12, the intermediate layer 2, and the copper layer 32 are all of copper, but the layers and the interfaces between them, can, however, also be detected by analysing the finished structure.

20 Like Figure 28, Figure 29 shows a passivation layer 9, in which there is an openings at the position of the contact area 7 of the component, on the surface of the component. On the surface of the passivation layer 9 is a polymer layer 25, which corresponds to that shown in connection with Figure 28. In the example of Figure 29, the surface of the
25 contact area 7 of the component has been a uncoated component when it was brought to the circuit-module manufacturing process. In such a component, the outer surface of the contact area 7, i.e. the contact surface, is thus typically formed already at the semiconductor factory. In the example of Figure 29, the material of the contact area 7 is aluminium.

30 In the example of Figure 29, the component is attached by a polymer layer 25 to the conductor foil 12, in which contact openings 8 are made in the manner depicted in the

methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the contact area 7, have been made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is made using one or more chemical growing methods, in a corresponding manner to that described above. In the example of Figure 29, the intermediate layer 2 is made in several parts and comprises several layers. In Figure 28, the intermediate layer is, in addition, to facilitate the description, divided into three parts, a base part 36, a wall part 37, and a conductor part 38. The base part 36 is the part that grows on the surface of the contact terminal 7, 17 to the bottom of the contact hole 18, 28, the wall part 37 is the part that grows on the surfaces of the side walls of the contact hole 18, 28, and the conductor part 38 is the part that grows to form part of the conductor 22 being manufactured.

The intermediate layer 2 of Figure 29 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. In the example of Figure 29, the conductor foil 12 is of copper, so that when using a zincate process the first intermediate layer 33 grows only on the base part 36 of the intermediate layer 2. From this, manufacture can be continued, for example, by using a chemical nickel-growing method to make the second intermediate layer 34. The nickel grows on both the base part 36 and the conductor part 38 of the intermediate layer and, when using some growing methods, on the wall part 37 too on the surface of the polymer 25. The third intermediate layer 35 is made from copper on top of the second intermediate layer 34 using a chemical growing method, so that the copper grows on the base part 36, the wall part 37, and the conductor part 38. A layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element.

In the case of Figure 29, it should be noted that, in the finished circuit module, the layers 33 and 34 do not have precise boundaries as shown in the figure, but instead the layers can appear as overlapping or mixed, for example, from the effect of diffusion. For example, in the case of the first intermediate layer 33 containing zinc, the zinc can be located as a concentration profile in the interface between the aluminium and nickel 34

and partly inside the aluminium 7 and the nickel layer 34.

In the contact structure of Figure 29, other material combinations can also be used. For example, suitably selected intermediate-layer structures from the intermediate-layer constructions 1 - 7 described above can be used to form the contact structure depicted by Figure 29 and also the contact structures depicted by Figures 30 - 33. In addition, the contact structure of Figure 29 can also be manufactured with the aid of the materials shown by Figure 28, in such a way that the first intermediate layer 33 and the second intermediate layer 34 are made by sputtering. In that case, the sputtered intermediate layers 33 and 34 will grow to the base part 36 and the conductor part 38, but not to any substantial extent to the wall part 37, provided the contact hole 18, 28 does not widen towards the contact opening 8. One possibility is to use a first intermediate layer 33 containing zinc and on the surface of this either directly a third intermediate layer 35 made from nickel by a chemical growing method, or a construction, in which a second intermediate layer 34 made from nickel-aluminium is used between the layers 33 and 35. In such an embodiment, there is no need at all of chemical copper growing, as the nickel forms a vertical contact along the side wall of the contact hole.

Figure 30 shows yet another contact-element structure. In the structure of Figure 30, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel-aluminium and the third intermediate layer 35 is of nickel grown by a chemical growing method. This, in the structure of Figure 30, the contact hole is filled with nickel, i.e. the conductor core 29 of the contact element is nickel. Otherwise, the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 30.

Figure 31 shows yet another contact-element structure. In the structure of Figure 31, the intermediate layer 2 comprises a first intermediate layer 33 and a second intermediate layer 34. The first intermediate layer 33 can be manufactured, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate

layer 34 is of copper grown by a chemical growing method, or alternatively of nickel grown by a selective chemical growing method. Alternatively, the structure of Figure 31 can also be made in such a way that the first and second intermediate layers 33 and 34 are replaced with a single layer of chemically grown nickel. The conductor core 29 is typically copper and the conductor 22 comprises a first and second copper layer 12 and 32. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 31.

Figure 32 shows yet another contact-element structure. In the structure of Figure 32, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method, the growing method is selective, in such a way that the nickel grows on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 32 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 32.

Figure 33 shows yet another contact-element structure. The method described in connection with Figures 10 - 17, for example, in which a photo-resist layer 30 is used, can be used for making the structure of Figure 32. In the structure of Figure 33, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method of the example, the growing method is selective, in such a way that the nickel grows only on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 33 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with

Figures 28 and 29 apply in the case of the structure of Figure 33.

Thus, in the embodiments a method is presented for the manufacture of a circuit module, in which method

- 5
 - a conductor foil 12 is taken,
 - a component 6, which comprises contact areas 7, the material of which contains a first metal, is taken,
 - 10
 - the component 6 is attached to a conductor foil 12 by means of a polymer layer 25,
 - an insulator layer 1 is manufactured around the component 6 attached to the conductor foil 12,
 - 15
 - contact holes 18, 28 are made in the polymer layer 25 at the positions of the contact areas 7, in such a way that the contact surface area A_{CONYI} between each contact hole 18, 28 and the corresponding contact area 7 is less than the surface area A_{PAD} of the contact area 7, and
 - 20
 - an intermediate layer 2, which contains at least a third metal, is grown at least on the surface of the contact areas 7 in the contact holes 18, 28, and
 - 25
 - a layer 32 of a second metal is grown, which layer 32 is in contact with the surface of the intermediate layer 2 and extends along the conductors 22 being made, and
 - conductors 22 are formed by patterning the conductor foil 12, and, if necessary, also the intermediate layer 2 on the surface of the conductor foil 12 and/or the layer 32 of a second metal.
 - 30

In a typical embodiment, the contact holes 8 are made in the conductor foil 12 before

attaching the component, so that the component is thus attached to a conductor foil 12 equipped with contact openings. In the commonest form of this type of embodiment, the contact openings do not extend to the surfaces of the contact areas 7, so that after the attaching of the component 6 contact holes 18, 28 are further opened through the contact openings 8.

In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.

In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.

When making the intermediate-layer construction, at least one chemical growing method is typically used.

The embodiments depict a circuit module, which comprises

- an insulator layer 1,
- inside the insulator layer 1, at least one component 6, which comprises contact areas 7, the material of which contains a first metal,

- on the surface of the insulator layer 1, conductors 22, which comprise at least a first layer 12 and a second layer 32, in such a way that at least the second layer 32 contains a second metal, and
 - 5 - contact elements for forming electrical contacts between the contact areas 7 and the conductors 22, which contact elements comprise an intermediate layer 2, which contains a third metal, on the surface of the material of the contact area 7,
 - in which the first, second, and third metals are different metals, and
 - 10 - the contact surface area $A_{COT\ 1}$ between the intermediate layer 2 and the contact area 7 is less than the surface area A_{PAD} of the contact area.
- In one embodiment, the first metal is aluminium, the second metal is copper, and the
- 15 third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.
- In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course,
- 20 in addition to nickel, also contain other metals or metal alloys, as stated above.
- In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in
- 25 addition to nickel, also contain other metals or metal alloys, as stated above.
- In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.
- 30 In a typical embodiment, the contact elements comprise a copper core 29 made using an electrochemical growing method, which, in the direction of the side walls and the component 6 is bounded by the intermediate layer 2 and in the direction of the conductor

22 connects continuously, i.e. without an interface to the material of the second layer 32 of the conductor 22. In other words, the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is manufactured in the same process, so that the parts are attached permanently to each other and there is no interface between them. Between the first layer 12 and second layer 22 of the conductor, on the other hand, there is typically an interface, or a corresponding transition zone, which can be detected, for example, by analysing the crystalline structure or impurity concentration of the metal.

10 In one embodiment, the width W_{CONT} of the contact surface between the contact element and the contact area 7 of the component is 0 - 20 % less than the greatest width W_{MAX} of the contact element in the same direction.

15 The contact elements usually fill entirely the contact holes 18, 28, i.e. the contact elements are not hollow, but are solidly of conductor material.

Usually, the aim in the embodiments is for the height H of the contact element to be less than, or equal to the greatest width W_{MAX} of the contact element.

20 There are also embodiments of the circuit module, in which the insulator layer 1 includes at least one layer of fibre material 19, in which there is an opening in the fibre material 19 for the component 6, as well as a uniform polymer layer, which is attached to the fibre material 19 and to the components 6, 16.

25 The manufacturing processes described above and their sub-processes can be modified in many ways. For example, the use of an actual adhesive depicted above in attaching the component to the conductor foil 12 can be replaced with some other adhesion mechanism. On example that can be given is the use of an insulator layer 13 possessing an adhesion property on the surface of the conductor foil 12 (see Figure 1 and the corresponding description). The components 6 are then pressed directly against the
30 insulator layer 13, so that the components attach sufficiently in place in a manner correspondingly to that described in connection with the embodiment using adhesive.

Such an insulator layer 13 can contain, for example, a tape-like surfacing, or consist of a polymer or similar material that is shapable at least in its surface part.

5 The method can also be implemented without the use of an adhesive 5 or an adhesion property. In that case, the components 6 can be attached in place, for example, mechanically or with the aid of a vacuum. The vacuum or similar temporary attachment can then be maintained until the component 6 is sufficiently secured in place with the aid of the insulator material 1.

10 The component 6 to be attached can be, for example, an integrated circuit, such as a memory chip, processor, or ASIC. The component to be attached can also be, for example, a MEMS, LED, or passive component. The component to be attached can be cased or uncased and its contact terminals can consists of contact areas 7, contact bumps 17, or similar. There can also be a conductor coating thinner than an actual contact bump
15 on the surface of the contact areas of the component.

A different material of the insulator layer 1 from those in the examples described above can also be selected. The insulator layer 1 can be manufactured from a suitable polymer or from a material containing polymer. The material of manufacture of the insulator
20 layer 1 can be, for example, in a liquid or pre-hardened form (such as prepreg). In the manufacture of the insulator layer 1 it is possible to use, for example, glass-fibre reinforced sheet, such as an FR4 or FR5-type sheet. Other examples of materials, which can be used in the manufacture of the insulator layer 1 are PI (polyimide), aramide, polytetrafluoroethylene, and Teflon®. Instead of, or as well as thermosetting plastics,
25 thermoplastics too, for example some suitable LCP (liquid crystal polymer) material can be used in the manufacture of the insulator layer 1.

In addition, it is obvious to one skilled in the art that the features described above of the invention can be used as part of some larger totality, for example, in such a way that the
30 electronics module is manufactured partly using some method according to the prior art and partly using the embodiments depicted here. It is also possible to manufacture additional circuit-board layers on the surface or surfaces of the electronic-module

structures described above, or also to attach components, for example, by means of the surface-mounting technique.

5 One skilled in the art will also understand that, when reference is made in the present document to a specific material, for example, aluminium, nickel, or copper, the reference is to a material, which in terms of the application is substantially of the said material. The material referred to can thus, in addition to the said principal element contain, from the point of view of the application, insubstantial amounts of impurities and other elements. For example, an aluminium contact area is usually of a material that typically
10 contains a minimum of 95 % aluminium.

When, on the other hand, reference is made to a material containing some specific element, this means that the material contains an essentially large content of the said element. In addition, the material can contain substantial or insubstantial amounts of
15 other elements. For example, the layer containing zinc will thus contain an amount of zinc that is of significance in terms of the contact properties between the aluminium and the next metal.

The examples given above depict some possible methods and structures, which the aid
20 of which our invention can be exploited. However, our invention is not restricted to only the examples and embodiments described above, but instead the invention covers numerous other methods and structures, taking into account the full scope of the Claims and the equivalence interpretation.

Claims:

1. Circuit module, comprising
 - a first insulator layer having a first surface and a second surface;
 - at least one second insulator layer on the first surface;
 - at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing a first metal,
 - conductors on the second surface of the first insulator layer, the conductors comprising at least a first layer and a second layer, in such a way that at least the second layer contains a second metal, and
 - contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal, a contact surface area ($A_{CONT\ I}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal.
2. The circuit module of Claim 1, wherein the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.
3. The circuit module of Claim 1, wherein the first metal is gold, the second metal is copper, and the third metal is nickel.
4. The circuit module of Claim 1, wherein the intermediate layer comprises a layer containing zinc.
5. The circuit module of Claim 1, wherein the intermediate layer comprises a layer containing copper.
6. The circuit module of Claim 1, wherein the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium.
7. The circuit module of Claim 1, wherein the intermediate layer extends along the side

walls of the contact elements between the contact terminals and the conductors.

8. The circuit module of Claim 1, wherein each contact element comprises a copper core, which connects continuously to the material of the second layer of the conductors.

5

9. The circuit module of Claim 1, wherein the conductors comprise

a first layer of copper on the second surface of the first insulator layer, and

10

a second layer of copper on the surface of the first copper layer.

10. The circuit module of Claim 1, wherein the conductors comprise

a first layer of copper on the second surface of the first insulator layer,

15

an intermediate layer on the surface of the first copper layer, and

a second layer of copper on the surface of the intermediate layer.

20

11. The circuit module of Claim 10, wherein the intermediate layer between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.

25

12. The circuit module of Claim 1, wherein a width (W_{CONT}) of the contact surface between the contact element and the contact terminal of the component is 0 - 20 % less than a greatest width (W_{MAX}) of the contact element in the same direction.

13. The circuit module of Claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (W_{MAX}) of the contact element.

30

14. The circuit module of Claim 1, wherein the at least one second insulator layer contains at least one layer of fibre material and an opening in the fibre material for the at

least one component.

15. The circuit module of Claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

16. The circuit module of Claim 15, wherein the polymer layer comprises layer of a hardened adhesive.

17. Circuit module, comprising

- a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;
- a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer covering the first surface of the conductors;
- at least one second insulator layer on the first surface of the first insulator layer;
- at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal;
- contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal, a contact surface area ($A_{CONT\ 1}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal;
- at least one layer of metal in the contact terminals containing a first metal;
- at least one layer of metal in the conductors containing a second metal; and
- the intermediate layer containing a third metal.

18. The circuit module of claim 18, comprising

- a layer of hardened adhesive between the first insulator layer and the at least one component.

19. Circuit module, comprising

a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;

5 a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer entirely covering the first surface of the conductors;

at least one second insulator layer on the first surface of the first insulator layer;

at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal; and

10 contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal, a contact surface area ($A_{CONT\ 1}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the
15 contact terminal.

20. The circuit module of claim 18, comprising

a layer of hardened adhesive between the first insulator layer and the at least one component.

(57) Abstract:

Manufacturing method and circuit module, which comprises an insulator layer and, inside the insulator layer, at least one component, which comprises contact areas, the material of which contains a first metal. On the surface of the insulator layer are conductors, which comprise at least a first layer and a second layer, in such a way that at least the second layer contains a second metal. The circuit module comprises contact elements between the contact areas and the conductors for forming electrical contacts. The contact elements, for their part, comprise, on the surface of the material of the contact area, an intermediate layer, which contains a third metal, in such a way that the first, second, and third metals are different metals and the contact surface area (A_{CONTI}), between the intermediate layer and the contact area is less than the surface area (A_{PAD}) of the contact area.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Circuit module and method of manufacturing the same		
First Named Inventor/Applicant Name:		Petteri Palm		
Filer:		Joshua Paul Wert/Ross Worrell		
Attorney Docket Number:		IMB 22 US CON		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	18635497
Application Number:	14231758
International Application Number:	
Confirmation Number:	1010
Title of Invention:	Circuit module and method of manufacturing the same
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert/Ross Worrell
Filer Authorized By:	Joshua Paul Wert
Attorney Docket Number:	IMB 22 US CON
Receipt Date:	01-APR-2014
Filing Date:	
Time Stamp:	03:30:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1600
RAM confirmation Number	7997
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Application Data Sheet	IMB22USCON_2014-04-01_ADS.pdf	1421424 6e10af20a29dd4a5b07e6a56ab65cb19d9c4841	no	5
Warnings:					
Information:					
2		IMB22USCON_2014-04-01_DECLARATION_SIGNED.pdf	244823 a8491de261f564ac1a122c45b1e83d97b96e1fef	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Oath or Declaration filed		2	3	
Warnings:					
Information:					
3	Drawings-other than black and white line drawings	IMB22USCON_2014-04-01_Drawings.pdf	181372 dd09be65fc693be95166906e74241164a1e3522	no	15
Warnings:					
Information:					
4	Transmittal of New Application	IMB22USCON_2014-04-01_SB0005_New_application_fill.pdf	1092974 00998164f7d1697dcc58c9b62d84b10fbff25bf5	no	2
Warnings:					
Information:					
5		IMB22USCON_2014-04-01_Specification.pdf	185710 c0c6ffeb170f1a12ed5ed4ee6e1f11809cc88ae9	yes	47
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	42	
	Claims		43	46	
	Abstract		47	47	
Warnings:					
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6	Fee Worksheet (SB06)	fee-info.pdf	32657 9f206d385813c3aa6089210bafae656aed5cb9ed	no	2
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US CON
		Application Number	
Title of Invention	Circuit module and method of manufacturing the same		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Petteri		Palm		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Helsinki	Country Of Residenceⁱ	FI		
Citizenship under 37 CFR 1.41(b)ⁱ		FI			
Mailing Address of Applicant:					
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City	Helsinki	State/Province			
Postal Code	00660	Countryⁱ	FI		
Applicant 2					
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Risto		Tuominen		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Helsinki	Country Of Residenceⁱ	FI		
Citizenship under 37 CFR 1.41(b)ⁱ		FI			
Mailing Address of Applicant:					
Address 1	c/o GE Embedded Electronics Oy				
Address 2	Kuortaneenkatu 2				
City	Helsinki	State/Province			
Postal Code	00510	Countryⁱ	FI		
Applicant 3					
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Antti		lihol		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Helsinki	Country Of Residenceⁱ	FI		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		IMB 22 US CON	
		Application Number			
Title of Invention		Circuit module and method of manufacturing the same			
Citizenship under 37 CFR 1.41(b) i		FI			
Mailing Address of Applicant:					
Address 1		Hiomotie 18 B 40			
Address 2					
City	Helsinki	State/Province			
Postal Code	00380	Country	FI		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	95002		
Email Address	posti@seppolaine.fi	Add Email	Remove Email

Application Information:

Title of the Invention	Circuit module and method of manufacturing the same		
Attorney Docket Number	IMB 22 US CON	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US CON
		Application Number	
Title of Invention	Circuit module and method of manufacturing the same		
Customer Number	95002		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/990785	2009-05-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12/990785	a 371 of international	PCT/FI2009/050383	2009-05-11

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. [Add](#)

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
20085443	FI	2008-05-12	☒ Yes ☐ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. [Add](#)

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove			
If the Assignee is an Organization check here. ☒			
Organization Name	GE Embedded Electronics Oy		

Mailing Address Information:

Address 1	Kuortaneenkatu 2		
Address 2			
City	Helsinki	State/Province	
Country ⁱ	FI	Postal Code	00510
Phone Number		Fax Number	
Email Address			

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US CON
		Application Number	
Title of Invention	Circuit module and method of manufacturing the same		

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Joshua P. Wert Reg. No 65880/			Date (YYYY-MM-DD)	2014-04-01
First Name	Joshua	Last Name	Wert	Registration Number	65880

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : Not Yet Assigned Confirmation No. : N/A
Applicant : GE Embedded Electronics Oy
Filed : 2014-03-31
TC/AU : Not Yet Assigned
Examiner : Not Yet Assigned

Attorney Docket No. : IMB 22 US CON

M/S Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION FILED UNDER 37 CFR 1.63(d)

Sir:

In regards to the present application a copy of a previously executed declaration is attached herein in accordance with 37 CFR 1.63(d). The present declaration was filed in the parent application 12/990,785 on March 11, 2010. Should there be any problems with the acceptance of the present declaration, the Office is respectfully requested to call the undersigned at 571-480-8372 in order to expedite the pre-examination formalities process.

Respectfully submitted,

/ Joshua P. Wert Reg. No. 65880/

Joshua P. Wert
Reg. No. 65880
Seppo Laine Oy
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FIN-00180 Helsinki, Finland
Tel. (US) +1 571-480-8372

April 1, 2014

Seppo Laine Oy

JPW / rw

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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of
Invention

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

As the below named inventor(s), I/we declare that:

This declaration is directed to:

- ☒ The attached application, or
☐ Application No. _____ filed on _____
☐ As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)

Inventor one: Petteri Palmi Date: 28.10.2010

Signature: [Signature] Citizen of: FI

Inventor two: Risto Tuominen Date: 6.10.2010

Signature: [Signature] Citizen of: FI

☒ Additional inventors or a legal representative are being named on 1 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet
	Page <u>2</u> of <u>2</u>

Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
An/ti		Initials	
Inventor's Signature		Date <u>Oct. 28 2010</u>	
Residence: City	State	Country	FI Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 21 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

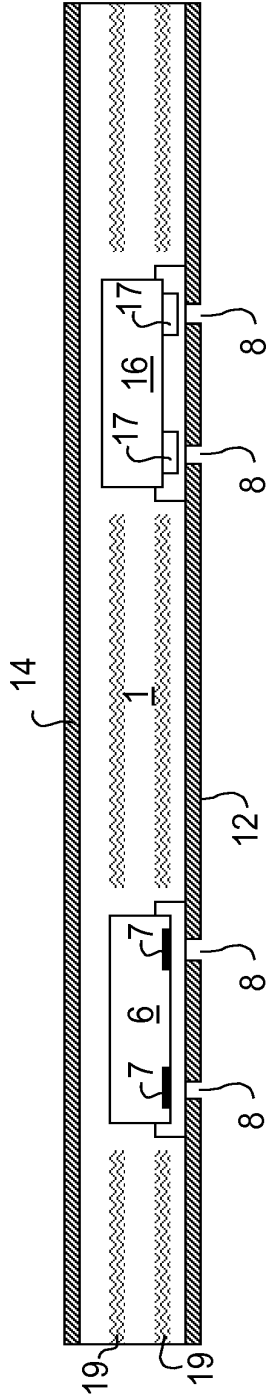


Fig. 3

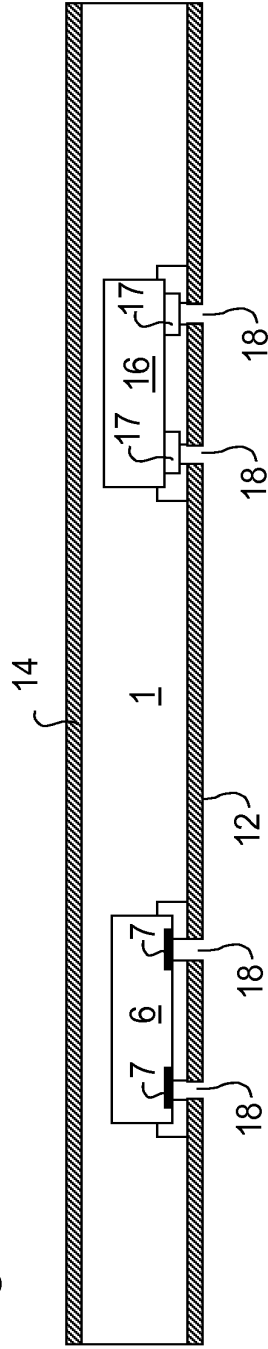


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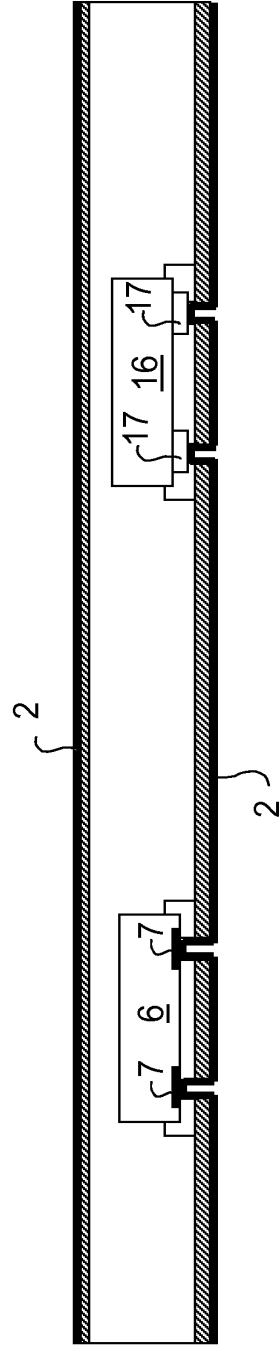


Fig. 5

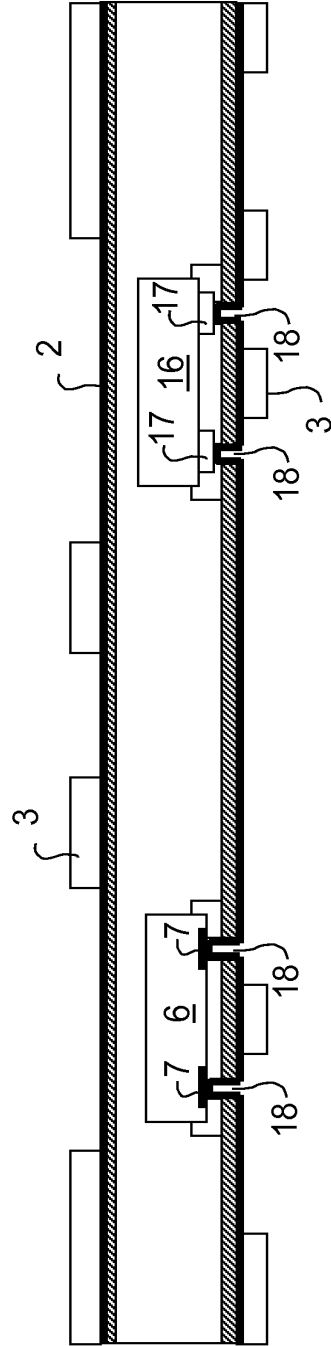


Fig. 6

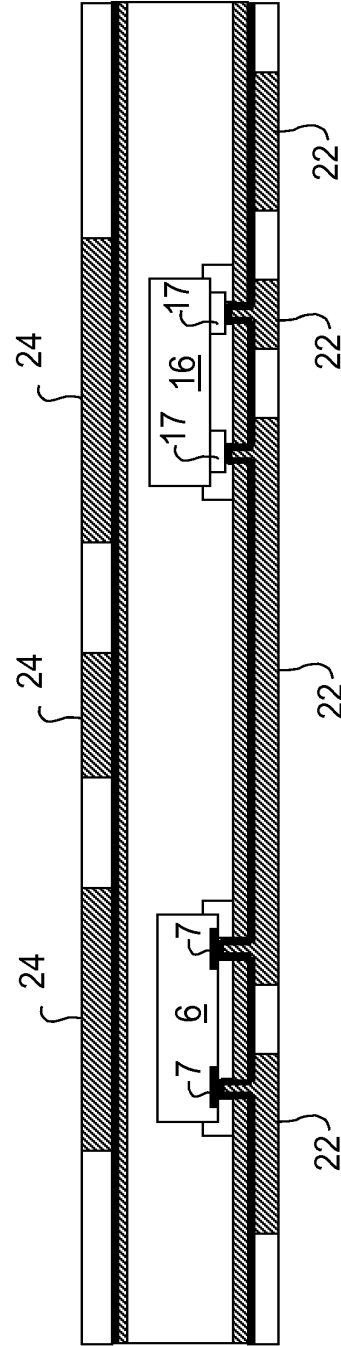


Fig. 7

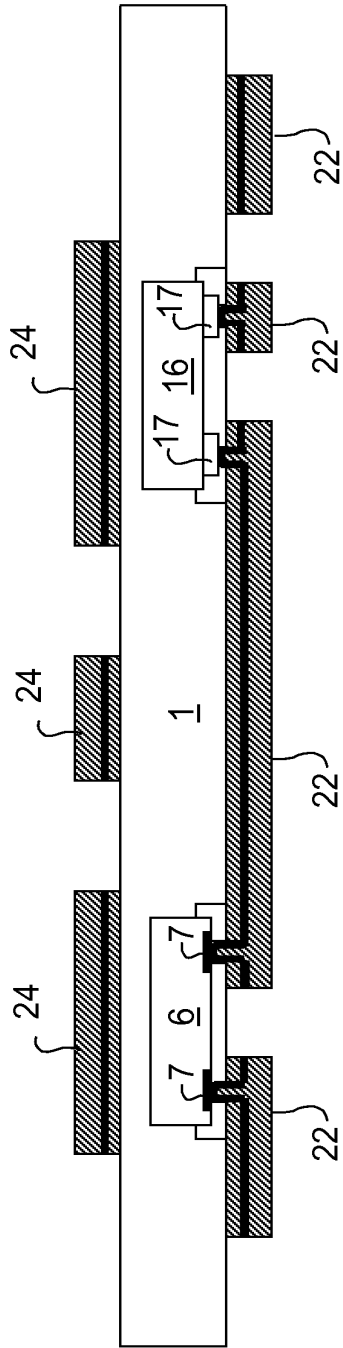


Fig. 8

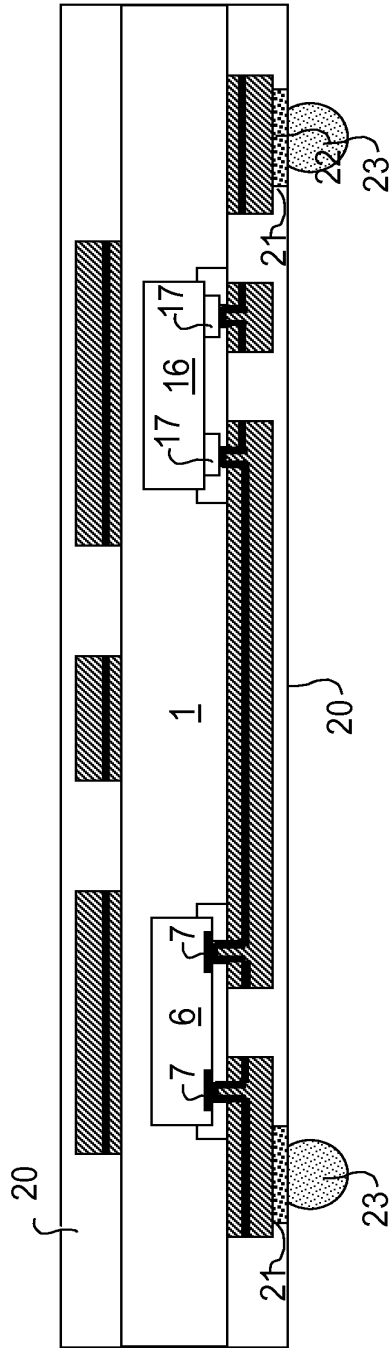


Fig. 9

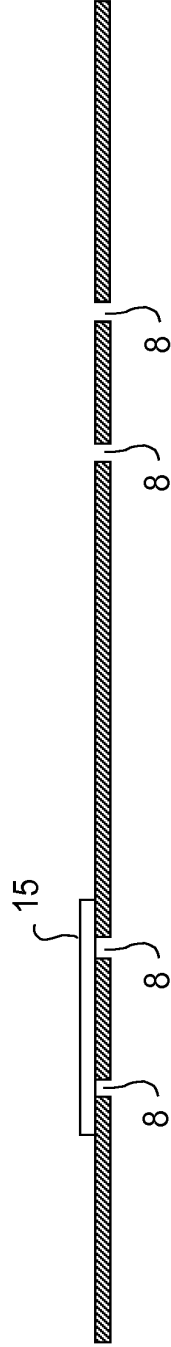


Fig. 10

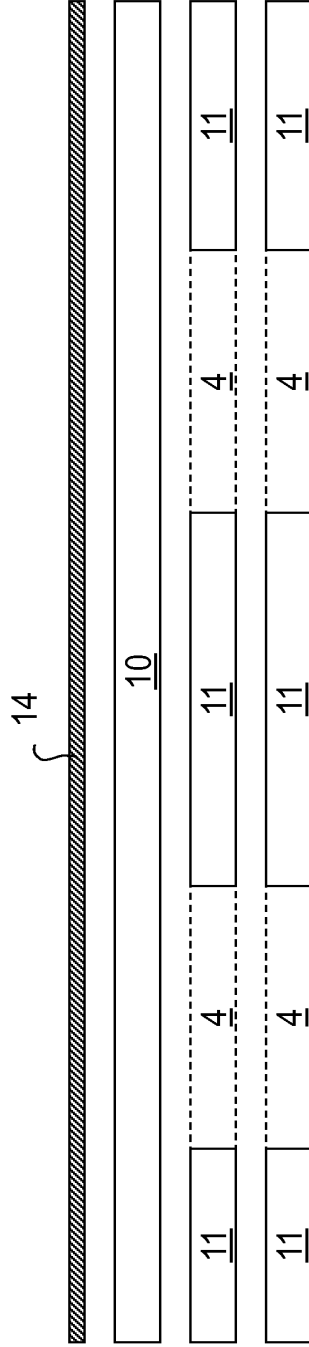
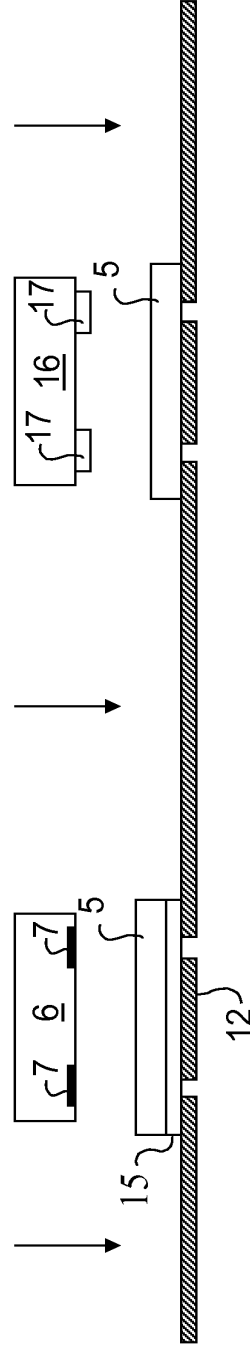


Fig. 11



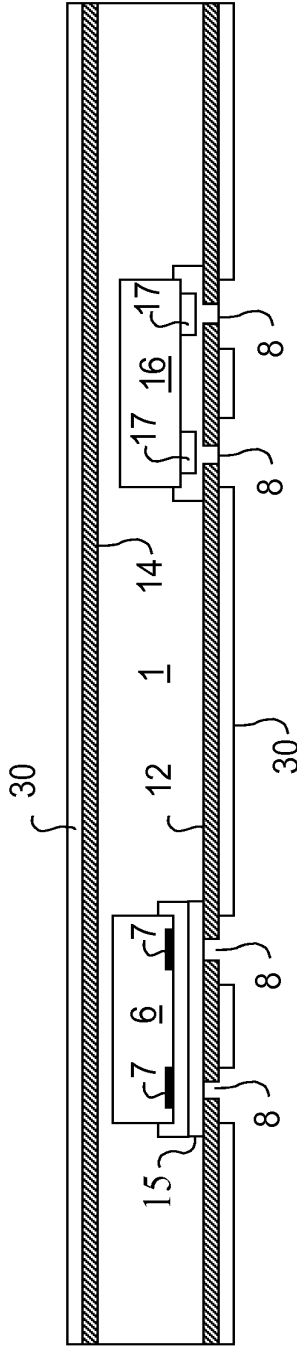


Fig. 12

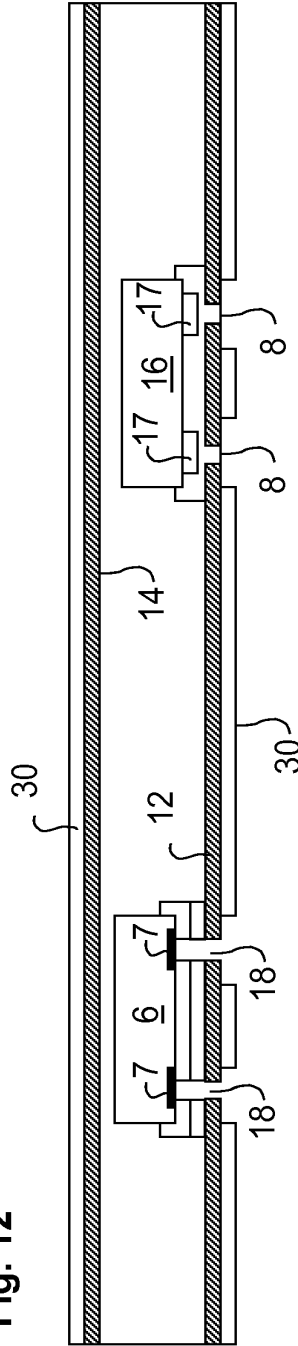


Fig. 13

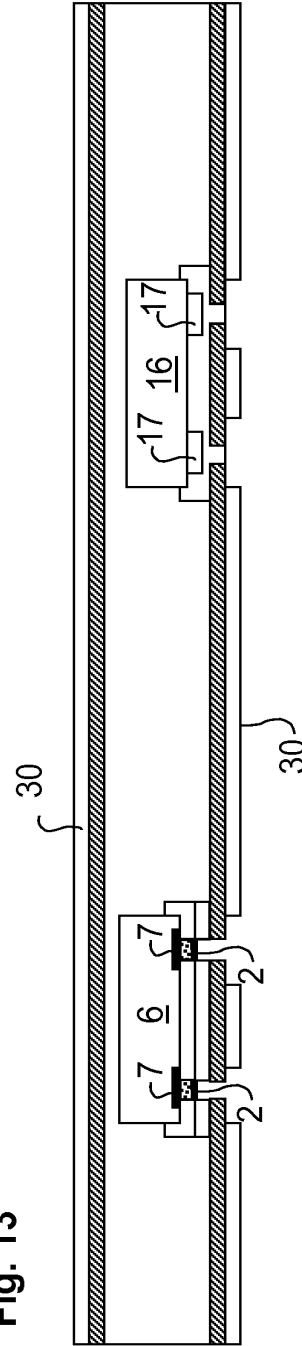


Fig. 14

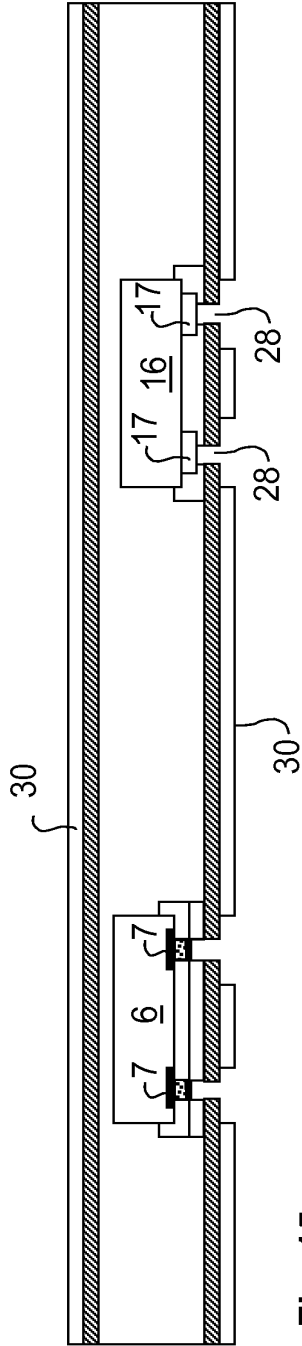


Fig. 15

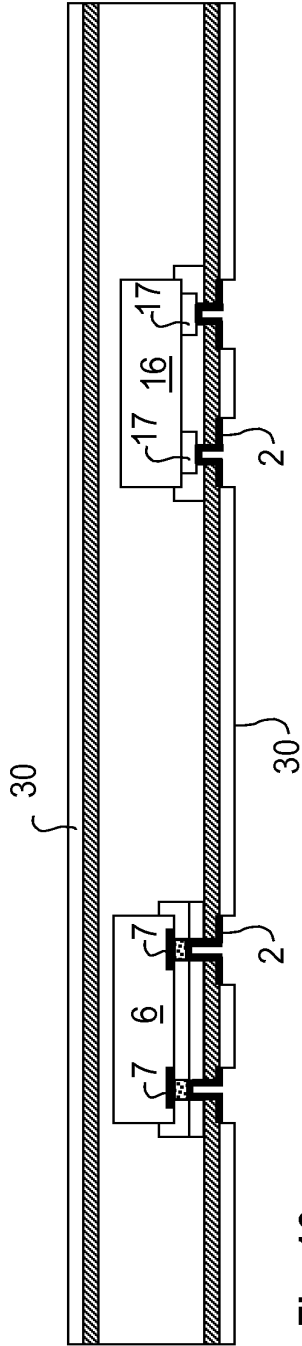


Fig. 16

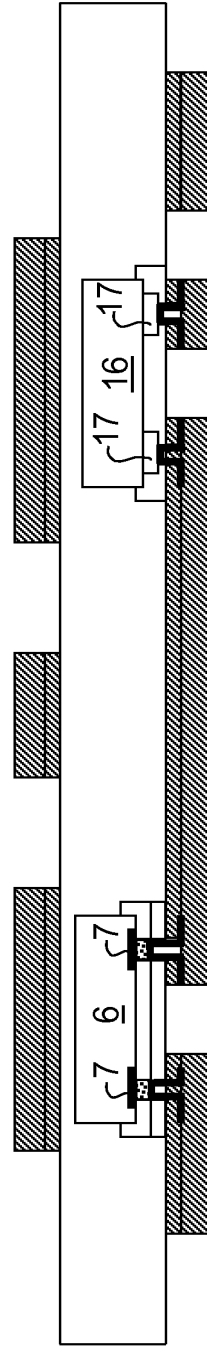


Fig. 17

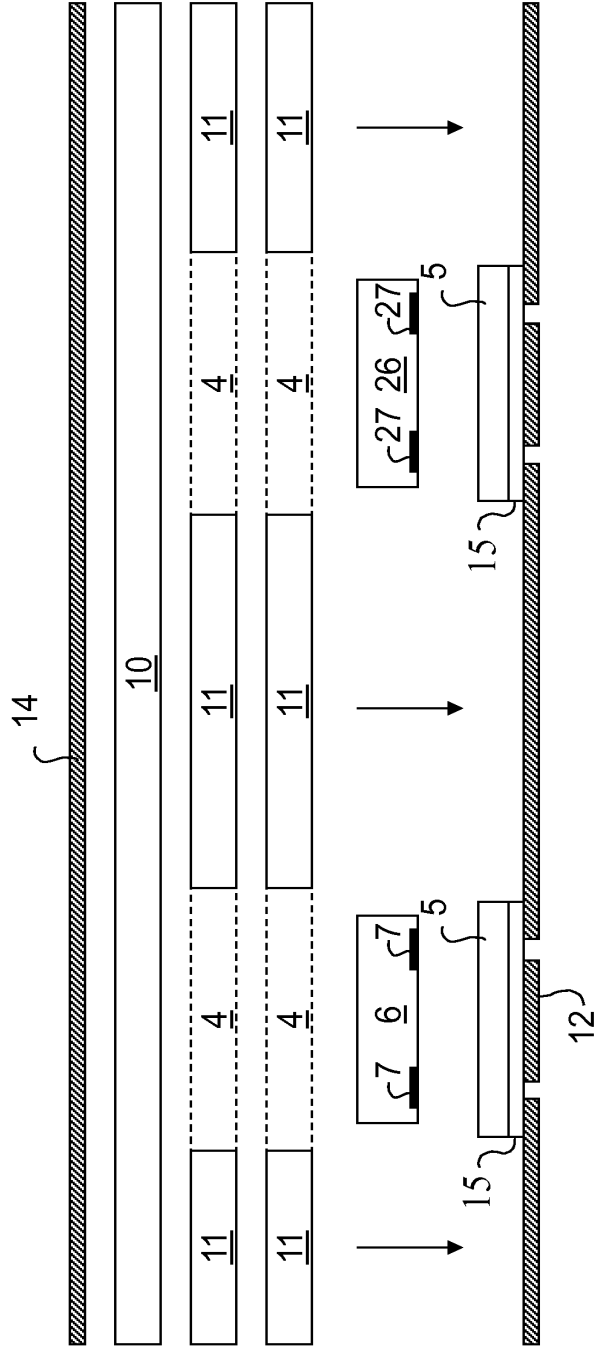


Fig. 18

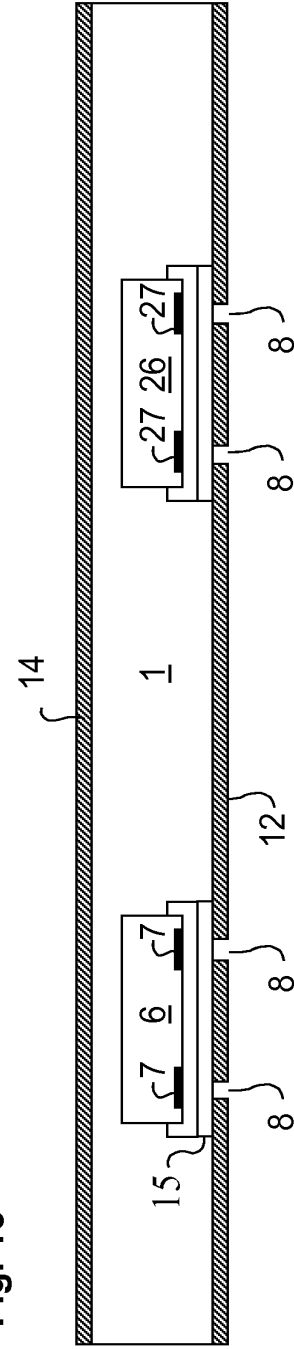


Fig. 19

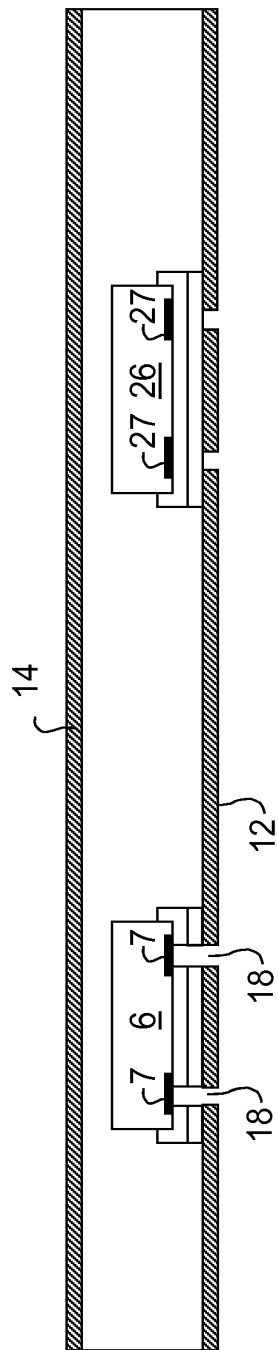


Fig. 20

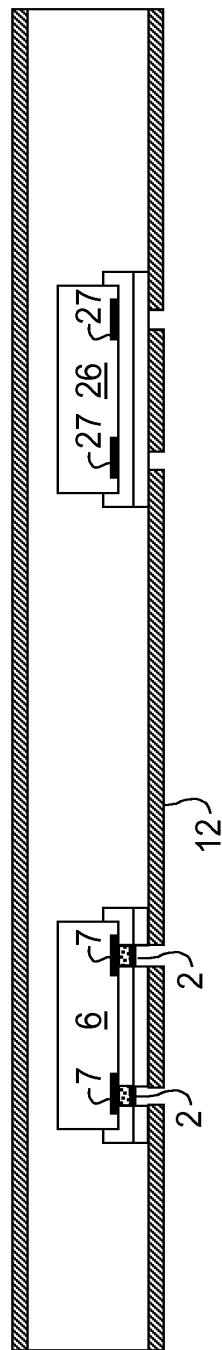


Fig. 21

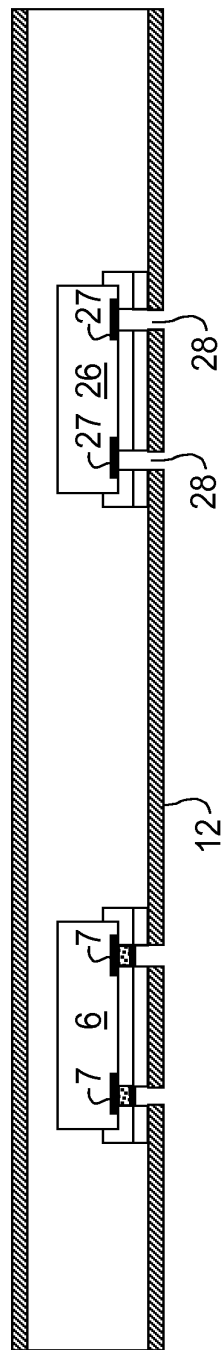


Fig. 22

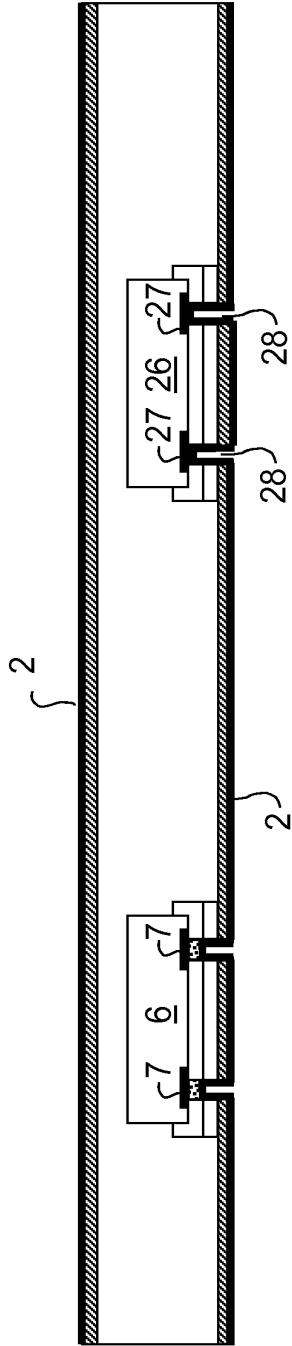


Fig. 23

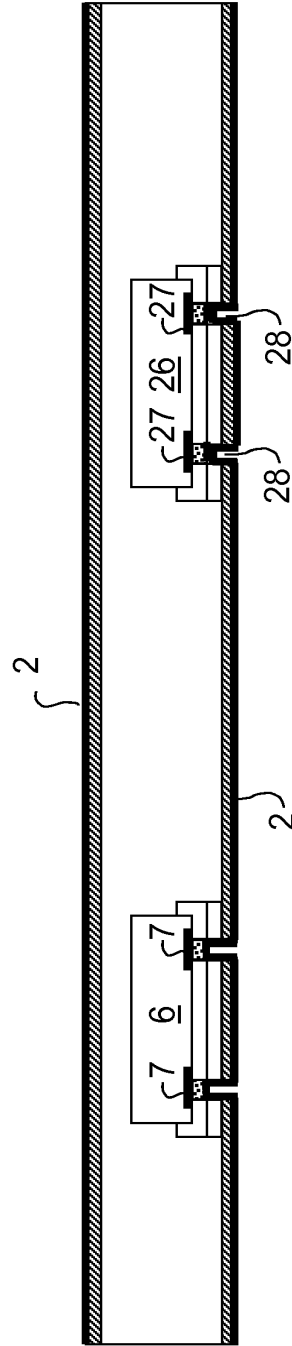


Fig. 24



Fig. 25

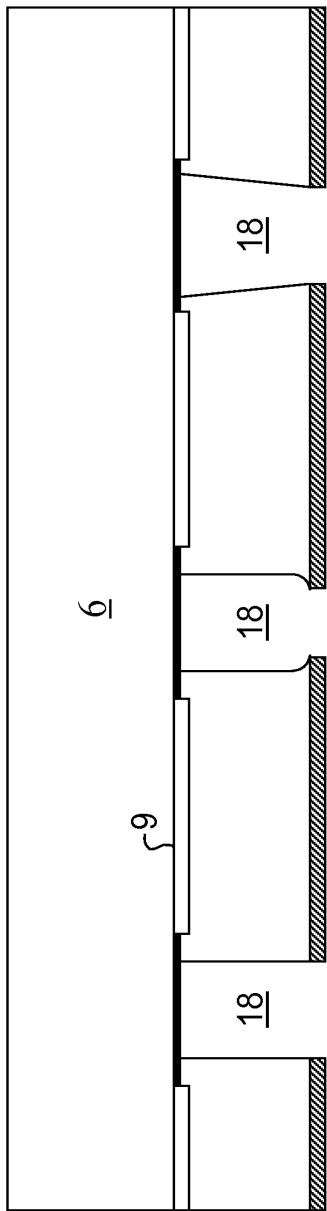


Fig. 26

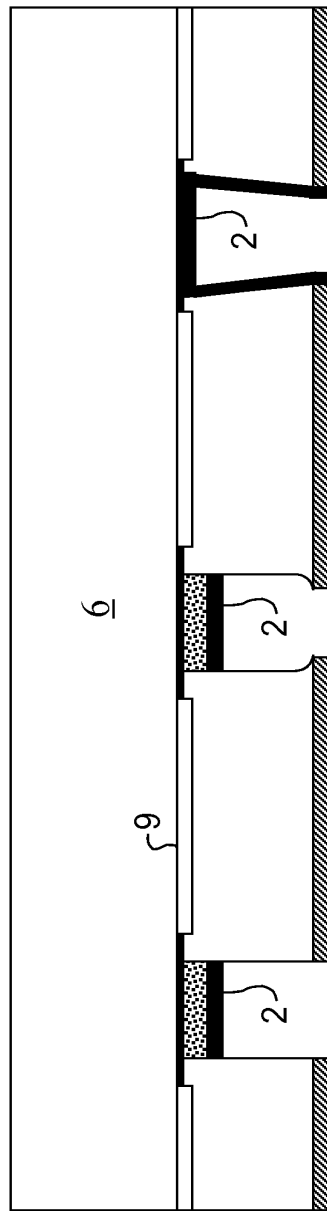


Fig. 27

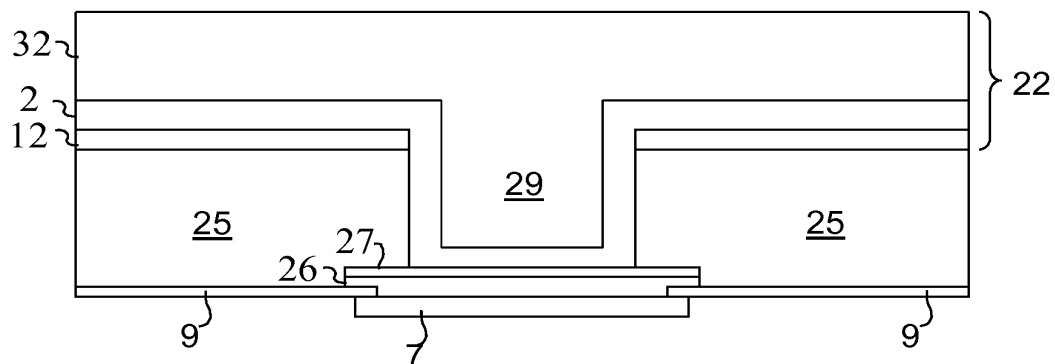


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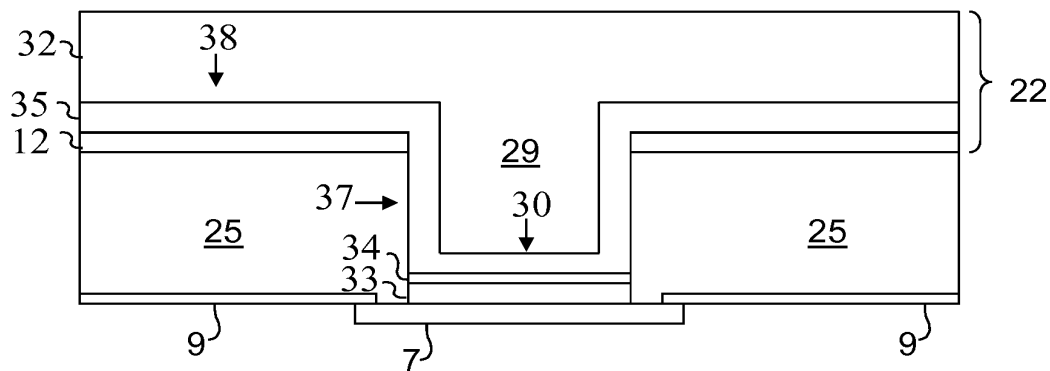


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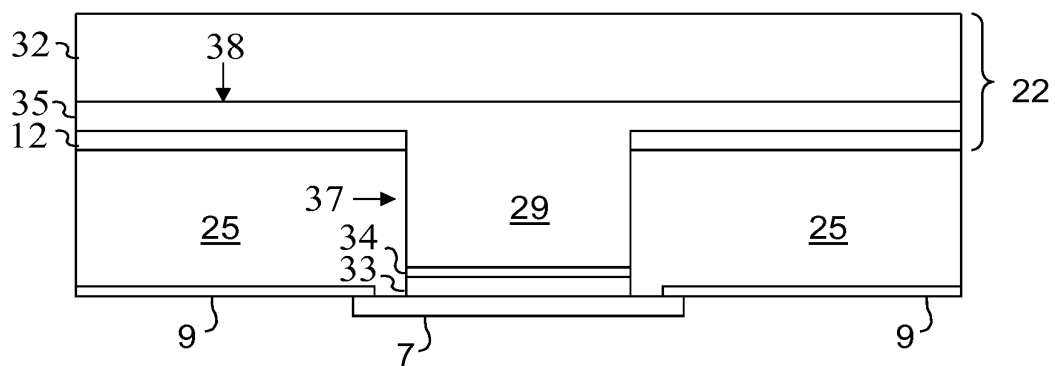


Fig. 30

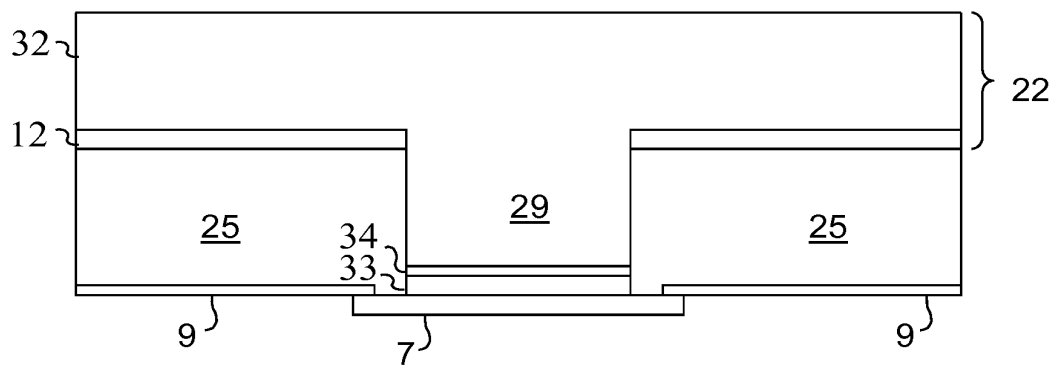


Fig. 31

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