

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5948335

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	6991966	
Patent Number:	7294529	
Patent Number:	7299546	
Patent Number:	7673387	
Patent Number:	7696005	
Patent Number:	8062537	
Patent Number:	8225499	
Patent Number:	8238113	
Patent Number:	8240032	
Patent Number:	8286341	
Patent Number:	8547701	
Patent Number:	8581109	
Patent Number:	8631566	
Patent Number:	8659134	
Patent Number:	8699233	
Patent Number:	8735735	
Patent Number:	8964409	
Patent Number:	8984746	
Patent Number:	9301394	
Patent Number:	9420694	

Property Type	Number
Patent Number:	9425158
Patent Number:	9999136
Patent Number:	8076586
Patent Number:	8704359
Patent Number:	9363898
Patent Number:	8240033

CORRESPONDENCE DATA

Fax Number: (703)643-9789

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4349062975

Email: yoon@capitoliplaw.com

Correspondent Name: YEASUN YOON

Address Line 1: 20319 KIAWAH ISLAND DR

Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER: PA01GETOIMBERATEK

NAME OF SUBMITTER: YEASUN YOON

SIGNATURE: /yoon/

DATE SIGNED: 02/05/2020

This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7

source=imbera assignment#page1.tif

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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this “**Assignment**”) is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company (“**Assignor**”), in favor of **ImberaTek, LLC**, a Delaware limited liability company (“**Assignee**”).

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the “**Patent Sale Agreement**”); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the “**Patents**”).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

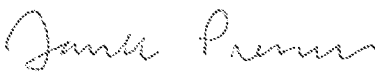
Name: PATRICK K. PATNODE

Title: AUTHORIZED SIGNATORY

Acknowledgement:

State of New York)
County of Schenectady)

ss.


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8024403
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRP10307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A I, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A I, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1 , US10010019B2, US2018352689A I	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15'937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	04/15/2014	8699233	IMB 22 US	3345
95002	7590	03/26/2014		

Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 518 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Petteri Palm, Helsinki, FINLAND;
Risto Tuominen, Espoo, FINLAND;
Antti Iihola, Helsinki, FINLAND;

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

095002 7590 11/21/2013
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	11/03/2010	Potteri Palm	IMB 22 US	3345

TITLE OF INVENTION: CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	02/21/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NORRIS, JEREMY C	2847	17A-257000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Seppo Laine Oy
2. Joshua P. Wert
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE (CITY and STATE OR COUNTRY)

GE Embedded Electronics Oy

Helsinki (FI)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number (enclose an extra copy of this form)

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Joshua P. Wert Reg. No. 65880/

Date 2014-02-20

Typed or printed name Joshua P. Wert

Registration No. 65880

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		12990785		
Filing Date:		03-Nov-2010		
Title of Invention:		CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
First Named Inventor/Applicant Name:		Petteri Palm		
Filer:		Joshua Paul Wert/Ross Worrell		
Attorney Docket Number:		IMB 22 US		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	18247907
Application Number:	12990785
International Application Number:	
Confirmation Number:	3345
Title of Invention:	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert/Ross Worrell
Filer Authorized By:	Joshua Paul Wert
Attorney Docket Number:	IMB 22 US
Receipt Date:	20-FEB-2014
Filing Date:	03-NOV-2010
Time Stamp:	07:59:59
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	9881
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	IMB22US_2014-02-20_Issue_fee.pdf	209055 26760e8d364ac58431b44b5774fa6d607d334c5b	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32282 8594a5849e72a029bb311f3805890c77ba36c907	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			241337		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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NOTICE OF ALLOWANCE AND FEE(S) DUE

95002 7590 11/21/2013
Seppo Laine Oy
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FINLAND

EXAMINER

NORRIS, JEREMY C

ART UNIT

PAPER NUMBER

2847

DATE MAILED: 11/21/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	11/03/2010	Petteri Palm	IMB 22 US	3345

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APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	02/21/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
 or **Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

95002 7590 11/21/2013
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	11/03/2010	Petteri Palm	IMB 22 US	3345

TITLE OF INVENTION: CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	02/21/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
NORRIS, JEREMY C	2847	174-257000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	11/03/2010	Petteri Palm	IMB 22 US	3345
95002	7590	11/21/2013	EXAMINER	
Seppo Laine Oy Joshua P. Wert Itamerenkatu 3B Helsinki, FI00180 FINLAND			NORRIS, JEREMY C	
			ART UNIT	PAPER NUMBER
			2847	

DATE MAILED: 11/21/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 355 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 355 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and
December 31, 2013**

(Addendum to PTOL-85)

If the “Notice of Allowance and Fee(s) Due” has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to \$0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 12/990,785	Applicant(s) PALM ET AL.	
	Examiner JEREMY NORRIS	Art Unit 2847	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 09/25/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-11, 13-25 and 27-37. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____ | <ol style="list-style-type: none"> 5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____ |
|---|---|

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 1-11, 13-25 and 27-37 are allowed.

The following is an examiner's statement of reasons for allowance: Claim 1 states the limitation "attaching at least one additional component within the circuit module by means of a second polymer layer, said second polymer layer differing from the first polymer layer by at least one property of the polymer layers." This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art. Claim 14 states the limitation "on the surface of the insulator layer, conductors, which comprise a first layer of copper on the surface of the insulator layer, and a second layer of copper on the surface of the first copper layer." This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art. Claim 23 states the limitation "in which part of the intermediate layer extends along the side walls of the contact elements between the contact areas and the conductors." This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art. Claim 27 states the limitation "a first layer of copper on the surface of the insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer." This limitation, in conjunction with the

other claimed features, was neither found to be disclosed in nor suggested by the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY NORRIS whose telephone number is (571)272-1932. The examiner can normally be reached on Mon, Wed, Fri 10am-6pm; Tues, Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy J. Thompson can be reached on 571-272-2342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Primary Examiner
Art Unit 2847

/Jeremy C. Norris/
Primary Examiner, Art Unit 2847

Search Notes 	Application/Control No. 12990785	Applicant(s)/Patent Under Reexamination PALM ET AL.
	Examiner JEREMY NORRIS	Art Unit 2835

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
174	262-266, 260	3-18-13	jcsn
361	792-795, 761-764	3-18-13	jcsn
	update search	11-13-13	jcsn
029	832-841	11-13-13	jcsn

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
174	260,262-266	3-18-13	jcsn
361	761-764,792-795	3-18-13	jcsn
029	832-841	11-13-13	jcsn

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Issue Classification 	Application/Control No. 12990785	Applicant(s)/Patent Under Reexamination PALM ET AL.
	Examiner JEREMY NORRIS	Art Unit 2847

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION										
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED					
361		761				H	0	5	K	1 / 16 (2006.0)						
CROSS REFERENCE(S)						H	0	5	K	1 / 18 (2006.0)						
						H	0	5	K	3 / 30 (2006.01.01)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															
174	260															
29	832															

NONE		Total Claims Allowed:	
		35	
(Assistant Examiner)	(Date)		
/JEREMY NORRIS/ Primary Examiner.Art Unit 2847	11/15/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	18, 19

Issue Classification 	Application/Control No. 12990785	Applicant(s)/Patent Under Reexamination PALM ET AL.
	Examiner JEREMY NORRIS	Art Unit 2847

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
24	1	4	17	14	33										
25	2	5	18	15	34										
26	3	6	19	16	35										
27	4	7	20	22	36										
28	5	8	21	23	37										
29	6	9	22												
30	7	17	23												
31	8	18	24												
32	9	19	25												
33	10		26												
34	11	20	27												
	12	21	28												
35	13	10	29												
1	14	11	30												
2	15	12	31												
3	16	13	32												

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 35	
/JEREMY NORRIS/ Primary Examiner.Art Unit 2847 (Primary Examiner) _____ (Date) _____		11/15/2013 O.G. Print Claim(s) 1	O.G. Print Figure 18, 19

Application No.: 12/990,785
Docket No.: IMB 22 US
Reply to Office Action dated: 2013-03-25

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 12/990,785 Confirmation No. : 3345
Applicant : PALM, Petteri et al.
Filed : 2010-11-03
TC/AU : 2835
Examiner : NORRIS, Jeremy C.

Attorney Docket No. : IMB 22 US

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-FINAL OFFICE ACTION

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated March 25, 2013, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) Method for manufacturing a circuit module, the method comprising;
 - taking a conductor foil,
 - making contact openings in the conductor foil for the manufacture of contact elements,
 - taking a first component, which comprises contact areas, the material of which contains a first metal,
 - attaching the first component to the conductor foil by means of a first polymer layer,
 - attaching at least one additional component within the circuit module by means of a second polymer layer, said second polymer layer differing from the first polymer layer by at least one property of the polymer layers,
 - manufacturing an insulator layer around the component attached to the conductor foil,
 - making contact holes in the polymer layer at the positions of the contact areas, in such a way that the contact surface area between each contact hole and the corresponding contact area is less than the surface area of the contact area, and
 - growing an intermediate layer at least on the surface of the contact areas in the contact holes, the intermediate layer containing at least a third metal,
 - growing a layer of a second metal, which layer is in contact with the surface of the intermediate layer and extends along the conductors being made, and
 - forming conductors by patterning the conductor foil, and, if necessary, also the intermediate layer on the surface of the conductor foil and/or the layer of a second metal.
2. (Previously Presented) Method according to Claim 1, in which
 - the contact openings are manufactured before the attachment of the

component,

the component is attached to a conductor foil equipped with contact openings, and

after the attachment of the component, contact holes are opened through the contact openings.

3. (Previously Presented) Method according to Claim 2, in which the contact holes are opened through the contact openings using a CO₂ laser, in which case the conductor foil is used as a mask.
4. (Previously Presented) Method according to Claim 1, in which the first metal is aluminium, the second metal is copper, and the third metal contains at least one of the metals zinc and nickel.
5. (Previously Presented) Method according to Claim 1, in which the first metal is gold, the second metal is copper, and the third metal is nickel.
6. (Previously Presented) Method according to Claim 1, in which the intermediate layer comprises a layer containing zinc, which is manufactured using a double zincate process.
7. (Previously Presented) Method according to Claim 1, in which the intermediate layer comprises a layer containing nickel, which is manufactured using a chemical nickel-growing method.
8. (Previously Presented) Method according to Claim 1, in which the intermediate layer comprises a layer containing copper, which is manufactured using a chemical copper-growing method.
9. (Previously Presented) Method according to any of Claim 1, in which the insulator layer is manufactured in such a way that at least one insulator sheet containing a

fibre material and a pre-hardened polymer is taken,

a hole for the component is made in the insulator sheet containing a fibre material, and

the insulator sheet or insulator sheets are laminated together with the conductor foil and its related structures.

10. (Previously Presented) Method according to Claim 1, in which the surface of the conductor foil, to which the component is attached, comprises a uniform insulator layer.

11. (Previously Presented) Method according to Claim 1, in which a spacer is placed between the component and the conductor foil.

12. (Cancelled)

13. (Previously Presented) Method according to Claim 1, in which the component to be attached is a bumpless component.

14. (Currently Amended) Circuit module, which comprises;

an insulator layer,

inside the insulator layer, at least one component, which comprises contact areas, the material of which contains a first metal,

on the surface of the insulator layer, conductors, which comprise a first layer of copper on the surface of the insulator layer, and a second layer of copper on the surface of the first copper layer~~at least a first layer and a second layer, in such a way that at least the second layer contains a second metal,~~ and

contact elements between the contact areas and the conductors for forming electrical contacts, which contact elements comprise an intermediate layer, which contains a third metal, on the surface of the material of the contact area,

wherein the first, second, and third metals are different metals, and

the contact surface area between the intermediate layer and the contact area is

less than the surface area of the contact area.

15. (Original) Circuit module according to Claim 14, in which the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.
16. (Original) Circuit module according to Claim 14, in which the first metal is gold, the second metal is copper, and the third metal is nickel.
17. (Previously Presented) Circuit module according to Claim 14, in which the material of the contact areas is mainly aluminium.
18. (Previously Presented) Circuit module according to Claim 14, in which the intermediate layer comprises a layer containing zinc.
19. (Previously Presented) Circuit module according to Claim 18, in which the intermediate layer comprises, in addition to the layer containing zinc, at least one second intermediate metal layer.
20. (Previously Presented) Circuit module according to Claim 19, in which the at least one second intermediate metal layer is of copper grown by a chemical growing process.
21. (Previously Presented) Circuit module according to Claim 20, in which the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium between the layer containing zinc and the copper layer.
22. (Previously Presented) Circuit module according to Claim 18, in which the layer containing zinc contains zinc, copper, nickel, and iron.
23. (Currently Amended) ~~Circuit-A circuit module according to Claim 14, which~~

comprises;
an insulator layer,
inside the insulator layer, at least one component, which comprises contact
areas, the material of which contains a first metal,
on the surface of the insulator layer, conductors, which comprise at least a
first layer and a second layer, in such a way that at least the second layer contains a
second metal, and
contact elements between the contact areas and the conductors for forming
electrical contacts, which contact elements comprise an intermediate layer, which
contains a third metal, on the surface of the material of the contact area, in which part
of the intermediate layer extends along the side walls of the contact elements between
the contact areas and the conductors,
wherein the first, second, and third metals are different metals, and
the contact surface area between the intermediate layer and the contact area is
less than the surface area of the contact area.

24. (Previously Presented) Circuit module according to Claim 23, in which the contact elements comprise a copper core made using an electrochemical growing method, which, in the direction of the side wall and component, is bounded by the intermediate layer and, in the direction of the conductor connects continuously, i.e. without an interface, to the material of the second layer of the conductor.

25. (Previously Presented) Circuit module according to Claim 23, in which the part of the intermediate layer extending along the side walls of the of the contact elements contains copper grown by a chemical growing method, or nickel grown by a chemical growing method.

26. (Cancelled)

27. (Currently Amended) ~~Circuit A circuit module according to Claim 14, in which the~~
~~conductors comprise~~ which comprises;

an insulator layer,
inside the insulator layer, at least one component, which comprises contact
areas, the material of which contains a first metal,
on the surface of the insulator layer, conductors, which comprise a first layer
of copper on the surface of the insulator layer, an intermediate layer on the surface of
the first copper layer, and a second layer of copper on the surface of the intermediate
layer, and
contact elements between the contact areas and the conductors for forming
electrical contacts, which contact elements comprise an intermediate layer, which
contains a third metal, on the surface of the material of the contact area,
wherein the first, second, and third metals are different metals, and
the contact surface area between the intermediate layer and the contact area is
less than the surface area of the contact area.

28. (Previously Presented) Circuit module according to Claim 27, in which the part of the intermediate layer between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.
29. (Previously Presented) Circuit module according to Claim 14, in which the width of the contact surface between the contact element and the contact area of the component is 0 - 20 % less than the greatest width of the contact element in the same direction.
30. (Previously Presented) Circuit module according to Claim 14, in which the height of the contact element is less than or equal to the greatest width of the contact element.
31. (Previously Presented) Circuit module according to Claim 14, in which the insulator layer contains at least one layer of fibre material, in which there is an opening in the fibre material for the component, as well as a unified polymer layer,

which is attached to the fibre material and to the component.

32. (Previously Presented) Circuit module according to Claim 14, which comprises a polymer layer, between the conductors and the component, in which layer there are contact holes for the contact elements, and in which the contact elements fill the contact holes completely.
33. (Previously Presented) Circuit module according to Claim 32, in which the polymer layer between the conductors and the component comprises a first and a second polymer layer, in which the first polymer layer is of a first polymer and the second polymer layer is of a hardened adhesive.
34. (Previously Presented) Circuit module according to Claim 33, in which the first polymer layer and the second polymer layer are local, in such a way that they exist essentially only at the location of the component.
35. (Previously Presented) Circuit module according to Claim 14, in which the component comprises a passivation layer on the surface of the component and the contact areas are located inside openings in the passivation layer, in which case the intermediate layer extends through the opening in the passivation layer.
36. (New) Circuit module according to Claim 27, in which the intermediate layer comprises a layer containing zinc.
37. (New) Circuit module according to Claim 27, which comprises a polymer layer, between the conductors and the component, in which layer there are contact holes for the contact elements, and in which the contact elements fill the contact holes completely.

REMARKS/ARGUMENTS

Claims 1-11, 13-25 and 27-37 are pending. Claims 12 and 26 have been cancelled. Claims 36 and 37 have been added and correspond to original claims 18 and 33 respectively. Claim 1 has been amended to incorporate the subject matter of claim 12. Claim 14 has been amended to incorporate the subject matter of claim 26. Claims 23 and 27 have been amended to be drafted in independent format and incorporate the subject matter of previous claim 14. No new matter has been added.

Regarding Claim Rejections under 35 U.S.C. § 102(b)

The claims have been amended as described above in view of the Examiner's indication of allowable subject matter in light of U.S. 6,242,282 to Fillion. The Applicant's amendments in the present response do not represent a forfeiture of the originally claimed subject matter but are being made in order to advance prosecution at this time. The Applicant reserves the right to pursue the original subject matter of the claims in the future.

CONCLUSION

The Applicant believes that that present application is in condition for allowance. Notice of the same is earnestly solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Joshua Wert, Reg. No. 65880 at (571) 480-8372, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

/ Joshua P. Wert Reg. No. 65880/

Joshua P. Wert
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Seppo Laine Oy

JPW / rw

Application No.: 12/990,785
Docket No.: IMB 22 US
Reply to Office Action dated: 2013-03-25

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September 25, 2013

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	12/990,785
	Filing Date	11/03/2010
	First Named Inventor	Petteri Palm
	Art Unit	2835
	Examiner Name	NORRIS, JEREMY C
	Attorney Docket Number	IMB 22 US
Total Number of Pages in This Submission		

ENCLOSURES (Check all that apply)		
☒ Fee Transmittal Form ☒ Fee Attached ☒ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☒ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation ☐ Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☐ Other Enclosure(s) (please identify below):
<div style="border: 1px solid black; padding: 2px;">Remarks</div>		
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm Name	Seppo Laine Oy	
Signature	/Joshua P. Wert Reg. No. 65880/	
Printed name	Joshua P. Wert	
Date	2013-09-25	Reg. No. 65880

CERTIFICATE OF TRANSMISSION/MAILING			
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Typed or printed name		Date	

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)		Docket Number (Optional) IMB 22 US																																		
Application Number 12/990,785	Filed 2010-11-03																																			
For PALM, Petteri et al.																																				
Art Unit 2835	Examiner NORRIS, JEREMY C																																			
<p>This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.</p> <p>The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):</p> <table style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;"><u>Fee</u></th><th style="text-align: center;"><u>Small Entity Fee</u></th><th style="text-align: center;"><u>Micro Entity Fee</u></th><th></th></tr></thead><tbody><tr><td>☐ One month (37 CFR 1.17(a)(1))</td><td style="text-align: center;">\$200</td><td style="text-align: center;">\$100</td><td style="text-align: center;">\$50</td><td>\$ _____</td></tr><tr><td>☐ Two months (37 CFR 1.17(a)(2))</td><td style="text-align: center;">\$600</td><td style="text-align: center;">\$300</td><td style="text-align: center;">\$150</td><td>\$ _____</td></tr><tr><td>☒ Three months (37 CFR 1.17(a)(3))</td><td style="text-align: center;">\$1,400</td><td style="text-align: center;">\$700</td><td style="text-align: center;">\$350</td><td>\$ 1400</td></tr><tr><td>☐ Four months (37 CFR 1.17(a)(4))</td><td style="text-align: center;">\$2,200</td><td style="text-align: center;">\$1,100</td><td style="text-align: center;">\$550</td><td>\$ _____</td></tr><tr><td>☐ Five months (37 CFR 1.17(a)(5))</td><td style="text-align: center;">\$3,000</td><td style="text-align: center;">\$1,500</td><td style="text-align: center;">\$750</td><td>\$ _____</td></tr></tbody></table> <p>☐ Applicant asserts small entity status. See 37 CFR 1.27.</p> <p>☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.</p> <p>☐ A check in the amount of the fee is enclosed.</p> <p>☐ Payment by credit card. Form PTO-2038 is attached.</p> <p>☐ The Director has already been authorized to charge fees in this application to a Deposit Account.</p> <p>☐ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number _____.</p> <p>☒ Payment made via EFS-Web.</p> <p>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p> <p>I am the</p> <p>☐ applicant/inventor.</p> <p>☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).</p> <p>☒ attorney or agent of record. Registration number 65880.</p> <p>☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.</p> <table style="width: 100%; border-collapse: collapse;"><tr><td style="width: 50%; padding: 5px;">/Joshua P. Wert Reg. No. 65880/ _____ Signature</td><td style="width: 50%; padding: 5px;">2013-09-25 _____ Date</td></tr><tr><td style="padding: 5px;">Joshua P. Wert _____ Typed or printed name</td><td style="padding: 5px;">571-480-8372 _____ Telephone Number</td></tr></table> <p>NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.</p> <p>☒ * Total of 1 forms are submitted.</p>				<u>Fee</u>	<u>Small Entity Fee</u>	<u>Micro Entity Fee</u>		☐ One month (37 CFR 1.17(a)(1))	\$200	\$100	\$50	\$ _____	☐ Two months (37 CFR 1.17(a)(2))	\$600	\$300	\$150	\$ _____	☒ Three months (37 CFR 1.17(a)(3))	\$1,400	\$700	\$350	\$ 1400	☐ Four months (37 CFR 1.17(a)(4))	\$2,200	\$1,100	\$550	\$ _____	☐ Five months (37 CFR 1.17(a)(5))	\$3,000	\$1,500	\$750	\$ _____	/Joshua P. Wert Reg. No. 65880/ _____ Signature	2013-09-25 _____ Date	Joshua P. Wert _____ Typed or printed name	571-480-8372 _____ Telephone Number
	<u>Fee</u>	<u>Small Entity Fee</u>	<u>Micro Entity Fee</u>																																	
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Joshua P. Wert _____ Typed or printed name	571-480-8372 _____ Telephone Number																																			

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		12990785		
Filing Date:		03-Nov-2010		
Title of Invention:		CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
First Named Inventor/Applicant Name:		Petteri Palm		
Filer:		Joshua Paul Wert/Ross Worrell		
Attorney Docket Number:		IMB 22 US		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1614	1	420	420
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 3 months with \$0 paid	1253	1	1400	1400
Miscellaneous:				
Total in USD (\$)				1820

Electronic Acknowledgement Receipt

EFS ID:	16946403
Application Number:	12990785
International Application Number:	
Confirmation Number:	3345
Title of Invention:	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert/Ross Worrell
Filer Authorized By:	Joshua Paul Wert
Attorney Docket Number:	IMB 22 US
Receipt Date:	25-SEP-2013
Filing Date:	03-NOV-2010
Time Stamp:	08:15:33
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1820
RAM confirmation Number	9224
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		IMB22US2013-09-25_Amendment.pdf	137311 afa656c6c92244cad5cbb1a5522903897e903c5b	yes	10
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	8	
	Applicant Arguments/Remarks Made in an Amendment		9	10	
Warnings:					
Information:					
2	Transmittal Letter	IMB22US2013-09-25_SB0021_General_transmittal.pdf	265026 5c7fd926fd0b0f824d0f656c8c0f8964ce91d957	no	2
Warnings:					
Information:					
3	Extension of Time	IMB22US2013-09-25_SB0022_Extension.pdf	187769 6c85f74b8899f64824e28ead500aacc623a14c3	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32693 f3960fd06f4420de79e4e1a2ca652fe5be8e8bc5	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			622799		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 12/990,785		Filing Date 11/03/2010		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL				
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	09/25/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 35	Minus	** 35	= 0	X \$80 =		0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
					TOTAL ADD'L FEE		0		
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$		=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$		=	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
					TOTAL ADD'L FEE				
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/990,785	11/03/2010	Petteri Palm	IMB 22 US	3345
95002	7590	03/25/2013		
Seppo Laine Oy Joshua P. Wert Itamerenkatu 3B Helsinki, FI00180 FINLAND			EXAMINER NORRIS, JEREMY C	
			ART UNIT 2835	PAPER NUMBER
			MAIL DATE 03/25/2013	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/990,785	Applicant(s) PALM ET AL.	
	Examiner JEREMY NORRIS	Art Unit 2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-35 is/are pending in the application.
 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1,4,6,8,10,11,13-15,17-20,29,30 and 32 is/are rejected.
- 8) ☒ Claim(s) 2,3,5,7,9,12,16,21-28,31 and 33-35 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6, 8, 10, 11, 13-15, 17-20, 29, 30, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,242,282 B1 (Fillion).

Fillion discloses a method for manufacturing a circuit module, the method comprising taking a conductor foil (220), making contact openings (238; figure 16) in the conductor foil for the manufacture of contact elements, taking a component (210), which comprises contact areas (230), the material of which contains a first metal (col. 4, lines 1-15), attaching the component to the conductor foil by means of a polymer layer (236), manufacturing an insulator layer (240) around the component attached to the conductor foil, making contact holes (col. 4, lines 45-60) in the polymer layer at the positions of the contact areas, in such a way that the contact surface area, between each contact hole and the corresponding contact area is less than the surface area of the contact area, and growing an intermediate layer (zincation, col. 4, lines 1-15) at least on the surface of the contact areas in the contact holes, the intermediate layer containing at least a

third metal (col. 4, lines 1-15), and growing a layer (244) of a second metal, which layer is in contact with the surface of the intermediate layer and extends along the conductors (280) being made, and forming conductors (280) by patterning (col. 3, lines 5-15) the conductor foil, and, if necessary, also the intermediate layer on the surface of the conductor foil and/or the layer of a second metal [claim 1], in which the first metal is aluminum (col. 4, lines 1-15), the second metal is copper (col. 10-15), and the third metal contains at least one of the metals zinc and nickel (col 4, lines 1-5) [claim 4], in which the intermediate layer comprises a layer containing zinc, which is manufactured using a double zincate process (col. 4, lines 1-15) [claim 6], in which the intermediate layer comprises a layer containing copper, which is manufactured using a chemical copper-growing method (col. 4, lines 1-15) [claim 8], in which the surface of the conductor foil, to which the component is attached, comprises a uniform insulator layer [claim 10], in which a spacer (236) is placed between the component and the conductor foil [claim 11], in which the component to be attached is a bumpless component [claim 13].

Similarly, Fillion discloses, a circuit module, which comprises an insulator layer (240), inside the insulator layer, at least one component (210), which comprises contact areas (230), the material of which contains a first metal (aluminum), on the surface of the insulator layer, conductors (222), which comprise at least a first layer and a second layer (col. 4, lines 10-20), in such a way that at least the second layer contains a second metal (copper or titanium), and contact elements (244) between the contact areas and the conductors for forming electrical contacts, which contact elements comprise an

intermediate layer (zincation, col. 4, lines 1-15), which contains a third metal, on the surface of the material of the contact area, wherein the first, second, and third metals are different metals, and the contact surface area between the intermediate layer and the contact area is less than the surface area of the contact area [claim 14], in which the first metal is aluminum, the second metal is copper, and the third metal is at least one of the metals zinc and nickel [claim 15], in which the material of the contact areas is mainly aluminum [claim 17], in which the intermediate layer comprises a layer containing zinc [claim 18], in which the intermediate layer (2) comprises, in addition to the layer containing zinc, at least one second intermediate metal layer (copper or titanium; col 4, lines 1-15) [claim 19], in which the at least one second intermediate metal layer (35) is of copper grown by a chemical growing process (col. 4, lines 1-15) [claim 20], in which the width of the contact surface between the contact element and the contact area of the component is 0 - 20 % less than the greatest width of the contact element in the same direction [claim 29], in which the height (H) of the contact element is less than, or equal to the greatest width of the contact element [claim 30], which comprises a polymer layer (236), between the conductors and the component, in which layer there are contact holes (283) for the contact elements, and in which the contact elements fill the contact holes (18, 28) completely [claim 32].

Allowable Subject Matter

Claims 2, 3, 5, 7, 9, 12, 16, 21-28, 31, and 33-35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Claims 2 and 3 state the limitation “in which the contact openings are manufactured before the attachment of the component), the component is attached to a conductor foil equipped with contact openings, and after the attachment of the component, contact holes are opened through the contact openings.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 5 states the limitation “in which the first metal is gold, the second metal is copper, and the third metal is nickel.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 7 states the limitation “in which the intermediate layer comprises a layer containing nickel, which is manufactured using a chemical nickel-growing method.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim, 9 states the limitation “in which the insulator layer is manufactured in such a way that at least one insulator sheet containing a fibre material and a pre-hardened polymer is taken, a hole for the component is made in the insulator sheet containing a fibre material, and the insulator sheet or insulator sheets are laminated together with the conductor foil and its related structures.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 12 states the limitation “in which, in addition to the component, at least one other component is located in the circuit module, in such a way that the manners of attachment of the first and second components differ from each other in the case of at

least one property of the polymer layer.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 16 states the limitation “in which the first metal is gold, the second metal is copper, and the third metal is nickel.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 21 states the limitation “in which the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminum between the layer containing zinc and the copper layer.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 22 states the limitation “in which the layer containing zinc contains zinc, copper, nickel, and iron.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claims 23-25 state the limitation “in which part of the intermediate layer extends along the side walls of the contact elements between the contact areas and the conductors.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 26 states the limitation “in which the conductors comprise a first layer of copper on the surface of the insulator layer, and a second layer of copper on the surface of the first copper layer.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claims 27 and 28 state the limitation “in which the conductors comprise a first layer of copper on the surface of the insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim

31 states the limitation “in which the insulator layer contains at least one layer of fibre material, in which there is an opening in the fibre material for the component, as well as a unified polymer layer, which is attached to the fibre material and to the component.”

This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claims 33 and 34 state the limitation “in which the polymer layer between the conductors and the component comprises a first and a second polymer layer, in which the first polymer layer is of a first polymer and the second polymer layer is of a hardened adhesive.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art. Claim 35 states the limitation “in which the component comprises a passivation layer (9) on the surface of the component and the contact areas (7) are located inside openings in the passivation layer, in which case the intermediate layer (2) extends through the opening in the passivation layer.” This limitation, in conjunction with the other claimed features, is neither disclosed in nor suggested by the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEREMY NORRIS whose telephone number is (571)272-1932. The examiner can normally be reached on Mon, Wed, Fri 10am-6pm; Tues, Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy J. Thompson can be reached on 571-272-2342. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
Primary Examiner
Art Unit 2835

/Jeremy C. Norris/
Primary Examiner, Art Unit 2835

Notice of References Cited	Application/Control No. 12/990,785	Applicant(s)/Patent Under Reexamination PALM ET AL.	
	Examiner JEREMY NORRIS	Art Unit 2835	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,242,282	06-2001	Fillion et al.	438/106
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

12990785 - GAU: 2835

PTO/SB/08a (07-09)

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				Application Number	
				Filing Date	
				First Named Inventor	Petteri Palm
				Art Unit	
				Examiner Name	
				Attorney Docket Number	IMB 22 US
Sheet	1	of	1		

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		WO 2006056643 A	06-01-2006	Imbera Electronics Oy		
		EP 1259103 A	11-20-2002	Ibiden Co Ltd		
		EP 0380289 A	08-01-1990	Fujitsu Ltd		
		WO 2009138560	11-19-2009	Imbera Electronics Oy		

Examiner Signature	/Jeremy Norris/	Date Considered	02/25/2013
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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Search Notes 	Application/Control No. 12990785	Applicant(s)/Patent Under Reexamination PALM ET AL.
	Examiner JEREMY NORRIS	Art Unit 2835

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
174	262-266, 260	3-18-13	jcsn
361	792-795, 761-764	3-18-13	jcsn

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
174	260,262-266	3-18-13	jcsn
361	761-764,792-795	3-18-13	jcsn

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CONFIRMATION NO. 3345

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/990,785	11/03/2010	174	2835	IMB 22 US		
RULE						
APPLICANTS INV001Petteri Palm, Helsinki, FINLAND; INV002Risto Tuominen, Espoo, FINLAND; INV003Antti Iihola, Helsinki, FINLAND; ** CONTINUING DATA ***** This application is a 371 of PCT/FI09/50383 05/11/2009 ** FOREIGN APPLICATIONS ***** FINLAND 20085443 05/12/2008 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/28/2010						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/JEREMY C NORRIS/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 15	TOTAL CLAIMS 35	INDEPENDENT CLAIMS 2
ADDRESS Seppo Laine Oy Joshua P. Wert Itamerenkatu 3B Helsinki, FI00180 FINLAND						
TITLE CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME						
FILING FEE RECEIVED 1760	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

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PTO/SB/08a (07-09)

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		Complete if Known		
		Application Number	12/990785	
		Filing Date	05-11-09	
		First Named Inventor	PALM, Petteri	
		Art Unit		
		Examiner Name		
Sheet	1	of	1	Attorney Docket Number IMB22US

[illegible][illegible]

Examiner Signature	/Jeremy Norris/	Date Considered	02/25/2013
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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.N./

Receipt date: 11/09/2010

12990785 - GAU: 2835

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known		
		Application Number	12/990785	
		Filing Date	Nov. 5, 2009	
		First Named Inventor	PALM, Petteri	
		Art Unit		
		Examiner Name		
Sheet 1		of 1	Attorney Docket Number	IMB 22 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Finnish Search Report of FI20085443, Jan. 30, 2009	

Examiner Signature	/Jeremy Norris/	Date Considered	02/25/2013
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
 This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.N./

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/990,785	11/03/2010	Petteri Palm	IMB 22 US

CONFIRMATION NO. 3345

95002
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

PUBLICATION NOTICE



OC000000046621377

Title:CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Publication No.US-2011-0061909-A1

Publication Date:03/17/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/990,785	11/03/2010		1760	IMB 22 US	35	2

CONFIRMATION NO. 3345

FILING RECEIPT



OC00000044706311*

95002
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Date Mailed: 12/07/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Petteri Palm, Helsinki, FINLAND;
Risto Tuominen, Espoo, FINLAND;
Antti Iihola, Helsinki, FINLAND;

Assignment For Published Patent Application

IMBERA ELECTRONICS OY, Espoo, FI

Power of Attorney: The patent practitioners associated with Customer Number 95002

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/FI09/50383 05/11/2009

Foreign Applications

FINLAND 20085443 05/12/2008

If Required, Foreign Filing License Granted: 11/28/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/990,785**

Projected Publication Date: 03/17/2011

Non-Publication Request: No

Early Publication Request: No

Title

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Preliminary Class**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 12/990,785	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	430
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	35	minus 20 = *	15			x 52 =	780
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
				TOTAL		TOTAL	1760
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/990,785	Petteri Palm	IMB 22 US

95002
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

INTERNATIONAL APPLICATION NO.	
PCT/FI09/50383	
I.A. FILING DATE	PRIORITY DATE
05/11/2009	05/12/2008

CONFIRMATION NO. 3345
371 ACCEPTANCE LETTER



Date Mailed: 12/07/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

11/03/2010
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1),
(c)(2) and (c)(4) REQUIREMENTS

11/03/2010
DATE OF COMPLETION OF ALL
35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363). Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 11/03/2010
- Copy of the International Search Report filed on 11/03/2010
- Preliminary Amendments filed on 11/03/2010
- Information Disclosure Statements filed on 11/03/2010
- Oath or Declaration filed on 11/03/2010
- Request for Immediate Examination filed on 11/03/2010
- U.S. Basic National Fees filed on 11/03/2010
- Priority Documents filed on 11/03/2010
- Power of Attorney filed on 11/03/2010
- Specification filed on 11/03/2010
- Claims filed on 11/03/2010
- Abstracts filed on 11/03/2010
- Drawings filed on 11/03/2010

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

TONI M HOOD

Telephone: (571) 272-3654

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 12/990,785	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
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MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
			TOTAL			TOTAL	1760
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
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AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE			TOTAL ADD'L FEE
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
12/990,785	Petteri Palm	IMB 22 US

95002
Seppo Laine Oy
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INTERNATIONAL APPLICATION NO.	
PCT/FI09/50383	
I.A. FILING DATE	PRIORITY DATE
05/11/2009	05/12/2008

CONFIRMATION NO. 3345
371 ACCEPTANCE LETTER



Date Mailed: 11/30/2010

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

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(c)(2) and (c)(4) REQUIREMENTS

11/03/2010
DATE OF COMPLETION OF ALL
35 U.S.C. 371 REQUIREMENTS

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- Drawings filed on 11/03/2010

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

TONI M HOOD

Telephone: (571) 272-3654



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/990,785	11/03/2010		1760	IMB 22 US	35	2

CONFIRMATION NO. 3345

FILING RECEIPT



OC00000044706311*

95002
Seppo Laine Oy
Joshua P. Wert
Itamerenkatu 3B
Helsinki, FI00180
FINLAND

Date Mailed: 11/30/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Risto Tuominen, Espoo, FINLAND;
Antti Iihola, Helsinki, FINLAND;

Assignment For Published Patent Application

IMBERA ELECTRONICS OY, Espoo, FI

Power of Attorney: The patent practitioners associated with Customer Number 95002

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/FI09/50383 05/11/2009

Foreign Applications

FINLAND 20085443 05/12/2008

If Required, Foreign Filing License Granted: 11/28/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/990,785**

Projected Publication Date: 371 Perfected

Non-Publication Request: No

Early Publication Request: No

Title

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Preliminary Class**PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES**

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET (FOR USE WITH FORM PTO-875)							SERIAL NO. <u>12/990785</u>		FILING DATE				
							APPLICANT(S)						
CLAIMS													
	AS FILED		AFTER 1 st AMENDMENT		AFTER 2 nd AMENDMENT			AS FILED		AFTER 1 st AMENDMENT		AFTER 2 nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.		IND.	DEP.	IND.	DEP.	IND.	DEP.
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100													
TOTAL IND.	2	↓	2	↓		↓	TOTAL IND.		↓		↓		↓
TOTAL DEP.	38	←	33	←		←	TOTAL DEP.		←		←		←
TOTAL CLAIMS	40		35				TOTAL CLAIMS						

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known		
		Application Number	12/990785	
		Filing Date	Nov. 5, 2009	
		First Named Inventor	PALM, Petteri	
		Art Unit		
		Examiner Name		
Sheet 1		of 1	Attorney Docket Number	IMB 22 US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Finnish Search Report of FI20085443, Jan. 30, 2009	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
 This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5 Appl. No. : 12/990,785
 Applicant : Petteri Palm et al.
 Filed : Nov. 3, 2010
 TC/AU : N/A
 Examiner : N/A
10 Attorney Docket No. : IMB 22 US

 MS Amendment
15 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

20

INFORMATION DISCLOSURE STATEMENT

Sir:

25 Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an
Information Disclosure Statement for consideration by the Examiner.

I. **LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION**

 The patents, publications, or other information submitted for consideration by
30 the Office are listed on the PTO-SB08(s) attached hereto.

II. **COPIES OF CITED DOCUMENTS**

 [X] Copies of all of the foreign patent documents and non-patent literature
are included.

35

 [] Copies of all of the foreign patent documents and non-patent literature
are included except for the following for the corresponding indicated reasons:

40

III. CONCISE EXPLANATION OF THE RELEVANCE

[X] For Documents in the English language listed on the attached PTO-SB08(s) it is believed that no statement of relevancy is required.

5 [X] The following foreign language documents correspond to the indicated English language documents:

FI 20050645 corresponds to US 2008/0196930

Therefore, it is believed that this in conjunction with the indicated English language documents satisfies the relevancy requirement

10

[] An English language version of a search report or action that indicates the degree of relevance found by the foreign office is attached, it is believed that this satisfies the requirement for a concise explanation of the corresponding documents. See MPEP 609(III)(A)(3)

15

[] A concise explanation of foreign language documents not covered by an indication above is as follows:

IV. FEES

20 [] This Information Disclosure Statement is being filed concurrently with the filing of a new patent application or RCE, therefore no fee is required.

[X] This Information Disclosure Statement is being filed within three months of the date of entry of the national stage as set forth in §1.491 in an international application (37 C.F.R. §1.97(b)(2)), therefore no fee is required.

25

[] This Information Disclosure Statement is being filed before the mailing date of a Final Office Action under 37 C.F.R. §1.113 or before the mailing date of a Notice of Allowance under 37 C.F.R. §1.311.

30

[] a fee as required by 37 C.F.R. §1.17(p) is attached.

[] a statement is attached below and no fee is required

If the Examiner has any questions concerning this Information Disclosure statement they are requested to contact the undersigned. If it is determined that this Information Disclosure Statement has been filed under the wrong rule, the Office is requested to consider this statement under the proper rule.

5

Respectfully submitted,

/ Joshua P. Wert Reg. No. 65880/

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2010-11-09

Electronic Acknowledgement Receipt	
EFS ID:	8795792
Application Number:	12990785
International Application Number:	
Confirmation Number:	3345
Title of Invention:	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert
Filer Authorized By:	
Attorney Docket Number:	IMB 22 US
Receipt Date:	09-NOV-2010
Filing Date:	
Time Stamp:	07:24:15
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Foreign Reference	FI20050645.pdf	1320561	no	41
			2a49a9ccc14f71d22a9475572966f164a763f65a		

Warnings:

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Information:

2	NPL Documents	IMB22_FI-search_report_20090130.pdf	104045 bd722defcc208dbcec7ffa84f70bd44ba5aa1454	no	1
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Warnings:

Information:

3	Information Disclosure Statement (IDS) Filed (SB/08)	IMB22US_20101109_IDS.pdf	343816 48c87ed23b3ff70c38f65fc2ce88d5d097e7e466	no	3
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4	Transmittal Letter	IMB22US_IDS_Submission.pdf	57542 2bc0948e45460d4ebcda14a9443159a084ab3d46	no	3
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Information:

Total Files Size (in bytes):	1825964
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



SUOMI – FINLAND
(FI)

PATENTTI- JA REKISTERIHALLITUS
PATENT- OCH REGISTERSTYRELSEN

[A] TIIVISTELMÄ - SAMMANDRAG

(11) (21) Patenttihakemus - Patentansökan 20050645

(51) Kv.lk. - Int.kl.

H05K 1/00 (2006.01)

H01L 21/60 (2006.01)

H05K 3/46 (2006.01)

(22) Hakemispäivä - Ansökningsdag 16.06.2005

(24) Alkupäivä - Löpdag 16.06.2005

(41) Tullut julkiseksi - Blivit offentlig 05.04.2007

(71) Hakija - Sökande

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2 •Iihola,Antti, Takomatie 14 A 6, 00380 Helsinki, SUOMI - FINLAND, (FI)

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(74) Asiamies - Ombud: Seppo Laine Oy
Itämerenkatu 3 B, 00180 Helsinki

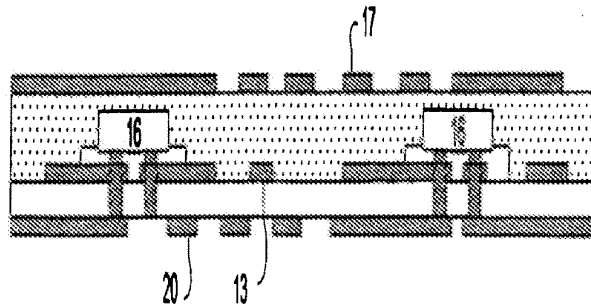
(54) Keksinnön nimitys - Uppfinningens benämning

**Menetelmä piirilevyrakenteen valmistamiseksi ja piirilevyrakenteen
Förfarande för tillverkning av kretskortskonstruktion och kretskortskonstruktion**

(57) Tiivistelmä - Sammandrag

Tässä julkaisussa on kuvattu menetelmä piirilevyrakenteen valmistamiseksi. Menetelmän mukaan valmistetaan johdekuvio (13) ja tähän kontaktiaukkoja komponentin (16) sähköisiä kontakteja varten. Tämän jälkeen komponentti (16) kiinnitetään johdekuvion (13) suhteen siten, että komponentin kontaktialueet tai kontaktinystyt tulevat kontaktiaukkojen kanssa kohdakkain. Tämän jälkeen kontaktiaukkoihin tuodaan sähköäjohtavaa materiaalia sähköisten kontaktien muodostamiseksi johdekuvion (13) ja komponentin (16) välille.

I denna publikation är beskrivet ett förfarande för tillverkning av en kretskortsstruktur. I enlighet med förfarandet bildas ett ledarmönster (13) och i detsamma kontaktöppningar för en komponents (16) elektriska kontakter. Härfter fästs komponenten (16) i förhållande till ledarmönstret (13) på så sätt, att komponentens kontaktområden eller kontaktknottor kommer att ligga mot kontaktöppningarna. Härfter bringas ett elledande material till kontaktöppningarna för att bilda elektriska kontakter mellan ledarmönstret (13) och komponenten (16).



Menetelmä piirilevyrakenteen valmistamiseksi ja piirilevyrakenne

Keksinnön kohteena menetelmä piirilevyrakenteen valmistamiseksi.

5 Valmistettu piirilevyrakenne voi muodostaa osan esimerkiksi piirilevystä, monikerros-piirilevystä, komponenttipakettista tai elektroniikkamoduulista.

Piirilevyrakenne voi olla tyyppiä, joka käsittää ainakin yhden kerroksen johdekuvioita sekä ainakin yhden komponentin, joka on liitetty sähköisesti johdekuvioihin.

10 Piirilevyrakenne voi olla myös tyyppiä, joka käsittää ainakin johdekuvioita ainakin kahdessa kerroksessa sekä ainakin yhden läpiviennin, joka liittää yhdessä kerroksessa olevan johteen sähköisesti toisessa kerroksessa olevaan johteeseen.

15 Keksinnön kohteena ovat siis monikerrospiirilevyjen valmistusmenetelmät. Keksinnön kohteena ovat myös sellaiset piirilevyjen valmistusmenetelmät, joissa ainakin yksi johdekuvioon yhdistetty komponentti ympäröidään eristemateriaalikerroksella. Tällaisia ratkaisuja voidaan kutsua vaihtoehtoisesti myös piirilevy- tai moduulirakenteiksi, jotka sisältävät haudattuja, upotettuja tai sisäänrakennettuja komponentteja (buried, embedded, built-in). Komponentin ympäröivä eristemateriaalikerros on tyypillisesti osa piirilevy- tai moduulirakenteen perusrakennetta, joka muodostaa tuen piirilevyn tai moduulin sisimmille johdekerroksille.

20 Hakemusjulkaisussa US 2005/0001331 on kuvattu piirilevyrakenteen valmistusmenetelmä, jossa ensin valmistetaan piirilevy, joka käsittää eristekerroksen ja tämän pinnalla olevan johdekuvion. Tämän jälkeen piirilevyn pinnalla oleviin johdekuvioihin liitetään puolijohdekomponentti soveltuvalla flip-chip-liitosmenetelmällä. Liitos tapahtuu puolijohdekomponentin pinnalla olevien kontaktinystyjen välityksellä. Komponentin liittämisen jälkeen US-julkaisun menetelmässä piirilevyn päälle
25 laminoidaan kuvioitu ja kuvioimaton eristemateriaalikerros sekä näiden pinnalle vielä johdekuviokerros.

Patenttijulkaisuissa US 6,038,133 ja US 6,489,685 sekä hakemusjulkaisussa US 2002/0117743 on kuvattu menetelmiä, joissa irrotettavan kalvon pinnalle valmistetaan johdekuvio ja puolijohdekomponentti liitetään johdekuvioon flip-chip-

liitosmenetelmällä. Tämän jälkeen komponentti ympäröidään eristemateriaalikerroksella ja irrotettava kalvo poistetaan.

Edellä mainituissa julkaisuissa US 6,038,133 ja US 2002/0117743 on kuvattu myös menetelmiä, joissa komponentti liitetään flip-chip-liitosmenetelmällä johdekuvioiden sijasta yhtenäiseen johdekalvoon, josta muodostetaan johdekuvioita prosessin myöhemmässä vaiheessa. Vastaavanlaisia menetelmiä on esitetty myös esimerkiksi julkaisuissa US 5,042,145; WO 2004/077902; WO 2004/077903 ja WO 2005/020651.

Edellä mainittujen menetelmätyyppien lisäksi tunnetaan vielä monia muita menetelmiä, joilla voidaan valmistaa komponentteja sisältäviä piirilevyrakenteita. Komponentit voidaan esimerkiksi ensin sijoittaa eristemateriaalikerroksen sisään ja liittää sähköisesti johdekerrokseen vasta tämän jälkeen, kuten on kuvattu hakemusjulkaisussa WO 2004/089048. Hakemusjulkaisun WO 2004/089048 menetelmässä komponentti liimataan johdekerroksen pinnalle ja komponentin liimaamisen jälkeen johdekerroksen pinnalle muodostetaan tai kiinnitetään eristemateriaalikerros, joka ympäröi johdekerrokseen liitetyn komponentin. Komponentin liimaamisen jälkeen valmistetaan myös läpiviennit, joiden kautta voidaan muodostaa sähköiset kontaktit johdekerroksen ja komponentin kontaktialueiden välille. Tämän jälkeen johdekerroksesta, jonka pinnalle komponentti liimattiin, muodostetaan johdekuvioita.

Liitettäessä komponentti yhtenäisen johdekalvon sijasta johdekuviioon saavutetaan se etu, että johdekuvio voidaan tarkastaa esimerkiksi optisella menetelmällä ennen komponenttien liittämistä piirilevyaihioon. Mikäli valmistettavat piirilevyt tai moduulin sisältävät kalliita komponentteja, tällä johdekuviion etukäteistarkastuksella voidaan saavuttaa kustannusetua, koska viallinen johdekuvio voidaan korjata tai poistaa prosessista aikaisemmassa vaiheessa. Päinvastaisessa menettelyssä johdekalvoon liitetty ja piirilevyaihioon jo upotetut komponentit menetetään, mikäli johdekalvon kuviointi epäonnistuu.

Keksinnön tarkoituksena on kehittää uusi menetelmä piirilevyrakenteen valmistamiseksi.

Keksinnön ensimmäisen näkökohdan mukaan piirilevyaihioon valmistetaan johdekuvio sekä kontaktiaukkoja läpivientien valmistamista varten. Tämän jälkeen johdekuviion pinnalle valmistetaan eristemateriaalikerros. Eristemateriaalikerrokseen kontakti-

aukkojen osoittamille kohdille valmistetaan reikiä, jotka ulottuvat eristemateriaalikerroksen sisällä tai vastakkaisella pinnalla olevaan toiseen johderakentecseen saakka. Tämän jälkeen reikiin tuodaan johdemateriaalia sähköisten kontaktien muodostamiseksi johdekuvion ja toisen johderakenteen välille. Toinen johderakenne voi olla esimerkiksi johdekuvio tai komponentin kontaktialue tai kontaktinysty.

Keksinnön toisen näkökohdan mukaan piirilevyaihioon valmistetaan johdekuvio sekä kontaktiaukkoja läpivientien valmistamista varten. Tämän jälkeen johdekuvion pinnalle valmistetaan eristemateriaalikerros sekä tämän pinnalle johdekerros tai johdekuviokerros. Eristemateriaalikerrokseen kontaktiaukkojen osoittamille kohdille valmistetaan reikiä, jotka ulottuvat eristekerroksen läpi johdekerrokseen tai johdekuviokerrokseen saakka. Tämän jälkeen reikiin tuodaan johdemateriaalia sähköisten kontaktien muodostamiseksi eristemateriaalikerroksen vastakkaisilla pinnoilla olevien johteiden välille.

Keksinnön kolmannen näkökohdan mukaan piirilevyaihioon valmistetaan johdekuvio, johon valmistetaan kontaktiaukot liitettävien komponenttien kontaktialueiden kohdille. Komponentti liitetään johdekuvioon ja muodostetaan sähköiset kontaktit komponentin kontaktialueiden ja johdekuvion välille johdekuvioon valmistettujen kontaktiaukkojen kautta.

Yhdessä sovellusmuodossa valmistetaan ensin johdekuvio ja tämän jälkeen johdekuvioon kontaktiaukot. Kontaktiaukkojen valmistamisen jälkeen komponentti kohdistetaan johdekuvion suhteen siten, että komponentin kontaktialueet tai kontaktinystyt tulevat kohdakkain kontaktiaukkojen kanssa.

Toisessa sovellusmuodossa valmistetaan yhtäaikaaisesti sekä johdekuvio että tähän tulevat kontaktiaukot. Johdekuvion valmistamisen jälkeen komponentti kohdistetaan johdekuvion suhteen siten, että komponentin kontaktialueet tai kontaktinystyt tulevat kohdakkain kontaktiaukkojen kanssa.

Kolmannessa sovellusmuodossa valmistetaan ensin johdekuvio ja johdekuvion valmistamisen jälkeen komponentti kohdistetaan johdekuvion suhteen ja kiinnitetään paikoilleen. Komponentin kiinnittämisen jälkeen valmistetaan johdekuvioon kontaktiaukot siten, että komponentin kontaktialueet tai kontaktinystyt tulevat kohdakkain kontaktiaukkojen kanssa.

Keksinnön neljännen näkökohdan mukaan tuodaan esiin piirilevyrakenne, joka on valmistettu keksinnön ensimmäisen, toisen tai kolmannen näkökohdan mukaisella menetelmällä.

- 5 Keksinnön viidennen näkökohdan mukaan tuodaan esiin piirilevyrakenne, joka käsittää johdekuviokerroksessa johteen sekä johteeseen liittyvän läpiviennin, joka yhdistää johteen toiseen johdekuviokerrokseen tai komponenttiin siten, että läpiviennin läpimitta on oleellisesti yhtä suuri tai suurempi kuin johteen leveys.

Edellä mainituilla keksinnön näkökohdilla on lisäksi kullakin useita erilaisia sovellusmuotoja, joita kuvataan lähemmin seuraavassa sovellusmuotojen kuvauksessa.

- 10 Keksinnön joidenkin näkökohtien ja sovellusmuotojen avulla saadaan aikaan esimerkiksi valmistusmenetelmä, joka mahdollistaa johdekuvion tarkastamisen ennen komponenttien liittämistä piirilevyaihiin.

- 15 Keksinnön joidenkin näkökohtien ja sovellusmuotojen avulla saadaan lisäksi aikaan valmistusmenetelmä, joka mahdollistaa sähköisten kontaktien valmistamisen läpivientimenetelmällä. Sovellusmuodoissa, joissa läpivienti yhdistyy komponenttiin, tällä saavutetaan esimerkiksi se etu, että komponenttien kontaktialueiden (kuten kontaktinystyjen) pinta voidaan puhdistaa ennen sähköisen kontaktin muodostamista. Läpivientimenetelmä mahdollistaa myös kontaktien valmistamisen kemiallisen tai sähkökemiallisen kasvatusmenetelmän avulla, jolloin on mahdollista saavuttaa
20 johdekuvion ja komponentin väliselle kontaktille erinomaiset sähköiset ominaisuudet. Läpivientimenetelmän yhteydessä voidaan käyttää myös muuta pinnoitusmenetelmää. Pinnoitusmenetelmänä voidaan käyttää esimerkiksi sputterointia, höyrystystä, kemiallista tai sähkökemiallista pinnoitusta tai jotain muuta soveltuvaa pinnoitusmenetelmää tai pinnoitusmenetelmien yhdistelmää.

- 25 Joidenkin sovellusmuotojen mukaan myös läpivientien kohdistus voidaan tarkastaa ennen komponenttien liittämistä tai piirilevyrakenteen valmistusprosessin jatkamista.

Sovellusmuodoissa, joissa kontaktiaukkojen valmistaminen suoritetaan itsekohdistavalla menetelmällä, läpiviennit tulevat automaattisesti oikealle kohdalle ainakin sen johdekuviokerroksen suhteen, johon kontaktiaukot valmistetaan.

- 30 Keksintöä tarkastellaan seuraavassa esimerkkien avulla ja oheisiin piirustuksiin viitaten.

Kuviot 1-14 esittävät poikkileikkauskuvasarjana piirilevyrakenteiden välivaiheita ensimmäisen suoritusesimerkin mukaisessa valmistusprosessissa.

Kuviot 15-23 esittävät poikkileikkauskuvasarjana piirilevyrakenteiden välivaiheita toisen suoritusesimerkin mukaisessa valmistusprosessissa.

- 5 Kuviot 24-32 esittävät poikkileikkauskuvasarjana piirilevyrakenteiden välivaiheita kolmannen suoritusesimerkin mukaisessa valmistusprosessissa.

Kuviot 33-42 esittävät poikkileikkauskuvasarjana piirilevyrakenteiden välivaiheita neljännen suoritusesimerkin mukaisessa valmistusprosessissa.

- 10 Kuvion 43-49 esittävät lähemmin läpivientien mitoittamista ja kohdistamista joissakin sovellusmuodoissa.

- Ensimmäisessä esimerkissä valmistus aloitetaan kuvion 1 mukaisesti tukikerroksesta 1, joka on ainakin yhdeltä pinnaltaan sähköä johtava. Kuviosarjan mukaisesti asemoituna ainakin tukikerroksen 1 yläpinta on johtava. Johtavuusominaisuutta tarvitaan tämän esimerkin mukaisen menetelmän myöhemmässä vaiheessa johtamaan elektrolyyttisen kasvatuksen tarvitsema virta alueelle, jolle kasvatetaan johdemateriaalia. Menetelmässä, jossa johdemateriaalin elektrolyyttinen kasvatus korvataan jollakin toisella valmistusmenetelmällä, tukikerroksen 1 johtavuusominaisuutta ei välttämättä tarvita, jolloin tukikerros 1 voi olla myös johtamaton. Kuvioiden esimerkissä tukikerros 1 on kuitenkin kauttaaltaan valmistettu johtavasta materiaalista, tyypillisesti metallista ja tavallisimmin kuparista. Tukikerroksen 1 tehtävänä on tarjota mekaaninen tuki piirilevyaihiolle, joten tukikerroksella 1 on oltava käsittelyyn tarvittava mekaaninen kestävyys ja jäykkyys. Kuparilevyn tapauksessa nämä ominaisuudet saavutetaan valitsemalla tukikerroksen 1 paksuudeksi esimerkiksi yli 50 mikrometriä.
- 15
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- Tämän jälkeen tukikerroksen 1 molemmille pinnoille levitetään resistikerrokset 2, tyypillisesti valoresistikerrokset. Tämä vaihe on kuvattu kuviossa 2. Valoresistikerros 2 valotetaan kuvioidun maskin läpi tukikerroksen 1 yhdeltä pinnalta ja tämän jälkeen aihio kehitetään. Kehittämisen jälkeen valotettu valoresistikerros 2 on kuvioitunut halutulla tavalla johdekuviomaskiksi, mitä on kuvattu kuviossa 3.
- 25

- Valmistusta jatketaan kasvattamalla elektrolyyttisesti johdemateriaalia, tyypillisesti kuparia, alueille, joilta valoresisti poistettiin. Tällöin tukikerroksen 1 pinnalle
- 30

muodostuu haluttu johdekuvio 3, joka on esitetty kuviossa 4. Johdekuvion paksuus voi olla esimerkiksi 20 mikrometriä ja myös valmistettavien johdekuvioiden viivanleveys voi olla alle 20 mikrometriä. Menetelmällä voidaan siis valmistaa myös pieniä ja tarkkoja johdekuvioita. Johdekuvioista 3 voidaan myös valmistaa paksuja suhteessa

5 johdekuvioiden leveyteen, jolloin saavutetaan hyvät johtavuusominaisuudet pienellä piirilevyrakenteen pinta-alan käytöllä. Johdekuvion 3 paksuus voi siis olla esimerkiksi oleellisesti yhtä suuri kuin leveys tai paksuus (korkeus) voi olla suurempi, esimerkiksi noin 1,2–3 kertaa suurempi kuin leveys.

Johdekuviot 3 voidaan valmistaa myös jollakin muulla kuin edellä kuvatulla

10 menetelmällä. Soveltuvia menetelmiä ovat esimerkiksi yhtenäisen johdekerroksen valmistaminen ja kuvioiminen esimerkiksi syövyttämällä tai laser-ablaatiolla.

Johdekuvioiden 3 valmistamisen jälkeen resistikerrokset 2 poistetaan. Kuvio 5 esittää piirilevyaihion resistikerrosten 2 poistamisen jälkeen. Tämän jälkeen, ennen komponentin 6 liittämistä piirilevyaihioon, johdekuvioon 3 valmistetaan kontaktiaukot

15 4 liitettävän komponentin 6 kontaktialueiden kohdalle. Kuvio 6 esittää piirilevyaihion tämän välivaiheen jälkeen. Kontaktiaukot 4 voidaan valmistaa esimerkiksi poraamalla laserin avulla. Kontaktiaukkojen 4 keskinäinen sijainti valitaan komponentin kontaktialueiden keskinäisen sijainnin mukaan ja kunkin kontaktiaukkoryhmän sijainti ja asema valitaan siten, että komponentti tulee sijoitetuksi oikein suhteessa koko

20 piirilevyrakenteeseen. Kutakin sähköisen kontaktin muodostamiseen osallistuvaa kontaktialuetta kohti valmistetaan siis yksi kontaktiaukko 4. Valmistettavien kontaktiaukkojen 4 pinta-ala voi olla jotakuinkin yhtä suuri kuin vastaavan kontaktialueen pinta-ala. Kontaktiaukon 4 pinta-ala voidaan toki valita myös pienemmäksi tai joissakin sovellusmuodoissa hieman suuremmaksi kuin vastaavan

25 kontaktialueen pinta-ala.

Kontaktiaukot 4 voidaan porata johdekuvion 3 tai tukikerroksen 1 suunnasta. Mikäli kontaktiaukot 4 porataan johdekuvion 3 suunnasta, porattavien aukkojen ei välttämättä tarvitse läpäistä kokonaan tukikerrosta 1. Tällaisessa sovellusmuodossa kontaktiaukot 4 avautuvat myöhemmin, kun tukikerros 1 irrotetaan. Kontaktiaukot 4 voidaan avata

30 myös siten, että johdekuvion 3 ja tukikerroksen 1 muodostamaa materiaalikerrosta ohennetaan etsaamalla tukikerroksen 1 suunnasta. Johdekuvio 3 ja tukikerros 1 voivat muodostua myös yhdestä materiaalikerroksesta. Tällöin tukikerrosta 1 vastaava osa

materiaalikerroksesta poistuu ja kontaktiaukot 4 avautuvat. Kontaktiaukon 4 on siis tarkoitus ulottua läpi koko johdekuvion 3. Poraus voidaan toteuttaa esimerkiksi mekaanisesti tai laserin avulla. Kontaktiaukot 4 on mahdollista valmistaa myös esimerkiksi plasmaetsauksen avulla.

- 5 Kontaktiaukot 4 voidaan myös suunnitella resistimaskiin, jolloin aukot 4 syntyvät johdekuvioon 3 tämän valmistamisen yhteydessä ja avautuvat, kun tukikerros 1 poistetaan.

- On myös mahdollista menetellä siten, että kontaktiaukot 4 valmistetaan vasta komponentin 6 liimaamisen jälkeen. Tällöin komponentti voidaan kohdistaa paikoilleen
 10 johdekuvion 3 avulla ja kontaktiaukot 4 valmistaan myös johdekuvion suhteen kohdistettuina. Myös tällä tavalla komponentin kontaktialueet tai kontaktinystyt tulevat kohdistetuiksi kontaktiaukkojen 4 suhteen. Tällaisessa sovellusmuodossa kontaktiaukot 4 valmistetaan johdekuvion 3 vastakkaisen pinnan suunnasta verrattuna johdekuvion 3 siihen pintaan, jonka suunnasta komponentti 6 liimataan. Viitaten kuvioon 6 voidaan
 15 mainita, että kontaktiaukot 4 voidaan valmistaa joko johdekuvion 3 suunnasta tai tukikerroksen 1 suunnasta. Kontaktiaukot 4 voivat ulottua molempien kerrosten 1 ja 3 läpi tai vaihtoehtoisesti muodostaa syvennyksen, joka ulottuu johdekuvion 3 läpi. On myös mahdollista valmistaa kontaktiaukot 4 vaiheittain siten, että ensin valmistetaan tukikerroksen 1 suunnasta syvennys, joka ei vielä ainakaan kokonaan läpäise
 20 johdekuviota 3, ja prosessin myöhemmässä vaiheessa kontaktiaukko 4 avataan läpäisemään johdekuvio 3. Esimerkin menetelmää voidaan modifioida myös siten, että komponentti 6 liimataan tukikerroksen 1 pinnalle ja sähköinen kontakti johdekuvion 3 ja komponentin välillä valmistetaan tukikerroksen 1 läpi. Tällöin tukikerros 1 on eristävä. Esimerkin menetelmää voidaan modifioida myös siten, että komponentti 6
 25 liimataan johtavan tukikerroksen 1 pinnalle ja tukikerroksen 1 johdemateriaali poistetaan johdekuvioiden 3 välisiltä alueilta.

- Komponentit 6 kiinnitetään johdekuvion 3 pinnalle liiman avulla. Liimaamista varten johdekuvion 3 liitospinnalle tai komponentin 6 liitospinnalle tai molemmille liitospinnoille levitetään liimakerros 5. Liima 5 voidaan levittää myös vaiheittain ja
 30 kerroksittain. Tämän jälkeen komponentit 6 voidaan kohdistaa komponenteille 6 suunniteltuihin asemiin kohdistusmerkkien avulla. Kuvio 8 esittää piirilevyaihion komponenttien 6 liimaamisen jälkeen.

Komponentin 6 liitospinnalla tarkoitetaan komponentin 6 sitä pintaa, joka tulee johdekuviota 3 kohti. Komponentin 6 liitospinta käsittää kontaktialueita, joiden välityksellä komponenttiin voidaan muodostaa sähköinen kontakti. Kontaktialueet voivat olla esimerkiksi komponentin 6 pinnalla olevia tasomaisia alueita tai tavallisemmin komponentin 6 pinnasta ulkonevia kontaktiulokkeita, kuten kontaktinystyjä. Kontaktialueita tai -ulokkeita on komponentissa 6 yleensä vähintään kaksi. Monimutkaisissa mikropiireissä kontaktialueita voi olla hyvinkin monta.

Monissa sovellusmuodoissa on edullista levittää liitospinnalle tai liitospinnoille liimaa niin runsaasti, että liima täyttää kauttaaltaan komponenttien 6 ja johdekuvion 3 sekä tukikerroksen 1 väliin jäävän tilan. Tällöin ei tarvita erillistä täyteainetta. Komponenttien 6 ja johdekuvion 3 sekä tukikerroksen 1 väliin jäävän tilan täyttyminen vahvistaa komponentin 6 ja johdekuvion 3 välistä mekaanista kytkentää, jolloin saavutetaan mekaanisesti kestävämpi rakenne. Kattava ja aukoton liimakerros myös tukee johdekuviota 3 ja suojaa rakennetta myöhemmissä prosessivaiheissa. Liimaamisen yhteydessä liimaa joutuu yleensä myös kontaktiaukkoihin 4.

Liimalla tarkoitetaan materiaalia, jolla komponentit voidaan kiinnittää johdekuvioon 3 ja tukikerrokseen 1. Liiman yksi ominaisuus on se, että liima voidaan levittää johdekuvion 3, tukikerroksen 1 ja/tai komponentin pinnalle suhteellisen juoksevassa tai muutoin pinnanmuotoihin mukautuvassa muodossa, esimerkiksi kalvon muodossa. Liiman toinen ominaisuus on se, että levittämisen jälkeen liima kovettuu tai voidaan kovettaa ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan (johdekuvion 3 suhteen) ainakin niin kauan kunnes komponentti kiinnitetään rakenteeseen jollakin muulla tavalla. Liiman kolmas ominaisuus on adheesiokyky eli kyky tarttua liimattavaa pintaan.

Liimaamisella tarkoitetaan komponentin ja johdekuvion 3 tai tukikerroksen kiinnittämistä toisiinsa liiman avulla. Liimattaessa siis liimaa tuodaan komponentin ja johdekuvion 3 ja/tai tukikerroksen 1 väliin ja asetetaan komponentti johdekuvion 3 suhteen sopivaan asemaan, jossa liima on kosketuksessa komponentin ja johdekuvion 3 ja/tai tukikerroksen 1 kanssa ja ainakin osittain täyttää komponentin ja piirilevyaihion välisen tilan. Tämän jälkeen liiman annetaan (ainakin osittain) kovettua tai liima aktiivisesti kovetetaan (ainakin osittain) siten, että komponentti kiinnittyy liiman avulla

piirilevyaihioon. Joissakin sovellusmuodoissa komponentin kontaktiulokkeet saattavat liimauksen aikana työntyä liimakerroksen läpi kosketukseen johdekuvion 3 kanssa.

Sovellusmuodoissa käytettävä liima on esimerkiksi lämpökovetteinen epoksi. Liima valitaan siten, että käytettävällä liimalla on riittävä adheesio piirilevyaihioon ja komponenttiin. Yksi edullinen liiman ominaisuus on sopiva lämpölaajenemiskerroin, jolloin liiman lämpölaajeneminen ei poikkea liian paljon ympäröivän materiaalin lämpölaajenemisesta prosessin aikana. Valittavalla liimalla tulisi myös mielellään olla lyhyt kovetus aika, mielellään korkeintaan muutamia sekunteja. Tässä ajassa liiman tulisi kovettua ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan. Lopullinen kovettuminen voi viedä selvästi enemmän aikaa ja loppukovetus voidaan suunnitella tapahtuvaksi myöhempien prosessivaiheiden yhteydessä. Liiman sähkönjohtavuus on mielellään eristemateriaalien sähkönjohtavuuden luokkaa.

Liitettävä komponentti 6 voi olla esimerkiksi integroitu piiri, kuten muistisiru, prosessori tai ASIC. Liitettävä komponentti voi olla myös esimerkiksi MEMS, LED tai passiivikomponentti. Liitettävä komponentti voi olla koteloitu tai koteloimaton ja se voi käsittää kontaktialueillaan kontaktinystyt tai olla nystytön. Komponentin kontaktialueiden pinnalla voi olla myös kontaktinystyä ohuempi johdepinnoite. Komponentin kontaktialueiden ulkopinta voi siis olla komponentin ulkopinnan tasalla, komponentin pinnassa olevien syvennysten pohjalla tai komponentin pinnasta esiin tulevien ulokkeiden pinnalla.

Komponenttien 6 liimaamisen jälkeen valmistetaan eristekerros 10, joka ympäröi komponentit 6 ja tukee johdekuvioita 3. Kuvion 9 esimerkissä eristekerros 10 muodostetaan tuomalla piirilevyaihion päälle eristemateriaalilevy 8, johon on tehty aukot komponenttien 6 kohdalle. Lisäksi eristemateriaalilevyn 8 päälle tuodaan yhtenäinen eristemateriaalilevy 9. Molemmat levyt voivat olla samanlaisia tai voidaan käyttää myös keskenään erilaisia levyjä, joista ainakin yksi on esikovetettu tai kovettamaton. Esimerkkejä soveltuvista eristekerroksen 10 materiaaleista ovat PI (polyimidi), FR4, FR5, aramidi, polytetrafluorieteeni, Teflon®, LCP (liquid crystal polymer) ja esikovetettu sidoskerros eli prepregi. Eristekerros voidaan siis levittää myös juoksevassa tai nestemäisessä muodossa.

Piirilevyaihion päälle tuodut eristemateriaalilevyt 8 ja 9 prässätään lämmön ja paineen avulla yhtenäiseksi eristekerrokseksi 10. Kuvio 10 esittää piirilevyaihion poikkileikkauksen tämän välivaiheen jälkeen. Eristemateriaalilevyissä, esimerkiksi levyn 9 yläpinnalla, voi olla myös valmiina johdekuviokerros, jolloin prässäyksen jälkeen piirilevyaihio käsittää vähintään kaksi johdekuviokerrosta. Eristekerroksen 10 valmistamisen jälkeen tukikerros 1 voidaan poistaa, jolloin saadaan aikaan kuvion 11 esittämä rakenne. Tukikerroksen 1 poistaminen voidaan suorittaa esimerkiksi syövyttämällä tai mekaanisesti.

Sovellusmuodossa, jossa tukikerros 1 ja johdekuviot 3 ovat samaa materiaalia, esimerkiksi kuparia, ja tukikerros 1 poistetaan syövyttämällä, johdekuvioiden 3 tukikerroksen 1 puoleinen rajapinta saadaan valmistettua tarkemmin, mikäli johdekuvioiden 3 ja tukikerroksen 1 välissä käytetään sopivaa välikerrosta, joka ei liukene käytettyyn etsiin tai liukenee tähän huomattavan hitaasti. Tällöin etsaus pysähtyy välikerrokseen ja johdekuvioiden 3 pinta saadaan määriteltyä tarkasti. Tällainen välikerros voidaan valmistaa esimerkiksi jostakin toisesta metallista. Välikerros voidaan valmistaa esimerkiksi koko tukikerroksen 1 pinnalle ennen johdekuvioiden 3 valmistamista ja poistaa tukikerroksen 1 poistamisen jälkeen esimerkiksi kemiallisesti jollakin toisella etsillä. On myös mahdollista valmistaa välikerros johdekuvioiden 3 kasvattamisen yhteydessä siten, että ensin kasvatetaan tukikerroksen 1 päälle välikerroksen materiaali ja sen välikerroksen materiaalin päälle itse johdekuviot 3. Tällaisessa sovellusmuodossa välikerros valmistetaan siis ainoastaan johdekuvioiden kohdalle, jolloin voidaan säästää välikerroksen materiaalia.

Seuraavaksi piirilevyaihioon valmistetaan läpiviennit, joiden avulla voidaan muodostaa sähköiset kontaktit komponenttien 6 kontaktialueiden 7 ja johdekuvioiden 3 välille. Läpivientien valmistamista varten kontaktiaukot 4 puhdistetaan aukkoihin mahdollisesti työntyneestä liimasta ja muusta materiaalista. Kontaktiaukkojen 4 puhdistamisen yhteydessä on mahdollista puhdistaa myös komponenttien 6 kontaktialueet 7, jolloin edellytykset korkealaatuisen sähköisen kontaktin valmistamiselle edelleen paranevat. Puhdistaminen voidaan suorittaa esimerkiksi plasmatekniikalla, kemiallisesti tai laserin avulla. Kuvion 12 esittää piirilevyaihion kontaktiaukkojen 4 ja kontaktialueiden 7 puhdistamisen jälkeen. Mikäli kontaktiaukot 4 ja kontaktialueet ovat valmiiksi riittävän puhtaat, puhdistaminen voidaan luonnollisesti jättää suorittamatta.

Puhdistamisen jälkeen on mahdollista myös tarkastaa komponentin 6 kohdistamisen onnistuminen, sillä oikein kohdistetun komponentin kontaktialueet 7 näkyvät kontaktiaukkojen 4 läpi johdekuvion suunnasta katsottaessa. Tarkastus voidaan toki tehdä monessa muussakin vaiheessa.

- 5 Tämän jälkeen kontaktiaukkoihin 4 tuodaan johdemateriaalia siten, että muodostuu sähköinen kontakti komponenttien 6 ja johdekuvion 3 välille. Johdemateriaali voidaan valmistaa esimerkiksi täyttämällä kontaktiaukot sähköä johtavalla pastalla. Johdemateriaali voidaan valmistaa myös jollakin useista piirilevyteollisuudessa tunnetuista kasvatusmenetelmistä. Hyvälaatuiset sähköiset kontaktit voidaan valmistaa esimerkiksi
- 10 muodostamalla metallurginen liitos kasvattamalla johdemateriaali kemiallisella tai sähkökemiallisella menetelmällä. Yksi hyvä vaihtoehto on ohuen kerroksen kasvattaminen kemiallisella menetelmällä ja kasvatuksen jatkaminen edullisemmalla sähkökemiallisella menetelmällä. Näiden menetelmien lisäksi voidaan toki käyttää myös jotakin muuta menetelmää, josta on hyötyä lopputuloksen kannalta.
- 15 Kuviosarjan esimerkissä kontaktiaukot 4, kontaktialueet 7, johdekuviot 3 sekä eristekerroksen 10 johdekuvioiden 3 väliin jäävä paljas pinta pinnoitetaan ensiksi ohuella johdekerroksella ja sen jälkeen johdekerroksen paksuutta kasvatetaan elektrolyytisesti kunnes kontaktiaukot 4 ovat täyttyneet johdemateriaalilla. Kuvio 13 kuvaa rakennetta kasvatuksen jälkeen. Tämän jälkeen piirilevyaihiota etsataan
- 20 ylimääräisen johdemateriaalin poistamiseksi. Kuvio 14 esittää piirilevyrakenteen etsauksen jälkeen.

- Kuviot 15–23 esittävät toisen esimerkin piirilevyrakenteen valmistamisesta. Kuvio 15 esittää kerroslevyn, joka käsittää tukikerroksen 11 ja johdekerroksen 12. Tukikerros 11 on tässä sovellusmuodossa sähköisesti eristävää materiaalia. Tukikerros 11 voi olla
- 25 esimerkiksi FR4 -levy tai sisältää jotakin muuta edellä eristekerroksen 10 yhteydessä mainittua materiaalia. Myös muita soveltuvia materiaaleja voidaan toki käyttää tukikerroksessa 11. Johdekerros 12 on tavallisimmin kuparia.

- Johdekerros 12 kuvioidaan johdekuvioiksi 13 esimerkiksi syövyttämällä. Tämä välivaihe on esitetty kuviossa 16. Seuraavaksi johdekuvioiden 13 ja tukikerroksen 11
- 30 läpi valmistetaan kontaktiaukot 14 liitettävien komponenttien 16 kontaktialueiden kohdille. Kontaktiaukot 14 valmistetaan samaan tapaan kuin edellä on kuvautut

kontaktiaukot 4. Kuvio 17 esittää piirilevyaihion kontaktiaukkojen 14 valmistamisen jälkeen.

Kontaktiaukkojen 14 valmistamisen jälkeen piirilevyaihiole levitetään liima 15 samaan tapaan kuin edellä on kuvattu liiman 5 yhteydessä. Kuvio 18 esittää piirilevyaihion liiman 15 kanssa. Tämän jälkeen komponentit 16 liimataan paikoilleen samaan tapaan kuin komponentit 6, jolloin päädytään kuvion 19 esittämään rakenteeseen. Tämän jälkeen piirilevyaihioon kiinnitetään eristemateriaalilevyjen 8 ja 9 tapaan eristemateriaalilevyt 18 ja 19. Tässä esimerkissä eristemateriaalilevyn 19 pinnalle kiinnitetään myös johdekerros 17. Kuvio 20 esittää tätä välivaihetta. Tämän jälkeen kontaktiaukot 14 ja komponenttien 16 kontaktialueet puhdistetaan. Kuvio 21 esittää piirilevyaihion tämän välivaiheen jälkeen.

Seuraavaksi muodostetaan sähköiset kontaktit komponentteihin 16. Myös tämä voidaan tehdä edellä esitettyyn tapaan esimerkiksi täyttämällä kontaktiaukot johdepastalla. Tällöin saavutetaan etuna lyhyt ja yksinkertainen valmistusprosessin. Tässä esimerkissä johdemateriaali kuitenkin kasvatetaan valmistamalla ohut pinnoite ja lisäämällä johdemateriaalin paksuutta elektrolyyttisellä kasvatuksella siten, että kontaktiaukot 14 täyttyvät. Samalla piirilevyaihioon kasvatetaan kolmas johdekerros 20, joka tulee myös sähköiseen kontaktiin komponenttien 16 kanssa. Kuvio 22 esittää piirilevyaihion tämän välivaiheen jälkeen.

Seuraavaksi johdekerrokset 17 ja 20 voidaan kuvioda esimerkiksi syövyttämällä, jolloin johdekerroksista 17 ja 20 saadaan valmistettua johdekuviot. Kuvio 23 esittää piirilevyn kuvioinnin jälkeen. Kuten kuviosta 23 voidaan havaita, komponenttien 16 kontaktialueet voidaan tämän valmistusmenetelmän avulla vapaavalintaisesti yhdistää joko johdekuviokerrokseen 13 tai johdekuviokerrokseen 20. Kontakti voidaan muodostaa yhtäaikaaisesti myös molempiin johdekuviokerroksiin 13 ja 20. Tämä ominaisuus tarjoaa mahdollisuuksia komponenttien 16 kontaktien joustavaan suunnitteluun ja tehokkaaseen tilankäyttöön piirilevyrakenteessa.

Kuviot 24–32 esittävät kolmannen esimerkin piirilevyrakenteen valmistamisesta. Tässä esimerkissä valmistus aloitetaan kuvion 24 esittämästä kerroslevystä, joka käsittää eristemateriaalikerroksen 21, jonka ensimmäisellä pinnalla on johdekerros 22 ja toisella pinnalla johdekerros 23. Johdekerrokset 22 ja 23 ovat tyypillisesti kuparia.

Eristemateriaalikerroksen 21 materiaali on edellä esitetyn esimerkin kerroksen 10 tapaan esimerkiksi FR4 tai jokin muu soveltuva eristemateriaali.

Johdekerrokset 22 ja 23 kuviodaan johdekuvioiksi 24 ja 25. Samalla voidaan myös valmistaa kullekin rakenteeseen sijoitettavalla komponentille 26 asennusaukko
 5 johdekuvioon 24 tai 25 ja vastaavasti johdekuvioon 25 tai 24 suunnitellaan johteet komponentin 26 kontaktialueisiin liittymistä varten. Muut alucet johdekuvioista 24 ja 25 voidaan suunnitella rakenteen muiden johdotustarpeiden mukaisesti.

Seuraavaksi piirilevyaihion molemmat pinnat päällystetään eristemateriaalikerroksilla 27. Eristemateriaalikerrokset 27 voidaan valmistaa esimerkiksi laminoimalla
 10 piirilevyaihion pinnoille esikövetetut eristemateriaalilevyt. Kuvion 26 esittää piirilevyaihion tämän vaiheen jälkeen.

Seuraavaksi piirilevyaihioon valmistetaan sopivan kokoisia ja muotoisia syvennyksiä 28 rakenteeseen upotettavia komponentteja 26 varten. Syvennykset 28 voidaan valmistaa tarkoituksen mukaisesti esimerkiksi jollakin tunnetulla piirilevyvalmistuksessa
 15 käytetyllä menetelmällä. Syvennykset 28 voidaan valmistaa esimerkiksi CO₂-laserablaatiomenetelmällä, kemiallisesti syövyttämällä tai mekaanisesti jyrsimällä. Syvennyksiä 28 on siis mahdollista valmistaa myös molempien pintojen suunnasta sovellusmuodoissa, joissa osa komponenteista 26 halutaan sijoittaa johdekuviota 24 kohti ja osa johdekuviota 25 kohti. Esimerkissä syvennykset 28 valmistetaan siten, että
 20 ne läpäisevät toisen eristemateriaalikerroksista 27 sekä suuren osan eristemateriaalikerroksesta 21 mutta ne eivät kuitenkaan ulotu aivan johdekuvioon 25 saakka. Tämä voidaan toteuttaa esimerkiksi käyttämällä syvennyksen 28 valmistuksessa menetelmää, joka mahdollistaa tarkan syvyyskontrollin. Toinen vaihtoehto on valmistaa eristemateriaalikerros 21 kerroksittain siten, että poistettava osa ja jätettävä osa
 25 poikkeavat ominaisuuksiltaan sopivasti. Tällöin syvennys 28 saadaan valmistettua sopivaan syvyyteen tämän poikkeavuuden ansiosta esimerkiksi siten, että syvennyksen 28 valmistusmenetelmä on selektiivinen tämän poikkeavuuden suhteen ja syvennys 28 pysähtyy itsestään eristemateriaalikerroksen 21 sisältämään rajapintaan.

Edelleen yksi mahdollisuus on valmistaa syvennys johdekuvioon 25 saakka ja jatkaa
 30 valmistusta paljaan johdekuvion 25 pinnalle. Vielä yksi mahdollisuus on valmistaa

syvennys johdekuvioon 25 saakka ja valmistaa syvennyksen pohjalle ohut eristekerros, joka peittää johdekuvion 25.

Seuraavaksi piirilevyaihioon valmistetaan kontaktiaukot 29 liitettävien komponenttien 26 kontaktialueiden kohdille. Kontaktiaukkojen 29 valmistaminen suoritetaan samaan
5 tapaan kuin edellä kuvatut kontaktiaukot 4. Kuvio 28 esittää piirilevyaihion tämän välivaiheen jälkeen.

Kontaktiaukkojen 29 valmistamisen jälkeen piirilevyaihiolle levitetään liima 30 samaan tapaan kuin edellä on kuvattu liiman 5 yhteydessä. Kuvio 29 esittää piirilevyaihion liiman 30 kanssa. Tämän jälkeen komponentit 26 liimataan paikoilleen samaan tapaan
10 kuin komponentit 6, jolloin päädytään kuvion 30 esittämään rakenteeseen. Tämän jälkeen syvennykset 28 voidaan täyttää täytemateriaalilla 31, mikäli rakennetta halutaan vahvistaa. Kuvio 31 esittää piirilevyaihion syvennyksien 28 täyttämisen jälkeen. Tämän jälkeen kontaktiaukot 29 ja komponenttien 26 kontaktialueet puhdistetaan ja komponentteihin 26 muodostetaan sähköiset kontaktit. Myös tämä voidaan tehdä
15 edeltävien esimerkkien tapaan täyttämällä kontaktiaukot johdepastalla tai kasvattamalla johdemateriaalia elektrolyyttisesti tai kemiallisesti. Kuvio 32 esittää piirilevyn kontaktien valmistamisen jälkeen.

Kuviot 33–42 esittävät neljännen esimerkin piirilevyrakenteen valmistamisesta. Tässä esimerkissä kuvataan johdekuviokerrosten välisten sähköisten kontaktien valmistamista,
20 joten esimerkin menetelmässä piirilevyrakenteen ei sisään sijoiteta puolijohdesiruja. Tällaisella menetelmällä voidaan siis valmistaa esimerkiksi piirilevy, jonka pinnalle liitetään erilliskomponentteja, kuten puolijohdesiruja. Vastaavaa menetelmää voidaan tuki käyttää myös puolijohdesiruja sisältävien piirilevyrakenteiden valmistamiseen tai sijoittaa puolijohdesiruja johonkin toiseen eristekerrokseen, joka yhdistetään
25 esimerkeissä kuvattuun piirilevyrakenteeseen.

Tässä esimerkissä valmistus aloitetaan kuvion 33 mukaisesti tukikerroksesta 101, jonka molemmille pinnoille levitetään kuvion 34 mukaisesti resistikerrokset 102, tyypillisesti valoresistikerrokset. Nämä menetelmävaiheet vastaavat ensimmäisen esimerkin
30 kuvioiden 1 ja 2 yhteydessä kuvattuja menetelmävaiheita. Kuvion 3 yhteydessä kuvattuun tapaan valoresistikerros 102 valotetaan ja kehitetään. Näin saavutetaan kuviossa 35 kuvattu rakenne.

- Tämän jälkeen valoresistiin 102 avautuneisiin aukkoihin kasvatetaan elektrolyyttisesti johdemateriaalia 103, tyypillisesti kuparia. Tämä vaihe vastaa kuvion 4 yhteydessä kuvattua vaihetta. Kuvion 36 esittää piirilevyaihion johdemateriaalin kasvattamisen jälkeen. Kuten kuvion 4 yhteydessä jo selostettiin, näin voidaan valmistaa hyvin tarkkoja johdekuvioita, joissa johtimilla on haluttu korkeuden ja leveyden suhde.
- Johdekuvioiden 103 valmistamisen jälkeen resistikerrokset 102 poistetaan. Kuvio 37 esittää piirilevyaihion resistikerrosten 102 poistamisen jälkeen. Tämän esimerkin kuvaamassa sovellusmuodossa kontaktiaukot 104 on suunniteltu johdekuvion 103 valotusmaskiin, jolloin valmistettu johdekuvio 103 sisältää jo valmiiksi kontaktiaukot 104. Toisin sanoen kontaktiaukot 104 ja johdekuvio 103 valmistetaan samanaikaisesti. Näin kontaktiaukot 104 tulevat kohdistettua aina oikein suhteessa johdekuviioon 103. Kontaktiaukkojen 104 sijainti johdekuvioiden suhteen määräytyy siis itsekohdistuvalla tavalla. Vastaavaa itsekohdistuvaa tapaa voidaan käyttää myös edellä esitettyjen esimerkkien kuvaamissa valmistusmenetelmissä. Toisaalta myös kuvioiden 33–42 esimerkissä voitaisiin käyttää edellä esitettyjä kontaktiaukkojen valmistusmenetelmiä, joissa kontaktiaukot valmistetaan erillisessä menetelmävaiheessa. Käytettävä kontaktiaukkojen kohdistus- ja valmistusmenetelmä voidaan siis valita sopivasti sovelluskohteen mukaan. Kuvioiden 33–42 esimerkissä kontaktiaukot 104 on kuvattu valmistettavaksi johdekuviokerrosten välisiä sähköisiä kontakteja varten ja edellisissä esimerkeissä johdekuviokerroksen ja komponentin välisiä kontakteja varten. Edeltäviä esimerkkejä voidaan kuitenkin aivan yhtä hyvin modifioida siten, että niiden avulla valmistetaan kontaktit johdekuviokerrosten välille, ja vastaavasti kuvioiden 33–42 esimerkkiä voidaan modifioida siten, että kontaktit muodostetaan johdekuviokerroksen ja komponentin välille.
- Seuraavaksi piirilevyaihion pinnalle, johdekuvioiden 103 päälle voidaan valmistaa eristekerros 110 ja tämän pinnalle johdekerros 107. Tämä voidaan suorittaa esimerkiksi laminoimalla kerrokset piirilevyaihion pintaan kuviossa 38 kuvatulla tavalla. Tarkemmin valmistusta ja vaihtoehtoisia valmistustapoja on kuvattu edellä kuvioiden 9 ja 10 yhteydessä. Eristekerroksen 110 valmistamisen jälkeen tukikerros 101 voidaan poistaa kuvion 11 yhteydessä esitettyyn tapaan. Kuvio 39 esittää piirilevyaihion poikkileikkauksen tämän välivaiheen jälkeen.

Seuraavaksi piirilevyaihioon valmistetaan läpiviennit, joiden avulla voidaan muodostaa sähköiset kontaktit johdekuvioiden 103 ja johdekerroksen 107 välille. Läpivientien valmistamista varten eristemateriaali 110 poistetaan kontaktiaukkojen 104 kohdalla. Puhdistaminen voidaan suorittaa esimerkiksi plasmatekniikalla, kemiallisesti tai laserin avulla. Kuvion 40 esittää piirilevyaihion sen jälkeen, kun läpivientireiät on avattu kontaktiaukkojen 104 kohdalle.

Tämän jälkeen kontaktiaukkoihin 104 ja läpivientireikiin tuodaan johdemateriaalia siten, että muodostuu sähköinen kontakti johdekuvioiden 103 ja johdekerroksen 107 välille. Johdemateriaali voidaan valmistaa esimerkiksi täyttämällä kontaktiaukot sähköä johtavalla pastalla. Johdemateriaali voidaan valmistaa myös jollakin useista piirilevyteollisuudessa tunnetuista kasvatusmenetelmistä. Hyvälaatuiset sähköiset kontaktit voidaan valmistaa esimerkiksi muodostamalla metallurginen liitos kasvattamalla johdemateriaali kemiallisella tai sähkökemiallisella menetelmällä. Yksi hyvä vaihtoehto on ohuen kerroksen kasvattaminen kemiallisella menetelmällä ja kasvatuksen jatkaminen edullisemmalla sähkökemiallisella menetelmällä. Näiden menetelmien lisäksi voidaan toki käyttää myös jotakin muuta menetelmää, josta on hyötyä lopputuloksen kannalta.

Kuviosarjan esimerkissä kontaktiaukot 104, läpivientireiät, johdekuviot 103 sekä eristekerroksen 110 johdekuvioiden 103 väliin jäävä paljas pinta pinnoitetaan ensiksi ohuella johdekerroksella ja sen jälkeen johdekerroksen paksuutta kasvatetaan elektrolyytisesti kunnes kontaktiaukot 104 ja läpivientireiät ovat täyttyneet johdemateriaalilla. Kuvio 41 kuvaa rakennetta kasvatuksen jälkeen. Läpiviennit voidaan toki valmistaa myös siten, että kontaktiaukot 104 täytetään ainoastaan osittain johdemateriaalilla. Yksi mahdollisuus on kasvattaa johdemateriaalia kontaktiaukkojen 104 sivuseinämille ja jättää kontaktiaukkojen 104 keskiosa ainakin pääosin vapaaksi johdemateriaalista.

Tämän jälkeen piirilevyaihiota etsataan ylimääräisen johdemateriaalin poistamiseksi. Lisäksi johdekerros 107 kuviodaan johdekuvioiksi 117 jollakin sopivalla kuviointi-menetelmällä. Johdekerroksen 107 kuviointi voidaan tehdä ennen ohennusetsausta, samanaikaisesti sen kanssa tai ohennusetsauksen jälkeen. Kuvio 42 esittää piirilevyrakenteen näiden prosessivaiheiden jälkeen. Valmistettu piirilevyrakenne

käsittää siis eristekerroksen 110 molemmilla pinnoilla johdekuviot 103 ja 117, jotka on yhdistetty sähköisesti toisiinsa läpivientien avulla.

- 5 Kuvioiden 33–42 esittämän neljännen esimerkin mukaisella menetelmän yhdessä muunnelmassa piirilevyaihioon pintaan kiinnitetään johdekerros 107 (ks. kuvio 38), jonka pinnalle on jo valmistettu johdekuviot. Mikäli johdekuviot valmistetaan sille pinnalle, joka painetaan eristekerrosta 110 vasten, johdekuvio saadaan tuotua lähelle johdekuviota 103, jolloin läpivienneistä saadaan valmistettua lyhyempiä. Tällaisessa sovellusmuodossa on myös mahdollista korvata johdekerros 107 eristekerroksella. Yhdessä sovellusmuodossa johdekerros 107 korvataan tukikerroksen 101 ja 10 johdekuvion 103 (vrt. kuvio 37) muodostamaa rakennetta vastaavalla rakenteella. Tällöin rakenteet voidaan esimerkiksi laminoida vastakkain siten, että johdekuviot 103 tulevat eristekerrosta 110 vasten. Johdekerros 107 tai korvaava eristekerros voidaan jopa kokonaan jättää poisikin, mikäli piirilevyaihioon kiinnitettävä johdekuvio on itsessään riittävän tukeva.
- 15 Edellä esitettyjä kuvioiden 33–42 esittämän neljännen esimerkin mukaisia menetelmiä voidaan modifioida myös siten, että kontaktiaukot 104 valmistetaan läpirei'iksi, jotka ulottuvat koko piirilevyaihion läpi. Kuvion 40 esimerkissä tämä tarkoittaisi sitä, että kontaktiaukot 104 läpäisisivät myös johdekerroksen 107. Tällainen sovellusmuoto soveltuu hyvin käytettäväksi pinnoitusmenetelmän yhteydessä.
- 20 Edellä esitettyjen esimerkkien mukaisilla menetelmillä on lukuisia muunnelmia ja esimerkkien kuvaamia menetelmiä voidaan myös yhdistellä toistensa kanssa. Muunnelmat voivat liittyä yksittäisiin prosessivaiheisiin tai prosessivaiheiden keskinäiseen järjestykseen.
- 25 Piirilevyrakenteeseen voidaan myös valmistaa monia sellaisia piirteitä, jotka eivät käyneet ilmi edellisistä esimerkeistä. Sähköisten kontaktien muodostamiseen osallistuvien läpivientien lisäksi piirilevyrakenteeseen voidaan esimerkiksi valmistaa lämpöläpivientejä, joiden tarkoitus on tehostaa lämmön johtumista pois komponentista 6, 16 tai 26. Lämmön johtumisen tehostuminen perustuu siihen, että lämpöläpiviennin lämmönjohtokyky on suurempi kuin komponenttia ympäröivän eristemateriaalin. Koska 30 sähkönjohteet ovat tyypillisesti myös hyviä lämmönjohteita, lämpöläpiviennit voidaan

useimmiten valmistaa samalla tekniikalla ja jopa samassa prosessivaiheessa kuin sähköiset kontaktit komponentteihin 6, 16 ja 26.

- Sähköisen kontaktin ja lämpökontaktin (lämpöläpiviennin) välillä on usein se ero, että lämpökontakti ei muodosta sähköistä kontaktia komponentin 6, 16 tai 26 kanssa.
- 5 Lämpökontakti voi esimerkiksi tulla kosketukseen komponentin kanssa sellaisessa kohdassa, jossa komponentin pinta on suojattu eristävällä suojakerroksella. Lämpökontaktin pinnan ja komponentin pinnan väliin voidaan jättää myös väli, joka voi olla esimerkiksi 1 – 15 mikrometriä. Lämmön johtumista voidaan vielä edelleen tehostaa valmistamalla komponentin pinnalle lämpönystyjiä, jotka on tarkoitettu lämmön
- 10 johtamiseen ulos komponentista. Tällöin komponentin lämpönystyt ja piirilevyrakenteen lämpöläpiviennit voivat tulla valmiissa rakenteessa mekaaniseen kontaktiin toistensa kanssa, jolloin lämpökontakti ja sähköinen kontakti vastaavat hyvin läheisesti toisiaan mekaanisten ja valmistusteknisten ominaisuuksiensa osalta.
- Yleisesti lämpöläpivientien tai lämpökontaktien lukumäärä, poikkipinta-ala ja sijainnit
- 15 valitaan lämmönsiirtotarpeen mukaan ja ottamalla huomioon se, että lämmönjohteilla ei aiheuteta kohtuuttomia häiriöitä komponentin sähköiselle toiminnalle. Lämpöläpivientien on kuitenkin edullisinta sijoittaa komponentin kohdalla tai aivan komponentin vieressä.
- Joissakin sovellusmuodoissa lämpökontakteja voidaan myös käyttää sähköisen
- 20 kontaktin muodostamiseen komponentin kanssa. Varsinkin komponentin maakontakti voi luontevasti soveltua tähän tarkoitukseen. Tällöin komponentin maakontaktista valmistetaan poikkipinta-alaltaan huomattavasti normaalia suurempi tai maakontakti muodostetaan useasta erillisestä maakontaktista, joiden yhteinen poikkipinta-ala on huomattavasti tavanomaista maakontaktia suurempi.
- 25 Edellisen perusteella onkin selvää, että edellä kuvattujen menetelmien avulla voidaan valmistaa sähköisiä kontakteja komponentin molemmille pääpinnoille, eli ensisijaiselle kontaktointipinnalle sekä tälle vastakkaiselle takapinnalle.
- Piirilevyrakenteeseen valmistetaan myös mielellään sähköisiä johdekuvioita vastaavia johdekuvioita lämmön johtamista varten. Lämpökontaktit valmistetaan tällaisten
- 30 lämmönjohteiden pinnalle, jolloin lämpökontaktit johtavat lämpöenergiaa komponentista lämmönjohteisiin, jotka johtavat lämpöenergiaa piirilevyrakenteen

lateraalisuunnassa pois komponentin läheisyydestä. Nämä lateraalisuuntaiset lämmönjohteet voivat edelleen yhdistyä vertikaalisuuntaisiin lämmönjohteisiin, joiden avulla lämpötehoa voidaan johtaa elektroniikkamoduulin tai muun piirilevyrakenteen sisemmistä kerroksista ulkopinnalle. Pintaan ulottuvat lämmönjohteet voidaan
 5 puolestaan kytkeä sopivaan lämpönieluun, jolloin komponentin jäähdytystä saadaan edelleen tehostettua.

Käytettäessä valmistusmenetelmää, jossa kontaktiaukot 4, 14, 29, 104 kohdistetaan ja valmistetaan johdekuvion valmistamisen jälkeen, menetelmän herkkyyttä kohdistusvirheille voidaan vähentää mitoittamalla kontaktiaukkojen 4, 14, 29, 104
 10 läpimitta johdekuvion johteiden leveyttä suuremmaksi. Tätä mielenkiintoista sovellusmuotoa on kuvataan seuraavassa tarkemmin kuvioiden 43–49 avulla.

Kuviossa 43 on esitetty johdekuvioon kuuluvan johteen 41 pää ja läpivienti 42 ylhäältä (tai alhaalta) eli piirilevyn pintaa kohti katsottuna. Kuvion 43 esittämässä tapauksessa läpiviennin 42 kohdistus on osunut hyvin kohdalleen johteen 41 päähän. Tämä
 15 tarkoittaa siis edellä kuvattujen ensimmäisen, toisen ja kolmannen esimerkin tapauksessa sitä, että vastaava kontaktiaukko 4, 14, 29, 104 on kohdistunut oikein suhteessa johdekuvioon 3, 13, 25, 103. Tässä tapauksessa kontaktiaukon (ja vastaavasti läpiviennin) läpimitalla ei olekaan merkitystä kohdistumisen ja kontaktin onnistumisen kannalta.

Kuviot 44–46 kuvaavat puolestaan erilaisia kohdistusvirhetilanteita, joissa kontaktiaukon sijainti on siirtynyt suhteessa kuvion 43 kuvaamaan tavoitetilään. Kuvioiden perusteella havaitaan, että jokaisessa tapauksessa kuitenkin syntyy hyvä sähköinen kontakti läpiviennin 42 ja johteen 41 välille. Hyvä kontakti saadaan aikaan varsinkin
 20 sellaisissa sovellusmuodoissa, joissa läpivienti täytetään kasvattamalla metallia kemiallisen ja/tai sähkökemiallisen menetelmän avulla. Tällöin läpiviennin 42 ja johteen 41 välillä on metallurginen liitos. Kuvioiden 44–46 perusteella on selvää, että tällainen läpivientien valmistusmenetelmä ei ole herkkä kohdistusvirheille. Tällaisen menetelmän avulla voidaan valmistaa myös tavanomaisten piirilevyprosessien yhteydessä monikerrospiirilevyyn yksi tai useampi johdekuviokerros, joka sisältää
 25 kapeita ja tiheästi sijoitettuja johteita 41.

Kontaktiaukon 4, 14, 29, 104 läpimitan vaikutusta kohdistustoleranssiin on kuvattu tarkemmin kuvioissa 47–49. Kuvio 47 esittää johteen 43, jonka pään läheisyyteen on valmistettu läpivienti. Läpiviennille on esitetty kolme eri asemaa (A, B ja C) ja kaksi erilaista läpimittaa (44, 45). Läpiviennillä 44 on pienempi läpimitta kuin läpiviennillä 45. Kussakin asemassa A, B ja C molempien läpivientien 44 ja 45 keskipisteet sijaitsevat samassa kohdassa johteen 43 suhteen. Kuvion esimerkistä havaitaan, että suuremman läpimitan omaavat läpiviennit 45A, 45B ja 45C muodostavat jokainen sähköisen kontaktin johteen 43 kanssa. Pienemmän läpimitan omaavista läpivienneistä sen sijaan ainoastaan 44C kykenee muodostamaan sähköisen kontaktin johteen 43 kanssa. Kontaktiaukon 4, 14, 29, 104 suurempi läpimitta vähentää siis huomattavasti valmistusprosessin herkkyyttä kontaktiaukon 4, 14, 29, 104 kohdistusvirheelle. Kuviossa 48 on esitetty johteen 43 ympärille kohdistustoleranssialue 47, jonka sisälle sattuva läpiviennin 45 keskipiste takaa hyvän sähköisen kontaktin. Läpiviennin 44 vastaava kohdistustoleranssialue 48 taas on esitetty kuviossa 49. Kuvioden 47–49 perusteella havaitaan, että läpiviennin läpimitan suurentaminen vähentää oleellisesti valmistusprosessin herkkyyttä läpiviennin kohdistusvirheelle. Samalla voidaan säilyttää johteen 43 leveys pienenä. Kontaktiaukon 4, 14, 29, 104 läpimitta voi olla esimerkiksi vähintään 0,8-kertainen, mielellään vähintään 1-kertainen, mieluummin vähintään 1,2 tai vähintään 1,5-kertainen johdekuvion 3, 13, 25, 103 vastaavan johteen leveyteen verrattuna.

Edellisten esimerkkien perusteella on selvää, että menetelmää voidaan käyttää myös monenlaisten kolmedimensionaalisten piirirakenteiden valmistamiseen. Menetelmää voidaan käyttää esim. siten, että useita puolijohdesiruja sijoitetaan päällekkäin ja näin muodostetaan useita puolijohdesiruja sisältävä paketti, jossa puolijohdesirut on kytketty toisiinsa yhdeksi toiminnalliseksi kokonaisuudeksi. Tällaista pakettia voidaan kutsua kolmedimensionaaliseksi multichip-moduuliksi. Tällaisessa moduulissa puolijohdesirut voidaan valita vapaasti ja eri puolijohdesirujen väliset kontaktit voidaan helposti valmistaa valittujen puolijohdesirujen mukaisesti.

Kuvioden esimerkit kuvaavat joitakin mahdollisia prosesseja, joiden avulla keksintöämme voidaan käyttää hyväksi. Keksintömme ei kuitenkaan rajoitu vain edellä esitettyihin prosesseihin, vaan keksintö kattaa muitakin erilaisia prosesseja ja niiden lopputuotteita, patenttivaatimusten täydessä laajuudessa ja ekvivalenssitulkinta

huomioon ottaen. Keksintö ei myöskään rajoitu vain esimerkkien kuvaamiin rakenteisiin ja menetelmiin, vaan alan ammattimiehelle on selvää, että keksintömme erilaisilla sovelluksilla voidaan valmistaa hyvin monenlaisia elektroniikkamoduuleja ja piirilevyjä, jotka poikkeavat suurestikin edellä esitetystä esimerkistä. Kuvioiden komponentit ja johdotukset on siis esitetty ainoastaan valmistusprosessin havainnollistamistarkoituksessa. Edellä esitettyjen esimerkkien prosesseihin voidaan tehdä runsaasti muutoksia, poikkeamatta silti keksinnön mukaisesta perusajatuksesta. Muutokset voivat liittyä esimerkiksi eri vaiheissa kuvattuihin valmistustekniikoihin tai prosessivaiheiden keskinäiseen järjestykseen.

- 10 Menetelmän avulla voidaan valmistaa myös komponenttipaketteja piirilevyille liittämistä varten. Tällaiset paketit voivat sisältää myös useampia komponentteja, jotka on kytketty sähköisesti toisiinsa.

15 Menetelmällä voidaan valmistaa myös kokonaisia sähköisiä moduuleja. Moduuli voi olla myös piirilevy, jonka ulkopinnalle voidaan kiinnittää komponentteja kuten tavalliseen piirilevyyn. Moduuli voi käsittää useita kerroksia ja näistä kerroksista yksi tai useampi voi käsittää kerroksen sisälle sijoitettuja puolijohdekomponentteja.

Patenttivaatimukset:

1. Menetelmä piirilevyrakenteen valmistamiseksi, jossa menetelmässä
 - valmistetaan johdekuvio (103),
 - valmistetaan johdekuvioon (103) kontaktiaukkoja (104) läpivientien valmistamista varten,
 - valmistetaan johdekuvion (103) pinnalle eristemateriaalikerros (110) sekä tämän pinnalle johdekerros (107) tai johdekuviokerros (117),
 - valmistetaan kontaktiaukkojen (104) kohdille läpireiät eristemateriaalikerrokseen (110), ja
- 10 – tuodaan läpireikiin sähköäjohtavaa materiaalia sähköisten kontaktien muodostamiseksi johdekuvion (103) ja johdekerroksen (109) tai johdekuviokerroksen (19) välille.
2. Menetelmä ainakin yhden komponentin (6; 16; 26) sisältävän piirilevyrakenteen valmistamiseksi, jossa menetelmässä
 - 15 – valmistetaan johdekuvio (3; 13; 25),
 - valmistetaan johdekuvioon (3; 13; 25) kontaktiaukkoja (4; 14; 29) komponentin (6; 16; 26) sähköisiä kontakteja varten,
 - kiinnitetään komponentti (6; 16; 26) johdekuvion (3; 13; 25) suhteen, ja
 - tuodaan kontaktiaukkoihin (4; 14; 29) sähköäjohtavaa materiaalia sähköisten kontaktien muodostamiseksi johdekuvion (3; 13; 25) ja komponentin (6; 16; 26) välille.
- 20 3. Patenttivaatimuksen 2 mukainen menetelmä, t u n n e t t u siitä, että komponentti (6; 16; 26) kiinnitetään johdekuvion (3; 13; 25) suhteen liimaamalla.
- 25 4. Patenttivaatimuksen 2 tai 3 mukainen menetelmä, t u n n e t t u siitä, että kiinnittämisen jälkeen komponentti (6; 16) ympäröidään eristemateriaalilla (8, 9; 18, 19).

5. Jonkin patenttivaatimuksen 2–4 mukainen menetelmä, t u n n e t t u siitä, että johdekuvio (25) valmistetaan eristemateriaalilevyn (21) pinnalle, eristemateriaalilevyyn (21) valmistetaan komponenttia (26) varten syvennys (28) ja komponentti kiinnitetään valmistettuun syvennykseen (28).
- 5 6. Jonkin patenttivaatimuksen 2–5 mukainen menetelmä, t u n n e t t u siitä, että komponentti (6; 16; 26) on pakkaamaton mikropiiri.
7. Jonkin patenttivaatimuksen 2–6 mukainen menetelmä, t u n n e t t u siitä, että piirilevyrakenteeseen valmistetaan sähköisten kontaktien lisäksi ainakin yksi lämpökontakti, jonka tarkoituksena on tehostaa lämpöenergian johtumista pois
10 komponentista (6; 16; 26).
8. Patenttivaatimuksen 7 mukainen menetelmä, t u n n e t t u siitä, että lämpökontakti valmistetaan samalla prosessilla kuin sähköinen kontakti.
9. Jonkin patenttivaatimuksen 2–8 mukainen menetelmä, t u n n e t t u siitä, että johdekuvio (3; 13; 25) on valmis ennen komponentin (6; 16; 26) kiinnittämistä
15 piirilevyrakenteeseen.
10. Jonkin patenttivaatimuksen 2–9 mukainen menetelmä, t u n n e t t u siitä, että kontaktiaukkoihin (4; 14; 29) tuodaan sähköäjohtavaa materiaalia pinnoitusmenetelmällä.
11. Jonkin patenttivaatimuksen 2–10 mukainen menetelmä, t u n n e t t u siitä, että
20 komponentin kontaktialueet tai kontaktinystyt tulevat kontaktiaukkojen (4; 14; 29) kanssa kohdakkain.
12. Jonkin patenttivaatimuksen 2–11 mukainen menetelmä, t u n n e t t u siitä, että kontaktiaukot (4; 14; 29) valmistetaan ennen komponentin (6) kiinnittämistä.
13. Jonkin patenttivaatimuksen 2–11 mukainen menetelmä, t u n n e t t u siitä, että
25 komponentti (6) kiinnitetään ennen kontaktiaukkojen (4; 14; 29) valmistamista.
14. Patenttivaatimuksen 1 mukainen menetelmä, t u n n e t t u siitä, että johdekuvio (3) on valmis ennen eristemateriaalikerroksen (10) valmistamista.

15. Patenttivaatimuksen 1 tai 14 mukainen menetelmä, tunnettu siitä, että läpireikiin tuodaan sähköäjohtavaa materiaalia pinnoitusmenetelmällä.
16. Jonkin patenttivaatimuksen 1–15 mukainen menetelmä, tunnettu siitä, että piirilevyrakenteeseen valmistetaan useampia johdekuviokerroksia.
- 5 17. Jonkin patenttivaatimuksen 1–16 mukainen menetelmä, tunnettu siitä, että kontaktiaukot (4; 14; 29; 104) valmistetaan johdekuvion (3; 13; 25; 103) valmistamisen jälkeen.
- 10 18. Jonkin patenttivaatimuksen 1–16 mukainen menetelmä, tunnettu siitä, että kontaktiaukot (4; 14; 29; 104) valmistetaan johdekuvioon (3; 13; 25; 103) samanaikaisesti johdekuvion (3; 13; 25; 103) valmistamisen kanssa.
- 15 19. Jonkin patenttivaatimuksen 1–18 mukainen menetelmä, tunnettu siitä, että ainakin yksi kontaktiaukko (4; 14; 29; 104) kohdistetaan johdekuvion (3; 13; 25; 103) johteeseen ja valmistetaan siten, että kontaktiaukon läpimitta on oleellisesti yhtä suuri kuin johteen leveys tai kontaktiaukon läpimitta on vähintään 1,2, mieluummin vähintään 1,5 kertaa suurempi kuin johteen leveys.
20. Jonkin patenttivaatimuksen 1–19 mukainen menetelmä, tunnettu siitä, että ainakin yksi kontaktiaukko (4; 14; 29; 104) sijaitsee osittain johdekuvion (3; 13; 25; 103) määrittelemien johteiden ulkopuolella.
- 20 21. Piirilevyrakenne, joka on valmistettu jonkin patenttivaatimuksen 1–20 määrittelemällä menetelmällä.
22. Piirilevyrakenne, joka käsittää johteen johdekuviokerroksessa (3; 13; 25; 103) sekä johteeseen liittyvän läpiviennin, joka yhdistää johteen toiseen johdekuviokerrokseen (117) tai komponenttiin (6), tunnettu siitä, että läpiviennin läpimitta on oleellisesti yhtä suuri tai suurempi kuin johteen leveys.
- 25 23. Patenttivaatimuksen 22 mukainen menetelmä, tunnettu siitä, että läpivientien materiaali on metallia, joka on valmistettu pinnoitusmenetelmällä.

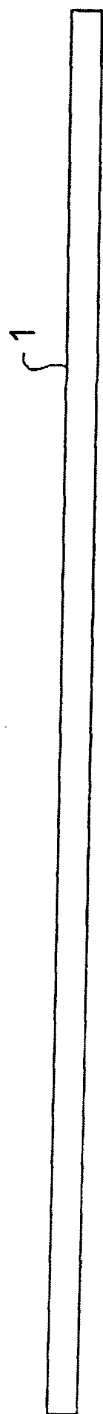


Fig. 1

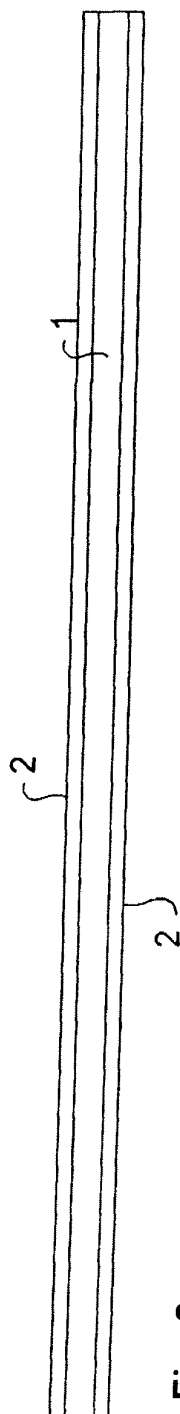


Fig. 2

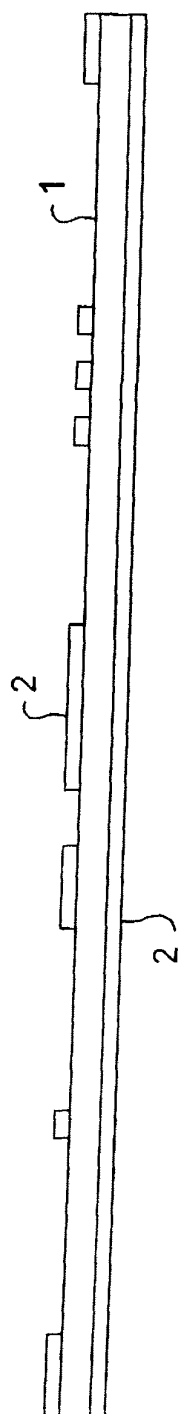


Fig. 3

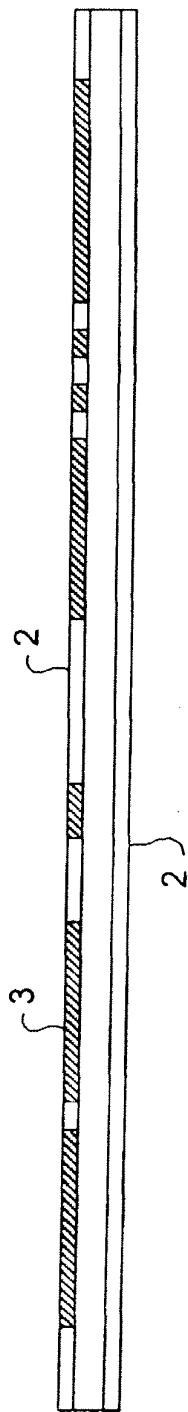


Fig. 4



Fig. 5



Fig. 6

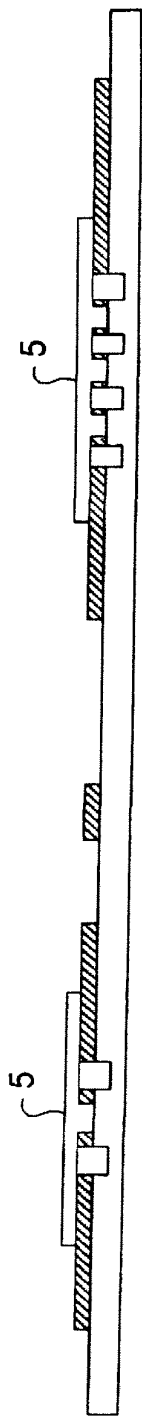


Fig. 7

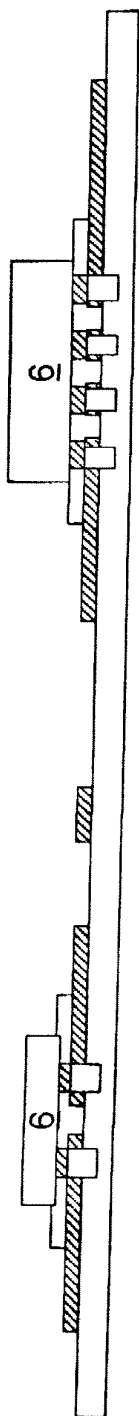


Fig. 8

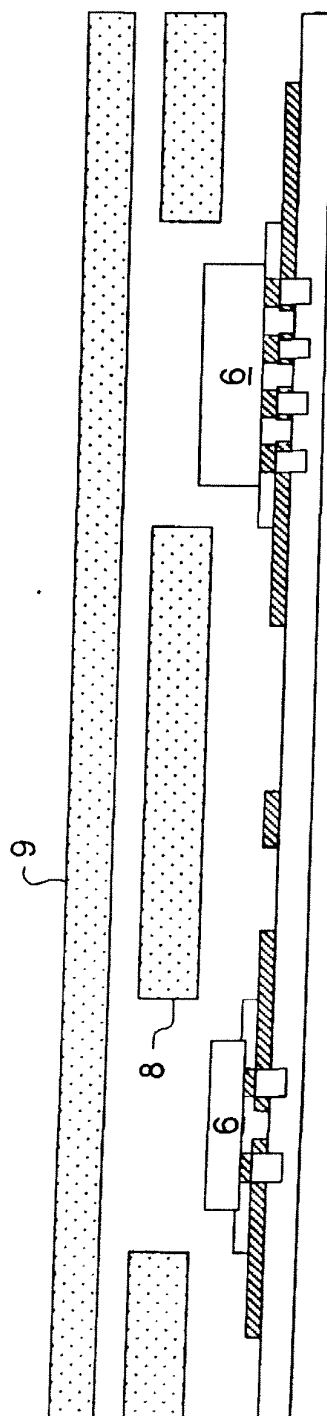


Fig. 9

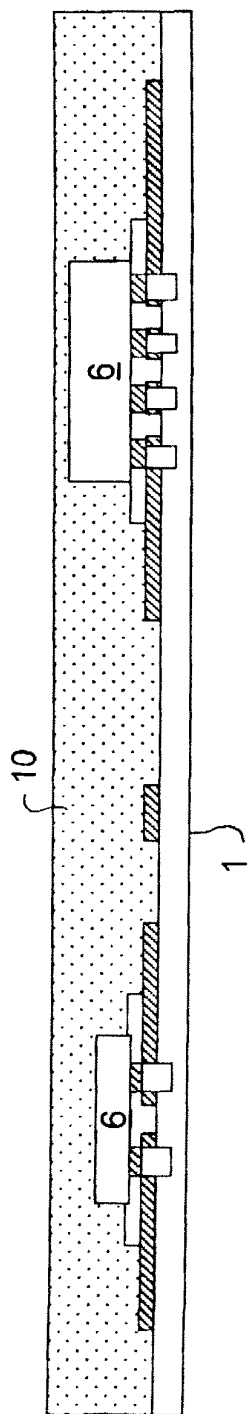


Fig. 10

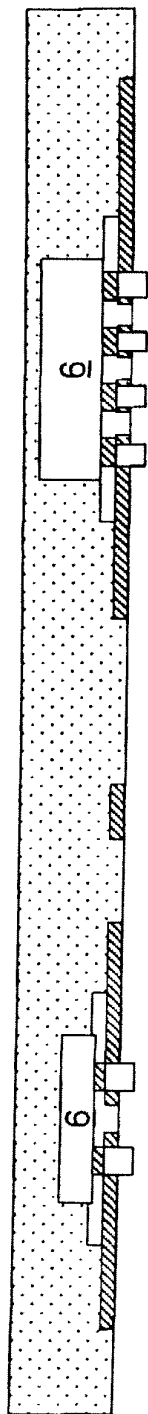


Fig. 11

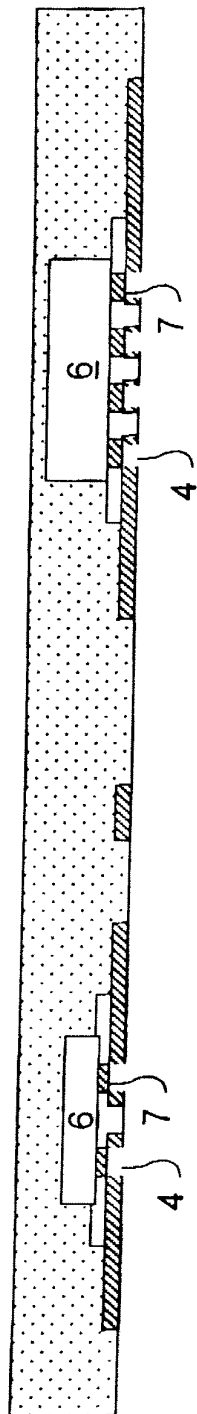


Fig. 12

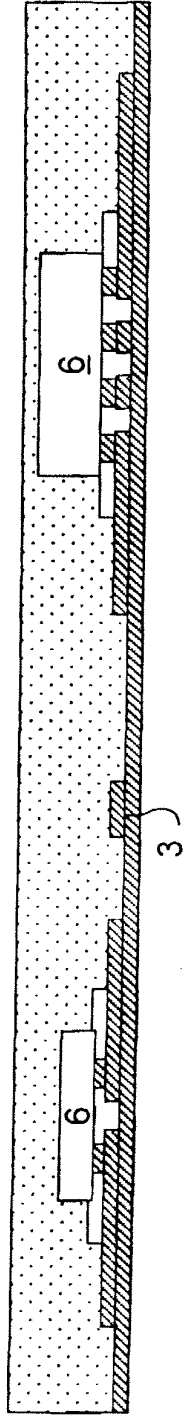


Fig. 13

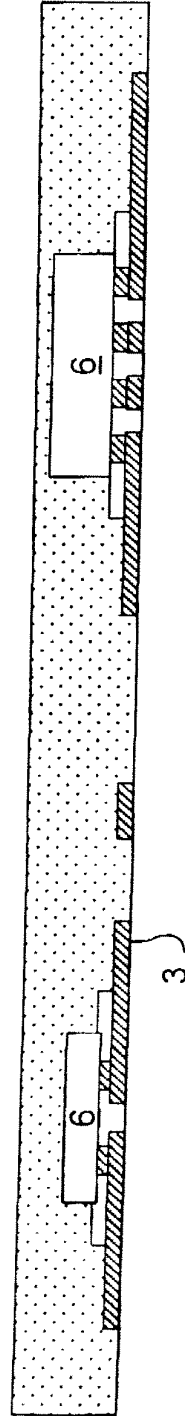


Fig. 14

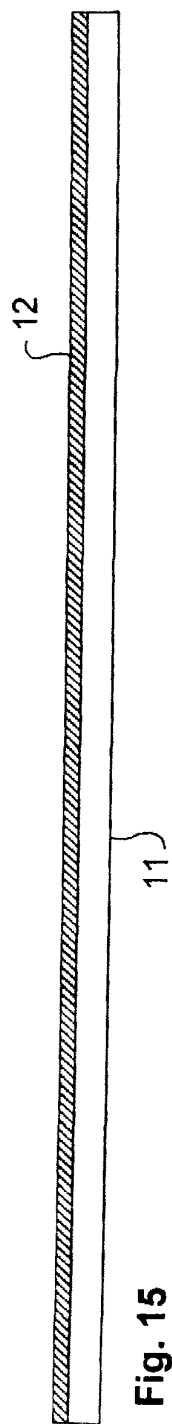
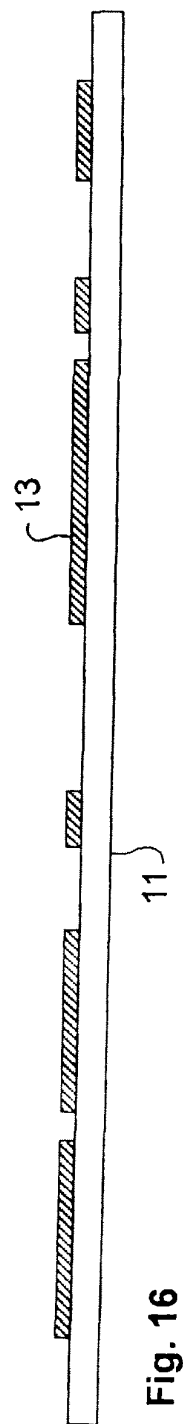
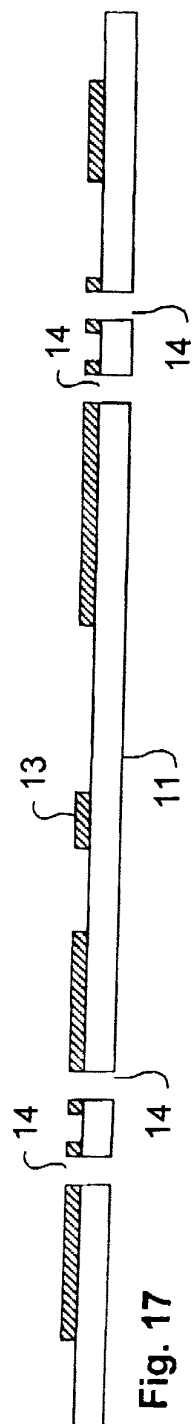
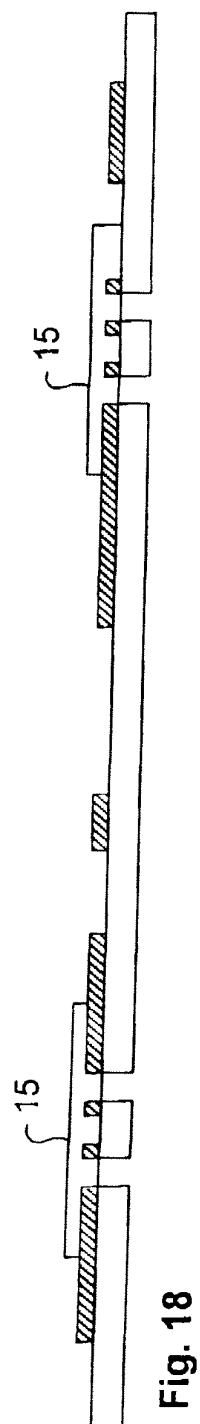




Fig. 19

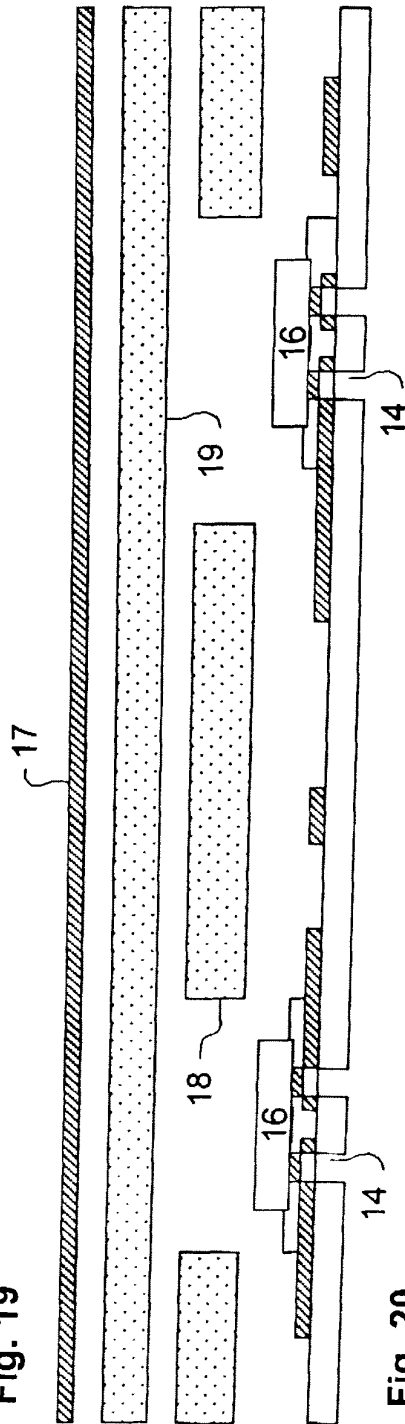


Fig. 20

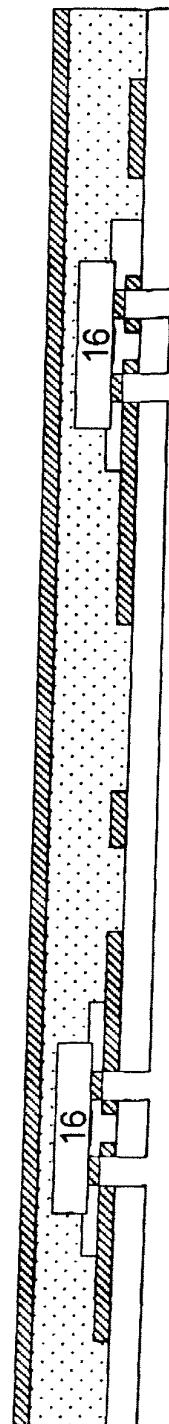


Fig. 21

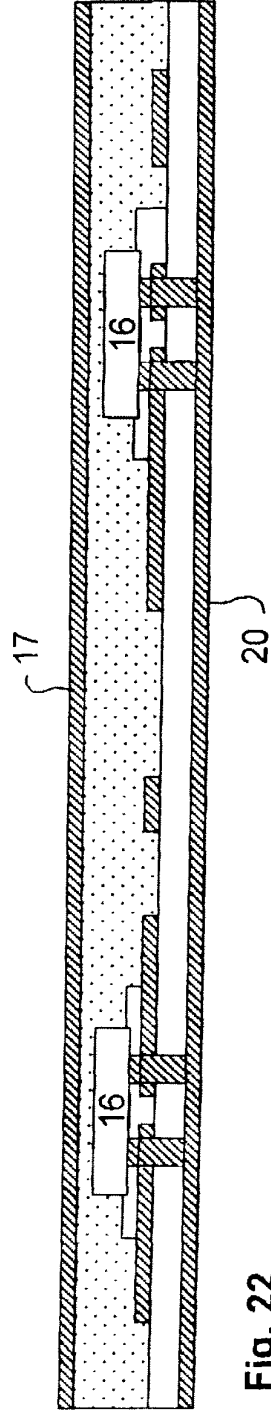


Fig. 22

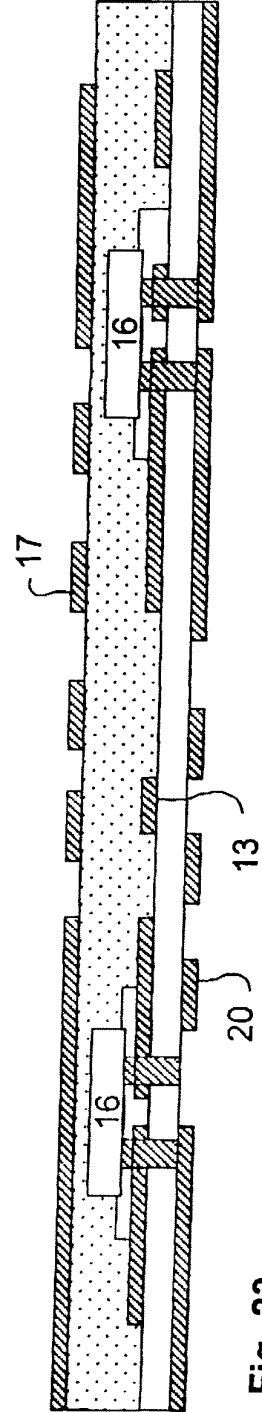


Fig. 23

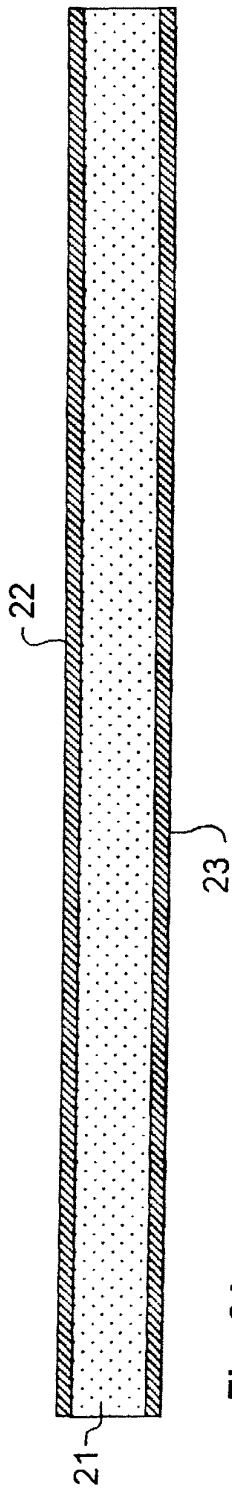


Fig. 24

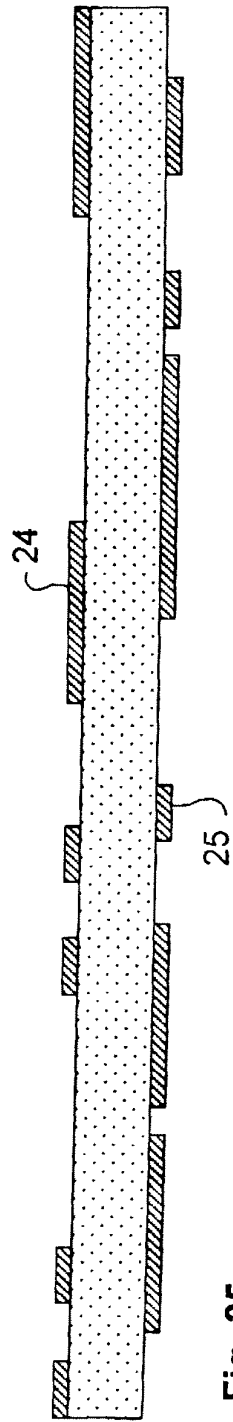


Fig. 25

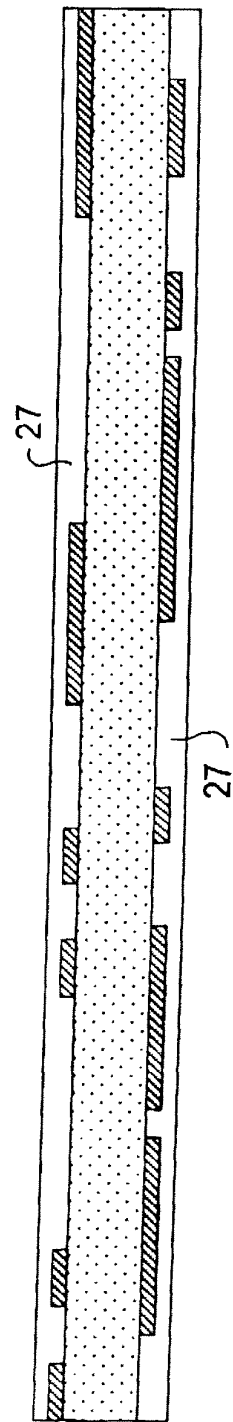


Fig. 26

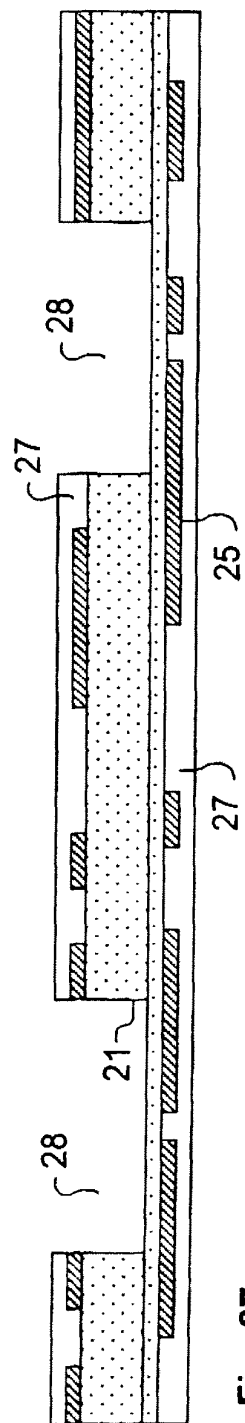


Fig. 27

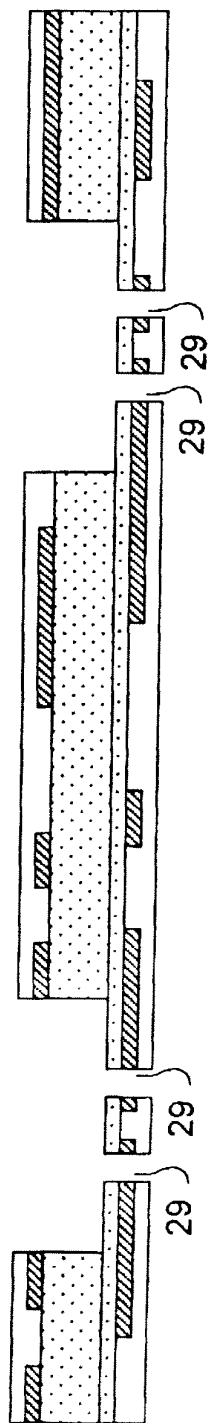


Fig. 28

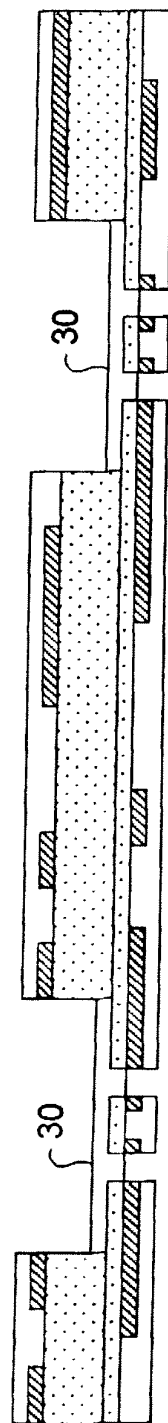


Fig. 29

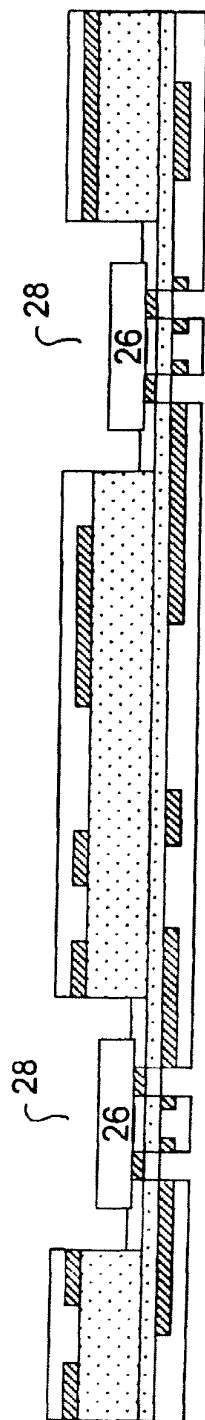


Fig. 30

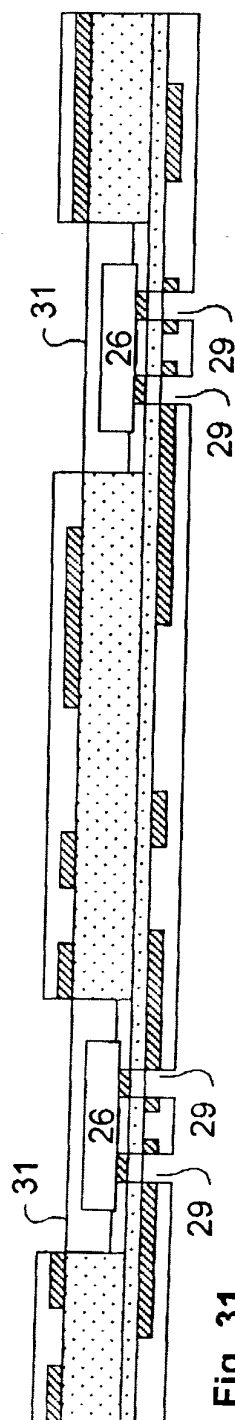


Fig. 31

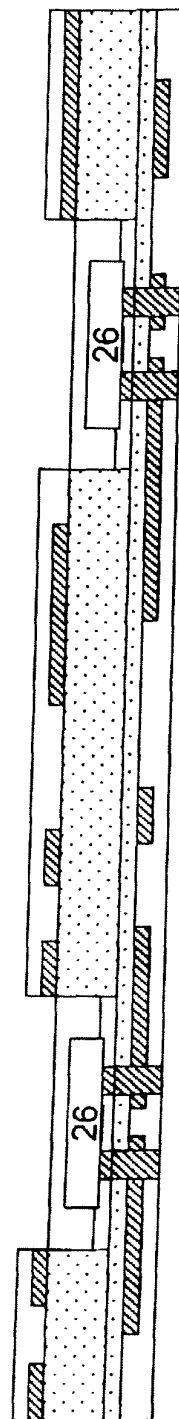


Fig. 32



Fig. 33

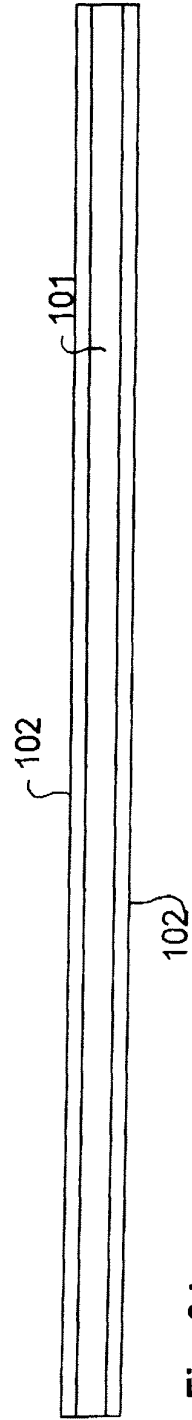


Fig. 34

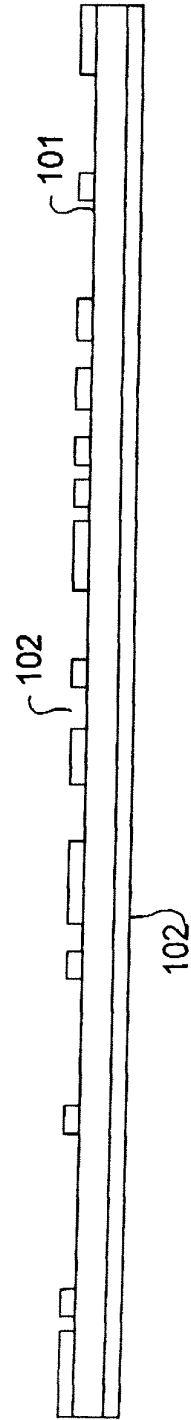


Fig. 35

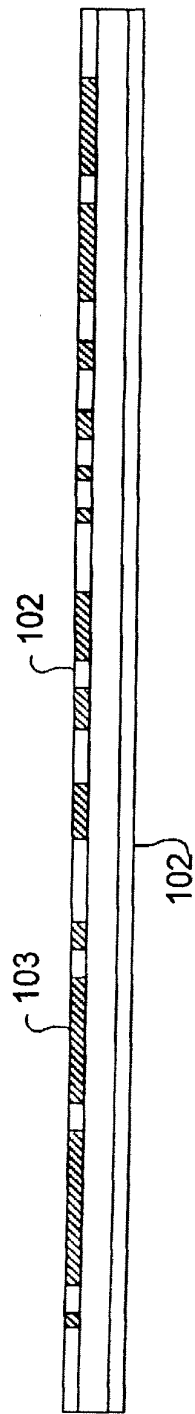


Fig. 36

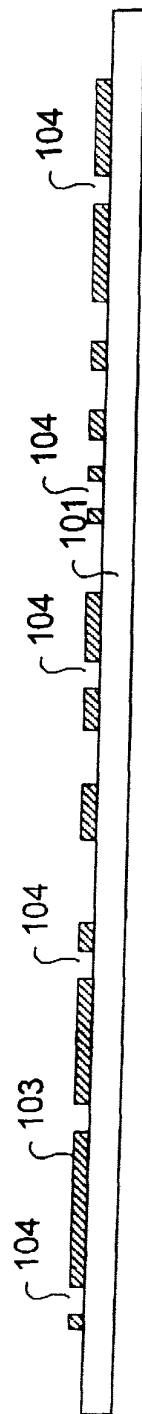


Fig. 37

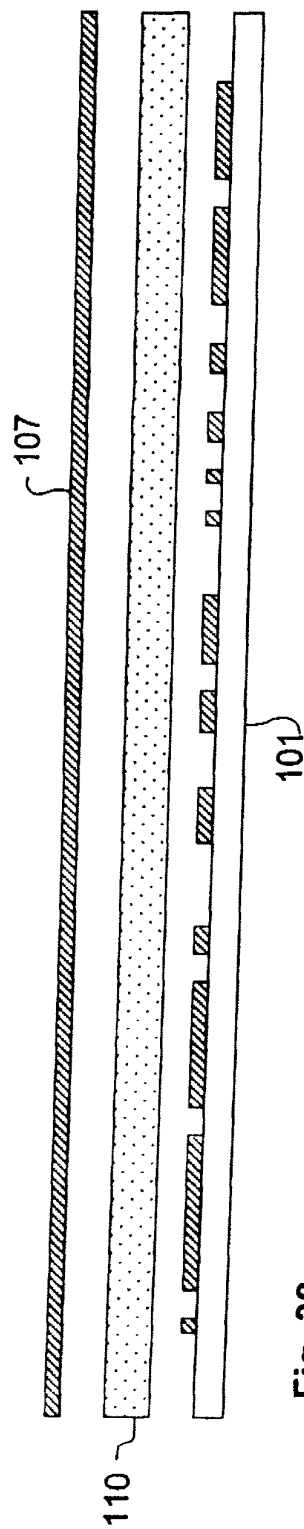


Fig. 38



Fig. 39

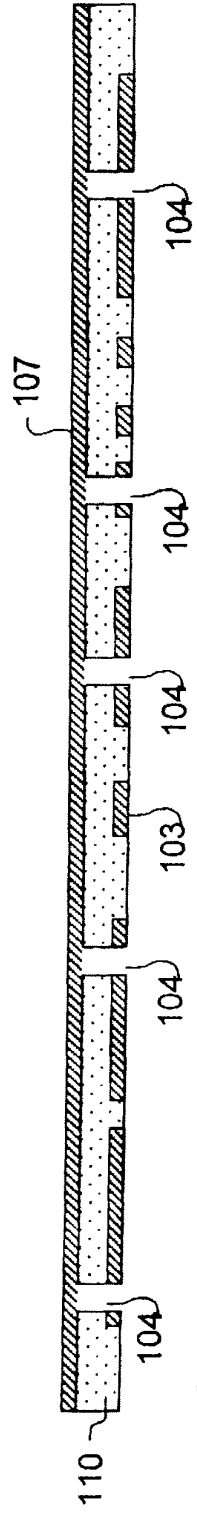


Fig. 40

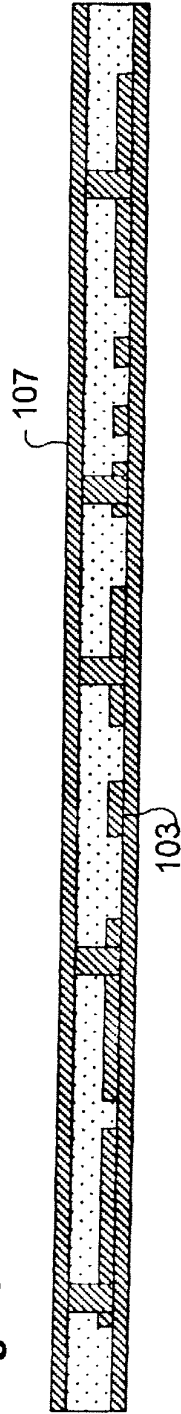


Fig. 41

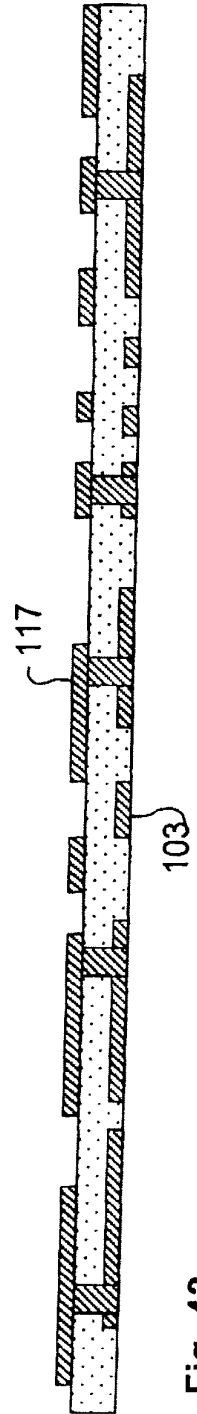


Fig. 42

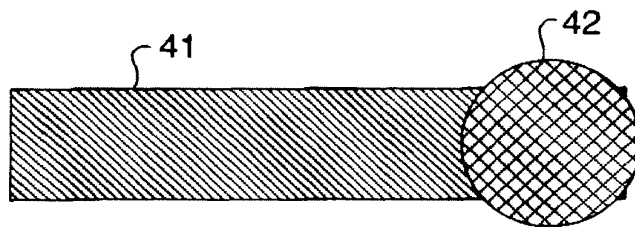


Fig. 43

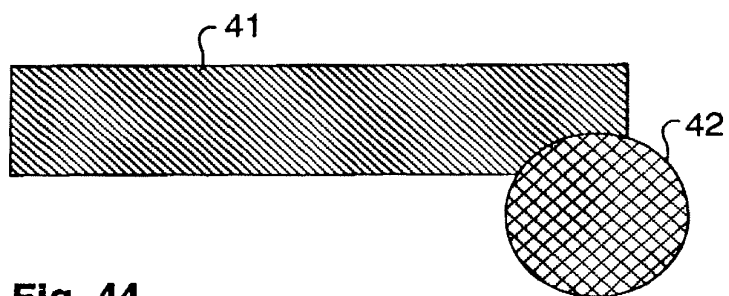


Fig. 44

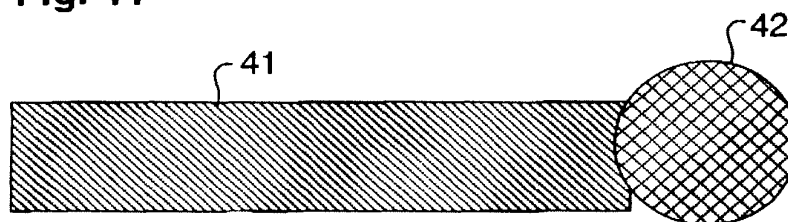


Fig. 45

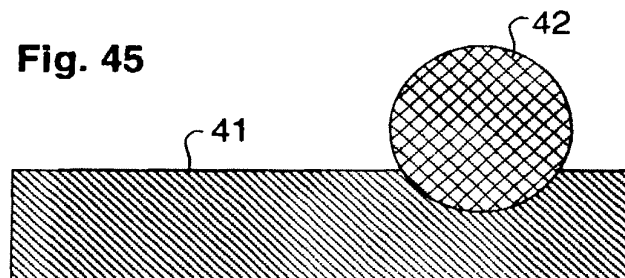


Fig. 46

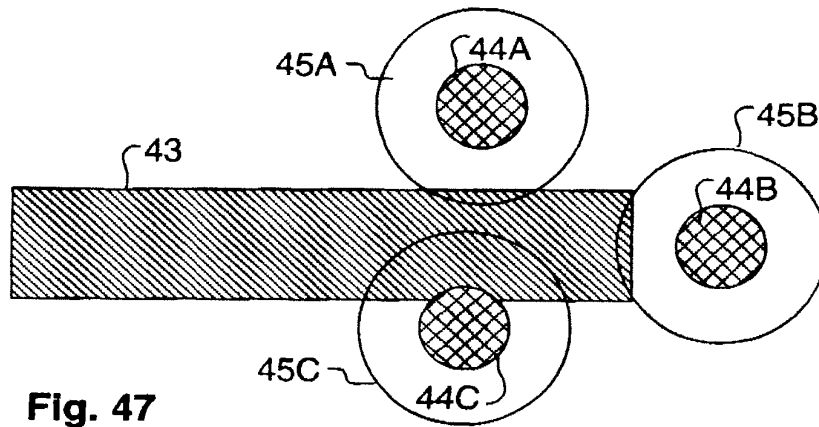


Fig. 47

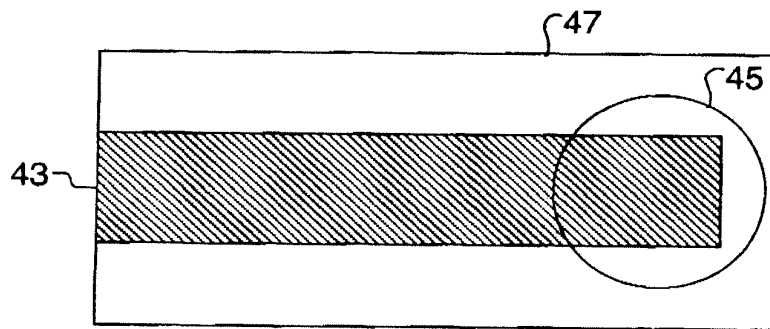


Fig. 48

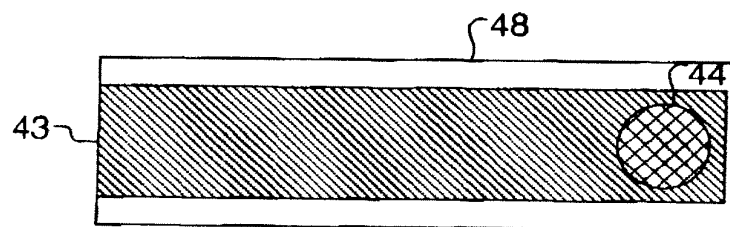


Fig. 49

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371		ATTORNEY'S DOCKET NUMBER IMB 22 US
		U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
INTERNATIONAL APPLICATION NO. PCT/FI2009/050383	INTERNATIONAL FILING DATE 2009-05-11	PRIORITY DATE CLAIMED 2008-05-12
TITLE OF INVENTION CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
APPLICANT(S) FOR DO/EO/US Petteri Palm et al		
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:		
1. ☒ This is a FIRST submission of items concerning a submission under 35 U.S.C. 371.		
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a submission under 35 U.S.C. 371.		
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.		
4. ☒ The US has been elected (Article 31).		
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))		
a. ☐ is attached hereto (required only if not communicated by the International Bureau).		
b. ☒ has been communicated by the International Bureau.		
c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).		
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).		
a. ☒ is attached hereto.		
b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).		
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))		
a. ☐ are attached hereto (required only if not communicated by the International Bureau).		
b. ☐ have been communicated by the International Bureau.		
c. ☒ have not been made; however, the time limit for making such amendments has NOT expired.		
d. ☐ have not been made and will not be made.		
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).		
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).		
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).		
Items 11 to 20 below concern document(s) or information included:		
11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.		
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.		
13. ☒ A preliminary amendment.		
14. ☒ An Application Data Sheet under 37 CFR 1.76.		
15. ☐ A substitute specification.		
16. ☒ A power of attorney and/or change of address letter.		
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.3 and 37 CFR 1.821- 1.825.		
18. ☐ A second copy of the published International Application under 35 U.S.C. 154(d)(4).		
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).		

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering information, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEE S OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO. PCT/FI2009/050383	ATTORNEY'S DOCKET NUMBER IMB 22 US
20. Other items or information:		
The following fees have been submitted		CALCULATIONS
21. ☒ Basic national fee (37 CFR 1.492(a))..... \$330		\$ 330
22. ☒ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4)..... \$0 All other situations..... \$220		\$ 220
23. ☒ Search fee (37 CFR 1.492(b)) If the written opinion of the ISA/US or the International preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4)..... \$0 Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority..... \$100 International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB..... \$430 All other situations..... \$540		\$ 430
TOTAL OF 21, 22 and 23 =		980
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). The fee is \$270 for each additional 50 sheets of paper or fraction thereof.		
Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to a whole number)
- 100 =	/50 =	x \$270
Surcharge of \$130.00 for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).		\$
CLAIMS	NUMBER FILED	NUMBER EXTRA
Total claims	35 - 20 =	15
Independent claims	2 - 3 =	0
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		+ \$390
TOTAL OF ABOVE CALCULATIONS =		\$ 1760
☐ Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by 1/2.		
SUBTOTAL =		\$ 1760
Processing fee of \$130.00 for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)).		\$
TOTAL NATIONAL FEE =		\$ 1760
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property		\$
TOTAL FEES ENCLOSED =		\$ 1760
		Amount to be refunded:
		\$
		Amount to be charged
		\$

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

- a. ☐ A check in the amount of \$ _____ to cover the above fees is enclosed.
- b. ☐ Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees.
- c. ☐ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. _____.
- d. ☒ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended paying fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

SEND ALL CORRESPONDENCE TO:

Customer Number 95002

/Joshua P. Wert Reg. No. 65880/

SIGNATURE

Joshua P. Wert

NAME

65880

REGISTRATION NUMBER

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US
		Application Number	
Title of Invention	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Petteri		Palm		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Helsinki	Country Of Residence	FI		
Citizenship under 37 CFR 1.41(b) i		FI			
Mailing Address of Applicant:					
Address 1	Alkutie 47 as. 1				
Address 2					
City	Helsinki	State/Province			
Postal Code	FI-00660	Country	FI		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Risto		Tuominen		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Espoo	Country Of Residence	FI		
Citizenship under 37 CFR 1.41(b) i		FI			
Mailing Address of Applicant:					
Address 1	c/o Imbera Electronics Oy, Ruukintie 2				
Address 2					
City	Espoo	State/Province			
Postal Code	FI-02330	Country	FI		
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Antti		lihol		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Helsinki	Country Of Residence	FI		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US
		Application Number	
Title of Invention	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		

Citizenship under 37 CFR 1.41(b) i		FI	
Mailing Address of Applicant:			
Address 1	Hiomotie 18 B 40		
Address 2			
City	Helsinki	State/Province	
Postal Code	FI-00380	Country	FI
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.			<input type="button" value="Add"/>

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	95002
Email Address	Posti@seppolaine.fi <input type="button" value="Add Email"/> <input type="button" value="Remove Email"/>

Application Information:

Title of the Invention	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
Attorney Docket Number	IMB 22 US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	8

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IMB 22 US
		Application Number	
Title of Invention	CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME		
Customer Number	95002		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/FI2009/050383	2009-05-11
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
20085443	FI	2008-05-12	☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.			
Assignee 1			Remove
If the Assignee is an Organization check here. ☒			
Organization Name	Imbera Electronics Oy		
Mailing Address Information:			
Address 1	Ruukintie 2		
Address 2			
City	Espoo	State/Province	
Country ⁱ	FI	Postal Code	FI-02330
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		IMB 22 US	
		Application Number			
Title of Invention		CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME			
Signature		/Joshua P. Wert Reg. No 65880/		Date (YYYY-MM-DD)	
				2010-11-01	
First Name	Joshua	Last Name	Wert	Registration Number	65880

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



(43) International Publication Date
19 November 2009 (19.11.2009)

(10) International Publication Number
WO 2009/138560 A1

- (51) **International Patent Classification:**
H01L 21/60 (2006.01) *H01L 23/538* (2006.01)
- (21) **International Application Number:**
PCT/FI2009/050383
- (22) **International Filing Date:**
11 May 2009 (11.05.2009)
- (25) **Filing Language:** Finnish
- (26) **Publication Language:** English
- (30) **Priority Data:**
20085443 12 May 2008 (12.05.2008) FI
- (71) **Applicant (for all designated States except US):** **IMBERA ELECTRONICS OY** [FI/FI]; Ruukintie 2, FI-02330 Espoo (FI).
- (72) **Inventors; and**
- (75) **Inventors/Applicants (for US only):** **PALM, Petteri** [FI/FI]; Alkutie 47 as. 1, FI-00660 Helsinki (FI). **TUOMINEN, Risto** [FI/FI]; c/o Imbera Electronics Oy, Ruukintie 2, FI-02330 Espoo (FI). **IIHOLA, Antti** [FI/FI]; Takomotie 14 A 6, FI-00380 Helsinki (FI).
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- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM,

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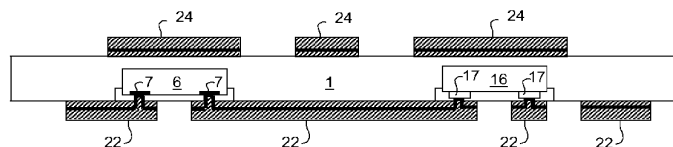


Fig. 8

(57) **Abstract:** Manufacturing method and circuit module, which comprises an insulator layer (1) and, inside the insulator layer (1), at least one component (6), which comprises contact areas (7), the material of which contains a first metal. On the surface of the insulator layer (1) are conductors (22), which comprise at least a first layer (12) and a second layer (32), in such a way that at least the second layer (32) contains a second metal. The circuit module comprises contact elements between the contact areas (7) and the conductors (22) for forming electrical contacts. The contact elements, for their part, comprise, on the surface of the material of the contact area (7), an intermediate layer (2), which contains a third metal, in such a way that the first, second, and third metals are different metals and the contact surface area ($A_{CONTACT}$), between the intermediate layer (2) and the contact area (7) is less than the surface area (A_{PAD}) of the contact area (7).

WO 2009/138560 A1

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Technical Field

5 The present invention relates to circuit modules, which comprise an insulator layer and, inside the insulator layer, at least one component, which comprises contact areas. In addition, the circuit modules comprise conductors on the surface of the insulator layer, through which a component can be connected to become part of a circuit outside the component. For creating electrical contacts, the circuit modules comprise contact
10 elements between the contact areas of the component and the conductors.

The invention also relates to methods for manufacturing the aforementioned circuit modules.

15

Background Art

In the background art, several different ways are described, by means of which circuit modules containing components located inside an insulator material can be manufactured. The background art also discloses several solutions for manufacturing
20 electrical contacts to the contact terminals of a component, by means of contact elements, and methods for manufacturing a conductor-pattern layer connected to the contact elements.

When evaluating circuit modules and manufacturing methods, attention can be paid, for
25 example, to the circuit module's properties achieved by the method, for example, its price, mechanical durability, and the thickness (thinness) that can be achieved. Depending on the applications, significant factors can also be the quality and durability of the electrical contacts and the reliability and quality of the electrical properties of the whole module. Significant properties to be examined in terms of manufacturing can also
30 be, for example, the reliability, yield, efficiency, price, and environmental friendliness of the manufacturing methods to be used. The practicability of the manufacturing method is also affected by the availability of raw materials and the ability of the method to place

different types of component in a circuit module.

All in all, the requirements set for manufacturing methods and circuit modules are thus very diverse and vary according to the application. This being the case, there is still a
5 need in the sector to develop new circuit-module structures and manufacturing methods, which can offer new or improved properties, or combinations of properties.

One line of development has been the placing of components inside the electronics module in a bumpless form, i.e. without growing bumps of top of the contact areas of the
10 component. Cost benefits can then be gained, as the components need no longer be transported during manufacture to a separate production plant to make the bumps.

The applicant's own patent and application publications disclose manufacturing techniques, which can also be used in connection with bump-free components. The
15 techniques described are particularly suitable for components, in which the material of the contact areas is copper. Of the applicant's own publications, those that can be referred to as most closely relating to the invention are the international patent application publications WO 2004/089048, WO 2005/027602, WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217, and
20 WO 2007/107630.

However, at present copper is quite little used as a conductor material in semiconductor processes. The most common conductor material is aluminium. In circuit-board manufacture, on the other hand, copper is the principal material for conductors. Copper
25 conductors of a circuit module can be grown directly on top of aluminium contact areas, but the contact between copper and aluminium is brittle, so that a module of this kind is not optimal in applications, in which mechanical stress acts on the circuit module.

An improved possibility to use contact areas of aluminium or contact areas containing
30 aluminium would mean that, in circuit modules and manufacturing methods, normal semiconductor circuits in a bumpless form could be used immediately after the semiconductor manufacturing processes and the passivation of the surface. As

aluminium is the conductor material most widely used in the semiconductor industry, good compatibility between the contact element of the circuit module and aluminium would also ensure that suitable semiconductor circuits would be abundantly and economically available. Attempts to develop such manufacturing methods have indeed
5 already been made for several decades in the field of component packaging technology. In component packaging solutions of this kind, the goal has been a technique, by means of which a relatively small component package could be manufactured around a component, to which a circuit board could then be attached later. Unlike packaging technology, the goal of the manufacturing techniques of the circuit module to which the
10 present invention relates is the ability to manufacture the entire circuit board in the same process, so as to completely eliminate the packaging stage of the separate component. Of course, this does not exclude the possibility of using the manufacturing method of the circuit module to manufacture only a component package.

15 The patent US 4 246 595, Noyori et al., discloses a method, in which the contact areas of a component are brought into contact with an insulator sheet, in which V-shaped openings have been made. First of all, a layer of titanium (Ti) or chromium (Cr) is grown on the surfaces of the openings and the aluminium contact areas. This intermediate metal layer is intended to prevent the copper from diffusing into the
20 aluminium and the semiconductor component, as well as to improve the adhesion between the copper and the aluminium. In addition, the intermediate layer acts as an electrical conductor later during electrochemical growing (electroplating), so that the intermediate metal layer will reliably cover also the side walls of the openings. The growing of the titanium or chromium layer requires the use of the sputtering technique,
25 for which reason the openings must also have a clear V shape. Sputtering is expensive when used on large surfaces (on circuit modules) while additionally the open V shape reduces the available conducting density. Contract structures of a corresponding type are also disclosed in patents US 4 783 695 and US 4 894 115, Eichelberger et al., and in patent US 5 353 195, Fillion et al.

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Later, in patent US 6 396 148, Eichelberger et al., an attempt is made to solve the problems relating to sputtering, by forming the intermediate metal layer by growing a

layer of nickel on the surface of the aluminium contact areas. According to the patent, the growing of the nickel is performed by means of a chemical growing method (electroless plating). Yet another layer, which also covers the side walls of the openings made in the insulating material for the contacts, is growing on top of the nickel layer by means of a chemical growing method. In the method, the components are attached first by their side and rear surfaces to the insulator layer and, after this, a photo-patternable polymer is spread on the front surface of the component and on top of the contact areas. The polymer is patterned by exposing it to light and developing it, to form openings for the contacts.

One possibility is to grow bumps on the surface of the conductors of the circuit-board part of the circuit module and attach the component to the conductors by a flip-chip mounting technique, for example, by ultrasound bonding. Such a method is disclosed in the applicant's own international patent application WO 2006/134220. Problems relating to both production and the quality of the contacts are associated with methods using flip-chip methods.

Disclosure of Invention

The object of the invention is to develop a new contact-element structure envisaging the utilization of bumpless components, as well as a circuit module and manufacturing technique using such a structure.

According to an aspect of the invention, a bumpless component is used in the circuit module, the material of the contact areas of which being of a different metal, or metal alloy to the conductors of the conductor layer of the circuit module. The contact areas of the component and the conductors of the circuit module are connected to each other with the aid of contact elements, which contain an intermediate layer, which contains a third metal or metal alloy, which differs from the material of the contact areas and conductors, on the surface of the material of the contact area. In addition, the contact surface area between the intermediate layer of each contact element and the contact area of the component is smaller than the surface area of the contact area.

According to another aspect of the invention, a manufacturing method is created in order to manufacture the circuit module described above, in which the component is attached to a conductor foil or conductor-pattern layer with the aid of a polymer layer and contact elements are made through the polymer layer. When making the contact elements, contact holes are made in the polymer layer on top of the contact areas, at the locations of the contact areas. The contact holes are dimensioned in such a way that the contact surface area between each contact hole and the corresponding contact area is smaller than the total surface area of the contact area. After this, the contact holes are filled with a conductor material, in such a way that filling is started by coating the surface of the contact areas with an intermediate layer, for example, by using one or more chemical metal-growing methods.

Thus, a new type of circuit module and manufacturing method is obtained, which can offer some advantages in terms of the applications of some circuit modules.

In addition, the invention has numerous special embodiments, which provide additional advantages.

In one embodiment, components are used in the circuit module, the material of the contact areas of which contains aluminium and the contact elements comprise a layer containing zinc on the surface of these contact areas containing aluminium. In addition, the contact elements are manufactured in such a way that the contact surface area between the layer containing zinc and the contact area is smaller than the total surface area of the actual contact area.

A layer containing zinc has been observed to be useful in terms of the quality of the electrical contact, as coating a layer containing zinc on the surface of an aluminium contact area prevents the re-oxidation of the aluminium surface and permits the creation of good adhesion between the aluminium and the next layer. In addition, the layer containing zinc improves the mechanical durability against lateral stress of the contact formed through the interface between the aluminium and the intermediate layer of other

metal.

5 We have observed that extremely good mechanical durability is achieved by using a double zincate process, in which the blank containing the components is subjected to the zincate process at least twice. Thus a more even and denser layer of zinc is made to grow on top of the aluminium contact surfaces. After a single zincate treatment, there is zinc on only some areas of the contact surfaces, or else the layer is porous, therefore a double zincate process is used in the preferred embodiment.

10 The possibility to use contact elements that are narrower than the contact area can, for its part, provide advantages, for example, by allowing the conductors connected to the contact elements to also be made narrow, especially in embodiments, in which the contact element is essentially of even width vertically, or only narrows moderately towards the component.

15 In an embodiment of the manufacturing process, in which contact openings are made in the conductor foil of the conductor-pattern layer prior to attaching the component, the component can be attached aligned relative to the contact openings while, in addition, the contact holes needed for the manufacture of the contact elements can be made through these contact openings, by using the material of the conductor foil or conductor-pattern layer as a mask. In such an embodiment, an advantage is obtained in the case of the alignment between the contact elements and the contact areas. In addition, an advantage is obtained in terms of the manufacture of the contact holes, because the holes can be opened using a CO₂ laser, for example.

25 In an embodiment, in which the contact holes are opened using a laser, the contact holes can be opened one component or component-group at a time, and thus the first intermediate layer can be manufactured first through the contact holes, on top of the contact areas of the first components, and then later the second intermediate layer can be manufactured through the contact holes opened later, on top of the contact areas of the second components. Thus, components, the materials of the contact areas of which differ from each other and are incompatible with the growth processes of the same

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intermediate layer, can be fitted in the same process.

In the embodiments, it is also possible to attach the components to the conductors by means of mutually differing polymer layers. Thus the properties of the insulation
5 between the component and the conductor can be arranged to also be suitable for different mechanical and electrical requirements.

Brief Description of Drawings

10 Figures 1 - 8 show the intermediate stages of a circuit module when using a manufacturing method according to one embodiment.

Figure 9 shows one example of a circuit module according to one embodiment.

15 Figures 10 - 17 show the intermediate stages of a circuit module when using a manufacturing method according to a second embodiment.

Figures 18 - 23 show the intermediate stages of a circuit module when using a manufacturing method according to a third embodiment.

20 Figure 24 shows one intermediate stage of a circuit module when using a manufacturing method according to a fourth embodiment.

25 Figure 25 shows one possible example of a contact hole and its dimensions made for a contact element of a circuit module.

Figure 26 shows examples of possible contact holes.

30 Figure 27 shows some embodiments of intermediate layers manufactured in the contact hole of Figure 26.

Figure 28 shows one contact-element structure.

Figure 29 shows a second contact-element structure.

Figure 30 shows a third contact-element structure.

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Figure 31 shows a fourth contact-element structure.

Figure 32 shows a fifth contact-element structure.

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Figure 33 shows a sixth contact-element structure.

Modes for Carrying Out the Invention

15 Figures 1 - 9 show one exemplary application of the manufacturing method according to one embodiment. In this embodiment, manufacture begins from a conductor foil 12, which of metal, for example. A suitable conductor foil 12 is, for example, a copper film, the thickness of which is in the range 1 - 70 μm , typically in the range 3 - 12 μm . Instead of a bare conductor foil 12, it is also possible to use as the base material a layered sheet, which comprises a conductor foil 12 and an insulator layer 13, which is shown by a broken line in Figure 1, on the surface of this. In the embodiments described in the following, it is possible to use such a layered sheet 12, 13, in place of the conductor foil 12.

25 Differing from what is shown in Figure 1, it is also possible to use a layered sheet, which comprises a support membrane on the second surface of the conductor foil 12. The support membrane is on the opposite surface of the conductor foil relative to the components to be attached to the conductor foil. If the layered sheet also comprises an insulator layer 13, the support membrane will then be on the opposite side of the conductor foil to the insulator membrane 13. The support membrane can be used, for example, to improve the mechanical stiffness and ease of handling at the start of the manufacturing process of the conductor foil 12, or the layered sheet 12, 13. The support membrane is, however, intended to be removed at a later stage in the process. It is also

30

possible to proceed by starting manufacture from a support membrane while a conductor foil 12, which is patterned or unpatterned, is made on the surface of this. The process examples and stages described in the application example can also be performed correspondingly when using a support membrane, though this is not stated separately. In the description hereinafter, however, reference will be made to a support membrane only when calling attention to something particularly noteworthy in the case of an embodiment using a support membrane. The actual support membrane can be, for example, of an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer. The thickness of the support membrane can be, for example, 25 - 400 μm . The thickness of the support membrane is typically in the range 35 - 105 μm .

Next, contact openings 8 are made in the conductor foil 12, which are located on the conductor foil 12 in such a way that they are placed at the positions of the contact terminals of the components being placed in the module being manufactured. Thus, an individual contact opening 8 is made in the conductor foil 12 for each contact terminal of the component. In this embodiment, the contact openings 8 can be manufactured with the aid of a UV laser. The contact openings 8 can also be manufactured, for example, mechanically by drilling, milling, or etching. In an embodiment using a support membrane, the contact openings 8 are preferably made from the direction of the opposite surface, in such a way that they penetrate the conductor foil 12 completely. However, the contact openings need not penetrate the sheet, instead the method can equally well also be designed in such a way that the contact openings 8 only extend as far as the surface of the material of the support membrane, or form recesses in the material of the support membrane, without, however, passing entirely through it. Also, the contact openings need not pass entirely through the conductor foil, if a thick conductor foil is used, which is thinned by etching in a later stage.

In the embodiment of Figure 1, the contact openings 8 are manufactured in such a way that the size of a contact opening 8 is less than the contact surface area of the contact material to be placed at the opening 8. The contact opening is typically circular in shape, though other shapes too can be used. The shape and size of the contact opening 8 are

selected in such a way that the contact surface of the contact terminal can cover the contact opening 8 entirely.

5 According to Figure 2, manufacture is continued by spreading adhesive layers 5 on the surface of the conductor foil 12, in the connection areas of the components. The adhesive layers will then also cover the contact openings 8. Alternatively, the adhesive 5 can be spread on the surface of the components. The adhesive can also be spread on the surface of both the component and the conductor foil 12. Typically, the adhesive is spread locally, so that the adhesive layers 5 will be located only in the connection areas
10 of the components.

The term adhesive refers to a material, by means of which the components can be attached to the conductor foil 12 or insulator layer 13 that acts as a base. One property of the adhesive is that the adhesive can be spread on the surface to be glued in a relatively
15 fluid form, or one that otherwise conforms to the surface shapes, for example, in the form of a film. A second property of the adhesive is that, after spreading, the adhesive hardens, or can be hardened, at least partly, in such a way that the adhesive is able to hold the component in place (relative to the conductor foil 12) at least until the component is secured to the construction in some other way. A third property of the
20 adhesive is an adhesive capability, i.e. an ability to stick to the surfaces being glued.

The term gluing, for its part, refers to the attachment of pieces to be glued to each other with the aid of an adhesive. In the embodiments, the adhesive is brought between the component and the conductor foil 12 or insulator layer 13 acting as a base and the
25 component is placed in a suitable position relative to the base, in which the adhesive is in contact with the component and the base and at least partly fills the space between the component and the base. After this, the adhesive is allowed (at least partly) to harden, or the adhesive is (at least partly) actively hardened, so that the component attaches to its base with the aid of the adhesive. In some embodiments, the contact protrusions of the
30 component may protrude during gluing through the adhesive layer to come into contact with the base.

The adhesive used in the embodiments is typically an epoxy-based adhesive, for example a heat-cured epoxy adhesive. The adhesive is selected in such a way that the adhesive to be used will have sufficient adhesion to the base and the component. One preferred property of the adhesive is a suitable coefficient of thermal expansion, so that
5 the thermal expansion of the adhesive will not differ too much from the thermal expansion of the surrounding material during the process. It would also be preferable for the adhesive selected to have a short hardening time, preferably of a few seconds at most. Within this time, it would be good for adhesive to harden at least partly, so that the adhesive can hold the component in place. Final hardening can take a clearly longer time
10 and can even be planned to take place in connection with later process stages. In addition, the stresses caused by the later process stages, such as thermal, chemical, or mechanical stress, are taken into account when selecting the adhesive. The electrical conductivity of the adhesive will be preferably in the order of the electrical conductivity of the insulator materials.

15
Next, components 6 and 16, which comprise contact terminals 7 and 17, are taken. Both components 6 and 16 are semiconductor components, for example, processors, memory chips, or other microcircuits. The contact terminals of the component 6 are contact areas 7, which are located essentially on the level of the surface of the component. Such
20 contact areas 7 of the component 6 are created at the semiconductor factory during the manufacturing process of the semiconductor component. The contact area 7 typically forms the surface of a conductor pattern on the metal used in the process. The metal used in the manufacturing process of semiconductor components is typically aluminium, though other metals, metal alloys, or other conductor materials can also be used. For
25 example, the use of copper has become common in semiconductor-component manufacturing processes.

The contact terminals of the component 16 are contact bumps 7, which protrude from the level of the surface of the component. Such contact bumps 17 are manufactured in a
30 bump-making process after the manufacture of the semiconductor component 16, typically in a separate factory. The contact bump 17 can contain one or more metals, metal alloys, or other conductor materials. Typically, the outer surface of the contact

bump 17, i.e. the contact surface, is made from copper or gold.

5 The components 6 and 16 are aligned relative to the contact openings 8, in such a way that each contact terminal 7, 17 comes next to the corresponding contact opening 8, and is pressed against the adhesive layer 5. After this, the adhesive is at least partly hardened, so as to prevent, or minimize the relative movement of the components 6, 16 and the conductor foil 12 after alignment. In alignment and gluing, the aim is to position the contact opening 8 to be in the centre of the corresponding contact terminal 7, 17.

10 After this, insulator sheets 11, in which openings are made for the components 6, 16, as well as a unified insulator sheet 10, which is of unhardened or pre-hardened polymer, are laminated on top of the conductor foil 12. During lamination, the insulator sheets 10, 11 are melted together and form a unified insulator layer 1 around the components 6, 16. In the embodiment of Figure 2, the insulator sheets 11 are fibre mats impregnated with polymer, or sheets containing pre-hardened polymer and reinforced with a fibre material.
15 The polymer can be, for example, epoxy and the fibre reinforcement can be, for example, glass-fibre mat. A typical example of a suitable insulating-sheet 11 material is an FR4-type glass-fibre reinforced epoxy sheet. Other reinforcement and polymer material combinations can be used, of course. When using several insulator sheets 11,
20 the sheets can also differ mutually.

In Figures 2 and 3, the fibre material is shown by wavy shading 19. In the figures hereinafter, the fibre material 19 is not shown, but these structures too include fibre material 19. The fibre material 19 contained in the insulator sheet 11 or the insulator sheets 11 acts as a reinforcement, which provides the electronic module being
25 manufactured with mechanical strength. According to the example of Figure 2, holes 4 are made in the insulator sheets 11 at the locations of the components 6, 16. The insulator sheets 11 are perforated particularly to make openings for components in the fibre material 19 contained in the insulator sheets 11. Without perforation, the components would press against the fibre-material layers 19 during lamination. The
30 unperforated insulator sheet 10, on the other hand, can be fibre-reinforced or unreinforced, depending on the embodiment.

The insulator sheets 10, 11 are typically selected in such a way that they contain enough fluid polymer for the polymer flowing in the lamination stage to be sufficient to fill the holes 4 made in the insulator sheets 11 for the component 6, 16, around the components.

5 The structure shown in Figure 3 is then obtained, in which the insulator layer 1 contains a tight polymer layer, which contains one or more reinforcements of a fibre material 19. The polymer layer is bound tightly to the fibre layer 19 while the tight polymer layer also attaches the components 6, 16 to the surfaces, so that a tight, unified, and mechanically strong insulator layer is formed, which contains the components 6, 16, and
10 which is, in addition, reinforced with fibre material 19.

In the example of Figure 2, a unified insulator sheet 10 is used, though the insulator sheet 10 can also be omitted from the structure. In that case, the insulator sheet 11 or insulator sheets 11 are selected in such a way that they themselves already contain
15 sufficient fluid polymer to fill the holes 4 in the insulator sheets 11 around the components 6, 16. However, it is typically easier to ensure the filling of the holes 4 by using a separate insulator sheet 10.

A conductor foil 14, which is preferably of a material that is similar to, and equally as
20 thick as the conductor foil 12, is also laminated with the insulator sheets 10, 11 into a single structure. Thus, the insulator layer 1 and the components 6, 16 remains between the corresponding conductor foils 12 and 14. Figure 3 shows this intermediate stage of the module manufacture. In the intermediate stage of Figure 3, there is adhesive on the contact surface of the contact terminals 7, 17 and typically also in the contact openings
25 18. In the stage shown in Figure 4, this adhesive is removed and contact holes 18, which extend to the contact surfaces of the contact terminals 7, 17 are formed at the positions of the contact openings 8.

With reference to Figure 3, it can be further stated that the structure can also be
30 manufactured in such a way that a unified layer of fibre material 19 runs between the components 6, 16 and the conductor foil 14. Such a construction can be used when the thickness of the components 6, 16 is sufficiently less than the thickness of the insulator

layer 1. The structure can be manufactured, for example, in such a way that a unified insulator sheet 10, which contains the fibre material 19 of the layer, can be laminated onto the structure.

5 If a support membrane is used in the embodiment on the surface of the conductor foil 12, as depicted in connection with the description of Figure 1, it is most suitable to remove the support membrane after the lamination, i.e. between the intermediate stages shown in Figures 3 and 4.

10 After lamination and the removal of the possible support layer, the adhesive layer, which has been created in the contact openings 8 and between the contact openings 8 and the contact terminals 7, 17, is removed. In the embodiment of the figures, the removal of the adhesive is implemented by the laser-ablation method, using a CO₂ laser. The ability of a CO₂ laser to vaporize organic insulating substances, such as epoxy-base adhesive, is
15 good, but its ability to vaporize copper or other metals is poor, so that the conductor foil 12 can be used as mask for making the contact holes 18. Thus, it is possible to manufacture contact holes 18, the diameter of which is less than the diameter of the beam of the CO₂ laser. This property creates a significant advantage, as the minimum diameter of the beam of a CO₂ laser is typically in the order of 75 µm, which is too large
20 when considering the manufacture of precise electronic module structures. A UV laser, on the other hand, can typically be used to manufacture clearly more precise structures. The minimum diameter of the beam of a UV laser can be, for example 25 µm, but a UV laser is not, on the other hand, suitable for removing adhesive from the contact openings 8 and from between the contact openings 8 and the contact terminals 7, 17.

25 Thus, the use of a conductor mask permits the manufacture of very precisely limited and precisely positioned contact holes 18 in an insulator material, such as the adhesive 5 using in the embodiment. In addition, the use of a CO₂ laser permits the cleaning of the contact surfaces of the contact terminals 7, 17 in the same process stage, without any
30 significant danger of destroying or damaging the contact terminals 7, 17. In the embodiment, the conductor foil 12 is of copper while the contact terminals 7, 17 of the component are also of metal, so that they are not sensitive to the beam of the CO₂ laser,

so that the process can be designed in such a way that the contact surfaces of the contact terminals 7, 17 will be sure to be cleaned sufficiently well. Thus, the advantage of the method described is that contact openings 8 can be made in the conductor foil 12 very precisely with the aid of a UV laser and, after this, the contact openings can be used as a mask for the making of the contact holes 18 by means of a CO₂ laser that is less precise, but safer for the structure.

If the contact holes 8 of the conductor foil 12 were to be manufactured only in this process stage, the method used for machining the metal of the conductor foil 12, for example, a UV laser, would more easily damage also the contact terminals 7, 17, because the energy required to penetrate the conductor foil 12 is significantly greater than the energy required to penetrate the adhesive or other insulation between the contact terminals 7, 17 and the conductor foil 12. In such a manufacturing method, it would be challenging to stop the drilling at precisely the correct depth. In addition, aligning the drilling would be more difficult, due to the deformations arising during lamination and for the reason that the contact terminals 7, 17 of the components cannot be seen through the solid metal film. The use of contact holes 8 pre-manufactured in the conductor foil 12 provides significant advantages, both in the alignment of the components 7, 17 and in the manufacture of the contact holes 18.

In Figure 5, an intermediate layer 2, which is of a suitable conductor material, is made in the contact holes 18. The intermediate layer 2 is manufactured using a suitable chemical conductor-material growing method (electroless plating). The intermediate layer 2 can also consist of a layer of two or more different materials, which are manufactured correspondingly using two or more methods. One purpose of the intermediate layer 2 is to form a conductor membrane for the side walls of the contact holes 18, which connects the contact terminals 7, 17 and the conductor foil 12 to each other. A second purpose of the intermediate layer 2 is to provide a material adapter between the material of the of the contact terminals 7, 17 and the conductor-pattern material to be connected to them. Such a material adapter can be required, for example, in order to ensure the quality of the mechanical or electrical contact and durability, for example, when the material of the conductor-pattern layers of the circuit module is copper and the material of the contact

terminals 7, 17 is something other than copper (Cu), for example aluminium (Al).

When manufacturing the intermediate layer 2, a suitable chemical growing method is used, because by means of such a method the conductor material can also be grown on the vertical surfaces of the contact holes 18, unlike when using sputtering, for example. An electrochemical method (electroplating) cannot be used in this stage, because the side walls of the contact holes 18 are not conducting. Alternatively, V-shaped-opening contact holes can be used and the intermediate layer 2 made by sputtering. Sputterable materials suitable for this purpose are, for example, titanium-wolfram (TiW) and chromium (Cr). A layer of nickel (Ni) and gold (Au) can also be grown on top of the TiW or Cr layer. In the example of Figure 5, nickel grown by a chemical method is used as the intermediate layer 2 in the example of Figure 5, however, so that the intermediate layer 2 will grow at the same time also on the surfaces of the conductor foils 12 and 14. Another example of the intermediate layer 2 is a layer containing zinc, manufactured on the surface of the contact terminals 7, 17, on top of which a layer of nickel (Ni) can further be manufactured. More alternatives that are possible are depicted in connection with the description of Figures 26 - 33.

In this embodiment, after the manufacture of the intermediate layer 2, manufacture is continued by spreading resist layers 3, typically photoresist layers, on both surfaces of the module. The resist layers 3 are patterned with the aid of a conductor-pattern mask by exposure and development, in such a way that the resist 3 is removed from the desired parts of the conductor patterns of the conductor-pattern layers. This intermediate stage is shown in Figure 6. After this, the module is taken to an electrochemical bath and voltage is led to the intermediate layers 2 of the module. The desired conductors of the conductor-pattern layer are then grown in the openings of the resist layers 3. The conductor material also grows in the contact holes 18, forming a conductor core to the contact elements, as can be seen from Figure 7. In the example of Figure 7, the conductors 22, 24 are electrochemically grown copper. Finally, thin etching-mask layers are grown on the surface of the conductors 22, 24. A layer of tin (Sn), for example, can act as the etching mask.

- Next, the resist layers 3 are removed, when, in the embodiment of the figures, the intermediate layer 2 is revealed from under the removed resist. The revealed part of the intermediate layer 2 is removed, for example, by etching, the same procedure being use for the parts of the conductor foils 12 and 14 revealed outer the conductors 22 and 24.
- 5 The etching-mask layer then protects the outermost surfaces of the conductors 22 and 24 from the effects of the etching. An electronic module, which contains two components 6 and 16 connected electrically to conductors 22, comprising two conductor-pattern layers (conductors 22 and 24), and shown in Figure 8, is then obtained.
- 10 In the example of Figures 6 and 7, the conductors 22 and 24 are grown directly into their correct shape in the openings made in the resist layer 3. However, the conductors 22 and 24 can also be manufactured in another way, both in this example and in the examples described hereinafter. One alternative way of manufacture is to grow a unified layer of conductor material over the surfaces of the entire module blank and to pattern the
- 15 conductor layer later by means of a lithography method, in order to form the conductors 22 and 24. Described in greater detail, it is possible to proceed, for example, in such a way that, continuing from the intermediate stage of Figure 5, copper is grown on the surfaces of both intermediate layers 2 by means of an electrochemical method. In that case, the contact holes 18 too are filled with copper. After this, resist layers are spread
- 20 on top of the copper layers, the resists are patterned, and the excess parts of copper, or the intermediate layer 2 and the conductor foils 12 and 14 are etched. After this, the resist mask is removed. Using either manufacturing method, the result is the structure shown in Figure 8.
- 25 Figure 8 can show an already finished simple circuit module, but manufacture is usually continued by manufacturing additional insulator and conductor layers on the surfaces of the circuit module, which are connected electrically with the aid of vias to the structure shown in Figure 8. In addition, it should be noted that vias can be manufactured in the module too of Figure 8, which connect the conductors 22 to the conductors 24. Such vias
- 30 can be manufactured in a corresponding manner to, and in the same process stages as described above in the manufacture of the contact elements.

The module of Figure 8 can be further refined in the manner shown in Figure 9, in such a way that the surfaces of the module are protect by protecting layers 20. In addition, in the example of Figure 9, external contact elements, which comprise bases 21 made on top of the conductor patterns 22, 24 and contact balls 23 made on their surfaces, are
5 manufactured in the module.

Figures 10 - 16 show a manufacturing method according to a second embodiment, up to a stage corresponding to the intermediate stage shown in Figure 5. Manufacture can be continued from the intermediate stage of Figure 16, for example, as shown by Figures
10 6 - 9, or suitably also in an alternative manner, in which the material of the conductors 22 and 24 is first of all grown over the entire surface and after that patterned to form conductors 22 and 24. The technical features and parameters presented in connection with the description of Figures 1 - 5 can also be applied in the process stages shown in Figures 10 - 16, so that there is no need to repeat all the details of the manufacturing
15 process and their advantages in the following embodiment. On the other hand, the essential differences between the embodiments shown by Figures 1 - 9 and Figures 10 - 16 are brought out in the following.

In the embodiment of Figures 10 - 16, manufacture starts, as in Figure 1, from a
20 conductor foil 12, in which contact openings 8 are made. After this, a spacer 15 is attached to the future attachment point of the component 6 on the surface of the conductor foil 12. The spacer 15 is of a suitable insulating material, for example, of pre-hardened adhesive or some other polymer, which has sufficient adhesion with the surface of the conductor foil 12. The spacer 15 can also be of hardened polymer, in
25 which case it can be attached to the surface of the conductor foil 12, for example with the aid of separate adhesive.

A spacer 15 can be used for many different reasons. One use of a spacer is to increase the insulating thickness between the component 6 and the conductor foil 12. The need to
30 increase the insulating thickness can be imposed, for example, by the requirements set by the electrical operation of the circuit module or the component 6. In that case, with the aid of the spacer 15 it is possible to set the properties of the insulation between the

component 6 and the conductor foil 12 as desired. The properties selected can be, for example, a desired specific resistance and spark-over resistance, which can be influenced by the selection of the material of the spacer 15 and the adhesive 5. The spacer can also be used to prevent a short-circuit between the component and the conductor foil 12. Such a use will come into question especially in embodiments in which the surface of the component 6 is pressed very close to the conductor foil, when a risk arises of unintended electrical contacts being formed between the conductor structures on the surface of the component and the conductor foil. A spacer can also be used to weaken the capacitive connection between the internal circuit elements of the component 6 and conductors 22 running next to the location of the component 6.

In addition to, or instead of a spacer 15, it is possible to use for the same purpose an insulator layer 13 entirely covering the surface of the conductor foil 12, as described in connection with Figure 1.

In the examples of Figures 10 - 16, a spacer 15 is used in connection with a bumpless component 6, but the contact terminals of a component 16 with bumps must be made to extend closer to the surface of the conductor foil 12, so that a sufficient insulating gap can be ensured between the opposite surface of the component 16 and the conductor foil 14. In the embodiment, spacers 15 selected component-specifically can be placed in the circuit module, in order to optimize the electrical and/or mechanical properties of the circuit-board module. The same module can thus also contain different kinds of spacers 15 and thus spacers 15 can also be used in series production, in order to make components 6, 16 coming from different sources and with different properties to each other compatible with the circuit-board manufacturing process being used. One example of a mechanical property requiring optimization is the thickness of the insulator layer 1 (and at the same time of the entire module), which can be reduced with the aid of suitable selected spacers 15, which can be seen, for example, in Figure 12.

According to Figure 11, manufacture is continued by spreading adhesive layers 5 on the surfaces of the conductor foil 12 and the spacer 15 in the connection areas of the components. The components 6 and 16 are aligned relative to the contact openings 8 and

glued in place. After that, in the example of Figure 11, insulator sheets 10, 11 and a conductor foil 14 are laminated on top of the conductor foil 12. Next, photo-resist layers 30, which are patterned in such a way that openings larger than the contact openings 8 are created at the positions of the contact openings 8, are spread on the surface of the conductor foils 12 and 14, or a coating is made electrophoretically on top of the entire conductor layer. This photo-resist layer 30 is used to limit the growth of an intermediate-layer material grown using a non-selective method to the contact holes and the immediate surroundings of the contact openings 8. Such a procedure can also be used in connection with the example described above, nor, on the other hand, is it essential in the examples of Figures 10 - 16. Figure 12 shows the module after these stages. The contact terminals 7 of the component 6 are covered by both a spacer 15 and adhesive 5. There is adhesive on the surface of the contact bumps 17 of the component 16 and in the corresponding contact openings 8.

In the stage shown in Figure 13, contact holes 18 are made at the positions of the contact openings 8 of the component 6. The contact holes are opened through the spacer 15 and the adhesive layer 5, as far as the contact surfaces of the contact terminals 7. In the embodiment of the figure, the opening of the contact holes 8 is implemented by the laser-ablation method, using a CO₂ laser, as described in connection with Figure 4. In the embodiment of Figures 10 - 16, the important fact is that contact holes are not opened at this stage of the position of the contact terminals 17 of the second component 16.

In the stage shown in Figure 14, an intermediate layer 2, which is of a suitable material, is made in the contact holes 18 of the component 6. The conductor material of the intermediate layer 2 is selected on the basis of the material of the contact terminals 7 of the component 6 and manufactured using a suitable chemical conductor-material growing method. In the example of the figure, the material of the contact terminals 7 of the component is aluminium and the material of the intermediate layer 2 is mainly a metal alloy containing zinc. The principles described in connection with Figure 5 above are applied to the growing of the intermediate layer. Unlike the example of Figure 5, in the case of Figure 14, it is, however, also possible to proceed in such a way that in this

stage the intermediate layer 2 is grown with the aid of a selective method only on the surface of the contact terminals 7, i.e. on the bottom of the contact holes 18 and not on the edges of the contact holes 18. In this embodiment, the intermediate layer 2 coming on the edges of the contact holes 18 is grown later in connection with the growing of the intermediate layer relating to the contact bumps 17 of the component 16. The embodiment using a selective growing method has the advantage that the intermediate layer 2 does not grow on top of the adhesive layer covering the contact bumps 17 of the component 16.

10 Manufacture is continued in the stage shown in Figure 15 by manufacturing contact holes 28 at the positions of the contact openings 8 of the second component 16. After this, the module according to Figure 16 is subjected to a suitable chemical conductor-material growing method. In the example of Figure 15, the growing method is non-selective and the conductor material grows on all the free surfaces of the module and thus also in the contact holes 18 of component 6 and in the contact holes 28 of component 16. However, the photo-resist layer 30 protects the surfaces of the module, so that the intermediate layer 2 grows only in the contact holes 18 and 28 and in their surroundings. After this, the photo-resist and the conductor material that may have grown on its surface is removed. Such an embodiment using a photo-resist layer 30 can be useful, for example, when nickel or some other metal differing from copper is grown in the openings of the photo-resist layer, for example, using a non-selective method. The conductors 22 and 24 can then be manufactured to consist of solely a copper layer.

In other embodiments, suitably selected selective growing methods can also be used and the conductor material is grown only on the surfaces of the contact bumps 17 of the component 16, correspondingly as described above in connection with Figure 14. In any case, at this stage the intermediate layer 2 is grown at least on the surfaces of the contact bumps 17 of the component 16 and on the surfaces of the side walls of the contact holes 28 and, in addition, if desired also on the surface of the intermediate layer 2 connected to the contact terminals 17 of the component 6 and/or on the surfaces of the side walls of the contact holes 18 of the component 6.

If the example of Figures 10 - 16 were to be implemented without the use of a photo-resist 30, in the example of Figure 16 the material of the surface of the contact bumps 17 of the component 16 could suitably also be copper and the material of intermediate layer 2 to be grown of the surface of the contact bumps 17 would then be copper manufactured suitably using a chemical growing method.

After the manufacture of the intermediate layer 2, in this embodiment manufacture can be continued, for example, in the manner stated in connection with the description of Figures 6 - 9, by manufacturing conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28.

Another alternative is to coat copper on both conducting surfaces of the module, after the removal of the photo-resist layer 30. After this, the copper layers can be patterned to form conductors 22 and 24, when the structure shown in Figure 17 will be obtained, in which the conductors 22 and 24 are formed of the first and second copper layers in the surroundings of the contact elements, as well as of an intermediate layer 2, which is of nickel for example, between them. Elsewhere, the conductors 22 and 24 are formed of a first and second copper layer, between which is the interface to be analysed. Once the structure of Figure 17 has been manufactured, it is possible, if desired, to continue in some manner described in connection with any of the previous examples.

Figure 18 - 23 show a manufacturing method according to a third embodiment, which is a variation of the embodiment shown in Figures 10 - 16. From the intermediate stage of Figure 23, manufacture can be continued, for example, in the manner shown in Figures 6 - 9. The technical features and parameters presented in connection with the description of Figures 1 - 5 and 10 - 16 can thus also be applied in the process stages shown in Figures 18 - 23, so that all the details and their advantages of the manufacturing process need not be unnecessarily repeated in the following embodiment. However, in the following the essential difference between the embodiments shown in Figures 10 - 16 and Figures 18 - 23 is presented.

In the embodiment of Figures 18 - 23, manufacture is commenced, as in the case of

Figure 10, from a conductor foil 12, in which contact openings 8 are made. After this, spacers 15 are attached to the surface of the conductor foil 12, to the future attachment points of the components 6 and 26. The spacers 15 of the components 6 and 26 can be mutually identical or selected component specifically, for example, in such a way that the spacer 15 of the component 6 is of a different material and/or thickness to the spacer 15 of the component 26.

According to Figure 18, manufacture is continued by spreading adhesive layers 5 on the connection areas of the components and by laminating insulator sheets 10, 11 and a conductor foil 14 to the blank, exactly as described in connection with Figure 11. Figure 19 show the module after these stages.

In the stage shown in Figure 19, contact holes 18 are made at the positions of the contact openings 8 of the component 6, as described in connection with Figure 13. At this stage, contact holes are not yet opened at the positions of the contact terminals 27 of the component 26.

The stage shown in Figure 21 corresponds completely to the method stage described in connection with Figure 14. In this embodiment, an intermediate layer 2, which is of two layers, is manufactured in the contact holes 18 of the component 6. In the example of the figure, the material of the contact terminals 7 of the component is aluminium. The two-layer intermediate layer 2 of the example comprises first a grown layer containing zinc and after this a grown nickel-aluminium layer. The nickel-aluminium layer is grown by means of a chemical method and is used to seal the layer containing zinc.

Manufacture is continued in the stage shown in Figure 22, by making contact holes 28 at the positions of the contact openings 8 of the second component 26. After this, according to Figure 23 the module is subjected to a suitable chemical conductor-material growing method. This stage corresponds to the method stage described in connection with Figure 16. In the example of Figure 23, the material of the surface of the contact terminals 27 of the component 26 is copper and the material of the intermediate layer 2 grown of the surface of the contact terminals is also copper.

Figure 24, for its part, shows a modification of the embodiment of Figures 18 - 23, in which, after the stage shown by Figure 22, a first intermediate layer is grown on top of the contact terminals 27 of the component 26, by means of a selective growing method and, after this, the growing of the intermediate layer 2 is continued using a non-selective method. In the example of Figure 24, the material on the surface of the contact terminals 27 of the component 26 is gold and the material of the intermediate layer 2 grown on the surface of the contact terminals 27 is nickel.

In the embodiments of these Figures 18 - 24, after the manufacture of the intermediate layers 2 it is possible to continue, for example, by making conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28, for example, by means of the manner stated in connection with the description of Figures 6 - 9.

Figure 25 shows in greater detail the shape of the contact hole and correspondingly also the shape of the contact element to be manufactured in this opening. The example of Figure 25 shows one possible shape, which can be achieved when using the embodiments described above. The shape can be affected with the aid of the shape of the contact openings 8 to be made in the conductor foil 12, the properties of the insulation between the conductor foil 12 and the component, and the operating parameters of the CO₂ laser. The contact hole of Figure 25 is rotationally symmetrical and the cross-section shown in the figure is taken through the central axis of the contact hole, i.e. it shows the widest possible cross-section. In Figure 25, the size and shape of the contact hole are determined with the aid of the following parameters:

- greatest width W_{MAX} , from which the greatest cross-sectional area A_{MAX} can be calculated,
- the width W_{CONT} of the contact between the contact element and the contact surface 7 of the component 6, from which the contact surface-area A_{CONT} between the contact element and the contact surface of the component can be calculated, and

- the width W_{HOLE} of the contact opening, from which the contact surface-area $A_{CONT\ 2}$ between the contact element and the conductor of the conductor-pattern layer can be calculated.

5

The figure also shows the width W_{PAD} of the contact surface of the component, from which the surface area A_{PAD} of the contact surface can be calculated, if the shape of the contact surface is known. The contact surface 7 can be, for example, square in shape and, when W_{PAD} represents the width of a side, the surface area of the contact surface is
 10 obtained as: $A_{PAD} = W_{PAD} \times W_{PAD}$. Of course, the surface areas can also be determined with the aid of surface-area measurement, which can be more practical if the surface area to be determined is of an irregular shape.

In the figure, the contact surface 7 is surrounded by a passivation layer 9 made on the
 15 surface of the component 6. In that case, the surface area A_{PAD} refers precisely to the surface area free to form a contact, i.e. the surface area of the surface that is revealed in the opening made in the passivation layer 9. In addition, the figure shows the distance H of the distance between the conductor foil 12 and the contact surface 7, which corresponds to the depth of the contact hole and is thus the height of the contact element
 20 to be made in the contact hole. Because the contact hole is filled entirely with conductor material, the other dimensions too of the contact hole correspond to the dimensions of the contact element and the parameters W_{MAX} and W_{HOLE} can also be used to refer to the corresponding dimensions of the contact element.

25 The following presents some typical parameters in connection with the embodiments described above:

$H = 1 - 50\ \mu\text{m}$, usually $5 - 30\ \mu\text{m}$;

30 $W_{PAD} = 20 - 1000\ \mu\text{m}$, usually $50 - 200\ \mu\text{m}$, and most usually about $100\ \mu\text{m}$; and

$W_{HOLE} = 5 - 500\ \mu\text{m}$, usually $20 - 75\ \mu\text{m}$, and most usually about $30 - 50\ \mu\text{m}$.

In addition, generally $W_{HOLE} \geq H$, which represents the reliable filling of the contact hole. The contact hole 18 is intended to be manufactured in such a way that the side walls of the hole would be vertical. In other words, the goal is a contact hole, the width and shape of which remains constant over the whole distance H between the conductor foil 12 and the contact surface 7, i.e. the contact hole would have the shape of the contact opening 8 over all of this distance. A shape that narrows towards the contact surface 7 is also good. In practice, when using the laser process described above the contact hole can, however, become widening towards the contact surface 7, or first widening and then narrowing, so that the contact hole is widest somewhere between the conductor foil 12 and the contact surface 7. Figure 25 shows a contact hole of this kind. Such a non-optimal shape is not problematic, provided the widening is not too great and the filling of the hole succeeds well.

Of the dimension values of the widths referred to above, the width W_{PAD} of the contact surface 7 of the component is determined through the selection of the component. If necessary, W_{PAD} can be measured separately from each straight line that runs through the centre point of the contact surface 7. This definition may be required when examining the dimension values referred to above and their ratios, if the shape of the contact surface 7 or of the contact opening 8 is irregular. In the most usual cases, the contact surface is, however, square, in which case the width of the side of the square can generally be used as the width W_{PAD} of the contact surface 7.

The width W_{HOLE} of the contact opening 8 is a parameter, which is selected when planning the manufacturing process. One parameter to be taken into account when selecting the width of the contact opening 8 is the width of the contact surface 7 of the component being used. The width of the contact opening 8 is selected in such a way that the contact hole to be made through the contact opening will meet the contact area 7 of the component over its entire cross-sectional area at the component end, and will not miss the contact area, for example, on the surface of the passivation layer. If the contact opening is circular in shape, with width W_{HOLE} of the contact opening is the diameter measured through the centre point of the circle. If, on the other hand, the contact opening

is irregular I shape, W_{HOLE} can, if necessary, be measured separately along each straight line that runs through the centre point of the contact opening 8. In the case of an irregular shape, when comparing the width W_{HOLE} of the contact opening with the width W_{PAD} of the contact surface, the comparison can always be made separately for each pair
 5 of widths measured through parallel straight lines. If necessary, the widths W_{HOLE} and W_{PAD} can also be compared in a corresponding manner to the other parameters described.

The ratios of the parameters described above can also be applied in connection with the
 10 contact bumps 17, in which case the surface area and width of the contact area will be replaced by the surface area and width of the contact bump and the distance H will be measured to the surface of the contact bump.

The shape of the contact hole can be influenced with the air of the laser parameters,
 15 which are selected according to the hole parameters and the properties of the insulation to be removed. The manufacturing result is, of course, also affected by the laser device being used. The suitability of the selected parameters for the process is indeed examined with the aid of a pilot manufacturing batch and, if necessary, the parameters are altered so that the desired result will be achieved.

20 In general, it is sensible in the manufacturing method to try to achieve a contact-hole shape, in which

$W_{CONT} = 0.5 - 1.5$ times W_{HOLE} , preferably $0.7 - 1.2$ times W_{HOLE} , and most preferably 0.8
 25 $- 1.0$ times W_{HOLE} , however, in such a way that $W_{CONT} < W_{PAD}$; and

$W_{MAX} =$ at most $100\ \mu\text{m}$, preferably at most $30\ \mu$, and most preferably at most $10\ \mu\text{m}$
 larger than whichever of the parameters W_{HOLE} and W_{CONT} is greater. Presented
 relatively, the objective would be for $W_{MAX} =$ at most $40\ \%$, preferably at most $20\ \%$, and
 30 most preferably at most $10\ \%$ greater than whichever of the parameters W_{HOLE} and W_{CONT} is greater.

In the most optimal shape of a contact element, W_{MAX} is essentially as large as W_{HOLE} and, in addition, W_{CONT} is 0 - 20 % smaller than W_{MAX} .

5 In the most typical embodiments, the contact surface 7 has a square shape and the contact opening 8 is circular in shape. In that case, A_{CONT1} is typically 10 - 75 % of the surface area A_{PAD} . A_{CONT1} and A_{CONT2} are typically mutually approximately of equal size, for example, with an accuracy of ± 20 %.

10 Figure 26 shows examples of other possible shapes of the contact holes 18. Figure 27, for its part, shows examples of intermediate layers 2 manufactured in such contact holes. In the examples of Figures 26 and 27, the component to be attached is bumpless. As can be seen from Figure 27, the intermediate layers 2 do not extend at all on top of the passivation layer 9 of the component, but instead are in contact only with the contact surface 7 of the component. With the aid of this feature, it is possible to see even from
15 the finished electronic module whether the component embedded in the electronic module has bumps or is bumpless. The bumps grown on the contact surface 7 of the component in the bump-creation processes always fill the entire contact surface 7 and always also spread slightly on top of the passivation layer 9. If, on the other hand, bumpless components are used in the embodiments described above, the intermediate
20 layer 2 and the contact element grow only into the contact hole 18, when in the finished electronic module the intermediate layer 2 will not extend on top of the component's passivation layer 9 and part of the contact surface 7 of the component will always remain free of the intermediate layer 2 (the edges of the contact surface 7) when the alignment and manufacture of the contact hole 8 have succeeded. Also in a possible
25 contact-hole 18 alignment-error situation, in which the contact opening 8 is not completely aligned with the contact surface 7, at least part of the edge areas of the contact surface 7 and of the passivation layer surrounding the edge area will be free of the intermediate layer 2.

30 If a bumpless component is manufactured by a semiconductor process using copper conductors, the contact area 7 is copper. In that case, the intermediate layer can be manufactured directly from chemically grown copper, which forms a conductor

surfacing also on the side walls of the contact hole 18. After this, the contact holes 18 can be filled and the thickness of the conductor layer increased using an electrochemical copper-growing method.

5 At the moment of writing of the present application, the most commonly used conductor material in semiconductor processes is, however, aluminium. Thus, the most common material of the contact area 7 of bumpless components too is aluminium and it is preferable to use an intermediate layer, with one or more layers manufactured from different materials, between the aluminium contact area and the copper conductors of the
10 electronics module. In the following, reference is made to a few possible intermediate-layer constructions:

Intermediate-layer construction 1

15 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the side walls of the contact hole 18. A layer of nickel, which does not grow at all or only poorly on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical
20 method on the surface of the nickel. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 2

25 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of copper is grown by a chemical method on the surface of the layer containing zinc. The copper grown by a chemical
30 growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 3

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of nickel-aluminium, which does not grow on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical method on the surface of the nickel-aluminium. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 4

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. A layer of nickel-aluminium is grown by a chemical method on the surface of the layer containing zinc. A layer of nickel is grown by a chemical method on the surface of the nickel-aluminium and a layer of copper is grown by a chemical method on the surface of the nickel.

Intermediate-layer construction 5

First of all, a layer containing zinc is grown on the surface of the aluminium contact layer 7. A layer of nickel is grown by a chemical method on the surface of the layer containing zinc.

Intermediate-layer construction 6

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, which grown nickel layer alone forms the intermediate layer 2.

Intermediate-layer construction 7

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, and a layer of copper is grown by a chemical method on the surface of the nickel.

5

In the above examples of intermediate-layer constructions, the layer containing zinc contains, for example, about 80 % zinc, about 16 % copper, about 2 - 3 % nickel, and about 2 - 3 % iron. This is only one possible example of alloy ratios suitable for the application, so that the alloy ratios can, of course, vary according to the applications. In
10 the above examples of intermediate constructions, the thickness of the layer containing zinc is less than 1 μm , usually as a single layer about 0.1 μm and as several layers, for example 0.3 - 0.4 μm . At its thinnest, the layer containing zinc can be about 5 - 10 nm after manufacture. When growing a layer containing nickel or nickel-aluminium on top of the layer containing zinc, at least some of the zinc atoms dissolve and are replaced
15 with nickel atoms. In the finished circuit module, it can be possible for the layer containing zinc to be observable as mainly a concentration profile of zinc in the interface between the aluminium and the material of the next layer. The layer containing zinc need not necessarily be precisely limited in the final product, because the zinc can diffuse to the adjacent material layers, particularly in stages of the manufacturing
20 process using higher temperatures.

In one preferred embodiment, the layer containing zinc is grown by a double zincate process. With a single zincate process, the zinc forms a non-uniform and uneven surface on top of the aluminium. The adhesion of a nickel layer grown on top of such a surface
25 is weaker and is less suitable for use with small micro-via openings. The quality of the grown zinc surface can be significantly improved by using a double zincate process. Typically, in such a process, after the first zincate treatment, the layer containing zinc is stripped using nitric acid (HNO_3), after which a second layer containing zinc is coated. By means of the double zincate process, a tight and uniform layer containing zinc is
30 obtained on the surface of the component's aluminium junction interface.

The thickness of the nickel-aluminium layer, for its part, can be, for example, 0.2 - 2

μm. The thickness of the nickel layer, on the other hand, can be, for example 0.5 - 20 μm, typically 2 - 10 μm. The layer thicknesses too are only examples of the possible layer thicknesses and other layer thicknesses can also be used.

- 5 In the embodiments, the electrochemically grown copper layer can have a thickness of, for example, 5 - 30 μm, typically 10 - 20 μm. The copper layer grown by a chemical growing method, for its part, is generally manufactured to be clearly thinner, and its thickness in the embodiments is, for example, 0.1 - 2 μm, typically 200 - 800 nm.
- 10 In the manufacturing methods described above, it is, of course, also possible to use intermediate-layer constructions and materials, for example tin, other than those referred to above. It is also possible to grown a nickel layer directly on the surface of the aluminium, for example, by alkali etching and flushing the surface after this with propan-2-ol and immediately after this coating with propan-2-ol at boiling point in a
- 15 warm chemical nickel bath. In addition, the surface of the layer containing zinc could also be coated with chromium and gold on the surface of the nickel.

Figure 28 shows yet another possible contact structure, in which it is possible to use components, the contact area of which is pre-equipped with base-metallurgical layers, though bumps as such are not made. Figure 29 shows one possible corresponding contact structure, implemented with a bumpless component.

Figure 28 shows a passivation layer 9 on the surface of the component, in which there is an opening at the position of the contact area 7 of the component. There is a polymer layer 25 of the surface of the passivation layer 9. The polymer layer 25 can consist of one or more polymer layers. The material of the polymer layer 25 can contain, for example, an insulator layer 13 depicted in connection with Figure 1, adhesive 5 depicted in connection with Figure 2, and/or a spacer depicted in connection with Figure 11. The base metallurgy, which in this case comprises two layers, is made on the surface of the contact area 7 of the component. The first base-metallurgy layer 26 is a layer of, for example, chromium (Cr) or titanium-wolfram (TiW) manufactured by sputtering. The second base-metallurgy layer 27 is a layer of, for example, nickel (Ni), copper (Cu), or

gold (Au), manufactured by sputtering. The actual bump comprises further a gold or copper layer, for example, grown chemically or electrochemically, on the surface of the second base-metallurgy layer 27.

5 In the example of Figure 28, the component is attached by a polymer layer 25 to a conductor foil 12, in which contact openings 8 have been made as depicted in the methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the second base-metallurgy layer 27, are made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is
10 made using one or more chemical growing methods, in a corresponding manner to that depicted in the methods described above. In the example of Figure 28, the intermediate layer 2 is of copper grown using a chemical growing method. On top of this intermediate layer a layer 32 of copper is grown using an electrochemical growing method. The electrochemically grown copper also forms the conductor core 29 of the contact element.
15 It can be seen from Figure 28 that the conductor foil 12, the intermediate layer 2, and the copper layer 32 together form the material of the conductor 22. In the example, the conductor foil 12, the intermediate layer 2, and the copper layer 32 are all of copper, but the layers and the interfaces between them, can, however, also be detected by analysing the finished structure.

20 Like Figure 28, Figure 29 shows a passivation layer 9, in which there is an openings at the position of the contact area 7 of the component, on the surface of the component. On the surface of the passivation layer 9 is a polymer layer 25, which corresponds to that shown in connection with Figure 28. In the example of Figure 29, the surface of the
25 contact area 7 of the component has been a uncoated component when it was brought to the circuit-module manufacturing process. In such a component, the outer surface of the contact area 7, i.e. the contact surface, is thus typically formed already at the semiconductor factory. In the example of Figure 29, the material of the contact area 7 is aluminium.

30 In the example of Figure 29, the component is attached by a polymer layer 25 to the conductor foil 12, in which contact openings 8 are made in the manner depicted in the

methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the contact area 7, have been made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is made using one or more chemical growing methods, in a corresponding manner to that described above. In the example of Figure 29, the intermediate layer 2 is made in several parts and comprises several layers. In Figure 28, the intermediate layer is, in addition, to facilitate the description, divided into three parts, a base part 36, a wall part 37, and a conductor part 38. The base part 36 is the part that grows on the surface of the contact terminal 7, 17 to the bottom of the contact hole 18, 28, the wall part 37 is the part that grows on the surfaces of the side walls of the contact hole 18, 28, and the conductor part 38 is the part that grows to form part of the conductor 22 being manufactured.

The intermediate layer 2 of Figure 29 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. In the example of Figure 29, the conductor foil 12 is of copper, so that when using a zincate process the first intermediate layer 33 grows only on the base part 36 of the intermediate layer 2. From this, manufacture can be continued, for example, by using a chemical nickel-growing method to make the second intermediate layer 34. The nickel grows on both the base part 36 and the conductor part 38 of the intermediate layer and, when using some growing methods, on the wall part 37 too on the surface of the polymer 25. The third intermediate layer 35 is made from copper on top of the second intermediate layer 34 using a chemical growing method, so that the copper grows on the base part 36, the wall part 37, and the conductor part 38. A layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element.

In the case of Figure 29, it should be noted that, in the finished circuit module, the layers 33 and 34 do not have precise boundaries as shown in the figure, but instead the layers can appear as overlapping or mixed, for example, from the effect of diffusion. For example, in the case of the first intermediate layer 33 containing zinc, the zinc can be located as a concentration profile in the interface between the aluminium and nickel 34

and partly inside the aluminium 7 and the nickel layer 34.

In the contact structure of Figure 29, other material combinations can also be used. For example, suitably selected intermediate-layer structures from the intermediate-layer constructions 1 - 7 described above can be used to form the contact structure depicted by Figure 29 and also the contact structures depicted by Figures 30 - 33. In addition, the contact structure of Figure 29 can also be manufactured with the aid of the materials shown by Figure 28, in such a way that the first intermediate layer 33 and the second intermediate layer 34 are made by sputtering. In that case, the sputtered intermediate layers 33 and 34 will grow to the base part 36 and the conductor part 38, but not to any substantial extent to the wall part 37, provided the contact hole 18, 28 does not widen towards the contact opening 8. One possibility is to use a first intermediate layer 33 containing zinc and on the surface of this either directly a third intermediate layer 35 made from nickel by a chemical growing method, or a construction, in which a second intermediate layer 34 made from nickel-aluminium is used between the layers 33 and 35. In such an embodiment, there is no need at all of chemical copper growing, as the nickel forms a vertical contact along the side wall of the contact hole.

Figure 30 shows yet another contact-element structure. In the structure of Figure 30, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel-aluminium and the third intermediate layer 35 is of nickel grown by a chemical growing method. This, in the structure of Figure 30, the contact hole is filled with nickel, i.e. the conductor core 29 of the contact element is nickel. Otherwise, the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 30.

Figure 31 shows yet another contact-element structure. In the structure of Figure 31, the intermediate layer 2 comprises a first intermediate layer 33 and a second intermediate layer 34. The first intermediate layer 33 can be manufactured, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate

layer 34 is of copper grown by a chemical growing method, or alternatively of nickel grown by a selective chemical growing method. Alternatively, the structure of Figure 31 can also be made in such a way that the first and second intermediate layers 33 and 34 are replaced with a single layer of chemically grown nickel. The conductor core 29 is typically copper and the conductor 22 comprises a first and second copper layer 12 and 32. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 31.

Figure 32 shows yet another contact-element structure. In the structure of Figure 32, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method, the growing method is selective, in such a way that the nickel grows on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 32 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 32.

Figure 33 shows yet another contact-element structure. The method described in connection with Figures 10 - 17, for example, in which a photo-resist layer 30 is used, can be used for making the structure of Figure 32. In the structure of Figure 33, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method of the example, the growing method is selective, in such a way that the nickel grows only on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 33 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with

Figures 28 and 29 apply in the case of the structure of Figure 33.

Thus, in the embodiments a method is presented for the manufacture of a circuit module, in which method

5

- a conductor foil 12 is taken,

- a component 6, which comprises contact areas 7, the material of which contains a first metal, is taken,

10

- the component 6 is attached to a conductor foil 12 by means of a polymer layer 25,

15

- an insulator layer 1 is manufactured around the component 6 attached to the conductor foil 12,

20

- contact holes 18, 28 are made in the polymer layer 25 at the positions of the contact areas 7, in such a way that the contact surface area A_{CONY1} between each contact hole 18, 28 and the corresponding contact area 7 is less than the surface area A_{PAD} of the contact area 7, and

25

- an intermediate layer 2, which contains at least a third metal, is grown at least on the surface of the contact areas 7 in the contact holes 18, 28, and

- a layer 32 of a second metal is grown, which layer 32 is in contact with the surface of the intermediate layer 2 and extends along the conductors 22 being made, and

30

- conductors 22 are formed by patterning the conductor foil 12, and, if necessary, also the intermediate layer 2 on the surface of the conductor foil 12 and/or the layer 32 of a second metal.

In a typical embodiment, the contact holes 8 are made in the conductor foil 12 before

attaching the component, so that the component is thus attached to a conductor foil 12 equipped with contact openings. In the commonest form of this type of embodiment, the contact openings do not extend to the surfaces of the contact areas 7, so that after the attaching of the component 6 contact holes 18, 28 are further opened through the contact openings 8.

In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.

In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.

When making the intermediate-layer construction, at least one chemical growing method is typically used.

The embodiments depict a circuit module, which comprises

- an insulator layer 1,
- inside the insulator layer 1, at least one component 6, which comprises contact areas 7, the material of which contains a first metal,

- on the surface of the insulator layer 1, conductors 22, which comprise at least a first layer 12 and a second layer 32, in such a way that at least the second layer 32 contains a second metal, and
 - 5 - contact elements for forming electrical contacts between the contact areas 7 and the conductors 22, which contact elements comprise an intermediate layer 2, which contains a third metal, on the surface of the material of the contact area 7,
 - in which the first, second, and third metals are different metals, and
 - 10 - the contact surface area A_{COT1} between the intermediate layer 2 and the contact area 7 is less than the surface area A_{PAD} of the contact area.
- In one embodiment, the first metal is aluminium, the second metal is copper, and the
- 15 third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.
- In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course,
- 20 in addition to nickel, also contain other metals or metal alloys, as stated above.
- In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.
- 25 In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.
- 30 In a typical embodiment, the contact elements comprise a copper core 29 made using an electrochemical growing method, which, in the direction of the side walls and the component 6 is bounded by the intermediate layer 2 and in the direction of the conductor

22 connects continuously, i.e. without an interface to the material of the second layer 32 of the conductor 22. In other words, the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is manufactured in the same process, so that the parts are attached permanently to each other and there is no interface
5 between them. Between the first layer 12 and second layer 22 of the conductor, on the other hand, there is typically an interface, or a corresponding transition zone, which can be detected, for example, by analysing the crystalline structure or impurity concentration of the metal.

10 In one embodiment, the width W_{CONT} of the contact surface between the contact element and the contact area 7 of the component is 0 - 20 % less than the greatest width W_{MAX} of the contact element in the same direction.

The contact elements usually fill entirely the contact holes 18, 28, i.e. the contact
15 elements are not hollow, but are solidly of conductor material.

Usually, the aim in the embodiments is for the height H of the contact element to be less than, or equal to the greatest width W_{MAX} of the contact element.

20 There are also embodiments of the circuit module, in which the insulator layer 1 includes at least one layer of fibre material 19, in which there is an opening in the fibre material 19 for the component 6, as well as a uniform polymer layer, which is attached to the fibre material 19 and to the components 6, 16.

25 The manufacturing processes described above and their sub-processes can be modified in many ways. For example, the use of an actual adhesive depicted above in attaching the component to the conductor foil 12 can be replaced with some other adhesion mechanism. On example that can be given is the use of an insulator layer 13 possessing an adhesion property on the surface of the conductor foil 12 (see Figure 1 and the
30 corresponding description). The components 6 are then pressed directly against the insulator layer 13, so that the components attach sufficiently in place in a manner correspondingly to that described in connection with the embodiment using adhesive.

Such an insulator layer 13 can contain, for example, a tape-like surfacing, or consist of a polymer or similar material that is shapable at least in its surface part.

5 The method can also be implemented without the use of an adhesive 5 or an adhesion property. In that case, the components 6 can be attached in place, for example, mechanically or with the aid of a vacuum. The vacuum or similar temporary attachment can then be maintained until the component 6 is sufficiently secured in place with the aid of the insulator material 1.

10 The component 6 to be attached can be, for example, an integrated circuit, such as a memory chip, processor, or ASIC. The component to be attached can also be, for example, a MEMS, LED, or passive component. The component to be attached can be cased or uncased and its contact terminals can consists of contact areas 7, contact bumps 17, or similar. There can also be a conductor coating thinner than an actual contact bump
15 on the surface of the contact areas of the component.

A different material of the insulator layer 1 from those in the examples described above can also be selected. The insulator layer 1 can be manufactured from a suitable polymer or from a material containing polymer. The material of manufacture of the insulator
20 layer 1 can be, for example, in a liquid or pre-hardened form (such as prepreg). In the manufacture of the insulator layer 1 it is possible to use, for example, glass-fibre reinforced sheet, such as an FR4 or FR5-type sheet. Other examples of materials, which can be used in the manufacture of the insulator layer 1 are PI (polyimide), aramide, polytetrafluoroethylene, and Teflon®. Instead of, or as well as thermosetting plastics,
25 thermoplastics too, for example some suitable LCP (liquid crystal polymer) material can be used in the manufacture of the insulator layer 1.

In addition, it is obvious to one skilled in the art that the features described above of the invention can be used as part of some larger totality, for example, in such a way that the
30 electronics module is manufactured partly using some method according to the prior art and partly using the embodiments depicted here. It is also possible to manufacture additional circuit-board layers on the surface or surfaces of the electronic-module

structures described above, or also to attach components, for example, by means of the surface-mounting technique.

5 One skilled in the art will also understand that, when reference is made in the present document to a specific material, for example, aluminium, nickel, or copper, the reference is to a material, which in terms of the application is substantially of the said material. The material referred to can thus, in addition to the said principal element contain, from the point of view of the application, insubstantial amounts of impurities and other elements. For example, an aluminium contact area is usually of a material that typically
10 contains a minimum of 95 % aluminium.

When, on the other hand, reference is made to a material containing some specific element, this means that the material contains an essentially large content of the said element. In addition, the material can contain substantial or insubstantial amounts of
15 other elements. For example, the layer containing zinc will thus contain an amount of zinc that is of significance in terms of the contact properties between the aluminium and the next metal.

The examples given above depict some possible methods and structures, which the aid
20 of which our invention can be exploited. However, our invention is not restricted to only the examples and embodiments described above, but instead the invention covers numerous other methods and structures, taking into account the full scope of the Claims and the equivalence interpretation.

Claims:

1. Method for manufacturing a circuit module, the method comprising

5 taking a conductor foil (12),

making contact openings (8) in the conductor foil (12) for the manufacture of contact elements,

10 taking a component (6), which comprises contact areas (7), the material of which contains a first metal,

attaching the component (6) to the conductor foil (12) by means of a polymer layer (25),

15 manufacturing an insulator layer (1) around the component (6) attached to the conductor foil (12),

20 making contact holes (18, 28) in the polymer layer (25) at the positions of the contact areas (7), in such a way that the contact surface area (A_{CONT1}), between each contact hole (18, 28) and the corresponding contact area (7) is less than the surface area (A_{PAD}) of the contact area (7), and

25 growing an intermediate layer (2) at least on the surface of the contact areas (7) in the contact holes (18, 28), the intermediate layer (2) containing at least a third metal, and

30 growing a layer (32) of a second metal, which layer (32) is in contact with the surface of the intermediate layer (2) and extends along the conductors (22) being made, and

forming conductors (22) by patterning the conductor foil (12), and, if necessary,

also the intermediate layer (2) on the surface of the conductor foil (12) and/or the layer (32) of a second metal.

2. Method according to Claim 1, in which

5

the contact openings (8) are manufactured before the attachment of the component (6),

the component (6) is attached to a conductor foil (12) equipped with contact
10 openings, and

after the attachment of the component (6), contact holes (18, 28) are opened through the contact openings (8).

15 3. Method according to Claim 2, in which the contact holes (18, 28) are opened through the contact openings (8) using a CO₂ laser, in which case the conductor foil (12) is used as a mask.

20 4. Method according to any of Claims 1 - 3, in which the first metal is aluminium, the second metal is copper, and the third metal contains at least one of the metals zinc and nickel.

5. Method according to any of Claims 1 - 3, in which the first metal is gold, the second metal is copper, and the third metal is nickel.

25

6. Method according to any of Claims 1 - 4, in which the intermediate layer (2) comprises a layer (33) containing zinc, which is manufactured using a double zincate process.

30 7. Method according to any of Claims 1 - 6, in which the intermediate layer (2) comprises a layer (34) containing nickel, which is manufactured using a chemical nickel-growing method.

8. Method according to any of Claims 1 - 7, in which the intermediate layer (2) comprises a layer (35) containing copper, which is manufactured using a chemical copper-growing method.
- 5
9. Method according to any of Claims 1 - 8, in which the insulator layer (11) is manufactured in such a way that
- at least one insulator sheet (11) containing a fibre material (19) and a pre-
- 10 hardened polymer is taken,
- a hole for the component (6) is made in the insulator sheet (11) containing a fibre material (19), and
- 15 the insulator sheet (11) or insulator sheets (11) are laminated together with the conductor foil (12) and its related structures.
10. Method according to any of Claims 1 - 9, in which the surface of the conductor foil (12), to which the component (6) is attached, comprises a uniform insulator layer (13).
- 20
11. Method according to any of Claims 1 - 10, in which a spacer (15) is placed between the component (6) and the conductor foil (12).
12. Method according to any of Claims 1 - 11, in which, in addition to the component (6), at least one other component (16) is located in the circuit module, in such a way that the manners of attachment of the first and second components differ from each other in the case of at least one property of the polymer layer (25).
- 25
13. Method according to any of Claims 1 - 12, in which the component (6) to be attached is a bumpless component.
- 30
14. Circuit module, which comprises

an insulator layer (1),

5 inside the insulator layer (1), at least one component (6), which comprises
contact areas (7), the material of which contains a first metal,

10 on the surface of the insulator layer (1), conductors (22), which comprise at least
a first layer (12) and a second layer (32), in such a way that at least the second layer (32)
contains a second metal, and

15 contact elements between the contact areas (7) and the conductors (22) for
forming electrical contacts, which contact elements comprise an intermediate layer (2),
which contains a third metal, on the surface of the material of the contact area (7),

wherein the first, second, and third metals are different metals, and

the contact surface area ($A_{CONT\ 1}$) between the intermediate layer (2) and the
contact area (7) is less than the surface area (A_{PAD}) of the contact area.

20 15. Circuit module according to Claim 14, in which the first metal is aluminium, the
second metal is copper, and the third metal is at least one of the metals zinc and nickel.

25 16. Circuit module according to Claim 14, in which the first metal is gold, the second
metal is copper, and the third metal is nickel.

17. Circuit module according to Claim 14 or 15, in which the material of the contact
areas (7) is mainly aluminium.

30 18. Circuit module according to Claim 14, 15, or 17, in which the intermediate layer (2)
comprises a layer (33) containing zinc.

19. Circuit module according to Claim 18, in which the intermediate layer (2) comprises,

in addition to the layer (33) containing zinc, at least one second intermediate metal layer (34, 35).

20. Circuit module according to Claim 19, in which the at least one second intermediate metal layer (35) is of copper grown by a chemical growing process.

21. Circuit module according to Claim 20, in which the intermediate layer (2) comprises at least one layer (34) of nickel and/or of nickel and aluminium between the layer (33) containing zinc and the copper layer (35).

22. Circuit module according to any of Claims 18 - 21, in which the layer containing zinc contains zinc, copper, nickel, and iron.

23. Circuit module according to any of Claims 14 - 22, in which part of the intermediate layer (2) extends along the side walls of the contact elements between the contact areas (7) and the conductors (22).

24. Circuit module according to Claim 23, in which the contact elements comprise a copper core (29) made using an electrochemical growing method, which, in the direction of the side wall and component (6), is bounded by the intermediate layer (2) and, in the direction of the conductor (22) connects continuously, i.e. without an interface, to the material of the second layer (32) of the conductor (22).

25. Circuit module according to Claim 23 or 24, in which the part (37) of the intermediate layer (2) extending along the side walls of the of the contact elements contains copper grown by a chemical growing method, or nickel grown by a chemical growing method.

26. Circuit module according to any of Claims 14 - 25, in which the conductors (22) comprise

a first layer (12) of copper on the surface of the insulator layer (1), and

a second layer (32) of copper on the surface of the first copper layer.

27. Circuit module according to any of Claims 14 - 25, in which the conductors (22)
5 comprise

a first layer (12) of copper on the surface of the insulator layer (1),

an intermediate layer (2) on the surface of the first copper layer, and
10

a second layer (32) of copper on the surface of the intermediate layer.

28. Circuit module according to Claim 27, in which the part of the intermediate layer (2)
between the first and second coppers layers comprises copper grown by a chemical
15 growing method or nickel grown by a chemical growing method.

29. Circuit module according to any of Claims 14 - 28, in which the width (W_{CONT}) of
the contact surface between the contact element and the contact area (7) of the
component is 0 - 20 % less than the greatest width (W_{MAX}) of the contact element in the
20 same direction.

30. Circuit module according to any of Claims 14 - 29, in which the height (H) of the
contact element is less than, or equal to the greatest width (W_{MAX}) of the contact element.

25 31. Circuit module according to any of Claims 14 - 30, in which the insulator layer (1)
contains at least one layer of fibre material (19), in which there is an opening in the fibre
material (19) for the component (6), as well as a unified polymer layer, which is attached
to the fibre material (19) and to the component (6).

30 32. Circuit module according to any of Claims 14 - 31, which comprises a polymer layer
(25), between the conductors (22) and the component (6), in which layer there are
contact holes (18, 18) for the contact elements, and in which the contact elements fill the

contact holes (18, 28) completely.

33. Circuit module according to Claim 32, in which the polymer layer (25) between the conductors (22) and the component (6) comprises a first (15) and a second (5) polymer layer, in which the first polymer layer (15) is of a first polymer and the second polymer layer (5) is of a hardened adhesive.

34. Circuit module according to Claim 33, in which the first polymer layer (15) and the second polymer layer (5) are local, in such a way that they exist essentially only at the location of the component (6).

35. Circuit module according to any of Claims 14 - 34, in which the component comprises a passivation layer (9) on the surface of the component and the contact areas (7) are located inside openings in the passivation layer, in which case the intermediate layer (2) extends through the opening in the passivation layer.

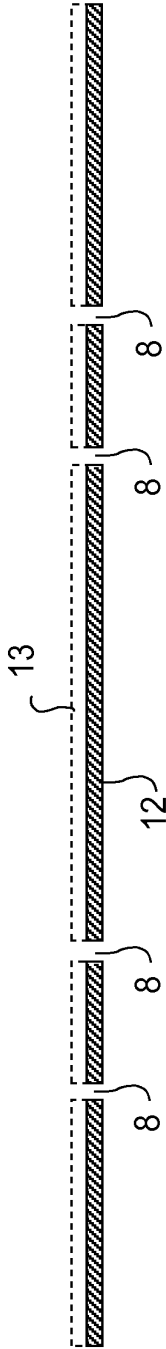


Fig. 1

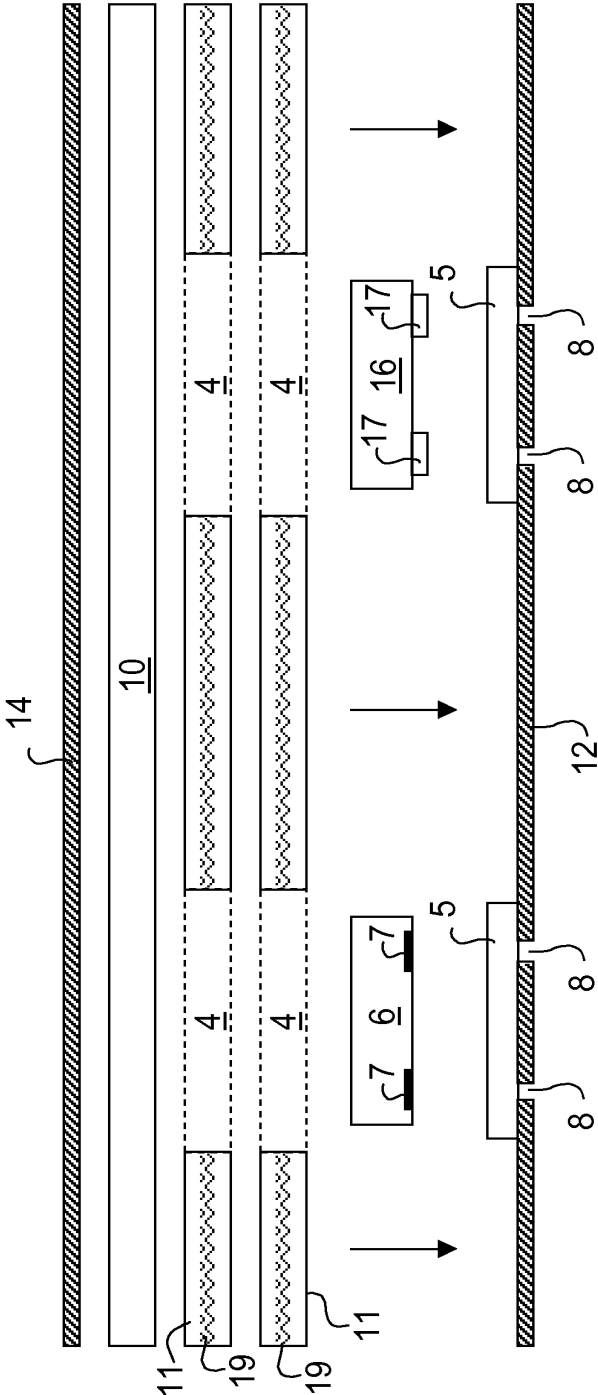


Fig. 2

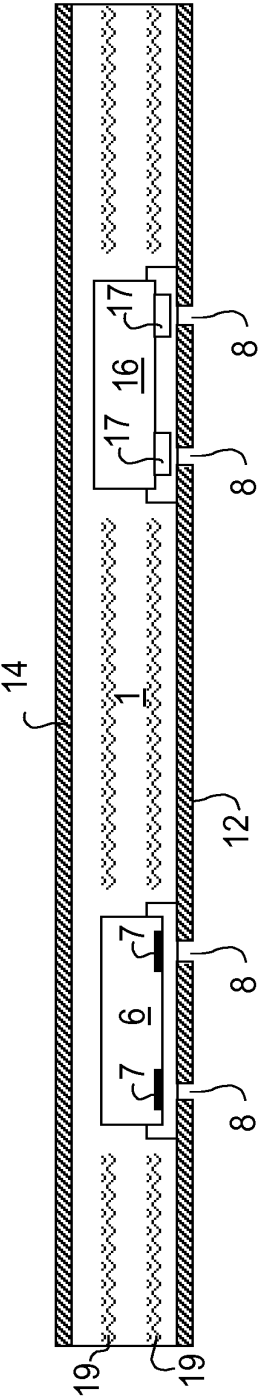


Fig. 3

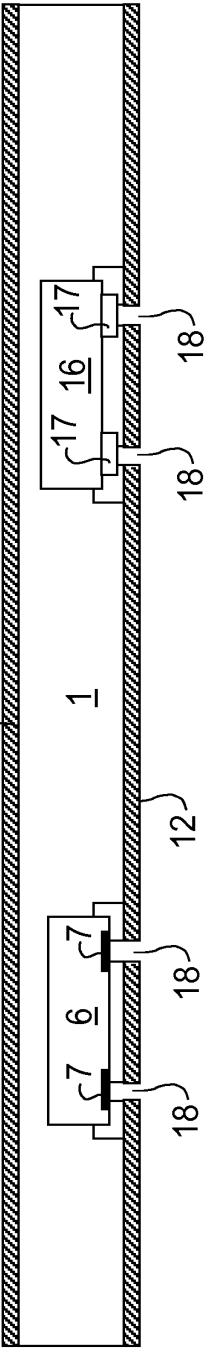


Fig. 4

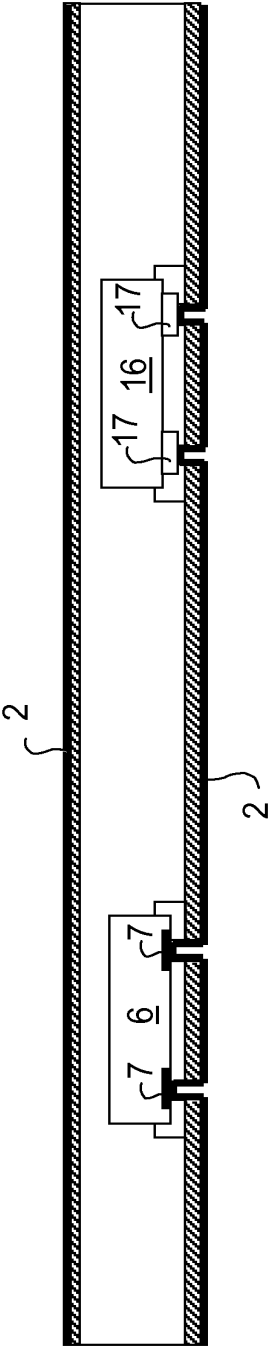


Fig. 5

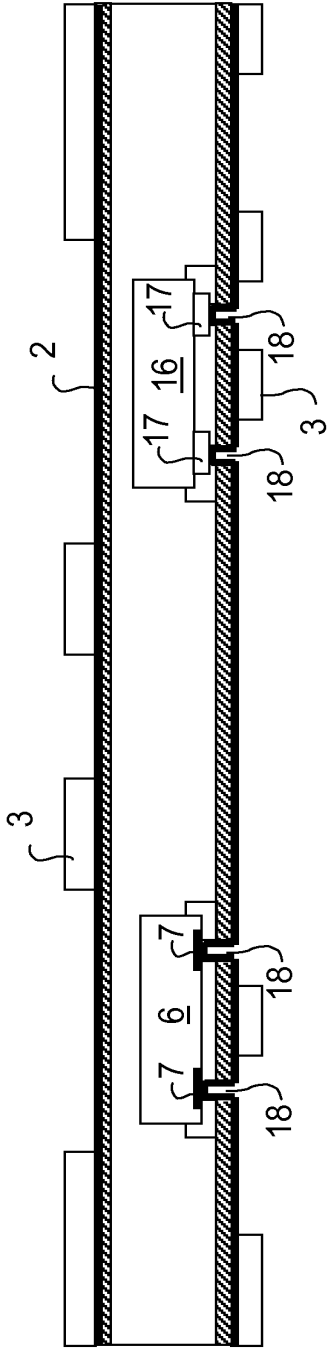


Fig. 6

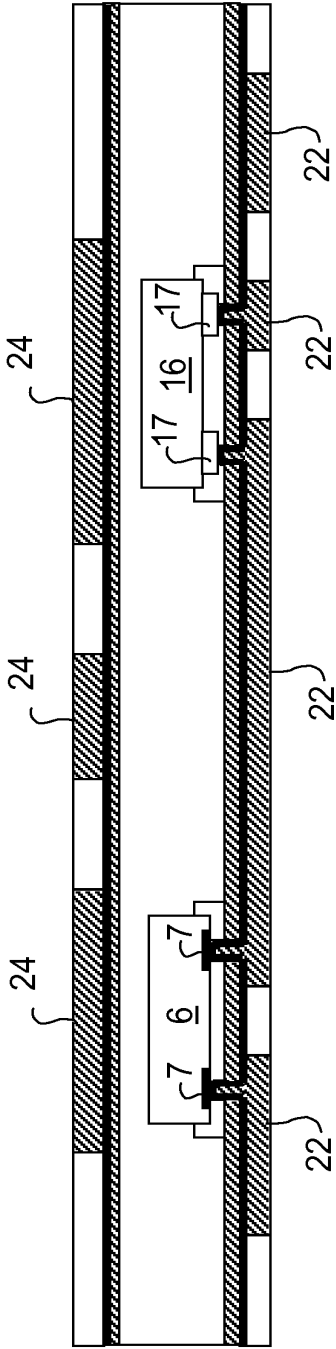


Fig. 7

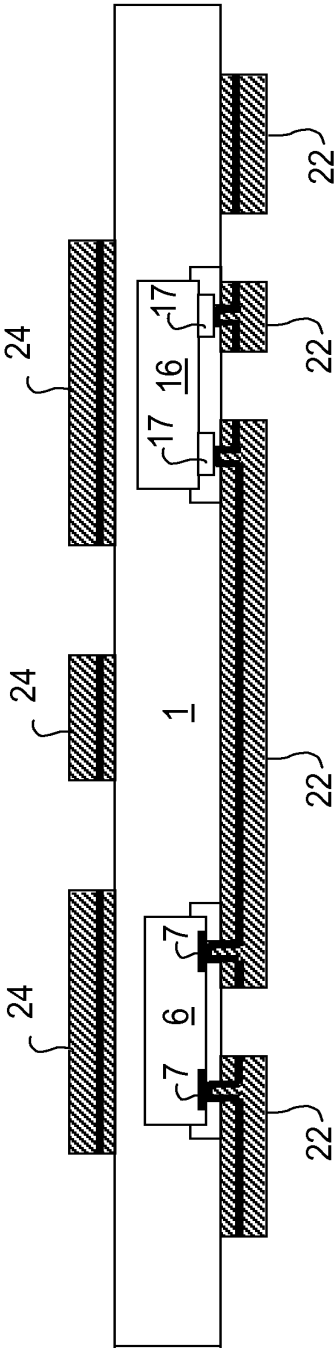


Fig. 8

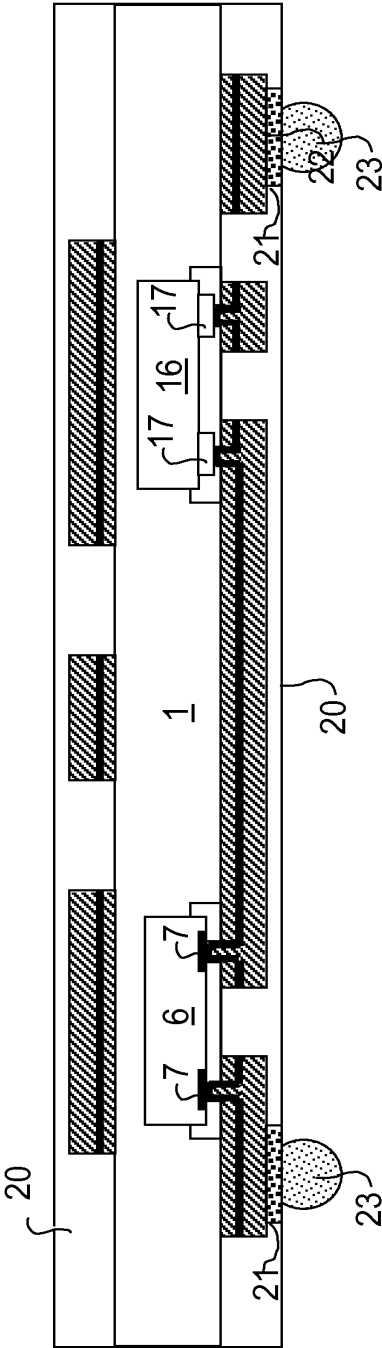


Fig. 9

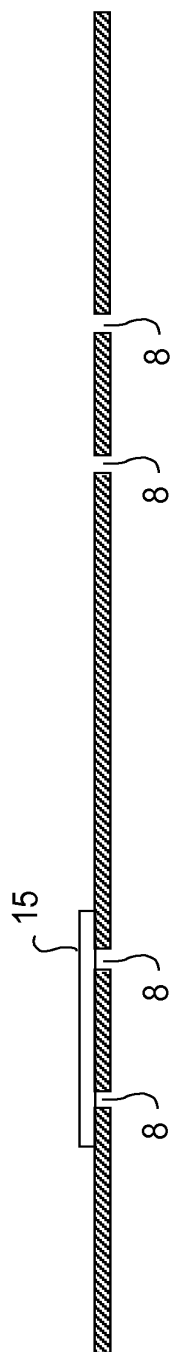


Fig. 10

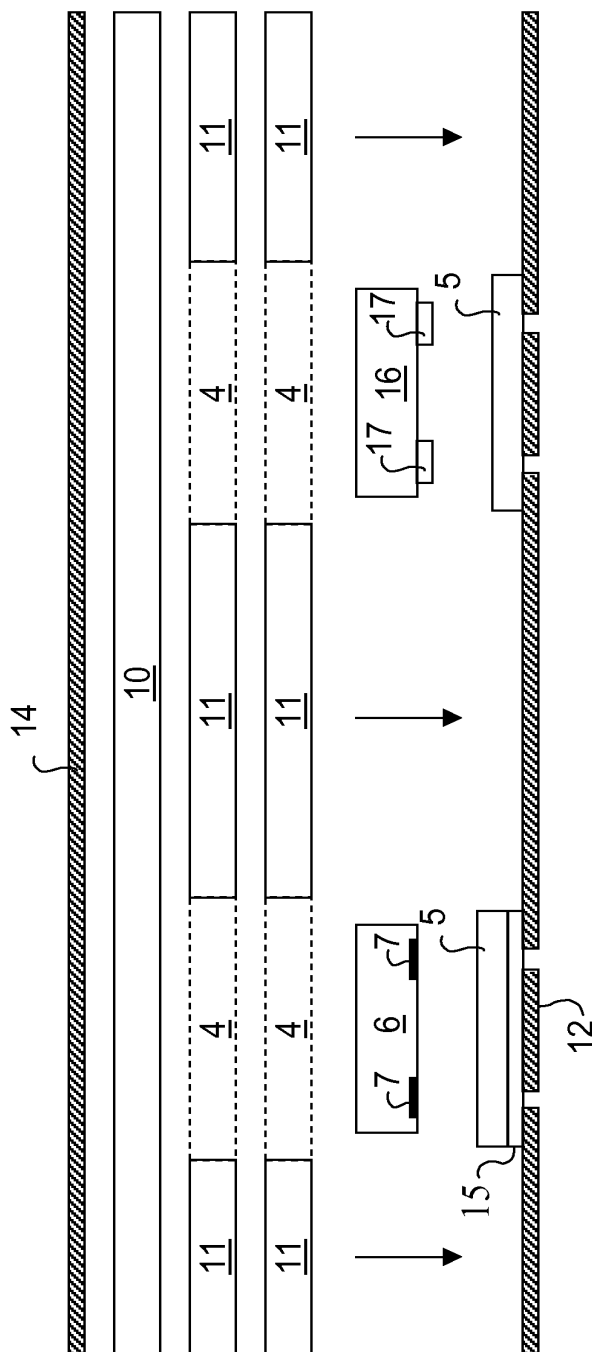


Fig. 11

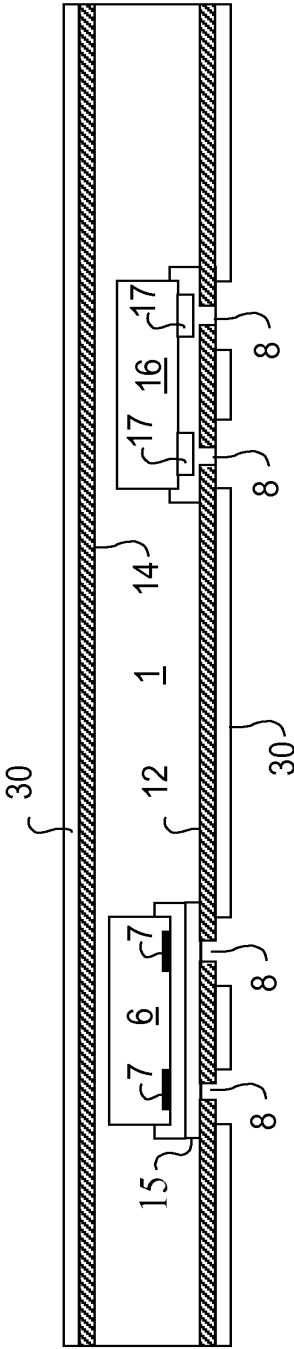


Fig. 12

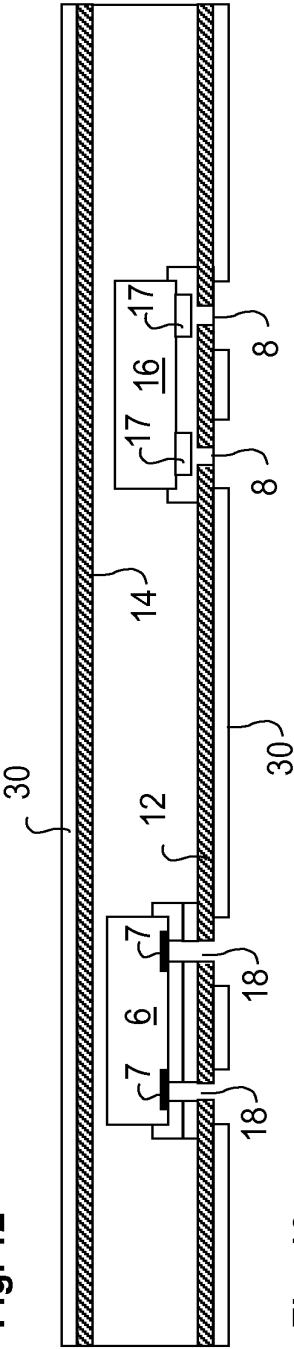


Fig. 13

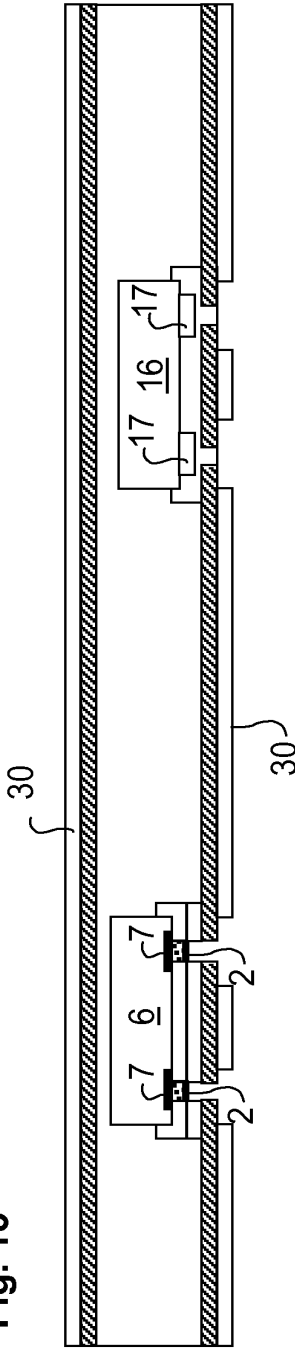


Fig. 14

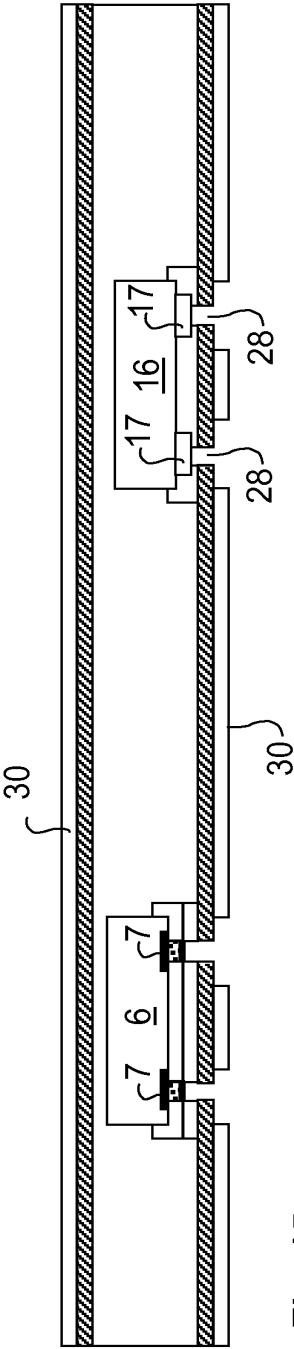


Fig. 15

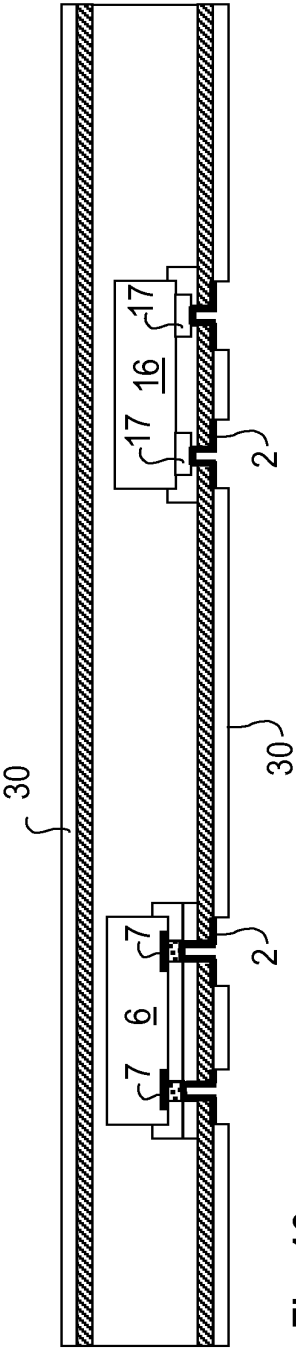


Fig. 16

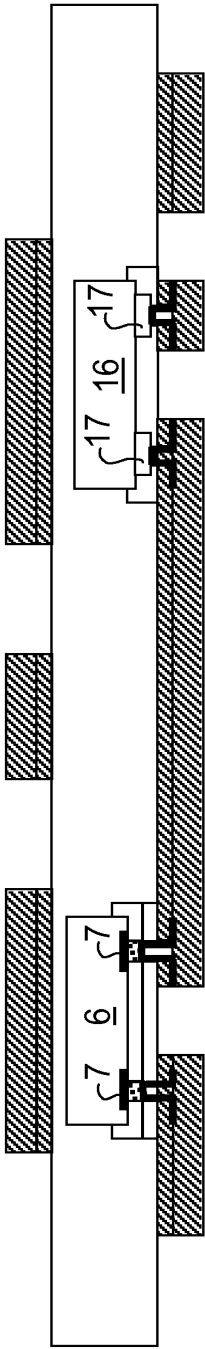


Fig. 17

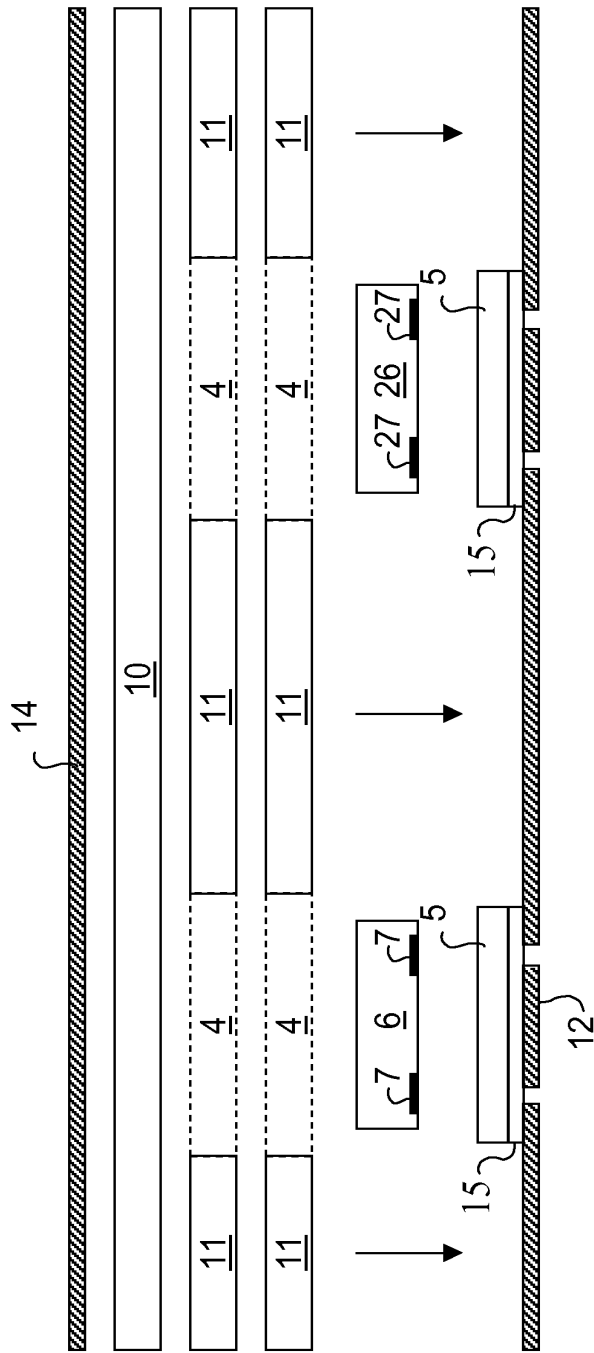


Fig. 18

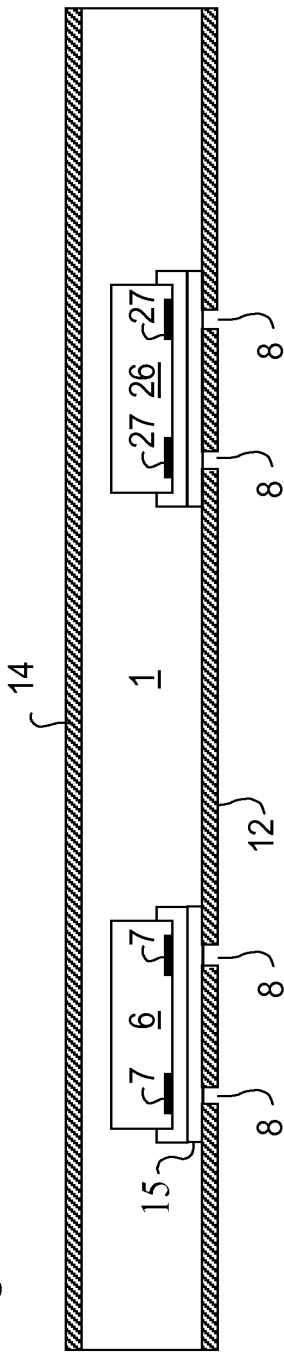


Fig. 19

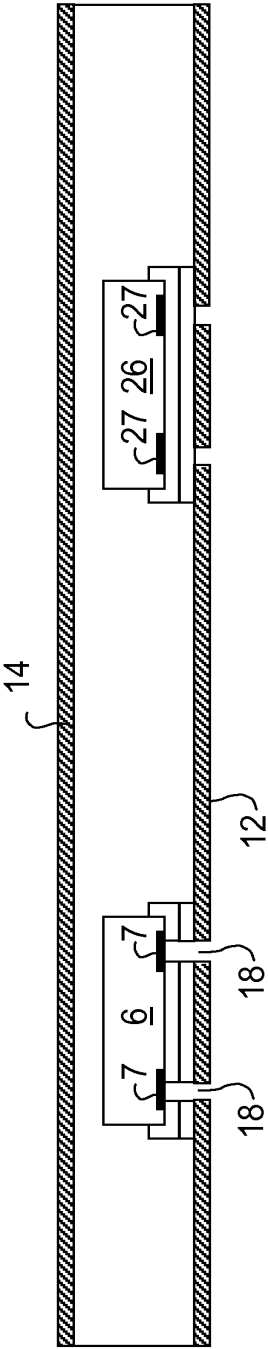


Fig. 20

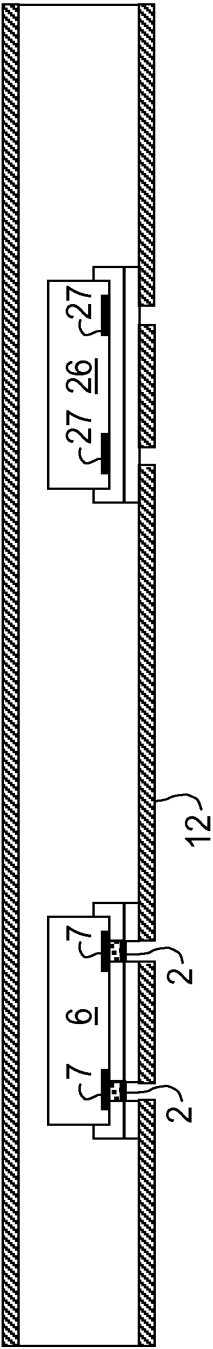


Fig. 21

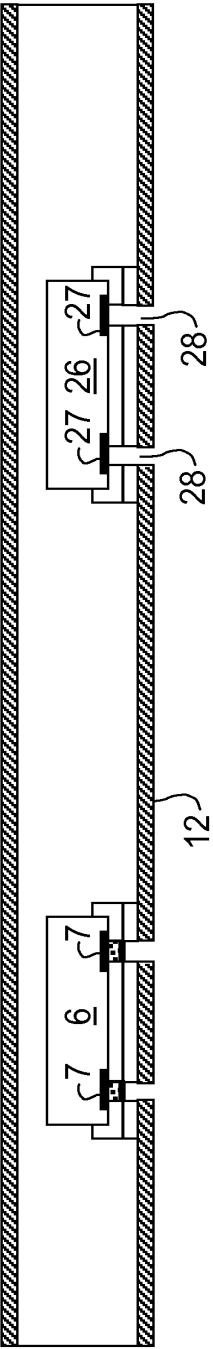


Fig. 22

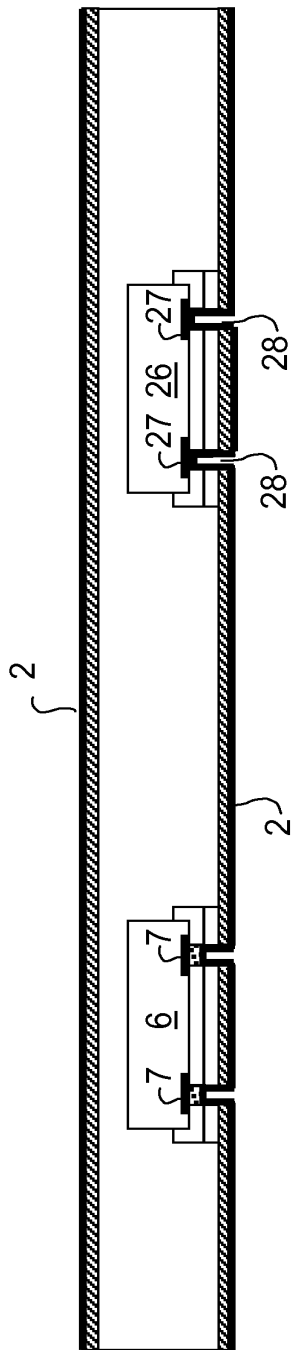


Fig. 23

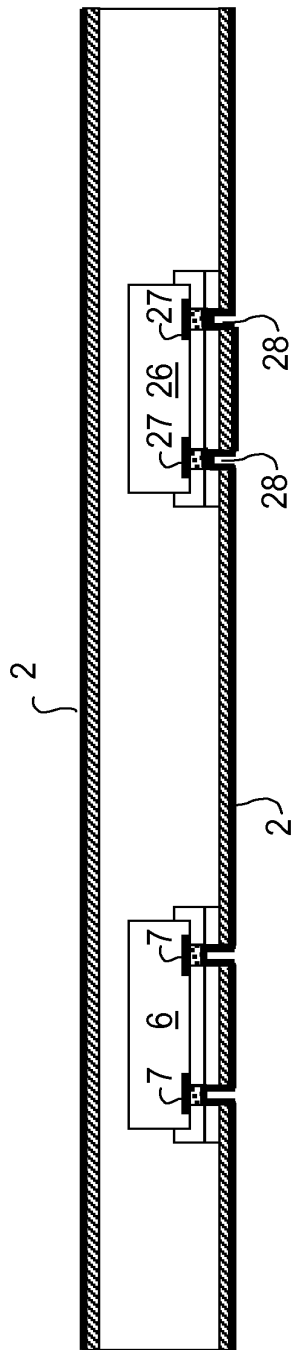


Fig. 24

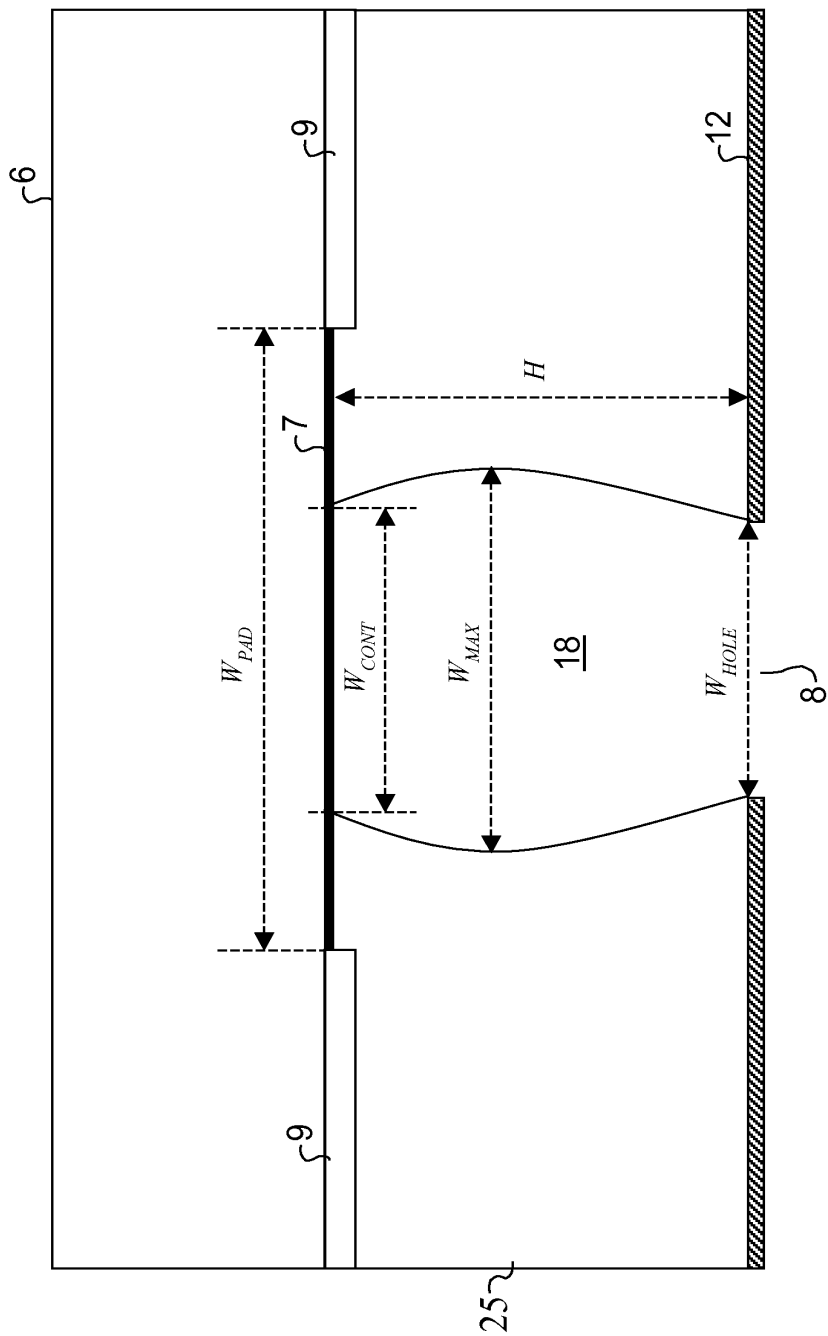


Fig. 25

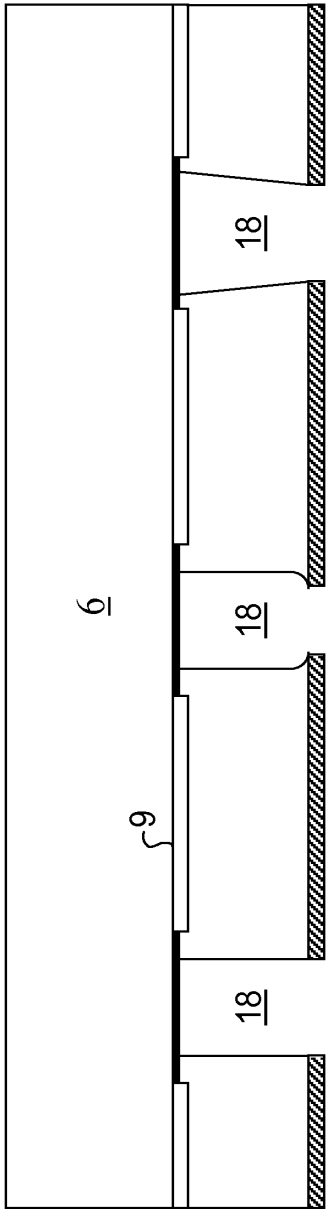


Fig. 26

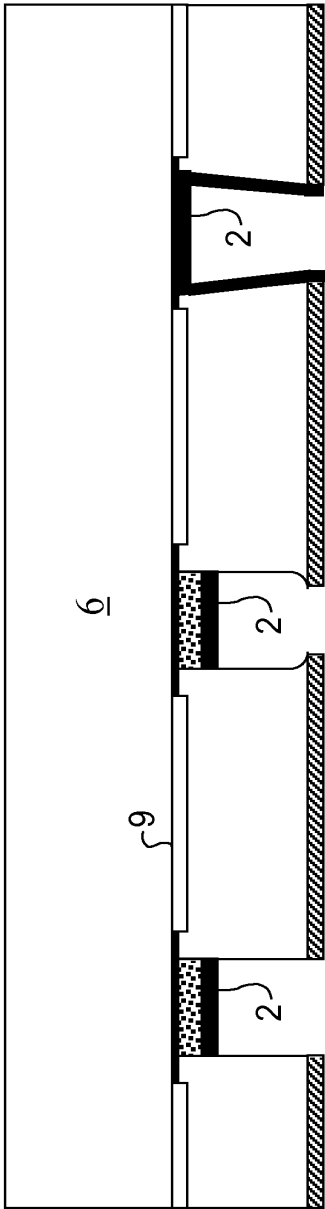


Fig. 27

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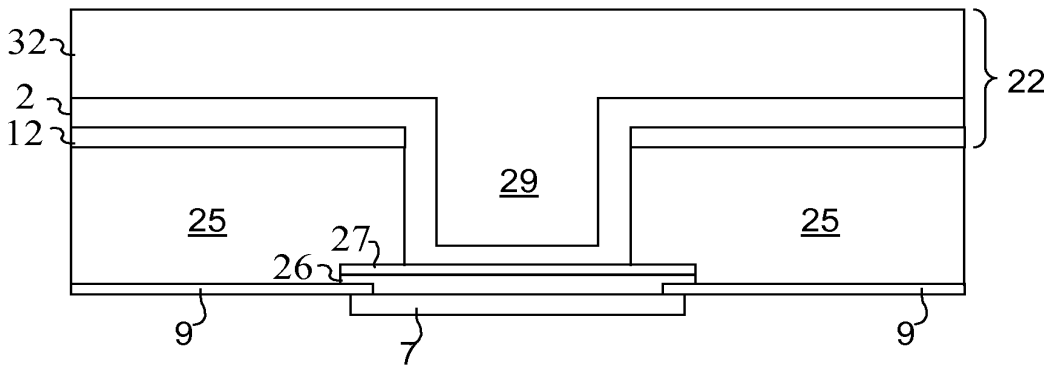


Fig. 28

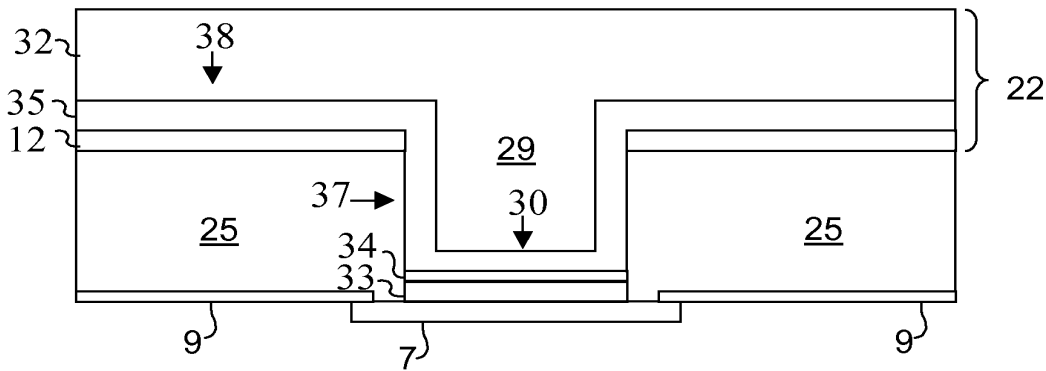


Fig. 29

14/15

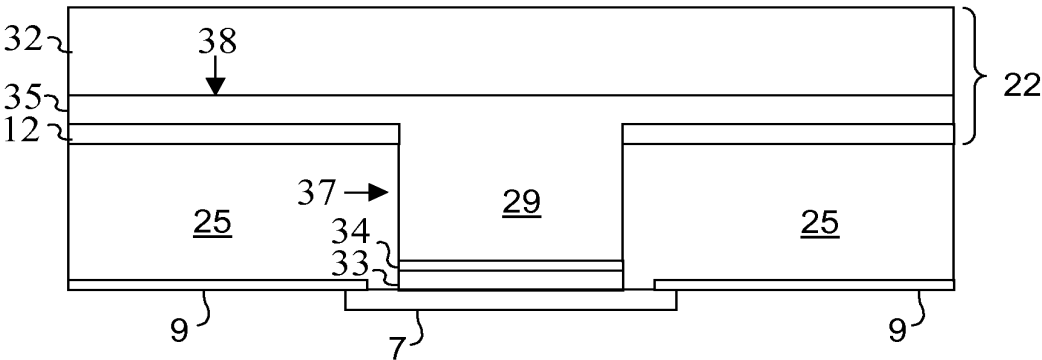


Fig. 30

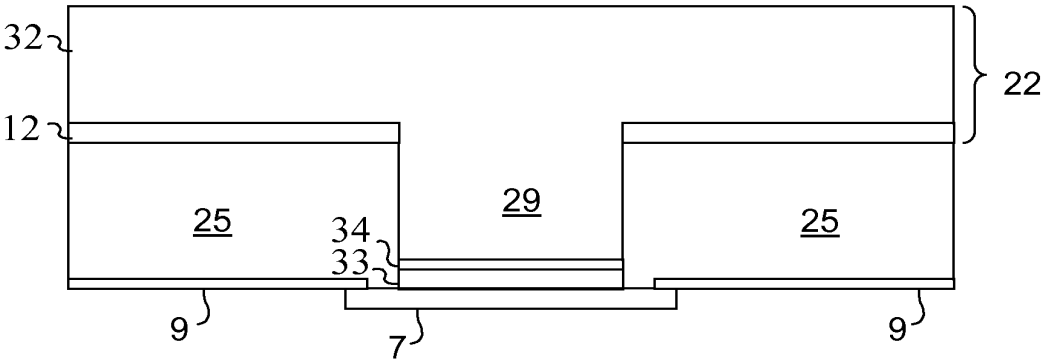


Fig. 31

15/15

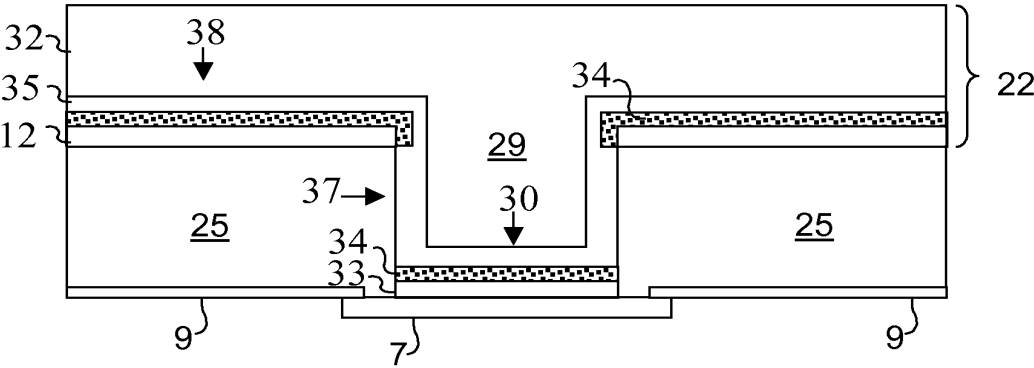


Fig. 32

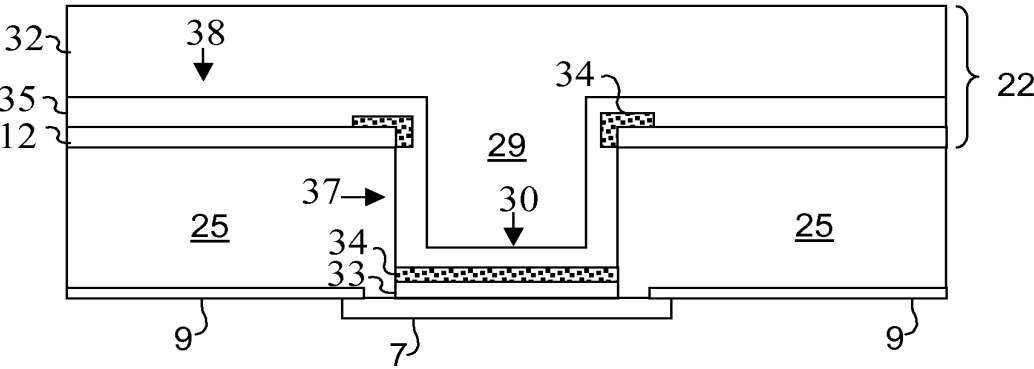


Fig. 33

INTERNATIONAL SEARCH REPORT

International application No
PCT/FI2009/050383

A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/056643 A (IMBERA ELECTRONICS OY [FI]; TUOMINEN RISTO [FI]; IIHOLA ANTTI [FI]) 1 June 2006 (2006-06-01) cited in the application figures 1-9	1-3, 7-14, 17, 23-35
Y	page 4, line 31 - page 17, line 9 -----	4-7, 15, 16, 18-22, 28
A	US 4 246 595 A (NOYORI MASAHARU ET AL) 20 January 1981 (1981-01-20) column 4, lines 15-27 -----	1-35
Y	US 6 396 148 B1 (EICHELBARGER CHARLES W [US] ET AL) 28 May 2002 (2002-05-28) column 2, lines 46-62 column 9, lines 38-44 -----	7, 28
	----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

10 September 2009

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INTERNATIONAL SEARCH REPORT

International application No

PCT/FI2009/050383

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1 259 103 A (IBIDEN CO LTD [JP]) 20 November 2002 (2002-11-20) paragraphs [0019] - [0023], [0052], [0056] -----	4, 6, 15, 18-22
Y	EP 0 380 289 A (FUJITSU LTD [JP]) 1 August 1990 (1990-08-01) column 4, lines 17-20 -----	5, 16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/FI2009/050383

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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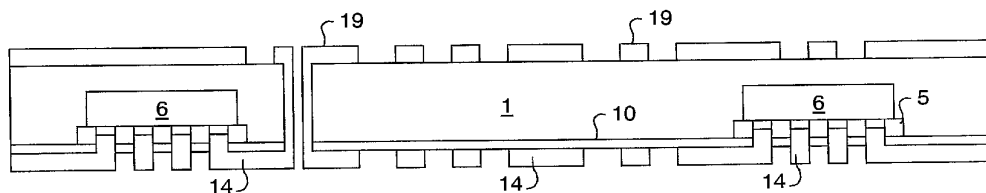
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR MANUFACTURING AN ELECTRONICS MODULE



(57) Abstract: Method for manufacturing an electronic module, which electronic module includes a component (6), which has contact areas (17), which are connected electrically to a conductor-pattern layer (14). The manufacture according to the method starts from a layered membrane, which comprises at least a conductor layer (4) and an insulator layer (10) on the first surface of the conductor layer (4). Contact openings (17), the mutual positions of which correspond to the mutual positions of the contact areas (7) of the component (6), and which penetrate both the conductor layer (4) and the insulator layer (10), are made in the membrane. After the manufacture of the contact openings (17), the component (6) is attached to the surface of the insulator layer (10), in such a way that the contact areas (7) of the component (6) line up next to the contact openings (17). After this, at least in the contact openings (17) and the contact areas (7) of the component (6) a conductor material is made, which connects the component (6) to the conductor layer (4) and the conductor layer (4) is patterned to form a conductor-pattern layer (14).

WO 2006/056643 A2

METHOD FOR MANUFACTURING AN ELECTRONICS MODULE

The present invention relates to a method for manufacturing an electronic module.

- 5 The invention particularly relates to a manufacturing method, in which one or more components are embedded in an installation base and connected to a conductor-pattern structure. The electronic module being manufactured can be a module like a circuit board, which contains several components, which are connected to each other electrically through conductor structures manufactured in the electronic module. The
- 10 electronic module can contain microcircuits, to which several contact terminals are connected. In addition to, or instead of microcircuits, other components too, for example passive components, can be embedded in an installation base. The intention is thus to embed in the electronic module components that are typically attached uncased to a circuit board (to the surface of the circuit board). Another important component group
- 15 consists of components that are typically encased for attachment to a circuit board. The electronic modules, to which the invention relates, can of course also include other kinds of components.

- Patent publication US 6,284,564 B1 discloses a method for manufacturing an electronic
- 20 module. In the method, manufacture is started from an insulating membrane. On one side of the insulating membrane an adhesive is spread, either in such a way that the adhesive is spread on the bare insulating membrane, or that conductor patterns are first made on the insulating membrane. After this, holes for vias are drilled in the insulating membrane. Holes are also drilled at the locations of the contact areas of the component
- 25 to be attached to the electronic module. After this, the component is attached to the adhesive layer, aligned relative to the holes drilled in the contact areas. A conductor layer is grown in the drilled holes and on the free surface of the insulating membrane, and is patterned to form a conductor-pattern layer.

- 30 Patent publication US 6,475,877 B1 discloses another method for manufacturing an electronic module. Manufacture is started from a bare insulating membrane. The

- insulating membrane is first surface with a conductor surfacing and after this the conductor surface is patterned with opening at the contact areas of the component to be attached. After this, an adhesive is spread on the opposite side of the insulating membrane, with the aid of which the component is attached to the surface of the
- 5 membrane, aligned with the aid of the openings patterned in the conductor surfacing. After this, holes are opened through the insulator and adhesive layers, at the opening patterned in the conductor surfacing. Metal, which is patterned to form a conductor-pattern layer, is grown in the openings and on top of the conductor surfacing.
- 10 In the methods described above, the component is aligned either directly in the via (US 6,284,564 B1) or both the component and the via are aligned with the aid of a fixed alignment mask formed in the conductor surfacing (US 6,475,877 B1). For this reason, it can be assumed that there will be good alignment accuracy between the component, the via, and the conductor pattern. When attempting to manufacture small and reliable
- 15 structures cost-effectively, the alignment of the component is an important factor. It should be possible to align the component very precisely and reliably, because wrongly aligned components will cause reliability problems and also reduce the yield, in which case the profitability of the manufacture of the modules will suffer.
- 20 The invention is intended to create a new method, by means of which components can be placed inside a circuit board or other electronic module. Further, the new method should, like the methods referred to above, permit the accurate alignment of the components.
- The invention is based on starting manufacture from a layered membrane, which
- 25 comprises at least a conductor layer and an insulator layer on the first surface of this. In addition, on the second surface of the conductor layer there can be a support layer, which can be of insulating or conductive material. After this, contact openings are made at locations corresponding to the future positions of the contact areas of the components. After this, the components are attached, aligned relative to the contact openings in the
- 30 insulating layer, on the first surface of the conductor layer. The attachment can take place, for example, with the aid of an insulating adhesive. After this, electrical contacts

between the conductor layer and the contact areas of the components are formed through the contact openings. After the electrical contacts are manufactured, conductor patterns are manufactured from the conductor layer.

- 5 More specifically, the method according to the invention is characterized by what is stated in Claim 1.

The invention offers an alternative manufacturing method to the methods described above, which has advantageous properties in terms of certain applications.

10

In the method according to the invention, the basic material for the layered membrane can be selected, for example, to have a suitable stiffness in terms of the manufacturing process, irrespective of the thickness and material properties of the insulator layer.

- 15 Unlike the solutions of the publications US 6,284,564 B1 and US 6,475,877 B1, this provides a possibility to select the thickness and material of the insulator layer to be optimal from the point of view of the electronic module being manufactured. In practise, the solutions of the above-mentioned publications require polyimide film to be used as the insulator layer.

- 20 Despite this, the stiffness of the layered membrane in the embodiments of the invention can also be selected to be optimal in terms of the manufacturing process. A suitable stiffness in the layered membrane can be achieved with the aid of the conductor layer, or, if necessary, a support membrane can be used.

- 25 For corresponding reasons, the thickness of the insulator layer in the embodiments of the invention can, if necessary, also be selected to be clearly thinner than when using the method disclosed in the publications referred to above. The component can, of course, also be glued directly to the surface of the conductor layer - without the insulating layer in between - but the use of an insulator layer can be considered to have some advantages,
30 at least in the case of certain applications. First of all, air bubbles may remain in the adhesive layer, which may cause a source of faults, because in that case insulating

material may be lacking between the conductor layer and the component. Air bubbles can also lead to an undesired etching result in processes using chemical etching. In addition, with the aid of a suitably chosen, ready-made insulator layer it is possible to achieve a better adhesion in the conductor layer than with an adhesive.

5

In the embodiments, it is also possible to use such an insulating layer on the surface of the conductor layer, which has itself an adhesion property in the direction of the component. In that case, there will be no need for a separate gluing stage and the manufacturing process will be simplified. Using such an embodiment, at least in some cases it will be possible to achieve more economical manufacturing costs and a better yield.

10

Further, there is the difference from the solutions disclosed in the publications US 6,284,564 B1 and US 6,475,877 B1 that the layered membrane that is the basic material already contains a conductor layer of a substantial thickness, so that the conductor material demanded in the conductor-pattern layer will not necessarily need to be introduced to the module blank in connection with the metallization of the contact openings. Thus, it will also be possible to use such contact-opening metallization or filling methods, which do not increase the conductor material on flat surfaces very much, or do not increase it at all. The use of electrochemical growing, on the other hand, achieves the advantage that there is no need to make a conductive surfacing on the surface of the insulator layer in order to create a counter-electrode.

15

20

In one embodiment of the invention, an adhesive layer is only used in the area between the component and the insulator layer, so that the consumption of adhesive can be reduced, compared to the methods disclosed in the aforementioned publications.

25

In the following, the invention is examined with the aid of examples and with reference to the accompanying drawings.

30

Figures 1 - 9 show a series of cross-sections of manufacturing methods according to one

embodiment.

In the methods according to the embodiments, manufacturing can commence, for example, from a bare conductor layer 4, which can be, for example, a layered membrane formed of a metal layer and an insulator layer 10. One applicable manufacturing material for the conductor layer 4 is, for example, copper foil (Cu). If the conductor layer 4 selected for the process is very thin, or if the conductor layer is not mechanically durable for other reasons, it is recommended that the conductor layer 4 be supported with the aid of a support layer 12. The support layer 12 can be, for example, an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer.

The insulator layer 10 can be, for example, a polymer, such as an epoxy. The thickness of the insulating is typically less than 200 micrometres, for example 1 - 20 micrometres and preferably less than 10 micrometres. When manufacturing thin electronic modules, at suitable thickness for the insulating layer will be typically in the range from about 4 to about 7 micrometres.

The layered membrane can be manufactured by using manufacturing methods that are well known in the circuit-board industry. The layered membrane can be manufactured, for example, by laminating the layers together.

Before the attachment of the component 6 to the layered membrane, contact openings 17 are made in the conductor layer 4 and the insulator layer 10 at the positions of the contact areas 7 of the component 6. The contact openings 17 can be made, for example, by drilling with the aid of a laser. The mutual positions of the contact openings 17 are selected according to the mutual positions of the contact areas 7 of the component while the location and position of each group of contact openings are selected in such a way that the component will be positioned correctly relative to the entire electronic module. Thus, typically one contact opening 17 is made for each contact area 7 participating in the creation of an electrical contact. The surface area of the contact openings 17 being

manufactured can be more or less as great as the surface area of the corresponding contact area 7. Of course, the surface area of the contact opening 17 can also be chosen to be smaller, or in some embodiments slightly larger than the surface area of the corresponding contact area 7. If the surface area of the contact area 7 is very large, several contact openings can be manufactured for each contact area.

The contact openings 17 can be drilled from the direction of the first or the second surface. If a support layer 12 is used in the embodiment, and is thus on the second surface of the conductor layer, it can be advantageous to drill the contact openings 17 from the direction of the first surface, because in that case the openings to be drilled do not need to penetrate the support layer 12 entirely. In such an embodiment, the contact openings 17 open later, when the support layer 12 is detached. The contact openings can also be opened in such a way that the material layer formed by the conductor layer 4 and the support layer 12 is thinned by etching from the direction of the support layer. The conductor layer 4 and the support layer 12 can also be formed from a single material layer. In that case, the part of the material layer corresponding to the support layer 12 is removed and the contact openings 17 open. The contact opening 17 is thus intended to extend through the entire conductor layer 4.

The components 6 are attached to the surface of the insulator layer 10 with the aid of an adhesive. For gluing, an adhesive layer 5 is spread on the attachment surface of the insulating layer 10, or on the attachment surface of the component 6, or on the attachment surfaces of both. After this, the components 6 can be aligned to the positions planned for the components 6, with the aid of the contact areas 17, the holes 3, or other alignment marks made in the base.

Instead of glue, it is also possible to use a suitable tape or other adhesive to attach the component 6. It is also possible for the insulating layer 10 itself to have a sufficient adhesive ability to hold the component in place for at least until the component is secured in place with the aid of the insulating-material layer 1. In that case no separate glue or tape will be required.

- The term attachment surface of the component 6 refers to that surface of the component 6, which faces towards the insulator layer 10. The attachment surface of the component 6 comprises contact areas, through which an electrical contact can be formed to the component. The contact area can be, for example, flat areas on the surface of the component 6, or more usually contact protrusions protruding from the surface of the component 6. There are generally at least two contact areas or protrusions in the component 6. In complex microcircuits, there can be a great many contact areas.
- 10 In many embodiments, it is preferable to spread so much adhesive on the attachment surface or attachment surfaces that the adhesive fills the space remaining between the component 6 and the insulator layer 10. In that case, a separate filler agent will not be required. Filling the space remaining between the components 6 and the insulator layer 10 reinforces the mechanical connection between the component 6 and the insulator
- 15 layer 10, so that a mechanically more durable construction will be achieved. During gluing, adhesive will also enter the contact openings 17.

- The term adhesive refers to a material, by means of which the components are attached to the insulator layer 10. One property of the adhesive is that the adhesive can be spread on the surface of the insulator layer and/or of the component in a relatively liquid form, or in one that otherwise conforms to the surface shapes, for example, in the form of a membrane. Another property of the adhesive is that after spreading the adhesive hardens or can be hardened at least partly, in such a way that the adhesive can hold the component in place (relative to the insulator layer 10) at least until the component is attached to the construction in some other way. A third property of the adhesive is its adhesive ability, i.e. its ability to adhere to the surface being glued.
- 20
- 25

- The term gluing refers to attaching the component and the insulator layer 10 to each other with the aid of an adhesive. In gluing, the adhesive is thus brought between the component and the insulator layer 10 and the component is placed in a suitable position relative to the insulator layer 10, in which the adhesive is in contact with the component
- 30

and the insulator layer 10 and at least partly fills the space between the component and the insulator layer 10. After this, the adhesive is allowed to harden (at least partly), or the adhesive is actively cured (at least partly), in such a way that the component is attached to the insulator layer 10 with the aid of the adhesive. In some embodiments, the contact
5 protrusions of the component may, during the gluing, protrude through the adhesive layer and even extend to the contact openings 17.

The adhesive used in the embodiments is, for example, a thermally hardening epoxy. The adhesive is selected in such a way that the adhesive being used has sufficient
10 adhesion to the insulator layer 10 and the component. One preferred property of the adhesive is a suitable thermal expansion coefficient, so that during the process the thermal expansion of the adhesive will not differ too greatly from that of the surrounding material. The adhesive selected should also preferably have a short hardening time, preferably of a few seconds at most. In this time the adhesive should harden at least
15 partly, so that the adhesive will be able to hold the component in place. The final hardening can take clearly more time and can indeed be planned to take place in connection with a later process stage. The adhesive should also withstand the process temperatures used, for example, heating to a temperature of 100 - 265 °C a few times, and other manufacturing-process strain, for example, chemical or mechanical strain. The
20 adhesive preferably has an electrical conductivity that is of the same order as that of insulating materials.

A suitable insulating-material layer 1 is selected as the base material of the electronic module, for example, a circuit board. The insulating-material layer 1 can be, for
25 example, a polymer base, such as a glass-fibre-reinforced epoxy sheet FR4. Other examples of suitable materials for the insulating-material layer 1 are PI (polyimide), FR5, aramid, polytetrafluoroethylene, Teflon®, LCP (liquid crystal polymer), and a precured binder layer, i.e. prepreg.

30 Using a suitable method, recesses or vias, selected according to the size and mutual position of the components 6 glued to the insulator layer 10, are made in the insulating-

material layer 1. The recesses or vias can also be made slightly larger than the components 6, in which case the alignment of the insulating-material layer 1 relative to the insulator layer 10 and the components 6 will not be so critical. If in the process an insulating-material layer 1, in which vias are made for the components 6, is used, certain advantages can be gained by using additionally a separate insulating-material layer 11, in which holes are not made. Such an insulating-material layer 11 can be located on top of the insulating-material layer 1, to cover the vias made for the components.

The insulating-material layer 1 can also be made in such a way that insulating material in a liquid form is spread on top of the insulator layer 10 and the component 6, or a partly unhardened insulating-material sheet is placed on them. After this, the insulating material is cured, which creates the insulating-material layer 1.

If a second conductor layer is desired in the electronic module being manufactured, this can be made, for example, on the surface of the insulating-material layer 1. In embodiments, in which a second insulating-material layer 11 is used, the conductor layer can be made on the surface of this second insulating-material layer 11. Conductor patterns 19 can be made from the second conductor layer 9. The conductor layer 9 can be made, for example, in a similar manner to the conductor membrane 4. However, it is not necessary to make a second conductor membrane 9 in simple embodiments and when making simple electronic modules. A second conductor membrane 9 can, however, be exploited in many ways, such as an additional space for conductor patterns and components 6 and protecting the entire module from electromagnetic radiation (EMC protection). A second conductor membrane 9 can also be used to reinforce the structure and reduce, for example, warping of the module.

Vias are made in the electronic module, through which electrical contacts can be formed between the contact areas of the components 6 and the conductor layer 4. For the making of the vias, the contact openings 17 are cleaned of adhesive and other materials that may have entered the openings. This is naturally performed from the direction of the second surface of the conductor material 4, as the components are glued to the first surface. In

connection with the cleaning of the contact openings, it is also possible to clean the contact areas 7 of the components 6, which will further improve the preconditions for the manufacture of a high-quality electrical contact. Cleaning can take place, for example, using plasma technology, chemically, or with the aid of a laser. If the contact openings
5 17 and the contact areas are already sufficiently clean, cleaning can naturally be omitted.

After cleaning, it is also possible to check the success of the alignment of the component 6, as the contact areas 7 of a correctly aligned component will appear through the contact openings 17, when viewed from the direction of the conductor layer 4.

10

The success of the alignment of the component 6 can also be checked prior to cleaning, if the adhesive does not fill the contact openings 17, the adhesive is transparent, or if the conductor layer 4, the insulator layer 10, and the possible support layer 12 are so thin that the contact areas 7 or the component can be seen through the layers. Checking is
15 easiest when a transparent adhesive is used.

After this, a conductor material is brought to the holes 17, in such a way that an electrical contact is formed between the components 6 and the conductor layer 4. The conductor material can be made, for example, by filling the contact openings with an electrically
20 conductive paste. The conductor material can also be made using one of the several growing methods known in the circuit-board industry. At present, the best electrical contacts are made by forming a metallurgical joint, for example, by growing the conductor material using a chemical or electrochemical method. The intention is thus to
25 always use such methods, at least in the most demanding embodiments. One good alternative is to grow a thin layer using a chemical method and to continue the growth with a more economical electrochemical method. In addition to these methods, it is of course also possible to use some other method, which is advantageous in terms of the final result.

30 In the following, some possible embodiments will be examined in greater detail, with the aid of the procedural stages shown in Figures 1 - 9.

Stage A (Figure 1):

In stage A, a suitable layered membrane, which comprises a conductor layer 4 and an insulator layer 10 on the first side of the conductor layer 4, is selected as the starting material for the process. A layered membrane, in which a support layer 12 is on one surface of the conductor layer 4, can also be selected as the starting material. The support layer 12 is optional and is shown by a broken line and only in Figure 2. The layered membrane can be manufactured, for example, by taking a support base 12 suitable for processing and attaching a suitable conductor membrane to the surface of this support base 12, to create a conductor layer 4, as well as an insulator membrane to create the insulator layer 10.

The support base 12 can be, for example, of an electrically conductive material, such as aluminium (Al), or of an insulating material, such as a polymer. The conductor layer 4 can be created, for example by attaching thin metal foil to one surface of the support base 12, for example, by laminating it from copper (Cu). The metal foil can be attached to the support base, for example, by using an adhesive layer, which is spread on the surface of the support base 12 or metal foil, prior to the lamination of the metal layer. At this stage, there need be no patterns in the metal foil.

The insulator layer 10, can in turn be of epoxy, for example.

Stage B (Figure 2):

Contact openings 17 are made from the vias required by the electrical contacts of the components. The contact openings 17 are made through the insulator layer 10 and the conductor layer 4, for example, with a laser or mechanically by drilling. In the embodiment of the figure, the contact openings 17 are drilled from the direction of the first surface of the conductor layer and extend to the material of the support layer 12. In the embodiment of the figure, a via 3, which can be used as an aid in aligning, is made in addition to the contact openings 17.

Stage C (Figure 3):

In stage C, an adhesive layer 5 is spread on top of the insulator layer 10, in the areas to which the components 6 are to be attached. These areas can be termed connection areas.

- 5 The adhesive layers 5 can be aligned, for example, with the aid of the contact openings 17. The thickness of the adhesive layer is selected in such a way that the adhesive completely fills the space between the component 6 and the insulator layer 10, when the component 6 is pressed onto the adhesive layer 5. If the component 6 includes contact protrusions 7, the thickness of the adhesive layer 5 should be greater, for example, about
- 10 1.1 - 10 times, than the height of the contact protrusions 7, so that the space between the component 6 and the insulator layer 10 will be well filled. The surface area of the adhesive layer 5 formed for the component 6 can also be slightly greater than the corresponding surface area of the component 6, which will also help to reduce the risk of inadequate filling.

15

- Stage C can be modified in such a way that the adhesive layer 5 is spread on the connector surfaces of the components 6, instead of on the connector areas of the insulator layer 10. This can be performed, for example, in such a way that the component is dipped in adhesive before it is assembled in place in the electronic module. It is also
- 20 possible to proceed by spreading the adhesive on both the connector areas of the insulator layer 10 and on the connector surfaces of the components 6.

The adhesive used is thus an electrical insulator, so that electrical contacts between the contact areas 7 of the components 6 do not arise in the adhesive layer 5 itself.

25

Stage D (Figure 4):

- In stage D, the components 6 are set in place in the electronic module. This can be done, for example, by using the aid of an assembly machine to press the components 6 into the
- 30 adhesive layer 5. In the assembly stage, it is possible to proceed in the manner disclosed in the publications US 6,284,564 B1 and US 6,475,877 B1, while it is in any case

possible to align the components 6 equally accurately in place with the aid of the contact openings 17. In more approximate alignment, it is also possible to use the vias 3 or other available alignment marks, if such have been made in the board.

- 5 The components 6 can be glued singly, or in suitable groups. The typical procedure is for the module blank to be brought to a suitable position relative to the assembly machine, after which the component 6 is aligned and pressed onto the module blank, which is held stationary during alignment and attachment.

10 **Stage E (Figure 5):**

- An insulating-material layer 1, in which there are ready made holes 2 or recesses for the glued components 6, is placed on top of the insulator layer 10. The insulating-material layer 1 can be manufactured from a suitable polymer base, in which holes or recesses,
15 selected according to the size and position of the components 6, are made using some suitable method. The polymer base can be, for example, a pre-preg base, which is known and widely used in the circuit-board industry.

- It is best to perform stage E only after the adhesive layer 5 has been cured, or otherwise
20 hardened sufficiently for the components 6 to remain in place while the insulating-material layer 1 is set in place.

- The insulating-material layer 1 can also be made in such a way that a sheet of insulating material, which is hardened later, with no holes in it is placed on top of the component
25 and the insulator layer 10. Such a sheet can be, for example, suitably selected prepreg. The insulating-material layer 1 can also be made in such a way that an insulating material, which is later hardened, is spread in a liquid form on top of the component and the insulator layer 10.

30 **Stage F (Figure 6):**

In stage F, an unpatterned insulating-material layer 11 is set on top of the insulating-material layer 1 and then a conductor layer 9 is set on top of it. Like the insulating-material layer 1, the insulating-material layer 11 can be manufactured from a suitable polymer membrane, for example, from the aforementioned pre-preg base. The conductor
5 layer 9 can be, for example, copper foil, or some other membrane suitable for the purpose.

Stage F is advantageous in embodiments, in which the insulating-material layer 1 contains open holes 2 around the components 6 and also if it is desired to attach a
10 conductor layer 9 to the opposite side of the insulating-material layer 1. The insulating material 11 will then fill the openings 2 of the components and secure the conductor layer 9 and the insulating-material layer 1 to each other. It is also possible to proceed in such a way that the openings 2 are filled with a separate filler. The second conductor layer 9 can also be attached directly against the insulating-material layer 1, before the
15 layer 1 is cured.

Stage F is thus advantageous in some embodiments, but in most embodiments can just as well be omitted or replaced with another kind of procedure.

20 **Stage G (Figure 7):**

In this stage, the layers 1, 11, and 9 are pressed with the aid of heat and pressure; in such a way that the polymer (in the layers 1 and 11) forms a unified and tight layer around the components 6 between the conductor layers 4 and 9. This procedure makes the second
25 conductor layer 9 quite even and flat.

When manufacturing simple electronic modules including a single conductor pattern layer 14, stage F can even be entirely omitted, or the layers 1 and 11 can be laminated to the structure without the conductor layer 9.

30

Stage G is thus closely related to stage F, so that the modifications presented above in

connection with stage F also concern stage G.

If the layered membrane includes a support layer 12, the support layer 12 can be detached or otherwise removed from the structure in this stage. The removal can be
5 performed, for example, mechanically or by etching.

In an embodiment, in which there is a thick unified conductor layer (4 and 12 together) on the surface of the insulating-material layer 1, a portion of the conductor layer corresponding to the support layer 12 can be etched away. In this way it is possible to
10 open the contact openings 17 on the second side of the conductor layer 4. The contact openings 17 will then, however, be generally filled with adhesive 5.

After this, the contact openings 17 are cleaned of adhesive using a suitable method, for example, chemically, by a laser, or by plasma etching. At the same time, the contact
15 areas 7 of the component, which are located on the "bottom" of the contact openings 17, are also cleaned.

In this stage, if it is so wished, other holes, for example, a hole 3 through the insulating-material layer 1 for a via, can also be made.

20

Stage H (Figure 8):

In stage H, conductor material is grown in the contact openings 17. In the example process, the conductor material is grown at the same time also elsewhere on top of the
25 base, thus increasing the thickness of the insulating layers 4 and 9 too. If desired, conductor material can also be grown in the hole 3.

The conductor material to be grown can be, for example, copper, or some other sufficiently electrically conductive material. The selection of the conductor material
30 takes into account the ability of the material to form an electrical contact with the material of the contact protrusions 7 of the component 6. In one example process, the

conductor material is mainly copper. The copper metallizing can be performed by depositing a thin layer of chemical copper in the holes 17, after which plating is continued using an electrochemical copper-growing method. Chemical copper is used in the example because it will also form a deposit on top of the adhesive and act as an electrical conductor in electrochemical plating. The metal can thus be grown using a wet-chemical method, so that the growing is cheap and the conductor structure is of good quality.

Stage H is intended to form an electrical contact between the component 6 and the conductor layer 4. Thus, in stage H it is not essential to increase the thickness of the conductor layers 4 and 9, but instead the process can equally well be designed so that in stage H the holes 17 are only filled with a suitable material. The electrical contact can be made, for example, by filling the contact openings 17 with an electrically conductive paste, or by using some other suitable microvia metallizing method.

Stage I (Figure 9):

In stage I, the desired conductor patterns 14 and 19 are made from the conductor layers 4 and 9 on the surfaces of the base. If in the embodiment only the conductor layer 4 is used, the patterns are formed only on one side of the base. It is also possible to proceed by forming conductor patterns only from the conductor layer 4, even though a second conductor layer 9 is used in the embodiment. In such an embodiment, the unpatterned conductor layer 9 can act, for example, as a layer that supports or protects the electronic module mechanically, or as protection against electromagnetic radiation.

The conductor patterns 14 can be made by removing the conductor material of the conductor layer 4 from outside the conductor patterns. The conductor material can be removed, for example, using some of the patterning and etching methods that are widely used and well known in the circuit-board industry.

After stage I, the electronics module includes a component 6, or several components 6,

as well as conductor patterns 14 and 19 (in some embodiments, only the conductor patterns 14), with the aid of which the component 6, or components can be connected to an external circuit, or to each other. The preconditions then exist for manufacturing an operational totality. The process can thus be designed in such a way that the electronic module is ready after stage I and Figure 9 indeed shows an example of one possible electronic module. If desired, the process can also be continued after stage I, for example, by coating the electronic module with a protective agent, or by manufacturing additional conductor pattern layers on the first and/or second surface of the electronic module.

The examples of the above series of figures show some possible processes, with the aid of which our invention can be exploited. However, our invention is not restricted only to the processes described above, but instead the invention also covers other various processes and their end products, taking into account the full scope and equivalence interpretation of the Claims. The invention is also not restricted to only the constructions and methods shown by the examples, but instead it will be obvious to one versed in the art that the various applications of our invention can be used to manufacture very many different kinds of electronic modules and circuit-boards, which differ even greatly from the examples described above. The components and circuits of the figures are thus shown only for the purpose of illustrating the manufacturing process. Thus many alterations can be made to the processes of the examples described above, without, however, deviating from the basic idea according to the invention. The changes can relate, for example, to the manufacturing techniques described in the different stages, or to the mutual order of the process stages.

Claims:

1. Method for manufacturing an electronic module, which electronic module includes at least one component (6), which has at least one contact area (7), which is connected
 5 electrically to a conductor-pattern layer (14), c h a r a c t e r i z e d in that, the method comprises
- taking a layered membrane, which comprises at least a conductor layer (4) and an insulator layer (10) on the first surface of the conductor layer (4),
 - making contact openings (17) in the conductor layer (4), the mutual positions of
 10 which correspond to the mutual positions of the contact areas (7) of each component (6) to be connected and which penetrate both the conductor layer (4) and the insulator layer (10),
 - after the manufacture of the contact openings (17), attaching each component (6) to the surface of the insulator layer (10) of the layered membrane, positioned such that
 15 the contact areas (7) of the component (6) become aligned on the corresponding contact openings (17),
 - making, at least in the contact openings (17) and the contact areas (7) of the component (6), a conductor material that connects the component (6) to the conductor layer (4), and
 - 20 – patterning the conductor layer (4) to form a conductor-pattern layer (14).
2. Method according to Claim 1, c h a r a c t e r i z e d in that, before the contact openings (17) are made, the layered membrane consists of a conductor layer (4) and an insulator layer (10) on the first surface of the conductor layer (4).
 25
3. Method according to Claim 1, c h a r a c t e r i z e d in that before the contact openings (17) are made, the layered membrane comprises a support layer (12) on the second surface of the conductor layer (4).

4. Method according to any of Claims 1 - 3, characterized in that before the contact openings (17) are made, the conductor layer (4) of the layered membrane contains essentially all the conductor material, from which the conductor-pattern layer (14) is later created.

5

5. Method according to any of Claims 1 - 4, characterized in that the insulator layer (10) of the layered membrane is of epoxy.

10

6. Method according to any of Claims 1 - 5, characterized in that the thickness of the insulator layer (10) of the layered membrane is less than 10 micrometres, preferably in the range 4 - 7 micrometres.

15

7. Method according to any of Claims 1 - 6, characterized in that the component is attached to the insulator layer (10) by an insulating adhesive (5).

8. Method according to any of Claims 1 - 7, characterized in that the conductive material connecting the component (6) to the conductor layer (4) is manufactured by using a chemical and/or electrochemical metallization method.

20

9. Method according to any of Claims 1 - 8, characterized in that the conductive material connecting the component (6) to the conductor layer (4) is formed by filling the contact openings (17) with a conductive material, for example, a conductive paste.

25

10. Method according to any of Claims 1 - 9, characterized in that at least one second conductor-pattern layer (19) is manufactured in the electronic module.

11. Method according to any of Claims 1 - 10, characterized in that more than one component (6) is placed in the electronic module and the embedded components (6) are connected electrically to each other in order to create an operational totality.

30

12. Method according to any of Claims 1 - 11, in which at least one component (6) to be attached to the conductor layer (4) is an unpacked microcircuit chip.

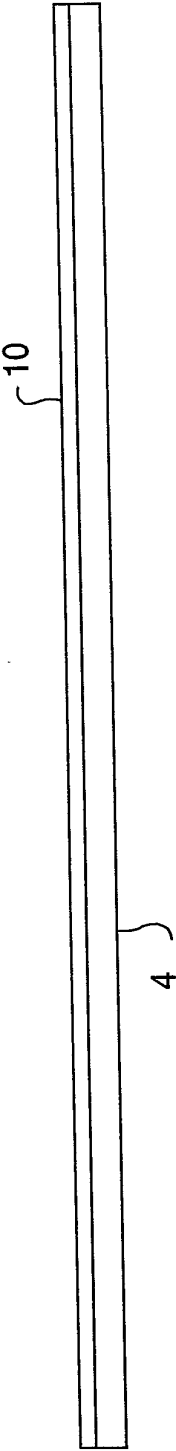


Fig. 1

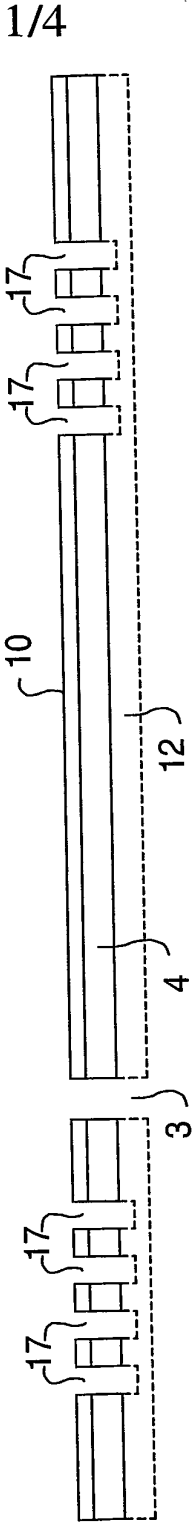


Fig. 2

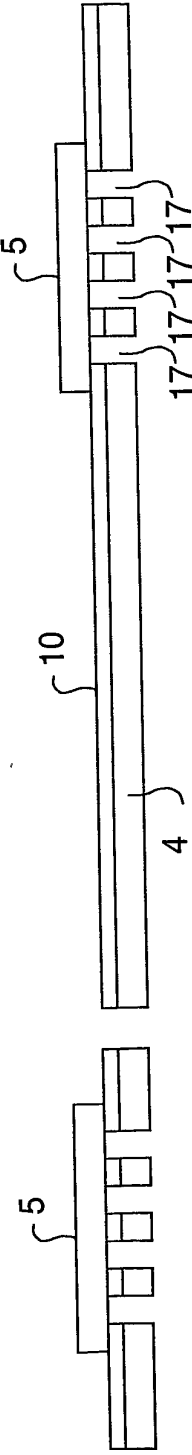


Fig. 3

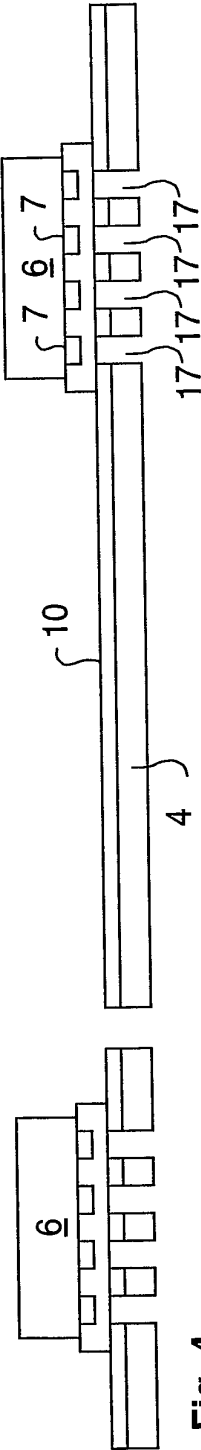


Fig. 4

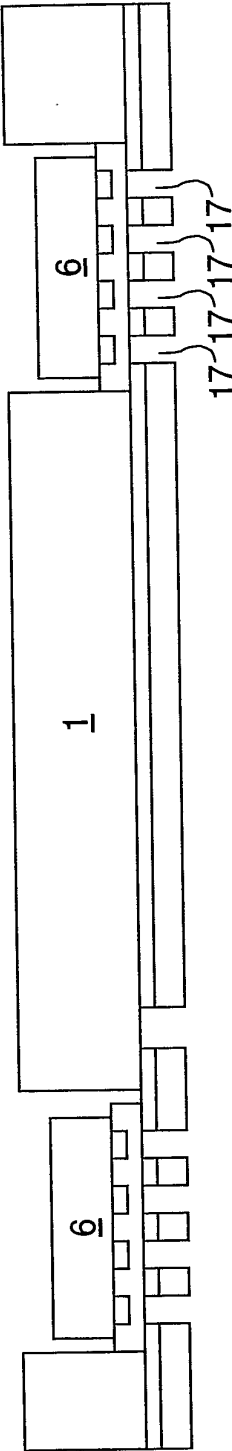
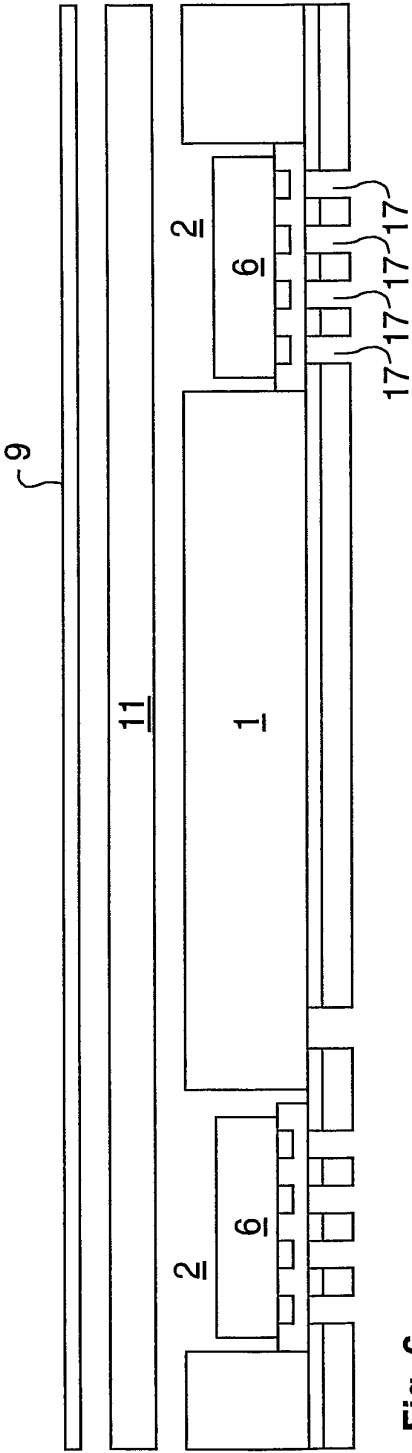
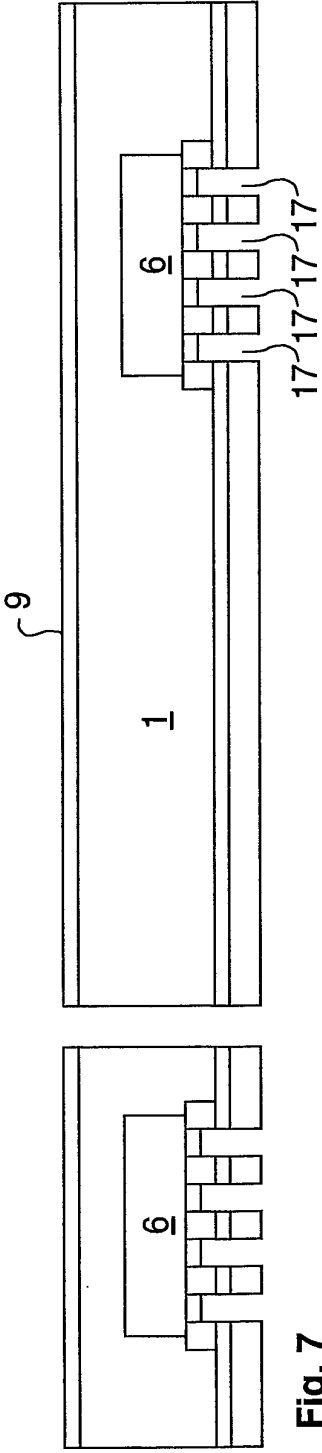


Fig. 5



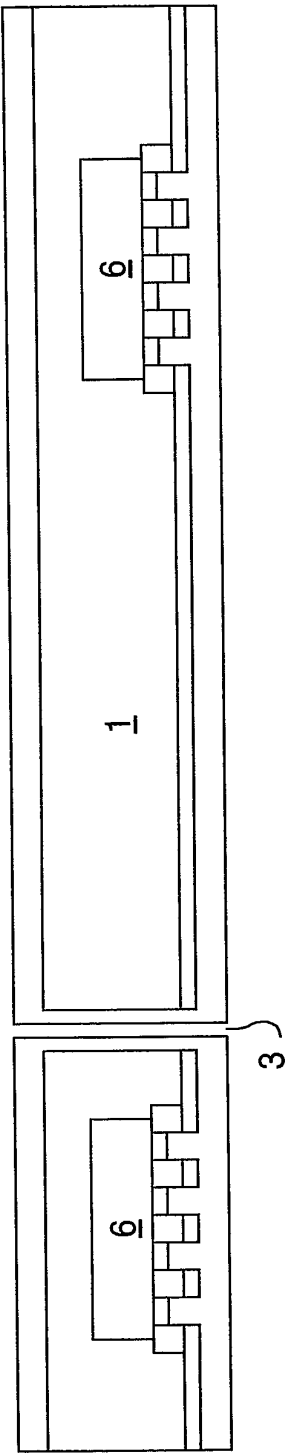


Fig. 8

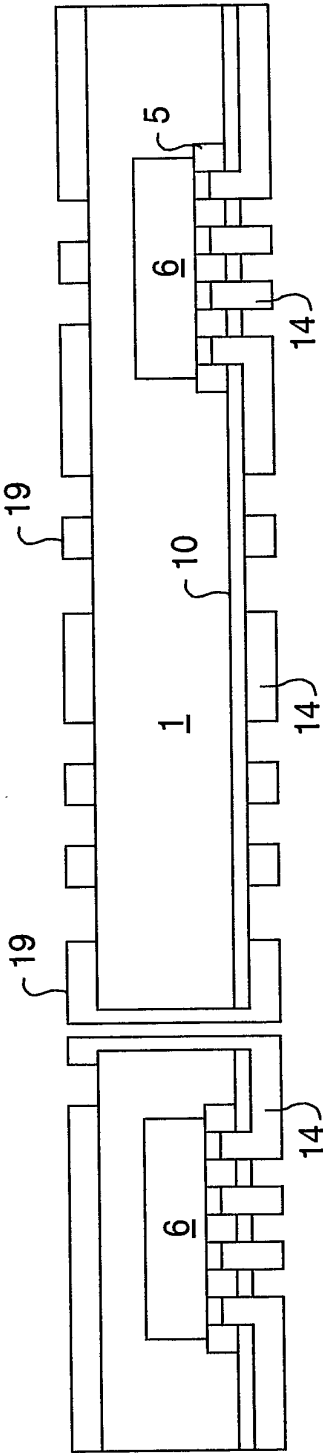


Fig. 9

PIIRIMODUULI JA MENETELMÄ PIIRIMODUULIN VALMISTAMISEKSI

Tekniikan ala

5 Keksintö liittyy piirimoduuleihin, jotka käsittävät eristekerroksen ja eristekerroksen sisällä ainakin yhden komponentin, joka käsittää kontaktialueita. Lisäksi piirimoduulit käsittävät eristekerroksen pinnalla johteita, joiden kautta komponentti voidaan kytkeä osaksi komponentin ulkopuolista piiriä. Sähköisten kontaktien muodostamista varten piirimoduulit käsittävät kontaktielementtejä komponentin kontaktialueiden ja johteiden välillä.

Keksintö liittyy myös menetelmiin edellä mainittujen piirimoduulien valmistamiseksi.

10

Tunnettu tekniikka

Tunnetussa tekniikassa on kuvattu useita erilaisia tapoja, joilla voidaan valmistaa eristemateriaalin sisään sijoitettuja komponentteja sisältäviä piirimoduuleja. Tunnettu tekniikka esittää myös useita ratkaisuja sähköisten kontaktien valmistamiseksi komponentin kontaktiterминаaleihin kontaktielementtien välityksellä sekä menetelmiä 15 kontaktielementteihin liittyvän johdekuviokerroksen valmistamiseksi.

Piirimoduuleja ja valmistusmenetelmiä arvioitaessa voidaan kiinnittää huomiota esimerkiksi menetelmällä saavutettavan piirimoduulin ominaisuuksiin, esimerkiksi hintaan, mekaaniseen kestävyys ja saavutettavissa olevaan paksuuteen (ohuuteen). Sovelluskohteista riippuen merkittäviä seikkoja ovat myös sähköisten kontaktien laatu ja kestävyys sekä koko moduulin sähköisten ominaisuuksien luotettavuus ja laatu. 20 Valmistuksen kannalta merkittäviä tarkasteltavia ominaisuuksia voivat olla myös esimerkiksi käytettävien valmistusmenetelmien luotettavuus, saanto, tehokkuus, hinta ja ympäristöystävällisyys. Valmistusmenetelmän käyttökelpoisuuteen vaikuttaa myös raaka-aineiden saatavuus ja menetelmän kyky sijoittaa piirimoduuliin erilaisia 25 komponentteja.

Ylipäätään valmistusmenetelmille ja piirimoduuleille asetetut vaatimukset ovat siis hyvin monimuotoisia ja vaihtelevat sovelluskohteen mukaan. Näin ollen alalla on edelleen tarvetta kehittää uusia piirimoduulirakenteita ja valmistusmenetelmiä, jotka voivat tarjota uusia tai parannettuja ominaisuuksia tai ominaisuusyhdistelmiä.

Yksi kehityslinja on ollut komponenttien sijoittaminen elektroniikkamoduulin sisään nystyttöminä eli ilman nystyjen kasvattamista komponentin kontaktialueiden päälle. Tällöin olisi mahdollista saada kustannusetua, sillä komponentteja ei enää tarvitse välillä kuljettaa erilliseen tuotantolaitokseen nystyjen valmistamista varten.

- 5 Hakijan omissa patentti- ja hakemusjulkaisuissa on kuvattu valmistustekniikoita, joita voidaan käyttää myös nystyttömien komponenttien yhteydessä. Kuvatut tekniikat soveltuvat erityisen hyvin sellaisille komponenteille, joiden kontaktialueiden materiaali on kupari. Hakijan omista julkaisuista läheisimmin keksintöön liittyvinä viitattakoon kansainvälisiin patenttihakemusjulkaisuihin WO 2004/089048, WO 2005/027602,
10 WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217 ja WO 2007/107630.

- Kupari on kuitenkin tällä hetkellä varsin vähän käytetty johdemateriaali puolijohdeprosesseissa. Yleisin johdemateriaali on alumiini. Piirilevyn valmistuksessa taas kupari on johteiden pääasiallinen materiaali. Piirimoduulin kupariset johteet on
15 mahdollista kasvattaa suoraan alumiinisten kontaktialueiden päälle, mutta kuparin ja alumiinin välinen kontakti on hauras, joten tällainen moduuli ei ole optimaalinen sovelluskohteeseen, jossa piirimoduuliin kohdistuu mekaanista rasitusta.

- Parannettu mahdollisuus käyttää alumiinisia tai alumiinia sisältäviä kontaktialueita tarkoittaisi siis sitä, että piirimoduulissa ja valmistusmenetelmässä olisi mahdollista
20 käyttää tavallisia puolijohdepiirejä nystyttöminä suoraan puolijohteiden valmistusprosessien ja pinnan passivoinnin jälkeen. Koska alumiini on puolijohdeteollisuudessa yleisimmin käytetty johdemateriaali, piirimoduulin kontaktielementin hyvä yhteensopivuus alumiinin kanssa varmistaisi myös sen, että sopivia puolijohdepiirejä olisi saatavilla runsaasti ja edullisesti. Tällaisia valmistusmenetelmiä onkin yritetty
25 kehittää jo vuosikymmenten ajan komponenttien paketoititekniikan piirissä. Tällaisissa komponenttien paketoitiratkaisuissa on ollut tavoitteena tekniikka, jolla komponentin ympärille voitaisiin valmistaa suhteellisen pienikokoinen komponenttipakkaus, joka sitten myöhemmin on tarkoitus liittää piirilevyyn. Paketoititekniikasta poiketen tämän keksinnön kohteena olevien piirimoduulin valmistusmenetelmien tavoitteena on
30 kyvykyys valmistaa koko piirilevy samassa prosessissa siten, että erillinen komponentin paketoitivaihe voidaan jättää kokonaan pois. Tämä ei tietenkään sulje

pois sitä mahdollisuutta, että piirimoduulin valmistusmenetelmällä valmistettaisiin ainoastaan komponenttipaketti.

Patentissa US 4 246 595, Noyori et al., on kuvattu menetelmä, jossa komponentin kontaktialueet tuodaan kontaktiin eristekalvon kanssa, johon on tehty V-muotoiset
 5 avaukset. Avauksiin ja alumiinisten kontaktialueiden pinnoille kasvatetaan ensin kerros titaania (Ti) tai kromia (Cr). Tämän välimetallikerroksen tarkoituksena on estää kuparia diffuusiota alumiiniin ja puolijohdekomponenttiin sekä parantaa kuparin ja alumiinin välistä adheesiota. Lisäksi välimetallikerros toimii sähkönsiirteena myöhemmän sähkökemiallisen kasvatuksen (electroplating) aikana, joten välimetallikerroksen on luotettavasti katettava myös avausten sivuseinämät. Titaani- tai kromi-
 10 kerroksen kasvattaminen edellyttää sputterointitekniikan käyttöä, mistä syystä avausten täytyy myös olla selvästi V-muotoisia. Sputterointi on kallista suuremmille pinnoille (piirimoduuleille) käytettynä ja lisäksi avara V-muoto pienentää saavutettavissa olevaa johdotustiheyttä. Vastaavan tyyppisiä kontaktirakenteita on kuvattu myös patenteissa
 15 US 4 783 695 ja US 4 894 115, Eichelberger et al., sekä patentissa US 5 353 195, Fillion et al.

Myöhemmin patentissa US 6 396 148, Eichelberger et al., pyritään ratkaisemaan sputterointiin liittyviä ongelmia siten, että välimetallikerros muodostetaan kasvattamalla alumiinisten kontaktialueiden pinnalle kerros nikkeliä. Patentin mukaan nikkelin
 20 kasvattaminen suoritetaan kemiallisella kasvatusmenetelmällä (electroless plating). Nikkelikerroksen päälle kasvatetaan kemiallisella kasvatusmenetelmällä vielä toinen kerros, joka peittää myös eristemateriaaliin kontakteja varten tehtyjen avausten sivuseinämät. Menetelmässä komponentit kiinnitetään ensin sivu- ja takapinnoiltaan eristekerrokseen ja tämän jälkeen komponentin etupinnalle ja kontaktialueiden päälle
 25 levitetään valokuvioitava polymeeri. Polymeeri kuvioidaan valottamalla ja kehittämällä avausten muodostamiseksi kontakteja varten.

Yksi mahdollisuus on kasvattaa nystyt piirimoduulin piirilevyosan johteiden pinnalle ja liittää komponentti johteisiin flip-chip -liitostekniikalla, esimerkiksi ultraäänibondauksella. Tällainen menetelmä on kuvattu hakijan omassa kansainvälisessä
 30 patenttihakemuskäytännössä WO 2006/134220. Flip-chip -liitostekniikoita käyttäviin menetelmiin liittyy sekä tuotannollisia että kontaktin laatuun liittyviä ongelmia.

Keksinnön kuvaus

Tämän keksinnön tarkoituksena on kehittää nystyttömien komponenttien hyödyntämistä silmällä pitäen uusi kontaktielementtirakenne ja tällaista rakennetta käyttävä piirimoduuli ja valmistusmenetelmä.

- 5 Keksinnön yhden näkökannan mukaan piirimoduulissa käytetään nystyöntä komponenttia, jonka kontaktialueiden materiaali on eri metallia tai metalliseosta kuin piimoduulin johdekerrosten johteet. Komponentin kontaktialueet ja piirimoduulin johteet yhdistetään toisiinsa kontaktielementtien avulla, jotka sisältävät kontaktialueen materiaalin pinnalla välikerroksen, joka sisältää kolmatta metallia tai metalliseosta joka poikkeaa kontaktialueiden ja johteiden materiaalista. Lisäksi kunkin kontaktielementin välikerroksen ja komponentin kontaktialueen välinen kontaktipinta-ala on pienempi kuin kontaktialueen pinta-ala.

- 15 Keksinnön toisen näkökannan mukaan luodaan valmistusmenetelmä edellä kuvatun piirimoduulin valmistamiseksi, jossa komponentti kiinnitetään johdekalvoon tai johdekuviokerrokseen polymeerikerroksen avulla ja kontaktielementit valmistetaan polymeerikerroksen läpi. Kontaktielementtejä valmistettaessa kontaktialueiden päällä olevaan polymeerikerrokseen tehdään kontaktireiät kontaktialueiden kohdille. Kontaktireiät mitoitetaan siten, että kunkin kontaktireiän ja vastaavan kontaktialueen välinen kontaktipinta-ala on pienempi kuin kontaktialueen kokonaispinta-ala. Tämän jälkeen kontaktireiät täytetään johdemateriaalilla siten, että täyttäminen aloitetaan pinnoittamalla kontaktialueiden pinnalle välikerros esimerkiksi käyttämällä yhtä tai useampaa kemiallista metallinkasvatusmenetelmää.

Näin saadaan aikaan uudenlainen piirimoduuli ja valmistusmenetelmä, joka voi tarjota joitakin etuja joidenkin piirimoduulien sovelluskohteiden kannalta.

- 25 Lisäksi keksinnöllä on lukuisia erityisiä sovellusmuotoja, jotka tarjoavat lisää etuja.

Yhdessä sovellusmuodossa piirimoduulissa käytetään komponenttia, jonka kontaktialueiden materiaali sisältää alumiinia ja kontaktielementit käsittävät näiden alumiinia sisältävien kontaktialueiden pinnalla sinkkiä sisältävän kerroksen. Lisäksi kontaktielementit on valmistettu siten, että sinkkiä sisältävän kerroksen ja

kontaktialueen välinen kontaktipinta-ala on pienempi kuin itse kontaktialueen kokonaispinta-ala.

- 5 Sinkkiä sisältävän kerroksen on havaittu olevan hyödyllinen sähköisen kontaktin laadun kannalta, sillä sinkkiä sisältävän kerroksen pinnoittaminen alumiinisen kontaktialueen pinnalle estää alumiinipinnan uudelleen oksidoitumisen ja mahdollistaa hyvän adheesion muodostumisen alumiinin ja seuraavan kerroksen välille. Lisäksi sinkkiä sisältävä kerros parantaa alumiinin ja muuta metallia olevan välikerroksen välisen rajapinnan kautta muodostuvan kontaktin mekaanista kestävyyttä sivuttaissuuntaista rasitusta vastaan.
- 10 Olemme havainneet, että erityisen hyvä mekaaninen kestävyys saavutetaan käyttämällä kaksinkertaista sinkaattiprosessia, jossa komponentit sisältävä aihio altistetaan sinkaattiprosessille ainakin kahteen kertaan. Näin alumiinisten kontaktipintojen päälle saadaan kasvatettua tasaisempi ja tiiviimpi kerros sinkkiä. Yksinkertaisen sinkaattikäsittelyn jälkeen kontaktipinnoilla on sinkkiä tyypillisesti vain aluittain tai
- 15 kerros on huokoinen, joten edullisessa sovellusmuodossa käytetään kaksinkertaista sinkaattiprosessia.
- Mahdollisuus käyttää kontaktialuetta kapeampaa kontaktielementtiä voi puolestaan tarjota etua esimerkiksi siinä muodossa, että myös kontaktielementteihin liittyvät johteet voidaan näin valmistaa kapeiksi, varsinkin sellaisissa sovellusmuodoissa, joissa
- 20 kontaktielementti on korkeussuunnassa oleellisesti tasalevyinen tai ainoastaan maltillisesti komponenttia kohti kapeneva.
- Valmistusmenetelmän sovellusmuodossa, jossa johdekalvoon tai johdekuviokerrokseen tehdään kontaktiaukot ennen komponentin kiinnittämistä, komponentti voidaan kiinnittää kontaktiaukkojen suhteen kohdistettuna ja lisäksi kontaktielementtien valmistukseen tarvittavat kontaktireiät voidaan valmistaa näiden kontaktiaukkojen
- 25 kautta käyttämällä johdekalvon tai johdekuviokerroksen materiaalia maskina. Tällaisessa sovellusmuodossa saavutetaan etua kontaktielementtien ja kontaktialueiden välisen kohdistuksen osalta. Lisäksi saavutetaan etua kontaktireikien valmistuksen kannalta, koska reiät voidaan avata esimerkiksi CO₂-laserilla.
- 30 Sovellusmuodossa, jossa kontaktireiät avataan laserilla, kontaktireikiä on mahdollista avata komponentti tai komponenttiryhmä kerrallaan ja näin valmistaa ensin

ensimmäinen välikerros ensin avattujen kontaktireikien kautta ensimmäisten komponenttien kontaktialueiden päälle ja sitten myöhemmin valmistaa toinen välikerros myöhemmin avattujen kontaktireikien kautta toisten komponenttien kontaktialueiden päälle. Näin on mahdollista sovittaa samaan prosessiin komponentteja, joiden kontaktialueiden materiaalit poikkeavat toisistaan eivätkä ole yhteensopivia samojen välikerroksen kasvatusprosessien kanssa.

Sovellusmuodoissa on myös mahdollista kiinnittää komponentit johteisiin keskenään erilaisten polymeerikerrosten välityksellä. Näin voidaan komponentin ja johteen välisen eristeen ominaisuudet sovittaa sopiviksi myös erilaisiin mekaanisiin ja sähköisiin tarpeisiin.

Kuvioiden lyhyt esittely

Kuviot 1–8 esittävät piirimoduulin välivaiheita yhden sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 9 esittää yhtä esimerkkiä yhden sovellusmuodon mukaisesta piirimoduulista

Kuviot 10–17 esittävät piirimoduulin välivaiheita toisen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuviot 18–23 esittävät piirimoduulin välivaiheita kolmannen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 24 esittää piirimoduulin yhtä välivaiheita neljännen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 25 esittää yhtä mahdollista esimerkkiä piirimoduulin kontaktielementtiä varten tehdystä kontaktireiästä ja sen mittasuhteista

Kuvio 26 esittää esimerkkejä mahdollista kontaktirei'istä

Kuvio 27 esittää joitakin sovellusmuotoja kuvion 26 kontaktireikiin valmistetuista välikerroksista

Kuvion 28 esittää yhden kontaktielementtirakenteen

Kuvion 29 esittää toisen kontaktielementtirakenteen

Kuvion 30 esittää kolmannen kontaktielementtirakenteen

Kuvion 31 esittää neljännen kontaktielementtirakenteen

Kuvion 32 esittää viidennen kontaktielementtirakenteen

5 Kuvion 33 esittää kuudennen kontaktielementtirakenteen

Keksinnön suoritusmuotoja

10 Kuviot 1–9 esittävät yhden sovellusesimerkin yhden sovellusmuodon mukaisesta valmistusmenetelmästä. Tässä sovellusmuodossa valmistus aloitetaan johdekalvosta 12, joka on esimerkiksi metallia. Sopiva johdekalvo 12 on esimerkiksi kuparikalvo, jonka paksuus on välillä 1–70 μm , tyypillisesti välillä 3–12 μm . Paljaan johdekalvon 12 sijasta lähtömateriaalina voidaan käyttää myös kerroskalvoa, joka käsittää johdekalvon 12 ja tämän pinnalla eristekerroksen 13, joka kuviossa 1 on esitetty katkoviivoituksella. Seuraavassa kuvatuissa sovellusmuodoissa on mahdollista käyttää johdekalvon 12 sijasta tällaista kerroskalvoa 12, 13.

15 Kuvion 1 esittämästä poiketen voidaan käyttää myös sellaista kerroskalvoa, joka käsittää tukikalvon johdekalvon 12 toisella pinnalla. Tukikalvo on johdekalvoon liitettävien komponenttien suhteen johdekalvon vastakkaisella pinnalla. Mikäli kerroskalvo käsittää myös eristekerroksen 13, tukikalvo on tällöin johdekalvon vastakkaisella pinnalla kuin eristekerros 13. Tukikalvoa voidaan käyttää esimerkiksi parantamaan johdekalvon 12 tai kerroskalvon 12, 13 mekaanista jäykkyyttä ja käsiteltävyyttä valmistusprosessin alkuvaiheessa. Tukikalvo on kuitenkin tarkoitus poistaa valmistusprosessin myöhemmässä vaiheessa. On myös mahdollista menetellä siten, että valmistus aloitetaan tukikalvosta ja tämän pinnalle valmistetaan johdekalvo 12, joka on kuvioitu tai kuvioimaton. Sovellusesimerkeissä kuvatut prosessiesimerkit ja 20 vaiheet voidaan suorittaa vastaavalla tavalla myös tukikalvoa käytettäessä, vaikka tätä ei olisi erikseen mainittu. Jäljempänä tulevassa kuvauksessa on kuitenkin viitattu tukikalvoon ainoastaan silloin, kun prosessissa on tukikalvoa käyttävän sovellusmuodon osalta jotakin erityistä huomattavaa. Itse tukikalvo voi olla esimerkiksi sähköäjohtavaa materiaalia, kuten alumiinia (Al), terästä tai kuparia, tai eristävää materiaalia, kuten

polymeeriä. Tukikalvo voi olla paksuudeltaan esimerkiksi 25–400 µm. Tyypillinen tukikalvon paksuus on välillä 35–105 µm.

Seuraavaksi johdekalvoon 12 tehdään kontaktiaukot 8, jotka sijoitetaan johdekalvolle 12 siten, että ne sijaitsevat valmistettavaan moduuliin sijoitettavien komponenttien kontaktiterminaalien kanssa kohdakkain. Johdekalvoon 12 valmistetaan siis kutakin komponentin kontaktiterminaalia varten oma kontaktiaukko 8. Kontaktiaukot 8 valmistetaan tässä sovellusmuodossa UV-laserin avulla. Kontaktiaukot 8 voidaan valmistaa myös esimerkiksi mekaanisesti poraamalla, jyrsimällä tai etsaamalla. Tukikalvoa käyttävässä sovellusmuodossa kontaktiaukot 8 valmistetaan mielellään vastakkaisen pinnan suunnasta siten, että ne läpäisevät kokonaan johdekalvon 12. Kontaktiaukkojen ei kuitenkaan tarvitse läpäistä tukikalvoa vaan menetelmä voidaan aivan hyvin suunnitella myös siten, että kontaktiaukot 8 ainoastaan ulottuvat tukikalvon materiaalin pintaan saakka tai muodostavat syvennykset tukikalvon materiaaliin kuitenkin tätä läpäisemättä. Kontaktiaukon ei tarvitse myöskään läpäistä kokonaan johdekalvoa, mikäli käytetään paksua johdekalvoa, joka ohennusetsataan ohuemmaksi myöhemmässä vaiheessa.

Kuvion 1 sovellusmuodossa kontaktiaukot 8 valmistetaan siten, että kontaktiaukon 8 koko on pienempi kuin kontaktiaukon 8 kohdalle sijoitettavan kontaktiterminaalin kontaktipinta-ala. Muodoltaan kontaktiaukko on tyypillisesti pyöreä, mutta muita muotoja voidaan myös käyttää. Kontaktiaukon 8 muoto ja koko valitaan siten, että kontaktiterminaalin kontaktipinta kykenee kokonaan peittämään kontaktiaukon 8.

Kuvion 2 mukaisesti valmistusta jatketaan levittämällä johdekalvon 12 pinnalle, komponenttien liitântäalueille liimakerrokset 5. Tällöin liimakerrokset 5 peittävät myös kontaktiaukot 8. Vaihtoehtoisesti liima 5 voidaan levittää komponenttien pinnoille. Liima voidaan levittää myös sekä komponentin että johdekalvon 12 pinnalle. Tyypillisesti liima levitetään paikallisesti siten, että liimakerrokset 5 tulevat sijaitsemaan ainoastaan komponenttien liitântäalueilla.

Liimalla tarkoitetaan materiaalia, jolla komponentit voidaan kiinnittää alustana olevaan johdekalvoon 12 tai eristekerrokseen 13. Liiman yksi ominaisuus on se, että liima voidaan levittää liimattavalle pinnalle suhteellisen juoksevassa tai muutoin pinnanmuotoihin mukautuvassa muodossa, esimerkiksi kalvon muodossa. Liiman

5 toinen ominaisuus on se, että levittämisen jälkeen liima kovettuu tai voidaan kovettaa ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan (johdekalvon 12 suhteen) ainakin niin kauan kunnes komponentti kiinnitetään rakenteeseen jollakin muulla tavalla. Liiman kolmas ominaisuus on adheesiokyky eli
5 kyky tarttua liimattaviin pintoihin.

Liimaamisella taas tarkoitetaan liimattavien kappaleiden kiinnittämistä toisiinsa liiman avulla. Sovellusesimerkeissä liimaa tuodaan komponentin ja alustana olevan johdekalvon 12 tai eristekerroksen 13 väliin ja asetetaan komponentti alustan suhteen sopivaan asemaan, jossa liima on kosketuksessa komponentin ja alustan kanssa ja
10 ainakin osittain täyttää komponentin ja alustan välisen tilan. Tämän jälkeen liiman annetaan (ainakin osittain) kovettua tai liima aktiivisesti kovetetaan (ainakin osittain) siten, että komponentti kiinnittyy liiman avulla alustaan. Joissakin sovellusmuodoissa komponentin kontaktiulokkeet saattavat liimauksen aikana työntyä liimakerroksen läpi kosketukseen alustan kanssa.

15 Sovellusmuodoissa käytettävä liima on tyypillisesti epoksipohjainen liima, esimerkiksi lämpökovetteinen epoksiliima. Liima valitaan siten, että käytettävällä liimalla on riittävä adheesio alustaan ja komponenttiin. Yksi edullinen liiman ominaisuus on sopiva lämpölaajenemiskerroin, jolloin liiman lämpölaajeneminen ei poikkea liian paljon ympäröivän materiaalin lämpölaajenemisesta prosessin aikana. Olisi myös eduksi,
20 mikäli valittavalla liimalla olisi lyhyt kovetusaika, mielellään korkeintaan muutamia sekunteja. Tässä ajassa liiman olisi hyvä kovettua ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan. Lopullinen kovettuminen voi viedä selvästi enemmän aikaa ja loppukovetus voidaankin suunnitella tapahtuvaksi myöhempien prosessivaiheiden yhteydessä. Lisäksi liiman valinnassa otetaan huomioon myöhempien
25 valmistusprosessin vaiheiden aiheuttama rasitus, kuten terminen, kemiallinen tai mekaaninen rasitus. Liiman sähkönjohtavuus on mielellään eristemateriaalien sähkönjohtavuuden luokkaa.

Seuraavaksi otetaan komponentit 6 ja 16, jotka käsittävät kontaktiterminaleja 7 ja 17. Molemmat komponentit 6 ja 16 ovat puolijohdekomponentteja, esimerkiksi
30 prosessoreita, muistisiruja tai muita mikropiirejä. Komponentin 6 kontaktiterminaalit ovat kontaktialueita 7, jotka sijaitsevat oleellisesti komponentin pinnan tasalla. Tällaiset komponentin 6 kontaktialueet 7 on muodostettu puolijohdekomponentin valmistus-

prosessissa puolijohdetehtaalla. Kontaktialueen 7 muodostaa tyypillisesti prosessissa käytettyä metallia olevan johdekuvion pinta. Puolijohdekomponenttien valmistusprosessissa käytettävä metalli on yleisimmin alumiini, mutta myös muita metalleja, metalliseoksia tai muita johdemateriaaleja voidaan käyttää. Esimerkiksi kuparin käyttö on yleistynyt puolijohdekomponenttien valmistusprosesseissa.

Komponentin 16 kontaktiterminaalit ovat kontaktinystyjä 7, jotka ulkonevat komponentin pinnan tasalta. Tällaiset kontaktinystyt 17 on valmistettu nystytysprosessissa puolijohdekomponentin 16 valmistamisen jälkeen tyypillisesti erillisessä tehtaassa. Kontaktinysty 17 voi sisältää yhtä tai useampaa metallia, metalliseosta tai muuta johdemateriaalia. Tyypillisesti kontaktinystyn 17 uloin pinta eli kontaktipinta on valmistettu kuparista tai kullasta.

Komponentit 6 ja 16 kohdistetaan kontaktiaukkojen 8 suhteen siten, että kukin kontaktiterminaalit 7, 17 tulee vastaavan kontaktiaukon 8 kohdalle, ja painetaan vasten liimakerrosta 5. Tämän jälkeen liima ainakin osittain kovetetaan siten, että komponenttien 6, 16 ja johdekalvon 12 suhteellinen liike kohdistuksen jälkeen saadaan estettyä tai minimoitua. Kohdistuksessa ja liimaamisessa pyritään sellaiseen aseointiin, että kontaktiaukko 8 olisi keskellä vastaavaa kontaktiterminaalit 7, 17.

Tämän jälkeen kuvion 2 esimerkissä johdekalvon 12 päälle laminoidaan eristekalvoja 11, joihin on tehty komponentteja 6, 16 varten aukot, sekä yhtenäinen eristekalvo 10, joka on kovettamatonta tai esikovetettua polymeeriä. Laminoidaessa eristekalvot 10, 11 sulautuvat yhteen ja muodostavat komponenttien 6, 16 ympärille yhtenäisen eristekerroksen 1. Kuvion 2 sovellusmuodossa eristekalvot 11 ovat polymeerillä impregnoituja kuitumattoja tai kuitumateriaalilla vahvistettuja, esikovetettua polymeeriä sisältäviä kalvoja. Polymeeri voi olla esimerkiksi epoksi ja kuituvahviste voi olla esimerkiksi lasikuitumatto. Tyypillinen esimerkki sopivasta eristekalvon 11 materiaalista onkin FR4-tyyppinen lasikuituvahvistettu epoksikalvo. Myös muita vahviste- ja polymeerimateriaaliyhdistelmiä voidaan toki käyttää. Käytettäessä useampaa eristekalvoa 11 on myös mahdollista, että kalvot ovat keskenään erilaisia.

Kuitumateriaalia on kuvattu kuvioissa 2 ja 3 aaltoviivoituksella 19. Jäljempänä tulevilla kuvioissa kuitumateriaalia 19 ei ole esitetty, mutta myös nämä rakenteet sisältävät kuitumateriaalin 19. Eristekalvon 11 tai eristekalvojen 11 sisältämä kuitumateriaali 19

toimii vahvikkeena, joka antaa valmistettavalle elektroniikkamoduulille mekaanista lujuutta. Kuvion 2 esimerkin mukaisesti eristekalvoihin 11 on tehty reiät 4 komponenttien 6, 16 kohdille. Eristekalvot 11 rei'itetään erityisesti sen takia, että eristekalvojen 11 sisältämään kuitumateriaaliin 19 saadaan valmistettua aukot 5 komponentteja varten. Ilman rei'itystä komponentit painautuisivat laminoitaessa kuitumateriaalikerroksia 19 vasten. Rei'ittämätön eristekalvo 10 sen sijaan voi sovellusmuodosta riippuen olla kuituvahvistettu tai vahvistamaton.

Eristekalvot 10, 11 valitaan tyypillisesti siten, että se sisältävät niin paljon virtauskelpoista polymeeriä, että laminointivaiheessa virtaava polymeeri riittää 10 täyttämään eristekalvoihin 11 komponentteja 6, 16 varten tehdyt reiät 4 komponenttien ympäriltä. Tällöin saadaan kuvion 3 esittämä rakenne, jossa eristekerros 1 sisältää tiiviin polymeerikerroksen, joka sisältää yhden tai useamman kuitumateriaalia 19 olevan vahvikkeen. Polymeerikerros sitoutuu tiiviisti kuitumateriaaliin 19 ja tiivis polymeerikerros kiinnittyy myös komponenttien 6, 16 pintoihin, jolloin muodostuu 15 tiivis, yhtenäinen ja mekaanisesti luja eristekerros, joka sisältää komponentteja 6, 16 ja joka on lisäksi vahvistettu kuitumateriaalilla 19.

Kuvion 2 esimerkissä käytettiin yhtenäistä eristekalvoa 10, mutta eristekalvo 10 on myös mahdollista jättää pois rakenteesta. Tällöin eristekalvo 11 tai eristekalvot 11 valitaan siten, että ne jo itsessään sisältävät riittävästi virtauskykyistä polymeeriä 20 eristekalvojen 11 sisältämien reikien 4 täyttämiseksi komponenttien 6, 16 ympäriltä. Tyypillisesti reikien 4 täytyminen on kuitenkin helpompi varmistaa käyttämällä erillistä eristekalvoa 10.

Eristekalvojen 10, 11 kanssa yhdessä rakenteeseen laminoidaan myös johdekalvo 14, joka on mielellään samanlaista ja yhtä paksua materiaalia kuin johdekalvo 12. 25 Eristekerros 1 ja komponentit 6, 16 jäävät näin vastaavanlaisten johdekalvojen 12 ja 14 väliin. Moduulinvalmistuksen tällainen välivaihe on esitetty kuviossa 3. Kuvion 3 välivaiheessa kontaktiterminaalien 7, 17 kontaktipinnoilla ja tyypillisesti myös kontaktiaukoissa 8 on liimaa. Kuvion 4 esittämässä vaiheessa tämä liima poistetaan ja muodostetaan kontaktiaukkojen 8 kohdalle kontaktireiät 18, jotka ulottuvat 30 kontaktiterminaalien 7, 17 kontaktipinnoille saakka.

Kuvioon 3 viitaten mainittakoon vielä, että rakenne voidaan valmistaa myös siten, että komponenttien 6, 16 ja johdekalvon 14 välissä kulkee yhtenäinen kerros kuitumateriaalia 19. Tällaista rakennetta voidaan käyttää silloin, kun komponenttien 6, 16 paksuus on riittävän paljon pienempi kuin eristekerroksen 1 paksuus. Rakenne voidaan valmistaa esimerkiksi siten, että rakenteeseen laminoidaan yhtenäinen eristekalvo 10, joka sisältää kerroksen kuitumateriaalia 19.

Mikäli sovellusmuodossa käytetään johdekalvon 12 pinnalla tukikalvoa, kuten on edellä kuvion 1 selityksen yhteydessä kuvattu, tukikalvo on sopivinta poistaa laminoinnin jälkeen eli kuvioden 3 ja 4 esittämien välivaiheiden välissä.

Laminoinnin ja mahdollisen tukikalvon poistamisen jälkeen poistetaan kontaktiaukkoihin 8 ja kontaktiaukkojen 8 ja kontaktiterminaalien 7, 17 väliin syntynyt liimakeros. Kuvioden sovellusmuodossa liiman poistaminen toteutetaan laserablaatiomenetelmällä käyttämällä CO₂-laseria. CO₂-laserin kyky haihduttaa orgaanisia eristeaineita, kuten epoksipohjaista liimaa, on hyvä mutta kyky haihduttaa kuparia tai muita metalleja on heikko, joten johdekalvoa 12 voidaan käyttää maskina kontaktireikien 18 valmistamiselle. Näin on mahdollista valmistaa kontaktireikiä 18, joiden halkaisija on pienempi kuin CO₂-laserin säteen halkaisija. Tämä ominaisuus muodostaa merkittävän edun, sillä CO₂-laserin säteen minihalkaisija on tyypillisesti luokkaa 75 µm, mikä on liian suuri tarkkojen elektroniikkamoduulirakenteiden valmistamista ajatellen. UV-laserilla taas tyypillisesti pystytään valmistamaan selvästi tarkempia rakenteita. UV-laserin säteen minimihalkaisija voi olla esimerkiksi 25 µm, mutta UV-laser taas ei sovellu liiman poistamiseen kontaktiaukoista 8 ja kontaktiaukkojen 8 ja kontaktiterminaalien 7, 17 välistä.

Johdekalvomaskin käyttäminen mahdollistaa siis hyvin tarkkarajaisten ja tarkasti kohdistettujen kontaktireikien 18 valmistamisen eristemateriaaliin, kuten sovellusmuodossa käytettyyn liimaan 5. Lisäksi CO₂-laserin käyttö mahdollistaa kontaktiterminaalien 7, 17 kontaktipintojen puhdistamisen samassa prosessivaiheessa ilman merkittävää vaaraa kontaktiterminaalien 7, 17 tuhoutumisesta tai vaurioitumisesta. Sovellusmuodossa johdekalvo 12 on kuparia ja komponentin kontaktiterminaalit 7, 17 ovat myös metallia, joten ne eivät ole herkkiä CO₂-laserin säteelle ja näin ollen prosessi voidaan suunnitella siten, että kontaktiterminaalien 7, 17 kontaktipinnat tulevat varmasti riittävän hyvin puhdistetuiksi. Esitetyn menetelmän etuna on siis se, että johdekalvoon

12 voidaan valmistaa kontaktiaukot 8 hyvin tarkasti UV-laserin avulla ja tämän jälkeen käyttää kontaktiaukkoja 8 maskina kontaktireikien 18 valmistamiselle epätarkemmalla mutta rakenteen kannalta turvallisemmalla CO₂-laserilla.

5 Mikäli johdekalvon 12 kontaktireiät 8 valmistettaisiin vasta tässä prosessivaiheessa, johdekalvon 12 metallin työstämiseen käytettävä menetelmä, esimerkiksi UV-laser, vaurioittaisi helpommin myös kontaktiterminaalieja 7, 17, koska johdekalvon 12 läpäisemiseen tarvittava energia on merkittävästi suurempi kuin liiman 5 tai muun kontaktiterminaalien 7, 17 ja johdekalvon 12 välissä olevan eristeen läpäisemiseen tarvittava energia. Porauksen pysäyttäminen juuri oikeaan syvyyteen olisi siis
10 haastavaan tällaisessa valmistusmenetelmässä. Lisäksi porauksen kohdistaminen olisi vaikeampaa laminoinnin aikana syntyneiden muodonmuutosten johdosta ja siitä syystä, että komponenttien kontaktiterminaalieja 7, 17 ei voi nähdä yhtenäisen metallikalvon läpi. Johdekalvoon 12 esivalmistettujen kontaktireikien 8 käyttö tarjoaakin merkittäviä etuja sekä komponenttien 7, 17 kohdistamisessa että kontaktireikien 18
15 valmistamisessa.

Kuviossa 5 kontaktireikiin 18 valmistetaan välikerros 2, joka on soveltuvaa johdemateriaalia. Välikerros 2 valmistetaan soveltuvalla kemiallisella johdemateriaalin kasvatusmenetelmällä (electroless plating). Välikerros 2 voi koostua myös kahdesta tai useammasta eri materiaalia olevasta kerroksesta, jotka valmistetaan vastaavasti kahdella
20 tai useammalla menetelmällä. Välikerroksen 2 yhtenä tarkoituksena on muodostaa kontaktireikien 18 sivuseinämille johdekalvo, joka yhdistää kontaktiterminaalien 7, 17 ja johdekalvon 12 toisiinsa. Välikerroksen 2 toisena tarkoituksena on materiaalisovituksen tarjoaminen kontaktiterminaalien 7, 17 materiaalin ja näihin yhdistettävien johdekuvioiden materiaalin välillä. Tällaista materiaalisovitusta voidaan tarvita esimerkiksi
25 mekaanisen tai sähköisen kontaktin laadun ja kestävyysvarmistamiseksi esimerkiksi silloin, kun piirimoduulin johdekuviokerrosten materiaali on kupari ja kontaktiterminaalien 7, 17 materiaali on jokin muu kuin kupari (Cu), esimerkiksi alumiini (Al).

Välikerroksen 2 valmistamisessa käytetään soveltuvaa kemiallista kasvatusmenetelmää, koska tällaisella menetelmällä on mahdollista kasvattaa johdemateriaalia myös
30 kontaktireikien 18 pystysuorille pinnoille toisin kuin esimerkiksi sputteroimalla. Sähkökemiallista menetelmää (electroplating) taas ei voi tässä vaiheessa käyttää, koska kontaktireikien 18 sivuseinämät eivät ole johtavia. Vaihtoehtoisesti voidaan käyttää V-

- muotoisesti avautuvia kontaktireikiä ja sputtertoimalla valmistettua välikerrosta 2. Tarkoitukseen soveltuvia sputteroitavia materiaaleja ovat esimerkiksi titaani-wolframi (TiW) ja kromi (Cr). TiW- tai Cr-kerroksen päälle voidaan myös kasvattaa kerros nikkeliä (Ni) ja kultaa (Au). Kuvion 5 esimerkissä käytetään kuitenkin välikerroksena 2
- 5 kemiallisella menetelmällä kasvatettua nikkeliä, jolloin välikerros 2 kasvaa samalla myös johdekalvojen 12 ja 14 pinnoille. Toinen esimerkki välikerroksesta 2 on kontaktiterminaalien 7, 17 pinnalle valmistettava sinkkiä sisältävä kerros, jonka päälle voidaan vielä valmistaa kerros nikkeliä (Ni). Lisää mahdollisia vaihtoehtoja kuvataan kuvioiden 26–33 kuvauksen yhteydessä.
- 10 Välikerroksen 2 valmistamisen jälkeen tässä sovellusmuodossa valmistamista jatketaan levittämällä moduulin molemmille pinnoille resistikerrokset 3, tyypillisesti valoresistikerrokset. Resistikerrokset 3 kuvioidaan johdekuviomaskin avulla valottamalla ja kehittämällä siten, että resisti 3 poistuu johdekuviokerrosten haluttujen johdekuvioiden kohdilta. Tämä välivaihe on kuvattu kuviossa 6. Tämän jälkeen
- 15 moduuli viedään sähkökemialliseen kylpyyn ja moduulin välikerrokseen 2 johdetaan jännite. Tällöin resistikerrosten 3 aukkoihin kasvatetaan halutut johdekuviokerrosten johteet 22, 24. Johdemateriaali kasvaa samalla myös kontaktireikiin 18 muodostaen kontaktielementeille johdeytimen, mikä käy ilmi kuviosta 7. Kuvion 7 esimerkissä johteet 22, 24 ovat sähkökemiallisesti kasvatettua kuparia. Lopuksi johteiden 22, 24
- 20 pinnalle kasvatetaan ohuet etsausmaskikerrokset. Etsausmaskina voi toimia esimerkiksi kerros tinaa (Sn).
- Seuraavaksi poistetaan resistikerrokset 3, jolloin kuvioiden sovellusmuodossa poistetun resistin alta paljastuu välikerros 2. Paljastunut osa välikerrosta 2 poistetaan esimerkiksi etsaamalla ja samoin menetellään johteiden 22 ja 24 ulkopuolelta paljastuneille osille
- 25 johdekalvoja 12 ja 14. Etsausmaskikerros suojaa tällöin johteiden 22 ja 24 ulommaisia pintoja etsin vaikutusta vastaan. Tällöin saadaan kuvion 8 esittämä kaksi johdekuviokerrosta (johteet 22 ja 24) käsittävä elektroniikkamoduuli, joka sisältää kaksi johteisiin 22 sähköisesti kytkettyä komponenttia 6 ja 16.
- Kuvioiden 6 ja 7 esimerkissä johteet 22 ja 24 kasvatetaan suoraan oikeaan muotoonsa resistikerrokseen 3 tehtyihin aukkoihin. Johteet 22 ja 24 voidaan kuitenkin valmistaa myös toisella tapaa sekä tässä esimerkissä että jäljempänä kuvatuissa esimerkeissä. Yksi vaihtoehtoinen valmistustapa on kasvattaa yhtenäinen kerros johdemateriaalia koko
- 30

- moduuliaihiön pintojen yli ja kuvioida johdekerros myöhemmin litografiamenetelmällä johteiden 22 ja 24 muodostamiseksi. Täsmällisemmin kuvattuna voidaan menetellä esimerkiksi siten, että kuvion 5 välivaiheesta jatketaan kasvattamalla molempien välikerrosten 2 pinnoille kuparia sähkökemiallisella menetelmällä. Tällöin myös kontaktireiät 18 täyttyvät kuparilla. Tämän jälkeen kuparikerrosten päälle levitetään resistikerrokset, kuvioidaan resistit ja etsataan ylimääräiset osat kuparista, välikerroksista 2 ja johdekalvoista 12 ja 14. Tämän jälkeen resistimaski poistetaan. Molemmilla valmistustavoilla päädytään kuvion 8 esittämään rakenteeseen.
- Kuvio 8 voi esittää jo valmista yksikertaista piirimoduulia, mutta valmistusta yleensä jatketaan valmistamalla piirimoduulin pinnoille lisää eriste- ja johdekuviokerroksia, jotka yhdistetään sähköisesti kuvion 8 esittämää rakenteeseen läpivientien avulla. Lisäksi on huomattava, että kuvion 8 moduuliinkin on voitu valmistaa läpivientejä, jotka yhdistävät johteita 22 johteisiin 24. Tällaisia läpivientejä voidaan valmistaa vastaavalla tavalla ja samoissa prosessivaiheissa kuin edellä on kontaktielementtien valmistamisesta esitetty.
- Kuvion 8 moduulia voidaan jatkojalostaa myös kuvion 9 esittämään tapaan siten, että moduulin pinnat suojataan suojakerroksilla 20. Lisäksi kuvion 9 esimerkissä moduuliin on valmistettu ulkoiset kontaktielimet, jotka käsittävät johdekuvioiden 22, 24 päälle valmistetut alustat 21 sekä näiden pinnoille valmistetut kontaktipallot 23.
- Kuviot 10–16 esittävät toisen sovellusmuodon mukaisen valmistusmenetelmän kuvion 5 esittämää välivaihetta vastaavaan vaiheeseen saakka. Kuvion 16 välivaiheesta valmistusta voidaan jatkaa esimerkiksi kuvioiden 6–9 esittämällä tavalla tai sopivasti myös vaihtoehtoisella tavalla, jossa johteiden 22 ja 24 materiaali ensin kasvatetaan kauttaaltaan koko pinnalle ja sen jälkeen kuvioidaan johteiksi 22 ja 24. Kuvioiden 1–5 selostuksen yhteydessä esitetyt tekniset piirteet ja parametrit ovat sovellettavissa myös kuvioiden 10–16 esittämissä prosessivaiheissa, joten valmistusprosessin kaikkia yksityiskohtia ja niiden etuja ei seuraavassa suoritusesimerkissä toisteta turhan toiston välttämiseksi. Sen sijaan seuraavassa tuodaan esille oleelliset eroavaisuuden kuvioiden 1–9 ja kuvioiden 10–16 esittämien sovellusmuotojen välillä.
- Kuvioiden 10–16 sovellusmuodossa valmistus aloitetaan kuvion 1 tapaan johdekalvosta 12, johon tehdään kontaktiaukot 8. Tämän jälkeen johdekalvon 12 pinnalle,

komponentin 6 tulevalle kiinnityskohdalle kiinnitetään korotuspala 15. Korotuspala 15 on soveltuvaa eristemateriaalia, esimerkiksi esikovetettua liimaa tai muuta polymeeriä, jolla on riittävä tarttuvuus johdekalvon 12 pintaan. Korotuspala 15 voi olla myös kovettunutta polymeeriä, jolloin se voidaan kiinnittää johdekalvon 12 pintaan
5 esimerkiksi erillisen liiman avulla.

Korotuspalaa 15 voidaan käyttää monestakin syystä. Yksi korotuspalan käyttötarkoitus on kasvattaa komponentin 6 ja johdekalvon 12 välistä eristepaksuutta. Tarve eristepaksuuden kasvattamiseen voi tulla esimerkiksi piirimoduulin tai komponentin 6 sähköisen toiminnan asettamista vaatimuksista. Tällöin korotuspalan 15 avulla voidaan
10 asettaa komponentin 6 ja johdekalvon 12 välisen eristyksen ominaisuudet halutuksi. Valittavia ominaisuuksia voi olla esimerkiksi haluttu ominaisvastus ja läpilyöntikestävyys, johon voidaan vaikuttaa korotuspalan 15 ja liiman 5 materiaalin valinnalla. Korotuspalaa voidaan käyttää myös komponentin ja johdekalvon 12 välisen oikosulun ehkäisemiseen. Tällainen käyttö tulee kyseeseen erityisesti sellaisissa
15 sovellusmuodoissa, joissa komponentin 6 pinta painautuu hyvin lähelle johdekalvoa, jolloin syntyy riski tahattomien sähköisten kontaktien muodostumisesta komponentin pinnalla olevien johderakenteiden ja johdekalvon välille. Korotuspalaa voidaan käyttää myös kapasitiivisen kytketymisen heikentämiseksi komponentin 6 sisäisten piirielementtien ja komponentin 6 kohdalla kulkevien johteiden 22 välillä.

20 Korotuspalan 15 lisäksi tai sijasta samaan tarkoitukseen voidaan käyttää myös johdekalvon 12 pinnan kauttaaltaan peittävää eristekerrosta 13, jota kuvattiin kuvion 1 yhteydessä.

Kuvioiden 10–16 esimerkissä nystyttömän komponentin 6 yhteydessä käytetään korotuspalaa 15, mutta nystyllisen komponentin 16 kontaktiterminaalit 17 on saatava
25 ulottumaan lähemmäs johdekalvon 12 pintaa, jotta komponentin 16 vastakkaisen pinnan ja johdekalvon 14 välille saadaan varmistettua riittävä eristeväli. Sovellusmuodossa voidaankin piirimoduuliin sijoittaa komponenttikohtaisesti valittuja korotuspaloja 15 piirilevymoduulin sähköisten ja/tai mekaanisten ominaisuuksien optimoimiseksi. Sama piirimoduuli voi siis sisältää myös ominaisuuksiltaan erilaisia korotuspaloja 15 ja näin
30 ollen korotuspaloja 15 on mahdollista käyttää myös sarjatuotannossa eri lähteistä tulevien ja ominaisuuksiltaan toisistaan poikkeavien komponenttien 6, 16 saattamiseksi yhteensopiviksi käytetyn piirilevynvalmistusprosessin kanssa. Yksi esimerkki

optimoitavasta mekaanisesta ominaisuudesta on eristekerroksen 1 (ja samalla koko piirimoduulin) paksuus, jota voidaan pienentää sopivasti valittujen korotuspalojen 15 avulla, mikä voidaan nähdä esimerkiksi kuviosta 12.

Kuvion 11 mukaisesti valmistusta jatketaan levittämällä liimakerrokset 5
 5 komponenttien liitäntäalueille johdekalvon 12 ja korotuspalan 15 pinnoilla. Komponentit 6 ja 16 kohdistetaan kontaktiaukkojen 8 suhteen ja liimataan paikoilleen. Tämän jälkeen kuvion 11 esimerkissä johdekalvon 12 päälle laminoidaan eristekalvot 10, 11 sekä johdekalvo 14. Seuraavaksi johdekalvojen 12 ja 14 pinnoille levitetään valoresistikerrokset 30, jotka kuviodaan siten, että kontaktiaukkojen 8 kohdille syntyy
 10 kontaktiaukkoja 8 suuremmat avaukset tai pinnoitetaan elektroforeettisesti koko johtavan kerroksen päälle. Tätä valoresistikerrosta 30 käytetään rajaamaan myöhemmin ei-selektiivisellä menetelmällä kasvatettavan välikerrosmateriaalin kasvaminen kontaktireikiin ja kontaktiaukkojen 8 välittömään ympäristöön. Tällaista menettelyä on mahdollista käyttää myös edellä esitettyjen esimerkkien yhteydessä eikä se toisaalta ole
 15 välttämätöntä kuvioden 10–16 esimerkissä. Kuvio 12 esittää moduulia näiden vaiheiden jälkeen. Komponentin 6 kontaktiterminaalit 7 ovat nyt sekä korotuspalan 15 että liiman 5 peittämiä. Komponentin 16 kontaktinystyjen 17 pinnoilla ja vastaavissa kontaktiaukoissa 8 on liimaa.

Kuvion 13 esittämässä vaiheessa komponentin 6 kontaktiaukkojen 8 kohdalle valmis-
 20 tetaan kontaktireiät 18. Kontaktireiät avataan korotuspalan 15 ja liimakerroksen 5 läpi aina kontaktiterminaalien 7 kontaktipinnoille saakka. Kuvion sovellusmuodossa kontaktireikien 8 avaaminen toteutetaan laser-ablaatiomenetelmällä käyttämällä CO₂-laseria kuten edellä kuvion 4 yhteydessä on kuvattu. Kuvioden 10–16 sovellusmuodossa on merkittävää se, että toisen komponentin 16 kontaktiterminaalien
 25 17 kohdalle ei avata vielä tässä vaiheessa kontaktireikiä.

Kuvion 14 esittämässä vaiheessa komponentin 6 kontaktireikiin 18 valmistetaan välikerros 2, joka on soveltuvaa johdemateriaalia. Välikerroksen 2 johdemateriaali valitaan komponentin 6 kontaktiterminaalien 7 materiaalin perusteella ja valmistetaan soveltuvalla kemiallisella johdemateriaalin kasvatusmenetelmällä. Kuvion esimerkissä
 30 komponentin kontaktiterminaalien 7 materiaali on alumiini ja välikerroksen 2 materiaali on pääasiassa sinkkiä sisältävä metalliseos. Välikerroksen kasvattamiseen sovelletaan edellä kuvion 5 yhteydessä esitettyjä periaatteita. Kuvion 5 esimerkistä poiketen kuvion

14 tapauksessa on kuitenkin mahdollista menetellä myös siten, että tässä vaiheessa välikerros 2 kasvatetaan selektiivisen menetelmän avulla ainoastaan kontaktiterminaalien 7 pinnalle eli kontaktireikien 18 pohjalle eikä kontaktireikien 18 reunoille. Tällaisessa sovellusmuodossa kontaktireikien 18 reunoille tuleva välikerroksen 2 osa kasvatetaan myöhemmin komponentin 16 kontaktinystyihin 17 liittyvän välikerroksen kasvattamisen yhteydessä. Selektiivistä kasvatusmenetelmää käyttävässä sovellusmuodossa on se etu, että välikerros 2 ei kasva komponentin 16 kontaktinystyt 17 peittävän liimakerroksen päälle.

Valmistusta jatketaan kuvion 15 esittämässä vaiheessa valmistamalla toisen komponentin 16 kontaktiaukkojen 8 kohdalle kontaktireiät 28. Tämän jälkeen kuvion 16 mukaisesti moduuli altistetaan sopivalle kemialliselle johdemateriaalin kasvatusmenetelmälle. Kuvion 15 esimerkissä kasvatusmenetelmä on ei-selektiivinen ja johdemateriaalia kasvaa moduulin kaikille vapaille pinnoille ja näin myös komponentin 6 kontaktireikiin 18 ja komponentin 16 kontaktireikiin 28. Valoresistikerros 30 kuitenkin suojaa moduulin pintoja, joten välikerros 2 kasvaa ainoastaan kontaktireikiin 18 ja 28 sekä näiden ympäristöön. Tämän jälkeen valoresistikerros 30 ja sen pinnalle mahdollisesti kasvanut johdemateriaali poistetaan. Tällainen valoresistikerrosta 30 käyttävä sovellusmuoto voi olla hyödyllinen esimerkiksi silloin, kun valoresistikerroksen aukkoihin kasvatetaan ei-selektiivisellä menetelmällä esimerkiksi nikkeliä tai muuta kuparista poikkeavaa metallia. Tällöin johteet 22 ja 24 voidaan valmistaa pelkästään kuparikerroksista koostuviksi.

Toisissa sovellusmuodoissa on myös mahdollista käyttää sopivasti valittua selektiivistä kasvatusmenetelmää ja kasvattaa johdemateriaalia ainoastaan komponentin 16 kontaktinystyjen 17 pinnoille vastaavasti kuin edellä kuvion 14 yhteydessä selostettiin. Joka tapauksessa tässä vaiheessa kasvatetaan välikerros 2 ainakin komponentin 16 kontaktinystyjen 17 pinnoille ja kontaktireikien 28 sivuseinämien pinnoille ja lisäksi haluttaessa myös komponentin 6 kontaktiterminaleihin 7 liittyvän välikerroksen 2 pinnalle ja/tai komponentin 6 kontaktireikien 18 sivuseinämien pinnoille.

Mikäli kuvioden 10-16 esimerkki toteutettaisiin ilman valoresistin 30 käyttöä, kuvion 16 esimerkissä komponentin 16 kontaktinystyjen 17 pinnan materiaali voisi sopivasti olla myös kupari ja kontaktinystyjen 17 pinnalle kasvatettavan välikerroksen 2 materiaali olisi tällöin sopivasti kemiallisella kasvatusmenetelmällä valmistettu kupari.

Välikerrosten 2 valmistamisen jälkeen tässä sovellusmuodossa valmistamista voidaan jatkaa esimerkiksi kuvioden 6–9 selostuksen yhteydessä kerrottuun tapaan valmistamalla moduulin pinnalle johdekuvioita ja johdeytimet kontaktireikiin 18 ja 28 sijoittuville kontaktielementeille.

- 5 Toinen vaihtoehto on pinnoittaa moduulin molemmille johtaville pinnoille kuparia valoresistikerroksen 30 poistamisen jälkeen. Tämän jälkeen kuparikerrokset voidaan kuvioda johteiksi 22 ja 24, jolloin saadaan kuvion 17 esittämä rakenne, jossa johteet 22 ja 24 muodostuvat kontaktielementtien ympäristössä ensimmäisestä ja toisesta kuparikerroksesta sekä näiden välissä olevasta välikerroksesta 2, joka on esimerkiksi
10 nikkeliä. Muualla johteet 22 ja 24 muodostuvat ensimmäisestä ja toisesta kuparikerroksesta, joiden välillä on analysoitavissa oleva rajapinta. Kuvion 17 rakenteesta valmistusta voidaan haluttaessa jatkaa esimerkiksi jollakin edellisten esimerkkien yhteydessä kuvatulla tavalla.

- Kuviot 18–23 esittävät kolmannen sovellusmuodon mukaisen valmistusmenetelmän,
15 joka on muunnelma kuvioden 10–16 esittämästä sovellusmuodosta. Kuvion 23 välivaiheesta valmistusta voidaan jatkaa esimerkiksi kuvioden 6–9 esittämällä tavalla. Kuvioden 1–5 ja 10–16 selostuksen yhteydessä esitetyt tekniset piirteet ja parametrit ovat siis sovellettavissa myös kuvioden 18–23 esittämissä prosessivaiheissa, joten valmistusprosessin kaikkia yksityiskohtia ja niiden etuja ei seuraavassa suoritus-esimerkissä toisteta turhan toiston välttämiseksi. Sen sijaan seuraavassa tuodaan
20 esille oleelliset eroavaisuuden kuvioden 10–16 ja kuvioden 18–23 esittämien sovellusmuotojen välillä.

- Kuvioden 18–23 sovellusmuodossa valmistus aloitetaan kuvion 10 tapaan johdekalvosta 12, johon tehdään kontaktiaukot 8. Tämän jälkeen johdekalvon 12
25 pinnalle, komponenttien 6 ja 26 tuleville kiinnityskohdille kiinnitetään korotuspalat 15. Komponenttien 6 ja 26 korotuspalat 15 voivat olla keskenään identtisiä tai komponenttikohtaisesti valittuja esimerkiksi siten, että komponentin 6 korotuspala 15 on erilaista materiaalia ja/tai eripaksuinen kuin komponentin 26 korotuspala 15.

- Kuvion 18 mukaisesti valmistusta jatketaan levittämällä liimakerrokset 5
30 komponenttien liitântäalueille ja laminoimalla aihioon eristekalvot 10, 11 ja johdekalvo

14 aivan kuin kuvion 11 yhteydessä on esitetty. Kuvio 19 esittää moduulia näiden vaiheiden jälkeen.

Kuvion 19 esittämässä vaiheessa komponentin 6 kontaktiaukkojen 8 kohdalle valmistetaan kontaktireiät 18 kuvion 13 yhteydessä selostettuun tapaan. Komponentin 26 kontaktiterminaalien 27 kohdalle ei avata vielä tässä vaiheessa kontaktireikiä.

Kuvion 21 esittämä vaihe vastaa täysin kuvion 14 yhteydessä esitettyä menetelmävaihetta. Tässä sovellusmuodossa komponentin 6 kontaktireikiin 18 valmistetaan välikerros 2, joka on kaksikerroksinen. Kuvion esimerkissä komponentin kontaktiterminaalien 7 materiaali on alumiini. Esimerkin kaksikerroksinen välikerros 2 käsittää ensin kasvatetun sinkkiä sisältävän kerroksen ja tämän jälkeen kasvatetun nikkeli-alumiini -kerroksen. Nikkeli-alumiini -kerros kasvatetaan kemiallisella menetelmällä ja sitä käytetään sinkkiä sisältävän kerroksen tiivistämiseen.

Valmistusta jatketaan kuvion 22 esittämässä vaiheessa valmistamalla toisen komponentin 26 kontaktiaukkojen 8 kohdalle kontaktireiät 28. Tämän jälkeen kuvion 23 mukaisesti moduuli altistetaan sopivalle kemialliselle johdemateriaalin kasvatusmenetelmälle. Tämä vaihe vastaa kuvion 16 yhteydessä selostettua menetelmävaihetta. Kuvion 23 esimerkissä komponentin 26 kontaktiterminaalien 27 pinnan materiaali on kupari ja kontaktiterminaalien 27 pinnalle kasvatettavan välikerroksen 2 materiaali on myös kupari.

Kuviossa 24 on puolestaan esitetty kuvioden 18–23 sovellusmuodosta sellainen modifikaatio, jossa kuvion 22 esittämän vaiheen jälkeen komponentin 26 kontaktiterminaalien 27 päälle kasvatetaan ensimmäinen välikerros selektiivisellä kasvatusmenetelmällä ja tämän jälkeen välikerroksen 2 kasvattamista jatketaan ei-selektiivisellä menetelmällä. Kuvion 24 esimerkissä komponentin 26 kontaktiterminaalien 27 pinnan materiaali on kulta ja kontaktiterminaalien 27 pinnalle kasvatettavan välikerroksen 2 materiaali on nikkeli.

Välikerrosten 2 valmistamisen jälkeen näissä kuvioden 18–24 sovellusmuodoissa valmistamista voidaan jatkaa esimerkiksi kuvioden 6–9 selostuksen yhteydessä kerrottuun tapaan valmistamalla moduulin pinnalle johdekuvioita ja johdeytimet kontaktireikiin 18 ja 28 sijoittuville kontaktielementeille.

Kuvio 25 esittää tarkemmin kontaktireiän ja vastaavasti myös tähän aukkoon valmistettavan kontaktielementin muotoa. Kuvion 25 esimerkki esittää yhden mahdollisen muodon, joka voidaan saavuttaa edellä esitettyjä sovellusmuotoja käyttäessä. Muotoon voidaan vaikuttaa johdekalvoon 12 tehtävien kontaktiaukkojen 8
5 muodon, johdekalvon 12 ja komponentin välissä olevan eristeen ominaisuuksien ja CO₂-laserin käyttöparametrien avulla. Kuvion 25 kontaktireikä on pyörähdys-symmetrinen ja kuvion esittämä poikkileikkaus on otettu kontaktireiän keskiakselin kautta eli esittää leveintä mahdollista poikkileikkausta. Kuviossa 25 kontaktireiän kokoa ja muotoa on määritelty seuraavien parametrien avulla:

- 10 – suurin leveys W_{MAX} , josta voidaan laskea kontaktielementin suurin poikkipinta-ala A_{MAX} ,
- kontaktielementin ja komponentin 6 kontaktipinnan 7 välisen kontaktin leveys W_{CONT} , josta voidaan laskea kontaktielementin ja komponentin kontaktipinnan välinen kontaktipinta-ala $A_{CONT 1}$, ja
- 15 – kontaktiaukon leveys W_{HOLE} , josta voidaan laskea kontaktielementin ja johdekuviokerroksen johteen välinen kontaktipinta-ala $A_{CONT 2}$.

Kuviossa on kuvattu myös komponentin kontaktipinnan 7 leveys W_{PAD} , josta voidaan laskea kontaktipinnan pinta-ala A_{PAD} , kun tiedetään kontaktipinnan muoto. Kontaktipinta 7 voi olla esimerkiksi neliön muotoinen ja W_{PAD} :n edustaessa sivun
20 leveyttä kontaktipinnan pinta-alaksi saadaan: $A_{PAD} = W_{PAD} \times W_{PAD}$. Pinta-alat on toki mahdollista määrittää myös pinta-alamittauksen avulla, mikä voikin olla käytännöllisempää ainakin silloin, kun määritettävä pinta-ala on epäsäännöllisen muotoinen.

Kuviossa kontaktipintaa 7 ympäröi komponentin 6 pinnalle valmistettu
25 passivointikerros 9. Tällöin kontaktipinnan pinta-alalla A_{PAD} tarkoitetaan nimenomaan kontaktin muodostamiselle vapaata pinta-alaa eli sen pinnan pinta-ala, joka on paljastettuna passivointikerrokseen 9 tehdyssä avauksessa. Lisäksi kuviossa on esitetty johdekalvon 12 ja kontaktipinnan 7 välimatka H , joka vastaa kontaktireiän syvyyttä ja näin ollen kontaktireikään valmistettavan kontaktielementin korkeutta. Koska
30 kontaktireikä täytetään kokonaan johdemateriaalilla, myös kontaktireiän muut mitat

vastaavat kontaktielementin mittoja ja parametreilla W_{MAX} ja W_{HOLE} voidaan viitata myös kontaktielementin vastaaviin mittoihin.

Seuraavassa esitetään edellä kuvattujen sovellusmuotojen yhteydessä tyypillisiä parametreja:

5 $H = 1\text{--}50\text{ }\mu\text{m}$, tavallisesti $5\text{--}30\text{ }\mu\text{m}$;

$W_{PAD} = 20\text{--}1000\text{ }\mu\text{m}$, tavallisemmin $50\text{--}200\text{ }\mu\text{m}$ ja tavallisimmin noin $100\text{ }\mu\text{m}$; ja

$W_{HOLE} = 5\text{--}500\text{ }\mu\text{m}$, tavallisemmin $20\text{--}75\text{ }\mu\text{m}$ ja tavallisimmin noin $30\text{--}50\text{ }\mu\text{m}$.

Lisäksi yleensä $W_{HOLE} \geq H$, mikä edistää kontaktireiän luotettavaa täyttymistä. Kontaktireikä 18 pyritään valmistamaan siten, että reiän sivuseinämät olisivat pystysuorat. Toisin sanoen tavoitteena on kontaktireikä, jonka leveys ja muoto säilyy vakiona koko johdekalvon 12 ja kontaktipinnan 7 välisen välimatkan H eli kontaktireikä olisi koko tämän matkan kontaktiaukon 8 muotoinen. Myös kontaktipintaa 7 kohti heikosti kapeneva muoto on hyvä. Käytännössä edellä kuvattua laserprosessia käytettäessä kontaktireiästä voi kuitenkin tulla esimerkiksi kontaktipintaa 7 kohti
10 levenevä tai ensin levenevä ja sitten kapeneva siten, että kontaktireikä on leveimmillään jossakin johdekalvon 12 ja kontaktipinnan 7 välillä. Kuvion 25 esittää tällaisen kontaktireiän. Tällainen epäoptimaalinen muoto ei ole ongelmallinen, mikäli vain levenemä ei ole liian suuri ja reiän täyttö onnistuu hyvin.

Edellä viitatuissa leveyksien mitta-arvoista komponentin kontaktipinnan 7 leveys W_{PAD}
20 määrittyy komponentin valinnan kautta. W_{PAD} voidaan tarvittaessa mitata erikseen jokaista sellaista suoraa pitkin, joka kulkee kontaktipinnan 7 keskipisteen kautta. Tätä määritelmää voidaan tarvita edellä viitattuja mitta-arvoja ja niiden suhteita tarkasteltaessa, mikäli kontaktipinnan 7 tai kontaktiaukon 8 muoto on epäsäännöllinen. Tavallisimmassa tapauksessa kontaktipinta on kuitenkin neliömäinen, jolloin
25 kontaktipinnan 7 leveytenä W_{PAD} voidaan yleensä käyttää neliön sivun leveyttä.

Kontaktiaukon 8 leveys W_{HOLE} on parametri, joka valitaan valmistusprosessia suunniteltaessa. Yksi kontaktiaukon 8 leveyttä valittaessa huomioon otettava parametri on käytettävän komponentin kontaktipinnan 7 leveys. Kontaktiaukon 8 leveys valitaan siten, että kontaktiaukon kautta valmistettava kontaktisreikä osuu komponentin päässä
30 koko poikkipinnaltaan komponentin kontaktialueeseen 7 eikä kontaktialueen ohi

esimerkiksi passivointikerroksen pintaan. Mikäli kontaktiaukko on muodoltaan pyöreä, kontaktiaukon leveys W_{HOLE} on ympyrän keskipisteen kautta mitattu halkaisija. Mikäli taas kontaktiaukko on muodoltaan epäsäännöllinen, W_{HOLE} voidaan tarvittaessa mitata erikseen jokaista sellaista suoraa pitkin, joka kulkee kontaktiaukon 8 keskipisteen kautta. Epäsäännöllisen muodon tapauksessa verrattaessa kontaktiaukon leveyttä W_{HOLE} kontaktipinnan leveyteen W_{PAD} , vertailu voidaan tehdä aina erikseen kullekin parille samansuuntaisten suorien kautta mitattuja leveyksiä. Leveyksiä W_{HOLE} ja W_{PAD} voidaan tarvittaessa verrata vastaavalla tavalla myös muihin esitettyihin parametreihin.

Edellä esitettyjä parametrien suhteita voidaan soveltaan myös kontaktinystyjen 17 yhteydessä, jolloin kontaktialueen pinta-ala ja leveys korvataan kontaktinystyn pinta-alalla ja leveydellä ja välimatka H mitataan kontaktinystyn pintaan.

Kontaktireiän muotoon voidaan vaikuttaa laserin parametrien avulla, jotka valitaan reiän parametrien ja poistettavan eristeen ominaisuuksia mukaan. Valmistustulokseen vaikuttaa tietysti myös käytössä oleva laserlaite. Valittujen parametrien sopivuus prosessiin tarkastetaan koevernaisuserän avulla ja tarvittaessa parametreja muutetaan siten, että haluttu tulos saavutetaan.

Yleensä valmistusmenetelmässä on järkevää pyrkiä sellaiseen kontaktireiän muotoon, jossa

$W_{CONT} = 0,5-1,5$ kertaa W_{HOLE} , mielellään $0,7-1,2$ kertaa W_{HOLE} ja mieluiten $0,8-1,0$ kertaa W_{HOLE} , kuitenkin siten, että $W_{CONT} < W_{PAD}$; ja

$W_{MAX} =$ korkeintaan $100\ \mu\text{m}$, mielellään korkeintaan $30\ \mu\text{m}$ ja mieluiten korkeintaan $10\ \mu\text{m}$ suurempi kuin se parametreista W_{HOLE} ja W_{CONT} , joka on suurempi. Suhteellisesti esitettynä tavoitteena olisi, että $W_{MAX} =$ korkeintaan $40\ \%$, mielellään korkeintaan $20\ \%$ ja mieluiten korkeintaan $10\ \%$ suurempi kuin se parametreista W_{HOLE} ja W_{CONT} , joka on suurempi.

Optimaalisimmassa kontaktielementin muodossa W_{MAX} on oleellisesti yhtä suuri kuin W_{HOLE} ja lisäksi W_{CONT} on $0-20\ \%$ pienempi kuin W_{MAX} .

Tyypillisimmissä sovellusmuodoissa kontaktipinta 7 on muodoltaan neliskulmainen ja kontaktiaukko 8 ympyrän muotoinen. Tällöin $A_{CONT\ 1}$ on tyypillisesti $10-75\ \%$ pinta-

alasta A_{PAD} , $A_{CONT\ 1}$ ja $A_{CONT\ 2}$ tyypillisesti keskenään suunnilleen yhtä suuria esimerkiksi tarkkuudella $\pm 20\ %$.

Kuvio 26 esittää esimerkkejä muista mahdollisista kontaktireikien 18 muodoista. Kuvion 27 taas esittää esimerkkejä tällaisiin kontaktireikiin valmistetuista välikerroksista 2. Kuvioiden 26 ja 27 esimerkeissä liitettävä komponentti on nystytön. Kuten kuviosta 27 voi nähdä, välikerrokset 2 eivät ulotu ollenkaan komponentin passivointikerroksen 9 päälle vaan ovat kontaktissa ainoastaan komponentin kontaktipinnan 7 kanssa. Tämän piirteen avulla voidaan nähdä valmiistakin elektroniikkamoduulista se, onko komponentti upotettu elektroniikkamoduuliin nystyllisenä vai nystyttömänä. Nystytysprosesseissa komponentin kontaktipinnalle 7 kasvatettavat nystyt täyttävät aina koko kontaktipinnan 7 ja leviävät aina myös hieman passivointikerroksen 9 päälle. Mikäli taas edellä kuvatuissa suoritus-esimerkeissä käytetään nystytöntä komponenttia, välikerros 2 ja kontaktielementti kasvavat ainoastaan kontaktireikään 18, jolloin valmiissa elektroniikkamoduulissa välikerros 2 ei ulotu komponentin passivointikerroksen 9 päälle ja osa komponentin kontaktipinnasta 7 jää vapaaksi välikerroksesta 2 (kontaktipinnan 7 reunat) aina kun kontaktireiän 18 kohdistus ja valmistus on onnistunut. Myös mahdollisessa kontaktireiän 18 kohdistusvirhetilanteessa, jossa kontaktiaukko 8 ei täysin sijaitse kontaktipinnan 7 kohdalla, ainakin osa kontaktipinnan 7 reuna-alueista ja reuna-aluetta ympäröivästä passivointikerroksesta on vapaa välikerroksesta 2.

Mikäli nystytön komponentti on valmistettu kuparijohteita käyttävällä puolijohdeprosessilla, kontaktialue 7 on kuparia. Tällöin välikerros voidaan valmistaa suoraan kemiallisesti kasvatetusta kuparista, joka muodostaa johdepinnoitteen myös kontaktireiän 18 sivuseinämille. Tämän jälkeen kontaktireiät 18 voidaan täyttää ja johdekerroksen paksuutta kasvattaa sähkökemiallisella kuparinkasvatusmenetelmällä.

Tämän hakemuksen kirjoitushetkellä yleisin puolijohdeprosesseissa käytettävä johdemateriaali on kuitenkin alumiini. Tällöin myös nystyttömien komponenttien yleisin kontaktialueen 7 materiaali on alumiini ja on edullista käyttää eri materiaaleista valmistettuja yksi tai useampikerroksisia välikerroksia alumiinisen kontaktialueen ja elektroniikkamoduulin kuparisten johteiden välissä. Seuraavassa mainitaan muutamia mahdollisia välikerrosten rakenteita:

Välikerrosrakenne 1

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä, joka ei kasva tai kasvaa heikosti polymeeripinnalle. Nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvavamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

10 Välikerrosrakenne 2

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

Välikerrosrakenne 3

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeli-alumiinia, joka ei kasva polymeeripinnalle. Nikkeli-alumiinin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

Välikerrosrakenne 4

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeli-alumiinia. Nikkeli-alumiinin pinnalle kasvatetaan kemiallisella menetelmällä

kerros nikkeliä ja nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia.

Välikerrosrakenne 5

- 5 Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä.

Välikerrosrakenne 6

- 10 Alumiinisen kontaktialueen 7 pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä, joka kasvatettu nikkelikerros yksin muodostaa välikerroksen 2.

Välikerrosrakenne 7

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä ja nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia.

- 15 Edellä esitetyissä välikerrosrakenteiden esimerkeissä sinkkiä sisältävä kerros sisältää esimerkiksi noin 80 % sinkkiä, noin 16 % kuparia, noin 2-3 % nikkeliä ja noin 2-3 % rautaa. Tämä on ainoastaan yksi mahdollinen esimerkki käyttökohteeseen soveltuvista seossuhteista, joten seossuhteita voidaan toki vaihdella sovelluskohteiden mukaan.
- 20 Edellä esitetyissä välikerrosrakenteiden esimerkeissä sinkkiä sisältävän kerroksen paksuus on alle 1 µm, tavallisesti yksikertaisena kerroksena noin 0,1 µm ja useampana kerroksena esimerkiksi noin 0,3–0,4 µm. Ohuimmillaan sinkkiä sisältävä kerros voi olla noin 5–10 nm valmistamisen jälkeen. Kasvatettaessa nikkeliä tai nikkeli-alumiiniä sinkkiä sisältävän kerroksen päälle ainakin osa sinkkiatomeista liukenee ja korvautuu nikkeliatomeilla. Lopullisessa piirimoduulissa voi olla mahdollista, että sinkkiä sisältävä kerros on havaittavissa lähinnä sinkin konsentraatioprofiilina alumiinin ja
- 25 seuraavan kerroksen materiaalin rajapinnassa. Sinkkiä sisältävä kerros ei siis välttämättä ole tarkkarajaisena lopullisessa tuotteessa, koska sinkki voi diffuusoitua viereisiin materiaalikerroksiin erityisesti korkeampia lämpötiloja käyttävissä valmistusprosessin vaiheissa.

- Edullisessa sovellusmuodossa sinkkiä sisältävä kerros kasvatetaan kaksinkertaisella sinkaattiprosessilla. Yksinkertaisella sinkaattiprosessilla kasvatettu sinkki muodostaa epäyhtenäisen ja epätasaisen pinnan alumiinin päälle. Tällaisen pinnan päälle kasvatetun nikkeli-kerroksen adheesio on heikompi ja se soveltuu huonommin käytettäväksi pienillä
- 5 mikrovia-avauksilla. Kasvatetun sinkkipinnan laatua saadaan merkittävästi parannettua käyttämällä kaksinkertaista sinkaattiprosessia. Tyypillisesti tällaisessa prosessissa ensimmäisen sinkattikäsittelyn jälkeen sinkkiä sisältävä kerros stripataan typpihapolla (HNO_3), jonka jälkeen pinnoitetaan toinen sinkkiä sisältävä kerros. Kaksinkertaisella sinkaattiprosessilla saadaan aikaan tiivis ja yhtenäinen sinkkiä sisältävä kerros
- 10 komponentin alumiinisen liitosalueen pinnalle.
- Nikkeli-alumiini kerroksen paksuus voi puolestaan olla esimerkiksi 0,2–2 μm . Nikkelikerroksen paksuus taas voi olla esimerkiksi 0,5–20 μm , tyypillisesti 2–10 μm . Myös kerrospaksuudet ovat ainoastaan esimerkkejä mahdollisista kerrospaksuuksista ja muita kerrospaksuuksia voidaan myös hyvin käyttää.
- 15 Sovellusmuodoissa sähkökemiallisesti kasvatettava kuparikerros voi olla paksuudeltaan esimerkiksi välillä 5–30 μm , tyypillisesti välillä 10–20 μm . Kemiallisella kasvatusmenetelmällä kasvatettava kuparikerros taas yleensä valmistetaan selvästi ohuemmaksi ja sen paksuus on sovellusmuodoissa esimerkiksi välillä 0,1–2 μm , tyypillisesti välillä 200–800 nm.
- 20 Edellä kuvatuissa valmistusmenetelmissä voidaan toki käyttää myös muita kuin edellä mainittuja välikerrosrakenteita ja materiaaleja, esimerkiksi tinaa. Alumiinin pinnalle on myös mahdollista kasvattaa suoraan nikkeli-kerros poistamalla alumiinin pinnalla oleva oksidikerros esimerkiksi alkaalisella etsillä ja huuhtomalla pinta tämän jälkeen esimerkiksi propan-2-olissa ja välittömästi tämän jälkeen pinnoittamalla propan-2-olin
- 25 kiehumispistettä lämpimämmässä kemiallisessa nikkelikylvyssä. Lisäksi sinkkiä sisältävän kerroksen pinnalle olisi mahdollista pinnoittaa myös esimerkiksi kromia ja nikkelin pinnalle kultaa.
- Kuvio 28 esittää vielä yhden mahdollisen kontaktirakenteen, jossa voidaan käyttää komponenttia, jonka kontaktialue on ennalta varustettu alusmetallurgisilla kerroksilla,
- 30 mutta varsinaista nystyä ei ole valmistettu. Kuvio 29 esittää yhden mahdollisen vastaavan kontaktirakenteen toteutettuna nystyttömän komponentin kanssa.

Kuvio 28 esittää komponentin pinnalla olevan passivointikerroksen 9, jossa on avaus komponentin kontaktialueen 7 kohdalla. Passivointikerroksen 9 pinnalla on polymeerikerros 25. Polymeerikerros 25 voi koostua yhdestä tai useammasta polymeerikerroksesta. Polymeerikerroksen 25 materiaali voi sisältää esimerkiksi kuvion 1 yhteydessä kuvattua eristekerrosta 13, kuvion 2 yhteydessä kuvattua liimaa 5 ja/tai kuvion 11 yhteydessä kuvattua korotuspalaa. Komponentin kontaktialueen 7 pinnalle on valmistettu alusmetallurgia, joka tässä esimerkissä käsittää kaksi kerrosta. Ensimmäinen alusmetallurgiakerros 26 on sputtertoimalla valmistettu kerros esimerkiksi kromia (Cr) tai titaani-wolframia (TiW). Toinen alusmetallurgiakerros 27 on sputtertoimalla valmistettu kerros esimerkiksi nikkeliä (Ni), kuparia (Cu) tai kultaa (Au). Varsinainen nysty käsittäisi vielä esimerkiksi kemiallisesti tai sähkökemiallisesti kasvatetun kulta- tai kuparikerroksen toisen alusmetallurgiakerroksen 27 pinnalla.

Kuvion 28 esimerkissä komponentti on kiinnitetty polymeerikerroksen 25 välityksellä johdekalvoon 12, johon on tehty edellä esitetyissä menetelmissä kuvattuun tapaan kontaktiaukot 8. Kontaktiaukkojen 8 kautta on valmistettu kontaktireiät 18 tai 28, joihin kontaktielementti on valmistettu kontaktiin toisen alusmetallurgiakerroksen 27 kanssa. Kontaktielementti on valmistettu siten, että ensin on kasvatettu yhtä tai useampaa kemiallista kasvatusmenetelmää käyttäen välikerros 2 vastaavaan tapaan kuin edellä esitetyissä menetelmissä on kuvattu. Kuvion 28 esimerkissä välikerros 2 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Tämän välikerroksen päälle on kasvatettu kerros 32 kuparia sähkökemiallisella kasvatusmenetelmällä. Sähkökemiallisesti kasvatettu kupari muodostaa myös kontaktielementin johdeytimen 29. Kuviosta 28 nähdään myös se, että johdekalvo 12, välikerros 2 ja kuparikerros 32 muodostavat yhdessä johteen 22 materiaalin. Esimerkissä johdekalvo 12, välikerros 2 ja kuparikerros 32 ovat kaikki kuparia, mutta kerrokset ja niiden väliset rajapinnat on kuitenkin mahdollista havaita myös valmista rakennetta analysoimalla.

Kuvio 29 esittää kuvion 28 tapaan komponentin pinnalla olevan passivointikerroksen 9, jossa on avaus komponentin kontaktialueen 7 kohdalla. Passivointikerroksen 9 pinnalla on polymeerikerros 25, joka vastaan kuvion 28 yhteydessä esitettyä. Kuvion 29 esimerkissä komponentin kontaktialueen 7 pinta on ollut päällysteetön komponentti silloin, kun se on tuotu piirimoduulin valmistusprosessiin. Tällaisessa komponentissa

kontaktialueen 7 ulkopinta eli kontaktipinta on siis tyypillisesti muodostettu jo puolijohdetehtaalla. Kuvion 29 esimerkissä kontaktialueen 7 materiaali on alumiini.

Kuvion 29 esimerkissä komponentti on kiinnitetty polymeerikerroksen 25 välityksellä johdekalvoon 12, johon on tehty edellä esitetyissä menetelmissä kuvattuun tapaan kontaktiaukot 8. Kontaktiaukkojen 8 kautta on valmistettu kontaktireiät 18 tai 28, joihin kontaktielementti on valmistettu kontaktiin kontaktialueen 7 kanssa. Kontaktielementti on valmistettu siten, että ensin on kasvatettu yhtä tai useampaa kemiallista kasvatusmenetelmää käyttäen välikerros 2 vastaavaan tapaan kuin edellä esitetyissä menetelmissä on kuvattu. Kuvion 29 esimerkissä välikerros 2 on valmistettu useammassa osassa ja käsittää useita kerroksia. Kuviossa 28 välikerros on lisäksi selityksen helpottamista varten jaettu kolmeen osaan, pohjaosaan 36, seinämäosaan 37 ja johdeosaan 38. Pohjaosa 36 on se osa, joka kasvaa kontaktiterminaalien 7, 17 pinnalle kontaktireiän 18, 28 pohjalle, seinämäosa 37 on se osa, joka kasvaa kontaktireiän 18, 28 sivuseinämien pinnoille ja johdeosa 38 on se osa, joka kasvaa osaksi valmistettavaa johdetta 22.

Kuvion 29 välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Kuvion 29 esimerkissä johdekalvo 12 on kuparia, joten sinkkaattiprosessia käytettäessä ensimmäinen välikerros 33 kasvaa ainoastaan välikerroksen 2 pohjaosaan 36. Tästä valmistusta voidaan jatkaa esimerkiksi valmistamalla toinen välikerros 34 kemiallisella nikkeli- tai kuparikalvoilla. Nikkeli kasvaa sekä välikerroksen pohjaosaan 36 että johdeosaan 38 ja joillakin kasvatusmenetelmillä myös polymeerin 25 pinnalle seinämäosaan 37. Toisen välikerroksen 34 päälle valmistetaan kolmas välikerros 35 kuparista kemiallisella kasvatusmenetelmällä, jolloin kupari kasvaa pohjaosaan 36, seinämäosaan 37 ja johdeosaan 38. Kolmannen välikerroksen päälle kasvatetaan kerros 32 kuparia sähkökemiallisella kasvatusmenetelmällä, joka muodostaa myös kontaktielementin johdeytimen 29.

Kuvion 29 osalta on huomattava, että kerrokset 33 ja 34 eivät välttämättä ole lopullisessa piirimoduulissa kuvion esittämään tapaan tarkkarajaisia vaan kerrokset voivat ilmetä lomittuneina tai sekoittuneina, esimerkiksi diffuusion vaikutuksesta. Esimerkiksi sinkkiä sisältävän ensimmäisen välikerroksen 33 tapauksessa sinkki voi

sijaita konsentraatioprofiilina alumiinin ja nikkelin 34 välisessä rajapinnassa ja osittain alumiinin 7 ja nikkelikerroksen 34 sisällä.

Kuvion 29 kontaktirakenteessa voidaan käyttää myös muita materiaalikombinaatioita. Esimerkiksi sopivasti valittuja välikerrosrakenteita edellä kuvatuista välikerrosrakenteista 1–7 ja näiden muunnelmia voidaan käyttää kuvion 29 kuvaaman kontaktirakenteen ja myös kuvioden 30–33 kuvaamien kontaktirakenteiden muodostamiseen. Lisäksi kuvion 29 kontaktirakenne on mahdollista valmistaa myös kuvion 28 esittämien materiaalien avulla siten, että ensimmäinen välikerros 33 ja toinen välikerros 34 valmistetaan sputtertoimalla. Tällöin sputteroidut välikerrokset 33 ja 34 kasvavat sekä pohjaosaan 36 että johdeosaan 38 mutta eivät oleellisessa määrin seinämäosaan 37, mikäli kontaktireikä 18, 28 ei ole kontaktiaukkoa 8 kohti levenevä. Yksi mahdollisuus on käyttää sinkkiä sisältävää ensimmäisen välikerrosta 33 ja tämän pinnalla joko suoraan nikkelistä kemiallisella kasvatusmenetelmällä valmistettua kolmatta välikerrosta 35 tai rakennetta, jossa kerrosten 33 ja 35 välissä käytetään nikkeli-alumiinista valmistettua toista välikerrosta 34. Tällaisessa sovellusmuodossa ei tarvita lainkaan kemiallista kuparinkasvatusta, sillä nikkeli muodostaa pystysuuntaisen kontaktin kontaktireiän sivuseiniä pitkin.

Kuvio 30 esittää vielä yhden kontaktielementtirakenteen. Kuvion 30 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on nikkeli-alumiinia ja kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Kuvion 30 rakenteessa siis kontaktireikä täytetään nikkelillä eli kontaktielementin johdeydin 29 on nikkeliä. Muutoin kuvion 30 rakenteen osalta pätevät kuvioden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

Kuvio 31 esittää vielä yhden kontaktielementtirakenteen. Kuvion 31 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33 ja toisen välikerroksen 34. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai vaihtoehtoisesti selektiivisellä kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Vaihtoehtoisesti kuvion 31 rakenne voidaan valmistaa myös siten, että ensimmäinen ja toinen välikerros 33 ja 34

korvataan yhdellä kerroksella kemiallisesti kasvatettua nikkeliä. Johdeydin 29 on tyypillisesti kuparia ja johde 22 käsittää ensimmäisen ja toisen kuparikerroksen 12 ja 32. Muutoin kuvion 31 rakenteen osalta pätevät kuvioiden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

- 5 Kuvio 32 esittää vielä yhden kontaktielementtirakenteen. Kuvion 32 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Esimerkin
10 menetelmässä kasvatusmenetelmä on selektiivinen siten, että nikkeli kasvaa ainoastaan johtavan materiaalin päälle. Kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Vaihtoehtoisesti kuvion 32 rakenne voidaan valmistaa myös siten, että ensimmäinen välikerros 33 jätetään pois. Johdeydin 29 on tyypillisesti kuparia. Muutoin kuvion 32 rakenteen osalta pätevät kuvioiden 28 ja 29
15 yhteydessä esitetyt tekniset piirteet.

- Kuvio 33 esittää vielä yhden kontaktielementtirakenteen. Kuvion 33 rakenteen valmistamiseen voidaan käyttää esimerkiksi kuvioiden 10–17 yhteydessä kuvattua menetelmää, jossa käytettiin valoresistikerrosta 30. Kuvion 33 rakenteessa välikerros 2
20 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Esimerkin menetelmässä kasvatusmenetelmä on selektiivinen siten, että nikkeli kasvaa ainoastaan johtavan materiaalin päälle. Kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Vaihtoehtoisesti kuvion 33 rakenne voidaan valmistaa myös siten, että ensimmäinen välikerros 33 jätetään pois. Johdeydin 29 on tyypillisesti kuparia. Muutoin kuvion 33 rakenteen osalta pätevät kuvioiden 28 ja 29
25 yhteydessä esitetyt tekniset piirteet.

- Sovellusmuodoissa on siis tuotu esiin menetelmä piirimoduulin valmistamiseksi, jossa
30 menetelmässä

– otetaan johdekalvo 12,

- otetaan komponentti 6, joka käsittää kontaktialueita 7, joiden materiaali sisältää ensimmäistä metallia,
- kiinnitetään komponentti 6 johdekalvoon 12 polymeerikerroksen 25 välityksellä,
- valmistetaan johdekalvoon 12 kiinnitetyn komponentin 6 ympärille eristekerros 1,
- 5 – valmistetaan polymeerikerrokseen 25 kontaktialueiden 7 kohdille kontaktireiät 18, 28 siten, että kunkin kontaktireiän 18, 28 ja vastaavan kontaktialueen 7 välinen kontaktipinta-ala A_{CONT1} on pienempi kuin kontaktialueen 7 pinta-ala A_{PAD} , ja
- kasvatetaan ainakin kontaktirei'issä 18, 28 olevien kontaktialueiden 7 pinnalle välikerros 2, joka sisältää ainakin kolmatta metallia,
- 10 – kasvatetaan kerros 32 toista metallia, joka kerros 32 on kontaktissa välikerroksen 2 pinnan kanssa ja ulottuu pitkin valmistettavia johteita 22, ja
- muodostetaan johteet 22 kuvioimalla johdekalvo 12, ja mikäli tarpeen myös johdekalvon 12 pinnalla oleva välikerros 2 ja/tai toista metallia oleva kerros 32.

15 Tyypillisessä sovellusmuodossa kontaktiaukot 8 valmistetaan johdekalvoon 12 ennen komponentin 6 kiinnittämistä, jolloin komponentti 6 siis kiinnitetään kontaktiaukoilla varustettuun 8 johdekalvoon 12. Tavallisimmassa tällaisessa sovellusmuodossa kontaktiaukot eivät ulotu kontaktialueiden 7 pinnoille saakka, joten komponentin 6 kiinnittämisen jälkeen vielä avataan kontaktireiät 18, 28 kontaktiaukkojen 8 kautta.

20 Yhdessä sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on sinkki. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää sinkin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Toisessa sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

25 Kolmannessa sovellusmuodossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Tavallisimmassa sovellusmuodossa kontaktialueiden 7 materiaali on pääasiallisesti alumiinia ja johteiden materiaali on kuparia ja näiden välillä on jokin edellä esitetyistä välikerrosrakenteista 1–7.

5 Välikerrosrakenteen valmistamisessa käytetään tyypillisesti ainakin yhtä kemiallista kasvatusmenetelmää.

Sovellusmuodot kuvaavat piirimoduulin, joka käsittää

- eristekerroksen 1,
- eristekerroksen 1 sisällä ainakin yhden komponentin 6, joka käsittää kontaktialueita 7, joiden materiaali sisältää ensimmäistä metallia,
- 10 – eristekerroksen 1 pinnalla johteita 22, jotka käsittävät ainakin ensimmäisen kerroksen 12 ja toisen kerroksen 32 siten, että ainakin toinen kerros 32 sisältää toista metallia, ja
- kontaktielementtejä kontaktialueiden 7 ja johteiden 22 välillä sähköisten kontaktien muodostamista varten, jotka kontaktielementit käsittävät kontaktialueen 7
- 15 materiaalin pinnalla välikerroksen 2, joka sisältää kolmatta metallia,
- jossa ensimmäinen, toinen ja kolmas metalli ovat eri metalleja, ja
- välikerroksen 2 ja kontaktialueen 7 välinen kontaktipinta-ala $A_{CONT\ 1}$ on pienempi kuin kontaktialueen 7 pinta-ala A_{PAD} .

20 Yhdessä sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on sinkki. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää sinkin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Toisessa sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

25 Kolmannessa sovellusmuodossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Tavallisimmassa sovellusmuodossa kontaktialueiden 7 materiaali on pääasiallisesti alumiinia ja johteiden materiaali on kuparia ja näiden välillä on jokin edellä esitetyistä välikerrosrakenteista 1–7.

5 Tyypillisessä sovellusmuodossa kontaktielementit käsittävät sähkökemiallisella kasvatusmenetelmällä valmistetun kupariytimen 29, joka sivuseinämien ja komponentin 6 suunnassa rajautuu välikerrokseen 2 ja johteen 22 suunnassa yhdistyy jatkuvasti eli ilman rajapintaa johteen 22 toisen kerroksen 32 materiaaliin. Toisin sanoen kontaktielementin kupariydin 29 ja johteen 22 toisen kerroksen 32 materiaali on valmistettu samassa prosessissa, jolloin osat liittyvät kiinteästi yhteen eikä niiden välillä
10 ole rajapintaa. Johteen ensimmäisen kerroksen 12 ja toisen kerroksen 32 välillä taas on tyypillisesti rajapinta tai vastaava siirrosalue, joka voidaan havaita esimerkiksi metallin kiderakennetta tai epäpuhtauskonsentraatiota analysoimalla.

Yhdessä sovellusmuodossa kontaktielementin ja komponentin kontaktialueen 7 välisen kontaktipinnan leveys W_{CONT} on 0–20 % pienempi kuin kontaktielementin suurin leveys
15 W_{MAX} samassa suunnassa.

Kontaktielementit täyttävät tavallisesti kokonaan kontaktireiät 18, 28 eli kontaktielementit eivät ole onttoja vaan ovat kokonaan johdemateriaalia.

Tavallisesti sovellusmuodoissa pyritään siihen, että kontaktielementin korkeus H on pienempi tai yhtä suuri kuin kontaktielementin suurin leveys W_{MAX} .

20 Piirimoduulilla on myös sovellusmuotoja, joissa eristekerros 1 sisältää ainakin yhden kerroksen kuitumateriaalia 19, jossa kuitumateriaalissa 19 on aukko komponenttia 6 varten, sekä yhtenäisen polymeerikerroksen, joka on kiinnittynyt kuitumateriaaliin 19 ja komponentteihin 6, 16.

Edellä esitetyjä valmistusmenetelmiä ja niiden osaprosesseja voidaan modifioida
25 monin tavoin. Esimerkiksi edellä kuvattu varsinaisen liiman käyttö komponentin kiinnittämisessä johdekalvoon 12 voidaan korvata muulla adheesiomekanismeilla. Yhtenä esimerkkinä mainittakoon adheesio-ominaisuuden omaavan eristekerroksen 13 käyttö johdekalvon 12 pinnalla (vrt. kuvio 1 ja vastaava selitys). Tällöin komponentit 6 painetaan suoraan eristekerrosta 13 vasten siten, että komponentin kiinnittyvät
30 vastaavalla tavalla riittävästi paikoilleen kuin liimaa käyttävän sovellusmuodon

yhteydessä kuvataan. Tällainen eristekerros 13 voi sisältää esimerkiksi teippimäisen pinnoitteen tai koostua ainakin pintaosaltaan muovautuvasta polymeerista tai vastaavasta materiaalista.

Menetelmä voidaan toteuttaa myös ilman liiman 5 tai adheesio-ominaisuuden käyttöä.

- 5 Tällöin komponentit 6 voidaan kiinnittää paikoilleen esimerkiksi mekaanisesti tai alipaineen avulla. Tällöin alipainetta tai vastaavaa väliaikaista kiinnitystä voidaan ylläpitää kunnes komponentti 6 on riittävästi kiinnittynyt paikoilleen eristemateriaalin 1 avulla.

- 10 Liitettävä komponentti 6 voi olla esimerkiksi integroitu piiri, kuten muistisiru, prosessori tai ASIC. Liitettävä komponentti voi olla myös esimerkiksi MEMS, LED tai passiivikomponentti. Liitettävä komponentti voi olla koteloitu tai koteloimaton ja sen kontaktiterminaalit voivat koostua kontaktialueista 7, kontaktinystyistä 17 tai vastaavista. Komponentin kontaktialueiden pinnalla voi olla myös varsinaista kontaktinystyä ohuempi johdepinnoite.

- 15 Myös eristekerroksen 1 materiaali voidaan valita edellä kuvatuista esimerkeistä poikkeavasti. Eristekerros 1 voidaan valmistaa soveltuvasta polymeeristä tai polymeeriä sisältävästä materiaalista. Eristekerroksen 1 valmistusmateriaali voi olla esimerkiksi nestemäisessä tai esikövetetussa muodossa (kuten prepreg). Eristekerroksen 1 valmistamisessa voidaan käyttää esimerkiksi lasikuituvahvistettua epoksilevyä, kuten
20 FR4- tai FR5-tyyppistä levyä. Muita esimerkkejä materiaaleista, joita voidaan käyttää eristekerroksen 1 valmistamisessa ovat PI (polyimidi), aramidi, polytetrafluorieteeni ja Teflon®. Kertamuovien sijasta tai ohella eristekerroksen 1 valmistamisessa voidaan käyttää hyväksi myös kestopuoveja, esimerkiksi jotakin soveltuvaa LCP-materiaalia (liquid crystal polymer).

- 25 Lisäksi alan ammattilaiselle on selvää, että edellä kuvattuja keksinnön piirteitä voidaan käyttää osana suurempaa kokonaisuutta, esimerkiksi siten, että elektroniikkamoduuli valmistetaan osittain tunnetun tekniikan mukaisia menetelmiä käyttäen ja osittain tässä kuvatus keksinnön sovellusmuotoja käyttäen. Edellä esitettyjen elektroniikkamoduulirakenteiden pinnalle tai pinnoille on myös mahdollista valmistaa lisää piirilevykerroksia
30 tai myös liittää komponentteja esimerkiksi pintaliitostekniikalla.

Alan ammattilainen ymmärtää myös sen, että kun tässä dokumentissa viitataan tiettyyn materiaaliin, esimerkiksi alumiinina, nikkelinä tai kuparina, viittauksella tarkoitetaan materiaalia, joka käyttökohteen kannalta on oleellisesti mainittua materiaalia. Viitattu materiaali voi siis mainitun pääasiallisen ainesosansa lisäksi sisältää käyttökohteen kannalta epäoleellisia määriä epäpuhtauksia ja muita ainesosia. Esimerkiksi alumiininen kontaktialue on tavallisesti materiaalia, joka sisältää tyypillisesti vähintään 95 % alumiinia.

Kun taas viitataan materiaalin sisältävän jotakin tiettyä ainesosaa, tällä tarkoitetaan sitä, että materiaali sisältää mainittua ainesosaa käyttökohteen kannalta oleellisen suuren pitoisuuden. Lisäksi materiaali voi sisältää oleellisia tai epäoleellisia määriä muita ainesosia. Esimerkiksi sinkkiä sisältävä kerros sisältää siis sellaisen määrän sinkkiä, jotta tällä on merkitystä alumiinin ja seuraavan metallin välisen kontaktin ominaisuuksien kannalta.

Edellä esitetyt esimerkit kuvaavat joitakin mahdollisia menetelmiä ja rakenteita, joiden avulla keksintöämme voidaan käyttää hyväksi. Keksintöämme ei kuitenkaan rajoitu vain edellä esitettyihin esimerkkeihin ja sovellusmuotoihin, vaan keksintö kattaa lukuisia muitakin menetelmiä ja rakenteita, patenttivaatimusten täydessä laajuudessa ja ekvivalenssitulkinta huomioon ottaen.

Patenttivaatimukset:

1. Menetelmä piirimoduulin valmistamiseksi, jossa menetelmässä

otetaan johdekalvo (12),

5 valmistetaan johdekalvoon (12) kontaktiaukot (8) kontaktielementtien valmistamista varten,

otetaan komponentti (6), joka käsittää kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia,

kiinnitetään komponentti (6) johdekalvoon (12) polymeerikerroksen (25) välityksellä,

10 valmistetaan johdekalvoon (12) kiinnitetyn komponentin (6) ympärille eristekerros (1),

valmistetaan polymeerikerrokseen (25) kontaktialueiden (7) kohdille kontaktireiät (18, 28) siten, että kunkin kontaktireiän (18, 28) ja vastaavan kontaktialueen (7) välinen kontaktipinta-ala ($A_{CONT\ i}$) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}), ja

15 kasvatetaan ainakin kontaktirei'issä (18, 28) olevien kontaktialueiden (7) pinnalle välikerros (2), joka sisältää ainakin kolmatta metallia,

kasvatetaan kerros (32) toista metallia, joka kerros (32) on kontaktissa välikerroksen (2) pinnan kanssa ja ulottuu pitkin valmistettavia johteita (22), ja

20 muodostetaan johteet (22) kuvioimalla johdekalvo (12), ja mikäli tarpeen myös johdekalvon (12) pinnalla oleva välikerros (2) ja/tai toista metallia oleva kerros (32).

2. Patenttivaatimuksen 1 mukainen menetelmä, jossa

kontaktiaukot (8) valmistetaan ennen komponentin (6) kiinnittämistä,

komponentti (6) kiinnitetään kontaktiaukoilla varustettuun (8) johdekalvoon (12), ja

25 komponentin (6) kiinnittämisen jälkeen avataan kontaktireiät (18, 28) kontaktiaukkojen (8) kautta.

3. Patenttivaatimuksen 2 mukainen menetelmä, jossa kontaktireiät (18, 28) avataan kontaktiaukkojen (8) kautta CO₂-laserilla, jolloin johdekalvoa (12) käytetään maskina.
4. Jonkin patenttivaatimuksen 1–3 mukainen menetelmä, jossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli sisältää ainakin yhden metalleista sinkki ja nikkeli.
5. Jonkin patenttivaatimuksen 1–3 mukainen menetelmä, jossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli.
6. Jonkin patenttivaatimuksen 1–4 mukainen menetelmä, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33), joka valmistetaan kaksinkertaisella sinkkaattiprosessilla.
10. Jonkin patenttivaatimuksen 1–6 mukainen menetelmä, jossa välikerros (2) käsittää nikkeliä sisältävän kerroksen (34), joka valmistetaan kemiallisella nikkelinkasvatusmenetelmällä.
8. Jonkin patenttivaatimuksen 1–7 mukainen menetelmä, jossa välikerros (2) käsittää kuparia sisältävän kerroksen (35), joka valmistetaan kemiallisella kuparinkasvatusmenetelmällä.
15. Jonkin patenttivaatimuksen 1–8 mukainen menetelmä, jossa eristekerros (1) valmistetaan siten, että

otetaan ainakin yksi kuitumateriaalia (19) ja esikövetettua polymeeriä sisältävä eristekalvo (11),

valmistetaan kuhunkin kuitumateriaalia (19) sisältävään eristekalvoon (11) reikäkomponenttia (6) varten, ja

laminoidaan eristekalvo (11) tai eristekalvot (11) yhteen johdekalvon (12) ja siihen liittyvien rakenteiden kanssa.
25. Jonkin patenttivaatimuksen 1–9 mukainen menetelmä, jossa johdekalvon (12) pinta, jolle komponentti (6) kiinnitetään, käsittää yhtenäisen eristekerroksen (13).
11. Jonkin patenttivaatimuksen 1–10 mukainen menetelmä, jossa komponentin (6) ja johdekalvon (12) väliin sijoitetaan korotuspala (15).

12. Jonkin patenttivaatimuksen 1–11 mukainen menetelmä, jossa piirimoduuliin sijoitetaan komponentin (6) lisäksi ainakin yksi toinen komponentti (16) siten, että ensimmäisen ja toisen komponentin kiinnitystavat eroavat toisistaan polymeerikerrosten (25) ainakin yhden ominaisuuden osalta.
- 5 13. Jonkin patenttivaatimuksen 1–12 mukainen menetelmä, jossa kiinnitettävä komponentti (6) on nystytön komponentti.
14. Piirimoduuli, joka käsittää
- eristekerroksen (1),
- eristekerroksen (1) sisällä ainakin yhden komponentin (6), joka käsittää
- 10 kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia,
- eristekerroksen (1) pinnalla johteita (22), jotka käsittävät ainakin ensimmäisen kerroksen (12) ja toisen kerroksen (32) siten, että ainakin toinen kerros (32) sisältää toista metallia, ja
- kontaktielementtejä kontaktialueiden (7) ja johteiden (22) välillä sähköisten
- 15 kontaktien muodostamista varten, jotka kontaktielementit käsittävät kontaktialueen (7) materiaalin pinnalla välikerroksen (2), joka sisältää kolmatta metallia,
- jossa ensimmäinen, toinen ja kolmas metalli ovat eri metalleja, ja
- välikerroksen (2) ja kontaktialueen (7) välinen kontaktipinta-ala ($A_{CONT\ 1}$) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}).
- 20 15. Patenttivaatimuksen 14 mukainen piirimoduuli, jossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on ainakin yksi metalleista sinkki ja nikkeli.
16. Patenttivaatimuksen 14 mukainen piirimoduuli, jossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli.
- 25 17. Patenttivaatimuksen 14 tai 15 mukainen piirimoduuli, jossa kontaktialueiden (7) materiaali on pääasiallisesti alumiinia.

18. Patenttivaatimuksen 14, 15 tai 17 mukainen piirimoduuli, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33).
19. Patenttivaatimuksen 18 mukainen piirimoduuli, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33) lisäksi ainakin yhden toisen välimetallikerroksen (34, 35).
- 5 20. Patenttivaatimuksen 19 mukainen piirimoduuli, jossa ainakin yksi toinen välimetallikerros (35) on kemiallisella kasvatusmenetelmällä kasvatettua kuparia.
21. Patenttivaatimuksen 20 mukainen piirimoduuli, jossa välimetallikerros (2) käsittää sinkkiä sisältävän kerroksen (33) ja kuparikerroksen (35) välissä ainakin yhden kerroksen (34) nikkeliä ja/tai nikkelin ja alumiinin seosta.
- 10 22. Jonkin patenttivaatimuksen 18–21 mukainen piirimoduuli, jossa sinkkiä sisältävä kerros sisältää sinkkiä, kuparia, nikkeliä ja rautaa.
23. Jonkin patenttivaatimuksen 14–22 mukainen piirimoduuli, jossa osa välikerroksesta (2) ulottuu kontaktielementtien sivuseinämiä pitkin kontaktialueiden (7) ja johteiden (22) välillä.
- 15 24. Patenttivaatimuksen 23 mukainen piirimoduuli, jossa kontaktielementit käsittävät sähkökemiallisella kasvatusmenetelmällä valmistetun kupariytimen (29), joka sivuseinämien ja komponentin (6) suunnassa rajautuu välikerrokseen (2) ja johteen (22) suunnassa yhdistyy jatkuvasti eli ilman rajapintaa johteen (22) toisen kerroksen (32) materiaaliin.
- 20 25. Patenttivaatimuksen 23 tai 24 mukainen piirimoduuli, jossa välikerroksen (2) kontaktielementtien sivuseinämiä pitkin ulottuva osa (37) sisältää kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä.
- 25 26. Jonkin patenttivaatimuksen 14–25 mukainen piirimoduuli, jossa johteet (32) käsittävät
- eristekerroksen (1) pinnalla ensimmäisen kerroksen (12) kuparia, ja
- ensimmäisen kuparikerroksen pinnalla toisen kerroksen (32) kuparia.

27. Jonkin patenttivaatimuksen 14–25 mukainen piirimoduuli, jossa johteet (32) käsittävät

eristekerroksen (1) pinnalla ensimmäisen kerroksen (12) kuparia,

ensimmäisen kuparikerroksen pinnalla välikerroksen (2), ja

5 välikerroksen pinnalla toisen kerroksen (32) kuparia.

28. Patenttivaatimuksen 27 mukainen piirimoduuli, jossa ensimmäisen ja toisen kuparikerroksen välissä oleva välikerroksen (2) osa käsittää kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä.

10 29. Jonkin patenttivaatimuksen 14–28 mukainen piirimoduuli, jossa kontaktielementin ja komponentin kontaktialueen (7) välisen kontaktipinnan leveys (W_{CONT}) on 0–20 % pienempi kuin kontaktielementin suurin leveys (W_{MAX}) samassa suunnassa.

30. Jonkin patenttivaatimuksen 14–29 mukainen piirimoduuli, jossa kontaktielementin korkeus (H) on pienempi tai yhtä suuri kuin kontaktielementin suurin leveys (W_{MAX}).

15 31. Jonkin patenttivaatimuksen 14–30 mukainen piirimoduuli, jossa eristekerros (1) sisältää ainakin yhden kerroksen kuitumateriaalia (19), jossa kuitumateriaalissa (19) on aukko komponenttia (6) varten, sekä yhtenäisen polymeerikerroksen, joka on kiinnittynyt kuitumateriaaliin (19) ja komponenttiin (6).

20 32. Jonkin patenttivaatimuksen 14–31 mukainen piirimoduuli, joka käsittää johteiden (22) ja komponentin (6) välissä polymeerikerroksen (25), jossa on kontaktireiät (18, 28) kontaktielementtejä varten, ja jossa kontaktielementit täyttävät kokonaan kontaktireiät (18, 28).

25 33. Patenttivaatimuksen 32 mukainen piirimoduuli, jossa johteiden (22) ja komponentin (6) välissä oleva polymeerikerros (25) käsittää ensimmäisen (15) ja toisen polymeerikerroksen (5), jossa ensimmäinen polymeerikerros (15) on ensimmäistä polymeeriä ja toinen polymeerikerros (5) on kovettunutta liimaa.

34. Patenttivaatimuksen 33 mukainen piirimoduuli, jossa ensimmäinen polymeerikerros (15) ja toinen polymeerikerros (5) ovat paikallisia siten, että ne ovat läsnä ainoastaan oleellisesti komponentin (6) kohdalla.

- 5 35. Jonkin patenttivaatimuksen 14–34 mukainen piirimoduuli, jossa komponentti käsittää passivointikerroksen (9) komponentin pinnalla ja kontaktialueet (7) sijaitsevat passivointikerroksessa (9) olevien avausten sisällä, jolloin välikerros (2) ulottuu passivointikerroksessa (9) olevan avauksen läpi.

(57) Tiivistelmä:

Valmistusmenetelmä ja piirimoduuli, joka käsittää eristekerroksen (1) ja eristekerroksen (1) sisällä ainakin yhden komponentin (6), joka käsittää kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia. Eristekerroksen (1) pinnalla on johteita (22), jotka käsittävät ainakin ensimmäisen kerroksen (12) ja toisen kerroksen (32) siten, että ainakin toinen kerros (32) sisältää toista metallia. Piirimoduuli käsittää kontaktielementtejä kontaktialueiden (7) ja johteiden (22) välillä sähköisten kontaktien muodostamista varten. Kontaktielementit puolestaan käsittävät kontaktialueen (7) materiaalin pinnalla välikerroksen (2), joka sisältää kolmatta metallia siten, että ensimmäinen, toinen ja kolmas metalli ovat eri metalleja ja välikerroksen (2) ja kontaktialueen (7) välinen kontaktipinta-ala (A_{CONT}) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}).

(Fig. 8)

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
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First Named Inventor/Applicant Name:		Petteri Palm		
Filer:		Joshua Paul Wert		
Attorney Docket Number:		IMB 22 US		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
National Stage Fee	1631	1	330	330
Natl Stage Search Fee - Report provided	1642	1	430	430
National Stage Exam - all other cases	1633	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1615	15	52	780
Miscellaneous-Filing:				
Petition:				

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Patent-Appeals-and-Interference:				
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Extension-of-Time:				
Miscellaneous:				
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EFS ID:	8756748
Application Number:	12990785
International Application Number:	PCT/FI09/50383
Confirmation Number:	3345
Title of Invention:	Circuit Module and Method of Manufacturing the same
First Named Inventor/Applicant Name:	Petteri Palm
Customer Number:	95002
Filer:	Joshua Paul Wert
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Foreign Reference	EP0380289B1.pdf	478604 e449c84c72a858c94b1b6aa0a1596acf52d8cf3	no	11
Warnings:					
Information:					
2	Foreign Reference	EP1259103.pdf	1011918 bcd7a2a7a01dde30d40f959cbcf1a7e68d1e79e	no	50
Warnings:					
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3	Drawings-only black and white line drawings	IMB22_figs.pdf	93026 dad66c2ad5169abfd72f354ced87d5cc3d92e61	no	15
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4		IMB22Eng.pdf	181030 e1ca0ea4e42d6c8ec5fe01aaac194ca0d5d259c1	yes	50
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	Document Description		Start	End	
	Specification		1	42	
	Claims		43	49	
	Abstract		50	50	
Warnings:					
Information:					
5	Information Disclosure Statement (IDS) Filed (SB/08)	IMB22US_IDS.pdf	269476 d7f777b00669c6ca63d7a4bf529965d4902d3191	no	2
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6		IMB22US_POA_DEC.PDF	194982 910ed67841779b2da68260d0d571d97c55598f6	yes	5
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	Oath or Declaration filed		4	5
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7	Preliminary Amendment	IMB22US_Preliminary_amendment.pdf	96837 b7b1942ea0abf59c8e8b76d0352a96f70013dbfd	no 9
Warnings:				
Information:				
8	Transmittal of New Application	IMB22US_pto-1390.pdf	4879429 9e8b88ab0879d042c796d559852bc74a11d12ee6	no 4
Warnings:				
Information:				
9	Application Data Sheet	IMB22US_sb0014_ADS.pdf	1104823 5896a284c216fe36cb961430313c209d831ab7d5	no 5
Warnings:				
Information:				
10	Foreign Reference	WO09138560.pdf	2684322 3eb8190ba2cc590a72ca9b19f53983caba2285ae	no 68
Warnings:				
Information:				
11	Foreign Reference	WO2006056643.pdf	1077417 ac13cdb6111a3ad5e26e83fd72d3de8af140c8da	no 24
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Information:				
12	Documents submitted with 371 Applications	IMB22_as_filed.PDF	354102 10500253e562ce228a95b301cd3b0dbdca d7cd71	no 43
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13	Fee Worksheet (PTO-875)	fee-info.pdf	36369 f128cd0f5366436b95166f8a4f1cd70c6c89c24	no 2
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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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(54) **A process of manufacturing a multi-layer ceramic substrate assembly**

Verfahren zum Herstellen eines keramischen Mehrschichtsubstrates

Procédé de fabrication d'un substrat céramique multicouche

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EP-A- 0 166 401 EP-A- 0 198 354
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- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 20, no. 10, March 1978, page 3856, New York, US; J. GOW, III et al.: "Modified Cr dam for MC metallurgy"**
- **PATENT ABSTRACTS OF JAPAN, vol. 12, no. 340 (E-659)[3195], 19 September 1988; & JP-A-63 107 056**

EP 0 380 289 B1

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

The present invention relates to a process of manufacturing a multi-layer ceramic substrate assembly.

A multi-layer ceramic substrate assembly provided with pins to enable it to be used as a connector is known. The pins are mounted on pads on a surface of the substrate, the pad for the pins being connected to via-pads electrically connected to (via-conductors) in the substrate. Additional pads are connected to the pads for pins, for later modifications of the circuit. Such a multi-layer ceramic substrate assembly is illustrated in Figs. 1-3. In these figures, 1 denotes a ceramic substrate body having via-conductors 2 and interconnecting lines 3, 4 denotes a via upper pad, 5 an upper insulating layer of polyimide, 6 a pin soldered to the via upper pad 4, and 7 a via lower pad. More specifically, the via upper pad 4 comprises a via pad 11, an I/O (in/out) pin pad 12, a modification pad 13, and connecting patterns 14 and 15.

The modification pads 13 are used when the circuit of the substrate is to be changed from the original circuit, by wiring between the modification pads 13 with a discrete wire, and if necessary, disconnecting the I/O pin pad 12 from the via upper pad 13. The wiring to the modification pad 13 is made by soldering a wire to the pad 13. To prevent a flow of a solder from the modification pad 13 to the I/O pin pad 12 during the reflow of the solder, a solder dam 16 is provided between the modification pad 13 and the I/O pad 12, the solder dam 16 being made of a resin such as polyimide (Fig. 3). The solder dam 16 mechanically prevents a flow of the solder 17, but cannot prevent a diffusion of the solder 17 under the resin solder dam 16, i.e., along the surface of the underlying gold plating layer 18, which is a common material used for the pads 11, 12 and 13 as well as the connecting patterns 14 and 15, because the gold plating layer is very easily wetted by the solder. If the solder flows from the modification pad 13 onto the I/O pin pad 12, the solder fixing the I/O pins is damaged and the fixing of the I/O pins is adversely affected, making the connector difficult to use. This adverse affect on the fixing of the pins must be prevented.

The object of the present invention is to devise a process forming an assembly with a solder dam which ensures a prevention of a flow of a solder between pads.

IBM Technical Disclosure Bulletin, Vol. 20, No. 10, March 1978, page 3856 discloses a modified dam for metallised ceramic metallurgy in which a solder dam of chromium oxide is formed on a copper layer.

In accordance with the present invention, there is provided a process of manufacturing a multi-layer ceramic substrate assembly, the method comprising the steps of: preparing a multi-layer ceramic substrate; forming a pattern of nickel on a surface of the substrate, the pattern including first, second and third portions, the first and second portions being connected by the third portion in the pattern, the first portion of the pattern be-

ing electrically connected with a conductor in the multi-layer ceramic substrate, and the nickel being wettable with a solder; forming a first soldering pad of a second electric conductor metal on the first portion of the pattern; forming a second soldering pad of a third electric conductor metal on the second portion of the pattern, wherein the second and third conductor metals are chosen from the group consisting of gold and alloys thereof; entirely covering the resulting pattern with titanium; selectively heat treating the titanium and the nickel at the third portion of the pattern at such a temperature that the titanium reacts with the nickel to form a titanium-nickel intermetallic compound on the top surface of the nickel connection conductor but no reaction occurs between the titanium and the soldering pads; and selectively etching the titanium remaining at least on the first and second portions, without etching the titanium-nickel alloy, to remove the titanium remaining at least on the first and second portions; wherein the first and second soldering pads are wettable with a solder and the titanium-nickel alloy is not wettable with a solder.

In a preferred embodiment, a pin is fixed on the first portion of the above pattern with a solder having a relatively high melting point. The second portion of the pattern is used for modification of the circuit in the multi-layer ceramic substrate assembly.

Also, in a preferred embodiment, the pattern of the first electric conductor metal is made of a combination of a copper lower layer and a nickel top layer formed on the copper lower layer, the first and second soldering pads are made of gold.

In a further preferred embodiment, a first solder having a first melting point is used for the first soldering pad to which a pin is fixed by the first solder, and a second solder having a second melting point lower than the first melting point is used for the second soldering pad.

The typical electric conductor for the connecting pattern includes copper, silver, gold, nickel, etc., and these metals, alloys or compounds may be used in combination, for example, in the form of a laminate.

The characteristic feature of the present invention is the formation of a solder dam made of a titanium nickel alloy not wettable with a solder, in combination with the connecting pattern made of an electric conductor metal.

An example of a multi-layer ceramic substrate assembly manufactured by a process according to the invention and a known example as well as some comparative examples are illustrated in the accompanying drawings, in which:-

Figures 1-3 illustrate a typical multi-layer ceramic substrate assembly, in which Fig. 3 shows a prior art assembly portion;

Figs. 4 and 5 are cross-sectional views of an upper via pad of a multi-layer ceramic substrate assembly manufactured by a process according to the present invention after and during manufacture respectively; and,

Figs. 6-11 are photographs of the upper via pad having various solder dams, after a heat treatment.

Figure 2 is a plan view of an upper via pad of a multi-layer ceramic substrate assembly, on which an I/O pin is to be fixed. This upper via pad includes a via pad 31, an I/O pin pad 32, a modification pad 33, a connecting pattern 34 between the via pad 31 and the I/O pin pad 32, and a connecting pattern 35 between the I/O pin pad 32 and modification pad 33. The via pad 31 is electrically connected to a via-conductor in the multi-ceramic substrate.

Figure 4 is a sectional view of the upper via pad of Fig. 2 along the line 4A-4A cutting the I/O pin pad 32, the modification pad 33 and the connecting pattern 35. The not shown section of the upper pad cutting from the via pad 31 to the connecting pattern 34 to the I/O pin pad 33 is basically similar to Fig. 5, although the via pad 31 is connected to a via-conductor in the substrates as shown in Fig. 1. In Fig. 4, 32 and 33 denote the I/O pin pad 32 and the modification pad 33 made of a gold, respectively, 36 denotes a solder dam made of a titanium-nickel intermetallic compound, 37 a top conductor layer made of nickel, 38 a body conductor layer made of copper, 39 an insulating layer made of polyimide, and 40 a multi-layer ceramic layer.

In Figs. 2 and 4, the I/O pin and modification pads 32 and 33 of gold are a good electric conductor and easily wettable with a solder, and the solder dam 36 of titanium-nickel is not wettable with a solder. The conductor layers 37 and 38 of nickel and copper are a good electric conductor. The nickel conductor layer 37 is inserted as a barrier between the copper conductor layer 38 and the gold pads 32 and 33, and although still a good conductor is inferior to copper in the electric conductivity thereof. The nickel layer 37 is wettable with a solder, and therefore, requires a good solder dam. In the prior art, an organic layer of polyimide is used as the solder dam, but the solder flows along the interface between the polyimide and the nickel layer because the solder has a good wettability with the nickel. To avoid this flow of a solder under the polyimide, a metal not wettable with a solder was proposed for use as a connecting pattern, per se, with an organic solder dam thereon, but this disadvantageously lowered the electric conductivity of the connecting pattern between the pads. In contrast, by the process according to the present invention, a nickel alloy such as a titanium-nickel intermetallic compound is formed as a solder dam on a connecting pattern of a good electric conductor metal such as copper or nickel, and the adhesion of the nickel alloy solder dam to the metal connecting pattern is strong enough to prevent a flow of a solder therebetween.

In the process the above upper via pad is manufactured as follows. Figure 5 shows a step of manufacturing the upper via pad of Figs. 2 and 4. A multi-layer ceramic substrate 40 (e.g., thickness 12 mm) is prepared in a conventional way. After the polyimide insulating layer 39

(e.g., thickness 20 μ m) is formed on the multi-layer ceramic substrate 40, the copper body conductor layer 38 (e.g., thickness 4 μ m) and the top conductor layer 37 (e.g., thickness 2 μ m) are formed in the form of an upper via pad including the three pads 31-33 and the two connecting patterns 34-35, by sputtering. Then three gold pads 31-33 (e.g., thickness 0.5 - 1 μ m) are formed on the nickel top conductor layer 37 (the plan view shown in Fig. 2) by plating and selectively etching the gold plating layer on the connecting patterns 34 and 35.

Then a titanium layer 41 (e.g., thickness 100 nm) is deposited entirely over the gold pads 31-33, the nickel connecting patterns 34-35, and the polyimide layer 39. This is followed by a heat treatment at 500°C for 60-90 minutes, by which the gold pads 31-33 are not changed and the nickel top conductor layer 37 at the connecting patterns 33-34 selectively reacts with the titanium to form a titanium-nickel intermetallic compound, Ti₂-Ni₃. This titanium-nickel intermetallic compound forms a solder dam 36 covering the nickel top conductor layer 37 at the connecting patterns 33-34.

Then the ceramic substrate is immersed in a hydrogen fluoride solvent (about 1% conc.). During this immersion, the titanium-nickel intermetallic compound on the connecting patterns 33-34 is not dissolved but remains, and the titanium layer 41 over the pads 31-33 and the polyimide layer 39 is selectively dissolved. Thereafter, the upper via pad as shown in Fig. 4 is obtained. As mentioned before, the gold pads 31-33 are wettable with a solder but the titanium-nickel intermetallic compound connecting patterns 33-34 are not wettable with a solder, and thus form or function as a solder dam. Accordingly, a solder dam is easily formed on the connecting patterns.

Moreover, this process of forming the solder dam does not require a photolithography step, because the solder dam of the titanium-nickel intermetallic compound is selectively formed at the connecting patterns by the heat treatment, and the titanium-nickel intermetallic compound acts as a mask in the following etching step, and therefore, the process is simple. In contrast, in the prior art, the formation of a solder dam of a polyimide requires such a photolithography step.

After formation of the upper via pads, as above, I/O pins 42 are soldered to the I/O pin pads 32 with a solder 43 having a relatively high melting point, such as gold-tin (about 350°C). Then, a solder 44 having a relatively low melting point such as tin (about 250°C) is bonded on the modification pad 33 for later use. The soldering is carried out by preliminary bonding the solders 43 and 44 to the pads, setting and fixing the I/O pins 42 to the I/O pin pads, and carrying out a reflow heat treatment in an oven (at about 350°C), whereby a multi-layer ceramic substrate assembly or connector is produced.

When the original circuit of the assembly is to be changed, discrete wires are used to connect between desired I/O pins and/or via conductors, and the discon-

nection of the I/O pins from via conductors is made by cutting the connecting pattern between the I/O pin pad and the via pad, usually by a laser. The wires are bonded to desired modification pads with the solder. This soldering can be conducted at a relatively low temperature (about 250°C) at which the solder fixing the I/O pins to the I/O pin pads 32 is not damaged, because the solder fixing the I/O pins has a relatively high melting point (about 350°C). Note, during this heat treatment for soldering the wire to the modification pad, the solder cannot flow to the I/O pin pad 32 because of the presence of the solder dam 36.

EXAMPLES

Solder dams were formed from various materials, and the flow of the solder through the solder dam was examined. Figures 6-11 show the results after a heat treatment at 350°C for 3 minutes. The photographs were taken at a magnification of 50. In Figs. 6-8, the upper pad is an I/O pin pad, the lower left pad is a via pad, the lower right pad is a modification pad, and the connecting patterns can be seen between the pads. Figures 9-11 are symmetrical to Figs. 6-8 at the left and right sides thereof.

Figure 6 shows the results obtained with a solder dam formed of the titanium-nickel intermetallic compound made as described above; the results are good in that no solder flows onto or through the solder dam.

Figures 7 to 11 illustrate comparative examples.

Figure 7 shows the results obtained with a solder dam of sputtered chromium. The results are good in that no solder flows onto or through the solder dam.

Figure 8 shows the results obtained with a solder dam of sputtered chromium with a coat of polyimide thereon. The results are good in that no solder flows onto or through the solder dams.

Figure 9 shows the results obtained with a solder dam of plated gold. The results are not good in that solder flows onto and through the connecting patterns: The black at the connecting patterns indicates the flowed solder; the partially seen white is due to light reflection when taking the photo.

Figure 10 shows the results obtained with a solder dam of polyimide over plated gold connecting patterns. The results are not good in that solder flows partially under the left hand solder dam and onto the right hand solder dam; the right hand connecting pattern having a dark color in comparison with the whiteness of Figs. 6-8, indicating a flow of solder in the lower layer.

Figure 11 shows the results obtained with a solder dam of sputtered nickel. The results are not good in that solder flows into and through the right hand solder dam, and a similar solder flow will occur at the left hand solder dam.

Claims

1. A process of manufacturing a multi-layer ceramic substrate assembly, the method comprising the steps of: preparing a multi-layer ceramic substrate (1); forming a pattern (37) of nickel on a surface of the substrate, the pattern including first, second and third portions, the first and second portions being connected by the third portion in the pattern, the first portion of the pattern being electrically connected with a conductor (2) in the multi-layer ceramic substrate, and the nickel being wettable with a solder; forming a first soldering pad (32) of a second electric conductor metal on the first portion of the pattern; forming a second soldering pad (33) of a third electric conductor metal on the second portion of the pattern, wherein the second and third conductor metals are chosen from the group consisting of gold and alloys thereof; entirely covering the resulting pattern with titanium (41); selectively heat treating the titanium (41) and the nickel at the third portion of the pattern at such a temperature that the titanium reacts with the nickel to form a titanium-nickel intermetallic compound on the top surface of the nickel connection conductor but no reaction occurs between the titanium and the soldering pads; and selectively etching the titanium (41) remaining at least on the first and second portions, without etching the titanium-nickel alloy, to remove the titanium remaining at least on the first and second portions; wherein the first and second soldering pads are wettable with a solder and the titanium-nickel alloy (36) is not wettable with a solder.
2. A process according to claim 1, further comprising the step of bonding a first solder (43) having a first melting point on the first soldering pad (32) and a second solder (44) having a second melting point lower than the first melting point on the second soldering pad (33).
3. A process according to claim 2, wherein the first solder (43) is gold-tin and the second solder (44) is tin.
4. A process according to claim 2 or claim 3, further comprising the step of soldering a pin (42) to the first soldering pad (32) by the first solder (43).
5. A process according to any of claims 1 to 4, further comprising the step of forming a body conductor copper layer (38) on the multi-layer ceramic substrate, followed by forming the pattern of the first electric conductor metal as a nickel pattern (37) on the body conductor copper layer.
6. A process according to any of claims 1 to 5, further comprising a preliminary step of forming an insulating layer of polyimide (39) on the surface of the mul-

ti-layer ceramic substrate.

Patentansprüche

1. Herstellungsverfahren eines Vielschicht-Keramik-substrataufbaus mit den Schritten: Präparieren eines Vielschicht-Keramiksubstrats (1); Bilden eines Musters (37) aus Nickel auf einer Fläche des Substrats, wobei das Muster erste, zweite und dritte Abschnitte aufweist, von denen der erste und zweite Abschnitt durch den dritten Abschnitt im Muster verbunden sind und der erste Abschnitt des Musters elektrisch mit einem Leiter (2) im Vielschicht-Keramiksubstrat verbunden ist und das Nickel mit einem Lot benetzbar ist; Bilden eines ersten Lötstützpunkts (32) eines zweiten elektrischen Leitermetalls auf dem ersten Abschnitt des Musters; Bilden eines zweiten Lötstützpunkts (33) eines dritten elektrischen Leitermetalls auf dem zweiten Abschnitt des Musters, wobei das zweite und dritte Leitermetall aus der Gruppe Gold und seine Legierungen ausgewählt sind; vollständiges Überdecken des resultierenden Musters mit Titan (41); selektives Wärmebehandeln des Titans (41) und des Nickels im dritten Abschnitt des Musters bei einer Temperatur, so daß das Titan mit dem Nickel reagiert und eine TitanNickel-intermetallische Bindung an der Oberfläche des Verbindungsleiters aus Nickel bildet, aber keine Reaktion zwischen dem Titan und den Lötstützpunkten stattfindet; sowie selektives Ätzen des auf mindestens dem ersten und zweiten Abschnitt verbleibenden Titans (41), ohne die Titan-Nickel-Legierung zu ätzen, um das mindestens auf dem ersten und zweiten Abschnitt verbleibende Titan zu entfernen; wobei die ersten und zweiten Lötstützpunkte mit einem Lot benetzbar sind und die Titan-Nickel-Legierung (36) nicht mit einem Lot benetzbar ist.
2. Verfahren nach Anspruch 1, zusätzlich mit dem Schritt, ein erstes Lot (43) mit einem ersten Schmelzpunkt auf dem ersten Lötstützpunkt (32) anzubringen und ein zweites Lot (44) mit einem zweiten Schmelzpunkt, der niedriger als der erste Schmelzpunkt ist, auf dem zweiten Lötstützpunkt (33).
3. Verfahren nach Anspruch 2, wobei das erste Lot (43) Gold-Zinn ist und das zweite Lot (44) Zinn ist.
4. Verfahren nach Anspruch 2 oder 3, zusätzlich mit dem Schritt, einen Stift (42) an den ersten Lötstützpunkt (32) mittels des ersten Lots (43) zu löten.
5. Verfahren nach einem der Ansprüche 1 bis 4, zusätzlich mit dem Schritt, eine Körperlechterschicht (38) aus Kupfer auf dem Vielschicht-Keramiksub-

strat zu bilden, gefolgt vom Bilden des Musters des ersten elektrischen Leitermetalls als Muster (37) aus Nickel auf der Körperlechterschicht aus Kupfer.

6. Verfahren nach einem der Ansprüche 1 bis 5, zusätzlich mit einem vorangehenden Schritt, eine Isolierschicht aus Polyimid (39) auf der Fläche des Vielschicht-Keramiksubstrats zu bilden.

Revendications

1. Procédé de fabrication d'un substrat céramique à couches multiples, procédé comportant les étapes consistant à :
préparer un substrat céramique à couches multiples (1); former un motif (37) de nickel sur une surface du substrat, le motif comprenant des première, seconde et troisième parties, les première et seconde parties étant reliées par la troisième partie dans le motif, la première partie du motif étant reliée électriquement par un conducteur (2) dans le substrat céramique à couches multiples, et le nickel pouvant être mouillé par une soudure; former un premier plot de soudage (32) d'un second métal électriquement conducteur sur la première partie du motif; former un second plot de soudage (33) en un troisième métal électriquement conducteur sur la seconde partie du motif, dans lequel les second et troisième métaux conducteurs sont choisis parmi le groupe constitué par l'or et ses alliages; recouvrir entièrement le motif résultant de titane (41); traiter thermiquement sélectivement le titane (41) et le nickel dans la troisième partie du motif à une température telle que le titane réagit avec le nickel pour former un composé intermétallique titane-nickel sur la surface supérieure du conducteur de liaison en nickel, mais qu'aucune réaction n'apparaisse entre le titane et les plots de soudage; et graver sélectivement le titane (41) demeurant au moins sur les première et seconde parties, sans graver l'alliage de titane-nickel, pour éliminer le titane subsistant au moins sur les première et seconde parties; dans lequel les premier et second plots de soudage peuvent être mouillés par une soudure et l'alliage de titane-nickel (36) n'est pas mouillable avec une soudure.
2. Procédé selon la revendication 1, comportant en outre l'étape de liaison d'une première soudure (43) ayant un premier point de fusion sur le premier plot de soudage (32) et d'une seconde soudure (44) ayant un second point de fusion inférieur au premier point de fusion sur le second plot de soudage (33).
3. Procédé selon la revendication 2, dans lequel la première soudure (43) est de l'or-étain et la seconde soudure (44) est de l'étain.

4. Procédé selon la revendication 2 ou la revendication 3, comportant en outre l'étape de soudage d'une broche (42) au premier plot de soudage (32) par la première soudure (43).

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5. Procédé selon l'une quelconque des revendications 1 à 4, comportant en outre l'étape de formation d'un corps conducteur sous forme de feuille de cuivre (38) sur le substrat céramique à couches multiples, suivie de la formation du motif du premier métal conducteur électriquement en tant que motif de nickel (37) sur le corps conducteur sous forme de feuille de cuivre.

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6. Procédé selon l'une quelconque des revendications 1 à 5, comportant en outre une étape préliminaire de formation d'une couche isolante de polyimide (39) sur la surface du substrat céramique à couches multiples.

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Fig. 1

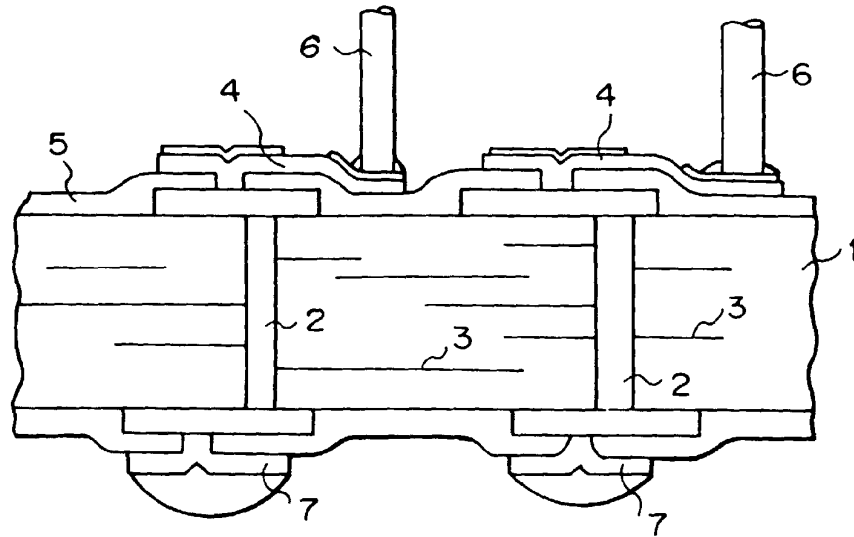


Fig. 2

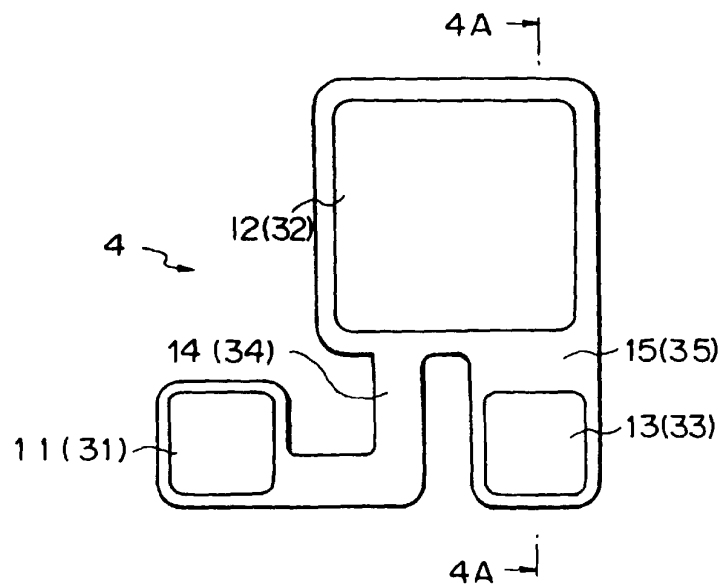


Fig. 3

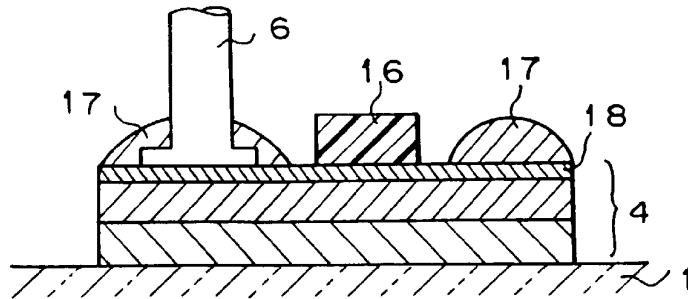


Fig. 4

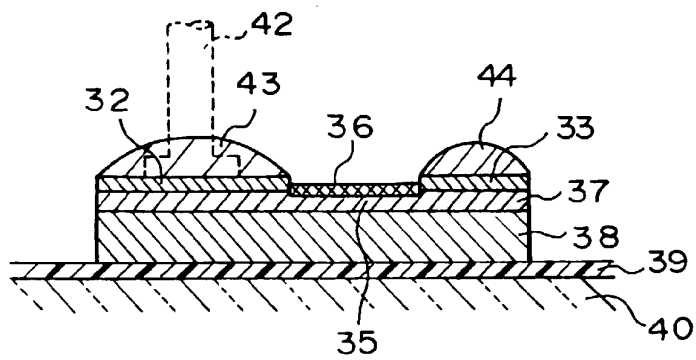


Fig. 5

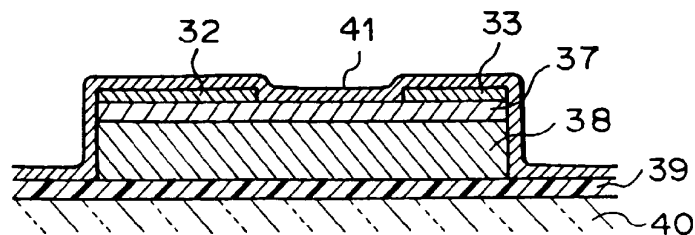


Fig. 6

TI-NI
(GOOD)

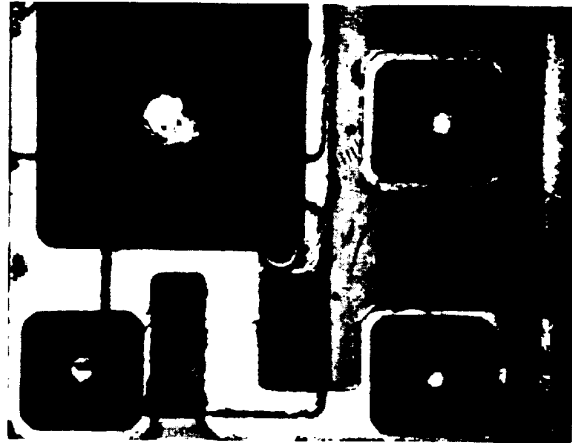


Fig. 7

SPUTTERED
CR
(GOOD)

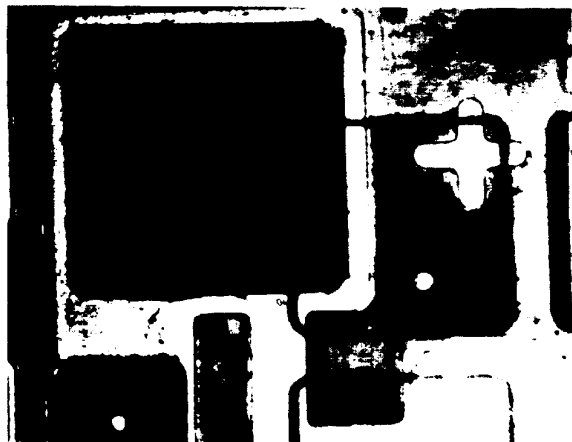


Fig. 8

SPATTERED
CR
+
POLYIMIDE
(GOOD)

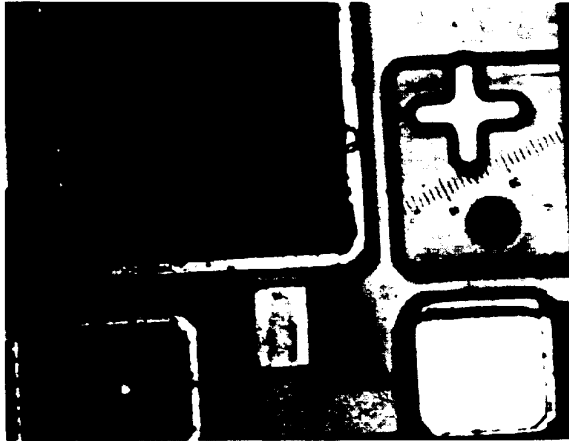


Fig. 9

AU ONLY
(NO GOOD)



Fig.10

AU
+
POLYIMIDE
(NO GOOD)

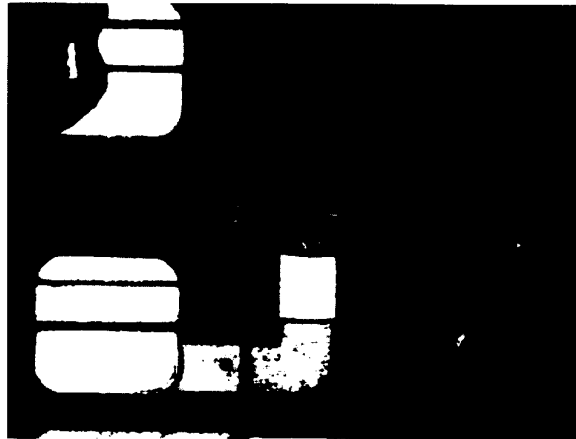


Fig.11

SPUTTERED NI
(NO GOOD)





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(54) **MULTILAYER PRINTED WIRING BOARD AND METHOD FOR PRODUCING MULTILAYER
PRINTED WIRING BOARD**

MEHRSCHICHTIGE LEITERPLATTE UND VERFAHREN ZU IHRER HERSTELLUNG

CARTE A CIRCUITS IMPRIMES MULTICOUCHE ET PROCEDE DE PRODUCTION D'UNE CARTE
A CIRCUITS IMPRIMES MULTICOUCHE

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US-A- 5 386 623 **US-A- 6 110 806**

• **GDULA M ET AL: "A HIGH-SPEED, HIGH-DENSITY MULTIPROCESSING MODULE MADE WITH THE GENERAL ELECTRIC HIGH-DENSITY INTERCONNECT TECHNOLOGY" DIGITAL SIGNAL PROCESSING, ACADEMIC PRESS, ORLANDO, FL, US, vol. 2, no. 4, 1 October 1992 (1992-10-01), pages 247-251, XP000393639 ISSN: 1051-2004**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

Technical Field of the Invention

5 **[0001]** The present invention relates to a buildup multilayer printed circuit board and particularly relates to a multilayer printed circuit board including electronic components such as an IC chip and a multilayer printed circuit board manufacturing method.

Background of the Invention

10 **[0002]** An IC chip is electrically connected to a printed circuit board by a mounting method such as a wire bonding method, a TAB method or a flip-chip method.

[0003] In the wire bonding method, an IC chip is die-bonded to a printed circuit board by adhesive or the like, the pads of the printed circuit board are connected to the pads of the IC chip by wires such as metallic wires and then a sealing resin such as a thermosetting resin or a thermoplastic resin is applied to protect the IC chip and the wire.

15 **[0004]** In the TAB method, wires referred to as leads are connected in the block by a solder or the like and then the bumps of an IC chip and the pads of a printed circuit board are sealed by a resin.

[0005] In the flip-chip method, the pads of an IC chip are connected to the pads of a printed circuit board by through bumps and the gaps between the bumps and the respective pads are filled with a resin.

20 **[0006]** In each of these mounting methods, however, the IC chip and the printed circuit board are electrically connected to each other through lead members (wires, leads or bumps) for connection therebetween. These lead members tend to be cut off and eroded, making the connection of the printed circuit board to the IC chip cut off or causing malfunctions.

[0007] In addition, in each of these mounting methods, a sealing thermoplastic resin such as an epoxy resin is employed to protect the IC chip. However, if bubbles are contained at the time of filling the resin, then the lead members are broken, the IC pads are eroded and reliability of the IC chip is deteriorated due to the bubbles. To seal the IC chip or the like by a thermoplastic resin, it is required to create resin filling plungers and metallic molds in accordance with the respective components of the printed circuit board. Further, in case of employing a thermosetting resin, it is necessary to select a thermosetting resin in view of the materials of the lead members, a solder resist and the like, thereby disadvantageously causing cost increase.

30 **[0008]** Publication GDULA M ET AL: "A HIGH-SPEED, HIGH-DENSITY MULTIPROCESSING MODULE MADE WITH THE GENERAL ELECTRIC HIGH-DENSITY INTERCONNECT TECHNOLOGY" DIGITAL SIGNAL PROCESSING, ACADEMIC PRESS, ORLANDO, FL, US, vol. 2, no. 4, 1 October 1992 (1992-10-01), pages 247-251, discloses a method of manufacturing a multilayer printed circuit board comprising an embedded electronic component.

[0009] The present invention has been made to solve the above-stated problems. It is an object of the present invention to propose a multilayer printed circuit board capable of being directly, electrically connected to an IC chip without using a leadmember and a manufacturing method of the multilayer printed circuit board.

35 **[0010]** After being devoted to the intensive studies of the multilayer wiring board, the inventors of the present invention finally devised a structure capable of electrically connecting a multilayer printed circuit board to an IC chip without using leads and a sealing resin by providing opening portions, through holes and counterbore portions in the resin insulating substrate to thereby contain an electronic component such as an IC chip therein in advance, building up a plurality of interlayer insulating layers, providing via holes on the die pads of the IC chip by photoetching or laser, forming conductor circuits serving as conductive layers, and further providing the interlayer insulating layers and the conductive layers repeatedly to thereby provide the multilayer printed circuit board.

45 **[0011]** Moreover, the inventors of the present invention devised a structure of mounting an electronic component, such as an IC chip, on the surface layer of the multilayer printed circuit board by providing opening portions, through holes and counterbore portions in the resin insulating substrate to thereby contain an electronic component, such as an IC chip, therein in advance, building up interlayer insulating layers, providing via holes on the die pads of the IC chip by photoetching or laser, then forming conductor circuits serving as conductive layers and further providing the interlayer insulating layers and the conductive layers repeatedly. With this structure, it is possible to electrically connect the multilayer printed circuit board to the IC chip in without using leads. It is also possible to mount the electronic components such as the IC chip having different functions and to obtain a multilayer printed circuit board having a greater function. To be specific, a cache memory is embedded as the IC chip included in the board and an IC chip having an operation function is mounted on the front surface of the multilayer printed circuit board, whereby it is possible to arrange the IC chip and the cache memory in proximity while separately manufacturing the cache memory having low yield and the IC chip.

50 **[0012]** Furthermore, after being devoted to the intensive studies, the inventors of the present invention devised providing opening portions, through holes and counterbore portions in resin insulating substrate to thereby contain an electronic component such as an IC chip in advance and forming a transition layer consisting of at least two-layer structure on the die pad of the IC chip. An interlayer insulating layer is provided on the transition layer and a via hole is

provided on a via hole which is the transition layer of the IC chip by photo-etching or laser and a conductor circuit serving as a conductive layer. Thereafter, interlayer insulating layers and conductive layers are repeatedly built up and a multilayer printed circuit board is provided, thereby making it possible to electrically connect the multilayer printed circuit board to the IC chip without using a sealing resin and leads. Further, since the transition layer is formed on the IC chip portion, the IC chip portion is flattened. Accordingly, the upper interlayer insulating layer is flattened and the thickness thereof becomes uniform. Further, the transition layer makes it possible to maintain the stability of a shape in case of forming the via hole on the upper layer.

[0013] The reasons for providing the transition layer on the pad of the IC chip are as follows. First, if the die pad becomes fine pitch and small in size, alignment at the time of forming via holes becomes difficult. Due to this, by providing a transition layer, the alignment is facilitated. If the transition layer is provided, buildup layers can be stably formed even while a die pad pitch is 150 μm or less and a pad size is 20 μm or less. If the via hole is formed in the interlayer insulating layer with the die pad on which the transition layer is not formed and the diameter of the via is larger than the diameter of the die pad, then a polyimide layer serving as the protective layer of the surface of the die pad is dissolved and damaged at the time of removing the residue on the bottom of the via and roughening the surface of the interlayer resin insulating layer. On the other hand, if laser is applied and the via diameter is larger than the diameter of the die pad, a polyimide layer (or protective layer of the IC) is damaged by the laser. Moreover, if the die pad of the IC chip is very small and the diameter of the via is larger than the size of the die pad, then positioning becomes quite difficult even by photo-etching or laser and connection errors occur between the die pad and the via hole.

[0014] By providing the transition layer on the die pad, by contrast, it is possible to ensure connecting the via on the die pad even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less, thereby improving the connection between the pad and the via and reliability. In addition, by interposing the transition layer having a larger diameter on the pad of the IC chip, the fear that the protective film of die pad and the IC are dissolved and damaged if the protective film is immersed in an acid or an etching solution in later steps such as a de-smear and plating steps or conducting various annealing steps, is eliminated.

[0015] The multilayer printed circuit board itself fulfils the functions. In some cases, BGA, solder bumps or PGA (conductive connection pins) may be provided to connect to a mother board or a daughter board which is an external board so as to function as a package substrate for a semiconductor device. With this constitution, wiring length and loop inductance can be reduced compared with a case of connecting the multilayer wiring board to the external board by a conventional mounting method.

[0016] Now, the transition layer defined in the present invention will be described.

[0017] The transition layer means a mediate layer provided on an intermediate portion so as to directly connect the IC chip, which is a semiconductor element, to the printed circuit board without using a conventional IC chip mounting technique. The transition layer is characterized by being formed out of two or more metallic layers or by being made larger than the die pad of the IC chip which is the semiconductor element. The transition layer thus characterized enables the enhancement of electrical connection and positioning characteristics and via hole processing by means of laser or photo-etching without damaging the die pad. This can ensure embedding and containing the IC chip in the printed circuit board, and connecting the IC chip to the printed circuit board. This also enables a metallic layer serving as the conductive layer of the printed circuit board to be directly formed on the transition layer. For example, the conductive layer is the via hole of the interlayer resin insulating layer or a through hole on the substrate.

[0018] As a resin substrate for including electronic components such as the IC chip therein used in the present invention, a substrate obtained by building up prepregs impregnated with a resin or a glass epoxy resin obtained by impregnating an epoxy resin, a BT resin, a phenol resin or the like with a reinforcement or a core material such as a glass epoxy resin. An ordinary resin substrate used for the printed circuit board may be used. Alternatively, a double-sided copper-clad laminate, a one-sided plate, a resin plate without a metallic film or a resin film may be used. However, if the resin is heated at 350 °C or higher, the resin is dissolved and carbonated. Further, ceramic cannot be used for the substrate since it is inferior in outside workability.

[0019] The IC chip is coupled to a resin insulating substrate such as a core substrate in which a cavity formed as a counterbore, a through hole or an opening for containing an electronic component such as the IC chip, by an adhesive or the like.

[0020] The entire surface of the core substrate including the IC chip is subjected to deposition, sputtering or the like, thereby forming a conductive metallic film (or first thin film layer) on the entire surface. The metal used may be tin, chromium, titanium, nickel, zinc, cobalt, gold, copper or the like. The thickness of the conductive metallic film is preferably between 0.001 and 2.0 μm . If the thickness is smaller than 0.001 μm , the conductive metallic film cannot be provided uniformly on the entire surface. It is difficult to form a conductive metallic film having a thickness exceeding 2.0 μm and even if formed, the film does not improve advantages. The thickness is more preferably between 0.01 and 1.0 μm . If chromium is used, the thickness is preferably 0.1 μm .

[0021] The first thin film layer covers the die pad, thereby making it possible to improve the adhesiveness of the transition layer and the IC chip to an interface with the die pad. Further, by covering the die pad with such a metal, it is

possible to prevent the entry of moisture into the interface, to prevent the dissolution and erosion of the die pad and to improve reliability. In addition, the first thin film layer allows the connection between the multilayer printed circuit board and the IC chip by a mounting method without using leads. If using chromium, nickel or titanium, it is possible to prevent the entry of moisture into the interface and excellent metal adhesiveness is ensured. The thickness of chromium, titanium or the like is set so that the sputtered layer does not crack and that adhesiveness between the metal and the upper layer is ensured. With a reference to a positioning mark on the IC chip, a positioning mark is formed on the core substrate.

[0022] The second thin film layer is formed on the first thin film layer by sputtering, deposition or electroless plating. The metal used is exemplified by nickel, copper, gold, silver or the like. It is preferable to use copper because it has appropriate electrical characteristic and is economical and a thickening layer formed in a later step mainly consists of copper.

[0023] The reason for providing the second thin film layer is that only the first thin film layer cannot provide an electroplating lead to form a thickening layer to be described later. The second thin film layer 36 is employed as a thickening lead. The thickness of the second thin film is preferably 0.01 to 5 μm . If the thickness is smaller than 0.01 μm , the second thin film layer cannot function as a lead. If the thickness exceeds 5 μm , the lower first thin film layer is cut more than the second thin film layer to thereby generate gaps, moisture tends to enter the interference and reliability deteriorates during etching.

[0024] The second thin film layer is thickened by electroless plating or electroplating. The type of a metal formed is exemplified by copper, nickel, gold, silver, zinc, iron or the like. It is preferable to use copper for electroplating because copper has appropriate electrical characteristic, is economical, has the strength and structural resistance of the transition layer and a conductor layer to be build up in a later step mainly consists of copper. The thickness of the second thin film layer is preferably 1 to 20 μm . If the thickness is smaller than 1 μm , the connection reliability of the layer with the upper via hole deteriorates. If the thickness exceeds 20 μm , undercut occurs during etching and thereby gaps are generated in the interface between the formed transition layer and the via hole. In some cases, the first thin film layer may be directly plated to thicken the layer or multiple layers may be provided.

[0025] Thereafter, an etching resist is formed with reference to the positioning mark on the core substrate, exposure and development are performed to expose the portions of the metal other than that of the transition layer and etching is then performed, thereby forming a transition layer consisting of the first thin film layer, the second thin film layer and a thickening layer on the die pad of the IC chip.

[0026] In case of forming a transition layer by a subtractive process, a metallic film is thickened by electroless plating or electroplating. The type of the plated member to be formed is exemplified by copper, nickel, gold, silver, zinc, iron or the like. It is preferable to use copper because copper has appropriate electrical characteristic and is economical and a buildup conductive layer to be formed later mainly consists of copper. The thickness is preferably in the range of 1 to 20 μm . If the thickness exceeds the range, undercut occurs during etching and gaps may be generated in the interface between the transition layer and the via hole to be formed. Thereafter, an etching resist is formed, exposure and development are performed to the portion of the metal other than that of the transition layer, thereby forming a transition layer on the pad of the IC chip.

[0027] As stated above, the inventors of the present invention devised including an IC chip in a package substrate by containing the IC chip in a recess formed in the core substrate and building up an interlayer resin insulating layer and a conductive circuit on the core substrate.

[0028] According to this method, a metallic film is formed on the entire surface of the core substrate containing the IC chip so as to cover or protect the pad of the IC chip, or, in some cases, forming a transition layer on the pad, thereby electrically connecting the pad to the via hole of the interlayer resin insulating layer.

[0029] However, since the metallic film is formed on the entire surface, a positioning mark formed on the IC chip is concealed and a mask on which wirings are drawn or a laser device cannot be positioned relative to the substrate. Due to this, it is estimated that a positional error occurs between the pad on the IC chip and the via hole and that electrical connection cannot be established between the pad and the via hole.

[0030] The present invention has been made to solve the above-stated problems. It is another object of the present invention to propose a method of a multilayer printed circuit board manufacturing method capable of being appropriately connected to an IC chip included in the multilayer printed circuit board.

[0031] The objects of the invention have been achieved by the multilayer printed circuit board and the method defined in the claims.

Brief Description of the Drawings

[0032]

FIG. 1 is a diagram showing a process for manufacturing a multilayer printed circuit board in the first embodiment according to the present invention;

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FIG. 2 is a diagram showing a process for manufacturing the multilayer printed circuit board in the first embodiment;
FIG. 3 is a diagram showing a process for manufacturing the multilayer printed circuit board in the first embodiment;
FIG. 4 is a diagram showing a process for manufacturing the multilayer printed circuit board in the first embodiment;
FIG. 5 is a diagram showing a process for manufacturing the multilayer printed circuit board in the first embodiment;
5 FIG. 6 is a cross-sectional view of the multilayer printed circuit board in the first embodiment;
FIG. 7 (A) is a drawing showing an enlarged transition layer shown in FIG. 3 (A), FIG. 7(B) is a diagram seen from B of FIG. 7(A) and FIGS. 7(C), (D) and (E) are explanatory views for modifications of the transition layer;
FIG. 8 (A) is a perspective view of the multilayer printed circuit board in the first embodiment, and FIG. 8(B) is an explanatory view for the multilayer printed circuit board which is partly enlarged;
10 FIG. 9(A) is a perspective view of a multilayer printed circuit board in the first modification of the first embodiment, and FIG. 9 (B) is an explanatory view for the multilayer printed circuit board which is partly enlarged;
FIG. 10 is a cross-sectional view of a printed circuit board in the second modification of the first embodiment;
FIG. 11 is a cross-sectional view of a printed circuit board in the third modification of the first embodiment;
FIG. 12 is a cross-sectional view of a multilayer printed circuit board in the fourth modification of the first embodiment;
15 FIG. 13 is a diagram showing a process for manufacturing a multilayer printed circuit board in the second embodiment;
FIG. 14 is a diagram showing a process for manufacturing a multilayer printed circuit board in the second embodiment;
FIG. 15 is a diagram showing a process for manufacturing a multilayer printed circuit board in the second embodiment;
FIG. 16 is a diagram showing a process for manufacturing a multilayer printed circuit board in the second embodiment;
FIG. 17 is a diagram showing a process for manufacturing a multilayer printed circuit board in the second embodiment;
20 FIG. 18 is a cross-sectional view of the multilayer printed circuit board in the second embodiment;
FIG. 19(A) is a plan view of a core substrate shown in FIG. 13(D), and FIG. 19(B) is a plan view of FIG. 13(E);
FIG. 20(A) is a plan view of the core substrate before a photomask film is mounted, and FIG. 20(B) is a plan view of the core substrate in a state in which the photomask film is mounted;
FIG. 21 is a cross-sectional view of a multilayer printed circuit board in the first modification of the second embodiment;
25 FIG. 22 is a diagram showing a process for manufacturing a multilayer printed circuit board in the third embodiment;
FIG. 23 is a diagram showing a process for manufacturing the multilayer printed circuit board in the third embodiment;
FIG. 24 is a diagram showing a process for manufacturing the multilayer printed circuit board in the third embodiment;
FIG. 25 is a diagram showing a process for manufacturing the multilayer printed circuit board in the third embodiment;
FIG. 26 is a cross-sectional view of the multilayer printed circuit board in the third embodiment;
30 FIG. 27 (A) is an enlarged, explanatory view for a die pad portion shown in FIG. 22(C), FIG. 27(B) is an enlarged, explanatory view for a die pad portion shown in FIG. 23 (A), and FIG. 27 (C) is an enlarged, explanatory view for a die pad portion shown in FIG. 24(A);
FIG. 28 is a cross-sectional view of a multilayer printed circuit board in the first modification of the third embodiment;
FIGS. 29(A), (B) and (C) are drawings showing an enlarged die pad portion in the first modification of the third embodiment, wherein FIG. 29 (A) shows a state before an oxide film removal process, FIG. 29 (B) shows a state after the oxide film removal process and FIG. 29 (C) shows a state after a transition layer is formed on a die pad.

Best Modes for Working the Invention

40 **[0033]** The embodiments of the present invention will be described hereinafter with reference to the drawings.

[First Embodiment]

45 **[0034]** First, the constitution of a multilayer printed circuit board according to the first embodiment of the present invention will be described with reference to FIG. 6 showing the cross-sectional view of a multilayer printed circuit board 10.

[0035] As shown in FIG. 6, the multilayer printed circuit board 10 consists of a core substrate 30 containing therein an IC chip 20, an interlayer resin insulating layer 50 and an interlayer resin insulating layer 150. Via holes 60 and conductor circuits 58 are formed on the interlayer resin insulating layer 50. Via holes 160 and conductor circuits 158 are formed on the interlayer resin insulating layer 150.

50 **[0036]** The IC chip 20 is covered with a passivation film 22 and die pads 24 each constituting an input/output terminal are provided in the openings of the passivation film 22. A transition layer 38 is formed on each die pad 24 made of aluminum. The transition layer 38 consists of three layers of the first thin film layer 33, the second thin film layer 36 and a thickening layer 37.

55 **[0037]** A solder resist layer 70 is provided on the interlayer resin insulating layer 150. BGAs 76 for connecting to an external substrate such as a daughter board or a mother board which is not shown in FIG. 6 are provided on the conductor circuits 158 under the openings 71 of the solder resist layer 70, respectively.

[0038] In the multilayer printed circuit board 10 in the first embodiment, the IC chip 20 is included in the core substrate 30 in advance and the transition layer 38 is provided on each die pad 24 of the IC chip 20. Due to this, it is possible to

electrically connect the IC chip to the multilayer printed circuit board (or package substrate) without using lead members and a sealing resin. Further, since the transition layers 38 are formed on the IC chip portion, the IC chip portion is flattened and the upper interlayer insulating layer 50 is, therefore, flattened to thereby provide uniform film thickness. Further, because of the transition layers, it is possible to maintain the stability of shape even if the via holes 60 provided in the upper layer are formed.

[0039] Furthermore, by providing the transition layers 38 made of copper on the respective die pads 24, it is possible to prevent resin residues on the die pads 24 and to prevent the die pads 24 from being discolored or dissolved even after impregnating the multilayer printed circuit board in an acid, an oxidizer or an etching solution in a later step or conducting various annealing steps. Thus, connection characteristic between the die pads of the IC chip and the via holes and reliability can be improved. Furthermore, by interposing the transition layers 38 each having a diameter of 60 μm or more on the respective die pads 24 each having a diameter of about 40 μm , it is possible to ensure connecting the via holes each having a diameter of 60 μm or more.

[0040] Next, a method of manufacturing the multilayer printed circuit board described above with reference to FIG. 6 will be described with reference to FIGS. 1 to 5.

(1) First, an insulating resin substrate (or core substrate) 30 in which prepregs each having a core material made of glass cloths or the like and impregnated with a resin such as epoxy are built up, is used as a starting material (see FIG. 1(A)). Next, a recess 32 for containing an IC chip is formed on one side of the core substrate 30 by counter boring (see FIG. 1(B)). While the recess is provided by counter boring herein, it is also possible to form a core substrate having a containing section by laminating an insulating resin substrate having an opening portion and an insulating resin substrate without an opening.

(2) Then, an adhesive material 34 is applied to the recess 32 using a printing machine. At this time, potting instead of application may be conducted. Next, an IC chip 20 is mounted on the adhesive material 34 (see FIG. 1(C)).

(3) Then, the upper surface of the IC chip 20 is depressed or struck to thereby completely contain the IC chip 20 in the recess 32 (see FIG. 1(D)). By doing so, the core substrate 30 can be smoothed.

(4) Thereafter, the entire surface of the core substrate 30 which contains the IC chip 20 therein is subjected to deposition or sputtering to form the conductive, first thin film layer 33 on the entire surface (FIG. 2(A)). A metal used may be tin, chromium, titanium, nickel, zinc, cobalt, gold or copper. Nickel, chromium or titanium is more preferable because it is capable of suppressing the entry of moisture into an interface, appropriate for film formation and in electrical characteristic. The thickness of the first thin film layer 33 is preferably 0.001 to 2.0 μm , more preferably, 0.01 to 1.0 μm . In case of chromium, the thickness is preferably 0.1 μm .

The die pad 24 is covered with the first thin film layer 33, thereby making it possible to improve the adhesiveness of the transition layer and the IC chip to the interface with the die pad 24. Also, by covering the die pad 24 with the metal, it is possible to prevent moisture from entering the interface, to prevent the dissolution and erosion of the die pad and to improve reliability. Further, the first thin film layer 33 allows the die pad to connect with the IC chip by a mounting method without using a lead. Here, if chromium, titanium or nickel is used, it is possible to prevent the entry of moisture into the interface and to ensure high metal adhesiveness.

(5) The second thin film layer 36 is formed on the first thin film layer 33 by sputtering, deposition or electroless plating (FIG. 2(B)). A metal used herein may be nickel, copper, gold or silver. Copper is preferable because the copper has good electrical characteristic and is economical and because a buildup conductor layer to be formed in a later step mainly consists of copper.

The reason for providing the second thin film layer is that an electroplating lead for forming a thickening layer to be described later cannot be provided only with the first thin film layer. The second thin film layer 36 is used as a lead for thickening and preferably 0.01 to 5 μm in thickness. The thickness is more preferably 0.1 to 3 μm . The second thin film layer having such a thickness is optimum to cover the first thin film and serve as a lead. If the thickness is less than 0.01 μm , the second thin film layer cannot function as a lead. If the thickness exceeds 5 μm , the first thin film layer under the second thin film layer is cut more than the second thin film layer and gaps are generated between the first and second thin film layers during etching. This makes the entry of moisture easier and deteriorates reliability.

A preferable combination of the first and second thin film layer is chromium - copper, chromium - nickel, titanium - copper, titanium - nickel or the like. These combinations are superior to the other combinations in view of junction with a metal and electrical conductivity.

(6) Thereafter, a resist is applied, exposure and development are conducted to provide a plated resist 35 while providing an opening on the upper portion of the die pad of the IC chip, and electroplating is conducted under the following conditions to thereby provide an electroplated film (or thickening film) 37 (FIG. 2(C)).

[Electroplating Solution]	
sulfuric acid	2.24 mol/l
copper sulfate	0.26 mol/l

(continued)

additive 19.5 mol/l
(Kapalacid HL manufactured by Atotech Japan)

[Electroplating Conditions]

current density 1 A/dm²
duration 65 minutes
temperature 22±2°C

After removing the plating resist 35, the electroless-plated, second thin film layer 36 and first thin film layer 33 under the plating resist 35 are etched away, thereby forming a transition layer 38 on each of the die pads 24 of the IC chip (FIG. 2(D)). The transition layer is formed by the plating resist in this case. Alternatively, the transition layer may be formed on each die pad by after uniformly forming an electroless-plated film on the electroless-plated, second thin film layer 36, forming an etching resist, conducting exposure and development to expose the metal other than that of the transition layer, and conducting etching. The thickness of the electroplated film is preferably in the range of 1 to 20 μm. If the thickness exceeds the range, undercut may possibly occur during the etching to generate gaps in the interface between the transition layer to be formed and the via hole.

(7) Next, an etching solution is sprayed onto the substrate and the surface of the transition layer 38 is etched, thereby forming a rough surface 38α (see FIG. 3 (A)). The rough surface can be also formed by electroless plating or an oxidation-reduction process. FIG. 7 (A) is an enlarged view of the transition layer 38 shown in FIG. 3(A). FIG. 7(B) is a view seen from B of FIG. 7(A). The transition layer 38 is a three-layer structure consisting of the first thin film layer 33, the second thin film layer 36 and the thickening layer 37. As shown in FIG. 7 (A), the transition is formed to be circular. It is also possible to form the transition layer to be not circular but ellipsoidal as shown in FIG. 7 (C), rectangular as shown in FIG. 7(D) or oval as shown in FIG. 7(E).

(8) A thermosetting resin sheet having a thickness of 50 μm is vacuum-compression laminated onto the substrate which has gone through the above-stated steps at a pressure of 5 kg/cm² while raising temperature to 50 to 150°C, thereby providing an interlayer resin insulating layer 50 (see FIG. 3(B)). The degree of vacuum at the time of vacuum compression is 10 mmHg.

(9) Next, using CO₂ gas laser having a wavelength of 10.4 μm, via hole openings 48 each having a diameter of 80 μm are provided in the interlayer resin insulating layer 50 under the conditions of a beam diameter of 5 mm, a top hat mode, a pulse width of 5.0 μm, a mask hole diameter of 0.5 mm and one shot (see FIG. 3(C)). Using a chromic acid, resin residues in the openings 48 are removed. By providing the transition layer 38 made of copper on each die pad 24, it is possible to prevent resin residues on the die pad 24, thereby improving connection characteristic between the die pad 24 and a via hole 60 to be described later and improving reliability. Furthermore, by interposing the transition layer 38 having a diameter of 60 μm or more on the die pad 24 having a diameter of about 40 μm, it is possible to ensure connecting the via hole opening 48 having a diameter of 60 μm. While the resin residues are removed by using a permanganic acid, a de-smear process can be also conducted using oxygen plasma.

(10) Next, the resultant substrate is immersed in an oxidizer such as a chromic acid or a permanganic acid or the like, thereby providing a rough surface 50α on the interlayer resin insulating layer 50 (see FIG. 3(D)). The rough surface 50α is preferably formed in the range of 0.05 to 5 μm. For example, the substrate is immersed in 50 g/l of a sodium permanganate solution at a temperature of 60°C for 5 to 25 minutes, thereby providing a rough surface 50α of 1 to 5 μm. Alternatively, by performing a plasma process using SV-4540 manufactured by ULVAC JAPAN Ltd., the rough surface 50α can be formed on the interlayer resin insulating layer 50. In that case, argon gas is used as inactive gas to perform a plasma process for two minutes under conditions of electric power of 200W, a gas pressure of 0.6 Pa and a temperature of 70°C.

(11) A metallic layer 52 is provided on the interlayer resin insulating layer 50 on which the rough surface 50α is formed (see FIG. 4 (A)). The metallic layer 52 is formed by electroless plating. By supplying a catalyst such as a palladium catalyst to the surface layer of the interlayer resin insulating layer 50 in advance and immersing the substrate into an electroless plating solution for 5 to 60 minutes, the metallic layer 52 which is a plated film in the range of 0.1 to 5 μm is provided. For example, the substrate was immersed in the following solution at a solution temperature of 34°C for 40 minutes:

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[Electroless Plating Solution]

NiSO ₄	0.003 mol/l
tartaric acid	0.200 mol/l
copper sulfate	0.030 mol/l
HCHO	0.050 mol/l
NaOH	0.100 mol/l
α,α' -bipyridyl	100 mg/l
polyethylene glycol (PEG)	0.10 g/l

Alternatively, an Ni/Cu metallic layer 52 can be formed on the surface of the interlayer resin insulating layer 50 by exchanging internal argon gas and then conducting sputtering with Ni and Cu as targets under conditions of an air pressure of 0.6 Pa, a temperature of 80°C, power of 200W and a duration of five minutes with the same device as that used for the above-stated plasma process. At this time, the thickness of an Ni/Cu metallic layer 52 formed is 0.2 μm . Alternatively, the metallic film can be formed by deposition, electrodeposition or the like instead of sputtering. It is also possible to form a thin layer by a physical method such as sputtering, deposition or electrodeposition and then to conduct electroless plating.

(12) A commercially available photosensitive dry film is bonded to the substrate 30 which has been subjected to the above process, a chromium glass mask is mounted, exposure is performed at 40 mJ/cm² and then a development process is conducted with 0.8% sodium carbonate, thereby providing plating resists 54 each having a thickness of 25 μm (see FIG. 4 (B)). Next, electroplating is conducted under the following conditions to form an electroplated film 56 having a thickness of 18 μm . An additive in the electroplating solution is Kapalacid HL manufactured by Atotech Japan.

[Electroplating Solution]

sulfuric acid	2.24 mol/l
copper sulfate	0.26 mol/l
additive	19.5 mol/l
(Kapalacid HL manufactured by Atotech Japan)	

[Electro Plating Conditions]

current density	1A/dm ²
duration	65 minutes
temperature	22 $\pm$ 2°C

(13) After separating and removing the plating resist 54 with 5%NaOH, the metallic layer 52 under the plating resist is dissolved and removed by etching using a mixture solution of an nitric acid and oxygenated water, conductor circuits 58 each consisting of the metallic layer 52 and the electroplated film 56 and having a thickness of 16 μm and via holes 60 are formed and etched by an etching solution containing a cupric salt complex and an organic acid, thereby forming rough surfaces 58 α and 60 α (see FIG. 4(C)). Alternatively, the rough surfaces can be formed by electroless plating or an oxidization-reduction process.

(14) Next, the steps of (9) to (13) stated above are repeated, thereby forming an upper interlayer resin insulating layer 150 and conductor circuits 158 (include via holes 160)(see FIG. 5(A)).

(15) Then, 46.67 parts by weight of oligomer (having a molecular weight of 4000) which is obtained by forming 50% of epoxy groups of 60 parts by weight of a cresol novolac epoxy resin (manufactured by Nippon Kayaku) dissolved in diethylene glycol dimethyl ether (DMDG) into an acrylic structure and which imparts photosensitive characteristic, 15 parts by weight of 80 wt% of a bisphenol A epoxy resin (product name: Epicoat 1001 manufactured by Yuka Shell) dissolved in methylethyl keton, 1.6 parts by weight of an imidazole hardening agent (product name: 2E4MZ-CN manufactured by Shikoku Chemicals), 3 parts by weight of polyhydric acryl monomer which is a photosensitive monomer (product name: R604 manufactured by Kyoei Chemical), 1.5 parts by weight of polyhydric acryl monomer (product name: DPE6A manufactured by Kyoei Chemical), and 0.71 parts by weight of a dispersing defoaming agent (product name: S-65 manufactured by Sannopuko) are contained in a container, agitated and mixed to adjust mixture compositions. Then, 2.0 parts by weight of benzophenone (manufactured by Kanto Chemical) serving as a photoinitiator and 0.2 parts by weight of Michler's ketone (manufactured by Kanto Chemical) serving as a photosensitizer are added to the mixture compositions, thereby obtaining a solder resist composition (or organic resin insulating material) adjusted to have a viscosity of 2.0 Pa·s.

Note that the viscosity is measured by using No. 4 rotor of a B-type viscometer (DVL-B manufactured by Tokyo Keiki) when the velocity is 60 rpm and using No. 3 rotor of the same when the velocity is 6 rpm.

(16) Next, the solder resist composition is applied to the substrate 30 to have a thickness of 20 μm and a drying process is conducted at 70°C for 20 minutes and 70°C for 30 minutes. Then, a photomask film having a pattern of the solder resist opening portions drawn thereon and a thickness of 5 mm is made hermetic contact with the solder resist layer 70, exposure is performed with ultraviolet rays with 1000 mj/cm^2 and then a development process is performed with a DMTG solution, thereby forming openings 71 each having a land diameter of 620 μm and an opening diameter of 460 μm (see FIG. 5(B)).

(17). Next, the substrate on which the solder resist layer (or organic resin insulating layer) 70 is formed, is immersed in an electroless nickel plating solution containing nickel chloride (2.3×10^{-1} mol/l); sodium hypophosphite (2.8×10^{-1} mol/l), sodium citrate (1.6×10^{-1} mol/l and having $\text{pH} = 4.5$ for 20 minutes, and a nickel plate layer 72 having a thickness of 5 μm is formed on each opening portion 71. Then, the substrate is further immersed in an electroless plating solution containing gold potassium cyanide (7.6×10^{-3} mol/l), ammonia chloride (1.9×10^{-1} mol/l), sodium citrate (1.2×10^{-1} mol/l and sodium hypophosphite (1.7×10^{-1} mol/l) under the condition of 80°C for 7.5 minutes and a gold plated layer 74 having a thickness of 0.03 μm is formed on the nickel plated layer 72, thereby forming a solder pad 75 on each conductor layer 158 (see FIG. 5(C)).

(18) Thereafter, a solder paste is printed on the opening portion 71 of the solder resist layer 70 and reflowed at 200°C, thereby forming a BGAs 76. As a result, it is possible to obtain a multilayer printed circuit board 10 including the IC chip 20 and having the BGAs 76 (see FIG. 6). Instead of the BGAs, PGA (conductive contact pins) may be arranged.

[0041] In the above-stated embodiment, the thermosetting resin sheet is used for the interlayer resin insulating layers 50 and 150. The thermosetting resin insulating sheet contains a refractory resin, soluble particles, a hardening agent and other components. The materials will now be described one by one.

[0042] The epoxy resin which can be used in the thermosetting resin sheet in the first embodiment has a structure that particles soluble in an acid or an oxidizer (to be referred to as "soluble particles" hereinafter) are dispersed in a resin which is refractory with respect to an acid or an oxidizer (to be referred to as "refractory resin" hereinafter). The expressions "refractory" and "soluble" are used as follows. When materials are immersed in a solution composed of the same acid or the same oxidizer for the same time, a material of a type which is dissolved at a relatively high dissolving rate is called a "soluble" material and a material of a type which is dissolved at a relatively slow dissolving rate is called "refractory material" for convenience.

[0043] The soluble particles are exemplified by resin particles which are soluble in an acid or an oxidizer (to be referred to as "soluble resin particles" hereinafter), inorganic particles which are soluble in an acid or an oxidizer (to be referred to as "inorganic soluble particles" hereinafter), metal particles which are soluble in an acid or an oxidizer (to be referred to as "soluble metal particles" hereinafter) and the like. The foregoing soluble particles may be employed solely or two or more particles may be mixed.

[0044] The shape of each of the soluble particles is not limited. The shape may be a spherical shape or a pulverized shape. It is preferable that the soluble particles have a uniform shape. The reason for this lies in that a rough surface having uniformly rough pits and projections can be formed.

[0045] It is preferable that the mean particle size of the soluble particles is 0.1 μm to 10 μm . When the particles have the diameters satisfying the foregoing range, two or more particles having different particle sizes may be employed. That is, soluble particles having a mean particle size of 0.1 μm to 0.5 μm and soluble particles having a mean particle size of 1 μm to 3 μm may be mixed. Thus, a more complicated rough surface can be formed. Moreover, the adhesiveness with the conductor circuit can be improved. In the first embodiment, the particle size of the soluble particles is the length of a longest portion of each of the soluble particles.

[0046] The soluble resin particles are exemplified by particles constituted by a thermosetting resin or a thermoplastic resin. When the particles are immersed in solution composed of an acid or an oxidizer, the particles must exhibit dissolving rate higher than that of the foregoing refractory resin.

[0047] Specifically, the soluble resin particles are exemplified by particles constituted by an epoxy resin, a phenol resin, a polyimide resin, a polyphenylene resin, a polyolefin resin or a fluorine resin. The foregoing material may be employed solely or two or more materials may be mixed.

[0048] The soluble resin particles may exemplified by resin particles constituted by rubber. The rubber above is exemplified by polybutadiene rubber, a variety of denatured polybutadiene rubber, such as denatured epoxy rubber, denatured urethane rubber or denatured (meta) acrylonitrile rubber, and (meta) acrylonitrile butadiene rubber containing a carboxylic group. When the foregoing rubber material is employed, the soluble resin particles can easily be dissolved in an acid or an oxidizer. That is, when the soluble resin particles are dissolved with an acid, dissolution is permitted with an acid other than a strong acid, and when dissolved with an oxidizer, dissolution is permitted with permanganate which has a relatively weak oxidizing power. When chromic acid is employed, dissolution is permitted even at a low concentration. Therefore, the retention of the acid or the oxidizer on the surface of the resin can be prevented. When a catalyst, such as palladium chloride, is supplied after the rough surface has been formed as described later, the inhibition

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of supply of the catalyst and the oxidation of the catalyst can be prevented.

[0049] The inorganic soluble particles are exemplified by particles made of at least a material selected from a group consisting of an aluminum compound, a calcium compound, a potassium compound, a magnesium compound and a silicon compound.

5 **[0050]** The aluminum compound is exemplified by alumina, aluminum hydroxide and the like. The calcium compound is exemplified by calcium carbonate, calcium hydroxide and the like. The potassium compound is exemplified by potassium carbonate and the like. The magnesium compound is exemplified by magnesia, dolomite, basic magnesium carbonate and the like. The silicon compound is exemplified by silica, zeolite and the like. The foregoing material may be employed solely or two or more materials may be mixed.

10 **[0051]** The soluble metal particles are exemplified by particles constituted by at least one material selected from a group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, potassium and silicon. The soluble metal particles may have surfaces coated with a resin or the like in order to maintain insulating characteristic.

[0052] When two or more types of the soluble particles are mixed, it is preferable that the combination of the two types of soluble particles is a combination of resin particles and inorganic particles. Since each of the particles has low electric conductivity, insulating characteristic with the resin film can be maintained. Moreover, the thermal expansion can easily be adjusted with the refractory resin. Thus, the occurrence of a crack on the interlayer resin insulating layer constituted by the resin film can be prevented. The separation between the interlayer resin insulating layer and the conductor circuit can be prevented.

20 **[0053]** The refractory resin is not limited when the resin is able to maintain the shape of the rough surface when the rough surface is formed on the interlayer resin insulating layer by using an acid or an oxidizer. For example, the refractory resin is exemplified by a thermosetting resin, a thermoplastic resin and their composite material. As an alternative to this, the foregoing photosensitive resin of a type having photosensitive characteristics imparted thereto may be employed. When the photosensitive resin is employed, exposure and development processes can be performed to of the interlayer resin insulating layers to thereby form openings for the via holes.

25 **[0054]** In particular, it is preferable that the resin containing a thermosetting resin is employed. In the foregoing case, the shape of the rough surface can be maintained against a plating solution and when a variety of heating processes are performed.

30 **[0055]** The refractory resin is exemplified by an epoxy resin, a phenol resin, a phenoxy resin, a polyimide resin, a polyphenylene resin, a polyolefin resin, a fluorine resin and the like. The foregoing material may be employed solely or two or more types of the materials may be mixed. A thermosetting resin, a thermoplastic resin or a complex thereof may be employed.

[0056] It is preferable that an epoxy resin having two or more epoxy groups in one molecule thereof is employed. The reason for this lies in that the foregoing rough surface can be formed. Moreover, excellent heat resistance and the like can be obtained. Thus, the concentration of a stress onto the metallic layer can be prevented even under a heat cycle condition. Thus, the occurrence of separation of the metallic layer can be prevented.

35 **[0057]** The epoxy resin is exemplified by a cresol novolac epoxy resin, a bisphenol-A epoxy resin, a bisphenol-F epoxy resin, a phenol novolac epoxy resin, an alkylphenol novolac epoxy resin, a biphenol-F epoxy resin, a naphthalene epoxy resin, a dicyclopentadiene epoxy resin, an epoxy material constituted by a condensation material of phenol and an aromatic aldehyde having a phenol hydroxyl group, triglycidyl isocyanurate and alicyclic epoxy resin. The foregoing material may be employed solely or two or more material may be mixed. Thus, excellent heat resistance can be obtained.

40 **[0058]** It is preferable that the soluble particles in the resin film used in the first embodiment are substantially uniformly dispersed in the refractory resin. The reason for this lies in that a rough surface having uniform pits and projections can be formed. When via holes and through holes are formed in the resin film, adhesiveness with the metallic layer of the conductor circuit can be maintained. As an alternative to this, a resin film containing soluble particles in only the surface layer on which the rough surface is formed may be employed. Thus, the portions of the resin film except for the surface layer is not exposed to an acid or an oxidizer. Therefore, the insulating characteristic between conductor circuits through the interlayer resin insulating layers can reliably be maintained.

45 **[0059]** It is preferable that the amount of the soluble particles which are dispersed in the refractory resin is 3 wt% to 40 wt% with respect to the resin film. When the amount of mixture of the soluble particles is lower than 3 wt%, the rough surface having required pits and projections cannot be formed. When the amount is higher than 40wt%, the deep portions of the resin film are undesirably dissolved when the soluble particles are dissolved by using an acid or an oxidizer. Thus, the insulating layer constituted by the resin film cannot be maintained. This sometimes causes short circuit.

50 **[0060]** It is preferable that the resin film contains a hardening agent and other components as well as the refractory resin.

[0061] The hardening agent is exemplified by an imidazole hardening agent, an amino hardening agent, a guanidine hardening agent, an epoxy adduct of each of the foregoing hardening agents, a microcapsule of each of the foregoing hardening agents and an organic phosphine compound such as triphenylphosphine or tetraphenyl phosphonium tetraphenyl borate.

55 **[0062]** It is preferable that the content of the hardening agent is 0.05 wt% to 10 wt% in the resin film. If the content is

lower than 0.05 wt%, the resin film cannot sufficiently be hardened. Thus, the introduction of the acid and the oxidizer into the resin film occurs more frequently and the insulating characteristic of the resin film sometimes deteriorates. When the content is higher than 10wt%, an excessively large quantity of the hardening agent component sometimes denatures the composition of the resin and the reliability sometimes deteriorates.

[0063] The other components are exemplified by an inorganic compound which does not exert an influence on the formation of the rough surface and a filler such as a resin. The inorganic compound is exemplified by silica, alumina, dolomite and the like. The resin is exemplified by a polyimide resin, a polyacrylic resin, a polyamideimide resin, a polyphenylene resin, a melanine resin, an olefin resin and the like. If any one of the foregoing fillers is contained, then the conformity of thermal expansion coefficients can be established and heat resistance, chemical resistance can be improved and the performance of the multilayer printed circuit board can be thereby improved.

[0064] The resin film may contain a solvent. The solvent is exemplified by ketone such as acetone, methyl ethyl ketone or cyclohexane, aromatic hydrocarbon such as ethyl acetate, butyl acetate, cellosolve acetate, toluene or xylene. The foregoing material may be employed solely or two or more materials may be mixed. However, the interlayer resin insulating layers made from the foregoing materials are dissolved and carbonated at a temperature of 350°C or higher.

[0065] After bonding the resin film, the film is opened by laser and via holes are formed in the interlayer resin insulating layers. Thereafter, the substrate is immersed in an acid or an oxidizer to thereby form rough surfaces on the interlayer resin insulating layers. The acid is exemplified by a strong acid such as a sulfuric acid, a phosphoric acid, a hydrochloric acid or a formic acid. The oxidizer is exemplified by a chromic acid, a mixture of chromium and a sulfuric acid, permanganate and the like. Soluble particles are dissolved or separated using the acid or oxidizer, thereby forming rough surfaces on the interlayer resin insulating layers. A catalyst such as Pb is supplied to the interlayer resin insulating layers on which the rough layers are formed, and then electroless plating is performed. Plating resist unformed regions are formed by providing a resist on the electroless plated film and conducting exposure and development. The regions are electroplated, the resist is separated, and the electroplated films on the interlayer resin insulating layers are removed by etching, thereby forming via holes and conductor circuits.

[0066] FIG. 8 (A) is a perspective view of the multilayer printed circuit board 10 according to the first embodiment. FIG. 8 (B) is an explanatory view showing the multilayer printed circuit board 10 which is partly enlarged. Semiconductor bumps (ball-grid arrays) 76 are provided in a hound's tooth manner on the entire surface of the multilayer printed circuit board 10. In the first embodiment, by forming the BGAs 76 on the IC chip 20, it is possible to shorten the lengths of wirings from the IC chip 20.

[First Modification of First Embodiment]

[0067] FIG. 9 (A) is a perspective view of a multilayer printed circuit board 10 according to the first modification of the first embodiment. FIG. 9(B) is an explanatory view showing the multilayer printed circuit board 10 which is partly enlarged in the modification. Semiconductor bumps (ball-grid arrays) 76 are provided in a hound's tooth manner on the surface of the multilayer printed circuit board 10 in all corners except for the portion on the IC chip 20. In this modification, by avoiding forming the bumps 76 on the IC chip 20, it is made advantageously difficult for the BGAs 76 to be thermally and electromagnetically influenced by the IC chip.

[Second Modification of First Embodiment]

[0068] Next, description will be given to a multilayer printed circuit board according to the second modification of the first embodiment with reference to FIG. 10. In the first embodiment stated above, description has been given to a case where the BGAs are arranged. In the second modification, which is almost the same as the first embodiment, the multilayer printed circuit board is constituted in a PGA mode for establishing connection through conductive connection pins 96 as shown in FIG. 10.

[Third Modification of First Embodiment]

[0069] Next, description will be given to a multilayer, printed circuit board according to the third modification of the first embodiment with reference to FIG. 11.

[0070] In the first embodiment stated above, the IC chip is contained in the recess 32 provided in the core substrate 30 by counter boring. In the third modification, by contrast, an IC chip 20 is contained in a through hole 32 formed in the core substrate 30. In this third modification, a heat sink can be directly attached to the rear surface side of the IC chip 20, so that it is advantageous that the IC chip 20 can be cooled efficiently.

[Fourth Modification of First Embodiment]

[0071] Next, a multilayer printed circuit board in the fourth modification of the first embodiment will be described with reference to FIG. 12.

[0072] In the first embodiment stated above, the IC chip is contained in the multilayer printed circuit board. In the fourth modification, by contrast, an IC chip 20 is contained in the multilayer printed circuit board and an IC chip 120 is mounted on the surface of the multilayer printed circuit board. As the IC chip 20 included in the layer, a cache memory having a relatively low calorific value is employed. As the IC chip 20 mounted on the surface, a CPU for arithmetic operation is employed.

[0073] The die pads 24 of the IC chip 20 and the die pads 124 of the IC chip 120 are mutually connected through transition layers 38 - via holes 60 - conductor circuits 58 - via holes 160 - conductor circuit 158 - BGAs 76U, respectively. On the other hand, the die pads 124 of the IC chip 120 and the pads 92 of a daughter board 90 are mutually connected through BGAs 76U - conductor circuits 158 - via holes 160 - conductor circuits 58 - via holes 60 - through holes 136 - via holes 60 - conductor circuits 58 - via holes 60 - conductor circuits 158 - BGAs 76U, respectively.

[0074] In the fourth modification, it is possible to arrange the IC chip 120 and the cache memory 20 in proximity while separately manufacturing the cache memory 20 having low yield and the IC chip 120 for the CPU, and to operate the IC chips at high speed. In this fourth modification, by including an IC chip in the multilayer printed circuit board and, at the same time, mounting an IC chip on the surface thereof, it is possible to package electronic components such as IC chips having different functions and to thereby obtain a multilayer printed circuit board having greater functions.

[0075] With the structure of the first embodiment, the IC chip and the printed circuit board can be connected to each other without using lead members. Due to this, resin sealing becomes unnecessary. Furthermore, since no defects resulting from the lead members and sealing resin occur, connection characteristic and reliability are improved. Besides, since the die pads of the IC chip are directly connected to the conductive layers of the printed circuit board, it is possible to improve electrical characteristic.

[0076] Moreover, compared with the conventional IC chip mounting method, the wiring length from the IC chip to the substrate to the external substrate can be advantageously shortened and loop inductance can be advantageously reduced.

[Second Embodiment]

[0077] Next, the constitution of a multilayer printed circuit board according to the second embodiment of the present invention will be described with reference to FIG. 18 showing the cross-section of a multilayer printed circuit board 210.

[0078] As shown in FIG. 18, the multilayer printed circuit board 210 consists of a core substrate 230 containing therein an IC chip 220, an interlayer resin insulating layer 250 and an interlayer resin insulating layer 350. Via holes 260 and conductor circuits 258 are formed on the interlayer resin insulating layer 250. Via holes 360 and conductor circuits 358 are formed on the interlayer resin insulating layer 350.

[0079] The IC chip 220 is covered with a passivation film 222, and die pads 224 each constituting an input/output terminal and positioning marks 223 are provided in the respective openings of the passivation film 222. A transition layer 238 mainly consisting of copper is formed on each die pad 224.

[0080] A solder resist layer 270 is provided on the interlayer resin insulating layer 350. BGAs 276 for connecting to an external substrate, such as a daughter board or a mother board which is not shown, are provided on the conductor circuits 358 under the openings 271 of the solder resist layer 270, respectively.

[0081] In the multilayer printed circuit board 210 in the second embodiment, the IC chip 220 is included in the core substrate 230 in advance and the transition layer 238 is provided on each die pad 224 of the IC chip 220. Due to this, it is possible to electrically connect the IC chip to the multilayer printed circuit board (or package substrate) without using lead members and a sealing resin.

[0082] Furthermore, by providing the transition layers 238 made of copper on the respective die pads 224, it is possible to prevent resin residues on the die pads 224 and to prevent the die pads 224 from being discolored or dissolved even after impregnating the multilayer printed circuit board in an acid, an oxidizer or an etching solution in a later step or conducting various annealing steps.

[0083] Moreover, in manufacturing steps to be described later, positioning marks 231 are formed on the core substrate 230 with reference to the positioning marks 223 of the IC chip 220 and the via holes 260 are formed to conform to the positioning marks 231, respectively. Due to this, it is possible to accurately position the via holes 260 on the pads 224 of the IC chip 220 and to ensure connecting the pads 224 to the via holes 260, respectively.

[0084] Next, a method of manufacturing the multilayer printed circuit board described above with reference to FIG. 18 will be described with reference to FIGS. 13 to 17.

(1) First, an insulating resin substrate (or core substrate) 230, in which prepregs each having a core material made

of glass cloths or the like and impregnated with a resin such as epoxy are built up, is used as a starting material (see FIG. 13 (A)). Next, a recess 232 for containing an IC chip is formed on one side of the core substrate 230 by counter boring (see FIG. 13 (B)).

(2) Then, an adhesive material 234 is applied to the recess 232 using a printing machine. At this time, potting instead of application may be conducted. Next, an IC chip 220 is mounted on the adhesive material 234 (see FIG. 13(C)).

(3) The upper surface of the IC chip 220 is depressed or struck to thereby completely contain the IC chip 220 in the recess 232 (see FIG. 13(D)). The plan view of the IC chip 220 and the core substrate 230 shown in FIG. 13 (D) are shown in FIG. 19 (A). The IC chip 220 contained in the recess 232 of the core substrate 230 is not accurately positioned relative to the core substrate because of the working accuracy of the recess and the interposition of the adhesive material 234.

(4) The positioning marks 223 provided in the four corners of the IC chip 220 are photographed by a camera 280, and recesses 231a are provided in the four corners of the core substrate 230 with reference to the positioning marks 223, respectively, by laser (FIG. 13(E)). The plan view of the IC chip 220 and the core substrate 230 shown in FIG. 13 (E) is shown in FIG. 19 (B).

(5) Thereafter, the entire surface of the core substrate 230 which contains the IC chip 220 therein is subjected to deposition or sputtering, to form a conductive metallic film 233 on the entire surface (FIG. 14 (A)). The metal used is formed out of one or more of tin, chromium, titanium, nickel, zinc, cobalt, gold, copper and the like. In some cases, two or more layers may be formed out of different metals. The thickness of the metallic layer is preferably in the range of 0.001 to 2.0 μm . More preferably, the thickness is 0.01 to 1.0 μm .

A plated film 236 may be formed on the metallic film 233 by electroless plating, electroplating or a combination thereof (FIG. 14(B)). The type of the metal used for plating is exemplified by copper, nickel, gold, silver, zinc or iron. Copper is preferably used because it has appropriate electrical characteristic and is economical and buildup conductor layers formed in a later step mainly consist of copper. The thickness of the plated film is preferably in the range of 0.01 to 5.0 μm . If the thickness is smaller than 0.01 μm , the plated film cannot be formed on the entire surface. If the thickness exceeds 5.0 μm , it becomes difficult to etch away the film. Besides, the positioning marks are embedded and cannot be recognized. The preferable range is 0.1 to 3.0 μm . The plated film can be also formed by sputtering or deposition.

(6) Thereafter, a resist 235 α is provided, a mask 239 on which patterns 239a and positioning marks 239b corresponding to the pads 224 are drawn is mounted (FIG. 14 (C)). This mask 235 is positioned while applying light from above and the image of reflection light from the positioning marks 231 is picked up by a camera 289 so that the positioning mark through holes 231a on the core substrate 230 side can fall in the positioning marks 239b which are drawn to be ring-shaped. In the second embodiment, since the copper plated film 236 is formed even on the positioning marks 231, the reflection light easily transmits the resist 235 α and the substrate and the mask can be easily positioned relative to each other.

(7) Plating resists 235 are formed so as to provide opening portions above the respective pads 224 of the IC chip by exposure and development and electroplated films 237 are provided by electroplating (FIG. 19(D)). After removing the plating resists 235, the electroless plated film 236 and the metallic film 233 under the plating resists 235 are removed, thereby forming transition layers 238 on the pads 224 of the IC chip and forming positioning marks 231 on the recesses 231a, respectively (FIG. 14(E)).

(8) Next, an etching solution is sprayed on the substrate and the surfaces of the transition layers 238 are etched, thereby forming rough surfaces 238 α , respectively (see FIG. 15 (A)). The rough surfaces can be formed by electroless plating or an oxidization-reduction process.

(9) The same thermosetting resin sheet as that in the first embodiment is vacuum-compression laminated onto the substrate which has gone through the above-stated steps and an interlayer resin insulating layer 250 is provided (see FIG. 15(B)).

(10) Next, the images of the positioning marks 231 are picked up by the camera 280 while transmitting the interlayer resin insulating layer 250, thereby conducting positioning. Via hole openings 248 each having a diameter of 80 μm are provided in the interlayer resin insulating layer 250 using CO₂ gas laser having a wavelength of 10.4 μm under the conditions of a beam diameter of 5 mm, a pulse width of 5.0 $\mu\text{seconds}$, a mask hole diameter of 0.5 mm and one shot (see FIG. 15(C)).

(11) Next, the surface of the interlayer resin insulating layer 250 is roughened to thereby form a rough surface 250 α (see FIG. 15 (E)).

(12) Then, a metallic layer 252 is formed on the surface of the interlayer resin insulating layer 250 (see FIG. 16(A)).

(13) A commercially available photosensitive dry film 254 α is bonded to the substrate 230 which has been completed with the above-stated steps, and a photomask film 253, on which patterns 253a and positioning marks 253b corresponding to the pads are drawn, is mounted. The plan view of the core substrate 230 before the photomask film 253 is mounted is shown in FIG. 20(A) and a state in which the photomask film 253 is mounted is shown in FIG. 20 (B). This mask 253 is positioned while light is applied from above and the image of reflection light from the positioning

marks 231 is picked up by the camera 289 so that the positioning marks 231 at the core substrate 230 sidemay fall in the positioning marks 253b which are drawn to be ring-shaped. In the second embodiment, since the plated film 237 is formed on the positioning marks 231, the reflection light is easily transmitted by the interlayer resin insulating layer 250 and the film 254 α and accurate positioning can be conducted. As stated above, the roughening process is conducted to the copper plated films 237 constituting the positioning marks 231. It is also possible not to conduct the roughening process so as to increase surface reflectance or to conduct the roughening process and then conducting a surface smoothing process using chemicals or laser.

(14) Thereafter, exposure is performed with 100 mJ/cm² and a development process is conducted with 0.8% of sodium carbonate, thereby forming plating resists 254 each having a thickness of 15 μ m (FIG. 16(C)).

(15) Next, electroplating is conducted under the same conditions as those in the first embodiment to thereby form an electroplated film 256 having a thickness of 15 μ m (see FIG. 16(D)).

(16) After separating and removing the plating resists 254 with 5%NaOH, the metallic layer 252 under the plating resists 254 is dissolved and removed by etching and conductor circuits 258 each consisting of the metallic layer 252, the electroplated film 256 and via holes 260 are formed and rough surfaces 258 α and 260 α are formed with an etching solution (see FIG. 17(A)).

(17) Next, the steps of (6) to (12) stated above are repeated, thereby forming an interlayer resin insulating layer 350 and conductor circuits 358 (include via holes 360) further above (see FIG. 17(B)).

(18) Next, the same solder resist composition as that in the first embodiment is applied to the substrate 230 to have a thickness of 20 μ m, and a drying process is conducted. After that, exposure is conducted with a photomask hermetically contacted with the solder resist layer 270, a development process is conducted with a DMTG solution, and opening portions 270 each having a diameter of 200 μ m are formed (see FIG. 17(C)).

(19) Then, the substrate on which the solder resist layer (or organic resin insulating layer) 270 is formed is immersed in an electroless nickel plating solution, thereby forming nickel plated layers 272 on opening portions 271, respectively. Further, the substrate is immersed in the electroless plating solution and a gold plated layer 274 having a thickness of 0.03 μ m is formed on each of the nickel plated layers 272, thereby forming solder pads 275 on the conductor circuits 358, respectively (see FIG. 17(D)).

(20) Thereafter, a solder paste is printed on the opening portions 271 of the solder resist layer 270 and reflowed at 200 °C, thereby forming BGAs 276. Thus, it is possible to obtain a multilayer printed circuit board 210 including the IC chip 220 and having the BGAs 276 (see FIG. 18). PGAs (conductive connection pins) instead of the BGAs may be arranged.

[First Modification of Second Embodiment]

[0085] Next, description will be given to a multilayer printed circuit board according to the first modification of the second embodiment of the present invention with reference to FIG. 21.

[0086] In the second embodiment stated above, the IC chip is contained in the multilayer printed circuit board. In the first modification of the second embodiment, by contrast, an IC chip 220 is contained in the multilayer printed circuit board and, at the same time, an IC chip 320 is mounted on the surface thereof. As for the IC chip 220 included in the circuit board, a cache memory having a relatively low calorific value is employed. As for the IC chip 320 on the surface, a CPU for arithmetic operation is mounted.

[0087] In this first modification of the second embodiment, penetrating holes 335 constituting the through holes 336 of a core substrate 230 are formed with reference to the positioning marks 231 of the core substrate.

[Third Embodiment]

[0088] Next, the constitution of a multilayer printed circuit board according to the third embodiment of the present invention will be described hereinafter with reference to FIG. 26 showing the cross section of a multilayer printed circuit board 410.

[0089] As shown in FIG. 26, the multilayer printed circuit board 410 consists of a core substrate 430 containing therein an IC chip 420, an interlayer resin insulating layer 450 and an interlayer resin insulating layer 550. Via holes 460 and conductor circuits 458 are formed on the interlayer resin insulating layer 450. Via holes 560 and conductor circuits 558 are formed on the interlayer resin insulating layer 550.

[0090] The IC chip 420 is covered with an IC protective film (made of passivation + polyimide) 422 and aluminum die pads 424 each constituting an input/output terminal are provided in the respective openings of the IC protective film 422. An oxide film 426 is formed on each die pad 424. A transition layer 438 is formed on each die pad 424 and the oxide film 426 on the surface, on which the die pad 424 and the transition layer 438 contact with each other, is removed.

[0091] A solder resist layer 470 is formed on the interlayer resin insulating layer 550. A solder bump 476 or a conductive connection pin, which is not shown, for connecting to an external substrate such as a daughter board or a mother board,

which is not shown, is provided on the conductor circuit 558 under each opening portion 471 of the solder resist layer 470.

[0092] In the multilayer printed circuit board 410 in this embodiment, the IC chip 420 is included in the core substrate 430 in advance and the transition layers 420 are provided on the die pads 424 of the IC chip 420, respectively. Due to this, alignment can be easily made when forming via holes and buildup layers can be stably formed even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less. If the via holes of the interlayer resin insulating layers are formed by photoetching with the die pads on which the transition layers are not formed and via hole diameter is larger than a die pad diameter, then the polyimide layer serving as the protective layer on the surface of each die pad is dissolved and damaged during a de-smear process conducted as a via hole bottom residue removal process and an interlayer resin insulating layer surface roughening process. On the other hand, in case of using laser, if the via hole diameter is larger than the die pad diameter, the die pads and passivation-polyimide layers (or IC protective films) are damaged by laser. Moreover, if the pads of the IC chip are very small and the via hole diameter is larger than the die pad size, then positioning becomes quite difficult even with a photoetching method or a laser method. As a result, connection errors between the die pads and the via holes frequently occur.

[0093] By providing the transition layers 438 on the respective die pads 424, by contrast, it is possible to ensure the connection of the via holes 460 to the die pads 424 even with a die pad pitch of 150 μm or less and a pad size of 20 μm or less, and the connection characteristic between the pads 424 and the via holes 460 and reliability are improved. Further, by interposing the transition layers each having a larger diameter on the respective pads of the IC chip, there is no fear of dissolving and damaging the die pads and the IC protective films (passivation-polyimide layers) even if the substrate is immersed in an acid or an etching solution in later steps such as de-smear and plating steps or the substrate has gone through various annealing steps.

[0094] Furthermore, since the oxide film 426 formed on the die pads 424 made of aluminum is removed on the surfaces on which the die pads 424 and the transition layers 438 contact with one another by an oxide film removal process to be described later, it is possible to reduce the electrical resistances of the die pads 424 and to increase the electrical conductivity thereof.

[0095] Next, a method of manufacturing the multilayer printed circuit board described above with reference to FIG. 26 will be described with reference to FIGS. 22 to 27.

(1) First, an insulating resin substrate (or core substrate) 430 in which prepregs each having a core material made of glass cloths or the like and impregnated with a resin such as epoxy are built up, is used as a starting material (see FIG. 22 (A)). Next, a recess 432 for containing an IC chip is formed on one side of the core substrate 430 by counter boring (see FIG. 22 (B)).

(2) Then, an adhesive material 434 is applied to the recess 432 using a printing machine. At this time, potting instead of application may be conducted. Next, an IC chip 420 is mounted on the adhesive material 434. The IC chip 420 is covered with an IC protective film (made of passivation + polyimide) 422, and die pads 424 each constituting an input/output terminal are provided in the respective openings of the IC protective film 422. Also, the surfaces of the die pads 424 are covered with oxide films 426, respectively (see FIG. 22(C)). Here, an explanatory view enlarging the die pad 424 portion of the IC chip 420 is shown in FIG. 27(A).

(3) Then, the upper surface of the IC chip 420 is depressed or struck to thereby completely contain the IC chip 420 in the recess 432 (see FIG. 22 (D)). It is thereby possible to flatten the core substrate 430.

(4) Next, the core substrate 430 containing therein the IC chip 420 is put in a sputtering device in a vacuum state. While argon gas which is inactive gas is used as sputtering gas, inverse sputtering is performed with the exposed oxide films 426 on the surfaces of the die pads 424 as targets, thereby removing the exposed oxide films 426 (see FIG. 23 (A)). Here, an explanatory view enlarging the die pad 424 portion of the IC chip 420 is shown in FIG. 27(B). It is thereby possible to reduce the electric resistances of the die pads 424, to improve the electric conductivities thereof and to improve the adhesiveness thereof with corresponding transition layers. In this case, inverse sputtering is employed as an oxide film removal process. A plasma process instead of the inverse sputtering can be employed. In case of the plasma process, the substrate is put in a device in a vacuum state, plasmas are discharged in oxygen or nitrogen, carbon dioxide and carbon tetrafluoride to thereby remove the oxide films on the surfaces of the die pads. It is also possible to process the die pad surfaces with an acid other than the plasma process and to remove the oxide films. It is preferable to use a phosphoric acid in the oxide film removal process. The oxide films are removed herein. Even if films such as anticorrosive nitride films are formed on the die pads, it is preferable to conduct a removal process so as to improve the electric conductivities of the die pads.

(5) Thereafter, using the same device consecutively, the entire surface of the core substrate 430 is sputtered with Cr and Cu as targets without exposing the IC chip to an oxygen atmosphere, thereby forming a conductive metallic film 433 on the entire surface (see FIG. 23 (B)). The metallic film 433 is preferably formed out of one or more layers of metals such as tin, chromium, titanium, nickel, zinc, cobalt, gold and silver. The thickness of the metallic film is preferably formed to be in the range of 0.001 to 2.0 μm . The thickness is more preferably 0.01 to 1.0 μm . The thickness of a chromium layer is set so as not to generate cracks on the sputtered layer and to sufficiently hermetically

contact with a copper sputtered layer. In the third embodiment, the removal of films and the formation of the lowermost layer (metallic layer) 433 of each transition layer are conducted in the same device under a non-oxygen atmosphere in succession. Due to this, it is possible to improve the electric conductivity between the die pads 424 of the IC chip and the transition layer 438 without forming oxide films on the pad surfaces again.

5 A plated film 436 may be formed on the metallic film 433 by electroless plating, electroplating or a combination thereof (see FIG. 23(C)). The type of the metal used for plating is exemplified by copper, nickel, gold, silver, zinc or iron. Copper is preferably used because it has appropriate electrical characteristic and is economical and buildup conductor layers formed in a later step mainly consist of copper. The thickness of the plated film is preferably in the range of 0.01 to 5.0 μm . The thickness is more preferably 0.1 to 3 μm . The plated film can be also formed by sputtering or deposition. The desirable combination of the first thin film layer and the second thin film layer is chromium - copper, chromium - nickel, titanium - copper, titanium - nickel or the like. These combinations are superior to the other combinations in junction with metal and electric conductivity.

10 (6) Thereafter, a resist is applied or a photosensitive film is laminated, and plating resists 435 are provided to provide openings on the upper portions of the pads of the IC chip 420 by exposure and development, thereby forming electroplated films 437 (see FIG. 23 (D)). The thickness of the electroplated film 437 is preferably about 1 to 20 μm . After removing the plating resists 435, the electroless plated film 436 and the metallic film 433 under the plating resists 435 are etched away, thereby forming transition layers 438 on the pads 424 of the IC chip, respectively (see FIG. 24(A)). Also, an explanatory view enlarging the die pad 424 portion of the IC chip 420 is shown in FIG. 27(C). In this case, the transition layers 438 are formed by the plating resists. It is also possible to form the transition layers 438 on the die pads 424 of the IC chip 420 by uniformly forming electroplated films 437 on the respective electroless plated film 436, forming an etching resist, conducting exposure and development to expose the portions of the metal other than those on the transition layers and conducting etching. In this case, the thickness of the electroless plated film 437 is preferably in the range of 1 to 20 μm . If the thickness exceeds that range, undercut occurs during the etching and gaps are generated in the interfaces between the transition layers and via holes to be formed.

25 (7) Next, an etching solution is sprayed on the substrate, the surfaces of the transition layers 438 are etched to thereby form rough surfaces 438 α on the respective surfaces (see FIG. 24(B)). It is also possible to form the rough surfaces by electroless plating or an oxidization-reduction process.

(8) A thermosetting resin sheet is vacuum-compression laminated onto the substrate which has gone through the above-stated steps as in the case of the first embodiment, thereby providing an interlayer resin insulating layer 450 (see FIG. 24(C)).

30 (9) Next, via hole openings 448 are provided in the interlayer resin insulating layer 450 using CO₂ gas laser (see FIG. 24(D)). Thereafter, resin residues on the openings 448 may be removed using an oxidizer such as a chromic acid or a permanganic acid. By providing the transition layers 438 made of copper on the die pads 424, respectively, alignment can be easily made at the time of forming via holes, the connection of the via holes onto the die pads 424 is ensured and the connection characteristics between the pads and the via holes and reliability are improved. Thus, it is possible to stably form buildup layers. By providing the transition layers each having a larger diameter on the respective pads of the IC chip, there is no fear of dissolving and damaging the die pads 424 and the IC protective films (passivation-polyimide layers) 422 even if the substrate is immersed in an acid or an etching solution in later steps such as a via hole bottom residue removal process, a de-smear process conducted as an interlayer resin insulating layer surface roughening process, a plating step and the like or if the substrate has gone through various annealing steps. In this case, the resin residues are removed by using a permanganic acid. It is also possible to conduct a de-smear process using oxygen plasma.

40 (10) Next, the surface of the interlayer resin insulating layer 450 is roughened to thereby form a rough surface 450 α (see FIG. 25(A)). This roughening step can be omitted.

45 (11) Next, after a palladium catalyst is supplied to the surface of the interlayer resin insulating layer 450, the substrate is immersed in an electroless plating solution and an electroless plated film 452 is formed on the surface of the interlayer resin insulating layer 450 (see FIG. 25 (B)).

(12) A commercially available photosensitive dry film is bonded to the substrate 430 which has been subjected to the above processes, a chromium glass mask is mounted, exposure is performed with 40 mj/cm^2 and then a development process is conducted with 0.8% sodium carbonate, thereby providing plating resists 454 each having a thickness of 25 μm . Next, electroplating is conducted under the same conditions as those in the first embodiment, thereby forming electroplated films 456 each having a thickness of 18 μm (see FIG. 25(C)).

50 (13) After separating and removing the plating resists 454 with 5%NaOH, the electroless plated film 452 under the plating resists is dissolved and removed by etching, conductor circuits 458 each consisting of the electroless plated film 452 and the electroplated film 456 and having a thickness of 16 μm and via holes 460 are formed, and rough surfaces 458 α and 960 α are formed by an etching solution (see FIG. 25 (D)). The following steps are the same as the steps (13) to (17) in the first embodiment stated above, which description will not be given herein.

[First Modification of Third Embodiment]

[0096] Now, a multilayer printed circuit board according to the first modification of the third embodiment of the present invention will be described with reference to FIGS. 28 and 29. FIG. 28 shows the cross-section of a multilayer printed circuit board 510 and FIGS. 29 are views showing an enlarged die pad 424 portion, where FIG. 29 (A) is a view showing a state before an oxide film removal process is conducted, FIG. 29 (B) is a view showing a state of the oxide film removal process and FIG. 29 (C) is a view showing a state after a transition layer 438 is formed on each die pad 429.

[0097] In the third embodiment stated above, description has been given to a case where BGAs are provided. In the first modification of the third embodiment, which is almost the same as the third embodiment, the multilayer printed circuit board is constituted in a PGA mode for establishing connection through conductive connection pins 496 as shown in FIG. 28.

[0098] In the manufacturing method of the first modification of the third embodiment, a part of the oxide film 426 of the die pad 424 is removed by conducting one of oxide film removal process from among an inverse sputtering process, a plasma process and an acid process as shown in FIG. 29 (B). Then, as shown in FIG. 29(C), a transition layer 438 consisting of a metallic film 433, an electroless plated film 436 and an electroplated film 437 is formed on the die pad 424. It is thereby possible to reduce the electric resistance of the die pad 426 and to improve electrical conductivity thereof as in the case of the third embodiment.

[Comparison Example]

[0099] A multilayer printed circuit board was obtained by forming transition layers as in the case of the third embodiment except that film removal was not conducted.

Test Result

[0100] The result of evaluating the multilayer printed circuit boards in the third embodiment and in the comparison example with respect to a total of four items of 1) sectional state, 2) resistance measurement value, 3) sectional state after reliability test, and 4) resistance measurement value after reliability test is shown in a table

Evaluation Result			
Classification	Item	Embodiment	Comparison Example
After Formation Of Transition	Whether Or Not Oxide Film Is Present	Not Present	Present
	Connection Resistance Value	0.095Ω	14.6Ω
After Reliability Test	Whether Or Not Oxide Film Is Present	Not Present	Present
	Whether Or Not Transition Is Separated	Not Present	Present
	Connection Resistance Value	0.105Ω	17.8Ω

1) Sectional State

[0101] After forming the transition layer, the layer was cut in cross section and whether or not an oxide film is present on the pad was observed with a microscope ($\times 100$).

2) Resistance Measurement Value

[0102] After forming the transition layer, connection resistance was measured. A numeric value measured is an average of those measured in 20 places.

3) Sectional State after Reliability Test

[0103] After forming the multilayer printed circuit board and then finishing a heat cycle test (1000 cycles with one cycle of (130°C / 3 minutes) + (-60°C / 3 minutes)), the multilayer printed circuit board was cut in cross section and whether or not an oxide film was present on the pad and whether or not the transition was separated was observed with the

microscope ($\times 100$).

4) Resistance Measurement Value after Reliability Test

[0104] After forming the multilayer printed circuit board and then finishing the heat cycle test (1000 cycles with one cycle of (130°C / 3 minutes) + (-60°C / 3 minutes)), connection resistance was measured. A numeric value measured is an average of those measured in 20 places.

[0105] As shown in the table, the multilayer printed circuit board in the third embodiment had no oxide film and had a low connection resistance value, so that no problem occurred to electrical connection. Besides, the multilayer printed circuit board in the third embodiment was less deteriorated after the reliability test. It is noted that even after repeating 2000 cycles of the heat cycle test, not so a great increase in resistance value was observed.

[0106] In the comparison example, the oxide film remained and the connection resistance value was high. In some cases, portions on which no electrical connection could be established were observed. This trend was more conspicuous after the reliability test.

Claims

1. A multilayer printed circuit board (10) having interlayer insulating layers (50, 150) and conductor layers (58) repeatedly formed on a substrate, (30) an electronic component (20) included in said substrate (30) and via holes (60) formed in the interlayer insulating layers (50, 150), and establishing connection through the via holes (60), **characterized in that** a mediate layer (38) connected to the via hole (60) of a lowermost interlayer insulating layer is formed on a pad (24) portion of said electronic component, said mediate layer (38) comprising at least 2 metal layers.
2. A multilayer printed circuit board (10) having interlayer insulating layers (50, 150) and conductor layers (58) repeatedly by formed on a substrate (30) an electronic component (20) included in said substrate (30) and via holes (60) formed in the interlayer insulating layers (50, 150), and establishing connection through the via holes (60), **characterized in that** a mediate layer (38) connected to the via hole (60) of a lowermost interlayer insulating layer is formed on a pad (24) portion of said electronic component, a width of said mediate layer being 1.0 to 30 times as large as a width of said pad.
3. A multilayer printed circuit board according to claim 1 or 2, **characterized in that** said board (10) is a package substrate.
4. A multilayer printed circuit board according to claim 1, **characterized in that** a width of said mediate layer is 1.0 to 30 times as large as a width of said pad.
5. A multilayer printed circuit board according to claims 1-4 **characterized in that** said mediate layer (38) comprises a first thin film layer (33), a second thin film layer (36) and a thickening layer (37).
6. A multilayer printed circuit board (10) according to any of claims 1 to 5, **characterized in that** said via hole (60) connected to said mediate layer (38) has the conductor layer (58).
7. A multilayer printed circuit board (10) according to claim 6, **characterized in that** the conductor layer (58) of the said via hole (60) consists of metal including copper.
8. A multilayer printed circuit board (10) according to any of claims 1 to 7, **characterized in that** said electronic component (20) consists of an IC chip.
9. A multilayer printed circuit board according to claim 5, **characterized in that** said first thin film layer (33) is made of one type or more selected from a group consisting of tin, chromium, titanium, nickel, zinc, cobalt, gold and copper.

10. A multilayer printed circuit board according to claim 5 or 9,
characterized in that
said second thin film layer (36) is made of one type of more selected from a group consisting of nickel, copper, gold and silver.
11. A method of manufacturing a multilayer printed circuit board (10) having interlayer resin insulating layers (50, 150) and conductor layers (58) repeatedly formed on a substrate (30) including an electronic component (20), **characterized in that**
the method comprises at least the following steps (a) to (d):
- (a) forming a first thin film layer (33), and a second thin film layer (36) on an entire surface of the substrate (30) into which said electronic component (20) is embedded;
 - (b) providing a resist on said thin film layer, and forming a thickening layer (37) on portions on which the resist is not formed; and
 - (c) removing the thin film layers (33,36) by etching, forming a mediate layer on a pad of the electronic component comprising an IC chip,
 - (d) embedding the electronic component (20) on which the mediate layer (38) is formed.
12. A multilayer printed circuit board manufacturing method according to claim 11, wherein
said first thin film layer (33) is subjected to one of sputtering and deposition.
13. A multilayer printed circuit board manufacturing method according to claim 11 or 12, wherein
said second thin film layer (36) is subjected to one of sputtering, deposition and electroless plating.

Patentansprüche

1. Mehrschichtige Leiterplatte (10) mit Zwischenlagen-Isolierschichten (50, 150) und Leiterschichten (58), die wiederholt auf einem Substrat (30) ausgebildet sind, wobei in dem Substrat (30) ein elektronisches Bauelement (20) enthalten ist, und Durchkontaktierungsöffnungen (60), die in den Zwischenlagen-Isolierschichten (50, 150) ausgebildet sind, wobei eine Verbindung durch die Durchkontaktierungsöffnungen (60) hergestellt wird, **dadurch gekennzeichnet, daß**
eine Mittlungsschicht (38), die mit dem Durchkontaktierungsloch (60) einer untersten Zwischenlagen-Isolierschicht verbunden ist, auf einem Kontaktfleckenabschnitt (24) des elektronischen Bauelements ausgebildet ist, wobei die Mittlungsschicht (38) mindestens zwei Metallschichten aufweist.
2. Mehrschichtige Leiterplatte (10) mit Zwischenlagen-Isolierschichten (50, 150) und Leiterschichten (58), die wiederholt auf einem Substrat (30) ausgebildet sind, wobei in dem Substrat (30) ein elektronisches Bauelement (20) enthalten ist, und Durchkontaktierungsöffnungen (60), die in den Zwischenlagen-Isolierschichten (50, 150) ausgebildet sind, wobei eine Verbindung durch die hergestellt wird, **dadurch gekennzeichnet, daß**
eine Mittlungsschicht (38), die mit dem Durchkontaktierungsloch (60) einer untersten Zwischenlagen-Isolierschicht verbunden ist, auf einem Kontaktfleckenabschnitt (24) des elektronischen Bauelements ausgebildet ist, wobei die Mittlungsschicht 1,0 bis 30 mal so breit ist wie der Kontaktfleckenabschnitt.
3. Mehrschichtige Leiterplatte nach Anspruch 1 oder 2, **dadurch gekennzeichnet, daß** die Platine (10) ein Baugruppensubstrat ist.
4. Mehrschichtige Leiterplatte nach Anspruch 1, **dadurch gekennzeichnet, daß** eine Breite der Mittlungsschicht 1,0 bis 30 mal so groß wie eine Breite des Kontaktflecks ist.
5. Mehrschichtige Leiterplatte nach einem der Ansprüche 1 bis 4, **dadurch gekennzeichnet, daß** die Mittlungsschicht (38) eine erste Dünnschicht (33), eine zweite Dünnschicht (36) und eine Verdickungsschicht (37) aufweist.
6. Mehrschichtige Leiterplatte (10) nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet, daß** das mit der Mittlungsschicht (38) verbundene Durchkontaktierungsloch (60) die Leiterschicht (58) aufweist.
7. Mehrschichtige Leiterplatte (10) nach Anspruch 6, **dadurch gekennzeichnet, daß** die Leiterschicht (58) des Durchkontaktierungslochs (60) aus Metall besteht, das Kupfer enthält.

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8. Mehrschichtige Leiterplatte (10) nach einem der Ansprüche 1 bis 7, **dadurch gekennzeichnet, daß** das elektronische Bauelement (20) aus einem IC-Chip besteht.
- 5 9. Mehrschichtige Leiterplatte nach Anspruch 5, **dadurch gekennzeichnet, daß** die erste Dünnschicht (33) aus einer oder mehreren Arten besteht, die aus einer Gruppe ausgewählt sind, die aus Zinn, Chrom, Titan, Nickel, Zink, Kobalt, Gold und Kupfer besteht.
- 10 10. Mehrschichtige Leiterplatte nach Anspruch 5 oder 9, **dadurch gekennzeichnet, daß** die zweite Dünnschicht (36) aus einer oder mehreren Arten besteht, die aus einer Gruppe ausgewählt sind, die aus Nickel, Kupfer, Gold und Silber besteht.
- 15 11. Verfahren zur Herstellung einer mehrschichtigen Leiterplatte (10) mit Zwischenlagen-Harzisolierschichten (50, 150) und Leiterschichten (58), die wiederholt auf einem Substrat (30) ausgebildet werden, das ein elektronisches Bauelement (20) enthält, **dadurch gekennzeichnet, daß** das Verfahren mindestens die folgenden Schritte (a) bis (d) aufweist:
- (a) Ausbilden einer ersten Dünnschicht (33) und einer zweiten Dünnschicht (36) auf einer gesamten Oberfläche des Substrats (30), in die das elektronische Bauelement (20) eingebettet ist;
- 20 (b) Bereitstellen eines Abdecklacks auf der Dünnschicht und Ausbilden einer Verdichtungsschicht (37) auf Abschnitten, auf denen der Abdecklack nicht ausgebildet ist;
- (c) Entfernen der Dünnschichten (33, 36) durch Ätzen, Bilden einer Mittlungsschicht auf einem Kontaktfleck des elektronischen Bauelements, das einen IC-Chip aufweist;
- (d) Einbetten des elektronischen Bauelements (20), auf dem die Mittlungsschicht (38) ausgebildet wird.
- 25 12. Herstellungsverfahren für mehrschichtige Leiterplatte nach Anspruch 11, wobei die erste Dünnschicht (33) einem Sputterprozeß oder einer Abscheidung unterzogen wird.
- 30 13. Herstellungsverfahren für mehrschichtige Leiterplatte nach Anspruch 11 oder 12, wobei die zweite Dünnschicht (36) einem Sputterprozeß, einer Abscheidung oder einer stromlosen Metallisierung unterzogen wird.

Revendications

- 35 1. Carte à circuit imprimé multicouche (10) ayant des couches isolantes (50, 150) entre les couches et des couches conductrices (58) formées de manière répétée sur un substrat (30), un composant électronique (20) inclus dans ledit substrat (30) et des trous d'interconnexion (60) formés dans les couches isolantes (50, 150) présentes entre les couches et établissant une connexion par les trous d'interconnexion (60), **caractérisée en ce que** :
- 40 une couche médiate (38) connectée au trou d'interconnexion (60) d'une couche isolante inter-couche la plus basse est formée sur une partie plage de connexion (24) dudit composant électronique, ladite couche médiate (38) comprenant au moins 2 couches de métal.
- 45 2. Carte à circuit imprimé multicouche (10) ayant des couches isolantes (50, 150) entre les couches et des couches conductrices (58) formées de manière répétée sur un substrat (30), un composant électronique (20) inclus dans ledit substrat (30) et des trous d'interconnexion (60) formés dans les couches isolantes (50, 150) présentes entre les couches et établissant une connexion par les trous d'interconnexion (60), **caractérisée en ce que** :
- 50 une couche médiate (38) connectée au trou d'interconnexion (60) d'une couche isolante inter-couche la plus basse est formée sur une partie plage de connexion (24) dudit composant électronique, une largeur de ladite couche médiate valant de 1,0 à 30 fois la largeur de ladite plage de connexion.
- 55 3. Carte à circuit imprimé multicouche selon la revendication 1 ou 2, **caractérisée en ce que** ladite carte (10) est un substrat de boîtier.
4. Carte à circuit imprimé multicouche selon la revendication 1, **caractérisée en ce que** la largeur de ladite couche médiate vaut de 1,0 à 30 fois la largeur de ladite plage de connexion.

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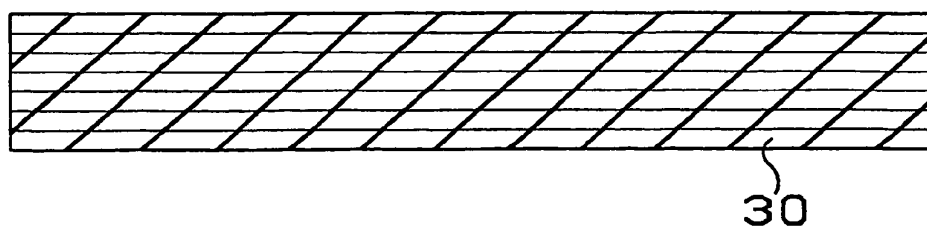
5. Carte à circuit imprimé multicouche selon l'une quelconque des revendications 1 à 4, **caractérisée en ce que** ladite couche médiate (38) comprend une première couche à film mince (33), une deuxième couche à film mince (36) et une couche d'épaississement (37).
- 5 6. Carte à circuit imprimé multicouche (10) selon l'une quelconque des revendications 1 à 5, **caractérisée en ce que** ledit trou d'interconnexion (60) connecté à ladite couche médiate (38) comporte la couche conductrice (58).
7. Carte à circuit imprimé multicouche (10) selon la revendication 6, **caractérisée en ce que** la couche conductrice (58) dudit trou d'interconnexion (60) est constituée de métal comportant du cuivre.
- 10 8. Carte à circuit imprimé multicouche (10) selon l'une quelconque des revendications 1 à 7, **caractérisée en ce que** ledit composant électronique (20) consiste en une puce de CI.
9. Carte à circuit imprimé multicouche selon la revendication 5, **caractérisée en ce que** ladite première couche à film mince (33) est faite d'un type ou plus choisi dans le groupe comprenant l'étain, le chrome, le titane, le nickel, le zinc, le cobalt, l'or et le cuivre.
- 15 10. Carte à circuit imprimé multicouche selon la revendication 5 ou 9, **caractérisée en ce que** ladite deuxième couche à film mince (36) est faite d'un type ou plus choisi dans le groupe comprenant le nickel, le cuivre, l'or et l'argent.
- 20 11. Procédé de fabrication d'une carte à circuit imprimé multicouche (10) ayant des couches isolantes en résine (50, 150) entre les couches et des couches conductrices (58) formées de manière répétée sur un substrat (30) comprenant un composant électronique (20), **caractérisé en ce que** :
- 25 le procédé comprend au moins les étapes (a) à (d) suivantes :
- (a) former une première couche à film mince (33) et une deuxième couche à film mince (36) sur une surface entière du substrat (30) dans lequel est incorporé ledit composant électronique (20) ;
- 30 (b) placer une réserve sur ladite couche à film mince, puis former une couche d'épaississement (37) sur des parties sur lesquelles la réserve n'est pas formée ; et
- (c) retirer les couches à film mince (33, 36) par attaque chimique, en formant une couche médiate sur une plage de connexion du composant électronique comprenant une puce de CI,
- (d) enrober le composant électronique (20) sur lequel la couche médiate (38) est formée.
- 35 12. Procédé de fabrication d'une carte à circuit imprimé multicouche selon la revendication 11, dans lequel on soumet ladite première couche à film mince (33) à un traitement choisi parmi une pulvérisation et un dépôt.
13. Procédé de fabrication d'une carte à circuit imprimé multicouche selon la revendication 11 ou 12, dans lequel on soumet ladite deuxième couche à film mince (36) à un traitement choisi parmi une pulvérisation, un dépôt et un placage anélectrolytique.
- 40

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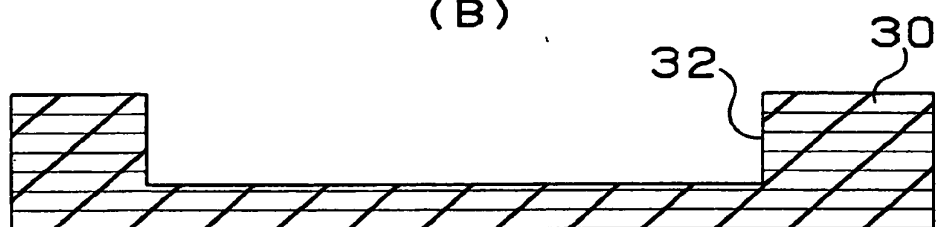
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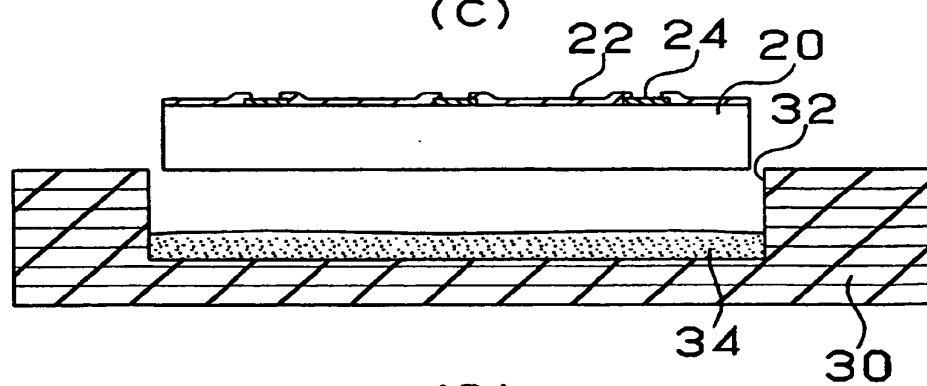
Fig. 1
(A)



(B)



(C)



(D)

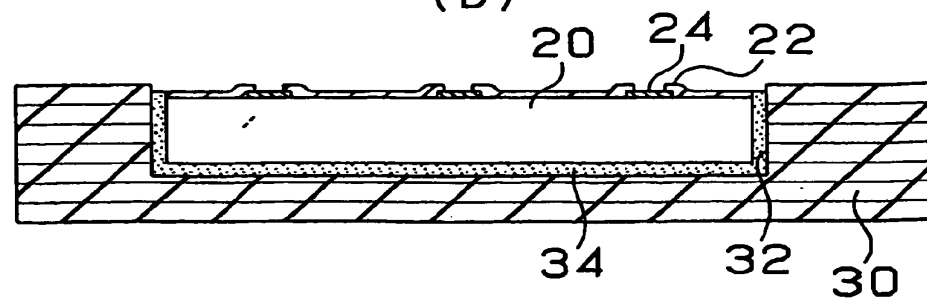
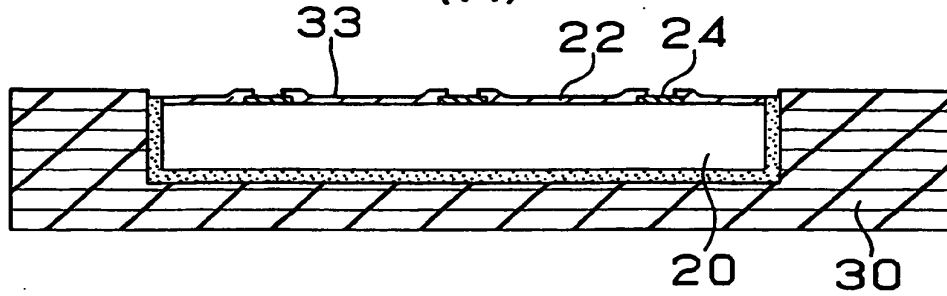
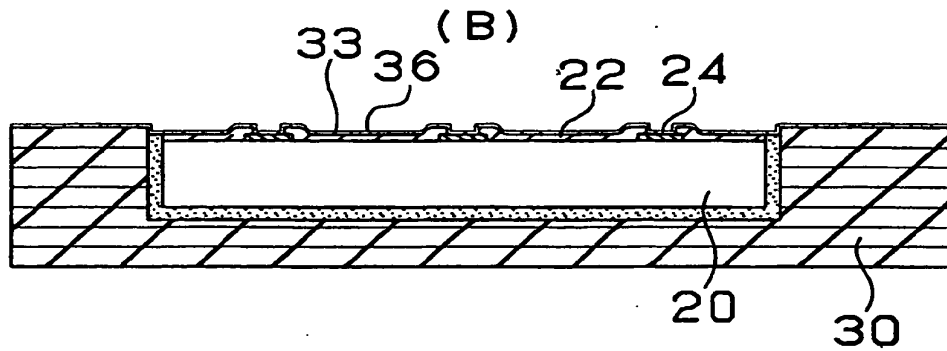


Fig. 2

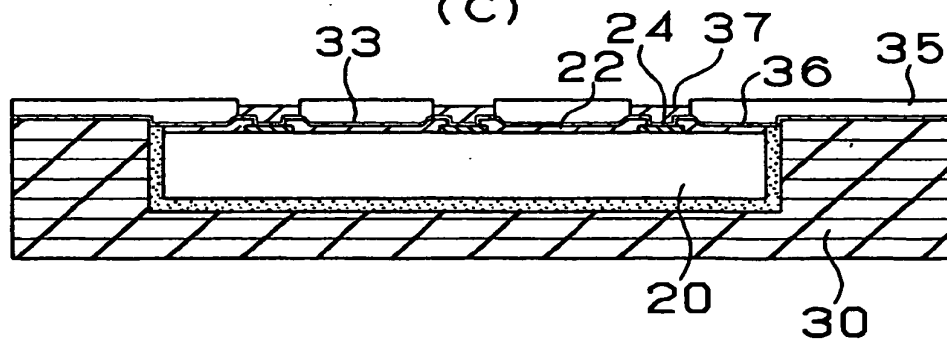
(A)



(B)



(C)



(D)

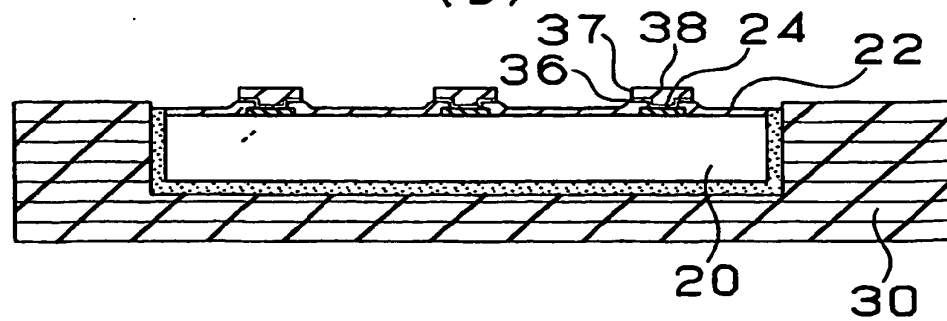


Fig. 3

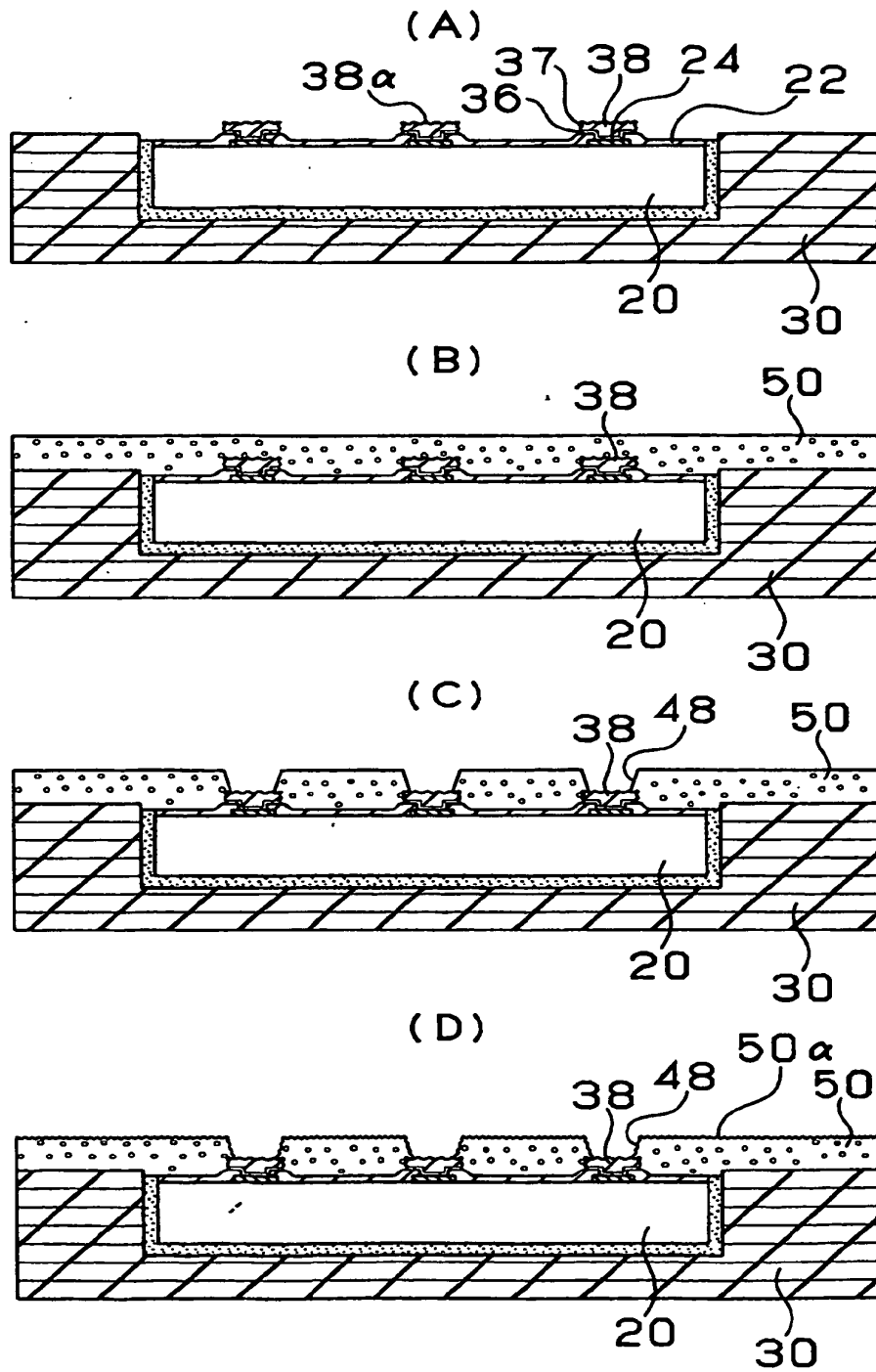
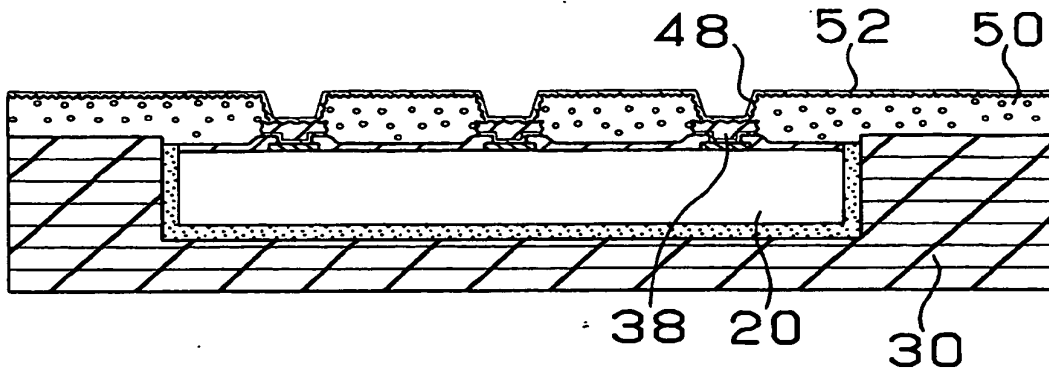
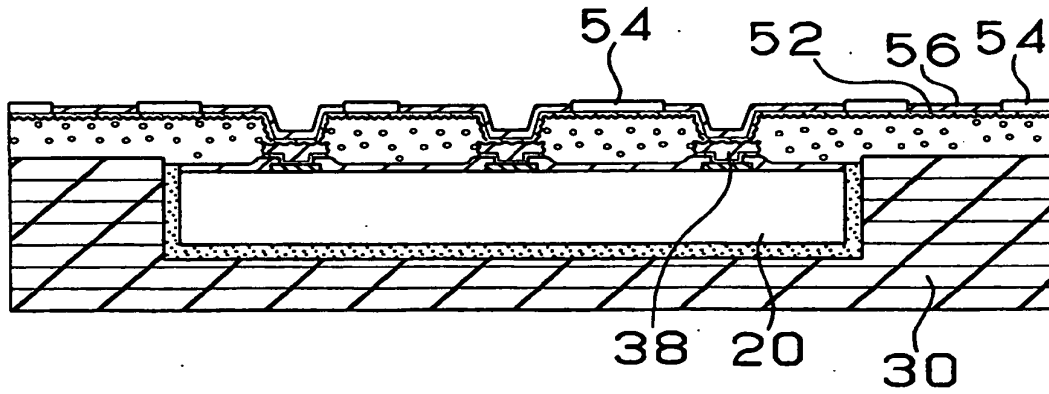


Fig. 4
(A)



(B)



(C)

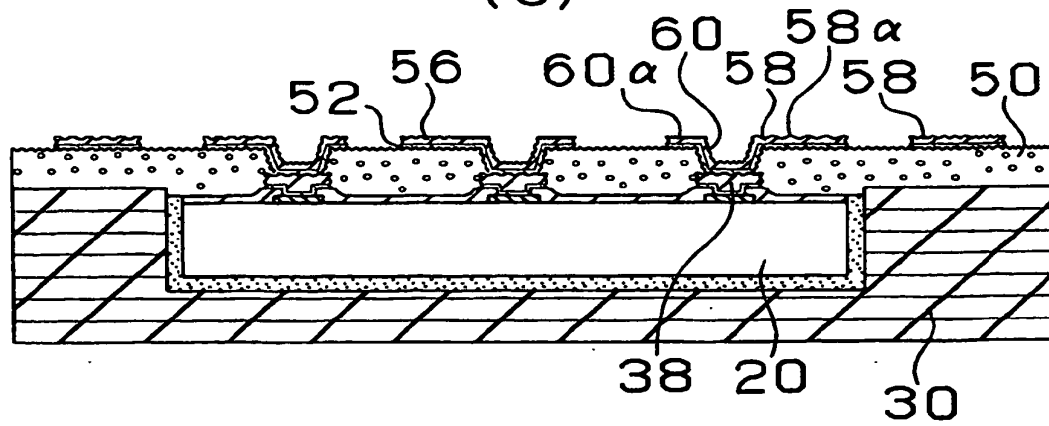
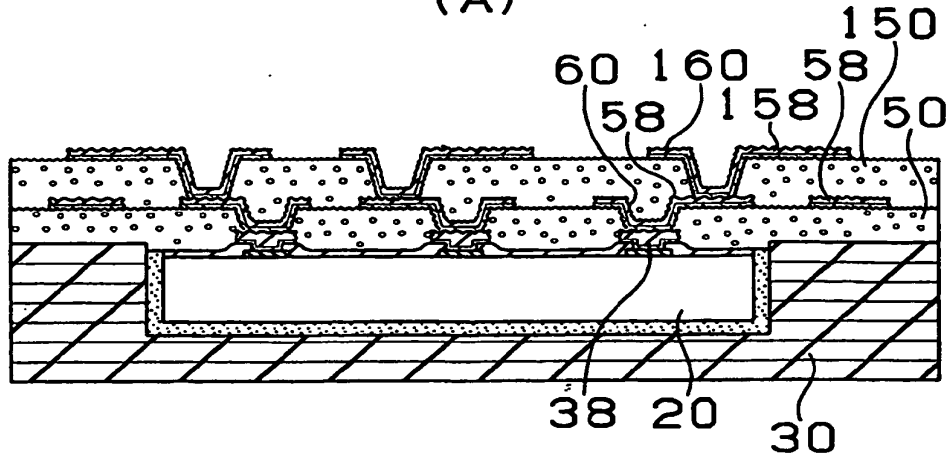
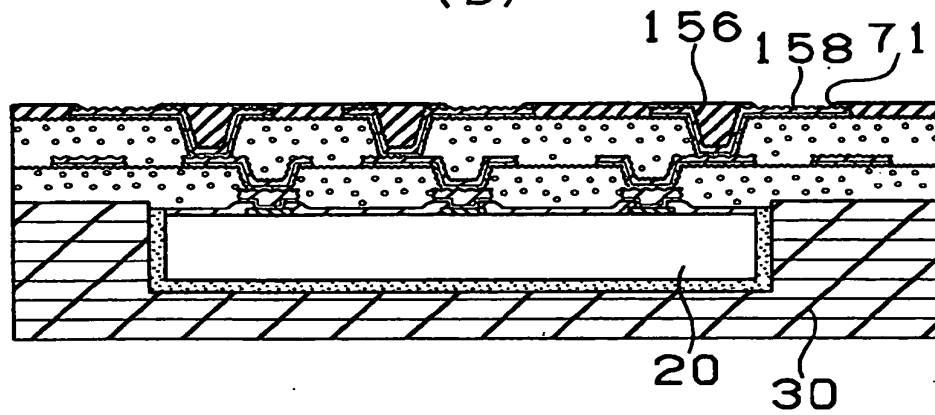


Fig. 5

(A)



(B)



(C)

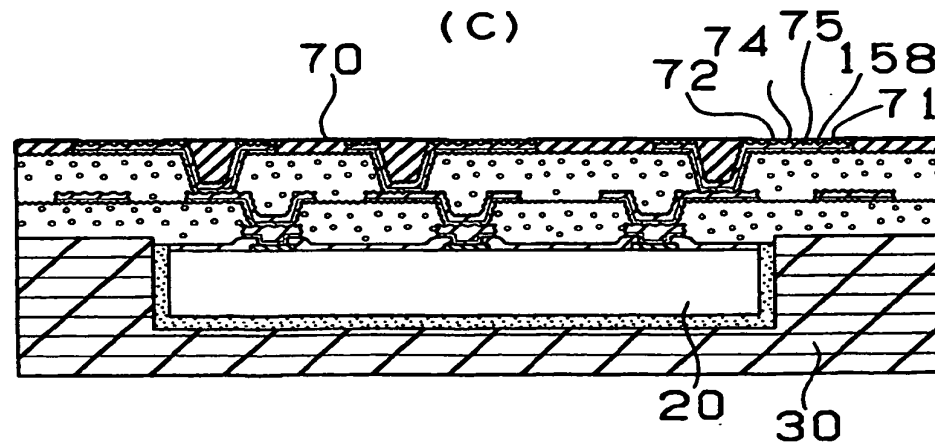


Fig. 6

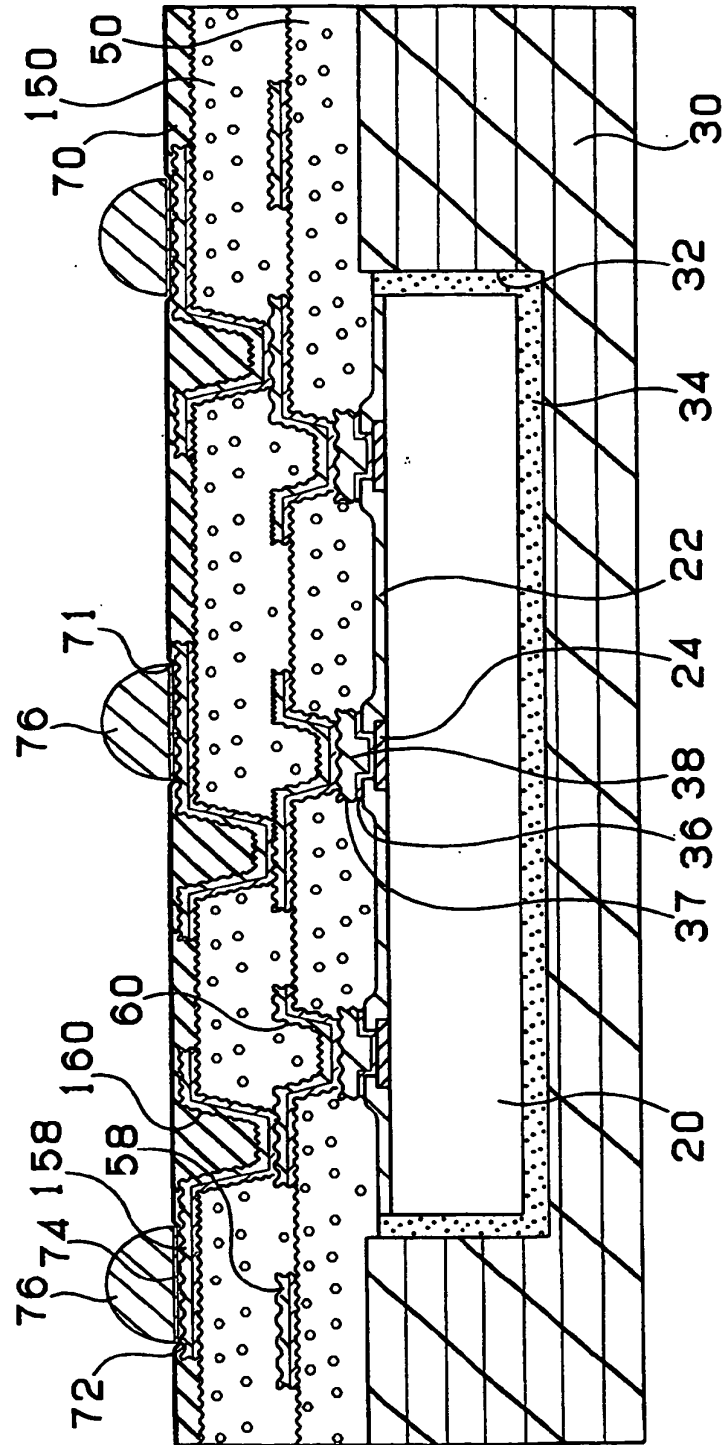
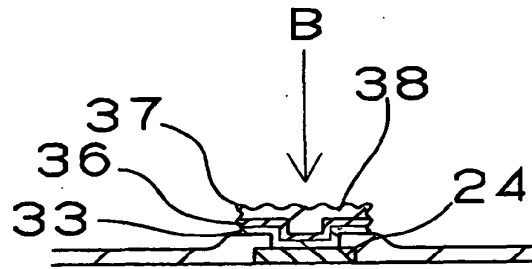
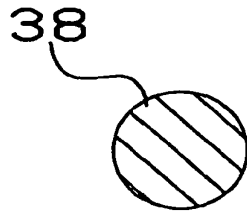


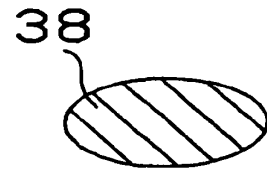
Fig. 7
(A)



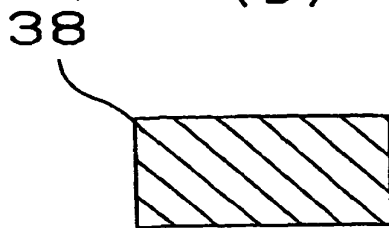
(B)



(C)



(D)



(E)

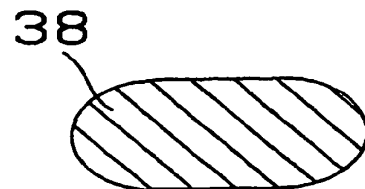
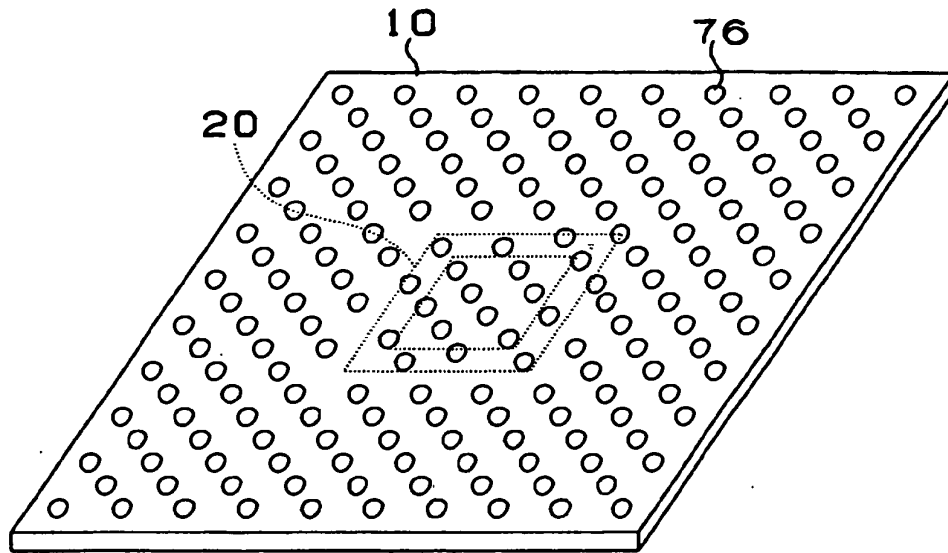


Fig. 8

(A)



(B)

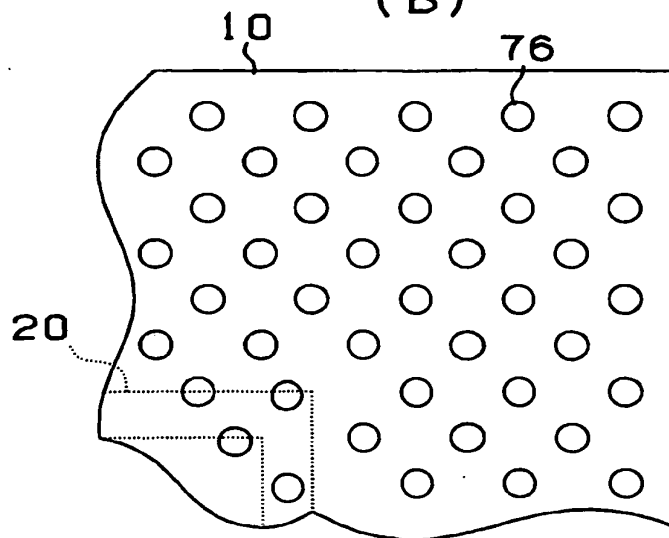
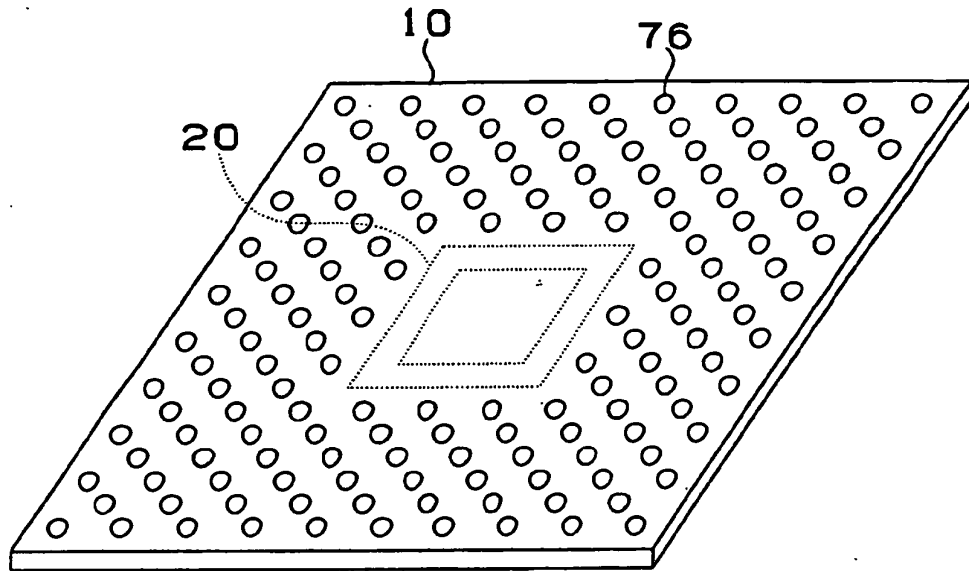


Fig. 9

(A)



(B)

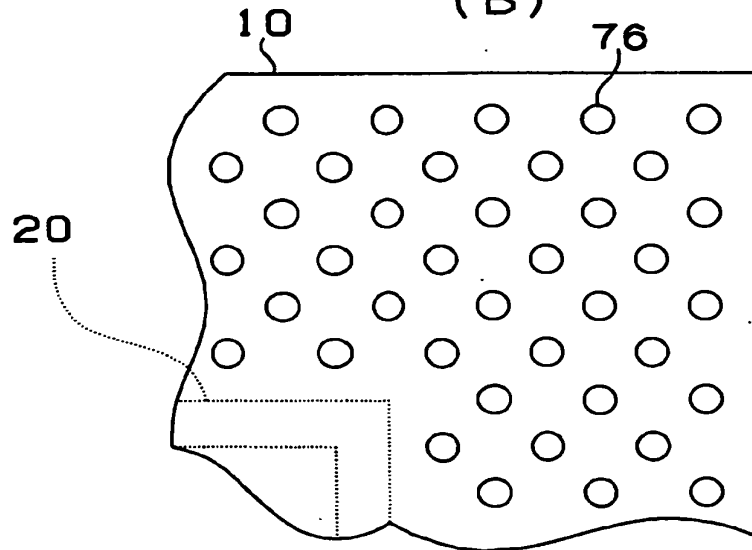


Fig. 10

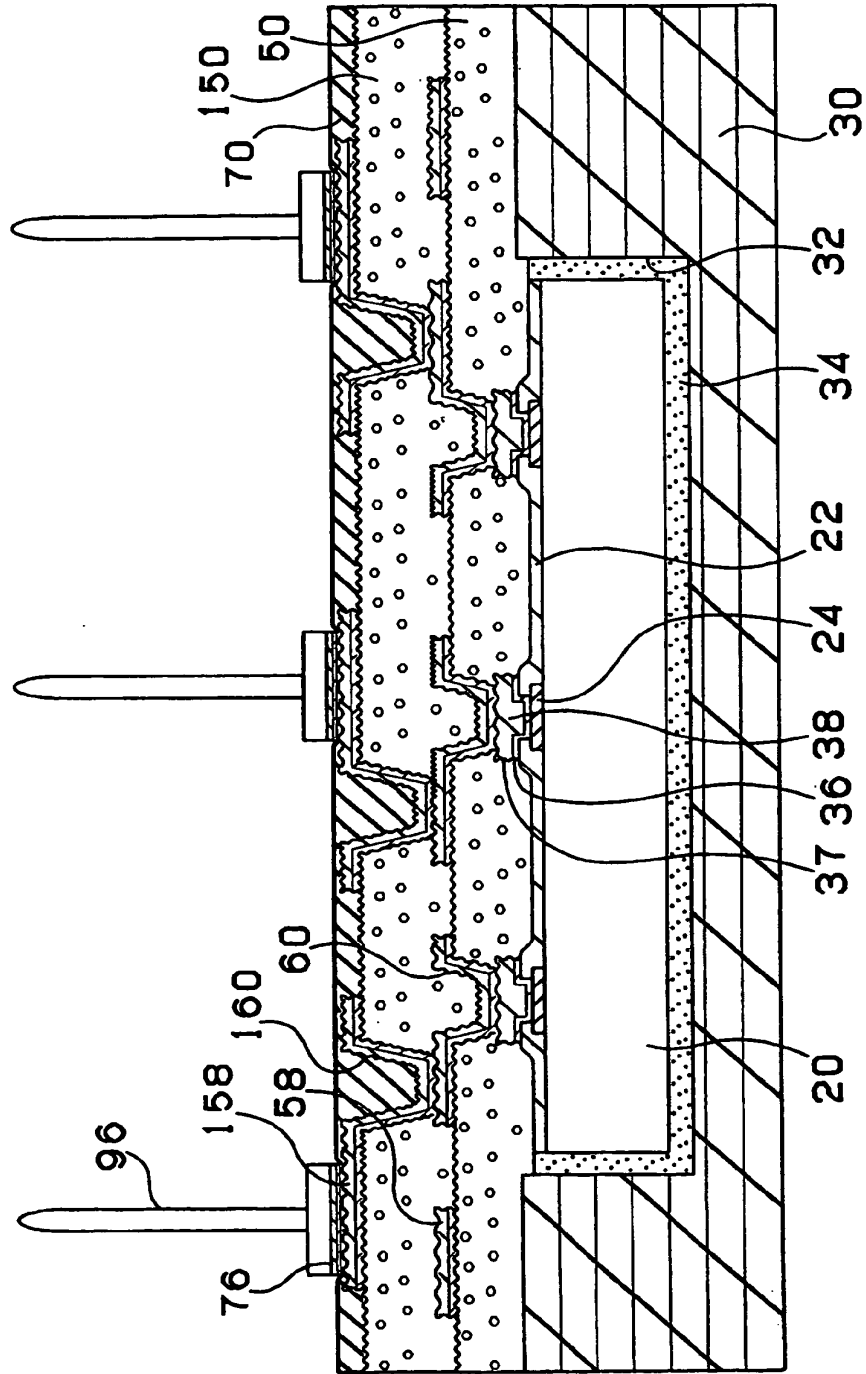


Fig. 11

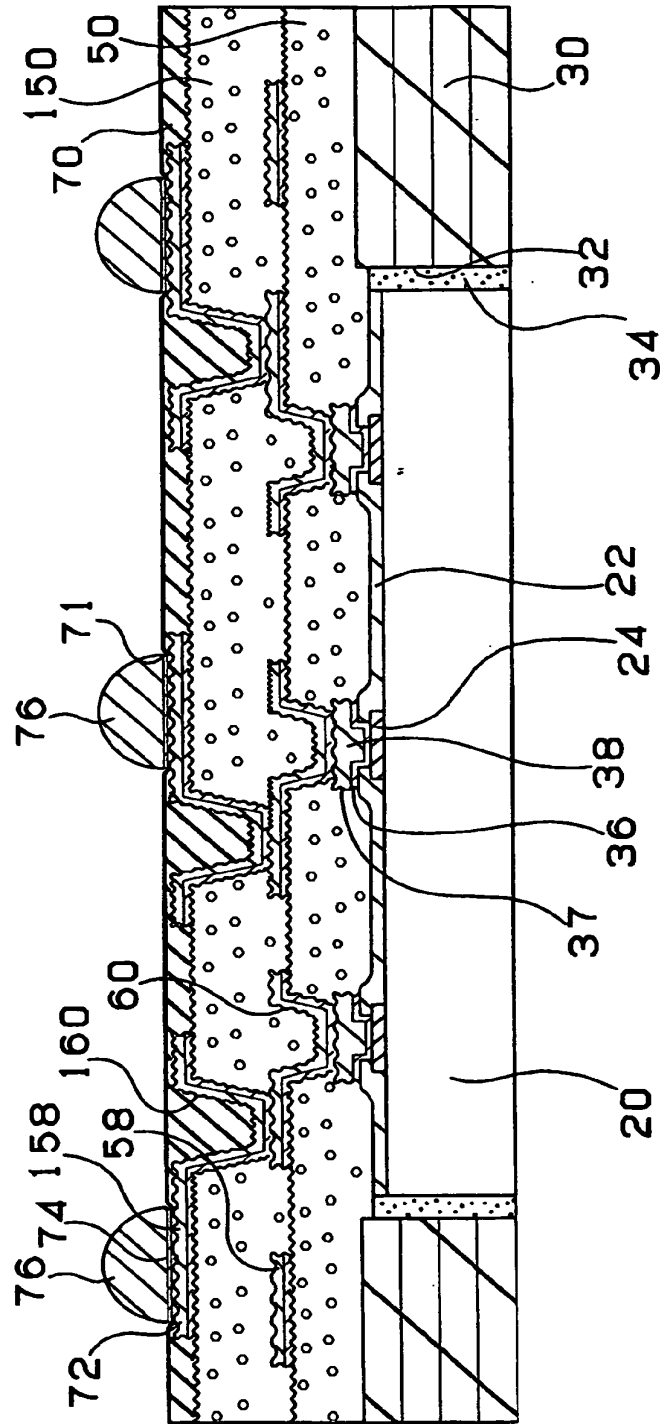


Fig. 12

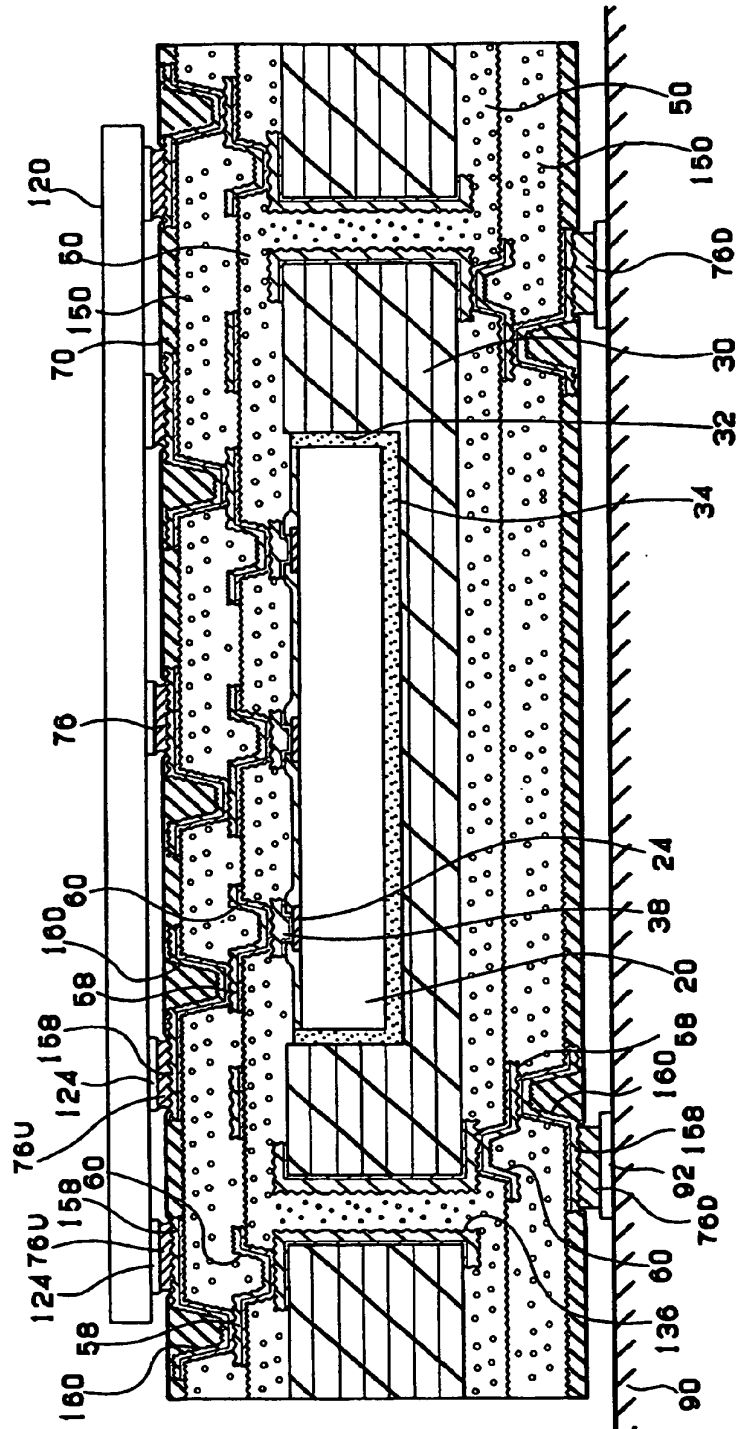


Fig. 13

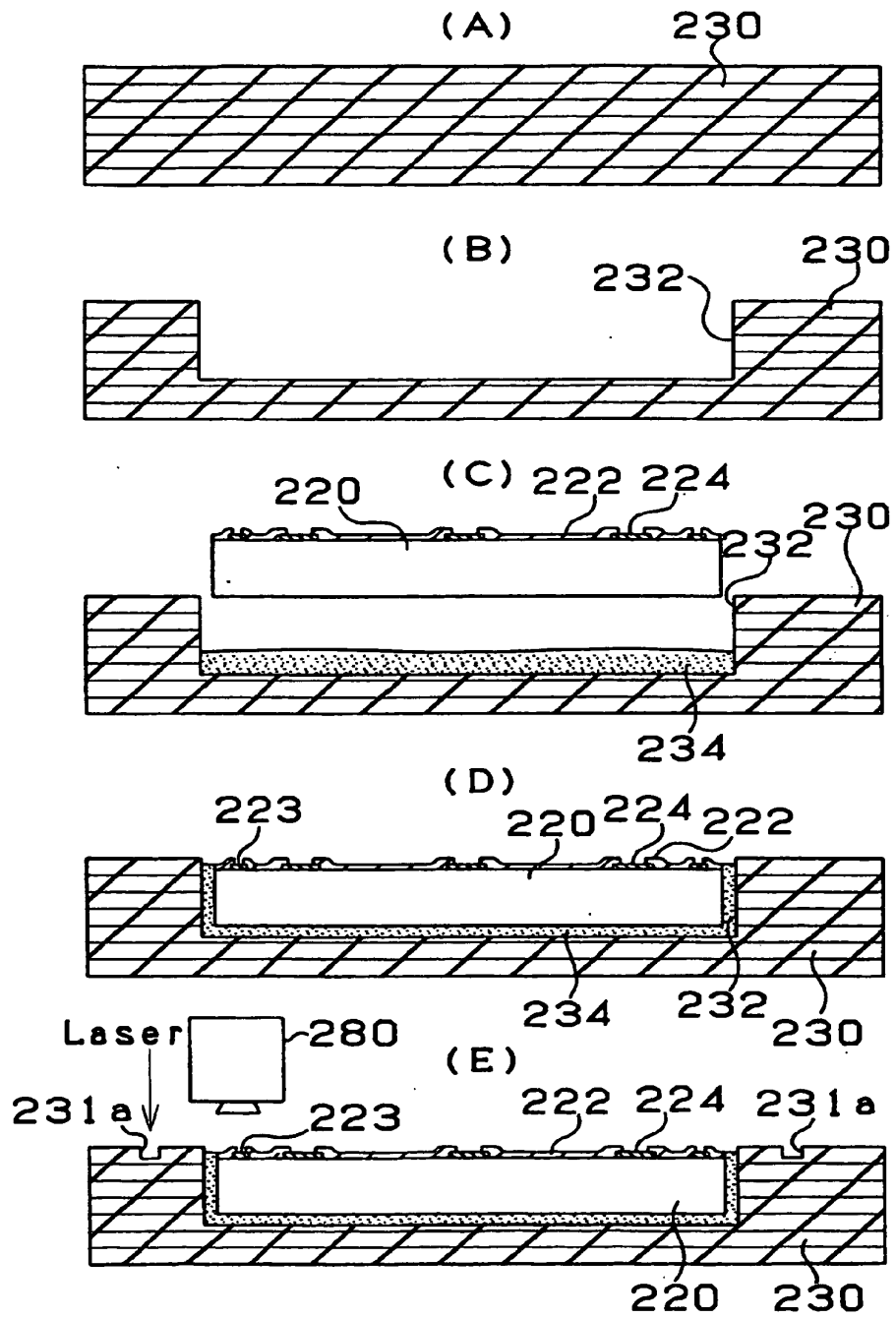


Fig. 14

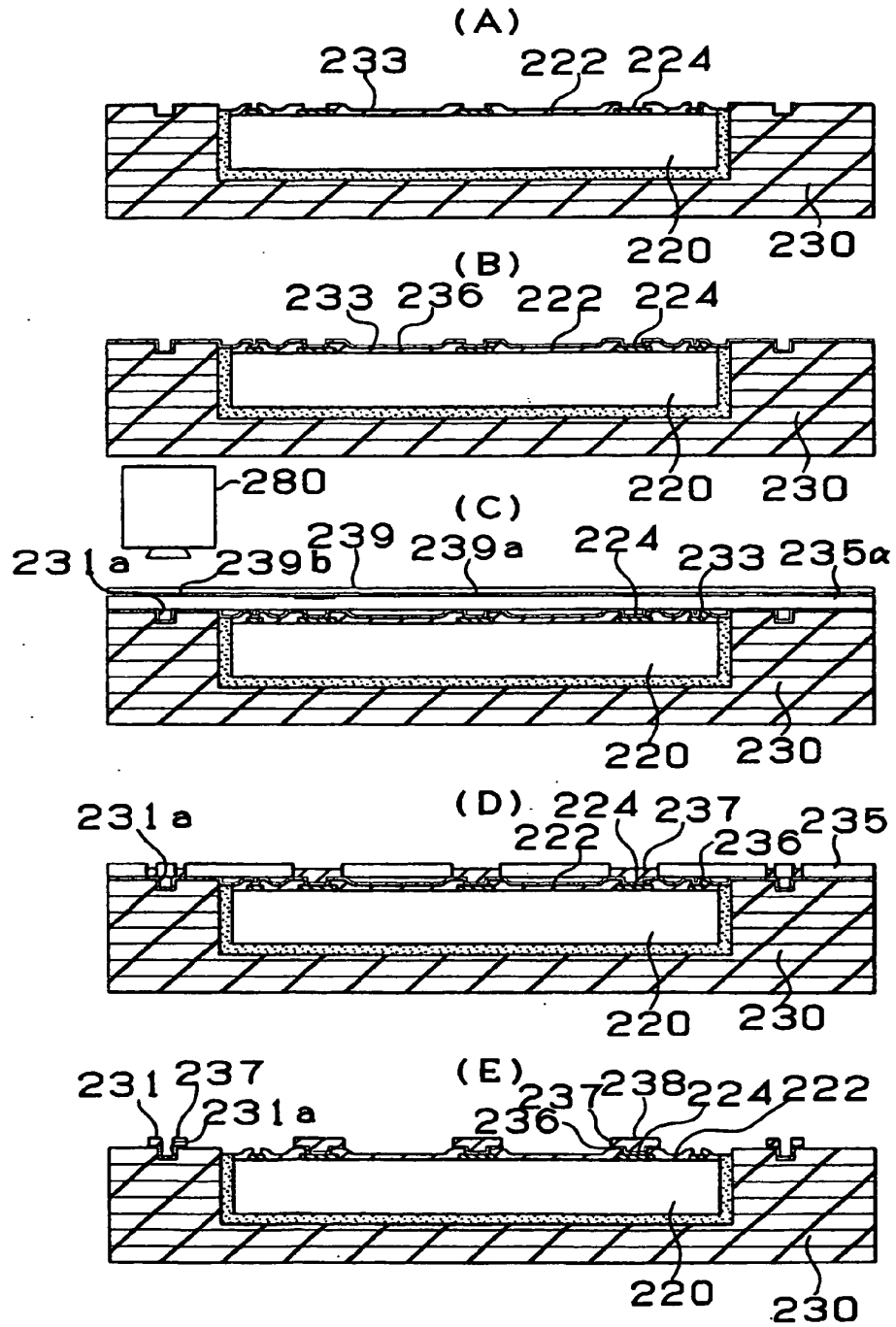


Fig. 15

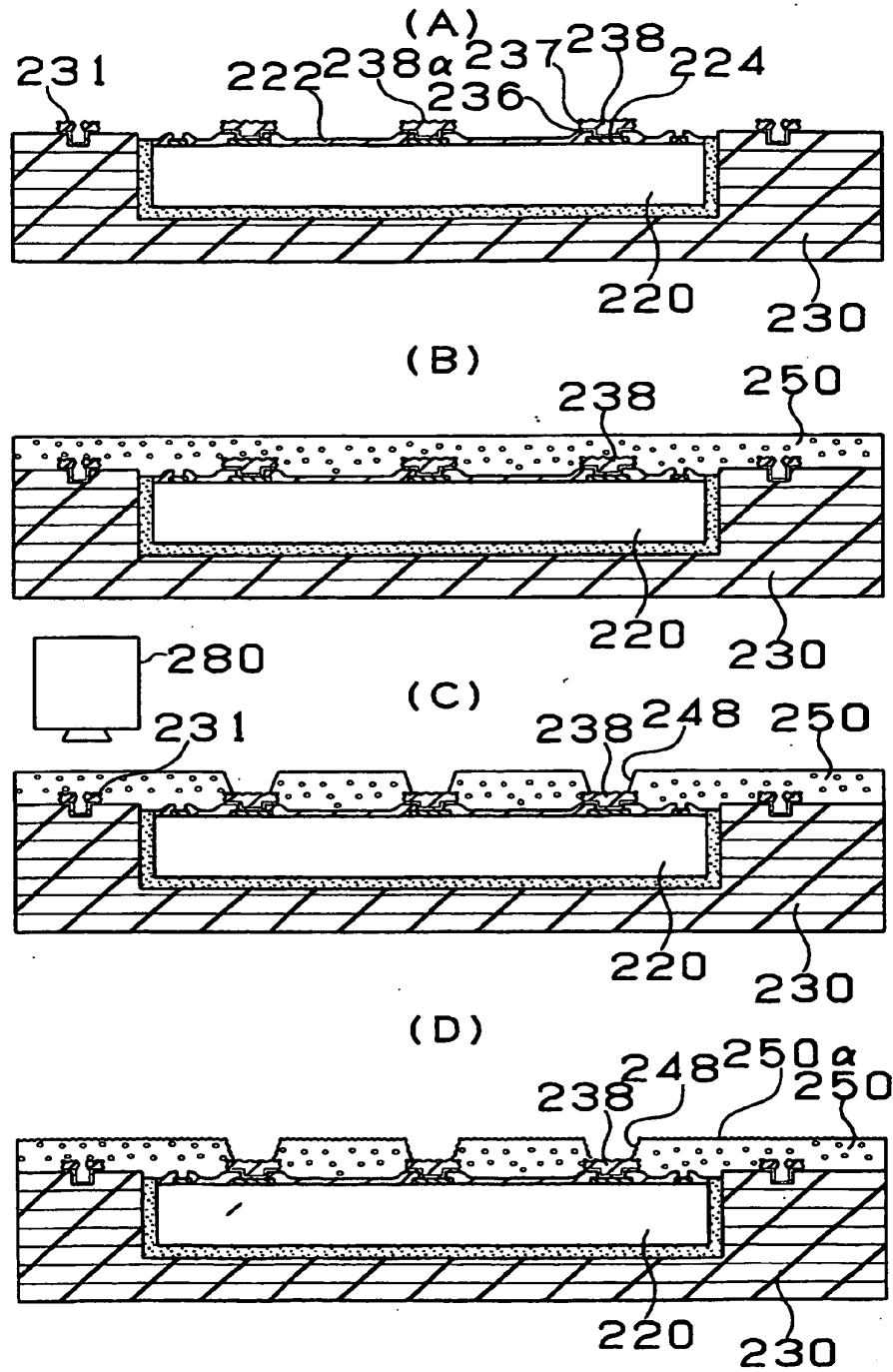


Fig. 16

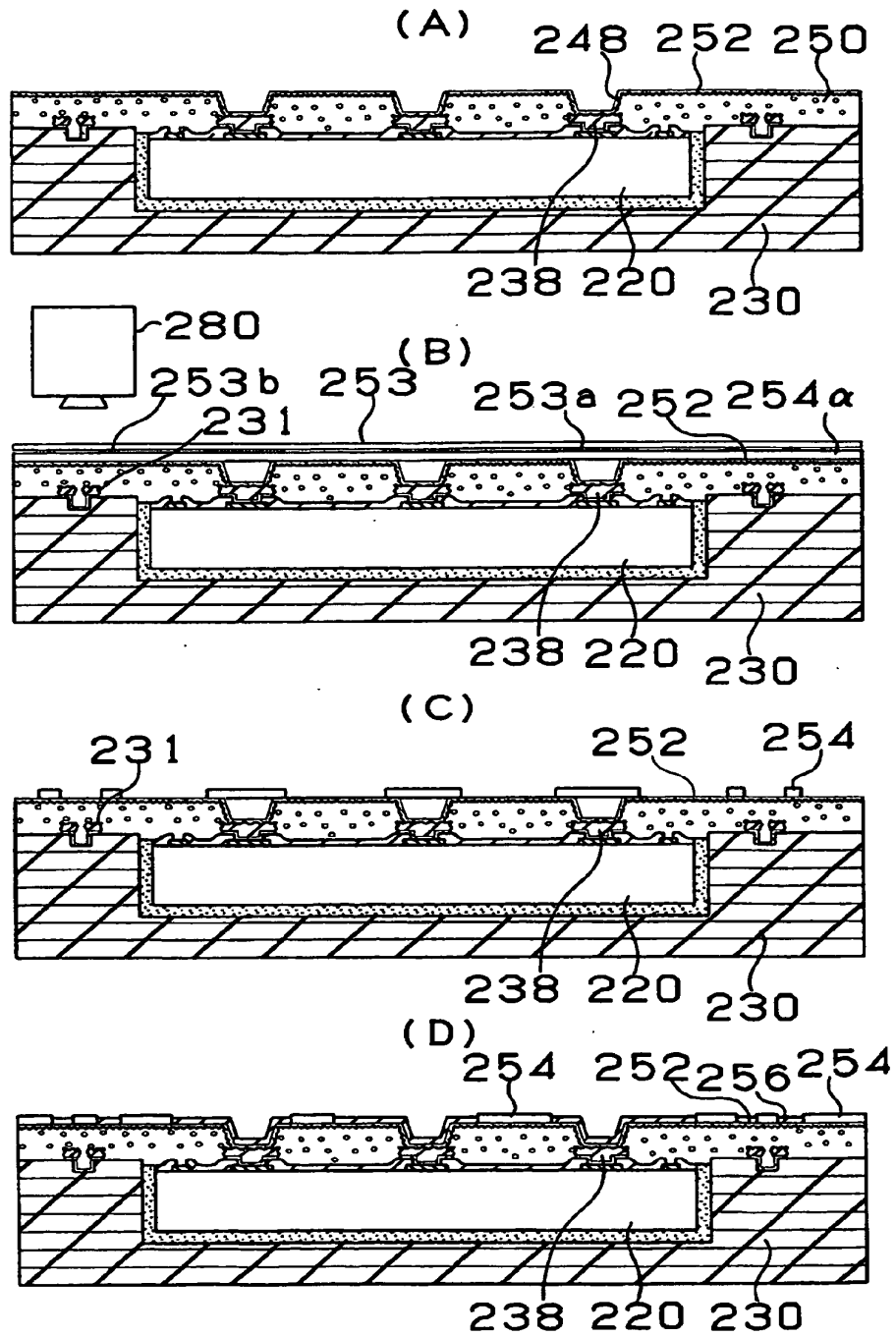


Fig. 17

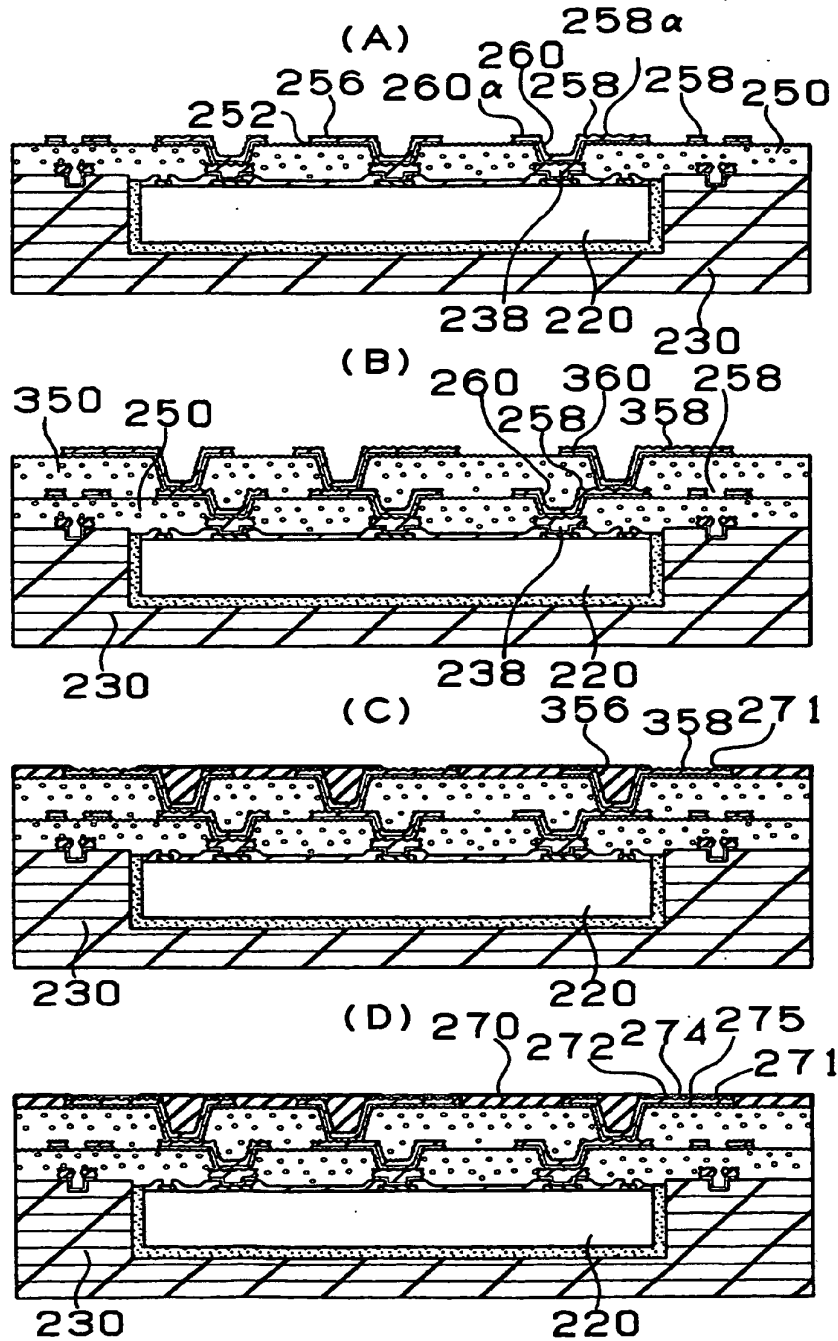


Fig. 18

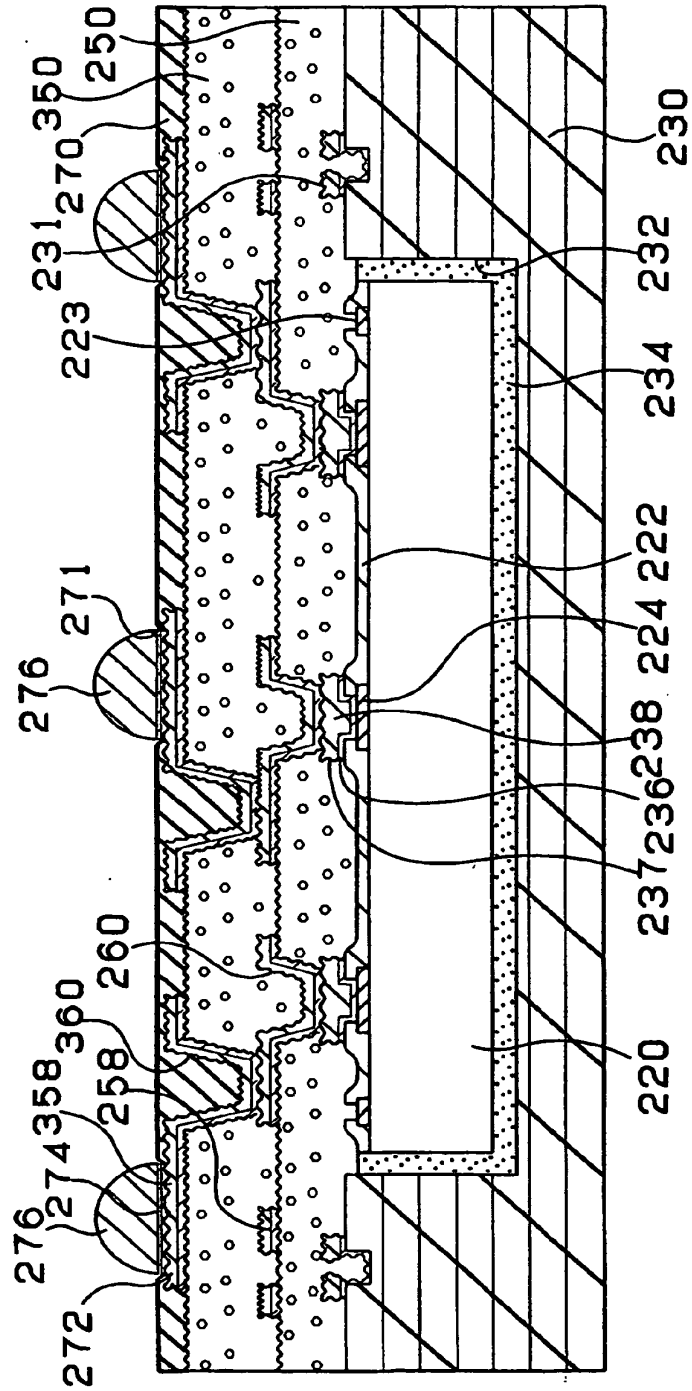
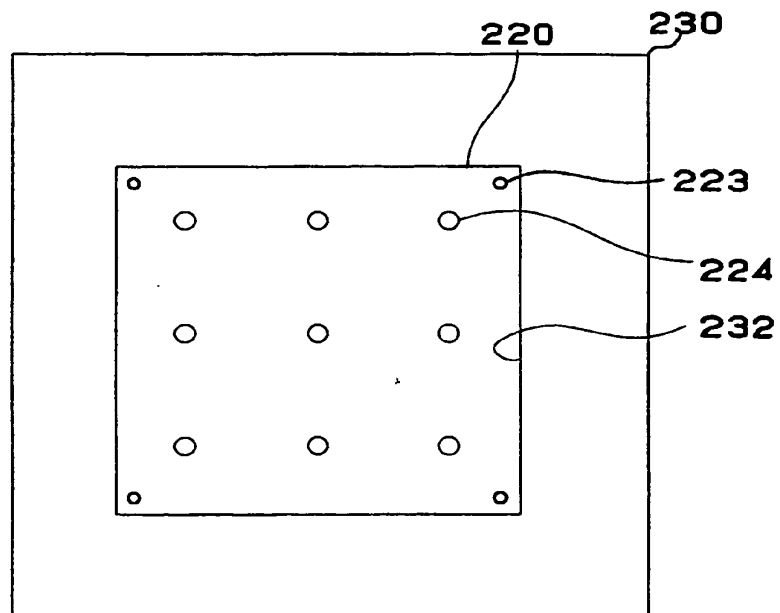


Fig. 19

(A)



(B)

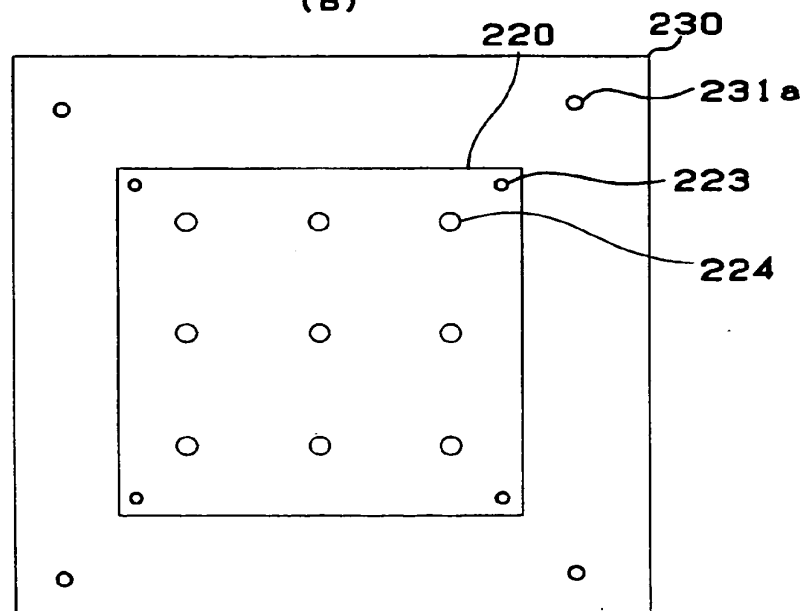
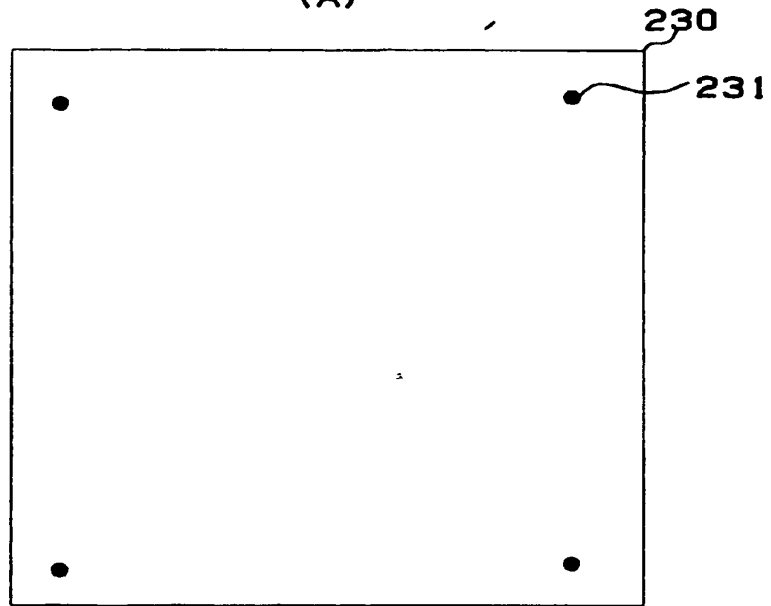


Fig. 20

(A)



(B)

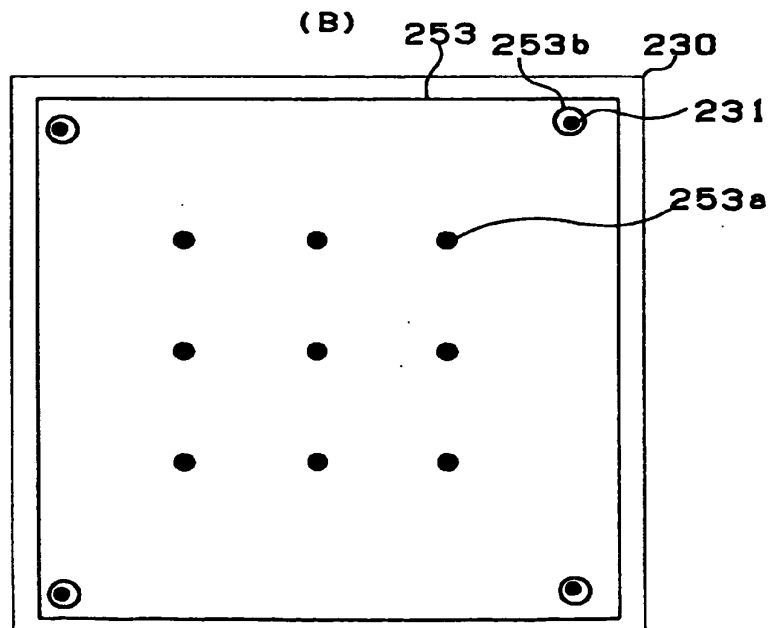


Fig. 21

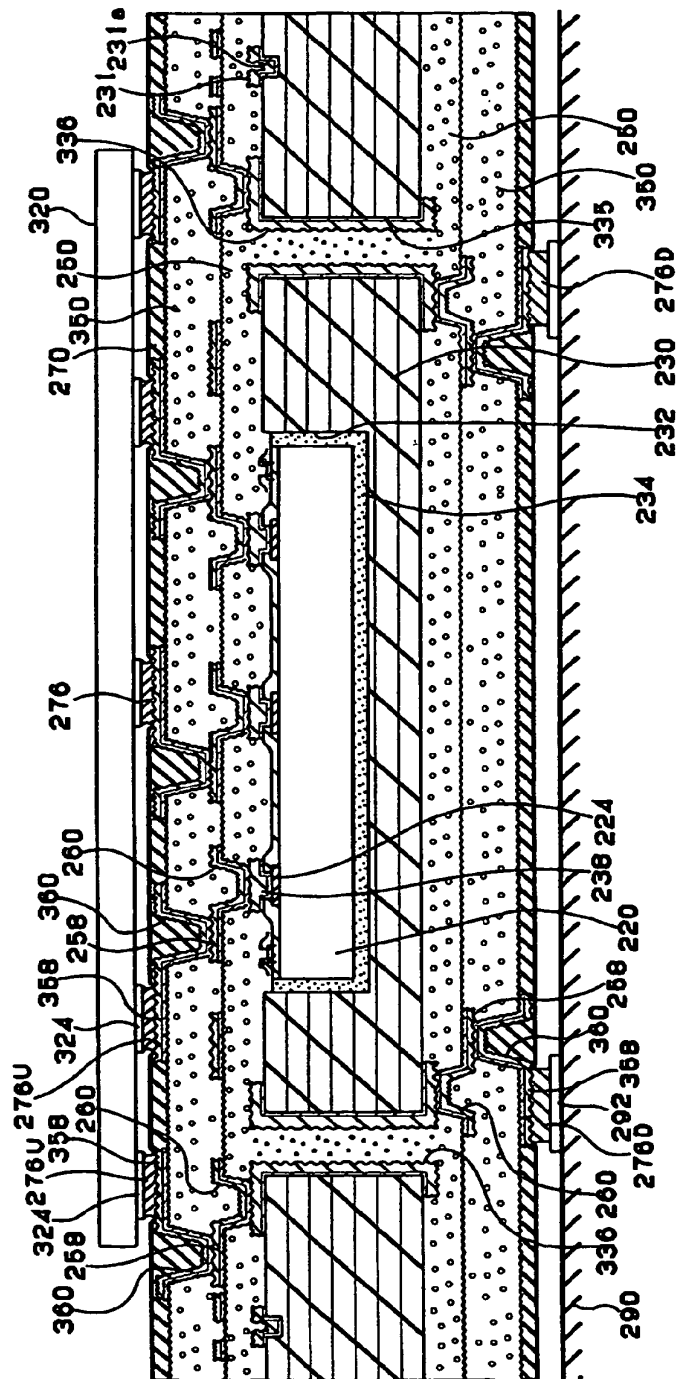
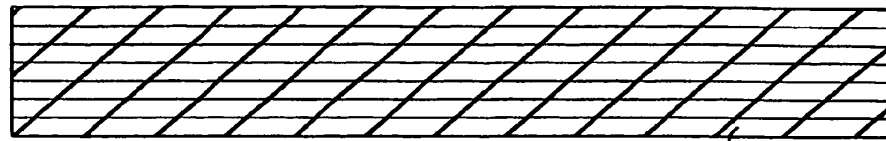
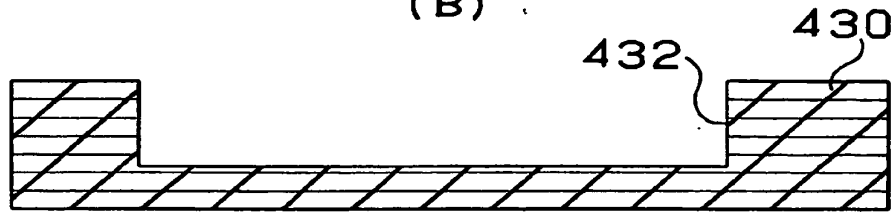


Fig. 22
(A)



430

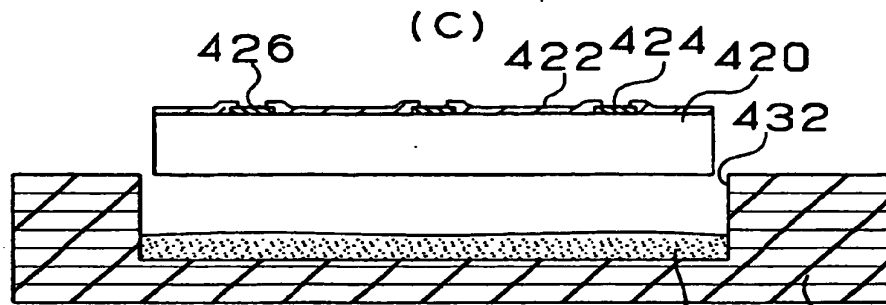
(B)



432

430

(C)



426

422

424

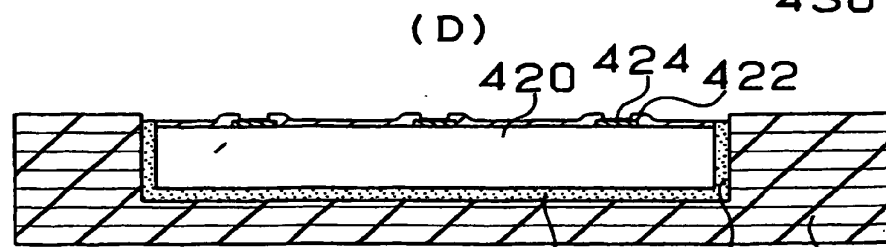
420

432

434

430

(D)



420

424

422

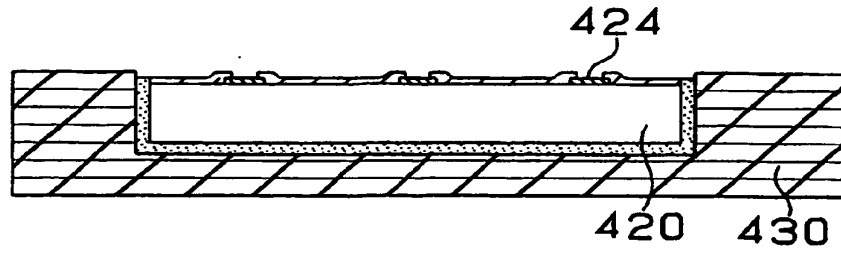
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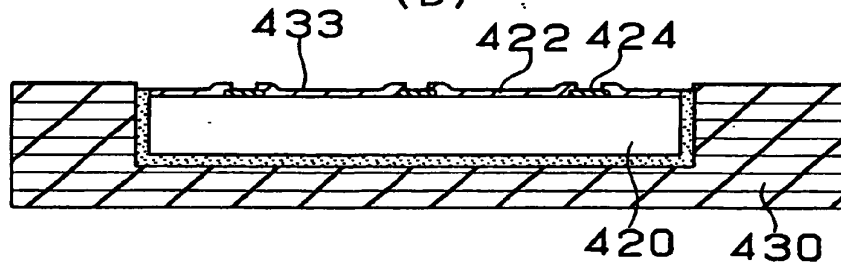
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Fig. 23

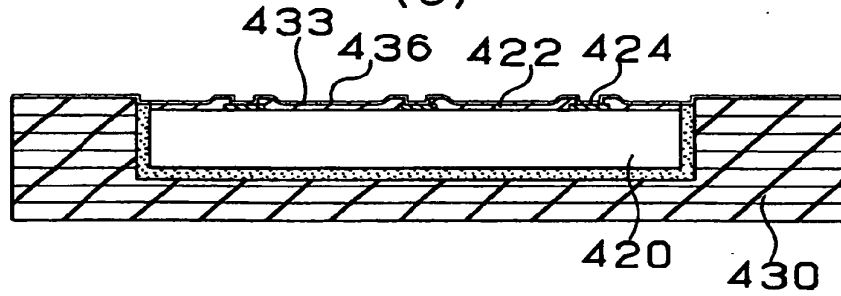
(A)



(B)



(C)



(D)

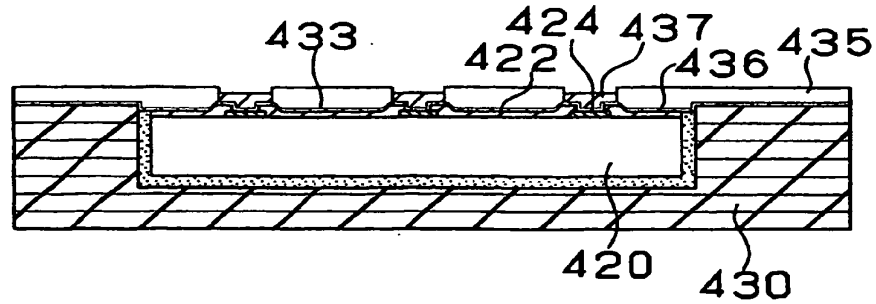
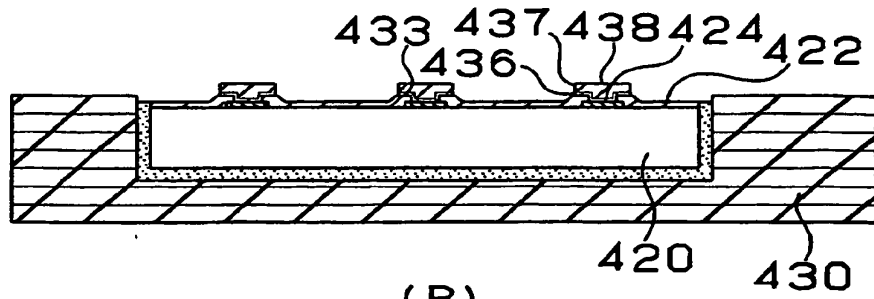
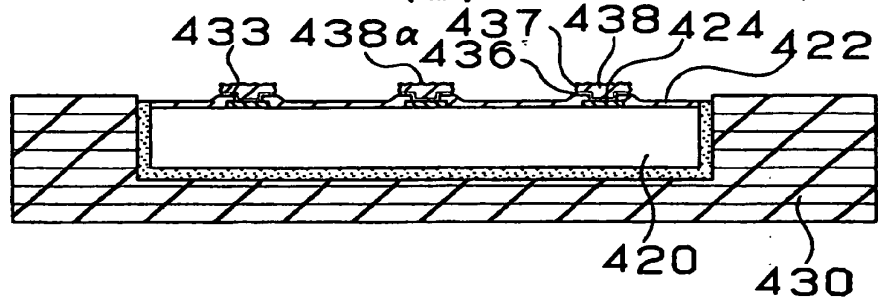


Fig. 24

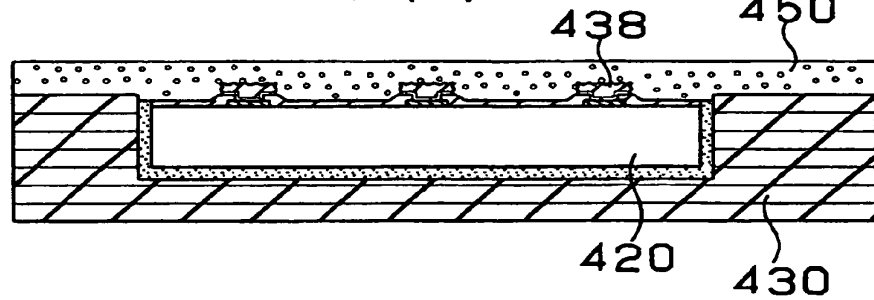
(A)



(B)



(C)



(D)

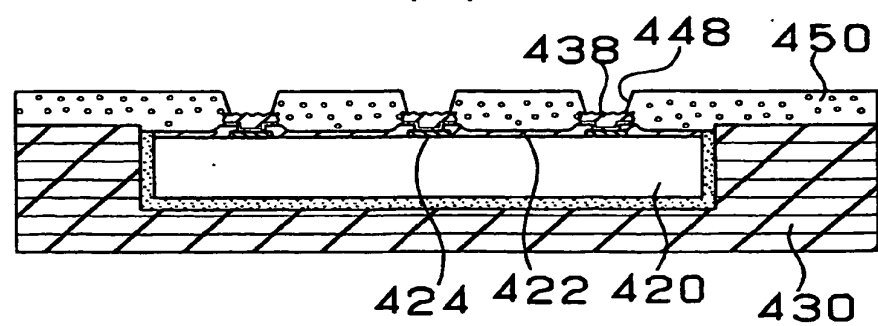
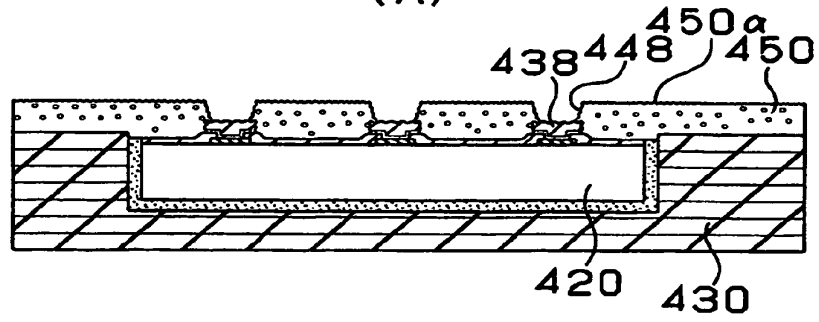
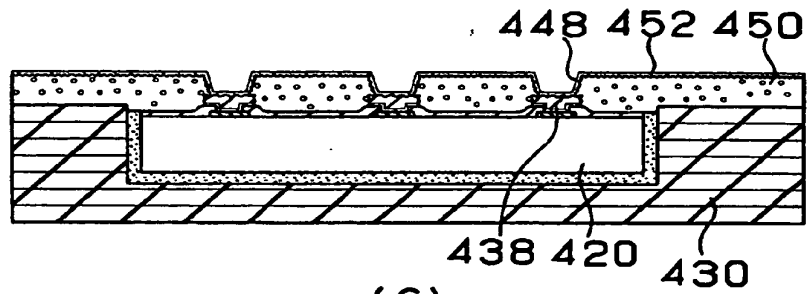


Fig. 25

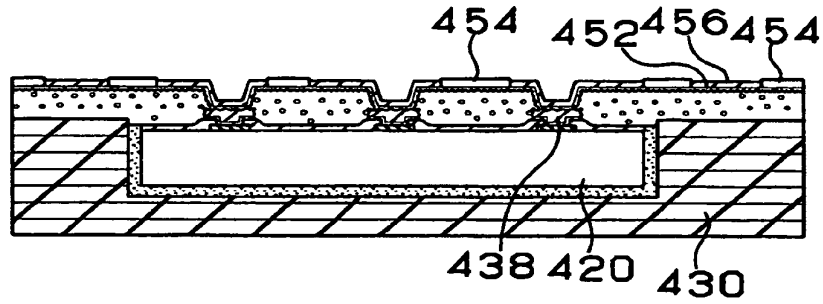
(A)



(B)



(C)



(D)

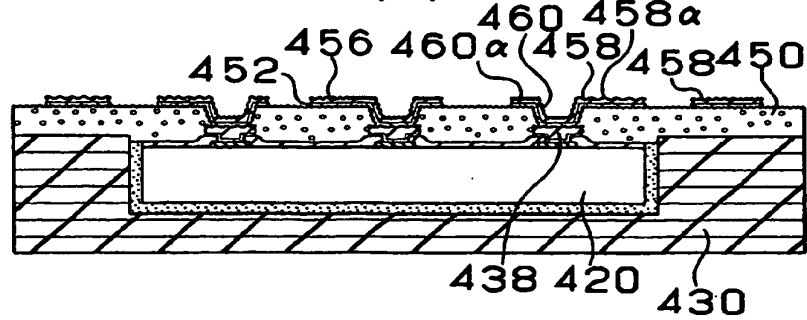


Fig. 26

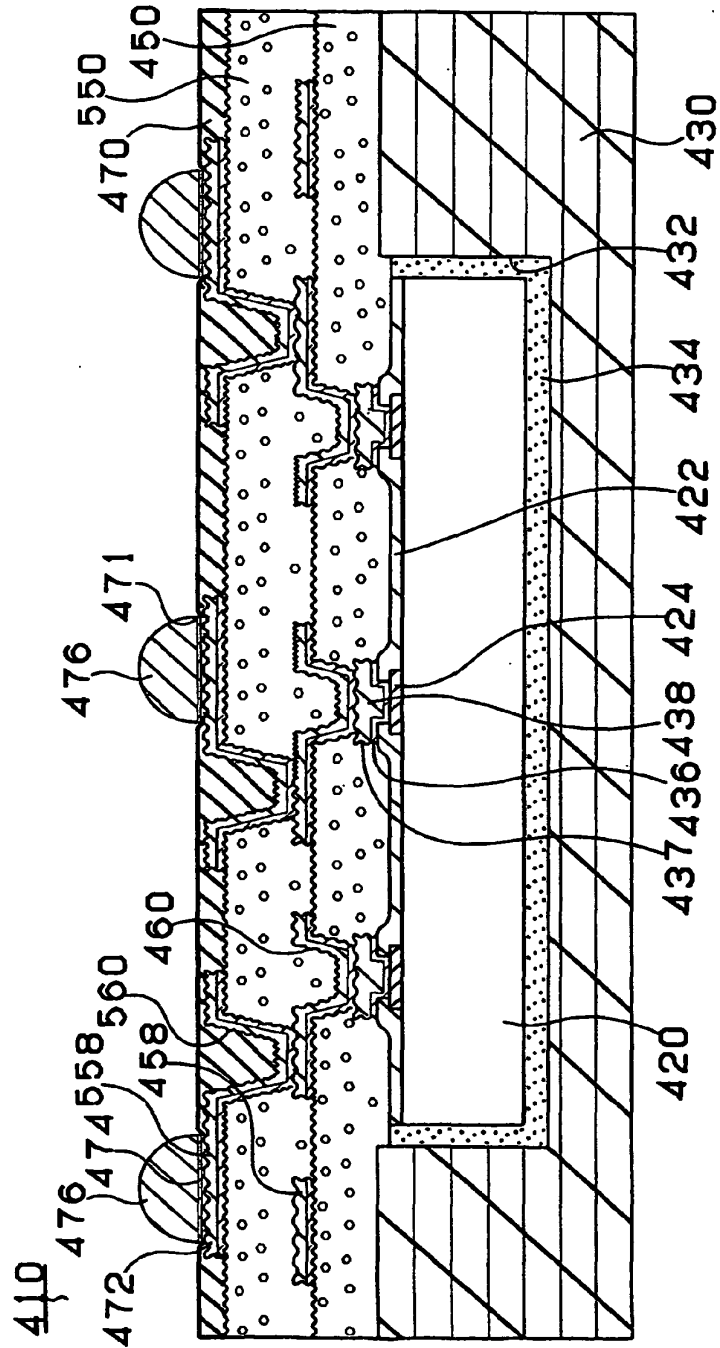
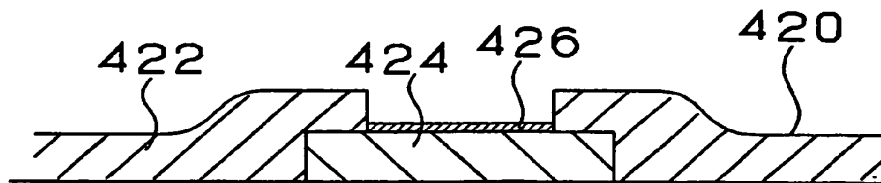
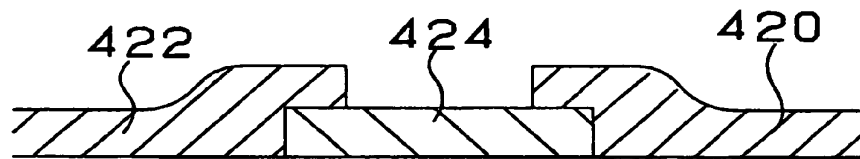


Fig. 27

(A)



(B)



(C)

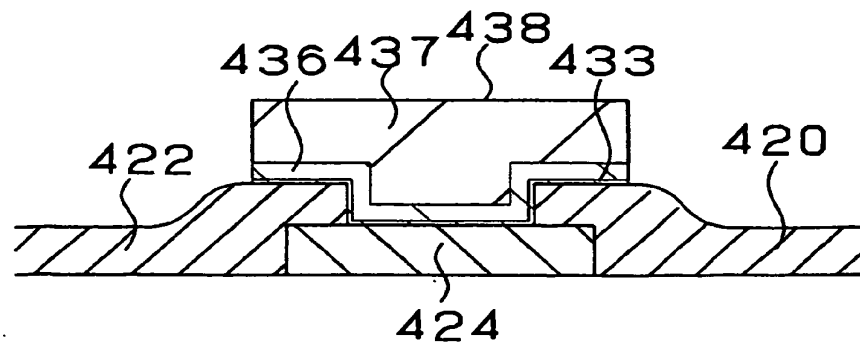


Fig. 28

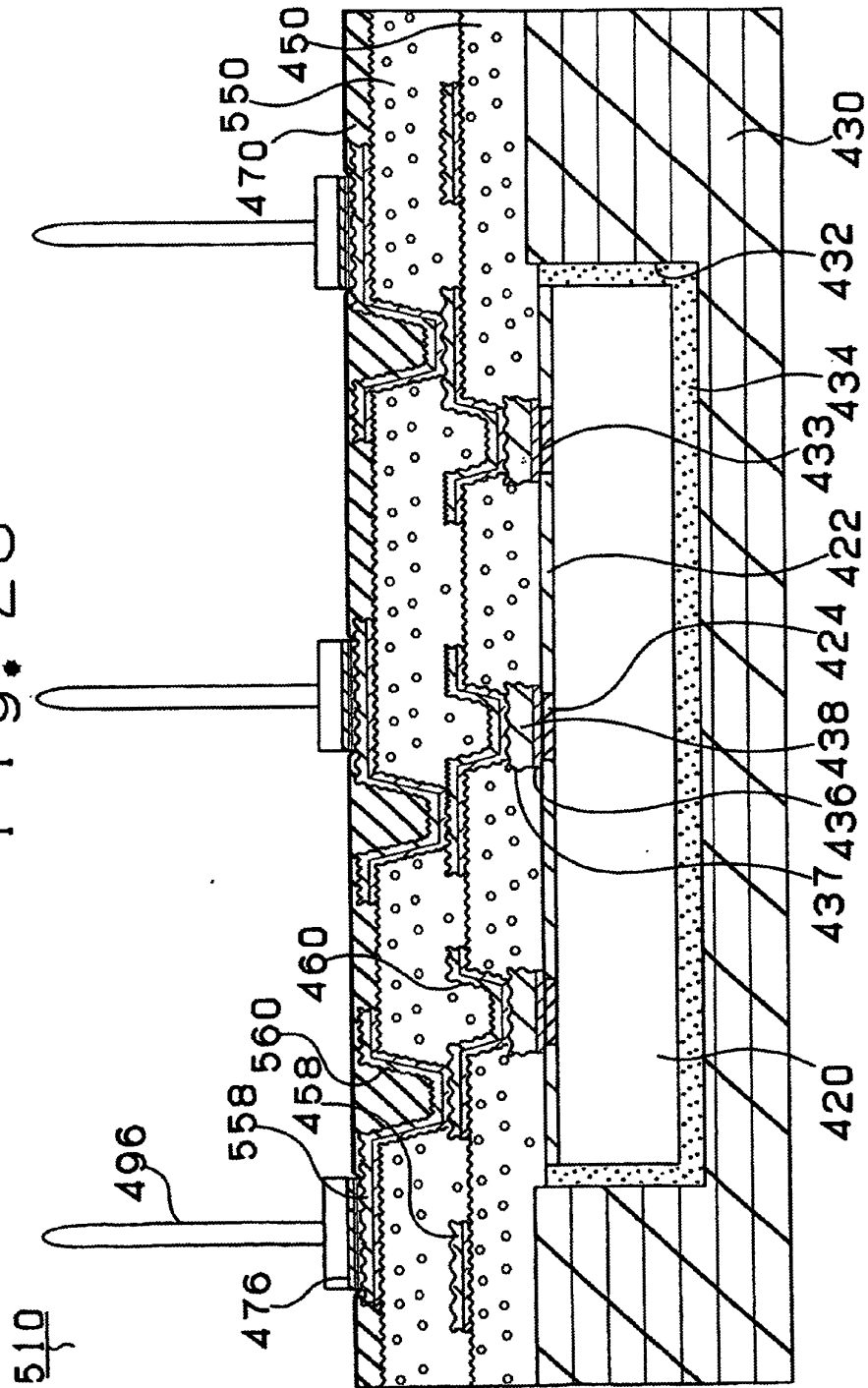
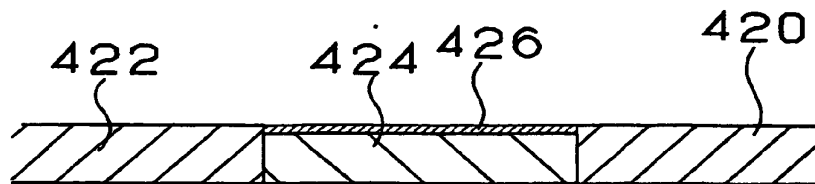
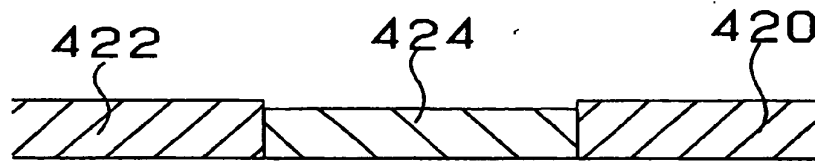


Fig. 29

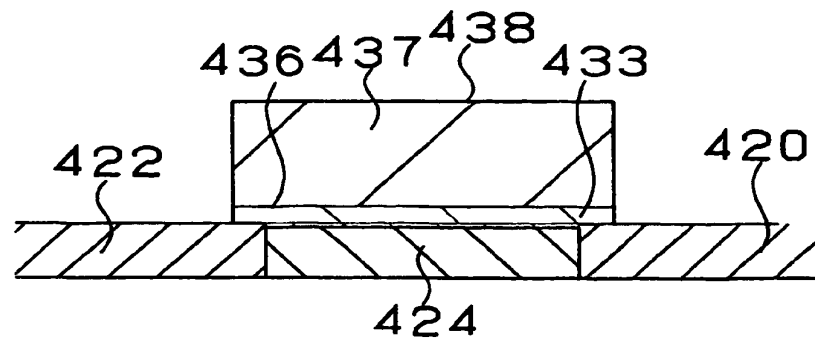
(A)



(B)



(C)



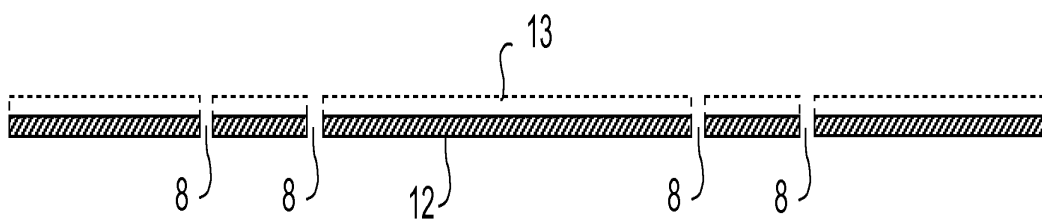


Fig. 1

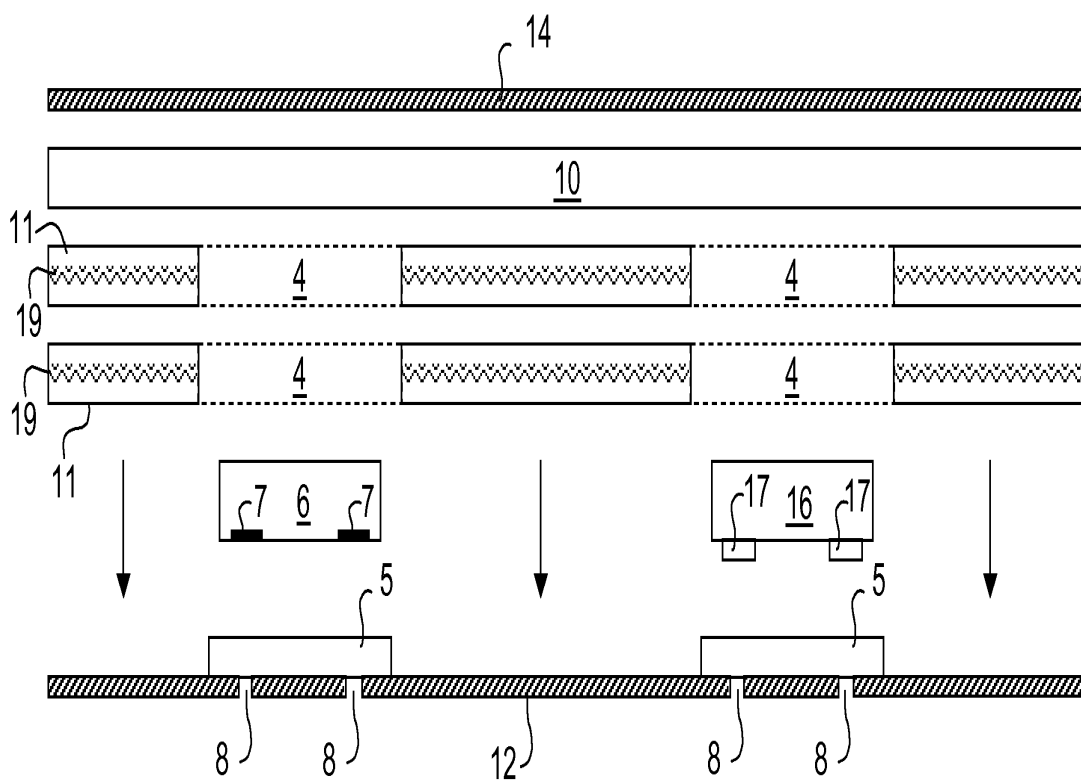


Fig. 2

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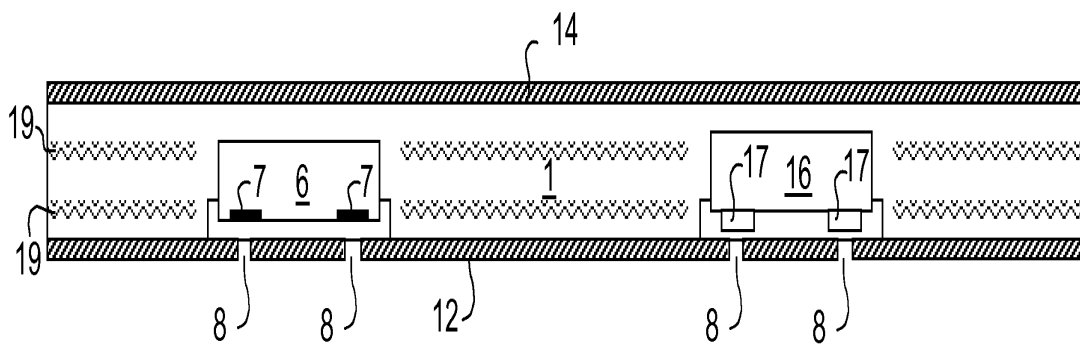


Fig. 3

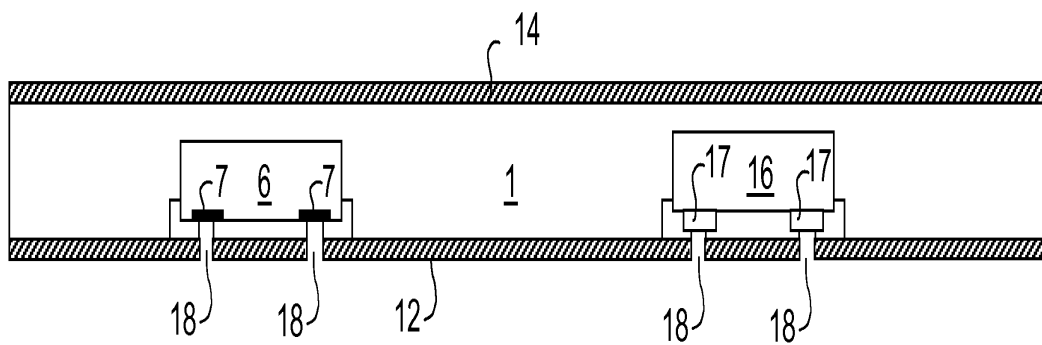


Fig. 4

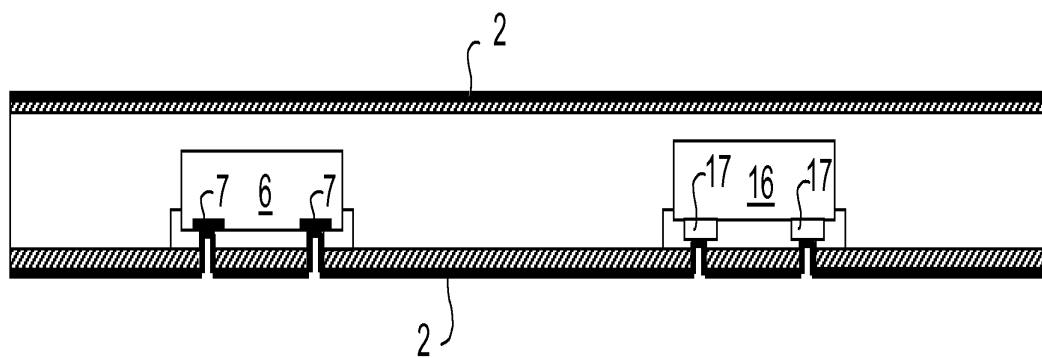


Fig. 5

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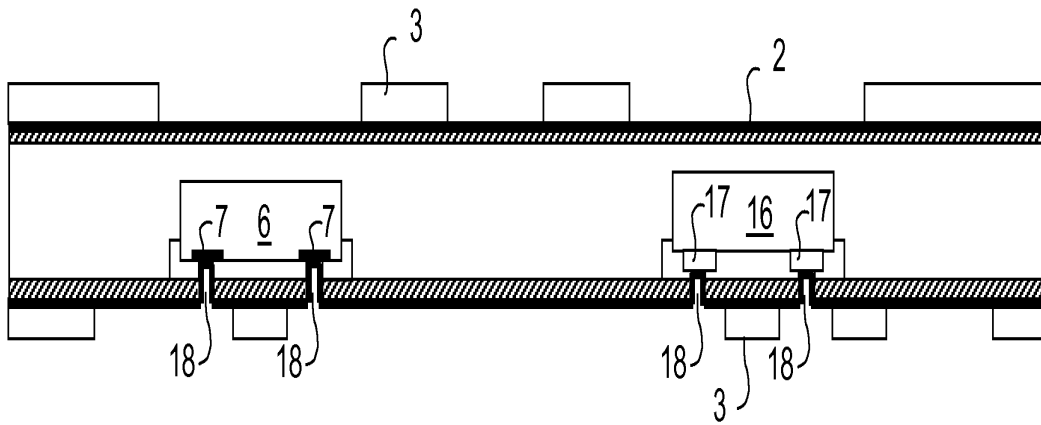


Fig. 6

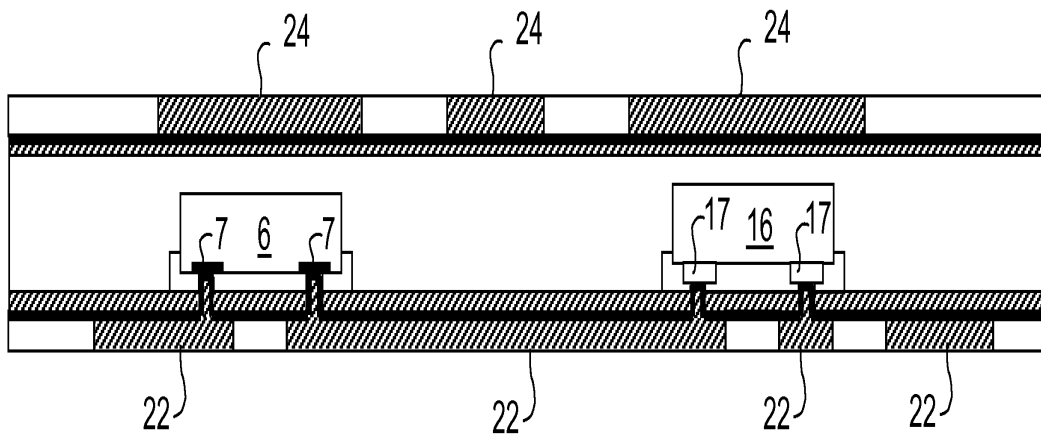


Fig. 7

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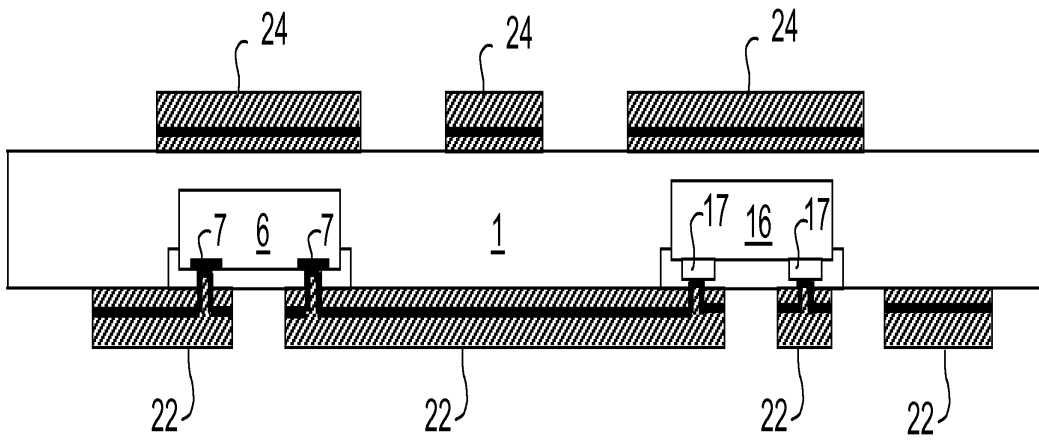


Fig. 8

4/15

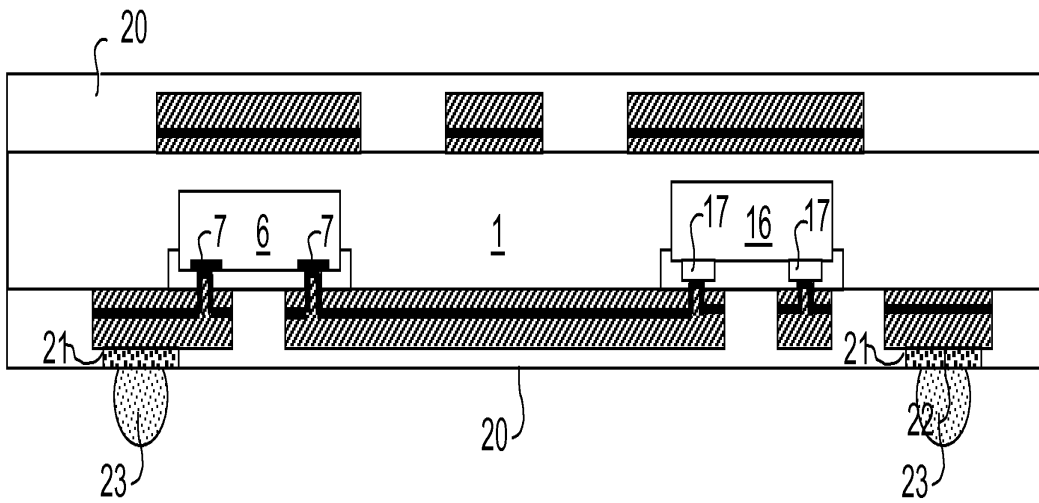


Fig. 9

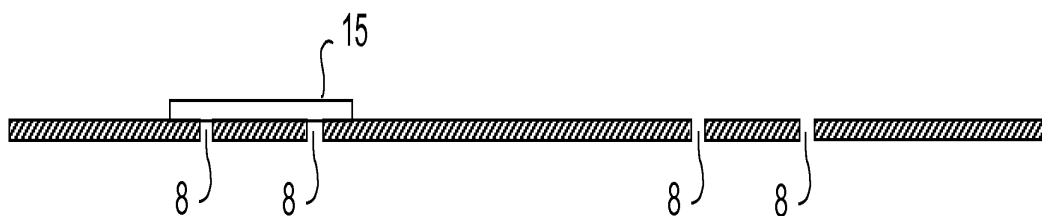


Fig. 10

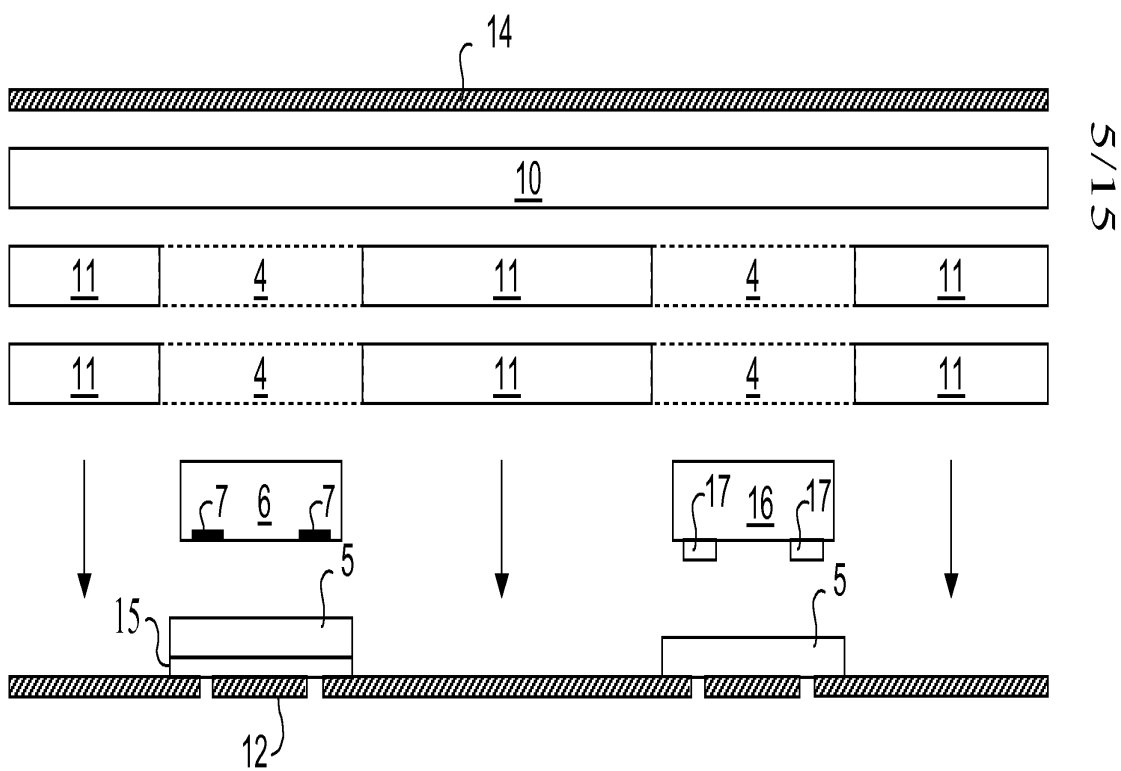


Fig. 11

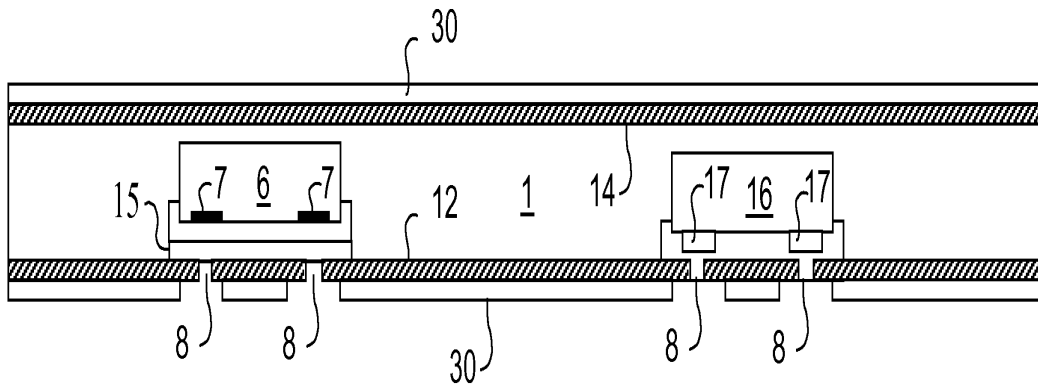


Fig. 12

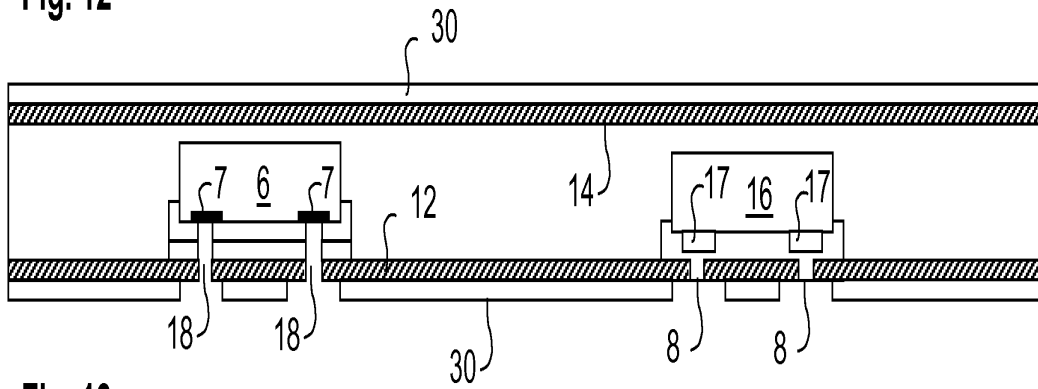


Fig. 13

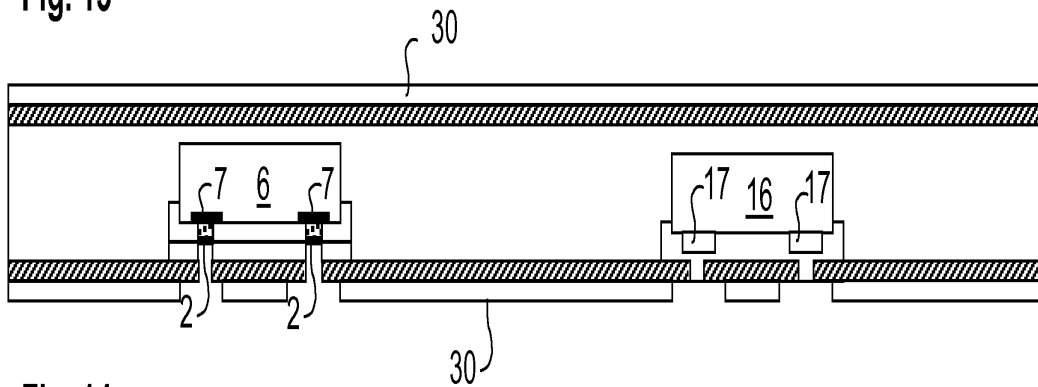


Fig. 14

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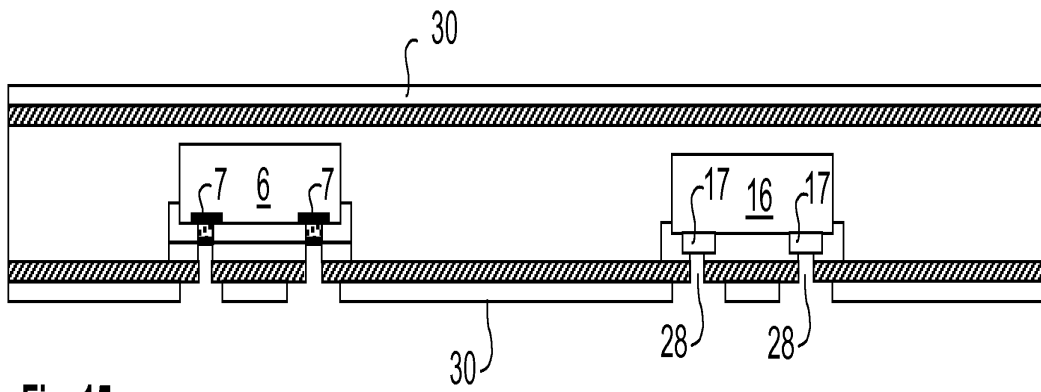


Fig. 15

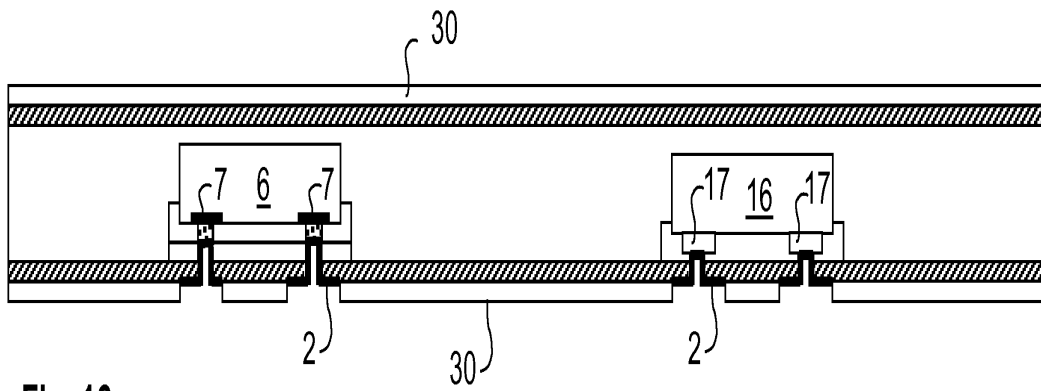


Fig. 16

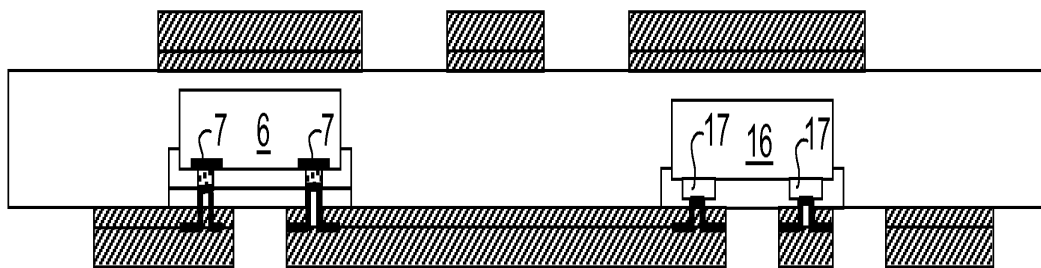


Fig. 17

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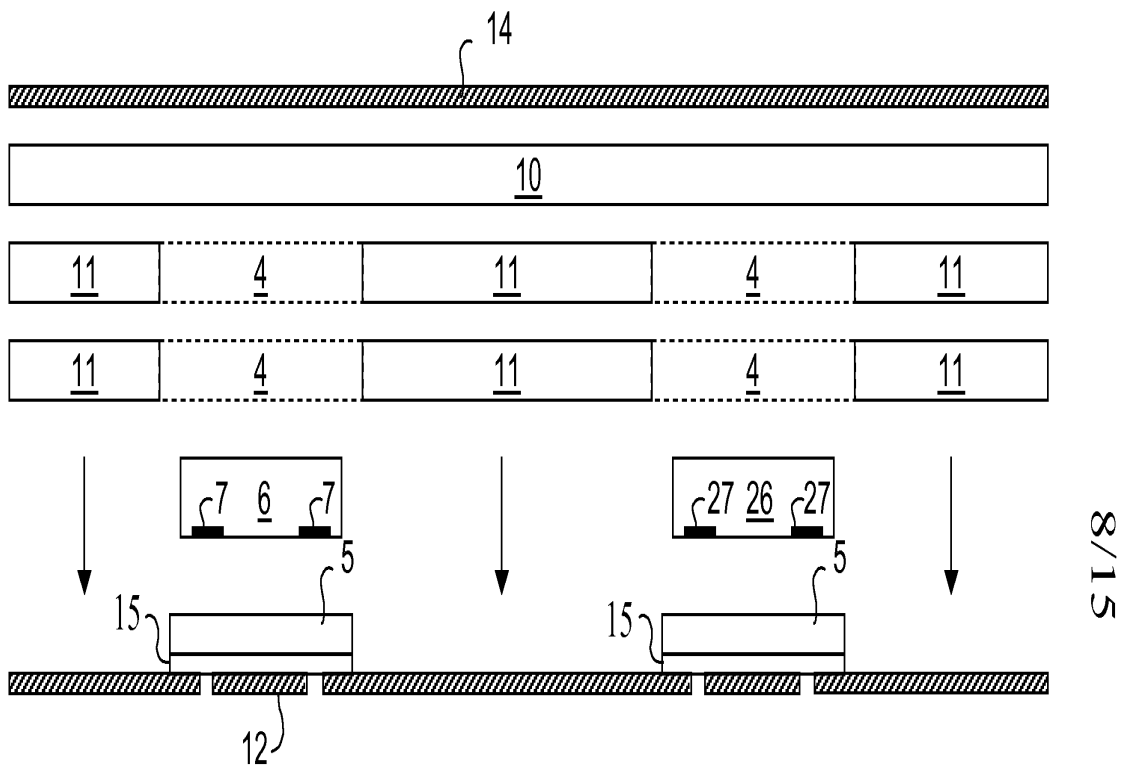


Fig. 18

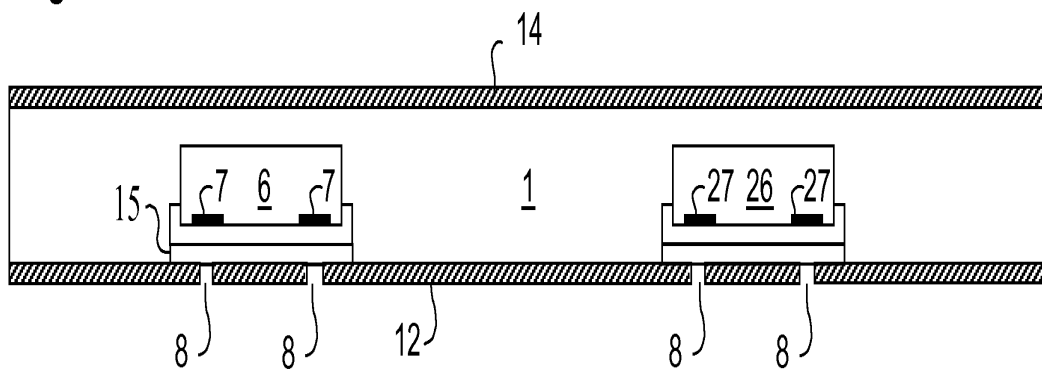


Fig. 19

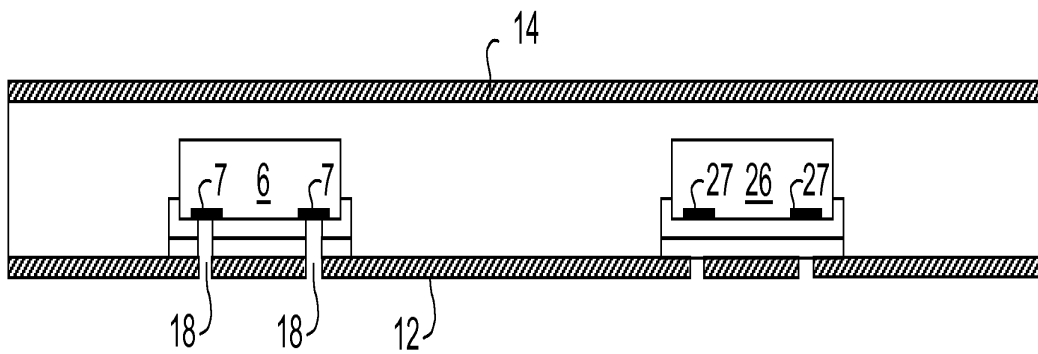


Fig. 20

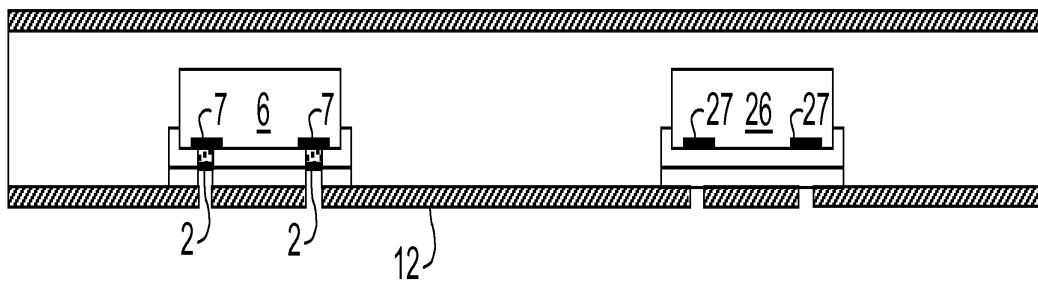


Fig. 21

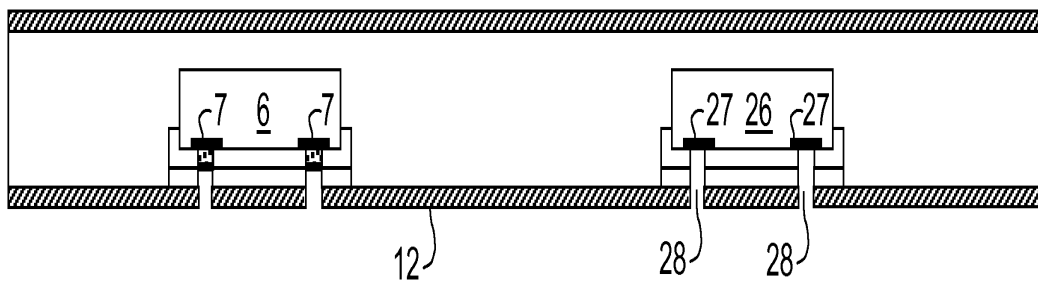


Fig. 22

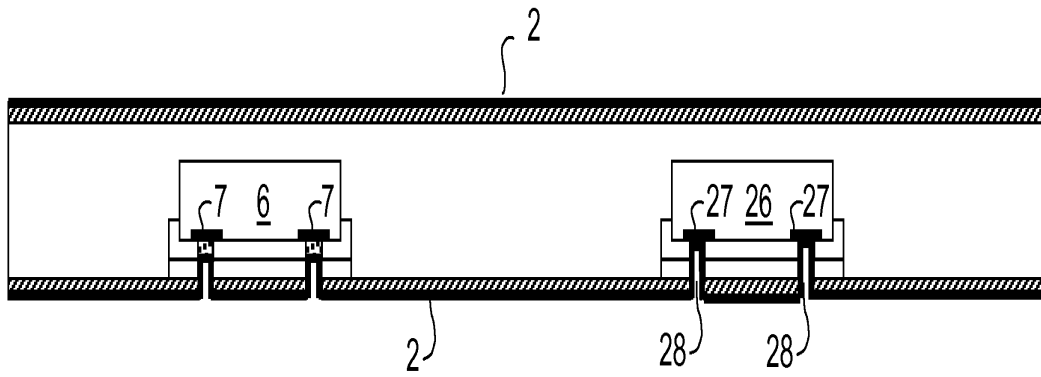


Fig. 23

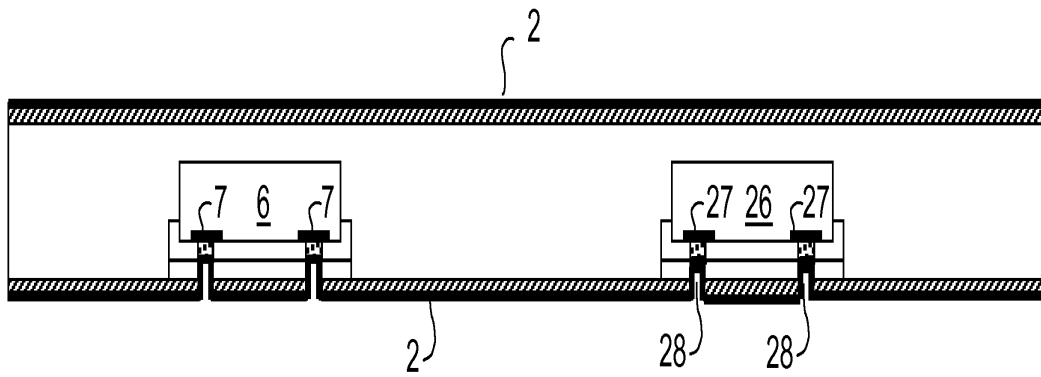
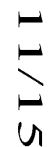


Fig. 24

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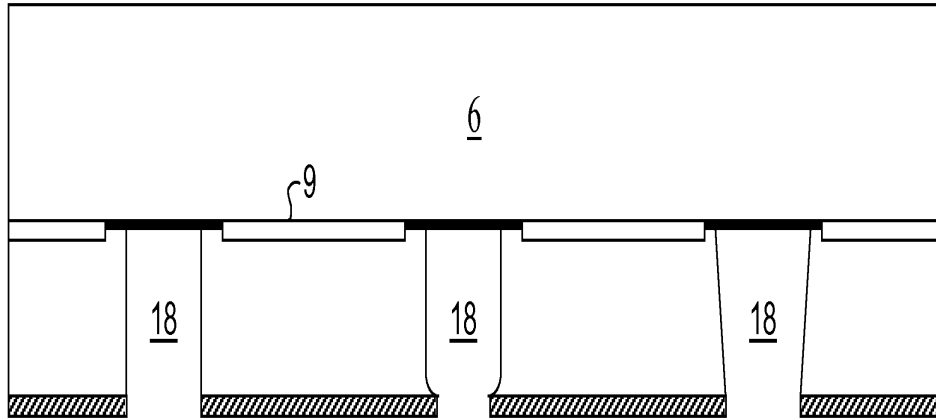


Fig. 26

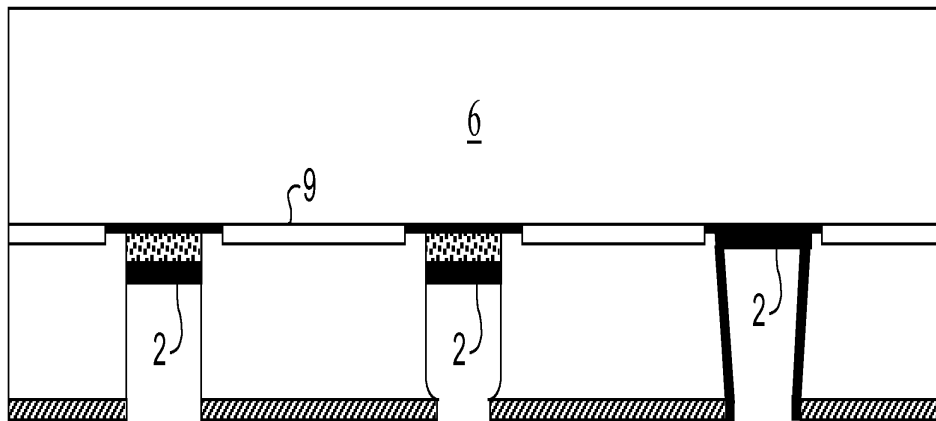


Fig. 27

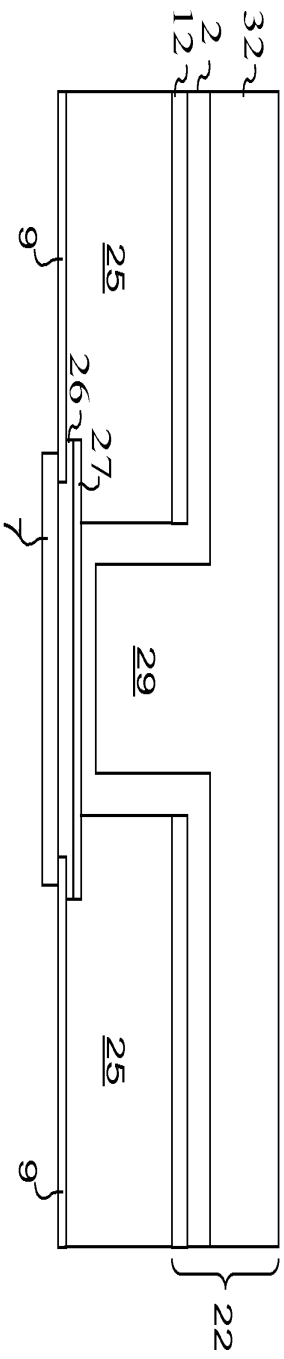


Fig. 28

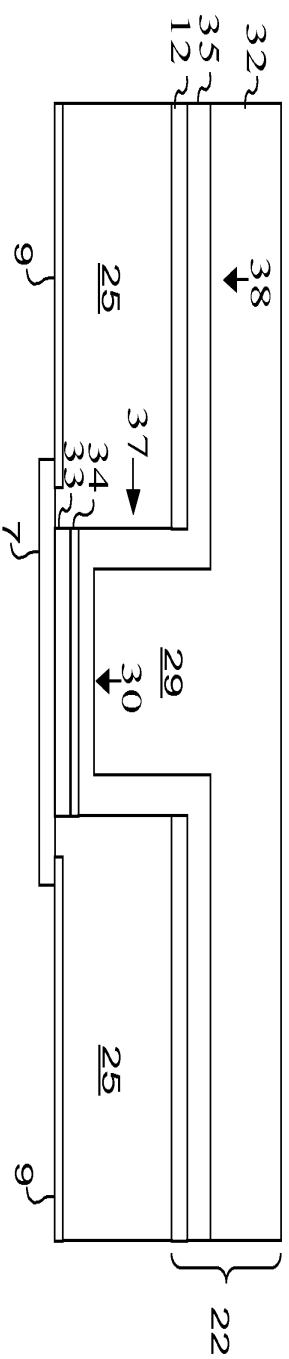


Fig. 29

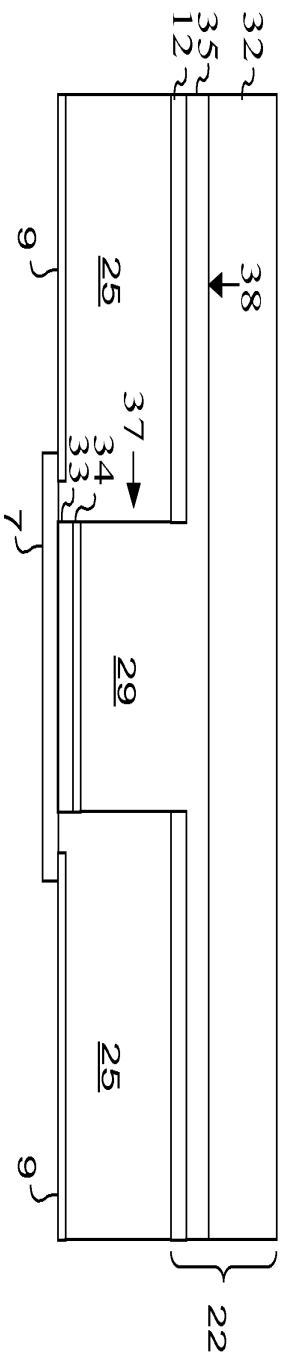


Fig. 30

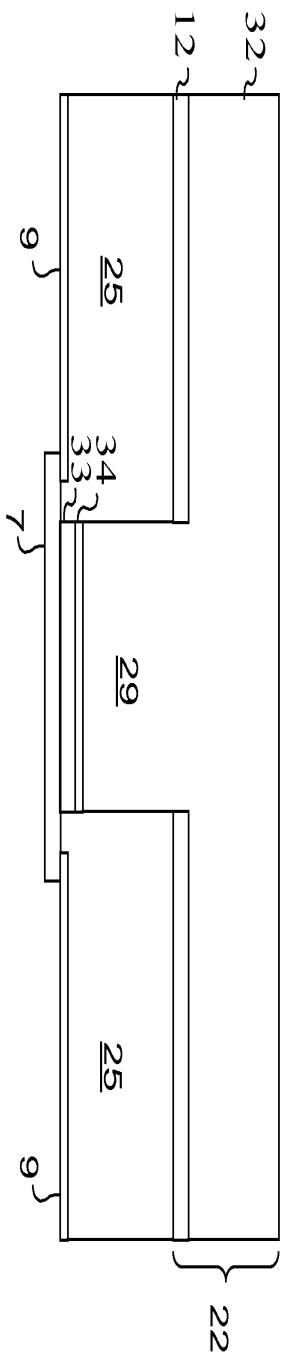


Fig. 31

5 The present invention relates to circuit modules, which comprise an insulator layer and, inside the insulator layer, at least one component, which comprises contact areas. In addition, the circuit modules comprise conductors on the surface of the insulator layer, through which a component can be connected to become part of a circuit outside the component. For creating electrical contacts, the circuit modules comprise contact
10 elements between the contact areas of the component and the conductors.

The invention also relates to methods for manufacturing the aforementioned circuit modules.

In the background art, several different ways are described, by means of which circuit modules containing components located inside an insulator material can be manufactured. The background art also discloses several solutions for manufacturing electrical contacts to the contact terminals of a component, by means of contact elements, and methods for manufacturing a conductor-pattern layer connected to the contact elements.

When evaluating circuit modules and manufacturing methods, attention can be paid, for example, to the circuit module's properties achieved by the method, for example, its price, mechanical durability, and the thickness (thinness) that can be achieved. Depending on the applications, significant factors can also be the quality and durability of the electrical contacts and the reliability and quality of the electrical properties of the whole module. Significant properties to be examined in terms of manufacturing can also be, for example, the reliability, yield, efficiency, price, and environmental friendliness of the manufacturing methods to be used. The practicability of the manufacturing method is also affected by the availability of raw materials and the ability of the method to place

different types of component in a circuit module.

All in all, the requirements set for manufacturing methods and circuit modules are thus very diverse and vary according to the application. This being the case, there is still a
 5 need in the sector to develop new circuit-module structures and manufacturing methods, which can offer new or improved properties, or combinations of properties.

One line of development has been the placing of components inside the electronics module in a bumpless form, i.e. without growing bumps of top of the contact areas of the
 10 component. Cost benefits can then be gained, as the components need no longer be transported during manufacture to a separate production plant to make the bumps.

The applicant's own patent and application publications disclose manufacturing techniques, which can also be used in connection with bump-free components. The
 15 techniques described are particularly suitable for components, in which the material of the contact areas is copper. Of the applicant's own publications, those that can be referred to as most closely relating to the invention are the international patent application publications WO 2004/089048, WO 2005/027602, WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217, and
 20 WO 2007/107630.

However, at present copper is quite little used as a conductor material in semiconductor processes. The most common conductor material is aluminium. In circuit-board manufacture, on the other hand, copper is the principal material for conductors. Copper
 25 conductors of a circuit module can be grown directly on top of aluminium contact areas, but the contact between copper and aluminium is brittle, so that a module of this kind is not optimal in applications, in which mechanical stress acts on the circuit module.

An improved possibility to use contact areas of aluminium or contact areas containing
 30 aluminium would mean that, in circuit modules and manufacturing methods, normal semiconductor circuits in a bumpless form could be used immediately after the semiconductor manufacturing processes and the passivation of the surface. As

aluminium is the conductor material most widely used in the semiconductor industry, good compatibility between the contact element of the circuit module and aluminium would also ensure that suitable semiconductor circuits would be abundantly and economically available. Attempts to develop such manufacturing methods have indeed
 5 already been made for several decades in the field of component packaging technology. In component packaging solutions of this kind, the goal has been a technique, by means of which a relatively small component package could be manufactured around a component, to which a circuit board could then be attached later. Unlike packaging technology, the goal of the manufacturing techniques of the circuit module to which the
 10 present invention relates is the ability to manufacture the entire circuit board in the same process, so as to completely eliminate the packaging stage of the separate component. Of course, this does not exclude the possibility of using the manufacturing method of the circuit module to manufacture only a component package.

15 The patent US 4 246 595, Noyori et al., discloses a method, in which the contact areas of a component are brought into contact with an insulator sheet, in which V-shaped openings have been made. First of all, a layer of titanium (Ti) or chromium (Cr) is grown on the surfaces of the openings and the aluminium contact areas. This intermediate metal layer is intended to prevent the copper from diffusing into the
 20 aluminium and the semiconductor component, as well as to improve the adhesion between the copper and the aluminium. In addition, the intermediate layer acts as an electrical conductor later during electrochemical growing (electroplating), so that the intermediate metal layer will reliably cover also the side walls of the openings. The growing of the titanium or chromium layer requires the use of the sputtering technique,
 25 for which reason the openings must also have a clear V shape. Sputtering is expensive when used on large surfaces (on circuit modules) while additionally the open V shape reduces the available conducting density. Contract structures of a corresponding type are also disclosed in patents US 4 783 695 and US 4 894 115, Eichelberger et al., and in patent US 5 353 195, Fillion et al.

30 Later, in patent US 6 396 148, Eichelberger et al., an attempt is made to solve the problems relating to sputtering, by forming the intermediate metal layer by growing a

layer of nickel on the surface of the aluminium contact areas. According to the patent, the growing of the nickel is performed by means of a chemical growing method (electroless plating). Yet another layer, which also covers the side walls of the openings made in the insulating material for the contacts, is growing on top of the nickel layer by means of a chemical growing method. In the method, the components are attached first by their side and rear surfaces to the insulator layer and, after this, a photo-patternable polymer is spread on the front surface of the component and on top of the contact areas. The polymer is patterned by exposing it to light and developing it, to form openings for the contacts.

10

One possibility is to grow bumps on the surface of the conductors of the circuit-board part of the circuit module and attach the component to the conductors by a flip-chip mounting technique, for example, by ultrasound bonding. Such a method is disclosed in the applicant's own international patent application WO 2006/134220. Problems relating to both production and the quality of the contacts are associated with methods using flip-chip methods.

15

Disclosure of Invention

The object of the invention is to develop a new contact-element structure envisaging the utilization of bumpless components, as well as a circuit module and manufacturing technique using such a structure.

20

According to an aspect of the invention, a bumpless component is used in the circuit module, the material of the contact areas of which being of a different metal, or metal alloy to the conductors of the conductor layer of the circuit module. The contact areas of the component and the conductors of the circuit module are connected to each other with the aid of contact elements, which contain an intermediate layer, which contains a third metal or metal alloy, which differs from the material of the contact areas and conductors, on the surface of the material of the contact area. In addition, the contact surface area between the intermediate layer of each contact element and the contact area of the component is smaller than the surface area of the contact area.

25

30

According to another aspect of the invention, a manufacturing method is created in order to manufacture the circuit module described above, in which the component is attached to a conductor foil or conductor-pattern layer with the aid of a polymer layer and contact elements are made through the polymer layer. When making the contact elements, contact holes are made in the polymer layer on top of the contact areas, at the locations of the contact areas. The contact holes are dimensioned in such a way that the contact surface area between each contact hole and the corresponding contact area is smaller than the total surface area of the contact area. After this, the contact holes are filled with a conductor material, in such a way that filling is started by coating the surface of the contact areas with an intermediate layer, for example, by using one or more chemical metal-growing methods.

Thus, a new type of circuit module and manufacturing method is obtained, which can offer some advantages in terms of the applications of some circuit modules.

In addition, the invention has numerous special embodiments, which provide additional advantages.

In one embodiment, components are used in the circuit module, the material of the contact areas of which contains aluminium and the contact elements comprise a layer containing zinc on the surface of these contact areas containing aluminium. In addition, the contact elements are manufactured in such a way that the contact surface area between the layer containing zinc and the contact area is smaller than the total surface area of the actual contact area.

A layer containing zinc has been observed to be useful in terms of the quality of the electrical contact, as coating a layer containing zinc on the surface of an aluminium contact area prevents the re-oxidation of the aluminium surface and permits the creation of good adhesion between the aluminium and the next layer. In addition, the layer containing zinc improves the mechanical durability against lateral stress of the contact formed through the interface between the aluminium and the intermediate layer of other

metal.

We have observed that extremely good mechanical durability is achieved by using a double zincate process, in which the blank containing the components is subjected to the zincate process at least twice. Thus a more even and denser layer of zinc is made to grow on top of the aluminium contact surfaces. After a single zincate treatment, there is zinc on only some areas of the contact surfaces, or else the layer is porous, therefore a double zincate process is used in the preferred embodiment.

The possibility to use contact elements that are narrower than the contact area can, for its part, provide advantages, for example, by allowing the conductors connected to the contact elements to also be made narrow, especially in embodiments, in which the contact element is essentially of even width vertically, or only narrows moderately towards the component.

In an embodiment of the manufacturing process, in which contact openings are made in the conductor foil of the conductor-pattern layer prior to attaching the component, the component can be attached aligned relative to the contact openings while, in addition, the contact holes needed for the manufacture of the contact elements can be made through these contact openings, by using the material of the conductor foil or conductor-pattern layer as a mask. In such an embodiment, an advantage is obtained in the case of the alignment between the contact elements and the contact areas. In addition, an advantage is obtained in terms of the manufacture of the contact holes, because the holes can be opened using a CO₂ laser, for example.

In an embodiment, in which the contact holes are opened using a laser, the contact holes can be opened one component or component-group at a time, and thus the first intermediate layer can be manufactured first through the contact holes, on top of the contact areas of the first components, and then later the second intermediate layer can be manufactured through the contact holes opened later, on top of the contact areas of the second components. Thus, components, the materials of the contact areas of which differ from each other and are incompatible with the growth processes of the same

intermediate layer, can be fitted in the same process.

In the embodiments, it is also possible to attach the components to the conductors by means of mutually differing polymer layers. Thus the properties of the insulation
 5 between the component and the conductor can be arranged to also be suitable for different mechanical and electrical requirements.

Brief Description of Drawings

10 Figures 1 - 8 show the intermediate stages of a circuit module when using a manufacturing method according to one embodiment.

Figure 9 shows one example of a circuit module according to one embodiment.

15 Figures 10 - 17 show the intermediate stages of a circuit module when using a manufacturing method according to a second embodiment.

Figures 18 - 23 show the intermediate stages of a circuit module when using a manufacturing method according to a third embodiment.

20

Figure 24 shows one intermediate stage of a circuit module when using a manufacturing method according to a fourth embodiment.

25 Figure 25 shows one possible example of a contact hole and its dimensions made for a contact element of a circuit module.

Figure 26 shows examples of possible contact holes.

30 Figure 27 shows some embodiments of intermediate layers manufactured in the contact hole of Figure 26.

Figure 28 shows one contact-element structure.

Figure 29 shows a second contact-element structure.

Figure 30 shows a third contact-element structure.

5

Figure 31 shows a fourth contact-element structure.

Figure 32 shows a fifth contact-element structure.

10

Figure 33 shows a sixth contact-element structure.

Modes for Carrying Out the Invention

15 Figures 1 - 9 show one exemplary application of the manufacturing method according to one embodiment. In this embodiment, manufacture begins from a conductor foil 12, which of metal, for example. A suitable conductor foil 12 is, for example, a copper film, the thickness of which is in the range 1 - 70 μm , typically in the range 3 - 12 μm . Instead of a bare conductor foil 12, it is also possible to use as the base material a layered sheet, which comprises a conductor foil 12 and an insulator layer 13, which is shown by a broken line in Figure 1, on the surface of this. In the embodiments described in the following, it is possible to use such a layered sheet 12, 13, in place of the conductor foil 12.

20

25 Differing from what is shown in Figure 1, it is also possible to use a layered sheet, which comprises a support membrane on the second surface of the conductor foil 12. The support membrane is on the opposite surface of the conductor foil relative to the components to be attached to the conductor foil. If the layered sheet also comprises an insulator layer 13, the support membrane will then be on the opposite side of the conductor foil to the insulator membrane 13. The support membrane can be used, for example, to improve the mechanical stiffness and ease of handling at the start of the manufacturing process of the conductor foil 12, or the layered sheet 12, 13. The support membrane is, however, intended to be removed at a later stage in the process. It is also

30

possible to proceed by starting manufacture from a support membrane while a conductor foil 12, which is patterned or unpatterned, is made on the surface of this. The process examples and stages described in the application example can also be performed correspondingly when using a support membrane, though this is not stated separately. In the description hereinafter, however, reference will be made to a support membrane only when calling attention to something particularly noteworthy in the case of an embodiment using a support membrane. The actual support membrane can be, for example, of an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer. The thickness of the support membrane can be, for example, 25 - 400 μm . The thickness of the support membrane is typically in the range 35 - 105 μm .

Next, contact openings 8 are made in the conductor foil 12, which are located on the conductor foil 12 in such a way that they are placed at the positions of the contact terminals of the components being placed in the module being manufactured. Thus, an individual contact opening 8 is made in the conductor foil 12 for each contact terminal of the component. In this embodiment, the contact openings 8 can be manufactured with the aid of a UV laser. The contact openings 8 can also be manufactured, for example, mechanically by drilling, milling, or etching. In an embodiment using a support membrane, the contact openings 8 are preferably made from the direction of the opposite surface, in such a way that they penetrate the conductor foil 12 completely. However, the contact openings need not penetrate the sheet, instead the method can equally well also be designed in such a way that the contact openings 8 only extend as far as the surface of the material of the support membrane, or form recesses in the material of the support membrane, without, however, passing entirely through it. Also, the contact openings need not pass entirely through the conductor foil, if a thick conductor foil is used, which is thinned by etching in a later stage.

In the embodiment of Figure 1, the contact openings 8 are manufactured in such a way that the size of a contact opening 8 is less than the contact surface area of the contact material to be placed at the opening 8. The contact opening is typically circular in shape, though other shapes too can be used. The shape and size of the contact opening 8 are

selected in such a way that the contact surface of the contact terminal can cover the contact opening 8 entirely.

5 According to Figure 2, manufacture is continued by spreading adhesive layers 5 on the surface of the conductor foil 12, in the connection areas of the components. The adhesive layers will then also cover the contact openings 8. Alternatively, the adhesive 5 can be spread on the surface of the components. The adhesive can also be spread on the surface of both the component and the conductor foil 12. Typically, the adhesive is spread locally, so that the adhesive layers 5 will be located only in the connection areas
10 of the components.

The term adhesive refers to a material, by means of which the components can be attached to the conductor foil 12 or insulator layer 13 that acts as a base. One property of the adhesive is that the adhesive can be spread on the surface to be glued in a relatively
15 fluid form, or one that otherwise conforms to the surface shapes, for example, in the form of a film. A second property of the adhesive is that, after spreading, the adhesive hardens, or can be hardened, at least partly, in such a way that the adhesive is able to hold the component in place (relative to the conductor foil 12) at least until the component is secured to the construction in some other way. A third property of the
20 adhesive is an adhesive capability, i.e. an ability to stick to the surfaces being glued.

The term gluing, for its part, refers to the attachment of pieces to be glued to each other with the aid of an adhesive. In the embodiments, the adhesive is brought between the component and the conductor foil 12 or insulator layer 13 acting as a base and the
25 component is placed in a suitable position relative to the base, in which the adhesive is in contact with the component and the base and at least partly fills the space between the component and the base. After this, the adhesive is allowed (at least partly) to harden, or the adhesive is (at least partly) actively hardened, so that the component attaches to its base with the aid of the adhesive. In some embodiments, the contact protrusions of the
30 component may protrude during gluing through the adhesive layer to come into contact with the base.

The adhesive used in the embodiments is typically an epoxy-based adhesive, for example a heat-cured epoxy adhesive. The adhesive is selected in such a way that the adhesive to be used will have sufficient adhesion to the base and the component. One preferred property of the adhesive is a suitable coefficient of thermal expansion, so that the thermal expansion of the adhesive will not differ too much from the thermal expansion of the surrounding material during the process. It would also be preferable for the adhesive selected to have a short hardening time, preferably of a few seconds at most. Within this time, it would be good for adhesive to harden at least partly, so that the adhesive can hold the component in place. Final hardening can take a clearly longer time and can even be planned to take place in connection with later process stages. In addition, the stresses caused by the later process stages, such as thermal, chemical, or mechanical stress, are taken into account when selecting the adhesive. The electrical conductivity of the adhesive will be preferably in the order of the electrical conductivity of the insulator materials.

Next, components 6 and 16, which comprise contact terminals 7 and 17, are taken. Both components 6 and 16 are semiconductor components, for example, processors, memory chips, or other microcircuits. The contact terminals of the component 6 are contact areas 7, which are located essentially on the level of the surface of the component. Such contact areas 7 of the component 6 are created at the semiconductor factory during the manufacturing process of the semiconductor component. The contact area 7 typically forms the surface of a conductor pattern on the metal used in the process. The metal used in the manufacturing process of semiconductor components is typically aluminium, though other metals, metal alloys, or other conductor materials can also be used. For example, the use of copper has become common in semiconductor-component manufacturing processes.

The contact terminals of the component 16 are contact bumps 7, which protrude from the level of the surface of the component. Such contact bumps 17 are manufactured in a bump-making process after the manufacture of the semiconductor component 16, typically in a separate factory. The contact bump 17 can contain one or more metals, metal alloys, or other conductor materials. Typically, the outer surface of the contact

bump 17, i.e. the contact surface, is made from copper or gold.

The components 6 and 16 are aligned relative to the contact openings 8, in such a way that each contact terminal 7, 17 comes next to the corresponding contact opening 8, and is pressed against the adhesive layer 5. After this, the adhesive is at least partly hardened, so as to prevent, or minimize the relative movement of the components 6, 16 and the conductor foil 12 after alignment. In alignment and gluing, the aim is to position the contact opening 8 to be in the centre of the corresponding contact terminal 7, 17.

After this, insulator sheets 11, in which openings are made for the components 6, 16, as well as a unified insulator sheet 10, which is of unhardened or pre-hardened polymer, are laminated on top of the conductor foil 12. During lamination, the insulator sheets 10, 11 are melted together and form a unified insulator layer 1 around the components 6, 16. In the embodiment of Figure 2, the insulator sheets 11 are fibre mats impregnated with polymer, or sheets containing pre-hardened polymer and reinforced with a fibre material. The polymer can be, for example, epoxy and the fibre reinforcement can be, for example, glass-fibre mat. A typical example of a suitable insulating-sheet 11 material is an FR4-type glass-fibre reinforced epoxy sheet. Other reinforcement and polymer material combinations can be used, of course. When using several insulator sheets 11, the sheets can also differ mutually.

In Figures 2 and 3, the fibre material is shown by wavy shading 19. In the figures hereinafter, the fibre material 19 is not shown, but these structures too include fibre material 19. The fibre material 19 contained in the insulator sheet 11 or the insulator sheets 11 acts as a reinforcement, which provides the electronic module being manufactured with mechanical strength. According to the example of Figure 2, holes 4 are made in the insulator sheets 11 at the locations of the components 6, 16. The insulator sheets 11 are perforated particularly to make openings for components in the fibre material 19 contained in the insulator sheets 11. Without perforation, the components would press against the fibre-material layers 19 during lamination. The unperforated insulator sheet 10, on the other hand, can be fibre-reinforced or unreinforced, depending on the embodiment.

The insulator sheets 10, 11 are typically selected in such a way that they contain enough fluid polymer for the polymer flowing in the lamination stage to be sufficient to fill the holes 4 made in the insulator sheets 11 for the component 6, 16, around the components.

5 The structure shown in Figure 3 is then obtained, in which the insulator layer 1 contains a tight polymer layer, which contains one or more reinforcements of a fibre material 19. The polymer layer is bound tightly to the fibre layer 19 while the tight polymer layer also attaches the components 6, 16 to the surfaces, so that a tight, unified, and mechanically strong insulator layer is formed, which contains the components 6, 16, and
10 which is, in addition, reinforced with fibre material 19.

In the example of Figure 2, a unified insulator sheet 10 is used, though the insulator sheet 10 can also be omitted from the structure. In that case, the insulator sheet 11 or insulator sheets 11 are selected in such a way that they themselves already contain
15 sufficient fluid polymer to fill the holes 4 in the insulator sheets 11 around the components 6, 16. However, it is typically easier to ensure the filling of the holes 4 by using a separate insulator sheet 10.

A conductor foil 14, which is preferably of a material that is similar to, and equally as
20 thick as the conductor foil 12, is also laminated with the insulator sheets 10, 11 into a single structure. Thus, the insulator layer 1 and the components 6, 16 remains between the corresponding conductor foils 12 and 14. Figure 3 shows this intermediate stage of the module manufacture. In the intermediate stage of Figure 3, there is adhesive on the contact surface of the contact terminals 7, 17 and typically also in the contact openings
25 18. In the stage shown in Figure 4, this adhesive is removed and contact holes 18, which extend to the contact surfaces of the contact terminals 7, 17 are formed at the positions of the contact openings 8.

With reference to Figure 3, it can be further stated that the structure can also be
30 manufactured in such a way that a unified layer of fibre material 19 runs between the components 6, 16 and the conductor foil 14. Such a construction can be used when the thickness of the components 6, 16 is sufficiently less than the thickness of the insulator

layer 1. The structure can be manufactured, for example, in such a way that a unified insulator sheet 10, which contains the fibre material 19 of the layer, can be laminated onto the structure.

5 If a support membrane is used in the embodiment on the surface of the conductor foil 12, as depicted in connection with the description of Figure 1, it is most suitable to remove the support membrane after the lamination, i.e. between the intermediate stages shown in Figures 3 and 4.

10 After lamination and the removal of the possible support layer, the adhesive layer, which has been created in the contact openings 8 and between the contact openings 8 and the contact terminals 7, 17, is removed. In the embodiment of the figures, the removal of the adhesive is implemented by the laser-ablation method, using a CO₂ laser. The ability of a CO₂ laser to vaporize organic insulating substances, such as epoxy-base adhesive, is
 15 good, but its ability to vaporize copper or other metals is poor, so that the conductor foil 12 can be used as mask for making the contact holes 18. Thus, it is possible to manufacture contact holes 18, the diameter of which is less than the diameter of the beam of the CO₂ laser. This property creates a significant advantage, as the minimum diameter of the beam of a CO₂ laser is typically in the order of 75 µm, which is too large
 20 when considering the manufacture of precise electronic module structures. A UV laser, on the other hand, can typically be used to manufacture clearly more precise structures. The minimum diameter of the beam of a UV laser can be, for example 25 µm, but a UV laser is not, on the other hand, suitable for removing adhesive from the contact openings 8 and from between the contact openings 8 and the contact terminals 7, 17.

25 Thus, the use of a conductor mask permits the manufacture of very precisely limited and precisely positioned contact holes 18 in an insulator material, such as the adhesive 5 using in the embodiment. In addition, the use of a CO₂ laser permits the cleaning of the contact surfaces of the contact terminals 7, 17 in the same process stage, without any
 30 significant danger of destroying or damaging the contact terminals 7, 17. In the embodiment, the conductor foil 12 is of copper while the contact terminals 7, 17 of the component are also of metal, so that they are not sensitive to the beam of the CO₂ laser,

so that the process can be designed in such a way that the contact surfaces of the contact terminals 7, 17 will be sure to be cleaned sufficiently well. Thus, the advantage of the method described is that contact openings 8 can be made in the conductor foil 12 very precisely with the aid of a UV laser and, after this, the contact openings can be used as a mask for the making of the contact holes 18 by means of a CO₂ laser that is less precise, but safer for the structure.

If the contact holes 8 of the conductor foil 12 were to be manufactured only in this process stage, the method used for machining the metal of the conductor foil 12, for example, a UV laser, would more easily damage also the contact terminals 7, 17, because the energy required to penetrate the conductor foil 12 is significantly greater than the energy required to penetrate the adhesive or other insulation between the contact terminals 7, 17 and the conductor foil 12. In such a manufacturing method, it would be challenging to stop the drilling at precisely the correct depth. In addition, aligning the drilling would be more difficult, due to the deformations arising during lamination and for the reason that the contact terminals 7, 17 of the components cannot be seen through the solid metal film. The use of contact holes 8 pre-manufactured in the conductor foil 12 provides significant advantages, both in the alignment of the components 7, 17 and in the manufacture of the contact holes 18.

In Figure 5, an intermediate layer 2, which is of a suitable conductor material, is made in the contact holes 18. The intermediate layer 2 is manufactured using a suitable chemical conductor-material growing method (electroless plating). The intermediate layer 2 can also consist of a layer of two or more different materials, which are manufactured correspondingly using two or more methods. One purpose of the intermediate layer 2 is to form a conductor membrane for the side walls of the contact holes 18, which connects the contact terminals 7, 17 and the conductor foil 12 to each other. A second purpose of the intermediate layer 2 is to provide a material adapter between the material of the of the contact terminals 7, 17 and the conductor-pattern material to be connected to them. Such a material adapter can be required, for example, in order to ensure the quality of the mechanical or electrical contact and durability, for example, when the material of the conductor-pattern layers of the circuit module is copper and the material of the contact

terminals 7, 17 is something other than copper (Cu), for example aluminium (Al).

When manufacturing the intermediate layer 2, a suitable chemical growing method is used, because by means of such a method the conductor material can also be grown on the vertical surfaces of the contact holes 18, unlike when using sputtering, for example. An electrochemical method (electroplating) cannot be used in this stage, because the side walls of the contact holes 18 are not conducting. Alternatively, V-shaped-opening contact holes can be used and the intermediate layer 2 made by sputtering. Sputterable materials suitable for this purpose are, for example, titanium-wolfram (TiW) and chromium (Cr). A layer of nickel (Ni) and gold (Au) can also be grown on top of the TiW or Cr layer. In the example of Figure 5, nickel grown by a chemical method is used as the intermediate layer 2 in the example of Figure 5, however, so that the intermediate layer 2 will grow at the same time also on the surfaces of the conductor foils 12 and 14. Another example of the intermediate layer 2 is a layer containing zinc, manufactured on the surface of the contact terminals 7, 17, on top of which a layer of nickel (Ni) can further be manufactured. More alternatives that are possible are depicted in connection with the description of Figures 26 - 33.

In this embodiment, after the manufacture of the intermediate layer 2, manufacture is continued by spreading resist layers 3, typically photoresist layers, on both surfaces of the module. The resist layers 3 are patterned with the aid of a conductor-pattern mask by exposure and development, in such a way that the resist 3 is removed from the desired parts of the conductor patterns of the conductor-pattern layers. This intermediate stage is shown in Figure 6. After this, the module is taken to an electrochemical bath and voltage is led to the intermediate layers 2 of the module. The desired conductors of the conductor-pattern layer are then grown in the openings of the resist layers 3. The conductor material also grows in the contact holes 18, forming a conductor core to the contact elements, as can be seen from Figure 7. In the example of Figure 7, the conductors 22, 24 are electrochemically grown copper. Finally, thin etching-mask layers are grown on the surface of the conductors 22, 24. A layer of tin (Sn), for example, can act as the etching mask.

- Next, the resist layers 3 are removed, when, in the embodiment of the figures, the intermediate layer 2 is revealed from under the removed resist. The revealed part of the intermediate layer 2 is removed, for example, by etching, the same procedure being use for the parts of the conductor foils 12 and 14 revealed outer the conductors 22 and 24.
- 5 The etching-mask layer then protects the outermost surfaces of the conductors 22 and 24 from the effects of the etching. An electronic module, which contains two components 6 and 16 connected electrically to conductors 22, comprising two conductor-pattern layers (conductors 22 and 24), and shown in Figure 8, is then obtained.
- 10 In the example of Figures 6 and 7, the conductors 22 and 24 are grown directly into their correct shape in the openings made in the resist layer 3. However, the conductors 22 and 24 can also be manufactured in another way, both in this example and in the examples described hereinafter. One alternative way of manufacture is to grow a unified layer of conductor material over the surfaces of the entire module blank and to pattern the
- 15 conductor layer later by means of a lithography method, in order to form the conductors 22 and 24. Described in greater detail, it is possible to proceed, for example, in such a way that, continuing from the intermediate stage of Figure 5, copper is grown on the surfaces of both intermediate layers 2 by means of an electrochemical method. In that case, the contact holes 18 too are filled with copper. After this, resist layers are spread
- 20 on top of the copper layers, the resists are patterned, and the excess parts of copper, or the intermediate layer 2 and the conductor foils 12 and 14 are etched. After this, the resist mask is removed. Using either manufacturing method, the result is the structure shown in Figure 8.
- 25 Figure 8 can show an already finished simple circuit module, but manufacture is usually continued by manufacturing additional insulator and conductor layers on the surfaces of the circuit module, which are connected electrically with the aid of vias to the structure shown in Figure 8. In addition, it should be noted that vias can be manufactured in the module too of Figure 8, which connect the conductors 22 to the conductors 24. Such vias
- 30 can be manufactured in a corresponding manner to, and in the same process stages as described above in the manufacture of the contact elements.

The module of Figure 8 can be further refined in the manner shown in Figure 9, in such a way that the surfaces of the module are protect by protecting layers 20. In addition, in the example of Figure 9, external contact elements, which comprise bases 21 made on top of the conductor patterns 22, 24 and contact balls 23 made on their surfaces, are manufactured in the module.

Figures 10 - 16 show a manufacturing method according to a second embodiment, up to a stage corresponding to the intermediate stage shown in Figure 5. Manufacture can be continued from the intermediate stage of Figure 16, for example, as shown by Figures 6 - 9, or suitably also in an alternative manner, in which the material of the conductors 22 and 24 is first of all grown over the entire surface and after that patterned to form conductors 22 and 24. The technical features and parameters presented in connection with the description of Figures 1 - 5 can also be applied in the process stages shown in Figures 10 - 16, so that there is no need to repeat all the details of the manufacturing process and their advantages in the following embodiment. On the other hand, the essential differences between the embodiments shown by Figures 1 - 9 and Figures 10 - 16 are brought out in the following.

In the embodiment of Figures 10 - 16, manufacture starts, as in Figure 1, from a conductor foil 12, in which contact openings 8 are made. After this, a spacer 15 is attached to the future attachment point of the component 6 on the surface of the conductor foil 12. The spacer 15 is of a suitable insulating material, for example, of pre-hardened adhesive or some other polymer, which has sufficient adhesion with the surface of the conductor foil 12. The spacer 15 can also be of hardened polymer, in which case it can be attached to the surface of the conductor foil 12, for example with the aid of separate adhesive.

A spacer 15 can be used for many different reasons. One use of a spacer is to increase the insulating thickness between the component 6 and the conductor foil 12. The need to increase the insulating thickness can be imposed, for example, by the requirements set by the electrical operation of the circuit module or the component 6. In that case, with the aid of the spacer 15 it is possible to set the properties of the insulation between the

component 6 and the conductor foil 12 as desired. The properties selected can be, for example, a desired specific resistance and spark-over resistance, which can be influenced by the selection of the material of the spacer 15 and the adhesive 5. The spacer can also be used to prevent a short-circuit between the component and the conductor foil 12. Such a use will come into question especially in embodiments in which the surface of the component 6 is pressed very close to the conductor foil, when a risk arises of unintended electrical contacts being formed between the conductor structures on the surface of the component and the conductor foil. A spacer can also be used to weaken the capacitive connection between the internal circuit elements of the component 6 and conductors 22 running next to the location of the component 6.

In addition to, or instead of a spacer 15, it is possible to use for the same purpose an insulator layer 13 entirely covering the surface of the conductor foil 12, as described in connection with Figure 1.

In the examples of Figures 10 - 16, a spacer 15 is used in connection with a bumpless component 6, but the contact terminals of a component 16 with bumps must be made to extend closer to the surface of the conductor foil 12, so that a sufficient insulating gap can be ensured between the opposite surface of the component 16 and the conductor foil 14. In the embodiment, spacers 15 selected component-specifically can be placed in the circuit module, in order to optimize the electrical and/or mechanical properties of the circuit-board module. The same module can thus also contain different kinds of spacers 15 and thus spacers 15 can also be used in series production, in order to make components 6, 16 coming from different sources and with different properties to each other compatible with the circuit-board manufacturing process being used. One example of a mechanical property requiring optimization is the thickness of the insulator layer 1 (and at the same time of the entire module), which can be reduced with the aid of suitable selected spacers 15, which can be seen, for example, in Figure 12.

According to Figure 11, manufacture is continued by spreading adhesive layers 5 on the surfaces of the conductor foil 12 and the spacer 15 in the connection areas of the components. The components 6 and 16 are aligned relative to the contact openings 8 and

glued in place. After that, in the example of Figure 11, insulator sheets 10, 11 and a conductor foil 14 are laminated on top of the conductor foil 12. Next, photo-resist layers 30, which are patterned in such a way that openings larger than the contact openings 8 are created at the positions of the contact openings 8, are spread on the surface of the conductor foils 12 and 14, or a coating is made electrophoretically on top of the entire conductor layer. This photo-resist layer 30 is used to limit the growth of an intermediate-layer material grown using a non-selective method to the contact holes and the immediate surroundings of the contact openings 8. Such a procedure can also be used in connection with the example described above, nor, on the other hand, is it essential in the examples of Figures 10 - 16. Figure 12 shows the module after these stages. The contact terminals 7 of the component 6 are covered by both a spacer 15 and adhesive 5. There is adhesive on the surface of the contact bumps 17 of the component 16 and in the corresponding contact openings 8.

In the stage shown in Figure 13, contact holes 18 are made at the positions of the contact openings 8 of the component 6. The contact holes are opened through the spacer 15 and the adhesive layer 5, as far as the contact surfaces of the contact terminals 7. In the embodiment of the figure, the opening of the contact holes 8 is implemented by the laser-ablation method, using a CO₂ laser, as described in connection with Figure 4. In the embodiment of Figures 10 - 16, the important fact is that contact holes are not opened at this stage of the position of the contact terminals 17 of the second component 16.

In the stage shown in Figure 14, an intermediate layer 2, which is of a suitable material, is made in the contact holes 18 of the component 6. The conductor material of the intermediate layer 2 is selected on the basis of the material of the contact terminals 7 of the component 6 and manufactured using a suitable chemical conductor-material growing method. In the example of the figure, the material of the contact terminals 7 of the component is aluminium and the material of the intermediate layer 2 is mainly a metal alloy containing zinc. The principles described in connection with Figure 5 above are applied to the growing of the intermediate layer. Unlike the example of Figure 5, in the case of Figure 14, it is, however, also possible to proceed in such a way that in this

stage the intermediate layer 2 is grown with the aid of a selective method only on the surface of the contact terminals 7, i.e. on the bottom of the contact holes 18 and not on the edges of the contact holes 18. In this embodiment, the intermediate layer 2 coming on the edges of the contact holes 18 is grown later in connection with the growing of the intermediate layer relating to the contact bumps 17 of the component 16. The embodiment using a selective growing method has the advantage that the intermediate layer 2 does not grow on top of the adhesive layer covering the contact bumps 17 of the component 16.

Manufacture is continued in the stage shown in Figure 15 by manufacturing contact holes 28 at the positions of the contact openings 8 of the second component 16. After this, the module according to Figure 16 is subjected to a suitable chemical conductor-material growing method. In the example of Figure 15, the growing method is non-selective and the conductor material grows on all the free surfaces of the module and thus also in the contact holes 18 of component 6 and in the contact holes 28 of component 16. However, the photo-resist layer 30 protects the surfaces of the module, so that the intermediate layer 2 grows only in the contact holes 18 and 28 and in their surroundings. After this, the photo-resist and the conductor material that may have grown on its surface is removed. Such an embodiment using a photo-resist layer 30 can be useful, for example, when nickel or some other metal differing from copper is grown in the openings of the photo-resist layer, for example, using a non-selective method. The conductors 22 and 24 can then be manufactured to consist of solely a copper layer.

In other embodiments, suitably selected selective growing methods can also be used and the conductor material is grown only on the surfaces of the contact bumps 17 of the component 16, correspondingly as described above in connection with Figure 14. In any case, at this stage the intermediate layer 2 is grown at least on the surfaces of the contact bumps 17 of the component 16 and on the surfaces of the side walls of the contact holes 28 and, in addition, if desired also on the surface of the intermediate layer 2 connected to the contact terminals 17 of the component 6 and/or on the surfaces of the side walls of the contact holes 18 of the component 6.

If the example of Figures 10 - 16 were to be implemented without the use of a photo-resist 30, in the example of Figure 16 the material of the surface of the contact bumps 17 of the component 16 could suitably also be copper and the material of intermediate layer 2 to be grown of the surface of the contact bumps 17 would then be copper manufactured suitably using a chemical growing method.

After the manufacture of the intermediate layer 2, in this embodiment manufacture can be continued, for example, in the manner stated in connection with the description of Figures 6 - 9, by manufacturing conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28.

Another alternative is to coat copper on both conducting surfaces of the module, after the removal of the photo-resist layer 30. After this, the copper layers can be patterned to form conductors 22 and 24, when the structure shown in Figure 17 will be obtained, in which the conductors 22 and 24 are formed of the first and second copper layers in the surroundings of the contact elements, as well as of an intermediate layer 2, which is of nickel for example, between them. Elsewhere, the conductors 22 and 24 are formed of a first and second copper layer, between which is the interface to be analysed. Once the structure of Figure 17 has been manufactured, it is possible, if desired, to continue in some manner described in connection with any of the previous examples.

Figure 18 - 23 show a manufacturing method according to a third embodiment, which is a variation of the embodiment shown in Figures 10 - 16. From the intermediate stage of Figure 23, manufacture can be continued, for example, in the manner shown in Figures 6 - 9. The technical features and parameters presented in connection with the description of Figures 1 - 5 and 10 - 16 can thus also be applied in the process stages shown in Figures 18 - 23, so that all the details and their advantages of the manufacturing process need not be unnecessarily repeated in the following embodiment. However, in the following the essential difference between the embodiments shown in Figures 10 - 16 and Figures 18 - 23 is presented.

In the embodiment of Figures 18 - 23, manufacture is commenced, as in the case of

Figure 10, from a conductor foil 12, in which contact openings 8 are made. After this, spacers 15 are attached to the surface of the conductor foil 12, to the future attachment points of the components 6 and 26. The spacers 15 of the components 6 and 26 can be mutually identical or selected component specifically, for example, in such a way that the spacer 15 of the component 6 is of a different material and/or thickness to the spacer 15 of the component 26.

According to Figure 18, manufacture is continued by spreading adhesive layers 5 on the connection areas of the components and by laminating insulator sheets 10, 11 and a conductor foil 14 to the blank, exactly as described in connection with Figure 11. Figure 19 show the module after these stages.

In the stage shown in Figure 19, contact holes 18 are made at the positions of the contact openings 8 of the component 6, as described in connection with Figure 13. At this stage, contact holes are not yet opened at the positions of the contact terminals 27 of the component 26.

The stage shown in Figure 21 corresponds completely to the method stage described in connection with Figure 14. In this embodiment, an intermediate layer 2, which is of two layers, is manufactured in the contact holes 18 of the component 6. In the example of the figure, the material of the contact terminals 7 of the component is aluminium. The two-layer intermediate layer 2 of the example comprises first a grown layer containing zinc and after this a grown nickel-aluminium layer. The nickel-aluminium layer is grown by means of a chemical method and is used to seal the layer containing zinc.

Manufacture is continued in the stage shown in Figure 22, by making contact holes 28 at the positions of the contact openings 8 of the second component 26. After this, according to Figure 23 the module is subjected to a suitable chemical conductor-material growing method. This stage corresponds to the method stage described in connection with Figure 16. In the example of Figure 23, the material of the surface of the contact terminals 27 of the component 26 is copper and the material of the intermediate layer 2 grown of the surface of the contact terminals is also copper.

Figure 24, for its part, shows a modification of the embodiment of Figures 18 - 23, in which, after the stage shown by Figure 22, a first intermediate layer is grown on top of the contact terminals 27 of the component 26, by means of a selective growing method and, after this, the growing of the intermediate layer 2 is continued using a non-selective method. In the example of Figure 24, the material on the surface of the contact terminals 27 of the component 26 is gold and the material of the intermediate layer 2 grown on the surface of the contact terminals 27 is nickel.

In the embodiments of these Figures 18 - 24, after the manufacture of the intermediate layers 2 it is possible to continue, for example, by making conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28, for example, by means of the manner stated in connection with the description of Figures 6 - 9.

Figure 25 shows in greater detail the shape of the contact hole and correspondingly also the shape of the contact element to be manufactured in this opening. The example of Figure 25 shows one possible shape, which can be achieved when using the embodiments described above. The shape can be affected with the aid of the shape of the contact openings 8 to be made in the conductor foil 12, the properties of the insulation between the conductor foil 12 and the component, and the operating parameters of the CO₂ laser. The contact hole of Figure 25 is rotationally symmetrical and the cross-section shown in the figure is taken through the central axis of the contact hole, i.e. it shows the widest possible cross-section. In Figure 25, the size and shape of the contact hole are determined with the aid of the following parameters:

- greatest width W_{MAX} , from which the greatest cross-sectional area A_{MAX} can be calculated,
- the width W_{CONT} of the contact between the contact element and the contact surface 7 of the component 6, from which the contact surface-area $A_{CONT 1}$ between the contact element and the contact surface of the component can be calculated, and

- the width W_{HOLE} of the contact opening, from which the contact surface-area $A_{CONT\ 2}$ between the contact element and the conductor of the conductor-pattern layer can be calculated.

5

The figure also shows the width W_{PAD} of the contact surface of the component, from which the surface area A_{PAD} of the contact surface can be calculated, if the shape of the contact surface is known. The contact surface 7 can be, for example, square in shape and, when W_{PAD} represents the width of a side, the surface area of the contact surface is obtained as: $A_{PAD} = W_{PAD} \times W_{PAD}$. Of course, the surface areas can also be determined with the aid of surface-area measurement, which can be more practical if the surface area to be determined is of an irregular shape.

10

In the figure, the contact surface 7 is surrounded by a passivation layer 9 made on the surface of the component 6. In that case, the surface area A_{PAD} refers precisely to the surface area free to form a contact, i.e. the surface area of the surface that is revealed in the opening made in the passivation layer 9. In addition, the figure shows the distance H of the distance between the conductor foil 12 and the contact surface 7, which corresponds to the depth of the contact hole and is thus the height of the contact element to be made in the contact hole. Because the contact hole is filled entirely with conductor material, the other dimensions too of the contact hole correspond to the dimensions of the contact element and the parameters W_{MAX} and W_{HOLE} can also be used to refer to the corresponding dimensions of the contact element.

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The following presents some typical parameters in connection with the embodiments described above:

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$H = 1 - 50\ \mu\text{m}$, usually $5 - 30\ \mu\text{m}$;

30

$W_{PAD} = 20 - 1000\ \mu\text{m}$, usually $50 - 200\ \mu\text{m}$, and most usually about $100\ \mu\text{m}$; and

$W_{HOLE} = 5 - 500\ \mu\text{m}$, usually $20 - 75\ \mu\text{m}$, and most usually about $30 - 50\ \mu\text{m}$.

In addition, generally $W_{HOLE} \geq H$, which represents the reliable filling of the contact hole. The contact hole 18 is intended to be manufactured in such a way that the side walls of the hole would be vertical. In other words, the goal is a contact hole, the width and shape of which remains constant over the whole distance H between the conductor foil 12 and the contact surface 7, i.e. the contact hole would have the shape of the contact opening 8 over all of this distance. A shape that narrows towards the contact surface 7 is also good. In practice, when using the laser process described above the contact hole can, however, become widening towards the contact surface 7, or first widening and then narrowing, so that the contact hole is widest somewhere between the conductor foil 12 and the contact surface 7. Figure 25 shows a contact hole of this kind. Such a non-optimal shape is not problematic, provided the widening is not too great and the filling of the hole succeeds well.

Of the dimension values of the widths referred to above, the width W_{PAD} of the contact surface 7 of the component is determined through the selection of the component. If necessary, W_{PAD} can be measured separately from each straight line that runs through the centre point of the contact surface 7. This definition may be required when examining the dimension values referred to above and their ratios, if the shape of the contact surface 7 or of the contact opening 8 is irregular. In the most usual cases, the contact surface is, however, square, in which case the width of the side of the square can generally be used as the width W_{PAD} of the contact surface 7.

The width W_{HOLE} of the contact opening 8 is a parameter, which is selected when planning the manufacturing process. One parameter to be taken into account when selecting the width of the contact opening 8 is the width of the contact surface 7 of the component being used. The width of the contact opening 8 is selected in such a way that the contact hole to be made through the contact opening will meet the contact area 7 of the component over its entire cross-sectional area at the component end, and will not miss the contact area, for example, on the surface of the passivation layer. If the contact opening is circular in shape, with width W_{HOLE} of the contact opening is the diameter measured through the centre point of the circle. If, on the other hand, the contact opening

is irregular I shape, W_{HOLE} can, if necessary, be measured separately along each straight line that runs through the centre point of the contact opening 8. In the case of an irregular shape, when comparing the width W_{HOLE} of the contact opening with the width W_{PAD} of the contact surface, the comparison can always be made separately for each pair
 5 of widths measured through parallel straight lines. If necessary, the widths W_{HOLE} and W_{PAD} can also be compared in a corresponding manner to the other parameters described.

The ratios of the parameters described above can also be applied in connection with the
 10 contact bumps 17, in which case the surface area and width of the contact area will be replaced by the surface area and width of the contact bump and the distance H will be measured to the surface of the contact bump.

The shape of the contact hole can be influenced with the air of the laser parameters,
 15 which are selected according to the hole parameters and the properties of the insulation to be removed. The manufacturing result is, of course, also affected by the laser device being used. The suitability of the selected parameters for the process is indeed examined with the aid of a pilot manufacturing batch and, if necessary, the parameters are altered so that the desired result will be achieved.

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In general, it is sensible in the manufacturing method to try to achieve a contact-hole shape, in which

$W_{CONT} = 0.5 - 1.5$ times W_{HOLE} , preferably $0.7 - 1.2$ times W_{HOLE} , and most preferably 0.8
 25 $- 1.0$ times W_{HOLE} , however, in such a way that $W_{CONT} < W_{PAD}$; and

$W_{MAX} =$ at most $100\ \mu\text{m}$, preferably at most $30\ \mu\text{m}$, and most preferably at most $10\ \mu\text{m}$
 larger than whichever of the parameters W_{HOLE} and W_{CONT} is greater. Presented
 relatively, the objective would be for $W_{MAX} =$ at most $40\ \%$, preferably at most $20\ \%$, and
 30 most preferably at most $10\ \%$ greater than whichever of the parameters W_{HOLE} and W_{CONT} is greater.

In the most optimal shape of a contact element, W_{MAX} is essentially as large as W_{HOLE} and, in addition, W_{CONT} is 0 - 20 % smaller than W_{MAX} .

5 In the most typical embodiments, the contact surface 7 has a square shape and the contact opening 8 is circular in shape. In that case, $A_{CONT\ 1}$ is typically 10 - 75 % of the surface area A_{PAD} . $A_{CONT\ 1}$ and $A_{CONT\ 2}$ are typically mutually approximately of equal size, for example, with an accuracy of ± 20 %.

10 Figure 26 shows examples of other possible shapes of the contact holes 18. Figure 27, for its part, shows examples of intermediate layers 2 manufactured in such contact holes. In the examples of Figures 26 and 27, the component to be attached is bumpless. As can be seen from Figure 27, the intermediate layers 2 do not extend at all on top of the passivation layer 9 of the component, but instead are in contact only with the contact surface 7 of the component. With the aid of this feature, it is possible to see even from
15 the finished electronic module whether the component embedded in the electronic module has bumps or is bumpless. The bumps grown on the contact surface 7 of the component in the bump-creation processes always fill the entire contact surface 7 and always also spread slightly on top of the passivation layer 9. If, on the other hand, bumpless components are used in the embodiments described above, the intermediate
20 layer 2 and the contact element grow only into the contact hole 18, when in the finished electronic module the intermediate layer 2 will not extend on top of the component's passivation layer 9 and part of the contact surface 7 of the component will always remain free of the intermediate layer 2 (the edges of the contact surface 7) when the alignment and manufacture of the contact hole 8 have succeeded. Also in a possible
25 contact-hole 18 alignment-error situation, in which the contact opening 8 is not completely aligned with the contact surface 7, at least part of the edge areas of the contact surface 7 and of the passivation layer surrounding the edge area will be free of the intermediate layer 2.

30 If a bumpless component is manufactured by a semiconductor process using copper conductors, the contact area 7 is copper. In that case, the intermediate layer can be manufactured directly from chemically grown copper, which forms a conductor

surfacing also on the side walls of the contact hole 18. After this, the contact holes 18 can be filled and the thickness of the conductor layer increased using an electrochemical copper-growing method.

5 At the moment of writing of the present application, the most commonly used conductor material in semiconductor processes is, however, aluminium. Thus, the most common material of the contact area 7 of bumpless components too is aluminium and it is preferable to use an intermediate layer, with one or more layers manufactured from different materials, between the aluminium contact area and the copper conductors of the
10 electronics module. In the following, reference is made to a few possible intermediate-layer constructions:

Intermediate-layer construction 1

15 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the side walls of the contact hole 18. A layer of nickel, which does not grow at all or only poorly on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical
20 method on the surface of the nickel. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 2

25 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of copper is grown by a chemical method on the surface of the layer containing zinc. The copper grown by a chemical
30 growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 3

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of nickel-aluminium, which does not grow on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical method on the surface of the nickel-aluminium. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 4

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. A layer of nickel-aluminium is grown by a chemical method on the surface of the layer containing zinc. A layer of nickel is grown by a chemical method on the surface of the nickel-aluminium and a layer of copper is grown by a chemical method on the surface of the nickel.

Intermediate-layer construction 5

First of all, a layer containing zinc is grown on the surface of the aluminium contact layer 7. A layer of nickel is grown by a chemical method on the surface of the layer containing zinc.

Intermediate-layer construction 6

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, which grown nickel layer alone forms the intermediate layer 2.

Intermediate-layer construction 7

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, and a layer of copper is grown by a chemical method on the surface of the nickel.

5

In the above examples of intermediate-layer constructions, the layer containing zinc contains, for example, about 80 % zinc, about 16 % copper, about 2 - 3 % nickel, and about 2 - 3 % iron. This is only one possible example of alloy ratios suitable for the application, so that the alloy ratios can, of course, vary according to the applications. In the above examples of intermediate constructions, the thickness of the layer containing zinc is less than 1 μm , usually as a single layer about 0.1 μm and as several layers, for example 0.3 - 0.4 μm . At its thinnest, the layer containing zinc can be about 5 - 10 nm after manufacture. When growing a layer containing nickel or nickel-aluminium on top of the layer containing zinc, at least some of the zinc atoms dissolve and are replaced with nickel atoms. In the finished circuit module, it can be possible for the layer containing zinc to be observable as mainly a concentration profile of zinc in the interface between the aluminium and the material of the next layer. The layer containing zinc need not necessarily be precisely limited in the final product, because the zinc can diffuse to the adjacent material layers, particularly in stages of the manufacturing process using higher temperatures.

20

In one preferred embodiment, the layer containing zinc is grown by a double zincate process. With a single zincate process, the zinc forms a non-uniform and uneven surface on top of the aluminium. The adhesion of a nickel layer grown on top of such a surface is weaker and is less suitable for use with small micro-via openings. The quality of the grown zinc surface can be significantly improved by using a double zincate process. Typically, in such a process, after the first zincate treatment, the layer containing zinc is stripped using nitric acid (HNO_3), after which a second layer containing zinc is coated. By means of the double zincate process, a tight and uniform layer containing zinc is obtained on the surface of the component's aluminium junction interface.

25

30

The thickness of the nickel-aluminium layer, for its part, can be, for example, 0.2 - 2

μm . The thickness of the nickel layer, on the other hand, can be, for example 0.5 - 20 μm , typically 2 - 10 μm . The layer thicknesses too are only examples of the possible layer thicknesses and other layer thicknesses can also be used.

- 5 In the embodiments, the electrochemically grown copper layer can have a thickness of, for example, 5 - 30 μm , typically 10 - 20 μm . The copper layer grown by a chemical growing method, for its part, is generally manufactured to be clearly thinner, and its thickness in the embodiments is, for example, 0.1 - 2 μm , typically 200 - 800 nm.
- 10 In the manufacturing methods described above, it is, of course, also possible to use intermediate-layer constructions and materials, for example tin, other than those referred to above. It is also possible to grown a nickel layer directly on the surface of the aluminium, for example, by alkali etching and flushing the surface after this with propan-2-ol and immediately after this coating with propan-2-ol at boiling point in a
- 15 warm chemical nickel bath. In addition, the surface of the layer containing zinc could also be coated with chromium and gold on the surface of the nickel.

Figure 28 shows yet another possible contact structure, in which it is possible to use components, the contact area of which is pre-equipped with base-metallurgical layers, though bumps as such are not made. Figure 29 shows one possible corresponding contact structure, implemented with a bumpless component.

Figure 28 shows a passivation layer 9 on the surface of the component, in which there is an opening at the position of the contact area 7 of the component. There is a polymer layer 25 of the surface of the passivation layer 9. The polymer layer 25 can consist of one or more polymer layers. The material of the polymer layer 25 can contain, for example, an insulator layer 13 depicted in connection with Figure 1, adhesive 5 depicted in connection with Figure 2, and/or a spacer depicted in connection with Figure 11. The base metallurgy, which in this case comprises two layers, is made on the surface of the contact area 7 of the component. The first base-metallurgy layer 26 is a layer of, for example, chromium (Cr) or titanium-wolfram (TiW) manufactured by sputtering. The second base-metallurgy layer 27 is a layer of, for example, nickel (Ni), copper (Cu), or

gold (Au), manufactured by sputtering. The actual bump comprises further a gold or copper layer, for example, grown chemically or electrochemically, on the surface of the second base-metallurgy layer 27.

5 In the example of Figure 28, the component is attached by a polymer layer 25 to a conductor foil 12, in which contact openings 8 have been made as depicted in the methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the second base-metallurgy layer 27, are made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is
10 made using one or more chemical growing methods, in a corresponding manner to that depicted in the methods described above. In the example of Figure 28, the intermediate layer 2 is of copper grown using a chemical growing method. On top of this intermediate layer a layer 32 of copper is grown using an electrochemical growing method. The electrochemically grown copper also forms the conductor core 29 of the contact element.
15 It can be seen from Figure 28 that the conductor foil 12, the intermediate layer 2, and the copper layer 32 together form the material of the conductor 22. In the example, the conductor foil 12, the intermediate layer 2, and the copper layer 32 are all of copper, but the layers and the interfaces between them, can, however, also be detected by analysing the finished structure.

20 Like Figure 28, Figure 29 shows a passivation layer 9, in which there is an openings at the position of the contact area 7 of the component, on the surface of the component. On the surface of the passivation layer 9 is a polymer layer 25, which corresponds to that shown in connection with Figure 28. In the example of Figure 29, the surface of the
25 contact area 7 of the component has been a uncoated component when it was brought to the circuit-module manufacturing process. In such a component, the outer surface of the contact area 7, i.e. the contact surface, is thus typically formed already at the semiconductor factory. In the example of Figure 29, the material of the contact area 7 is aluminium.

30 In the example of Figure 29, the component is attached by a polymer layer 25 to the conductor foil 12, in which contact openings 8 are made in the manner depicted in the

methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the contact area 7, have been made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is made using one or more chemical growing methods, in a corresponding manner to that described above. In the example of Figure 29, the intermediate layer 2 is made in several parts and comprises several layers. In Figure 28, the intermediate layer is, in addition, to facilitate the description, divided into three parts, a base part 36, a wall part 37, and a conductor part 38. The base part 36 is the part that grows on the surface of the contact terminal 7, 17 to the bottom of the contact hole 18, 28, the wall part 37 is the part that grows on the surfaces of the side walls of the contact hole 18, 28, and the conductor part 38 is the part that grows to form part of the conductor 22 being manufactured.

The intermediate layer 2 of Figure 29 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. In the example of Figure 29, the conductor foil 12 is of copper, so that when using a zincate process the first intermediate layer 33 grows only on the base part 36 of the intermediate layer 2. From this, manufacture can be continued, for example, by using a chemical nickel-growing method to make the second intermediate layer 34. The nickel grows on both the base part 36 and the conductor part 38 of the intermediate layer and, when using some growing methods, on the wall part 37 too on the surface of the polymer 25. The third intermediate layer 35 is made from copper on top of the second intermediate layer 34 using a chemical growing method, so that the copper grows on the base part 36, the wall part 37, and the conductor part 38. A layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element.

In the case of Figure 29, it should be noted that, in the finished circuit module, the layers 33 and 34 do not have precise boundaries as shown in the figure, but instead the layers can appear as overlapping or mixed, for example, from the effect of diffusion. For example, in the case of the first intermediate layer 33 containing zinc, the zinc can be located as a concentration profile in the interface between the aluminium and nickel 34

and partly inside the aluminium 7 and the nickel layer 34.

In the contact structure of Figure 29, other material combinations can also be used. For example, suitably selected intermediate-layer structures from the intermediate-layer constructions 1 - 7 described above can be used to form the contact structure depicted by Figure 29 and also the contact structures depicted by Figures 30 - 33. In addition, the contact structure of Figure 29 can also be manufactured with the aid of the materials shown by Figure 28, in such a way that the first intermediate layer 33 and the second intermediate layer 34 are made by sputtering. In that case, the sputtered intermediate layers 33 and 34 will grow to the base part 36 and the conductor part 38, but not to any substantial extent to the wall part 37, provided the contact hole 18, 28 does not widen towards the contact opening 8. One possibility is to use a first intermediate layer 33 containing zinc and on the surface of this either directly a third intermediate layer 35 made from nickel by a chemical growing method, or a construction, in which a second intermediate layer 34 made from nickel-aluminium is used between the layers 33 and 35. In such an embodiment, there is no need at all of chemical copper growing, as the nickel forms a vertical contact along the side wall of the contact hole.

Figure 30 shows yet another contact-element structure. In the structure of Figure 30, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel-aluminium and the third intermediate layer 35 is of nickel grown by a chemical growing method. This, in the structure of Figure 30, the contact hole is filled with nickel, i.e. the conductor core 29 of the contact element is nickel. Otherwise, the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 30.

Figure 31 shows yet another contact-element structure. In the structure of Figure 31, the intermediate layer 2 comprises a first intermediate layer 33 and a second intermediate layer 34. The first intermediate layer 33 can be manufactured, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate

layer 34 is of copper grown by a chemical growing method, or alternatively of nickel grown by a selective chemical growing method. Alternatively, the structure of Figure 31 can also be made in such a way that the first and second intermediate layers 33 and 34 are replaced with a single layer of chemically grown nickel. The conductor core 29 is typically copper and the conductor 22 comprises a first and second copper layer 12 and 32. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 31.

Figure 32 shows yet another contact-element structure. In the structure of Figure 32, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method, the growing method is selective, in such a way that the nickel grows on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 32 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 32.

Figure 33 shows yet another contact-element structure. The method described in connection with Figures 10 - 17, for example, in which a photo-resist layer 30 is used, can be used for making the structure of Figure 32. In the structure of Figure 33, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method of the example, the growing method is selective, in such a way that the nickel grows only on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 33 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with

Figures 28 and 29 apply in the case of the structure of Figure 33.

Thus, in the embodiments a method is presented for the manufacture of a circuit module, in which method

- 5
 - a conductor foil 12 is taken,
 - a component 6, which comprises contact areas 7, the material of which contains a first metal, is taken,
 - 10
 - the component 6 is attached to a conductor foil 12 by means of a polymer layer 25,
 - an insulator layer 1 is manufactured around the component 6 attached to the conductor foil 12,
 - 15
 - contact holes 18, 28 are made in the polymer layer 25 at the positions of the contact areas 7, in such a way that the contact surface area A_{CONY1} between each contact hole 18, 28 and the corresponding contact area 7 is less than the surface area A_{PAD} of the contact area 7, and
 - 20
 - an intermediate layer 2, which contains at least a third metal, is grown at least on the surface of the contact areas 7 in the contact holes 18, 28, and
 - 25
 - a layer 32 of a second metal is grown, which layer 32 is in contact with the surface of the intermediate layer 2 and extends along the conductors 22 being made, and
 - conductors 22 are formed by patterning the conductor foil 12, and, if necessary, also the intermediate layer 2 on the surface of the conductor foil 12 and/or the layer 32 of a second metal.
 - 30

In a typical embodiment, the contact holes 8 are made in the conductor foil 12 before

attaching the component, so that the component is thus attached to a conductor foil 12 equipped with contact openings. In the commonest form of this type of embodiment, the contact openings do not extend to the surfaces of the contact areas 7, so that after the attaching of the component 6 contact holes 18, 28 are further opened through the contact openings 8.

In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.

In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.

When making the intermediate-layer construction, at least one chemical growing method is typically used.

The embodiments depict a circuit module, which comprises

- an insulator layer 1,
- inside the insulator layer 1, at least one component 6, which comprises contact areas 7, the material of which contains a first metal,

- on the surface of the insulator layer 1, conductors 22, which comprise at least a first layer 12 and a second layer 32, in such a way that at least the second layer 32 contains a second metal, and
 - 5 - contact elements for forming electrical contacts between the contact areas 7 and the conductors 22, which contact elements comprise an intermediate layer 2, which contains a third metal, on the surface of the material of the contact area 7,
 - in which the first, second, and third metals are different metals, and
 - 10 - the contact surface area $A_{COT\ 1}$ between the intermediate layer 2 and the contact area 7 is less than the surface area A_{PAD} of the contact area.
- In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.
- 15 In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.
- 20 In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.
- 25 In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.
- 30 In a typical embodiment, the contact elements comprise a copper core 29 made using an electrochemical growing method, which, in the direction of the side walls and the component 6 is bounded by the intermediate layer 2 and in the direction of the conductor

22 connects continuously, i.e. without an interface to the material of the second layer 32 of the conductor 22. In other words, the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is manufactured in the same process, so that the parts are attached permanently to each other and there is no interface
 5 between them. Between the first layer 12 and second layer 22 of the conductor, on the other hand, there is typically an interface, or a corresponding transition zone, which can be detected, for example, by analysing the crystalline structure or impurity concentration of the metal.

10 In one embodiment, the width W_{CONT} of the contact surface between the contact element and the contact area 7 of the component is 0 - 20 % less than the greatest width W_{MAX} of the contact element in the same direction.

The contact elements usually fill entirely the contact holes 18, 28, i.e. the contact
 15 elements are not hollow, but are solidly of conductor material.

Usually, the aim in the embodiments is for the height H of the contact element to be less than, or equal to the greatest width W_{MAX} of the contact element.

20 There are also embodiments of the circuit module, in which the insulator layer 1 includes at least one layer of fibre material 19, in which there is an opening in the fibre material 19 for the component 6, as well as a uniform polymer layer, which is attached to the fibre material 19 and to the components 6, 16.

25 The manufacturing processes described above and their sub-processes can be modified in many ways. For example, the use of an actual adhesive depicted above in attaching the component to the conductor foil 12 can be replaced with some other adhesion mechanism. On example that can be given is the use of an insulator layer 13 possessing an adhesion property on the surface of the conductor foil 12 (see Figure 1 and the
 30 corresponding description). The components 6 are then pressed directly against the insulator layer 13, so that the components attach sufficiently in place in a manner correspondingly to that described in connection with the embodiment using adhesive.

Such an insulator layer 13 can contain, for example, a tape-like surfacing, or consist of a polymer or similar material that is shapable at least in its surface part.

5 The method can also be implemented without the use of an adhesive 5 or an adhesion property. In that case, the components 6 can be attached in place, for example, mechanically or with the aid of a vacuum. The vacuum or similar temporary attachment can then be maintained until the component 6 is sufficiently secured in place with the aid of the insulator material 1.

10 The component 6 to be attached can be, for example, an integrated circuit, such as a memory chip, processor, or ASIC. The component to be attached can also be, for example, a MEMS, LED, or passive component. The component to be attached can be cased or uncased and its contact terminals can consists of contact areas 7, contact bumps 17, or similar. There can also be a conductor coating thinner than an actual contact bump
15 on the surface of the contact areas of the component.

A different material of the insulator layer 1 from those in the examples described above can also be selected. The insulator layer 1 can be manufactured from a suitable polymer or from a material containing polymer. The material of manufacture of the insulator
20 layer 1 can be, for example, in a liquid or pre-hardened form (such as prepreg). In the manufacture of the insulator layer 1 it is possible to use, for example, glass-fibre reinforced sheet, such as an FR4 or FR5-type sheet. Other examples of materials, which can be used in the manufacture of the insulator layer 1 are PI (polyimide), aramide, polytetrafluoroethylene, and Teflon®. Instead of, or as well as thermosetting plastics,
25 thermoplastics too, for example some suitable LCP (liquid crystal polymer) material can be used in the manufacture of the insulator layer 1.

In addition, it is obvious to one skilled in the art that the features described above of the invention can be used as part of some larger totality, for example, in such a way that the
30 electronics module is manufactured partly using some method according to the prior art and partly using the embodiments depicted here. It is also possible to manufacture additional circuit-board layers on the surface or surfaces of the electronic-module

structures described above, or also to attach components, for example, by means of the surface-mounting technique.

5 One skilled in the art will also understand that, when reference is made in the present document to a specific material, for example, aluminium, nickel, or copper, the reference is to a material, which in terms of the application is substantially of the said material. The material referred to can thus, in addition to the said principal element contain, from the point of view of the application, insubstantial amounts of impurities and other elements. For example, an aluminium contact area is usually of a material that typically
10 contains a minimum of 95 % aluminium.

When, on the other hand, reference is made to a material containing some specific element, this means that the material contains an essentially large content of the said element. In addition, the material can contain substantial or insubstantial amounts of
15 other elements. For example, the layer containing zinc will thus contain an amount of zinc that is of significance in terms of the contact properties between the aluminium and the next metal.

The examples given above depict some possible methods and structures, which the aid
20 of which our invention can be exploited. However, our invention is not restricted to only the examples and embodiments described above, but instead the invention covers numerous other methods and structures, taking into account the full scope of the Claims and the equivalence interpretation.

Claims:

1. Method for manufacturing a circuit module, the method comprising

5 taking a conductor foil (12),

making contact openings (8) in the conductor foil (12) for the manufacture of contact elements,

10 taking a component (6), which comprises contact areas (7), the material of which contains a first metal,

attaching the component (6) to the conductor foil (12) by means of a polymer layer (25),

15 manufacturing an insulator layer (1) around the component (6) attached to the conductor foil (12),

20 making contact holes (18, 28) in the polymer layer (25) at the positions of the contact areas (7), in such a way that the contact surface area ($A_{CONT\ I}$), between each contact hole (18, 28) and the corresponding contact area (7) is less than the surface area (A_{PAD}) of the contact area (7), and

25 growing an intermediate layer (2) at least on the surface of the contact areas (7) in the contact holes (18, 28), the intermediate layer (2) containing at least a third metal, and

30 growing a layer (32) of a second metal, which layer (32) is in contact with the surface of the intermediate layer (2) and extends along the conductors (22) being made, and

forming conductors (22) by patterning the conductor foil (12), and, if necessary,

also the intermediate layer (2) on the surface of the conductor foil (12) and/or the layer (32) of a second metal.

2. Method according to Claim 1, in which

5

the contact openings (8) are manufactured before the attachment of the component (6),

the component (6) is attached to a conductor foil (12) equipped with contact
10 openings, and

after the attachment of the component (6), contact holes (18, 28) are opened through the contact openings (8).

15 3. Method according to Claim 2, in which the contact holes (18, 28) are opened through the contact openings (8) using a CO₂ laser, in which case the conductor foil (12) is used as a mask.

20 4. Method according to any of Claims 1 - 3, in which the first metal is aluminium, the second metal is copper, and the third metal contains at least one of the metals zinc and nickel.

5. Method according to any of Claims 1 - 3, in which the first metal is gold, the second metal is copper, and the third metal is nickel.

25

6. Method according to any of Claims 1 - 4, in which the intermediate layer (2) comprises a layer (33) containing zinc, which is manufactured using a double zincate process.

30 7. Method according to any of Claims 1 - 6, in which the intermediate layer (2) comprises a layer (34) containing nickel, which is manufactured using a chemical nickel-growing method.

8. Method according to any of Claims 1 - 7, in which the intermediate layer (2) comprises a layer (35) containing copper, which is manufactured using a chemical copper-growing method.

5

9. Method according to any of Claims 1 - 8, in which the insulator layer (11) is manufactured in such a way that

at least one insulator sheet (11) containing a fibre material (19) and a pre-hardened polymer is taken,

10

a hole for the component (6) is made in the insulator sheet (11) containing a fibre material (19), and

15

the insulator sheet (11) or insulator sheets (11) are laminated together with the conductor foil (12) and its related structures.

10. Method according to any of Claims 1 - 9, in which the surface of the conductor foil (12), to which the component (6) is attached, comprises a uniform insulator layer (13).

20

11. Method according to any of Claims 1 - 10, in which a spacer (15) is placed between the component (6) and the conductor foil (12).

12. Method according to any of Claims 1 - 11, in which, in addition to the component (6), at least one other component (16) is located in the circuit module, in such a way that the manners of attachment of the first and second components differ from each other in the case of at least one property of the polymer layer (25).

25

13. Method according to any of Claims 1 - 12, in which the component (6) to be attached is a bumpless component.

30

14. Circuit module, which comprises

an insulator layer (1),

inside the insulator layer (1), at least one component (6), which comprises
5 contact areas (7), the material of which contains a first metal,

on the surface of the insulator layer (1), conductors (22), which comprise at least
a first layer (12) and a second layer (32), in such a way that at least the second layer (32)
contains a second metal, and
10

contact elements between the contact areas (7) and the conductors (22) for
forming electrical contacts, which contact elements comprise an intermediate layer (2),
which contains a third metal, on the surface of the material of the contact area (7),

15 wherein the first, second, and third metals are different metals, and

the contact surface area ($A_{CONT\ I}$) between the intermediate layer (2) and the
contact area (7) is less than the surface area (A_{PAD}) of the contact area.

20 15. Circuit module according to Claim 14, in which the first metal is aluminium, the
second metal is copper, and the third metal is at least one of the metals zinc and nickel.

16. Circuit module according to Claim 14, in which the first metal is gold, the second
metal is copper, and the third metal is nickel.

25 17. Circuit module according to Claim 14 or 15, in which the material of the contact
areas (7) is mainly aluminium.

18. Circuit module according to Claim 14, 15, or 17, in which the intermediate layer (2)
30 comprises a layer (33) containing zinc.

19. Circuit module according to Claim 18, in which the intermediate layer (2) comprises,

in addition to the layer (33) containing zinc, at least one second intermediate metal layer (34, 35).

20. Circuit module according to Claim 19, in which the at least one second intermediate metal layer (35) is of copper grown by a chemical growing process.

21. Circuit module according to Claim 20, in which the intermediate layer (2) comprises at least one layer (34) of nickel and/or of nickel and aluminium between the layer (33) containing zinc and the copper layer (35).

22. Circuit module according to any of Claims 18 - 21, in which the layer containing zinc contains zinc, copper, nickel, and iron.

23. Circuit module according to any of Claims 14 - 22, in which part of the intermediate layer (2) extends along the side walls of the contact elements between the contact areas (7) and the conductors (22).

24. Circuit module according to Claim 23, in which the contact elements comprise a copper core (29) made using an electrochemical growing method, which, in the direction of the side wall and component (6), is bounded by the intermediate layer (2) and, in the direction of the conductor (22) connects continuously, i.e. without an interface, to the material of the second layer (32) of the conductor (22).

25. Circuit module according to Claim 23 or 24, in which the part (37) of the intermediate layer (2) extending along the side walls of the of the contact elements contains copper grown by a chemical growing method, or nickel grown by a chemical growing method.

26. Circuit module according to any of Claims 14 - 25, in which the conductors (22) comprise

a first layer (12) of copper on the surface of the insulator layer (1), and

a second layer (32) of copper on the surface of the first copper layer.

27. Circuit module according to any of Claims 14 - 25, in which the conductors (22)
5 comprise

a first layer (12) of copper on the surface of the insulator layer (1),

an intermediate layer (2) on the surface of the first copper layer, and
10

a second layer (32) of copper on the surface of the intermediate layer.

28. Circuit module according to Claim 27, in which the part of the intermediate layer (2)
between the first and second coppers layers comprises copper grown by a chemical
15 growing method or nickel grown by a chemical growing method.

29. Circuit module according to any of Claims 14 - 28, in which the width (W_{CONT}) of
the contact surface between the contact element and the contact area (7) of the
component is 0 - 20 % less than the greatest width (W_{MAX}) of the contact element in the
20 same direction.

30. Circuit module according to any of Claims 14 - 29, in which the height (H) of the
contact element is less than, or equal to the greatest width (W_{MAX}) of the contact element.

25 31. Circuit module according to any of Claims 14 - 30, in which the insulator layer (1)
contains at least one layer of fibre material (19), in which there is an opening in the fibre
material (19) for the component (6), as well as a unified polymer layer, which is attached
to the fibre material (19) and to the component (6).

30 32. Circuit module according to any of Claims 14 - 31, which comprises a polymer layer
(25), between the conductors (22) and the component (6), in which layer there are
contact holes (18, 18) for the contact elements, and in which the contact elements fill the

contact holes (18, 28) completely.

33. Circuit module according to Claim 32, in which the polymer layer (25) between the conductors (22) and the component (6) comprises a first (15) and a second (5) polymer layer, in which the first polymer layer (15) is of a first polymer and the second polymer layer (5) is of a hardened adhesive.

34. Circuit module according to Claim 33, in which the first polymer layer (15) and the second polymer layer (5) are local, in such a way that they exist essentially only at the location of the component (6).

35. Circuit module according to any of Claims 14 - 34, in which the component comprises a passivation layer (9) on the surface of the component and the contact areas (7) are located inside openings in the passivation layer, in which case the intermediate layer (2) extends through the opening in the passivation layer.

(57) Abstract:

Manufacturing method and circuit module, which comprises an insulator layer (1) and, inside the insulator layer (1), at least one component (6), which comprises contact areas (7), the material of which contains a first metal. On the surface of the insulator layer (1) are conductors (22), which comprise at least a first layer (12) and a second layer (32), in such a way that at least the second layer (32) contains a second metal. The circuit module comprises contact elements between the contact areas (7) and the conductors (22) for forming electrical contacts. The contact elements, for their part, comprise, on the surface of the material of the contact area (7), an intermediate layer (2), which contains a third metal, in such a way that the first, second, and third metals are different metals and the contact surface area (A_{CONT1}), between the intermediate layer (2) and the contact area (7) is less than the surface area (A_{PAD}) of the contact area (7).

(Figure 8)

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<p>Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.</p> <p>Substitute for form 1449/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(Use as many sheets as necessary)</i></p>				<p>Complete if Known</p>	
				Application Number	
				Filing Date	
				First Named Inventor	Petteri Palm
				Art Unit	
				Examiner Name	
				Attorney Docket Number	IMB 22 US
Sheet	1	of	1		

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
		WO 2006056643 A	06-01-2006	Imbera Electronics Oy		
		EP 1259103 A	11-20-2002	Ibiden Co Ltd		
		EP 0380289 A	08-01-1990	Fujitsu Ltd		
		WO 2009138560	11-19-2009	Imbera Electronics Oy		

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	
	Filing Date	
	First Named Inventor	Petteri Palm
	Title	Circuit Module and Method of Manufacturing
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IMB 22 US

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

95002

OR

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OR

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Address

City State Zip

Country

Telephone Email

I am the:

☒ Applicant/Inventor.

OR

☐ Assignee of record of the entire interest. See 37 CFR 3.71
Statement under 37 CFR 3.73(b)(1) Form PTO/SB/96 submitted herewith or filed on _____

SIGNATURE of Applicant or Assignee of Record

Signature		Date	29.10.2010
Name	Petteri Palm	Telephone	
Title and Company			

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 3 forms are submitted.

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	Filing Date	
	First Named Inventor	Petteri Palm
	Title	Circuit Module and Method of Manufacturing
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IMB 22 US

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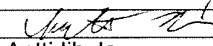
☒ Applicant/Inventor.

OR

☐ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Assignee of Record

Signature		Date	28.10.2010
Name	Antti Iihola	Telephone	
Title and Company			

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POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	
	Filing Date	
	First Named Inventor	Petteri Palm
	Title	Circuit Module and Method of Manufacturing
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IMB 22 US

I hereby revoke all previous powers of attorney given in the above-identified application.

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☒ Applicant/Inventor.

OR

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Applicant or Assignee of Record

Signature	<i>Risto Tuominen</i>	Date	6.10.2010
Name	Risto Tuominen	Telephone	
Title and Company	CTO Imbion Electronics		

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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)****Title of
Invention****CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME**

As the below named inventor(s), I/we declare that:

This declaration is directed to:



The attached application, or



Application No. _____ filed on _____



As amended on _____ (if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

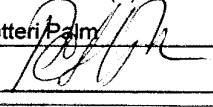
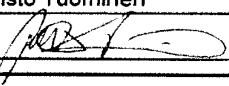
I/we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

All statements made herein of my/our own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF INVENTOR(S)Inventor one: Petteri Palmi Date: 29.10.2010Signature:  Citizen of: FIInventor two: Risto Tuominen Date: 6.10.2010Signature:  Citizen of: FI☒ Additional inventors or a legal representative are being named on 1 additional form(s) attached hereto.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION	ADDITIONAL INVENTOR(S) Supplemental Sheet <div style="text-align: right;">Page <u>2</u> of <u>2</u></div>
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Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Anttl		liholá	
Inventor's Signature		Oct. 28 2010 Date	
Residence: City	State	Country	FI Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country
Name of Additional Joint Inventor, if any:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle (if any))		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	Zip	Country

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5 Appl. No. : Not Yet Assigned Confirmation No. : N/A
 Applicant : Petteri Palm et al.
 Filed :
 TC/AU : Not Yet Assigned
 Examiner : Not Yet Assigned
10 Attorney Docket No. : IMB 22 US

 M/S Preliminary Amendment
15 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

20

PRELIMINARY AMENDMENT

Sir:

25 In connection with the utility patent application filed herewith, which is a
National Phase application based on PCT Application No. PCT/FI2009/050383, please
amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2
30 of this paper.

Remarks/Arguments begin on page 9 of this paper.

35

40

45

REMARKS/ARGUMENTS

Please enter the above amendments prior to calculation of the filing fees. It is believed that no fee is required for the submission of this Preliminary Amendment.

5

Respectfully submitted,

/ Joshua P. Wert Reg. No. 65880/

10

Joshua P. Wert
Reg. No. 65880
Seppo Laine Oy
Itämerenkatu 3 B
FIN-00180 Helsinki, Finland
Tel. (US) +1 571-480-8372
Tel. +358 9 6859 5643
Fax +358 9 6859 5610
e-mail: Joshua.Wert@Seppolaine.fi

15

20

2010-11-01

Amendments to the Claims:

5 This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

- 10 1. (Currently Amended) Method for manufacturing a circuit module, the method comprising:
- 15 taking a conductor foil ~~(12)~~,
 - making contact openings ~~(8)~~ in the conductor foil ~~(12)~~ for the manufacture of contact elements,
 - 20 taking a component ~~(6)~~, which comprises contact areas ~~(7)~~, the material of which contains a first metal,
 - attaching the component ~~(6)~~ to the conductor foil ~~(12)~~ by means of a polymer layer ~~(25)~~,
 - 25 manufacturing an insulator layer ~~(1)~~ around the component ~~(6)~~ attached to the conductor foil ~~(12)~~,
 - making contact holes ~~(18, 28)~~ in the polymer layer ~~(25)~~ at the positions of the contact areas ~~(7)~~, in such a way that the contact surface area ~~(A_{CONTACT})~~, between each contact hole ~~(18, 28)~~ and the corresponding contact area ~~(7)~~ is less than the surface area ~~(A_{PAD})~~ of the contact area ~~(7)~~, and
 - 30 growing an intermediate layer ~~(2)~~ at least on the surface of the contact areas ~~(7)~~ in the contact holes ~~(18, 28)~~, the intermediate layer ~~(2)~~ containing at least a third metal, and
 - 35 growing a layer ~~(32)~~ of a second metal, which layer ~~(32)~~ is in contact with the surface of the intermediate layer ~~(2)~~ and extends along the conductors ~~(22)~~ being made,

and

5 | forming conductors ~~(22)~~ by patterning the conductor foil ~~(12)~~, and, if necessary, also the intermediate layer ~~(2)~~ on the surface of the conductor foil ~~(12)~~ and/or the layer ~~(32)~~ of a second metal.

2. (Currently Amended) Method according to Claim 1, in which

10 | the contact openings ~~(8)~~ are manufactured before the attachment of the component ~~(6)~~,

the component ~~(6)~~ is attached to a conductor foil ~~(12)~~ equipped with contact openings, and

15 | after the attachment of the component ~~(6)~~, contact holes ~~(18, 28)~~ are opened through the contact openings ~~(8)~~.

20 | 3. (Currently Amended) Method according to Claim 2, in which the contact holes ~~(18, 28)~~ are opened through the contact openings ~~(8)~~ using a CO₂ laser, in which case the conductor foil ~~(12)~~ is used as a mask.

25 | 4. (Currently Amended) Method according to ~~any of Claims 1–3~~ Claim 1, in which the first metal is aluminium, the second metal is copper, and the third metal contains at least one of the metals zinc and nickel.

5. (Currently Amended) Method according to ~~any of Claims 1–3~~ Claim 1, in which the first metal is gold, the second metal is copper, and the third metal is nickel.

30 | 6. (Currently Amended) Method according to ~~any of Claims 1–4~~ Claim 1, in which the intermediate layer ~~(2)~~ comprises a layer ~~(33)~~ containing zinc, which is manufactured using a double zincate process.

7. (Currently Amended) Method according to ~~any of Claims 1–6~~ Claim 1, in which the

intermediate layer (2) comprises a layer (34) containing nickel, which is manufactured using a chemical nickel-growing method.

8. (Currently Amended) Method according to ~~any of Claims 1—7~~ Claim 1, in which the intermediate layer (2) comprises a layer (35) containing copper, which is manufactured using a chemical copper-growing method.

9. (Currently Amended) Method according to ~~any of Claims 1—8~~ Claim 1, in which the insulator layer (11) is manufactured in such a way that

at least one insulator sheet (11) containing a fibre material (19) and a pre-hardened polymer is taken,

a hole for the component (6) is made in the insulator sheet (11) containing a fibre material (19), and

the insulator sheet (11) or insulator sheets (11) are laminated together with the conductor foil (12) and its related structures.

10. (Currently Amended) Method according to ~~any of Claims 1—9~~ Claim 1, in which the surface of the conductor foil (12), to which the component (6) is attached, comprises a uniform insulator layer (13).

11. (Currently Amended) Method according to ~~any of Claims 1—10~~ Claim 1, in which a spacer (15) is placed between the component (6) and the conductor foil (12).

12. (Currently Amended) Method according to ~~any of Claims 1—11~~ Claim 1, in which, in addition to the component (6), at least one other component (16) is located in the circuit module, in such a way that the manners of attachment of the first and second components differ from each other in the case of at least one property of the polymer layer (25).

13. (Currently Amended) Method according to ~~any of Claims 1—12~~ Claim 1, in which the component (6) to be attached is a bumpless component.

14. (Currently Amended) Circuit module, which comprises:
- an insulator layer-(1),
- inside the insulator layer-(1), at least one component-(6), which comprises contact areas-(7), the material of which contains a first metal,
- on the surface of the insulator layer-(1), conductors-(22), which comprise at least a first layer (12)-and a second layer-(32), in such a way that at least the second layer (32)-contains a second metal, and
- contact elements between the contact areas (7)-and the conductors (22)-for forming electrical contacts, which contact elements comprise an intermediate layer-(2), which contains a third metal, on the surface of the material of the contact area-(7),
- wherein the first, second, and third metals are different metals, and
- the contact surface area (~~$A_{CONTACT}$~~)-between the intermediate layer (2)-and the contact area (7)-is less than the surface area (~~A_{PID}~~)-of the contact area.
15. (Original) Circuit module according to Claim 14, in which the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.
16. (Original) Circuit module according to Claim 14, in which the first metal is gold, the second metal is copper, and the third metal is nickel.
17. (Currently Amended) Circuit module according to Claim 14-or-15, in which the material of the contact areas (7)-is mainly aluminium.
18. (Currently Amended) Circuit module according to Claim 14, 15, or 17, in which the intermediate layer (2) comprises a layer (33)-containing zinc.

19. (Currently Amended) Circuit module according to Claim 18, in which the intermediate layer (2) comprises, in addition to the layer (33) containing zinc, at least one second intermediate metal layer (34, 35).
- 5 20. (Currently Amended) Circuit module according to Claim 19, in which the at least one second intermediate metal layer (35) is of copper grown by a chemical growing process.
21. (Currently Amended) Circuit module according to Claim 20, in which the intermediate layer (2) comprises at least one layer (34) of nickel and/or of nickel and aluminium
10 between the layer (33) containing zinc and the copper layer (35).
22. (Currently Amended) Circuit module according to ~~any of Claims 18–21~~ Claim 18, in which the layer containing zinc contains zinc, copper, nickel, and iron.
- 15 23. (Currently Amended) Circuit module according to ~~any of Claims 14–22~~ Claim 14, in which part of the intermediate layer (2) extends along the side walls of the contact elements between the contact areas (7) and the conductors (22).
24. (Currently Amended) Circuit module according to Claim 23, in which the contact
20 elements comprise a copper core (29) made using an electrochemical growing method, which, in the direction of the side wall and component (6), is bounded by the intermediate layer (2) and, in the direction of the conductor (22) connects continuously, i.e. without an interface, to the material of the second layer (32) of the conductor (22).
- 25 25. (Currently Amended) Circuit module according to Claim 23 ~~or~~ 24, in which the part (37) of the intermediate layer (2) extending along the side walls of the of the contact elements contains copper grown by a chemical growing method, or nickel grown by a chemical growing method.
- 30 26. (Currently Amended) Circuit module according to ~~any of Claims 14–25~~ Claim 14, in which the conductors (22) comprise;
- a first layer (12) of copper on the surface of the insulator layer (1), and

- a second layer (32) of copper on the surface of the first copper layer.
27. (Currently Amended) Circuit module according to ~~any of Claims 14–25~~ Claim 14, in which the conductors (22) comprise;
- a first layer (12) of copper on the surface of the insulator layer (1),
- an intermediate layer (2) on the surface of the first copper layer, and
- a second layer (32) of copper on the surface of the intermediate layer.
28. (Currently Amended) Circuit module according to Claim 27, in which the part of the intermediate layer (2) between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.
29. (Currently Amended) Circuit module according to ~~any of Claims 14–28~~ Claim 14, in which the width (W_{CONT}) of the contact surface between the contact element and the contact area (7) of the component is 0 - 20 % less than the greatest width (W_{MAX}) of the contact element in the same direction.
30. (Currently Amended) Circuit module according to ~~any of Claims 14–29~~ Claim 14, in which the height (H) of the contact element is less than, or equal to the greatest width (W_{MAX}) of the contact element.
31. (Currently Amended) Circuit module according to ~~any of Claims 14–30~~ Claim 14, in which the insulator layer (1) contains at least one layer of fibre material (19), in which there is an opening in the fibre material (19) for the component (6), as well as a unified polymer layer, which is attached to the fibre material (19) and to the component (6).
32. (Currently Amended) Circuit module according to ~~any of Claims 14–31~~ Claim 14, which comprises a polymer layer (25), between the conductors (22) and the component (6), in which layer there are contact holes (18, 18) for the contact elements, and in which the

contact elements fill the contact holes (18, 28) completely.

33. (Currently Amended) Circuit module according to Claim 32, in which the polymer layer (25) between the conductors (22) and the component (6) comprises a first (15) and a second (5) polymer layer, in which the first polymer layer (15) is of a first polymer and the second polymer layer (5) is of a hardened adhesive.

34. (Currently Amended) Circuit module according to Claim 33, in which the first polymer layer (15) and the second polymer layer (5) are local, in such a way that they exist essentially only at the location of the component (6).

35. (Currently Amended) Circuit module according to ~~any of Claims 14–34~~ Claim 14, in which the component comprises a passivation layer (9) on the surface of the component and the contact areas (7) are located inside openings in the passivation layer, in which case the intermediate layer (2) extends through the opening in the passivation layer.

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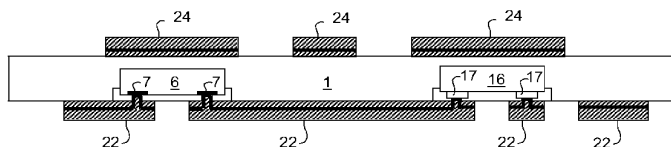


Fig. 8

(57) **Abstract:** Manufacturing method and circuit module, which comprises an insulator layer (1) and, inside the insulator layer (1), at least one component (6), which comprises contact areas (7), the material of which contains a first metal. On the surface of the insulator layer (1) are conductors (22), which comprise at least a first layer (12) and a second layer (32), in such a way that at least the second layer (32) contains a second metal. The circuit module comprises contact elements between the contact areas (7) and the conductors (22) for forming electrical contacts. The contact elements, for their part, comprise, on the surface of the material of the contact area (7), an intermediate layer (2), which contains a third metal, in such a way that the first, second, and third metals are different metals and the contact surface area (A_{CONT1}), between the intermediate layer (2) and the contact area (7) is less than the surface area (A_{PAD}) of the contact area (7).

CIRCUIT MODULE AND METHOD OF MANUFACTURING THE SAME

Technical Field

5 The present invention relates to circuit modules, which comprise an insulator layer and, inside the insulator layer, at least one component, which comprises contact areas. In addition, the circuit modules comprise conductors on the surface of the insulator layer, through which a component can be connected to become part of a circuit outside the component. For creating electrical contacts, the circuit modules comprise contact
10 elements between the contact areas of the component and the conductors.

The invention also relates to methods for manufacturing the aforementioned circuit modules.

15

Background Art

In the background art, several different ways are described, by means of which circuit modules containing components located inside an insulator material can be manufactured. The background art also discloses several solutions for manufacturing
20 electrical contacts to the contact terminals of a component, by means of contact elements, and methods for manufacturing a conductor-pattern layer connected to the contact elements.

When evaluating circuit modules and manufacturing methods, attention can be paid, for
25 example, to the circuit module's properties achieved by the method, for example, its price, mechanical durability, and the thickness (thinness) that can be achieved. Depending on the applications, significant factors can also be the quality and durability of the electrical contacts and the reliability and quality of the electrical properties of the whole module. Significant properties to be examined in terms of manufacturing can also
30 be, for example, the reliability, yield, efficiency, price, and environmental friendliness of the manufacturing methods to be used. The practicability of the manufacturing method is also affected by the availability of raw materials and the ability of the method to place

different types of component in a circuit module.

All in all, the requirements set for manufacturing methods and circuit modules are thus very diverse and vary according to the application. This being the case, there is still a
5 need in the sector to develop new circuit-module structures and manufacturing methods, which can offer new or improved properties, or combinations of properties.

One line of development has been the placing of components inside the electronics module in a bumpless form, i.e. without growing bumps of top of the contact areas of the
10 component. Cost benefits can then be gained, as the components need no longer be transported during manufacture to a separate production plant to make the bumps.

The applicant's own patent and application publications disclose manufacturing techniques, which can also be used in connection with bump-free components. The
15 techniques described are particularly suitable for components, in which the material of the contact areas is copper. Of the applicant's own publications, those that can be referred to as most closely relating to the invention are the international patent application publications WO 2004/089048, WO 2005/027602, WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217, and
20 WO 2007/107630.

However, at present copper is quite little used as a conductor material in semiconductor processes. The most common conductor material is aluminium. In circuit-board manufacture, on the other hand, copper is the principal material for conductors. Copper
25 conductors of a circuit module can be grown directly on top of aluminium contact areas, but the contact between copper and aluminium is brittle, so that a module of this kind is not optimal in applications, in which mechanical stress acts on the circuit module.

An improved possibility to use contact areas of aluminium or contact areas containing
30 aluminium would mean that, in circuit modules and manufacturing methods, normal semiconductor circuits in a bumpless form could be used immediately after the semiconductor manufacturing processes and the passivation of the surface. As

aluminium is the conductor material most widely used in the semiconductor industry, good compatibility between the contact element of the circuit module and aluminium would also ensure that suitable semiconductor circuits would be abundantly and economically available. Attempts to develop such manufacturing methods have indeed
5 already been made for several decades in the field of component packaging technology. In component packaging solutions of this kind, the goal has been a technique, by means of which a relatively small component package could be manufactured around a component, to which a circuit board could then be attached later. Unlike packaging technology, the goal of the manufacturing techniques of the circuit module to which the
10 present invention relates is the ability to manufacture the entire circuit board in the same process, so as to completely eliminate the packaging stage of the separate component. Of course, this does not exclude the possibility of using the manufacturing method of the circuit module to manufacture only a component package.

15 The patent US 4 246 595, Noyori et al., discloses a method, in which the contact areas of a component are brought into contact with an insulator sheet, in which V-shaped openings have been made. First of all, a layer of titanium (Ti) or chromium (Cr) is grown on the surfaces of the openings and the aluminium contact areas. This intermediate metal layer is intended to prevent the copper from diffusing into the
20 aluminium and the semiconductor component, as well as to improve the adhesion between the copper and the aluminium. In addition, the intermediate layer acts as an electrical conductor later during electrochemical growing (electroplating), so that the intermediate metal layer will reliably cover also the side walls of the openings. The growing of the titanium or chromium layer requires the use of the sputtering technique,
25 for which reason the openings must also have a clear V shape. Sputtering is expensive when used on large surfaces (on circuit modules) while additionally the open V shape reduces the available conducting density. Contract structures of a corresponding type are also disclosed in patents US 4 783 695 and US 4 894 115, Eichelberger et al., and in patent US 5 353 195, Fillion et al.

30 Later, in patent US 6 396 148, Eichelberger et al., an attempt is made to solve the problems relating to sputtering, by forming the intermediate metal layer by growing a

layer of nickel on the surface of the aluminium contact areas. According to the patent, the growing of the nickel is performed by means of a chemical growing method (electroless plating). Yet another layer, which also covers the side walls of the openings made in the insulating material for the contacts, is growing on top of the nickel layer by means of a chemical growing method. In the method, the components are attached first by their side and rear surfaces to the insulator layer and, after this, a photo-patternable polymer is spread on the front surface of the component and on top of the contact areas. The polymer is patterned by exposing it to light and developing it, to form openings for the contacts.

One possibility is to grow bumps on the surface of the conductors of the circuit-board part of the circuit module and attach the component to the conductors by a flip-chip mounting technique, for example, by ultrasound bonding. Such a method is disclosed in the applicant's own international patent application WO 2006/134220. Problems relating to both production and the quality of the contacts are associated with methods using flip-chip methods.

Disclosure of Invention

The object of the invention is to develop a new contact-element structure envisaging the utilization of bumpless components, as well as a circuit module and manufacturing technique using such a structure.

According to an aspect of the invention, a bumpless component is used in the circuit module, the material of the contact areas of which being of a different metal, or metal alloy to the conductors of the conductor layer of the circuit module. The contact areas of the component and the conductors of the circuit module are connected to each other with the aid of contact elements, which contain an intermediate layer, which contains a third metal or metal alloy, which differs from the material of the contact areas and conductors, on the surface of the material of the contact area. In addition, the contact surface area between the intermediate layer of each contact element and the contact area of the component is smaller than the surface area of the contact area.

According to another aspect of the invention, a manufacturing method is created in order to manufacture the circuit module described above, in which the component is attached to a conductor foil or conductor-pattern layer with the aid of a polymer layer and contact elements are made through the polymer layer. When making the contact elements, contact holes are made in the polymer layer on top of the contact areas, at the locations of the contact areas. The contact holes are dimensioned in such a way that the contact surface area between each contact hole and the corresponding contact area is smaller than the total surface area of the contact area. After this, the contact holes are filled with a conductor material, in such a way that filling is started by coating the surface of the contact areas with an intermediate layer, for example, by using one or more chemical metal-growing methods.

Thus, a new type of circuit module and manufacturing method is obtained, which can offer some advantages in terms of the applications of some circuit modules.

In addition, the invention has numerous special embodiments, which provide additional advantages.

In one embodiment, components are used in the circuit module, the material of the contact areas of which contains aluminium and the contact elements comprise a layer containing zinc on the surface of these contact areas containing aluminium. In addition, the contact elements are manufactured in such a way that the contact surface area between the layer containing zinc and the contact area is smaller than the total surface area of the actual contact area.

A layer containing zinc has been observed to be useful in terms of the quality of the electrical contact, as coating a layer containing zinc on the surface of an aluminium contact area prevents the re-oxidation of the aluminium surface and permits the creation of good adhesion between the aluminium and the next layer. In addition, the layer containing zinc improves the mechanical durability against lateral stress of the contact formed through the interface between the aluminium and the intermediate layer of other

metal.

5 We have observed that extremely good mechanical durability is achieved by using a double zincate process, in which the blank containing the components is subjected to the zincate process at least twice. Thus a more even and denser layer of zinc is made to grow on top of the aluminium contact surfaces. After a single zincate treatment, there is zinc on only some areas of the contact surfaces, or else the layer is porous, therefore a double zincate process is used in the preferred embodiment.

10 The possibility to use contact elements that are narrower than the contact area can, for its part, provide advantages, for example, by allowing the conductors connected to the contact elements to also be made narrow, especially in embodiments, in which the contact element is essentially of even width vertically, or only narrows moderately towards the component.

15 In an embodiment of the manufacturing process, in which contact openings are made in the conductor foil of the conductor-pattern layer prior to attaching the component, the component can be attached aligned relative to the contact openings while, in addition, the contact holes needed for the manufacture of the contact elements can be made through these contact openings, by using the material of the conductor foil or conductor-pattern layer as a mask. In such an embodiment, an advantage is obtained in the case of the alignment between the contact elements and the contact areas. In addition, an advantage is obtained in terms of the manufacture of the contact holes, because the holes can be opened using a CO₂ laser, for example.

25 In an embodiment, in which the contact holes are opened using a laser, the contact holes can be opened one component or component-group at a time, and thus the first intermediate layer can be manufactured first through the contact holes, on top of the contact areas of the first components, and then later the second intermediate layer can be manufactured through the contact holes opened later, on top of the contact areas of the second components. Thus, components, the materials of the contact areas of which differ from each other and are incompatible with the growth processes of the same

30

intermediate layer, can be fitted in the same process.

In the embodiments, it is also possible to attach the components to the conductors by means of mutually differing polymer layers. Thus the properties of the insulation
5 between the component and the conductor can be arranged to also be suitable for different mechanical and electrical requirements.

Brief Description of Drawings

10 Figures 1 - 8 show the intermediate stages of a circuit module when using a manufacturing method according to one embodiment.

Figure 9 shows one example of a circuit module according to one embodiment.

15 Figures 10 - 17 show the intermediate stages of a circuit module when using a manufacturing method according to a second embodiment.

Figures 18 - 23 show the intermediate stages of a circuit module when using a manufacturing method according to a third embodiment.

20 Figure 24 shows one intermediate stage of a circuit module when using a manufacturing method according to a fourth embodiment.

Figure 25 shows one possible example of a contact hole and its dimensions made for a
25 contact element of a circuit module.

Figure 26 shows examples of possible contact holes.

Figure 27 shows some embodiments of intermediate layers manufactured in the contact
30 hole of Figure 26.

Figure 28 shows one contact-element structure.

Figure 29 shows a second contact-element structure.

Figure 30 shows a third contact-element structure.

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Figure 31 shows a fourth contact-element structure.

Figure 32 shows a fifth contact-element structure.

10

Figure 33 shows a sixth contact-element structure.

Modes for Carrying Out the Invention

15 Figures 1 - 9 show one exemplary application of the manufacturing method according to one embodiment. In this embodiment, manufacture begins from a conductor foil 12, which of metal, for example. A suitable conductor foil 12 is, for example, a copper film, the thickness of which is in the range 1 - 70 μm , typically in the range 3 - 12 μm . Instead of a bare conductor foil 12, it is also possible to use as the base material a layered sheet, which comprises a conductor foil 12 and an insulator layer 13, which is shown by a
20 broken line in Figure 1, on the surface of this. In the embodiments described in the following, it is possible to use such a layered sheet 12, 13, in place of the conductor foil 12.

25 Differing from what is shown in Figure 1, it is also possible to use a layered sheet, which comprises a support membrane on the second surface of the conductor foil 12. The support membrane is on the opposite surface of the conductor foil relative to the components to be attached to the conductor foil. If the layered sheet also comprises an insulator layer 13, the support membrane will then be on the opposite side of the conductor foil to the insulator membrane 13. The support membrane can be used, for
30 example, to improve the mechanical stiffness and ease of handling at the start of the manufacturing process of the conductor foil 12, or the layered sheet 12, 13. The support membrane is, however, intended to be removed at a later stage in the process. It is also

possible to proceed by starting manufacture from a support membrane while a conductor foil 12, which is patterned or unpatterned, is made on the surface of this. The process examples and stages described in the application example can also be performed correspondingly when using a support membrane, though this is not stated separately. In the description hereinafter, however, reference will be made to a support membrane only when calling attention to something particularly noteworthy in the case of an embodiment using a support membrane. The actual support membrane can be, for example, of an electrically conductive material, such as aluminium (Al), steel, or copper, or an insulating material, such as a polymer. The thickness of the support membrane can be, for example, 25 - 400 μm . The thickness of the support membrane is typically in the range 35 - 105 μm .

Next, contact openings 8 are made in the conductor foil 12, which are located on the conductor foil 12 in such a way that they are placed at the positions of the contact terminals of the components being placed in the module being manufactured. Thus, an individual contact opening 8 is made in the conductor foil 12 for each contact terminal of the component. In this embodiment, the contact openings 8 can be manufactured with the aid of a UV laser. The contact openings 8 can also be manufactured, for example, mechanically by drilling, milling, or etching. In an embodiment using a support membrane, the contact openings 8 are preferably made from the direction of the opposite surface, in such a way that they penetrate the conductor foil 12 completely. However, the contact openings need not penetrate the sheet, instead the method can equally well also be designed in such a way that the contact openings 8 only extend as far as the surface of the material of the support membrane, or form recesses in the material of the support membrane, without, however, passing entirely through it. Also, the contact openings need not pass entirely through the conductor foil, if a thick conductor foil is used, which is thinned by etching in a later stage.

In the embodiment of Figure 1, the contact openings 8 are manufactured in such a way that the size of a contact opening 8 is less than the contact surface area of the contact material to be placed at the opening 8. The contact opening is typically circular in shape, though other shapes too can be used. The shape and size of the contact opening 8 are

selected in such a way that the contact surface of the contact terminal can cover the contact opening 8 entirely.

5 According to Figure 2, manufacture is continued by spreading adhesive layers 5 on the surface of the conductor foil 12, in the connection areas of the components. The adhesive layers will then also cover the contact openings 8. Alternatively, the adhesive 5 can be spread on the surface of the components. The adhesive can also be spread on the surface of both the component and the conductor foil 12. Typically, the adhesive is spread locally, so that the adhesive layers 5 will be located only in the connection areas
10 of the components.

The term adhesive refers to a material, by means of which the components can be attached to the conductor foil 12 or insulator layer 13 that acts as a base. One property of the adhesive is that the adhesive can be spread on the surface to be glued in a relatively
15 fluid form, or one that otherwise conforms to the surface shapes, for example, in the form of a film. A second property of the adhesive is that, after spreading, the adhesive hardens, or can be hardened, at least partly, in such a way that the adhesive is able to hold the component in place (relative to the conductor foil 12) at least until the component is secured to the construction in some other way. A third property of the
20 adhesive is an adhesive capability, i.e. an ability to stick to the surfaces being glued.

The term gluing, for its part, refers to the attachment of pieces to be glued to each other with the aid of an adhesive. In the embodiments, the adhesive is brought between the component and the conductor foil 12 or insulator layer 13 acting as a base and the
25 component is placed in a suitable position relative to the base, in which the adhesive is in contact with the component and the base and at least partly fills the space between the component and the base. After this, the adhesive is allowed (at least partly) to harden, or the adhesive is (at least partly) actively hardened, so that the component attaches to its base with the aid of the adhesive. In some embodiments, the contact protrusions of the
30 component may protrude during gluing through the adhesive layer to come into contact with the base.

The adhesive used in the embodiments is typically an epoxy-based adhesive, for example a heat-cured epoxy adhesive. The adhesive is selected in such a way that the adhesive to be used will have sufficient adhesion to the base and the component. One preferred property of the adhesive is a suitable coefficient of thermal expansion, so that
5 the thermal expansion of the adhesive will not differ too much from the thermal expansion of the surrounding material during the process. It would also be preferable for the adhesive selected to have a short hardening time, preferably of a few seconds at most. Within this time, it would be good for adhesive to harden at least partly, so that the adhesive can hold the component in place. Final hardening can take a clearly longer time
10 and can even be planned to take place in connection with later process stages. In addition, the stresses caused by the later process stages, such as thermal, chemical, or mechanical stress, are taken into account when selecting the adhesive. The electrical conductivity of the adhesive will be preferably in the order of the electrical conductivity of the insulator materials.

15
Next, components 6 and 16, which comprise contact terminals 7 and 17, are taken. Both components 6 and 16 are semiconductor components, for example, processors, memory chips, or other microcircuits. The contact terminals of the component 6 are contact areas 7, which are located essentially on the level of the surface of the component. Such
20 contact areas 7 of the component 6 are created at the semiconductor factory during the manufacturing process of the semiconductor component. The contact area 7 typically forms the surface of a conductor pattern on the metal used in the process. The metal used in the manufacturing process of semiconductor components is typically aluminium, though other metals, metal alloys, or other conductor materials can also be used. For
25 example, the use of copper has become common in semiconductor-component manufacturing processes.

The contact terminals of the component 16 are contact bumps 7, which protrude from the level of the surface of the component. Such contact bumps 17 are manufactured in a
30 bump-making process after the manufacture of the semiconductor component 16, typically in a separate factory. The contact bump 17 can contain one or more metals, metal alloys, or other conductor materials. Typically, the outer surface of the contact

bump 17, i.e. the contact surface, is made from copper or gold.

5 The components 6 and 16 are aligned relative to the contact openings 8, in such a way that each contact terminal 7, 17 comes next to the corresponding contact opening 8, and is pressed against the adhesive layer 5. After this, the adhesive is at least partly hardened, so as to prevent, or minimize the relative movement of the components 6, 16 and the conductor foil 12 after alignment. In alignment and gluing, the aim is to position the contact opening 8 to be in the centre of the corresponding contact terminal 7, 17.

10 After this, insulator sheets 11, in which openings are made for the components 6, 16, as well as a unified insulator sheet 10, which is of unhardened or pre-hardened polymer, are laminated on top of the conductor foil 12. During lamination, the insulator sheets 10, 11 are melted together and form a unified insulator layer 1 around the components 6, 16. In the embodiment of Figure 2, the insulator sheets 11 are fibre mats impregnated with polymer, or sheets containing pre-hardened polymer and reinforced with a fibre material.
15 The polymer can be, for example, epoxy and the fibre reinforcement can be, for example, glass-fibre mat. A typical example of a suitable insulating-sheet 11 material is an FR4-type glass-fibre reinforced epoxy sheet. Other reinforcement and polymer material combinations can be used, of course. When using several insulator sheets 11,
20 the sheets can also differ mutually.

In Figures 2 and 3, the fibre material is shown by wavy shading 19. In the figures hereinafter, the fibre material 19 is not shown, but these structures too include fibre material 19. The fibre material 19 contained in the insulator sheet 11 or the insulator sheets 11 acts as a reinforcement, which provides the electronic module being
25 manufactured with mechanical strength. According to the example of Figure 2, holes 4 are made in the insulator sheets 11 at the locations of the components 6, 16. The insulator sheets 11 are perforated particularly to make openings for components in the fibre material 19 contained in the insulator sheets 11. Without perforation, the components would press against the fibre-material layers 19 during lamination. The
30 unperforated insulator sheet 10, on the other hand, can be fibre-reinforced or unreinforced, depending on the embodiment.

The insulator sheets 10, 11 are typically selected in such a way that they contain enough fluid polymer for the polymer flowing in the lamination stage to be sufficient to fill the holes 4 made in the insulator sheets 11 for the component 6, 16, around the components.

5 The structure shown in Figure 3 is then obtained, in which the insulator layer 1 contains a tight polymer layer, which contains one or more reinforcements of a fibre material 19. The polymer layer is bound tightly to the fibre layer 19 while the tight polymer layer also attaches the components 6, 16 to the surfaces, so that a tight, unified, and mechanically strong insulator layer is formed, which contains the components 6, 16, and
10 which is, in addition, reinforced with fibre material 19.

In the example of Figure 2, a unified insulator sheet 10 is used, though the insulator sheet 10 can also be omitted from the structure. In that case, the insulator sheet 11 or insulator sheets 11 are selected in such a way that they themselves already contain
15 sufficient fluid polymer to fill the holes 4 in the insulator sheets 11 around the components 6, 16. However, it is typically easier to ensure the filling of the holes 4 by using a separate insulator sheet 10.

A conductor foil 14, which is preferably of a material that is similar to, and equally as
20 thick as the conductor foil 12, is also laminated with the insulator sheets 10, 11 into a single structure. Thus, the insulator layer 1 and the components 6, 16 remains between the corresponding conductor foils 12 and 14. Figure 3 shows this intermediate stage of the module manufacture. In the intermediate stage of Figure 3, there is adhesive on the contact surface of the contact terminals 7, 17 and typically also in the contact openings
25 18. In the stage shown in Figure 4, this adhesive is removed and contact holes 18, which extend to the contact surfaces of the contact terminals 7, 17 are formed at the positions of the contact openings 8.

With reference to Figure 3, it can be further stated that the structure can also be
30 manufactured in such a way that a unified layer of fibre material 19 runs between the components 6, 16 and the conductor foil 14. Such a construction can be used when the thickness of the components 6, 16 is sufficiently less than the thickness of the insulator

layer 1. The structure can be manufactured, for example, in such a way that a unified insulator sheet 10, which contains the fibre material 19 of the layer, can be laminated onto the structure.

5 If a support membrane is used in the embodiment on the surface of the conductor foil 12, as depicted in connection with the description of Figure 1, it is most suitable to remove the support membrane after the lamination, i.e. between the intermediate stages shown in Figures 3 and 4.

10 After lamination and the removal of the possible support layer, the adhesive layer, which has been created in the contact openings 8 and between the contact openings 8 and the contact terminals 7, 17, is removed. In the embodiment of the figures, the removal of the adhesive is implemented by the laser-ablation method, using a CO₂ laser. The ability of a CO₂ laser to vaporize organic insulating substances, such as epoxy-base adhesive, is
15 good, but its ability to vaporize copper or other metals is poor, so that the conductor foil 12 can be used as mask for making the contact holes 18. Thus, it is possible to manufacture contact holes 18, the diameter of which is less than the diameter of the beam of the CO₂ laser. This property creates a significant advantage, as the minimum diameter of the beam of a CO₂ laser is typically in the order of 75 µm, which is too large
20 when considering the manufacture of precise electronic module structures. A UV laser, on the other hand, can typically be used to manufacture clearly more precise structures. The minimum diameter of the beam of a UV laser can be, for example 25 µm, but a UV laser is not, on the other hand, suitable for removing adhesive from the contact openings 8 and from between the contact openings 8 and the contact terminals 7, 17.

25 Thus, the use of a conductor mask permits the manufacture of very precisely limited and precisely positioned contact holes 18 in an insulator material, such as the adhesive 5 using in the embodiment. In addition, the use of a CO₂ laser permits the cleaning of the contact surfaces of the contact terminals 7, 17 in the same process stage, without any
30 significant danger of destroying or damaging the contact terminals 7, 17. In the embodiment, the conductor foil 12 is of copper while the contact terminals 7, 17 of the component are also of metal, so that they are not sensitive to the beam of the CO₂ laser,

so that the process can be designed in such a way that the contact surfaces of the contact terminals 7, 17 will be sure to be cleaned sufficiently well. Thus, the advantage of the method described is that contact openings 8 can be made in the conductor foil 12 very precisely with the aid of a UV laser and, after this, the contact openings can be used as a mask for the making of the contact holes 18 by means of a CO₂ laser that is less precise, but safer for the structure.

If the contact holes 8 of the conductor foil 12 were to be manufactured only in this process stage, the method used for machining the metal of the conductor foil 12, for example, a UV laser, would more easily damage also the contact terminals 7, 17, because the energy required to penetrate the conductor foil 12 is significantly greater than the energy required to penetrate the adhesive or other insulation between the contact terminals 7, 17 and the conductor foil 12. In such a manufacturing method, it would be challenging to stop the drilling at precisely the correct depth. In addition, aligning the drilling would be more difficult, due to the deformations arising during lamination and for the reason that the contact terminals 7, 17 of the components cannot be seen through the solid metal film. The use of contact holes 8 pre-manufactured in the conductor foil 12 provides significant advantages, both in the alignment of the components 7, 17 and in the manufacture of the contact holes 18.

In Figure 5, an intermediate layer 2, which is of a suitable conductor material, is made in the contact holes 18. The intermediate layer 2 is manufactured using a suitable chemical conductor-material growing method (electroless plating). The intermediate layer 2 can also consist of a layer of two or more different materials, which are manufactured correspondingly using two or more methods. One purpose of the intermediate layer 2 is to form a conductor membrane for the side walls of the contact holes 18, which connects the contact terminals 7, 17 and the conductor foil 12 to each other. A second purpose of the intermediate layer 2 is to provide a material adapter between the material of the of the contact terminals 7, 17 and the conductor-pattern material to be connected to them. Such a material adapter can be required, for example, in order to ensure the quality of the mechanical or electrical contact and durability, for example, when the material of the conductor-pattern layers of the circuit module is copper and the material of the contact

terminals 7, 17 is something other than copper (Cu), for example aluminium (Al).

When manufacturing the intermediate layer 2, a suitable chemical growing method is used, because by means of such a method the conductor material can also be grown on the vertical surfaces of the contact holes 18, unlike when using sputtering, for example. An electrochemical method (electroplating) cannot be used in this stage, because the side walls of the contact holes 18 are not conducting. Alternatively, V-shaped-opening contact holes can be used and the intermediate layer 2 made by sputtering. Sputterable materials suitable for this purpose are, for example, titanium-wolfram (TiW) and chromium (Cr). A layer of nickel (Ni) and gold (Au) can also be grown on top of the TiW or Cr layer. In the example of Figure 5, nickel grown by a chemical method is used as the intermediate layer 2 in the example of Figure 5, however, so that the intermediate layer 2 will grow at the same time also on the surfaces of the conductor foils 12 and 14. Another example of the intermediate layer 2 is a layer containing zinc, manufactured on the surface of the contact terminals 7, 17, on top of which a layer of nickel (Ni) can further be manufactured. More alternatives that are possible are depicted in connection with the description of Figures 26 - 33.

In this embodiment, after the manufacture of the intermediate layer 2, manufacture is continued by spreading resist layers 3, typically photoresist layers, on both surfaces of the module. The resist layers 3 are patterned with the aid of a conductor-pattern mask by exposure and development, in such a way that the resist 3 is removed from the desired parts of the conductor patterns of the conductor-pattern layers. This intermediate stage is shown in Figure 6. After this, the module is taken to an electrochemical bath and voltage is led to the intermediate layers 2 of the module. The desired conductors of the conductor-pattern layer are then grown in the openings of the resist layers 3. The conductor material also grows in the contact holes 18, forming a conductor core to the contact elements, as can be seen from Figure 7. In the example of Figure 7, the conductors 22, 24 are electrochemically grown copper. Finally, thin etching-mask layers are grown on the surface of the conductors 22, 24. A layer of tin (Sn), for example, can act as the etching mask.

- Next, the resist layers 3 are removed, when, in the embodiment of the figures, the intermediate layer 2 is revealed from under the removed resist. The revealed part of the intermediate layer 2 is removed, for example, by etching, the same procedure being use for the parts of the conductor foils 12 and 14 revealed outer the conductors 22 and 24.
- 5 The etching-mask layer then protects the outermost surfaces of the conductors 22 and 24 from the effects of the etching. An electronic module, which contains two components 6 and 16 connected electrically to conductors 22, comprising two conductor-pattern layers (conductors 22 and 24), and shown in Figure 8, is then obtained.
- 10 In the example of Figures 6 and 7, the conductors 22 and 24 are grown directly into their correct shape in the openings made in the resist layer 3. However, the conductors 22 and 24 can also be manufactured in another way, both in this example and in the examples described hereinafter. One alternative way of manufacture is to grow a unified layer of conductor material over the surfaces of the entire module blank and to pattern the
- 15 conductor layer later by means of a lithography method, in order to form the conductors 22 and 24. Described in greater detail, it is possible to proceed, for example, in such a way that, continuing from the intermediate stage of Figure 5, copper is grown on the surfaces of both intermediate layers 2 by means of an electrochemical method. In that case, the contact holes 18 too are filled with copper. After this, resist layers are spread
- 20 on top of the copper layers, the resists are patterned, and the excess parts of copper, or the intermediate layer 2 and the conductor foils 12 and 14 are etched. After this, the resist mask is removed. Using either manufacturing method, the result is the structure shown in Figure 8.
- 25 Figure 8 can show an already finished simple circuit module, but manufacture is usually continued by manufacturing additional insulator and conductor layers on the surfaces of the circuit module, which are connected electrically with the aid of vias to the structure shown in Figure 8. In addition, it should be noted that vias can be manufactured in the module too of Figure 8, which connect the conductors 22 to the conductors 24. Such vias
- 30 can be manufactured in a corresponding manner to, and in the same process stages as described above in the manufacture of the contact elements.

The module of Figure 8 can be further refined in the manner shown in Figure 9, in such a way that the surfaces of the module are protect by protecting layers 20. In addition, in the example of Figure 9, external contact elements, which comprise bases 21 made on top of the conductor patterns 22, 24 and contact balls 23 made on their surfaces, are
5 manufactured in the module.

Figures 10 - 16 show a manufacturing method according to a second embodiment, up to a stage corresponding to the intermediate stage shown in Figure 5. Manufacture can be continued from the intermediate stage of Figure 16, for example, as shown by Figures
10 6 - 9, or suitably also in an alternative manner, in which the material of the conductors 22 and 24 is first of all grown over the entire surface and after that patterned to form conductors 22 and 24. The technical features and parameters presented in connection with the description of Figures 1 - 5 can also be applied in the process stages shown in Figures 10 - 16, so that there is no need to repeat all the details of the manufacturing
15 process and their advantages in the following embodiment. On the other hand, the essential differences between the embodiments shown by Figures 1 - 9 and Figures 10 - 16 are brought out in the following.

In the embodiment of Figures 10 - 16, manufacture starts, as in Figure 1, from a
20 conductor foil 12, in which contact openings 8 are made. After this, a spacer 15 is attached to the future attachment point of the component 6 on the surface of the conductor foil 12. The spacer 15 is of a suitable insulating material, for example, of pre-hardened adhesive or some other polymer, which has sufficient adhesion with the surface of the conductor foil 12. The spacer 15 can also be of hardened polymer, in
25 which case it can be attached to the surface of the conductor foil 12, for example with the aid of separate adhesive.

A spacer 15 can be used for many different reasons. One use of a spacer is to increase the insulating thickness between the component 6 and the conductor foil 12. The need to
30 increase the insulating thickness can be imposed, for example, by the requirements set by the electrical operation of the circuit module or the component 6. In that case, with the aid of the spacer 15 it is possible to set the properties of the insulation between the

component 6 and the conductor foil 12 as desired. The properties selected can be, for example, a desired specific resistance and spark-over resistance, which can be influenced by the selection of the material of the spacer 15 and the adhesive 5. The spacer can also be used to prevent a short-circuit between the component and the conductor foil 12. Such a use will come into question especially in embodiments in which the surface of the component 6 is pressed very close to the conductor foil, when a risk arises of unintended electrical contacts being formed between the conductor structures on the surface of the component and the conductor foil. A spacer can also be used to weaken the capacitive connection between the internal circuit elements of the component 6 and conductors 22 running next to the location of the component 6.

In addition to, or instead of a spacer 15, it is possible to use for the same purpose an insulator layer 13 entirely covering the surface of the conductor foil 12, as described in connection with Figure 1.

In the examples of Figures 10 - 16, a spacer 15 is used in connection with a bumpless component 6, but the contact terminals of a component 16 with bumps must be made to extend closer to the surface of the conductor foil 12, so that a sufficient insulating gap can be ensured between the opposite surface of the component 16 and the conductor foil 14. In the embodiment, spacers 15 selected component-specifically can be placed in the circuit module, in order to optimize the electrical and/or mechanical properties of the circuit-board module. The same module can thus also contain different kinds of spacers 15 and thus spacers 15 can also be used in series production, in order to make components 6, 16 coming from different sources and with different properties to each other compatible with the circuit-board manufacturing process being used. One example of a mechanical property requiring optimization is the thickness of the insulator layer 1 (and at the same time of the entire module), which can be reduced with the aid of suitable selected spacers 15, which can be seen, for example, in Figure 12.

According to Figure 11, manufacture is continued by spreading adhesive layers 5 on the surfaces of the conductor foil 12 and the spacer 15 in the connection areas of the components. The components 6 and 16 are aligned relative to the contact openings 8 and

glued in place. After that, in the example of Figure 11, insulator sheets 10, 11 and a conductor foil 14 are laminated on top of the conductor foil 12. Next, photo-resist layers 30, which are patterned in such a way that openings larger than the contact openings 8 are created at the positions of the contact openings 8, are spread on the surface of the conductor foils 12 and 14, or a coating is made electrophoretically on top of the entire conductor layer. This photo-resist layer 30 is used to limit the growth of an intermediate-layer material grown using a non-selective method to the contact holes and the immediate surroundings of the contact openings 8. Such a procedure can also be used in connection with the example described above, nor, on the other hand, is it essential in the examples of Figures 10 - 16. Figure 12 shows the module after these stages. The contact terminals 7 of the component 6 are covered by both a spacer 15 and adhesive 5. There is adhesive on the surface of the contact bumps 17 of the component 16 and in the corresponding contact openings 8.

In the stage shown in Figure 13, contact holes 18 are made at the positions of the contact openings 8 of the component 6. The contact holes are opened through the spacer 15 and the adhesive layer 5, as far as the contact surfaces of the contact terminals 7. In the embodiment of the figure, the opening of the contact holes 8 is implemented by the laser-ablation method, using a CO₂ laser, as described in connection with Figure 4. In the embodiment of Figures 10 - 16, the important fact is that contact holes are not opened at this stage of the position of the contact terminals 17 of the second component 16.

In the stage shown in Figure 14, an intermediate layer 2, which is of a suitable material, is made in the contact holes 18 of the component 6. The conductor material of the intermediate layer 2 is selected on the basis of the material of the contact terminals 7 of the component 6 and manufactured using a suitable chemical conductor-material growing method. In the example of the figure, the material of the contact terminals 7 of the component is aluminium and the material of the intermediate layer 2 is mainly a metal alloy containing zinc. The principles described in connection with Figure 5 above are applied to the growing of the intermediate layer. Unlike the example of Figure 5, in the case of Figure 14, it is, however, also possible to proceed in such a way that in this

stage the intermediate layer 2 is grown with the aid of a selective method only on the surface of the contact terminals 7, i.e. on the bottom of the contact holes 18 and not on the edges of the contact holes 18. In this embodiment, the intermediate layer 2 coming on the edges of the contact holes 18 is grown later in connection with the growing of the intermediate layer relating to the contact bumps 17 of the component 16. The embodiment using a selective growing method has the advantage that the intermediate layer 2 does not grow on top of the adhesive layer covering the contact bumps 17 of the component 16.

10 Manufacture is continued in the stage shown in Figure 15 by manufacturing contact holes 28 at the positions of the contact openings 8 of the second component 16. After this, the module according to Figure 16 is subjected to a suitable chemical conductor-material growing method. In the example of Figure 15, the growing method is non-selective and the conductor material grows on all the free surfaces of the module and thus also in the contact holes 18 of component 6 and in the contact holes 28 of component 16. However, the photo-resist layer 30 protects the surfaces of the module, so that the intermediate layer 2 grows only in the contact holes 18 and 28 and in their surroundings. After this, the photo-resist and the conductor material that may have grown on its surface is removed. Such an embodiment using a photo-resist layer 30 can be useful, for example, when nickel or some other metal differing from copper is grown in the openings of the photo-resist layer, for example, using a non-selective method. The conductors 22 and 24 can then be manufactured to consist of solely a copper layer.

In other embodiments, suitably selected selective growing methods can also be used and the conductor material grown only on the surfaces of the contact bumps 17 of the component 16, correspondingly as described above in connection with Figure 14. In any case, at this stage the intermediate layer 2 is grown at least on the surfaces of the contact bumps 17 of the component 16 and on the surfaces of the side walls of the contact holes 28 and, in addition, if desired also on the surface of the intermediate layer 2 connected to the contact terminals 17 of the component 6 and/or on the surfaces of the side walls of the contact holes 18 of the component 6.

If the example of Figures 10 - 16 were to be implemented without the use of a photo-resist 30, in the example of Figure 16 the material of the surface of the contact bumps 17 of the component 16 could suitably also be copper and the material of intermediate layer 2 to be grown of the surface of the contact bumps 17 would then be copper
5 manufactured suitably using a chemical growing method.

After the manufacture of the intermediate layer 2, in this embodiment manufacture can be continued, for example, in the manner stated in connection with the description of Figures 6 - 9, by manufacturing conductor patterns on the surface of the module and
10 conductor cores for the contact elements located in the contact holes 18 and 28.

Another alternative is to coat copper on both conducting surfaces of the module, after the removal of the photo-resist layer 30. After this, the copper layers can be patterned to form conductors 22 and 24, when the structure shown in Figure 17 will be obtained, in
15 which the conductors 22 and 24 are formed of the first and second copper layers in the surroundings of the contact elements, as well as of an intermediate layer 2, which is of nickel for example, between them. Elsewhere, the conductors 22 and 24 are formed of a first and second copper layer, between which is the interface to be analysed. Once the structure of Figure 17 has been manufactured, it is possible, if desired, to continue in
20 some manner described in connection with any of the previous examples.

Figure 18 - 23 show a manufacturing method according to a third embodiment, which is a variation of the embodiment shown in Figures 10 - 16. From the intermediate stage of Figure 23, manufacture can be continued, for example, in the manner shown in Figures
25 6 - 9. The technical features and parameters presented in connection with the description of Figures 1 - 5 and 10 - 16 can thus also be applied in the process stages shown in Figures 18 - 23, to that all the details and their advantages of the manufacturing process need not be unnecessarily repeated in the following embodiment. However, in the following the essential difference between the embodiments shown in Figures 10 - 16 and Figures 18 - 23 is presented.
30

In the embodiment of Figures 18 - 23, manufacture is commenced, as in the case of

Figure 10, from a conductor foil 12, in which contact openings 8 are made. After this, spacers 15 are attached to the surface of the conductor foil 12, to the future attachment points of the components 6 and 26. The spacers 15 of the components 6 and 26 can be mutually identical or selected component specifically, for example, in such a way that the spacer 15 of the component 6 is of a different material and/or thickness to the spacer 15 of the component 26.

According to Figure 18, manufacture is continued by spreading adhesive layers 5 on the connection areas of the components and by laminating insulator sheets 10, 11 and a conductor foil 14 to the blank, exactly as described in connection with Figure 11. Figure 19 show the module after these stages.

In the stage shown in Figure 19, contact holes 18 are made at the positions of the contact openings 8 of the component 6, as described in connection with Figure 13. At this stage, contact holes are not yet opened at the positions of the contact terminals 27 of the component 26.

The stage shown in Figure 21 corresponds completely to the method stage described in connection with Figure 14. In this embodiment, an intermediate layer 2, which is of two layers, is manufactured in the contact holes 18 of the component 6. In the example of the figure, the material of the contact terminals 7 of the component is aluminium. The two-layer intermediate layer 2 of the example comprises first a grown layer containing zinc and after this a grown nickel-aluminium layer. The nickel-aluminium layer is grown by means of a chemical method and is used to seal the layer containing zinc.

Manufacture is continued in the stage shown in Figure 22, by making contact holes 28 at the positions of the contact openings 8 of the second component 26. After this, according to Figure 23 the module is subjected to a suitable chemical conductor-material growing method. This stage corresponds to the method stage described in connection with Figure 16. In the example of Figure 23, the material of the surface of the contact terminals 27 of the component 26 is copper and the material of the intermediate layer 2 grown of the surface of the contact terminals is also copper.

Figure 24, for its part, shows a modification of the embodiment of Figures 18 - 23, in which, after the stage shown by Figure 22, a first intermediate layer is grown on top of the contact terminals 27 of the component 26, by means of a selective growing method and, after this, the growing of the intermediate layer 2 is continued using a non-selective method. In the example of Figure 24, the material on the surface of the contact terminals 27 of the component 26 is gold and the material of the intermediate layer 2 grown on the surface of the contact terminals 27 is nickel.

In the embodiments of these Figures 18 - 24, after the manufacture of the intermediate layers 2 it is possible to continue, for example, by making conductor patterns on the surface of the module and conductor cores for the contact elements located in the contact holes 18 and 28, for example, by means of the manner stated in connection with the description of Figures 6 - 9.

Figure 25 shows in greater detail the shape of the contact hole and correspondingly also the shape of the contact element to be manufactured in this opening. The example of Figure 25 shows one possible shape, which can be achieved when using the embodiments described above. The shape can be affected with the aid of the shape of the contact openings 8 to be made in the conductor foil 12, the properties of the insulation between the conductor foil 12 and the component, and the operating parameters of the CO₂ laser. The contact hole of Figure 25 is rotationally symmetrical and the cross-section shown in the figure is taken through the central axis of the contact hole, i.e. it shows the widest possible cross-section. In Figure 25, the size and shape of the contact hole are determined with the aid of the following parameters:

- greatest width W_{MAX} , from which the greatest cross-sectional area A_{MAX} can be calculated,
- the width W_{CONT} of the contact between the contact element and the contact surface 7 of the component 6, from which the contact surface-area A_{CONT} between the contact element and the contact surface of the component can be calculated, and

- the width W_{HOLE} of the contact opening, from which the contact surface-area $A_{CONT\ 2}$ between the contact element and the conductor of the conductor-pattern layer can be calculated.

5

The figure also shows the width W_{PAD} of the contact surface of the component, from which the surface area A_{PAD} of the contact surface can be calculated, if the shape of the contact surface is known. The contact surface 7 can be, for example, square in shape and, when W_{PAD} represents the width of a side, the surface area of the contact surface is obtained as: $A_{PAD} = W_{PAD} \times W_{PAD}$. Of course, the surface areas can also be determined with the aid of surface-area measurement, which can be more practical if the surface area to be determined is of an irregular shape.

In the figure, the contact surface 7 is surrounded by a passivation layer 9 made on the surface of the component 6. In that case, the surface area A_{PAD} refers precisely to the surface area free to form a contact, i.e. the surface area of the surface that is revealed in the opening made in the passivation layer 9. In addition, the figure shows the distance H of the distance between the conductor foil 12 and the contact surface 7, which corresponds to the depth of the contact hole and is thus the height of the contact element to be made in the contact hole. Because the contact hole is filled entirely with conductor material, the other dimensions too of the contact hole correspond to the dimensions of the contact element and the parameters W_{MAX} and W_{HOLE} can also be used to refer to the corresponding dimensions of the contact element.

The following presents some typical parameters in connection with the embodiments described above:

$H = 1 - 50\ \mu\text{m}$, usually $5 - 30\ \mu\text{m}$;

$W_{PAD} = 20 - 1000\ \mu\text{m}$, usually $50 - 200\ \mu\text{m}$, and most usually about $100\ \mu\text{m}$; and

$W_{HOLE} = 5 - 500\ \mu\text{m}$, usually $20 - 75\ \mu\text{m}$, and most usually about $30 - 50\ \mu\text{m}$.

In addition, generally $W_{HOLE} \geq H$, which represents the reliable filling of the contact hole. The contact hole 18 is intended to be manufactured in such a way that the side walls of the hole would be vertical. In other words, the goal is a contact hole, the width and shape of which remains constant over the whole distance H between the conductor foil 12 and the contact surface 7, i.e. the contact hole would have the shape of the contact opening 8 over all of this distance. A shape that narrows towards the contact surface 7 is also good. In practice, when using the laser process described above the contact hole can, however, become widening towards the contact surface 7, or first widening and then narrowing, so that the contact hole is widest somewhere between the conductor foil 12 and the contact surface 7. Figure 25 shows a contact hole of this kind. Such a non-optimal shape is not problematic, provided the widening is not too great and the filling of the hole succeeds well.

Of the dimension values of the widths referred to above, the width W_{PAD} of the contact surface 7 of the component is determined through the selection of the component. If necessary, W_{PAD} can be measured separately from each straight line that runs through the centre point of the contact surface 7. This definition may be required when examining the dimension values referred to above and their ratios, if the shape of the contact surface 7 or of the contact opening 8 is irregular. In the most usual cases, the contact surface is, however, square, in which case the width of the side of the square can generally be used as the width W_{PAD} of the contact surface 7.

The width W_{HOLE} of the contact opening 8 is a parameter, which is selected when planning the manufacturing process. One parameter to be taken into account when selecting the width of the contact opening 8 is the width of the contact surface 7 of the component being used. The width of the contact opening 8 is selected in such a way that the contact hole to be made through the contact opening will meet the contact area 7 of the component over its entire cross-sectional area at the component end, and will not miss the contact area, for example, on the surface of the passivation layer. If the contact opening is circular in shape, with width W_{HOLE} of the contact opening is the diameter measured through the centre point of the circle. If, on the other hand, the contact opening

is irregular I shape, W_{HOLE} can, if necessary, be measured separately along each straight line that runs through the centre point of the contact opening 8. In the case of an irregular shape, when comparing the width W_{HOLE} of the contact opening with the width W_{PAD} of the contact surface, the comparison can always be made separately for each pair
 5 of widths measured through parallel straight lines. If necessary, the widths W_{HOLE} and W_{PAD} can also be compared in a corresponding manner to the other parameters described.

The ratios of the parameters described above can also be applied in connection with the
 10 contact bumps 17, in which case the surface area and width of the contact area will be replaced by the surface area and width of the contact bump and the distance H will be measured to the surface of the contact bump.

The shape of the contact hole can be influenced with the air of the laser parameters,
 15 which are selected according to the hole parameters and the properties of the insulation to be removed. The manufacturing result is, of course, also affected by the laser device being used. The suitability of the selected parameters for the process is indeed examined with the aid of a pilot manufacturing batch and, if necessary, the parameters are altered so that the desired result will be achieved.

20

In general, it is sensible in the manufacturing method to try to achieve a contact-hole shape, in which

$W_{CONT} = 0.5 - 1.5$ times W_{HOLE} , preferably $0.7 - 1.2$ times W_{HOLE} , and most preferably 0.8
 25 $- 1.0$ times W_{HOLE} , however, in such a way that $W_{CONT} < W_{PAD}$; and

$W_{MAX} =$ at most $100\ \mu\text{m}$, preferably at most $30\ \mu$, and most preferably at most $10\ \mu\text{m}$ larger than whichever of the parameters W_{HOLE} and W_{CONT} is greater. Presented relatively, the objective would be for $W_{MAX} =$ at most $40\ \%$, preferably at most $20\ \%$, and
 30 most preferably at most $10\ \%$ greater than whichever of the parameters W_{HOLE} and W_{CONT} is greater.

In the most optimal shape of a contact element, W_{MAX} is essentially as large as W_{HOLE} and, in addition, W_{CONT} is 0 - 20 % smaller than W_{MAX} .

5 In the most typical embodiments, the contact surface 7 has a square shape and the contact opening 8 is circular in shape. In that case, A_{CONT1} is typically 10 - 75 % of the surface area A_{PAD} . A_{CONT1} and A_{CONT2} are typically mutually approximately of equal size, for example, with an accuracy of ± 20 %.

10 Figure 26 shows examples of other possible shapes of the contact holes 18. Figure 27, for its part, shows examples of intermediate layers 2 manufactured in such contact holes. In the examples of Figures 26 and 27, the component to be attached is bumpless. As can be seen from Figure 27, the intermediate layers 2 do not extend at all on top of the passivation layer 9 of the component, but instead are in contact only with the contact surface 7 of the component. With the aid of this feature, it is possible to see even from
15 the finished electronic module whether the component embedded in the electronic module has bumps or is bumpless. The bumps grown on the contact surface 7 of the component in the bump-creation processes always fill the entire contact surface 7 and always also spread slightly on top of the passivation layer 9. If, on the other hand, bumpless components are used in the embodiments described above, the intermediate
20 layer 2 and the contact element grow only into the contact hole 18, when in the finished electronic module the intermediate layer 2 will not extend on top of the component's passivation layer 9 and part of the contact surface 7 of the component will always remain free of the intermediate layer 2 (the edges of the contact surface 7) when the alignment and manufacture of the contact hole 8 have succeeded. Also in a possible
25 contact-hole 18 alignment-error situation, in which the contact opening 8 is not completely aligned with the contact surface 7, at least part of the edge areas of the contact surface 7 and of the passivation layer surrounding the edge area will be free of the intermediate layer 2.

30 If a bumpless component is manufactured by a semiconductor process using copper conductors, the contact area 7 is copper. In that case, the intermediate layer can be manufactured directly from chemically grown copper, which forms a conductor

surfacing also on the side walls of the contact hole 18. After this, the contact holes 18 can be filled and the thickness of the conductor layer increased using an electrochemical copper-growing method.

5 At the moment of writing of the present application, the most commonly used conductor material in semiconductor processes is, however, aluminium. Thus, the most common material of the contact area 7 of bumpless components too is aluminium and it is preferable to use an intermediate layer, with one or more layers manufactured from different materials, between the aluminium contact area and the copper conductors of the
10 electronics module. In the following, reference is made to a few possible intermediate-layer constructions:

Intermediate-layer construction 1

15 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the side walls of the contact hole 18. A layer of nickel, which does not grow at all or only poorly on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical
20 method on the surface of the nickel. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 2

25 First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of copper is grown by a chemical method on the surface of the layer containing zinc. The copper grown by a chemical
30 growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 3

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. The layer containing zinc manufactured by a zincate process does not grow on the polymer surfaces of the contact hole 18. A layer of nickel-aluminium, which does not grow on a polymer surface, is grown by a chemical method on the surface of the layer containing zinc. A layer of copper is grown by a chemical method on the surface of the nickel-aluminium. The copper grown by a chemical growing method can be made to grow reliably also on top of polymer, thus making the side walls of the contact holes 18 conductive for later electrochemical growing.

Intermediate-layer construction 4

First of all, a layer containing zinc is grown on the surface of the aluminium contact area 7. A layer of nickel-aluminium is grown by a chemical method on the surface of the layer containing zinc. A layer of nickel is grown by a chemical method on the surface of the nickel-aluminium and a layer of copper is grown by a chemical method on the surface of the nickel.

Intermediate-layer construction 5

First of all, a layer containing zinc is grown on the surface of the aluminium contact layer 7. A layer of nickel is grown by a chemical method on the surface of the layer containing zinc.

Intermediate-layer construction 6

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, which grown nickel layer alone forms the intermediate layer 2.

Intermediate-layer construction 7

A layer of nickel is grown by a chemical method on the surface of the aluminium contact area 7, and a layer of copper is grown by a chemical method on the surface of the nickel.

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In the above examples of intermediate-layer constructions, the layer containing zinc contains, for example, about 80 % zinc, about 16 % copper, about 2 - 3 % nickel, and about 2 - 3 % iron. This is only one possible example of alloy ratios suitable for the application, so that the alloy ratios can, of course, vary according to the applications. In the above examples of intermediate constructions, the thickness of the layer containing zinc is less than 1 μm , usually as a single layer about 0.1 μm and as several layers, for example 0.3 - 0.4 μm . At its thinnest, the layer containing zinc can be about 5 - 10 nm after manufacture. When growing a layer containing nickel or nickel-aluminium on top of the layer containing zinc, at least some of the zinc atoms dissolve and are replaced with nickel atoms. In the finished circuit module, it can be possible for the layer containing zinc to be observable as mainly a concentration profile of zinc in the interface between the aluminium and the material of the next layer. The layer containing zinc need not necessarily be precisely limited in the final product, because the zinc can diffuse to the adjacent material layers, particularly in stages of the manufacturing process using higher temperatures.

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In one preferred embodiment, the layer containing zinc is grown by a double zincate process. With a single zincate process, the zinc forms a non-uniform and uneven surface on top of the aluminium. The adhesion of a nickel layer grown on top of such a surface is weaker and is less suitable for use with small micro-via openings. The quality of the grown zinc surface can be significantly improved by using a double zincate process. Typically, in such a process, after the first zincate treatment, the layer containing zinc is stripped using nitric acid (HNO_3), after which a second layer containing zinc is coated. By means of the double zincate process, a tight and uniform layer containing zinc is obtained on the surface of the component's aluminium junction interface.

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The thickness of the nickel-aluminium layer, for its part, can be, for example, 0.2 - 2

μm. The thickness of the nickel layer, on the other hand, can be, for example 0.5 - 20 μm, typically 2 - 10 μm. The layer thicknesses too are only examples of the possible layer thicknesses and other layer thicknesses can also be used.

- 5 In the embodiments, the electrochemically grown copper layer can have a thickness of, for example, 5 - 30 μm, typically 10 - 20 μm. The copper layer grown by a chemical growing method, for its part, is generally manufactured to be clearly thinner, and its thickness in the embodiments is, for example, 0.1 - 2 μm, typically 200 - 800 nm.
- 10 In the manufacturing methods described above, it is, of course, also possible to use intermediate-layer constructions and materials, for example tin, other than those referred to above. It is also possible to grown a nickel layer directly on the surface of the aluminium, for example, by alkali etching and flushing the surface after this with propan-2-ol and immediately after this coating with propan-2-ol at boiling point in a
- 15 warm chemical nickel bath. In addition, the surface of the layer containing zinc could also be coated with chromium and gold on the surface of the nickel.

Figure 28 shows yet another possible contact structure, in which it is possible to use components, the contact area of which is pre-equipped with base-metallurgical layers, though bumps as such are not made. Figure 29 shows one possible corresponding contact structure, implemented with a bumpless component.

Figure 28 shows a passivation layer 9 on the surface of the component, in which there is an opening at the position of the contact area 7 of the component. There is a polymer layer 25 of the surface of the passivation layer 9. The polymer layer 25 can consist of one or more polymer layers. The material of the polymer layer 25 can contain, for example, an insulator layer 13 depicted in connection with Figure 1, adhesive 5 depicted in connection with Figure 2, and/or a spacer depicted in connection with Figure 11. The base metallurgy, which in this case comprises two layers, is made on the surface of the contact area 7 of the component. The first base-metallurgy layer 26 is a layer of, for example, chromium (Cr) or titanium-wolfram (TiW) manufactured by sputtering. The second base-metallurgy layer 27 is a layer of, for example, nickel (Ni), copper (Cu), or

gold (Au), manufactured by sputtering. The actual bump comprises further a gold or copper layer, for example, grown chemically or electrochemically, on the surface of the second base-metallurgy layer 27.

5 In the example of Figure 28, the component is attached by a polymer layer 25 to a conductor foil 12, in which contact openings 8 have been made as depicted in the methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the second base-metallurgy layer 27, are made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is
10 made using one or more chemical growing methods, in a corresponding manner to that depicted in the methods described above. In the example of Figure 28, the intermediate layer 2 is of copper grown using a chemical growing method. On top of this intermediate layer a layer 32 of copper is grown using an electrochemical growing method. The electrochemically grown copper also forms the conductor core 29 of the contact element.
15 It can be seen from Figure 28 that the conductor foil 12, the intermediate layer 2, and the copper layer 32 together form the material of the conductor 22. In the example, the conductor foil 12, the intermediate layer 2, and the copper layer 32 are all of copper, but the layers and the interfaces between them, can, however, also be detected by analysing the finished structure.

20 Like Figure 28, Figure 29 shows a passivation layer 9, in which there is an openings at the position of the contact area 7 of the component, on the surface of the component. On the surface of the passivation layer 9 is a polymer layer 25, which corresponds to that shown in connection with Figure 28. In the example of Figure 29, the surface of the
25 contact area 7 of the component has been a uncoated component when it was brought to the circuit-module manufacturing process. In such a component, the outer surface of the contact area 7, i.e. the contact surface, is thus typically formed already at the semiconductor factory. In the example of Figure 29, the material of the contact area 7 is aluminium.

30 In the example of Figure 29, the component is attached by a polymer layer 25 to the conductor foil 12, in which contact openings 8 are made in the manner depicted in the

methods described above. Contact holes 18 or 28, in which a contact element is made in contact with the contact area 7, have been made through the contact openings 8. The contact element is made in such a way that first of all an intermediate layer 2 is made using one or more chemical growing methods, in a corresponding manner to that described above. In the example of Figure 29, the intermediate layer 2 is made in several parts and comprises several layers. In Figure 28, the intermediate layer is, in addition, to facilitate the description, divided into three parts, a base part 36, a wall part 37, and a conductor part 38. The base part 36 is the part that grows on the surface of the contact terminal 7, 17 to the bottom of the contact hole 18, 28, the wall part 37 is the part that grows on the surfaces of the side walls of the contact hole 18, 28, and the conductor part 38 is the part that grows to form part of the conductor 22 being manufactured.

The intermediate layer 2 of Figure 29 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. In the example of Figure 29, the conductor foil 12 is of copper, so that when using a zincate process the first intermediate layer 33 grows only on the base part 36 of the intermediate layer 2. From this, manufacture can be continued, for example, by using a chemical nickel-growing method to make the second intermediate layer 34. The nickel grows on both the base part 36 and the conductor part 38 of the intermediate layer and, when using some growing methods, on the wall part 37 too on the surface of the polymer 25. The third intermediate layer 35 is made from copper on top of the second intermediate layer 34 using a chemical growing method, so that the copper grows on the base part 36, the wall part 37, and the conductor part 38. A layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element.

In the case of Figure 29, it should be noted that, in the finished circuit module, the layers 33 and 34 do not have precise boundaries as shown in the figure, but instead the layers can appear as overlapping or mixed, for example, from the effect of diffusion. For example, in the case of the first intermediate layer 33 containing zinc, the zinc can be located as a concentration profile in the interface between the aluminium and nickel 34

and partly inside the aluminium 7 and the nickel layer 34.

In the contact structure of Figure 29, other material combinations can also be used. For example, suitably selected intermediate-layer structures from the intermediate-layer constructions 1 - 7 described above can be used to form the contact structure depicted by Figure 29 and also the contact structures depicted by Figures 30 - 33. In addition, the contact structure of Figure 29 can also be manufactured with the aid of the materials shown by Figure 28, in such a way that the first intermediate layer 33 and the second intermediate layer 34 are made by sputtering. In that case, the sputtered intermediate layers 33 and 34 will grow to the base part 36 and the conductor part 38, but not to any substantial extent to the wall part 37, provided the contact hole 18, 28 does not widen towards the contact opening 8. One possibility is to use a first intermediate layer 33 containing zinc and on the surface of this either directly a third intermediate layer 35 made from nickel by a chemical growing method, or a construction, in which a second intermediate layer 34 made from nickel-aluminium is used between the layers 33 and 35. In such an embodiment, there is no need at all of chemical copper growing, as the nickel forms a vertical contact along the side wall of the contact hole.

Figure 30 shows yet another contact-element structure. In the structure of Figure 30, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel-aluminium and the third intermediate layer 35 is of nickel grown by a chemical growing method. This, in the structure of Figure 30, the contact hole is filled with nickel, i.e. the conductor core 29 of the contact element is nickel. Otherwise, the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 30.

Figure 31 shows yet another contact-element structure. In the structure of Figure 31, the intermediate layer 2 comprises a first intermediate layer 33 and a second intermediate layer 34. The first intermediate layer 33 can be manufactured, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate

layer 34 is of copper grown by a chemical growing method, or alternatively of nickel grown by a selective chemical growing method. Alternatively, the structure of Figure 31 can also be made in such a way that the first and second intermediate layers 33 and 34 are replaced with a single layer of chemically grown nickel. The conductor core 29 is typically copper and the conductor 22 comprises a first and second copper layer 12 and 32. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 31.

Figure 32 shows yet another contact-element structure. In the structure of Figure 32, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method, the growing method is selective, in such a way that the nickel grows on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 32 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with Figures 28 and 29 apply in the case of the structure of Figure 32.

Figure 33 shows yet another contact-element structure. The method described in connection with Figures 10 - 17, for example, in which a photo-resist layer 30 is used, can be used for making the structure of Figure 32. In the structure of Figure 33, the intermediate layer 2 comprises a first intermediate layer 33, a second intermediate layer 34, and a third intermediate layer 35. The first intermediate layer 33 can be made, for example, by using a chemical growing method to grow a layer containing zinc. The second intermediate layer 34 is of nickel grown by a chemical growing method. In the method of the example, the growing method is selective, in such a way that the nickel grows only on top of conductive material. The third intermediate layer 35 is of copper grown by a chemical growing method. Alternatively, the structure of Figure 33 can also be made in such a way that the first intermediate layer 33 is omitted. The conductor core 29 is typically of copper. Otherwise the technical features described in connection with

Figures 28 and 29 apply in the case of the structure of Figure 33.

Thus, in the embodiments a method is presented for the manufacture of a circuit module, in which method

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- a conductor foil 12 is taken,

- a component 6, which comprises contact areas 7, the material of which contains a first metal, is taken,

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- the component 6 is attached to a conductor foil 12 by means of a polymer layer 25,

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- an insulator layer 1 is manufactured around the component 6 attached to the conductor foil 12,

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- contact holes 18, 28 are made in the polymer layer 25 at the positions of the contact areas 7, in such a way that the contact surface area A_{CONY1} between each contact hole 18, 28 and the corresponding contact area 7 is less than the surface area A_{PAD} of the contact area 7, and

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- an intermediate layer 2, which contains at least a third metal, is grown at least on the surface of the contact areas 7 in the contact holes 18, 28, and

- a layer 32 of a second metal is grown, which layer 32 is in contact with the surface of the intermediate layer 2 and extends along the conductors 22 being made, and

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- conductors 22 are formed by patterning the conductor foil 12, and, if necessary, also the intermediate layer 2 on the surface of the conductor foil 12 and/or the layer 32 of a second metal.

In a typical embodiment, the contact holes 8 are made in the conductor foil 12 before

attaching the component, so that the component is thus attached to a conductor foil 12 equipped with contact openings. In the commonest form of this type of embodiment, the contact openings do not extend to the surfaces of the contact areas 7, so that after the attaching of the component 6 contact holes 18, 28 are further opened through the contact
5 openings 8.

In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

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In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.

15 In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.

20 In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.

When making the intermediate-layer construction, at least one chemical growing method is typically used.

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The embodiments depict a circuit module, which comprises

- an insulator layer 1,
- 30 - inside the insulator layer 1, at least one component 6, which comprises contact areas 7, the material of which contains a first metal,

- on the surface of the insulator layer 1, conductors 22, which comprise at least a first layer 12 and a second layer 32, in such a way that at least the second layer 32 contains a second metal, and
 - 5 - contact elements for forming electrical contacts between the contact areas 7 and the conductors 22, which contact elements comprise an intermediate layer 2, which contains a third metal, on the surface of the material of the contact area 7,
 - in which the first, second, and third metals are different metals, and
 - 10 - the contact surface area A_{COT1} between the intermediate layer 2 and the contact area 7 is less than the surface area A_{PAD} of the contact area.
- In one embodiment, the first metal is aluminium, the second metal is copper, and the third metal is zinc. In such an embodiment, the intermediate layer 2 can, of course, in addition to zinc, also contain other metals or metal alloys, as stated above.
- In a second embodiment, the first metal is aluminium, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.
- 20 In a third embodiment, the first metal is gold, the second metal is copper, and the third metal is nickel. In such an embodiment, the intermediate layer 2 can, of course, in addition to nickel, also contain other metals or metal alloys, as stated above.
- 25 In the commonest embodiment, the material of the contact areas 7 is mainly aluminium and the material of the conductors is copper and between them is one of the intermediate-layer constructions 1 - 7 described above.
- 30 In a typical embodiment, the contact elements comprise a copper core 29 made using an electrochemical growing method, which, in the direction of the side walls and the component 6 is bounded by the intermediate layer 2 and in the direction of the conductor

22 connects continuously, i.e. without an interface to the material of the second layer 32 of the conductor 22. In other words, the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is manufactured in the same process, so that the parts are attached permanently to each other and there is no interface
5 between them. Between the first layer 12 and second layer 22 of the conductor, on the other hand, there is typically an interface, or a corresponding transition zone, which can be detected, for example, by analysing the crystalline structure or impurity concentration of the metal.

10 In one embodiment, the width W_{CONT} of the contact surface between the contact element and the contact area 7 of the component is 0 - 20 % less than the greatest width W_{MAX} of the contact element in the same direction.

The contact elements usually fill entirely the contact holes 18, 28, i.e. the contact
15 elements are not hollow, but are solidly of conductor material.

Usually, the aim in the embodiments is for the height H of the contact element to be less than, or equal to the greatest width W_{MAX} of the contact element.

20 There are also embodiments of the circuit module, in which the insulator layer 1 includes at least one layer of fibre material 19, in which there is an opening in the fibre material 19 for the component 6, as well as a uniform polymer layer, which is attached to the fibre material 19 and to the components 6, 16.

25 The manufacturing processes described above and their sub-processes can be modified in many ways. For example, the use of an actual adhesive depicted above in attaching the component to the conductor foil 12 can be replaced with some other adhesion mechanism. On example that can be given is the use of an insulator layer 13 possessing an adhesion property on the surface of the conductor foil 12 (see Figure 1 and the
30 corresponding description). The components 6 are then pressed directly against the insulator layer 13, so that the components attach sufficiently in place in a manner correspondingly to that described in connection with the embodiment using adhesive.

Such an insulator layer 13 can contain, for example, a tape-like surfacing, or consist of a polymer or similar material that is shapable at least in its surface part.

5 The method can also be implemented without the use of an adhesive 5 or an adhesion property. In that case, the components 6 can be attached in place, for example, mechanically or with the aid of a vacuum. The vacuum or similar temporary attachment can then be maintained until the component 6 is sufficiently secured in place with the aid of the insulator material 1.

10 The component 6 to be attached can be, for example, an integrated circuit, such as a memory chip, processor, or ASIC. The component to be attached can also be, for example, a MEMS, LED, or passive component. The component to be attached can be cased or uncased and its contact terminals can consists of contact areas 7, contact bumps 17, or similar. There can also be a conductor coating thinner than an actual contact bump
15 on the surface of the contact areas of the component.

A different material of the insulator layer 1 from those in the examples described above can also be selected. The insulator layer 1 can be manufactured from a suitable polymer or from a material containing polymer. The material of manufacture of the insulator
20 layer 1 can be, for example, in a liquid or pre-hardened form (such as prepreg). In the manufacture of the insulator layer 1 it is possible to use, for example, glass-fibre reinforced sheet, such as an FR4 or FR5-type sheet. Other examples of materials, which can be used in the manufacture of the insulator layer 1 are PI (polyimide), aramide, polytetrafluoroethylene, and Teflon®. Instead of, or as well as thermosetting plastics,
25 thermoplastics too, for example some suitable LCP (liquid crystal polymer) material can be used in the manufacture of the insulator layer 1.

In addition, it is obvious to one skilled in the art that the features described above of the
30 invention can be used as part of some larger totality, for example, in such a way that the electronics module is manufactured partly using some method according to the prior art and partly using the embodiments depicted here. It is also possible to manufacture additional circuit-board layers on the surface or surfaces of the electronic-module

structures described above, or also to attach components, for example, by means of the surface-mounting technique.

5 One skilled in the art will also understand that, when reference is made in the present document to a specific material, for example, aluminium, nickel, or copper, the reference is to a material, which in terms of the application is substantially of the said material. The material referred to can thus, in addition to the said principal element contain, from the point of view of the application, insubstantial amounts of impurities and other elements. For example, an aluminium contact area is usually of a material that typically
10 contains a minimum of 95 % aluminium.

When, on the other hand, reference is made to a material containing some specific element, this means that the material contains an essentially large content of the said element. In addition, the material can contain substantial or insubstantial amounts of
15 other elements. For example, the layer containing zinc will thus contain an amount of zinc that is of significance in terms of the contact properties between the aluminium and the next metal.

The examples given above depict some possible methods and structures, which the aid
20 of which our invention can be exploited. However, our invention is not restricted to only the examples and embodiments described above, but instead the invention covers numerous other methods and structures, taking into account the full scope of the Claims and the equivalence interpretation.

Claims:

1. Method for manufacturing a circuit module, the method comprising

5 taking a conductor foil (12),

making contact openings (8) in the conductor foil (12) for the manufacture of contact elements,

10 taking a component (6), which comprises contact areas (7), the material of which contains a first metal,

attaching the component (6) to the conductor foil (12) by means of a polymer layer (25),

15 manufacturing an insulator layer (1) around the component (6) attached to the conductor foil (12),

20 making contact holes (18, 28) in the polymer layer (25) at the positions of the contact areas (7), in such a way that the contact surface area (A_{CONT1}), between each contact hole (18, 28) and the corresponding contact area (7) is less than the surface area (A_{PAD}) of the contact area (7), and

25 growing an intermediate layer (2) at least on the surface of the contact areas (7) in the contact holes (18, 28), the intermediate layer (2) containing at least a third metal, and

30 growing a layer (32) of a second metal, which layer (32) is in contact with the surface of the intermediate layer (2) and extends along the conductors (22) being made, and

forming conductors (22) by patterning the conductor foil (12), and, if necessary,

also the intermediate layer (2) on the surface of the conductor foil (12) and/or the layer (32) of a second metal.

2. Method according to Claim 1, in which

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the contact openings (8) are manufactured before the attachment of the component (6),

the component (6) is attached to a conductor foil (12) equipped with contact
10 openings, and

after the attachment of the component (6), contact holes (18, 28) are opened through the contact openings (8).

15 3. Method according to Claim 2, in which the contact holes (18, 28) are opened through the contact openings (8) using a CO₂ laser, in which case the conductor foil (12) is used as a mask.

20 4. Method according to any of Claims 1 - 3, in which the first metal is aluminium, the second metal is copper, and the third metal contains at least one of the metals zinc and nickel.

5. Method according to any of Claims 1 - 3, in which the first metal is gold, the second metal is copper, and the third metal is nickel.

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6. Method according to any of Claims 1 - 4, in which the intermediate layer (2) comprises a layer (33) containing zinc, which is manufactured using a double zincate process.

30 7. Method according to any of Claims 1 - 6, in which the intermediate layer (2) comprises a layer (34) containing nickel, which is manufactured using a chemical nickel-growing method.

8. Method according to any of Claims 1 - 7, in which the intermediate layer (2) comprises a layer (35) containing copper, which is manufactured using a chemical copper-growing method.
- 5
9. Method according to any of Claims 1 - 8, in which the insulator layer (11) is manufactured in such a way that
- at least one insulator sheet (11) containing a fibre material (19) and a pre-
- 10 hardened polymer is taken,
- a hole for the component (6) is made in the insulator sheet (11) containing a fibre material (19), and
- 15 the insulator sheet (11) or insulator sheets (11) are laminated together with the conductor foil (12) and its related structures.
10. Method according to any of Claims 1 - 9, in which the surface of the conductor foil (12), to which the component (6) is attached, comprises a uniform insulator layer (13).
- 20
11. Method according to any of Claims 1 - 10, in which a spacer (15) is placed between the component (6) and the conductor foil (12).
12. Method according to any of Claims 1 - 11, in which, in addition to the component (6), at least one other component (16) is located in the circuit module, in such a way that the manners of attachment of the first and second components differ from each other in the case of at least one property of the polymer layer (25).
- 25
13. Method according to any of Claims 1 - 12, in which the component (6) to be attached is a bumpless component.
- 30
14. Circuit module, which comprises

an insulator layer (1),

5 inside the insulator layer (1), at least one component (6), which comprises
contact areas (7), the material of which contains a first metal,

 on the surface of the insulator layer (1), conductors (22), which comprise at least
a first layer (12) and a second layer (32), in such a way that at least the second layer (32)
contains a second metal, and

10

 contact elements between the contact areas (7) and the conductors (22) for
forming electrical contacts, which contact elements comprise an intermediate layer (2),
which contains a third metal, on the surface of the material of the contact area (7),

15

 wherein the first, second, and third metals are different metals, and

 the contact surface area ($A_{CONT\ 1}$) between the intermediate layer (2) and the
contact area (7) is less than the surface area (A_{PAD}) of the contact area.

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15. Circuit module according to Claim 14, in which the first metal is aluminium, the
second metal is copper, and the third metal is at least one of the metals zinc and nickel.

16. Circuit module according to Claim 14, in which the first metal is gold, the second
metal is copper, and the third metal is nickel.

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17. Circuit module according to Claim 14 or 15, in which the material of the contact
areas (7) is mainly aluminium.

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18. Circuit module according to Claim 14, 15, or 17, in which the intermediate layer (2)
comprises a layer (33) containing zinc.

19. Circuit module according to Claim 18, in which the intermediate layer (2) comprises,

in addition to the layer (33) containing zinc, at least one second intermediate metal layer (34, 35).

20. Circuit module according to Claim 19, in which the at least one second intermediate metal layer (35) is of copper grown by a chemical growing process.

21. Circuit module according to Claim 20, in which the intermediate layer (2) comprises at least one layer (34) of nickel and/or of nickel and aluminium between the layer (33) containing zinc and the copper layer (35).

22. Circuit module according to any of Claims 18 - 21, in which the layer containing zinc contains zinc, copper, nickel, and iron.

23. Circuit module according to any of Claims 14 - 22, in which part of the intermediate layer (2) extends along the side walls of the contact elements between the contact areas (7) and the conductors (22).

24. Circuit module according to Claim 23, in which the contact elements comprise a copper core (29) made using an electrochemical growing method, which, in the direction of the side wall and component (6), is bounded by the intermediate layer (2) and, in the direction of the conductor (22) connects continuously, i.e. without an interface, to the material of the second layer (32) of the conductor (22).

25. Circuit module according to Claim 23 or 24, in which the part (37) of the intermediate layer (2) extending along the side walls of the of the contact elements contains copper grown by a chemical growing method, or nickel grown by a chemical growing method.

26. Circuit module according to any of Claims 14 - 25, in which the conductors (22) comprise

a first layer (12) of copper on the surface of the insulator layer (1), and

a second layer (32) of copper on the surface of the first copper layer.

27. Circuit module according to any of Claims 14 - 25, in which the conductors (22)
5 comprise

a first layer (12) of copper on the surface of the insulator layer (1),

an intermediate layer (2) on the surface of the first copper layer, and
10

a second layer (32) of copper on the surface of the intermediate layer.

28. Circuit module according to Claim 27, in which the part of the intermediate layer (2)
between the first and second coppers layers comprises copper grown by a chemical
15 growing method or nickel grown by a chemical growing method.

29. Circuit module according to any of Claims 14 - 28, in which the width (W_{CONT}) of
the contact surface between the contact element and the contact area (7) of the
component is 0 - 20 % less than the greatest width (W_{MAX}) of the contact element in the
20 same direction.

30. Circuit module according to any of Claims 14 - 29, in which the height (H) of the
contact element is less than, or equal to the greatest width (W_{MAX}) of the contact element.

25 31. Circuit module according to any of Claims 14 - 30, in which the insulator layer (1)
contains at least one layer of fibre material (19), in which there is an opening in the fibre
material (19) for the component (6), as well as a unified polymer layer, which is attached
to the fibre material (19) and to the component (6).

30 32. Circuit module according to any of Claims 14 - 31, which comprises a polymer layer
(25), between the conductors (22) and the component (6), in which layer there are
contact holes (18, 18) for the contact elements, and in which the contact elements fill the

contact holes (18, 28) completely.

33. Circuit module according to Claim 32, in which the polymer layer (25) between the conductors (22) and the component (6) comprises a first (15) and a second (5) polymer layer, in which the first polymer layer (15) is of a first polymer and the second polymer layer (5) is of a hardened adhesive.

34. Circuit module according to Claim 33, in which the first polymer layer (15) and the second polymer layer (5) are local, in such a way that they exist essentially only at the location of the component (6).

35. Circuit module according to any of Claims 14 - 34, in which the component comprises a passivation layer (9) on the surface of the component and the contact areas (7) are located inside openings in the passivation layer, in which case the intermediate layer (2) extends through the opening in the passivation layer.

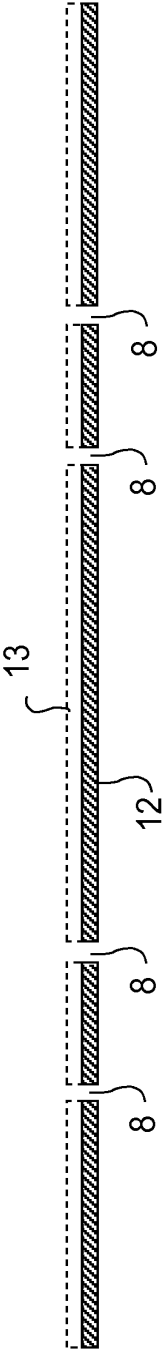


Fig. 1

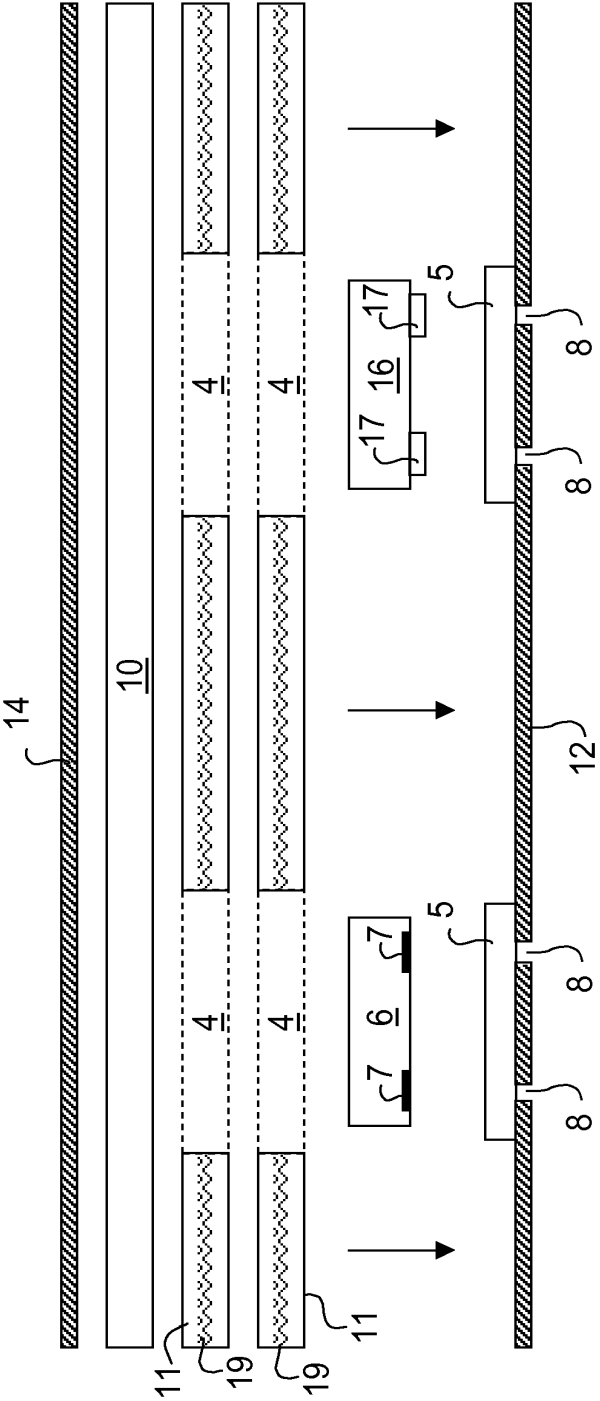


Fig. 2

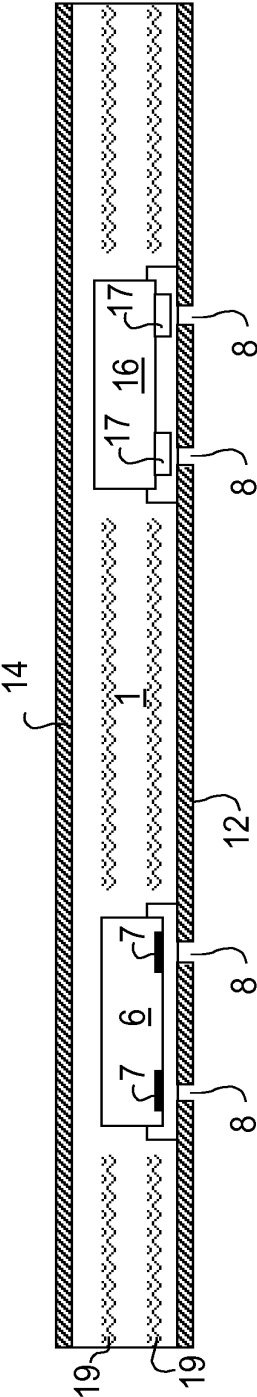


Fig. 3

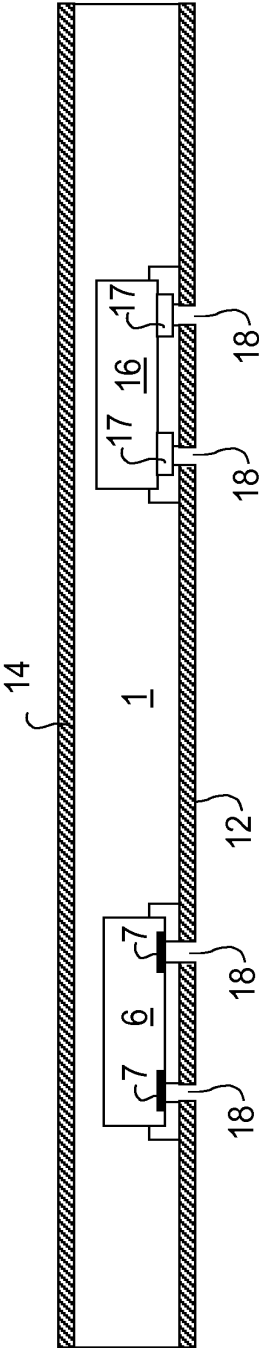


Fig. 4

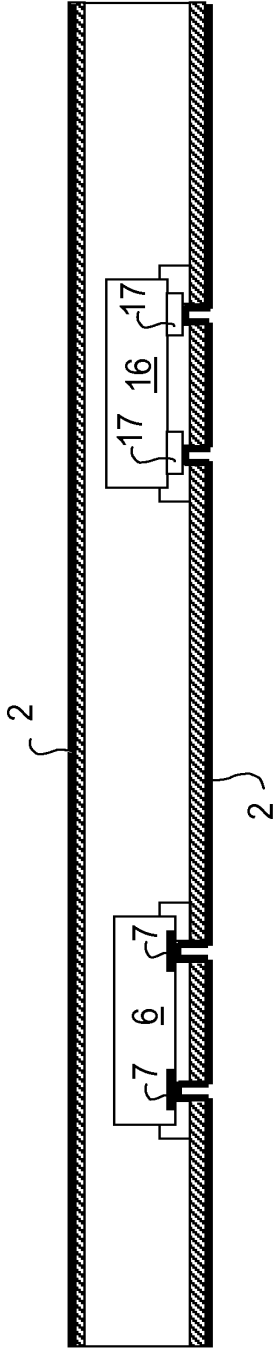


Fig. 5

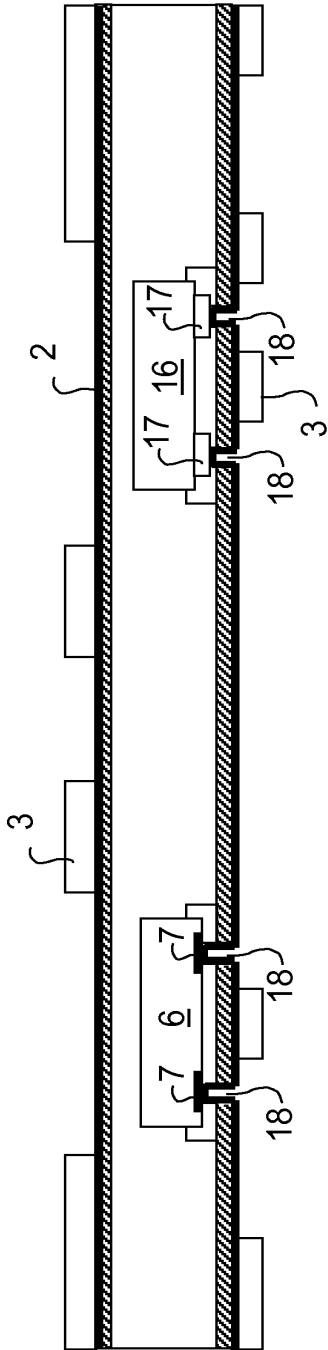


Fig. 6

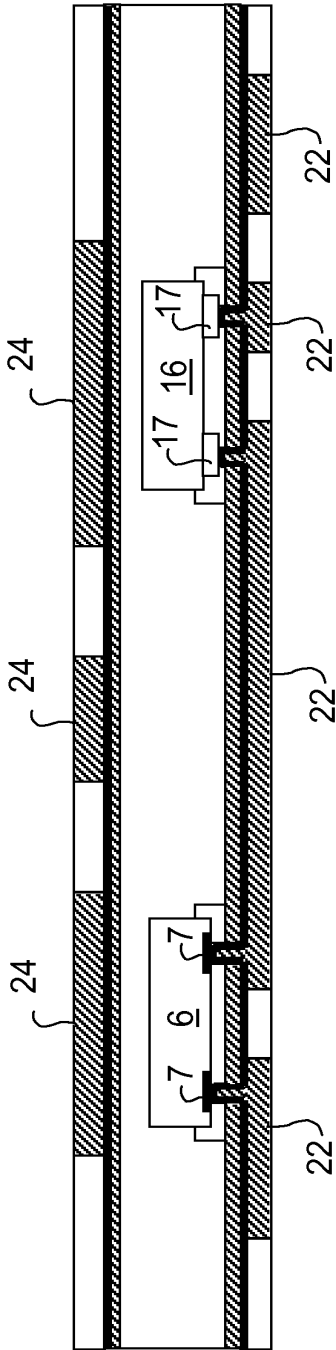


Fig. 7

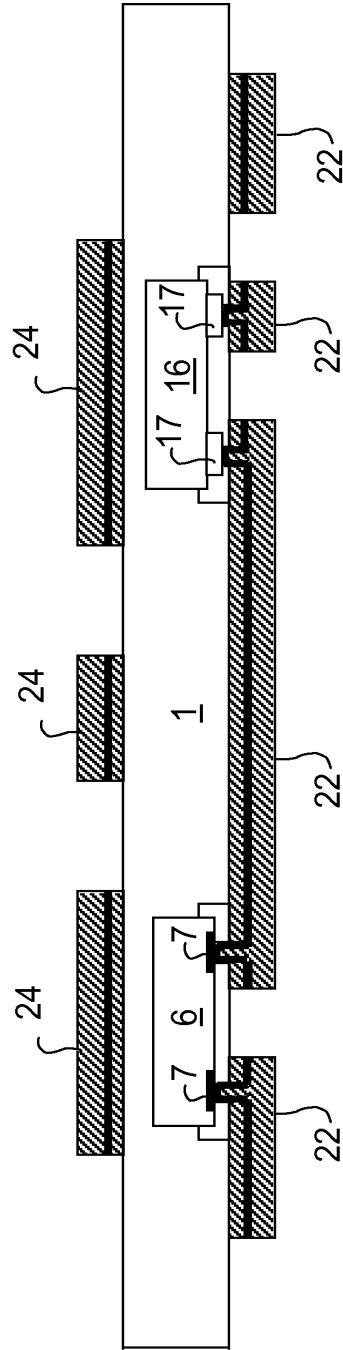


Fig. 8

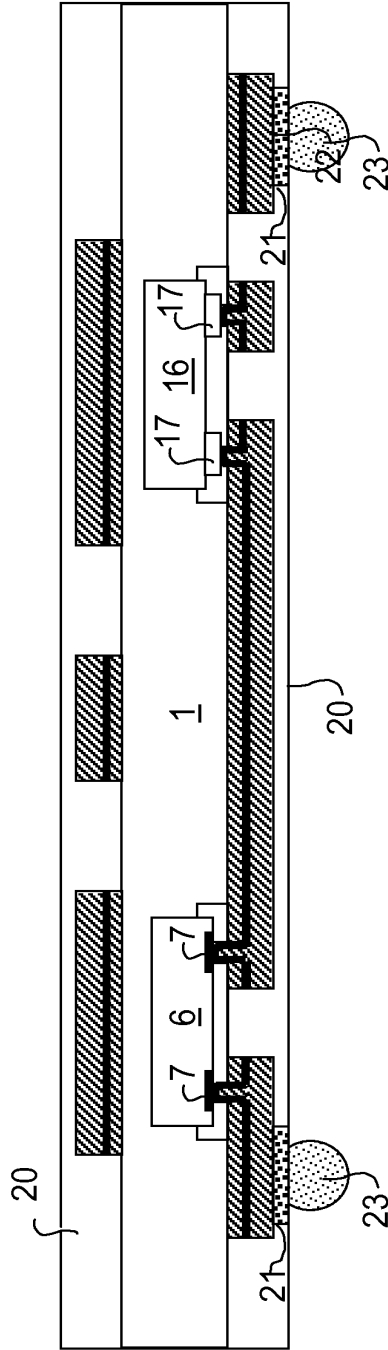


Fig. 9

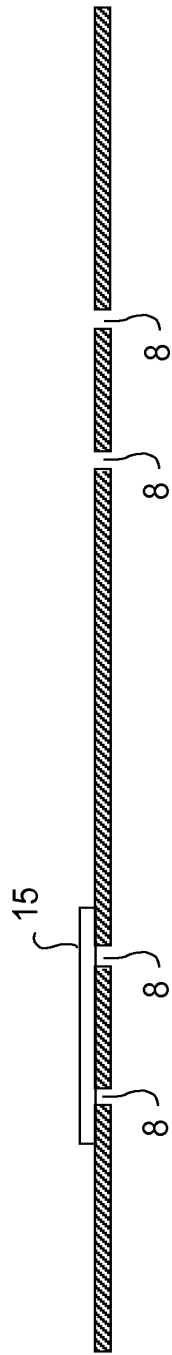


Fig. 10

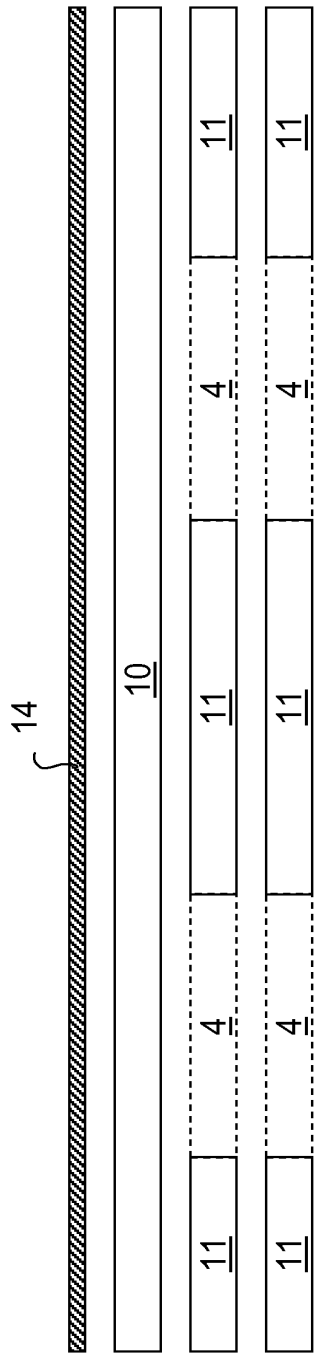
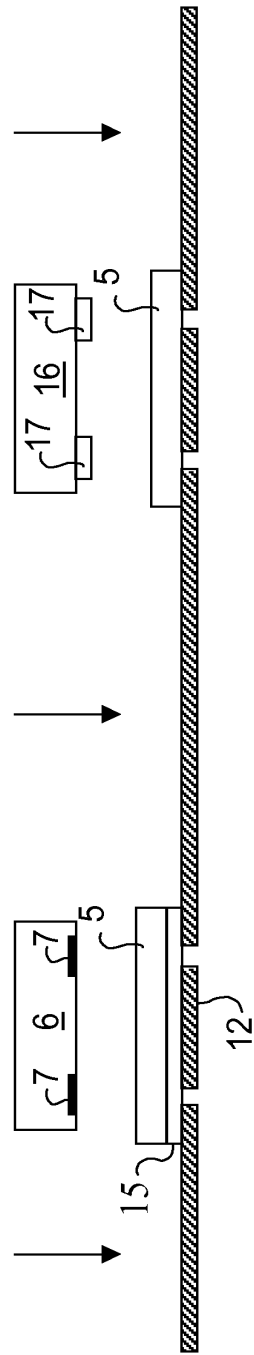


Fig. 11

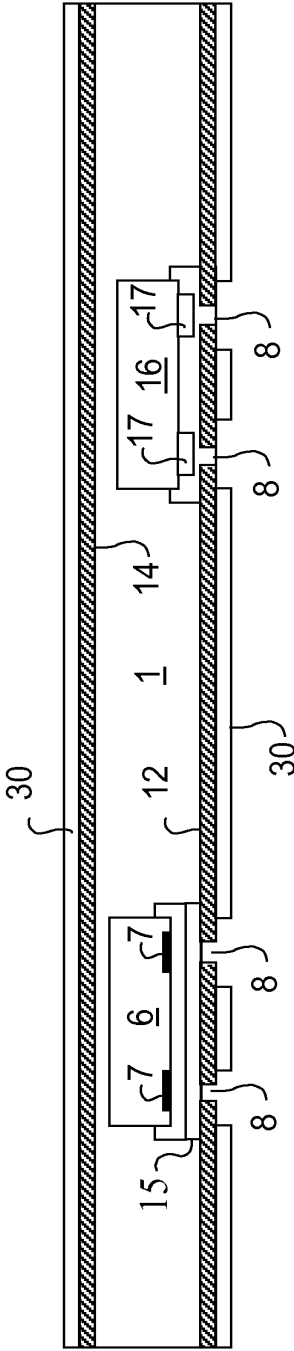


Fig. 12

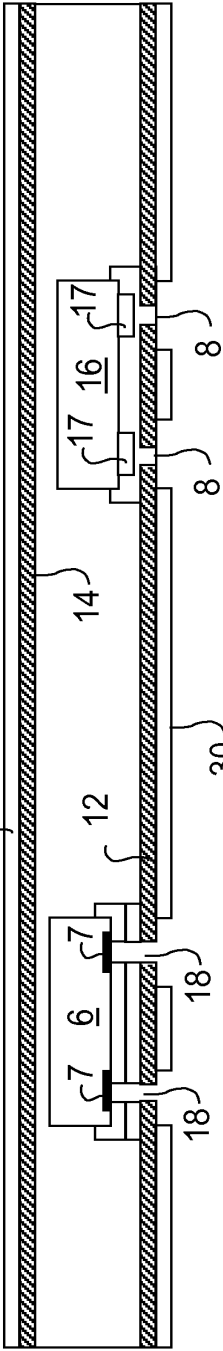


Fig. 13

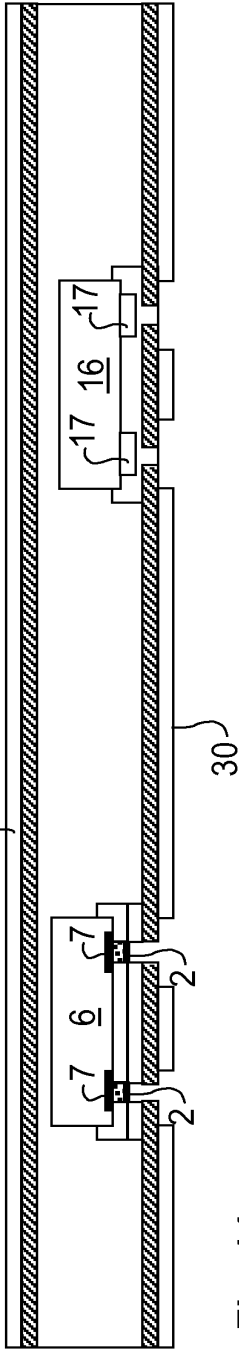


Fig. 14

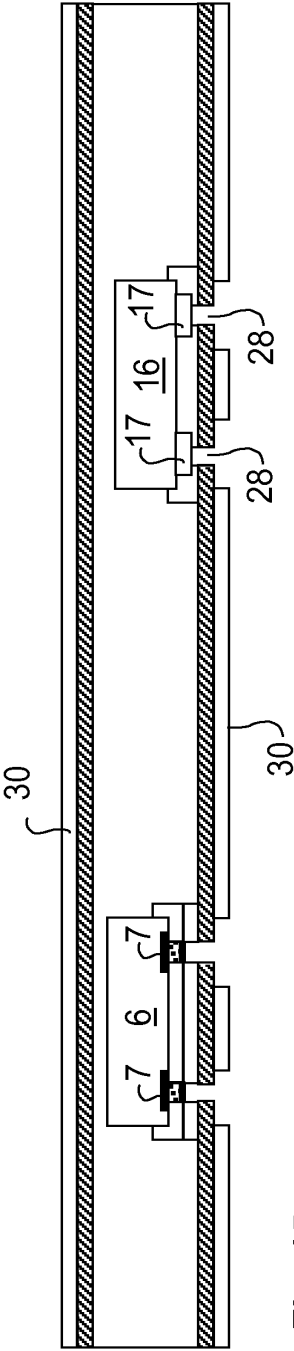


Fig. 15

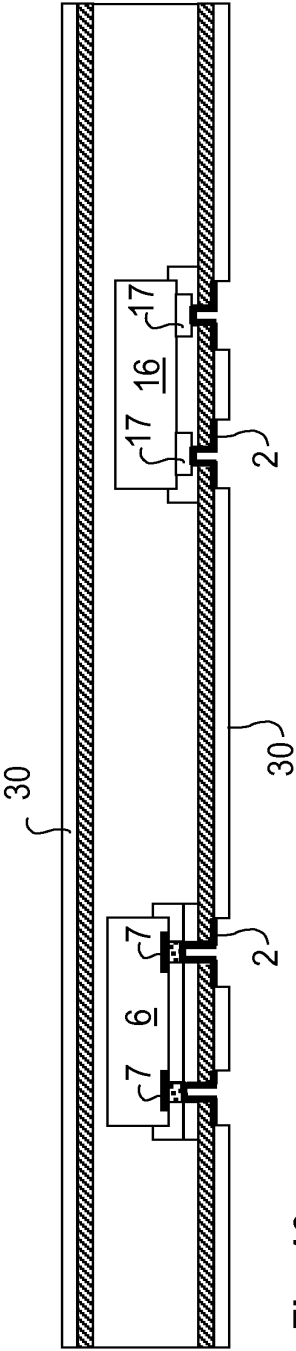


Fig. 16

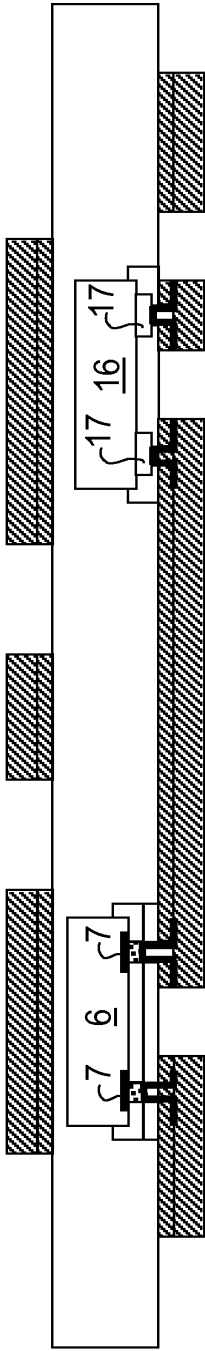


Fig. 17

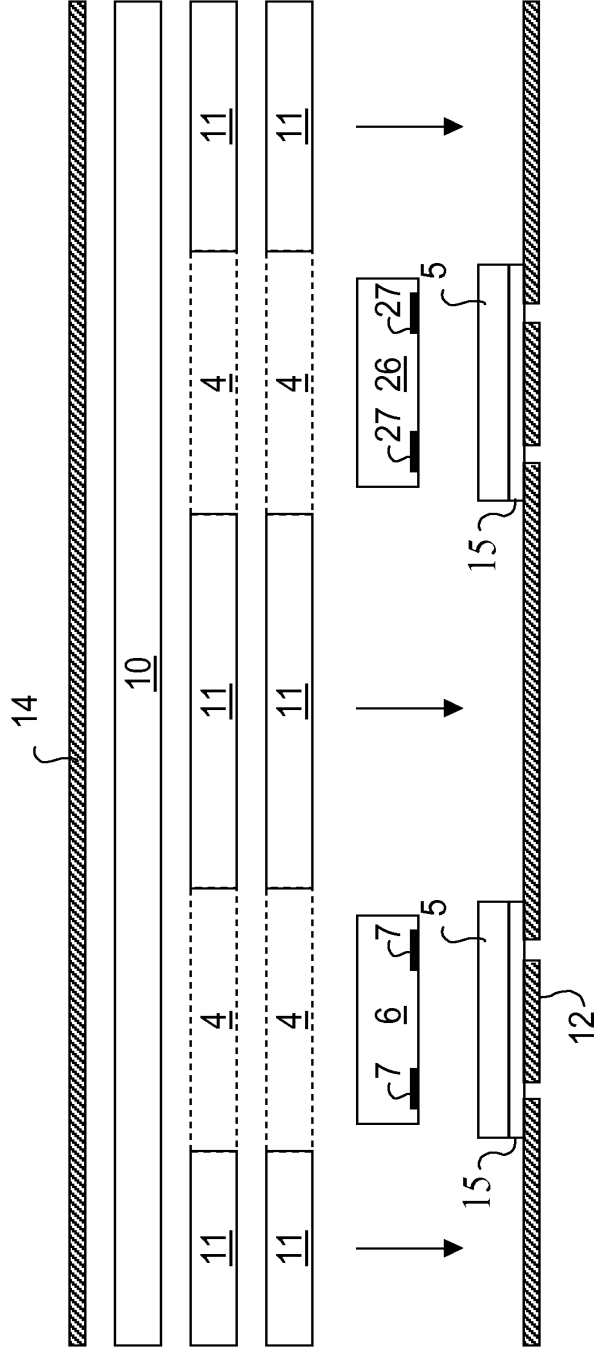


Fig. 18

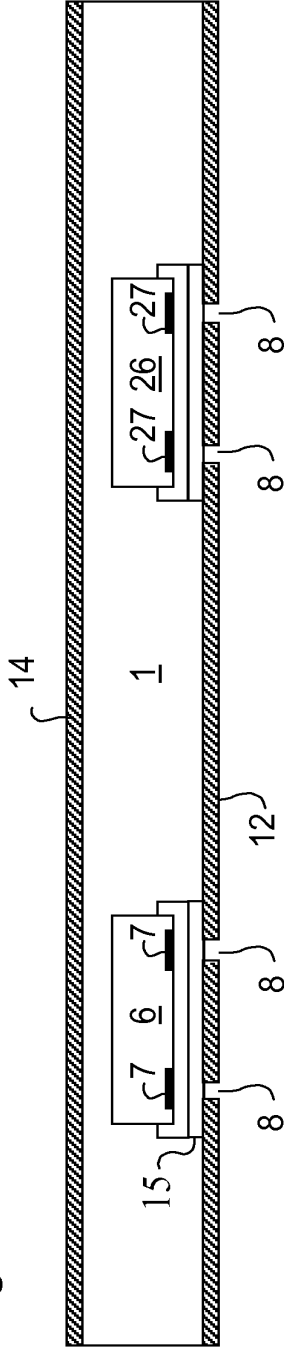


Fig. 19

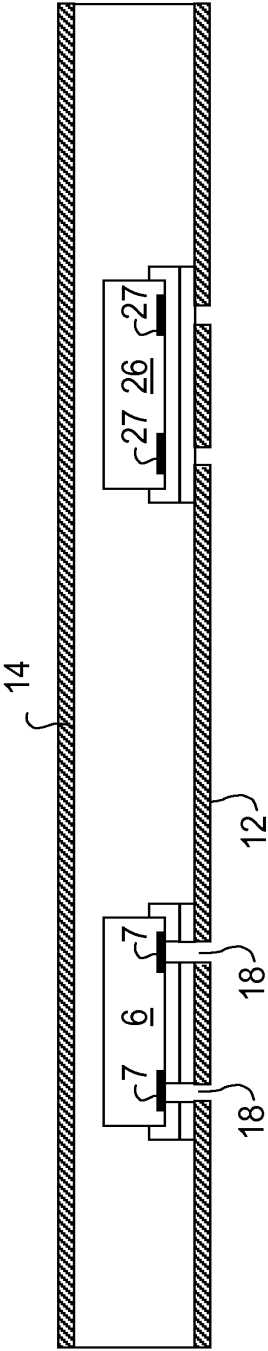


Fig. 20

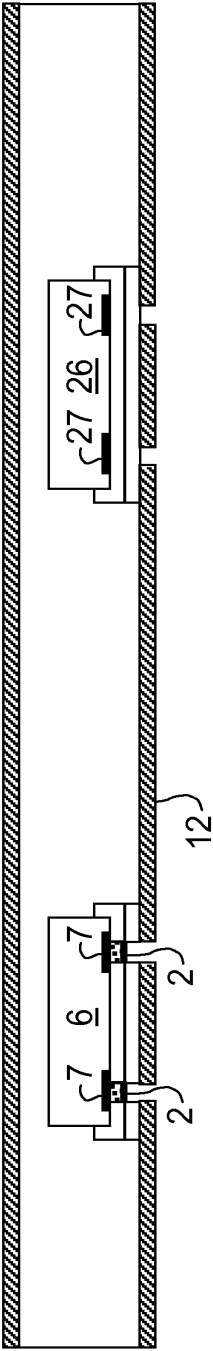


Fig. 21

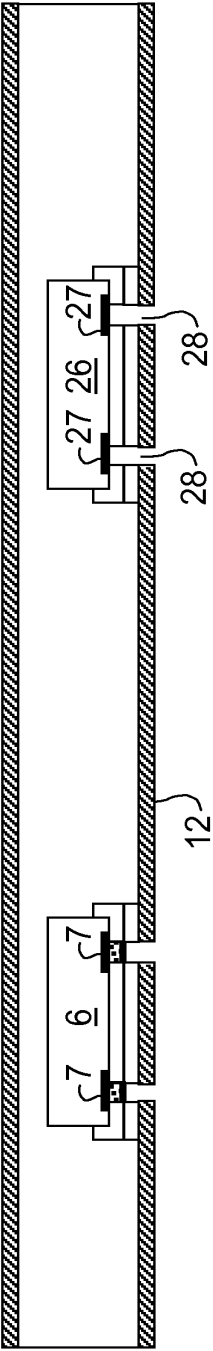
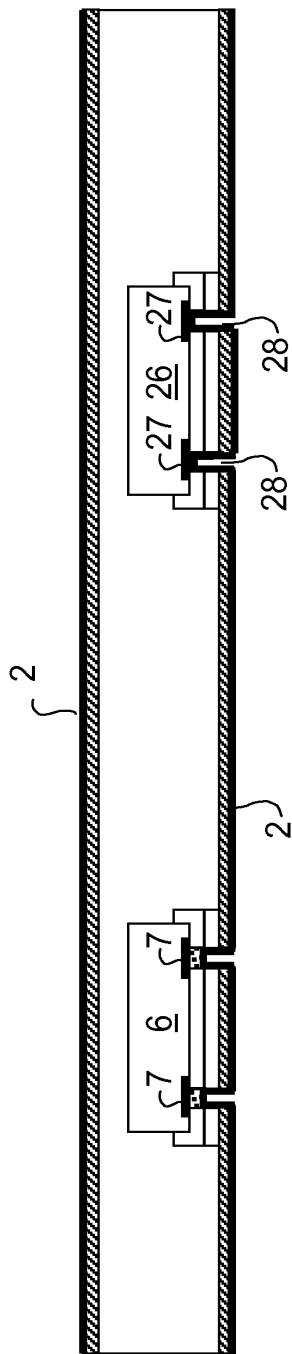
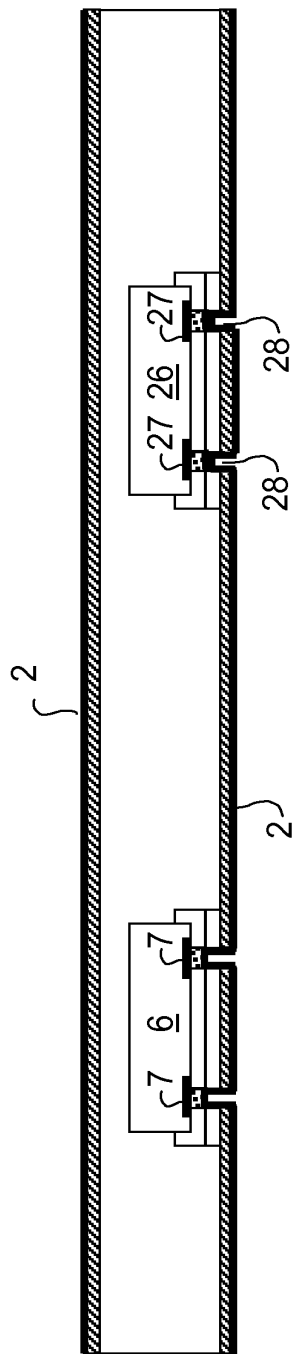


Fig. 22



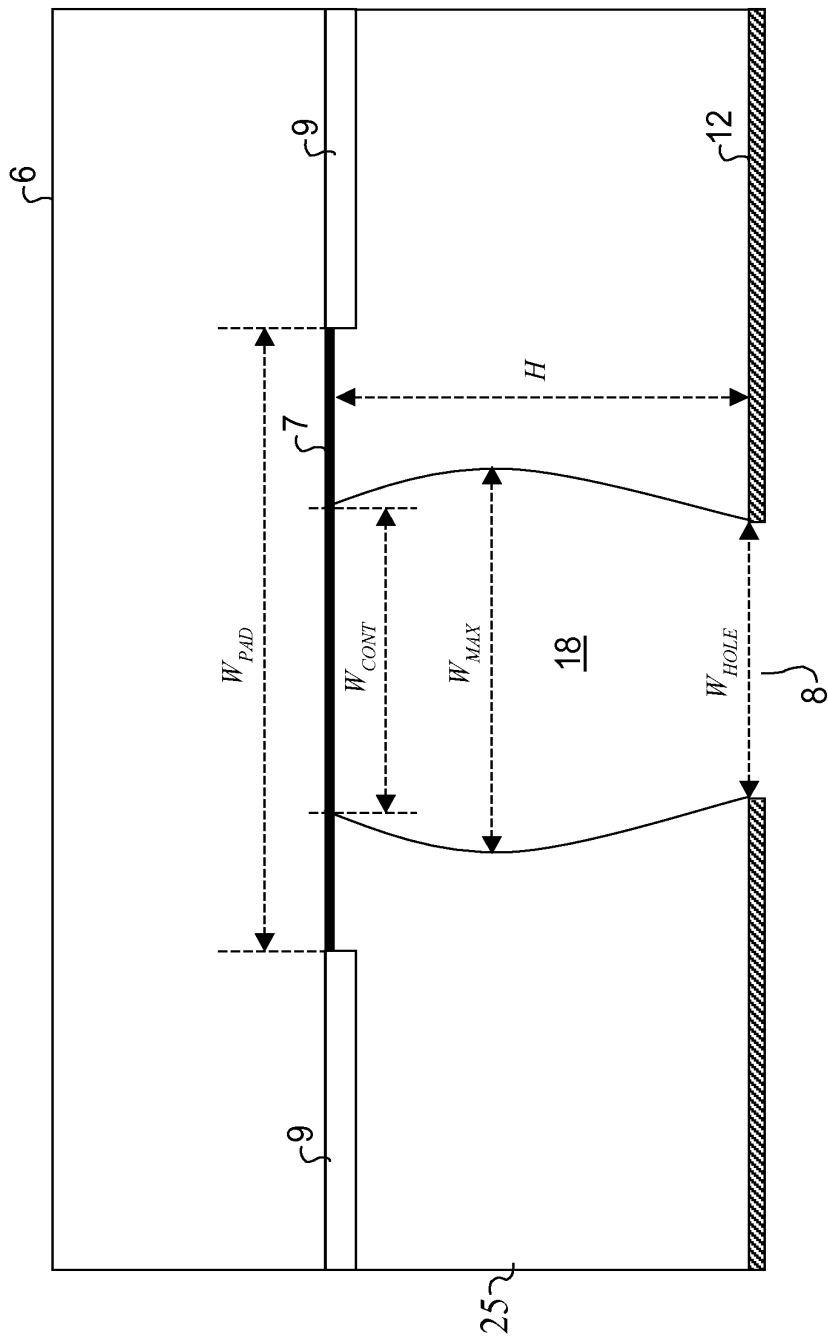


Fig. 25

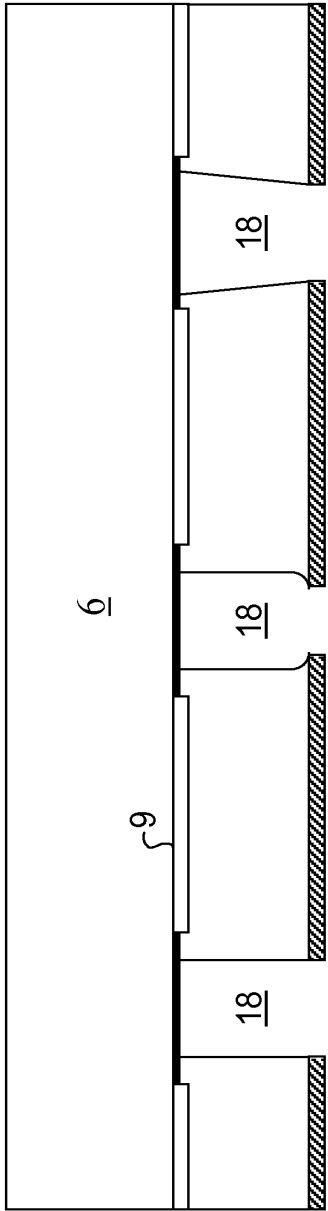


Fig. 26

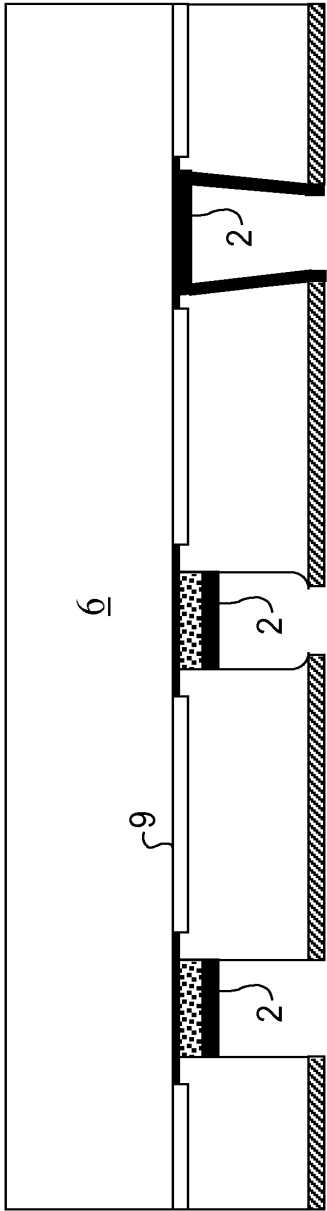


Fig. 27

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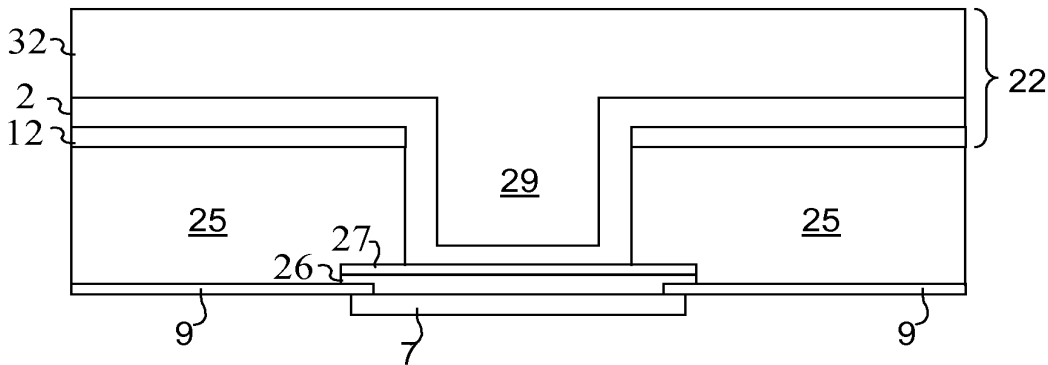


Fig. 28

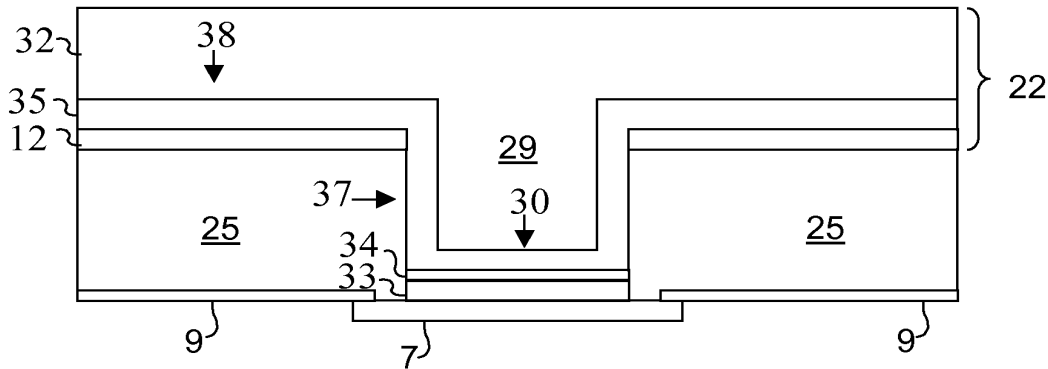


Fig. 29

14/15

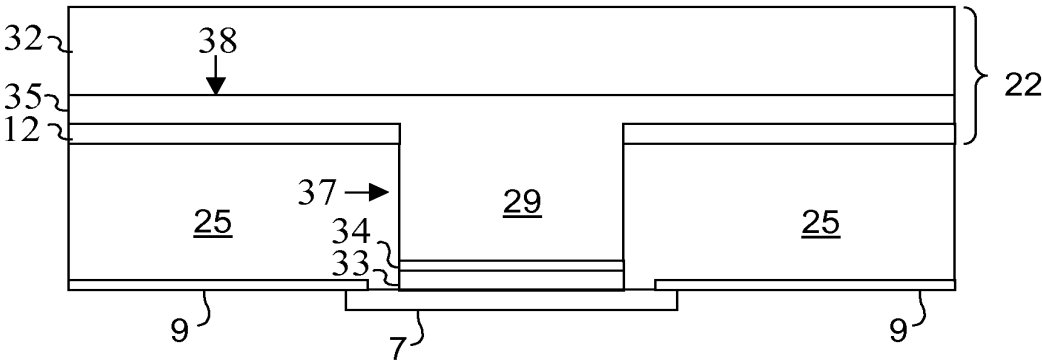


Fig. 30

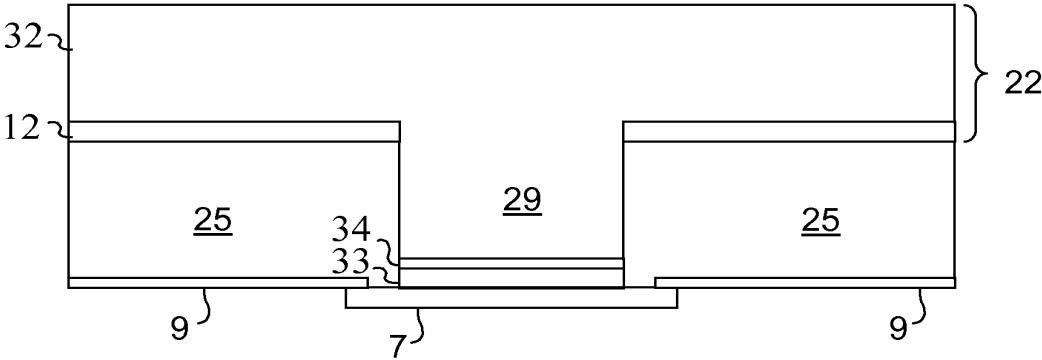


Fig. 31

15/15

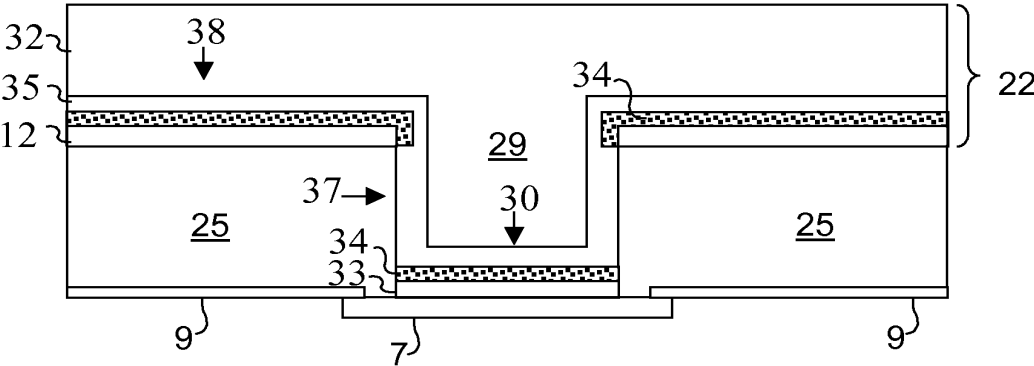


Fig. 32

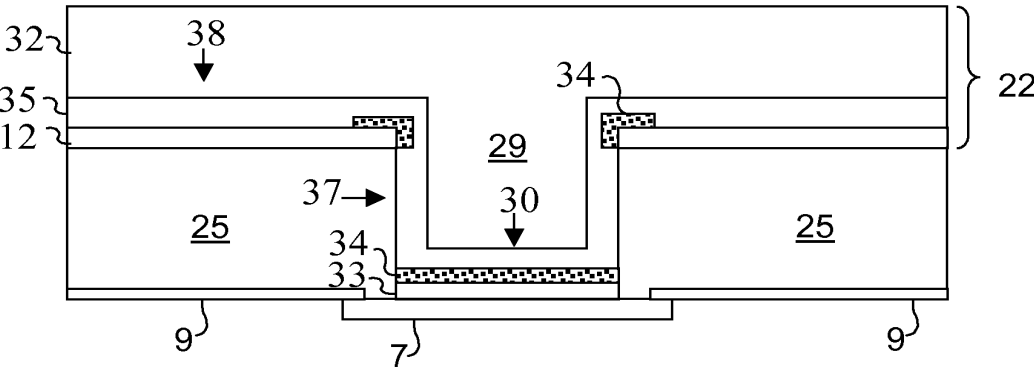


Fig. 33

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Keksinnön nimitys
Title of invention**"Piirimoduuli ja menetelmä piirimoduulin valmistamiseksi"**

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PIIRIMODUULI JA MENETELMÄ PIIRIMODUULIN VALMISTAMISEKSI

Tekniikan ala

Keksintö liittyy piirimoduuleihin, jotka käsittävät eristekerroksen ja eristekerroksen sisällä ainakin yhden komponentin, joka käsittää kontaktialueita. Lisäksi piirimoduulit käsittävät eristekerroksen pinnalla johteita, joiden kautta komponentti voidaan kytkeä osaksi komponentin ulkopuolista piiriä. Sähköisten kontaktien muodostamista varten piirimoduulit käsittävät kontaktielementtejä komponentin kontaktialueiden ja johteiden välillä.

Keksintö liittyy myös menetelmiin edellä mainittujen piirimoduulien valmistamiseksi.

10 Tunnettu tekniikka

Tunnetussa tekniikassa on kuvattu useita erilaisia tapoja, joilla voidaan valmistaa eristemateriaalin sisään sijoitettuja komponentteja sisältäviä piirimoduuleja. Tunnettu tekniikka esittää myös useita ratkaisuja sähköisten kontaktien valmistamiseksi komponentin kontaktiterminaleihin kontaktielementtien välityksellä sekä menetelmiä kontaktielementteihin liittyvän johdekuviokerroksen valmistamiseksi.

Piirimoduuleja ja valmistusmenetelmiä arvioitaessa voidaan kiinnittää huomiota esimerkiksi menetelmällä saavutettavan piirimoduulin ominaisuuksiin, esimerkiksi hintaan, mekaaniseen kestävyYTEEN ja saavutettavissa olevaan paksuuteen (ohuuteen). Sovelluskohteista riippuen merkittäviä seikkoja ovat myös sähköisten kontaktien laatu ja kestävyys sekä koko moduulin sähköisten ominaisuuksien luotettavuus ja laatu. Valmistuksen kannalta merkittäviä tarkasteltavia ominaisuuksia voivat olla myös esimerkiksi käytettävien valmistusmenetelmien luotettavuus, saanto, tehokkuus, hinta ja ympäristöystävällisyys. Valmistusmenetelmän käyttökelpoisuuteen vaikuttaa myös raaka-aineiden saatavuus ja menetelmän kyky sijoittaa piirimoduuliin erilaisia komponentteja.

Ylipäättään valmistusmenetelmille ja piirimoduuleille asetetut vaatimukset ovat siis hyvin monimuotoisia ja vaihtelevat sovelluskohteen mukaan. Näin ollen alalla on edelleen tarvetta kehittää uusia piirimoduulirakenteita ja valmistusmenetelmiä, jotka voivat tarjota uusia tai parannettuja ominaisuuksia tai ominaisuusyhdistelmiä.

Yksi kehityslinja on ollut komponenttien sijoittaminen elektroniikkamoduulin sisään nystyttöminä eli ilman nystyjen kasvattamista komponentin kontaktialueiden päälle. Tällöin olisi mahdollista saada kustannusetua, sillä komponentteja ei enää tarvitse välillä kuljettaa erilliseen tuotantolaitokseen nystyjen valmistamista varten.

- 5 Hakijan omista patentti- ja hakemusjulkaisuissa on kuvattu valmistustekniikoita, joita voidaan käyttää myös nystyttömien komponenttien yhteydessä. Kuvatut tekniikat soveltuvat erityisen hyvin sellaisille komponenteille, joiden kontaktialueiden materiaali on kupari. Hakijan omista julkaisuista läheisimmin keksintöön liittyvinä viitattakoon kansainvälisiin patenttihakemusjulkaisuihin WO 2004/089048, WO 2005/027602,
 10 WO 2005/125298, WO 2006/013230, WO 2006/056643, WO 2006/134216, WO 2006/134217 ja WO 2007/107630.

- Kupari on kuitenkin tällä hetkellä varsin vähän käytetty johdemateriaali puolijohdeprosesseissa. Yleisin johdemateriaali on alumiini. Piirilevyn valmistuksessa taas kupari on johteiden pääasiallinen materiaali. Piirimoduulin kupariset johteet on
 15 mahdollista kasvattaa suoraan alumiinisten kontaktialueiden päälle, mutta kuparin ja alumiinin välinen kontakti on hauras, joten tällainen moduuli ei ole optimaalinen sovelluskohteeseen, jossa piirimoduuliin kohdistuu mekaanista rasitusta.

- Parannettu mahdollisuus käyttää alumiinisia tai alumiinia sisältäviä kontaktialueita tarkoittaisi siis sitä, että piirimoduulissa ja valmistusmenetelmässä olisi mahdollista
 20 käyttää tavallisia puolijohdepiirejä nystyttöminä suoraan puolijohteiden valmistusprosessien ja pinnan passivoinnin jälkeen. Koska alumiini on puolijohdeteollisuudessa yleisimmin käytetty johdemateriaali, piirimoduulin kontaktielementin hyvä yhteensopivuus alumiinin kanssa varmistaisi myös sen, että sopivia puolijohdepiirejä olisi saatavilla runsaasti ja edullisesti. Tällaisia valmistusmenetelmiä onkin yritetty
 25 kehittää jo vuosikymmenten ajan komponenttien paketoitintekniikan piirissä. Tällaisissa komponenttien paketoitintekniikoissa on ollut tavoitteena tekniikka, jolla komponentin ympärille voitaisiin valmistaa suhteellisen pienikokoinen komponenttipakkaus, joka sitten myöhemmin on tarkoitus liittää piirilevyyn. Paketoitintekniikasta poiketen tämän keksinnön kohteena olevien piirimoduulin valmistusmenetelmien tavoitteena on
 30 kyvykyys valmistaa koko piirilevy samassa prosessissa siten, että erillinen komponentin paketoitinvaihe voidaan jättää kokonaan pois. Tämä ei tietenkään sulje

pois sitä mahdollisuutta, että piirimoduulin valmistusmenetelmällä valmistettaisiin ainoastaan komponenttipaketti.

Patentissa US 4 246 595, Noyori et al., on kuvattu menetelmä, jossa komponentin kontaktialueet tuodaan kontaktiin eristekalvon kanssa, johon on tehty V-muotoiset avaukset. Avauksiin ja alumiinisten kontaktialueiden pinnoille kasvatetaan ensin kerros titaania (Ti) tai kromia (Cr). Tämän välimetallikerroksen tarkoituksena on estää kuparia diffuusiota alumiiniin ja puolijohdekomponenttiin sekä parantaa kuparin ja alumiinin välistä adheesiota. Lisäksi välimetallikerros toimii sähkönsäilytyksenä myöhemmän sähkökemiallisen kasvatuksen (electroplating) aikana, joten välimetallikerroksen on luotettavasti katettava myös avausten sivuseinämät. Titaani- tai kromikerroksen kasvattaminen edellyttää sputterointitekniikan käyttöä, mistä syystä avausten täytyy myös olla selvästi V-muotoisia. Sputterointi on kallista suuremmille pinnoille (piirimoduuleille) käytettynä ja lisäksi avara V-muoto pienentää saavutettavissa olevaa johdotustiheyttä. Vastaavan tyyppisiä kontaktirakenteita on kuvattu myös patenteissa US 4 783 695 ja US 4 894 115, Eichelberger et al., sekä patentissa US 5 353 195, Fillion et al.

Myöhemmin patentissa US 6 396 148, Eichelberger et al., pyritään ratkaisemaan sputterointiin liittyviä ongelmia siten, että välimetallikerros muodostetaan kasvattamalla alumiinisten kontaktialueiden pinnalle kerros nikkeliä. Patentin mukaan nikkelin kasvattaminen suoritetaan kemiallisella kasvatusmenetelmällä (electroless plating). Nikkelikerroksen päälle kasvatetaan kemiallisella kasvatusmenetelmällä vielä toinen kerros, joka peittää myös eristemateriaaliin kontakteja varten tehtyjen avausten sivuseinämät. Menetelmässä komponentit kiinnitetään ensin sivu- ja takapinnoiltaan eristekerrokseen ja tämän jälkeen komponentin etupinnalle ja kontaktialueiden päälle levitetään valokuvioitava polymeeri. Polymeeri kuvioidaan valottamalla ja kehittämällä avausten muodostamiseksi kontakteja varten.

Yksi mahdollisuus on kasvattaa nystyt piirimoduulin piirilevyosan johteiden pinnalle ja liittää komponentti johteisiin flip-chip -liitostekniikalla, esimerkiksi ultraäänibondauksella. Tällainen menetelmä on kuvattu hakijan omassa kansainvälisessä patenttihakemusjulkaisussa WO 2006/134220. Flip-chip -liitostekniikoita käyttäviin menetelmiin liittyy sekä tuotannollisia että kontaktin laatuun liittyviä ongelmia.

Keksinnön kuvaus

Tämän keksinnön tarkoituksena on kehittää nystyttömien komponenttien hyödyntämistä silmällä pitäen uusi kontaktielementtirakenne ja tällaista rakennetta käyttävä piirimoduuli ja valmistusmenetelmä.

- 5 Keksinnön yhden näkökannan mukaan piirimoduulissa käytetään nystytöntä komponenttia, jonka kontaktialueiden materiaali on eri metallia tai metalliseosta kuin piimoduulin johdekerrosten johteet. Komponentin kontaktialueet ja piirimoduulin johteet yhdistetään toisiinsa kontaktielementtien avulla, jotka sisältävät kontaktialueen materiaalin pinnalla välikerroksen, joka sisältää kolmatta metallia tai metalliseosta joka
- 10 poikkeaa kontaktialueiden ja johteiden materiaalista. Lisäksi kunkin kontaktielementin välikerroksen ja komponentin kontaktialueen välinen kontaktipinta-ala on pienempi kuin kontaktialueen pinta-ala.

- Keksinnön toisen näkökannan mukaan luodaan valmistusmenetelmä edellä kuvatun piirimoduulin valmistamiseksi, jossa komponentti kiinnitetään johdekalvoon tai
- 15 johdekuviokerrokseen polymeerikerroksen avulla ja kontaktielementit valmistetaan polymeerikerroksen läpi. Kontaktielementtejä valmistettaessa kontaktialueiden päällä olevaan polymeerikerrokseen tehdään kontaktireiät kontaktialueiden kohdille. Kontaktireiät mitoitetaan siten, että kunkin kontaktireiän ja vastaavan kontaktialueen välinen kontaktipinta-ala on pienempi kuin kontaktialueen kokonaispinta-ala. Tämän
- 20 jälkeen kontaktireiät täytetään johdemateriaalilla siten, että täyttäminen aloitetaan pinnoittamalla kontaktialueiden pinnalle välikerros esimerkiksi käyttämällä yhtä tai useampaa kemiallista metallinkasvatusmenetelmää.

Näin saadaan aikaan uudenlainen piirimoduuli ja valmistusmenetelmä, joka voi tarjota joitakin etuja joidenkin piirimoduulien sovelluskohteiden kannalta.

- 25 Lisäksi keksinnöllä on lukuisia erityisiä sovellusmuotoja, jotka tarjoavat lisää etuja.

Yhdessä sovellusmuodossa piirimoduulissa käytetään komponenttia, jonka kontaktialueiden materiaali sisältää alumiinia ja kontaktielementit käsittävät näiden alumiinia sisältävien kontaktialueiden pinnalla sinkkiä sisältävän kerroksen. Lisäksi kontaktielementit on valmistettu siten, että sinkkiä sisältävän kerroksen ja

kontaktialueen välinen kontaktipinta-ala on pienempi kuin itse kontaktialueen kokonaispinta-ala.

Sinkkiä sisältävän kerroksen on havaittu olevan hyödyllinen sähköisen kontaktin laadun kannalta, sillä sinkkiä sisältävän kerroksen pinnoittaminen alumiinisen kontaktialueen pinnalle estää alumiinipinnan uudelleen oksidoitumisen ja mahdollistaa hyvän adheesion muodostumisen alumiinin ja seuraavan kerroksen välille. Lisäksi sinkkiä sisältävä kerros parantaa alumiinin ja muuta metallia olevan välikerroksen välisen rajapinnan kautta muodostuvan kontaktin mekaanista kestävyyttä sivuttaissuuntaista rasitusta vastaan.

Olemme havainneet, että erityisen hyvä mekaaninen kestävyys saavutetaan käyttämällä kaksinkertaista sinkkaattiprosessia, jossa komponentit sisältävä aihio altistetaan sinkkaattiprosessille ainakin kahteen kertaan. Näin alumiinisten kontaktipintojen päälle saadaan kasvatettua tasaisempi ja tiiviimpi kerros sinkkiä. Yksinkertaisen sinkkaattikäsitellyn jälkeen kontaktipinnoilla on sinkkiä tyypillisesti vain aluittain tai kerros on huokoinen, joten edullisessa sovellusmuodossa käytetään kaksinkertaista sinkkaattiprosessia.

Mahdollisuus käyttää kontaktialuetta kapeampaa kontaktielementtiä voi puolestaan tarjota etua esimerkiksi siinä muodossa, että myös kontaktielementteihin liittyvät johteet voidaan näin valmistaa kapeiksi, varsinkin sellaisissa sovellusmuodoissa, joissa kontaktielementti on korkeussuunnassa oleellisesti tasalevyinen tai ainoastaan maltillisesti komponenttia kohti kapeneva.

Valmistusmenetelmän sovellusmuodossa, jossa johdekalvoon tai johdekuviokerrokseen tehdään kontaktiaukot ennen komponentin kiinnittämistä, komponentti voidaan kiinnittää kontaktiaukkojen suhteen kohdistettuna ja lisäksi kontaktielementtien valmistukseen tarvittavat kontaktireiät voidaan valmistaa näiden kontaktiaukkojen kautta käyttämällä johdekalvon tai johdekuviokerroksen materiaalia maskina. Tällaisessa sovellusmuodossa saavutetaan etua kontaktielementtien ja kontaktialueiden välisen kohdistuksen osalta. Lisäksi saavutetaan etua kontaktireikien valmistuksen kannalta, koska reiät voidaan avata esimerkiksi CO₂-laserilla.

Sovellusmuodossa, jossa kontaktireiät avataan laserilla, kontaktireikiä on mahdollista avata komponentti tai komponenttiryhmä kerrallaan ja näin valmistaa ensin

ensimmäinen välikerros ensin avattujen kontaktireikien kautta ensimmäisten komponenttien kontaktialueiden päälle ja sitten myöhemmin valmistaa toinen välikerros myöhemmin avattujen kontaktireikien kautta toisten komponenttien kontaktialueiden päälle. Näin on mahdollista sovittaa samaan prosessiin komponentteja, joiden kontaktialueiden materiaalit poikkeavat toisistaan eivätkä ole yhteensopivia samojen välikerroksen kasvatusprosessien kanssa.

Sovellusmuodoissa on myös mahdollista kiinnittää komponentit johteisiin keskenään erilaisten polymeerikerrosten välityksellä. Näin voidaan komponentin ja johteen välisen eristeen ominaisuudet sovittaa sopiviksi myös erilaisiin mekaanisiin ja sähköisiin tarpeisiin.

Kuvioiden lyhyt esittely

Kuviot 1–8 esittävät piirimoduulin välivaiheita yhden sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 9 esittää yhtä esimerkkiä yhden sovellusmuodon mukaisesta piirimoduulista

Kuviot 10–17 esittävät piirimoduulin välivaiheita toisen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuviot 18–23 esittävät piirimoduulin välivaiheita kolmannen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 24 esittää piirimoduulin yhtä välivaiheita neljännen sovellusmuodon mukaista valmistusmenetelmää käytettäessä

Kuvio 25 esittää yhtä mahdollista esimerkkiä piirimoduulin kontaktielementtiä varten tehdystä kontaktireiästä ja sen mittasuhteista

Kuvio 26 esittää esimerkkejä mahdollista kontaktirei'istä

Kuvio 27 esittää joitakin sovellusmuotoja kuvion 26 kontaktireikiin valmistetuista välikerroksista

Kuvion 28 esittää yhden kontaktielementtirakenteen

Kuvion 29 esittää toisen kontaktielementtirakenteen

Kuvion 30 esittää kolmannen kontaktielementtirakenteen

Kuvion 31 esittää neljännen kontaktielementtirakenteen

Kuvion 32 esittää viidennen kontaktielementtirakenteen

5 Kuvion 33 esittää kuudennen kontaktielementtirakenteen

Keksinnön suoritusmuotoja

10 Kuviot 1–9 esittävät yhden sovellusesimerkin yhden sovellusmuodon mukaisesta valmistusmenetelmästä. Tässä sovellusmuodossa valmistus aloitetaan johdekalvosta 12, joka on esimerkiksi metallia. Sopiva johdekalvo 12 on esimerkiksi kuparikalvo, jonka paksuus on välillä 1–70 μm , tyypillisesti välillä 3–12 μm . Paljaan johdekalvon 12 sijasta lähtömateriaalina voidaan käyttää myös kerroskalvoa, joka käsittää johdekalvon 12 ja tämän pinnalla eristekerroksen 13, joka kuviossa 1 on esitetty katkoviivoituksella. Seuraavassa kuvatuissa sovellusmuodoissa on mahdollista käyttää johdekalvon 12 sijasta tällaista kerroskalvoa 12, 13.

15 Kuvion 1 esittämästä poiketen voidaan käyttää myös sellaista kerroskalvoa, joka käsittää tukikalvon johdekalvon 12 toisella pinnalla. Tukikalvo on johdekalvoon liitettävien komponenttien suhteen johdekalvon vastakkaisella pinnalla. Mikäli kerroskalvo käsittää myös eristekerroksen 13, tukikalvo on tällöin johdekalvon vastakkaisella pinnalla kuin eristekerros 13. Tukikalvoa voidaan käyttää esimerkiksi
20 parantamaan johdekalvon 12 tai kerroskalvon 12, 13 mekaanista jäykkyyttä ja käsiteltävyyttä valmistusprosessin alkuvaiheessa. Tukikalvo on kuitenkin tarkoitus poistaa valmistusprosessin myöhemmässä vaiheessa. On myös mahdollista menetellä siten, että valmistus aloitetaan tukikalvosta ja tämän pinnalle valmistetaan johdekalvo 12, joka on kuvioitu tai kuvioimaton. Sovellusesimerkeissä kuvatut prosessiesimerkit ja
25 vaiheet voidaan suorittaa vastaavalla tavalla myös tukikalvoa käytettäessä, vaikka tätä ei olisi erikseen mainittu. Jäljempänä tulevassa kuvauksessa on kuitenkin viitattu tukikalvoon ainoastaan silloin, kun prosessissa on tukikalvoa käyttävän sovellusmuodon osalta jotakin erityistä huomattavaa. Itse tukikalvo voi olla esimerkiksi sähköäjohtavaa materiaalia, kuten alumiinia (Al), terästä tai kuparia, tai eristävää materiaalia, kuten

polymeeriä. Tukikalvo voi olla paksuudeltaan esimerkiksi 25–400 µm. Tyypillinen tukikalvon paksuus on välillä 35–105 µm.

Seuraavaksi johdekalvoon 12 tehdään kontaktiaukot 8, jotka sijoitetaan johdekalvolle 12 siten, että ne sijaitsevat valmistettavaan moduuliin sijoitettavien komponenttien kontaktiterminaalien kanssa kohdakkain. Johdekalvoon 12 valmistetaan siis kutakin komponentin kontaktiterminaalia varten oma kontaktiaukko 8. Kontaktiaukot 8 valmistetaan tässä sovellusmuodossa UV-laserin avulla. Kontaktiaukot 8 voidaan valmistaa myös esimerkiksi mekaanisesti poraamalla, jyrsimällä tai etsaamalla. Tukikalvoa käyttävässä sovellusmuodossa kontaktiaukot 8 valmistetaan mielellään vastakkaisen pinnan suunnasta siten, että ne läpäisevät kokonaan johdekalvon 12. Kontaktiaukkojen ei kuitenkaan tarvitse läpäistä tukikalvoa vaan menetelmä voidaan aivan hyvin suunnitella myös siten, että kontaktiaukot 8 ainoastaan ulottuvat tukikalvon materiaalin pintaan saakka tai muodostavat syvennykset tukikalvon materiaaliin kuitenkin tätä läpäisemättä. Kontaktiaukon ei tarvitse myöskään läpäistä kokonaan johdekalvoa, mikäli käytetään paksua johdekalvoa, joka ohennusetsataan ohuemmaksi myöhemmässä vaiheessa.

Kuvion 1 sovellusmuodossa kontaktiaukot 8 valmistetaan siten, että kontaktiaukon 8 koko on pienempi kuin kontaktiaukon 8 kohdalle sijoitettavan kontaktiterminaalin kontaktipinta-ala. Muodoltaan kontaktiaukko on tyypillisesti pyöreä, mutta muita muotoja voidaan myös käyttää. Kontaktiaukon 8 muoto ja koko valitaan siten, että kontaktiterminaalin kontaktipinta kykenee kokonaan peittämään kontaktiaukon 8.

Kuvion 2 mukaisesti valmistusta jatketaan levittämällä johdekalvon 12 pinnalle, komponenttien liitäntäalueille liimakerrokset 5. Tällöin liimakerrokset 5 peittävät myös kontaktiaukot 8. Vaihtoehtoisesti liima 5 voidaan levittää komponenttien pinnoille. Liima voidaan levittää myös sekä komponentin että johdekalvon 12 pinnalle. Tyypillisesti liima levitetään paikallisesti siten, että liimakerrokset 5 tulevat sijaitsemaan ainoastaan komponenttien liitäntäalueilla.

Liimalla tarkoitetaan materiaalia, jolla komponentit voidaan kiinnittää alustana olevaan johdekalvoon 12 tai eristekerrokseen 13. Liiman yksi ominaisuus on se, että liima voidaan levittää liimattavalle pinnalle suhteellisen juoksevassa tai muutoin pinnanmuotoihin mukautuvassa muodossa, esimerkiksi kalvon muodossa. Liiman

5 toinen ominaisuus on se, että levittämisen jälkeen liima kovettuu tai voidaan kovettaa ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan (johdekalvon 12 suhteen) ainakin niin kauan kunnes komponentti kiinnitetään rakenteeseen jollakin muulla tavalla. Liiman kolmas ominaisuus on adheesiokyky eli
5 kyky tarttua liimattaviin pintoihin.

Liimaamisella taas tarkoitetaan liimattavien kappaleiden kiinnittämistä toisiinsa liiman avulla. Sovellusesimerkeissä liimaa tuodaan komponentin ja alustana olevan johdekalvon 12 tai eristekerroksen 13 väliin ja asetetaan komponentti alustan suhteen sopivaan asemaan, jossa liima on kosketuksessa komponentin ja alustan kanssa ja
10 ainakin osittain täyttää komponentin ja alustan välisen tilan. Tämän jälkeen liiman annetaan (ainakin osittain) kovettua tai liima aktiivisesti kovetetaan (ainakin osittain) siten, että komponentti kiinnittyy liiman avulla alustaan. Joissakin sovellusmuodoissa komponentin kontaktiulokkeet saattavat liimauksen aikana työntyä liimakerroksen läpi kosketukseen alustan kanssa.

15 Sovellusmuodoissa käytettävä liima on tyypillisesti epoksipohjainen liima, esimerkiksi lämpökovetteinen epoksiliima. Liima valitaan siten, että käytettävällä liimalla on riittävä adheesio alustaan ja komponenttiin. Yksi edullinen liiman ominaisuus on sopiva lämpölaajenemiskerroin, jolloin liiman lämpölaajeneminen ei poikkea liian paljon ympäröivän materiaalin lämpölaajenemisesta prosessin aikana. Olisi myös eduksi,
20 mikäli valittavalla liimalla olisi lyhyt kovetus aika, mielellään korkeintaan muutamia sekunteja. Tässä ajassa liiman olisi hyvä kovettua ainakin osittain siten, että liima kykenee pitämään komponentin paikoillaan. Lopullinen kovettuminen voi viedä selvästi enemmän aikaa ja loppukovetus voidaankin suunnitella tapahtuvaksi myöhempien prosessivaiheiden yhteydessä. Lisäksi liiman valinnassa otetaan huomioon myöhempien
25 valmistusprosessin vaiheiden aiheuttama rasitus, kuten terminen, kemiallinen tai mekaaninen rasitus. Liiman sähkönjohtavuus on mielellään eristemateriaalien sähkönjohtavuuden luokkaa.

Seuraavaksi otetaan komponentit 6 ja 16, jotka käsittävät kontaktiterminaaleja 7 ja 17. Molemmat komponentit 6 ja 16 ovat puolijohdekomponentteja, esimerkiksi
30 prosessoreita, muistisiruja tai muita mikropiirejä. Komponentin 6 kontaktiterminaalit ovat kontaktialueita 7, jotka sijaitsevat oleellisesti komponentin pinnan tasalla. Tällaiset komponentin 6 kontaktialueet 7 on muodostettu puolijohdekomponentin valmistus-

prosessissa puolijohdetehtaalla. Kontaktialueen 7 muodostaa tyypillisesti prosessissa käytettyä metallia olevan johdekuvion pinta. Puolijohdekomponenttien valmistusprosessissa käytettävä metalli on yleisimmin alumiini, mutta myös muita metalleja, metalliseoksia tai muita johdemateriaaleja voidaan käyttää. Esimerkiksi kuparin käyttö on yleistynyt puolijohdekomponenttien valmistusprosesseissa.

Komponentin 16 kontaktiterminaalit ovat kontaktinystyjä 7, jotka ulkonevat komponentin pinnan tasalta. Tällaiset kontaktinystyt 17 on valmistettu nystytysprosessissa puolijohdekomponentin 16 valmistamisen jälkeen tyypillisesti erillisessä tehtaassa. Kontaktinysty 17 voi sisältää yhtä tai useampaa metallia, metalliseosta tai muuta johdemateriaalia. Tyypillisesti kontaktinystyn 17 uloin pinta eli kontaktipinta on valmistettu kuparista tai kullasta.

Komponentit 6 ja 16 kohdistetaan kontaktiaukkojen 8 suhteen siten, että kukin kontaktiterminaalit 7, 17 tulee vastaavan kontaktiaukon 8 kohdalle, ja painetaan vasten liimakerrosta 5. Tämän jälkeen liima ainakin osittain kovetetaan siten, että komponenttien 6, 16 ja johdekalvon 12 suhteellinen liike kohdistuksen jälkeen saadaan estettyä tai minimoitua. Kohdistuksessa ja liimaamisessa pyritään sellaiseen asemointiin, että kontaktiaukko 8 olisi keskellä vastaavaa kontaktiterminaalit 7, 17.

Tämän jälkeen kuvion 2 esimerkissä johdekalvon 12 päälle laminoidaan eristekalvoja 11, joihin on tehty komponentteja 6, 16 varten aukot, sekä yhtenäinen eristekalvo 10, joka on kovettamatonta tai esikovetettua polymeeriä. Laminoitaessa eristekalvot 10, 11 sulautuvat yhteen ja muodostavat komponenttien 6, 16 ympärille yhtenäisen eristekerroksen 1. Kuvion 2 sovellusmuodossa eristekalvot 11 ovat polymeerillä impregnoituja kuitumattoja tai kuitumateriaalilla vahvistettuja, esikovetettua polymeeriä sisältäviä kalvoja. Polymeeri voi olla esimerkiksi epoksi ja kuituvahviste voi olla esimerkiksi lasikuitumatto. Tyypillinen esimerkki sopivasta eristekalvon 11 materiaalista onkin FR4-tyyppinen lasikuituvahvistettu epoksikalvo. Myös muita vahviste- ja polymeerimateriaaliyhdistelmiä voidaan tuki käyttää. Käytettäessä useampaa eristekalvoa 11 on myös mahdollista, että kalvot ovat keskenään erilaisia.

Kuitumateriaalia on kuvattu kuvioissa 2 ja 3 aaltoviivoituksella 19. Jäljempänä tulevilla kuvioissa kuitumateriaalia 19 ei ole esitetty, mutta myös nämä rakenteet sisältävät kuitumateriaalin 19. Eristekalvon 11 tai eristekalvojen 11 sisältämä kuitumateriaali 19

toimii vahvikkeena, joka antaa valmistettavalle elektroniikkamoduulille mekaanista
 lujuutta. Kuvion 2 esimerkin mukaisesti eristekalvoihin 11 on tehty reiät 4
 komponenttien 6, 16 kohdille. Eristekalvot 11 rei'itetään erityisesti sen takia, että
 eristekalvojen 11 sisältämään kuitumateriaaliin 19 saadaan valmistettua aukot
 5 komponentteja varten. Ilman rei'tystä komponentit painautuisivat laminoitaessa
 kuitumateriaalikerroksia 19 vasten. Rei'ttämätön eristekalvo 10 sen sijaan voi
 sovellusmuodosta riippuen olla kuituvahvistettu tai vahvistamaton.

Eristekalvot 10, 11 valitaan tyypillisesti siten, että se sisältävät niin paljon
 virtauskelpoista polymeeriä, että laminoitivaiheessa virtaava polymeeri riittää
 10 täyttämään eristekalvoihin 11 komponentteja 6, 16 varten tehdyt reiät 4 komponenttien
 ympäriltä. Tällöin saadaan kuvion 3 esittämä rakenne, jossa eristekerros 1 sisältää tiiviin
 polymeerikerroksen, joka sisältää yhden tai useamman kuitumateriaalia 19 olevan
 vahvikkeen. Polymeerikerros sitoutuu tiiviisti kuitumateriaaliin 19 ja tiivis
 polymeerikerros kiinnittyy myös komponenttien 6, 16 pintoihin, jolloin muodostuu
 15 tiivis, yhtenäinen ja mekaanisesti luja eristekerros, joka sisältää komponentteja 6, 16 ja
 joka on lisäksi vahvistettu kuitumateriaalilla 19.

Kuvion 2 esimerkissä käytettiin yhtenäistä eristekalvoa 10, mutta eristekalvo 10 on
 myös mahdollista jättää pois rakenteesta. Tällöin eristekalvo 11 tai eristekalvot 11
 valitaan siten, että ne jo itsessään sisältävät riittävästi virtauskykyistä polymeeriä
 20 eristekalvojen 11 sisältämien reikien 4 täyttämiseksi komponenttien 6, 16 ympäriltä.
 Tyypillisesti reikien 4 täyttyminen on kuitenkin helpompi varmistaa käyttämällä erillistä
 eristekalvoa 10.

Eristekalvojen 10, 11 kanssa yhdessä rakenteeseen laminoidaan myös johdekalvo 14,
 joka on mielellään samanlaista ja yhtä paksua materiaalia kuin johdekalvo 12.
 25 Eristekerros 1 ja komponentit 6, 16 jäävät näin vastaavanlaisten johdekalvojen 12 ja 14
 väliin. Moduulinvalmistuksen tällainen välivaihe on esitetty kuviossa 3. Kuvion 3
 välivaiheessa kontaktiterminaalien 7, 17 kontaktipinnoilla ja tyypillisesti myös
 kontaktiaukoissa 8 on liimaa. Kuvion 4 esittämässä vaiheessa tämä liima poistetaan ja
 muodostetaan kontaktiaukkojen 8 kohdalle kontaktireiät 18, jotka ulottuvat
 30 kontaktiterminaalien 7, 17 kontaktipinnoille saakka.

Kuvioon 3 viitaten mainittakoon vielä, että rakenne voidaan valmistaa myös siten, että komponenttien 6, 16 ja johdekalvon 14 välissä kulkee yhtenäinen kerros kuitumateriaalia 19. Tällaista rakennetta voidaan käyttää silloin, kun komponenttien 6, 16 paksuus on riittävän paljon pienempi kuin eristekerroksen 1 paksuus. Rakenne voidaan valmistaa esimerkiksi siten, että rakenteeseen laminoidaan yhtenäinen eristekalvo 10, joka sisältää kerroksen kuitumateriaalia 19.

Mikäli sovellusmuodossa käytetään johdekalvon 12 pinnalla tukikalvoa, kuten on edellä kuvion 1 selityksen yhteydessä kuvattu, tukikalvo on sopivinta poistaa laminoinnin jälkeen eli kuvioden 3 ja 4 esittämien välivaiheiden välissä.

Laminoinnin ja mahdollisen tukikalvon poistamisen jälkeen poistetaan kontaktiaukkoihin 8 ja kontaktiaukkojen 8 ja kontaktiterminaalien 7, 17 väliin syntynyt liimakeros. Kuvioden sovellusmuodossa liiman poistaminen toteutetaan laser-ablaatiomenetelmällä käyttämällä CO₂-laseria. CO₂-laserin kyky haihduttaa orgaanisia eristeaineita, kuten epoksipohjaista liimaa, on hyvä mutta kyky haihduttaa kuparia tai muita metalleja on heikko, joten johdekalvoa 12 voidaan käyttää maskina kontaktireikien 18 valmistamiselle. Näin on mahdollista valmistaa kontaktireikiä 18, joiden halkaisija on pienempi kuin CO₂-laserin säteen halkaisija. Tämä ominaisuus muodostaa merkittävän edun, sillä CO₂-laserin säteen minihalkaisija on tyypillisesti luokkaa 75 µm, mikä on liian suuri tarkkojen elektroniikkamoduulirakenteiden valmistamista ajatellen. UV-laserilla taas tyypillisesti pystytään valmistamaan selvästi tarkempia rakenteita. UV-laserin säteen minimihalkaisija voi olla esimerkiksi 25 µm, mutta UV-laser taas ei sovellu liiman poistamiseen kontaktiaukoista 8 ja kontaktiaukkojen 8 ja kontaktiterminaalien 7, 17 välistä.

Johdekalvomaskin käyttäminen mahdollistaa siis hyvin tarkkarajaisten ja tarkasti kohdistettujen kontaktireikien 18 valmistamisen eristemateriaaliin, kuten sovellusmuodossa käytettyyn liimaan 5. Lisäksi CO₂-laserin käyttö mahdollistaa kontaktiterminaalien 7, 17 kontaktipintojen puhdistamisen samassa prosessivaiheessa ilman merkittävää vaaraa kontaktiterminaalien 7, 17 tuhoutumisesta tai vaurioitumisesta. Sovellusmuodossa johdekalvo 12 on kuparia ja komponentin kontaktiterminaalit 7, 17 ovat myös metallia, joten ne eivät ole herkkiä CO₂-laserin säteelle ja näin ollen prosessi voidaan suunnitella siten, että kontaktiterminaalien 7, 17 kontaktipinnat tulevat varmasti riittävän hyvin puhdistetuiksi. Esitetyn menetelmän etuna on siis se, että johdekalvoon

12 voidaan valmistaa kontaktiaukot 8 hyvin tarkasti UV-laserin avulla ja tämän jälkeen käyttää kontaktiaukkoja 8 maskina kontaktireikien 18 valmistamiselle epätarkemmalla mutta rakenteen kannalta turvallisemmalla CO₂-laserilla.

5 Mikäli johdekalvon 12 kontaktireiät 8 valmistettaisiin vasta tässä prosessivaiheessa, johdekalvon 12 metallin työstämiseen käytettävä menetelmä, esimerkiksi UV-laser, vaurioittaisi helpommin myös kontaktiterminaaleja 7, 17, koska johdekalvon 12 läpäisemiseen tarvittava energia on merkittävästi suurempi kuin liiman 5 tai muun kontaktiterminaalien 7, 17 ja johdekalvon 12 välissä olevan eristeen läpäisemiseen tarvittava energia. Porauksen pysäyttäminen juuri oikeaan syvyyteen olisi siis
10 haastavaan tällaisessa valmistusmenetelmässä. Lisäksi porauksen kohdistaminen olisi vaikeampaa laminoinnin aikana syntyneiden muodonmuutosten johdosta ja siitä syystä, että komponenttien kontaktiterminaaleja 7, 17 ei voi nähdä yhtenäisen metallikalvon läpi. Johdekalvoon 12 esivalmistettujen kontaktireikien 8 käyttö tarjoaakin merkittäviä etuja sekä komponenttien 7, 17 kohdistamisessa että kontaktireikien 18
15 valmistamisessa.

Kuviossa 5 kontaktireikiin 18 valmistetaan välikerros 2, joka on soveltuvaa johdemateriaalia. Välikerros 2 valmistetaan soveltuvalla kemiallisella johdemateriaalin kasvatusmenetelmällä (electroless plating). Välikerros 2 voi koostua myös kahdesta tai useammasta eri materiaalia olevasta kerroksesta, jotka valmistetaan vastaavasti kahdella
20 tai useammalla menetelmällä. Välikerroksen 2 yhtenä tarkoituksena on muodostaa kontaktireikien 18 sivuseinämille johdekalvo, joka yhdistää kontaktiterminaalin 7, 17 ja johdekalvon 12 toisiinsa. Välikerroksen 2 toisena tarkoituksena on materiaalisovituksen tarjoaminen kontaktiterminaalin 7, 17 materiaalin ja näihin yhdistettävien johdekuvioiden materiaalin välillä. Tällaista materiaalisovitusta voidaan tarvita esimerkiksi
25 mekaanisen tai sähköisen kontaktin laadun ja kestävyuden varmistamiseksi esimerkiksi silloin, kun piirimoduulin johdekuviokerrosten materiaali on kupari ja kontaktiterminaalien 7, 17 materiaali on jokin muu kuin kupari (Cu), esimerkiksi alumiini (Al).

Välikerroksen 2 valmistamisessa käytetään soveltuvaa kemiallista kasvatusmenetelmää, koska tällaisella menetelmällä on mahdollista kasvattaa johdemateriaalia myös
30 kontaktireikien 18 pystysuorille pinnoille toisin kuin esimerkiksi sputteroimalla. Sähkökemiallista menetelmää (electroplating) taas ei voi tässä vaiheessa käyttää, koska kontaktireikien 18 sivuseinämät eivät ole johtavia. Vaihtoehtoisesti voidaan käyttää V-

muotoisesti avautuvia kontaktireikiä ja sputteroimalla valmistettua välikerrosta 2. Tarkoitukseen soveltuvia sputteroitavia materiaaleja ovat esimerkiksi titaani-wolframi (TiW) ja kromi (Cr). TiW- tai Cr-kerroksen päälle voidaan myös kasvattaa kerros nikkeliä (Ni) ja kultaa (Au). Kuvion 5 esimerkissä käytetään kuitenkin välikerroksena 2
 5 kemiallisella menetelmällä kasvatettua nikkeliä, jolloin välikerros 2 kasvaa samalla myös johdekalvojen 12 ja 14 pinnoille. Toinen esimerkki välikerroksesta 2 on kontaktiterminaalien 7, 17 pinnalle valmistettava sinkkiä sisältävä kerros, jonka päälle voidaan vielä valmistaa kerros nikkeliä (Ni). Lisää mahdollisia vaihtoehtoja kuvataan kuvioden 26–33 kuvauksen yhteydessä.

10 Välikerroksen 2 valmistamisen jälkeen tässä sovellusmuodossa valmistamista jatketaan levittämällä moduulin molemmille pinnoille resistikerrokset 3, tyypillisesti valoresistikerrokset. Resistikerrokset 3 kuvioidaan johdekuviomaskin avulla valottamalla ja kehittämällä siten, että resisti 3 poistuu johdekuviokerrosten haluttujen johdekuvioiden kohdilta. Tämä välivaihe on kuvattu kuviossa 6. Tämän jälkeen
 15 moduuli viedään sähkökemialliseen kylpyyn ja moduulin välikerrokseen 2 johdetaan jännite. Tällöin resistikerrosten 3 aukkoihin kasvatetaan halutut johdekuviokerrosten johteet 22, 24. Johdemateriaali kasvaa samalla myös kontaktireikiin 18 muodostaen kontaktielementeille johdeytimen, mikä käy ilmi kuviosta 7. Kuvion 7 esimerkissä johteet 22, 24 ovat sähkökemiallisesti kasvatettua kuparia. Lopuksi johteiden 22, 24
 20 pinnalle kasvatetaan ohuet etsausmaskikerrokset. Etsausmaskina voi toimia esimerkiksi kerros tinaa (Sn).

Seuraavaksi poistetaan resistikerrokset 3, jolloin kuvioden sovellusmuodossa poistetun resistin alta paljastuu välikerros 2. Paljastunut osa välikerrosta 2 poistetaan esimerkiksi etsaamalla ja samoin menetellään johteiden 22 ja 24 ulkopuolelta paljastuneille osille
 25 johdekalvoja 12 ja 14. Etsausmaskikerros suojaa tällöin johteiden 22 ja 24 ulommaisia pintoja etsin vaikutusta vastaan. Tällöin saadaan kuvion 8 esittämä kaksi johdekuviokerrosta (johteet 22 ja 24) käsittävä elektroniikkamoduuli, joka sisältää kaksi johteisiin 22 sähköisesti kytkettyä komponenttia 6 ja 16.

Kuvioden 6 ja 7 esimerkissä johteet 22 ja 24 kasvatetaan suoraan oikeaan muotoonsa resistikerrokseen 3 tehtyihin aukkoihin. Johteet 22 ja 24 voidaan kuitenkin valmistaa myös toisella tapaa sekä tässä esimerkissä että jäljempänä kuvatuissa esimerkeissä. Yksi vaihtoehtoinen valmistustapa on kasvattaa yhtenäinen kerros johdemateriaalia koko

moduuliaihion pintojen yli ja kuvioda johdekerros myöhemmin litografiamenetelmällä johteiden 22 ja 24 muodostamiseksi. Tasmällisemmin kuvattuna voidaan menetellä esimerkiksi siten, että kuvion 5 välivaiheesta jatketaan kasvattamalla molempien välikerrosten 2 pinnoille kuparia sähkökemiallisella menetelmällä. Tällöin myös kontaktireiät 18 täyttyvät kuparilla. Tämän jälkeen kuparikerrosten päälle levitetään resistikerrokset, kuviodaan resistit ja etsataan ylimääräiset osat kuparista, välikerroksista 2 ja johdekalvoista 12 ja 14. Tämän jälkeen resistimaski poistetaan. Molemmilla valmistustavoilla päädytään kuvion 8 esittämään rakenteeseen.

Kuvio 8 voi esittää jo valmista yksikertaista piirimoduulia, mutta valmistusta yleensä jatketaan valmistamalla piirimoduulin pinnoille lisää eriste- ja johdekuviokerroksia, jotka yhdistetään sähköisesti kuvion 8 esittämää rakenteeseen läpivientien avulla. Lisäksi on huomattava, että kuvion 8 moduuliinkin on voitu valmistaa läpivientejä, jotka yhdistävät johteita 22 johteisiin 24. Tällaisia läpivientejä voidaan valmistaa vastaavalla tavalla ja samoissa prosessivaiheissa kuin edellä on kontaktielementtien valmistamisesta esitetty.

Kuvion 8 moduulia voidaan jatkojalostaa myös kuvion 9 esittämään tapaan siten, että moduulin pinnat suojataan suojakerroksilla 20. Lisäksi kuvion 9 esimerkissä moduuliin on valmistettu ulkoiset kontaktielimet, jotka käsittävät johdekuvioiden 22, 24 päälle valmistetut alustat 21 sekä näiden pinnoille valmistetut kontaktipallot 23.

Kuviot 10–16 esittävät toisen sovellusmuodon mukaisen valmistusmenetelmän kuvion 5 esittämää välivaihetta vastaavaan vaiheeseen saakka. Kuvion 16 välivaiheesta valmistusta voidaan jatkaa esimerkiksi kuvioiden 6–9 esittämällä tavalla tai sopivasti myös vaihtoehtoisella tavalla, jossa johteiden 22 ja 24 materiaali ensin kasvatetaan kauttaaltaan koko pinnalle ja sen jälkeen kuviodaan johteiksi 22 ja 24. Kuvioiden 1–5 selostuksen yhteydessä esitetyt tekniset piirteet ja parametrit ovat sovellettavissa myös kuvioiden 10–16 esittämissä prosessivaiheissa, joten valmistusprosessin kaikkia yksityiskohtia ja niiden etuja ei seuraavassa suoritusesimerkissä toisteta turhan toiston välttämiseksi. Sen sijaan seuraavassa tuodaan esille oleelliset eroavaisuuden kuvioiden 1–9 ja kuvioiden 10–16 esittämien sovellusmuotojen välillä.

Kuvioiden 10–16 sovellusmuodossa valmistus aloitetaan kuvion 1 tapaan johdekalvosta 12, johon tehdään kontaktiaukot 8. Tämän jälkeen johdekalvon 12 pinnalle,

komponentin 6 tulevalle kiinnityskohdalle kiinnitetään korotuspala 15. Korotuspala 15 on soveltuvaa eristemateriaalia, esimerkiksi esikovetettua liimaa tai muuta polymeeriä, jolla on riittävä tarttuvuus johdekalvon 12 pintaan. Korotuspala 15 voi olla myös kovettunutta polymeeriä, jolloin se voidaan kiinnittää johdekalvon 12 pintaan
5 esimerkiksi erillisen liiman avulla.

Korotuspala 15 voidaan käyttää monestakin syystä. Yksi korotuspalan käyttötarkoitus on kasvattaa komponentin 6 ja johdekalvon 12 välistä eristepaksuutta. Tarve eristepaksuuden kasvattamiseen voi tulla esimerkiksi piirimoduulin tai komponentin 6 sähköisen toiminnan asettamista vaatimuksista. Tällöin korotuspalan 15 avulla voidaan
10 asettaa komponentin 6 ja johdekalvon 12 välisen eristyksen ominaisuudet halutuiksi. Valittavia ominaisuuksia voi olla esimerkiksi haluttu ominaisvastus ja läpilyöntikestävyys, johon voidaan vaikuttaa korotuspalan 15 ja liiman 5 materiaalin valinnalla. Korotuspala 15 voidaan käyttää myös komponentin ja johdekalvon 12 välisen oikosulun ehkäisemiseen. Tällainen käyttö tulee kyseeseen erityisesti sellaisissa
15 sovellusmuodoissa, joissa komponentin 6 pinta painautuu hyvin lähelle johdekalvoa, jolloin syntyy riski tahattomien sähköisten kontaktien muodostumisesta komponentin pinnalla olevien johderakenteiden ja johdekalvon välille. Korotuspala 15 voidaan käyttää myös kapasitiivisen kytketymisen heikentämiseksi komponentin 6 sisäisten piirilementtien ja komponentin 6 kohdalla kulkevien johteiden 22 välillä.

20 Korotuspalan 15 lisäksi tai sijasta samaan tarkoitukseen voidaan käyttää myös johdekalvon 12 pinnan kauttaaltaan peittävää eristekerrosta 13, jota kuvattiin kuvion 1 yhteydessä.

Kuvioiden 10–16 esimerkissä nystyttömän komponentin 6 yhteydessä käytetään korotuspala 15, mutta nystyllisen komponentin 16 kontaktiterminaalit 17 on saatava
25 ulottumaan lähemmäs johdekalvon 12 pintaa, jotta komponentin 16 vastakkaisen pinnan ja johdekalvon 14 välille saadaan varmistettua riittävä eristeväli. Sovellusmuodossa voidaankin piirimoduuliin sijoittaa komponenttikohtaisesti valittuja korotuspaloja 15 piirilevymoduulin sähköisten ja/tai mekaanisten ominaisuuksien optimoimiseksi. Sama piirimoduuli voi siis sisältää myös ominaisuuksiltaan erilaisia korotuspaloja 15 ja näin
30 ollen korotuspaloja 15 on mahdollista käyttää myös sarjatuotannossa eri lähteistä tulevien ja ominaisuuksiltaan toisistaan poikkeavien komponenttien 6, 16 saattamiseksi yhteensopiviksi käytetyn piirilevyvalmistusprosessin kanssa. Yksi esimerkki

optimoitavasta mekaanisesta ominaisuudesta on eristekerroksen 1 (ja samalla koko piirimoduulin) paksuus, jota voidaan pienentää sopivasti valittujen korotuspalojen 15 avulla, mikä voidaan nähdä esimerkiksi kuviosta 12.

Kuvion 11 mukaisesti valmistusta jatketaan levittämällä liimakerrokset 5 komponenttien liitântäalueille johdekalvon 12 ja korotuspalan 15 pinnoilla. Komponentit 6 ja 16 kohdistetaan kontaktiaukkojen 8 suhteen ja liimataan paikoilleen. Tämän jälkeen kuvion 11 esimerkissä johdekalvon 12 päälle laminoidaan eristekalvot 10, 11 sekä johdekalvo 14. Seuraavaksi johdekalvojen 12 ja 14 pinnoille levitetään valoresistikerrokset 30, jotka kuviodaan siten, että kontaktiaukkojen 8 kohdille syntyy kontaktiaukkoja 8 suuremmat avaukset tai pinnoitetaan elektroforeettisesti koko johtavan kerroksen päälle. Tätä valoresistikerrosta 30 käytetään rajaamaan myöhemmin ei-selektiivisellä menetelmällä kasvatettavan välikerrosmateriaalin kasvaminen kontaktireikiin ja kontaktiaukkojen 8 välittömään ympäristöön. Tällaista menettelyä on mahdollista käyttää myös edellä esitettyjen esimerkkien yhteydessä eikä se toisaalta ole välttämätöntä kuvioden 10–16 esimerkissä. Kuvio 12 esittää moduulia näiden vaiheiden jälkeen. Komponentin 6 kontaktiterminaalit 7 ovat nyt sekä korotuspalan 15 että liiman 5 peittämiä. Komponentin 16 kontaktinystyjen 17 pinnoilla ja vastaavissa kontaktiaukoissa 8 on liimaa.

Kuvion 13 esittämässä vaiheessa komponentin 6 kontaktiaukkojen 8 kohdalle valmistetaan kontaktireiät 18. Kontaktireiät avataan korotuspalan 15 ja liimakerroksen 5 läpi aina kontaktiterminaalien 7 kontaktipinnoille saakka. Kuvion sovellusmuodossa kontaktireikien 8 avaaminen toteutetaan laser-ablaatiomenetelmällä käyttämällä CO₂-laseria kuten edellä kuvion 4 yhteydessä on kuvattu. Kuvioden 10–16 sovellusmuodossa on merkittävää se, että toisen komponentin 16 kontaktiterminaalien 17 kohdalle ei avata vielä tässä vaiheessa kontaktireikiä.

Kuvion 14 esittämässä vaiheessa komponentin 6 kontaktireikiin 18 valmistetaan välikerros 2, joka on soveltuvaa johdemateriaalia. Välikerroksen 2 johdemateriaali valitaan komponentin 6 kontaktiterminaalien 7 materiaalin perusteella ja valmistetaan soveltuvalla kemiallisella johdemateriaalin kasvatusmenetelmällä. Kuvion esimerkissä komponentin kontaktiterminaalien 7 materiaali on alumiini ja välikerroksen 2 materiaali on pääasiassa sinkkiä sisältävä metallisecos. Välikerroksen kasvattamiseen sovelletaan edellä kuvion 5 yhteydessä esitettyjä periaatteita. Kuvion 5 esimerkistä poiketen kuvion

14 tapauksessa on kuitenkin mahdollista menetellä myös siten, että tässä vaiheessa välikerros 2 kasvatetaan selektiivisen menetelmän avulla ainoastaan kontaktiterminaalien 7 pinnalle eli kontaktireikien 18 pohjalle eikä kontaktireikien 18 reunoille. Tällaisessa sovellusmuodossa kontaktireikien 18 reunoille tuleva välikerroksen 2 osa kasvatetaan myöhemmin komponentin 16 kontaktinystyihin 17 liittyvän välikerroksen kasvattamisen yhteydessä. Selektiivistä kasvatustapaa käyttävässä sovellusmuodossa on se etu, että välikerros 2 ei kasva komponentin 16 kontaktinystyt 17 peittävän liimakerroksen päälle.

Valmistusta jatketaan kuvion 15 esittämässä vaiheessa valmistamalla toisen komponentin 16 kontaktiaukkojen 8 kohdalle kontaktireiät 28. Tämän jälkeen kuvion 16 mukaisesti moduuli altistetaan sopivalle kemialliselle johdemateriaalin kasvatustapamäärälle. Kuvion 15 esimerkissä kasvatustapamäärä on ei-selektiivinen ja johdemateriaalia kasvaa moduulin kaikille vapaille pinnoille ja näin myös komponentin 6 kontaktireikiin 18 ja komponentin 16 kontaktireikiin 28. Valoresistikerros 30 kuitenkin suojaa moduulin pintoja, joten välikerros 2 kasvaa ainoastaan kontaktireikiin 18 ja 28 sekä näiden ympäristöön. Tämän jälkeen valoresistikerros 30 ja sen pinnalle mahdollisesti kasvanut johdemateriaali poistetaan. Tällainen valoresistikerrosta 30 käyttävä sovellusmuoto voi olla hyödyllinen esimerkiksi silloin, kun valoresistikerroksen aukkoihin kasvatetaan ei-selektiivisellä menetelmällä esimerkiksi nikkeliä tai muuta kuparista poikkeavaa metallia. Tällöin johteet 22 ja 24 voidaan valmistaa pelkästään kuparikerroksista koostuviksi.

Toisissa sovellusmuodoissa on myös mahdollista käyttää sopivasti valittua selektiivistä kasvatustapamäärää ja kasvattaa johdemateriaalia ainoastaan komponentin 16 kontaktinystyjen 17 pinnoille vastaavasti kuin edellä kuvion 14 yhteydessä selostettiin. Joka tapauksessa tässä vaiheessa kasvatetaan välikerros 2 ainakin komponentin 16 kontaktinystyjen 17 pinnoille ja kontaktireikien 28 sivuseinämien pinnoille ja lisäksi haluttaessa myös komponentin 6 kontaktiterminaaleihin 7 liittyvän välikerroksen 2 pinnalle ja/tai komponentin 6 kontaktireikien 18 sivuseinämien pinnoille.

Mikäli kuvioden 10-16 esimerkki toteutettaisiin ilman valoresistin 30 käyttöä, kuvion 16 esimerkissä komponentin 16 kontaktinystyjen 17 pinnan materiaali voisi sopivasti olla myös kupari ja kontaktinystyjen 17 pinnalle kasvatettavan välikerroksen 2 materiaali olisi tällöin sopivasti kemiallisella kasvatustapamäärällä valmistettu kupari.

Välikerrosten 2 valmistamisen jälkeen tässä sovellusmuodossa valmistamista voidaan jatkaa esimerkiksi kuvioden 6–9 selostuksen yhteydessä kerrottuun tapaan valmistamalla moduulin pinnalle johdekuvioita ja johdeytimet kontaktireikiin 18 ja 28 sijoittuville kontaktielementeille.

- 5 Toinen vaihtoehto on pinnoittaa moduulin molemmille johtaville pinnoille kuparia valoresistikerroksen 30 poistamisen jälkeen. Tämän jälkeen kuparikerrokset voidaan kuvioda johteiksi 22 ja 24, jolloin saadaan kuvion 17 esittämä rakenne, jossa johteet 22 ja 24 muodostuvat kontaktielementtien ympäristössä ensimmäisestä ja toisesta kuparikerroksesta sekä näiden välissä olevasta välikerroksesta 2, joka on esimerkiksi
- 10 nikkeliä. Muualla johteet 22 ja 24 muodostuvat ensimmäisestä ja toisesta kuparikerroksesta, joiden välillä on analysoitavissa oleva rajapinta. Kuvion 17 rakenteesta valmistusta voidaan haluttaessa jatkaa esimerkiksi jollakin edellisten esimerkkien yhteydessä kuvatulla tavalla.

- Kuviot 18–23 esittävät kolmannen sovellusmuodon mukaisen valmistusmenetelmän,
- 15 joka on muunnelma kuvioden 10–16 esittämästä sovellusmuodosta. Kuvion 23 välivaiheesta valmistusta voidaan jatkaa esimerkiksi kuvioden 6–9 esittämällä tavalla. Kuvioden 1–5 ja 10–16 selostuksen yhteydessä esitetyt tekniset piirteet ja parametrit ovat siis sovellettavissa myös kuvioden 18–23 esittämissä prosessivaiheissa, joten valmistusprosessin kaikkia yksityiskohtia ja niiden etuja ei seuraavassa
- 20 suoritus esimerkissä toisteta turhan toiston välttämiseksi. Sen sijaan seuraavassa tuodaan esille oleelliset eroavaisuuden kuvioden 10–16 ja kuvioden 18–23 esittämien sovellusmuotojen välillä.

- Kuvioden 18–23 sovellusmuodossa valmistus aloitetaan kuvion 10 tapaan johdekalvosta 12, johon tehdään kontaktiaukot 8. Tämän jälkeen johdekalvon 12
- 25 pinnalle, komponenttien 6 ja 26 tuleville kiinnityskohdille kiinnitetään korotuspalat 15. Komponenttien 6 ja 26 korotuspalat 15 voivat olla keskenään identtisiä tai komponenttikohdaisesti valittuja esimerkiksi siten, että komponentin 6 korotuspala 15 on erilaista materiaalia ja/tai eripaksuinen kuin komponentin 26 korotuspala 15.

- Kuvion 18 mukaisesti valmistusta jatketaan levittämällä liimakerrokset 5
- 30 komponenttien liitäntäalueille ja laminoimalla aihioon eristekalvot 10, 11 ja johdekalvo

14 aivan kuin kuvion 11 yhteydessä on esitetty. Kuvio 19 esittää moduulia näiden vaiheiden jälkeen.

Kuvion 19 esittämässä vaiheessa komponentin 6 kontaktiaukkojen 8 kohdalle valmistetaan kontaktireiät 18 kuvion 13 yhteydessä selostettuun tapaan. Komponentin 26 kontaktiterminaalien 27 kohdalle ei avata vielä tässä vaiheessa kontaktireikiä.

Kuvion 21 esittämä vaihe vastaa täysin kuvion 14 yhteydessä esitettyä menetelmävaihetta. Tässä sovellusmuodossa komponentin 6 kontaktireikiin 18 valmistetaan välikerros 2, joka on kaksikerroksinen. Kuvion esimerkissä komponentin kontaktiterminaalien 7 materiaali on alumiini. Esimerkin kaksikerroksinen välikerros 2 käsittää ensin kasvatetun sinkkiä sisältävän kerroksen ja tämän jälkeen kasvatetun nikkeli-alumiini -kerroksen. Nikkeli-alumiini -kerros kasvatetaan kemiallisella menetelmällä ja sitä käytetään sinkkiä sisältävän kerroksen tiivistämiseen.

Valmistusta jatketaan kuvion 22 esittämässä vaiheessa valmistamalla toisen komponentin 26 kontaktiaukkojen 8 kohdalle kontaktireiät 28. Tämän jälkeen kuvion 23 mukaisesti moduuli altistetaan sopivalle kemialliselle johdemateriaalin kasvatusmenetelmälle. Tämä vaihe vastaa kuvion 16 yhteydessä selostettua menetelmävaihetta. Kuvion 23 esimerkissä komponentin 26 kontaktiterminaalien 27 pinnan materiaali on kupari ja kontaktiterminaalien 27 pinnalle kasvatettavan välikerroksen 2 materiaali on myös kupari.

Kuviossa 24 on puolestaan esitetty kuvioiden 18–23 sovellusmuodosta sellainen modifikaatio, jossa kuvion 22 esittämän vaiheen jälkeen komponentin 26 kontaktiterminaalien 27 päälle kasvatetaan ensimmäinen välikerros selektiivisellä kasvatusmenetelmällä ja tämän jälkeen välikerroksen 2 kasvattamista jatketaan ei-selektiivisellä menetelmällä. Kuvion 24 esimerkissä komponentin 26 kontaktiterminaalien 27 pinnan materiaali on kulta ja kontaktiterminaalien 27 pinnalle kasvatettavan välikerroksen 2 materiaali on nikkeli.

Välikerrosten 2 valmistamisen jälkeen näissä kuvioiden 18–24 sovellusmuodoissa valmistamista voidaan jatkaa esimerkiksi kuvioiden 6–9 selostuksen yhteydessä kerrottuun tapaan valmistamalla moduulin pinnalle johdekuvioita ja johdeytimet kontaktireikiin 18 ja 28 sijoittuville kontaktielementeille.

Kuvio 25 esittää tarkemmin kontaktireiän ja vastaavasti myös tähän aukkoon valmistettavan kontaktielementin muotoa. Kuvion 25 esimerkki esittää yhden mahdollisen muodon, joka voidaan saavuttaa edellä esitettyjä sovellusmuotoja käyttäessä. Muotoon voidaan vaikuttaa johdekalvoon 12 tehtävien kontaktiaukkojen 8 muodon, johdekalvon 12 ja komponentin välissä olevan eristeen ominaisuuksien ja CO₂-laserin käyttöparametrien avulla. Kuvion 25 kontaktireikä on pyörähdys-symmetrinen ja kuvion esittämä poikkileikkaus on otettu kontaktireiän keskiakselin kautta eli esittää leveintä mahdollista poikkileikkausta. Kuviossa 25 kontaktireiän kokoa ja muotoa on määritelty seuraavien parametrien avulla:

- suurin leveys W_{MAX} , josta voidaan laskea kontaktielementin suurin poikkipinta-ala A_{MAX} ,
- kontaktielementin ja komponentin 6 kontaktipinnan 7 välisen kontaktin leveys W_{CONT} , josta voidaan laskea kontaktielementin ja komponentin kontaktipinnan välinen kontaktipinta-ala A_{CONT1} , ja
- kontaktiaukon leveys W_{HOLE} , josta voidaan laskea kontaktielementin ja johdekuviokerroksen johteen välinen kontaktipinta-ala A_{CONT2} .

Kuviossa on kuvattu myös komponentin kontaktipinnan 7 leveys W_{PAD} , josta voidaan laskea kontaktipinnan pinta-ala A_{PAD} , kun tiedetään kontaktipinnan muoto. Kontaktipinta 7 voi olla esimerkiksi neliön muotoinen ja W_{PAD} :n edustaessa sivun leveyttä kontaktipinnan pinta-alaksi saadaan: $A_{PAD} = W_{PAD} \times W_{PAD}$. Pinta-alat on toki mahdollista määrittää myös pinta-alamittauksen avulla, mikä voikin olla käytännöllisempää ainakin silloin, kun määritettävä pinta-ala on epäsäännöllisen muotoinen.

Kuviossa kontaktipintaa 7 ympäröi komponentin 6 pinnalle valmistettu passivointikerros 9. Tällöin kontaktipinnan pinta-alalla A_{PAD} tarkoitetaan nimenomaan kontaktin muodostamiselle vapaata pinta-alaa eli sen pinnan pinta-ala, joka on paljastettuna passivointikerrokseen 9 tehdyssä avauksessa. Lisäksi kuviossa on esitetty johdekalvon 12 ja kontaktipinnan 7 välimatka H , joka vastaa kontaktireiän syvyyttä ja näin ollen kontaktireikään valmistettavan kontaktielementin korkeutta. Koska kontaktireikä täytetään kokonaan johdemateriaalilla, myös kontaktireiän muut mitat

vastaavat kontaktielementin mittoja ja parametreilla W_{MAX} ja W_{HOLE} voidaan viitata myös kontaktielementin vastaaviin mittoihin.

Seuraavassa esitetään edellä kuvattujen sovellusmuotojen yhteydessä tyypillisiä parametreja:

5 $H = 1\text{--}50\text{ }\mu\text{m}$, tavallisesti $5\text{--}30\text{ }\mu\text{m}$;

$W_{PAD} = 20\text{--}1000\text{ }\mu\text{m}$, tavallisemmin $50\text{--}200\text{ }\mu\text{m}$ ja tavallisimmin noin $100\text{ }\mu\text{m}$; ja

$W_{HOLE} = 5\text{--}500\text{ }\mu\text{m}$, tavallisemmin $20\text{--}75\text{ }\mu\text{m}$ ja tavallisimmin noin $30\text{--}50\text{ }\mu\text{m}$.

Lisäksi yleensä $W_{HOLE} \geq H$, mikä edistää kontaktireiän luotettavaa täyttymistä. Kontaktireikä 18 pyritään valmistamaan siten, että reiän sivuseinämät olisivat
 10 pystysuorat. Toisin sanoen tavoitteena on kontaktireikä, jonka leveys ja muoto säilyy vakiona koko johdekalvon 12 ja kontaktipinnan 7 välisen välimatkan H eli kontaktireikä olisi koko tämän matkan kontaktiaukon 8 muotoinen. Myös kontaktipintaa 7 kohti heikosti kapeneva muoto on hyvä. Käytännössä edellä kuvattua laserprosessia käytettäessä kontaktireiästä voi kuitenkin tulla esimerkiksi kontaktipintaa 7 kohti
 15 levenevä tai ensin levenevä ja sitten kapeneva siten, että kontaktireikä on leveimmillään jossakin johdekalvon 12 ja kontaktipinnan 7 välillä. Kuvion 25 esittää tällaisen kontaktireiän. Tällainen epäoptimaalinen muoto ei ole ongelmallinen, mikäli vain levenemä ei ole liian suuri ja reiän täyttö onnistuu hyvin.

Edellä viitatuissa leveyksien mitta-arvoista komponentin kontaktipinnan 7 leveys W_{PAD}
 20 määräytyy komponentin valinnan kautta. W_{PAD} voidaan tarvittaessa mitata erikseen jokaista sellaista suoraa pitkin, joka kulkee kontaktipinnan 7 keskipisteen kautta. Tätä määritelmää voidaan tarvita edellä viitattuja mitta-arvoja ja niiden suhteita tarkasteltaessa, mikäli kontaktipinnan 7 tai kontaktiaukon 8 muoto on epäsäännöllinen. Tavallisimmassa tapauksessa kontaktipinta on kuitenkin neliömäinen, jolloin
 25 kontaktipinnan 7 leveytenä W_{PAD} voidaan yleensä käyttää neliön sivun leveyttä.

Kontaktiaukon 8 leveys W_{HOLE} on parametri, joka valitaan valmistusprosessia suunniteltaessa. Yksi kontaktiaukon 8 leveyttä valittaessa huomioon otettava parametri on käytettävän komponentin kontaktipinnan 7 leveys. Kontaktiaukon 8 leveys valitaan siten, että kontaktiaukon kautta valmistettava kontaktisreikä osuu komponentin päässä
 30 koko poikkipinnaltaan komponentin kontaktialueeseen 7 eikä kontaktialueen ohi

esimerkiksi passivointikerroksen pintaan. Mikäli kontaktiaukko on muodoltaan pyöreä, kontaktiaukon leveys W_{HOLE} on ympyrän keskpisteen kautta mitattu halkaisija. Mikäli taas kontaktiaukko on muodoltaan epäsäännöllinen, W_{HOLE} voidaan tarvittaessa mitata erikseen jokaista sellaista suoraa pitkin, joka kulkee kontaktiaukon 8 keskpisteen
 5 kautta. Epäsäännöllisen muodon tapauksessa verrattaessa kontaktiaukon leveyttä W_{HOLE} kontaktipinnan leveyteen W_{PAD} , vertailu voidaan tehdä aina erikseen kullekin parille samansuuntaisten suorien kautta mitattuja leveyksiä. Leveyksiä W_{HOLE} ja W_{PAD} voidaan tarvittaessa verrata vastaavalla tavalla myös muihin esitettyihin parametreihin.

Edellä esitettyjä parametrien suhteita voidaan soveltaan myös kontaktinystyjen 17 yhteydessä, jolloin kontaktialueen pinta-ala ja leveys korvataan kontaktinystyn pinta-
 10 alalla ja leveydellä ja välimatka H mitataan kontaktinystyn pintaan.

Kontaktireiän muotoon voidaan vaikuttaa laserin parametrien avulla, jotka valitaan reiän parametrien ja poistettavan eristeen ominaisuuksia mukaan. Valmistustulokseen vaikuttaa tietysti myös käytössä oleva laserlaite. Valittujen parametrien sopivuus
 15 prosessiin tarkastetaan koevalmistuserän avulla ja tarvittaessa parametreja muutetaan siten, että haluttu tulos saavutetaan.

Yleensä valmistusmenetelmässä on järkevää pyrkiä sellaiseen kontaktireiän muotoon, jossa

$W_{CONT} = 0,5-1,5$ kertaa W_{HOLE} , mielellään $0,7-1,2$ kertaa W_{HOLE} ja mieluiten $0,8-1,0$
 20 kertaa W_{HOLE} , kuitenkin siten, että $W_{CONT} < W_{PAD}$; ja

$W_{MAX} =$ korkeintaan $100\ \mu\text{m}$, mielellään korkeintaan $30\ \mu\text{m}$ ja mieluiten korkeintaan $10\ \mu\text{m}$ suurempi kuin se parametreista W_{HOLE} ja W_{CONT} , joka on suurempi. Suhteellisesti esitettynä tavoitteena olisi, että $W_{MAX} =$ korkeintaan $40\ \%$, mielellään korkeintaan $20\ \%$
 25 ja mieluiten korkeintaan $10\ \%$ suurempi kuin se parametreista W_{HOLE} ja W_{CONT} , joka on suurempi.

Optimaalisimmassa kontaktielementin muodossa W_{MAX} on oleellisesti yhtä suuri kuin W_{HOLE} ja lisäksi W_{CONT} on $0-20\ \%$ pienempi kuin W_{MAX} .

Tyypillisimmissä sovellusmuodoissa kontaktipinta 7 on muodoltaan neliskulmainen ja kontaktiaukko 8 ympyrän muotoinen. Tällöin $A_{CONT\ 1}$ on tyypillisesti $10-75\ \%$ pinta-

alasta A_{PAD} , $A_{CONT\ 1}$ ja $A_{CONT\ 2}$ tyypillisesti keskenään suunnilleen yhtä suuria esimerkiksi tarkkuudella $\pm 20\ %$.

Kuvio 26 esittää esimerkkejä muista mahdollisista kontaktireikien 18 muodoista. Kuvion 27 taas esittää esimerkkejä tällaisiin kontaktireikiin valmistetuista välikerroksista 2. Kuvioden 26 ja 27 esimerkeissä liitettävä komponentti on nystytön. Kuten kuvioista 26 ja 27 voi nähdä, välikerrokset 2 eivät ulotu ollenkaan komponentin passivointikerroksen 9 päälle vaan ovat kontaktissa ainoastaan komponentin kontaktipinnan 7 kanssa. Tämän piirteen avulla voidaan nähdä valmiistakin elektroniikkamoduulista se, onko komponentti upotettu elektroniikkamoduuliin nystyllisenä vai nystyttömänä. Nystytysprosesseissa komponentin kontaktipinnalle 7 kasvatettavat nystyt täyttävät aina koko kontaktipinnan 7 ja leviävät aina myös hieman passivointikerroksen 9 päälle. Mikäli taas edellä kuvatuissa suoritusesimerkeissä käytetään nystytöntä komponenttia, välikerros 2 ja kontaktielementti kasvavat ainoastaan kontaktireikään 18, jolloin valmiissa elektroniikkamoduulissa välikerros 2 ei ulotu komponentin passivointikerroksen 9 päälle ja osa komponentin kontaktipinnasta 7 jää vapaaksi välikerroksesta 2 (kontaktipinnan 7 reunat) aina kun kontaktireiän 18 kohdistus ja valmistus on onnistunut. Myös mahdollisessa kontaktireiän 18 kohdistusvirhetilanteessa, jossa kontaktiaukko 8 ei täysin sijaitse kontaktipinnan 7 kohdalla, ainakin osa kontaktipinnan 7 reuna-alueista ja reuna-aluetta ympäröivästä passivointikerroksesta on vapaa välikerroksesta 2.

Mikäli nystytön komponentti on valmistettu kuparijohteita käyttävällä puolijohdeprosessilla, kontaktialue 7 on kuparia. Tällöin välikerros voidaan valmistaa suoraan kemiallisesti kasvatetusta kuparista, joka muodostaa johdepinnoitteen myös kontaktireiän 18 sivuseinämille. Tämän jälkeen kontaktireiät 18 voidaan täyttää ja johdekerroksen paksuutta kasvattaa sähkökemiallisella kuparinkasvatusmenetelmällä.

Tämän hakemuksen kirjoitushetkellä yleisin puolijohdeprosesseissa käytettävä johdemateriaali on kuitenkin alumiini. Tällöin myös nystyttömien komponenttien yleisin kontaktialueen 7 materiaali on alumiini ja on edullista käyttää eri materiaaleista valmistettuja yksi tai useampikerroksisia välikerroksia alumiinisen kontaktialueen ja elektroniikkamoduulin kuparisten johteiden välissä. Seuraavassa mainitaan muutamia mahdollisia välikerrosten rakenteita:

Välikerrosrakenne 1

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä, joka ei kasva tai kasvaa heikosti polymeeripinnalle. Nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvavamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

10 Välikerrosrakenne 2

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

Välikerrosrakenne 3

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkaattiprosessilla valmistettu sinkkiä sisältävä kerros ei kasva kontaktireiän 18 sivuseinämien polymeeripinnoille. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeli-alumiinia, joka ei kasva polymeeripinnalle. Nikkeli-alumiinin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia. Kemiallisella kasvatusmenetelmällä kasvatettu kupari saadaan kasvamaan luotettavasti myös polymeerin päälle, jolloin kontaktireikien 18 sivuseinämät saadaan johtaviksi myöhempää sähkökemiallista kasvatusta varten.

Välikerrosrakenne 4

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeli-alumiinia. Nikkeli-alumiinin pinnalle kasvatetaan kemiallisella menetelmällä

kerros nikkeliä ja nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia.

Välikerrosrakenne 5

- 5 Alumiinisen kontaktialueen 7 pinnalle kasvatetaan ensin sinkkiä sisältävä kerros. Sinkkiä sisältävän kerroksen pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä.

Välikerrosrakenne 6

- 10 Alumiinisen kontaktialueen 7 pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä, joka kasvatettu nikkelikerros yksin muodostaa välikerroksen 2.

Välikerrosrakenne 7

Alumiinisen kontaktialueen 7 pinnalle kasvatetaan kemiallisella menetelmällä kerros nikkeliä ja nikkelin pinnalle kasvatetaan kemiallisella menetelmällä kerros kuparia.

- 15 Edellä esitetyissä välikerrosrakenteiden esimerkeissä sinkkiä sisältävä kerros sisältää esimerkiksi noin 80 % sinkkiä, noin 16 % kuparia, noin 2-3 % nikkeliä ja noin 2-3 % rautaa. Tämä on ainoastaan yksi mahdollinen esimerkki käyttökohteeseen soveltuvista seossuhteista, joten seossuhteita voidaan toki vaihdella sovelluskohteiden mukaan.
- 20 Edellä esitetyissä välikerrosrakenteiden esimerkeissä sinkkiä sisältävän kerroksen paksuus on alle 1 μm , tavallisesti yksikertaisena kerroksena noin 0,1 μm ja useampana kerroksena esimerkiksi noin 0,3–0,4 μm . Ohuimmillaan sinkkiä sisältävä kerros voi olla noin 5–10 nm valmistamisen jälkeen. Kasvatettaessa nikkeliä tai nikkeli-alumiinia sinkkiä sisältävän kerroksen päälle ainakin osa sinkkiatomeista liukenee ja korvautuu nikkeliatomeilla. Lopullisessa piirimoduulissa voi olla mahdollista, että sinkkiä sisältävä kerros on havaittavissa lähinnä sinkin konsentraatioprofilina alumiinin ja
- 25 seuraavan kerroksen materiaalin rajapinnassa. Sinkkiä sisältävä kerros ei siis välttämättä ole tarkkarajaisena lopullisessa tuotteessa, koska sinkki voi diffusoitua viereisiin materiaalikerrokseen erityisesti korkeampia lämpötiloja käytävissä valmistusprosessin vaiheissa.

Edullisessa sovellusmuodossa sinkkiä sisältävä kerros kasvatetaan kaksinkertaisella sinkkaattiprosessilla. Yksinkertaisella sinkkaattiprosessilla kasvatettu sinkki muodostaa epäyhtenäisen ja epätasaisen pinnan alumiinin päälle. Tällaisen pinnan päälle kasvatetun nikkeli-kerroksen adheesio on heikompi ja se soveltuu huonommin käytettäväksi pienillä mikrovia-avauksilla. Kasvatetun sinkkipinnan laatua saadaan merkittävästi parannettua käyttämällä kaksinkertaista sinkkaattiprosessia. Tyypillisesti tällaisessa prosessissa ensimmäisen sinkattikäsittelyn jälkeen sinkkiä sisältävä kerros stripataan tyypihapolla (HNO_3), jonka jälkeen pinnoitetaan toinen sinkkiä sisältävä kerros. Kaksinkertaisella sinkkaattiprosessilla saadaan aikaan tiivis ja yhtenäinen sinkkiä sisältävä kerros komponentin alumiinisen liitosalueen pinnalle.

Nikkeli-alumiini kerroksen paksuus voi puolestaan olla esimerkiksi 0,2–2 μm . Nikkelikerroksen paksuus taas voi olla esimerkiksi 0,5–20 μm , tyypillisesti 2–10 μm . Myös kerrospaksuudet ovat ainoastaan esimerkkejä mahdollisista kerrospaksuuksista ja muita kerrospaksuuksia voidaan myös hyvin käyttää.

Sovellusmuodoissa sähkökemiallisesti kasvatettava kuparikerros voi olla paksuudeltaan esimerkiksi välillä 5–30 μm , tyypillisesti välillä 10–20 μm . Kemiallisella kasvatusmenetelmällä kasvatettava kuparikerros taas yleensä valmistetaan selvästi ohuemmaksi ja sen paksuus on sovellusmuodoissa esimerkiksi välillä 0,1–2 μm , tyypillisesti välillä 200–800 nm.

Edellä kuvatuissa valmistusmenetelmissä voidaan toki käyttää myös muita kuin edellä mainittuja välikerrosrakenteita ja materiaaleja, esimerkiksi tinaa. Alumiinin pinnalle on myös mahdollista kasvattaa suoraan nikkeli-kerros poistamalla alumiinin pinnalla oleva oksidikerros esimerkiksi alkaalisella etsillä ja huuhtomalla pinta tämän jälkeen esimerkiksi propan-2-olissa ja välittömästi tämän jälkeen pinnoittamalla propan-2-olin kiehumispistettä lämpimämmässä kemiallisessa nikkelikylvyssä. Lisäksi sinkkiä sisältävän kerroksen pinnalle olisi mahdollista pinnoittaa myös esimerkiksi kromia ja nikkelin pinnalle kultaa.

Kuvio 28 esittää vielä yhden mahdollisen kontaktirakenteen, jossa voidaan käyttää komponenttia, jonka kontaktialue on ennalta varustettu alusmetallurgisilla kerroksilla, mutta varsinaista nystyä ei ole valmistettu. Kuvio 29 esittää yhden mahdollisen vastaavan kontaktirakenteen toteutettuna nystyttömän komponentin kanssa.

Kuvio 28 esittää komponentin pinnalla olevan passivointikerroksen 9, jossa on avaus komponentin kontaktialueen 7 kohdalla. Passivointikerroksen 9 pinnalla on polymeerikerros 25. Polymeerikerros 25 voi koostua yhdestä tai useammasta polymeerikerroksesta. Polymeerikerroksen 25 materiaali voi sisältää esimerkiksi kuvion 1
 5 yhteydessä kuvattua eristerakennetta 13, kuvion 2 yhteydessä kuvattua liimaa 5 ja/tai kuvion 11 yhteydessä kuvattua korotuspallaa. Komponentin kontaktialueen 7 pinnalle on valmistettu alusmetallurgia, joka tässä esimerkissä käsittää kaksi kerrosta. Ensimmäinen alusmetallurgikerros 26 on sputteroimalla valmistettu kerros esimerkiksi kromia (Cr) tai titaani-wolframia (TiW). Toinen alusmetallurgikerros 27 on sputteroimalla
 10 valmistettu kerros esimerkiksi nikkeliä (Ni), kuparia (Cu) tai kultaa (Au). Varsinainen nysty käsittäisi vielä esimerkiksi kemiallisesti tai sähkökemiallisesti kasvatetun kulta- tai kuparikerroksen toisen alusmetallurgikerroksen 27 pinnalla.

Kuvion 28 esimerkissä komponentti on kiinnitetty polymeerikerroksen 25 välityksellä johdekalvoon 12, johon on tehty edellä esitetyissä menetelmissä kuvattuun tapaan
 15 kontaktiaukot 8. Kontaktiaukkojen 8 kautta on valmistettu kontaktireiät 18 tai 28, joihin kontaktielementti on valmistettu kontaktiin toisen alusmetallurgikerroksen 27 kanssa. Kontaktielementti on valmistettu siten, että ensin on kasvatettu yhtä tai useampaa kemiallista kasvatusmenetelmää käyttäen välikerros 2 vastaavaan tapaan kuin edellä esitetyissä menetelmissä on kuvattu. Kuvion 28 esimerkissä välikerros 2 on
 20 kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Tämän välikerroksen päälle on kasvatettu kerros 32 kuparia sähkökemiallisella kasvatusmenetelmällä. Sähkökemiallisesti kasvatettu kupari muodostaa myös kontaktielementin johdeytimen 29. Kuviosta 28 nähdään myös se, että johdekalvo 12, välikerros 2 ja kuparikerros 32 muodostavat yhdessä johteen 22 materiaalin. Esimerkissä johdekalvo 12, välikerros 2 ja kuparikerros
 25 32 ovat kaikki kuparia, mutta kerrokset ja niiden väliset rajapinnat on kuitenkin mahdollista havaita myös valmista rakennetta analysoimalla.

Kuvio 29 esittää kuvion 28 tapaan komponentin pinnalla olevan passivointikerroksen 9, jossa on avaus komponentin kontaktialueen 7 kohdalla. Passivointikerroksen 9 pinnalla on polymeerikerros 25, joka vastaan kuvion 28 yhteydessä esitettyä. Kuvion 29
 30 esimerkissä komponentin kontaktialueen 7 pinta on ollut päällysteetön komponentti silloin, kun se on tuotu piirimoduulin valmistusprosessiin. Tällaisessa komponentissa

kontaktialueen 7 ulkopinta eli kontaktipinta on siis tyypillisesti muodostettu jo puolijohdetehtaalla. Kuvion 29 esimerkissä kontaktialueen 7 materiaali on alumiini.

Kuvion 29 esimerkissä komponentti on kiinnitetty polymeerikerroksen 25 välityksellä johdekalvoon 12, johon on tehty edellä esitetyissä menetelmissä kuvattuun tapaan kontaktiaukot 8. Kontaktiaukkojen 8 kautta on valmistettu kontaktireiät 18 tai 28, joihin kontaktielementti on valmistettu kontaktiin kontaktialueen 7 kanssa. Kontaktielementti on valmistettu siten, että ensin on kasvatettu yhtä tai useampaa kemiallista kasvatusmenetelmää käyttäen välikerros 2 vastaavaan tapaan kuin edellä esitetyissä menetelmissä on kuvattu. Kuvion 29 esimerkissä välikerros 2 on valmistettu useammassa osassa ja käsittää useita kerroksia. Kuviossa 28 välikerros on lisäksi selityksen helpottamista varten jaettu kolmeen osaan, pohjaosaan 36, seinämäosaan 37 ja johdeosaan 38. Pohjaosa 36 on se osa, joka kasvaa kontaktiterminaalin 7, 17 pinnalle kontaktireiän 18, 28 pohjalle, seinämäosa 37 on se osa, joka kasvaa kontaktireiän 18, 28 sivuseinämien pinnoille ja johdeosa 38 on se osa, joka kasvaa osaksi valmistettavaa johdetta 22.

Kuvion 29 välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Kuvion 29 esimerkissä johdekalvo 12 on kuparia, joten sinkkaattiprosessia käytettäessä ensimmäinen välikerros 33 kasvaa ainoastaan välikerroksen 2 pohjaosaan 36. Tästä valmistusta voidaan jatkaa esimerkiksi valmistamalla toinen välikerros 34 kemiallisella nikkelin kasvatusmenetelmällä. Nikkeli kasvaa sekä välikerroksen pohjaosaan 36 että johdeosaan 38 ja joillakin kasvatusmenetelmillä myös polymeerin 25 pinnalle seinämäosaan 37. Toisen välikerroksen 34 päälle valmistetaan kolmas välikerros 35 kuparista kemiallisella kasvatusmenetelmällä, jolloin kupari kasvaa pohjaosaan 36, seinämäosaan 37 ja johdeosaan 38. Kolmannen välikerroksen päälle kasvatetaan kerros 32 kuparia sähkökemiallisella kasvatusmenetelmällä, joka muodostaa myös kontaktielementin johdeytimen 29.

Kuvion 29 osalta on huomattava, että kerrokset 33 ja 34 eivät välttämättä ole lopullisessa piirimoduulissa kuvion esittämään tapaan tarkkarajaisia vaan kerrokset voivat ilmetä lomittuneina tai sekoittuneina, esimerkiksi diffuusion vaikutuksesta. Esimerkiksi sinkkiä sisältävän ensimmäisen välikerroksen 33 tapauksessa sinkki voi

sijaita konsentraatioprofilina alumiinin ja nikkelin 34 välisessä rajapinnassa ja osittain alumiinin 7 ja nikkelikerroksen 34 sisällä.

Kuvion 29 kontaktirakenteessa voidaan käyttää myös muita materiaalikombinaatioita. Esimerkiksi sopivasti valittuja välikerrosrakenteita edellä kuvatuista välikerrosrakenteista 1–7 ja näiden muunnelmia voidaan käyttää kuvion 29 kuvaaman kontaktirakenteen ja myös kuvioden 30–33 kuvaamien kontaktirakenteiden muodostamiseen. Lisäksi kuvion 29 kontaktirakenne on mahdollista valmistaa myös kuvion 28 esittämien materiaalien avulla siten, että ensimmäinen välikerros 33 ja toinen välikerros 34 valmistetaan sputteroimalla. Tällöin sputteroidut välikerrokset 33 ja 34 kasvavat sekä pohjaosaan 36 että johdeosaan 38 mutta eivät oleellisessa määrin seinämäosaan 37, mikäli kontaktireikä 18, 28 ei ole kontaktiaukkoa 8 kohti levenevä. Yksi mahdollisuus on käyttää sinkkiä sisältävää ensimmäisen välikerrosta 33 ja tämän pinnalla joko suoraan nikkelistä kemiallisella kasvatusmenetelmällä valmistettua kolmatta välikerrosta 35 tai rakennetta, jossa kerrosten 33 ja 35 välissä käytetään nikkeli-alumiinista valmistettua toista välikerrosta 34. Tällaisessa sovellusmuodossa ei tarvita lainkaan kemiallista kuparinkasvatusta, sillä nikkeli muodostaa pystysuuntaisen kontaktin kontaktireiän sivuseiniä pitkin.

Kuvio 30 esittää vielä yhden kontaktielementtirakenteen. Kuvion 30 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on nikkeli-alumiinia ja kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Kuvion 30 rakenteessa siis kontaktireikä täytetään nikkelillä eli kontaktielementin johdeydin 29 on nikkeliä. Muutoin kuvion 30 rakenteen osalta pätevät kuvioden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

Kuvio 31 esittää vielä yhden kontaktielementtirakenteen. Kuvion 31 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33 ja toisen välikerroksen 34. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai vaihtoehtoisesti selektiivisellä kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Vaihtoehtoisesti kuvion 31 rakenne voidaan valmistaa myös siten, että ensimmäinen ja toinen välikerros 33 ja 34

korvataan yhdellä kerroksella kemiallisesti kasvatettua nikkeliä. Johdeydin 29 on tyypillisesti kuparia ja johde 22 käsittää ensimmäisen ja toisen kuparikerroksen 12 ja 32. Muutoin kuvion 31 rakenteen osalta pätevät kuvioiden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

- 5 Kuvio 32 esittää vielä yhden kontaktielementtirakenteen. Kuvion 32 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Esimerkin menetelmässä kasvatusmenetelmä on selektiivinen siten, että nikkeli kasvaa ainoastaan johtavan materiaalin päälle. Kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Vaihtoehtoisesti kuvion 32 rakenne voidaan valmistaa myös siten, että ensimmäinen välikerros 33 jätetään pois. Johdeydin 29 on tyypillisesti kuparia. Muutoin kuvion 32 rakenteen osalta pätevät kuvioiden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

- Kuvio 33 esittää vielä yhden kontaktielementtirakenteen. Kuvion 33 rakenteen valmistamiseen voidaan käyttää esimerkiksi kuvioiden 10–17 yhteydessä kuvattua menetelmää, jossa käytettiin valoresistikerrosta 30. Kuvion 33 rakenteessa välikerros 2 käsittää ensimmäisen välikerroksen 33, toisen välikerroksen 34 ja kolmannen välikerroksen 35. Ensimmäinen välikerros 33 voidaan valmistaa esimerkiksi kasvattamalla kemiallisella kasvatusmenetelmällä sinkkiä sisältävä kerros. Toinen välikerros 34 on kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä. Esimerkin menetelmässä kasvatusmenetelmä on selektiivinen siten, että nikkeli kasvaa ainoastaan johtavan materiaalin päälle. Kolmas välikerros 35 on kemiallisella kasvatusmenetelmällä kasvatettua kuparia. Vaihtoehtoisesti kuvion 33 rakenne voidaan valmistaa myös siten, että ensimmäinen välikerros 33 jätetään pois. Johdeydin 29 on tyypillisesti kuparia. Muutoin kuvion 33 rakenteen osalta pätevät kuvioiden 28 ja 29 yhteydessä esitetyt tekniset piirteet.

- Sovellusmuodoissa on siis tuotu esiin menetelmä piirimoduulin valmistamiseksi, jossa menetelmässä

– otetaan johdekalvo 12,

- otetaan komponentti 6, joka käsittää kontaktialueita 7, joiden materiaali sisältää ensimmäistä metallia,
- kiinnitetään komponentti 6 johdekalvoon 12 polymeerikerroksen 25 välityksellä,
- valmistetaan johdekalvoon 12 kiinnitetyn komponentin 6 ympärille eristekerros 1,
- 5 – valmistetaan polymeerikerrokseen 25 kontaktialueiden 7 kohdille kontaktireiät 18, 28 siten, että kunkin kontaktireiän 18, 28 ja vastaavan kontaktialueen 7 välinen kontaktipinta-ala A_{CONT1} on pienempi kuin kontaktialueen 7 pinta-ala A_{PAD} , ja
- kasvatetaan ainakin kontaktirei'issä 18, 28 olevien kontaktialueiden 7 pinnalle välikerros 2, joka sisältää ainakin kolmatta metallia,
- 10 – kasvatetaan kerros 32 toista metallia, joka kerros 32 on kontaktissa välikerroksen 2 pinnan kanssa ja ulottuu pitkin valmistettavia johteita 22, ja
- muodostetaan johteet 22 kuvioimalla johdekalvo 12, ja mikäli tarpeen myös johdekalvon 12 pinnalla oleva välikerros 2 ja/tai toista metallia oleva kerros 32.

15 Tyypillisessä sovellusmuodossa kontaktiaukot 8 valmistetaan johdekalvoon 12 ennen komponentin 6 kiinnittämistä, jolloin komponentti 6 siis kiinnitetään kontaktiaukoilla varustettuun 8 johdekalvoon 12. Tavallisimmassa tällaisessa sovellusmuodossa kontaktiaukot eivät ulotu kontaktialueiden 7 pinnoille saakka, joten komponentin 6 kiinnittämisen jälkeen vielä avataan kontaktireiät 18, 28 kontaktiaukkojen 8 kautta.

20 Yhdessä sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on sinkki. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää sinkin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Toisessa sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

25 Kolmannessa sovellusmuodossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Tavallisimmassa sovellusmuodossa kontaktialueiden 7 materiaali on pääasiallisesti alumiinia ja johteiden materiaali on kuparia ja näiden välillä on jokin edellä esitetyistä välikerrosrakenteista 1–7.

5 Välikerrosrakenteen valmistamisessa käytetään tyypillisesti ainakin yhtä kemiallista kasvatusmenetelmää.

Sovellusmuodot kuvaavat piirimoduulin, joka käsittää

- eristekerroksen 1,
- eristekerroksen 1 sisällä ainakin yhden komponentin 6, joka käsittää kontaktialueita 7, joiden materiaali sisältää ensimmäistä metallia,
- 10 – eristekerroksen 1 pinnalla johteita 22, jotka käsittävät ainakin ensimmäisen kerroksen 12 ja toisen kerroksen 32 siten, että ainakin toinen kerros 32 sisältää toista metallia, ja
- kontaktielementtejä kontaktialueiden 7 ja johteiden 22 välillä sähköisten kontaktien muodostamista varten, jotka kontaktielementit käsittävät kontaktialueen 7
- 15 – materiaalin pinnalla välikerroksen 2, joka sisältää kolmatta metallia,
- jossa ensimmäinen, toinen ja kolmas metalli ovat eri metalleja, ja
- välikerroksen 2 ja kontaktialueen 7 välinen kontaktipinta-ala $A_{CONT\ 1}$ on pienempi kuin kontaktialueen 7 pinta-ala A_{PAD} .

20 Yhdessä sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on sinkki. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää sinkin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Toisessa sovellusmuodossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

25 Kolmannessa sovellusmuodossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli. Tällaisessa sovellusmuodossa välikerros 2 voi toki sisältää nikkelin lisäksi myös muita metalleja tai metalliseoksia, kuten edellä on käynyt ilmi.

Tavallisimmassa sovellusmuodossa kontaktialueiden 7 materiaali on pääasiallisesti alumiinia ja johteiden materiaali on kuparia ja näiden välillä on jokin edellä esitetyistä välikerrosrakenteista 1–7.

5 Tyypillisessä sovellusmuodossa kontaktielementit käsittävät sähkökemiallisella kasvatuserämenetelmällä valmistetun kupariytimen 29, joka sivuseinämien ja komponentin 6 suunnassa rajautuu välikerrokseen 2 ja johteen 22 suunnassa yhdistyy jatkuvasti eli ilman rajapintaa johteen 22 toisen kerroksen 32 materiaaliin. Toisin sanoen kontaktielementin kupariydin 29 ja johteen 22 toisen kerroksen 32 materiaali on valmistettu samassa prosessissa, jolloin osat liittyvät kiinteästi yhteen eikä niiden välillä 10 ole rajapintaa. Johteen ensimmäisen kerroksen 12 ja toisen kerroksen 32 välillä taas on tyypillisesti rajapinta tai vastaava siirrosalue, joka voidaan havaita esimerkiksi metallin kiderakennetta tai epäpuhtauskonsentraatiota analysoimalla.

Yhdessä sovellusmuodossa kontaktielementin ja komponentin kontaktialueen 7 välisen kontaktipinnan leveys W_{CONT} on 0–20 % pienempi kuin kontaktielementin suurin leveys 15 W_{MAX} samassa suunnassa.

Kontaktielementit täyttävät tavallisesti kokonaan kontaktireiät 18, 28 eli kontaktielementit eivät ole onttoja vaan ovat kokonaan johdemateriaalia.

Tavallisesti sovellusmuodoissa pyritään siihen, että kontaktielementin korkeus H on pienempi tai yhtä suuri kuin kontaktielementin suurin leveys W_{MAX} .

20 Piirimoduulilla on myös sovellusmuotoja, joissa eristekerros 1 sisältää ainakin yhden kerroksen kuitumateriaalia 19, jossa kuitumateriaalissa 19 on aukko komponenttia 6 varten, sekä yhtenäisen polymeerikerroksen, joka on kiinnittynyt kuitumateriaaliin 19 ja komponentteihin 6, 16.

Edellä esitettyjä valmistusmenetelmiä ja niiden osaprosesseja voidaan modifioida 25 monin tavoin. Esimerkiksi edellä kuvattu varsinaisen liiman käyttö komponentin kiinnittämisessä johdekalvoon 12 voidaan korvata muulla adheesiomekanismilla. Yhtenä esimerkkinä mainittakoon adheesio-ominaisuuden omaavan eristekerroksen 13 käyttö johdekalvon 12 pinnalla (vrt. kuvio 1 ja vastaava selitys). Tällöin komponentit 6 painetaan suoraan eristekerrosta 13 vasten siten, että komponentin kiinnittyvät 30 vastaavalla tavalla riittävästi paikoilleen kuin liimaa käyttävän sovellusmuodon

yhteydessä kuvataan. Tällainen eristekerros 13 voi sisältää esimerkiksi teippimäisen pinnoitteen tai koostua ainakin pintaosaltaan muovautuvasta polymeeristä tai vastaavasta materiaalista.

- Menetelmä voidaan toteuttaa myös ilman liiman 5 tai adheesio-ominaisuuden käyttöä. Tällöin komponentit 6 voidaan kiinnittää paikoilleen esimerkiksi mekaanisesti tai alipaineen avulla. Tällöin alipainetta tai vastaavaa väliaikaista kiinnitystä voidaan ylläpitää kunnes komponentti 6 on riittävästi kiinnittynyt paikoilleen eristemateriaalin 1 avulla.

- Liitettävä komponentti 6 voi olla esimerkiksi integroitu piiri, kuten muistisiru, prosessori tai ASIC. Liitettävä komponentti voi olla myös esimerkiksi MEMS, LED tai passiivikomponentti. Liitettävä komponentti voi olla koteloitu tai koteloimaton ja sen kontaktiterminaalit voivat koostua kontaktialueista 7, kontaktinystyistä 17 tai vastaavista. Komponentin kontaktialueiden pinnalla voi olla myös varsinaista kontaktinystyä ohuempi johdepinnoite.

- Myös eristekerroksen 1 materiaali voidaan valita edellä kuvatuista esimerkeistä poikkeavasti. Eristekerros 1 voidaan valmistaa soveltuvasta polymeeristä tai polymeeriä sisältävästä materiaalista. Eristekerroksen 1 valmistusmateriaali voi olla esimerkiksi nestemäisessä tai esikovetetussa muodossa (kuten prepreg). Eristekerroksen 1 valmistamisessa voidaan käyttää esimerkiksi lasikuituvahvistettua epoksilevyä, kuten FR4- tai FR5-tyyppistä levyä. Muita esimerkkejä materiaaleista, joita voidaan käyttää eristekerroksen 1 valmistamisessa ovat PI (polyimidi), aramidi, polytetrafluorieteeni ja Teflon®. Kertamuovien sijasta tai ohella eristekerroksen 1 valmistamisessa voidaan käyttää hyväksi myös kestumuoveja, esimerkiksi jotakin soveltuvaa LCP-materiaalia (liquid crystal polymer).

- Lisäksi alan ammattilaiselle on selvää, että edellä kuvattuja keksinnön piirteitä voidaan käyttää osana suurempaa kokonaisuutta, esimerkiksi siten, että elektroniikkamoduuli valmistetaan osittain tunnetun tekniikan mukaisia menetelmiä käyttäen ja osittain tässä kuvatun keksinnön sovellusmuotoja käyttäen. Edellä esitettyjen elektroniikkamoduulirakenteiden pinnalle tai pinnoille on myös mahdollista valmistaa lisää piirilevykerroksia tai myös liittää komponentteja esimerkiksi pintaliitostekniikalla.

Alan ammattilainen ymmärtää myös sen, että kun tässä dokumentissa viitataan tiettyyn materiaaliin, esimerkiksi alumiiniin, nikkeliin tai kuparinaan, viittauksella tarkoitetaan materiaalia, joka käyttökohteen kannalta on oleellisesti mainittua materiaalia. Viitattu materiaali voi siis mainitun pääasiallisen ainesosansa lisäksi sisältää käyttökohteen kannalta epäoleellisia määriä epäpuhtauksia ja muita ainesosia. Esimerkiksi alumiininen kontaktialue on tavallisesti materiaalia, joka sisältää tyypillisesti vähintään 95 % alumiinia.

Kun taas viitataan materiaalin sisältävän jotakin tiettyä ainesosaa, tällä tarkoitetaan sitä, että materiaali sisältää mainittua ainesosaa käyttökohteen kannalta oleellisen suuren pitoisuuden. Lisäksi materiaali voi sisältää oleellisia tai epäoleellisia määriä muita ainesosia. Esimerkiksi sinkkiä sisältävä kerros sisältää siis sellaisen määrän sinkkiä, jotta tällä on merkitystä alumiinin ja seuraavan metallin välisen kontaktin ominaisuuksien kannalta.

Edellä esitetyt esimerkit kuvaavat joitakin mahdollisia menetelmiä ja rakenteita, joiden avulla keksintöämme voidaan käyttää hyväksi. Keksintömme ei kuitenkaan rajoitu vain edellä esitettyihin esimerkkeihin ja sovellusmuotoihin, vaan keksintö kattaa lukuisia muitakin menetelmiä ja rakenteita, patenttivaatimusten täydessä laajuudessa ja ekvivalenssitulkinta huomioon ottaen.

Patenttivaatimukset:

1. Menetelmä piirimoduulin valmistamiseksi, jossa menetelmässä

otetaan johdekalvo (12),

5 valmistetaan johdekalvoon (12) kontaktiaukot (8) kontaktielementtien valmistamista varten,

otetaan komponentti (6), joka käsittää kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia,

kiinnitetään komponentti (6) johdekalvoon (12) polymeerikerroksen (25) välityksellä,

10 valmistetaan johdekalvoon (12) kiinnitetyn komponentin (6) ympärille eristekerros (1),

valmistetaan polymeerikerrokseen (25) kontaktialueiden (7) kohdille kontaktireiät (18, 28) siten, että kunkin kontaktireiän (18, 28) ja vastaavan kontaktialueen (7) välinen kontaktipinta-ala (A_{CONT1}) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}), ja

15 kasvatetaan ainakin kontaktirei'issä (18, 28) olevien kontaktialueiden (7) pinnalle välikerros (2), joka sisältää ainakin kolmatta metallia,

kasvatetaan kerros (32) toista metallia, joka kerros (32) on kontaktissa välikerroksen (2) pinnan kanssa ja ulottuu pitkin valmistettavia johteita (22), ja

20 muodostetaan johteet (22) kuvioimalla johdekalvo (12), ja mikäli tarpeen myös johdekalvon (12) pinnalla oleva välikerros (2) ja/tai toista metallia oleva kerros (32).

2. Patenttivaatimuksen 1 mukainen menetelmä, jossa

kontaktiaukot (8) valmistetaan ennen komponentin (6) kiinnittämistä,

komponentti (6) kiinnitetään kontaktiaukoilla varustettuun (8) johdekalvoon (12), ja

25 komponentin (6) kiinnittämisen jälkeen avataan kontaktireiät (18, 28) kontaktiaukkojen (8) kautta.

3. Patenttivaatimuksen 2 mukainen menetelmä, jossa kontaktireiät (18, 28) avataan kontaktiaukkojen (8) kautta CO₂-laserilla, jolloin johdekalvoa (12) käytetään maskina.
4. Jonkin patenttivaatimuksen 1–3 mukainen menetelmä, jossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli sisältää ainakin yhden metalleista sinkki ja nikkeli.
5. Jonkin patenttivaatimuksen 1–3 mukainen menetelmä, jossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli.
6. Jonkin patenttivaatimuksen 1–4 mukainen menetelmä, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33), joka valmistetaan kaksinkertaisella sinkkaattiprosessilla.
7. Jonkin patenttivaatimuksen 1–6 mukainen menetelmä, jossa välikerros (2) käsittää nikkeliä sisältävän kerroksen (34), joka valmistetaan kemiallisella nikkelinkasvatusmenetelmällä.
8. Jonkin patenttivaatimuksen 1–7 mukainen menetelmä, jossa välikerros (2) käsittää kuparia sisältävän kerroksen (35), joka valmistetaan kemiallisella kuparinkasvatusmenetelmällä.
9. Jonkin patenttivaatimuksen 1–8 mukainen menetelmä, jossa eristekerros (1) valmistetaan siten, että
 - otetaan ainakin yksi kuitumateriaalia (19) ja esikövetettua polymeeriä sisältävä eristekalvo (11),
 - valmistetaan kuhunkin kuitumateriaalia (19) sisältävään eristekalvoon (11) reikäkomponenttia (6) varten, ja
 - laminoidaan eristekalvo (11) tai eristekalvot (11) yhteen johdekalvon (12) ja siihen liittyvien rakenteiden kanssa.
10. Jonkin patenttivaatimuksen 1–9 mukainen menetelmä, jossa johdekalvon (12) pinta, jolle komponentti (6) kiinnitetään, käsittää yhtenäisen eristekerroksen (13).
11. Jonkin patenttivaatimuksen 1–10 mukainen menetelmä, jossa komponentin (6) ja johdekalvon (12) väliin sijoitetaan korotuspala (15).

12. Jonkin patenttivaatimuksen 1–11 mukainen menetelmä, jossa piirimoduuliin sijoitetaan komponentin (6) lisäksi ainakin yksi toinen komponentti (16) siten, että ensimmäisen ja toisen komponentin kiinnitystavat eroavat toisistaan polymeerikerrosten (25) ainakin yhden ominaisuuden osalta.
- 5 13. Jonkin patenttivaatimuksen 1–12 mukainen menetelmä, jossa kiinnitettävä komponentti (6) on nystytön komponentti.
14. Piirimoduuli, joka käsittää
- eristekeirroksen (1),
- eristekerroksen (1) sisällä ainakin yhden komponentin (6), joka käsittää
- 10 kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia,
- eristekerroksen (1) pinnalla johteita (22), jotka käsittävät ainakin ensimmäisen kerroksen (12) ja toisen kerroksen (32) siten, että ainakin toinen kerros (32) sisältää toista metallia, ja
- kontaktielementtejä kontaktialueiden (7) ja johteiden (22) välillä sähköisten
- 15 kontaktien muodostamista varten, jotka kontaktielementit käsittävät kontaktialueen (7) materiaalin pinnalla välikerroksen (2), joka sisältää kolmatta metallia,
- jossa ensimmäinen, toinen ja kolmas metalli ovat eri metalleja, ja
- välikerroksen (2) ja kontaktialueen (7) välinen kontaktipinta-ala ($A_{CONT\ 1}$) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}).
- 20 15. Patenttivaatimuksen 14 mukainen piirimoduuli, jossa ensimmäinen metalli on alumiini, toinen metalli on kupari ja kolmas metalli on ainakin yksi metalleista sinkki ja nikkeli.
16. Patenttivaatimuksen 14 mukainen piirimoduuli, jossa ensimmäinen metalli on kulta, toinen metalli on kupari ja kolmas metalli on nikkeli.
- 25 17. Patenttivaatimuksen 14 tai 15 mukainen piirimoduuli, jossa kontaktialueiden (7) materiaali on pääasiallisesti alumiinia.

18. Patenttivaatimuksen 14, 15 tai 17 mukainen piirimoduuli, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33).
19. Patenttivaatimuksen 18 mukainen piirimoduuli, jossa välikerros (2) käsittää sinkkiä sisältävän kerroksen (33) lisäksi ainakin yhden toisen välimetallikerroksen (34, 35).
- 5 20. Patenttivaatimuksen 19 mukainen piirimoduuli, jossa ainakin yksi toinen välimetallikerros (35) on kemiallisella kasvatusmenetelmällä kasvatettua kuparia.
21. Patenttivaatimuksen 20 mukainen piirimoduuli, jossa välimetallikerros (2) käsittää sinkkiä sisältävän kerroksen (33) ja kuparikerroksen (35) välissä ainakin yhden kerroksen (34) nikkeliä ja/tai nikkelin ja alumiinin seosta.
- 10 22. Jonkin patenttivaatimuksen 18–21 mukainen piirimoduuli, jossa sinkkiä sisältävä kerros sisältää sinkkiä, kuparia, nikkeliä ja rautaa.
23. Jonkin patenttivaatimuksen 14–22 mukainen piirimoduuli, jossa osa välikerroksesta (2) ulottuu kontaktielementtien sivuseinämiä pitkin kontaktialueiden (7) ja johteiden (22) välillä.
- 15 24. Patenttivaatimuksen 23 mukainen piirimoduuli, jossa kontaktielementit käsittävät sähkökemiallisella kasvatusmenetelmällä valmistetun kupariytimen (29), joka sivuseinämiensä ja komponentin (6) suunnassa rajautuu välikerrokseen (2) ja johteen (22) suunnassa yhdistyy jatkuvasti eli ilman rajapintaa johteen (22) toisen kerroksen (32) materiaaliin.
- 20 25. Patenttivaatimuksen 23 tai 24 mukainen piirimoduuli, jossa välikerroksen (2) kontaktielementtien sivuseinämiä pitkin ulottuva osa (37) sisältää kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä.
- 25 26. Jonkin patenttivaatimuksen 14–25 mukainen piirimoduuli, jossa johteet (32) käsittävät
- eristererroksen (1) pinnalla ensimmäisen kerroksen (12) kuparia, ja
- ensimmäisen kuparikerroksen pinnalla toisen kerroksen (32) kuparia.

27. Jonkin patenttivaatimuksen 14–25 mukainen piirimoduuli, jossa johteet (32) käsittävät

eristekerroksen (1) pinnalla ensimmäisen kerroksen (12) kuparia,

ensimmäisen kuparikerroksen pinnalla välikerroksen (2), ja

5 välikerroksen pinnalla toisen kerroksen (32) kuparia.

28. Patenttivaatimuksen 27 mukainen piirimoduuli, jossa ensimmäisen ja toisen kuparikerroksen välissä oleva välikerroksen (2) osa käsittää kemiallisella kasvatusmenetelmällä kasvatettua kuparia tai kemiallisella kasvatusmenetelmällä kasvatettua nikkeliä.

10 29. Jonkin patenttivaatimuksen 14–28 mukainen piirimoduuli, jossa kontaktielementin ja komponentin kontaktialueen (7) välisen kontaktipinnan leveys (W_{CONT}) on 0–20 % pienempi kuin kontaktielementin suurin leveys (W_{MAX}) samassa suunnassa.

30. Jonkin patenttivaatimuksen 14–29 mukainen piirimoduuli, jossa kontaktielementin korkeus (H) on pienempi tai yhtä suuri kuin kontaktielementin suurin leveys (W_{MAX}).

15 31. Jonkin patenttivaatimuksen 14–30 mukainen piirimoduuli, jossa eristekerros (1) sisältää ainakin yhden kerroksen kuitumateriaalia (19), jossa kuitumateriaalissa (19) on aukko komponenttia (6) varten, sekä yhtenäisen polymeerikerroksen, joka on kiinnittynyt kuitumateriaaliin (19) ja komponenttiin (6).

20 32. Jonkin patenttivaatimuksen 14–31 mukainen piirimoduuli, joka käsittää johteiden (22) ja komponentin (6) välissä polymeerikerroksen (25), jossa on kontaktireiät (18, 28) kontaktielementtejä varten, ja jossa kontaktielementit täyttävät kokonaan kontaktireiät (18, 28).

25 33. Patenttivaatimuksen 32 mukainen piirimoduuli, jossa johteiden (22) ja komponentin (6) välissä oleva polymeerikerros (25) käsittää ensimmäisen (15) ja toisen polymeerikerroksen (5), jossa ensimmäinen polymeerikerros (15) on ensimmäistä polymeeriä ja toinen polymeerikerros (5) on kovettunutta liimaa.

34. Patenttivaatimuksen 33 mukainen piirimoduuli, jossa ensimmäinen polymeerikerros (15) ja toinen polymeerikerros (5) ovat paikallisia siten, että ne ovat läsnä ainoastaan oleellisesti komponentin (6) kohdalla.

5 35. Jonkin patenttivaatimuksen 14–34 mukainen piirimoduuli, jossa komponentti käsittää passivointikerroksen (9) komponentin pinnalla ja kontaktialueet (7) sijaitsevat passivointikerroksessa (9) olevien avausten sisällä, jolloin välikerros (2) ulottuu passivointikerroksessa (9) olevan avauksen läpi.

(57) Tiivistelmä:

Valmistusmenetelmä ja piirimoduuli, joka käsittää eristekerroksen (1) ja eristekerroksen (1) sisällä ainakin yhden komponentin (6), joka käsittää kontaktialueita (7), joiden materiaali sisältää ensimmäistä metallia. Eristekerroksen (1) pinnalla on johteita (22), jotka käsittävät ainakin ensimmäisen kerroksen (12) ja toisen kerroksen (32) siten, että ainakin toinen kerros (32) sisältää toista metallia. Piirimoduuli käsittää kontaktielementtejä kontaktialueiden (7) ja johteiden (22) välillä sähköisten kontaktien muodostamista varten. Kontaktielementit puolestaan käsittävät kontaktialueen (7) materiaalin pinnalla välikerroksen (2), joka sisältää kolmatta metallia siten, että ensimmäinen, toinen ja kolmas metalli ovat eri metalleja ja välikerroksen (2) ja kontaktialueen (7) välinen kontaktipinta-ala ($A_{CONT\ 1}$) on pienempi kuin kontaktialueen (7) pinta-ala (A_{PAD}).

(Fig. 8)

LS

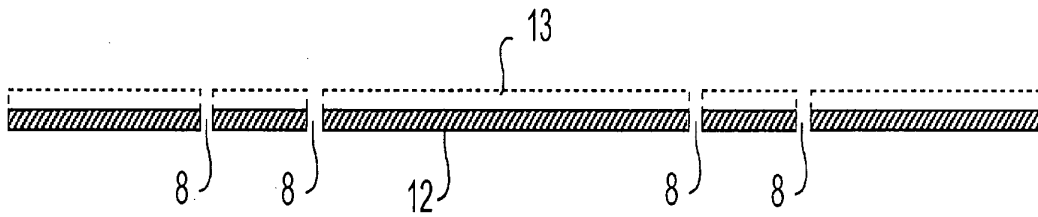


Fig. 1

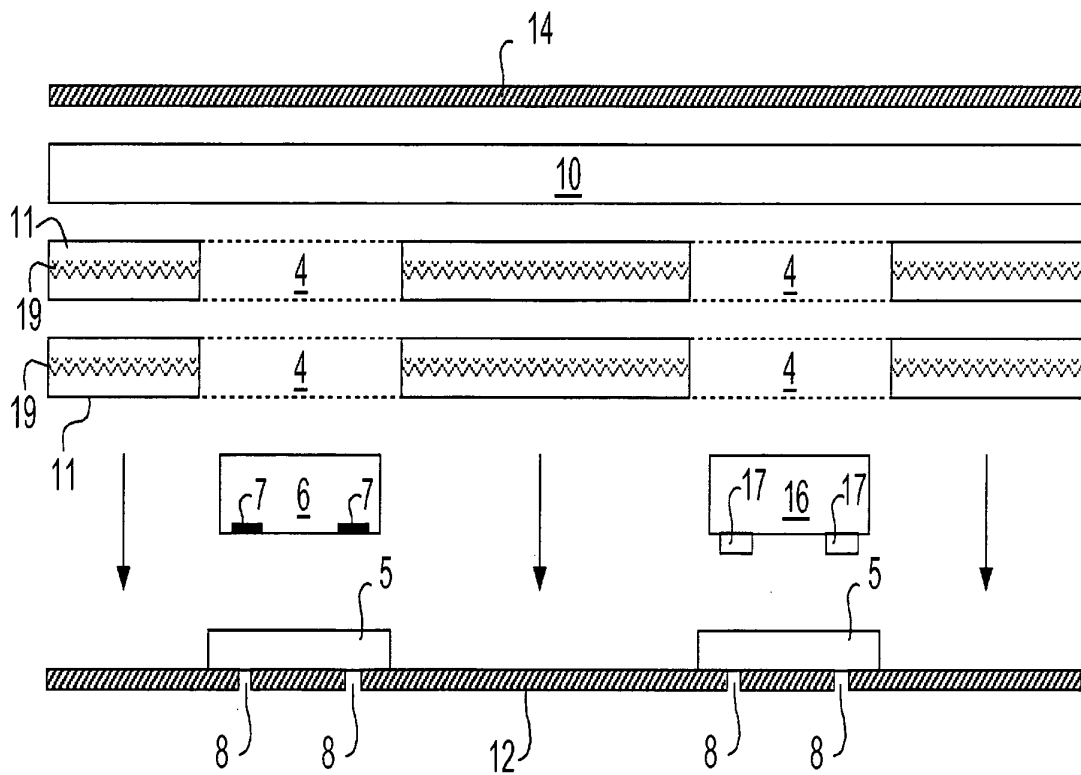


Fig. 2

1/15

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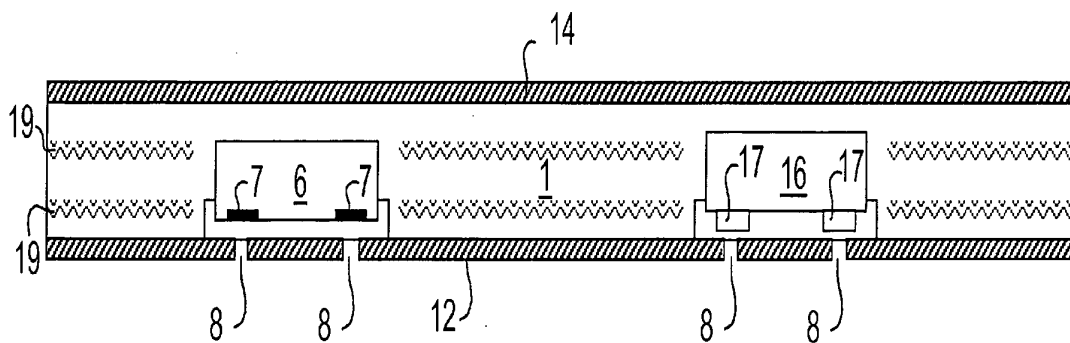


Fig. 3

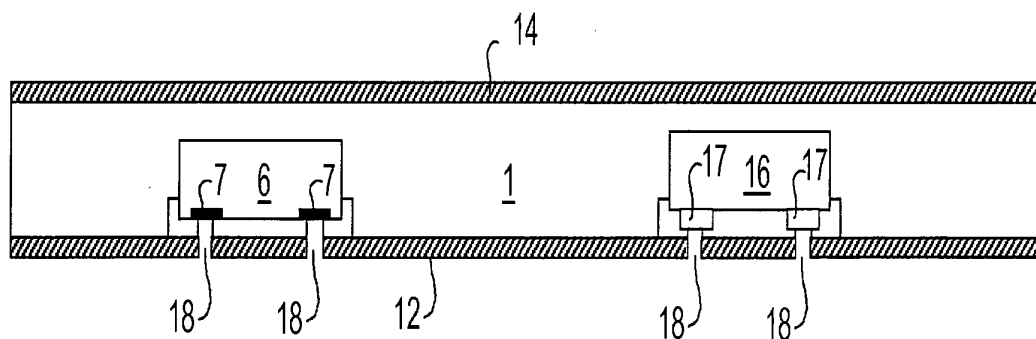


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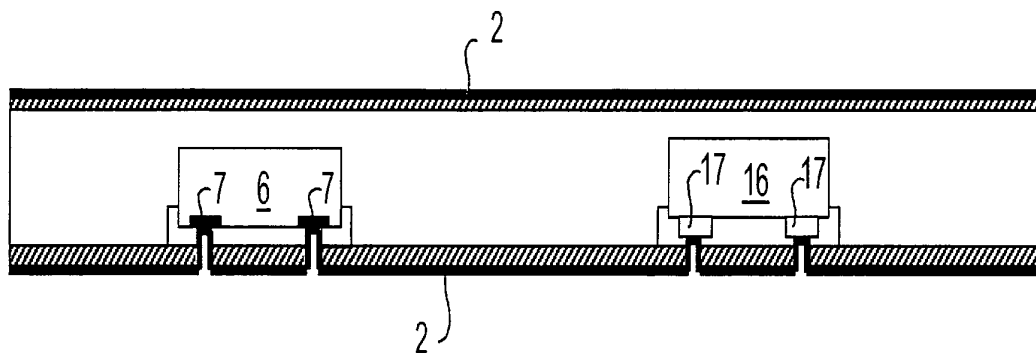


Fig. 5

2/15

L5

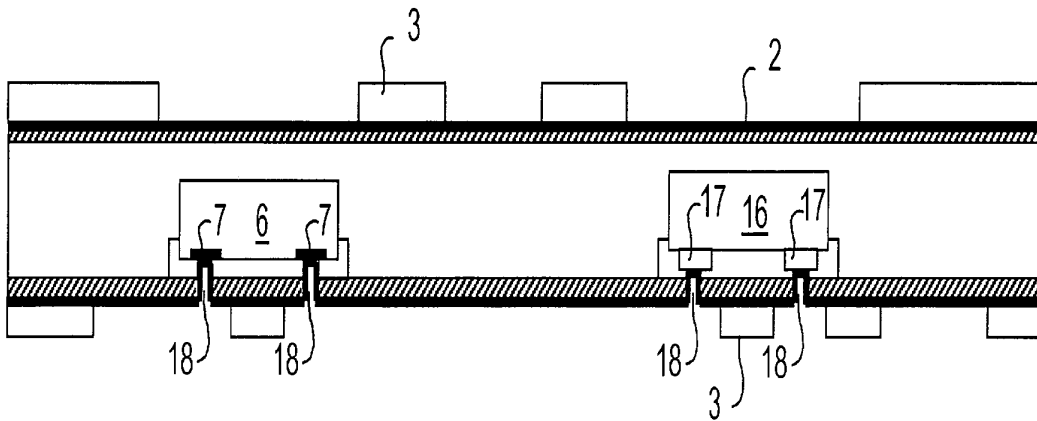


Fig. 6

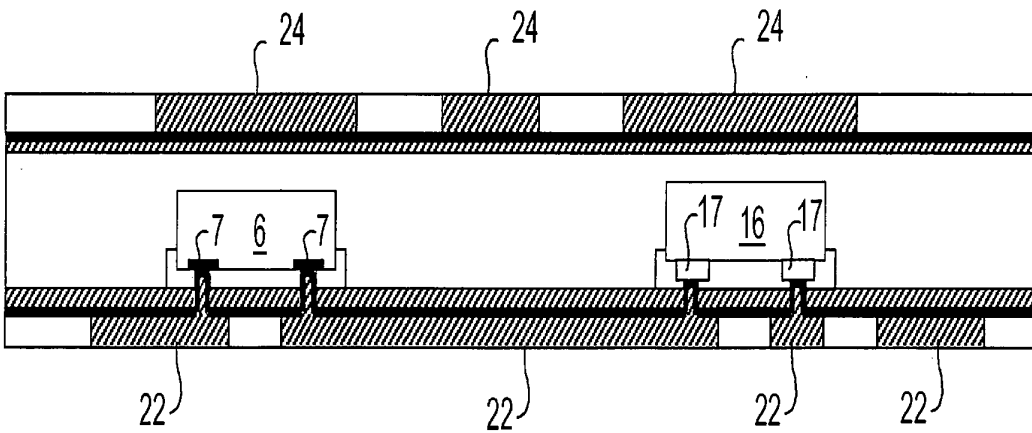


Fig. 7

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L 5

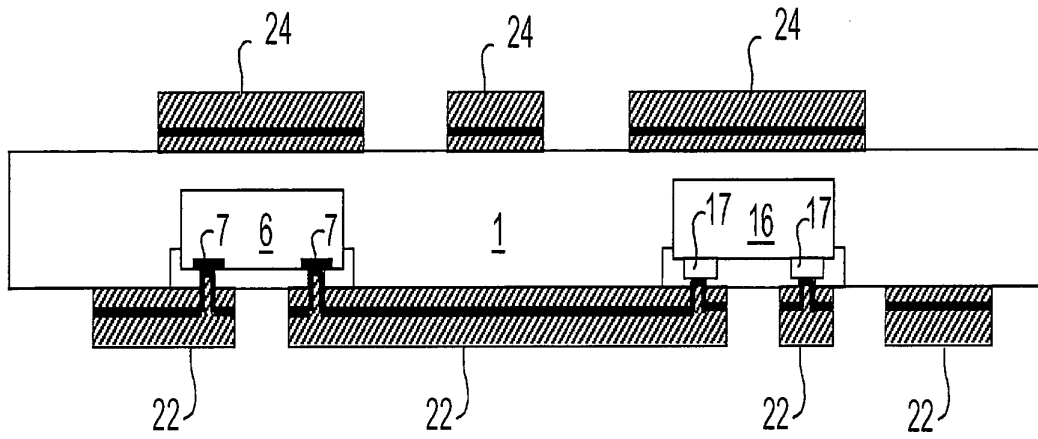


Fig. 8

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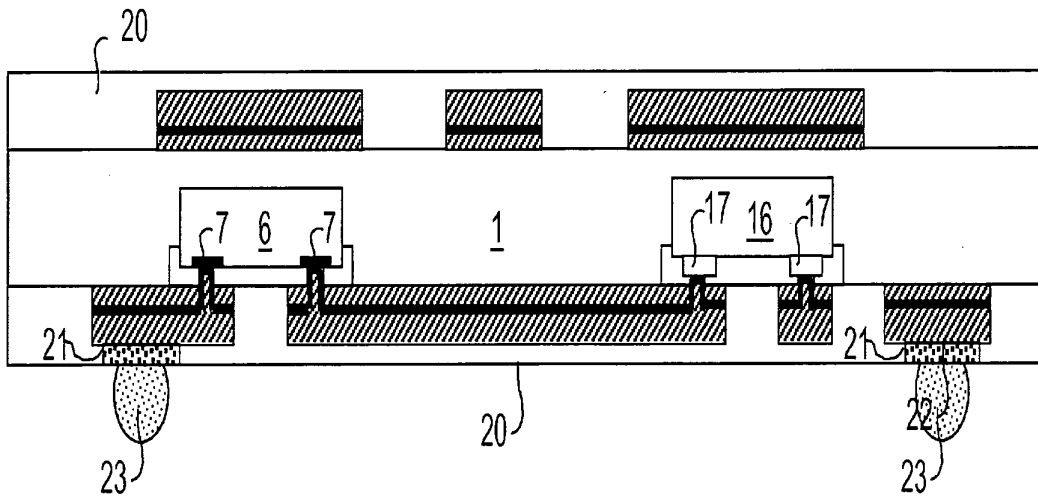


Fig. 9

LS

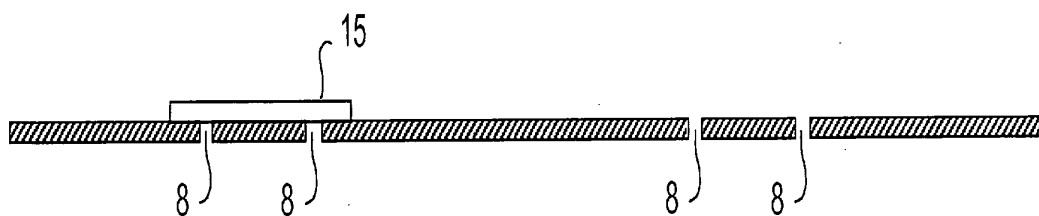
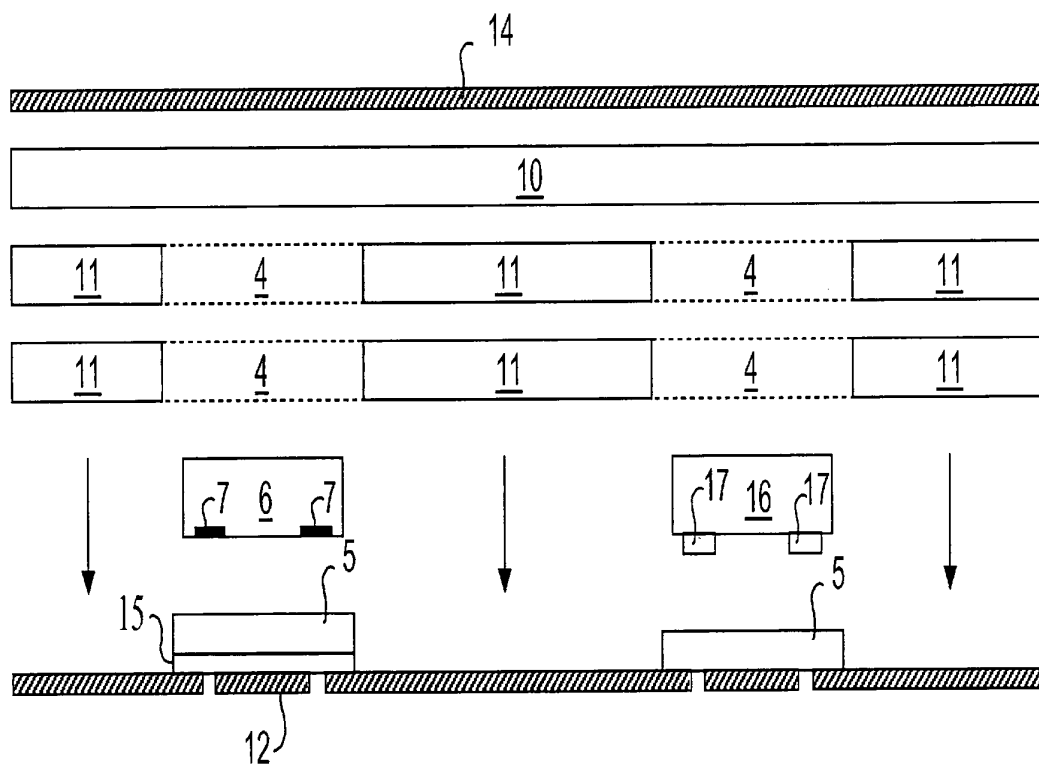


Fig. 10



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Fig. 11

L5

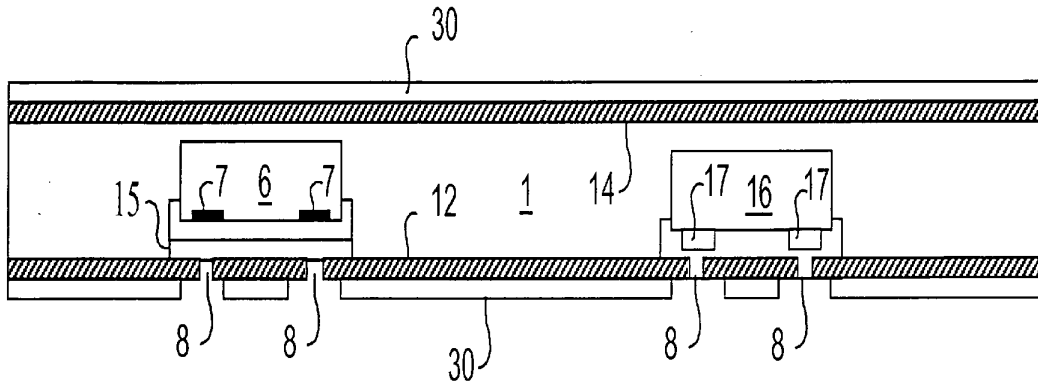


Fig. 12

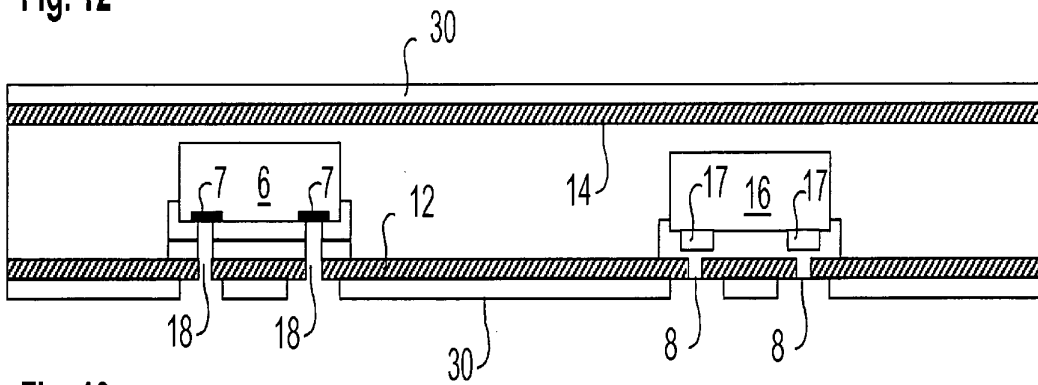


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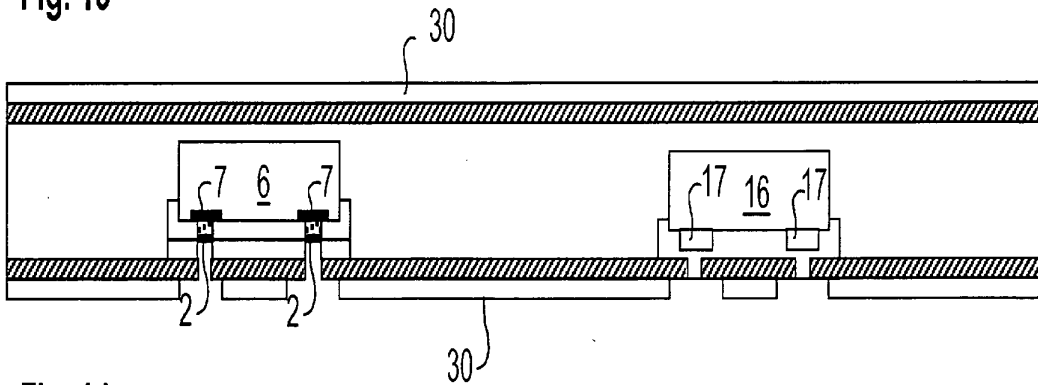


Fig. 14

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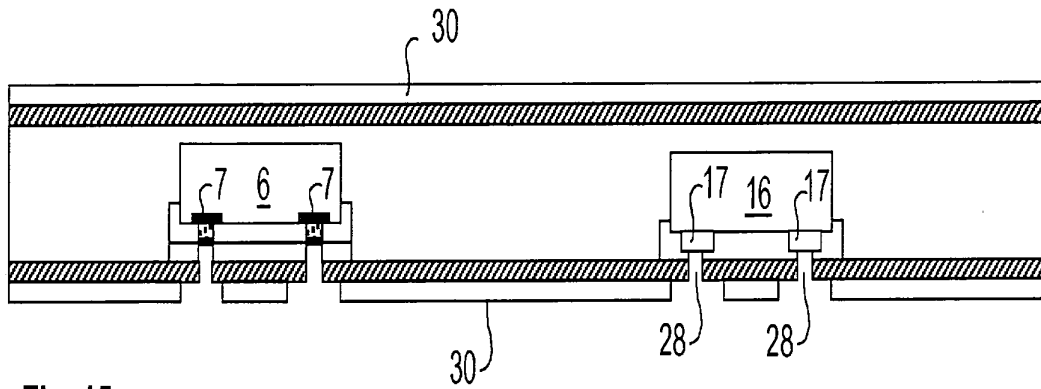


Fig. 15

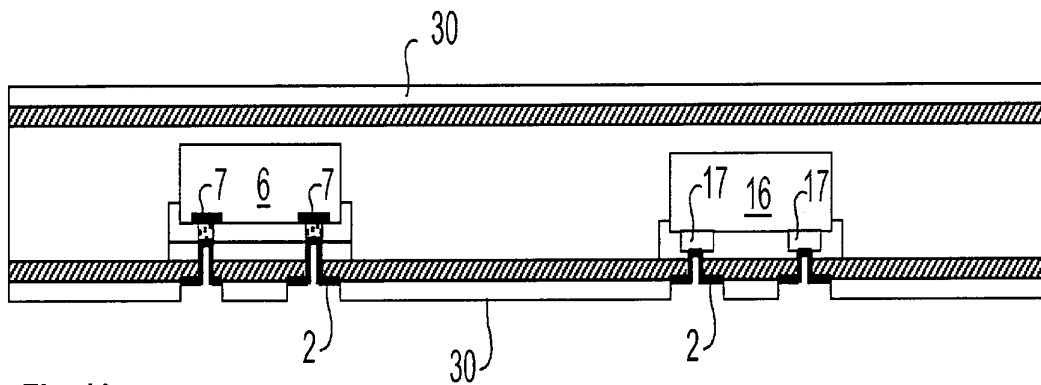


Fig. 16

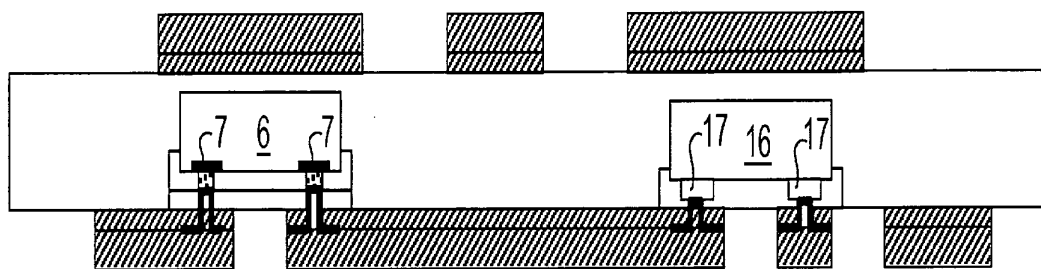


Fig. 17

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L 5

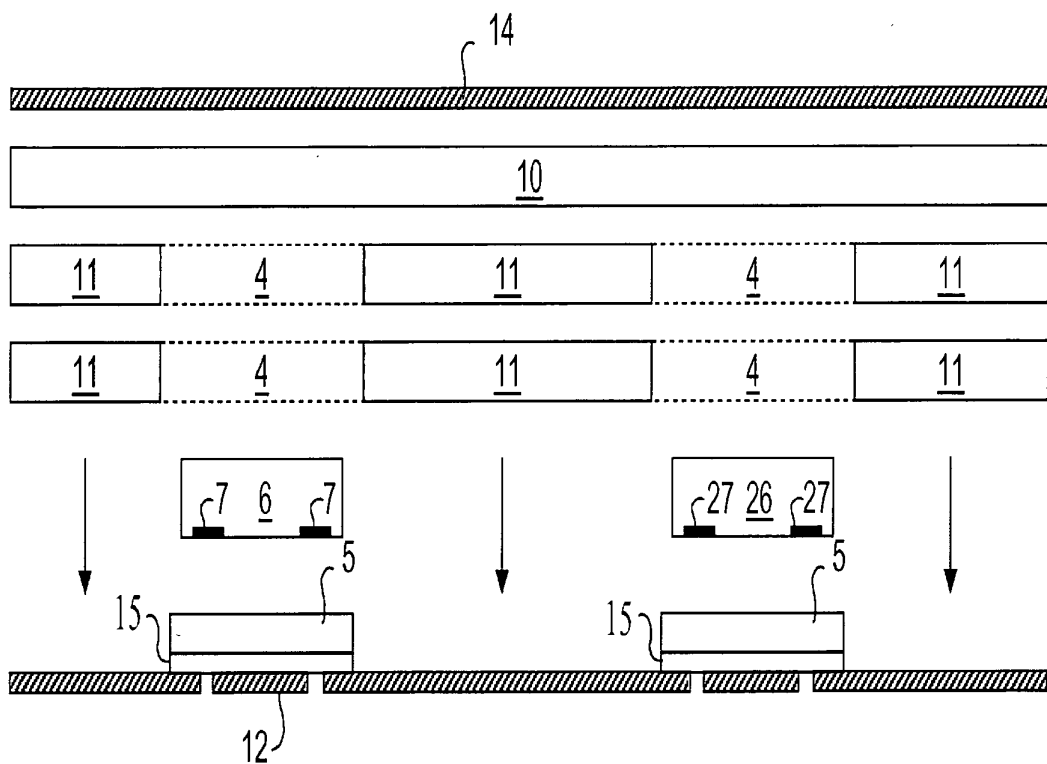


Fig. 18

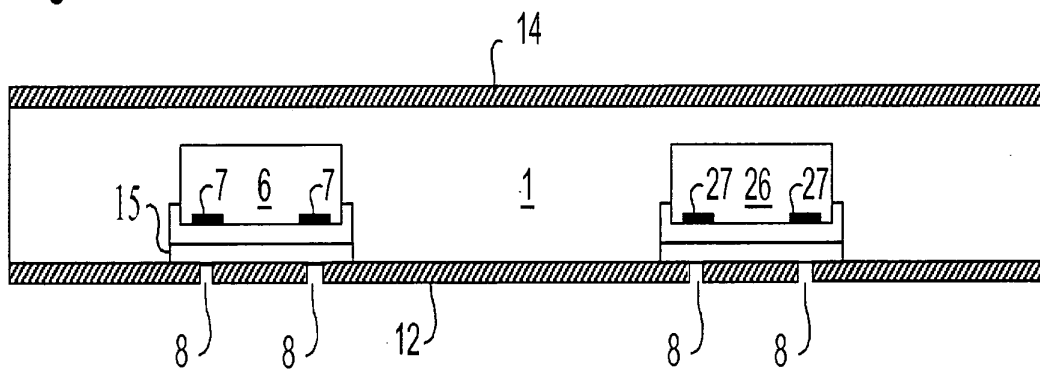


Fig. 19

L5

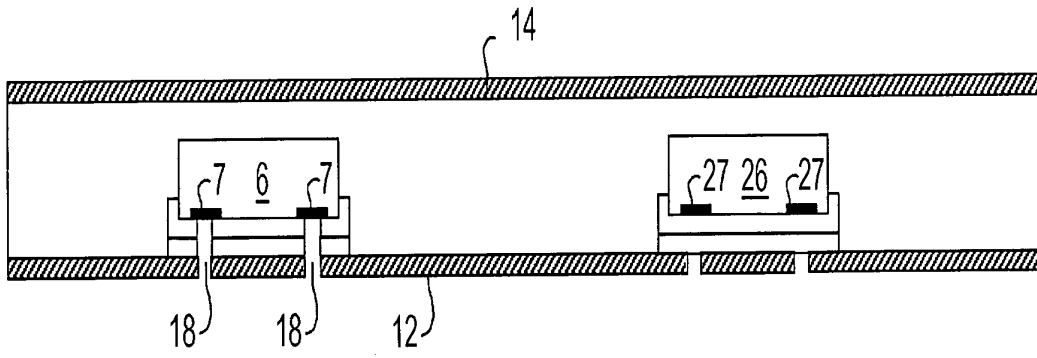


Fig. 20

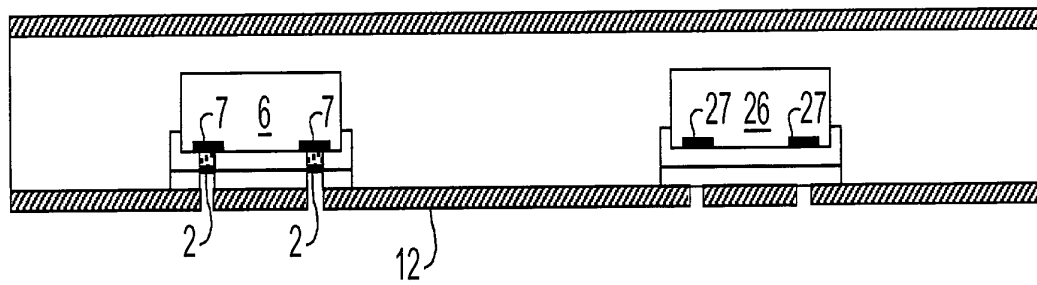


Fig. 21

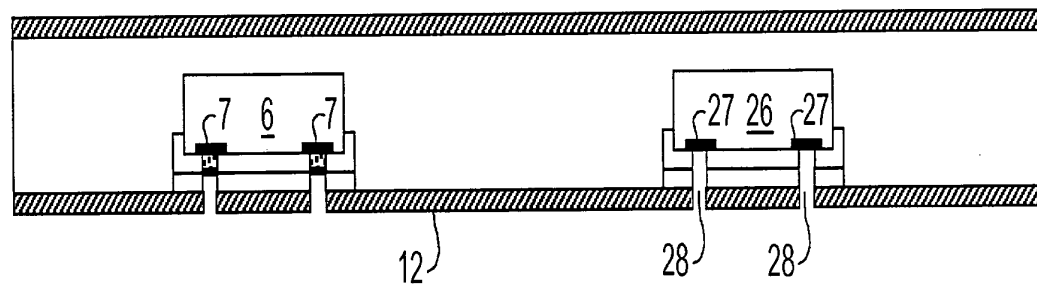


Fig. 22

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L5

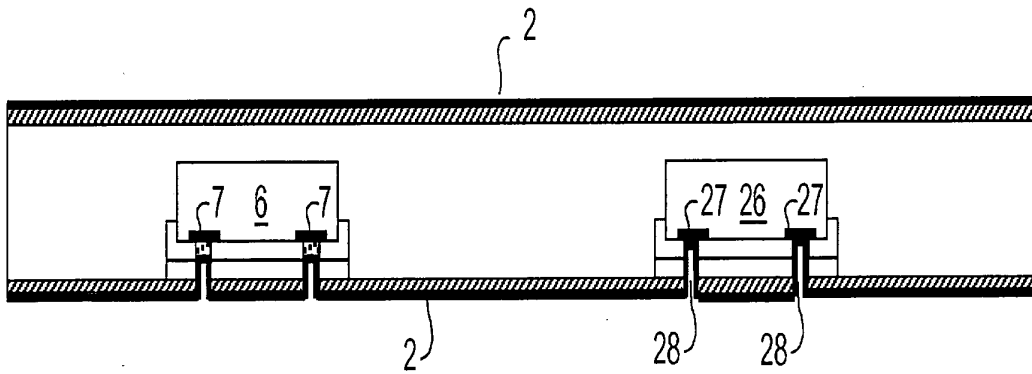


Fig. 23

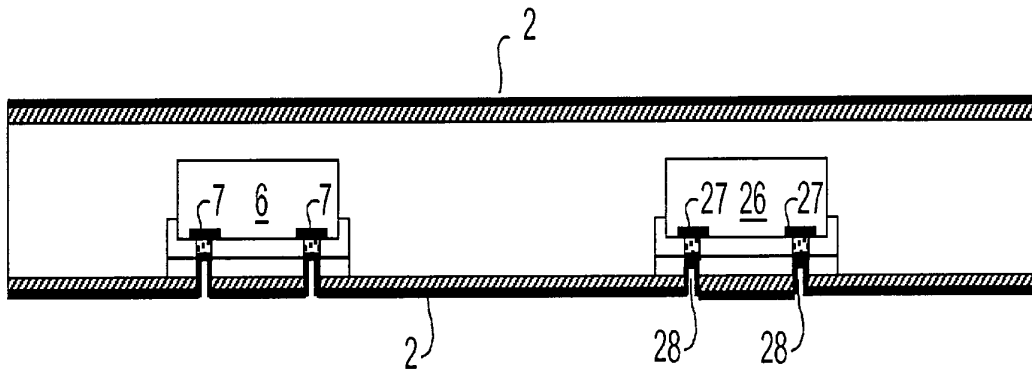
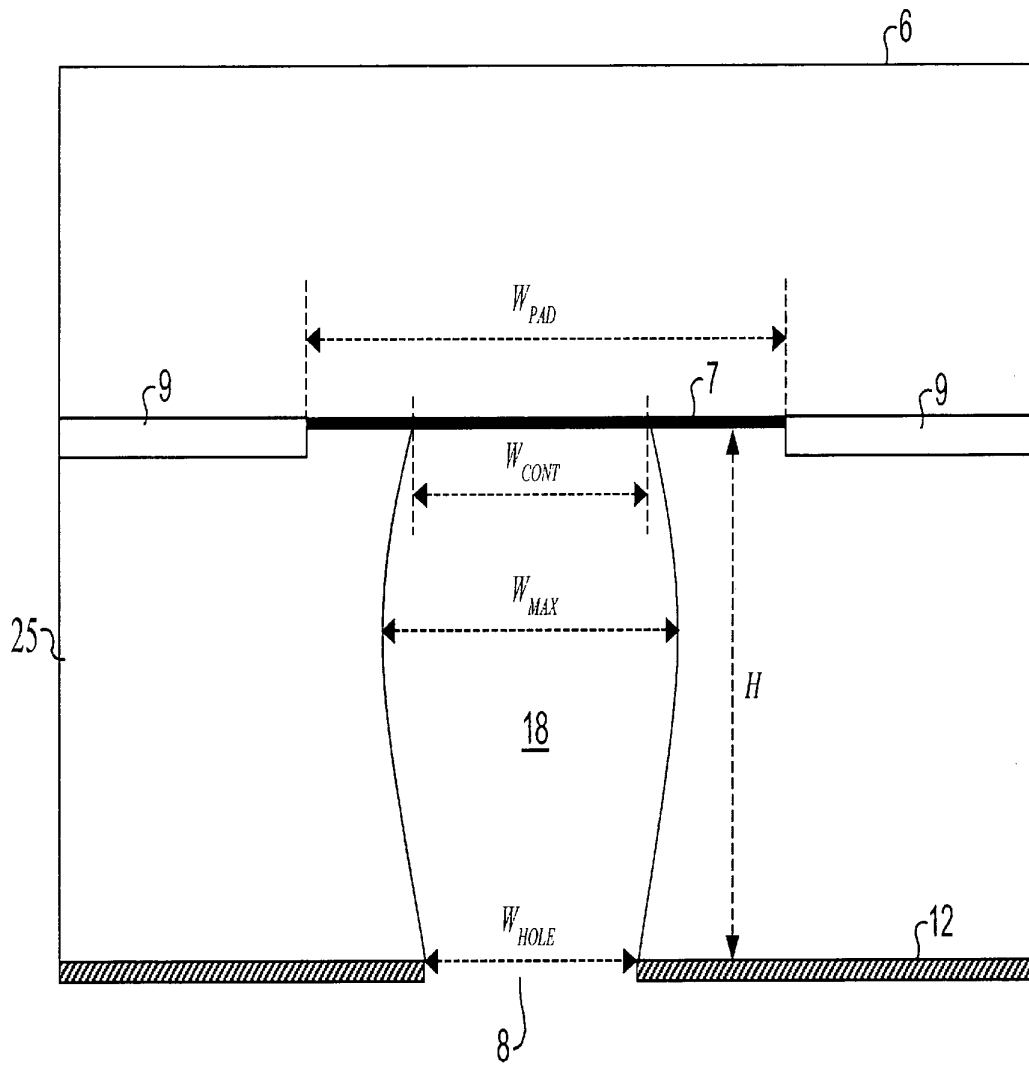


Fig. 24

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11/15

Fig. 25

L 5

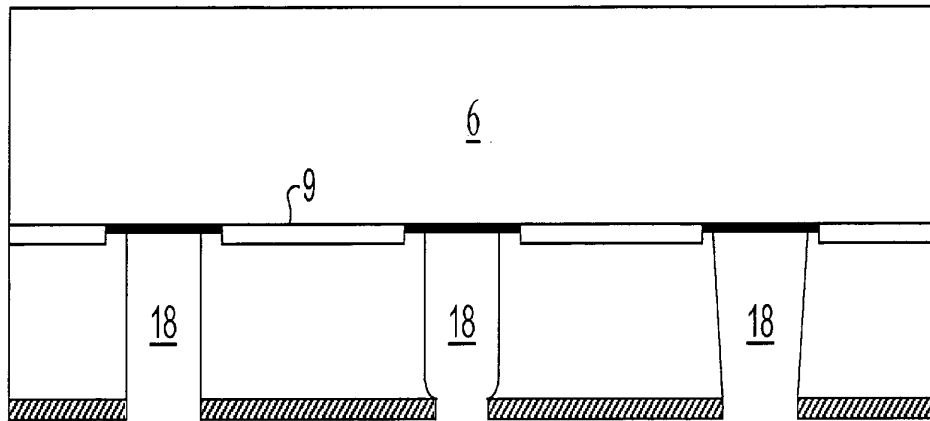


Fig. 26

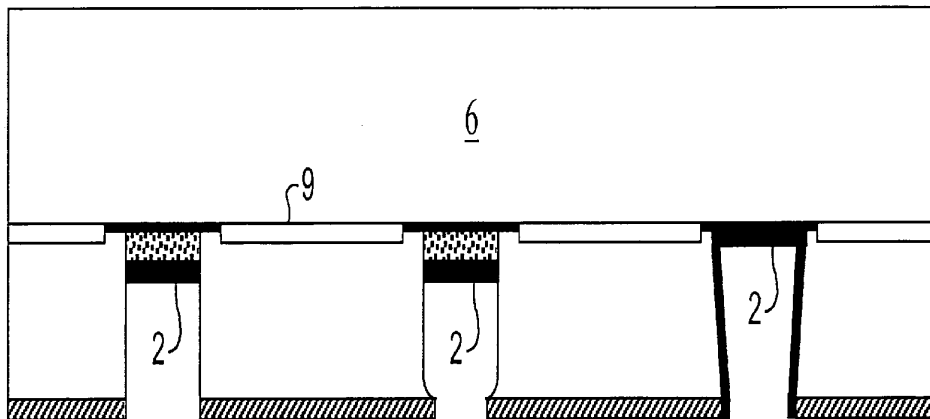


Fig. 27

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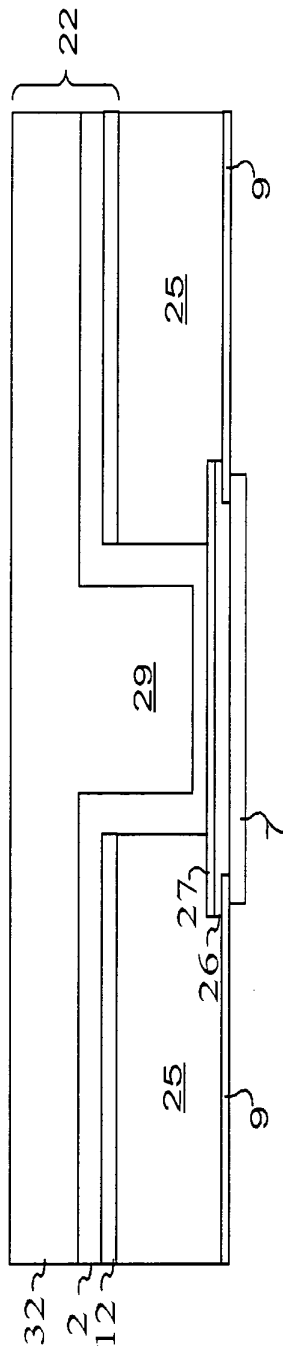


Fig. 28

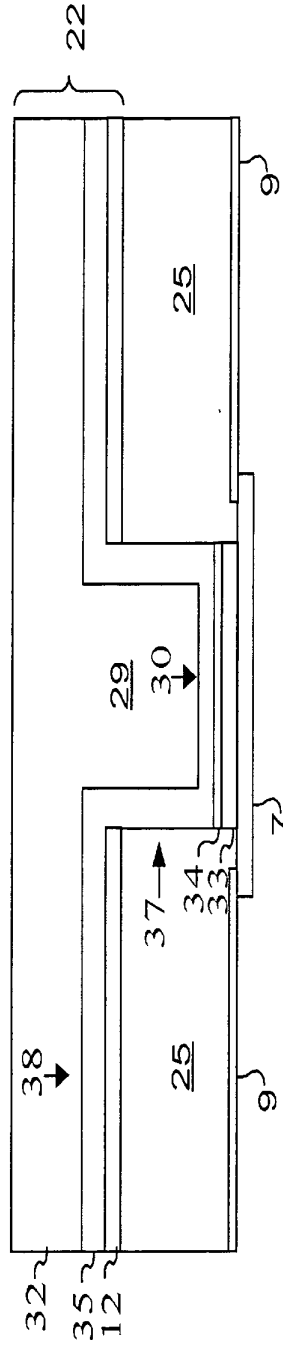


Fig. 29

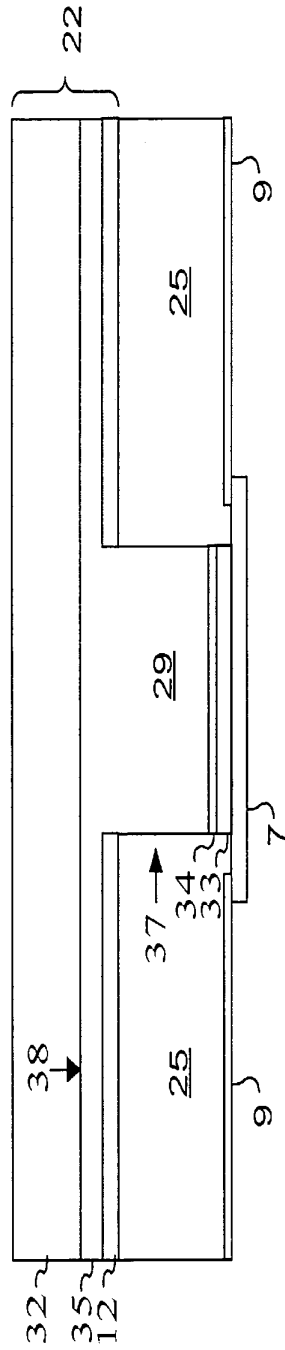


Fig. 30

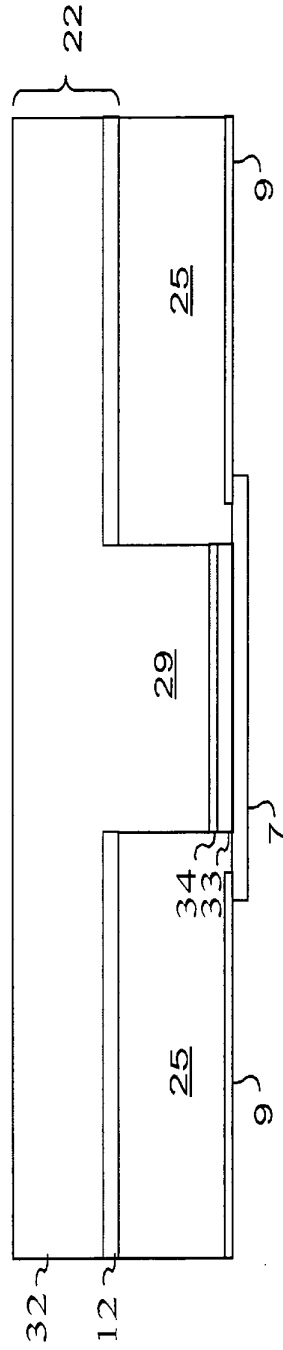


Fig. 31

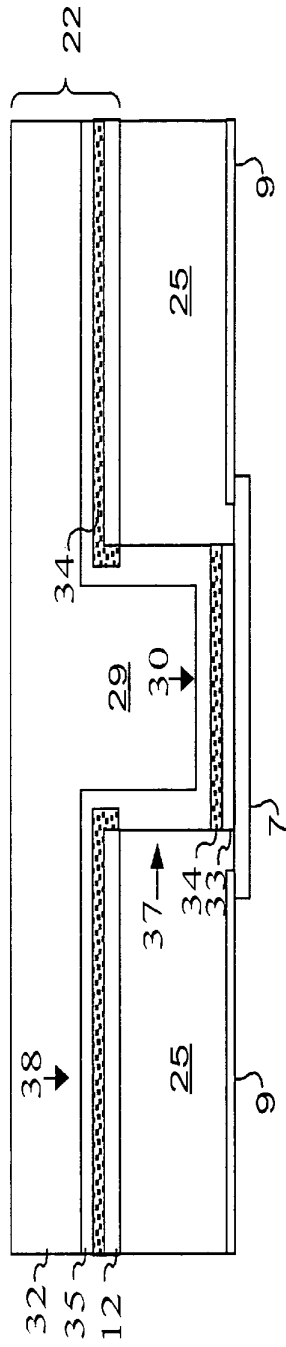


Fig. 32

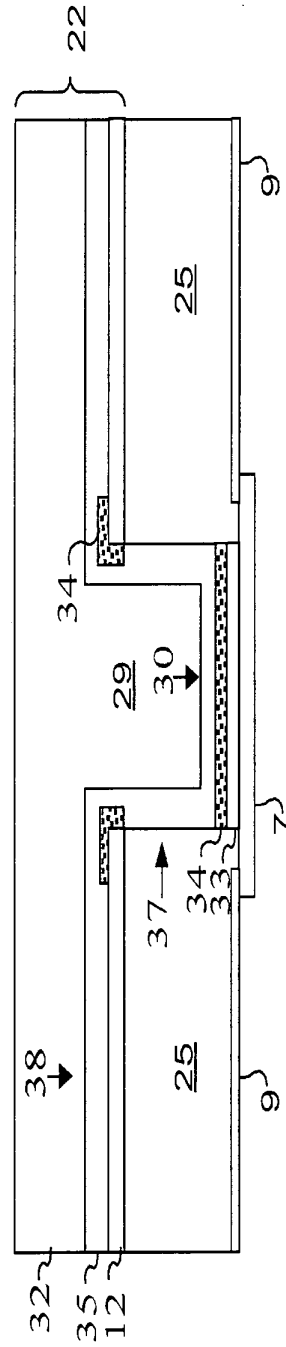


Fig. 33

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APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)				
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A	330				
☒ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A	430				
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A	220				
TOTAL CLAIMS (37 CFR 1.16(j))	35 minus 20 =	• 15	X \$ =				X \$52 =	780				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	• 0	X \$ =				X \$220 =	0				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL				TOTAL		1760			
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AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=			X \$ =	=			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			X \$ =	=			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
			TOTAL ADD'L FEE				TOTAL ADD'L FEE					
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=			X \$ =	=			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			X \$ =	=			
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
			TOTAL ADD'L FEE				TOTAL ADD'L FEE					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

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/EVA GILLIS/

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(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$ =				X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =				X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	11/03/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
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	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE			OR	TOTAL ADD'L FEE		
									0		
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
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	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

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