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UNIVERSITY OF CALIFORNIA,

IRVINE

Fluxless Tin Bonding Processes with Intermetallic Study and Aluminum Circuit Board Technology

DISSERTATION

submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in Engineering

by

Shou-Jen Hsu

Dissertation Committee:
Professor Chin C. Lee, Chair
Professor Farghalli A. Mohamed
Professor James C. Earthman

2015

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DEDICATION

To

my dear family and friends

Without their moral support, unconditional love, and encouragement,
this dissertation would have never been possible.

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2. S.-J. Hsu and C. C. Lee, "Fluxless Bonding of Si Chips to Low Carbon Steel Boards Using Electroplated Sn Solder," submitted

3. S.-J. Hsu, C.-H. Sha and C. C. Lee, "Fluxless Bonding of Si chips to Aluminum Boards Using Electroplated Sn Solder," Journal of Materials Science-Materials in Electronics, vol. 25, pp. 3276-3284, Aug. 2014

4. S.-J. Hsu and C. C. Lee, "Fluxless Tin Bonding Process with Suppressed Intermetallic Growth", IEEE Transactions on Components Packaging and Manufacturing Technology, vol. 4, pp. 551-559, Apr. 2014

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1. S.-J. Hsu and C. C. Lee, "Bonding of SiC chips to copper substrates using Ag-In system" in IEEE 65th Electronic Components and Technology Conference (ECTC), 2015, accepted

2. S.-J. Hsu and C. C. Lee, "Fluxless Tin Bonding of Silicon Chips to Iron," in IEEE 63rd Electronic Components and Technology Conference (ECTC), 2013, pp. 2276-2279

3. S.-J. Hsu and C. C. Lee, "A Monolithic Aluminum Circuit Board Structure," in IEEE 63rd Electronic Components and Technology Conference (ECTC), 2013, pp. 1346-1349

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ABSTRACT OF THE DISSERTATION

Fluxless Tin Bonding Processes with Intermetallic Study and Aluminum Circuit Board Technology

by

Shou-Jen Hsu

Doctor of Philosophy in Engineering

University of California, Irvine, 2015

Professor Chin C. Lee, Chair

This research starts with developing fluxless bonding process using electroplated Sn solder between Si chip and Al substrate. The joint thickness was controlled either by bonding pressure or by incorporating Cu spacers. Cu_6Sn_5 and Cu_3Sn IMCs are observed at Sn/Cu interface. A new two-step anodization process is also introduced to grow high quality alumina on Al boards and coat thick Cu layer over the alumina to produce a Cu/alumina/Al insulated metal substrate (IMS) structure. The measured resistance and breakdown voltage of the as-formed 50 μm anodic alumina layer is larger than 40 MΩ and 600 VDC, respectively. To test the reliability of the boards, they were put through 500 cycles of thermal cycling test and high temperature storage test. To ensure its compatibility with soldering operations, Cu substrates were bonded to the Al boards using a fluxless tin process.

The fluxless bonding process is also applied to bond Si chips to low carbon steel substrates electroplated with Ni with desired thickness. Ni_3Sn_4 is the only IMC formed at the Sn/Ni interface. In order to compare the result to the case without using underbump metallurgy. Sn was electroplated over low carbon steel directly and then Si was bonded to the low carbon steel

substrate. Sn solder layer was bonded to Fe substrate by forming $FeSn_2$ at the Sn/Fe boundary. These results suggest that Sn-Fe reaction system should be another promising bonding pair candidate that could mitigate excessive IMC thickness. The liquid Sn/solid Fe reaction couples were fabricated and annealed at different temperatures. The growth kinetics of $FeSn_2$ was modeled by parabolic law and empirical power law.

We finally move to develop a fluxless bonding process with suppressed IMC formation. According to Cr-Sn phase diagram, there is no IMC formation in Cr/Sn system. Cr is thus selected as the barrier metal. Several bonding experiments have been performed and the preliminary results show that high quality Sn joints could be produced with little IMC formation before high temperature aging.

Chapter One

Introduction

1.1 Electronic Packaging

To make integrated circuit (IC) chips operational, they need to be bonded and connected to packages using appropriate bonding medium. The packages along with the bonding medium serve the purposes of power distribution, signal distribution, heat dissipation, and protection for IC chips. To perform well, the packages are commonly bonded to solders due to the natures of high thermal conductivities, high electrical conductivities, and the low processing temperature. In current electronic packaging industries, the reliability of solder joints is a key design factor. Compared to extremely reliable solid-state devices, having the failure rate in parts-per-million (ppm), solder joints or interconnections have much higher failure rate, leading to short life time of products [1]. This short life time results from the use of flux in conventional soldering processes and the shear stress developed when bonding materials with mismatch in thermal expansion coefficient.

Another potential issue arises as the chip size continues to scale down. When more and more transistors are placed on the same Si chip size, larger pin-out numbers and smaller solder joints are inevitable. According to International Technology Roadmap for Semiconductors (ITRS),

by 2018, the pitch in flip-chip interconnects will become smaller than 70 μm for high performance applications [2]. Two problems occur. The first is increase in shear strain. The aspect ratio of flip-chip joints is constrained to 0.7 because it goes through molten phase in the reflow process. Therefore, smaller joints become shorter as well, resulting in larger shear strain arising from CTE mismatch between Si chips and package substrates. The second is increase in stress in the joints. Since intermetallic (IMC) thickness in the joint does not scale down with joint size, ratio of IMC thickness to joint height increases. This further enlarges the shear stress because the IMC does not deform as the soft solder does to accommodate CTE mismatch. To solve the problems mentioned above, solid state bonding technique is investigated.

In what follows, the soldering process and fluxing action are first reviewed. Fluxless bonding technique is then discussed. The dissertation outline is given at last.

1.2 The Soldering Process

Different from adhesive bonding and direct bonding techniques, soldering bonding relies on the chemical reaction between solders and as-bonded parts. Commonly used solder alloys contain elements that have low melting temperatures such as tin (Sn), indium (In), and bismuth (Bi). In the soldering process, the solder materials melt and react with to-be-bonded parts to form

intermetallic compounds (IMCs). Take Sn-based lead-free solder on copper as an example, during soldering process, solder melts and wets copper. The molten Sn solder dissolves copper (Cu) atoms to form solid Cu_6Sn_5 IMC at the interface as portrayed in Fig. 1.1. This Cu_6Sn_5 IMC layer joints solder and copper together. Thus, the intermetallic formation is an essential reaction to achieve bonding in nearly all soldering systems.

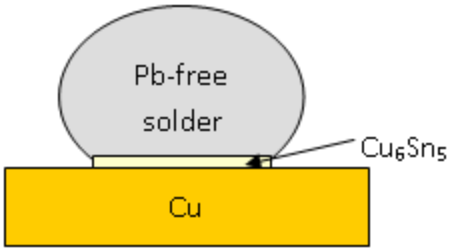

Fig. 1.1 A solder joint needs intermetallic formation to be achieved

1.3 The Fluxing Action

To achieve soldering joint formation, the chemical reaction that forms IMCs between molten phase and substrate need to occur. However, solder and substrate metals have a native oxide layer on their surface. These oxide layers usually have melting temperature higher than the soldering temperature, i.e. the melting temperatures of SnO and SnO_2 are 1,080°C and 1,630°C, respectively. They are also lighter than solders. During reflow process, the oxide layer does not melt and forms a thin film on the surface of molten solders. This oxide layer shields the molten phase from reacting with substrate metals. The joint, thus, is not formed unless the oxide layer is

removed. The flux containing resin acids mainly react with metal oxides such as CuO and SnO as follows,

$2\ R\text{-}COOH + CuO \rightarrow (R\text{-}COO)_2Cu + H_2O$

$2\ R\text{-}COOH + SnO \rightarrow (R\text{-}COO)_2Sn + H_2O$

where R represents the carboxyl residue. For the case of abietic acid, R = $C_{19}H_{29}$. In above equations, the Cu and Sn oxides convert into salts and water. As exhibited in Fig. 1.2, the fresh solder and base metals can contact intimately to form IMCs during reflow process once the metal oxides are removed by fluxing actions. As a result, the joint is achieved. During fluxing action, residues are accompanied, which are known to cause voids and uneven thickness in joints, leading to degrading the performance of device [3, 4]. In addition, some electronic devices are restricted from using flux such as optoelectronic devices, medical devices, and laser diodes because residues contaminate and corrode devices [5]. The fluxless process, thus, become very critical to improve reliability in the electronic packaging.

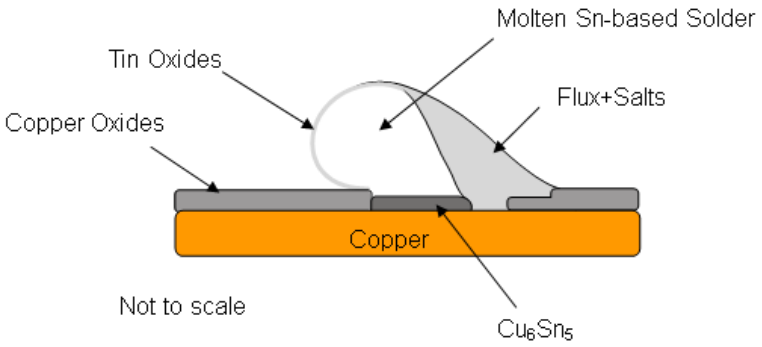

Fig. 1.2 Molten flux converts oxides into salts to expose fresh solder and fresh base metal, and to

shield them from further oxidation [6, 7]

1.4 Fluxless Bonding Technique

There are several approaches to achieve fluxless bonding. The first method is using acid vapor, acetic or formic acid, to reduce metal oxides [8-10]. Fundamentally, this method is similar to the conventional soldering process except that vapor chemicals rather than liquid chemicals are used. Acid vapor is known to be corrosive to devices as well. Another fluxless method is to treat the solder by fluorine (F) to convert tin oxide into tin oxyfluoride which can be dissolved by molten solder. The third method, invented by our group, is providing oxidation-free environment from solder manufacture to joint formation [11-13]. During the entire process, solders are prevented from oxidation. Table 1.1 lists the four requirements to prevent oxidation. First, solder materials should be fabricated in an oxidation-free environment such as vacuum deposition or electroplating method. Second, there should be a thin capping layer, usually gold (Au) or silver (Ag) layer, on the solder materials to protect inner solders from oxidation when solders are exposed to air. During the reflow process, this thin capping layer should dissolve and become part of joints. The fresh solders can react with base metals to form IMCs. Finally, the bonding process should be performed in vacuum, inert gas, or H_2 environment to inhibit oxidation. This oxidation-free fluxless soldering technology was first reported by our group in 1995 [14], and has been applied to developing

various fluxless processes based on Sn-Au, Sn-Cu, Sn-Ag, Sn-Bi, Sn-In, In-Au, In-Cu, In-Ag binary systems and In-Pb-Au ternary system [12-18].

The purpose of this dissertation is to produce solder joint between semiconductor dies or ceramic boards and commonly used metal substrates. Pure Sn is used as the bonding medium. The advantage of pure Sn system is that Sn is soft and ductile. It can endure large shear strain caused by CTE mismatch between semiconductor dies and substrates. The dissertation outline is presented in next section.

Table 1.1 Four basic requirements for oxidation-free fluxless bonding technology

Process	Approach
Solder manufacture	Electroplating or vacuum deposition
A capping layer over solder	Ag or Au
Dealing with capping layer	Dissolution
Bonding environment	Vacuum or inert gas or H_2

1.5 Dissertation Outline

In this dissertation, fluxless bonding techniques using electroplated Sn system are employed for various bonding designs and a new anodization method is developed to demonstrate the possibility and advantages of the aluminum circuit board technology. The materials fabrication, bonding furnace setup and process flow, and anodization process flow are described in Chapter 2.

In Chapter 3, a fluxless bonding process was developed to bond Si chip to Al boards using Cu as underbump metallurgy (UBM). This process surmounts the huge coefficient of thermal expansion (CTE) mismatch between Si (3 ppm/°C) and Al (23 ppm/°C). The solder joint thickness was controlled either by bonding pressure of 0.6, 2.5 and 32 psi or by incorporating Cu spacers of 50 μm in thickness. Scalloped-shaped Cu_6Sn_5 and thin Cu_3Sn intermetallic compounds (IMC) were formed at the Sn/Cu interface. Despite the large CTE mismatch, the joints are still well bonded. The bonding strength of the joint was evaluated by shear test. All the samples pass the strength requirement specified in MIL-STD-883H method 2019.8.

In Chapter 4, a novel Al circuit board technology fabricated using two-step anodization method and Cu electroplating was proposed and designed. Electrical resistance and breakdown voltage of the 50 μm anodic alumina layer were measured as > 40 MΩ and 600 VDC, respectively. The reliability tests on the Al circuit board were also conducted. The samples pass 500 cycles of thermal cycling test between -40°C and +85°C and 100 hours of high temperature storage test at 250°C. Cu substrate was also successfully bonded to the Al circuit board using electroplated Sn to ensure its compatibility with soldering operation.

In Chapter 5, a fluxless process of bonding Si chip to low carbon steel (Fe) using nickel (Ni) as underbump metallurgy was developed. The choice of Ni comes from the general idea that Ni is thought to possess slower rate of reaction with Sn. The reaction between Ni and Sn was

studied by varying the electroplated Ni UBM thickness and reflow time. It is observed that Ni_3Sn_4 is the only IMC formed at the Sn/Ni interface. To investigate the microstructure and morphology of the Ni_3Sn_4 IMC, the bulk of Sn was etched away to reveal the 3D microstructure.

In order to compare the result in Chapter 5 to the bonding of Si chip to low carbon steel without using UBM, Si chip was bonded directly to Sn-electroplated Fe substrate. The results were reported in Chapter 6. It is shown that $FeSn_2$ is the only IMC phase observed at the Sn/Fe interface. The IMC thickness is only 1.1 to 1.5 μm. This suggests that Sn-Fe reaction system should be another promising bonding pair candidate that could mitigate excessive IMC thickness.

In Chapter 7, the growth kinetics of $FeSn_2$ IMC between Sn and Fe liquid-solid reaction couple was studied. The growth kinetics of $FeSn_2$ was modeled by parabolic law and empirical power law. Based on the models, the growth constants, activation energy and time exponents were established from the data coming from different annealing temperatures.

In Chapter 8, a fluxless bonding process between direct-bonded Cu (DBC) alumina substrate and Cu substrate was developed with suppressed IMC formation at the bonding interface. The fundamental concept is to use Cr as the barrier layer between Sn and Cu. Several bonding experiments have been performed and the preliminary results show that high quality Sn joints could be produced with a little IMC formation before high-temperature aging. After aging at homologous temperature of 0.9 of Sn for 100–200 hours, Cu_6Sn_5 and Cu_3Sn IMCs are formed

locally at some microcracks or pinholes on the Cr layer. They are caused by the penetration of molten Sn through microcracks or pinholes and reaction with the underlying Cu.

In Chapter 9, a summary is given to point out important conclusions in this dissertation.

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Chapter Two

Experiment Setup and Techniques

2.1 Materials Fabrication

In the electronic packaging field, vacuum deposition, stencil printing, and electroplating method are three common methods to fabricate solder layers. In our cases, electron beam evaporation and electroplating are the two techniques we use for conducting experiments.

2.1.1 Electron Beam Evaporation

Electron beam (e-beam) evaporation is a form of physical vapor deposition (PVD). PVD processes are commonly used for the deposition of metallic films, because they can be performed at lower process risk and cheaper in regards to materials cost that Chemical Vapor Deposition (CVD). In e-beam evaporation, a target anode is bombarded with an electron beam given off by a charged tungsten filament under high vacuum. The electron beam causes atoms from the target to transform into the gaseous phase. The gas molecules are able to evaporate freely and then condense on all surfaces inside the chamber. The entire process takes place inside of a vacuum chamber and multi-layer coatings can be deposited in one duty cycle.

The vacuum deposition provides clean, uniform, and well thickness controlled metal layers. In one high vacuum cycle, usually 2×10^{-6} to 3×10^{-6} torrs, up to three or four metal layers can be deposited. These metal layers are efficiently prevented from oxidations. However, during deposition, the substrates undergo high temperature, which may incur unwanted interdiffusion and reaction between deposited metal layers and also cause breakage when bonding CTE mismatch materials. In addition, it is difficult to produce metal layers thicker than 10μm using vacuum deposition method, and to build and maintain a vacuum system is costly. In our experiment, e-beam deposition is used to produce thin metal films, serving as adhesion layers and capping layers.

Stencil printing and electroplating method, thus, become economical alternatives. Stencil printing is a wide used thick-film process for applying films of viscous solder pastes on substrates at room temperature. The typical stencil printing process starts with an UBM. Solder paste is stencil printed on the UBM, and then reflowed to form solder bumps. Since solders are exposed to air and get oxidized during manufacture and printing processes, flux is employed during the reflow process. As described in Section 1.3, joint quality degrades due to the usage of flux. In this research, the electroplating process is adapted to produce solder layers.

2.1.2 Electroplating

Electroplating is a process of depositing a metal layers on a conductive substrate immersed in an electrolytic bath composed of a solution of the salt of the metal to be plated. The deposition is driven by external DC current. The anode is made of the metal to be plated, and the cathode connects to the substrate. Take silver (Ag) electroplating as an example. At the anode, Ag atoms are dissolved by $Ag \rightarrow Ag^{+} + e^{-}$, and the reduction reaction at the cathode is $Ag^{+} + e^{-} \rightarrow Ag$. The Ag ions, thus, are plated onto the substrate surface. Compared to vacuum deposition, electroplating is less expensive and easily to fabricate thick layers. It can be implemented at relative low temperature, from room temperature to 80ºC. Although solders produced by electroplating method might get oxidized during manufacture, the metal oxides can be removed using proper chemical treatments. If the metal structure is designed well, the fresh metal can be protected by an outer capping layer and realize the fluxless bonding feature.

2.2 Vacuum Furnace and Bonding Setup

In this research, all of bonding process is done in a vacuum furnace built in house as depicted in Fig. 2.1 [1]. The vacuum furnace consists of a quartz cylinder, two stainless steel plates, a heating platform, and a ceramic post. The quartz cylinder, having the inner diameter of 130 mm and height of 200 mm, is sandwiched between two steel plates to construct a vacuum chamber.

The interference between the cylinder and the steel plate is sealed by an O-ring. It is easy to observe the sample during the reflow process because to the transparency of quartz. The temperature is monitored by two type-K thermocouples (Chromel+ Alumel-) at two locations, the top surface of sample and the sidewall of platform. Inside the vacuum furnace, a graphite platform is supported by a ceramic poster standing at the center of the base stainless steel plate.

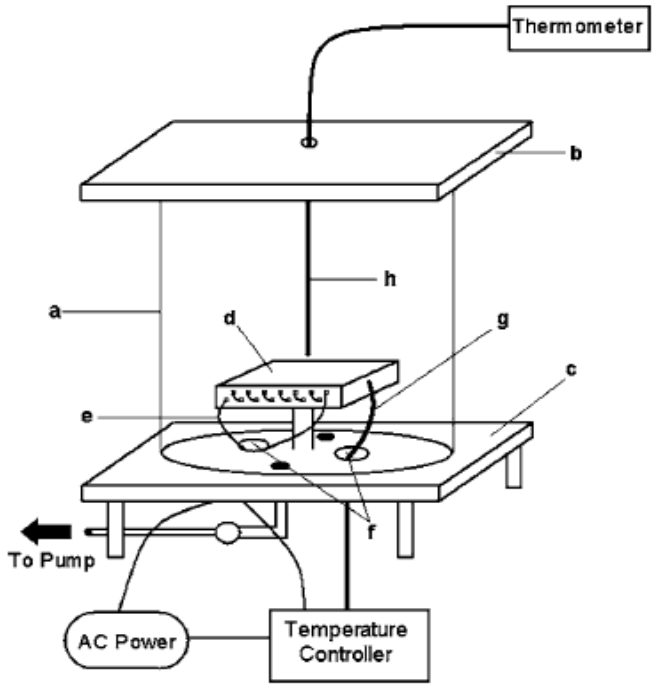

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Fig. 2.1 Schematic of the vacuum furnace showing key components: (a) quartz cylinder, (b) upper stainless plate, (c) base plate, (d) graphite platform, (e) heating wire, (f) electrical feedthroughs, (g) platform thermocouple, and (h) sample thermocouple

The graphite platform, having the size of 75×75×10 mm^3, is drilled with many holes to allow the heating wire (Nickel-Chromium alloy) going through the body of the block. The wire is

electrically insulated from the graphite using ceramic tubes as shown in Fig. 2.2. Graphite was chosen as the material of the platform because it has been experimentally proven that it absorbs 97% of radiation and is a nearly perfect emitter of radiation [2]. Therefore, the platform will absorb a maximum amount of heat given off by the wires. It is also easy to machine and can withstand very high temperature.

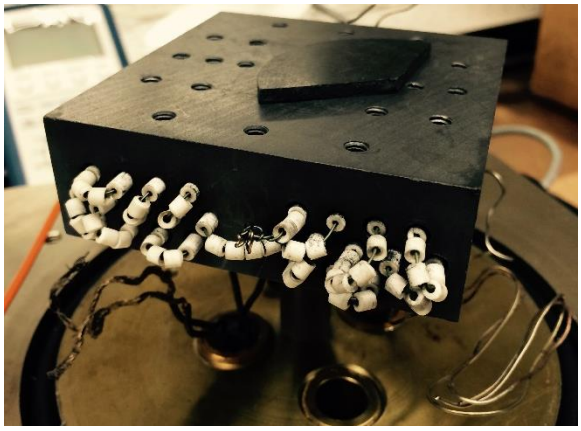

Fig. 2.2 Photo of the graphite heating platform

To achieve thermal isolation of the platform from the upper and base plates, a ceramic poster having relatively low thermal conductivity is utilized to support the platform. Once the chamber is pumped down, heat transfers to the upper and base plates from the platform through radiation mechanism only. Because the plates are constructed of stainless steel, being able to reflect and scatter radiation, the plates will not absorb much heat radiation and can keep cooled to low temperature with natural convection by ambient air. It is designed so that the platform is well

thermally isolated from the chamber enclosure that includes the cylinder wall and two steel plates. This is a unique feature of the furnace design. It allows for the platform to be heated to high temperatures while the temperature of the rest of the chamber remains relatively low, which is very important in the safety issue and the ability to seal the chamber in vacuum using O-rings. The upper plate is mounted with an ultra-Torr connector to take the small K-type thermocouple probe for measuring the sample temperature. The base plate contains four ports with National Pipe Thread (NPT). Two of these are occupied by feedthroughs. One feedthrough is for a pair of copper wires to pass into the chamber to connect to the two ends of the heating wire. The other is for thermocouple wires. The third port is used for the vacuum gauge, and the fourth port is for connecting to a mechanical pump. In this design, the chamber is allowed to pump down to 50 millitorrs and the maximum temperature of platform reaches up to 450ºC.

To conduct the reflow process in the vacuum chamber, the samples electroplated with solder layers are mounted in a graphite fixture and applied with a static pressure to ensure intimate contact. The assembly is then placed on the graphite platform. Once the vacuum furnace is pumped down and kept at 50 to 100 millitorrs to suppress oxidation during reflow, the temperature controller is turned on to heat up the platform. The reflow process is carried out at wide ranges of temperature and dwell time for different bonding systems. After reaching the peak temperature, the heater is turned off and the assembly is allowed to cool down naturally to room temperature in

a vacuum environment. Comparing to bonding in air, the amount of oxygen available to oxidize the molten solder is reduced by a factor of 15,200 in 50 millitorrs of vacuum.

2.3 Characterization Techniques

2.3.1 X-Ray Diffraction (XRD)

X-ray diffraction is used to identify the crystalline phases present in materials and to measure the structural properties, such as average grain size, crystallinity, lattice parameter, strain, and crystal defect, of multilayer films. X-ray diffraction peaks are produced by constructive interference of a monochromatic beam of x-rays scattered at specific angles from each lattice plane in a sample. An X-ray, generated by a cathode ray tube, is filtered to produce monochromatic radiation. These X-rays are then collimated to concentrate and direct the ray towards to the sample. The constructive interference happens when the interaction of incident rays and lattice plan satisfy Bragg's Law, $n\lambda = 2d\sin\theta$, where λ is the wavelength of electromagnetic radiation, d is the lattice spacing in the crystalline sample, and θ is the diffraction angle. The peak intensities are determined by the atomic arrangement within the lattice planes. These diffracted X-rays are then detected, processed and counted. Therefore, the X-ray diffraction pattern is the fingerprint of periodic atomic arrangements of a sample. By scanning the sample through a range of 2θ angles, all possible

diffraction directions of the lattice can be attained. In this study, it was applied to different materials and their results are presented as a plot of diffraction intensity corresponding to diffraction angles. Finally, to obtain these results, Rigaku SmartLab X-ray Diffractometer was used for X-ray diffraction analysis.

2.3.2 Scanning Electron Microscope (SEM)/Energy Dispersive X-ray Spectroscopy (EDX)

SEM is an electron microscope that uses focused beam of high energy electrons to image specimens. The high energy electrons interact with the atoms that make up the sample generating a variety of signals from the surface of the specimens. These signals, which includes secondary electrons (SE), back-scattered electrons (BSE), diffracted backscattered electrons (EBSD), characteristic X-rays, visible light (cathodoluminescence), specimen current, and transmitted electrons, reveal the specimens' surface topographies, chemical compositions, orientations, and crystalline structures. Fig. 2.3 displays the interaction volume and the signals produced by the interaction between electron beam and specimens [3]. The SE detector installed in the SEM captures the SE imaging high-resolution morphologies and topographies for the specimens' surfaces. Due to the very narrow electron beam, SEM micrographs have a large depth of field,

yielding a three-dimensional surface image of a specimen. BSE detectors may also be used in a SEM to illustrate contrasts in the composition of multiphase specimens. For instance, a stronger BSE intensity is detected if a larger number of backscattered electrons reaching to a BSE detector. Larger atoms, with a greater Z-number, have a higher probability of producing elastic collisions due to their larger cross-sectional area. Thus, elements with a greater atomic number (Z) show brighter images than smaller atomic number in BSE images. X-ray is also produced during the interaction of an electron beam with a specimen. The energy-dispersive detector is used to separate the characteristic x-rays of different elements into an energy spectrum. In addition, EDX software system is used to analyze the energy spectrum for determining the specific elements in the specimen. Energy dispersive X-ray spectroscopy can be used to find the chemical composition of materials in small area ($\sim 10^{-6}$ mm^2), and can create element composition mappings over this area. The spot size, defined as the diameter of the electron beam, depends on the density and atomic number of the interested elements and accelerating voltage. In this dissertation, Philips XL-30 FEG SEM was used.

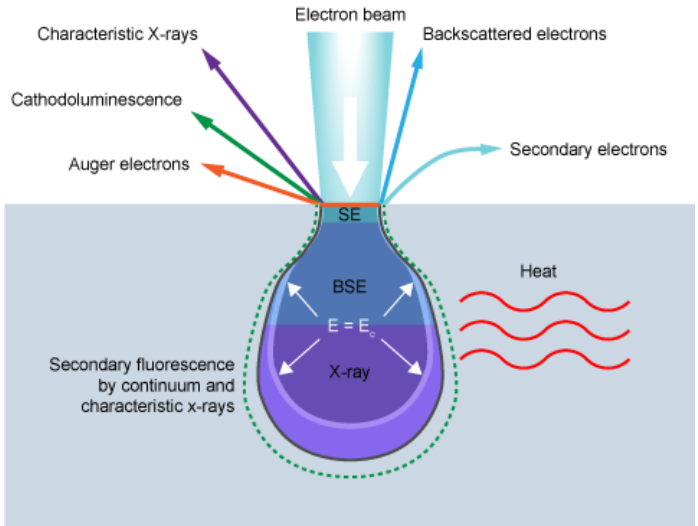

Fig. 2.3 The interaction volume and the signals produced by the interaction between the electron beam and specimen

2.4 References

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Chapter Three

Fluxless Bonding of Si chips to Aluminum Boards Using Electroplated Sn Solder

3.1 Introduction

Aluminum (Al) and its alloys have long been used in numerous products ranging from wrapping foils to airplanes. Al has the advantages of high thermal conductivity, high electrical conductivity, light weight, excellent resistance to corrosion, low cost, and ease of forging and machining. Despite all these advantages, its applications in electronic products have been limited to heatsinks [1-3] and casings. It has seldom been considered a substrate material to mount semiconductor chips and modules. There are two fundamental reasons: high coefficient of thermal expansion (CTE) and being unsolderable. Thus, the electronic industry has avoided its use as boards or substrates. The CTE mismatch between Si of 3 ppm/°C and Al of 23 ppm/°C is probably the highest among bonding pairs in electronic packaging. However, the use of Al is inevitable by virtue of its remarkable advantages as mentioned above. Al is extremely lightweight compared to other metals, making it the promising base material in manufacturing automobile and aircraft components and light-emitting diode (LED) lighting packages.

In this research, we set out to investigate techniques to surmount these two fundamental drawbacks and subsequently demonstrate the results that lead us to rethink aluminum and give aluminum another chance to perform. Our objective is to use Al as substrates or blocks to mount high power chips or modules using tin (Sn) without flux. An example of high power module is 100-watt LEDs assembled on a copper base that is attached to Al block for heat conduction. Present technique uses conductive adhesive to attach the module to the Al block [4-6]. The problem is that the adhesive has poor thermal conductivity. Another example is high power automobile module on alumina substrate that is attached to copper (Cu) base-plate for heat conduction. Using Al base-plate instead of Cu base-plate has advantages in reducing cost and weight and decreasing fuel consumption as well. The density of Al is only 30% of Cu. The price of Al is only 25% of Cu by weight and only 8% of Cu by volume.

In this research, we report preliminary results of fluxless bonding Si chips to Al substrates using Sn as the bonding medium. This work follows our previous works on other material systems [7-9]. After the samples were bonded, the quality and microstructure of the joints were examined using scanning electron microscopy (SEM) and the composition of the joints was studied with energy dispersive X-ray spectroscopy (EDX). The joint strength was examined by shear test. In what follows, we first present the experimental design and procedures. Experimental results are then reported and discussed. Finally, a short summary is given.

3.2 Experimental Design and Procedures

The soldering process used in electronic industries is a chemical reaction between metals which forms intermetallic compound (IMC) at the interfaces. It is believed that the IMC layer links the solder to the base metal. For Sn-containing solder on Cu, the IMCs are Cu_6Sn_5 and Cu_3Sn. Since Sn does not react with Al to form IMC, Al by itself is not solderable. The most popular method to make Al solderable is the zincation process, followed by electroless nickel plating and immersion gold deposition. The zincation process dissolves the surface aluminum oxide and deposits zinc (Zn) through electrochemical exchange reaction in alkaline zincate solution. Nonetheless, Zn deposition stops when the Al substrate is all covered with Zn. As a result, the zinc layer deposited is thin "20-50 nm" and multiple zincation operations are necessary for better surface uniformity and adhesion strength [10-12].

Instead of the zincation process, we developed an alternative technique to make Al solderable. Based on our experience and with the facilities available to us, we use electron beam evaporation to deposit Cr/Cu on Al for making it solderable. This process is easier to implement and can produce more reliability and reproducible results. Al substrates with 99% purity and dimensions of 20.6 mm × 25.4 mm × 1.7 mm (width × length × thickness) were sheared from Al 1100 sheet. They were thoroughly cleaned and slightly etched to remove surface oxide. Thin 100

nm Cr and 200 nm Cu layers were deposited on 6 mm × 6 mm area of the Al substrates in a high vacuum (2×10^{-6} torr) electron beam evaporation system. The Cr layer acts as an adhesion layer and the Cu layer prevents the Cr layer from oxidation. An additional 25 μm thick Cu was further electroplated in a pyrophosphate Cu plating bath at ambient temperature with current density of 30 mA/cm^2. Subsequently, a Sn layer of 85 μm thick was electroplated in a stannous bath under the condition of 43°C and pH of 1 with current density of 30 mA/cm^2. Silver (Ag) of 100 nm in thickness was then electroplated over Sn as capping layer to prevent Sn from oxidation. The Cr/Cu dual layer is employed as the interface layer between Sn solder and Al substrates.

Two-inch n-type Si wafers of 0.27 mm thick in (100) orientation were deposited with 30 nm Cr and 100 nm Au layers using electron beam evaporation. The Cr layer is an adhesion layer and the Au layer protects the Cr layer from oxidation when exposing to air. The wafers were then diced into 5 mm × 5 mm and 5 mm × 10 mm chips to be ready for bonding.

The first design is bonding a 5 mm × 5 mm Si chip on a 6 mm × 6 mm Al substrate on which 85 μm of Sn was plated. The desired Sn solder joint thickness is controlled by applying different static pressures throughout bonding process. The Si chip was placed face down on Al substrate whereby the pressure was applied on the backside of Si chip. The assembly was mounted on a heater graphite platform in a chamber. Static pressures selected are 0.6 psi (0.004 MPa), 2.5 psi (0.017 MPa), and 32 psi (0.221 MPa), respectively. The chamber was pumped down and kept

at 80 millitorrs to suppress oxidation and then the graphite platform was heated and temperature was monitored by a thermocouple during bonding process. The bonding process was conducted at 240°C with a dwell time of 3 minutes. The heater was then turned off and the assembly was allowed to cool down naturally to room temperature in vacuum environment. Later, an improved bonding process was developed to precisely control the solder joint thickness by integrating 50 μm thick Cu spacers between the Si chip and the Al substrate. Fig. 3.1 depicts the bonding structure and configuration using Cu spacers to control joint thickness. A 5 mm × 10 mm Si chip and Al substrate having 6 mm × 6 mm × 85 μm (width × length × thickness) Sn solder were held together and two 50 μm thick Cu shim spacers were inserted in between. A 70 g weight (4 psi) was exerted on the Si chip to ensure intimate contact. The assembly was then bonded using the same process aforementioned. In all processes, no flux was used.

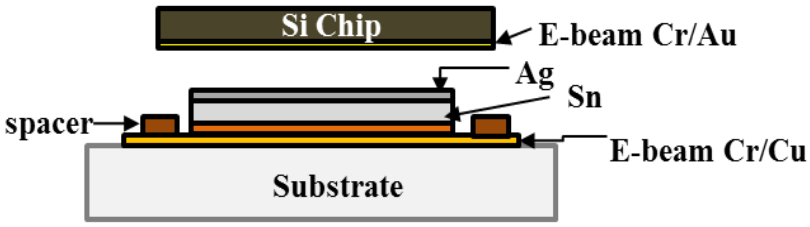


Fig. 3.1 Bonding structure and configuration of controlling joint thickness using Cu spacer

To evaluate the joint quality and to study the microstructure, the samples were mounted in epoxy resin, cut into halves, and polished properly for SEM cross-section image examination and

EDX composition analysis. Shear tests were implemented to measure the fracture force of the 6 samples bonded using the 50 μm thick Cu spacer.

3.3 Experimental results and discussion

3.3.1 Bonding design I

In the first design, different bonding pressures of 0.6 psi (0.004 MPa), 2.5 psi (0.017 MPa) and 32 psi (0.221 MPa) were employed to assess the fluxless bonding feasibility. The first assembly was bonded under 0.6 psi. Fig. 3.2 shows cross-section SEM images of a typical bonded portion. The upper interface between the silicon and the solder layer is sharp without any IMCs. The lower interface has two IMC layers as shown in Fig. 3.2(b).

Of these two IMC layers, the upper one (IMC1) exhibits scallop-shaped morphology. This type of morphology is favored by a high rate of free energy change [13-16]. Beneath IMC1 is another layer of thin IMC (IMC2). From EDX analysis data listed in Table 3.1, chemical compositions of IMC1 and IMC2 are Cu_6Sn_5 and Cu_3Sn, respectively.

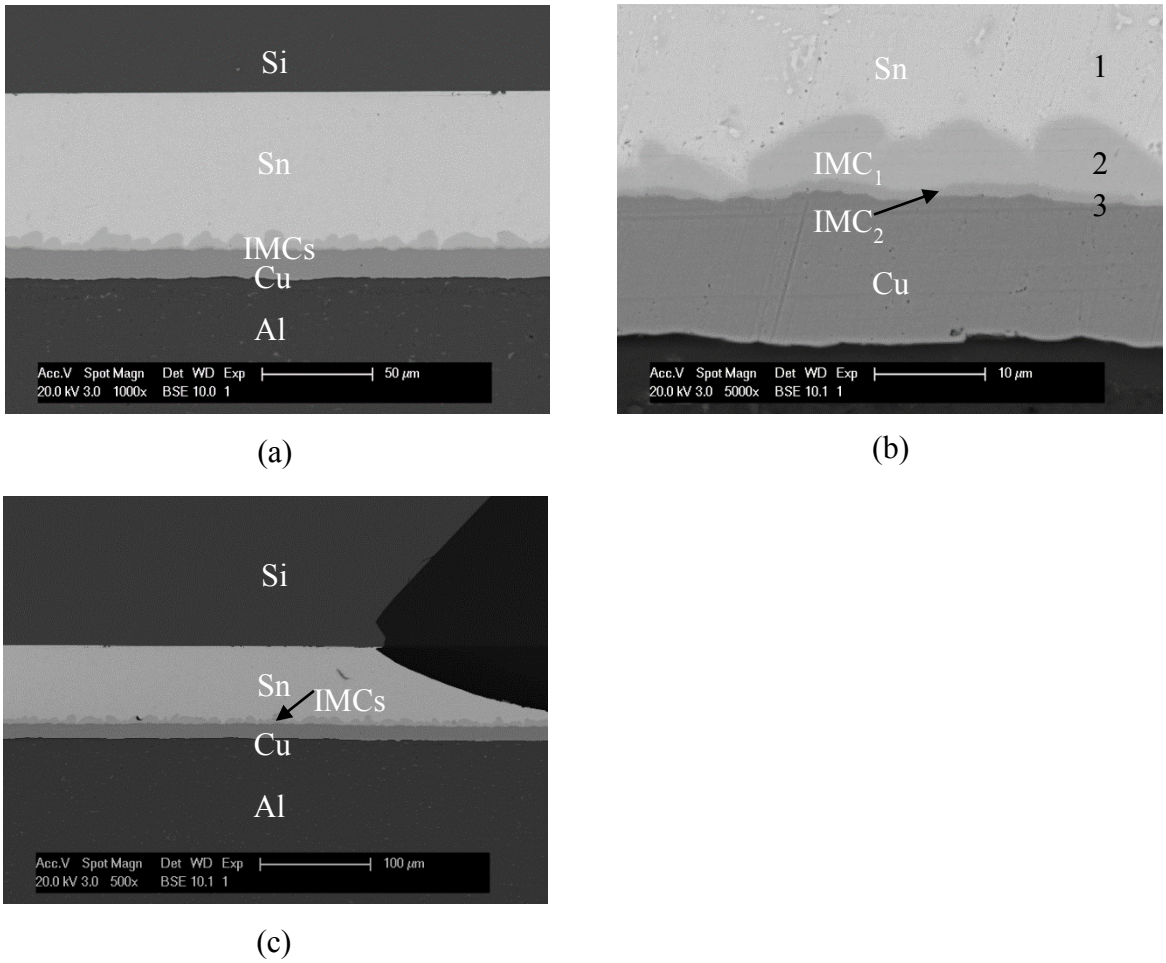


Fig. 3.2 Cross-section SEM images of the sample under bonding pressure of 0.6 psi at (a) low magnification (1000×), (b) high magnification (5000×) and (c) low magnification (500×), showing the joint on the edge

Table 3.1 EDX data of three regions marked as 1, 2 and 3 at the Sn/IMCs/Cu interface, as shown in Fig. 3.2(b)

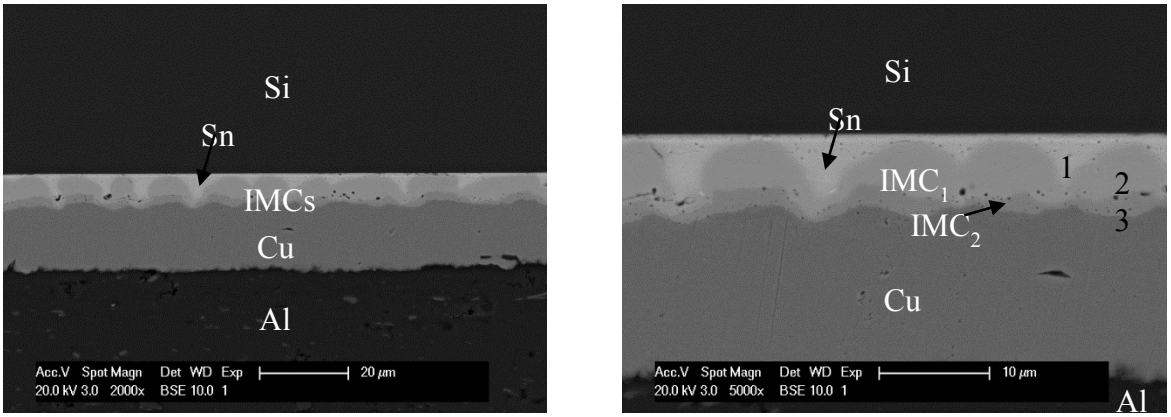
Region	Composition (atomic %)		Thickness
	Cu	Sn	(μm)
1	0	100	62-72
2	53.7	46.3	0-7
3	75.3	24.1	0-1

As can be seen in Fig. 3.2(a), the joint is quite uniform and is approximately 70 μm in thickness. When the Sn layer melts during bonding, the molten Sn wets the Cu on the Al substrate and Au on the Si chip very well. This could be seen in Fig. 3.2(c). Theoretically, the maximum stress-free shear strain is a commonly used indicator of possible breakage caused by CTE mismatch in a bilayer structure of different materials connected together by solder. In this model, it is assumed that both Si chip and Al substrate are free to contract during cooling down. This indicator is calculated by the equation [17],

$$\gamma = \frac{(\alpha_1 - \alpha_2)(T_2 - T_1)\frac{L}{2}}{h} \qquad (1)$$

where α_1 and α_2 are the CTE of silicon chip and aluminum, respectively, T_2 is the solidifying or the bonding temperature, T_1 is room temperature, L is diagonal length of the Si chip, h is the bonding layer thickness. Based on Eq. 1, the maximum stress-free shear strain for the Si-Al bonding pair with 70 μm Sn is calculated to be 26%. It is worth noting that "stress-free" means that the Si and Al are mechanically decoupled and no stress is induced. However, Si and Al are coupled once the solder solidifies. Thus, the stress-free strain is always higher than the actual strain.

This led us to reduce the Sn solder joint thickness by increasing the bonding pressure to 2.5 psi. On the cross section of the sample cut and polished as shown in Fig. 3.3, no voids are observed except a few Kirkendall voids near the Cu_6Sn_5 and Cu_3Sn IMC layers. Similarly, a scallop-shaped IMC layer and underlying thin IMC layer are observed. The EDX analysis results are listed in Table 3.2 and the EDX element mappings are displayed in Fig. 3.4.



(a) (b)

Fig. 3.3 Cross-section SEM images of the sample under bonding pressure of 2.5 psi at (a) low magnification (2000×) and (b) high magnification (5000×)

Table 3.2 EDX data of three regions marked as 1, 2 and 3 at the Si/Sn/IMCs/Cu interface shown in Fig. 3.3(b)

Region	Composition (atomic %)		Thickness
	Cu	Sn	(μm)
1	0	100	1-6
2	54.2	45.8	0-6
3	74.2	25.8	0-1

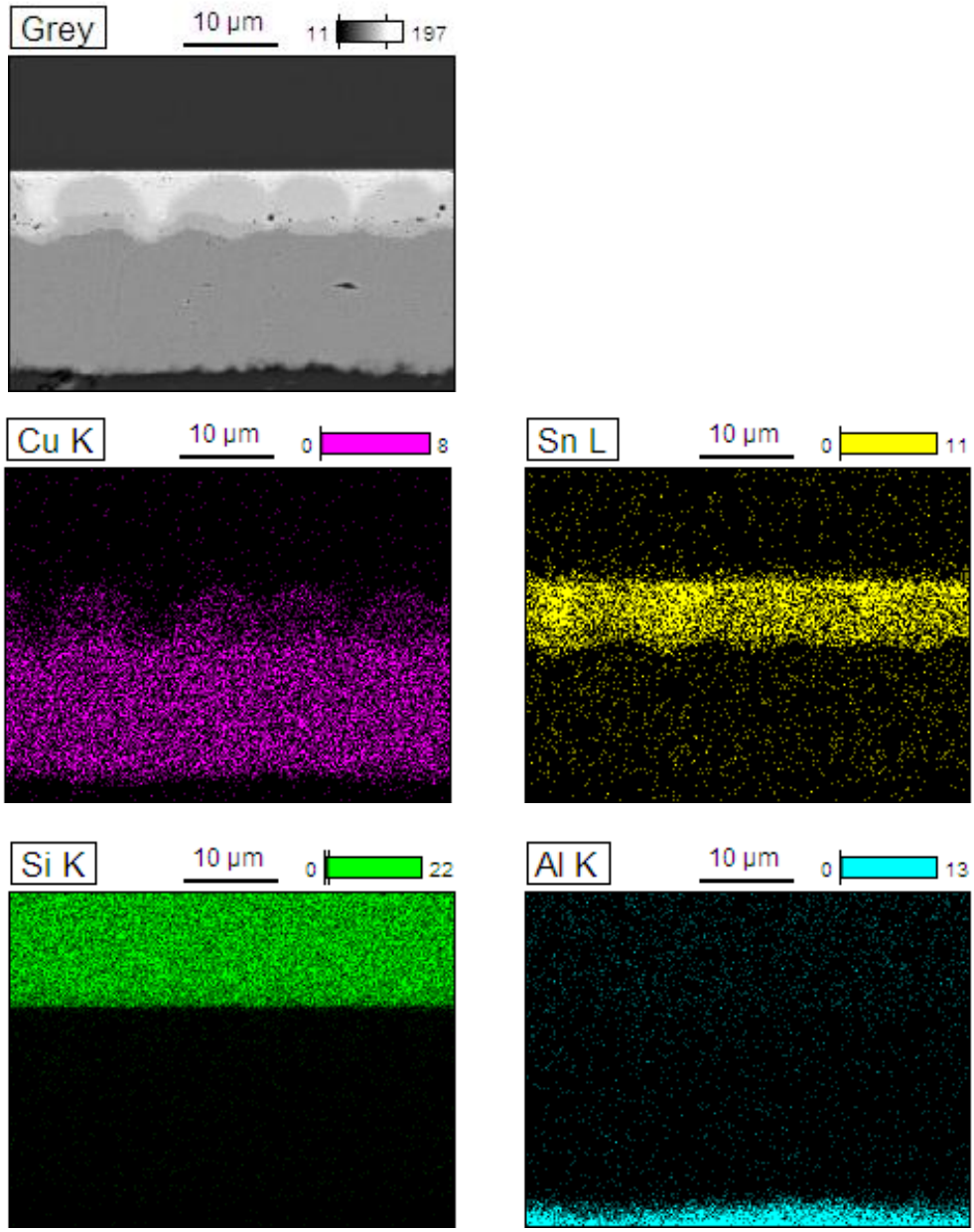
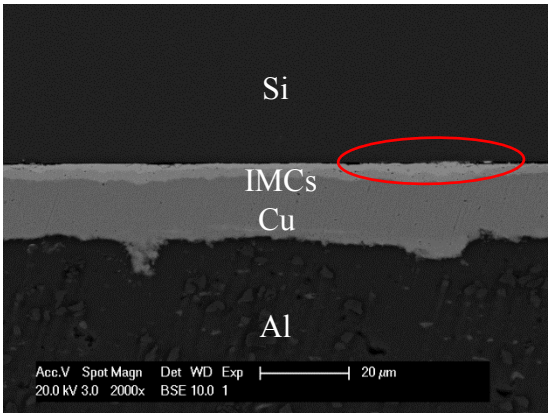


Fig. 3.4 EDX element mappings of the sample under bonding pressure of 2.5 psi

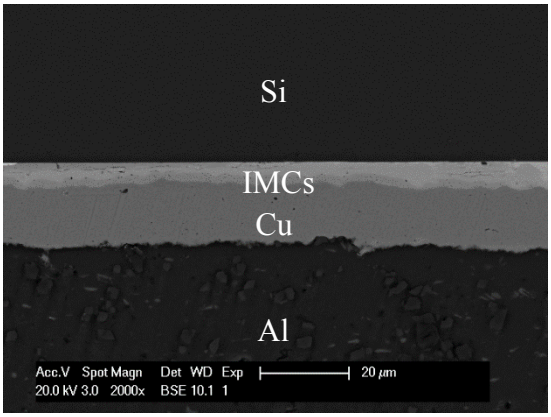
The compositions of the upper and lower IMC layers are determined as Cu_6Sn_5 and Cu_3Sn, respectively. The thickness of Sn layer in the joint is approximately 1 µm at the peaks of the scallop-shaped IMC layer and 6 µm at the grooves. The joint thickness including IMCs is about 7

μm. According to Eq. 1, the maximum stress-free shear strain is calculated to be 300%. In reality, the Si chip and Al substrate are mechanically coupled when the solder solidifies at 232°C. Below this temperature, stresses develop. We have, however, expected this bonded structure to break somewhere during cool down, but it did not. The Si chip is completely fine.

The bonding pressure was then increased to 32 psi. Fig. 3.5(a) shows the portion of the joint that was not well bonded, while Fig. 3.5(b) exhibits the well-bonded portion of the joint.



(a)



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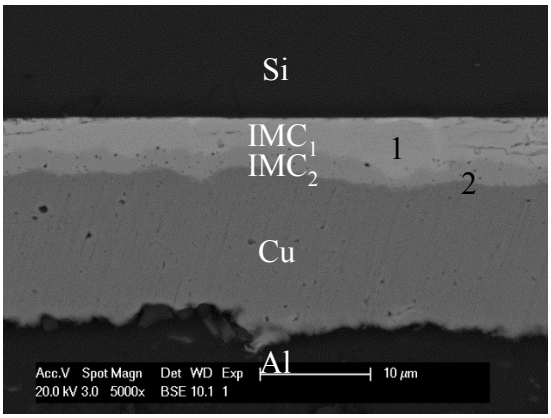


(c)

Fig. 3.5 Cross-section SEM images of the sample under bonding pressure of 32 psi at (a) low magnification (2000×) of the partially bonded region, (b) low magnification (2000×) of the well bonded region and (c) high magnification (5000×) of the well bonded region

Based on the EDX analysis results and the EDX element mappings as listed in Table 3.3 and shown in Fig. 3.6, respectively, it is found that, after solidification, almost no pure Sn was left in the joint. Sn was thoroughly consumed in forming IMC layers. The IMC joint thickness is only 5 μm. The bonded structure did not completely break or fracture. As a result, it is believed the joint and the bonding interfaces are strong enough to handle the large CTE mismatch between the Si chip and Al substrate.

Table 3.3 EDX data of two regions marked as 1 and 2 at the Si/IMCs/Cu interface shown in Fig. 3.5(c)

Region	Composition (atomic %)		Thickness
	Cu	Sn	(μm)
1	52.8	47.2	2-5
2	75.3	24.7	1-2

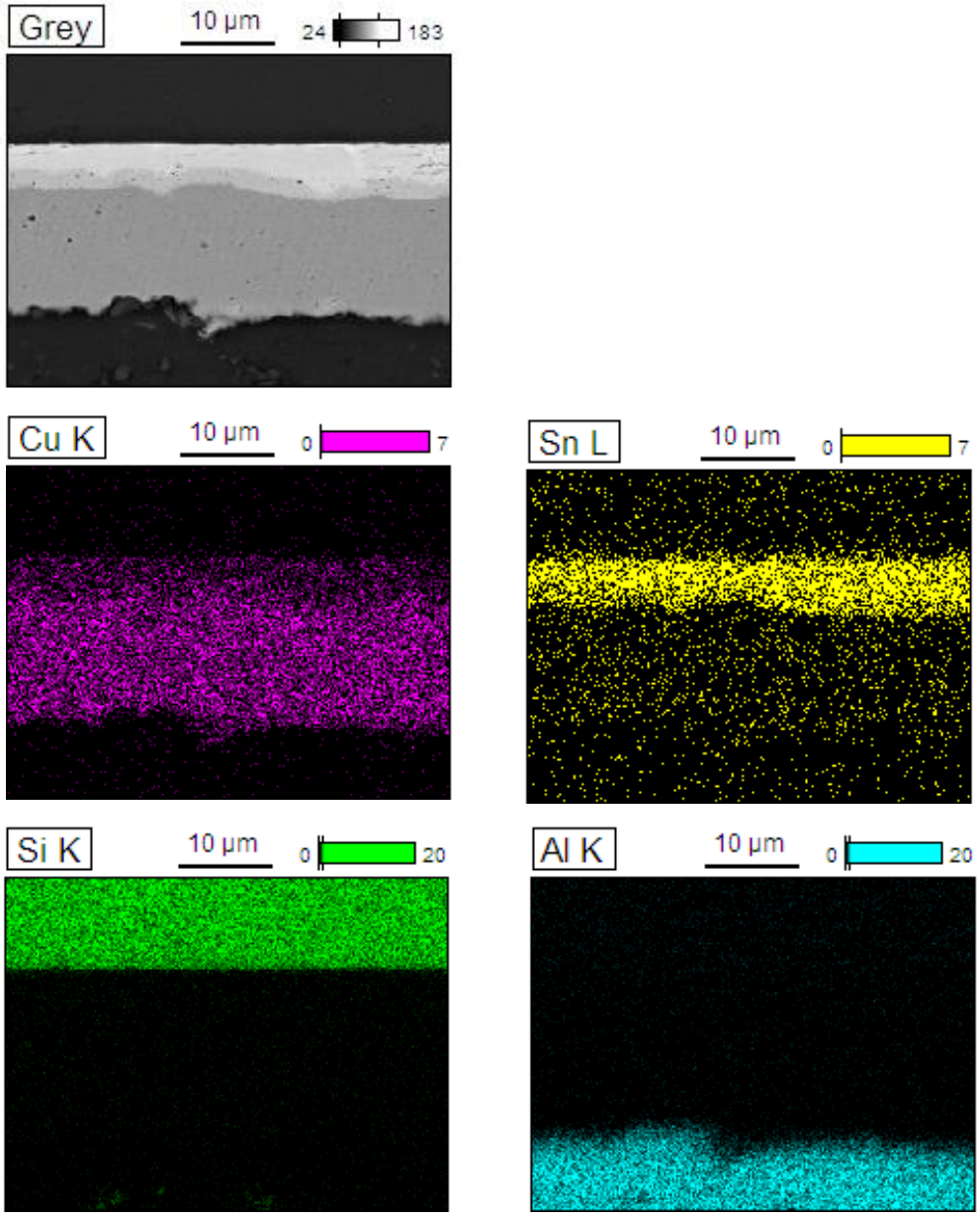
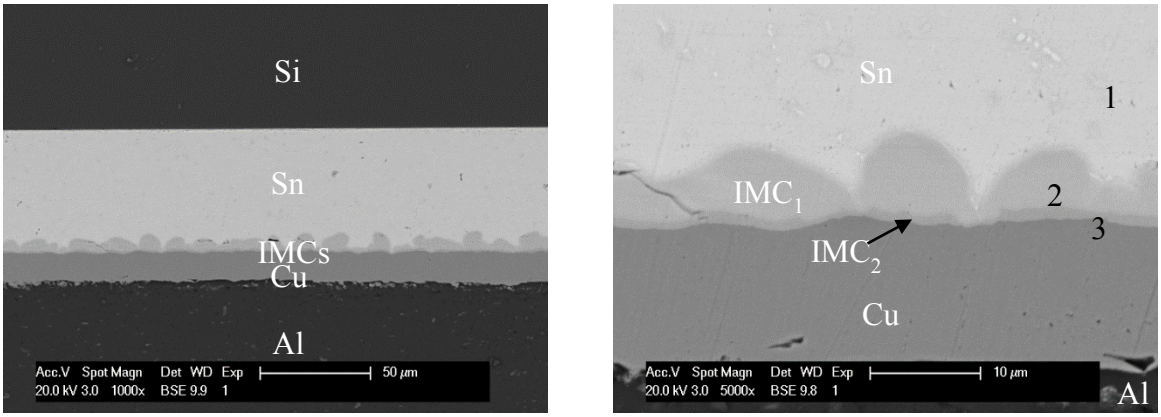


Fig. 3.6 EDX element mappings of the sample under bonding pressure of 32 psi

3.3.1 Bonding design II

In design I, the joints were strongly formed, proving that the fluxless bonding is achievable.

However, considering the practicality in packaging process, it is critical to maintain the reproducibility of our design. The fluidic nature of the molten Sn during bonding process makes the consistent control of joint thickness difficult. Uneven applying pressure in bonding process could make the Si chip incline toward an arbitrary direction, leading to various solder joint thicknesses of one sample. We have conceived a method for controlling the joint thickness precisely and easily by placing Cu shim spacers between the Si chip and the Al substrate. The cross-section SEM images of the bonded sample are displayed in Fig. 3.7.



(a) (b)

Fig. 3.7 Cross-section SEM images of the sample made with 50 μm Cu spacers at (a) low magnification (1000×) and (b) high magnification (5000×)

The sample was bonded perfectly. The upper interface between the silicon and the solder layer of this joint is even sharper than the joints in bonding design I. The nearly void-free result is attributed by the fluxless feature of this bonding process. If flux were used in attaching a chip of this size (5mm × 5mm), there would have been many voids in the joint because some molten flux

would be trapped there. The joint thickness of 50 μm is well controlled by the definite height of Cu spacers. The EDX analysis results are listed in Table 3.4.

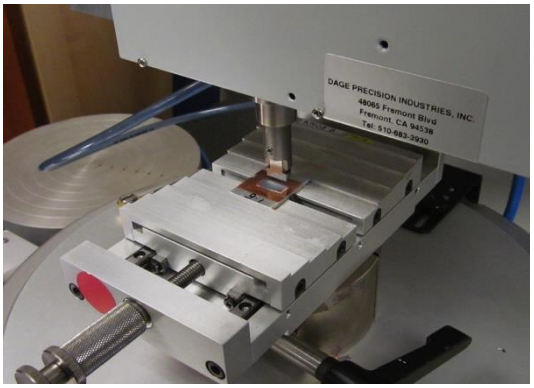
Table 3.4 EDX data of three regions marked as 1, 2 and 3 at the Sn/IMCs/Cu interface shown in Fig. 3.7(b)

Region	Composition (atomic %)		Thickness
	Cu	Sn	(μm)
1	0	100	50-53
2	52.7	42.3	0-7
3	75.7	24.3	0-1

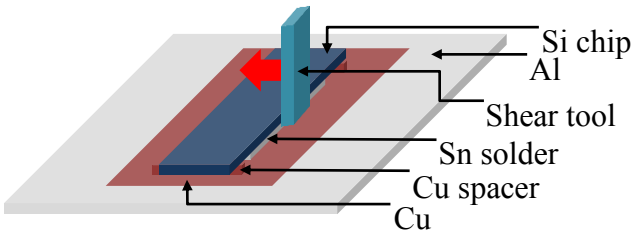
3.3.3 Shear test

Shear tests were performed on six samples bonded using 50 μm spacer. The samples were mounted on the stage, as shown in Fig. 3.8(a). A wedge tool pushed the edge of the Si chip under constant test speed of 350 μm/s. The measured fracture force of six samples ranges from 18.7 to 77.5 kg, as listed in Table 3.5. According to MIL-STD-883H method 2019.8, the minimum passing fracture force should be larger 5 kg for a 0.36 cm^2 bonding area. The fracture force of every sample far exceeds the passing requirement. The force versus displacement curve is displayed in Fig. 3.8(b). We wish to point out that the displacement is mainly caused by the shear tester. The tester does not have a sensor to measure the displacement caused by the sample. For samples 1, 3 and

6, the Si chip broke first. For the samples 2, 4 and 5, the whole Si chip was removed by the wedge tool. Fig. 3.9 displays EDX element mappings on the Al substrate of sample 5 after shear test. It is seen that the joint broke at two interfaces, some areas on Si/Sn interface and others on Sn/Cu6Sn5 interface. The joint did not break inside the Sn solder.



(a)



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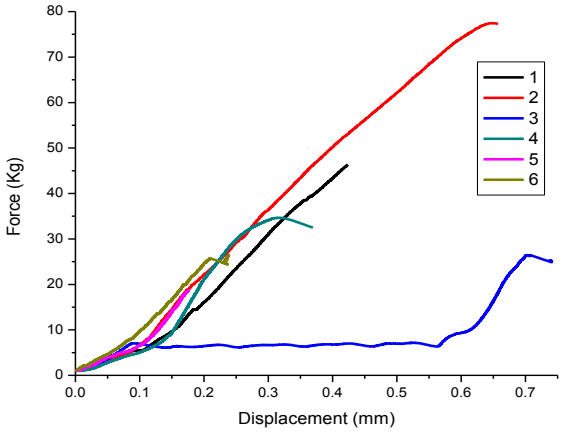
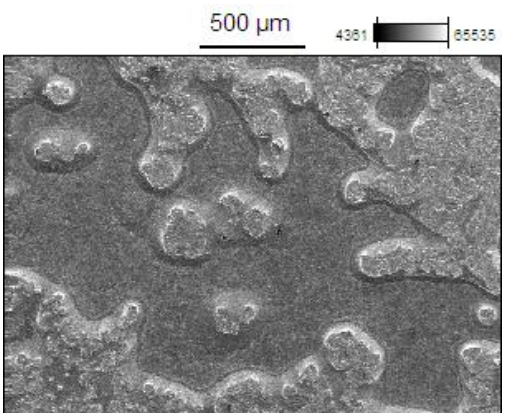


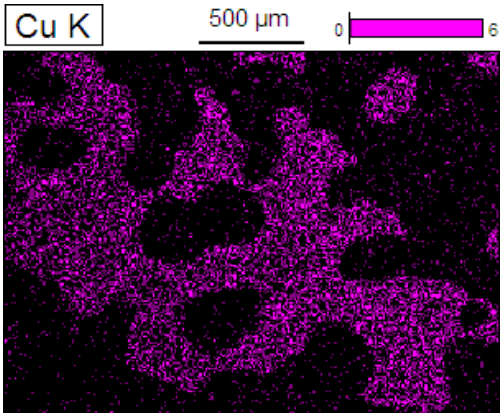
(c)

Fig. 3.8 Shear test: (a) shear tester, (b) schematic of test geometry, and (c) force versus displacement curves of six samples bonded using 50 μm spacer. The displacement is mainly caused by the shear tester. The tester does not have a sensor to measure the displacement caused by the sample

Table 3.5 Fracture forces, shear strengths and fracture modes of the six samples bonded using 50 μm spacer after the shear tests

Sample	Fracture force (Kg)	Shear Strength		Fracture mode and interface
		(MPa)	(psi)	
1	46.3	12.1	1750	Si chip broke
2	77.5	20.2	2927	Si/Sn interface
3	26.5	6.9	1001	Si chip broke
4	34.7	9.0	1309	Si/Sn interface
5	18.6	4.9	705	Si/Sn and Sn/IMC interfaces
6	26.5	6.9	1001	Si chip broke





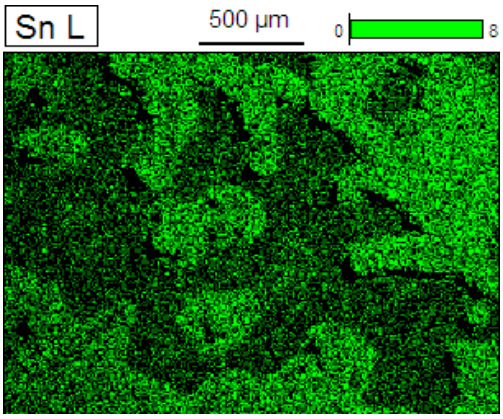


Fig. 3.9 A SEM image and EDX mappings on the Al substrate of sample 5 after fracture. On the SEM image, the light regions are Sn and the dark regions are Cu_6Sn_5. The joint broke on two interfaces: some regions on the Si/Sn interface and the rest on Sn/Cu_6Sn_5 interface. The joint did not break inside the Sn solder

3.4 Summary

In this study, a fluxless Sn process is developed to bond large Si chips to Al substrates. The Si chips are deposited with Cr/Au. The Al substrates are deposited with Cr/Cu and electroplated with thick Cu layer. A Sn layer is electroplated as the bonding medium and stress buffer to deal with large CTE mismatch between Si and Al. A thin Ag layer is placed over Sn layer to inhibit Sn oxidation. The bonding process is carried out in vacuum environment (80 millitorrs) to reduce Sn oxidation in molten phase. The resulting Sn joint thickness is controlled by bonding pressure or by utilizing Cu spacers. Cross-section SEM images indicate that high quality joints are fabricated and EDX analysis detects joint compositions. The joints bond to Cr layer deposited on Si chips without any IMC formation. They bond to Al substrates by forming IMC with Cu layers plated on Al. The bonding strength of the joint is strong as verified by measuring the fracture forces in standard shear test. This process has surmounted the challenge of large CTE mismatch between Si chips and Al substrates. Consequently, it is probably time for the electronic industry to reconsider

Al substrates in electronic assembly. This bonding process should be valuable in high power device packaging and automotive industry where lightweight is essential.

3.5 References

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Chapter Four

Fabrication of Insulated Metal Substrate (IMS) based on Anodization on Aluminum & Fluxless Bonding of Cu to IMS using Electroplated Tin Solder

4.1 Introduction

The most popular printed circuit board is constructed of epoxy-glass insulating board laminated with thin copper (Cu) foils on both sides where the circuits are built, as depicted in Fig. 4.1(a) [1]. The most widely used board material is known as FR4. However, as the industry has moved to lead-free soldering process, the use of higher melting point solders has driven the requirement of laminate materials with higher thermal stability. Laminates should be able to survive soldering temperatures that could be as high as 260°C. FR4 has glass transition temperature (T_g) of 140°C, making it inadequate in lead-free soldering process. Higher T_g materials have been developed. Examples of these laminates include those based on polyimides and liquid crystal polymers (LCPs), where the T_g could be as high as 280°C [2]. For high power circuit boards such as automotive power convertors, automotive power invertors, and microwave transmitters, the demand of thermal stability is even higher. The alumina substrate is therefore adopted as the board

material because of its excellent thermal stability and higher thermal conductivity than any of the polymer-based laminate materials. The maximum service temperature of alumina could be as high as 1500°C, while the polymer-based laminate

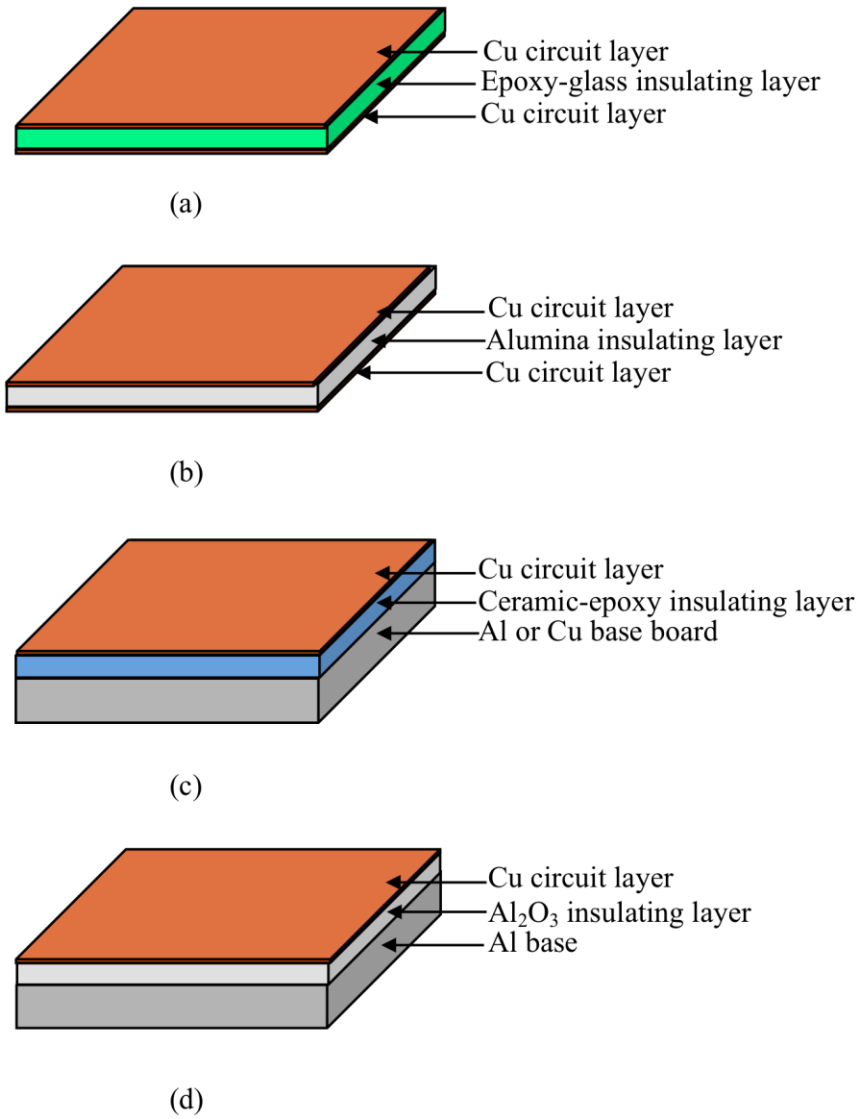


Fig. 4.1 Circuit board structures: (a) conventional printed circuit board (PCB), (b) Direct bonded Cu (DBC) board, (c) insulated metal substrate (IMS), and (d) Cu/alumina/Al board of this study

materials decompose at 500°C at most. The thermal conductivity of alumina is 30 W/m-K, but the highest thermal conductivity among the polymer-based laminate materials is only 0.95 W/m-K. In the commonly used structure, as portrayed in Fig. 4.1(b), the Cu sheets are bonded to the alumina by a direct-bonded Cu (DBC) process [3-4]. The DBC process involves a precisely controlled high-temperature oxidation process in the atmosphere of nitrogen containing about 1.4 mol% of oxygen, thus increasing the manufacturing cost. In general, the bottom Cu layer on the alumina substrate is soldered to a thick Cu heat spreader to dissipate heat. However, the alumina thickness is constrained to be not less than 0.25 mm due to mechanical reliability concern. Although the thermal conductivity of alumina is reasonably good, this results in significant thermal resistance for heat to conduct through the alumina and reach the Cu heat spreader. Another issue is the solder joint quality. For soldering large area alumina substrates, such as 20 mm × 20 mm, it is very difficult to achieve void-free joint. The solder joint adds additional thermal resistance. To increase heat conduction through the circuit board, insulated metal substrate (IMS) was developed [5-7], as shown in Fig. 4.1(c). It consists of aluminum (Al) or Cu base plate laminated with ceramic-epoxy and Cu foil. Ceramic fillers are added in order to increase the thermal conductivity [8-9]. This structure provides a thick base plate as heat spreader. However, it does not entirely solve the heat conduction problem because the ceramic-epoxy insulating layer has low thermal conductivity, 2-3 W/m-K. The trade-off between the performance and cost depends on the selection of filler types,

size, shape, etc., and the use of special wetting and dispersing agent. Thus, it is yet to find high volume applications due to the complexity in the fabrication process.

We have studied what have been done by the electronic industry in developing a circuit board structure for high power circuits over the last half century. It seems that no one has come up with an efficient structure. We thus investigated the fundamental requirements of an ideal structure. There are four requirements: highly conductive base plate, thin insulating layer with good thermal conductivity, Cu circuit layer, and high structure integrity. To meet these requirements, we began our structure design with Al as the base plate. Al has thermal conductivity of 237 W/m-K, close to 400 W/m-K of Cu. It is lightweight, corrosion resistant and low cost. It weighs only 30% of Cu and 35% of iron (Fe). It costs only 25% of Cu by weight [10] and only 7.5% of Cu by volume. It is easy to machine, cast, forge, shear, and roll. What's more important is that the thin Al_2O_3 insulating layer can be directly grown over Al base plate by anodization process, thus getting around the complicated manufacturing processes in DBC or IMS. Thin chromium (Cr) and Cu are then deposited, followed by Cu electroplating process to build up the Cu layer. Fig. 4.1(d) exhibits the resulting structure.

In what follows, experimental design and procedure is first reported. A concern of this structure is the high coefficient of thermal expansion (CTE) of Al, 23 ppm/°C. To ensure the structure integrity, several samples are fabricated and put through thermal cycling test and aging

test. The boards fabricated are cut in cross section, polished and evaluated by scanning electron microscopy (SEM) with energy dispersive X-ray spectroscopy (EDX). To demonstrate application of this structure, 10 mm × 12 mm Cu substrates are bonded to $Al/Al_2O_3/Cr/Cu$ boards using tin without any flux. The quality and microstructure of the joints are examined using SEM and EDX. The experimental results are presented and discussed. A summary is given.

4.2 Experimental Design and Procedures

The dielectric strength of alumina is 13.4 V/μm, which is low compared to 470-670 V/μm of SiO_2 [11]. Reason for this large difference in dielectric strength has never been explained in any literatures. To sustain 500 volts, the alumina thickness has to be at least 37 μm. A standard technique to grow thick alumina on Al is anodization. There are two basic anodization processes, porous-type and barrier-type, both of which are well-established [12-15]. The first process produces porous alumina. The pores allow the anodizing electrolyte to penetrate into the alumina for continuing growth. The alumina thickness ranges from a few μm to several hundred μm [16]. The pores make the alumina layer electrically conducting. In the industry, the pores are plugged by hydrated aluminum oxide, boehmite, which is formed in hot water at temperature range of 96-100°C [16]. In this project, high purity Al_2O_3 is needed and the use of sealant is not an option. We

then turned to the barrier-type process. It grows alumina without pores. However, the thickness is limited to several micrometers [16]. Numerous experiment runs were performed to grow alumina layer thicker than 5μm that is insulating, but without success. We finally came up with a two-step anodization technique that works well and forms high quality alumina, as illustrated on the process flow chart in Fig. 4.2. The first step grows thick alumina with pores by using sulfuric acid electrolyte. The second step seals the pores with alumina by using boric acid electrolyte.

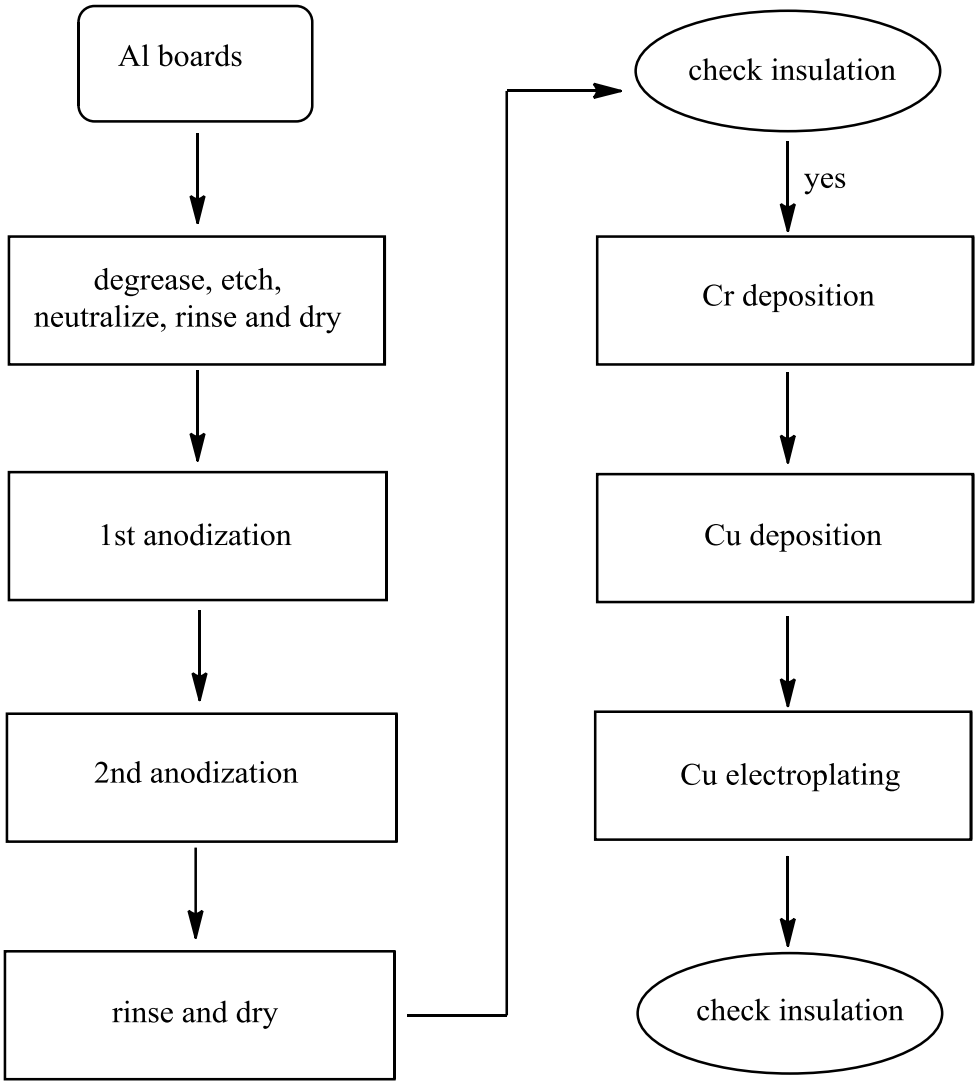


Fig. 4.2 Process flow chart of the board fabrication

Al 1100 (International Alloy Designation System) boards of 20.6 mm × 25.4 mm × 1.7 mm are degreased in acetone, etched in 1 M NaOH, neutralized in 1 M HNO_3, rinsed in deionized water, and dried by compressed air. After the two-step anodization process, the samples are rinsed in deionized water and dried with compressed air.

Before metallization with Cu, we have to make sure that the alumina layer is insulating. An Al foil is pressed over the anodized alumina layer and the resistance between the Al foil and the bottom side of the Al board is measured, as shown in Fig. 4.3(a). If the result shows that the alumina layer offers proper insulation, the sample is then metallized to form a Cu layer in the next step of the process. However, many samples made in our early process development phase seemed insulating when tested with aluminum foil but turned conducting upon Cu-metallization. It is thought that the conducting paths go through the pores in alumina, where the Al foil does not get to, but Cu does during deposition as illustrated in Fig. 4.3(b). In other words, during the metallization process, Cu gets into the pores in the alumina and shorts the alumina layer. We thus design a new measurement method to examine the insulation before Cu metallization, as portrayed in Fig. 4.3(c). Instead of Al foil, the anodized alumina is covered with saline water. If there are pores in anodized alumina, saline water will penetrate into the pores and reduce the electrical

insulation. The two-step anodization process was established according to this test method. All the samples made with the two-step anodization process could be perfectly insulating after Cu-metallization.

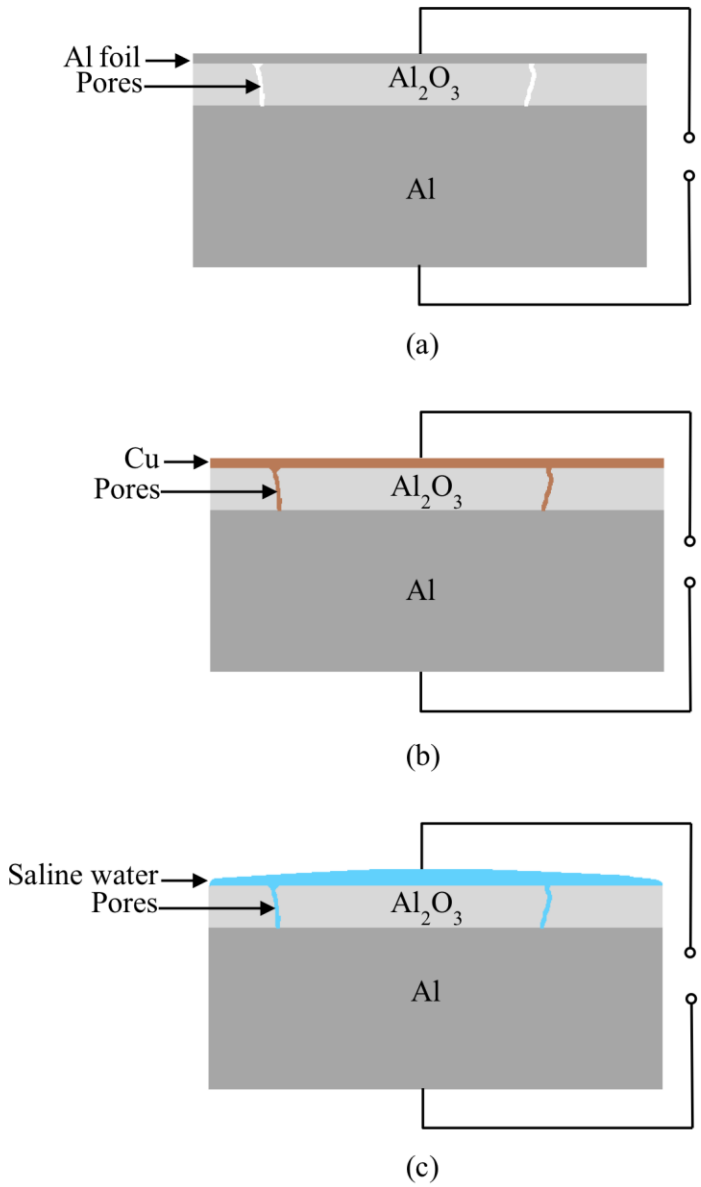


Fig. 4.3 Structures used during the development of Al circuit boards

The next step is to coat the alumina with Cu. We searched the literature extensively and could not find any established technique. The direct Cu bonding process is not applicable because it needs high temperature of 1067°C [3-4]. E-beam evaporation is another way to deposit metals on substrates. However, Cu does not adhere well on alumina, peeling off after deposition or during later handling. Cr is then used as the adhesion layer since it bonds to alumina and to Cu well. So, we tried our own process. Thin Cr (100 nm) and Cu (200 nm) layers are deposited sequentially on anodized Al boards in a high vacuum (2×10^{-6} torr) E-beam evaporation system. Here, Cr is expected to bond strongly to alumina and Cu protects the Cr from oxidation. Afterwards, 25 μm thick Cu is electroplated in a pyrophosphate Cu plating bath at ambient temperature with current density 30 mA/cm^2.

To test the alumina insulation, electrical resistance is measured between the Cu layer and bottom side of the Al board using a high precision digital multimeter. The breakdown voltage is measured by an adjustable high voltage DC power supply. Our concern on possible failure of the structure comes from the CTE mismatch among Cu, alumina and aluminum. They are 17 ppm/°C, 7 ppm/°C and 23 ppm/°C respectively. Despite the mismatch, no samples ever broke after fabrication. Still, we want to make sure that they do not break in applications. Accordingly, 13 samples are fabricated and put through thermal cycling test between -40 and +85 ºC. Furthermore, some samples are aged at 250°C for 10 hours and 100 hours, respectively.

To demonstrate that components can be attached to resulting Al boards, 10 mm × 12 mm Cu substrates are bonded using fluxless tin (Sn) process. Sn of 60 μm in thickness is electroplated in a stannous bath under the condition of 43°C and pH of 1 with current density of 30 mA/cm^2, followed by plating 100nm Ag capping layer. The Cu substrate are degreased with acetone and rinsed in deionized water. The Cu substrate is placed over the Al_2O_3/Cr/Cu board and held with 32 psi (0.22 MPa) of static pressure. The assembly is mounted on a graphite platform in a vacuum chamber pumped down and kept at 80 millitorrs. The graphite platform is then heated and the temperature of the sample is monitored by a thermocouple during the bonding process. The bonding temperature is 240°C with a dwell time of 3-5 minutes. The heater is then turned off and the assembly is allowed to cool down naturally to room temperature in vacuum environment. To assess the structural integrity of Al boards, samples are mounted in epoxy resin, cut into halves, and polished for examination using SEM and EDX. Samples of Cu bonded to Al board are also studied by SEM for joint microstructure evaluation and EDX for composition analysis.

4.3 Experimental results and discussion

After the anodization process, the electrical resistance of the sample was measured using the setup shown in Fig. 4.4. Table 4.1 presents resistance values during the process development

phase. The area of alumina layer on the Al boards is 20 mm × 20 mm. Using a two-step process, the measured resistance is higher than 40 MΩ which is the upper limit of the digital multimeter. The process was adjusted until 40 MΩ or higher resistance was achieved consistently. Cr and Cu were deposited over the alumina layer on the Al board. The electrical insulation was verified again.

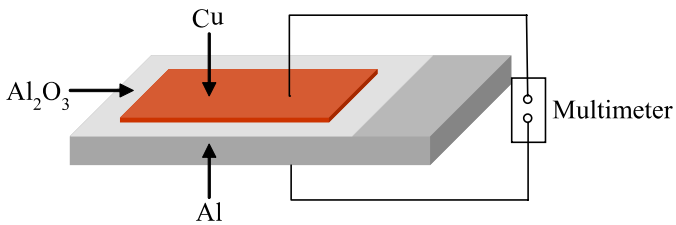


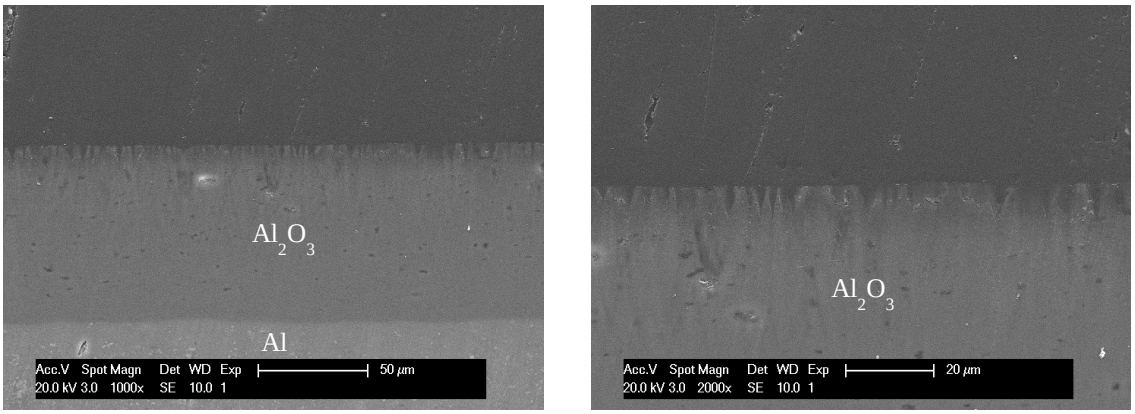
Fig. 4.4 Experimental setup to measure the electrical resistance of alumina layer grown on Al base

Table 4.1 Measured resistance of alumina layers grown by various anodization processes and electrolytes on Al boards. The area of alumina layer is 20 mm × 20 mm

Anodization and electrolytes	**Measured resistance**
one-step: tartaric acid	0.8 - 1.5 Ω
one-step: boric acid	1.5 - 3.5 kΩ
one-step: sulfuric acid	5.0 - 8.0 MΩ
two-step: sulfuric acid and boric acid	> 40 MΩ*

* Limit of the digital multimeter

Fig. 4.5(a) and (b) exhibit cross-section SEM images of a typical sample after the first anodization step. The alumina layer thickness is 80 μm. It was a challenge to polish an SEM sample that shows the pores. Fig. 4.5(b) does expose the pores clearly.



(a) (b)

Fig. 4.5 Cross-section SEM images of alumina layer after the first anodization step: (a) 1000× magnification, and (b) 2000× magnification. The alumina layer is 80 µm thick and pores are clearly seen in (b)

Figs. 4.6(a) and (b) exhibits the SEM image after the second anodization step. The thickness of the alumina reduces to 50µm and no pores are observed. The electrical resistance is higher than 40 MΩ. The mechanism for the anodization step is still being investigated. The breakdown voltage of the alumina layer was measured. It can withstand 600 VDC. The measured dielectric strength is 600 V / 50 µm = 12 V/µm, close to 13.4 V/µm reported of pure alumina substrate [7].

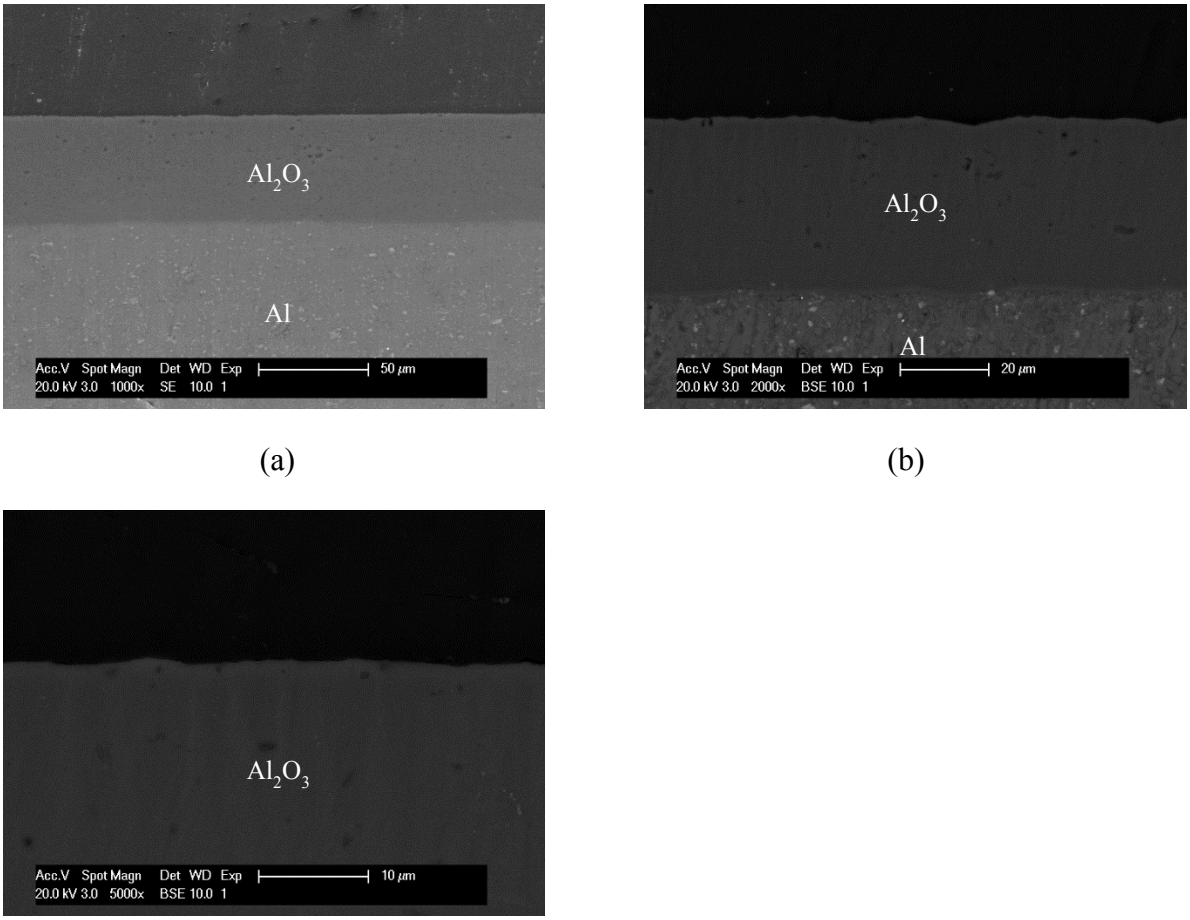
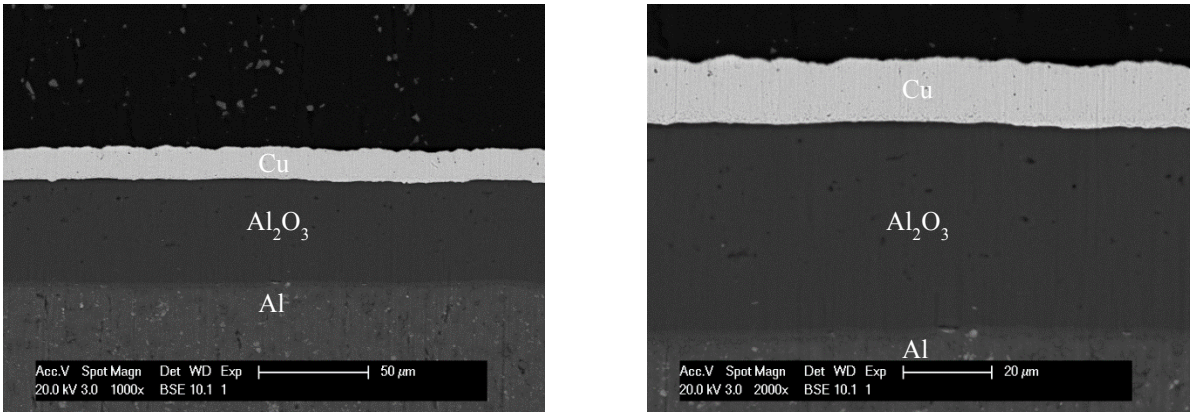


Fig. 4.6 Cross-section SEM image of alumina grown using the two-step anodization process: (a) 1000× magnification, (b) 2000× magnification and (c) 5000× magnification. The alumina layer is 50 µm thick and free of pores

To test the integrity of the board structure, 13 samples were put through thermal cycling test between -40 and +85°C. A sample was randomly selected after 500 cycles and evaluated. Fig. 4.7 displays the cross-section SEM images. The Al/Al_2O_3 interface and $Al_2O_3/Cr/Cu$ interface

remain sharp without any voids or cracks. The 50 μm thick Al_2O_3 layer shows no cracks, no pores, and no voids.



(a) (b)

Fig. 4.7 Cross-section SEM images of an Al circuit board after test of 500 thermal cycles between -40 and +85°C: (a) 1000× magnification, and (b) 2000× magnification. There is no visible change after the thermal cycling test

Several samples were subjected to high temperature storage at 250°C for 10 hours and 100 hours. Fig. 4.8 shows the cross section SEM images of two samples stored at 250°C for 10 hours and 100 hours. No defects were detected. Despite the significant CTE mismatch among Cu, alumina, and aluminum, the Al circuit boards survived the thermal cycling test and 250°C storage test without any degradation.

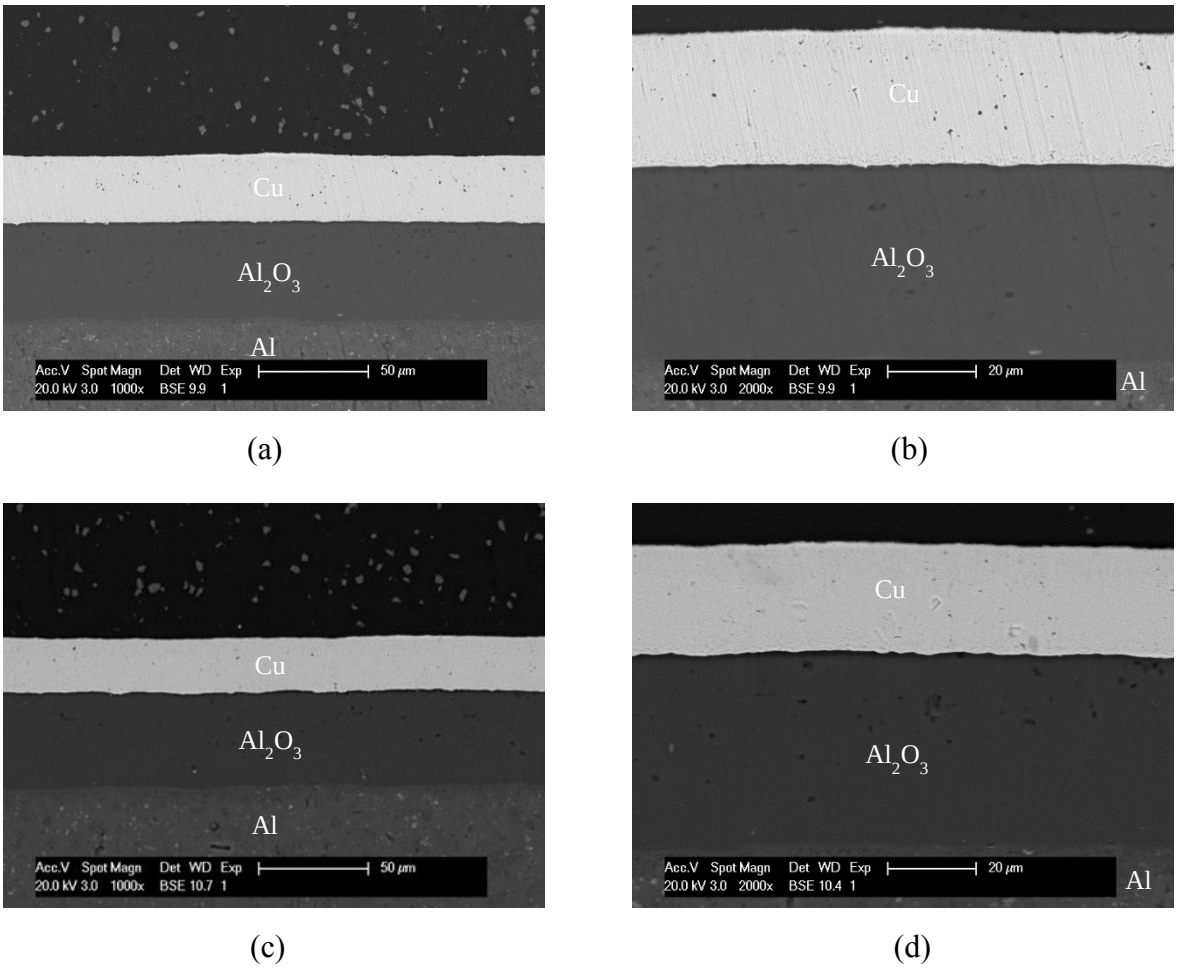
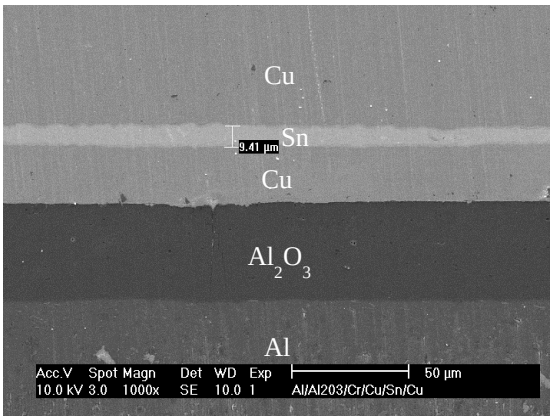


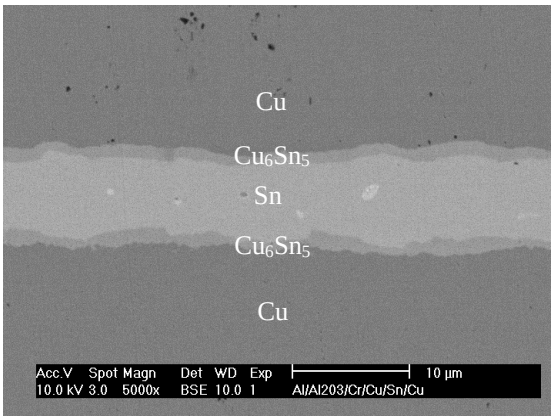
Fig. 4.8 Cross-section SEM images of Al circuit boards after storage at 250°C for 10 hours: (a) 1000× magnification, and (b) 2000× magnification and 100 hours: (c) 1000× magnification, and (d) 2000× magnification, respectively. There is no visible change after the high temperature storage test

To demonstrate that the Al circuit boards can sustain soldering operations, 10 mm × 12 mm Cu substrates were attached to Cu side of the boards using fluxless Sn bonding technique [17]. 60 µm thick Sn was plated on the Cu side of the board, followed by capping with 100nm Ag layer to prevent Sn from oxidation. The Cu substrate was placed over the Sn solder and held with 32 psi (0.22 MPa) static pressure. The assembly was then mounted on a graphite platform in a vacuum

chamber which was pumped and kept at 80 millitorrs to suppress oxidation. The graphite platform was heated and the temperature of the sample was monitored by a thermocouple during the bonding process. The bonding temperature was 240°C with a dwell time of 3-5 minutes. The heater was turned off and the assembly was allowed to cool naturally to room temperature in vacuum environment. Most of the Sn was squeezed out because of the 32 psi pressure applied. Shear strengths of the solder joints were not measured, but the Cu substrate could not be pushed off by a hand tool. Fig. 4.9 shows the cross-section SEM images of a typical sample. The joint exhibits high quality without any cracks, defects, or voids. The Sn joint bonds well to the Cu substrate and to the Cu layer on the Al board. Intermetallic compound (IMC) Cu_6Sn_5 is formed on Sn-Cu interfaces. The solder joint including the IMC layers is only 9.4 μm in thickness.



(a)



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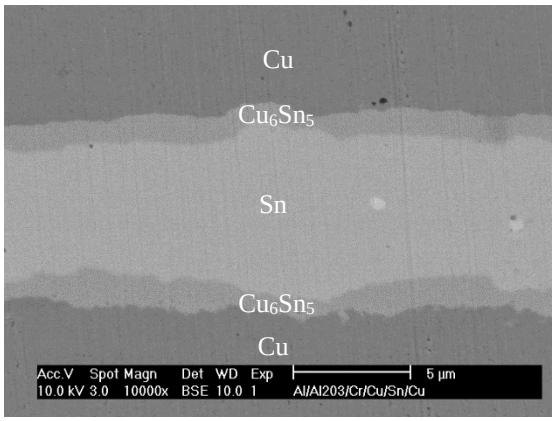

(c)

Fig. 4.9 Cross-section SEM images of Cu substrate bonded to an Al circuit board using fluxless tin at 240°C. The joint thickness is 9.4 µm including Cu_6Sn_5 layers. The Cu substrate is 10 mm × 12 mm in size

The Al boards have 50 µm alumina and 25 µm Cu. Since both the alumina and Cu are much thinner than the Al base thickness of 1700 µm, we can approximate the CTE of the board to be the same as Al. The CTE mismatch between the Cu substrate and Al board is then 17 ppm/°C versus 23 ppm/°C. A commonly used indicator on the severity of CTE mismatch of bonded structures is the maximum stress-free shear strain calculated assuming that the Cu substrate and the Al board are free to contract or expand [18],

$$\gamma = \frac{(\alpha_1 - \alpha_2)(T_2 - T_1)\frac{L}{2}}{h} \qquad (1)$$

where α_1 and α_2 are the CTE of Al and Cu, respectively, T_2 is the solder solidifying temperature, T_1 is the room temperature, L is the diagonal of the Cu substrate, and h is the bonding layer thickness. The maximum stress-free shear strain calculated is 120%. This is much higher than that of typical solder joints, at most 30%. We actually expected the bonded structures to break during

cooling down. But they all survived without any cracks.

4.4 Summary

Aluminum has thermal conductivity of 237 W/m-K, close to 400 W/m-K of Cu. It is lightweight, corrosion resistance and low cost. It weighs only 30% of Cu and 35% of Fe. It costs only 25% of Cu by weight and 7.5% of Cu by volume. It is easy to machine, cast, forge, shear, and roll. Two challenges of using Al as circuit board material are the growth of insulating layer and its high CTE. In this research, thin Al_2O_3 layer was grown on Al boards by a two-step anodization process to achieve high electrical insulation. Thin Cr and Cu were then deposited over the alumina layer, followed by Cu electroplating process to build the Cu layer to 25 µm. The alumina layer is as thick as 50 µm. The electricity resistivity measured is higher than 3.2×10^{10} Ω-cm, limited by the instrument. Thermal cycling test of 500 cycles between -40 to +85°C and 250°C storage test for 100 hours show no effects on the structural integrity and the electrical properties of the Al boards. To evaluate soldering operations on the Al boards, Cu substrates were bonded to the Cu side of the boards using a fluxless Sn process. High quality Sn joint with Cu_6Sn_5 on the Sn-Cu interface was achieved. Despite significant CTE mismatch between the Cu substrate and the Al board, no breakage and cracks are observed. This aluminum circuit board (ACB) technology

should open up applications where efficient heat transport from the circuit components to the base of the boards is essential. Application examples include high power light-emitting diode (LED) modules, automobile convertors and invertors, microwave transmitters and space electronics.

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Chapter Five

Fluxless Sn bonding of silicon chips to low carbon steel substrates using nickel under-bump metallurgy

5.1 Introduction

Ferrous metals are widely used for various applications in automotive and electronic packaging industries. For example, Invar alloy (Fe-36Ni) noted for its uniquely low coefficient of thermal expansion (CTE) around 0.8 to 1.6 ppm/°C has been utilized in manufacturing precision instruments where high dimensional stability is required. Alloy 42 (Fe-42Ni) and Kovar (Fe-29Ni-17Co) are controlled expansion alloys with CTE of 4.0 to 4.7 ppm/°C and 5.1 to 5.5 ppm/°C, respectively [1-2]. These controlled expansion alloys have been employed as lead-frame of plastic packages and headers of transistor because their CTE are close to that of silicon (3 ppm/°C) and lead-sealing glass. But one disadvantage of these alloys is the relatively low thermal conductivity (10-17 W/m-K) [3].

We thus searched for ferrous metals that have higher thermal conductivity and low CTE for electronic packaging applications. After a thorough research, AISI 1018 low carbon steel (Fe)

was selected for study. It has thermal conductivity of 51.9 W/m-K and CTE of 11.5 ppm/°C [4]. It also has very high tensile strength (635-696 MPa) and high melting point (1450-1540°C).

A challenge of using low carbon steel is that it rusts easily and its oxides are dissolvable in water. Thus, it corrodes. In this research, we use Ni as the underbump metallurgy (UBM) to treat the low carbon steel so that it is not only corrosion resistant but also solderable. Ni was chosen because Ni is thought to have slower rate of reaction with Sn [5-7]. To demonstrate its soldering quality, Si chips are bonded to the Fe substrates using Sn without any flux. The reactions during the bonding process are examined using scanning electron microscope (SEM) and energy dispersive X-ray (EDX). The reaction mechanism is suggested and the reaction rate is analyzed. The Sn portion of solder joint is chemically etched away to expose the IMC for analysis. In what follows, experimental design and procedures are first presented. Experimental results are reported and discussed. A summary is then given.

5.2 Experimental Design and Procedures

Among popular surface treatment methods on iron such as hot enamel coating, hot-dip zinc coating, PVD hard coating, CVD hard coating or electrochemical deposition [8], Ni plating was chosen because it not only can prevent corrosion but also make the surface solderable. Basically,

there are electroless nickel-phosphorus (Ni-P) plating process and electrolytic Ni plating process. Electroless Ni-P process was not chosen for this project because of formation of crystalline Ni_3P compound at the solder-Ni interface, which tends to weaken the solder joints [9-11]. Instead, Wood's nickel strike electroplating process was selected [12]. Substrates of 15 mm×13 mm×3.3 mm (width×length×thickness) were cut from AISI 1018 low carbon steel (Fe) sheet. They were ground using 800 and 1200 grit SiC-coated papers to smooth out the surface. They were cleaned with acetone and deionized water before electroplating. 1.5 µm Ni was plated on the Fe substrates with Wood's nickel strike followed by plating 70 µm thick of Sn solder layer in a stannous bath. In another design, the Ni thickness was increased to 4.5 µm. To produce the Si chips, two-inch n-type Si wafers in (100) orientation were deposited with 30 nm Cr and 100 nm Au layers using E-beam evaporation. The Cr layer is an adhesion layer and the Au layer is the capping layer that protects the Cr layer from oxidation when exposing to air. During the bonding process, the Au layer is completely dissolved in the molten Sn which then contacts the fresh Cr layer. The resulting Sn joint would contain only 0.23 at.% Au. The wafers were diced into 5 mm×10 mm chips ready for bonding. The Si chip and Fe substrate were held together with two 50 µm thick Cu spacers placed in between. The assembly was mounted on a heater graphite platform in a chamber with a 16 psi pressure applied on the Si chip to ensure intimate contact. The chamber was pumped down to 80 millitorrs and the graphite platform was then heated. The bonding process was conducted at

240°C with reflow time of 200 seconds or 300 seconds to see how the intermetallic compound (IMC) would grow. After bonding, the heater was turned off and the assembly was allowed to cool down naturally to room temperature in vacuum environment. The samples were mounted in epoxy, sectioned using slow speed diamond saw, ground with 800 and 1200 grit SiC paper and polished with alumina suspension solution for microstructure and composition examination. Some samples were etched with 12.5 vol% HCl + 87.5 vol% methanol solution to selectively etch Sn away to reveal the three-dimensional morphology of the IMCs at the interface. The microstructures were examined by SEM equipped with a back-scattered electron (BSE) image detector. The chemical compositions were analyzed using EDX spectroscopy. To determine the average thickness of the IMC layer, the area of the IMC layer was first estimated using image processing software. The average thickness was then determined by dividing the area of the IMC layer by the total length of the interface from the cross-section SEM micrographs. Table 5.1 lists five samples designed and made with different Ni thicknesses and reflow times.

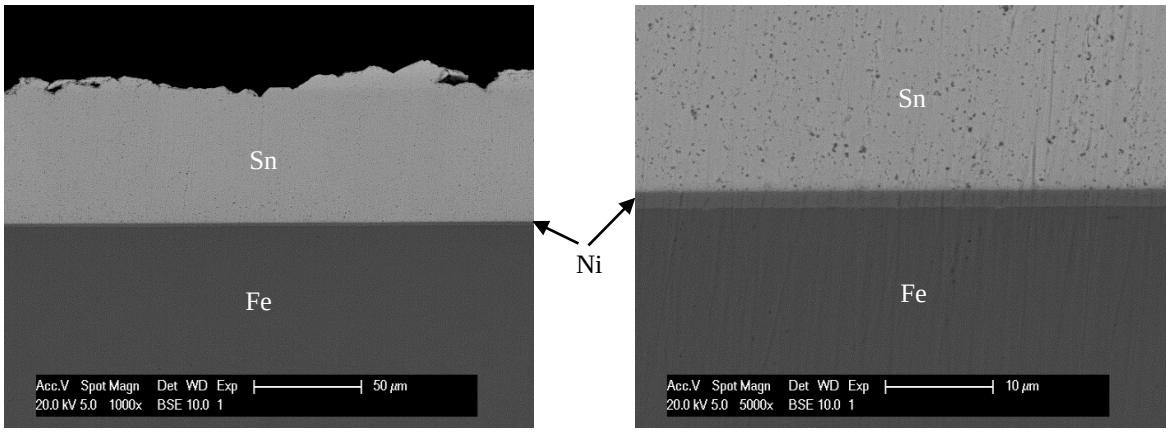
Table 5.1 Designs of samples of Si chip bonded to Ni-plated Fe substrate using fluxless Sn at 240°C reflow temperature

Sample designation	Ni thickness (μm)	Reflow time (seconds)	Remarks
A	1.5	300	
B	1.5	200	
C	4.5	200	

D	4.5	200	Sn etched away to expose Ni_3Sn_4 IMC for observation from the side (cross section)
E	4.5	200	Sn etched away to expose Ni_3Sn_4 IMC for observation from the top

5.3 Experimental results and discussion

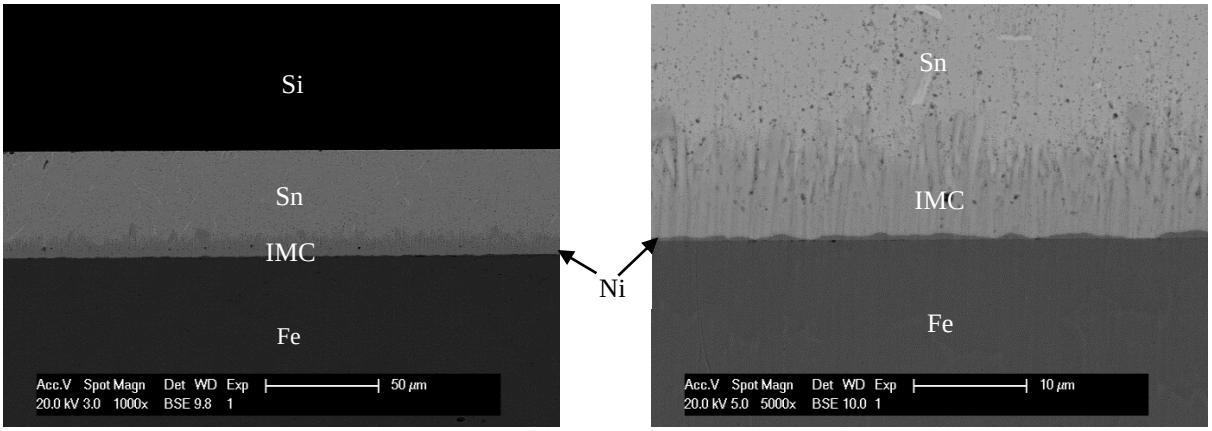
Fe substrates were electroplated with Ni and Sn layers sequentially. Prior to bonding, several as-plated samples were examined using SEM. Fig. 5.1 displays the cross-section images of a typical sample. The 1.5 µm Ni layer between the 70 µm Sn and Fe substrate is clearly seen. Its thickness is very uniform. Its interface with Fe and that with Sn are sharp, showing even Ni growth across the boundary.



(a) (b)

Fig. 5.1 Cross-section SEM images of a typical as-plated Fe substrate at (a) low magnification (1000×) and (b) high magnification (5000×). The substrate is electroplated with 1.5 μm Ni and 70 μm Sn

Si chips were then bonded to as-plated Fe substrates at conditions presented in the previous section with reflow time of 300 seconds. No flux was used in the bonding process. Fig. 5.2 shows the cross-section SEM images of sample A. No voids or gaps are observed at the Si/Sn and Sn/Ni interfaces, indicating that the Si chip is well bonded to the Fe substrate. The Sn thickness is 48 μm, close to the thickness of Cu spacers used to control the joint thickness. Part of Ni layer was consumed by interfacial reaction, forming a distinct IMC layer at the Sn/Ni interface.

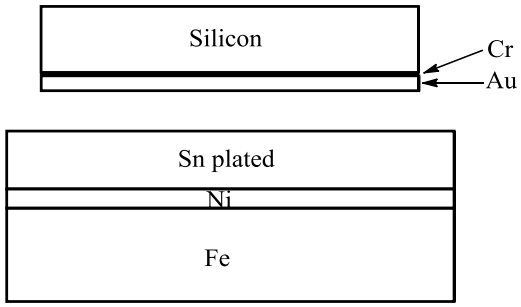


(a) (b)

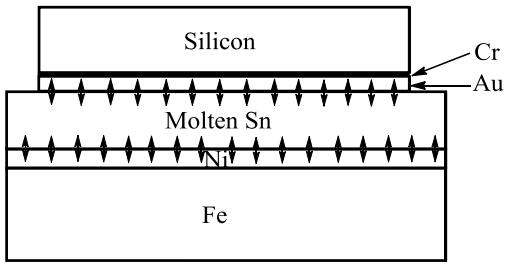
Fig. 5.2 Cross-section SEM images of sample A at (a) low magnification (1000×) and (b) high magnification (5000×). The sample is a Si chip bonded to Ni-plated Fe substrate with fluxless Sn at 240 °C with reflow time of 300 seconds

Fig. 5.3 depicts the schematics of the bonding mechanism. As mentioned earlier, the bonding between the as-plated Fe substrate and as-deposited Si chip is performed in a vacuum chamber where the oxidation is suppressed. As temperature goes above the Sn melting point, the

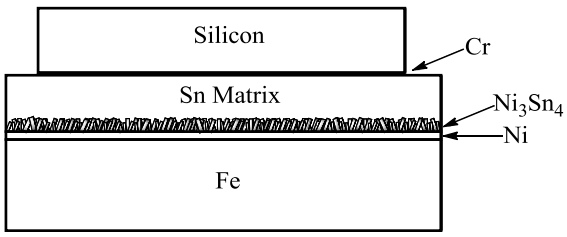
molten Sn begins to react with Au on the Si chip and Ni on the Fe substrate. On the Si side, the molten Sn dissolves the thin Au layer and the Au atoms are evenly distributed in the molten Sn. Now the molten Sn contacts the Cr layer, bringing Sn atoms within atomic distance of Cr atoms on the boundary. Based on the Cr-Sn phase diagram [13], shown in Fig. 5.4, Sn does not form IMC with Cr and the solid solubility of Cr in Sn is only 3×10^{-4} at.% at 232 °C. Thus, the thin Cr layer can sustain the molten Sn and bond to Sn without forming any IMC. The Cr layer does not show up on the SEM images in Fig. 5.2 because it is too thin. It is worth mentioning that no flux is needed to remove native oxide on Cr because Cr was never exposed to air either in the E-beam evaporation process or in the soldering process. In the meanwhile, on the Fe side, the molten Sn reacts with Ni layer to form IMC layer. As temperature goes below Sn melting point, Sn solidifies to result in a structure of Si/Cr/Sn/IMC/Ni/Fe-substrate.



(a) As deposited



(b) Above melting temperature of Sn



(c) After cooling down to room temperature

Fig. 5.3 Schematics illustrating the fluxless bonding mechanism

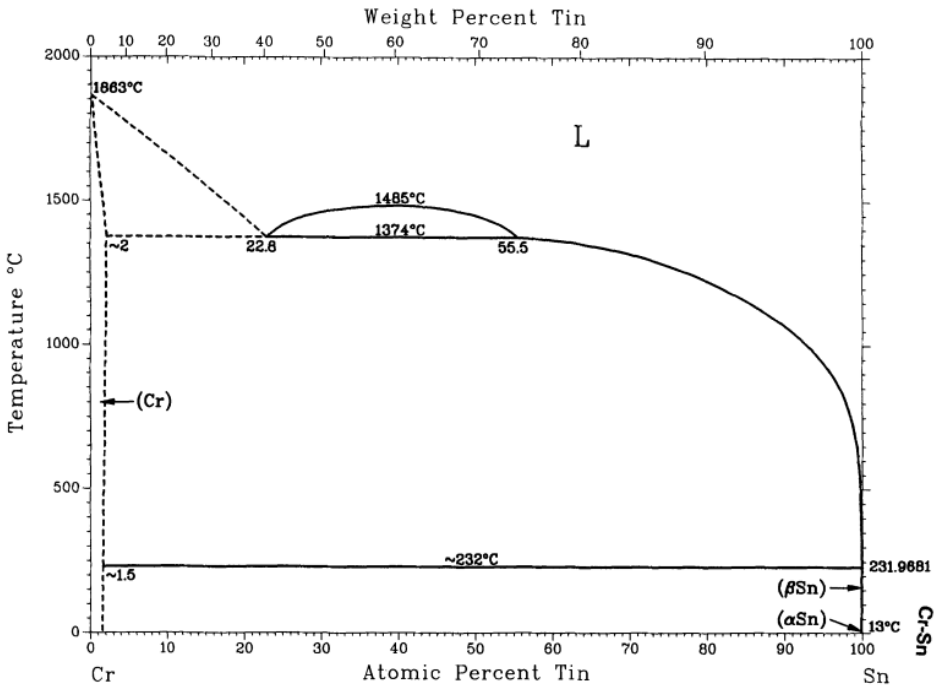
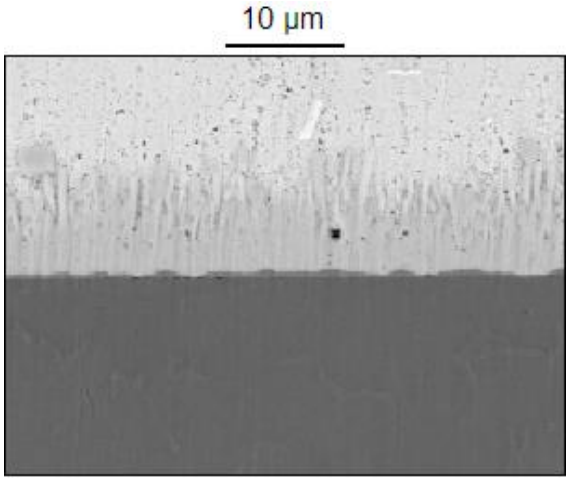
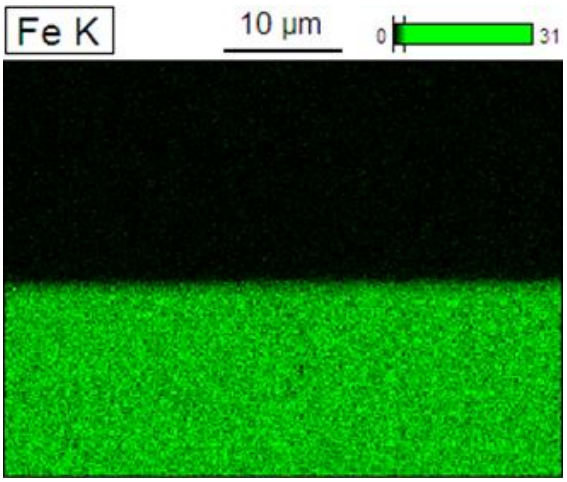


Fig. 5.4 The Cr-Sn binary phase diagram [13]

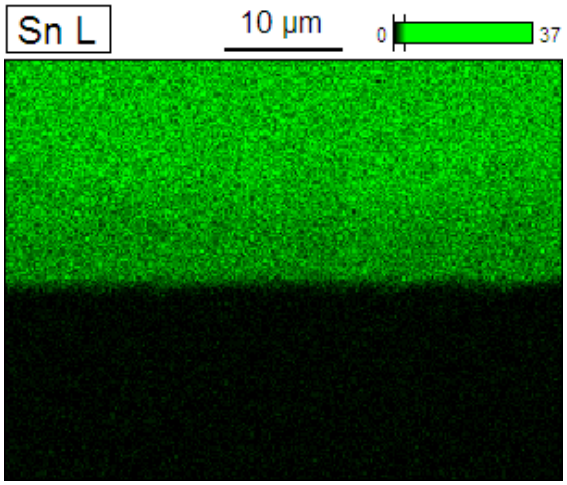
The IMC formation was further examined and analyzed. Samples D to E were made specifically for IMC growth study. The Sn/Ni interfacial reaction has been widely investigated [14-17]. It was found that Ni_3Sn_4 is the only IMC formed that could be identified in the reaction between Ni and pure Sn or Sn–rich alloys even though Ni_3Sn_2 and Ni_3Sn are also thermodynamically stable. The results observed in our research are similar. Fig. 5.5 displays the



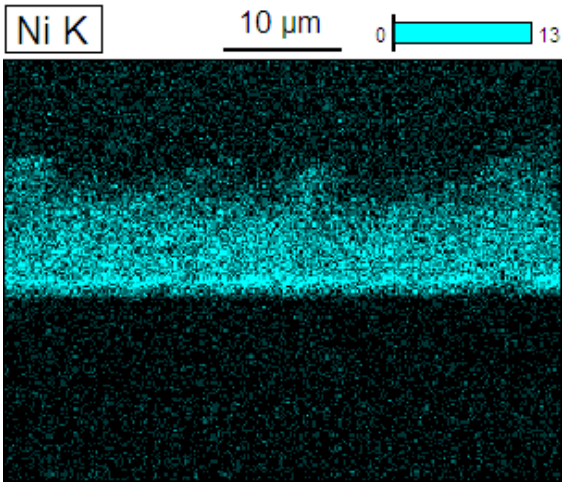
(a)



(b)



(c)



(d)

Fig. 5.5 Cross-section SEM images and element mappings at Sn/IMC/Ni of sample A. The Fe substrate was plated with 1.5 µm Ni followed by 70 µm Sn. The reflow time is 300 seconds during bonding

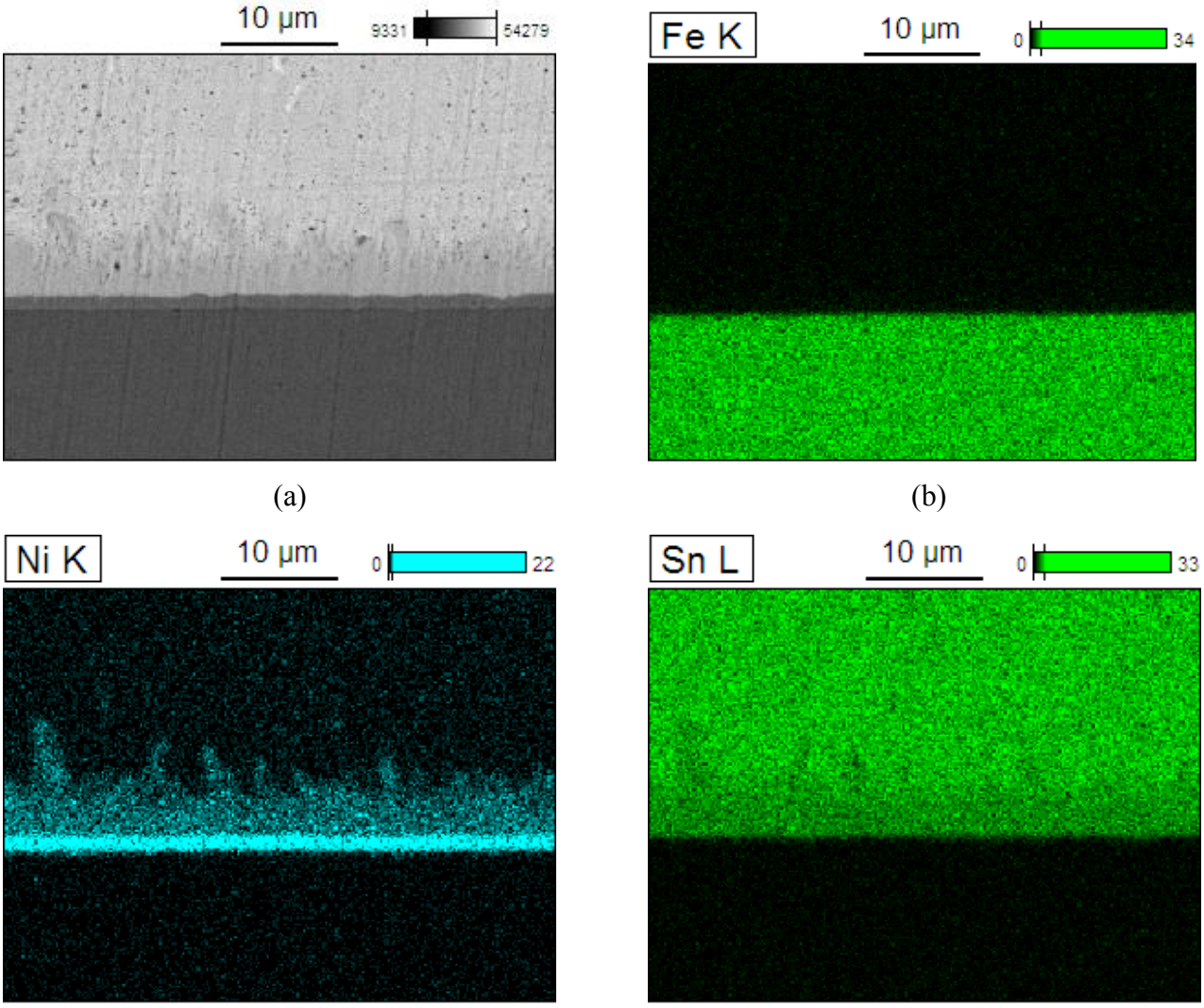
cross-section SEM images and the EDX element mappings of sample A in a typical Sn/IMC/Ni region.

The chemical composition of the IMC is determined to be Ni_3Sn_4 comprised of 42 at.% Ni and 58 at.% Sn based on EDX result. The IMC layer is where the Sn element and Ni element mappings overlap in the vertical direction. It is found the IMC grows in a rod-shaped manner toward the Sn matrix. The average IMC thickness is 8.5 µm determined by dividing the area of the IMC layer by the total length of the interface. Since the IMC growth is a key factor affecting the joint strength and reliability, its growth kinetic is worth further study. It is generally believed that the diffusion of Ni into molten Sn controls the heterogeneous nucleation of the IMC phase [18-19]. Several studies in literature report that the kinetic of the diffusion-controlled growth of Ni_3Sn_4 approximately follows a temperature and time-dependent parabolic growth law [18, 20-21],

$$X = Aexp\left(-\frac{Q}{RT}\right)t^n$$

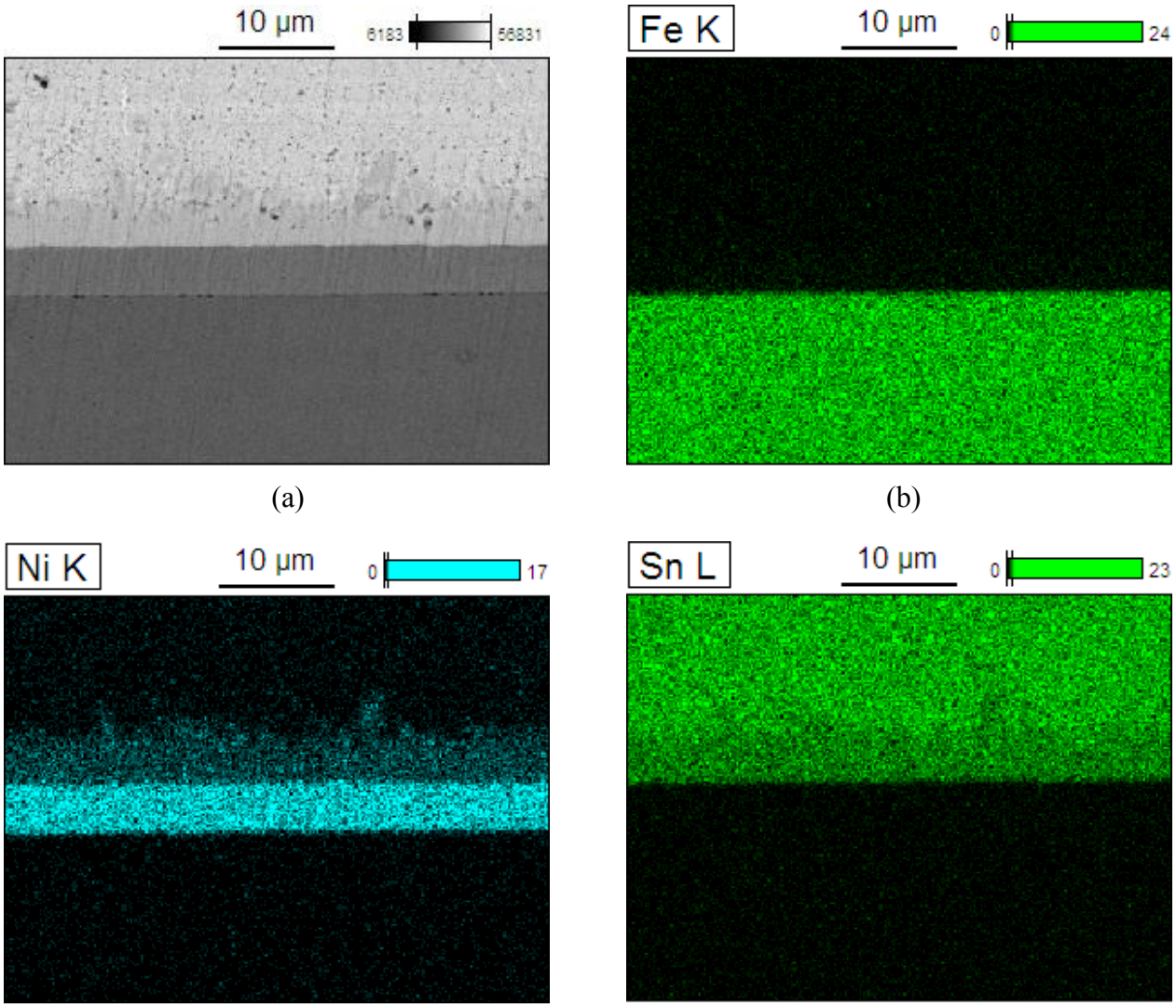
where X is the IMC thickness, A is the pre-exponential factor, Q is the activation energy, R is the gas constant, T is the reaction temperature, t is the reaction time and n is the time exponent. Fig. 5.6 presents the cross-section SEM images and EDX element mappings of sample B listed in Table 6.1. As compared to sample A, the reflow time was reduced from 300 seconds to 200 seconds. As

can be seen, less amount of Ni was consumed and a thicker Ni remained in the joint due to the shorter reflow time. The average IMC thickness layer is 5.1 µm as determined by the same method. The rod-shaped IMC structure is also observed. Sample C was made for comparison where the electroplated Ni layer on Fe substrate was increased to 4.5 µm while reflow time was kept at 200 seconds. Cross-section SEM images and element mappings are shown in Fig. 5.7. The average IMC thickness is 5.3 µm, which is very close to the thickness of IMC seen in sample B which was made with same reflow time. Based on these observations, we can presumably infer that the rate-determining factor in the IMC growth is the inter-diffusion on the interface between the molten Sn and solid Ni. The longer the reflow time, the more the Ni atoms react with Sn atoms, resulting in thicker IMC. The process is independent of the Ni layer thickness provided that there is enough Ni for the reaction. To investigate the microstructure and morphology of the Ni_3Sn_4 IMC, the bulk of Sn in the joints was selectively etched away to reveal the 3D microstructure. For sample D listed in Table 5.1, the Sn was etched away on the polished cross section from the side. Fig. 5.8 exhibits the SEM image. To obtain a top view of the IMC, the bulk of Sn joint of sample E was etched away completely. Fig. 5.9 displays its remarkable SEM image. In either sample, the Ni_3Sn_4 microstructure grows into the molten Sn in rod shape or polygonal shape. The length of the rod-shaped grains stretching into Sn matrix ranges from 3 µm to 10 µm. The lateral diameter of the rod-shaped grains ranges from 0.5 µm to 3 µm.



(a) (b) (c) (d)

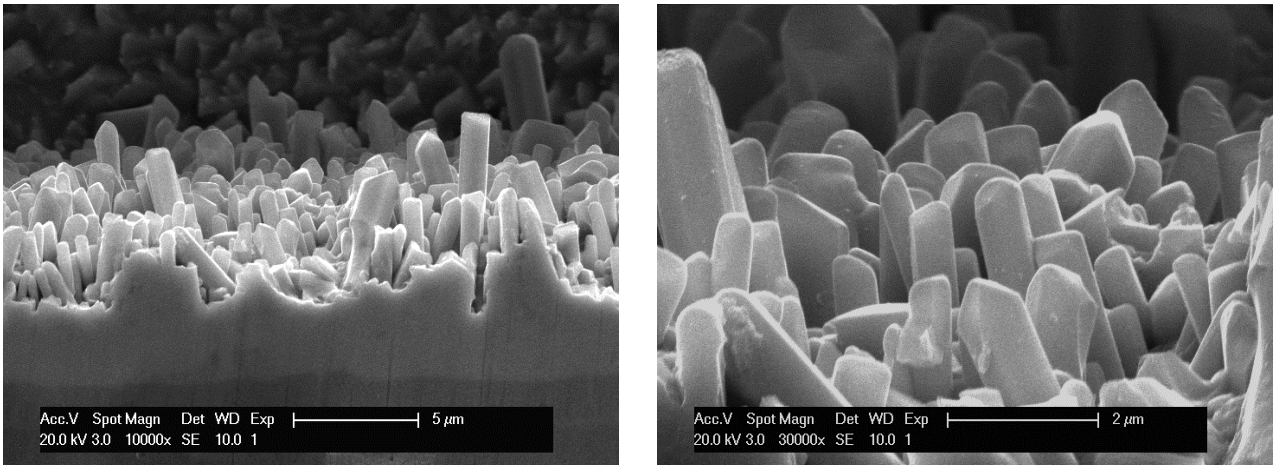
Fig. 5.6 Cross-section SEM images and element mappings at Sn/IMC/Ni of sample B. The Fe substrate was plated with 1.5 µm Ni followed by 70 µm Sn. The reflow time is 200 seconds during bonding



(a) (b)

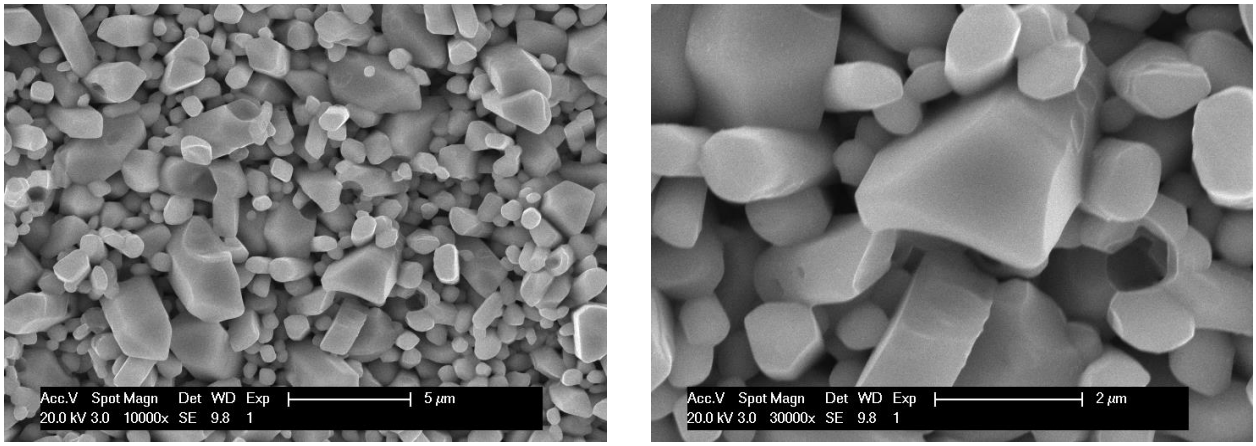
(c) (d)

Fig. 5.7 Cross-section SEM images and element mappings at Sn/IMC/Ni of sample C. The Fe substrate was plated with 4.5 µm Ni followed by 70 µm Sn. The reflow time is 200 seconds during bonding



(a) (b)

Fig. 5.8 SEM images of sample D showing the cross-section view of Ni_3Sn_4 IMC at (a) low magnification (10000×) and (b) high magnification (30000×). Sn was etched away to expose the IMC microstructure



(a) (b)

Fig. 5.9 SEM images of sample E showing the top view of Ni_3Sn_4 IMC at (a) low magnification (10000×) and (b) high magnification (30000×). Sn was etched away to expose the IMC microstructure

5.4 Summary

In this research, 5 mm×10 mm Si chips coated with thin Cr and Au layers are bonded at 240°C to Fe substrates which are electroplated with Ni and Sn without using any flux. SEM micrographs show that the joints contain few voids and the joint thickness is uniform. Bonding mechanism is established and intermetallic formation is analyzed. On the Si-Sn interface, no intermetallic formation incurs because the adhesion and barrier layer Cr does not react with Sn. On the Sn-Fe interface, only the intermetallic Ni_3Sn_4 is observed as identified by EDX. It is formed by reaction of molten Sn with Ni plated on the Fe substrate. The morphology of Ni_3Sn_4 is investigated by preferential etching. Rod-shaped or polygonal-shaped crystalline structures are observed. In electronic packaging, Fe was seldom adapted as substrates or base plates on which device chips or modules are soldered and attached to. The fluxless soldering process developed in this project should offer the automotive and electronic industries a new tool to expand the choice of substrate materials to include Fe.

5.5 References

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Chapter Six

Fluxless Sn bonding of silicon chips to low carbon steel substrates without under-bump metallurgy

6.1 Introduction

In our previous study, we have shown that silicon (Si) chip can be bonded to low carbon steel substrates using nickel (Ni) as underbump metallurgy (UBM) between tin (Sn) solder and low carbon steel substrates. In that study, Ni_3Sn_4 intermetallic compound was observed at the Sn-Fe interface. The IMC thickness increases from 5.1 to 8.5 μm as reflow time goes from 200 to 300 seconds. The rate of formation of Ni_3Sn_4 IMC in Ni/Sn binary system is not as slow as expected in comparison to the rate of Cu_6Sn_5 and/or Cu_3Sn IMC in Cu/Sn binary system. We thus embarked on finding another alternative UBM material. Finally we came up with an idea of utilizing Sn/Fe binary system for bonding without adding a layer of UBM. Based on Sn-Fe binary phase diagram [1], FeSn and $FeSn_2$ are two stable IMC phases at room temperature. However, studies on interfacial reactions between Fe and Sn-based alloys have shown that $FeSn_2$ is the only IMC phase observed at the interface [2-3]. We therefore decided to study the feasibility of using Sn/Fe binary system for bonding Si chips to Fe substrates.

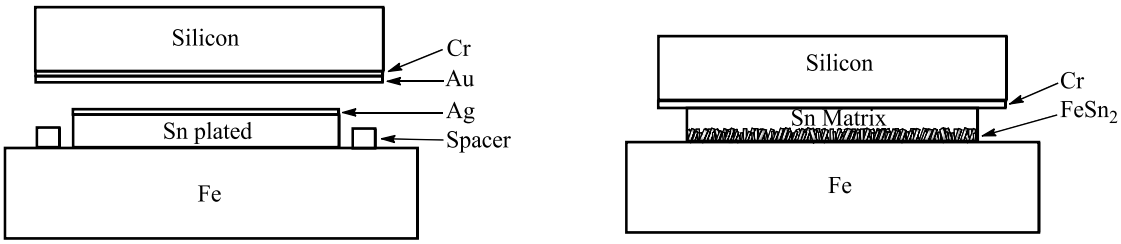
In this paper, we report results of bonding Si chips to Fe substrates using pure Sn solder. After the samples were bonded, the quality and microstructure of the joints were examined using scanning electron microscopy (SEM) and the composition of the joints was studied with energy dispersive X-ray spectroscopy (EDX). The joint strength was examined by shear test. In what follows, we first present the experimental design and procedures. Experimental results are then reported and discussed. Finally, a short summary is given.

6.2 Experimental Design and Procedures

Substrates of 15 mm×13 mm×3.3 mm (width×length×thickness) were cut from AISI 1018 low carbon steel sheet. Substrates were ground using 800 and 1200 grit SiC-coated papers to smooth the surface out and cleaned with acetone and deionized water before electroplating. 70 or 50 μm Sn was electroplated on the Fe substrates in a stannous bath under the condition of 43°C and pH of 1 with current density of 30 mA/cm^2, followed by a thin layer silver (Ag) of 100 nm in thickness over Sn as capping layer to prevent Sn from oxidation. To make the Si chips ready for bonding, two-inch n-type Si wafers in (100) orientation were deposited with 30 nm Cr and 100 nm Au layers using E-beam evaporation. The Cr layer acts an adhesion layer and the Au layer acts the

capping layer that protects the Cr layer from oxidation when exposing to air. The wafers were then diced into 5 mm×10 mm chips.

The Si chip and Fe substrate were held together with 50 or 30 μm thick spacers placed in between. Fig. 6.1(a) depicts the structure design of the bonding systems. The assembly was mounted on a heater graphite platform in a chamber with a 16 psi pressure applied on the Si chip to ensure intimate contact. The chamber was pumped down to 80 millitorrs and the graphite platform was then heated. The bonding process was conducted at 240°C with reflow time of 300 seconds. After bonding, the heater was turned off and the assembly was allowed to cool down naturally to room temperature in vacuum environment. For SEM examination, the samples were mounted in epoxy, sectioned using slow speed diamond saw, ground with 800 and 1200 grit SiC paper and polished with alumina suspension solution for microstructure and composition examination. The microstructures were examined by SEM equipped with a back-scattered electron (BSE) image detector. The chemical compositions were analyzed using EDX spectroscopy. Shear tests on the bonded were implemented to evaluate their shear strengths and fracture modes.

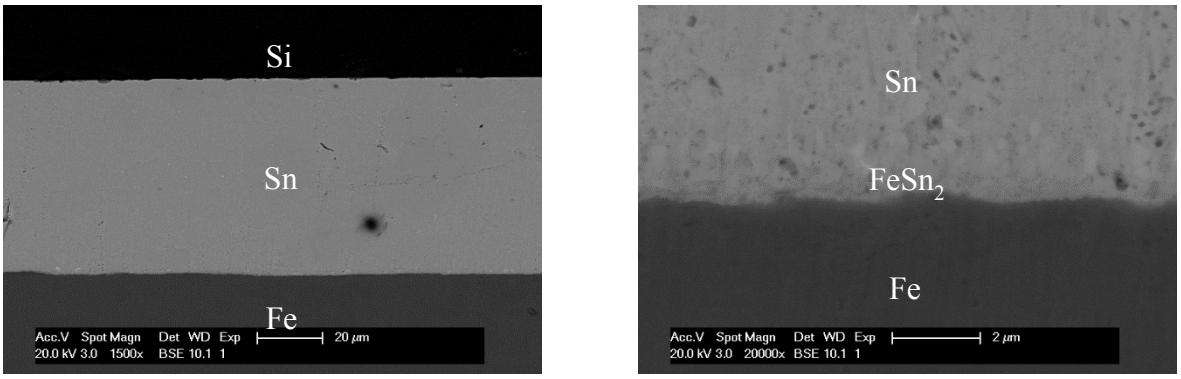


(a) (b)

Fig. 6.1 Schematics illustrating: (a) Bonding structure and configuration and (b) Layer structure after bonding

6.3 Experimental results and discussion

The fluidic nature of molten Sn during bonding process makes the consistent control of joint thickness difficult. Uneven application of pressure in bonding process could make the Si chip incline toward an arbitrary direction, resulting in joint thicknesses variation within one sample. To control the joint thickness, spacers of 50 and 30 μm thick were used. Fig. 6.1(b) displays the layer structure after bonding. The thin Au layer on Si/Cr and thin Ag on Sn were both dissolved at 240°C and eventually distributed in Sn matrix after cooling down to ambient temperature. Fig. 6.2 shows the cross-section SEM images of the bonded sample using 50 μm spacer. Si chip is well bonded to the Fe substrate.



(a) (b)

Fig. 6.2 Cross-section SEM images of the sample using 50 μm spacers at (a) lower magnification (1500×) and (b) higher magnification (20000×) showing the Sn/Fe interface

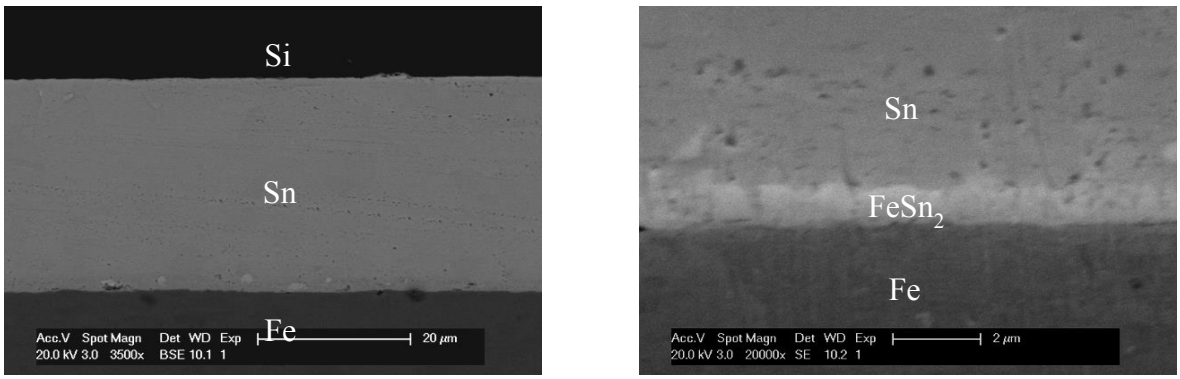
The Si/Cr-Sn interface is free from intermetallic compound (IMC) formation. On the other hand, it is observed that IMC layer of around 1.5 μm thick was formed at Sn-Fe interface. EDX analysis identified the chemical composition of IMC as $FeSn_2$, which is similar to the results in the studies on interfacial reactions between Fe and Sn-based alloys [2-3]. The Sn thickness is about 60 μm, which is larger than the spacer thickness. This may be ascribed to the improper setting during the bonding process. Theoretically, the possibility of solder joint breakage caused by CTE mismatch could be evaluated by the maximum shear strain. In this model, both Si chip and Fe substrate are assumed to be able to be free to contract during cooling down. This maximum shear strain is calculated by the well-known equation [4],

$$\gamma = \frac{(\alpha_1 - \alpha_2)(T_2 - T_1)\frac{L}{2}}{h} \qquad (1)$$

where α_1 and α_2 are the CTE of silicon chip and low carbon steel, respectively, T_2 is the solidifying or the bonding temperature, T_1 is room temperature, L is diagonal length of the Si chip, h is the thickness of the joint. For a joint thickness of 60 μm, the maximum shear strain is calculated to be 0.10. Fig. 6.2 shows that the joint has no crack at the bonding interfaces. The samples did not break despite the large CTE mismatch. These observations indicate that the bonded structure is strong enough to sustain the stress developed due to CTE mismatch.

Exhibited in Fig. 6.3 are the cross-section SEM images of the bonded sample using 30 μm spacer. Si chip is also well bonded to the Fe substrate. The Sn thickness is about 30 μm, close to

the thickness of the spacer. The IMC thickness is only about 1.1 μm. The chemical composition of the IMC was also confirmed as $FeSn_2$. The calculated maximum shear strain is 0.21. This means the 30 μm joint can also accommodate the thermal stress causing by the CTE mismatch, although the calculated maximum shear strain is two times larger than that of the 60 μm joint.



(a) (b)

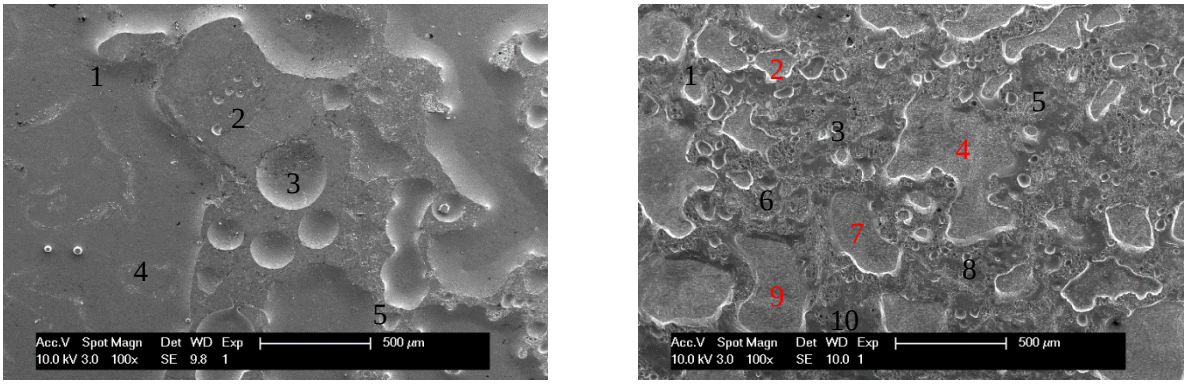
Fig. 6.3 Cross-section SEM images of the sample using 30 μm spacers at (a) lower magnification (3500×) and (b) higher magnification (20000×) showing the Sn/Fe interface

Shear tests were performed on six samples bonded using 30 μm spacer. The measured fracture force of six samples ranges from 5.0 to 23.5 kg, as listed in Table 6.1. According to MIL-STD-883H method 2019.8, the minimum passing fracture force should be larger than 5 kg for a 0.36 cm^2 bonding area. The fracture force of each sample (bonding area: 0.25 cm^2) exceeds the passing requirement.

Table 6.1 Fracture forces and shear strengths of the six samples bonded using 30 μm spacer after the shear tests

Sample	Fracture force (Kg)	Shear Strength	
		(MPa)	(psi)
1	8.6	3.4	496
2	5.0	2.0	285
3	10.7	4.3	682
4	23.5	9.4	1362
5	8.0	3.2	461

Fig. 6.4, Table 6.2 and Table 6.3 display EDX analysis results on the Fe substrate side of sample 2 and 4. Sample 2 shows the lowest fracture force and sample 4 exhibits the highest fracture force. It is seen that, in sample 2, the joint broke at the Cr/Sn interface. However, in sample 4, the joint broke at two interfaces: Cr/Sn and Sn/$FeSn_2$. These interfaces are illustrated in Fig. 6.1(b). The morphological observation shows that sample 4 has a coarser texture than sample 2. The low fracture force in sample 2 may be attributed to the contamination during the bonding process.



(a) (b)

Fig. 6.4 Top-view SEM images of (a) sample 2 and (b) sample 4 on Fe substrate side after the shear tests. The chemical compositions of the marked regions are shown in Table 6.2 and Table 6.3

Table 6.2 EDX analysis data of five regions marked as 1, 2, 3, 4 and 5, as shown in Fig. 6.4(a)

Region	Composition (atomic %)	
	Fe	Sn
1	0	100
2	0	100
3	0	100
4	0	100
5	0	100

Table 6.3 EDX analysis data of ten regions marked from 1 to 10, as shown in Fig. 6.4(b)

Region	Composition (atomic %)	
	Fe	Sn
1	0	100
2	23	77
3	0	100
4	25	75
5	0	100
6	0	100
7	28	72
8	0	100
9	28	72
10	0	100

6.4 Summary

In this work, we have successfully developed a fluxless process of bonding Si chips to low carbons steel substrates using electroplated Sn solder. Low carbons steel substrates were electroplated with 70 μm Sn, followed by thin layer of Ag (100 nm). Si chips were deposited with thin Cr (30nm) and Au (100nm) using E-beam evaporation in high vacuum environment. The Si chip was placed over the low carbon steel substrate and bonded at 240°C using 50 and 30 μm thick spacers to control joint thickness. The resulting joint is uniform as examined by scanning electron microscopy (SEM). Energy dispersive X-ray spectroscopy (EDX) confirmed that the IMC formed at Sn/Fe interface composition is $FeSn_2$. The IMC layer thickness is only 1.1 to 1.5 μm. The shear tests certified that the measured fracture forces of the bonded samples exceed the standard specified in MIL-STD-883H, method 2019.8. This process addresses a new method to bond Si chips to Fe substrates that expands the scope of bonding design in electronic packaging.

6.5 References

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Chapter Seven

Growth Kinetics of Intermetallic Compounds between Sn and Fe Liquid-Solid Reaction Couples

7.1 Introduction

Ferrous metals have had various applications in automotive and electronic industries. Ultra low carbon, low carbon, and micro-alloyed steels have been widely used as auto body material [1-3]. Invar (Fe-36Ni) is known for its uniquely low coefficient of thermal expansion (CTE) around 0.8 to 1.6 ppm/°C (measured between 30-100°C). It has been utilized in manufacturing precision instruments where high dimensional stability is required. Alloy 42 (Fe-42Ni) and Kovar (Fe-29Ni-17Co) are controlled expansion alloys with CTE of 4.0 to 4.7 ppm/°C (measured at 30-300°C) and 5.1 to 5.5 ppm/°C (measured at 30-450°C), respectively [4-6]. In electronics, these alloys have been used to make lead-frames of plastic packages and headers of transistor packages because their CTE is close to that of silicon (3 ppm/°C) and lead-sealing glass. They have also been chosen for manufacturing headers of laser diodes because their CTE matches well with that of gallium arsenide (GaAs) semiconductor (7 ppm/°C). One downside of these alloys is the relatively low thermal conductivity (10-17 W/m-K) [7]. We thus looked into ferrous metals that have higher

thermal conductivity and reasonably low CTE for electronic packaging applications. After a thorough search, AISI 1018 low carbon steel was selected for this study. It has thermal conductivity of 51.9 W/m-K and CTE of 11.5 ppm/°C [8].

During the process of producing the metallic bonding between solder and metal, molten phase solder wets metal surface and reacts with metal to form an intermetallic compound (IMC) layer between solder and metal. However, the brittle nature of IMC could make it possible to be the most vulnerable point in the solder joint. Last but not least, the formation of IMC occurs not only by liquid (molten solder)-solid (metal) reaction during reflow process but by the solid-solid reaction during storage and service life. It is therefore essential to study the mechanism and kinetics of the formation of IMC at the lead-free solders/metal substrate interface. The aim of this work is to explore the growth behavior of intermetallic compound between electroplated tin (Sn) and iron (Fe) at the temperatures above the melting point of Sn (231.93°C). In what follow, experimental design is first presented. Experimental results are reported and discussed. A brief summary is then given.

7.2 Experimental Design and Procedures

Substrates of 15 mm×13 mm×3.3 mm (width×length×thickness) were cut from AISI 1018

low carbon steel (Fe) sheet. They were ground using 800 and 1200 grit SiC-coated papers to smoothen out the surface. They were cleaned with acetone and deionized water before electroplating. Sn of 85 μm thick was electroplated over the Fe substrate in a stannous methanesulfonate bath under the condition of 43°C and pH of 1 with current density of 30 mA/cm^2. Matte Sn electroplating solution was chosen instead of bright Sn because matte is less prone to whisker formation [1]. The Sn-coated Fe substrates were then treated isothermally in 250°C, 335°C and 400°C air for different durations of time in a convection furnace that had been preheated to required temperatures. After the reactions, the Sn-coated Fe substrates were cooled in air and then mounted in epoxy resin. The samples were then cross-sectioned into halves. Microstructure observation and composition analysis were studied using scanning electron microscopy (SEM) and energy- dispersive X-ray spectroscopy (EDX). The composition of the IMC was also studied by X-ray diffraction (XRD) after etching the reacted Sn-coated Fe substrate with diluted HCl.

7.3 Experimental results and discussion

7.3.1 Microstructural evolution of the intermetallic compound layer

Fig. 7.1 exhibits the cross-section SEM images of the interfacial layer between Sn and Fe reacted at 250°C for 2, 12, 50, and 200 hours, respectively. It was seen that molten Sn reacted

readily with Fe to form IMC, an essential requirement of soldering action. This indicates that Fe is easily solderable without using flux, provided that the soldering interface is free of oxides. To estimate the average thickness of the IMC layer, the region of IMC layer was first evaluated using image processing software. The average thickness was then determined by dividing the area of the IMC layer by the total length of the interface from the cross-section SEM micrographs. The average IMC thickness obtained is 5.8 μm after isothermal annealing at 250°C for 2 hours as shown in Fig. 7.1(a). A thin layer of IMC about 1 μm was formed adjacent to Fe, which is composed of many IMC granules. IMC also grew vertically toward Sn matrix to form columnar crystals of different lengths, ranging from submicron to 5 μm. It was observed that some IMC columnar crystals detached from the continuous IMC layer and drifted into to the Sn solder bulk. This "spalling behavior" is similar to the literature data reported by Lin et al. and Teo et al [2-3]. EDX analysis confirmed the IMC composition to be $FeSn_2$. As annealing time increased to 12 hours, it was seen that the columnar IMC crystals grew in both longitudinal and lateral direction as displayed in Fig. 7.1(b). The average IMC thickness increases to 8.7 μm. Fig. 7.1(c) and 7.1(d) shows the SEM image after annealing at 250°C for 50 and 200 hours, respectively. After prolonged annealing, the columnar IMC crystals continued ripening and started to agglomerate together, and

ultimately formed a continuous IMC layer. The average IMC thicknesses after annealing at 250°C for 50 and 200 hours were estimated to be 13.3 and 20.9 μm, respectively.

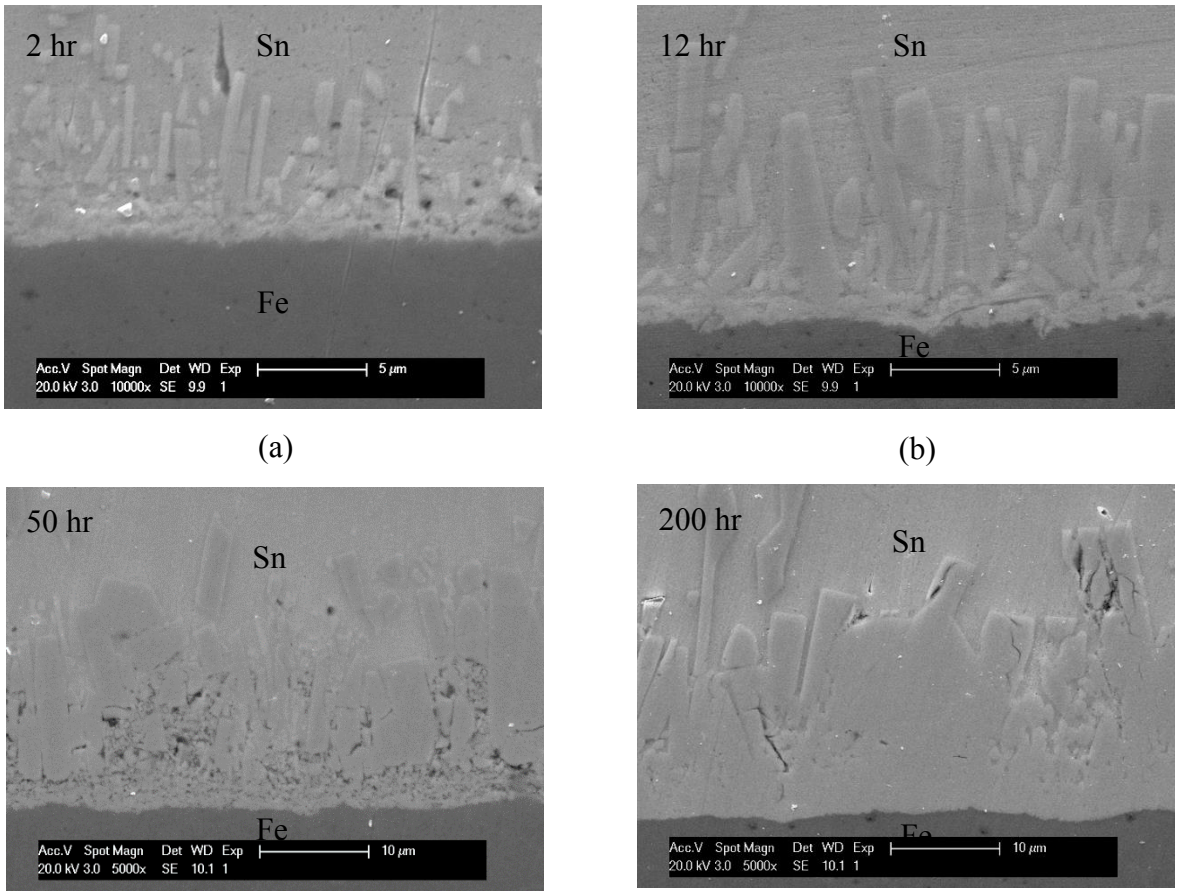

Fig. 7.1 Cross-section SEM micrographs of the interfacial layers between Sn solder and Fe metal substrates annealing at 250°C for (a) 2 hr, (b) 12 hr, (c) 50 hr and (d) 200 hr

Presented in Fig. 7.2 are the cross-section SEM images of the interfacial layer between Sn and Fe reacted at 335°C for 2, 12, 50 and 100 hours. Compared to the samples annealed at 250°C, the columnar IMC crystals in the samples annealed at 355°C exhibit more rounded edges. With longer annealing time up to 50 hours, the spalling behavior became obvious. It was also observed

that, when the annealing was extended to 100 hours, a large amount of the IMC spalled off and sporadically distributed in Sn matrix. Similar to the samples annealed at 250°C, the only IMC found is $FeSn_2$ as examined by EDX analysis. The average IMC thicknesses of the samples annealed at 335°C for 2, 12, 50 and 100 hours are 10.3, 23.0, 44.9 and 62.2 μm, respectively.

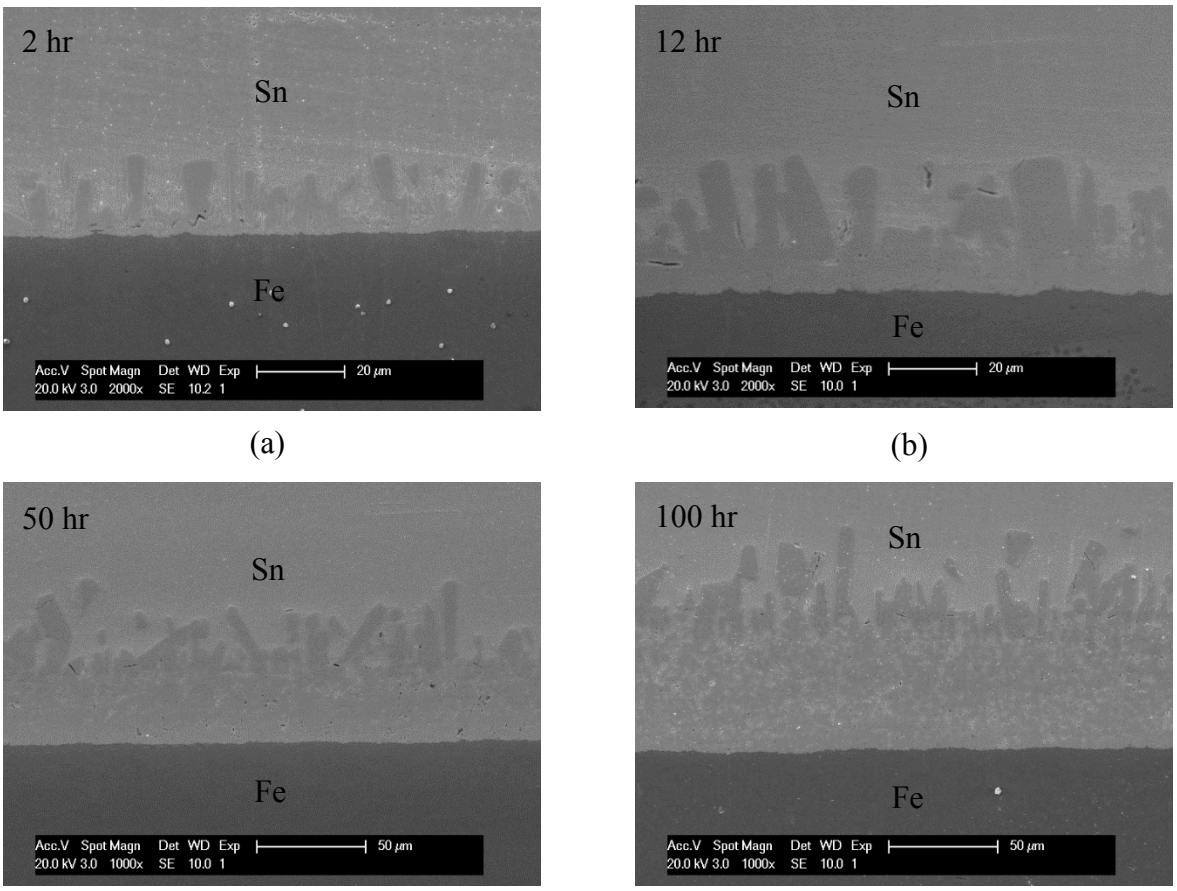

Fig. 7.2 Cross-section SEM micrographs of the interfacial layers between Sn solder and Fe metal substrates annealing at 335°C for (a) 2 hr, (b) 12 hr, (c) 50 hr and (d) 100 hr

As the annealing temperature increased to 400°C, IMC grew faster and the morphology is more irregular in comparison with the samples annealed at 335°C, as depicted in Fig. 7.3.

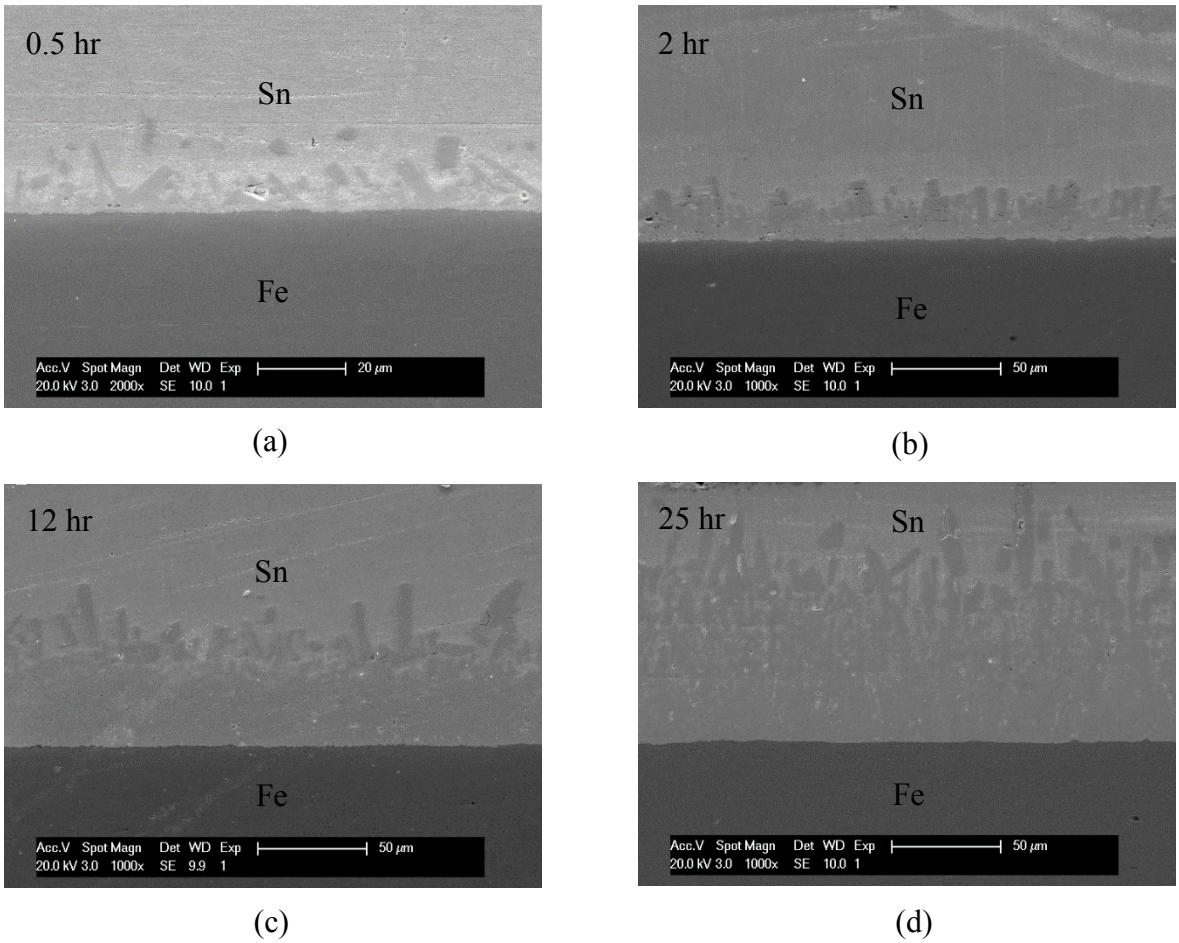

Fig. 7.3 Cross-section SEM micrographs of the interfacial layers between Sn solder and Fe metal substrates annealing at 400°C for (a) 0.5 hr, (b) 2 hr, (c) 12 hr and (d) 25 hr

The average IMC thicknesses of the samples annealed at 400°C for 0.5, 2, 15 and 25 hours are 9.9, 20.5, 53.4 and 75.3 µm, respectively. XRD pattern obtained from the top surface of the etched sample reacted at 400°C for 25 hours is shown in Fig. 7.4. Only Sn and $FeSn_2$ were identified in the XRD pattern. This is in agreement with the results obtained from EDX analysis that only $FeSn_2$ was found at the interface, so were observed in the samples after annealing at 250°C and 335°C. Although FeSn is also shown as a stable IMC in the Fe-Sn binary phase diagram,

FeSn IMC was not identified [4]. This result is consistent with the observations in other Sn-containing solder/ferrous metal reaction systems [5-7].

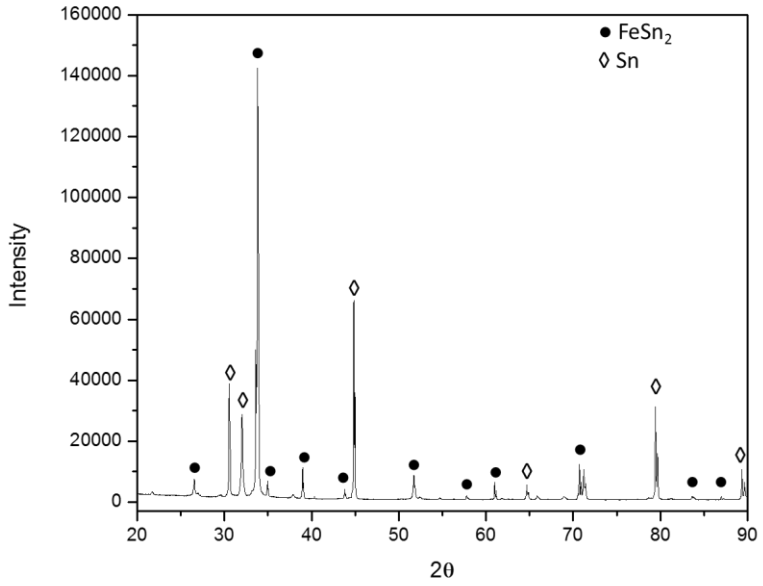

Fig. 7.4 X-ray diffraction pattern obtained from the top surface of the etched sample reacted at 400°C for 25 hours

7.3.2 Growth kinetics of the intermetallic compound layer

The data of the average $FeSn_2$ IMC thickness with respect to annealing time for each annealing temperature are plotted in Fig. 7.5.

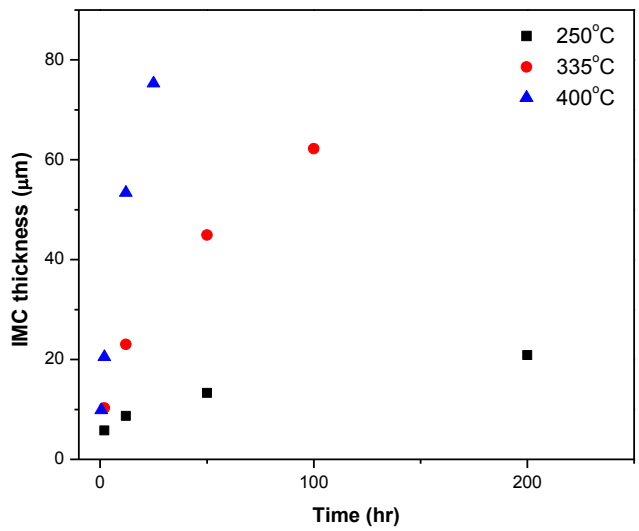

Fig. 7.5 Variation in the average thickness of the IMC with annealing time at 250°C, 335°C and 400°C

It is evident that the average IMC thickness increases as the annealing time and annealing temperature increases. Assuming that IMC formation is diffusion-controlled, the parabolic law holds.

$$d = kt^{\frac{1}{2}} \qquad (1)$$

Here, d is the average IMC thickness, t is the annealing time, k is the parabolic growth constant. This equation is derived from Fick's first law based upon the assumptions: (1) the change in concentration of diffusing components with distance within the IMC layer is linear and (2) the concentration of diffusing components at interlayer boundaries is constant [8-9]. The average $FeSn_2$ IMC thicknesses in meters are plotted as a function of the square root of the annealing time

in seconds for each annealing temperature and fitted with least-squares linear regression, as displayed in Fig. 7.6, so as to determine the values of k for each annealing temperature.

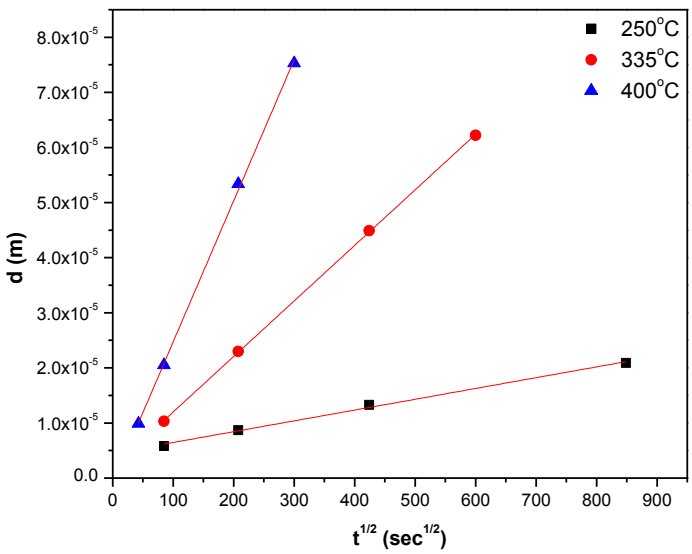

Fig. 7.6 Variation in the average thickness of the IMC as a function of the square root of annealing time at 250°C, 335°C and 400°C. The straight lines represent fits of the data by linear regression

The evaluated values of k are 1.96×10^{-8}, 1.01×10^{-7} and 2.56×10^{-7} m/s$^{1/2}$ at 250°C, 335°C and 400°C, respectively. The k values are subsequently analyzed to find the activation energy (Q) for the diffusion-controlled IMC growth using the Arrhenius equation,

$$k = k_0 \exp(\frac{-Q}{RT}) \qquad (2)$$

where k_0 is the pre-exponential factor, Q is the activation energy, R is the gas constant and T is the absolute temperature. Therefore, as shown in Fig. 7.7, the activation energy obtained from the plot of ln(k) versus 1/T is 50 KJ/mol (0.52 eV). This value is smaller than those reported previously

[10-12], where different annealing time, temperature and environment were conducted and diffusion couples were made with different process.

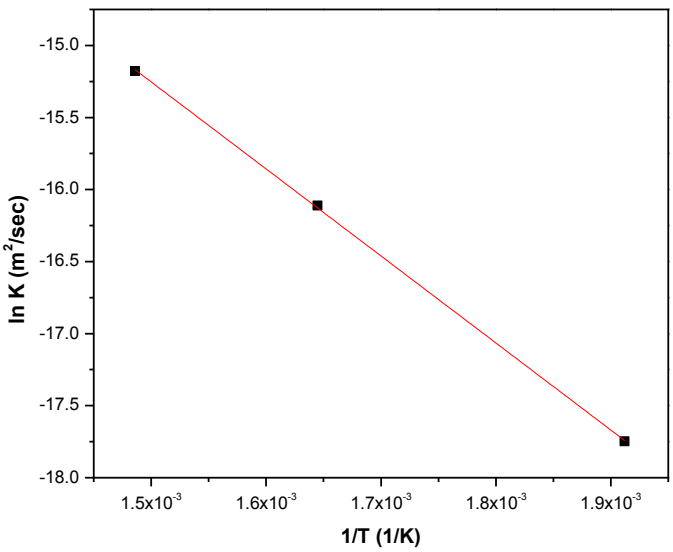

Fig. 7.7 Arrhenius plot for evaluating the activation energy for the growth of IMC. The straight line represents a fit of the data by linear regression

Analyzing the data shows the growth kinetics may also be modeled with an empirical power law:

$$d = kt^n \qquad (3)$$

Equation 3 is analogous to equation 1, except that the time exponent, n, is adopted as a variable.

Fig. 7.8 presents the regression curves.

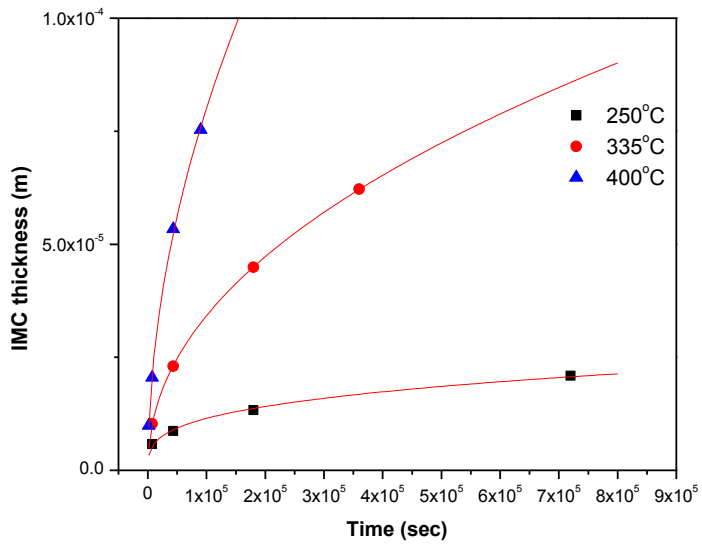

Fig. 7.8 Variation in the average thickness of the IMC with annealing time at 250°C, 335°C and 400°C. The curves represent fits of the data by regression with the equation $d = kt^n$

The values of time exponent, n, obtained by regression analysis, are 0.298, 0.466 and 0.509 at 250°C, 335°C and 400°C, respectively. The growth exponent, n, at 250°C takes a value of 0.298. The value deviates from the value (0.5) in parabolic law, indicating that the layer growth mechanism is not a simple Fickian diffusion process whereby volume (bulk) diffusion is assumed as the predominant diffusion path. In fact, it is possible that not only volume (bulk) diffusion but other diffusion paths contribute to the rate-controlling process as well. For instance, grain boundaries, dislocations and free surfaces are high-diffusivity paths or diffusion short circuits [13] in metals. Here, grain boundary diffusion could be used to account for this deviation from parabolic law. As can be seen in Fig. 7.1, at early stage (annealed for 12 hours) of the annealing process, the

grain sizes of the IMC near the interface close to Fe is small, suggesting that there are still enough fast paths (grain boundaries) for the interdiffusion of Sn and Fe atoms at the interface. In the course of time, the IMC grain size grows larger and the density of grain boundary is reduced. At some point the grain become large enough and connect together to form a continuous layer of IMC, as displayed in Fig. 7.1(d), the slow path (volume diffusion) turns out to take over the major diffusion transport mechanism. This is manifested by the observation of flatten-out of the growth curve at prolonged annealing time for annealing at 250°C. Similar studies in the literature have reported that the growth exponents range from 0.25 to 0.32 for similar solid-liquid reactive diffusion couples [14-16]. On the other hand, the obtained growth exponents are close to 0.5 for the annealing experiments conducted at higher temperatures; those are 0.47 at 335°C and 0.51 at 400°C. This means that the growth kinetics at 335°C and 400°C is diffusion-controlled. The spalling-out of large amount of IMC occurred at higher annealing temperature explains the reason why the growth kinetics complies with parabolic law. At higher annealing times, the diffusing components have higher mobility so the rate of formation IMC is faster. The IMC grows quickly but some of them float towards to Sn molten phase. The IMC grains do not have chance to undergo grain growth or Ostwald ripening. As shown in Fig. 7.2(d) and Fig. 7.3(d), the IMC does not form a continuous layer but sporadically distributes in the Sn matrix. The channels between IMC grains provide enough interdiffussion paths of reaction components. It is also worth mentioning that the

irregular morphology of the IMC could cause the disparity of growth exponent values as well. The parabolic model derived from Fick's first law is based on assumptions as mentioned previously. It is assumed that the change in concentration of diffusing components with distance within the IMC layer is linear. This reminds us of the fact that this is not the situation in the real case though. The shape of IMC varies from spherical to ellipsoidal or elongated columnar. At higher annealing temperature, the IMC even disintegrates into fragments. Here, the concentration of diffusing components, Sn and Fe atoms, cannot be linear with the $FeSn_2$ IMC layer. This makes the assumption inadequate in real case.

7.4 Summary

The Sn-Fe liquid-solid reactive diffusion couple was experimentally studied. The diffusion couples were prepared by electroplating matte Sn on low carbon steel and then annealed in air at 250, 335 and 400°C with various annealing time. Only $FeSn_2$ was recognized as the intermetallic compound at the interface. The $FeSn_2$ intermetallic compounds mainly grew towards Sn matrix with different geometrical shapes. Some of them spalled off the continuous intermetallic layer. It was also found that, at higher annealing temperatures and longer annealing time, the fragmented IMC was formed and scattered in the Sn matrix sporadically. The growth kinetics of the

intermetallic compound was first investigated using diffusion-controlled model. The obtained activation energy for the formation of the intermetallic compound is 50 KJ/mol. Further analyses showed that the average intermetallic compound thickness better obeys the empirical power function where the time exponent of the growth is not 0.5 as described in the diffusion-controlled model. The time exponents were evaluated to be 0.298, 0.466 and 0.509 at 250°C, 335°C and 400°C, respectively. The discrepancy of the time exponents is probably attributed to the effect of grain growth and the irregular morphological microstructures of the intermetallic compound layer.

7.5 References

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Chapter Eight

Fluxless tin bonding process with suppressed intermetallic growth

8.1 Introduction

Soldering is a metallurgical bonding process that joins two metals together using another metal or alloy having relatively low melting point and good wettablility. It has been widely used at different levels of electronics packaging and serves the purposes of electrical connection, heat transport and mechanical support [1-3]. It is well known that solder bonds to metals by forming intermetallic compounds (IMCs) on the interfaces. The IMCs formed between copper (Cu) and tin-containing solder are Cu_6Sn_5 and Cu_3Sn [4]. The Cu_3Sn grows adjacent to copper and Cu_6Sn_5 forms adjacent to the solder. Likewise, the only IMC detected between Ni and Sn-containing solder is Ni_3Sn_4 [3]. The IMC forms in layer structure and grows gradually during reflow processes or the service life.

It was well recognized that excessive intermetallic growth could deteriorate the joint reliability [5]-[6]. IMCs do not deform so easily as the solder in providing plastic strain to accommodate mismatch in the coefficient of thermal expansion (CTE). Extensive IMC growth reduces the solder thickness and thus increases the shear strain of the bonded structure.

Furthermore, metal/IMC interfaces often act as sites for crack initiation and propagation. It has been reported that, due to the difference in the intrinsic diffusivity of Cu and Sn in Cu_3Sn layer, Kirkendall voids form at the Cu/Cu_3Sn interface or within the Cu_3Sn layer [7-11]. These voids raise reliability concern because excessive void formation increases the possibility of joint fracture. In addition, spalling of Cu_3Sn or $(Ni,Cu)_3Sn_4$ off Cu was observed between high-lead 95Pb5Sn solder and Cu or Ti/Cu/Ni under bump metallization (UBM) [12]-[13]. Accordingly, the electronic industry has attempted various techniques to reduce the IMC growth. An obvious approach is to solder at the lowest possible temperature for the shortest possible time [14]. The most successful technique is to coat Cu electrodes with a nickel (Ni) layer [2, 15]. Popular Ni coating methods are electrolytic plating process and electroless nickel immersion gold (ENIG) process. During the soldering process, molten Sn reacts with Ni to form Ni_3Sn_4, which grows much more slowly compared to Cu_6Sn_5 [15]-[16]. In extensive IMC growth, the entire Ni layer is consumed and turned into Ni_3Sn_4 which now sees Cu electrodes. Consequently, IMCs such as $(Ni,Cu)_6Sn_5$ and $(Ni,Cu)_3Sn$ show up [17].

In many applications, higher solder joint operating temperature provides an edge. A guideline for the maximum operation temperature of solder joints is at the homologous temperature of 0.8 [18]. At this temperature, even the aforementioned Ni coating method is not good enough. Thus, we searched for techniques that prevent IMC growth. Our preliminary results suggest that

the technique that we identified works. To evaluate this technique, alumina substrates with direct-bonded Cu (DBC) are selected for bonding study. Si chips are bonded to DBC alumina using fluxless Sn process. The samples are annealed at 182°C, corresponding to 0.9 homologous temperature of tin, for different times to investigate the IMC growth. The samples are then examined using scanning electron microscope (SEM) and energy dispersive X-ray (EDX). In what follows, the design concept and experimental procedures are presented. Experimental results are reported and discussed. A summary is then given.

8.2 Experimental Design and Procedures

The design concept is first presented. Our previous experimental results have shown that Sn strongly bonds to silicon (Si) chips coated with chromium (Cr) [19]-[21]. Sn atoms bond to Cr atoms without forming IMC at the Si/Cr/Sn interface. Fig. 8.1 exhibits the Cr-Sn phase diagram [22]. It is seen that Cr and Sn do not react to form intermetallics. The solubility of Cr in molten Sn is only 3×10^{-4} at. % at 232°C. Furthermore, The solubility of Sn in solid Cr is approximately 2 at.% Sn even at temperature as high as 1,374°C. Accordingly, Cr is selected as the barrier metal between Sn and Cu to inhibit IMC growth.

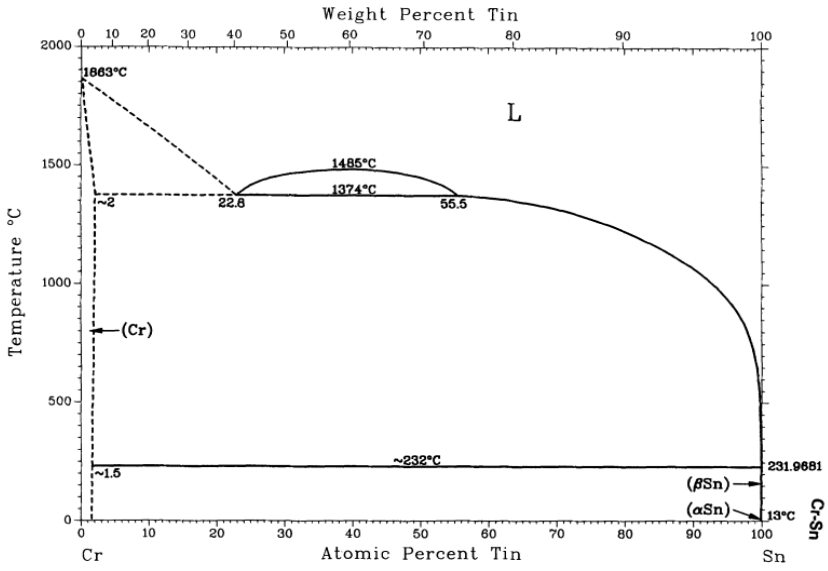


Fig. 8.1 The Cr-Sn binary phase diagram [22]

Alumina with direct-bonded Cu (DBC) is deposited with thin Cr and Cu layers. Cu substrates are also coated with thin Cr and Cu. The alumina substrate is bonded to the Cu substrate using fluxless Sn process. The samples are annealed at 182°C, corresponding to homologous temperature of 0.9 for Sn, for different times to evaluate the IMC growth. Cu substrates of 25.4 mm × 12.7 mm × 0.8 mm (width × length × thickness) are cut from 99.9% mirror-finished Cu sheet. Zirconium (Zr) doped alumina substrates of 15.66 mm × 20.07 mm × 0.25 mm (width × length × thickness) have direct bonded Cu (DBC) of 15.54 mm × 19.05 mm × 0.20 mm (width × length × thickness) on both sides. The Cu substrates and DBC alumina substrates are degreased with acetone and then etched in acetic acid at 35°C to remove native oxide. Both the Cu substrate and the DBC alumina substrate are deposited with Cr and Cu sequentially by E-beam evaporation

in a single run without breaking the vacuum. The Cr layer is employed as the barrier layer that blocks the liquid-solid reaction between molten Sn and the direct bonded Cu or between molten Sn and Cu substrate during the bonding process. Cr layer of different thickness is used to examine its blocking ability versus thickness. The thin Cu deposited over the Cr layer protects the Cr layer from oxidation and also acts as seed layer in the subsequent electroplating step. The Cu substrates with Cr/Cu are electroplated with 70 µm thick Sn in a stannous bath at 40°C. During the bonding process, the DBC alumina substrate and the as-plated Cu substrate are held together with two 50-µm-thick Cu spacers in between to control the Sn joint thickness. The assembly is mounted on a graphite platform inside a chamber. A pressure of 25 psi is applied on the assembly to ensure intimate contact. The chamber is pumped down to 80 millitorrs and the graphite platform was then heated. The bonding process is conducted between 227°C and 240°C with different reflow times. After bonding, the heater is turned off and the assembly is allowed to cool down naturally to room temperature in vacuum environment.

It is well known that IMCs form during the soldering process by liquid-solid reaction. The IMCs grow further during multiple solder reflows. Afterwards, the IMCs continue to grow during the service life of the electronic devices. This IMC growth during usage can be severe when the service temperature is high. To investigate the time-dependent solid-state IMC growth mechanism at the joint interfaces, several samples are subjected to accelerated aging test at various aging time

at 182°C, corresponding to Sn homologous temperature of 0.9. Table 8.1 lists a series of samples made with different Cr/Cu thicknesses, different reflow time, and various aging time. The microstructures are examined by scanning electron microscopy (SEM) equipped with a back-scattered electron (BSE) image detector. The chemical compositions are analyzed using energy dispersive X-ray spectroscopy (EDX). The bonded samples are mounted in epoxy, sectioned using slow speed diamond saw, ground with 800 and 1200 grit SiC paper and mechanically polished with alumina suspension to prepare the cross-section SEM samples.

8.3 Experimental results and discussion

In the first bonding design, designated as sample A in Table 8.1, the thickness of E-beam deposited Cr and Cu is 100 nm and 200 nm, respectively.

Table 8.1 Samples of DBC alumina substrate bonded to Cu substrate using fluxless Sn at 240°C reflow temperature

Sample designation	Cr thickness (nm)	Cu thickness (nm)	Reflow time (seconds)	Aging temperature (°C)	Aging time (hours)
A	100	200	290	-	-
B	500	100	180	-	-
C	500	100	180	182	10
D	500	100	180	182	100
E	500	100	180	182	200

The DBC alumina substrate was bonded to Cu substrates under the condition described in the previous section. Fig. 8.2 shows the cross-section SEM images of the sample.

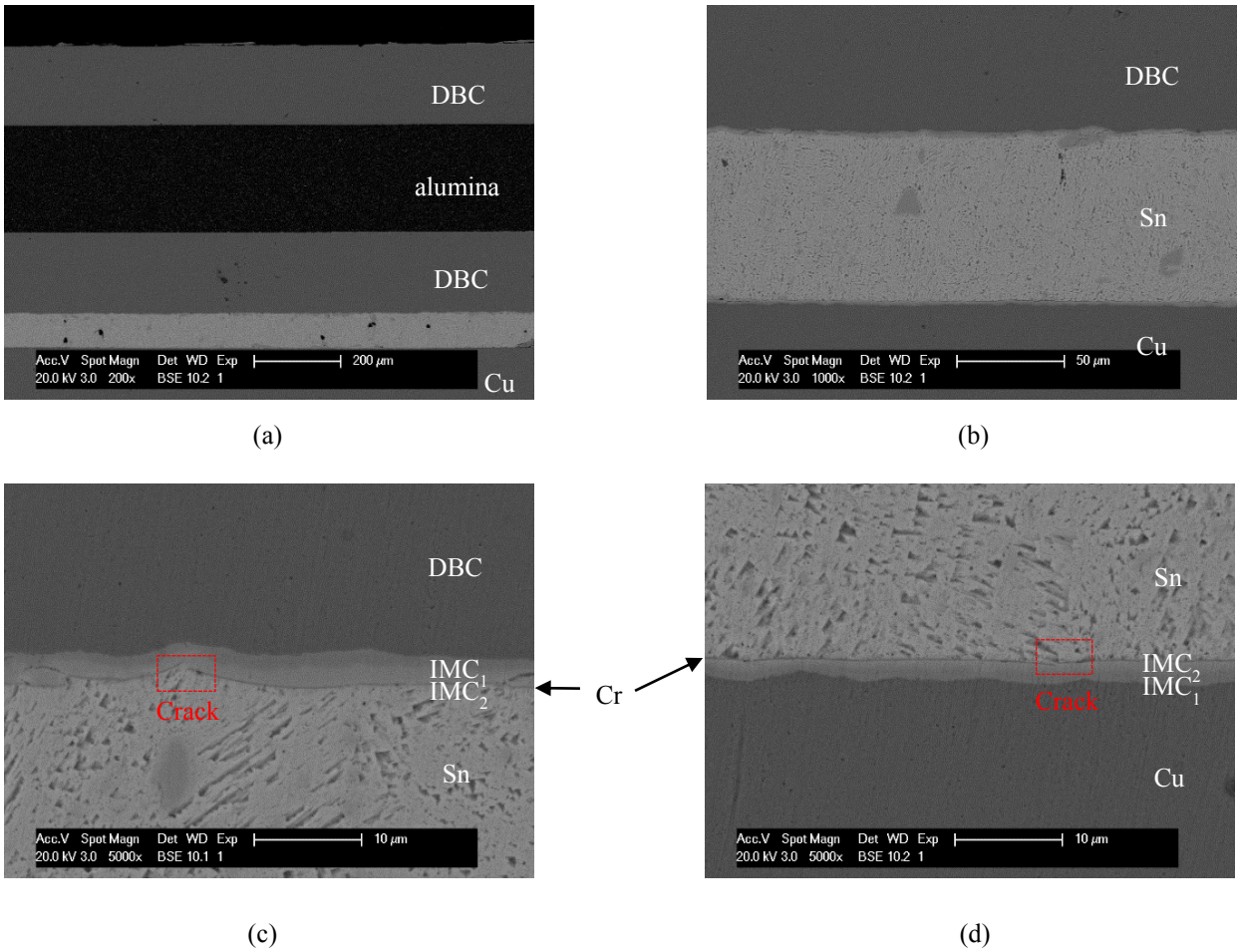


Fig. 8.2 Cross-section SEM images of sample A described in Table I at (a) low magnification (200×), (b) low magnification (1000×), (c) high magnification (5000×) at DBC/Cr/Sn interface, and (d) high magnification (5000×) at Sn/Cr/Cu substrate interface

As can be seen in Fig. 8.2(a), the DBC alumina substrate is well bonded to the Cu substrate. It is also observed that, in Figs. 8.2(c) and 8.2(d), IMC layers are formed at the DBC/Cr/Sn

interface and the Sn/Cr/Cu substrate interface. The IMC layer thickness is about 3 - 4 μm at the DBC/Sn interface and 2 - 3 μm at the Sn/Cu substrate interface. Each IMC layer includes two distinct sub-layers that are comprised of different IMCs. As indicated in Figs. 8.2(c) and 8.2(d), there are some cracks within the thin Cr layer. It was suspected that the cracks formed during the heating and cooling processes since there is considerable CTE mismatch between Cr and DBC alumina substrate or between Cr and Cu substrate. Table 8.2 lists the typical CTE values of the materials.

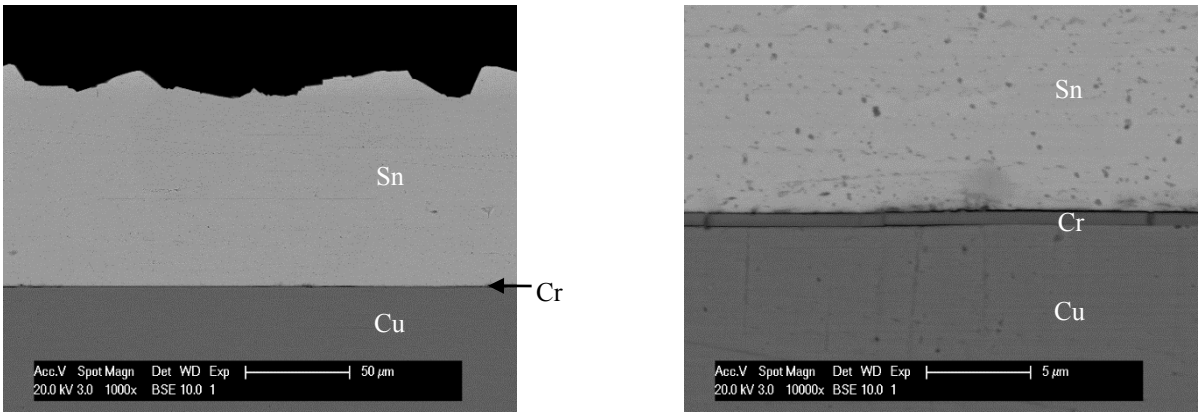
Table 8.2 Typical CTE values of the materials

Materials	Coefficient of thermal expansion (ppm/°C)
DBC alumina substrate	9.3
Cu substrate	17
Cr	4.9
Sn	22

Therefore, a Cr layer of 100 nm is too thin and too fragile to withstand the deformation because Cu has larger expansion or contraction than Cr during the soldering process. During the bonding process, the molten Sn penetrates through the cracks in the Cr layer to reach the Cu layer, thus forming IMC layers across the entire interfaces. This observation provides a clue that the Cr layer is indeed a critical factor.

To strengthen the Cr layer, its thickness was increased from 100 nm to 500 nm. Prior to

the bonding experiment, a Cu substrate E-beam deposited with 500 nm Cr and 100 nm Cu, and electroplated with 30 µm Sn layer was first examined using SEM. Fig 8.3 exhibits the cross-section images of an as-deposited sample.

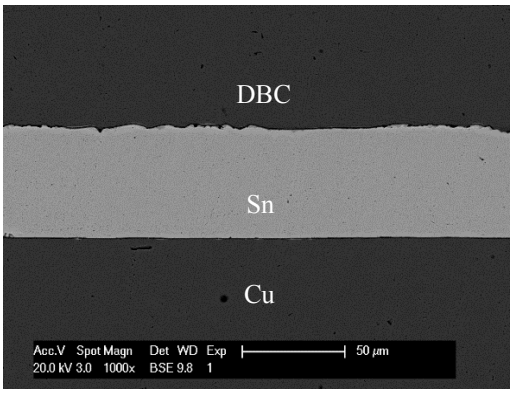


(a (b)

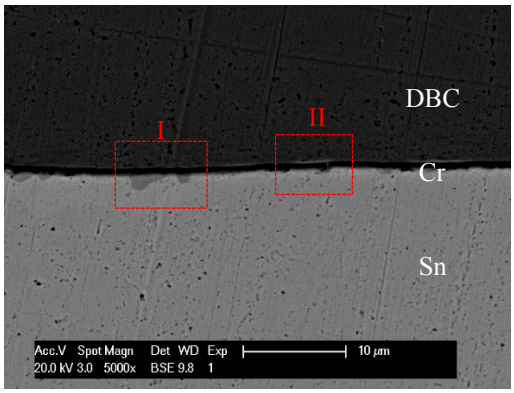
Fig. 8.3 Cross-section SEM images of a typical as-plated Cu substrate at (a) low magnification (1000×) and (b) high magnification (10000×). The substrate was E-beam deposited with 500 nm Cr and 100 nm Cu and was electroplated with 30 µm Sn

The 500 nm Cr layer between Sn and Cu substrate is clearly seen. Its thickness is uniform. The top surface of the electroplated Sn layer is uneven due to the limitation of the electroplating process. The second bonding design was then implemented. The sample was designated as sample B in Table 8.1. The DBC alumina substrate was bonded to Cu substrates under the similar condition as in sample A, whereas the reflow time was decreased from 290 seconds to 180 seconds. Fig. 8.4 presents the cross-section SEM images of sample B. No voids or gaps are found, indicating that the DBC alumina substrate is well bonded to the Cu substrate all over the cross section. It is worth noting that there is no distinct IMC layers formed at the interfaces. The IMC formation is localized at a few locations on the DBC/Cr/Sn interface. The locations are marked as type I and

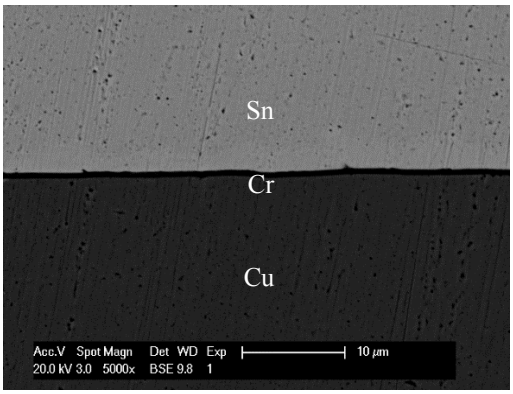
type II. Type I represents IMC formation between the Cr and Sn layers. It is caused by the diffusion of Cu atoms through a micro-crack or pinhole in the Cr layer to reach and react with the molten Sn. Type II represents IMC formation between the Cr and Cu layers. It is caused by diffusion of molten Sn through a micro-crack or pinhole in the Cr layer to reach the Cu layer and react with it. Other than a few localized IMC formations, there is no IMC along the interface between Cu and Cr and that between Cr and Sn. Fig. 8.5 displays the EDX element mappings of sample B. Fig. 8.6 depicts the schematics of the bonding mechanism.



(a)



(b)



(c)

Fig. 8.4 Cross-section SEM images of sample B described in Table I at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface

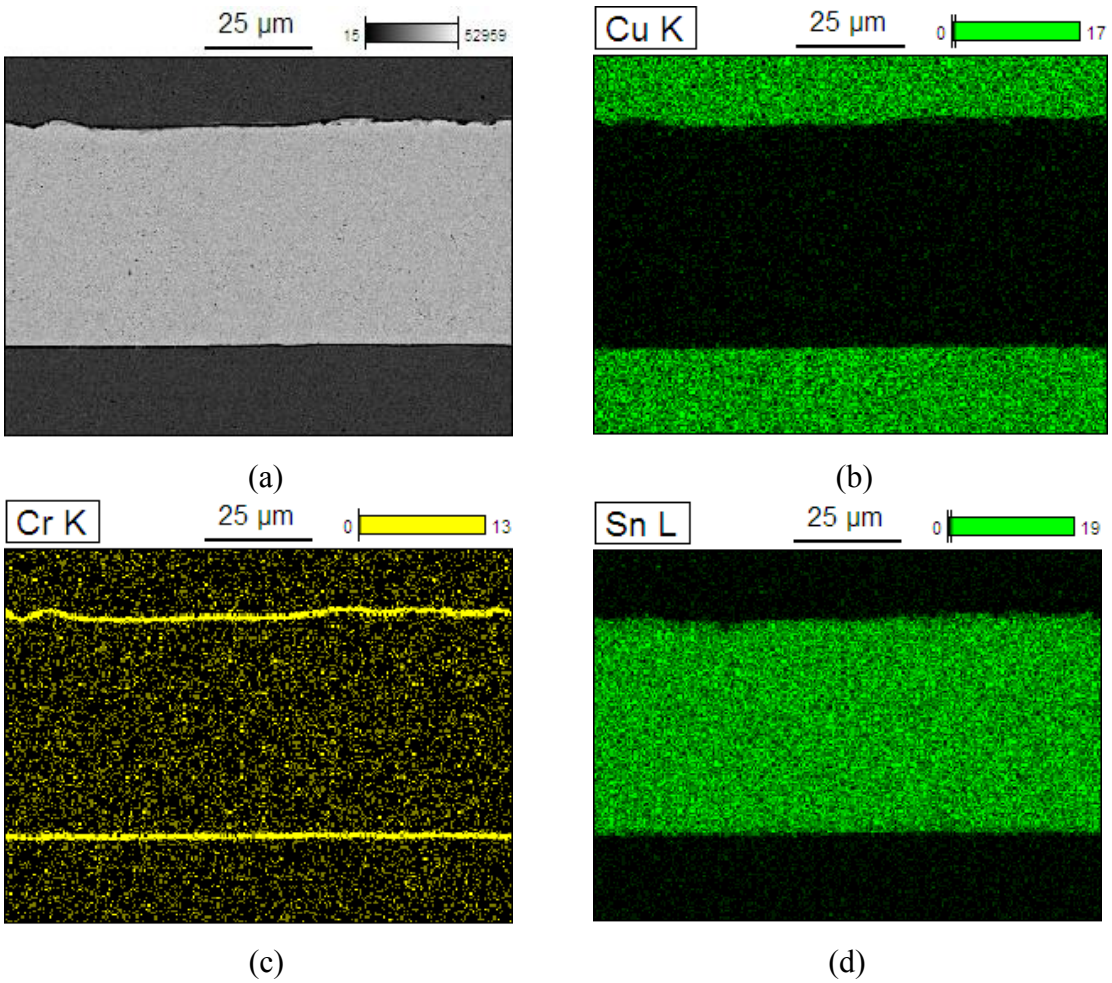


Fig. 8.5 Cross-section SEM image and element mappings of sample B described in Table 8.1 Distinct Cr layers on both interfaces are detected, suggesting that the Cr layer did not react with the molten Sn, as predicted by the Cr-Sn phase diagram, Fig. 8.1

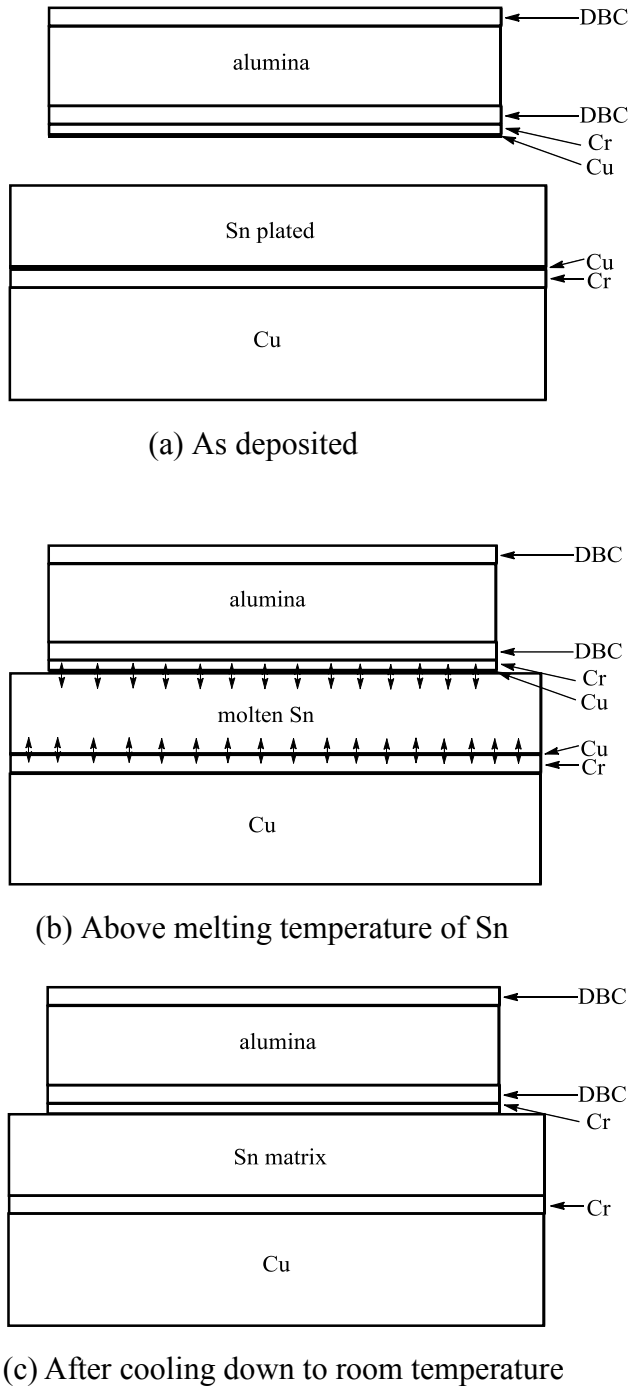
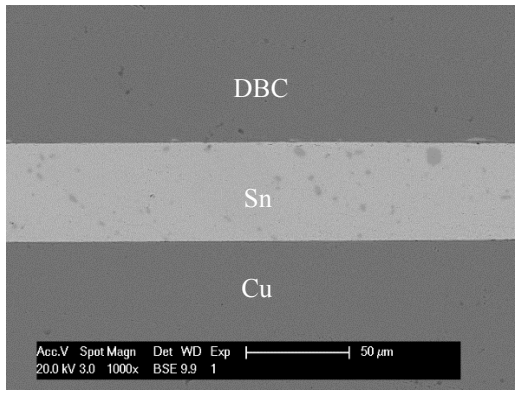


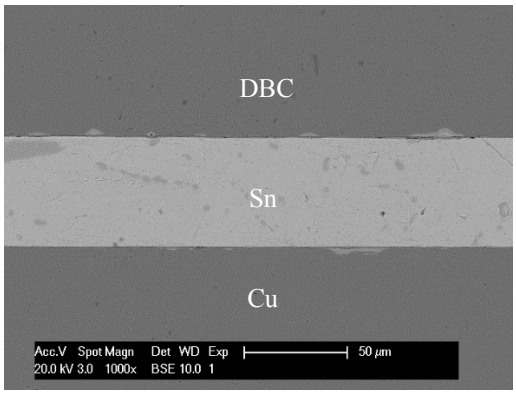
Fig. 8.6 Schematics illustrating the fluxless bonding mechanism

As temperature goes above Sn melting point, Sn melts and the molten Sn begins to react with thin Cu layers both on the DBC alumina layer and on the Cu substrate. At first, the molten

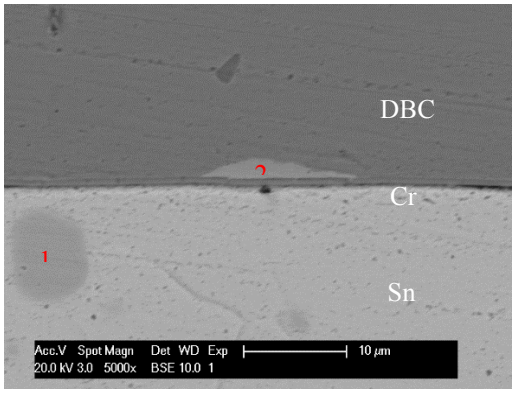
Sn dissolves the thin Cu layers and contacts the Cr layer and bonds to the Cr. It is noted that only when the thin Cu layer is dissolved in the molten Sn matrix would the fresh Cr layer be exposed to and bond to the molten Sn. No flux is needed to remove the native oxide on Cr because Cr was never exposed to the air either in the E-beam evaporation process or in the bonding process. Based on the Cr-Sn phase diagram [22], as shown in Fig. 8.1, there is no stable intermetallic phases exist in this system. Thus, the Cr layer can bond to Sn without forming IMC. As temperature goes down, solidification begins, resulting in a structure of DBC/alumina/DBC/Cr/Sn/Cr/Cu substrate, as illustrated in Fig. 8.6(c).To investigate IMC growth at high temperature, samples fabricated with the same procedures as sample B were subjected to aging test at 182°C with various times. This temperature corresponds to a homologous temperature $T_m = 0.9$ for Sn. Fig. 8.7 displays the cross-section SEM images of the sample aged for 10 hours. Fig. 8.7(a) shows one portion where the IMC formation occurs only at the DBC/Cr interface. Fig. 8.7(b) shows another portion where the IMC formation occurs at both interfaces.



(a)



(b)



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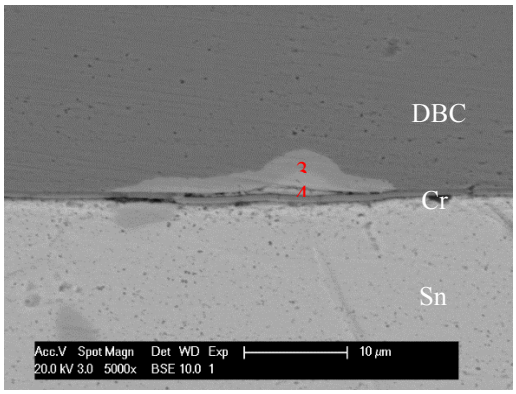
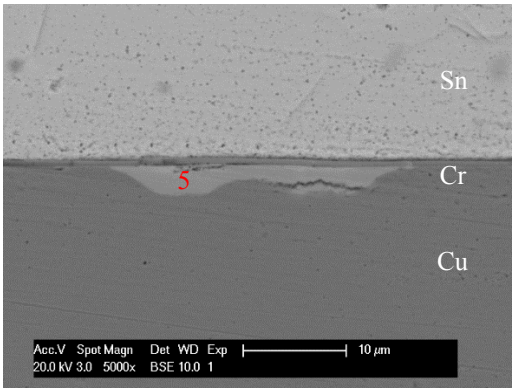


(d)



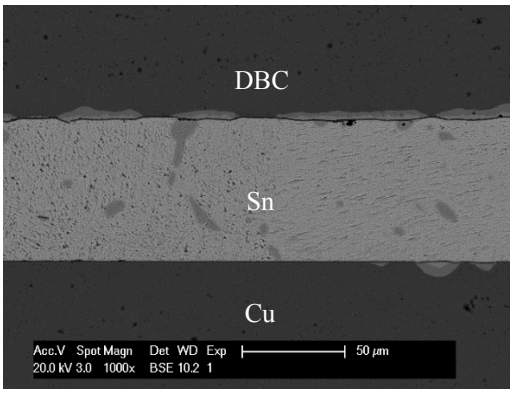
(e)

Region	Composition
1	Cu_6Sn_5
2	Cu_3Sn
3	Cu_3Sn
4	Cu_6Sn_5
5	Cu_3Sn

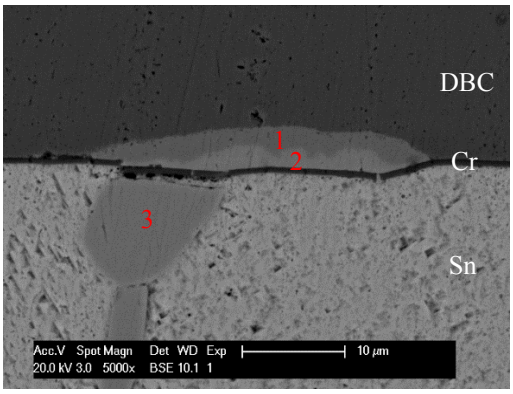
Fig. 8.7 Cross-section SEM images of sample C described in Table I at (a) low magnification (1000×) of the portion where IMC formation occurs only at DBC/Cr/Sn interface, (b) low magnification (1000×) of the portion where IMC formation occurs at DBC/Cr/Sn and Sn/Cr/Cu substrate interfaces, (c-d) high magnification (5000×) at DBC/Cr/Sn interface, and (e) high magnification (5000×) at Sn/Cr/Cu substrate interface

Based on the SEM images, IMC forms locally surrounding a micro-crack or a pinhole. It does not grow into an entire layer throughout the bonding interface. Figs. 8.7(c), (d), (e) show the IMC regions in more detailed. According to the EDX analysis, the IMC composition of region 1 inside the Sn joint corresponds to Cu_6Sn_5. This isolated IMC region was likely caused by the E-Beam deposited 200 nm Cu layers originally on Cr, which were dissolved by the molten Sn and reacted with it to form the IMC. The compositions of the IMC formed at region 2, 3 and 4 (the DBC/Cr interface) are Cu_3Sn, Cu_3Sn and Cu_6Sn_5, respectively, indicating that Cu_3Sn forms initially, followed by the formation of Cu_6Sn_5 during the solid-state IMC growth at the aging temperature. The only type of IMC formed at region 5 (the Cr/Cu substrate interface), is Cu_3Sn, which means that IMC growth is faster and more severe at the DBC/Cr interface than the Cr/Cu substrate interface.

Fig. 8.8 displays the cross-section SEM images of the sample aged at 182°C for 100 hours. The composition of the IMC formed at region 1, 5 and 6 is Cu_3Sn and the composition of the IMC formed at region 2, 3 and 4 is Cu_6Sn_5. It is clearly seen that the growth of IMCs at DBC/Cr and Cr/Cu substrate interfaces mainly continues in lateral direction and the size of Cu_6Sn_5 IMCs formed inside the Sn solder becomes larger.



(a)



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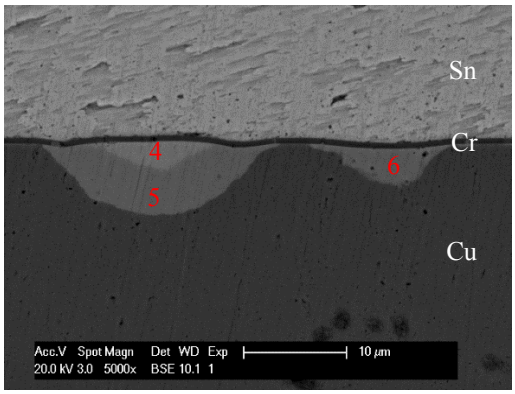


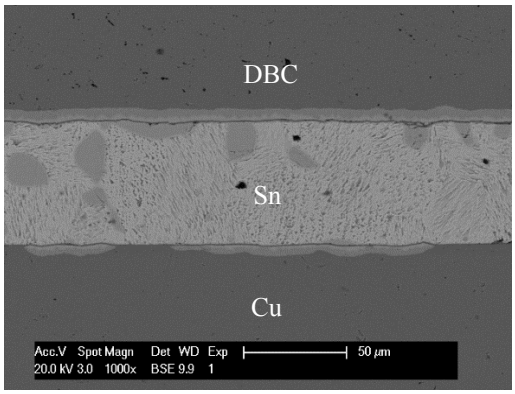
(c)

Region	Composition
1	Cu_3Sn
2	Cu_6Sn_5
3	Cu_6Sn_5
4	Cu_6Sn_5
5	Cu_3Sn
6	Cu_3Sn

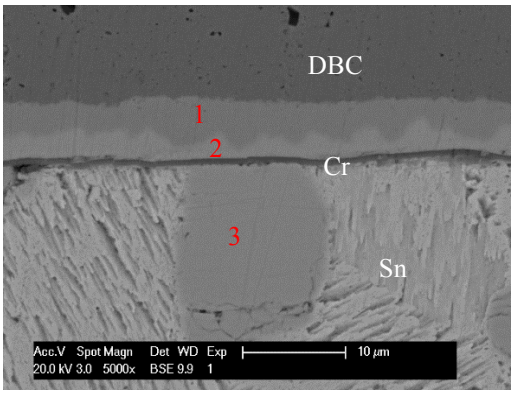
Fig. 8.8 Cross-section SEM images of sample D described in Table 8.1 at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface

Fig. 8.9 shows the cross-section SEM images of the sample aged at 182°C for 200 hours. The composition of the IMC formed at region 1 and 5 is Cu_3Sn and the composition of the IMC formed at region 2, 3 and 4 is Cu_6Sn_5. The IMC layer spreads out along the lateral direction at the boundary between DBC and Cr or between Cr and Cu substrate, but the rate of growth in vertical direction is not as fast as in lateral direction. It appears that Sn atoms diffuse through the micro-crack or the pinhole on the Cr layer and spread along the interface between Cr and Cu. The thickness of the IMC layer is around 7 µm. The micro-cracks and pinholes are probably caused by

surface defects and contaminations. Before depositing Cr and Cu layers in a vacuum chamber, the Cu substrates and DBC alumina samples were cleaned and prepared in a typical laboratory environment. Small surface defects and contaminations are very difficult to avoid. When Cr layer is deposited over these defects and contaminations, it does not bond and adhere to the underlying Cu. At the defect sites, the Cr film is weak and can be easily penetrated by the molten Sn during the bonding process and subsequent aging. In production environment, the defects and contaminations can be eliminated. Thus, there should be very few cracks and pinholes on the Cr layer. IMC formation caused by penetration of molten Sn through the cracks or pinholes, exhibited in Fig. 8.7, can be minimized.



(a)



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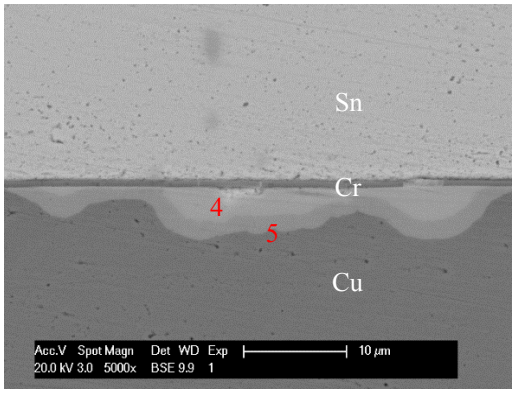

(c)

Region	Composition
1	Cu_3Sn
2	Cu_6Sn_5
3	Cu_6Sn_5
4	Cu_6Sn_5
5	Cu_3Sn

Fig. 8.9 Cross-section SEM images of sample E described in Table 8.1 at (a) low magnification (1000×), (b) high magnification (5000×) at DBC/Cr/Sn interface, and (c) high magnification (5000×) at Sn/Cr/Cu substrate interface

8.4 Summary

In this research, a fluxless bonding process between DBC alumina substrates and Cu substrates was developed with suppressed IMC formation at the bonding interfaces. It is a new process that deviates from the conventional soldering principle of requiring IMC formation as necessary condition of successful soldering. Numerous publications have reported that extensive IMC growth results in reduced solder joint reliability. This is particularly serious in flip-chip technology using solder bumps. In our high power electronic module project, we are looking to increase the operating temperature of solder die-attach to a homologous temperature of 0.8. For pure Sn solder, this corresponds to 131°C. High operating temperature allows us to raise the heatsink or coolant temperature. The hurdle of achieving high solder operating temperature is the extensive IMC growth. To suppress IMC growth at high temperature, Cr is selected as the barrier layer between Sn and the underlying Cu. After bonding, the Sn joints indeed have little IMC. After high temperature aging at 182°C for 100-200 hours, IMCs grow laterally along the Cr/Cu interface. Careful SEM and EDX evaluations have shown that the Sn atoms penetrate through micro-cracks

or pinholes on the Cr layer to reach Cu and react with the Cu. The Sn atoms further diffuse along the Cr/Cu interface to spread the IMC growth in the lateral direction. The 500 nm Cr layers are still there after the aging processes, indicating that Cr does not react with either Cu or Sn. The micro-cracks and pinholes are caused by defects that often stay on the substrate surfaces cleaned and prepared in a typical laboratory. In production environment, the micro-cracks and pinholes can be eliminated. Solder joints without intermetallic formation is thus potentially achievable.

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Chapter Nine

Summary

In this dissertation, fluxless bonding processes using electroplated Sn solder have been developed for different bonding designs. In contrast to the conventional soldering process, fluxless bonding technique eliminates any corrosion and contamination problems caused by flux. Without flux, it is possible to fabricate high quality joints in large bonding areas where the flux is difficult to clean entirely. It is of great importance to develop process to bond thermal expansion mismatch materials since shear stress produces in the bonded pair. Stress concentration at voids in joints could increases breakage probability. Sn was utilized as bonding medium in this research because it is soft and ductile. In addition, a new process of producing alumina film on aluminum substrate has been proposed to fabricate insulated metal substrate (IMS).

The research starts with the fluxless bonding of Si chip to aluminum substrate using electroplated Sn solder. The Al substrate was made solderable by coating with Cr and Cu. Si chip was deposited with Cr and Au. The joint thickness was controlled by bonding pressure or by using spacers. The SEM and EDX microscopic observations show that the joint is well-bonded and the Cu_6Sn_5 and Cu_3Sn IMCs are detected at the Sn/Cu interface. The joint strength was tested by shear test and all the samples passed the MIL-STD-883H, method 2019.8 standard.

A new anodization process is introduced to produce thick alumina film on aluminum substrate. The anodic alumina film is deposited with Cr and Cu by e-beam evaporation and electroplating to fabricate the Al/alumina/Cu insulated metal substrate. The electrical resistance and the breakdown of the alumina film are > 40 ΩM and 600 VDC, respectively. The reliability of the substrate was testified by thermal cycling test between -40ºC and +85ºC and high temperature storage test at 250ºC. In addition, Cu substrate was also bonded successfully to the Al/alumina/Cu insulated metal substrate using fluxless Sn bonding process.

Si chip is also bonded to low carbon steel substrate using the fluxless Sn bonding process. Ni was electroplated on low carbon steel substrate as the underbump metallurgy. Si chip was deposited with Cr and Au. The resulting joint is uniform after bonding and Ni_3Sn_4 IMC is formed at the Sn/Ni interface as examined by SEM and EDX analysis. The morphology of the Ni_3Sn_4 IMC is also revealed by etching Sn away from the joint. It is found that rod-shaped or polygonal-shaped Ni_3Sn_4 IMC is formed. The IMC thickness ranges from 5.1 to 8.4 μm.

Instead of using electroplated Ni on low carbon steel, we tried to electroplate Sn on low carbon steel directly and bond the Si chip on low carbon steel substrate without using any underbump metallurgy. It is observed that the joint is also well-bonded. $FeSn_2$ is the only IMC formed at the Sn/Fe boundary. It is worth noting that the IMC thickness in the Sn-Fe system is only 1.1 to 1.5 μm, which is much thinner than that in Sn-Ni system.

In order to investigate the growth behavior of the $FeSn_2$ IMC. The liquid Sn/solid Fe reaction couples were fabricated and annealed at different temperatures. Parabolic law and empirical power law were used to model the growth kinetics of $FeSn_2$ IMC. The growth constants, activation energy and time exponents were established at different annealing temperatures. It was found that the time exponent values obtained by fitting with empirical power law deviate from 0.5, meaning that volume (bulk) diffusion is not the only rate-controlling process in the liquid Sn/solid Fe reaction couple. Also, a variation in the time exponent values is indicative of the growth behavior is correlated with grain size growth and irregular grain morphology at different annealing stages.

We finally move to develop a process to suppress IMC formation using Cr as the barrier layer. In this research, several bonding experiments between direct-bonded Cu alumina substrate and the Cu substrate have been performed and the preliminary results show that high quality Sn joints could be produced with little IMC formation before high temperature aging. After aging at homologous temperature of 0.9 of Sn for 100-200 hours, Cu_6Sn_5 and Cu_3Sn IMCs are observed near micro-cracks or pinholes on the Cr layer. They are caused by penetration of molten Sn through micro-cracks or pinholes to react with the underlying Cu.