

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Palm et al.
U.S. Patent No.: 9,107,324 Attorney Docket No. 50095-0197IP1
Issue Date: August 11, 2015
Appl. Serial No.: 14/231,758
Filing Date: April 1, 2014
Title: CIRCUIT MODULE AND METHOD OF MANUFACTURING
THE SAME

DECLARATION OF DR. VIVEK SUBRAMANIAN

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: February 6, 2025

By: Vivek Subramanian

Vivek Subramanian, Ph.D.

Table of Contents

I.	ASSIGNMENT.....	4
II.	QUALIFICATIONS AND BACKGROUND INFORMATION.....	4
III.	LEGAL PRINCIPLES.....	8
	A. Anticipation	8
	B. Obviousness	9
	C. Claim Construction	10
IV.	PERSON OF ORDINARY SKILL IN THE ART	11
V.	MATERIALS CONSIDERED	12
VI.	OVERVIEW OF TECHNICAL TOPICS	21
	A. Zincating	21
VII.	OVERVIEW OF THE '324 PATENT	22
	A. Summary of the '324 Patent	22
	B. Prosecution History of the '324 Patent.....	27
VIII.	OVERVIEW OF THE CITED REFERENCES	28
	A. Overview of Sakamoto	28
	B. Overview of Eichelberger.....	34
	C. Overview of Chang.....	36
	D. Overview of Ito.....	37
	E. Overview of Tuominen.....	38
	F. Overview of Lee	39
IX.	GROUNDS 1A-102 and 1A-103: Claims 1-2, 4-11, 13-15, 17, and 19 are anticipated by or obvious over Sakamoto	42
	A. Analysis of Claims.....	42
X.	GROUND 1B: Claims 3 and 9-11 are obvious over Sakamoto in view of Eichelberger.....	82
	A. Analysis of Claims.....	82
XI.	GROUND 1C: Claims 9-11 are obvious over Sakamoto in view of Chang.....	88
	A. Combination of Sakamoto and Chang.....	88
	B. Analysis of claims.....	90
XII.	GROUND 1D: Claims 12, 13, and 15 are obvious over Sakamoto in view of Ito.....	90
	A. Analysis of claims.....	90
XIII.	GROUND 1E: Claims 15-16, 18, and 20 are obvious over Sakamoto in view of Tuominen.....	97
	A. Analysis of Claims.....	97

XIV. GROUNDS 2A, 2B: Claims 1-2, 4, 6-8, 10-12, and 15-20 are obvious over Lee or Lee in view of Sakamoto.....	99
A. Combination of Lee and Sakamoto	99
B. Analysis of claims.....	100
Ground 2B: Lee in view of Sakamoto renders obvious that the terminals 136 are composed of aluminum	104
Ground 2B: Lee in view of Sakamoto renders obvious that the third conductive layer 142 is composed of copper	117
Ground 2B: Lee in view of Sakamoto renders obvious that the second conductive layer 140 is electroless copper or electroless nickel	124
XV. GROUND 2B: Claims 5, 9, and 14 are obvious over Lee in view of Sakamoto	139
A. Analysis of claims.....	140
XVI. GROUND 2C: Claim 3 is obvious over Lee in view of Eichelberger (and optionally further in view of Sakamoto)	147
A. Analysis of claim 3	148
XVII. GROUND 2D: Claims 13 and 15 are obvious over Lee in view of Ito (and optionally further in view of Sakamoto)	150
A. Analysis of claims.....	150
XVIII.....GROUND 2E: Claims 15-16, 18, and 20 are obvious over Lee in view of Tuominen (and optionally further in view of Sakamoto).....	155
A. Analysis of claims.....	155
XIX. CONCLUSION.....	159

I, Dr. Vivek Subramanian, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of Apple (“Apple” or “Petitioner”). I understand that Apple is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 9,107,324 (“the ’324 Patent”) (APPLE-1001). I have been asked to provide my independent analysis of the ’324 Patent in light of the prior art publications cited below.

2. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’324 Patent, the prior art publications cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’324 Patent.

II. QUALIFICATIONS AND BACKGROUND INFORMATION

3. I have summarized in this section my educational background, career history, and other qualifications relevant to this matter. I have also included a current version of my curriculum vitae as APPLE-1004.

4. I am currently a Professor of Electrical and Microengineering at EPFL (École polytechnique fédérale de Lausanne) in Switzerland. Until 2020, I was a Professor of Electrical Engineering and Computer Sciences at the University

of California, Berkeley; I still maintain an adjunct professorship there while I graduate my remaining PhD students and complete my academic commitments to Berkeley.

5. I received a Bachelor's degree summa cum laude in electrical engineering from Louisiana State University in 1994. As an undergraduate, I performed research on various aspects of microelectronics. My research as an undergraduate resulted in several publications in international journals.

6. I received an M.S. and Ph.D. in electrical engineering, in 1996 and 1998, respectively, from Stanford University. As a graduate student at Stanford University, I received an Eastman Kodak fellowship from Kodak. During my MS / PhD, I worked as a research assistant in the Center for Integrated Systems at Stanford. From 1994 to 1998, I performed research in high-performance thin film transistors for high-performance 3D integrated logic, memory, and display applications.

7. Upon completing my PhD, I held three appointments simultaneously between 1998 and 2000. Between 1998 and 2000, I served as a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University, and as a Visiting Research Engineer in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, where my research focused on 25nm metal oxide semiconductor field effect

transistor (MOSFET) design and fabrication. I worked on technologies for high-performance transistor processes, and published several papers as a direct outcome of this technology development.

8. In July of 2000, I became an assistant professor in the University of California, Berkeley's Department of Electrical Engineering & Computer Sciences. In 2005, I was promoted to the position of tenured Associate Professor of Electrical Engineering & Computer Sciences at the University of California, Berkeley, and, in July of 2011, I was promoted to full Professor of Electrical Engineering and Computer Sciences. I was also responsible for all the semiconductor device and technology courses offered within the department. I taught these courses routinely, including both undergraduate and graduate courses. I also actively performed research in the area of semiconductor packaging, and have published journal articles and conference proceedings on the same.

9. In August of 2018, I became a professor at EPFL (École polytechnique fédérale de Lausanne) in Switzerland. Here, I perform teaching and research activities on advanced microsystems and electronics. I continue to maintain some research activities in the area of semiconductor packaging.

10. My research and teaching have focused on microelectronics for the majority of my professional career. I have co-founded companies working on electronic products, including Matrix Semiconductor Inc., Kovio, Inc. and Locix

Inc. All of these companies produced packaged semiconductor products and I was directly involved in the packaging technology scouting and development therein.

11. I have also authored or co-authored over 200 technical papers in international journals and conferences and have been named inventor or co-inventor on more than 60 patents covering several aspects of electronic systems, including packaging.

12. In the course of my educational and professional activities, I have become familiar with the state of the art in the field of electronics technologies during the late 1990s, early 2000s and beyond.

13. A detailed list of my other professional activities, memberships, and speaking engagements is included in my CV, which is attached as APPLE-1004.

14. Based on my experience and education, I believe that I am qualified to opine as to the knowledge and level of skill of one of ordinary skill in the art at the time of the alleged invention of the '324 Patent (which I further describe below) and what such a person would have understood at that time, and the state of the art during that time. Based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the 2000s and specifically during the time of the alleged invention of the '324 Patent. Indeed, I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

III. LEGAL PRINCIPLES

15. I have been informed about certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

A. Anticipation

16. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed limitations, it anticipates.

17. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (the so-called critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. § 102(e), if an invention described by that claim was described in a U.S.

patent granted on an application for a patent by another that was filed in the U.S.
before the date of invention for such a claim.

B. Obviousness

18. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others.

19. The '324 Patent was filed on April 1, 2014 claiming priority to PCT Application No. PCT/FI2009/050383, filed on May 11, 2009, and further to Finnish Application No. 20085443, filed on May 12, 2008. APPLE-1001, Cover. For purposes of my analysis here, I have applied a date of May 12, 2008 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than May 12, 2008.

20. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference or references themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and may be explicit or implicit from the prior art as a whole. I have been informed that the predictable combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

21. I understand that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the

claims, the specification, and the file history may be used to better construe a claim. I have followed this approach in my analysis.

22. I have also been informed that, according to 35 U.S.C. § 112, a patent claim may lack written description if the specification and earlier-filed priority applications fail to describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application and that the patentee invented what is claimed. I understand that even if a description would render obvious a claimed invention, such obviousness is not sufficient to satisfy the written description requirement for that claim. I have also been informed that a patent claim may be indefinite if, read in light of the specification and prosecution history, it fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

23. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). I have used the date of May 12, 2008 for reasons explained in Section III.B. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the early to mid-2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

24. A person of ordinary skill in the art at the time of the '324 Patent (a "POSITA") would have had a bachelor's degree in electrical engineering, material science, applied physics, or a related field, and at least three years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent, with additional education substituting for experience and vice versa. In view of the pertinent prior art discussed herein, my analysis would be the same applying a slightly higher or lower level of skill.

25. I have used May 12, 2008 as the point in time from which my analysis from the perspective of a POSITA is based, but my analysis would be similar even if the date was slightly earlier or later.

V. MATERIALS CONSIDERED

26. My analyses set forth in this declaration are based on my experience in the field of integrated circuit (IC) chips and packaging. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experiences, I understand and know of the capabilities of persons of ordinary skill in this field during the early- to mid-2000s and specifically during the time before the alleged priority date (May 12, 2008) for the '324 Patent, and I taught, participated in organizations, and worked closely with many such persons in the field during that time frame.

27. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the critical date for the '324 Patent; my own knowledge and experiences gained from my work experience in the field; and my experience in working with others, including teaching and advising others in the field. In addition, I have analyzed and utilized the following publications and materials:

- 28. APPLE-1001 U.S. Patent No. 9,107,324 (“the '324 Patent”)
- 29. APPLE-1002 U.S. Patent No. 9,107,324 File History
- 30. APPLE-1005 U.S. Patent Application Publication No. 2004/0168825 (“Sakamoto”)
- 31. APPLE-1006 U.S. Patent No. 6,396,148 (“Eichelberger”)
- 32. APPLE-1007 Green, T.A., “Gold electrodeposition for microelectronic, optoelectronic and microsystem applications.” *Gold Bull* 40, 105–114 (2007) (“Green”)
- 33. APPLE-1008 Chang, Shou-Yi, et al. “Integrated electrochemical deposition of copper metallization for ultralarge-scale integrated circuits.” *Journal of The Electrochemical Society* 151.1 (2003) (“Chang”)

34. APPLE-1009 Qi, Guojun, et al., “Zincating morphology of aluminum bond pad: its influence on quality of electroless nickel bumping.” *Thin Solid Films*, Volume 406, Issues 1–2 (2002) (“Qi”)
35. APPLE-1010 Arshad, M. et al., “The effects of zincation process on aluminum bond pad surfaces for electroless nickel immersion gold (ENIG) deposition,” *2004 IEEE International Conference on Semiconductor Electronics, Kuala Lumpur, Malaysia* (2004)
36. APPLE-1011 Lee, Sung-Ki et al., “A study on the nucleation behavior of zinc particles on aluminum substrate,” *Advances in Electronic Materials and Packaging* (2001)
37. APPLE-1012 U.S. Patent Application Publication No. 2007/0126030 (“Ito”)
38. APPLE-1014 International Patent Application Publication No. 2006/056643 (“Tuominen”)
39. APPLE-1015 U.S. Patent Application Publication No. 2008/0032447 (“Lee”)
40. APPLE-1016 U.S. Patent No. 4,246,595 (“Noroyi”)
41. APPLE-1017 Yung, W et al., “CO₂ laser drilling of micro-via without conformal mask in PCB manufacture.” *Proceedings of the 1st Pacific International Conference on Laser Materials Processing, Micro, Nano and*

Ultrafast Fabrication. PICALO (2004): 1st Pacific International Conference on Laser Materials Processing, Micro, Nano and Ultrafast Fabrication. Melbourne, Australia.

42. APPLE-1018 File history of U.S. Application No. 12/990,785
43. APPLE-1019 Hsu, S. (2015). Fluxless Tin Bonding Processes with Intermetallic Study and Aluminum Circuit Board Technology. *UC Irvine*.
44. APPLE-1020 Coombs, C. Printed Circuit Handbook (Sixth Edition), McGraw-Hill Companies (2008).
45. APPLE-1021 Weste, N. and Esraghian, K., Principles of CMOS VLSI Design, Addison-Wesley Publishing Company (1988).
46. APPLE-1022 Goh, W. et al., “The use of electroless copper seed in electrochemical deposited copper interconnect,” *Thin Solid Films* 462–463, (2004): 275-278
47. APPLE-1023 Kulkarni, A. K., and C. Lai. “New models for ohmic contacts to GaAs.” *Thin Solid Films* 164 (1988): 435-439.
48. APPLE-1024 Excerpt from Keller, H. and Erb, U., *Dictionary of Engineering Materials*, John Wiley & Sons, Hoboken, NJ (2004)
49. APPLE-1025 Excerpt from Kaplan, S., *Wiley Electrical and Electronics Engineering Dictionary*, John Wiley & Sons, Hoboken, NJ (2004)

50. APPLE-1026 Rossnagel, S, “Directional and preferential sputtering-based physical vapor deposition,” Thin Solid Films 263 (1995): 1-12

51. APPLE-1027 U.S. Patent No. 7,067,911

52. APPLE-1028 Bauer, M. and Schneider, J., “Adhesives in the Electronics Industry,” published in *Handbook of Adhesive Technology* (Second Edition), Marcel Dekker, New York, NY (2003)

53. This declaration refers to selected portions of the cited references for the sake of brevity. These references are examples. It should be understood that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entirety. Of course, I have also considered the claim of the '201 patent. The following table provides a quick sheet enumerating claim elements for ease of reference:

Claim 1	
[1pre]	Circuit module, comprising
[1a]	a first insulator layer having a first surface and a second surface;
[1b]	at least one second insulator layer on the first surface;
[1c]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing a first metal,

[1d]	conductors on the second surface of the first insulator layer, the conductors comprising at least a first layer and a second layer, in such a way that at least the second layer contains a second metal, and
[1e]	contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal,
[1f]	a contact surface area ($A_{\text{CONT 1}}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal.
Claim 2	
[2]	The circuit module of claim 1, wherein the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.
Claim 3	
[3]	The circuit module of claim 1, wherein the first metal is gold, the second metal is copper, and the third metal is nickel.
Claim 4	
[4]	The circuit module of claim 1, wherein the intermediate layer comprises a layer containing zinc.
Claim 5	
[5]	The circuit module of claim 1, wherein the intermediate layer comprises a layer containing copper.
Claim 6	
[6]	The circuit module of claim 1, wherein the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium.
Claim 7	

[7]	The circuit module of claim 1, wherein the intermediate layer extends along the side walls of the contact elements between the contact terminals and the conductors.
Claim 8	
[8]	The circuit module of claim 1, wherein each contact element comprises a copper core, which connects continuously to the material of the second layer of the conductors.
Claim 9	
[9]	The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, and a second layer of copper on the surface of the first copper layer.
Claim 10	
[10]	The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.
Claim 11	
[11]	The circuit module of claim 10, wherein the intermediate layer between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.
Claim 12	
[12]	The circuit module of claim 1, wherein a width (WCONT) of the contact surface between the contact element and the contact terminal of the component is 0-20% less than a greatest width (WMAX) of the contact element in the same direction.
Claim 13	
[13]	The circuit module of claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (WMAX) of the contact element.

Claim 14	
[14]	The circuit module of claim 1, wherein the at least one second insulator layer contains at least one layer of fibre material and an opening in the fibre material for the at least one component.
Claim 15	
[15]	The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.
Claim 16	
[16]	The circuit module of claim 15, wherein the polymer layer comprises layer of a hardened adhesive.
Claim 17	
[17pre]	Circuit module, comprising
[17a]	a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;
[17b]	a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer covering the first surface of the conductors;
[17c]	at least one second insulator layer on the first surface of the first insulator layer;
[17d]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal;
[17e]	contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,

[17f]	a contact surface area (ACONT 1) between the intermediate layer and the contact terminal being less than a surface area (APAD) of the contact terminal;
[17g]	at least one layer of metal in the contact terminals containing a first metal; at least one layer of metal in the conductors containing a second metal; and the intermediate layer containing a third metal.
Claim 18	
[18]	The circuit module of claim 17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.
Claim 19	
[19pre]	Circuit module, comprising
[19a]	a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;
[19b]	a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer entirely covering the first surface of the conductors;
[19c]	at least one second insulator layer on the first surface of the first insulator layer;
[19d]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal; and
[19e]	contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,
[19f]	a contact surface area (ACONT 1) between the intermediate layer and the contact terminal being less than a surface area (APAD) of the contact terminal.

Claim 20	
[20]	The circuit module of claim 19, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

VI. OVERVIEW OF TECHNICAL TOPICS

A. Zincating

54. Because substantial parts of the following discussion involve the “zincating” process, I provide here an overview of that topic. Zincating (or zincation) is a “widely used process” for aluminum contact pads. APPLE-1009, 1. “Aluminum [] is the dominant material for IC bond pad metallization. [] However, as aluminum instantaneously oxidizes during rinsing or exposure to air, the oxide films will completely suppress metallization or prevent the formation of intermetallic bonds between the EN [electroless nickel] and substrate, resulting in adhesion failure. Zincating of the aluminum pads is a widely used process step that activates the pads for subsequent EN deposition.” *Id.* “Zincation rel[ies] on the electrochemical exchange reaction between zinc ion in solution and aluminum metal to deposit zinc metal at the expense of aluminum dissolution []. Zincation is currently one of the most suitable processes to activate the aluminum surface for electroless technique []. Once this process is performed, aluminum coated with zinc then can be electroless plated by nickel.” APPLE-1010, 2. This is an “essential step to make aluminum pads actives [sic] for subsequent electroless

nickel plating.” APPLE-1011, 1. As a result, a zincated aluminum terminal electrode includes a “contact portion” composed of a “zinc layer” “about 0.3 μm ” thick at the top of the aluminum electrode. APPLE-1012, [0063], [0091].

55. Zincation is a “self-aligned” process, meaning that zinc is deposited selectively on aluminum and not deposited, or essentially not deposited, on many other materials. For example, Ito describes that, because zinc seed layers are formed in a self-aligned manner on aluminum contacts, and electroless nickel is subsequently formed self-alignedly on the zinc, “no patterning step is needed and the manufacturing process can be simplified.” APPLE-1012, [0065]-[0066], [0096]. Similarly, APPLE-1019 describes that “[t]he zincation process dissolves the surface aluminum oxide and deposits zinc (Zn) through electrochemical exchange reaction in alkaline zincate solution. Nonetheless, Zn deposition stops when the Al substrate is all covered with Zn. As a result, the zinc layer deposited is thin ‘20-50 nm’ and multiple zincation operations are necessary for better surface uniformity and adhesion strength.” APPLE-1019, 43.

VII. OVERVIEW OF THE ’324 PATENT

A. Summary of the ’324 Patent

56. The ’324 Patent relates to multi-chip circuit modules and purports to provide improvements for contacting these circuit modules and their chips.

APPLE-1001, 3:10-4:41, FIG. 9. The authors of the ’324 Patent describe that there

are difficulties in forming contacts between aluminum and copper, and that “[a]n improved possibility [is] to use contact areas of aluminium.” APPLE-1001, 2:6-7. For example, the ’324 Patent describes that “contact between copper and aluminium is brittle, so that a module of this kind is not optimal in applications, in which mechanical stress acts on the circuit module.” APPLE-1001, 2:3-5.

57. The Background of the ’324 Patent notes that previous work included the deposition of titanium, chromium, or nickel layers on aluminum contacts. *Id.*, 2:30-65. The sputter deposition of titanium and chromium is described as “expensive” and as reducing “conducting density.” APPLE-1001, 2:42-47. The nickel deposition disclosure discussed in the Background is Eichelberger (APPLE-1006), which I have considered at length below in analyzing the obviousness of the ’324 Patent’s claims. According to the ’324 Patent, Eichelberger describes an “electroless plating method” in which nickel is grown “on the surface of the aluminium contact areas.” APPLE-1001, 2:51-56. The ’324 Patent describes no downsides or drawbacks associated with this method. APPLE-1001, 2:51-65

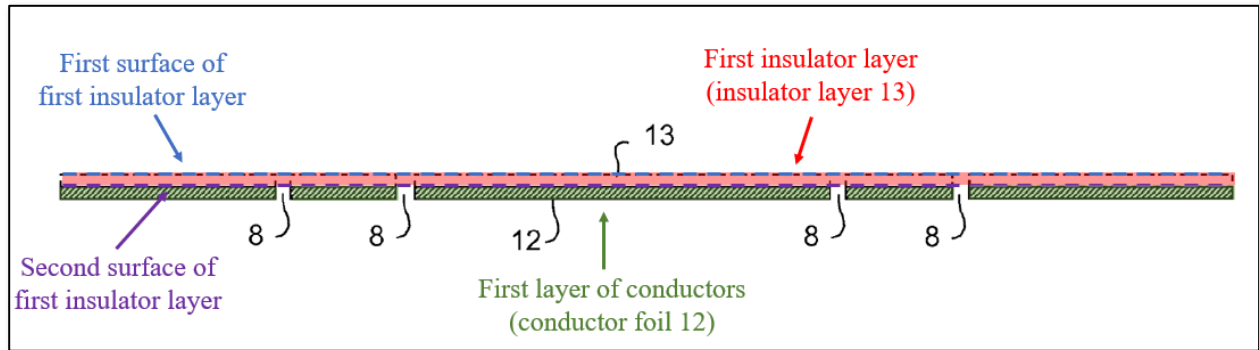
58. According to the ’324 Patent, the use of “contact holes [] dimensioned in such a way that the contact surface area [] is smaller than the total surface area of the contact area” provides improved alignment and permits the use of a laser for opening contact holes. *Id.*, 3:27-41, 4:21-25. As I discuss below with respect to

claim 1 in Ground 1A, this configuration was well-known and common in the art from well before the claimed priority date of the '324 Patent.

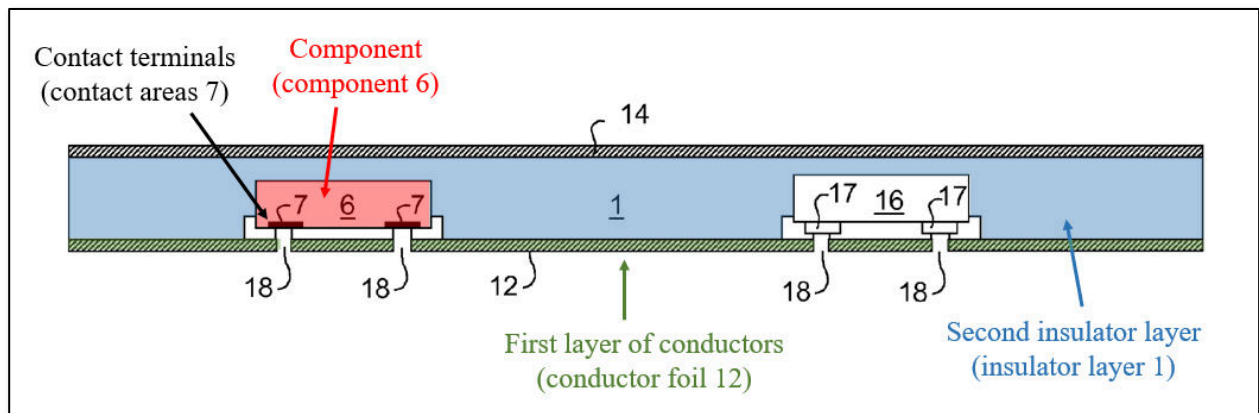
59. The '324 Patent also describes that certain combinations of materials (e.g., “a layer containing zinc on the surface of an aluminium contact area”) can be advantageous, for example, in obtaining “good adhesion.” APPLE-1001, 3:14-26, 3:55-4:5. For example, the '324 Patent notes that “extremely good mechanical durability is achieved by using a double zincate process.” EX-1001, 3:64-65. As I discuss in Section VI.A and in reference to [11] of Ground 2A, the zincate process was already well-established and common for metallizing aluminum contacts as of the priority date of the '324 Patent.

60. Claim 1 of the '324 Patent appears to be represented by FIGS. 1, 4 and 29. *See* APPLE-1001, 22:5-24:36. In FIG. 29, first, second, and third intermediate layers 33, 34, and 35 (described as together constituting an “intermediate layer 2”) are arranged on an “aluminum” contact area 7. *Id.*, 20:6-45. Layer 33 is formed “using a chemical growing method to grow a layer containing zinc,” which “grows only on the base part 36” because the conductor foil 12 is composed of copper. *Id.*, 28-33. This likely refers to the zincation process noted in ¶59, which grows a zinc layer selectively on the underlying aluminum contact area 7 and not on exposed copper of the conductor foil 12. Intermediate layers 34, 35 are composed of chemically-grown nickel and copper, respectively. APPLE-1001,

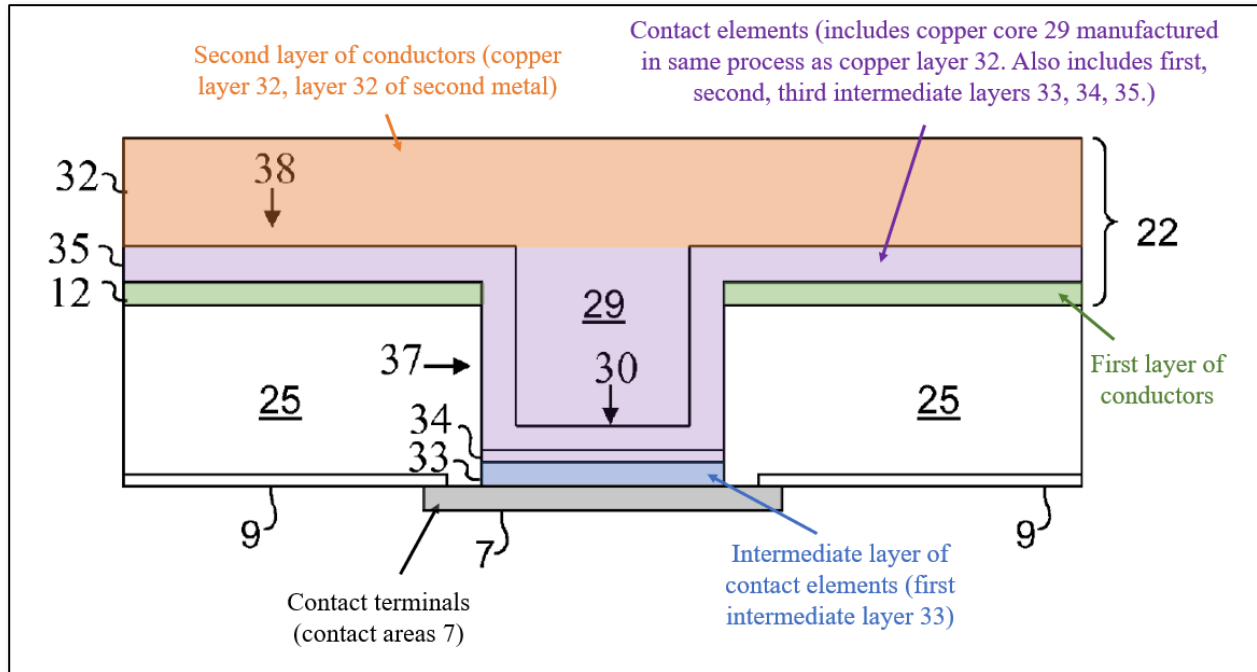
20:33-41. As such, the '324 Patent uses a multilayer structure to make an electrical connection to an aluminum contact. This structure and the corresponding elements of FIG. 29 are shown below. *See* APPLE-1001, 22:5-24:36.



Annotated '324 Patent FIG. 1



Annotated '324 Patent FIG. 4



Annotated '324 Patent FIG. 29

61. In this structure, copper “made using an electrochemical growing method” forms both “a copper core 29” and a “second layer 32” “manufactured in the same process,” so that the copper core 29 and the and the second layer 32 (or “copper layer 32”) “connect[] continuously” and “there is no interface between them.” APPLE-1001, 23:29-39. The copper core 29 is included in the contact elements. *Id.*

62. An “insulator layer 13,” shown in FIG. 1, corresponds to the “*first insulator layer*” of the claims. The insulator layer 13 is included in “a layered sheet, which comprises a conductor foil 12 and [the] insulator layer 13,” where the conductor foil 12 can be a copper foil (“copper film”) and the insulator layer 13 can be “a tape-like surfacing” or “a polymer or similar material that is shapeable at

least in its surface part.” APPLE-1001, 5:9-17; 24:4-6. The ’324 Patent describes that “[i]n the embodiments described in the following, it is possible to use such a layered sheet 12, 13 in place of the conductor foil 12.” APPLE-1001, 5:17-19. Based on this description and the claims, a POSITA would have understood that the claims are directed to embodiments that include the insulator layer 13 as the “*first insulator layer*.” See also the ’324 Patent’s description that the “polymer layer 25 [shown in FIG. 29 above] can contain, for example, an insulator layer 13 depicted in connection with FIG. 1.” APPLE-1001, 19:27-28.

B. Prosecution History of the ’324 Patent

63. U.S. 9,107,324 issued on July 17, 2012 from U.S. Patent Application No. 12/699,628, which was filed on February 3, 2010. See APPLE-1002. Not even a single Office Action was issued during prosecution of the ’324 Patent, and I note that the prior art analyzed here was never used in any rejection of the claims. See APPLE-1002

64. The Examiner’s reasons for allowance pointed to the limitation “contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal, a contact surface area ($A_{cont\ 1}$) between the intermediate layer and the contact terminal being less than a surface area (A_{pad}) of the contact terminal,” stating that

this limitation “was neither found to be disclosed in nor suggested by the prior art.”

APPLE-1002, 17. However, based on my knowledge and experience, and my review of the publications I discuss in more detail below, I do not agree that the ’324 Patent’s claims are patentable over the prior art. The Examiner apparently failed to fully consider the relevant art discussed herein, such as Sakamoto, Lee, and Eichelberger. Those of skill in the art were aware of circuit modules that shared ’324 Patent’s claims’ recited combinations of layers, metals, contact structures, and the like.

VIII. OVERVIEW OF THE CITED REFERENCES

A. Overview of Sakamoto

65. Sakamoto (US 2004/0168825) describes “a structure capable of electrically connecting a multilayer printed circuit board to an IC chip without using leads and a sealing resin by [] building up a plurality of interlayer insulating layers, providing via holes on the die pads [] by photoetching or laser, [and] forming conductor circuits serving as conductive layers.” APPLE-1005, [0009]. Sakamoto emphasizes the presence of “a transition layer consisting of at least two-layer structure on the die pad of the IC chip” to provide improved alignment and to protect the die pad during fabrication. *Id.*, [0011]-[0016]. This multilayer structure follows the same approach as in the ’324 Patent, e.g., as in FIG. 29 discussed above. For example, Sakamoto’s transition layer 38 on top of aluminum die pads

24 “consists of three layers” 33, 36, and 37, and similarly the ’324 Patent describes three “intermediate layers” 33, 34, and 35 on top of aluminum contact areas 7.

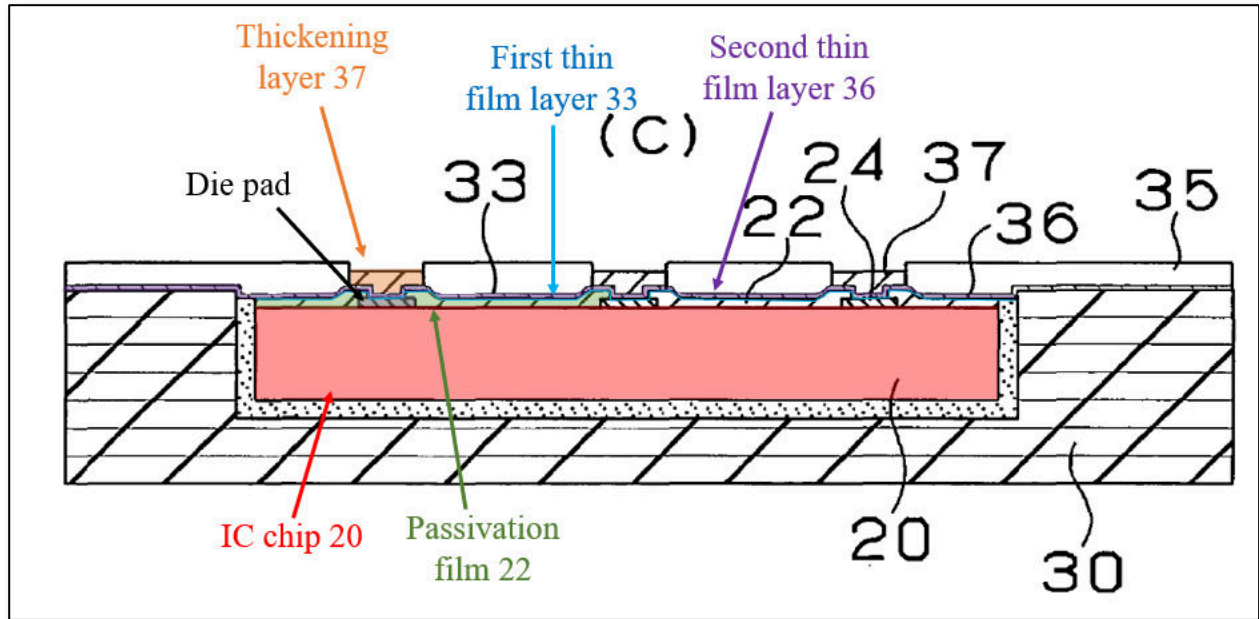
APPLE-1005, [0101]; APPLE-1001, 20:26-45.

66. Portions of Sakamoto refer to the desirability of having a transition layer that is larger than the underlying die pad. APPLE-1005, [0016], claim 7. However, FIG. 7 makes clear that the transition layer 38 has a varying width that is narrowest at the bottom (adjacent to the die pad 24) and widens at the top. The via hole in which the transition layer 38 is formed (and therefore the contact area between the transition layer 38 and the die pad 24) is **narrower** than the die pad 24, not wider, as shown at least by par. [0012] and FIG. 7.

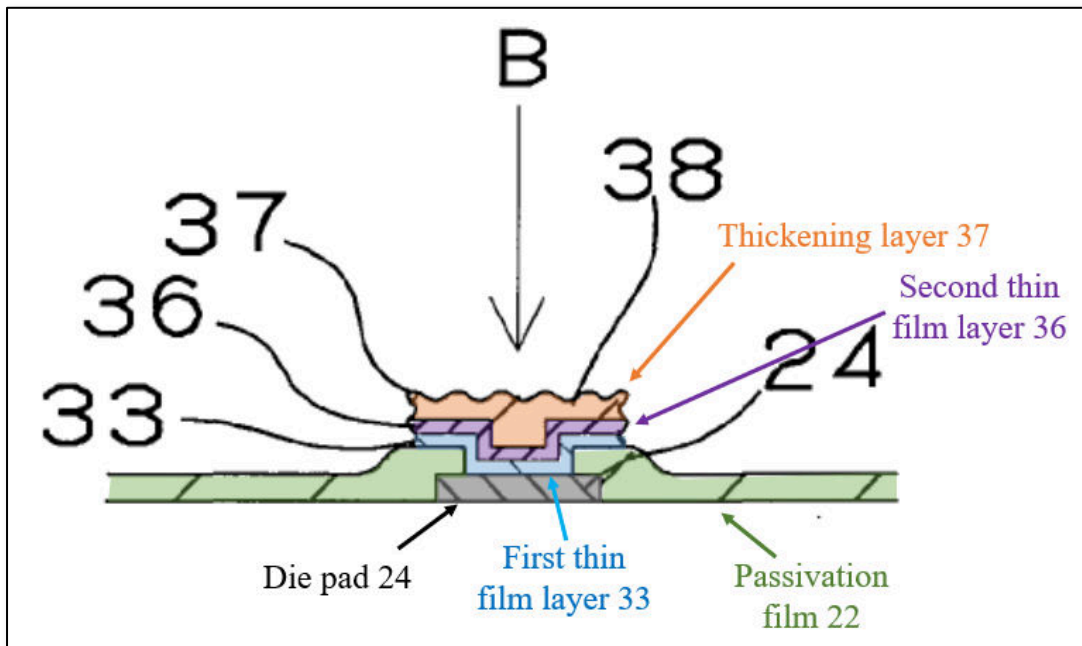
67. An example of the contact structure of Sakamoto is shown in FIGS. 2(C) and 7, reproduced below. A “transition layer 38” on the “die pad 24” of an “IC chip 20” includes “three layers” including a “first thin film layer 33,” a “second thin film layer 36,” and a “thickening film [or layer] 37.” APPLE-1005, [0101]. The first thin film layer 33 “covers the die pad, thereby making it possible to improve the adhesiveness of the transition layer and the IC chip to an interface with the die pad.” *Id.*, [0020]. The “second thin film layer 36” is “employed as a thickening lead.” *Id.*, [0022]. The “thickening layer 37” provides additional thickness and improves connection reliability. *Id.*, [0023]. I discuss the materials and deposition methods associated with these layers below with respect to the

claims of the '324 Patent. However, I will note here that Sakamoto's three layers can be composed of zinc, nickel, and copper, respectively, exactly matching the combination of materials disclosed in the '324 Patent. APPLE-1005, [0109]-[0115]; APPLE-1001, 20:26-45.

68. The transition layer 38 contacts the die pad 24 through an opening in a passivation film 22 (incorrectly given the reference number 24 in the specification). APPLE-1005, [0101], FIG. 2(C). A POSITA would have understood that the die pads and passivation film are distinct components and would not be given the same reference number. Further, the reference number 22 is unused in the specification, element 22 of the drawings has the configuration described for the passivation film, and paragraph [0202], describing another embodiment of Sakamoto, correctly refers to "IC protective film (made of passivation+polyimide) 422 and aluminum die pads 424." Therefore, the interpretation of element 22 as the "passivation film" is clear and unambiguous.



Annotated Sakamoto FIG. 2(C)

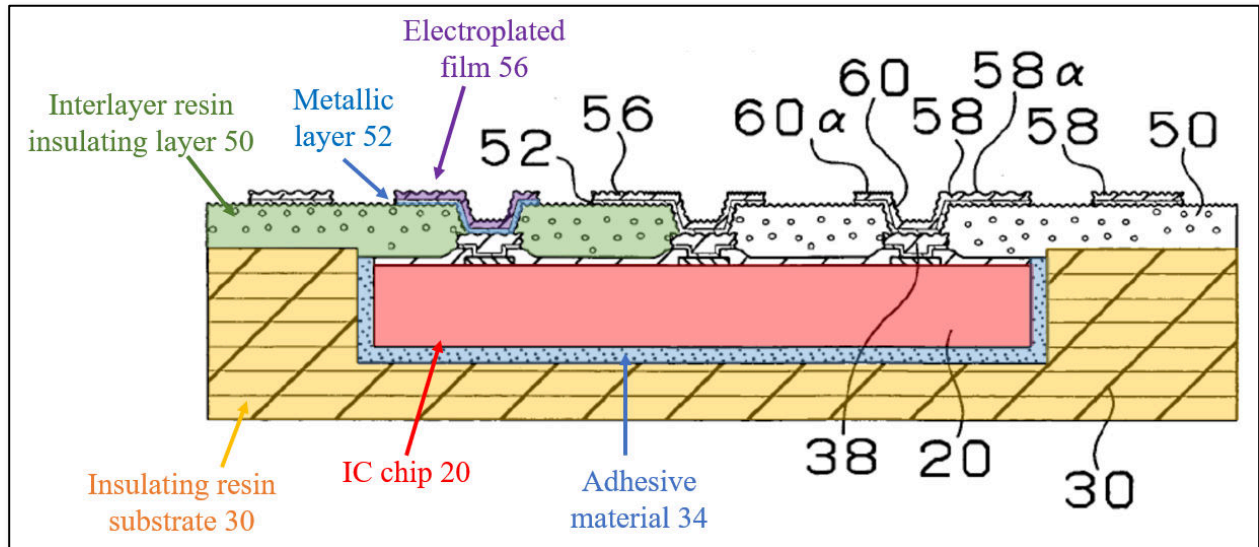


Annotated Sakamoto FIG. 7(A)

69. Sakamoto's structure after further processing is shown in FIG. 4(C), reproduced below. The three-layer structure noted above is retained in this FIG.

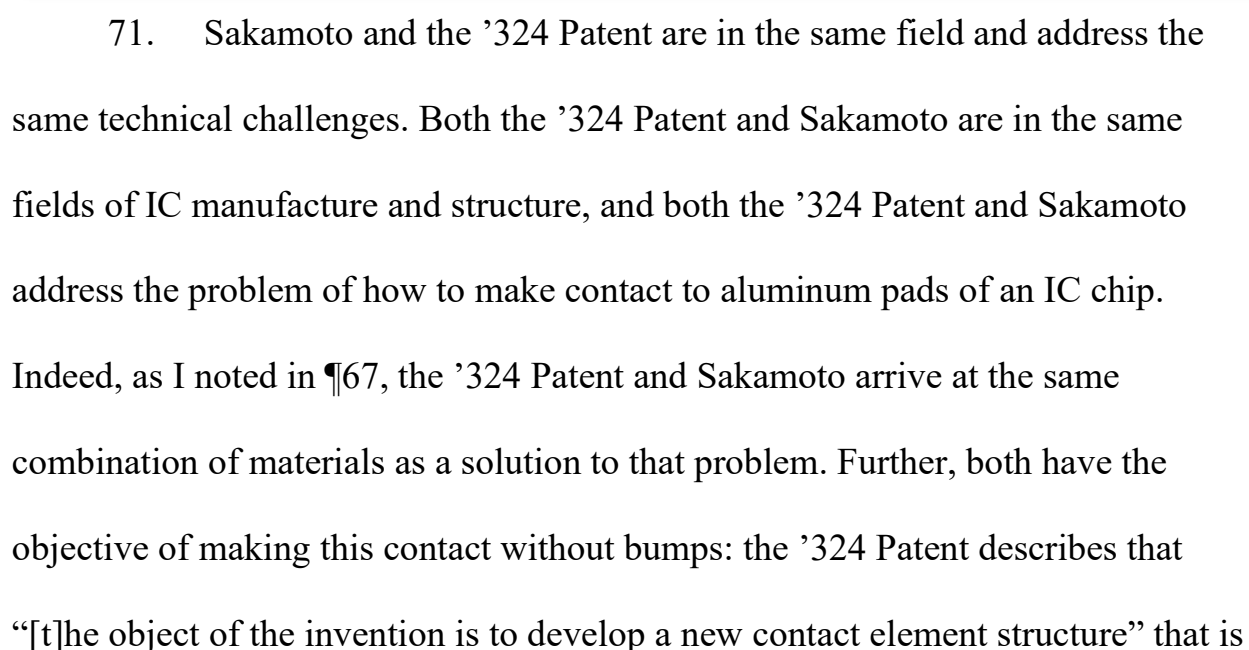
4(C) structure. Further, the IC chip 20 is mounted in an “adhesive material 34” provided in a recess of “an insulating resin substrate (or core substrate) 30.”

APPLE-1005, [0106], [0107], FIG. 1(D). An “interlayer resin insulating layer 50” is on the passivation film 22 and the transition layer 38. APPLE-1005, [0118], FIG. 4(C). “[C]onductor circuits 58 each consisting of [a] metallic layer 52 and [an] electroplated film 56” are on the interlayer resin insulating layer 50 and contact the transition layer 38. APPLE-1005, [0125], FIG. 4(C). Generally, the three-layer transition layer 38 is present to make suitable contact to the die pads 24 (serving a “transition” function), and the conductor circuits 58 are present to then connect the die pads 24 to other electrical components.



Annotated Sakamoto FIG. 4(C)

70. FIG. 6 of Sakamoto illustrates a fully-manufactured “multilayer printed circuit board 10” that includes the structures noted above with respect to FIGS. 2(C), 4(C), and 7. APPLE-1005, [0099], [0105]. Compared to the structure



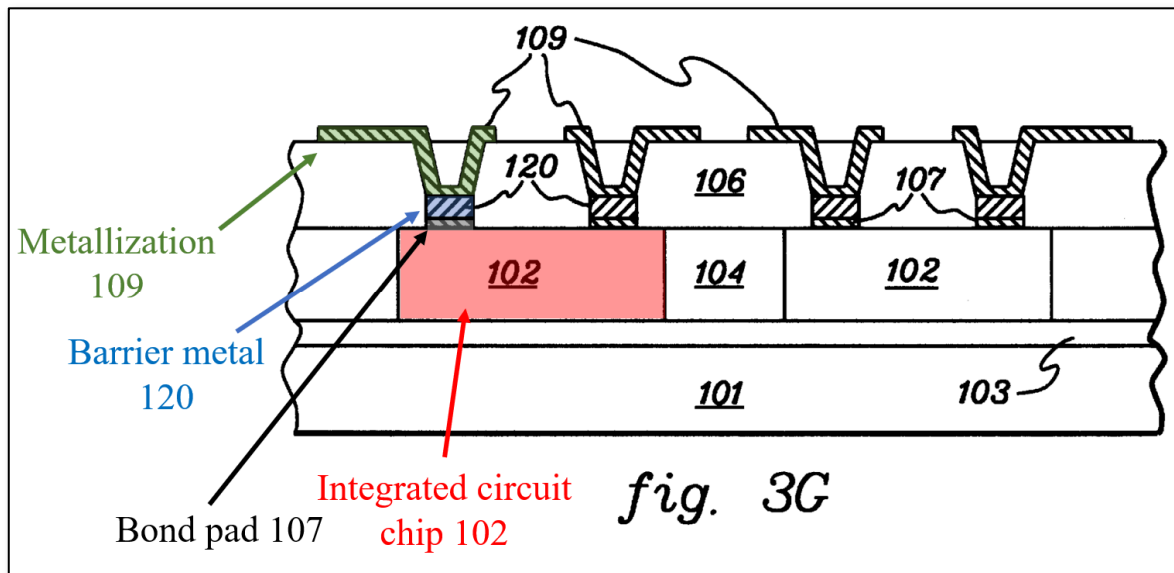
“**bumpless**, i.e. without growing bumps on top of the contact areas of the component.”¹ APPLE-1001, 1:48-51, 3:10-13. Similarly, Sakamoto describes that the use of a “transition layer 38” makes it “possible to electrically connect the IC chip to the multilayer printed circuit board” “**without using** a sealing resin, leads or **bumps**.” APPLE-1005, Abstract, [0050].

B. Overview of Eichelberger

72. Eichelberger (US 6,396,148) is a patent document discussed in the Background of the '324 Patent. APPLE-1001, 2:51-65. Eichelberger describes “first packaging structures and methods of fabrication” that employ “electroless metallizations.” APPLE-1006, Abstract. For example, Eichelberger describes that an “electroless metal coating” (a “barrier”) can be plated on aluminum contact pads to improve connection reliability and protect against “chemical attack” and corrosion. APPLE-1006, 4:44-61. The barrier can be, for example, an electroless nickel layer on which electroless copper is then deposited. APPLE-1006, Abstract, 8:26-36. Eichelberger discusses that “[c]ertain GaAs IC chips have gold pads” and that “the process described herein will also work with these types of bond pads.” APPLE-1006, 9:40-58.

¹ Emphasis is added throughout, except where noted otherwise.

73. Eichelberger's FIG. 3G, reproduced below, shows a similar configuration to that of Sakamoto, including an IC chip 102, a bond pad 107 on the IC chip 102, and multiple metal layers 120, 109 on the bond pad 107. APPLE-1006, 4:9-22, 8:10-13. This structure can include a zincation-deposited zinc layer between the bond pad 107 and the barrier metal 120. APPLE-1006, 5:54-6:16.



Annotated Eichelberger FIG. 3G

74. Eichelberger and the '324 Patent are in the same field and address the same technical challenges. Both address the challenges of contacting aluminum bond pads and disclose zincation, followed by nickel plating, as a key solution. *See* APPLE-1001, 1:64-2:65, 3:47-63; APPLE-1006, 1:22-26, 2:24-29, 5:54-6:16. Indeed, Eichelberger was recognized as relevant in the Background of the '324 Patent. APPLE-1001, 2:51-65.

C. Overview of Chang

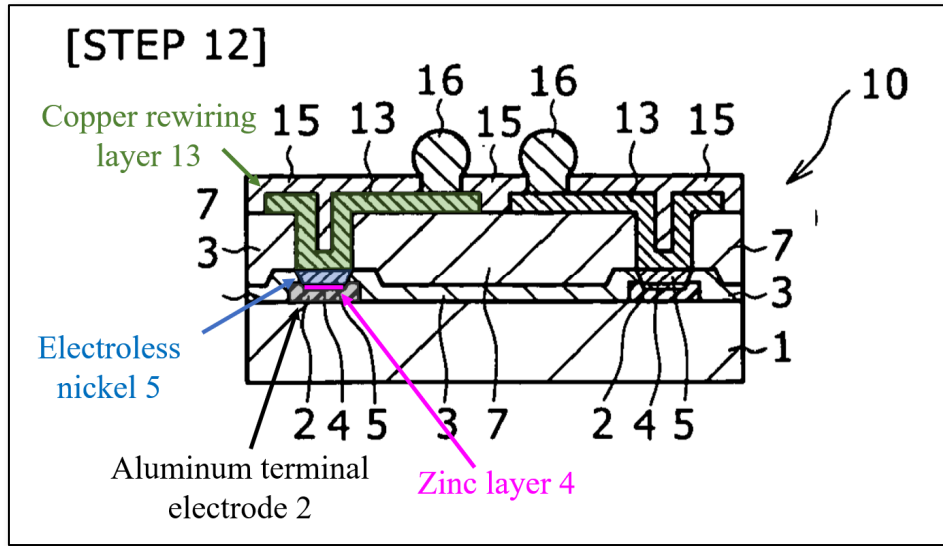
75. Chang is a journal article relating to a “low-temperature integrated electrochemical deposition process for next-generation Cu metallization.” APPLE-1008, 1. Chang describes a process by which “thin, smooth, conformal Cu seed layers” are used as seed layers for “subsequent electroplating [of copper] to accomplish Cu metallization with good quality.” APPLE-1008, 1-2.

76. Portions of Chang relate to surface treatments to facilitate electroless copper deposition, e.g., deposition of Pd catalysts. *See, e.g.*, APPLE-1008, 1 (“Experimental”). For purposes of my discussion here, I draw on Chang for its teachings related to the efficacy of performing electroplating of copper on underlying pure metallic copper seed layers, which are applicable regardless of the deposition method of the copper seed layers. Indeed, Chang notes that sputtered copper seed layers – which would be formable without requiring a catalyst – were known in the art. APPLE-1008, 1 6-7.

77. Chang and the ’324 Patent are in the same field and address the same technical challenges. For example, many embodiments in the ’324 Patent, along with claim 11, relate to forming copper layers by electroless plating, and Chang provides experimental methods for the “electroless plating of thin, smooth, conformal Cu seed layers.” APPLE-1001, 17:40-18:7, 19:41-61; APPLE-1008, 1.

D. Overview of Ito

78. Ito describes the manufacture of a “stacked multilayer” contact in which a “metal layer is self-alignedly formed relative to the terminal electrode. This does not need any patterning step thereby forming the contact portion simply and reliably.” APPLE-1012, [0062]. I discussed above in ¶VI.A that Ito’s process achieved self-alignment based on a combination of zincation on aluminum contacts and subsequent electroless plating of nickel on the zinc. For example, as shown below, FIG. 2L of Ito illustrates a structure including an aluminum terminal electrode 2; a zinc layer 4 formed by zincating on the aluminum terminal electrode 2; an electroless-plated nickel layer 5 on the zinc layer 4; and a copper rewiring layer 13 on the nickel layer 5. APPLE-1012, [0082], [0089], [0091], [0094]-[0096].

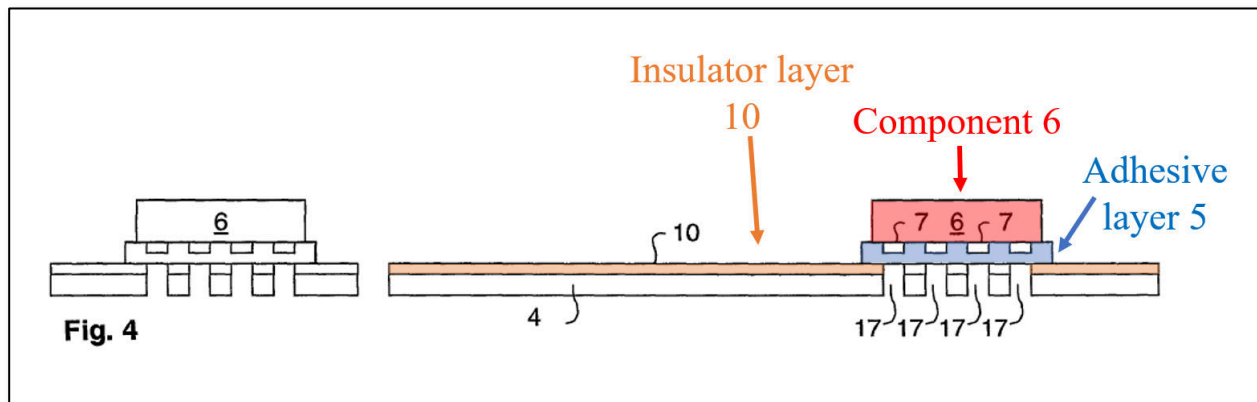


Annotated Ito FIG. 2L

79. Ito and the '324 Patent are in the same field and address the same technical challenges. Both Ito and the '324 Patent are directed to contact structures used in conjunction with copper foil-attached insulating resin sheets, and both disclose that zincation of aluminum contacts, after which electroless nickel is deposited, represents a solution to challenging in contact aluminum. APPLE-1001,3:55-4:5, 5:6-46, 17:40-51; APPLE-1012, [0063], [0065], [0073], [0093].

E. Overview of Tuominen

80. Tuominen, which shares two inventors with the '324 Patent, is directed to “components [] embedded in an installation base and connection to a conductor-pattern structure.” APPLE-1014, 1:5-7. FIG. 4 illustrates a configuration in which “an adhesive layer 5 is spread on the attachment surface of the insulating layer 10” to attach a component 6 to the insulator layer 10. APPLE-1014, 6:20-25.



Annotated Tuominen FIG. 4

81. Tuominen and the '324 Patent are in the same field and address the same technical challenges. These documents share multiple inventors, and, although researchers do sometimes work in disparate fields, these documents relate to very similar devices and technologies. For example, both Tuominen and the '324 Patent relate to similar modules in which a copper foil-based membrane is attached to components that are contacted through contact openings. *See, e.g.*, Tuominen FIG. 7 in comparison to FIG. 20 of the '324 Patent.

F. Overview of Lee

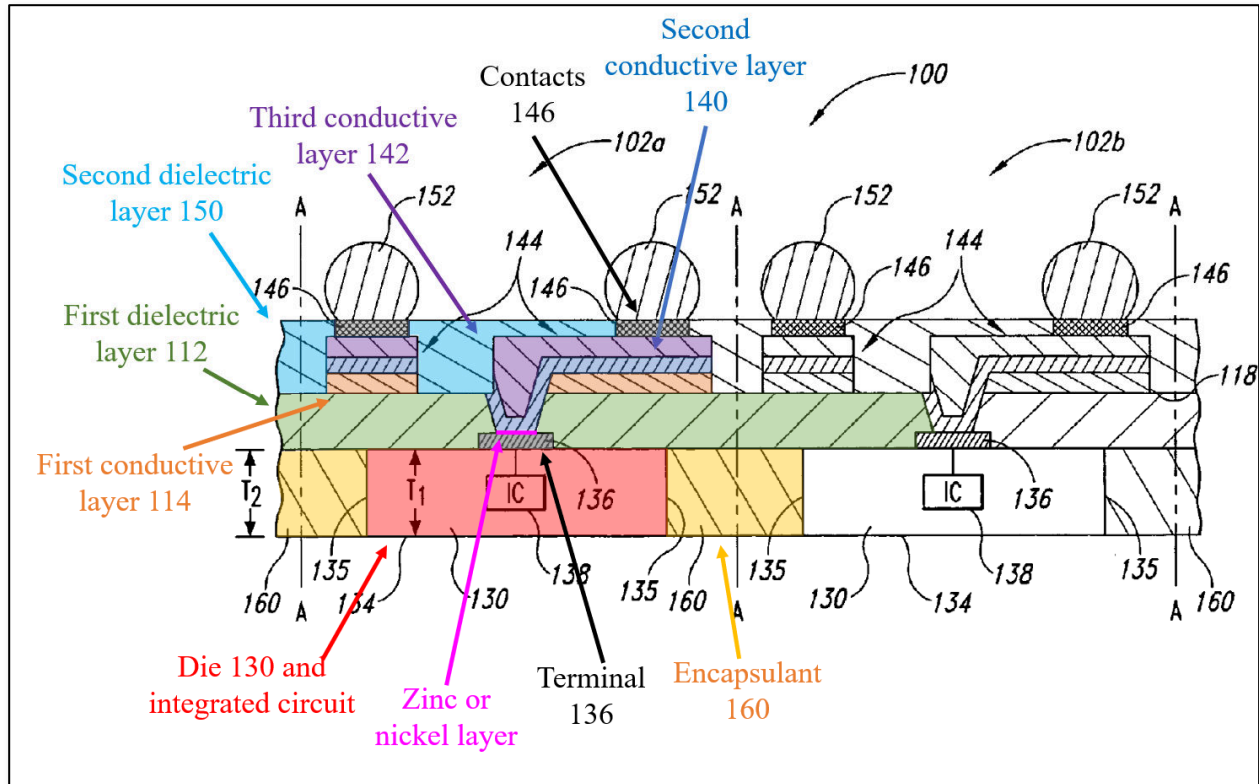
82. Lee is directed to microelectronic devices and manufacturing methods that offer improved yield and throughput. APPLE-1015, [0035]. Like the '324 Patent's, Lee's devices are formed based on a copper foil "first conductive layer 114." APPLE-1015, [0026]. Holes 120 are formed in the first conductive layer 114 and an attached dielectric layer 112, and this structure is attached to dies 130 having terminals 136 ("e.g., bond pads"). APPLE-1015, [0026]-[0029], FIGS. 1A-

1B. A contact structure, including a second conductive layer 140, a third conductive layer 142, and contacts 146, is then fabricated on the terminals 136.

APPLE-1015, [0029]-[0032], FIGS. 1B-1E.

83. In cases in which “the terminals 136 do not have a surface compatible with electroless plating, additional processes such as zincation, sputtering, and/or plating may be necessary to deposit a compatible conductive protective layer (e.g., a nickel layer) on the terminals 136 before depositing the second conductive layer 140.” APPLE-1015, [0030]. As a result, a zinc layer (“zincation”) or a “nickel layer” can be provided between the terminals 136 and the second conductive layer 140. That is, Lee agrees with both the ’324 Patent and several of the other documents cited here in teaching the efficacy of a multilayer structure for making contact to aluminum terminals. Portions of my discussion below are based on the presence of this zinc or nickel layer on the terminals 136, as shown in the annotated FIG. 1E below.

84. The resulting structure, with dies 130 encased in an encapsulant 160 and a second dielectric layer 150 provided on the first dielectric layer 112, is annotated below. APPLE-1015, [0033], FIG. 1E.



Annotated Lee FIG. 1E

85. Lee and the '324 Patent are in the same field and address the same technical challenges Both the '324 Patent and Lee are in the same field of endeavor of IC manufacture and structure, and both the '324 Patent and Lee address the problem of how to contact an IC chip attached to a copper foil by an insulating layer. APPLE-1001, 3:42-4:41; APPLE-1015, [0002]-[0006], [0026]. Lee and the '324 Patent arrive at the same solution of forming contact holes prior to attaching the IC chip: for example, the '324 Patent describes that "contact openings are made in the conductor foil of the conductor-pattern prior to attaching the component," in agreement with Lee's process as shown in FIGS. 1A-1B and reflected in claim 18. APPLE-1001, 4:13-25; APPLE-1015, [0026]-[0030]. Further, both the '324 Patent

and Lee address how contact holes can be dimensioned to improve alignment between contact pads and subsequent layers, arriving at the same solution of making the contact area less than the total pad area. APPLE-1001, 16:6-55, claim 1; APPLE-1015, [0029], FIG. 1B.

IX. GROUNDS 1A-102 and 1A-103: Claims 1-2, 4-11, 13-15, 17, and 19 are anticipated by or obvious over Sakamoto

86. Based on my analysis, Sakamoto anticipates and renders obvious claims 1-2, 4-11, 13-15, 17, and 19

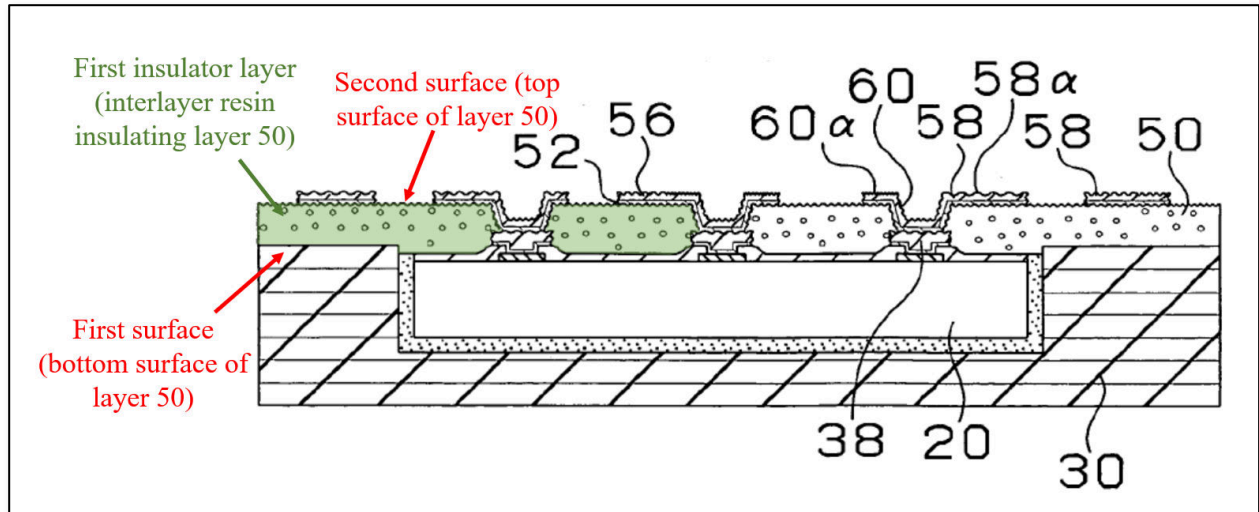
A. Analysis of Claims

[1pre]: Circuit module, comprising

87. Sakamoto's "multilayer printed circuit board 10" is a "circuit module." APPLE-1005, [0099]. Like the "finished simple circuit module" of FIG. 8 of the '324 Patent, Sakamoto's multilayer printed circuit board 10 includes an IC chip (20) embedded in an insulating material (30) and connected to a series of conducting layers (e.g., 38, 58, 158) that connect the IC chip to contact balls (76). APPLE-1001, 10:56, FIG. 8; APPLE-1005, FIG. 6.

[1a]: a first insulator layer having a first surface and a second surface;

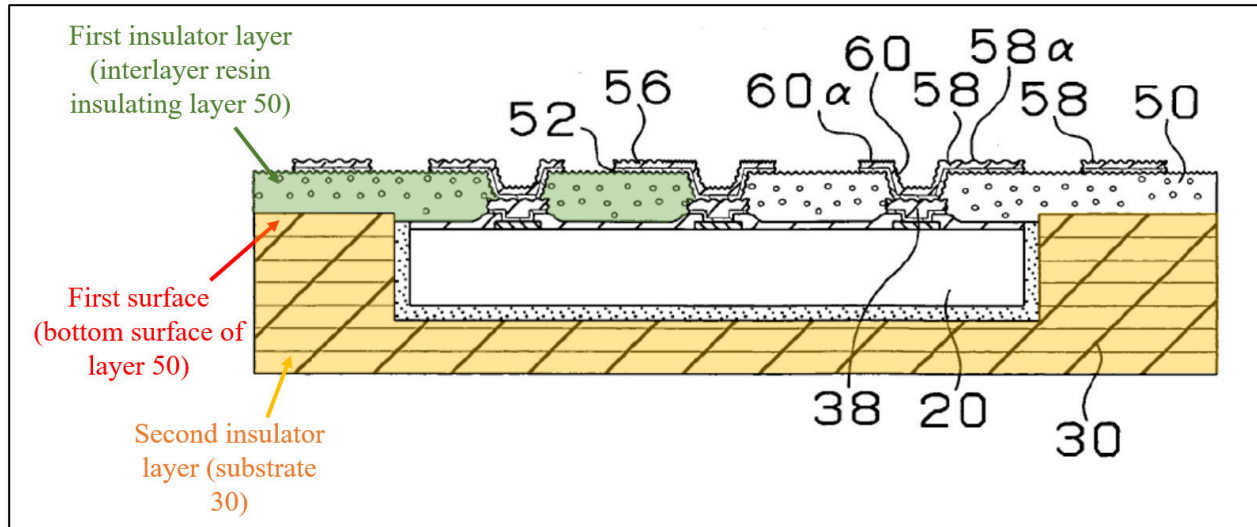
88. Sakamoto's "interlayer resin insulating layer 50" is a first insulator layer having a "*first surface*" (its bottom surface) and a "*second surface*" (its top surface). APPLE-1005, [0118], FIG. 4(C), FIG. 6.



Annotated Sakamoto FIG. 4(C)

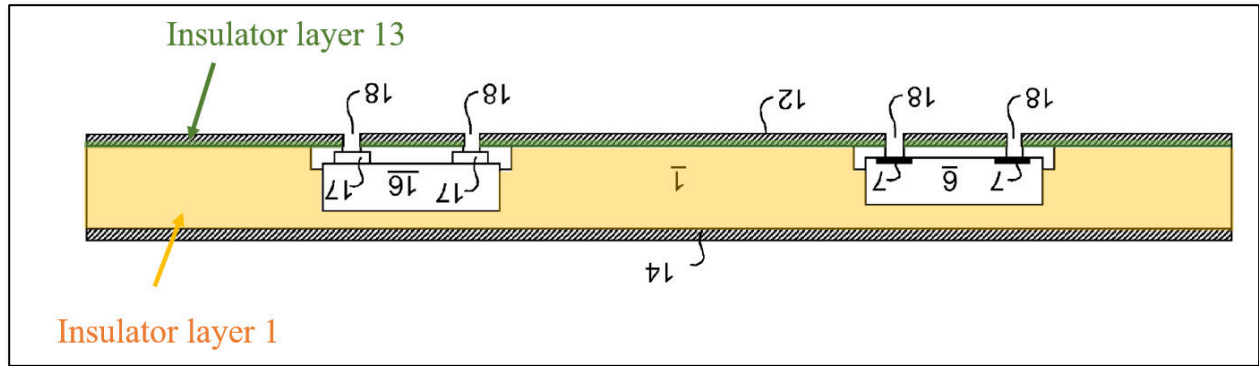
[1b]: at least one second insulator layer on the first surface;

89. Sakamoto's "insulating resin substrate (or core substrate) 30" is a "second insulator layer" on the "first surface" (the bottom surface of the interlayer resin insulating layer 50). APPLE-1005, [0106], FIG. 4(C), FIG 6.



Annotated Sakamoto FIG. 4(C)

90. The substrate 30 is an “insulator layer on the first surface” within the meaning of claim 1. For example, ’324 Patent FIGS. 1 and 4 illustrate “insulator layer 1” as an example of the “second insulator layer.” The insulator layer 1 is a “prepreg” layer or “an FR4 or FR5-type sheet,” which are common printed circuit board (PCB) substrate materials. APPLE-1001, 24:23-36; APPLE-1020, Chapter 6. Similarly, Sakamoto describes that the substrate 30 is part of a “multilayer printed circuit board 10” and can include multiple prepreg layers and/or multiple substrate layers. APPLE-1005, [0100], [0106]. Further, the relative arrangement of Sakamoto’s substrate 30 and insulating layer 50 (mapped above to the “first insulator layer”) matches the relative arrangement of the ’324 Patent’s insulator layer 1 and insulator layer 13 (the “first insulator layer” and “second insulator layer,” respectively), as shown below.

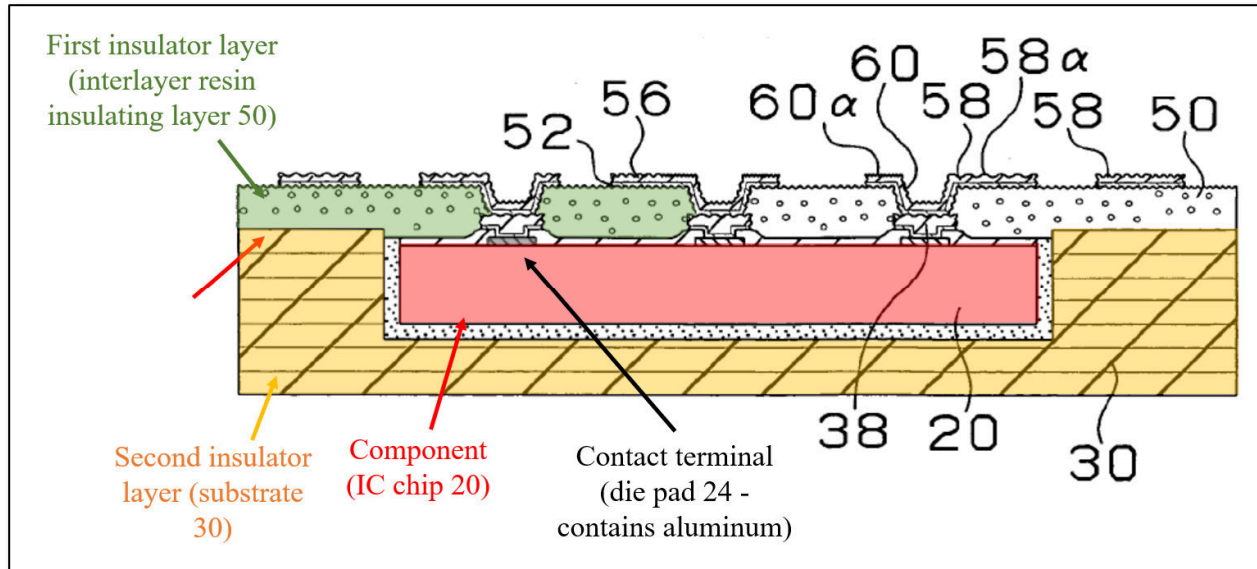


Annotated '324 Patent FIG. 4

[1c]: at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing a first metal,

91. Sakamoto's "IC [integrated circuit] chip 20" is a "*component*" that is inside the "*second insulator layer*" (the insulating resin substrate 30). APPLE-1005, [0108], FIG. 6. This description in Sakamoto is similar to that of the '324 Patent that "[t]he component [] can be, for example, an integrated circuit." APPLE-1001, 24:14-15.

92. Further, the *at least one component* (the IC chip 20) comprises "die pads 24," "each constituting an input/output terminal," which are "*contact terminals*." APPLE-1005, [0101], FIG. 6. For example, a POSITA would have understood that "contact" is made to the IC chip 20 using these die pads 24 ("terminals"). The die pads 24 are "made of **aluminum**," an example of a "*first metal*." APPLE-1005, [0101]; *see also id.*, [0051] ("the pad of the IC chip is normally formed out of aluminum or the like.").



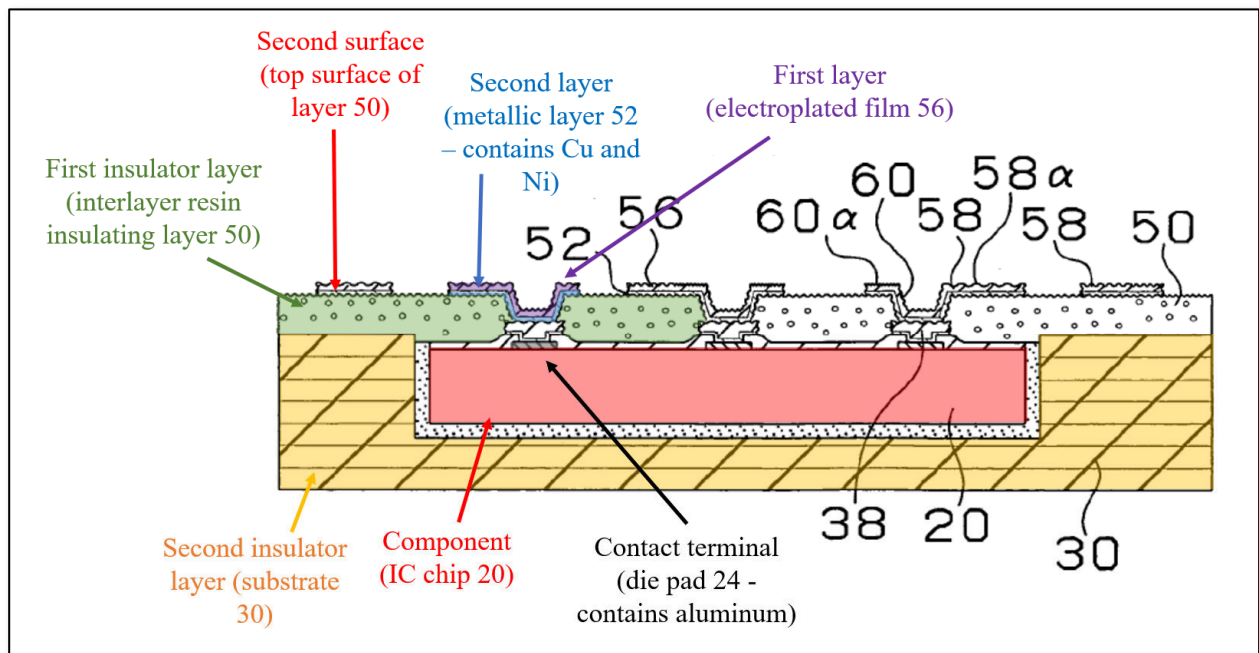
Annotated Sakamoto FIG. 4(C)

[1d]: conductors on the second surface of the first insulator layer, the conductors comprising at least a first layer and a second layer, in such a way that at least the second layer contains a second metal, and

93. Sakamoto's "conductor circuits 58 are *conductors*." APPLE-1005, [0125]. Besides Sakamoto's description of these circuits 58 as "**conductor** circuits," a POSITA would have recognized that the materials disclosed for the conductor circuits 58 (e.g., nickel/copper and copper) are metallic conductors.

94. The conductor circuits 58 are on the "*second surface*" (top surface) of the "*first insulator layer*" (interlayer resin insulating layer 50). APPLE-1005, [0011], [0125], FIG. 6. For example, their arrangement is similar to that of the '324 Patent's conductor foil 12 ("*conductors*") and polymer layer 25/insulator layer 13 ("*first insulator layer*"). APPLE-1001, 22:3-26, FIG. 29.

95. The conductor circuits 58 include a “*first layer*” (electroplated film 56) and a “*second layer*” (metallic layer 52). APPLE-1005, [0125], FIG. 4(C), FIG. 6. At least the metallic layer 52 (an example of the *second layer*) includes a “*second metal*.” For example, Sakamoto describes that the metallic layer 52 is an “Ni/Cu” layer. APPLE-1005, [0123]. Both nickel and copper are metals. Thus, the metallic layer 52 contains, as the “*second metal*,” **copper or nickel**.



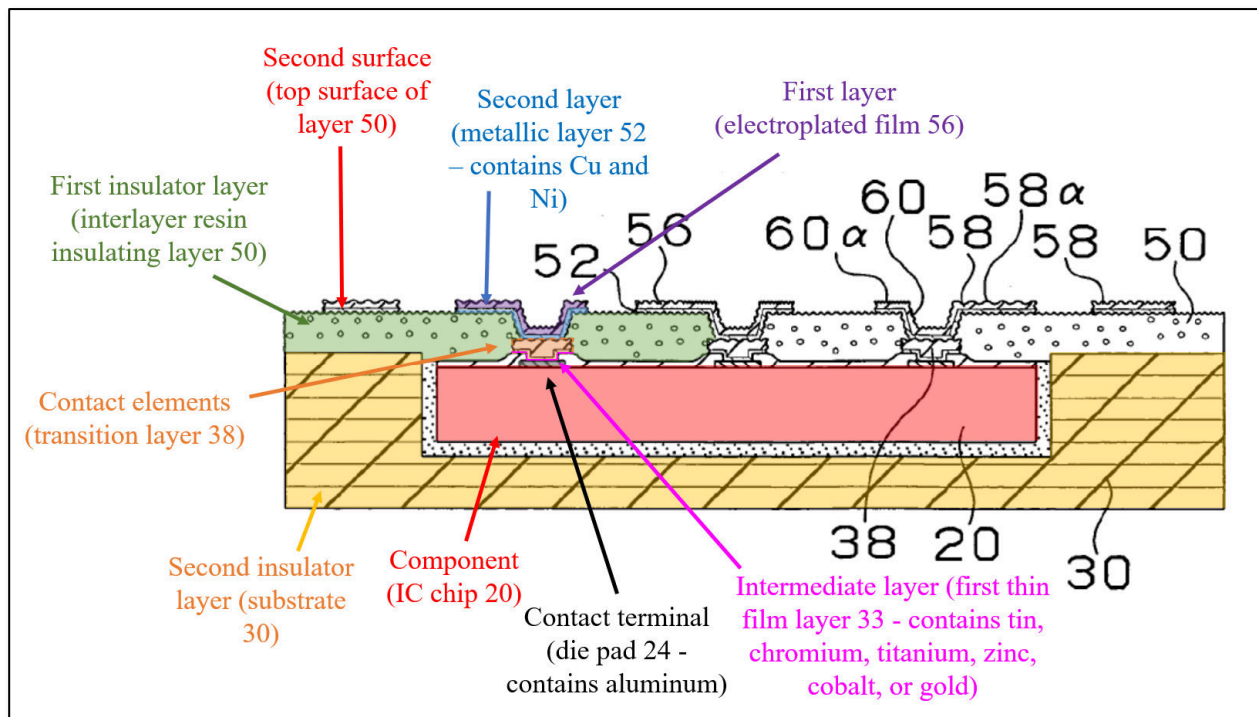
Annotated Sakamoto FIG. 4(C)

[1e]: contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal,

96. Sakamoto's "transition layer 38" comprises "*contact elements*" between the "*contact terminals*" (die pads 24) and the "*conductors*" (conductor circuits 58 including metallic layer 52 and electroplated film 56). APPLE-1005, [0101], FIG. 4(C) and 6. The transition layer 38 is "*for forming electrical contacts*" and would therefore be understood as a "*contact element*." Further, Sakamoto describes that die pads 24 of separate IC chips 20, 120 "are mutually connected through transition layers 38." APPLE-1005, [0164]. This is also evidenced by Sakamoto's description that "[t]he transition layer means a mediate layer provided on an intermediate portion so as to directly connect the IC chip, which is a semiconductor element, to the printed circuit board without using a conventional IC chip mounting technique." APPLE-1005, [0016]. Therefore, a POSITA would have understood the transition layer 38 as an element providing a contact function.

97. The transition layer 38 ("*contact elements*") comprises first thin film layer 33, an "*intermediate layer*," intermediate between the die pad 24 and the second thin film layer 36. APPLE-1005, [0020], [0109], FIG. 7(A). The first thin film layer 33 is "*on the surface of the contact terminal*" (die pad 24), as explained by Sakamoto's description that "[t]he first thin film layer covers the die pad, thereby making it possible to improve the adhesiveness of the transition layer and the IC chip to an interface with the die pad," and as shown in FIGS. 4(C), 6 and 7(A). APPLE-1005, [0020], FIGS. 6, 7(A).

98. The first thin film layer 33 (“*intermediate layer*”) contains a *third metal*, for example, “**tin, chromium, titanium, [] zinc, cobalt, [or] gold.**” APPLE-1005, [0109]. Each of the foregoing materials is a metal.



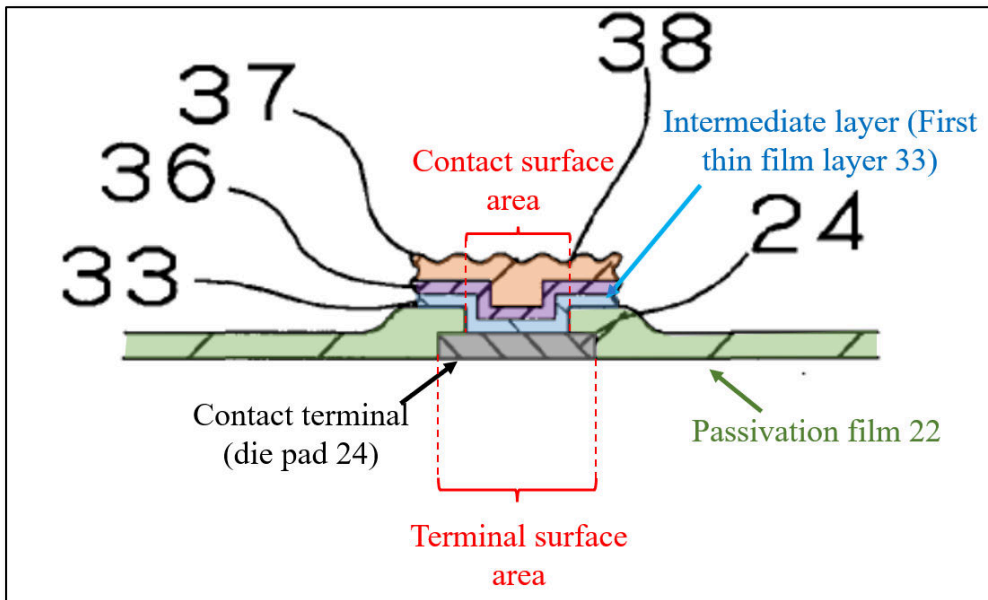
Annotated Sakamoto FIG. 4(C)

99. In summary, the applied mapping of Sakamoto’s elements to those of claim 1 are shown in the table below:

First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	• Metallic layer 52 (<i>second layer</i>), and • Electroplated film 56 (<i>first layer</i>)	Cu or Ni	• First thin film layer 33 (<i>intermediate layer</i>), • Second thin film layer 36, and • Thickening layer 37	Sn, Ti, Zn, Co, or Au

[1f]: a contact surface area (A_{CONT1}) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal.

100. According to the mappings discussed for [1c] and [1e], this claim element corresponds to a contact surface area between the first thin film layer 33 (“*intermediate layer*”) and the die pad 24 (“*contact terminals*”) being less than a surface area of the die pad 24. This configuration is disclosed, for example, by Sakamoto’s FIG. 7(A), which illustrates that “die pads 24 [] are provided in the openings of the passivation film [22]” and which clearly shows the contact surface area being less than the surface area of the die pad 24. APPLE-1005, [0101].



Annotated Sakamoto FIG. 7(A)

101. FIGS. 1(D), 2(C), 4(C), 6, and 7(A) show that the passivation layer 22 covers outer portions of the die pad 24, with only a central portion of the die pad 24 exposed. The first thin film layer 33 deposited on the exposed portion of the die pad 24 forms a contact surface area that is less than a surface area of the die pad 24, because the exposed portion – the only portion in contact with the first thin film layer 33 – is smaller than the full surface area of the die pad 24. A difference between the terminal width and the contact width are shown in annotated FIG. 7(A) above.

102. Although this difference is illustrated as a difference between widths or diameters, the illustrated relationship would correspondingly apply for areas as well. For example, Sakamoto discloses that the die pads 24 have a “diameter,” suggesting that the die pads 24 can be circular. APPLE-1005, [0104]. This would

be a natural choice of shape to match the circular shape of the transition layer 38, as shown in FIG. 7(B). Additionally, since only a singular diameter is called out, a POSITA would understand this to indicate that the dimensions are symmetric across the axes. I note further than the use of such cross-sectional diagrams are common in the art, and a POSITA would recognize that the cross-section is a clear indication of a smaller area of contact. The via holes in interlayer resin insulating layer 50, too, are described as having a “diameter,” from which it follows that it would have been obvious to make the holes in passivation film 22 (which define the contact area between the first thin film layer 33 and the die pad 24) circular, as a matter of applying the same teaching to a similar configuration and as a matter of simple design choice. Therefore, given die pads 24 with diameter r_1 and holes in passivation film 22 with diameter $r_2 < r_1$, the corresponding areas would satisfy $A_{CONT1} = \pi r_2^2 < A_{PAD} = \pi r_1^2$. Similar reasoning would apply to other shapes of the die pads and/or holes in passivation film 22.

103. Sakamoto’s drawings clearly and unambiguously show the presence of substantial overlap between the passivation layer 22 and the die pads 24. APPLE-1005, FIGS. 1(D), 2(C), 4(C), 6, and 7(A). For example, the passivation layer 22 is illustrated with clear bumps or steps due to its overlap with the die pads 24, and the deposited layers 33, 36, 37 are illustrated as protruding into a recess formed by the bumps/steps. APPLE-1005, FIGS. 1(D), 2(C), 4(C), 6, and 7(A).

The downward protrusion of the first thin film layer 33 contacts less than an entirety of the surface area of the die pad 24, such that the “contact surface area” element of claim 1 is satisfied.

104. Indeed, the recited idea – that a contact surface area is less than a total surface area of the bottom pad – has been standard in circuit manufacturing for decades, well predating the priority date of the ’324 Patent. This arrangement reduces the negative impact of any misalignments in forming the contact hole (for Sakamoto, holes in the passivation layer 22). For example, when the contact hole is smaller than the pad, the contact hole can deviate somewhat from its target position while still remaining entirely on the pad, and an etch that forms the contact hole will terminate at the pad without removing material adjacent to the pad.

105. As examples, FIGS. 4.14, 5.25, and 7.14 of APPLE-1021, a classic undergraduate textbook on very large scale integration (VLSI) design from the 1980s, each show the recited contact area relationship. APPLE-1021, 81, 106 165.

106. Apart from Sakamoto’s express disclosure of this claim limitation, it also would have been obvious to form the contact surface area between the first thin film layer 33 and the die pad 24 to be less than a surface area of the die pad 24, based on Sakamoto’s disclosed manufacturing process and based on Sakamoto’s teachings with respect to hole formation. In Sakamoto’s fabrication method, “openings” are present in the passivation film 22, and the first thin film

layer 33 is formed by “deposition or sputtering” over “the entire surface of the core substrate 30 which contains the IC chip 20,” including in the openings in the passivation film 22. APPLE-1005, [0101], [0109].

107. Sakamoto does not disclose how the openings in the passivation layer 22 are formed. However, Sakamoto discusses detailed considerations for forming “via holes” in interlayer insulating layers such as the interlayer resin insulating layer 50. APPLE-1005, [0011]-[0013]. Sakamoto describes that “if laser is applied and the via diameter is larger than the diameter of the die pad, a polyimide layer (or protective layer of the IC) is damaged by the laser. Moreover, if the die pad of the IC chip is very small and the diameter of the via is larger than the size of the die pad, then positioning becomes quite difficult even by photo-etching or laser and connection errors occur between the die pad and the via hole.” APPLE-1005, [0012]. This means that the hole formed in the insulating layer by the laser should be smaller than the die pad, so that the laser does not impinge outside the die pad. Further, large holes relative to the die pad can make alignment more difficult, another reason for which the hole should be smaller than the die pad.

108. A POSITA would have understood that these same considerations would apply to forming the openings in the passivation layer 22, for example, so that the openings could be formed by the same laser technology used to form holes in layer 50, and, therefore, would have been motivated to make the openings

smaller than the die pads 24, matching the illustrations in Sakamoto's figures.

Based on this configuration, the laser could be used without damaging portions of the IC chip 20 underlying the passivation layer 22 and outside the die pads 24.

With this obvious configuration, which would protect the IC chip 20 from damage and make alignment more reliable, the contact surface area between the first thin film layer 33 and the die pad 24 would be less than the surface area of the die pad 24.

[2]: The circuit module of claim 1, wherein the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.

109. In the mappings applied for claim 1, the die pads 24 are “made of **aluminum**” (the *first metal*), the metallic layer 52 corresponding to the “*second layer*” of the “*conductors*” includes “**Cu**” (the *second metal*), and the first thin film layer 33 corresponding to the “*intermediate layer*” can be any of several metals, including “**zinc**” (the *third metal*). APPLE-1005, [0051], [0101], [0109], [0123].

[4]: The circuit module of claim 1, wherein the intermediate layer comprises a layer containing zinc.

110. Sakamoto describes that the “metal used” for the first thin film layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be

tin, chromium, titanium, nickel, **zinc**, cobalt, gold, or copper.” APPLE-1005, [0109]. See discussion at [1e].

[5]: The circuit module of claim 1, wherein the intermediate layer comprises a layer containing copper.

111. Sakamoto describes that the “metal used” for the first thin film layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be tin, chromium, titanium, nickel, zinc, cobalt, gold, or **copper**.” APPLE-1005, [0109]. See discussion at [1e]. As such, the “*third metal*” recited in claim 1 can be copper. APPLE-1005, [0109].

112. As explained above, the metallic layer 52 (corresponding to the “*second layer*” of the “*conductors*,” which contains a “*second metal*”) is “**Ni**/Cu”, such that the “*second metal*” can be nickel.

113. As discussed for claim 1, the “*first metal*” is the “**aluminum**” of the die pads 24. APPLE-1005, [0051]

[6]: The circuit module of claim 1, wherein the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium.

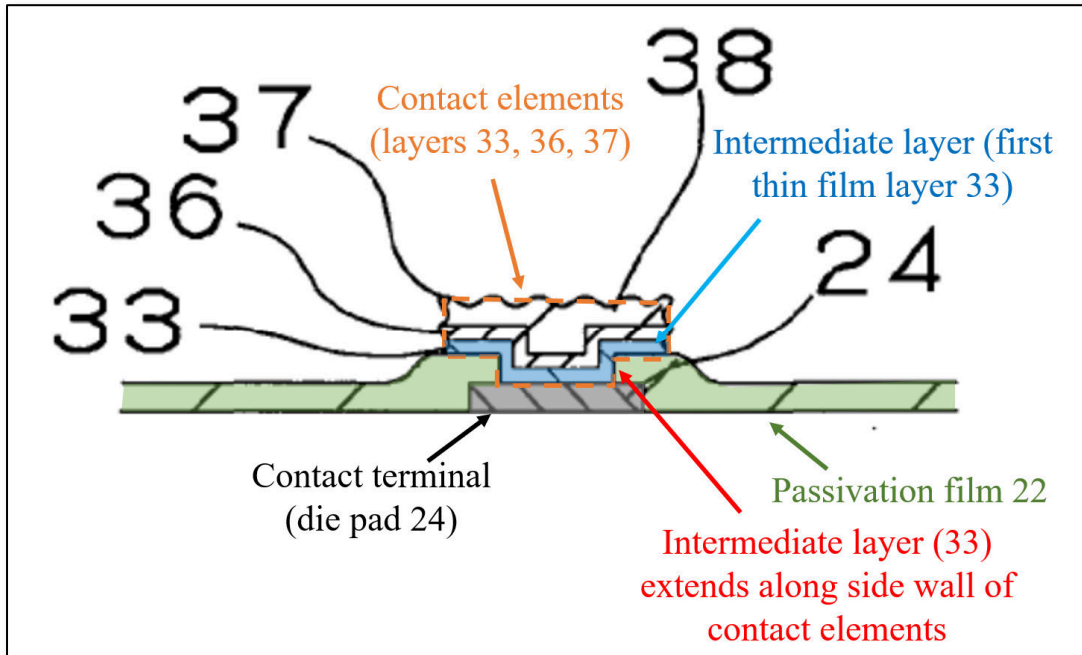
114. Sakamoto describes that the “metal used” for the first thin film layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be tin, chromium, titanium, **nickel**, zinc, cobalt, gold, or copper.” APPLE-1005, [0109].

115. The metallic layer 52 (corresponding to the “*second layer*” of the “*conductors*,” which contains a “*second metal*”) is “Ni/Cu”, such that the “*second metal*” can be copper.

116. As discussed for claim 1, the “*first metal*” is the “**aluminum**” of the die pads 24. APPLE-1005, [0051]

[7]: *The circuit module of claim 1, wherein the intermediate layer extends along the side walls of the contact elements between the contact terminals and the conductors.*

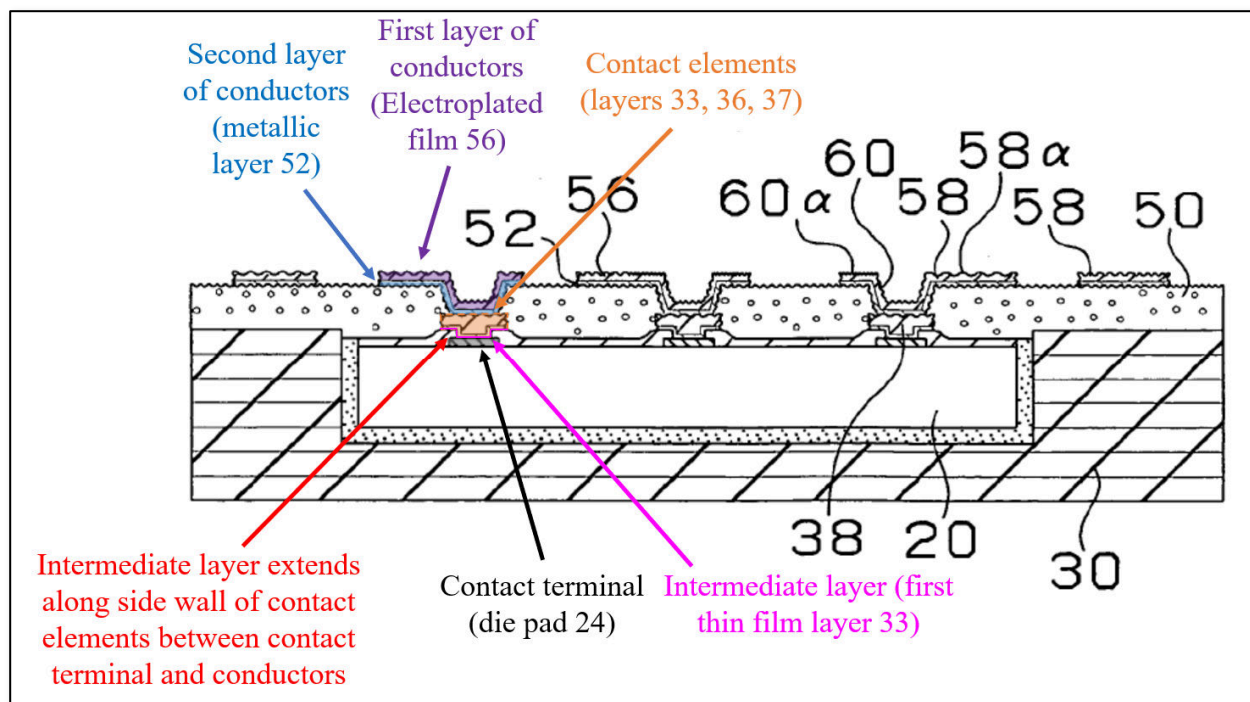
117. As discussed at [1e], Sakamoto’s transition layer 38, which includes layers 33, 36, and 37, is applied as the “*contact elements*,” and the first thin film layer 33 is applied as the “*intermediate layer*.” APPLE-1005, [0101], [0109]. As shown in the annotated FIG. 7(A) below, the first thin film layer 33 extends along side walls of the transition layer 38. APPLE-1005, FIG. 7(A). This arrangement of the first thin film layer 33 follows from the “deposition or sputtering” of the first thin film layer 33 “on the entire surface.” APPLE-1005, [0109]. Sputtering, for example, is known for providing a generally conformal coating profile that can deposit layers such as the first thin film layer 33 on vertical surfaces such as side walls. APPLE-1026, Abstract.



Annotated Sakamoto FIG. 7(A)

118. Further, as shown below, the extension of the first thin film layer 33 along the side walls of the transition layer 38 is between the die pad 24 (“*contact terminals*”) and the metallic layer 52/electroplated film 56 (“*conductors*”).

APPLE-1005, FIG. 6. As such, claim 7 is satisfied.



Annotated Sakamoto FIG. 4(C)

[8]: The circuit module of claim 1, wherein each contact element comprises a copper core, which connects continuously to the material of the second layer of the conductors.

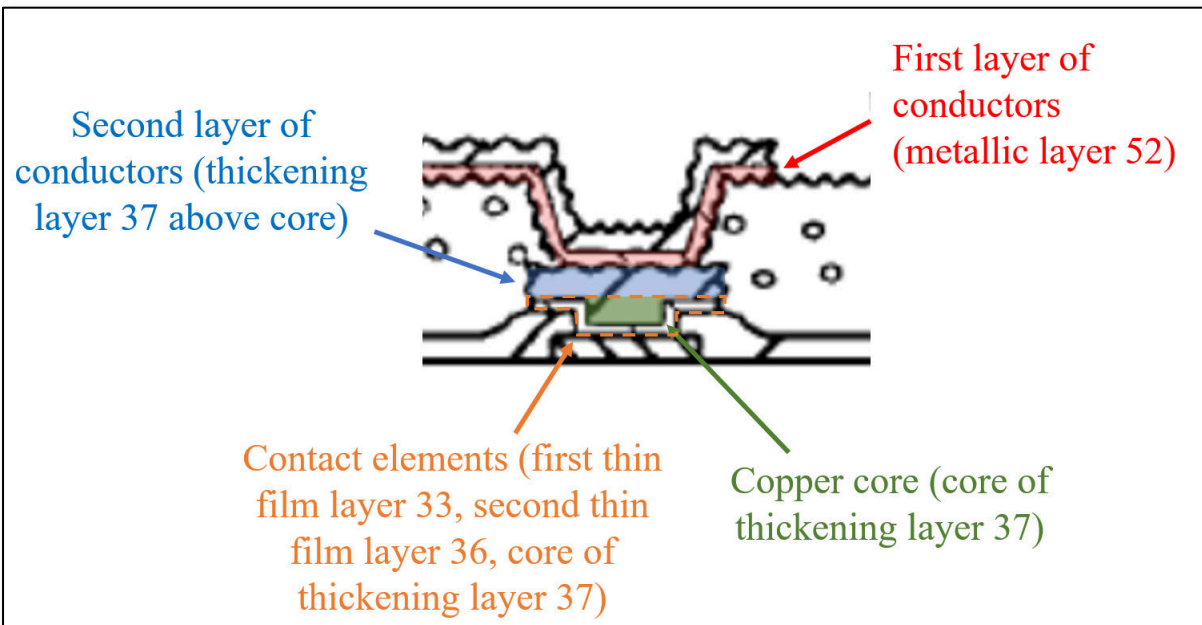
119. Sakamoto's thickening layer 37 includes a "*copper core*" that "*connects continuously to the material of the second layer of the conductors.*" For claim 1, the first thin film layer 33, the second thin film layer 36, and the entirety of the thickening layer 37 were together applied as the "*contact elements.*" However, it is equally valid to apply the first thin film layer 33, the second thin film layer 36, and the core of the thickening layer 37 as the "*contact elements.*" This mapping is in close agreement with the '324 Patent's treatment of similar

elements, e.g., the description that “electrochemically grown copper also forms the conductor core 29 of the contact element.” APPLE-1001, 19:54-55.

120. Further, for claim 1, the metallic layer 52 and the electroplated film 56 were together applied as the “*conductors*.” However, it is equally valid to apply each of the metallic layer 52, the electroplated film 56, **and** the thickening layer 37 above the core as the “*conductors*,” of which the metallic layer 52 is applied as the “*first layer*” and the thickening layer 37 above the core is applied as the “*second layer*.” Sakamoto discloses that the thickening layer 37 is an electroplated **copper** layer, such that this mapping corresponds to the “*second metal*” (of the “*conductors*”) being **copper**. APPLE-1005, [0025], [0111], [0114]. This mapping, too, is in close agreement with the ’324 Patent’s description of similar elements, e.g., the description that “conductor 22” includes “layer 32,” which is “manufactured in the same process” as the “copper core 29.” APPLE-1001, 23:30-39.

121. These alternative mappings are shown in the table and the annotated, enlarged portion of FIG. 4(C) below.

First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	• Metallic layer 52 (<i>first layer</i>), • Electroplated film 56, and • Thickening layer 37 above core (<i>second layer</i>)	Cu	• First thin film layer 33 (<i>intermediate layer</i>), • Second thin film layer 36, and • Core of thickening layer 37 (<i>copper core</i>)	Sn, Ti, Ni, Zn, Co, or Au

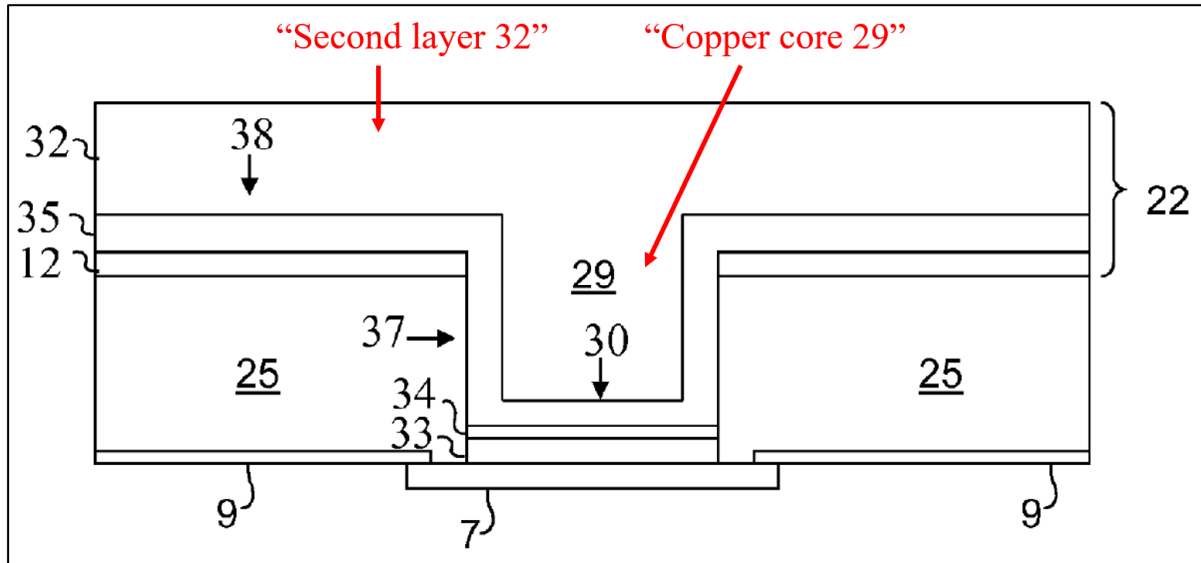


Annotated portion of Sakamoto FIG. 4(C)

122. The core of the thickening layer 37 is a “*copper core*” that “*connects continuously*” to the material of the thickening layer 37 above the core (“*second layer of the conductors*”), because these elements are formed in a common, continuous electroplating process. APPLE-1005, [0114]. That is, the thickening layer 37 is formed in a continuous electroplating process, and this process would

not involve any discontinuity in deposited material between copper of the core and copper above the core. APPLE-1005, [0114].

123. The foregoing mapping, in which a portion of a single material, grown in a single process, is applied as both the “*copper core*” and the “*second layer*” of the conductors, is consistent with the ’324 Patent’s description of those same elements. For example, the ’324 Patent describes that “[a] layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element” and that “the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is manufactured in the same process, so that [] there is no interface between them.” APPLE-1001, 20:42-45, 23:35-39. The copper core 29 and the second layer 32 are described as “connect[ing] continuously, i.e., without an interface.” APPLE-1001, 30-35. And FIG. 29 of the ’324 Patent, reproduced below, similarly illustrates a continuous connection between the copper core 29 and the second layer 32. This configuration exactly matches the configuration of Sakamoto’s layer 37, such that layer 37 has the recited characteristic.



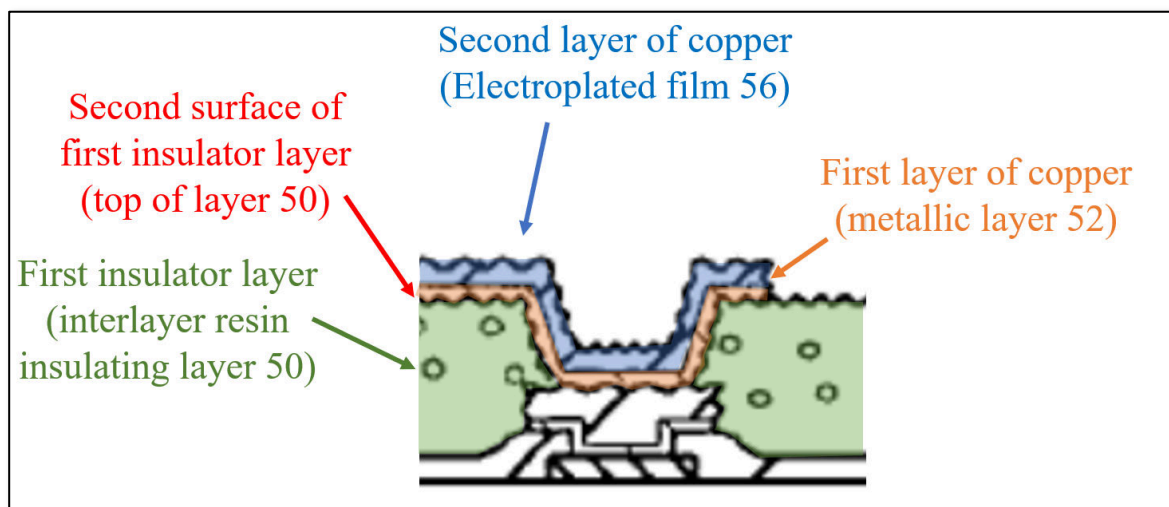
Annotated '324 Patent FIG. 29

[9]: The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, and a second layer of copper on the surface of the first copper layer.

124. As discussed for [1d], Sakamoto's "metallic layer 52," which is "*on the second surface of the first insulator layer*" (interlayer resin insulating layer 50), along with the "electroplated film 56," are applied as teaching the *conductors*. APPLE-1005, [0121]-[0124]. The electroplated film 56 is on the surface of the metallic layer 52. APPLE-1005, FIG. 6.

125. The electroplated film 56 is an electroplated **copper** layer, or “*second layer of copper*”. APPLE-1005, [0123]. The metallic layer 52 is described as a nickel-**copper** layer that can be deposited by electroless plating, sputtering, or another method. APPLE-1005, [0121]-[0122]. Therefore, to the extent “*layer of*

copper” is interpreted as “layer containing copper,” the metallic layer 52 is a “*first layer of copper*.”



Annotated portion of Sakamoto FIG. 4(C)

126. To the extent “*layer of copper*” is interpreted as referring to pure metallic copper, it would have been obvious to form the metallic layer 52 out of copper instead of nickel-copper. A POSITA would have recognized the function of the metallic layer 52 as a “seed layer,” a thin (“0.2 μm ”) layer that is deposited to serve as a substrate for subsequent deposition of a thicker layer – in the case of Sakamoto, the “electroplated film 56,” which has a disclosed thickness of 18 μm . APPLE-1005, [0122]-[0123]. Seed layers can be used when a deposition method used to form the thicker film is incompatible with an underlying material. Specifically, electroplating (as opposed to electroless plating) is typically incompatible with deposition on insulating layers, because electroplating relies on the presence of a current through conductive materials. *See, e.g.,* Chang (APPLE-

1008) at 1 (“the need of sputtered Cu seed layers for electroplating”); APPLE-1020 at 1477 (“A two-step process is required to produce sputtering/plating-type adhesiveless laminates. The first step is a kind of sputtering process to produce seed layers on substrate films. The seed layers have two functions: to generate conductive layers on the nonconductive plastic films, and to increase the bonding strength between base films and conductor layers. Generally, the sputtered layers are thinner than 100 nm. Therefore, the second step builds the thick conductor layers by electrical plating”); APPLE-1022 at 1 (“Copper (Cu) electroplating (EP) process requires a Cu seed to conduct the current.”).

127. Therefore, in the case of Sakamoto, the electroplating method used to form the electroplated film 56 would likely be incompatible with the underlying interlayer resin insulating layer 50, if not for the presence of the metallic layer 52 in-between, acting as a seed layer. APPLE-1005, [0121][0124], FIG. 6.

128. In view of this purpose of the metallic layer 52, it would have been obvious to make the metallic layer 52 a copper layer instead of a nickel-copper layer. Sakamoto’s disclosures with respect to layers 36 and 37 teach that a copper layer can be an effective seed layer for subsequent electroplating. More specifically, Sakamoto teaches that the second thin film layer 36 can be formed by “sputtering, deposition or electroless plating” (that is, the same methods used to form the metallic layer 52), and that, subsequently, a copper thickening layer 37 is

electroplated on the second thin film layer 36 (the same material and method used to form the electroplated film 56 on the metallic layer 52). APPLE-1005, [0111]-[0114]. The second thin film layer 36 has the function of providing “an electroplating lead for forming a thickening layer [37],” which is the same function performed by the metallic layer 52. APPLE-1005, [0112].

129. For the second thin film layer 36, “**copper** is preferable because the copper has good electrical characteristic and is economical and because a buildup conductor layer to be formed in a layer step mainly consists of copper.” APPLE-1005, [0111]. As such, based on Sakamoto’s recognition that a copper layer can serve the function of a seed layer for subsequent copper electroplating in the second thin film layer 36, it would have been obvious to substitute a copper layer for the nickel-copper metallic layer 52. This would have constituted nothing more than the substitution of copper for nickel-copper, both of which Sakamoto recognizes as equivalent in their function as a seed layer.

130. As another reason for the obviousness of this substitution, in the context of Sakamoto’s parallel discussion that the second thin film layer 36 can be composed of copper, it would have been obvious to try substituting a copper layer for the nickel-copper metallic layer 52, with copper being one of a finite number of identified, predictable materials for forming a layer by electroless plating or sputtering. APPLE-1005, [0111], [0121]-[0122]. It would have been natural for a

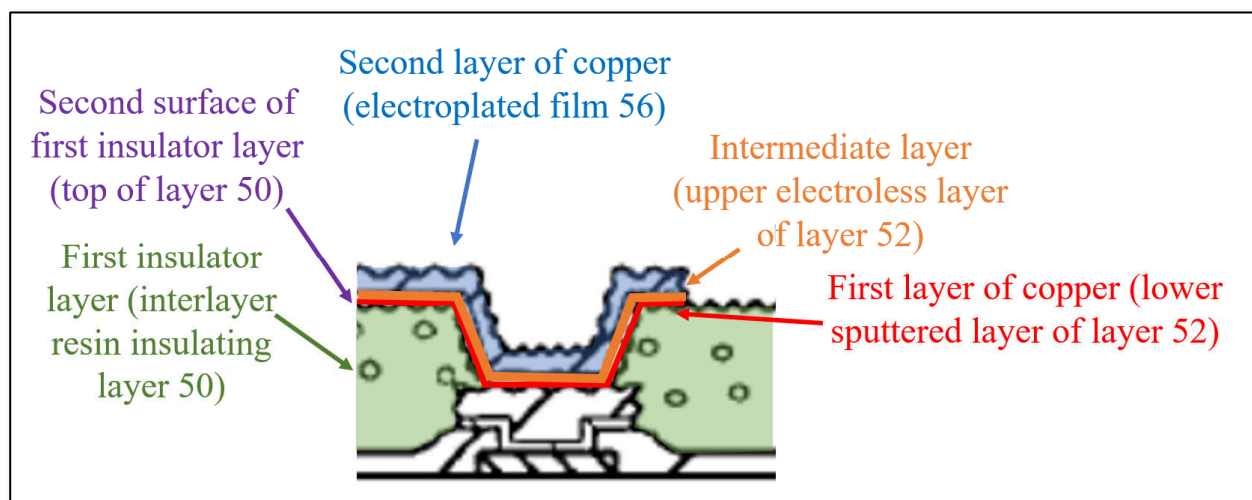
POSITA to try using the relatively small number of common electroless and/or sputtered metals to identify the one(s) providing the best performance.

131. With the metallic layer 52 modified to be a pure “layer of copper,” the metallic layer 52 (“*first layer of copper*”) and the electroplated film 56 (“*second layer of copper*”) satisfy claim 9 even when “*layer of copper*” is interpreted to require pure copper.

[10]: *The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.*

132. As discussed for [1d], Sakamoto’s “metallic layer 52,” which is on the second surface of the *first insulator layer* (interlayer resin insulating layer 50), along with the “electroplated film 56,” are applied as teaching the *conductors*. APPLE-1005, [0121]-[0124].

133. Sakamoto further describes that the metallic layer 52 can be formed by “form[ing] a thin layer by a physical method such as sputtering, deposition or electrode position and then [] conduct[ing] electroless plating.” APPLE-1005, [0122]. That is, Sakamoto teaches that the metallic layer 52 can include a lower sputtered layer and an upper layer formed by electroless plating. This arrangement is shown in annotated FIG. 4(C) below.



Annotated portion of Sakamoto FIG. 4(C)

134. In this configuration of Sakamoto's device, the lower sputtered layer of layer 52 (applied as the "*first layer of copper*") is on the *second surface of the first insulator layer*; the upper layer of layer 52, formed by electroless plating (applied as the "*intermediate layer*") is on the surface of the *first layer of copper*; and the electroplated film 56 (applied as the "*second layer of copper*") is on the surface of the *intermediate layer*. As discussed for [1d], the electroplated film 56 is an electroplated **copper** layer. APPLE-1005, [0123]. Also, the metallic layer 52 is a "Ni/Cu" layer, such that, to the extent "*layer of copper*" is interpreted as "layer containing copper," the lower sputtered layer of layer 52 is a "*first layer of copper*" satisfying claim 10.

135. To the extent "layer of copper" is interpreted as referring to pure metallic copper, it would have been obvious to form the metallic layer 52 (in this

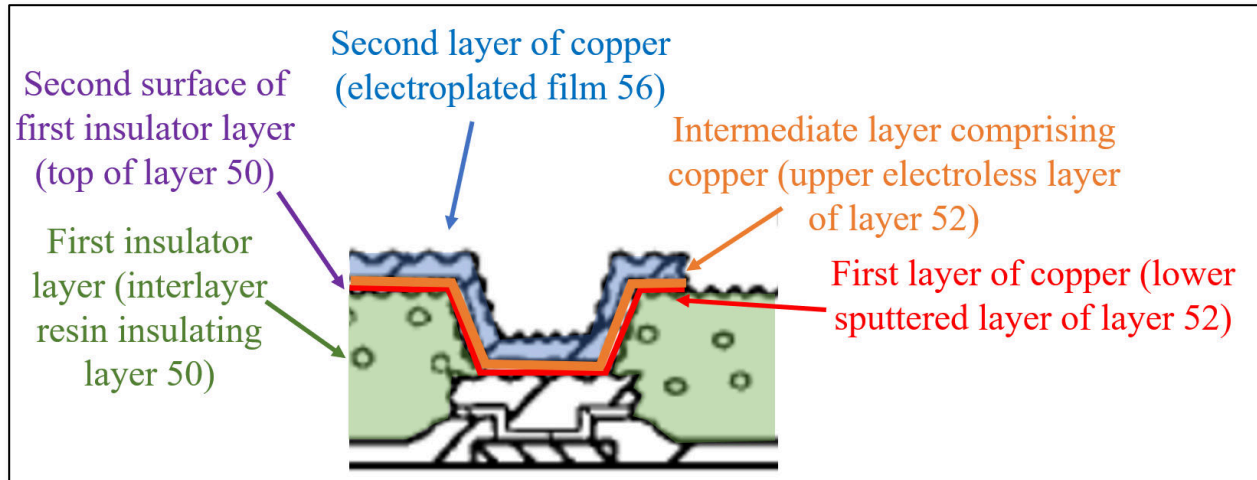
case, the lower sputtered layer and the upper layer formed by electroless plating) as a copper layer for the reasons discussed for [9], such that it would have been obvious to form the lower sputtered layer as a “*first layer of copper.*”

[11]: *The circuit module of claim 10, wherein the intermediate layer between the first and second coppers [sic] layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.*

136. The upper layer of Sakamoto’s layer 52, formed by electroless plating, is an “*intermediate layer*” comprising “*copper grown by a chemical growing method or nickel grown by a chemical growing method.*” As discussed for [10], in the case where the metallic layer 52 includes a lower sputtered copper layer and an upper copper layer formed by electroless plating, the upper layer (*intermediate layer*) comprises copper. APPLE-1005, [0122]. “Electroless plating” is described by the ’324 Patent as a “chemical growing method.” APPLE-1001, 2:56. This is distinguished from the ’324 Patent’s description of “electrochemical growing (electroplating).” APPLE-1001, 2:40-41.

137. As such, Sakamoto’s copper upper layer formed by electroless plating comprises “*copper grown by a chemical growing method.*”

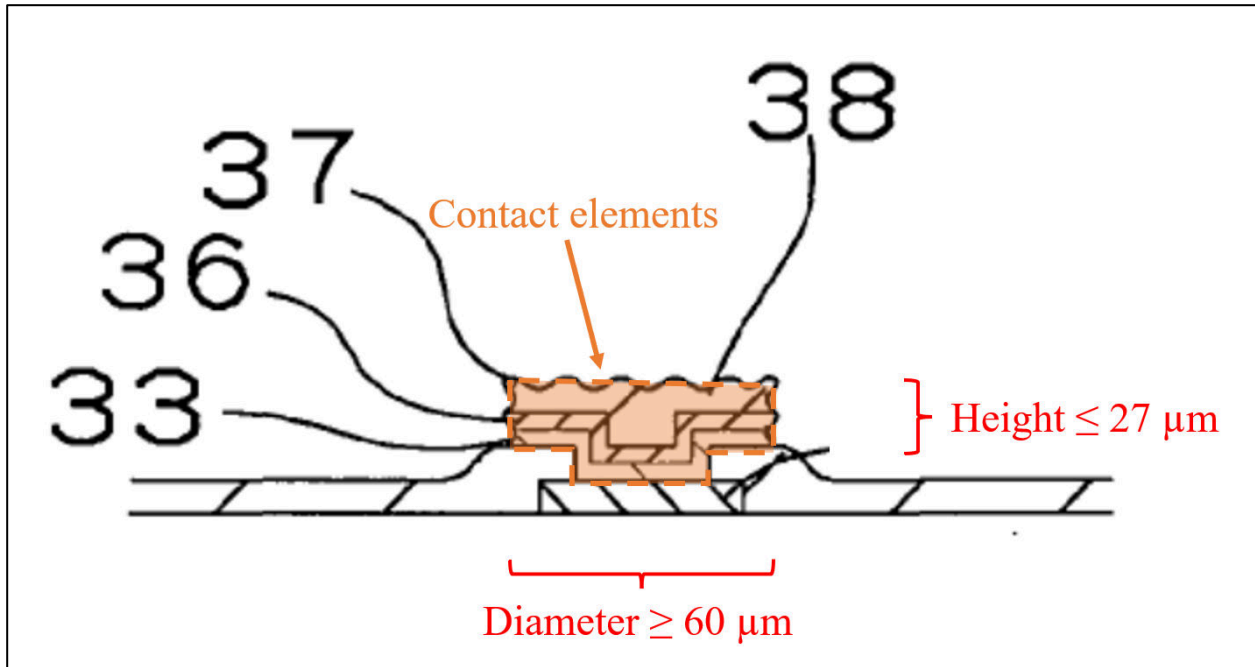
138. As an alternative to pure copper, the upper layer of layer 52 can be an “Ni/Cu” layer as directly disclosed by Sakamoto, in which case the upper layer also “*comprises copper.*” APPLE-1005, [0121]-[0122].



Annotated portion of Sakamoto FIG. 4(C)

[13]: The circuit module of claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (W_{MAX}) of the contact element.

139. Sakamoto's layers 33, 36, and 37, together corresponding to the "contact element," have a total height less than or equal to their greatest width. Sakamoto describes that the first thin film layer 33 has a greatest thickness of 2.0 μm , that the second thin film layer 36 has a greatest thickness of 5 μm , and that the thickening layer 37 has a greatest thickness of 20 μm . APPLE-1005, [0109], [0112], [0116]. Accordingly, the greatest thickness taught by Sakamoto for the "contact element" is 27 μm . Sakamoto also describes that the transition layer 38 (that is, layers 33, 36, and 37 together) has "a diameter of 60 μm or more." APPLE-1005, [0119]. Because 60 μm (W_{MAX}) is greater than 27 μm (H), Sakamoto satisfies claim 13.

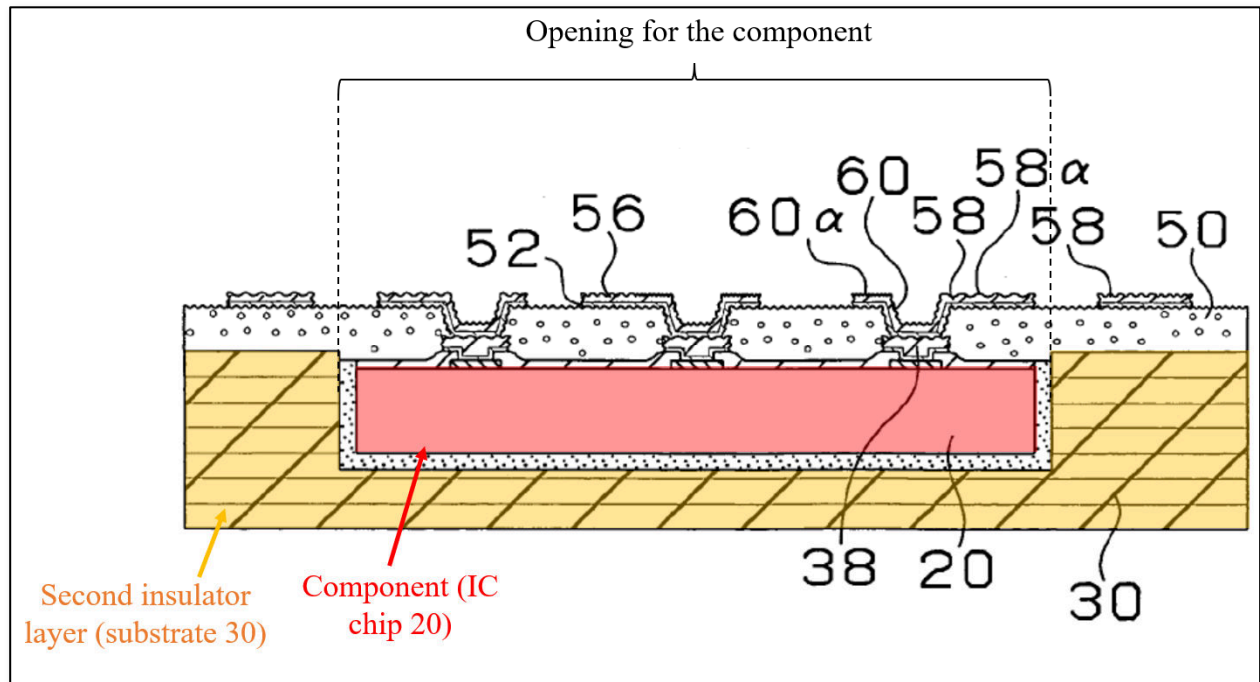


Annotated portion of Sakamoto FIG. 7(A)

[14]: The circuit module of claim 1, wherein the at least one second insulator layer contains at least one layer of fibre material and an opening in the fibre material for the at least one component.

140. Sakamoto's substrate 30 is a "second insulator layer" satisfying claim 14. As discussed for [1b] above, the "insulating resin substrate (or core substrate) 30" is applied as the "second insulator layer." APPLE-1005, [0106]. The substrate 30 includes "prepegs each having a core material made of glass **cloths** or the like." APPLE-1005, [0106]. The disclosure of "cloths," along with more generally Sakamoto's description of prepegs, teaches the presence of "*at least one layer of fibre material*" in the substrate 30. See APPLE-1020 Chapter 6.

141. Further, as shown in annotated FIG. 4(C) below, the fibre material of the substrate 30 includes an opening for IC chip 20 (the “*at least one component*”).

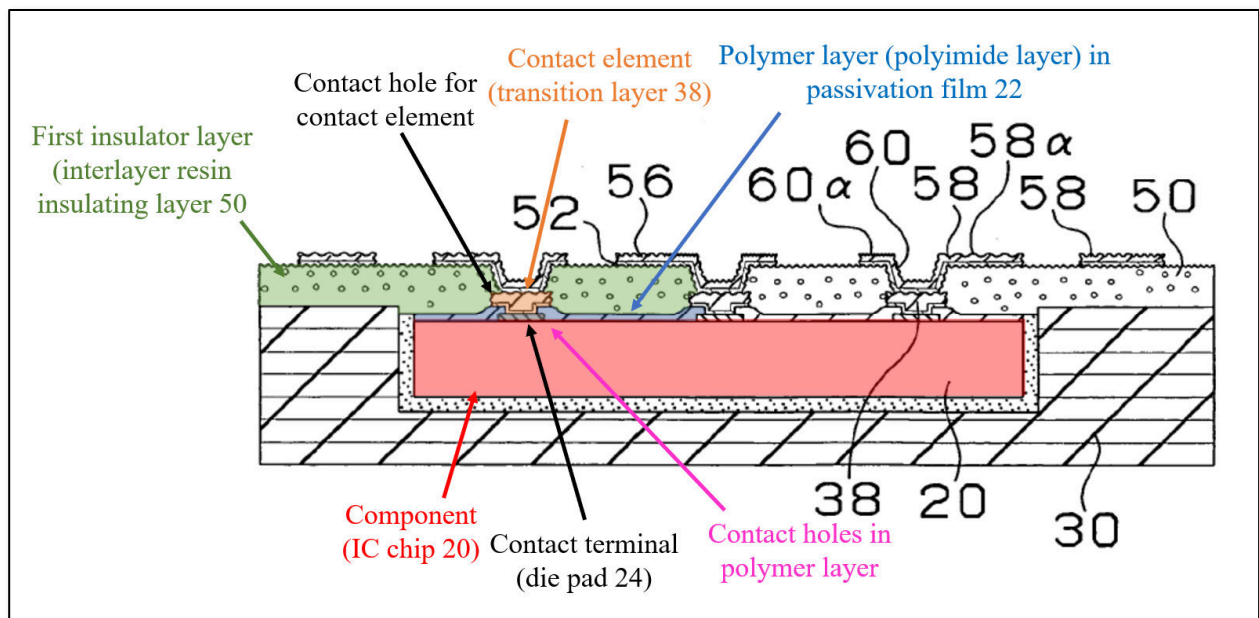


Annotated Sakamoto FIG. 4(C)

[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

142. Sakamoto’s “polyimide layer” is a “*polymer layer*” satisfying claim 15. For example, Sakamoto discloses that a polyimide layer (an example of a *polymer layer*) can be provided together with the passivation film 22. Polyimide is a well-known and common polymer. Sakamoto’s Background section assumes the presence of a “polyimide layer (or protective layer of the IC)” that is damaged by a

laser if “the via diameter is larger than the diameter of the die pad.” APPLE-1005, [0012]. Because the laser in this scenario would impinge outside and adjacent to the die pads 24, the polyimide layer would be located together with the passivation film 22. As shown in annotated FIG. 4(C) below, the passivation film 22 is between the interlayer resin insulating layer 50 (“*first insulator layer*”) and the IC chip 20 (“*at least one component*”), and the passivation film 22 includes contact holes for the transition layer 38 (“*contact elements*”). APPLE-1005, [0101], FIG. 6. As such, Sakamoto discloses the presence of a polyimide layer (“*polymer layer*”) having the arrangement of the passivation film 22 and satisfying claim 15.



Annotated Sakamoto FIG. 4(C)

143. Further, in reference to a “third embodiment” (distinct from the “first embodiment” that has heretofore been the focus of discussion), Sakamoto describes that “[t]he IC chip 420 is covered with an IC protective film (made of

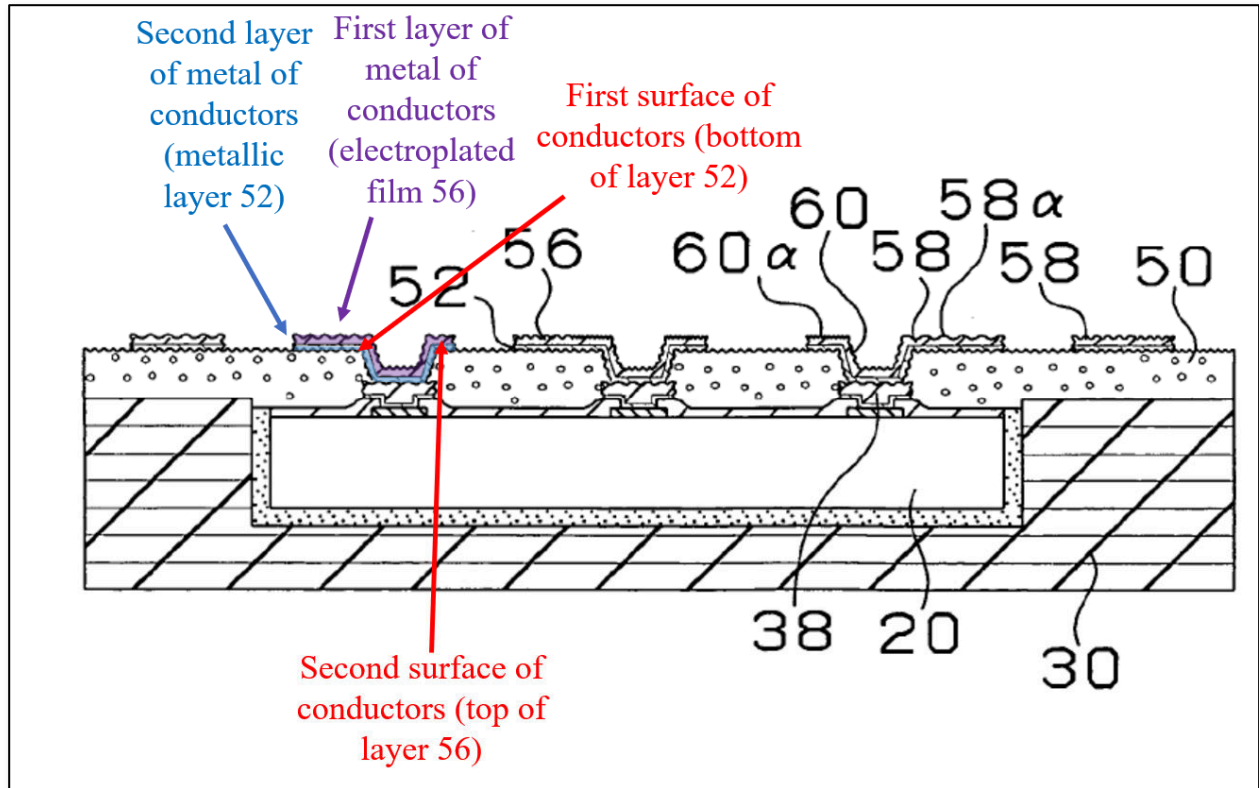
passivation+polyimide) 422.” APPLE-1005, [0202]. Accordingly, to the extent the polyimide is not already understood as being present, it would have been obvious to also include the polyimide (a polymer) in the passivation film 22 of the first embodiment in order to achieve the “protective” characteristics that Sakamoto describes are provided by a “polyimide layer.” APPLE-1005, [0012]. For example, APPLE-1020 describes that polyimide is the “dielectric of choice” for use “with thin-film copper conductors.” APPLE-1020, 74. The polyimide would have the positioning and configuration of the passivation film 22 and therefore satisfy claim 15.

[17pre]: Circuit module, comprising:

144. *See discussion at [1pre] above.*

[17a]: a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;

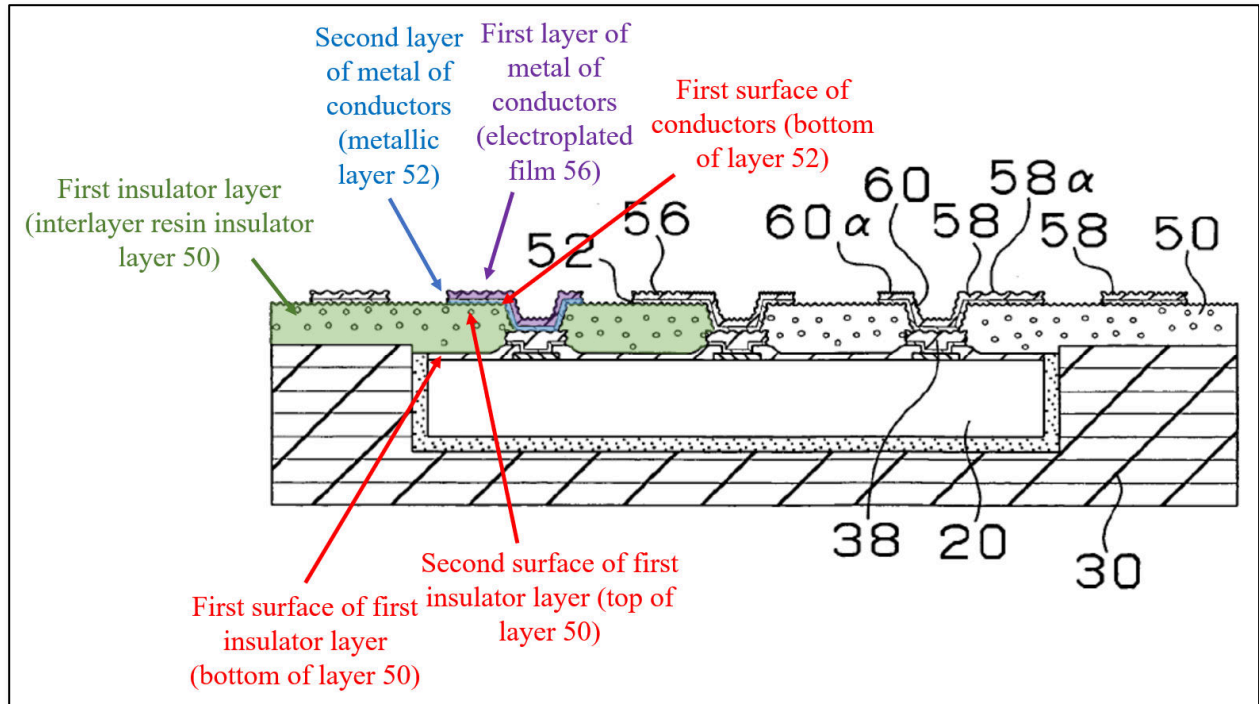
145. *See discussion at [1d]. Sakamoto’s “metallic layer 52” and “electroplated film 56,” together applied as “a conductor layer” and “conductors,” are “two layers of metal” between first and second surfaces, as shown below. APPLE-1005, [0121]-[0123]. For example, the metallic layer 52 is composed of “Ni/Cu” (a metal), and the electroplated film 56 is composed of copper (a metal). APPLE-1005, [0121]-[0123].*



Annotated Sakamoto FIG. 4(C)

[17b]: a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer covering the first surface of the conductors;

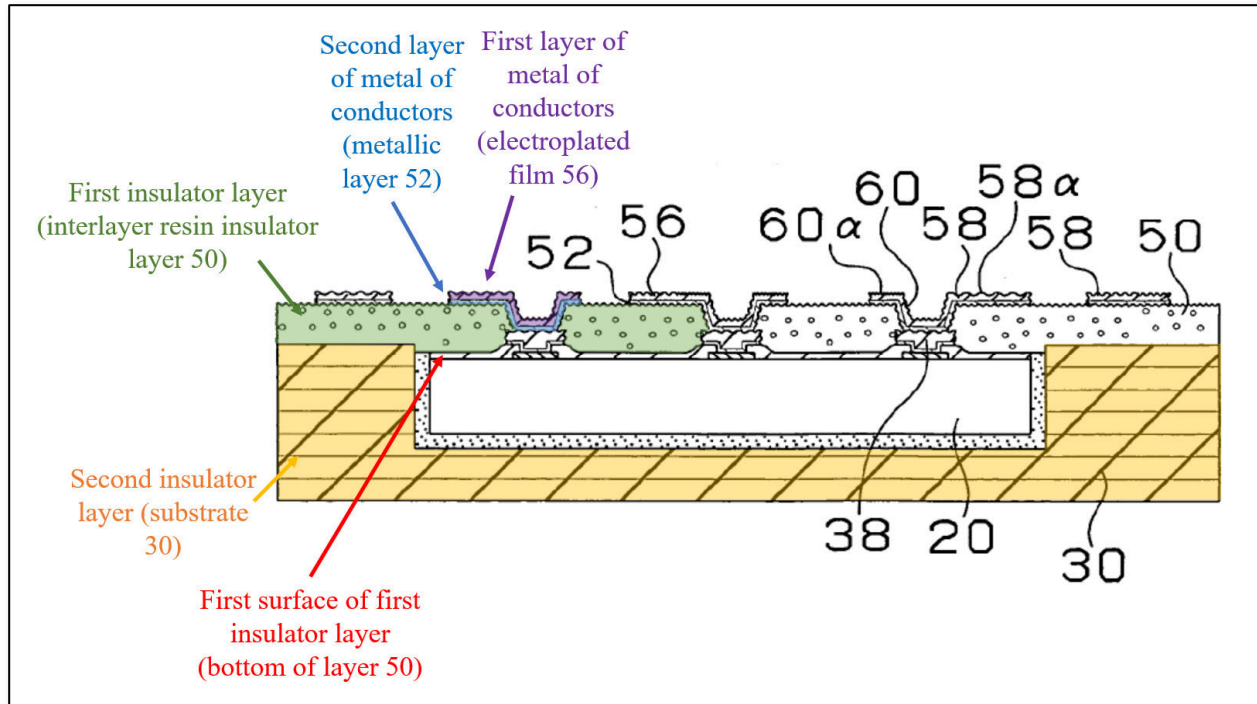
146. See discussion at [1a]. Sakamoto's interlayer resin insulation layer 50 is a "first insulator layer" having a first (bottom) surface and a second (top) surface covering the first (bottom) surface of the conductors.



Annotated Sakamoto FIG. 4(C)

[17c]: at least one second insulator layer on the first surface of the first insulator layer;

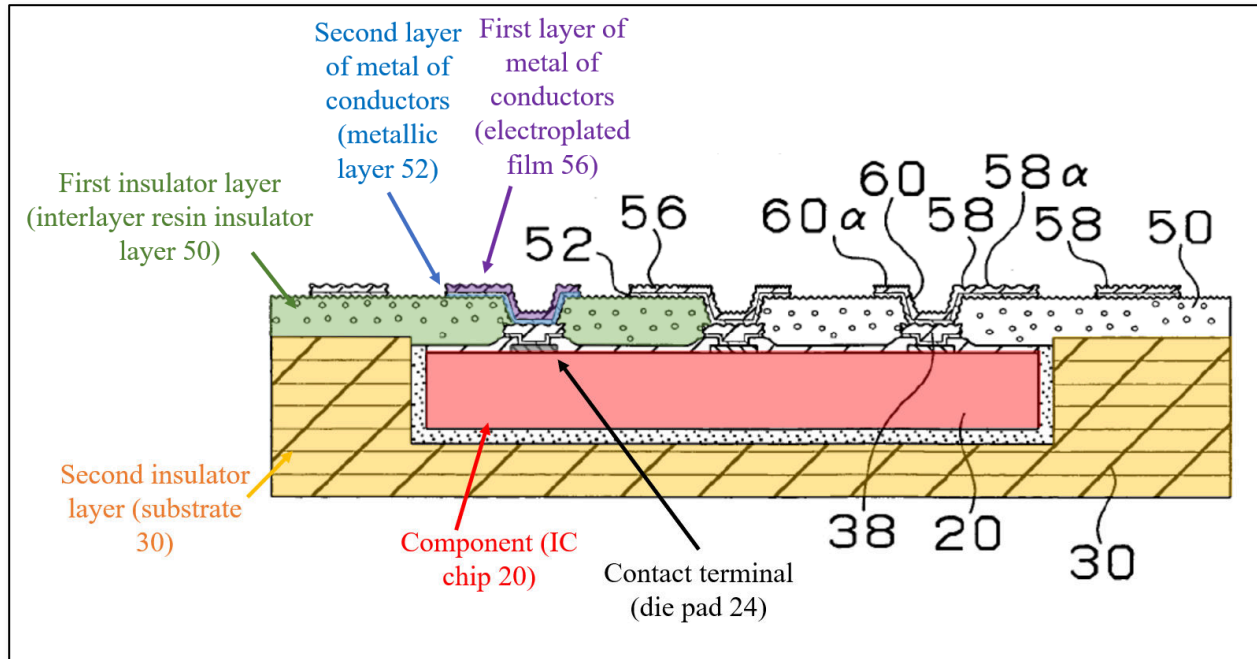
147. See discussion at [1b]. Sakamoto's "insulating resin substrate (or core substrate) 30" is a "second insulator layer on the first surface of the first insulator layer." APPLE-1005, [0106].



Annotated Sakamoto FIG. 4(C)

[17d]: at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal;

148. See discussion at [1c]. The “IC chip 20” is a “component” that is inside the “second insulator layer” (the insulating resin substrate 30). APPLE-1005, [0108], FIG. 6. The IC chip 20 comprises “die pads 24,” which, “each constituting an input/output terminal,” are contact terminals. APPLE-1005, [0101], FIG. 6. The die pads 24 are composed of aluminum and therefore contain “at least one layer of metal.” APPLE-1005, [0051], [0101].



Annotated Sakamoto FIG. 4(C)

[17e]: contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,

149. See discussion at [1e]. Sakamoto's "transition layer 38," between the "contact terminals" (die pads 24) and the "conductors" (conductor circuits 58 including metallic layer 52 and electroplated film 56), constitutes "contact elements." APPLE-1005, [0101], FIG. 6. The transition layer 38 includes an "intermediate layer" (first thin film layer 33) that contains at least one layer of



150. See discussion at [1f]. A contact surface area between the first thin film layer 33 (“*intermediate layer*”) and the die pad 24 (“*contact terminal*”) is less than a surface area of the die pad 24. APPLE-1005, FIG. 6.

[17g]: at least one layer of metal in the contact terminals containing a first metal; at least one layer of metal in the conductors containing a second metal; and the intermediate layer containing a third metal.

151. See discussion at [1c], [1d], and [1e] above. Sakamoto's die pads 24 ("contact terminals") are composed of **aluminum**, a first metal; the metallic layer 52 (included in the "conductors") is composed of **copper** and **nickel**, either of which is a second metal; and the first thin film layer 33 ("intermediate layer") can be composed of "**tin, chromium, titanium, [] zinc, cobalt, [or] gold.**" APPLE-1005, [0051], [0101], [0109]-[0110], [0123].

[19]: Circuit module, comprising

a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;

a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer entirely covering the first surface of the conductors;

at least one second insulator layer on the first surface of the first insulator layer;

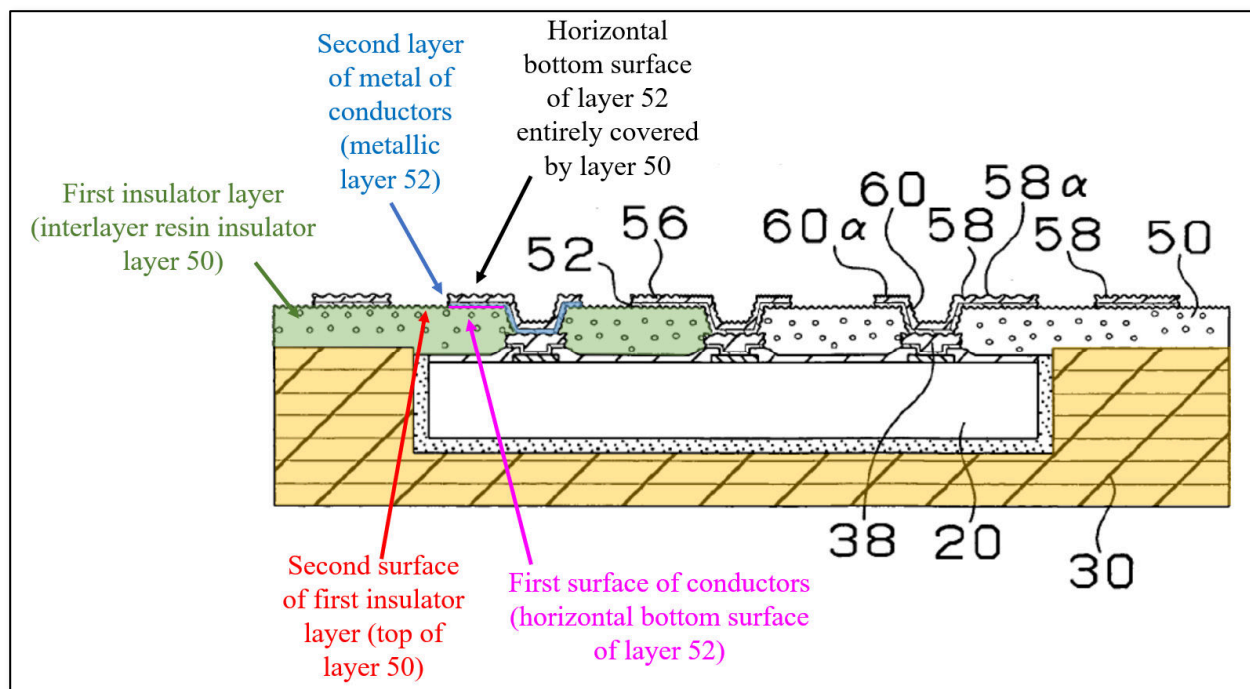
at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal; and

contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements

comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,

a contact surface area (ACONT 1) between the intermediate layer and the contact terminal being less than a surface area (APAD) of the contact terminal.

152. See discussion at claims 1 and 17 above. Claim 19 is identical to claim 17 except for (1) omitting recitation of the first, second, and third metals and (2) reciting “*the second surface of the first insulator layer entirely covering the first surface of the conductors.*” The latter element is satisfied by the top surface of Sakamoto’s interlayer resin insulating layer 50 (“*first insulator layer*”) entirely covering the bottom horizontal surface of the metallic layer 52 (included in the “*conductors*”), the bottom horizontal surface being the “*first surface of the conductors*” applied for claim 19. APPLE-1005, FIG. 6.



Annotated Sakamoto FIG. 4(C)

X. GROUND 1B: Claims 3 and 9-11 are obvious over Sakamoto in view of Eichelberger

153. Based on my analysis, Sakamoto and Eichelberger render obvious claims 3 and 9-11.

A. Analysis of Claims

[3]: *The circuit module of claim 1, wherein the first metal is gold, the second metal is copper, and the third metal is nickel.*

154. In the mapping applied above for claim 1, the “*first metal*” of Sakamoto’s die pad 24 is aluminum, the “*second metal*” of Sakamoto’s metallic layer 52 is copper or nickel, and the “*third metal*” of Sakamoto’s first thin film layer 33 is “tin, chromium, titanium, [] zinc, cobalt, [or] gold.” APPLE-1005,

[0051], [0101], [0109], [0123]. The first thin film layer 33 can also include nickel or copper. APPLE-1005, [0109].

155. In view of Eichelberger, it would have been obvious to have the die pad 24 include gold (instead of or in addition to aluminum), such that the “*first metal*” is gold. Eichelberger describes that “[c]ertain GaAs IC chips have **gold pads**.” APPLE-1006, 9:42-43. For example, Eichelberger describes that “a Global Positioning System (GPS) module consist[s] of three separate IC chips []. The front end [IC chip] is GaAs with gold bond pads.” APPLE-1006, 9:53-55. Gold bond pads are widely known as particularly applicable to GaAs devices compared to silicon devices, because gold forms deep trap states in silicon but forms effective Ohmic contacts to GaAs. *See* APPLE-1023.

156. In at least the case where the IC chip 20 of Sakamoto is a GaAs IC chip, it would have been obvious to form the die pad 24 as a gold pad, based on Eichelberger’s description that GaAs IC chips have gold pads. APPLE-1006, 9:42-43. Sakamoto discloses no restriction as to the type of the IC chip 20, and a GaAs chip would be one of various chip types that could be used as the IC chip 20, in addition to, for example, silicon chips. In that context, causing the die pad 24 to contain gold would simply be a selection of one of a finite number of identified, predictable materials for die pads, in addition to the aluminum disclosed by Sakamoto and Eichelberger and the copper and nickel disclosed by Eichelberger.

APPLE-1005, [0051], [0101]; APPLE-1006, 9:38-59. It would have been obvious for a POSITA to try using these materials as the die pads 24 to make effective (e.g., Ohmic or low-resistance) contact with the IC chips 20.

157. Also, Sakamoto describes that gold may be integrated elsewhere in Sakamoto's circuit board (e.g., as the first thin film layer 33 or the second thin film layer 36), such that the use of gold for the die pad 24 would not constitute the introduction of an entirely new material. APPLE-1005, [0109]-[0111]. That is, a POSITA would recognize that Sakamoto teaches gold as being generally compatible with Sakamoto's processes and materials, and as such would naturally have tried using gold for the die pads 24 as a matter of routine experimentation.

158. Further, a POSITA would have been motivated by specific advantages provided by gold. For example, Sakamoto describes that the oxidation of aluminum pads "causes an increase in the connection resistance of the pad," and a POSITA, based on the common knowledge that gold is resistant to oxidation, would have found it obvious to try using gold to achieve lower connection resistance. APPLE-1005, [0051]. Indeed, gold was widely known as an effective material to include as, or as part of, contact terminals. For example, Green describes that "[i]n the micro-electronics industry, the electrodeposition of gold has been traditionally used to metallise contact pads on semiconductor integrated circuits (ICs)." Gold provides "excellent corrosion resistance, solderability and

bondability and [] high electrical and thermal conductivity.” *Id.* It would have been obvious for a POSITA to try to realize these advantages by having the die pad 24 contain gold, e.g., as an entirety of the die pad 24 or as a deposited layer of the die pad 24 as taught by Green.

159. In addition, the use of gold as, or as part of, the die pad 24 would have been compatible with subsequent deposition of the first thin film layer 33 on the die pad 24. Although Eichelberger describes that “electroless nickel will not deposit on the gold,” Sakamoto discloses that the first thin film layer 33 can be deposited by sputtering as opposed to electroless plating, permitting deposition of the first thin film layer 33. APPLE-1006, 9:47-48; APPLE-1005, [0109]. Sakamoto further describes that the use of nickel is “preferable,” further reinforcing Sakamoto’s disclosure of having the first thin film layer 33 contain nickel as the “*third metal*.” APPLE-1005, [0109]. In view of its compatibility with deposition of the first thin film layer 33 on the die pad 24, the substitution of gold for aluminum in the die pad would have been within the skill of a POSITA.

160. Accordingly, having the die pad 24 contain **gold** as the “*first metal*,” the metallic layer 52 contain **copper** as the “*second metal*,” and the first thin film layer 33 contain **nickel** as the “*third metal*” would have been obvious.

[9]: *The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, and a second*

layer of copper on the surface of the first copper layer.

161. As discussed for [9], claim 9 is taught by Sakamoto. Claim 9 is also obvious over Sakamoto in view of Eichelberger. The “Cu/Ni” metallic layer 52 serves as a seed layer for subsequent electroplating of the copper electroplated film 56, and the arguments for Ground 1A describe why, in the case where “*layer of copper*” is interpreted as requiring pure metallic copper, it would have been obvious to modify the copper-nickel metallic layer 52 to be pure metallic copper.

162. Eichelberger corroborates and reinforces the obviousness of this modification by directly disclosing the use of an “electroless [deposited]” “**copper** seed layer 109’ deposited over polymer surface 106.” APPLE-1006, 8:10-11, 8:22. This arrangement is similar to that of Sakamoto’s metallic layer 52, which is deposited by electroless plating over the surface of the interlayer resin insulating layer 50. APPLE-1005, [0121]. Layer 109 is then “plated up” on the seed layer 109’, matching Sakamoto’s description that an electroplated copper film 56 is formed on the metallic layer 52. APPLE-1006, 8:16-25; APPLE-1005, [0123]. That is, both Sakamoto’s metallic layer 52 and Eichelberger’s copper seed layer 109 are deposited onto an insulating layer by electroless deposition, and both layers are then further plated. This teaches the suitability of copper as a seed layer material, e.g., as opposed to copper-nickel.

163. In view of Eichelberger's corroborating description, it would have been obvious to make the metallic layer 52 and the electroplated film 56 first and second layers of copper, respectively.

[10]: The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.

164. See discussion at [9] and [10] for Ground 1A and [9] for Ground 1B. For the reasons provided for [9] for Ground 1B, Eichelberger reinforces the obviousness of forming a lower sputtered layer of the metallic layer 52 as a copper layer to be the "*first layer of copper*" and forming an upper layer of the metallic layer 52 as a copper layer to be the "*intermediate layer*," in the case where "*layer of copper*" is interpreted as requiring pure metallic copper. APPLE-1005, [0122], FIG. 6. The electroplated film 56 is a "*second layer of copper on the surface of the intermediate layer*." APPLE-1005, [0123], FIG. 6.

[11]: The circuit module of claim 10, wherein the intermediate layer between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.

165. See discussion at [9]-[10] for Grounds 1A and 1B. The upper layer of the metallic layer 52, formed by "electroless plating," is an "*intermediate layer*"

“*grown by a chemical growing method*” and arranged as recited in claim 11.

APPLE-1005, [0122], FIG. 6. For the reasons provided for [9] for Ground 1B, Eichelberger reinforces the obviousness of having this upper layer, which serves as a seed layer for subsequent electroplating, be pure copper, in the case where “*layer of copper*” is interpreted as requiring pure copper.

166. Alternatively, the upper layer can be an “Ni/Cu” layer as disclosed by Sakamoto, in which case the upper layer also “*comprises copper.*” APPLE-1005, [0121]-[0122].

XI. GROUND 1C: Claims 9-11 are obvious over Sakamoto in view of Chang

167. Based on my analysis, Sakamoto and Chang render obvious claims 9-11.

A. Combination of Sakamoto and Chang

168. Chang provides further evidence that, as discussed for [9]-[11] for Grounds 1A and 1B, it would have been obvious to make Sakamoto’s metallic layer 52 a copper layer rather than a copper-nickel layer, in the case where “*layer of copper*” is interpreted as requiring pure metallic copper. As discussed for [9] for Ground 1A, the copper-nickel metallic layer 52 functions as a seed layer to permit the subsequent deposition of the electroplated film 56, e.g., because electroplating may not be possible on the interlayer resin insulating layer 50 on which layer 52 is deposited. However, Chang demonstrates that the use of **copper** seed layers results

in “**smooth surfaces** of [subsequently] electrodeposited [electroplated] Cu films” analogous to the electroplated film 56 deposited on the metallic layer 52. APPLE-1005, [0121]; APPLE-1008, 5. These electrodeposited Cu films exhibited “high purity, small roughness, low electrical resistivity, low residual stresses, good adhesion to substrates, and excellent superfilling.” APPLE-1008, 7.

169. Based on this, a POSITA would have recognized that the metallic layer 52 need not be a copper-nickel layer but, rather, that a layer of copper would be suitable for the function of the metallic layer 52. Indeed, based on Chang’s disclosure of the high quality of the resulting electroplated Cu films, the POSITA would have been motivated to use a layer of copper to achieve those same advantages. APPLE-1008, 7. A POSITA would also have identified that Sakamoto (for layer 56 deposited on layer 52) and Chang both employ electroplating solutions including sulfuric acid and copper sulfate, such that the POSITA would have expected the advantages provided by Chang’s copper seed layers to also be provided by a copper metallic layer 52, e.g., based on Chang, Sakamoto’s electroplating process would have been compatible with a copper seed layer. APPLE-1005, [0123]; APPLE-1008, Table II.

170. In view of this fundamental similarity in their electroplating processes, it would have been within the skill of a POSITA to successfully electroplate the copper seed layer, e.g., by routine adjustment of the parameters

(e.g., current density, duration, and temperature) that Sakamoto and Chang recognize as relevant for electroplating. APPLE-1005, [0124]; APPLE-1008, 2. It also would have been within the skill of a POSITA to successfully deposit the copper seed layer itself, in view of Chang's detailed process discussion and the similarity of Sakamoto's and Chang's electroless plating solutions. APPLE-1005, [0121]; APPLE-1008, Table I.

171. Therefore, it would have been obvious for a POSITA to make the metallic layer 52 a layer of copper.

B. Analysis of claims

172. [9], [10], [11]: See corresponding discussion of claims 9-11 for Ground 1B. For the reasons provided there and in Section XI.A, Chang further evidences the obviousness of making the metallic layer 52 a "*first layer of copper*," including, in the case of claim 11, making the lower sputtered layer and upper electroless layer of the metallic layer 52 layers of copper. The reasoning is otherwise identical to that provided for claims 9-11 for Grounds 1A and 1B.

XII. GROUND 1D: Claims 12, 13, and 15 are obvious over Sakamoto in view of Ito

173. Based on my analysis, Sakamoto and Ito render obvious claims 12, 13, and 15.

A. Analysis of claims

[12]: The circuit module of claim 1, wherein a width (W_{CONT}) of the contact

surface between the contact element and the contact terminal of the component is 0-20% less than a greatest width (W_{MAX}) of the contact element in the same direction.

174. It would have been obvious to replace Sakamoto's first thin film layer 33 with Ito's zincated zinc layer 4, on Sakamoto's die pad 24, such that a width of the contact surface between the zinc layer 4 (the "*contact element*") and the die pad 24 ("*contact terminal*") is 0-20% less than a greatest width of the zinc layer 4.

175. This modification would have been obvious for several reasons. First, as discussed in Section VI.A, zincating was a widely-used, conventional first step for forming contact stacks on aluminum pads. As a POSITA would have recognized, the zinc layer would prevent oxidation of the aluminum die pad 24 and provide a surface for subsequent electroless deposition of the second thin film layer 36. Indeed, Sakamoto recognizes that oxidation of the aluminum die pad 24 may be problematic, describing, in relation to a "third embodiment," that an "oxide film removal process" is performed on an "oxide film [] formed on the die pads [] made of aluminum" "to reduce the electrical resistances of the die pads." APPLE-1005, [0200], [0206]. In view of Ito's disclosure that "oxide on the aluminium surface is removed by zincating to form the zinc layer 4," it would have been obvious for a POSITA to form the zinc layer to remove the oxide film and obtain lower resistances. APPLE-1012, [0093]. It is typically desirable to reduce contact

resistance as much as possible, and, because aluminum oxide is a dielectric, the presence of aluminum oxide can cause increased resistance.

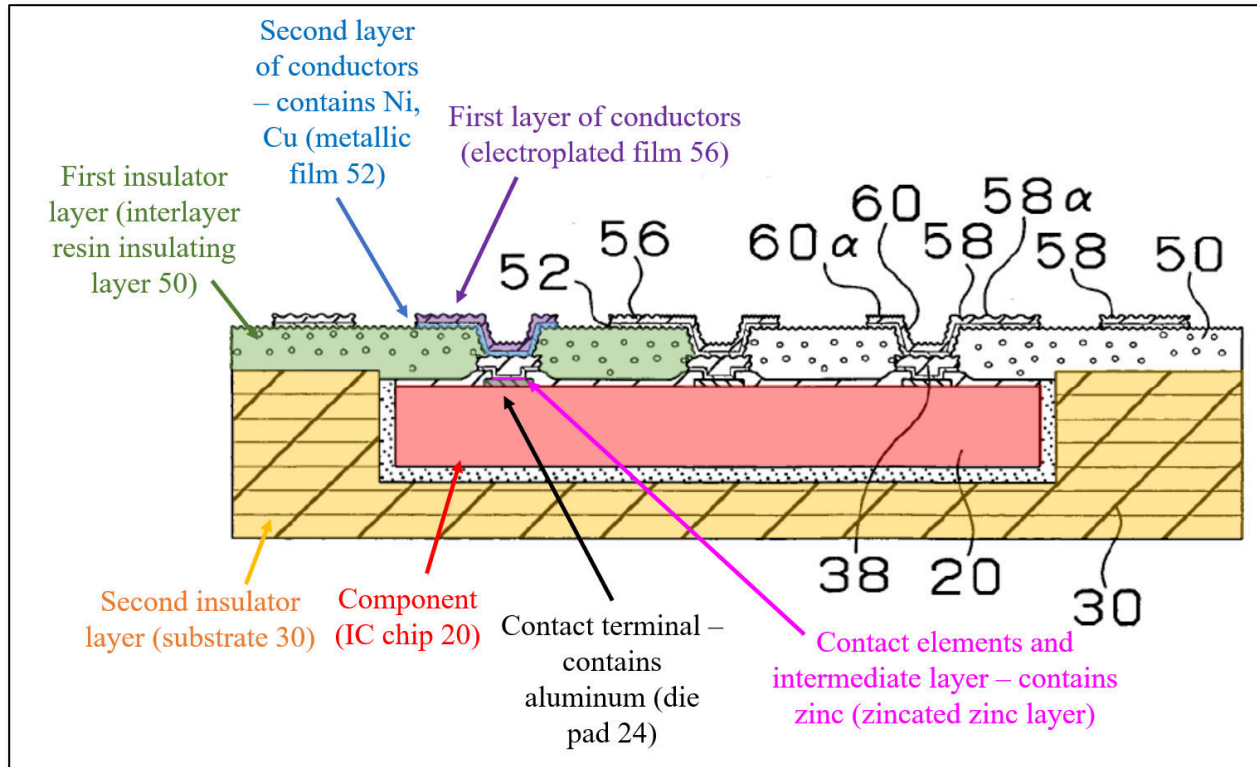
176. Further, as a POSITA would have recognized, the zinc layer 4 would be a close structural and functional substitute for the first thin film layer 33. The two layers have similar thicknesses (0.3 μm for the zinc layer 4, near the middle of the “0.01 to 1.0 μm ” range of the first thin film layer 33), can both be composed of zinc, are both described as providing improved adhesion to the underlying pad, and are both subsequently covered by a layer that can be electroless nickel. APPLE-1005, [0109]-[0111]; APPLE-1012, [0082], [0091], [0095]. *See* Ito’s disclosure that “a nickel-plated layer 5 having a thickness of about 5 μm is formed on the terminal electrode 2, on which the zinc layer 4 has been formed, by an electroless plating method.” APPLE-1012, [0095]. As such, the simple substitution of the zinc layer 4 for the first thin film layer 33 would have been obvious.

177. It also would have been obvious to perform zincation for the first thin film layer 33 to achieve other advantages disclosed by Ito in association with zincation, e.g., “reliable adhesion,” a nickel-plated layer “reliably, firmly formed on the terminal electrode,” and “self-aligned” fabrication “so that no patterning step is needed. APPLE-1012, [0082], [0096].

178. In this modified Sakamoto-Ito circuit board, the zinc layer constitutes both the “contact elements” and the “intermediate layer.” Mappings of the

modified Sakamoto-Ito circuit board to the elements of claims 1 and 12, shown in the annotated figure and table below, are otherwise identical to those discussed for claim 1 in Ground 1A. As shown in this figure, the zinc layer is limited to the extent of the underlying die pad (*contact terminal*), because of the “self-aligned” growth of the zinc layer 4, which naturally forms only on the aluminum die pad “so that no patterning step is needed.” APPLE-1012, [0096]. *See* Section VI.A above.

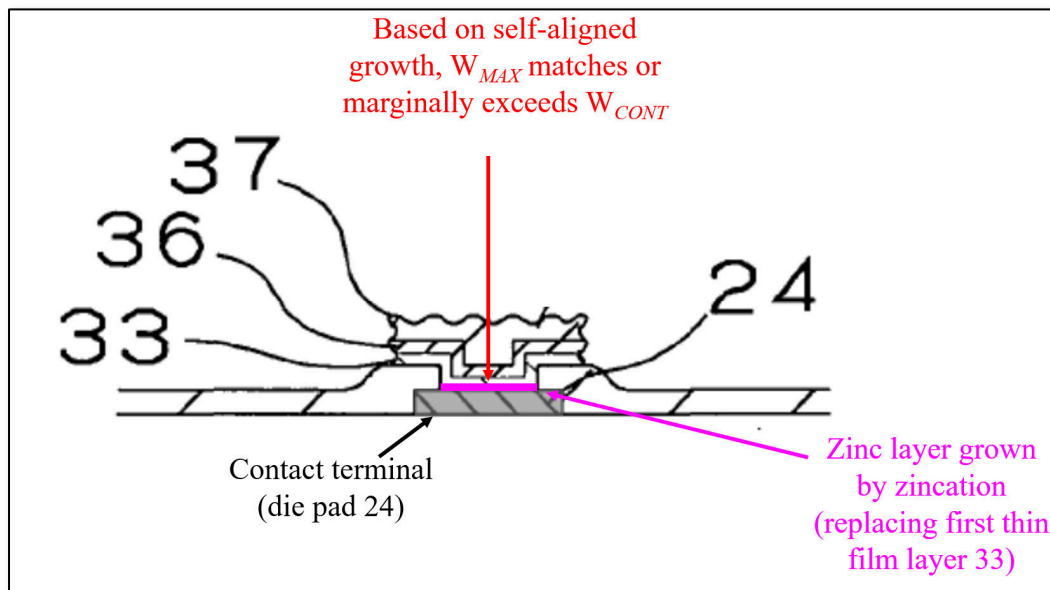
First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	• Metallic layer 52 (<i>second layer</i>), and • Electroplated film 56 (<i>first layer</i>)	Cu or Ni	• Zinc layer 4 (<i>intermediate layer</i>)	Zn



Sakamoto-Ito circuit board based on Sakamoto FIG. 4(C)

179. In this Sakamoto-Ito circuit board, because of the self-aligned nature of the zinc growth directly on the aluminum die pad 24, a width of the contact surface between the zinc layer (*contact elements*) and the die pad 24 (*contact terminal*) is 0-20% less than a greatest width of the zinc layer in the same direction, satisfying claim 11. That is, the width of the contact surface is substantially equal to (or 0% less than) the greatest width of the zinc layer, within the scope of the claim. To the extent the zinc layer may grow marginally laterally beyond the exposed surface of the die pad 24 based on sloped sidewalls of the contact hole, this growth would be very limited (e.g., “0.3 μm” of width compared to a “30 μm” diameter of Ito’s opening 9, which is compatible with the “40 μm”

diameter of the die pad 24), and the zinc layer would still satisfy claim 12. APPLE-1005, [0104]; APPLE-1012, [0091], [0106]. 0.3 μm corresponds to the maximum possible lateral growth of the zinc layer beyond the die pad 24 and the die pad's contact surface, given the disclosed zinc thickness of 0.3 μm . APPLE-1012, [0091]. Further, 0.3 μm is only 1% of 30 μm , such that, even with this level of lateral growth of the zinc layer, W_{CONT} would be only 1% less than W_{MAX} .



Annotated Sakamoto FIG. 7(A)

[13]: The circuit module of claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (W_{MAX}) of the contact element.

180. The zinc layer of the Sakamoto-Ito device – applied as the “contact element” as for [12] – has a height $H = “0.3 \mu\text{m}.”$ APPLE-1012, [0091]. This height is significantly less than the contact element (width of the zinc layer), which

is approximately 30 μm based on Ito's opening diameter. APPLE-1012, [0106].

The contact element width is approximately 30 μm because the contact element (zinc layer) grows selectively/self-alignedly on the portion of the die pad 24 exposed by the opening, which would be obvious to form with Ito's 30 μm diameter as a matter of design choice.

[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

181. It would have been obvious to use Ito's "first passivation layer 101" as, or in, Sakamoto's "passivation film 22," such that the first passivation layer 101 is a "*polymer layer*" between the "*first insulator layer*" (insulator resin insulating layer 50) and the "*component*" (IC chip 20) and includes contact holes for the "*contact elements*" (die pads 24). APPLE-1005, FIG. 6. Specifically, Ito discloses that a "first passivation layer 101 includes a benzocyclobutene (BCB) resin or a polyimide resin." APPLE-1012, [0010]. Both of these materials are polymers.

182. In view of Ito's disclosure that these materials can be used for a "passivation layer," it would have been obvious to use a layer of one of these polymer materials as, or in, Sakamoto's "passivation film," thereby satisfying claim 15. The obviousness is reinforced by Sakamoto's explicit disclosure that the

passivation film 422 of another embodiment includes “polyimide.” APPLE-1005, [0202]. Therefore, the selection of BCB resin or polyimide resin for the passivation film 22 would have been merely the selection of a material known to provide passivation.

XIII. GROUND 1E: Claims 15-16, 18, and 20 are obvious over Sakamoto in view of Tuominen

183. Based on my analysis, Sakamoto and Tuominen render obvious claims 15-16, 18, and 20.

A. Analysis of Claims

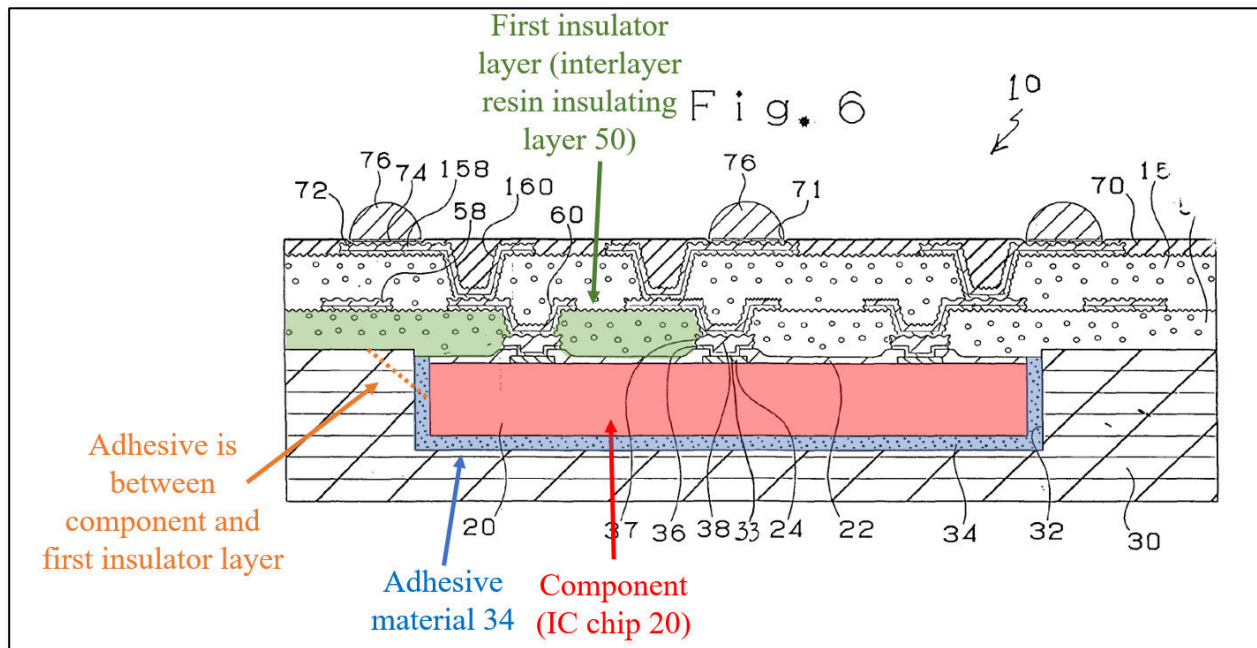
[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

[16]: The circuit module of claim 15, wherein the polymer layer comprises layer of a hardened adhesive.

184. It would have been obvious to introduce Tuominen’s “adhesive 5” in-between Sakamoto’s interlayer resin insulating layer 50 and IC chip 20 to attach the layer 50 (which is “vacuum-compression laminated onto the substrate”) to the IC chip 20. It would have been obvious to have the adhesive 5 be hardened to better secure the layer to the IC chip 20. *See* [15]-[16] in Ground 2E.

[18]: The circuit module of claim 17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

185. In view of Tuominen, it would have been obvious to harden Sakamoto's "adhesive material 34," thereby satisfying claim 18. As shown below, Sakamoto's "adhesive material 34" is between the interlayer resin insulating layer 50 ("first insulator layer") and IC chip 20 ("component"). APPLE-1005, [0106], FIG. 6.



Annotated Sakamoto FIG. 6

186. Tuominen defines that "[t]he term **adhesive** refers to a material, by means of which the components are attached to the insulator layer 10. [] Another property of the adhesive is that after spreading **the adhesive hardens or can be hardened at least partly, in such a way that the adhesive can hold the component in place.**" APPLE-1014, 7:18-24. In view of this disclosure, it would

have been obvious to have the adhesive material 34 be “*hardened*,” in order to securely attach (or “hold”) the IC chip 20 to the substrate 30 as taught by Tuominen.

[20]: The circuit module of claim 19, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

187. See discussion for [18] at Ground 1E.

XIV. GROUNDS 2A, 2B: Claims 1-2, 4, 6-8, 10-12, and 15-20 are obvious over Lee or Lee in view of Sakamoto

188. Based on my analysis, claims 1-2, 4, 6-8, 10-12, 15, 17, and 19 are obvious over Lee, and claims 1-2, 4, 6-8, 10-12, and 15-20 are obvious over Lee or Lee in view of Sakamoto.

A. Combination of Lee and Sakamoto

189. In this section, Sakamoto is applied to corroborate the metals of several layers for which Lee does not explicitly disclose a composition. Lee lacks explicit disclosure that the terminals 136 are aluminum, that the second conductive layer 140 is nickel (for claims 7 and 11), or that the third conductive layer 142 is copper (for claims 8 and 10-11), although these compositions are implicitly disclosed or obvious for reasons I set forth below. Sakamoto provides explicit teaching and motivation for the use of aluminum, nickel, and copper, respectively, for those elements.

190. Sakamoto is applied in combination with Lee for several other teachings in the following section (Section XV).

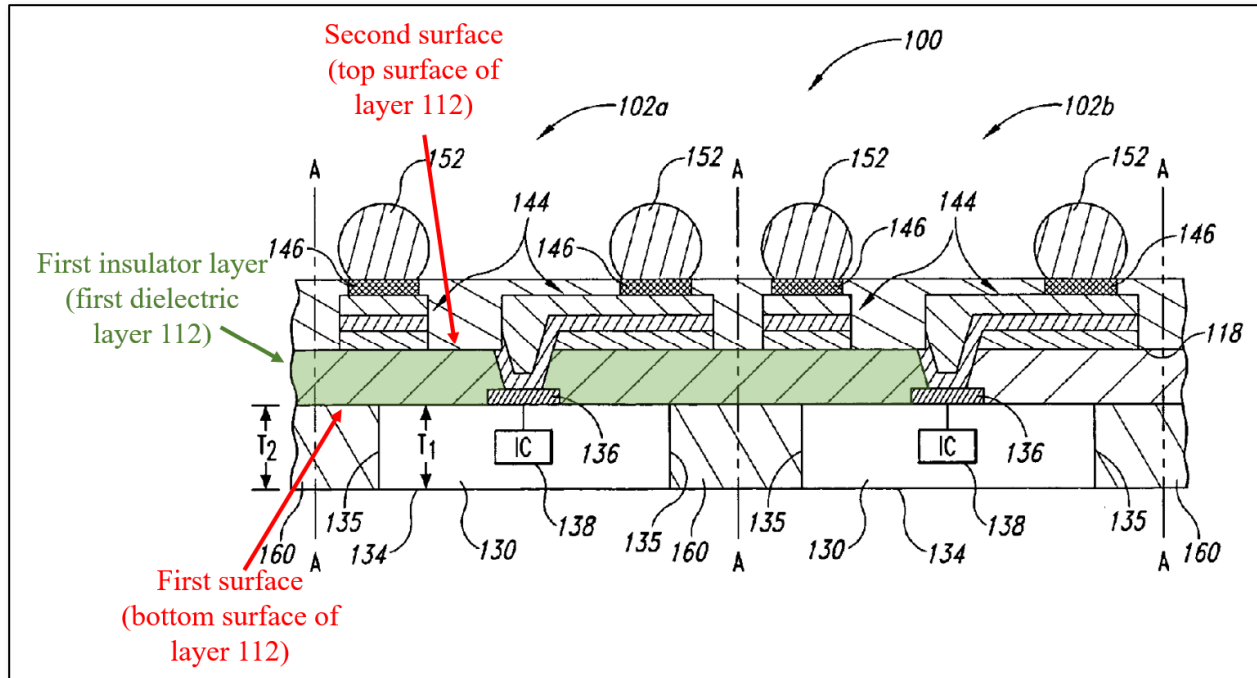
B. Analysis of claims

[1pre]: Circuit module, comprising

191. Lee's "microelectronic device assembly 100" is a "*circuit module*." APPLE-1015, [0033]. Like the "finished simple circuit module" of FIG. 8 of the '324 Patent, Lee's microelectronic device assembly 100 includes an IC chip (138) embedded in an insulating material (160) and connected to a series of conducting layers (e.g., 114, 140, 142, 146) that connect the IC chip to contact balls (152). APPLE-1001, 10:56, FIG. 8; APPLE-1005, FIG. 1E.

[1a]: a first insulator layer having a first surface and a second surface;

192. Lee's "first dielectric layer 112," which "can be a resin coated copper (RCC) or pre-preg material with woven fiber cloth embedded in a B-stage resin," is a "*first insulator layer*" and has first and second surfaces, as shown below. APPLE-1015, [0026]. A POSITA would have interpreted the term "dielectric" as referring specifically to an insulating material.



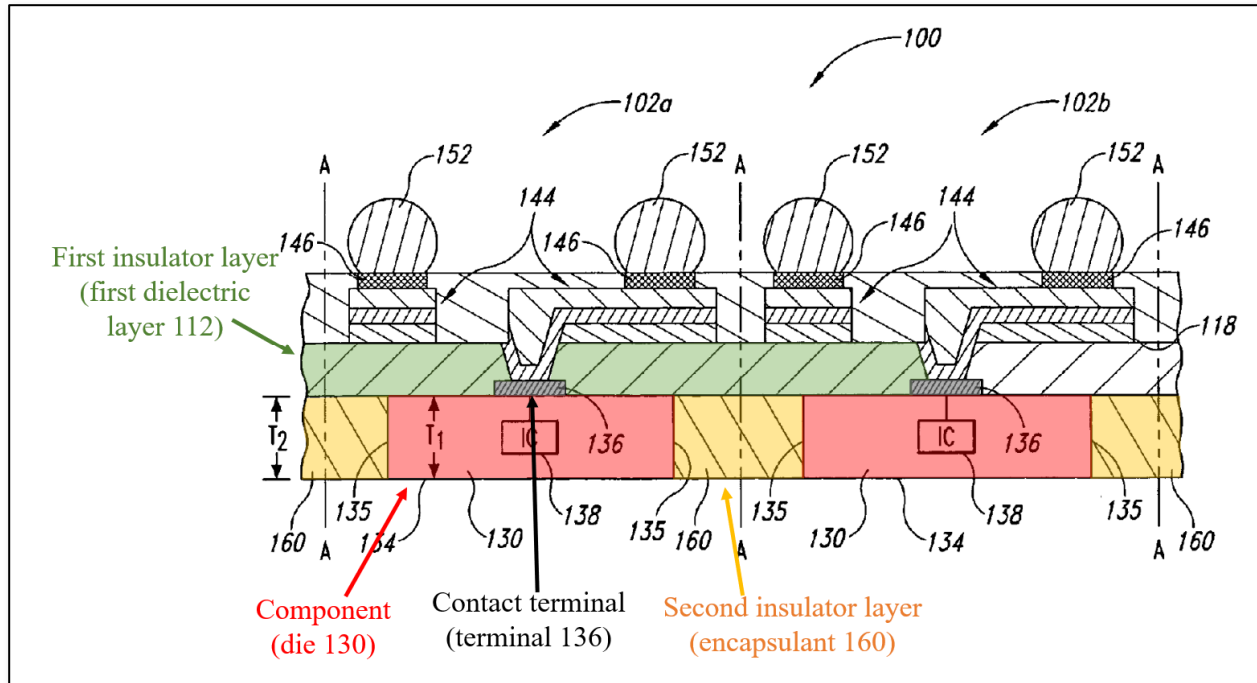
Annotated Lee FIG. 1E

[1b]: at least one second insulator layer on the first surface;

193. Lee’s “encapsulant 160,” which is on the bottom (“*first*”) surface of the first dielectric layer 112 (“*first insulator layer*”) is a “*second insulator layer*.” APPLE-1015, [0033], FIG. 1E. A POSITA would have recognized the encapsulant 160 as referring to an insulator layer based on standard terminology in the field. For example, the Wiley Dictionary of Engineering Materials defines “encapsulant” as “[a]n **insulating** material in the form of a conformal or thixotropic polymer coating, or a molten polymer or elastomer film or foam applied to an object, such as a small electronic component or device...”, and the Wiley Electrical and Electronics Engineering Dictionary defines “encapsulant” as “[f]or instance, a wax, a plastic, or a ceramic” (known insulators) and “encapsulate” as “to encase or



194. Lee's dies 130, which are inside the encapsulant 160 ("*second insulator layer*") and have terminals 136 that are "*contact terminals*," are "*at least one component*." APPLE-1015, [0029], [0033], FIG. 1E. A POSITA would have recognized that the terminals 136 are configured for making electrical contact with/to the dies 130.



Annotated Lee FIG. 1E

195. Lee does not explicitly disclose the material(s) of the terminals 136 (*contact terminals*). However, Lee’s disclosure that “zincation” can be performed on the terminals 136 amounts to an implicit disclosure that the terminals 136 are composed of **aluminum**. For circuit modules in the 2000s, aluminum was a standard material for use in contact terminals, and zincation was a standard process for use on aluminum contact terminals. In the absence of disclosure to the contrary, a POSITA would have generally assumed that, if a terminal were being processed by “zincation” to prepare the terminal for further layer deposition, the terminal would likely be an aluminum terminal. *See* my overview of zincation in Section VI.A.

196. It would have been obvious to use aluminum for the terminals 136, based on the disclosure of “zincation” and the knowledge that aluminum contacts were common in the field. Indeed, the ’324 Patent admits in its Technical Field and Background sections that “circuit modules comprise conductors on the surface of the insulator layer, through which a component can be connected to become part of a circuit outside the component. [] **The most common conductor material is aluminium.**” APPLE-1001, 1:9-10, 1:65-66. Accordingly, the use of aluminum for the terminals 136 (as the “*first metal*”) would have been nothing more than the selection of the most common material used for that purpose.

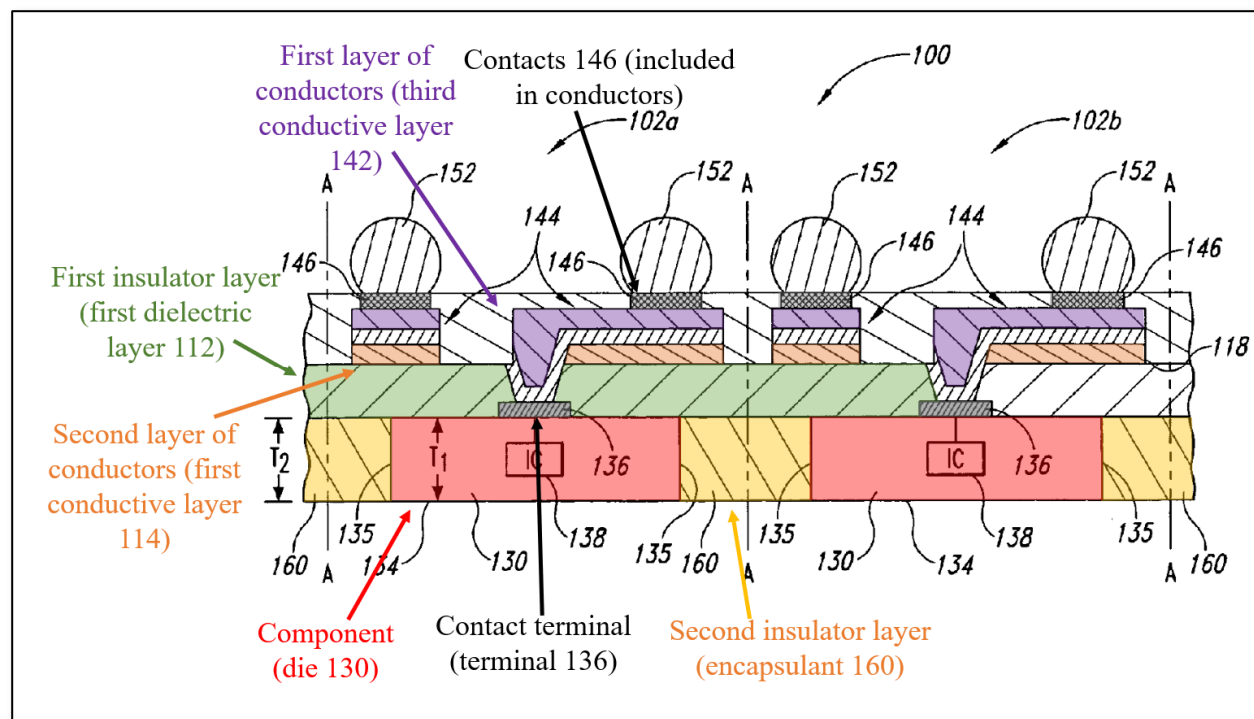
Ground 2B: Lee in view of Sakamoto renders obvious that the terminals 136 are composed of aluminum

197. The use of aluminum for the terminals 136 is also obvious in view of Sakamoto. Sakamoto notes that “the pad of the IC chip is normally formed out of **aluminum** or the like” and describes die pads 24 that are “made of **aluminum.**” APPLE-1005, [0051], [0101]. A POSITA, in selecting a metal for the terminals 136, would have found it obvious to try aluminum based on Sakamoto’s disclosure that aluminum is suitable (and, indeed, “normal”) for this purpose. APPLE-1005, [0051]. The use of aluminum would have been nothing more than the selection of the most common terminal material and one of a small number of typical materials for that purpose. A POSITA would have had a reasonable expectation of success in

using aluminum, given that Lee also describes the use of “zincation” on the terminals 136, a process known to provide favorable results when applied to aluminum contacts. APPLE-1015, [0029].

[1d]: conductors on the second surface of the first insulator layer, the conductors comprising at least a first layer and a second layer, in such a way that at least the second layer contains a second metal, and

198. Lee’s first conductive layer 114, third conductive layer 142, and contacts 146 are together “*conductors*,” of which the third conductive layer 142 and the first conductive layer 114 are examples of the “*first layer*” and the “*second layer*,” respectively. APPLE-1015, [0030]-[0033], FIG. 1E. The first conductive layer 114 is on the top surface (*second surface*) of the first dielectric layer 112 (*first insulator layer*). APPLE-1015, FIG. 1E. Note that the contacts 146 can equally be excluded from the “*conductors*” without departing from claim 1.



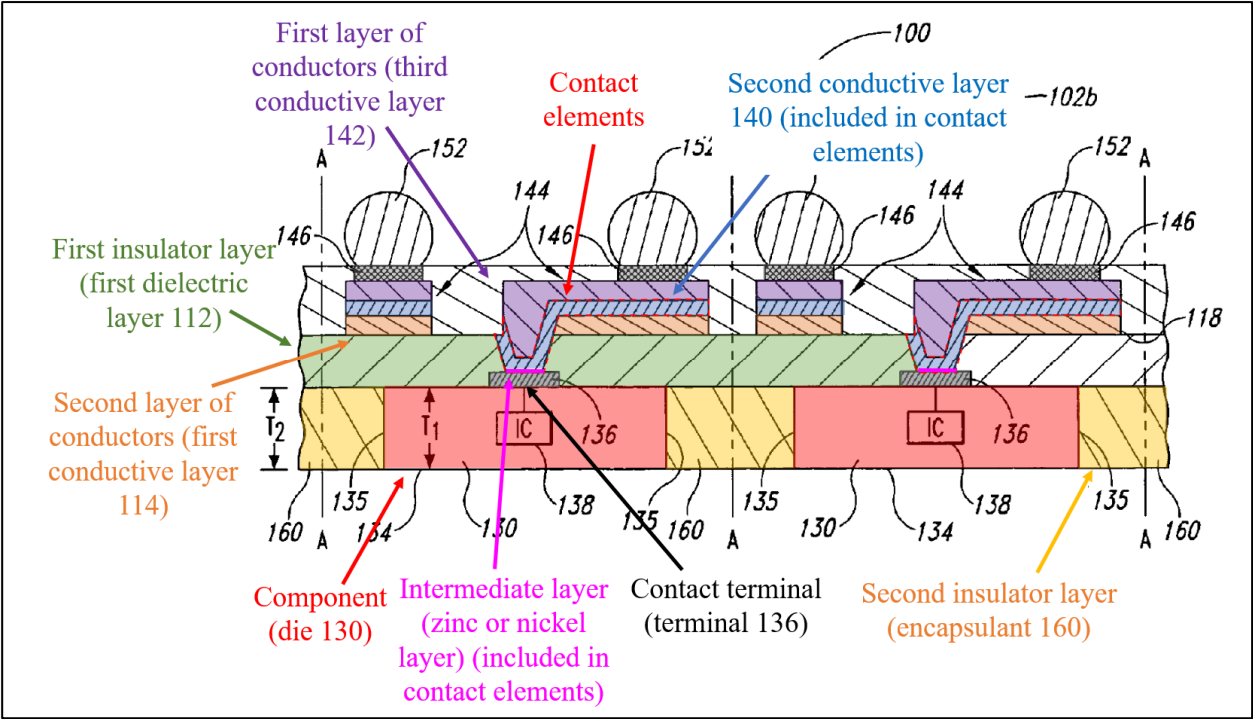
Annotated Lee FIG. 1E

199. The first conductive layer 114 (*second layer* of the *conductors*) can be a “copper foil,” such that the “*second metal*” is **copper**. APPLE-1015, [0026].

[1e]: contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal,

200. Lee's zinc or nickel layer and "second conductive layer 140" together are "*contact elements*" that are between the terminals 136 ("*contact terminals*") and the third conductive layer 142 ("*conductors*"). APPLE-1015, [0030], FIG. 1E. Of these layers, the zinc or nickel layer is an "*intermediate layer*" on the surface of

the contact terminals and containing a “third metal,” **zinc** or **nickel**. APPLE-1015, [0030], FIG. 6. See my discussion in Section VIII.F for details on Lee’s explicit disclosure of this zinc or nickel layer.



Annotated Lee FIG. 1E

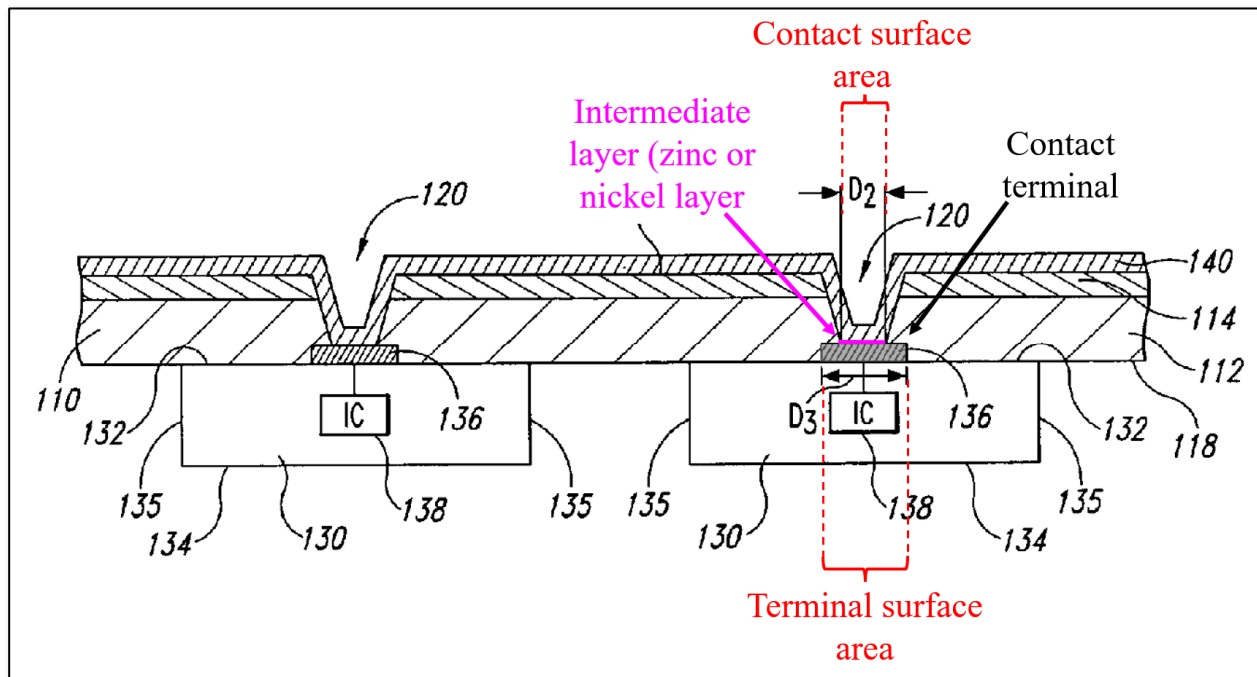
First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	• First conductive layer 114 (<i>second layer</i>), • Third conductive layer 142 (<i>first layer</i>), and • Contacts 146	Cu	• Zinc or nickel layer (<i>intermediate layer</i>), and • Second conductive layer 140	Zn or Ni

[1f]: a contact surface area (A_{CONT1}) between the intermediate layer and the

contact terminal being less than a surface area (A_{PAD}) of the contact terminal.

201. The contact surface area between Lee's zinc or nickel layer ("intermediate layer") and terminal 136 ("contact terminal") is less than a surface area of the terminal 136. Lee describes that "[t]he individual terminals 136 may have a dimension D_3 greater than the second dimension D_2 (FIG. 1A) of the holes 120 to facilitate proper alignment." APPLE-1015, [0029], FIG. 1B. The zinc or nickel layer is formed in the holes 120 "on the terminals 136," e.g., in the case of zincation, would exhibit self-aligned growth on exposed portion of the terminals 136, as discussed in Sections VI.A and XII.A. APPLE-1015, [0030]. That is, the contact surface area of the zinc layer is defined by the second dimension D_2 that corresponds to an exposed area of the terminals 136.

202. Accordingly, because the exposed terminal area corresponding to dimension D_2 is less than the total terminal area corresponding to dimension D_3 , a contact surface area between the zinc or nickel layer ("intermediate layer") and the terminal 136 ("contact terminals") is less than a surface area of the terminal 136, satisfying element [1f]. APPLE-1015, FIG. 1B. My comments in Section IX.A with respect to the relationship between width/diameter and area are equally applicable here, e.g., a relationship between the dimensions D_2 and D_3 would have been understood as indicating a relationship between corresponding areas (a contact surface area and a terminal surface area).



Annotated Lee FIG. 1B

[2]: The circuit module of claim 1, wherein the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.

203. Lee discloses that the “first metal” of the “contact terminals” (terminals 136) is **aluminum**, the “second metal” of the “second layer” (first conductive layer 114) is **copper**, and the “third metal” of the zinc or nickel layer is **zinc** or **nickel**. See discussion at [1c]-[1e]. Alternatively, as discussed for [1c], the identification of the first metal as aluminum is obvious over Lee and over Lee in view of Sakamoto.

[4]: The circuit module of claim 1, wherein the intermediate layer comprises

a layer containing zinc.

204. As discussed for [1e], Lee's **zinc** or nickel layer (e.g., formed by "zincation") is applied as the "*intermediate layer*." APPLE-1015, [0030].

[6]: *The circuit module of claim 1, wherein the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium.*

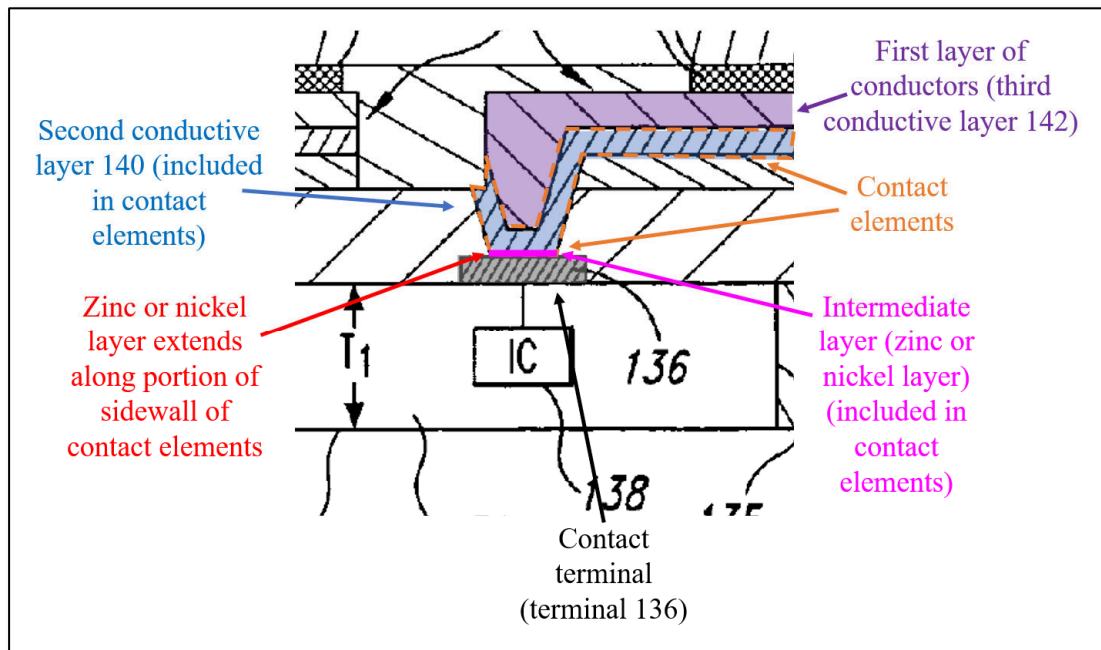
205. As discussed for [1e], Lee's zinc or **nickel** layer (e.g., "a nickel layer") is applied as the "*intermediate layer*." APPLE-1015, [0030].

[7]: *The circuit module of claim 1, wherein the intermediate layer extends along the side walls of the contact elements between the contact terminals and the conductors.*

206. As discussed at [1e], Lee's zinc or nickel layer and second conductive layer are applied as the "*contact elements*," and the zinc or nickel layer is applied as the "*intermediate layer*." APPLE-1015, [0030]. The zinc or nickel layer defines a portion of side walls of the *contact elements*, such that the zinc or nickel layer ("*intermediate layer*") "*extends along*" the side walls. In the case of a zinc layer formed by zincation, the extension along the side walls would be limited but finite, e.g., extension along the side walls to the zincation layer thickness of 0.3 μm disclosed by Ito. APPLE-1012, [0091]. In the case of a "sputter[ed]" nickel or zinc layer as disclosed by Lee, generally-conformal sputtering would be expected to

deposit a relatively uniform layer along much or all of the side walls. APPLE-1015, [0030].

207. As shown in annotated FIG. 1E below, the zinc or nickel layer is between the terminal 136 (“*contact terminal*”) and the third conductive layer 142 (“*first layer of the conductors*”). APPLE-1015, [0030]-[0031], FIG. 1E.



Annotated portion of Lee FIG. 1E

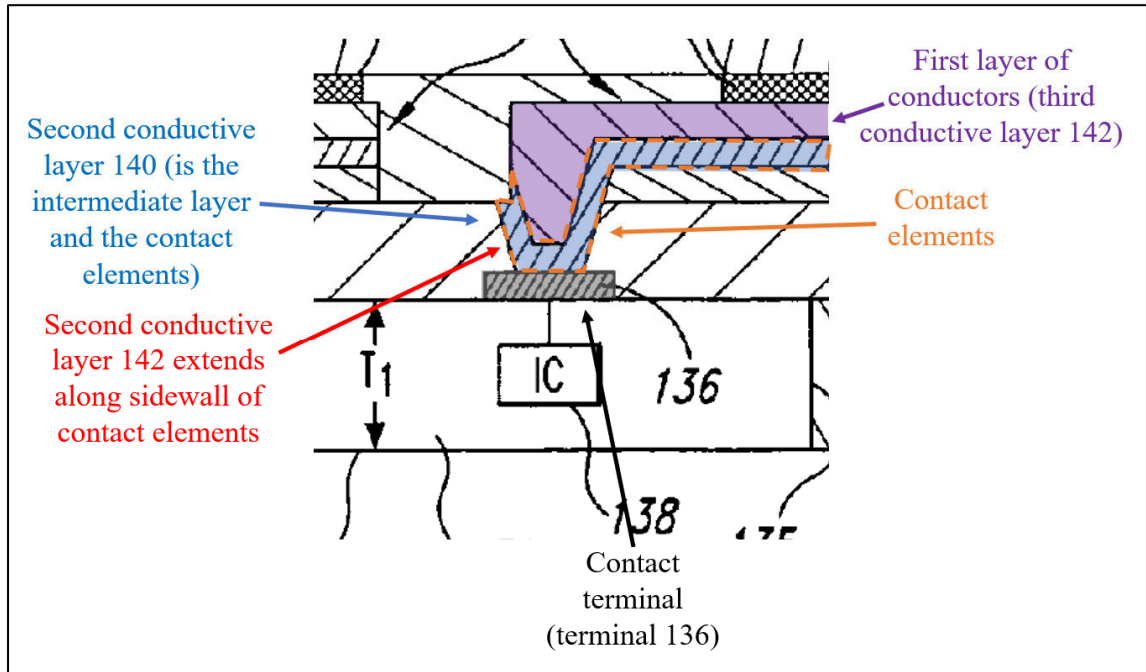
208. As an alternative teaching of claim 7, in the case where the zinc or nickel layer is omitted, the second conductive layer 140 can be applied as the “*intermediate layer*.” APPLE-1015, [0030]. For example, Lee describes that the zinc or nickel layer is included “[i]n **several embodiments**, in which the terminals 136 do not have a surface compatible with electroless plating [of the second conductive layer 140].” APPLE-1015, [0030]. Lee also discloses that the second

conductive layer 1140 “can be formed [] by electroless plating, **physical vapor deposition**, [or] **sputtering**.” APPLE-1015, [0030]. Accordingly, the zinc or nickel layer is not universally required but, rather, can be omitted, for example, in the case where the second conductive layer 140 is deposited by physical vapor deposition or sputtering. As compared to electroless plating, which is a chemical process, sputtering and physical vapor deposition are physical processes that are less sensitive to the composition of the underlying layer.

209. In that case, the second conductive layer 140 is on the surface of the terminal 136 (*contact terminal*) as the “*intermediate layer*,” and also forms the *contact elements*.” This alternative mapping is summarized in the table below. As discussed below in reference to [11], although Lee lacks explicit disclosure of the “*third metal*” of the second conductive layer 140, it would have been obvious to use nickel for this layer, e.g., in view of Lee’s disclosure that it can be formed by “electroless plating,” and/or in view of Sakamoto. APPLE-1015, [0030]. Therefore, the “*third metal*” can be **nickel**.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	• First conductive layer 114 (<i>second layer</i>), • Third conductive layer 142 (<i>first layer</i>), and • Contacts 146	Cu	• Second conductive layer 140 (<i>intermediate layer</i>)	Ni

210. As shown below, the second conductive layer 140, applied as the “*intermediate layer*” and the “*contact elements*” extends along (and defines) side walls of the “*contact elements*,” satisfying claim 7. APPLE-1015, FIG. 1E. Further, the second conductive layer 140 is between the terminal 136 (“*contact terminal*”) and the third conductive layer 142 (“*first layer*” of the “*conductors*”). APPLE-1015, [0030]-[0031], FIG. 1E. Therefore, this alternative mapping also satisfies claim 7.



Annotated portion of Lee FIG. 1E

[8]: The circuit module of claim 1, wherein each contact element comprises a copper core, which connects continuously to the material of the second layer of the conductors.

211. Lee's third conductive layer 142 includes a "copper core" that connects continuously to the material of the "second layer of the conductors" (third conductive layer 142 above the core). For claim 1, the first conductive layer 114, contacts 146, and the entirety of the third conductive layer 142 were together applied as the "conductors." However, it is equally valid to apply the first conductive layer 114, the contacts 146, and the third conductive layer 142 above the core, as the "conductors," of which the first conductive layer 114 is applied as the "first layer" and the third conductive layer 142 above the core is applied as the

“*second layer.*” For reasons discussed for [8] in Section IX.A, this interpretation is entirely consistent with Sakamoto’s labeling and discussion of similar elements, e.g., the copper core 29 and the second layer 32.

212. It would have been obvious to have the third conductive layer 142 be composed of **copper**, in view of Lee’s description that the layer is formed by “electroplating.” APPLE-1015, [0031]. Copper was widely known as the most common material for “electroplating” of a conductive layer in this field. APPLE-1015, [0031]. *See, e.g.*, the ’324 Patent’s Background disclosure of “electroplating” of copper in Noyori (APPLE-1001, 2:33-42; APPLE-1016, 4:15-35); Sakamoto’s descriptions of copper electroplating (APPLE-1005, [0023], [0123]); Ito’s disclosure of “electrolytic plating” of copper (APPLE-1012, [0020]); and Chang’s description that “[e]lectroplating [of copper] has the advantages of low processing temperature, low cost, high throughput, and good film quality, and thus becomes more attractive” (APPLE-1008, 1). Absent an indication otherwise, a POSITA would have understood a bare reference to “electroplating” to likely refer to, or at least to obviously cover, a copper layer. For example, it was widely known that copper was among a small number of materials that were commonly electroplated to form layers in circuit devices, such that it would have been obvious to try using copper as the third conductive layer 142.

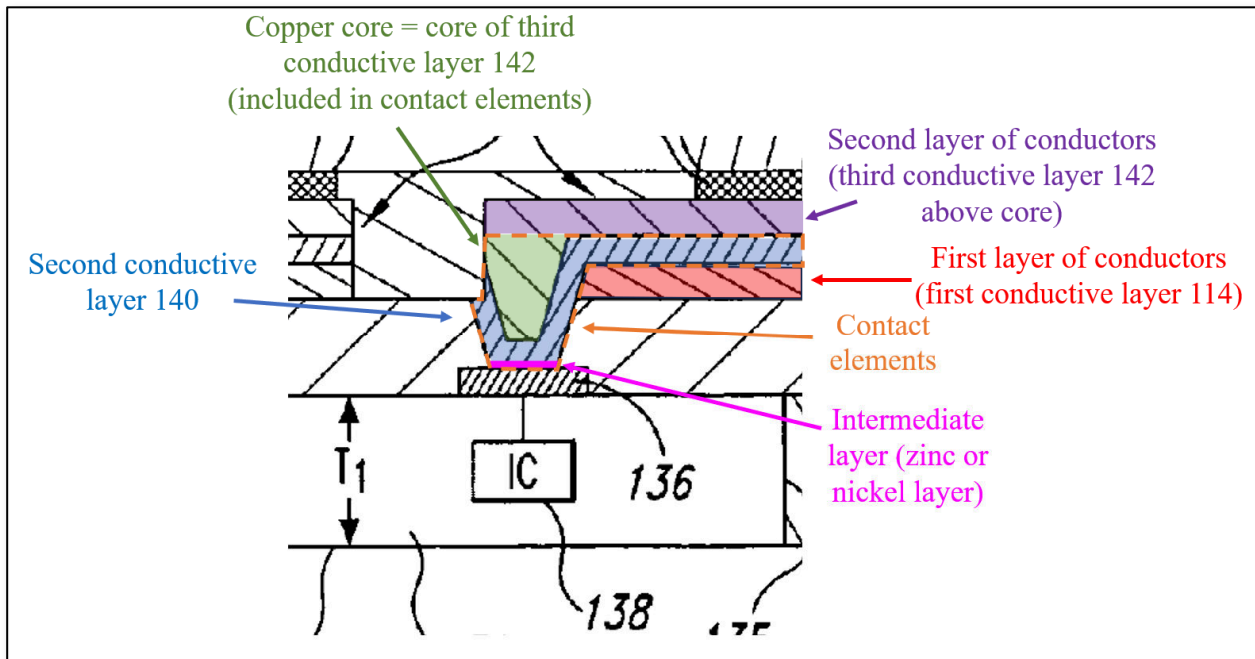
213. Therefore, in this mapping applied for claim 8, the “*second metal*” of the “*second layer of the conductors*” (the third conductive layer 142 above the core) is **copper**.

214. Further, for claim 1, the zinc or nickel layer and the second conductive layer 140 were together applied as the “*contact elements*.” However, it is equally valid to include each of the zinc or nickel layer, the second conductive layer 140, **and** the core of the third conductive layer 142 as the “*contact elements*.” For reasons discussed for [8] in Section IX.A, this interpretation is entirely consistent with Sakamoto’s labeling and discussion of similar elements, e.g., the copper core 29 and the second layer 32.

215. The core of the third conductive layer 142 is a “*copper core*” that “*connects continuously*” to the material of the third conductive layer 142 above the core, because these elements are formed in a common, continuous “electroplating” process that, as discussed above, deposits **copper**. APPLE-1015, [0031]. For example, the continuous process of “electroplating material” to form the third conductive layer 142 would have resulted in a continuous connection between the single portion of material that forms the core of the third conductive layer 142 and the third conductive layer 142 above the core. APPLE-1015, [0031].

216. These alternative mappings are shown in the table and the annotated, enlarged portion of FIG. 1E below.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	- First conductive layer 114 (<i>first layer</i>), - Third conductive layer 142 above core (<i>second layer</i>), and - Contacts 146	Cu	- Zinc or nickel layer (<i>intermediate layer</i>), - Second conductive layer 140, and - Core of third conductive layer 142	Zn or Ni

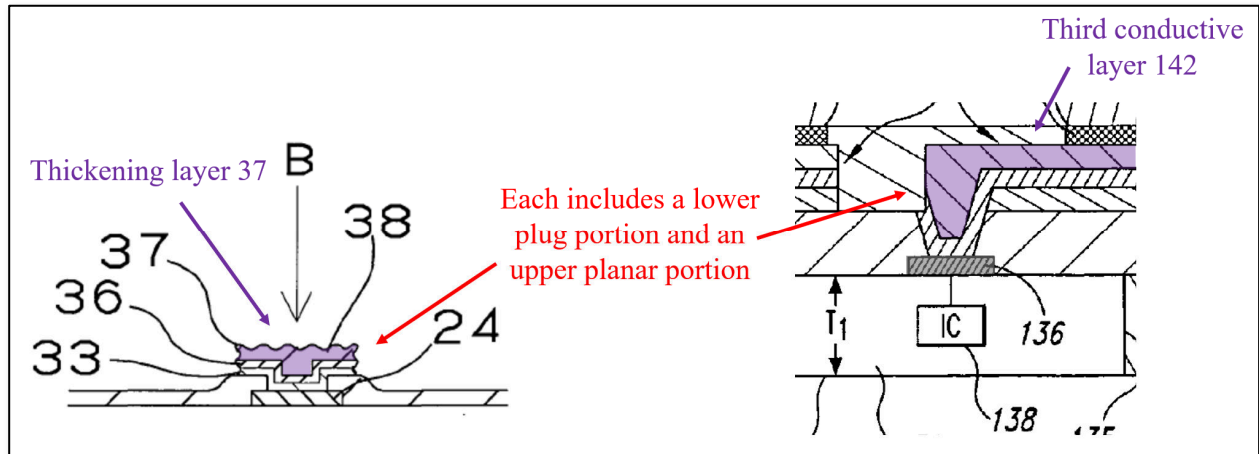


Annotated portion of Lee FIG. 1E

Ground 2B: Lee in view of Sakamoto renders obvious that the third conductive layer 142 is composed of copper

217. The use of copper for the third conductive layer 142 is also obvious in view of Sakamoto. In selecting a metal to use for the third conductive layer 142, it would have been obvious for a POSITA to look to Sakamoto's thickening layer 37,

which is similar in several ways to the third conductive layer 142. First, both layers are deposited by “electroplating.” APPLE-1005, [0114]; APPLE-1015, [0031]. Second, both layers are deposited onto an underlying conductive layer (the “second conductive layer 140” for Lee, and the “metal” “second thin film layer 36” for Sakamoto). APPLE-1005, [0111], [0114]; APPLE-1015, [0031]. Third, both layers have a similar morphology, including a plug portion and an overlying planar portion, as shown below. APPLE-1005, FIG. 6(A); APPLE-1015, FIG. 1E. Given the common deposition method, underlying substrate, and layer morphology, it would have been obvious for a POSITA to try using copper for the third conductive layer 142.



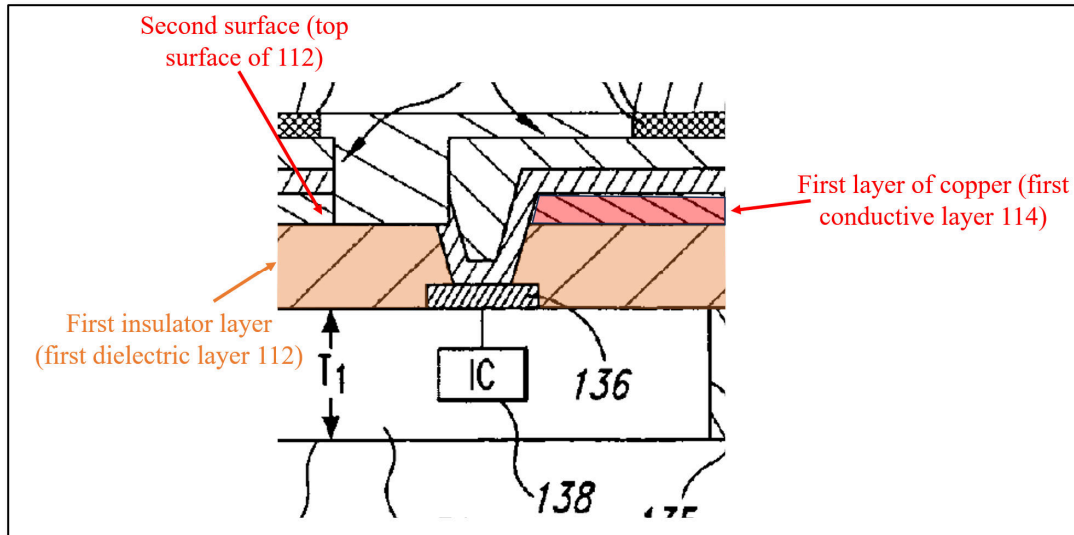
Left: Sakamoto FIG. 6(A); Right: portion of Lee FIG. 1E (annotated)

218. Moreover, a POSITA would have had a reasonable expectation of success in using copper for the third conductive layer 142, as Sakamoto provides detailed electroplating solution composition and electroplating conditions that would have guided a POSITA in electroplating copper. APPLE-1005, [0114]-

[0115]. For example, a POSITA would have had a reasonable expectation of success by performing routine experimentation based on Sakamoto's solution of sulfuric acid, copper sulfate, and disclosed additive, and based on Sakamoto's specific current density, duration, and temperature of electroplating. *Id.* The reasonable expectation would have reinforced by the fact that, like Sakamoto's thickening layer 37, Lee's third conductive layer 142 is electroplated onto an underlying conductive layer, such that process compatibility would be expected.

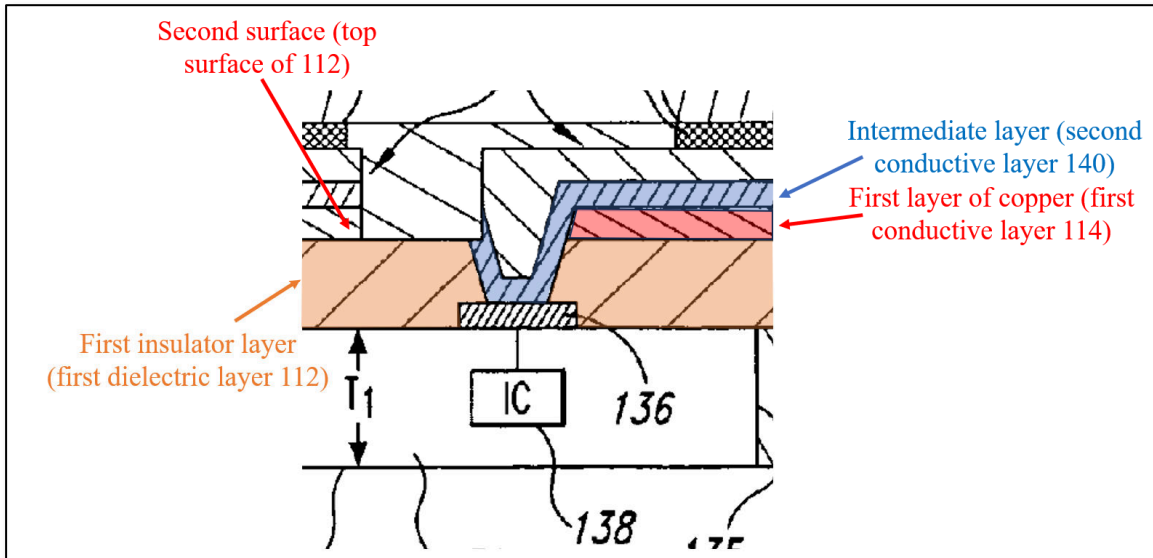
[10]: The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.

219. Lee's conductive layers 114, 140, 142 are respectively a "*first layer of copper*," "*intermediate layer*," and "*second layer of copper*" satisfying claim 10. First, as discussed for claim 1, the "*conductors*" include Lee's first conductive layer 114, which is "**copper** foil." APPLE-1015, [0026]. Further, the first conductive layer 114 is on the "*second surface*" (top surface) of the "*first insulator layer*" (first dielectric layer 112). APPLE-1015, [0026], FIG. 1E. Therefore, the first conductive layer 114 is a "*first layer of copper*" on the second surface of the first insulator layer.



Annotated portion of Lee FIG. 1E

220. For claim 1, Lee's second conductive layer 140 was applied as part of the "*contact elements*." However, it is equally valid to include the second conductive layer 140 in the "*conductors*." As shown in FIG. 1E, the second conductive layer 140 is an "*intermediate layer*" on the surface of the "*first copper layer*" (first conductive layer 114), as recited in claim 10. Note that, in the case of this mapping, the "*intermediate layer*" of claim 1 (for purposes of my discussion, treated as distinct from "*an intermediate layer*" of claim 10) is still met by Lee's zinc or nickel layer.

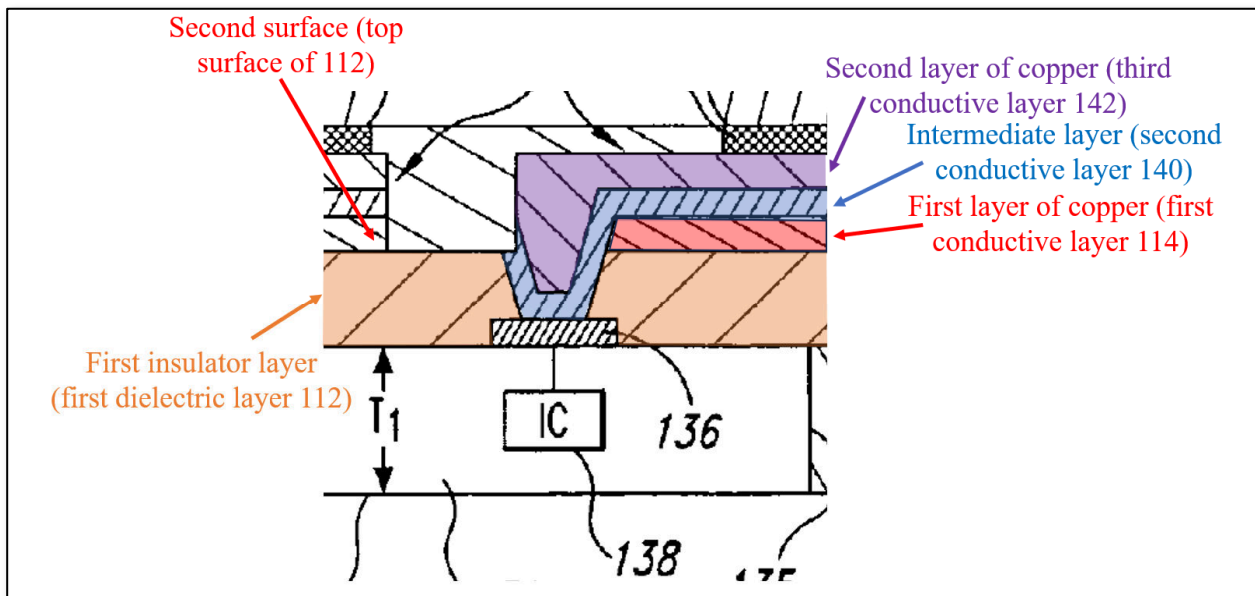


Annotated portion of Lee FIG. 1E

221. Lee's third conductive layer 142 is on the surface of the "*intermediate layer*" (second conductive layer 140). APPLE-1015, FIG. 1E. As discussed for [8] above, it would have been obvious to make the third conductive layer 142 a copper layer based on general knowledge in the art and/or in view of Sakamoto. APPLE-1015, [0031]. As such, the third conductive layer 142 is a "*second layer of copper*" on the surface of the "*intermediate layer*" (second conductive layer 140) as recited in claim 10.

222. These mappings are summarized in the table and drawing below.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	- First conductive layer 114 (<i>first layer of copper; “first layer” of claim 1</i>), - Second conductive layer 140 (<i>intermediate layer</i>), - Third conductive layer 142 (<i>second layer of copper; “second layer” of claim 1</i>), and - Contacts 146	Cu	Zinc or nickel layer (<i>“intermediate layer” of claim 1</i>)	Zn or Ni



Annotated portion of Lee FIG. 1E

[11]: The circuit module of claim 10, wherein the intermediate layer between the first and second coppers [sic] layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.

223. As discussed for [10], the “intermediate layer” is Lee’s second conductive layer 140, which “can be formed on the substrate 110 by electroless

plating, physical vapor deposition, sputtering, or other suitable processes.”

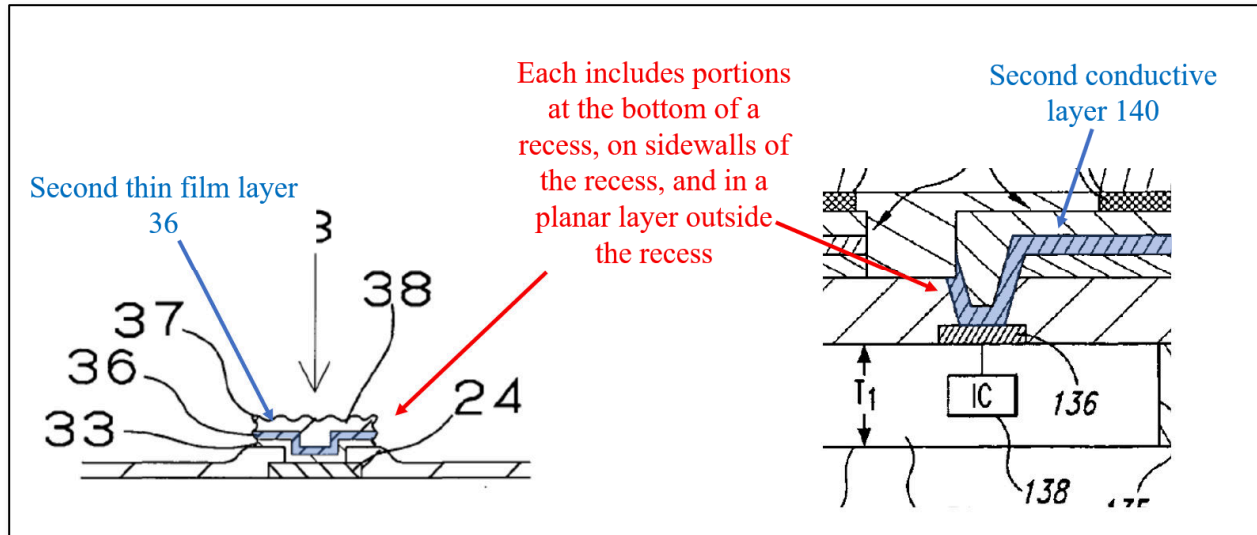
APPLE-1015, [0030]. It would have been obvious to have the *intermediate layer* be nickel grown by electroless plating, as the most-common conductive material, or among the most common materials, to electrolessly plate on zincated aluminum terminals.

224. Electroless nickel plating would have been understood by a POSITA as among the most obvious electroless plating processes to perform on a zincation-grown zinc layer, as the second conductive layer 140. *See* discussion at Section VI.A, which establishes that zincation of aluminum pads is a common preliminary step to electroless nickel plating. *See also, e.g.*, APPLE-1009 at 1 (“the electroless nickel (EN) metallization and bumping process is relatively low cost and straightforward... Zincating of the aluminum pads is a widely used process step that activates the pads for subsequent EN deposition”), APPLE-1010 at 2 (“Zincation is currently one of the most suitable processes to activate the aluminum surface for electroless technique []. Once this process is performed, aluminum coated with zinc then can be electroless plated by nickel”), APPLE-1011 at 1 (“Zincate treatment of aluminum pads is an essential step to make aluminum pads actives [sic] for subsequent electroless nickel plating”), APPLE-1027 at 21-22 (“the nickel surface layer is electrolessly deposited on the zincated aluminum base”).

225. Accordingly, the electroless nickel second conductive layer 140 obviously includes “*nickel grown by a chemical growing method*” and satisfies claim 11.

Ground 2B: Lee in view of Sakamoto renders obvious that the second conductive layer 140 is electroless copper or electroless nickel

226. The use of electroless copper or electroless nickel for the second conductive layer 140 is also obvious in view of Sakamoto. In selecting a metal to use for the second conductive layer 140, it would have been obvious to look to Sakamoto’s second thin film layer 36, which is similar to the second conductive layer 140. First, both layers can be deposited by “electroless plating.” APPLE-1005, [0021]; APPLE-1015, [0030]. Second, both layers are deposited on an underlying metal layer that can be zinc or nickel (the zinc or nickel layer for Lee, and the first thin film layer 33 for Sakamoto). APPLE-1005, [0109]; APPLE-1015, [0030]. Third, both layers have similarly morphology, being deposited in a recess, on sidewalls of the recess, and in a planar layer outside the recess, as shown below. APPLE-1005, FIG. 7(A); APPLE-1015, FIG. 1E. Given the common deposition method, underlying substrate, and layer morphology, and based on Sakamoto’s disclosure that the second thin film layer 36 can be electroless copper or electroless nickel, it would have been obvious for a POSITA to try using electroless copper or electroless nickel for the second conductive layer 140. APPLE-1005, [0111].



Left: Sakamoto FIG. 6(A); Right: portion of Lee FIG. 1E (annotated)

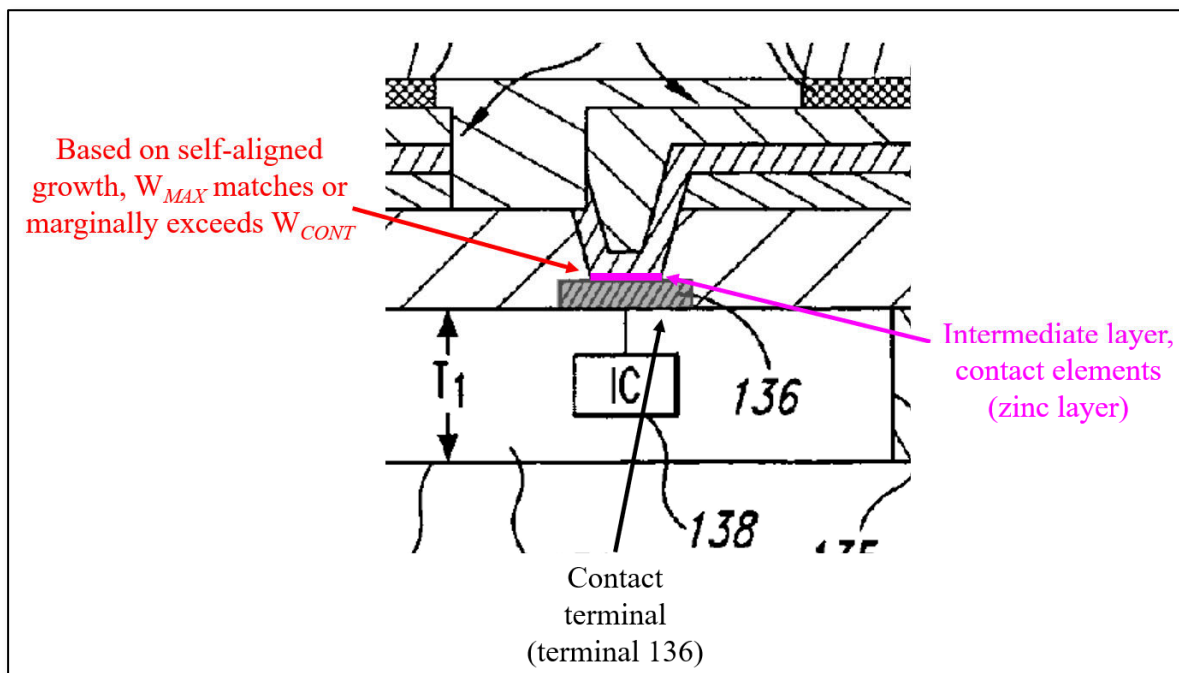
227. Moreover, a POSITA would have had a reasonable expectation of success in using electroless copper or electroless nickel to deposit the second conductive layer 140 on a zinc layer formed by zincation, given that Lee also describes the use of “zincation,” a process known to prepare aluminum contacts for subsequent electroless plating. APPLE-1005, [0030].

[12]: The circuit module of claim 1, wherein a width (W_{CONT}) of the contact surface between the contact element and the contact terminal of the component is 0-20% less than a greatest width (W_{MAX}) of the contact element in the same direction.

228. For claim 1, the “contact elements” were mapped to Lee’s zinc or nickel layer and second conductive layer 140. However, it is equally valid to apply only the zinc or nickel layer as the “contact elements,” as shown in the chart and

figure below, where the zinc or nickel layer is specifically a zinc layer formed by zincation.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	- First conductive layer 114 (<i>second layer</i>), - Third conductive layer 142 (<i>first layer</i>), and - Contacts 146	Cu	Zinc layer (<i>intermediate layer</i>)	Zn



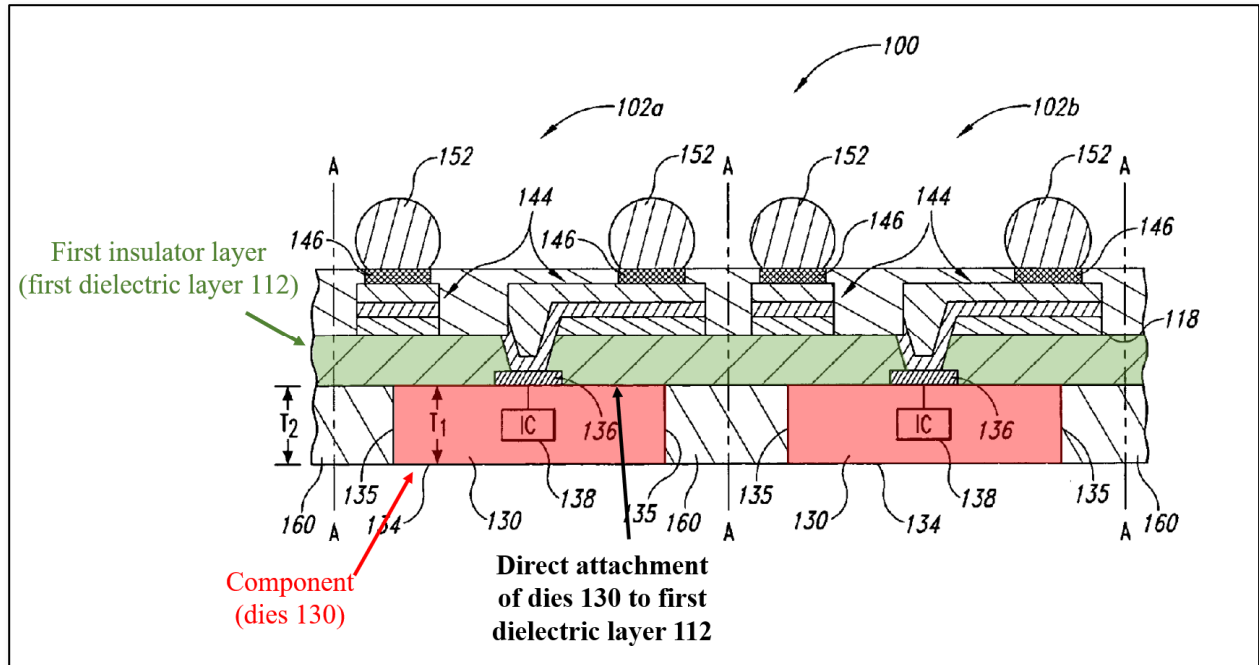
Annotated portion of Lee FIG. 1E

229. Based on this mapping, claim 12 requires that a width of the contact surface between Lee's zinc layer and Lee's terminal 136 is 0-20% less than a greatest width of the zinc layer in the same direction. As discussed for [12] at

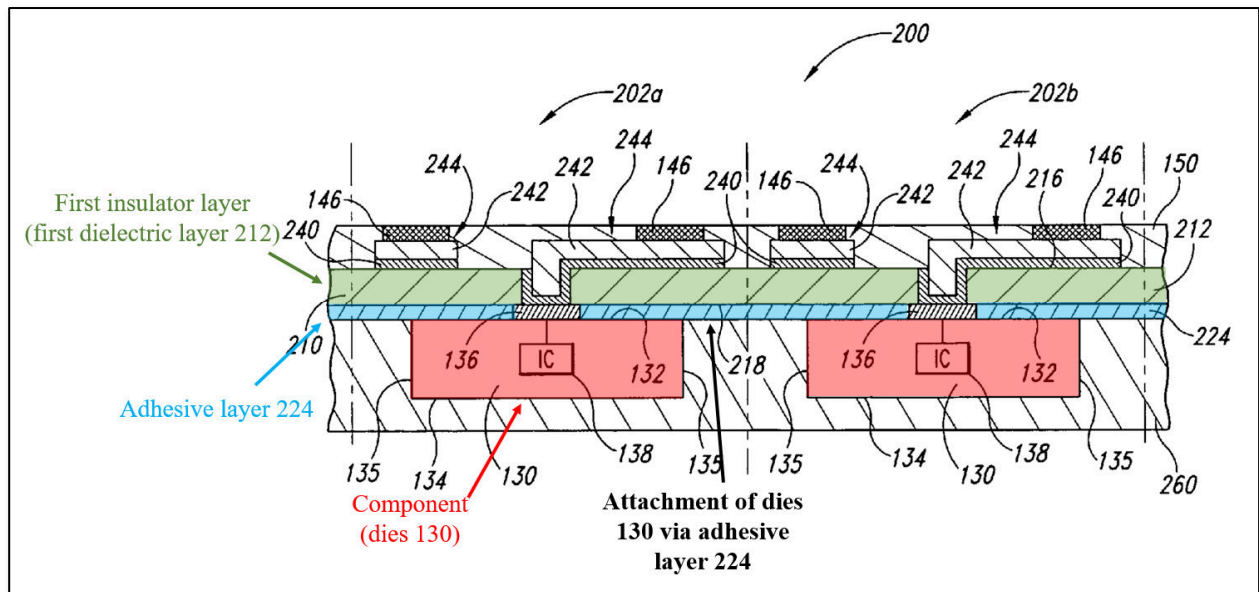
Ground 1D, for a zinc layer grown by “zincation” on the terminal 136 as disclosed by Lee, the zinc layer has a greatest width that matches the width of the contact surface, or at most exceeds the width of the contact surface very marginally due to a sloped sidewall of Lee’s holes 120. Therefore, this arrangement satisfies claim 12.

[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

230. Lee’s disclosure of an “adhesive layer” teaches the elements of claim 15. APPLE-1015, [037]. While the illustrated embodiment of FIG. 1E is “without an adhesive,” “in other embodiments, such as the embodiments [of] FIGS. 2A-3B, the microelectronic device assembly may include an adhesive for attaching the dies 130 to the substrate 110.” APPLE-1015, [0029]. As shown in the comparative figures below, the dies 130 in FIG. 1E are attached directly to the first dielectric layer 112 of the substrate 110, while the dies 130 in FIG. 2B are attached to a first dielectric layer 212 of a substrate 210 by an “adhesive layer 224.” APPLE-1015, [0029], [0037].



Annotated Lee FIG. 1E



Annotated Lee FIG. 2B

231. In an embodiment that “include[s] an adhesive [layer 224] for attaching the dies 130 to the substrate 110” as disclosed by Lee, the adhesive layer 224 would be a “polymer layer” between the “first insulator layer” (first dielectric

layer 112) and the “*at least one component*” (dies 130). APPLE-1015, [0029]. For example, Lee describes that the “adhesive layer 224 may be a pre-preg material,” which Lee, in the context of the first dielectric layer 112, describes as “woven fiber cloth embedded in a B-stage resin.” APPLE-1015, [0026], [0040]. A “B-stage resin” is a “*polymer*,” e.g., in that B-stage resins are partially polymerized. APPLE-1020, 133. Moreover, when the B-stage resin is fully cured (which would have been obvious, as discussed for [16] below), the resin would be a C-stage resin in a state of “‘full’ cure,” that is, essentially full polymerization. *Id.*

232. Further, “*contact holes*” for the “*contact elements*” (terminals 136) would be present in the adhesive layer 224, based on Lee’s description that “the adhesive layer 224 includes a plurality of second holes 220b aligned with corresponding first holes 220a in the substrate 210.” APPLE-1015, [0038]. Therefore, the adhesive layer 224 applied to the FIG. 1E embodiment of Lee satisfies claim 15.

233. To the extent Lee’s foregoing description is not interpreted as a **direct** disclosure of the use of the polymeric B-stage resin in the adhesive layer 224 as applied to the structure of FIG. 1E (e.g., because Lee may **explicitly** disclose only that the adhesive layer 224 “may be a pre-preg material”), it would have been obvious for a POSITA to use the B-stage resin as a known example of the “pre-preg material” of the adhesive layer 224, in view of Lee’s description that the first

dielectric layer 112 “can be [] pre-preg material with woven fiber cloth embedded in a B-stage resin.” APPLE-1015, [0026], [0040]. For example, in a case where the first dielectric layer 112 may not include an adhesive, the POSITA would have known that the pre-preg material, including the B-stage resin, would be a suitable adhesive to include in the adhesive layer 224.

[16]: The circuit module of claim 15, wherein the polymer layer comprises layer of a hardened adhesive.

234. It would have been obvious to cure the B-stage resin included in the adhesive layer 224 (“*polymer layer*”) discussed with respect to [15], so that the B-stage resin would become “fully cure[d]” and hardened. APPLE-1015, [0030]; Although Lee does not explicitly describe that the adhesive layer 224 becomes fully cured, Lee described curing **another** adhesive material, the “partially cured material in the first dielectric layer 112,” so that the material becomes “fully cure[d].” APPLE-1015, [0029]-[0030]. It would have been obvious to apply this same teaching to the B-stage resin of the adhesive layer 224: a POSITA would have recognized that “B-stage” refers to a state of partial curing, and, therefore, the application of “heat to fully cure” the B-stage resin of the adhesive layer 224 would have amounted to nothing more than the use of a known technique (“heat[ing] to fully cure”) to a material similar to the “partially cured material in the first dielectric layer 112.” APPLE-1015, [0029]-[0030]; APPLE-1020, 133. As

a result of the curing, the resin would become “hardened.” Indeed, the hardening of resin adhesives during curing is well known. *See* APPLE-1028.

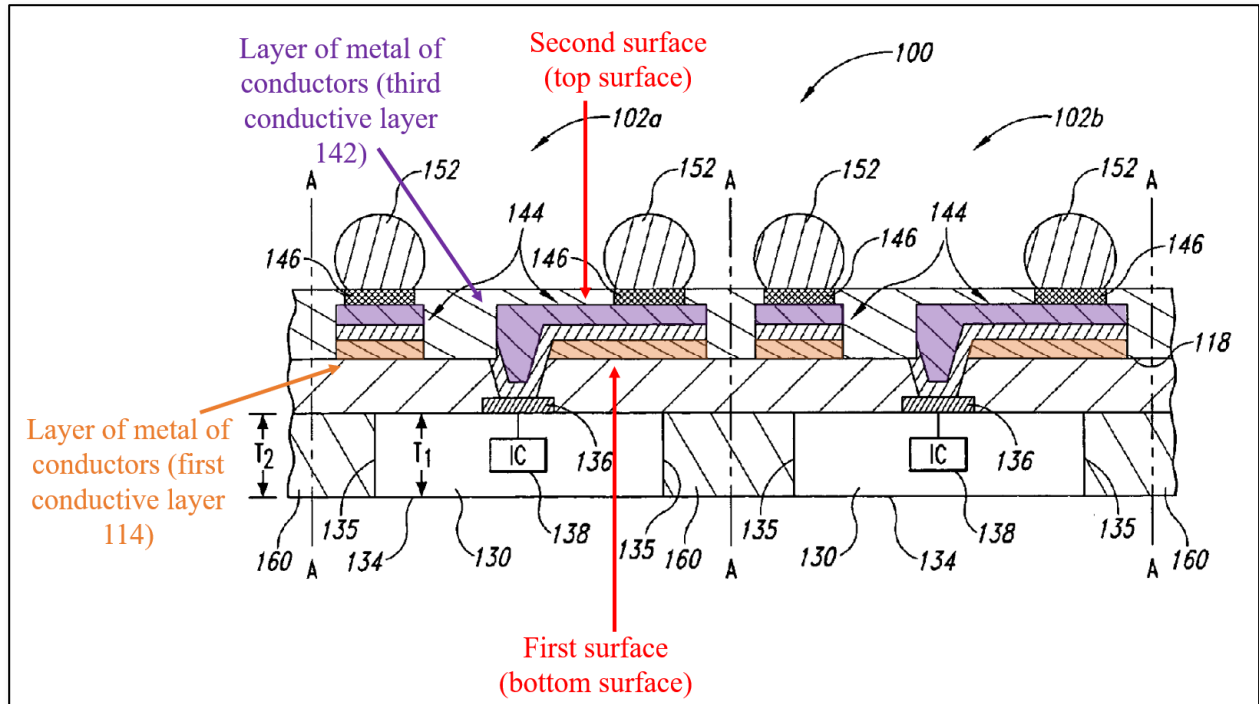
[17pre]: Circuit module, comprising:

235. *See* discussion at [1pre].

[17a]: a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;

236. *See* discussion at [1d]. Lee’s “first conductive layer 114” and “third conductive layer 142,” together applied as “*a conductor layer*” and “*conductors*,” are “*two layers of metal*” between first and second surfaces, as shown below.

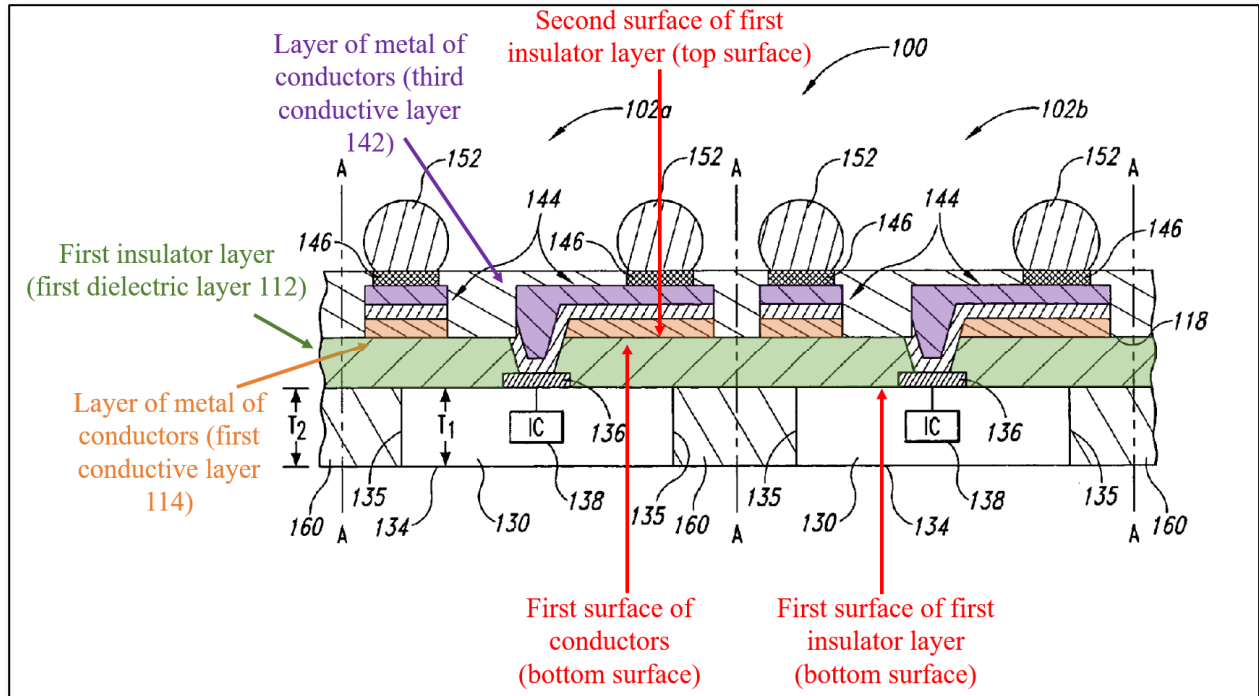
APPLE-1015, [0026]-[0031], FIG. 1E. For example, the first conductive layer 114 is copper foil (a metal), and the third conductive layer 142, being deposited by “electroplating,” is also a metal. APPLE-1015, [0026], [0031]. For example, *see* discussion at [8] for Ground 2A/2B above as to why the third conductive layer 142 is, or obviously is, copper, a metal. The contacts 146 can optionally be included in the *conductor layer*.



Annotated Lee FIG. 1E

[17b]: a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer covering the first surface of the conductors;

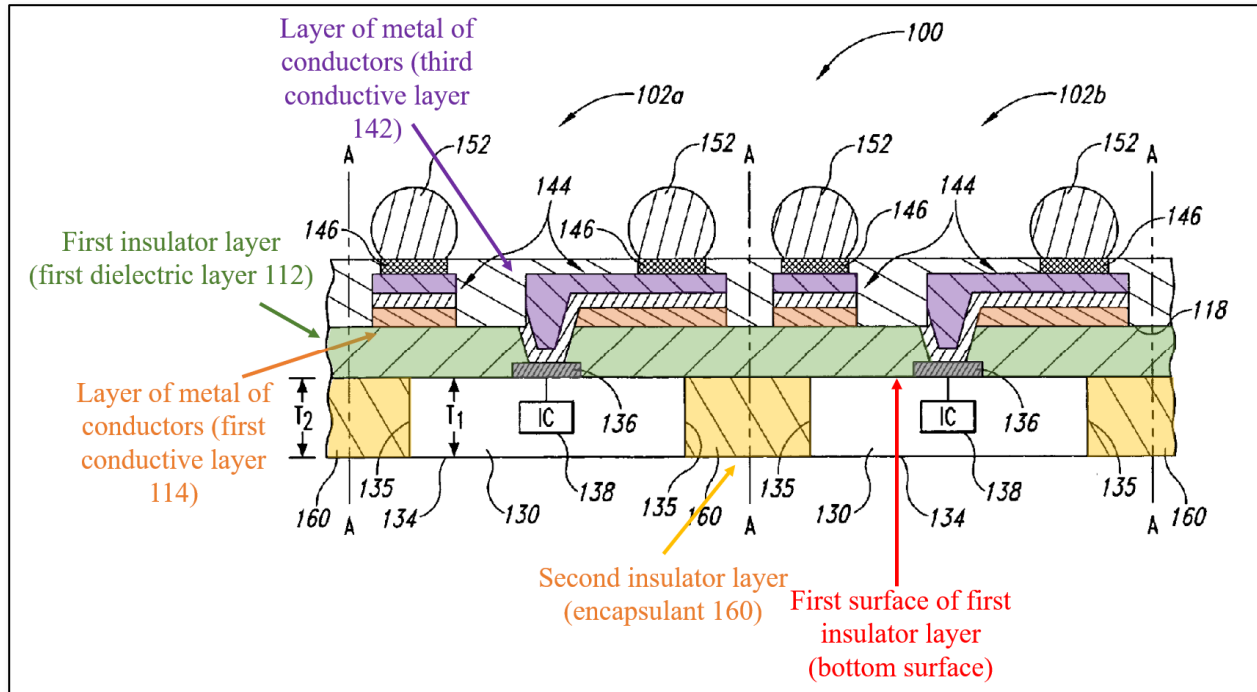
237. See discussion at [1a]. Lee's first dielectric layer 112 is a "first insulator layer" having a first (bottom) surface and a second (top) surface covering the first (bottom) surface of the conductors. APPLE-1015, [0026].



Annotated Lee FIG. 1E

[17c]: at least one second insulator layer on the first surface of the first insulator layer;

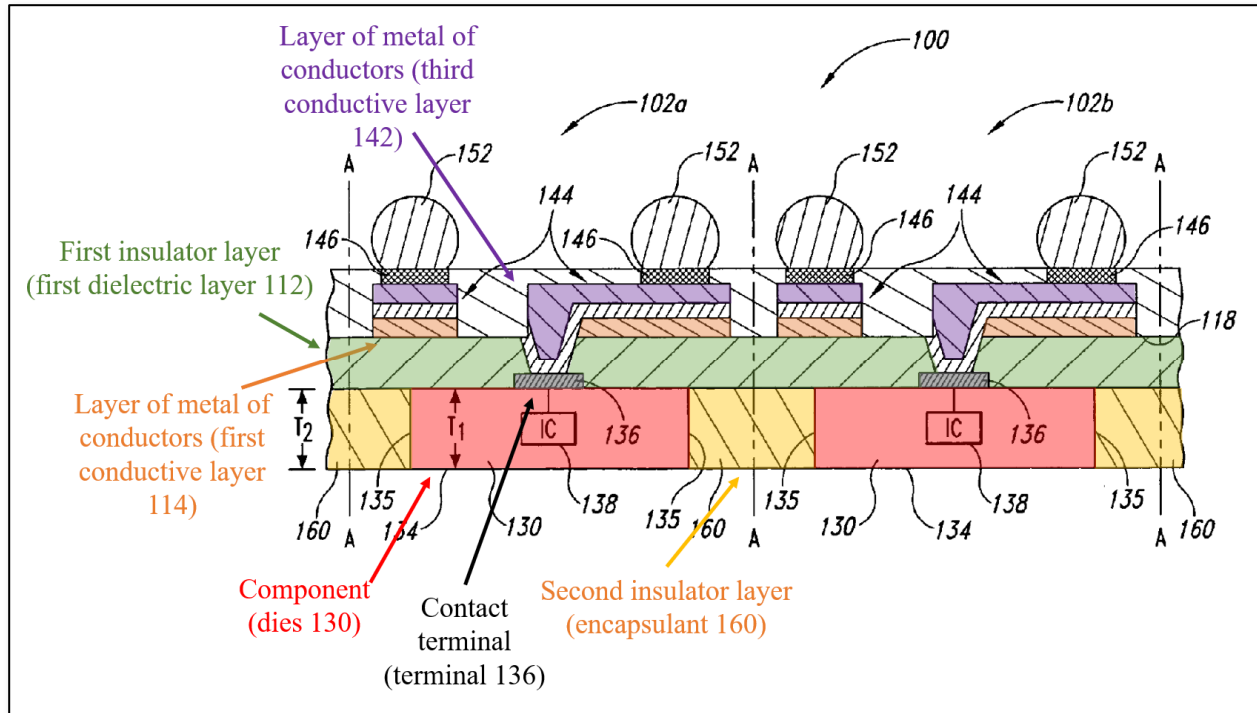
238. See discussion at [1b]. Lee's "encapsulant 160" is a "second insulator layer on the first surface of the first insulator layer." APPLE-1015, [0033].



Annotated Lee FIG. 1E

[17d]: at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal;

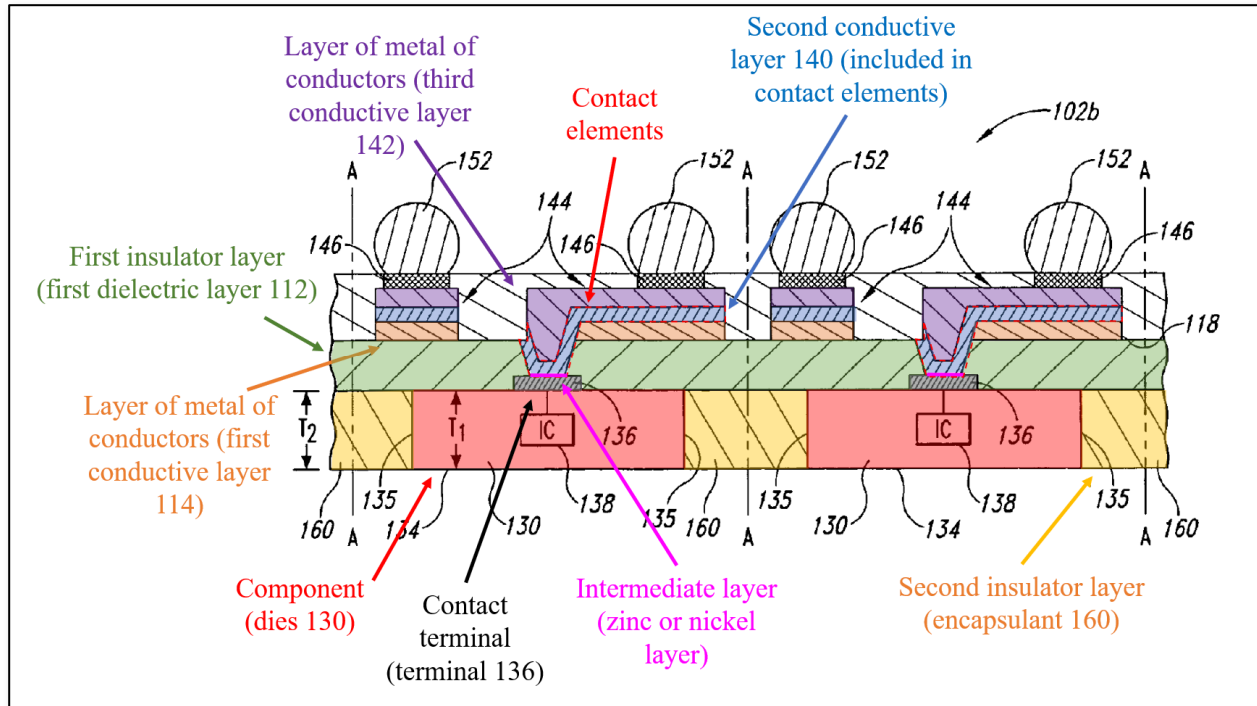
239. See discussion at [1c]. The “dies 130” are components that are inside the *second insulator layer* (encapsulant 160). APPLE-1015, [0029], [0033], FIG. 1E. The dies 130 comprise “terminals 136” which are “*contact terminals*.” APPLE-1005, [0101], FIG. 6. As discussed for [1c], the terminals 136 are, or obviously are, composed of aluminum and therefore contain “*at least one layer of metal*.” APPLE-1015, [0030].



Annotated Lee FIG. 1E

[17e]: contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,

240. See discussion at [1e]. Lee's zinc or nickel layer and second conductor layer 140 are between the "*contact terminals*" (terminals 136) and the *conductors* (e.g., third conductive layer 142) and constitute "*contact elements*." APPLE-1015, [0030], FIG. 3. The zinc or nickel layer is an "*intermediate layer*" that contains "*at least one layer of metal*," e.g., the zinc or nickel. APPLE-1015, [0030].



Annotated Lee FIG. 1E

[17f]: a contact surface area (A_{CONT1}) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal;

241. See discussion at [1f] for Ground 2A. A contact surface area between the zinc or nickel layer (“intermediate layer”) and the terminal 136 (“contact terminal”) is less than a surface area of the terminal 136. APPLE-1015, [0027], FIG. 1B.

[17g]: at least one layer of metal in the contact terminals containing a first metal; at least one layer of metal in the conductors containing a second metal; and the intermediate layer containing a third metal.

242. See discussion at [1c], [1d], and [1e]. Lee's terminals 136 (*"contact terminals"*) are, or obviously are, composed of **aluminum**, a *first metal*; the first conductive layer 114 of the *"conductors"* is composed of **copper**, a *second metal*; and the zinc or nickel layer is composed of **zinc or nickel**, a *third metal*. APPLE-1015, [0026], [0030].

[18]: The circuit module of claim 17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

243. Lee renders obvious a *"layer of hardened adhesive"* between the *"first insulator layer"* (first dielectric layer 112) and the *"at least one component"* (die 130). As discussed for [15], Lee discloses an *"adhesive layer 224"* between the *"first dielectric layer 112"* (*first insulator layer*) and the *"dies 130"* (*at least one component*). APPLE-1015, [0029], [0038], FIG. 2B. As discussed for [16], it would have been obvious to make this *"adhesive layer 224"* a *"hardened adhesive"* based on Lee's disclosure of *"fully cur[ing] the partially cured material in the dielectric layer 112"* APPLE-1015, [0030].

[19]: Circuit module, comprising
a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;
a first insulator layer having a first surface and a second surface, the second

surface of the first insulator layer entirely covering the first surface of the conductors;

at least one second insulator layer on the first surface of the first insulator layer;

at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal; and

contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,

a contact surface area ($A_{CONT\ 1}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal.

244. See discussion at claims 1 and 17. Claim 19 is identical to claim 17 except for (1) omitting recitation of the first, second, and third metals and (2) reciting “*the second surface of the first insulator layer entirely covering the first surface of the conductors.*” The latter element is satisfied by the top surface of Lee’s first dielectric layer 112 (*first insulator layer*) entirely covering the bottom horizontal surface of the first conductive layer 114, the bottom horizontal surface

1E.



245. *See* [18] above.

246. Based on my analysis, claims 5, 9, and 14 are obvious over Lee in
of Sakamoto.

A. Analysis of claims

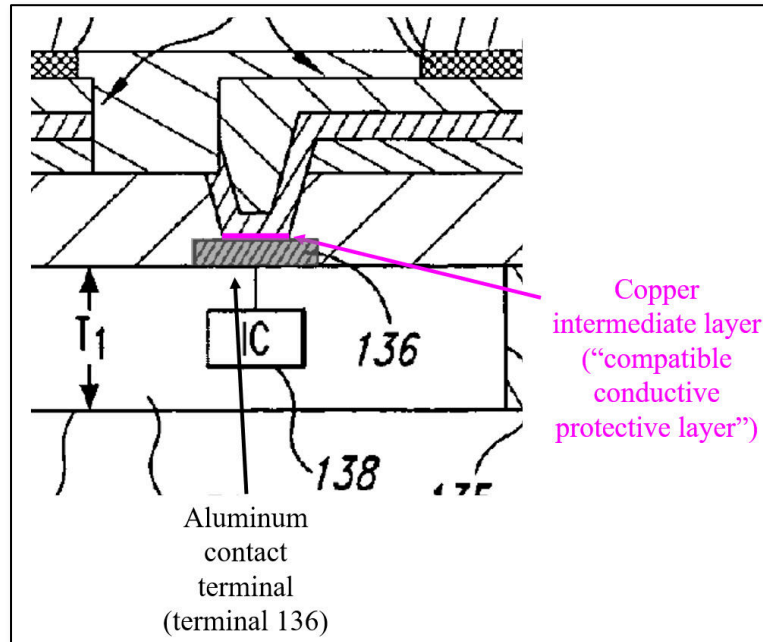
[5]: The circuit module of claim 1, wherein the intermediate layer comprises a layer containing copper.

247. It would have been obvious to use copper in Lee's "compatible conductive protective layer" ("*intermediate layer*"). In the mapping for Lee discussed for Ground 2A, examples were applied in which the "compatible conductive protective layer" is zinc or nickel. APPLE-1015, [0030]. However, Lee does not restrict this layer to zinc or nickel, and, in view of Sakamoto, it would have been obvious to use **copper** for this layer, satisfying claim 5. Specifically, in selecting a metal to use for the "compatible conductive protective layer," it would have been obvious for a POSITA to look to Sakamoto's first thin film layer 33, which can be composed of copper and is similar in several ways to the compatible conductive protective layer. APPLE-1005, [0109]. First, both layers can be deposited by "sputtering." APPLE-1005, [0109]; APPLE-1015, [0030]. Second, both layers are deposited on an underlying aluminum contact pad. APPLE-1005, [0110]; APPLE-1015, [0030]. Third, both layers are used as a substrate for subsequent electroless plating or sputtering of another metal layer (the second conductive layer 140 for Lee, or the second thin film layer 36 for Sakamoto). APPLE-1005, [0021]; APPLE-1015, [0030]. Given the common deposition methods and layer arrangements, it would have been obvious for a POSITA to try

using, for the compatible conductive protective layer, the metals disclosed by Sakamoto for the first thin film layer 33, including **copper**. Copper is one of only eight possible metals that Sakamoto discloses may be used. APPLE-1005, [0109].

248. A POSITA would have had a reasonable expectation of success in using copper, based at least on Sakamoto's guidance with respect to layer thickness ("preferably, 0.01 to 1.0 μm ") and provided details on the fabrication process. APPLE-1005, [0109], [0211]-[0212]. A POSITA could follow this recipe to successfully deposit a copper compatible conductive protective layer.

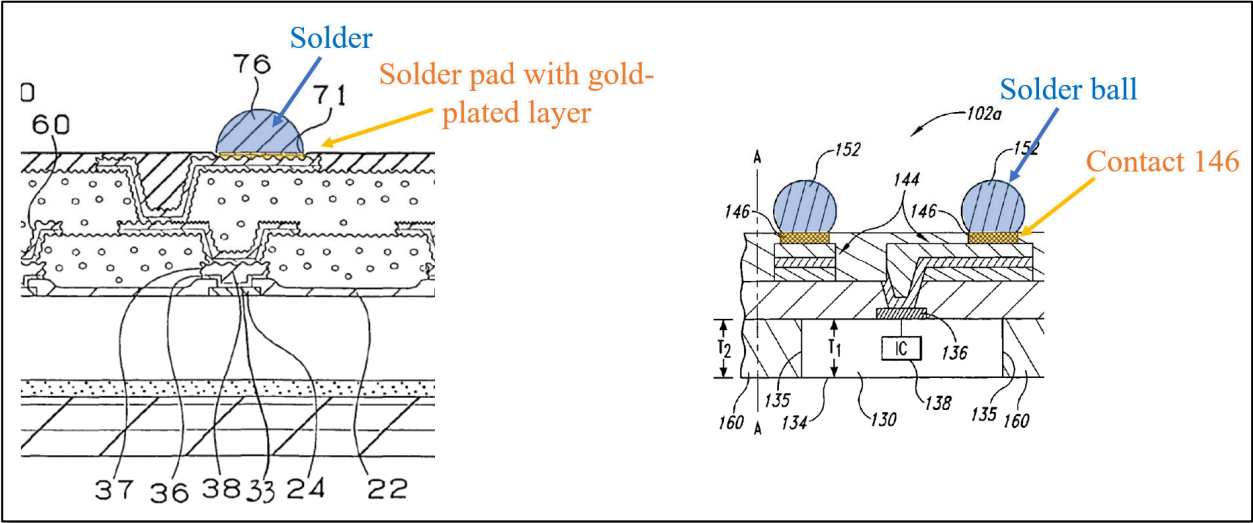
249. Accordingly, it would have been obvious for the "*third metal*" of the "*intermediate layer*" to be copper.



Annotated portion of Lee FIG. 1E

250. Moreover, although, for claim 1, the first conductive layer 114 was applied as the “*second layer*” of the “*conductors*” having the “*second metal*,” it is equally valid to apply the contacts 146 as the “*second layer*” of the “*conductors*.” Although Lee does not disclose a composition of the contacts 146, in view of Sakamoto, it would have been obvious to have the contacts 146 be “gold plated” as described for Sakamoto’s analogous “solder pads 75,” which, like the contacts 146, form an uppermost contact surface on which solder is applied. APPLE-1005, [0130], FIG. 6; APPLE-1015, [0034], FIG. 1E. The selection of gold would therefore have constituted only trying one of a finite number of obvious contact materials to use for a solder pad, and, further, applying a known technique (gold

solder pads) to Lee’s device, to obtain a predictable result. Accordingly, the “second metal” of the *conductors* can be **gold**.



Left: portion of Sakamoto FIG. 6; Right: portion of Lee FIG. 1E (annotated)

251. The mapping applied for claim 5 is summarized in the following table.

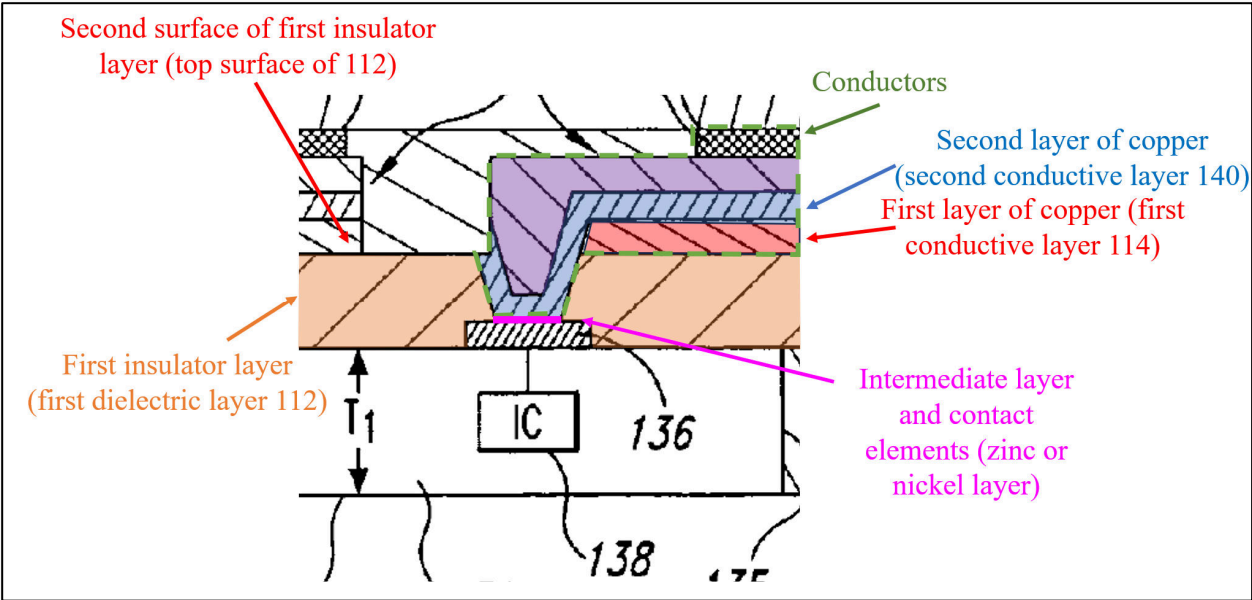
First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	• First conductive layer 114 (<i>first layer</i>), • Third conductive layer 142, and • Contacts 146 (<i>second layer</i>)	Au	• “Compatible conductive protective layer” (<i>intermediate layer</i>), and • Second conductive layer 140	Cu

[9]: The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, and a second layer of copper on the surface of the first copper layer.

252. Lee in view of Sakamoto renders obvious that the second conductive layer 140 is a layer of copper. *See* discussion at [11] for Ground 2A for why, in view of Sakamoto, it would have been obvious for the second conductive layer 140 to be a layer of electroless copper. Further, although, for claim 1, the second conductive layer 140 was applied as part of the “*contact elements*,” it is equally valid to apply the second conductive layer 140 as a “*second layer of copper*” of the “*conductors*.”

253. The “copper foil” “first conductive layer 114” is a “*first layer of copper on the second surface of the first insulator layer*.”

254. Therefore, Claim 9 is satisfied by the foregoing mappings summarized below.



Annotated portion of Lee FIG. 1E

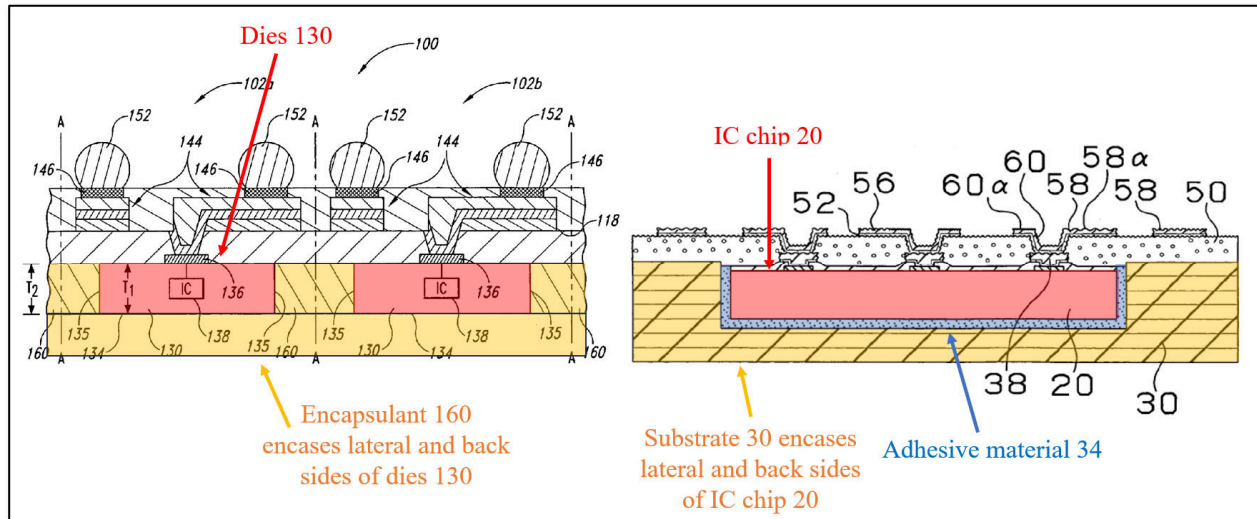
First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	• First conductive layer 114 (first layer of copper, first layer), • Second conductive layer 140 (second layer of copper, second layer), • Third conductive layer 142, and • Contacts 146	Cu	• Zinc or nickel layer (intermediate layer)	Zn or Ni

[14]: The circuit module of claim 1, wherein the at least one second insulator layer contains at least one layer of fibre material and an opening in the fibre material for the at least one component.

255. It would have been obvious to encapsulate Lee’s dies 130 in the substrate 30 of Sakamoto, such that the “second insulator” (substrate 30) would

contain at least one layer of fibre material and openings in the fibre material for the dies 130. As discussed for claim 1, Lee discloses that an encapsulant 160 “encases” the dies 130. APPLE-1015, [0033]. The encapsulant 160 can encase not only the lateral ends 135 of the dies 130 but also the “back sides 134 of the dies,” for example, by having “the second thickness T_2 of the encapsulant 160 [being] greater than the first thickness T_1 of the dies 130.” APPLE-1015, [0033].

256. Sakamoto’s “insulating resin substrate (or core substrate) 30” has a similar configuration, encasing lateral ends and a back side of the IC chip 20 in conjunction with an adhesive material 34, as shown below. APPLE-1005, [0106]-[0108], FIG. 6.



Left: Lee FIG. 1E; Right: Sakamoto FIG. 6 (annotated)

257. It would have been obvious, as a matter of design choice, to apply Sakamoto’s configuration to Lee’s device assembly, for example, by encasing Lee’s dies 130 in Sakamoto’s substrate 30 and adhesive material 34. The

encapsulant 160 and the substrate 30 serve the same function of encasement (or “contain[ment]”) and insulation. APPLE-1005, [0108]; APPLE-1015, [0033].

Further, the replacement of the encapsulant 160 by the substrate 30 and adhesive material 34 would have been well within the skill of a POSITA with a reasonable expectation of success, especially in view of Sakamoto’s explicit disclosure of the materials and manufacturing process associated with the substrate 30. APPLE-1005, [0106]-[0108]. For example, in conjunction with FIGS. 1(A)-1(C), Sakamoto provides a step-by-step process in which a recess 32 is formed in the substrate 30, the adhesive material 34 is applied in the recess 32, and the IC chip 20 is contained in the recess 32. APPLE-1005, [0106]-[0108]. Following this recipe, a POSITA could have successfully applied Sakamoto’s substrate 30 and adhesive material 34 to Lee.

258. As discussed for [14] at Ground 1A, the substrate 30 includes “glass cloths” “*contain[ing] at least one layer of fibre material.*” APPLE-1005, [0106].

Further, the substrate 30, replacing the encapsulant 160, would include “*an opening*” in the fibre material, at the top of the recess 32, for the “*at least one component*” (dies 130), matching the configuration in both Sakamoto’s and Lee’s structures. APPLE-1005, FIG. 6; APPLE-1015, FIG. 1E.

XVI. GROUND 2C: Claim 3 is obvious over Lee in view of Eichelberger (and optionally further in view of Sakamoto)

259. Based on my analysis, claim 3 is obvious over Lee in view of Eichelberger. To the extent Sakamoto is found necessary to render obvious the aluminum terminals 136 for claim 1, Sakamoto is included in this ground.

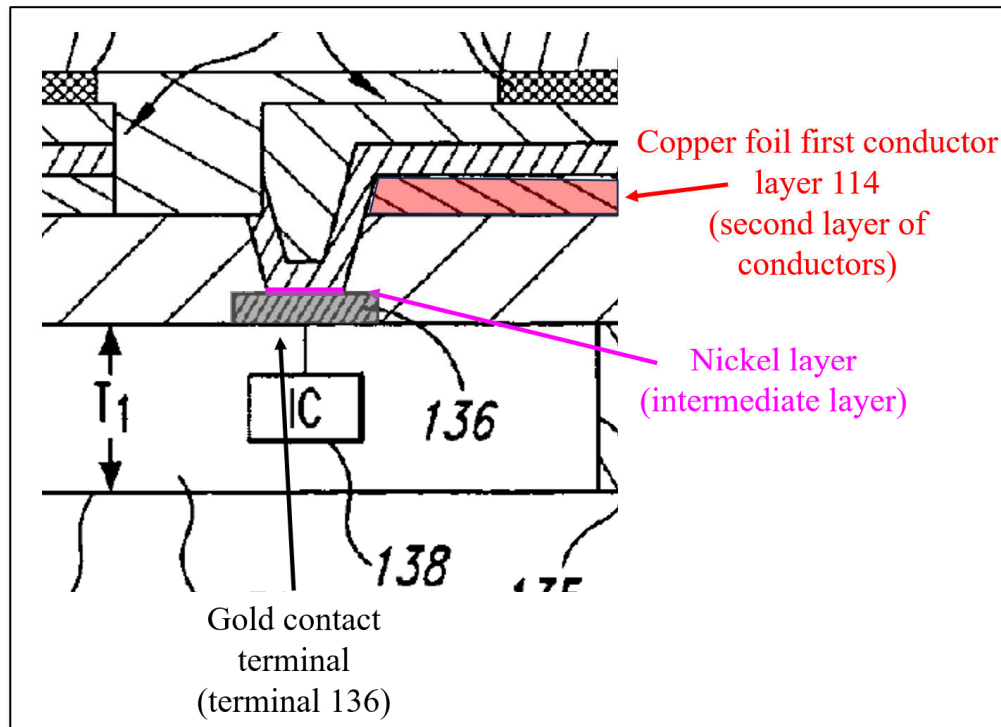
A. Analysis of claim 3

[3]: The circuit module of claim 1, wherein the first metal is gold, the second metal is copper, and the third metal is nickel.

260. It would have been obvious to use gold for Lee's terminals 136, as taught by Eichelberger, such that the terminals contain **gold** as the "*first metal*." Lee does not explicitly disclose a material for the terminals 136 (also referred to as "bond-pads"). APPLE-1015, [0029]. However, Eichelberger discloses the use of "gold" "bond pads." APPLE-1006, 9:38-58. In selecting a metal for the terminals 136, it would have been obvious for a POSITA to look to Eichelberger's bond pads and to try using the "gold" bond pads disclosed by Eichelberger, for reasons discussed for [3] of Ground 1B. Causing the terminal 136 to contain gold would simply be a selection of one of a finite number of identified, predictable materials for bond-pads, in addition to the aluminum, copper, and nickel also disclosed by Eichelberger. APPLE-1006, 9:38-58. A POSITA would also have been motivated by the advantages discussed for [3] for Ground 1B, e.g., compatibility with GaAs devices and anti-oxidation characteristics.

261. Moreover, a POSITA would have had a reasonable expectation of success in using gold, for example, based on Lee's disclosure that "a nickel layer" can be "sputtered" onto the terminals 136 to provide "a surface compatible with electroless plating." APPLE-1015, [0030]. A POSITA would have recognized that the nickel layer (constituting the "*intermediate layer*" containing the "*third metal*") could be sputtered onto the gold terminals 136 to successfully form the nickel layer, because sputtering is known as being generally compatible with a wide variety of underlying materials.

262. As discussed for claim 1, the copper of Lee's first conductive layer 114 (corresponding to the "*second layer*" of the "*conductors*") is a "*second metal*." Therefore, claim 3 is satisfied based on the *first metal* of the terminals 136 being **gold**, the *second metal* of the "copper foil" first conductive layer 114 being **copper**, and the *third metal* of the "nickel layer" being nickel.



Annotated portion of Lee FIG. 1E

XVII. GROUND 2D: Claims 13 and 15 are obvious over Lee in view of Ito (and optionally further in view of Sakamoto)

263. Based on my analysis, claim 13 and 15 are obvious over Lee in view of Ito. To the extent Sakamoto is found necessary to render obvious the aluminum terminals 136 for claim 1, Sakamoto is included in this ground.

A. Analysis of claims

[13]: The circuit module of claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (W_{MAX}) of the contact element.

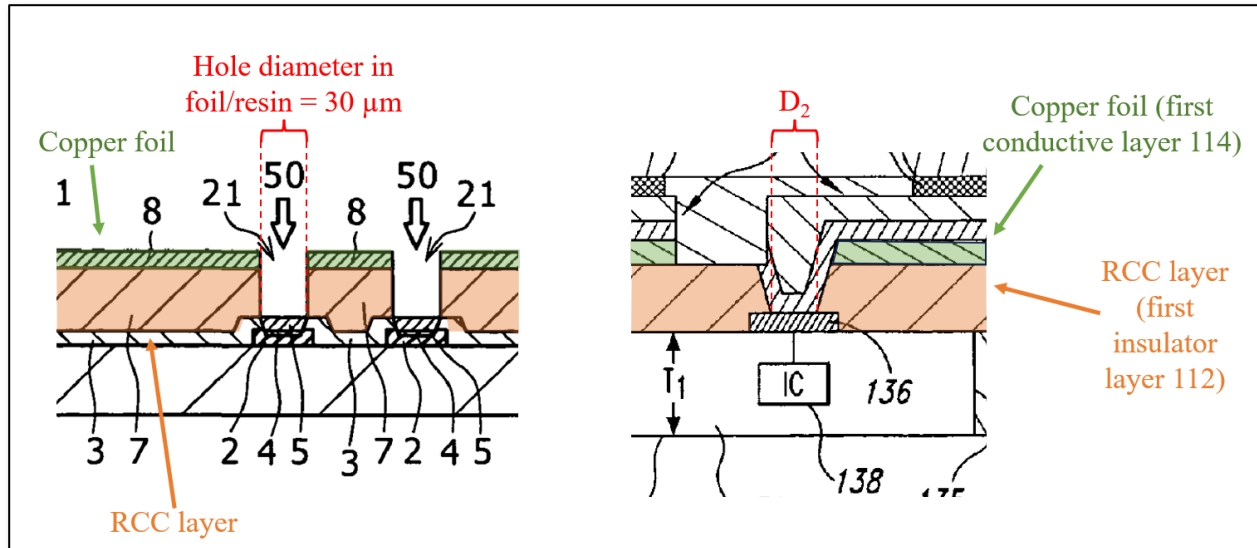
264. It would have been obvious to apply Ito's element dimensions to Lee's structure, thereby obtaining dimensions satisfying claim 13. Although Lee describes the use of holes 120 with dimensions D_1 , D_2 for contacting underlying

terminals 136, and discloses dimension D_3 for the terminals 136, with $D_3 < D_2$, Lee does not explicitly disclose values for these dimensions. APPLE-1015, [0027]-[0029]. Nor does Lee explicitly disclose thicknesses for layers such as the zinc layer formed by zincation, or the second conductor layer 140. APPLE-1015, [0030].

265. It would have been obvious to a POSITA, in selecting values for these dimensions, to apply Ito's teachings for similar corresponding layers. First, with respect to height, based on Ito's teaching that "zincating" on an "aluminum" "terminal electrode" results in "a zinc layer 4 having a thickness of about 0.3 μm ," it would have been obvious to use the same or a similar thickness for Lee's "zincation"-formed zinc layer on the aluminum "terminals 136." APPLE-1015, [0030]; APPLE-1012, [0091]. With the zinc layer applied as the "*contact elements*," the "*contact elements*" have a height H of about 0.3 μm .

266. With respect to width, as discussed in Section VI.A, the "self-aligned" zincation process means that the zinc layer grown by zincation on Lee's terminal 136 would have a greatest width matching, or effectively matching, the width D_2 (which can be equal to D_1) of the holes 120 in the first dielectric layer 112/first conductive layer 114 that expose the terminals 136. APPLE-1012, [0096]; APPLE-1015, [0026], [0029].

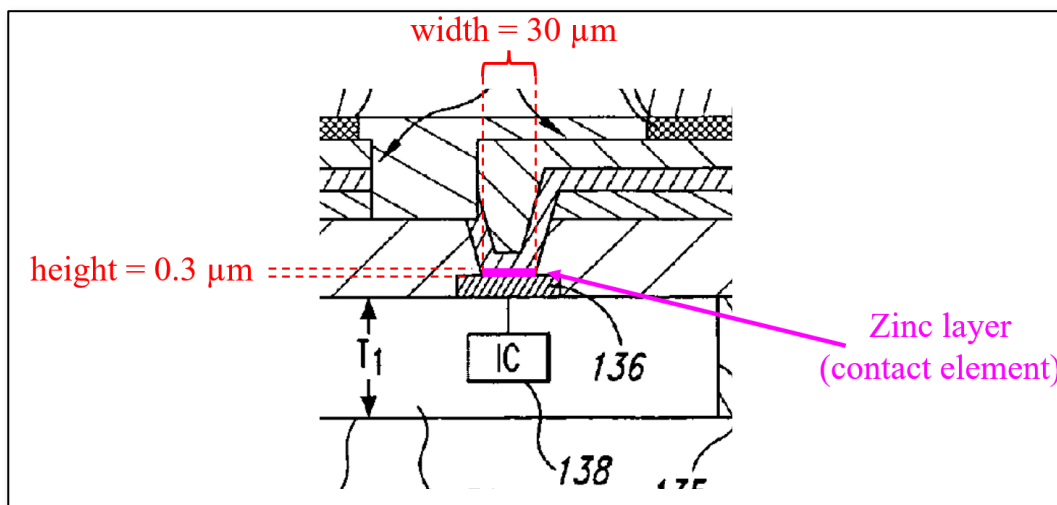
267. Although Lee does not explicitly disclose a value for D_1 or D_2 , Ito discusses “openings 21” in a combination of an “insulating resin layer 7” and a “copper foil layer 8.” APPLE-1012, [0138]. The openings 21 have a “size [] of about 30 μm in diameter.” APPLE-1012, [0138]. It would have been obvious to apply this or a similar opening size as Lee’s D_1 and D_2 , based on the close similarity of the layers in question. Ito’s openings 21 are formed through the same combination of materials as Lee’s holes 120: the openings 21 are through a “resin-coated copper (RCC)” layer 7 and a “copper foil layer 8,” while Lee’s holes 120 are through a “resin coated copper (RCC)” layer 112 and a “copper foil” layer 112. APPLE-1012, [0099], [0107], [0138]; APPLE-1015, [0026]. Further, the openings 21 and the holes 120 are used for the same purpose: for making contact to underlying contact terminals. This correspondence is illustrated below.



Left: portion of Ito FIG. 4A; Right: portion of Lee FIG. 1E (annotated)

268. In addition, both Ito's openings 21 and Lee's holes 120 can be formed using a laser. APPLE-1012, [0138]; APPLE-1015, [0028].

269. Therefore, it would have been obvious, as the application of a known technique from Ito to a very similar device structure in Lee, to apply Ito's hole size of "about 30 μm" as Lee's diameter D₁ and/or D₂. APPLE-1012, [0138]. Based on this dimension, Lee's zinc layer (*contact element*) has a height of 0.3 μm and a maximum width of about 30 μm, satisfying claim 13. Note that these values differ from one another by a factor of 100, such that, for example, Lee's hole diameter could be made much smaller without departing from the scope of claim 13.



Annotated portion of Lee FIG. 1E

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	• First conductive layer 114 (second layer), • Third conductive layer 142 (first layer), and • Contacts 146	Cu	• Zinc layer (intermediate layer)	Zn

[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

270. It would have been obvious to provide Ito's "first passivation layer 101" on the top surface of Lee's dies 130, with contact holes for the terminals 136, in order to passivate the surface. For example, to the extent the first dielectric layer

112 may fail to passivate the surface, a POSITA would have been motivated to obtain passivation by including the first passivation layer 101. The first passivation layer 101 (e.g., “a benzocyclobutene (BCB) resin or a polyimide resin”) would be a polymer layer satisfying claim 15. APPLE-1012, [0010].

XVIII. GROUND 2E: Claims 15-16, 18, and 20 are obvious over Lee in view of Tuominen (and optionally further in view of Sakamoto).

271. Based on my analysis, claims 15-16, 18, and 20 are obvious over Lee in view of Tuominen. To the extent Sakamoto is found necessary to render obvious the aluminum terminals 136 for claim 1, Sakamoto is included in this ground.

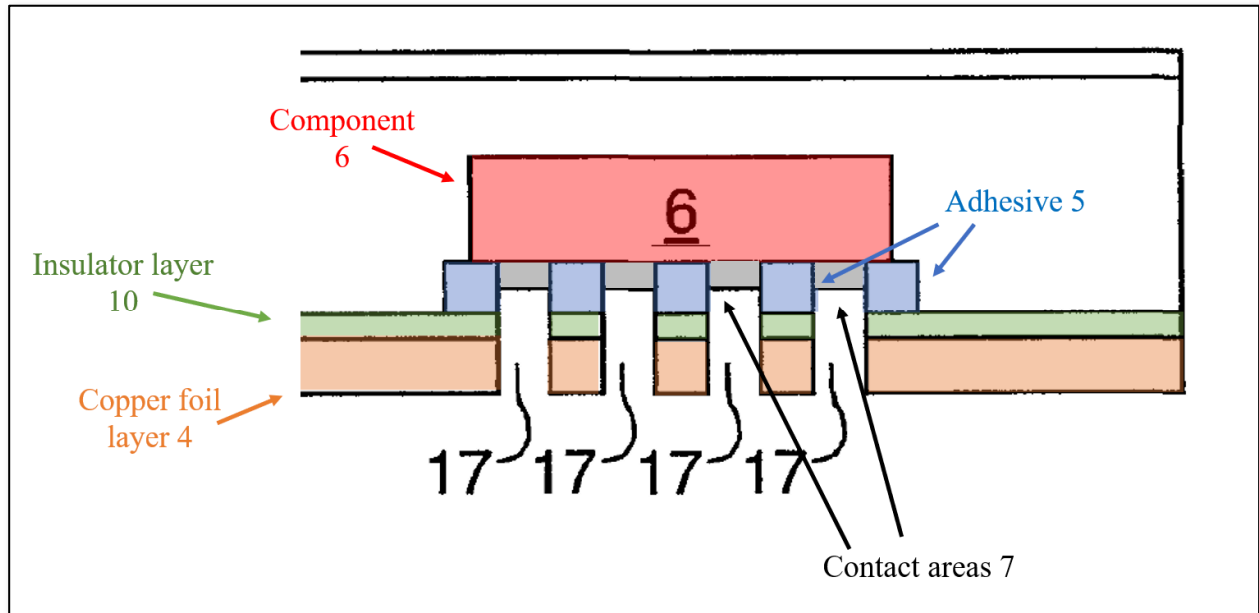
A. Analysis of claims

[15]: The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.

272. It would have been obvious to use Tuominen’s “adhesive 5” to attach Lee’s dies 130 to Lee’s first dielectric layer 112, such that the adhesive (a “polymer layer”) is between the “first insulator layer” (first dielectric layer 112) and the “at least one component” (dies 130) and includes “contact holes.” In Tuominen, the adhesive 5 is used to attach “components 6” (e.g., chips) to an “insulator layer 10.” APPLE-1014, 6:20-25, 19:31-32, FIGS. 3-4. The “insulator layer 10” is included in a “layered membrane” with a “copper foil” (conductor

layer 4). APPLE-1014, 5:3-21. Openings in the adhesive 5 expose contact areas 7.

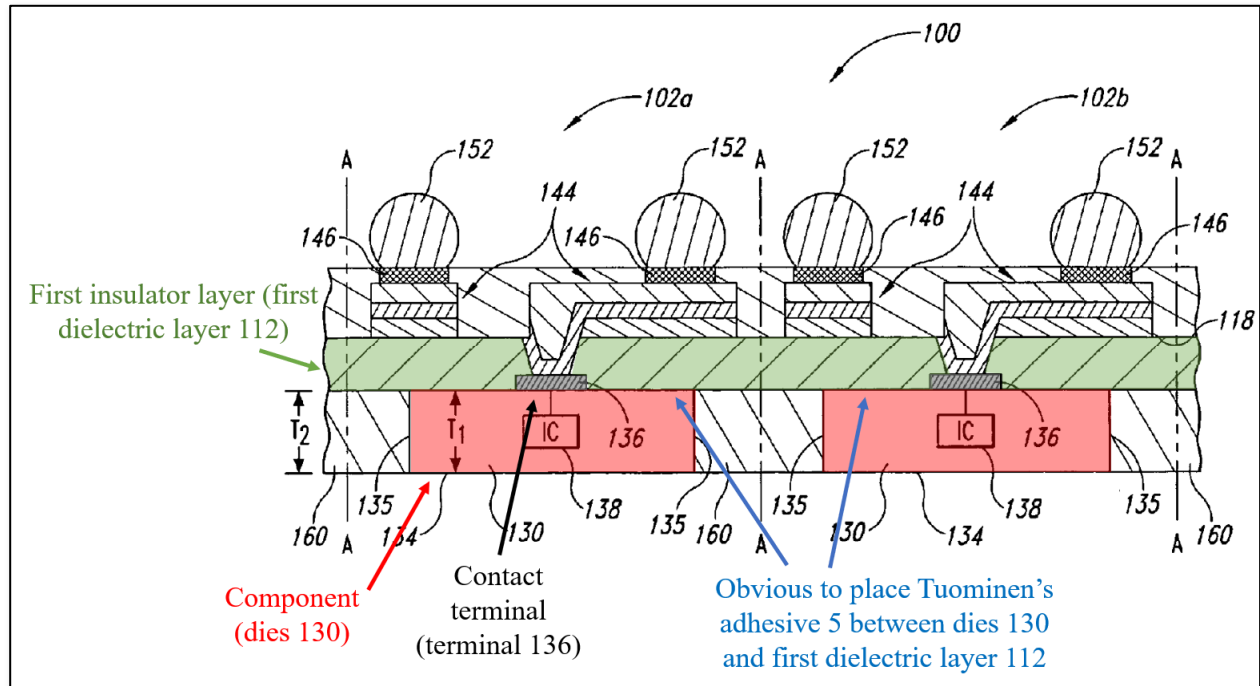
APPLE-1014, 9:26:10:5.



Annotated portion of Tuominen FIG. 9

273. It would have been obvious to use this attachment method, using the adhesive 5, to attach Lee's dies 130 to the first dielectric layer 112. The structures being attached are essentially the same: Lee attaches dies 130 to a combination of a first dielectric layer 112 and a copper foil 114, whereas Tuominen attaches components 6 to a combination of an insulator layer 10 and a copper foil layer 4. APPLE-1015, [0026]; APPLE-1014, 5:3-11. And Lee describes that, although the first dielectric 112 may have adhesive properties that allow attachment "without an adhesive," "in other embodiments [] the microelectronic device assembly may include an adhesive for attaching the dies 130 to the substrate 110." APPLE-1015, [0029]. It would have been obvious, in these "other embodiments," to apply

Tuominen's known method, including the use of the adhesive 5, to obtain the predictable result of the dies 130 attached to the first dielectric layer 112 by the adhesive 5.



Annotated Lee FIG. 1E

274. Tuominen's adhesive 5 is "a thermally hardening epoxy," a polymer. APPLE-1014, 8:8. *See* APPLE-1020, Chapter 7. As a result, when the adhesive 5 is used to attach Lee's dies 130 to Lee's first dielectric layer 112, the resulting structure would include "a polymer layer" (the adhesive 5) between the "first insulator layer" (first dielectric layer 112) and "the at least one component" (dies 130). Further, "contact holes for the contact elements" (terminals 136) would be present in the adhesive to permit electrical connection to the dies 130, matching the

configuration of contact holes in Tuominen's adhesive 5 and Lee's first dielectric layer 112. APPLE-1014, FIG. 9; APPLE-1015, FIG. 1E.

[16]: The circuit module of claim 15, wherein the polymer layer comprises layer of a hardened adhesive.

275. It would have been obvious to have Tuominen's adhesive 5, integrated into Lee's structure as discussed with respect to [15], be a "*hardened adhesive*." For example, Tuominen describes that the adhesive 5 is a "thermally **hardening** epoxy" that can undergo a "final hardening." APPLE-1014, 8:8-21. Tuominen also discusses that "after spreading the adhesive hardens or can be hardened at least partly, in such a way that the adhesive can hold the component in place." APPLE-1014, 7:18-26. It would have been obvious for a POSITA to harden the adhesive to obtain the predictable, desirable result of securing Lee's first dielectric layer 112 to Lee's dies 130, as taught by Tuominen.

[18]: The circuit module of claim 17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

276. See discussion at [15] for Ground 2E.

[20]: The circuit module of claim 19, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

277. See discussion at [15] for Ground 2E.

XIX. CONCLUSION

278. The findings and opinions set forth in this declaration are based on my work and examinations to date.

279. I may continue my examinations. I may also receive additional documentation and other factual evidence over the course of this IPR that will allow me to supplement and/or refine my opinions. I reserve the right to add to, alter, or delete my opinions and my declaration upon discovery of any additional information. I reserve the right to make such changes as may be deemed necessary.

280. In signing this declaration, I recognize that the declaration will be filed as evidence in an IPR before the PTAB. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.