

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title: CIRCUIT MODULE AND METHOD OF MANUFACTURING
THE SAME

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 9,107,324 PURSUANT TO 35 U.S.C. §§311–319, 37 C.F.R. §42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 9,107,324 (“the ’324 Patent”)
APPLE-1002	U.S. Patent No. 9,107,324 File History
APPLE-1003	Declaration of Vivek Subramanian
APPLE-1004	Curriculum Vitae of Vivek Subramanian
APPLE-1005	U.S. Patent Application Publication No. 2004/0168825 (“Sakamoto”)
APPLE-1006	U.S. Patent No. 6,396,148 (“Eichelberger”)
APPLE-1007	Green, T.A., “Gold electrodeposition for microelectronic, optoelectronic and microsystem applications.” <i>Gold Bull</i> 40, 105–114 (2007) (“Green”)
APPLE-1008	Chang, Shou-Yi, et al. “Integrated electrochemical deposition of copper metallization for ultralarge-scale integrated circuits.” <i>Journal of The Electrochemical Society</i> 151.1 (2003) (“Chang”)
APPLE-1009	Qi, Guojun, et al., “Zincating morphology of aluminum bond pad: its influence on quality of electroless nickel bumping.” <i>Thin Solid Films</i> , Volume 406, Issues 1–2 (2002)
APPLE-1010	Arshad, M. et al., “The effects of zincation process on aluminum bond pad surfaces for electroless nickel immersion gold (ENIG) deposition,” <i>2004 IEEE International Conference on Semiconductor Electronics, Kuala Lumpur, Malaysia</i> (2004)

APPLE-1011	Lee, Sung-Ki et al., “A study on the nucleation behavior of zinc particles on aluminum substrate,” <i>Advances in Electronic Materials and Packaging</i> (2001)
APPLE-1012	U.S. Patent Application Publication No. 2007/0126030 (“Ito”)
APPLE-1013	[Reserved]
APPLE-1014	International Patent Application Publication No. 2006/056643 (“Tuominen”)
APPLE-1015	U.S. Patent Application Publication No. 2008/0032447 (“Lee”)
APPLE-1016	U.S. Patent No. 4,246,595 (“Noroyi”)
APPLE-1017	Yung, W et al., “CO2 laser drilling of micro-via without conformal mask in PCB manufacture.” <i>Proceedings of the 1st Pacific International Conference on Laser Materials Processing, Micro, Nano and Ultrafast Fabrication</i> . PICALO (2004): 1st Pacific International Conference on Laser Materials Processing, Micro, Nano and Ultrafast Fabrication. Melbourne, Australia.
APPLE-1018	File history of U.S. Application No. 12/990,785
APPLE-1019	Hsu, S. (2015). Fluxless Tin Bonding Processes with Intermetallic Study and Aluminum Circuit Board Technology. <i>UC Irvine</i> .
APPLE-1020	Coombs, C. Printed Circuit Handbook (Sixth Edition), McGraw-Hill Companies (2008).
APPLE-1021	Weste, N. and Esraghian, K., Principles of CMOS VLSI Design, Addison-Wesley Publishing Company (1988).

APPLE-1022	Goh, W. et al., “The use of electroless copper seed in electrochemical deposited copper interconnect,” Thin Solid Films 462–463, (2004): 275-278
APPLE-1023	Kulkarni, A. K., and C. Lai. “New models for ohmic contacts to GaAs.” Thin Solid Films 164 (1988): 435-439.
APPLE-1024	Excerpt from Keller, H. and Erb, U., Dictionary of Engineering Materials, John Wiley & Sons, Hoboken, NJ (2004)
APPLE-1025	Excerpt from Kaplan, S., Wiley Electrical and Electronics Engineering Dictionary, John Wiley & Sons, Hoboken, NJ (2004)
APPLE-1026	Rossnagel, S, “Directional and preferential sputtering-based physical vapor deposition,” Thin Solid Films 263 (1995): 1-12
APPLE-1027	U.S. Patent No. 7,067,911
APPLE-1028	Bauer, M. and Schneider, J., “Adhesives in the Electronics Industry,” published in <i>Handbook of Adhesive Technology</i> (Second Edition), Marcel Dekker, New York, NY (2003)
APPLE-1029	Declaration of June Ann Munford

LISTING OF CLAIMS

Claim 1	
[1pre]	Circuit module, comprising
[1a]	a first insulator layer having a first surface and a second surface;
[1b]	at least one second insulator layer on the first surface;
[1c]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing a first metal,
[1d]	conductors on the second surface of the first insulator layer, the conductors comprising at least a first layer and a second layer, in such a way that at least the second layer contains a second metal, and
[1e]	contact elements between the contact terminals and the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing a third metal,
[1f]	a contact surface area ($A_{\text{CONT 1}}$) between the intermediate layer and the contact terminal being less than a surface area (A_{PAD}) of the contact terminal.
Claim 2	
[2]	The circuit module of claim 1, wherein the first metal is aluminium, the second metal is copper, and the third metal is at least one of the metals zinc and nickel.
Claim 3	
[3]	The circuit module of claim 1, wherein the first metal is gold, the second metal is copper, and the third metal is nickel.
Claim 4	
[4]	The circuit module of claim 1, wherein the intermediate layer comprises a layer containing zinc.

Claim 5	
[5]	The circuit module of claim 1, wherein the intermediate layer comprises a layer containing copper.
Claim 6	
[6]	The circuit module of claim 1, wherein the intermediate layer comprises at least one layer of nickel and/or of nickel and aluminium.
Claim 7	
[7]	The circuit module of claim 1, wherein the intermediate layer extends along the side walls of the contact elements between the contact terminals and the conductors.
Claim 8	
[8]	The circuit module of claim 1, wherein each contact element comprises a copper core, which connects continuously to the material of the second layer of the conductors.
Claim 9	
[9]	The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, and a second layer of copper on the surface of the first copper layer.
Claim 10	
[10]	The circuit module of claim 1, wherein the conductors comprise a first layer of copper on the second surface of the first insulator layer, an intermediate layer on the surface of the first copper layer, and a second layer of copper on the surface of the intermediate layer.

Claim 11	
[11]	The circuit module of claim 10, wherein the intermediate layer between the first and second coppers layers comprises copper grown by a chemical growing method or nickel grown by a chemical growing method.
Claim 12	
[12]	The circuit module of claim 1, wherein a width (WCONT) of the contact surface between the contact element and the contact terminal of the component is 0-20% less than a greatest width (WMAX) of the contact element in the same direction.
Claim 13	
[13]	The circuit module of claim 1, wherein a height (H) of the contact element is less than, or equal to a greatest width (WMAX) of the contact element.
Claim 14	
[14]	The circuit module of claim 1, wherein the at least one second insulator layer contains at least one layer of fibre material and an opening in the fibre material for the at least one component.
Claim 15	
[15]	The circuit module of claim 1, comprising a polymer layer between the first insulator layer and the at least one component and contact holes for the contact elements in the polymer layer.
Claim 16	
[16]	The circuit module of claim 15, wherein the polymer layer comprises layer of a hardened adhesive.
Claim 17	
[17pre]	Circuit module, comprising

[17a]	a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;
[17b]	a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer covering the first surface of the conductors;
[17c]	at least one second insulator layer on the first surface of the first insulator layer;
[17d]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal;
[17e]	contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,
[17f]	a contact surface area (ACONT 1) between the intermediate layer and the contact terminal being less than a surface area (APAD) of the contact terminal;
[17g]	at least one layer of metal in the contact terminals containing a first metal; at least one layer of metal in the conductors containing a second metal; and the intermediate layer containing a third metal.
Claim 18	
[18]	The circuit module of claim 17, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.
Claim 19	
[19pre]	Circuit module, comprising
[19a]	a conductor layer comprising conductors, the conductors having a first surface and a second surface and at least two layers of metal between the first surface and the second surface;

[19b]	a first insulator layer having a first surface and a second surface, the second surface of the first insulator layer entirely covering the first surface of the conductors;
[19c]	at least one second insulator layer on the first surface of the first insulator layer;
[19d]	at least one component inside the at least one second insulator layer, the at least one component comprising contact terminals containing at least one layer of metal; and
[19e]	contact elements between at least some of the contact terminals and at least some of the conductors for forming electrical contacts, the contact elements comprising an intermediate layer on the surface of the contact terminal, the intermediate layer containing at least one layer of metal,
[19f]	a contact surface area (ACONT 1) between the intermediate layer and the contact terminal being less than a surface area (APAD) of the contact terminal.
Claim 20	
[20]	The circuit module of claim 19, comprising a layer of hardened adhesive between the first insulator layer and the at least one component.

I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for IPR of claims 1-20 (“Challenged Claims”) of U.S. Patent No. 9,107,324 (“the ’324 Patent”).

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. §42.104

A. Grounds for Standing Under 37 C.F.R. §42.104(a)

Petitioner certifies that IPR is available and Petitioner is not barred/estopped.

B. Challenge Under 37 C.F.R. §42.104(b) and Relief Requested

Petitioner requests IPR based on the following grounds. Additional explanation is provided in APPLE-1003, the Declaration of Dr. Subramanian. APPLE-1003, ¶1-280.

Ground	'324 Patent Claims	Basis for Rejection
1A-102, 1A-103	1-2, 4-11, 13-15, 17, 19	§102, §103 – Sakamoto (US 2004/0168825)
1B	3, 9-11	§103 – Sakamoto, Eichelberger (US 6,396,148)
1C	9-11	§103 – Sakamoto, Chang (“ <i>Integrated Electrochemical Deposition of Copper Metallization for Ultralarge-Scale Integrated Circuits</i> ”)
1D	12, 13, 15	§103 – Sakamoto, Ito (US 2007/0126030)
1E	15-16, 18, 20	§103 – Sakamoto, Tuominen (WO 2006/056643)
2A	1-2, 4, 6-8, 10-12, 15-20	§103 – Lee (US 2008/0032447)
2B	1-2, 4-12, 14-20	§103 – Lee, Sakamoto

Ground	'324 Patent Claims	Basis for Rejection
2C	3	§103 – Lee, Eichelberger
2D	13, 15	§103 – Lee, Ito
2E	15-16, 18, 20	§103 – Lee, Tuominen

The '324 Patent claims priority to Finnish Application No. 20085443, filed on May 12, 2008. APPLE-1001, Cover. Although priority is not conceded, each reference qualifies as prior art with respect to the earliest claimed priority date of May 12, 2008:

Reference	Date	Prior Art Under
Sakamoto	9/2/2004 (published)	§102(b)
Eichelberger	5/28/2002 (published)	§102(b)
Chang	01/2004 (published)	§102(b)
Ito	6/7/2007 (published)	§102(a)
	11/18/2006 (filed)	§102(e)
Lee	2/7/2008 (published)	§102(a)
	8/31/2006 (filed)	§102(e)
Tuominen	6/1/2006 (published)	§102(b)

Chang was available to the public at least by January 2004. *See* APPLE-1029.

C. Claim Construction

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Petitioner submits that formal claim constructions are presently unnecessary in view of substantial overlap between the prior art teachings applied in the grounds below and the preferred

embodiments of the '324 Patent.¹ *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); APPLE-1003, ¶21-23.

III. THE '324 PATENT

A. Summary

The '324 Patent purports to provide improvements for contacting circuit modules. APPLE-1001, 3:10-4:41; APPLE-1003, ¶56. It notes difficulties in forming contacts between aluminum and copper. APPLE-1001, 2:6-7; APPLE-1003, ¶56-59.

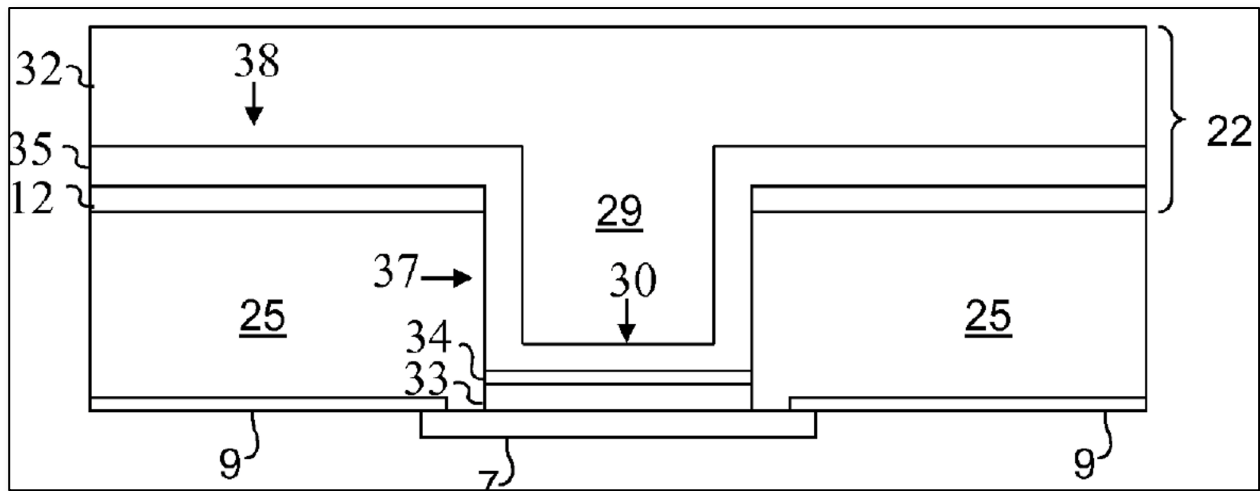
As best understood by Petitioner, claim 1 of the '324 Patent is represented by FIG. 29. *See* APPLE-1001, 22:5-24:36. In FIG. 29, first, second, and third intermediate layers 33, 34, and 35 are arranged on an “aluminum” contact area 7. *Id.*, 20:6-45. Layer 33 is formed “using a chemical growing method to grow a layer containing zinc,” which “grows only on the base part 36” because the conductor foil 12 is composed of copper. *Id.*, 28-33; APPLE-1003, ¶60. Intermediate layers 34, 35 are composed of chemically-grown nickel and copper, respectively. APPLE-1001, 20:33-41; APPLE-1003, ¶60. As such, the '324 Patent uses a

¹ Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

multilayer structure to make an electrical connection to an aluminum contact.

APPLE-1003, ¶¶60-62.

Copper “made using an electrochemical growing method” forms both “a copper core 29” and a “second layer 32” “manufactured in the same process,” so that the copper core 29 and the second layer 32 “connect[] continuously” and “there is no interface between them.” APPLE-1001, 23:29-39; APPLE-1003, ¶¶61.



'324 Patent FIG. 29

B. Prosecution History

U.S. 9,107,324 issued on July 17, 2012, from U.S. Patent Application No. 12/699,628, which was filed on February 3, 2010. *See* APPLE-1002. No Office Actions were issued during prosecution of the '324 Patent. The Examiner's reasons for allowance pointed to the claimed “contact elements” limitation, stating that this limitation “was neither found to be disclosed in nor suggested by the prior art.” APPLE-1002, 17; APPLE-1003, ¶¶63-64.

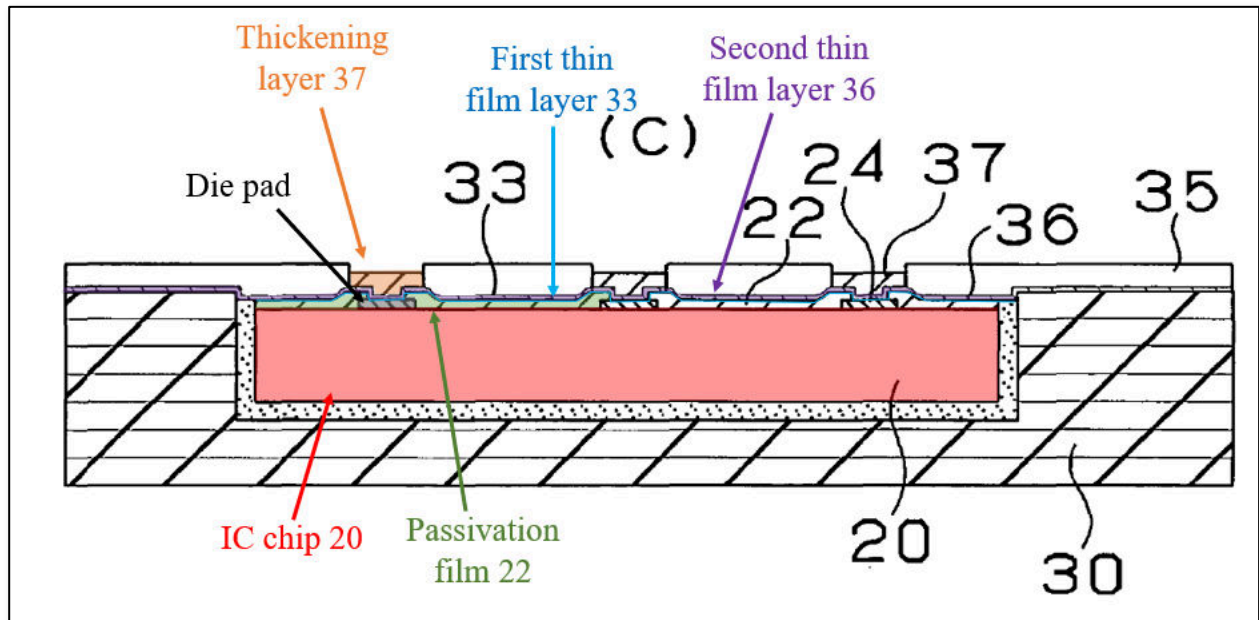
C. Level of Ordinary Skill

A person having ordinary skill in the art (“POSITA”) at the time of the alleged invention would have had a bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and at least three years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent, with additional education substituting for experience and vice versa. APPLE-1003, ¶24-25.

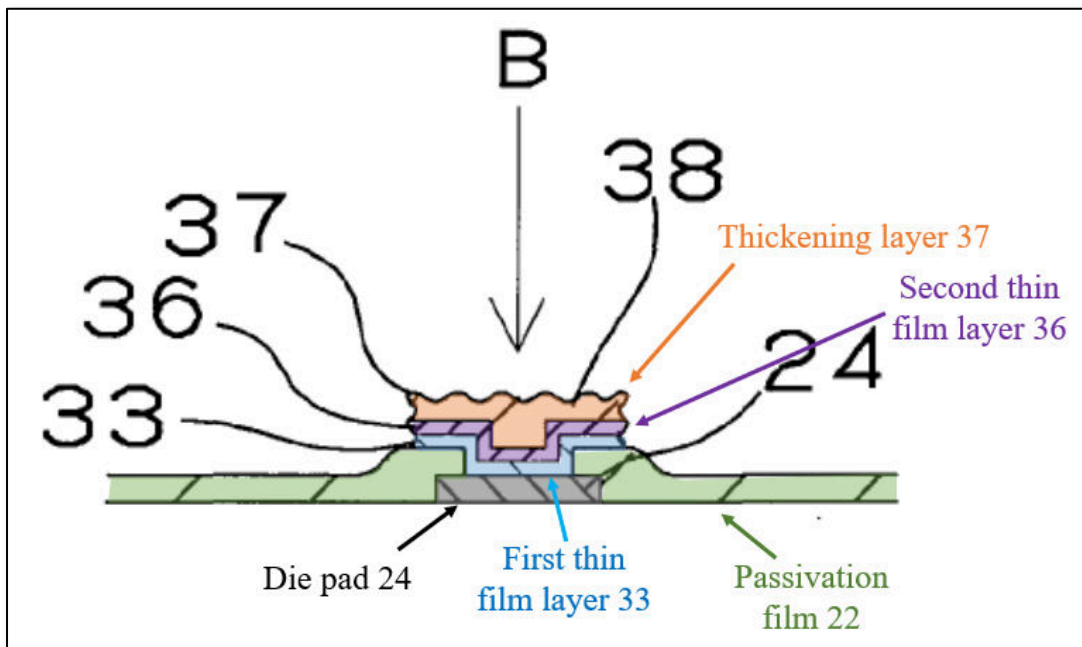
IV. GROUNDS 1A-102 and 1A-103: Claims 1-2, 4-11, 13-15, 17, and 19 are anticipated by or obvious over Sakamoto

A. Sakamoto

Sakamoto (US 2004/0168825) is directed to “a structure capable of electrically connecting a multilayer printed circuit board to an IC chip.” APPLE-1005, [0009]. An example of the contact structure of Sakamoto is shown in FIGS. 2(C) and 7, reproduced below. A “transition layer 38” on the “die pad 24” of an “IC chip 20” includes “three layers” including a “first thin film layer 33,” a “second thin film layer 36,” and a “thickening film [or layer] 37.” APPLE-1005, [0101]. The transition layer 38 contacts the die pad 24 through an opening in a passivation film 22 (incorrectly given the reference number 24 in the specification). APPLE-1005, [0101], FIG. 2(C); APPLE-1003, ¶65-68.



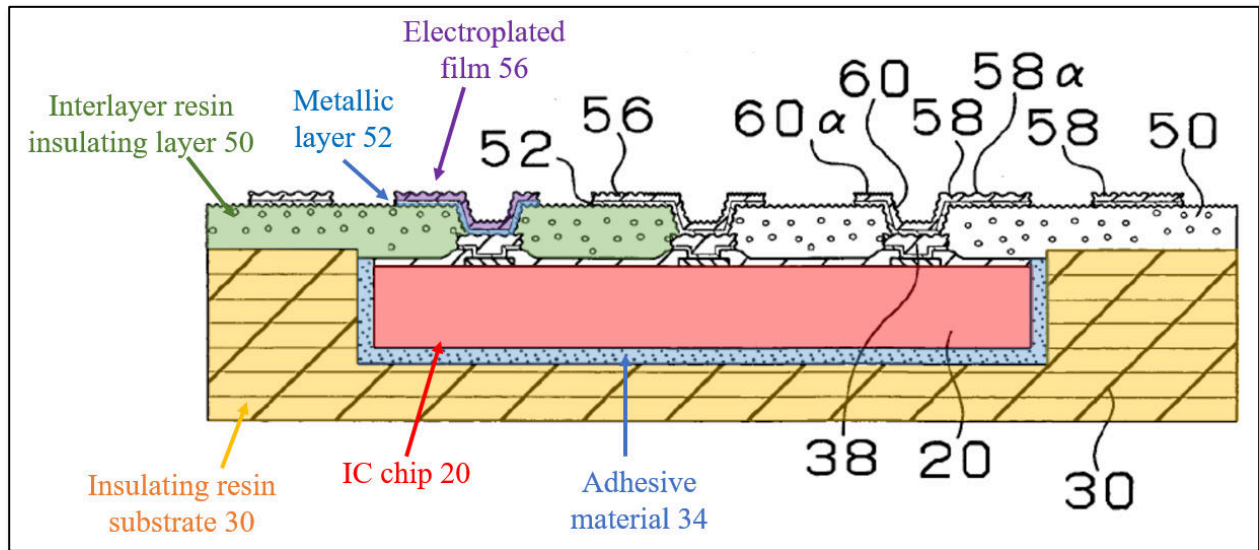
Sakamoto FIG. 2(C)²



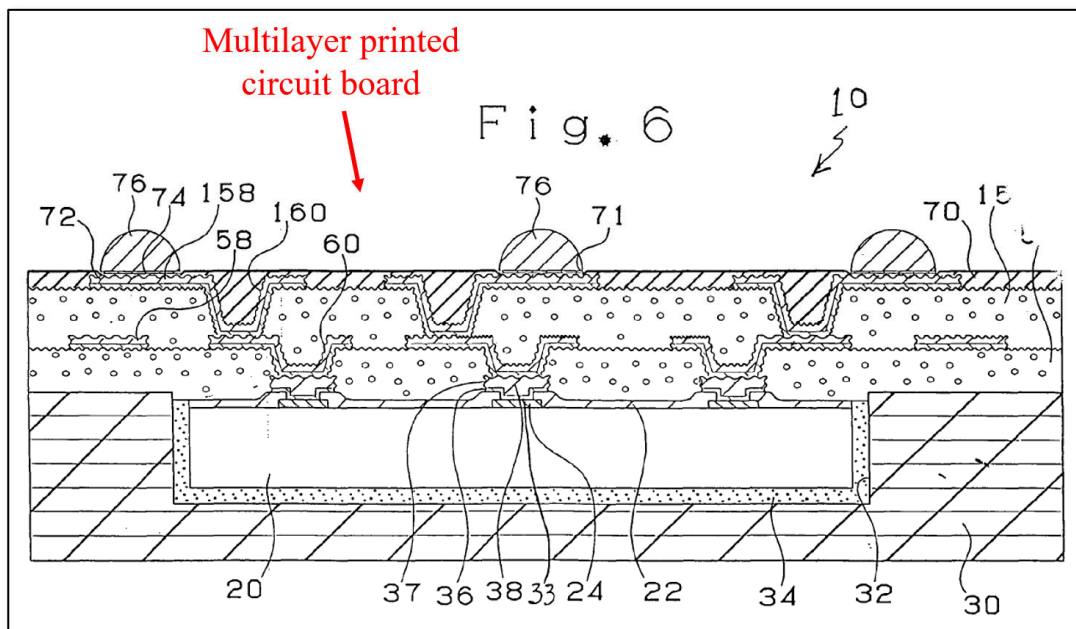
Sakamoto FIG. 7(A)

² Figure annotations added throughout.

The IC chip 20 is mounted in an “adhesive material 34” provided in a recess of “an insulating resin substrate (or core substrate) 30.” APPLE-1005, [0106], [0107], FIG. 1(D). An “interlayer resin insulating layer 50” is on the passivation film 22 and the transition layer 38. APPLE-1005, [0118], FIG. 4(C). “[C]onductor circuits 58 each consisting of [a] metallic layer 52 and [an] electroplated film 56” are on layer 50 and contact the transition layer 38. APPLE-1005, [0125], FIG. 4(C); APPLE-1003, ¶69. FIG. 6 of Sakamoto illustrates a fully-manufactured “multilayer printed circuit board.” APPLE-1005, [0099], [0105]; APPLE-1003, ¶70.



Sakamoto FIG. 4(C)



Sakamoto FIG. 6

Sakamoto is analogous art to the '324 Patent. APPLE-1003, ¶71. Both are in the same fields of endeavor of IC manufacture and structure and address the problem of contacting aluminum pads. The '324 Patent describes that "[t]he object of the invention is to develop a new contact element structure" that is "bumpless,

i.e. without growing bumps on top of the contact areas of the component.”³

APPLE-1001, 1:48-51, 3:10-13. Similarly, Sakamoto describes that the use of a “transition layer 38” makes it “possible to electrically connect the IC chip to the multilayer printed circuit board” “**without using** a sealing resin, leads or **bumps**.”

APPLE-1005, Abstract, [0050].

B. Analysis of Claims

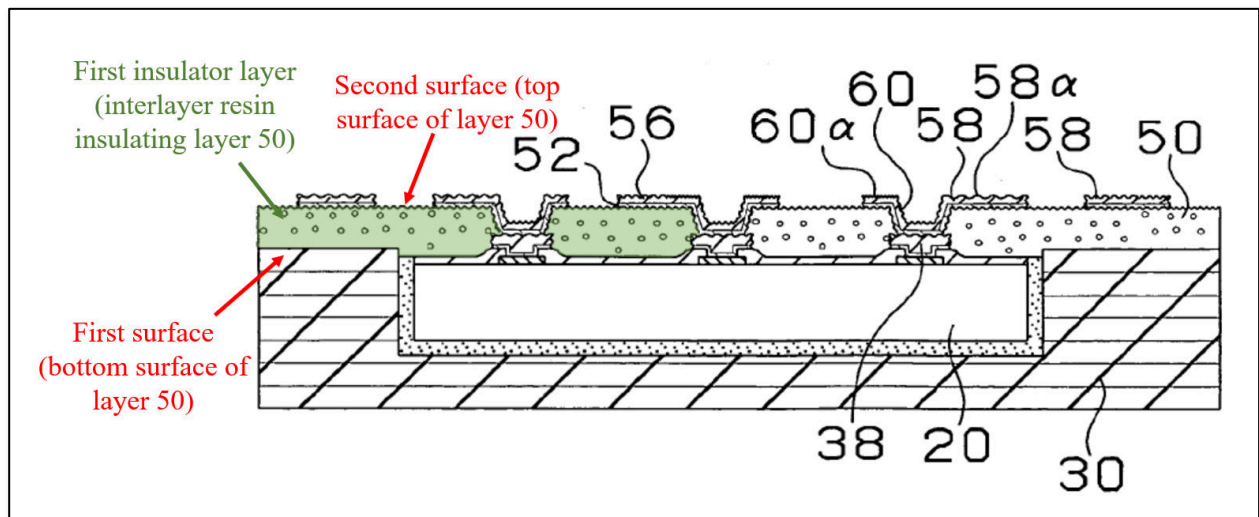
[1pre]:

Petitioner does not concede this preamble is limiting. Sakamoto’s “multilayer printed circuit board 10” is a “circuit module.” APPLE-1005, [0099], FIG. 6; APPLE-1003, ¶87.

[1a]:

Sakamoto’s “interlayer resin insulating layer 50” is a first insulator layer having a “*first surface*” (its bottom surface) and a “*second surface*” (its top surface). APPLE-1005, [0118], FIG. 6; APPLE-1003, ¶88.

³ Emphasis unless otherwise noted.



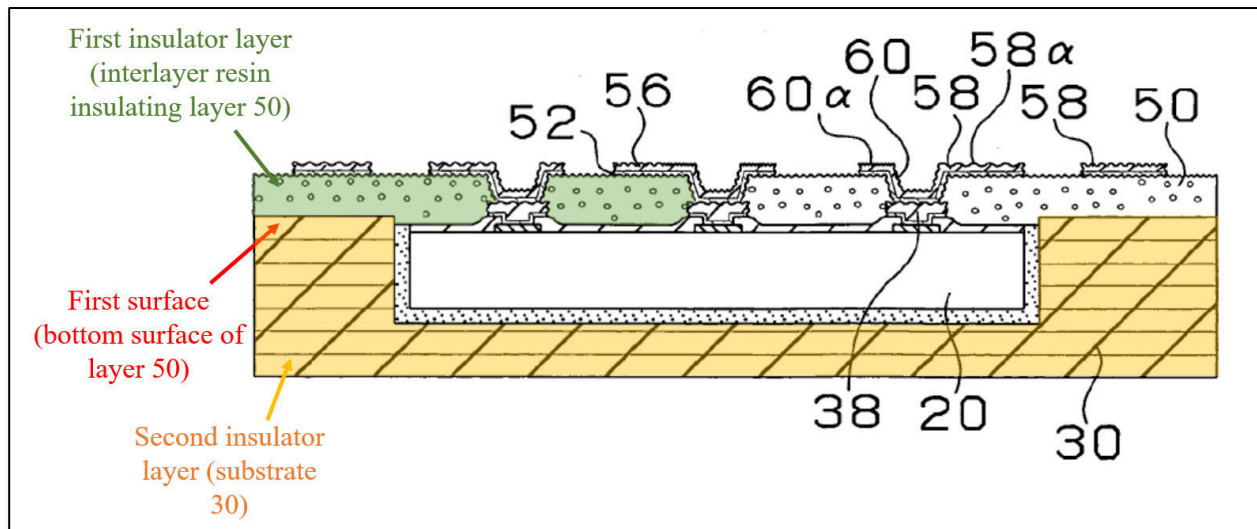
Sakamoto FIG. 4(C)

[1b]:

Sakamoto's "insulating resin substrate (or core substrate) 30" is a "*second insulator layer*" on the "*first surface*" (the bottom surface of layer 50). APPLE-1005, [0106], FIG. 6; APPLE-1003, ¶89.⁴ The substrate 30 is a layer of a "multilayer printed circuit board 10" and can itself include multiple prepreg layers and/or multiple substrate layers. APPLE-1005, [0100], [0106]; APPLE-1003, ¶90.

⁴ To the extent "at least one second insulator layer on the first surface" is interpreted as a product-by-process element, the recited process would have no patentable weight for purposes of determining unpatentability. *See Abbott Laboratories v. Sandoz, Inc.*, 566 F.3d 1282 (Fed. Cir. 2009) ("a product in the prior art made by a different process can anticipate a product-by-process claim").

See '324 Patent FIGS. 1 and 4, illustrating “insulator layer 1” as an example of the “*second insulator layer*.” APPLE-1003, ¶90. The insulator layer 1 is a “prepreg” layer or “an FR4 or FR5-type sheet,” which are common PCB substrate materials. APPLE-1001, 24:23-36; APPLE-1003, ¶90. The insulator layer 1 is “*on the first surface*” of the “insulator layer 13” (an example of the “*first insulator layer*”). APPLE-1001, FIGS. 1, 4; APPLE-1003, ¶90.



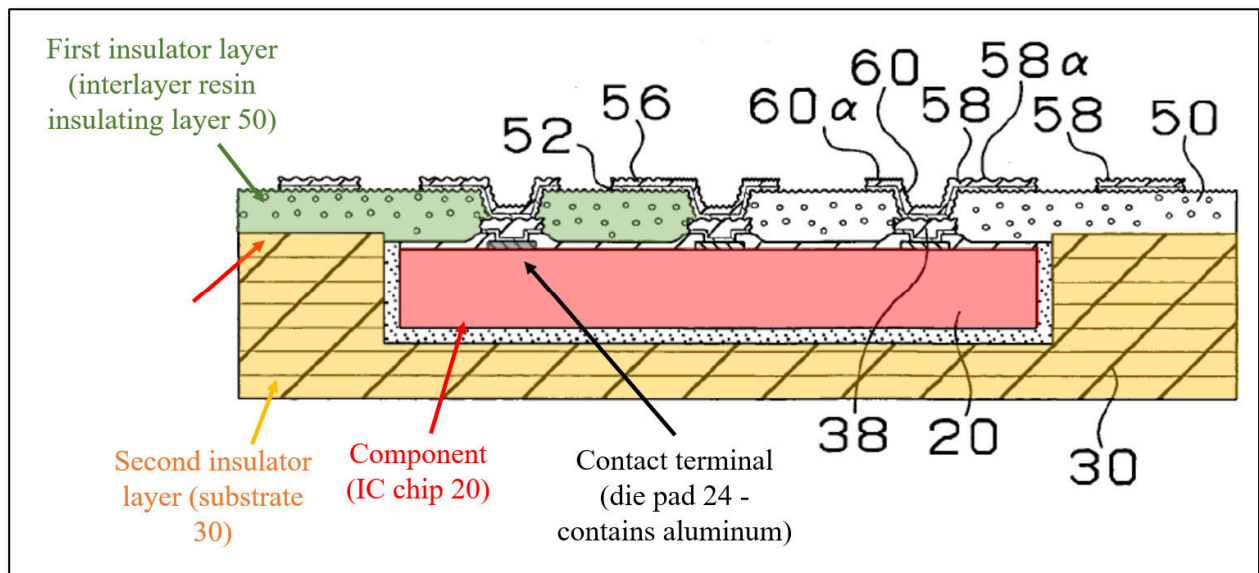
Sakamoto FIG. 4(C)

[1c]:

Sakamoto’s “IC [integrated circuit] chip 20” is a “*component*” that is inside the “*second insulator layer*” (substrate 30). APPLE-1005, [0108], FIG. 6; APPLE-1003, ¶91. Cf. the ’324 Patent’s description that “[t]he component [] can be, e.g., an integrated circuit.” APPLE-1001, 24:14-15.

The *at least one component* (the IC chip 20) comprises “die pads 24,” “each

constituting an input/output terminal,” which are “*contact terminals*.” APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶91. The die pads 24 are “made of **aluminum**,” an example of a “*first metal*.” APPLE-1005, [0101] *see also id.*, [0051] (“the pad of the IC chip is normally formed out of aluminum or the like.”); APPLE-1003, ¶92.



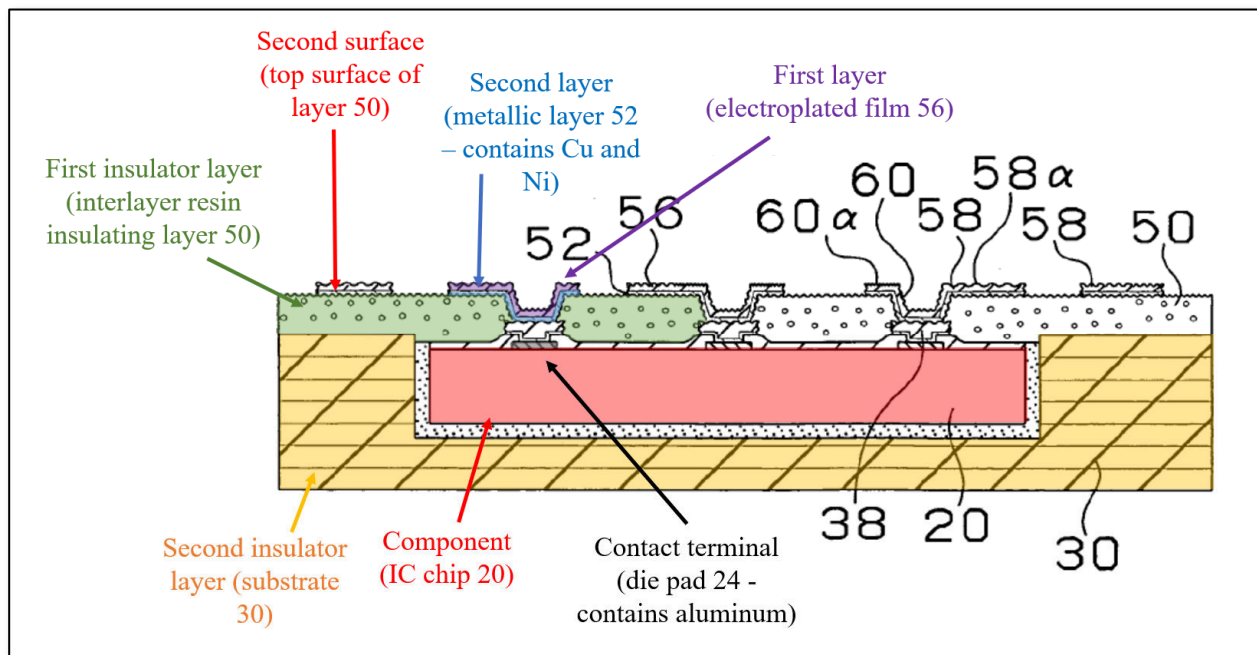
Sakamoto FIG. 4(C)

[1d]:

Sakamoto’s “conductor circuits 58 are *conductors*.” APPLE-1005, [0125]; APPLE-1003, ¶93. The conductor circuits 58 are on the “*second surface*” (top surface) of the “*first insulator layer*” (layer 50). APPLE-1005, [0011], [0125], FIG. 6; APPLE-1003, ¶94.

The conductor circuits 58 include a “*first layer*” (electroplated film 56) and a “*second layer*” (metallic layer 52). APPLE-1005, [0125], FIG. 6; APPLE-1003,

¶95. At least layer 52 (an example of the *second layer*) includes a “*second metal*.” For example, Sakamoto describes that layer 52 is an “Ni/Cu” layer. APPLE-1005, [0123]; APPLE-1003, ¶95. Thus, layer 52 contains, as the “*second metal*,” **copper** or **nickel**. APPLE-1003, ¶95.



Sakamoto FIG. 4(C)

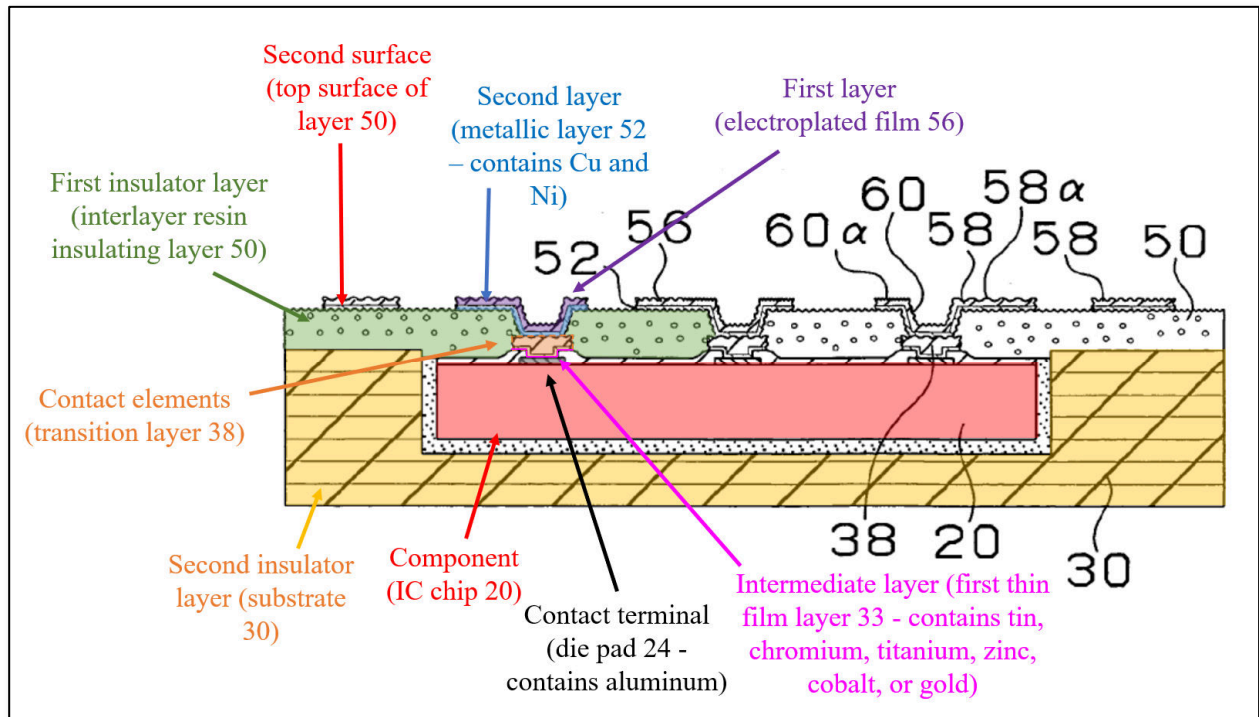
[1e]:

Sakamoto’s “transition layer 38” comprises “*contact elements*” between the “*contact terminals*” (die pads 24) and the “*conductors*” (conductor circuits 58 including metallic layer 52 and electroplated film 56). APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶96. The transition layer 38 is “*for forming electrical contacts*.” APPLE-1003, ¶96. For example, Sakamoto describes that die pads 24 of separate IC chips 20, 120 “are mutually connected through transition layers 38.” APPLE-

1005, [0164]; APPLE-1003, ¶96.

The transition layer 38 (“*contact elements*”) comprises first thin film layer 33, an “*intermediate layer*,” intermediate between the die pad 24 and the second thin film layer 36. APPLE-1005, [0020], [0109], FIG. 7(A); APPLE-1003, ¶97. Layer 33 is “*on the surface of the contact terminal*” (die pad 24). APPLE-1005, [0020], FIGS. 6, 7(A); APPLE-1003, ¶97.

Layer 33 (“*intermediate layer*”) contains a *third metal*, e.g., “**tin**, **chromium**, **titanium**, [] **zinc**, **cobalt**, [or] **gold**.” APPLE-1005, [0109]; APPLE-1003, ¶98.



Sakamoto FIG. 4(C)

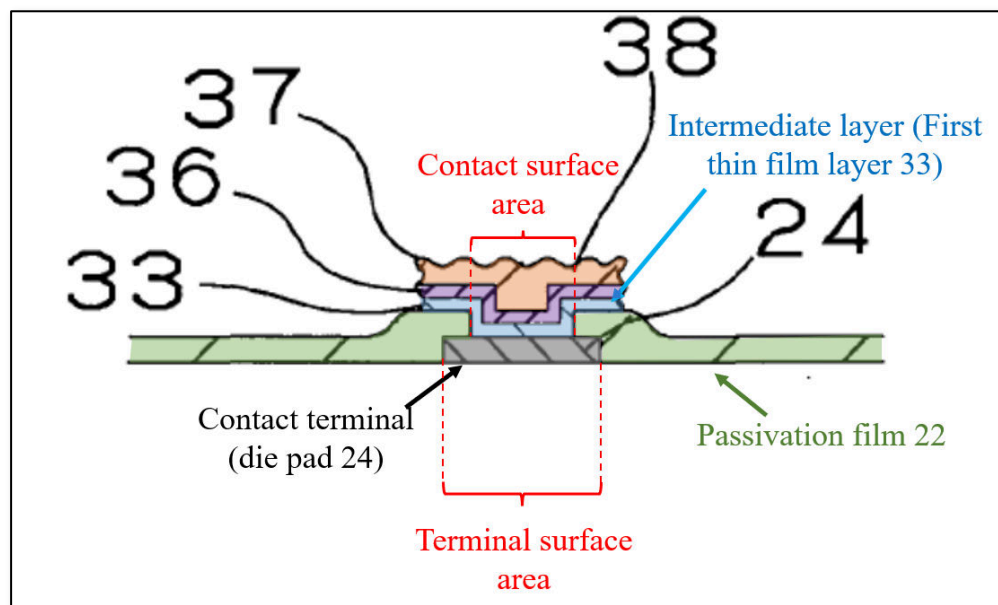
The applied mapping of Sakamoto's elements to those of claim 1 are shown in the table below. APPLE-1003, ¶99.

First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> • Metallic layer 52 (<i>second layer</i>), and • Electroplated film 56 (<i>first layer</i>) 	Cu or Ni	<ul style="list-style-type: none"> • First thin film layer 33 (<i>intermediate layer</i>), • Second thin film layer 36, and • Thickening layer 37 	Sn, Ti, Zn, Co, or Au

[1f]:

According to the mappings of [1c] and [1e], this claim element corresponds

to a contact surface area between the layer 33 (“*intermediate layer*”) and the die pad 24 (“*contact terminals*”) being less than a surface area of the die pad 24. This configuration is disclosed, e.g., by FIG. 7(A), which illustrates that “die pads 24 [] are provided in the openings of the passivation film [22].” APPLE-1005, [0101]; APPLE-1003, ¶100.



Sakamoto FIG. 7(A)

FIGS. 1(D), 2(C), 4(C), 6, and 7(A) show that the passivation layer 22 covers outer portions of the die pad 24, with only a central portion of the die pad 24 exposed. Layer 33 deposited on the exposed portion of the die pad 24 forms a contact surface area that is less than a surface area of the die pad 24, because the exposed portion – the only portion in contact with layer 33 – is smaller than the full surface area of the die pad 24. APPLE-1003, ¶101-102.

The teachings of Sakamoto's FIG. 7(A) and the other cited figures can be relied upon, even in the absence of explicit corresponding description in the Specification. *See In re Mraz*, 455 F.2d 1069, 1072 (C.C.P.A. 1972); *see also Cummins-Allison Corp. v. SBM Co.*, 484 F. App'x 499, 507 (Fed. Cir. 2012). Here, Sakamoto's drawings show, with great particularity and intentionality, the presence of substantial overlap between the passivation layer 22 and the die pads 24. APPLE-1005, FIGS. 1(D), 2(C), 4(C), 6, and 7(A); APPLE-1003, ¶103. For example, the passivation layer 22 is illustrated with clear bumps due to its overlap with the die pads 24, and the deposited layers 33, 36, 37 are shown protruding into a recess formed by the bumps. APPLE-1005, FIGS. 1(D), 2(C), 4(C), 6, and 7(A); APPLE-1003, ¶103. The downward protrusion of layer 33 contacts less than an entirety of the surface area of the die pad 24, such that the "contact surface area" element is satisfied. APPLE-1003, ¶103.

Indeed, the notion that a contact surface area is less than a total surface area of the bottom pad has been standard in circuit manufacturing for decades. APPLE-1003, ¶104-105.

Apart from Sakamoto's express disclosure, it also would have been obvious to form the contact surface area between layer 33 and the die pad 24 to be less than a surface area of the die pad 24, based on Sakamoto's teachings with respect to hole formation. APPLE-1003, ¶106. In the context of forming "via holes" in layer

50, Sakamoto discusses (i) the desirability of forming via holes smaller than the die pad so that a boring laser does not impinge outside the die pad, and (ii) that the via holes should be smaller than the die pad because large holes can make alignment more difficult. APPLE-1005, [0011]-[0013]; APPLE-1003, ¶107. A POSITA would have understood that these same considerations would apply to forming the openings in the passivation layer 22 and, therefore, would have been motivated to make the openings smaller than the die pads 24, matching the illustrations in Sakamoto's figures. APPLE-1003, ¶108. With this obvious configuration, the contact surface area between layer 33 and the die pad 24 would be less than the surface area of the die pad 24. APPLE-1003, ¶108.

[2]:

In the mappings applied for claim 1, die pads 24 are “made of **aluminum**” (the *first metal*), the metallic layer 52 corresponding to the “*second layer*” of the “*conductors*” includes “**Cu**” (the *second metal*), and the first thin film layer 33 corresponding to the “*intermediate layer*” can be any of several metals, including “**zinc**” (the *third metal*). APPLE-1005, [0051], [0101], [0109], [0123]; APPLE-1003, ¶109.

[4]:

Sakamoto describes that the “metal used” for layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be tin, chromium, titanium,

nickel, **zinc**, cobalt, gold, or copper.” APPLE-1005, [0109]; APPLE-1003, ¶110.

See [1e].

[5]:

Sakamoto describes that the “metal used” for layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be tin, chromium, titanium, nickel, zinc, cobalt, gold, or **copper**.” APPLE-1005, [0109]. *See* [1e]; APPLE-1005, [0109]; APPLE-1003, ¶111.

As explained above, layer 52 (corresponding to the “*second layer*” of the “*conductors*,” which contains a “*second metal*”) is “**Ni/Cu**” such that the “*second metal*” can be nickel. APPLE-1003, ¶112.

The “*first metal*” is the “**aluminum**” of the die pads 24. APPLE-1005, [0051]; APPLE-1003, ¶113.

[6]:

Sakamoto describes that the “metal used” for layer 33 (corresponding to the “*intermediate layer containing a third metal*”) “may be tin, chromium, titanium, **nickel**, zinc, cobalt, gold, or copper.” APPLE-1005, [0109]; APPLE-1003, ¶114.

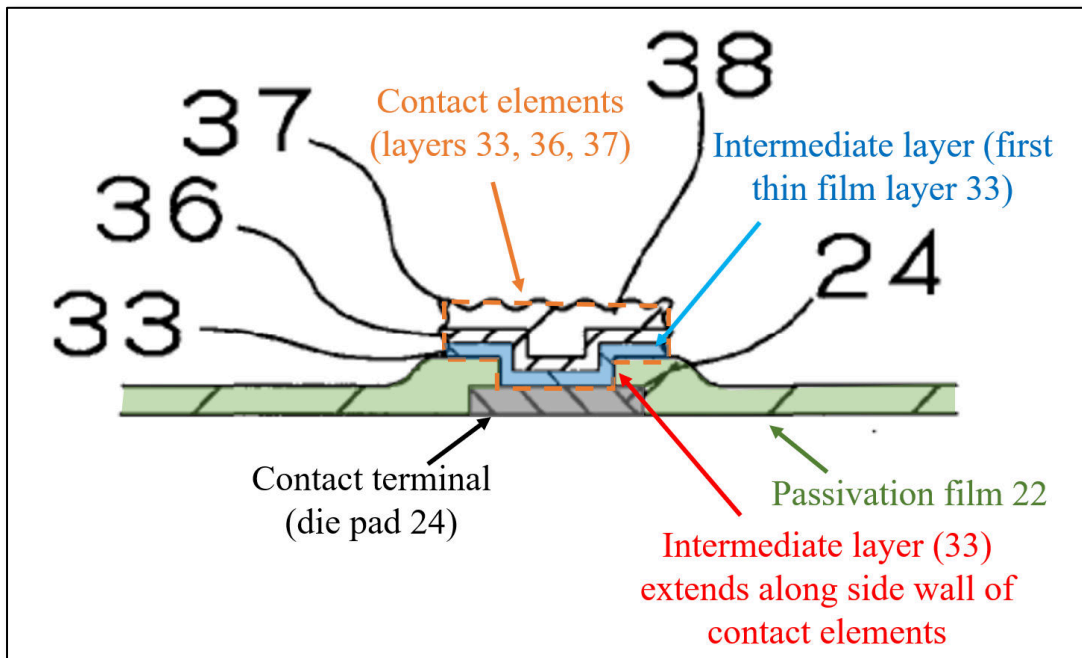
Layer 52 (corresponding to the “*second layer*” of the “*conductors*,” which contains a “*second metal*”) is “**Ni/Cu**” such that the “*second metal*” can be copper. APPLE-1003, ¶115.

The “*first metal*” is the “**aluminum**” of the die pads 24. APPLE-1005,

[0051]; APPLE-1003, ¶116.

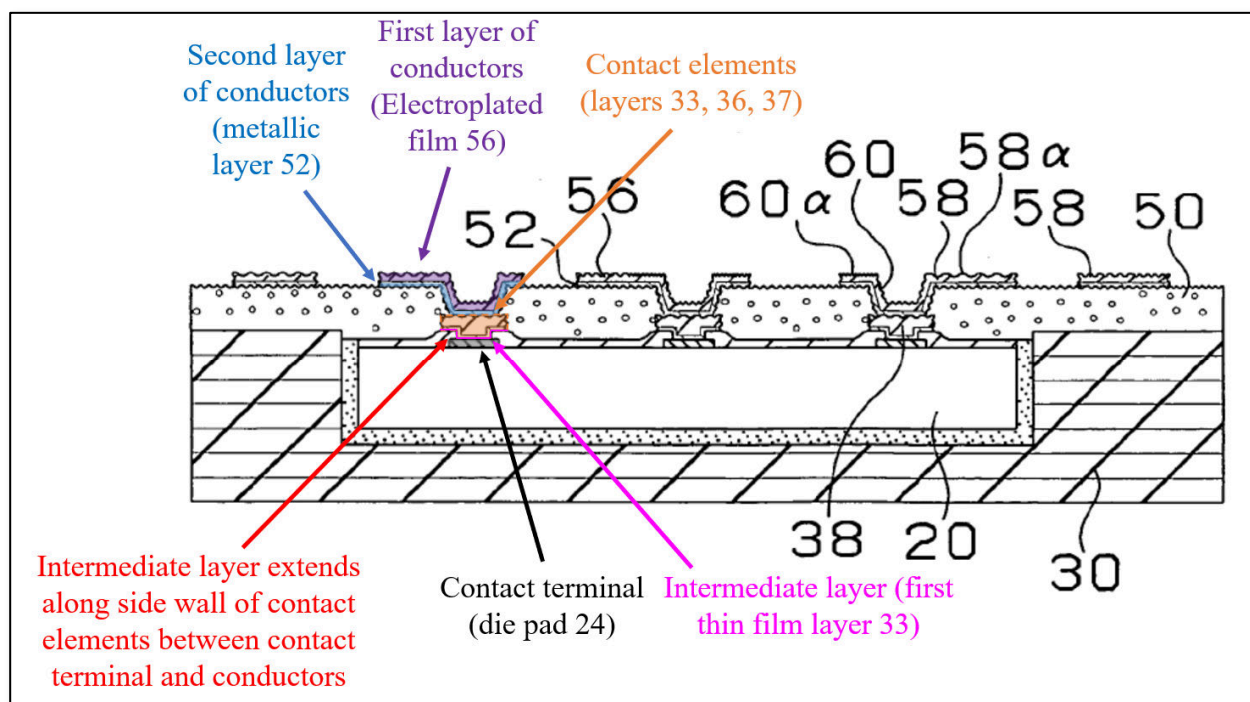
[7]:

Transition layer 38, which includes layers 33, 36, and 37, is applied as the “*contact elements*,” and layer 33 is applied as the “*intermediate layer*.” APPLE-1005, [0101], [0109]; APPLE-1003, ¶117. *See* [1e]. As shown below, the layer 33 extends along side walls of the transition layer 38. APPLE-1005, FIG. 7(A); APPLE-1003, ¶117.



Sakamoto FIG. 7(A)

As shown below, the extension of layer 33 along the side walls of the transition layer 38 is between the die pad 24 (“*contact terminals*”) and layer 52/film 56 (“*conductors*”). APPLE-1005, FIG. 6; APPLE-1003, ¶118.



Sakamoto FIG. 4(C)

[8]:

Thickening layer 37 includes a “*copper core*” that “*connects continuously to the material of the second layer of the conductors.*” APPLE-1003, ¶119. For claim 1, the entirety of layers 33, 36, and 37 were applied as the “*contact elements.*”

However, it is equally valid to apply layers 33 and 34 and the **core** of the thickening layer 37 as the “*contact elements*.” APPLE-1003, ¶119.

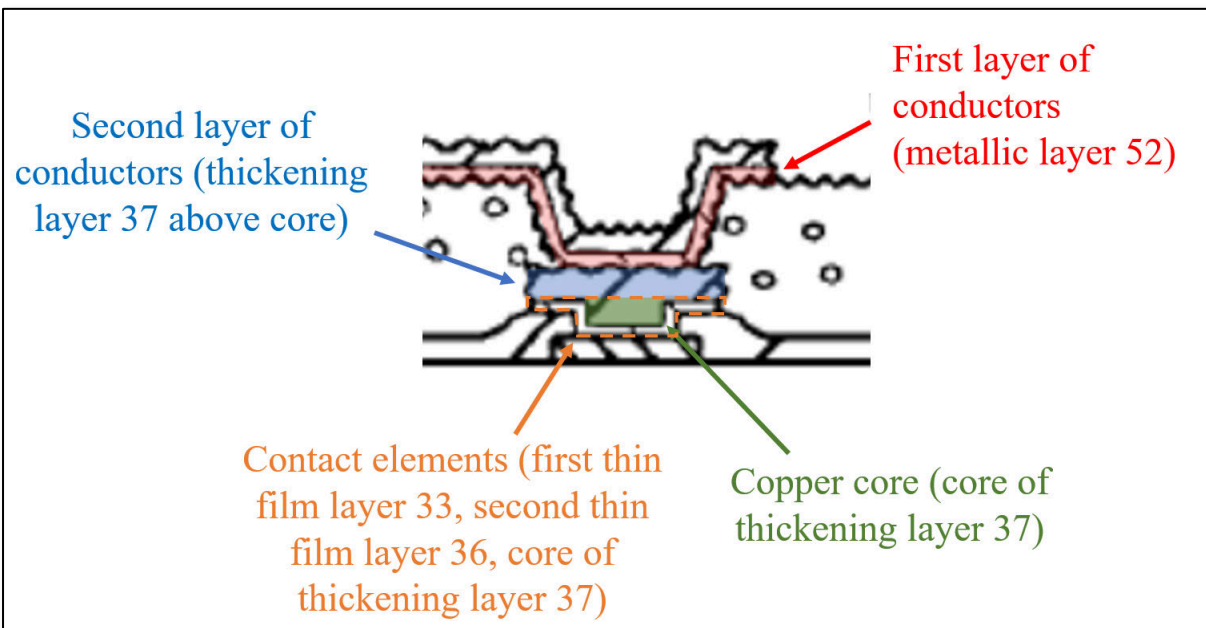
Further, for claim 1, layer 52 and film 56 were applied as the “conductors.” However, it is equally valid to apply layer 52, film 56, **and** the thickening layer 37 above the core as the “conductors,” of which layer 52 is applied as the “first layer” and the thickening layer 37 above the core is applied as the “second layer.”

APPLE-1003, ¶120. Sakamoto discloses that the thickening layer 37 is an electroplated **copper** layer, such that this mapping corresponds to the “*second metal*” (of the “*conductors*”) being **copper**. APPLE-1005, [0025], [0111], [0114]; APPLE-1003, ¶120.

These mappings are shown in the table and annotated FIG. 4(C) below.

APPLE-1003, ¶121.

First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none">• Metallic layer 52 (<i>first layer</i>),• Electroplated film 56, and• Thickening layer 37 above core (<i>second layer</i>)	Cu	<ul style="list-style-type: none">• First thin film layer 33 (<i>intermediate layer</i>),• Second thin film layer 36, and• Core of thickening layer 37 (<i>copper core</i>)	Sn, Ti, Ni, Zn, Co, or Au



Portion of Sakamoto FIG. 4(C)

The core of the thickening layer 37 is a “*copper core*” that “*connects continuously*” to the material of the thickening layer 37 above the core (“*second layer of the conductors*”), because these elements are formed in a common, continuous electroplating process. APPLE-1005, [0114]; APPLE-1003, ¶122.

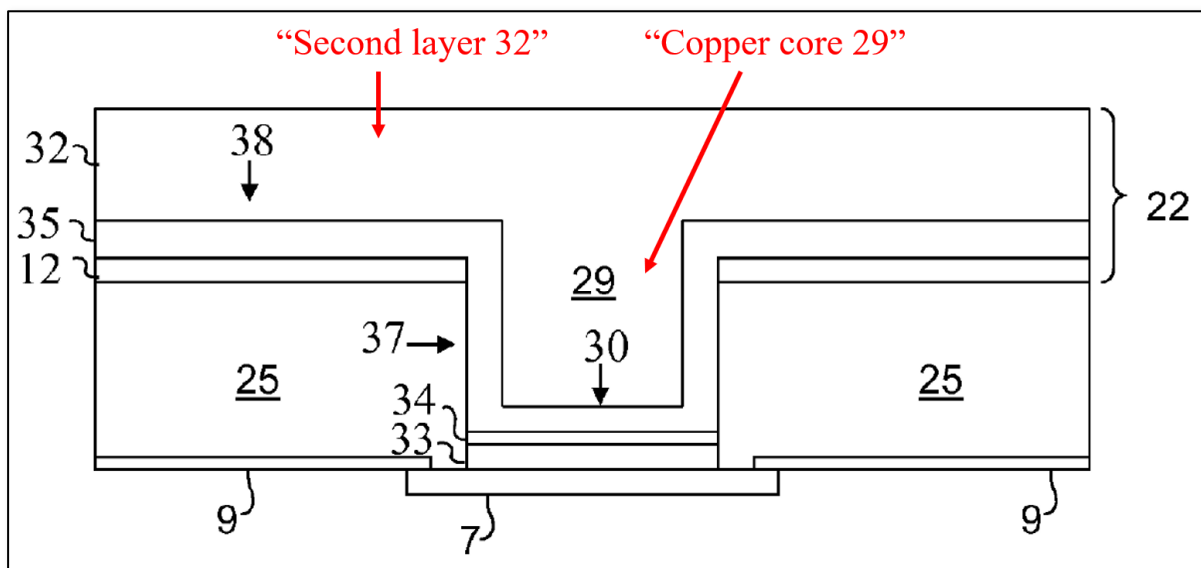
The foregoing mapping, in which a single material, grown in a single process, is applied as both the “*copper core*” and the “*second layer*” of the conductors, is consistent with the ’324 Patent’s description. APPLE-1003, ¶123. The ’324 Patent describes that “[a] layer 32 of copper is grown on top of the third intermediate layer using an electrochemical growing method, which also forms the conductor core 29 of the contact element” and that “the material of the copper core 29 of the contact element and of the second layer 32 of the conductor 22 is

manufactured in the same process, so that [] there is no interface between them.”

APPLE-1001, 20:42-45, 23:35-39. The copper core 29 and the second layer 32

“connect[] continuously, i.e., without an interface.” APPLE-1001, 30-35. FIG. 29

of the '324 Patent similarly illustrates a continuous connection between the copper core 29 and layer 32. APPLE-1003, ¶123.



'324 Patent FIG. 29

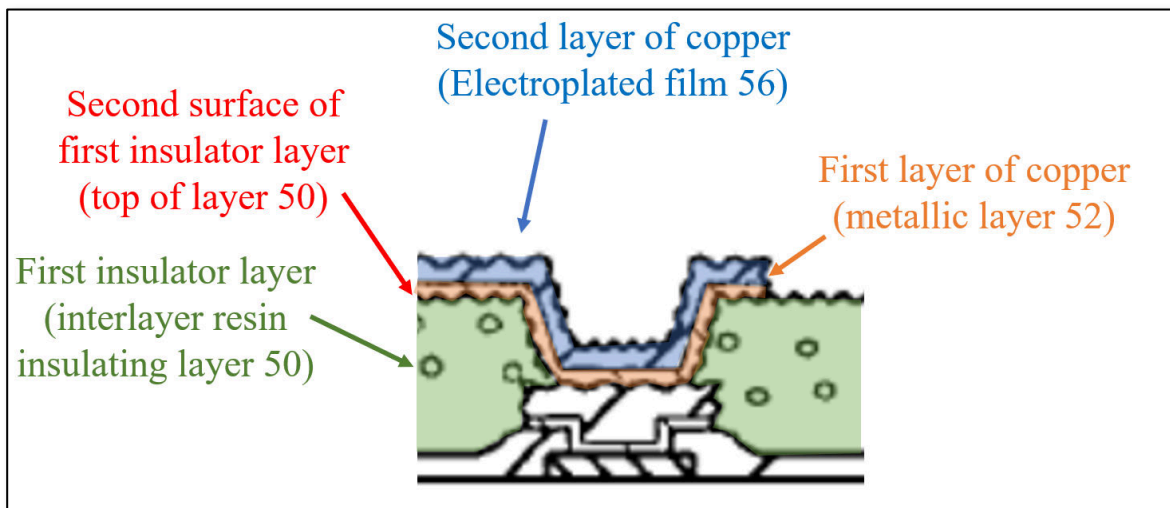
[9]:

“[M]etallic layer 52,” which is “*on the second surface of the first insulator layer*” (layer 50), along with the “electroplated film 56,” are applied as teaching the *conductors*. APPLE-1005, [0121]-[0124]; APPLE-1003, ¶124. *See* [1d]. Film 56 is on the surface of layer 52. APPLE-1005, FIG. 6; APPLE-1003, ¶124.

The electroplated film 56 is an electroplated **copper** layer, or “*second layer of copper*.” APPLE-1005, [0123]; APPLE-1003, ¶125. Layer 52 is a nickel-**copper**

layer that can be deposited by electroless plating, sputtering, or another method.

APPLE-1005, [0121]-[0122]; APPLE-1003, ¶125. Therefore, to the extent “*layer of copper*” is interpreted as “layer containing copper,” layer 52 is a “*first layer of copper*.”⁵



Portion of Sakamoto FIG. 4(C)

To the extent “*layer of copper*” is interpreted as referring to pure copper, it would have been obvious to form layer 52 out of copper instead of nickel-copper. APPLE-1003, ¶126. A POSITA would have recognized the function of layer 52 as a “seed layer” that is deposited to serve as a substrate for subsequent deposition of

⁵ Petitioner does not take a position on whether this claim requires a layer containing copper or a layer of pure copper. Rather, Petitioner provides invalidity positions under either interpretation. As such, resolution of this claim interpretation is not required for an invalidity determination here.

the electroplated film 56. APPLE-1005, [0122]-[0123]; APPLE-1003, ¶126. In view of this purpose of layer 52, it would have been obvious to make layer 52 a copper layer instead of a nickel-copper layer, because, as Dr. Subramanian explains, Sakamoto's disclosures with respect to layers 36, 37 teach that a copper layer can be an effective seed layer for subsequent electroplating, and it is *prima facie* obvious to substitute, for one component, another that the art has recognized as equivalent for the same purpose. *In re Ruff*, 256 F.2d 590, 592, 596 (C.C.P.A. 1958); APPLE-1003, ¶126-127. It would have been obvious to try substituting a copper layer for the nickel-copper layer 52, with copper being one of a finite number of identified, predictable materials for forming a layer by electroless plating or sputtering. APPLE-1005, [0111], [0121]-[0122]; APPLE-1003, ¶128-130.

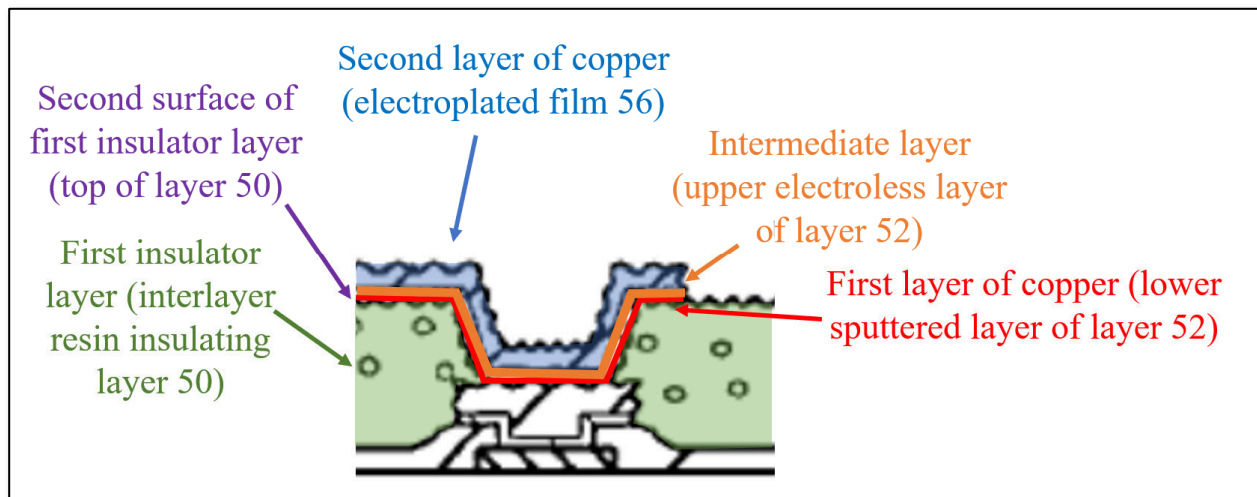
With layer 52 modified to be a layer of pure copper, claim 9 is satisfied even when "*layer of copper*" is interpreted to require pure copper. APPLE-1003, ¶131.

[10]:

"[M]etallic layer 52," which is on the second surface of the *first insulator layer* (layer 50), along with the "electroplated film 56," are applied as teaching the *conductors*. APPLE-1005, [0121]-[0124]; APPLE-1003, ¶132. *See* [1d].

Sakamoto describes that layer 52 can be formed by "form[ing] a thin layer by a physical method such as sputtering, deposition or electrode position and then

[] conduct[ing] electroless plating.” APPLE-1005, [0122]. Therefore, Sakamoto teaches that layer 52 can include a lower sputtered layer and an upper layer formed by electroless plating. APPLE-1003, ¶133. This arrangement is shown in annotated FIG. 4(C) below.



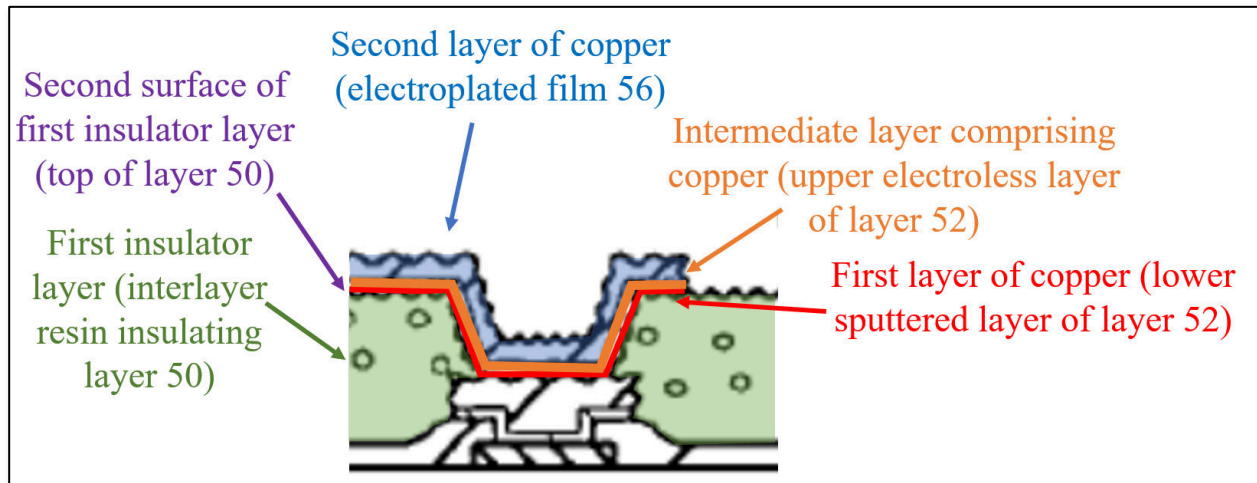
Portion of Sakamoto FIG. 4(C)

In this configuration, the lower sputtered layer of layer 52 (“*first layer of copper*”) is on the *second surface of the first insulator layer*; the upper electroless layer of layer 52 (“*intermediate layer*”) is on the surface of the *first layer of copper*; and the electroplated film 56 (“*second layer of copper*”) is on the surface of the *intermediate layer*. APPLE-1003, ¶134. The electroplated film 56 is **copper**. APPLE-1005, [0123]; APPLE-1003, ¶134. Also, layer 52 is a “Ni/**Cu**” layer, such that, to the extent “*layer of copper*” is interpreted as “layer containing copper,” the lower sputtered layer of layer 52 is a “*first layer of copper*” satisfying claim 10.

To the extent “layer of copper” is interpreted as referring to pure copper, it would have been obvious (for the reasons discussed for [9]) to form layer 52 (in this case, the lower sputtered layer and the upper layer formed by electroless plating) as a copper layer, thus rendering obvious forming the lower sputtered layer as a “*first layer of copper.*” APPLE-1003, ¶135.

[11]:

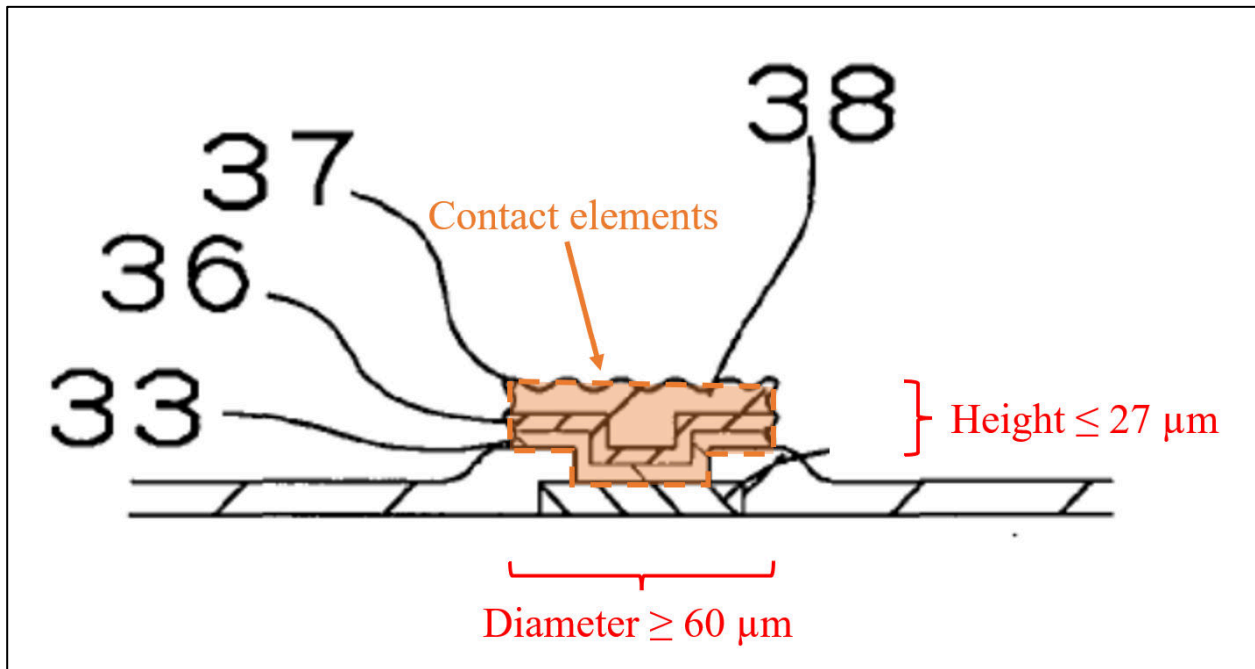
The upper layer of layer 52, formed by electroless plating, is an “*intermediate layer*” comprising “*copper grown by a chemical growing method or nickel grown by a chemical growing method.*” As discussed for [10], in the case where the metallic layer 52 includes a lower sputtered copper layer and an upper copper layer formed by electroless plating, the upper layer (*intermediate layer*) comprises copper. APPLE-1005, [0122]; APPLE-1003, ¶136. “Electroless plating” is described by the ’324 Patent as a “chemical growing method.” APPLE-1001, 2:56. As such, Sakamoto’s copper upper layer formed by electroless plating comprises “*copper grown by a chemical growing method.*” APPLE-1003, ¶137.



Portion of Sakamoto FIG. 4(C)

[13]:

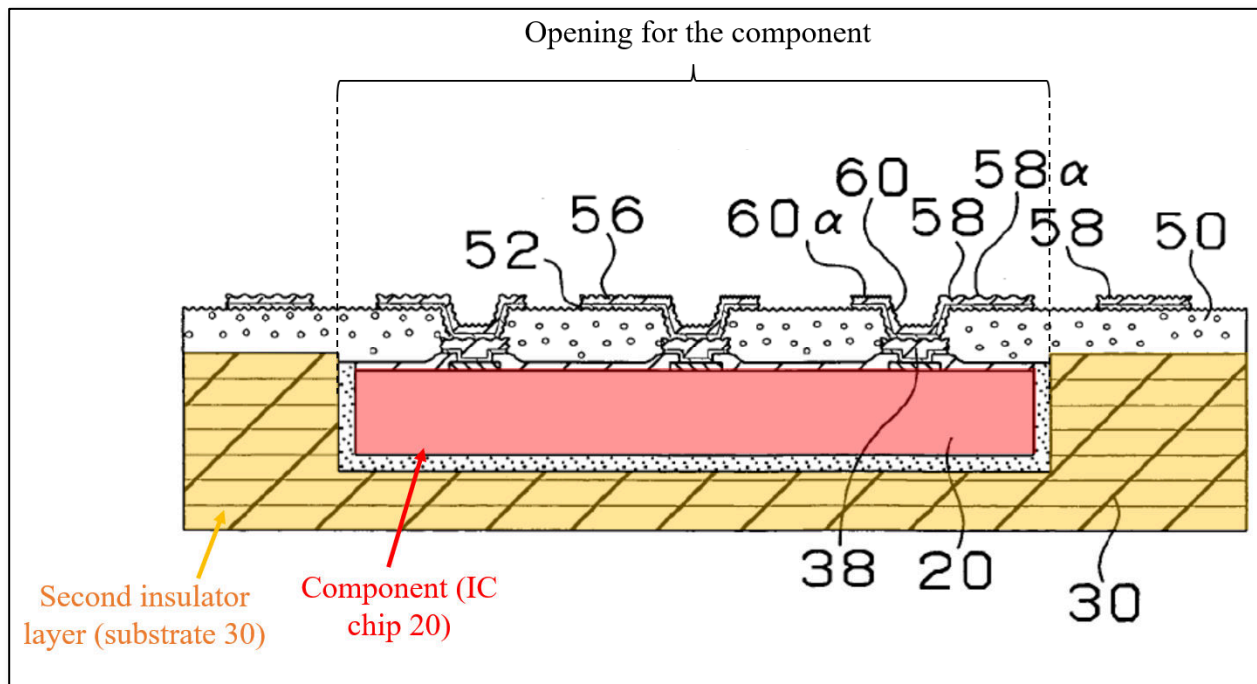
Layers 33, 36, and 37, forming the “*contact element*,” have a total height less than or equal to their greatest width. Sakamoto describes that layer 33 has a greatest thickness of 2.0 μm , that layer 36 has a greatest thickness of 5 μm , and that layer 37 has a greatest thickness of 20 μm . APPLE-1005, [0109], [0112], [0116]. Accordingly, the greatest thickness taught by Sakamoto for the “*contact element*” is 27 μm . APPLE-1003, ¶139. Sakamoto also describes that the transition layer 38 (layers 33, 36, and 37 together) has “a diameter of 60 μm or more.” APPLE-1005, [0119]. Because 60 μm (W_{MAX}) is greater than 27 μm (H), Sakamoto satisfies claim 13. APPLE-1003, ¶139.



Portion of Sakamoto FIG. 7(A)

[14]:

Substrate 30 is a “*second insulator layer*” satisfying claim 14. APPLE-1003, ¶140. The substrate 30 includes “prepregs each having a core material made of glass **cloths** or the like.” APPLE-1005, [0106]. The disclosure of “cloths” teaches the presence of “*at least one layer of fibre material*” in the substrate 30. APPLE-1003, ¶140. As shown below, the fibre material of the substrate 30 includes an opening for IC chip 20 (the “*at least one component*”). APPLE-1003, ¶141.

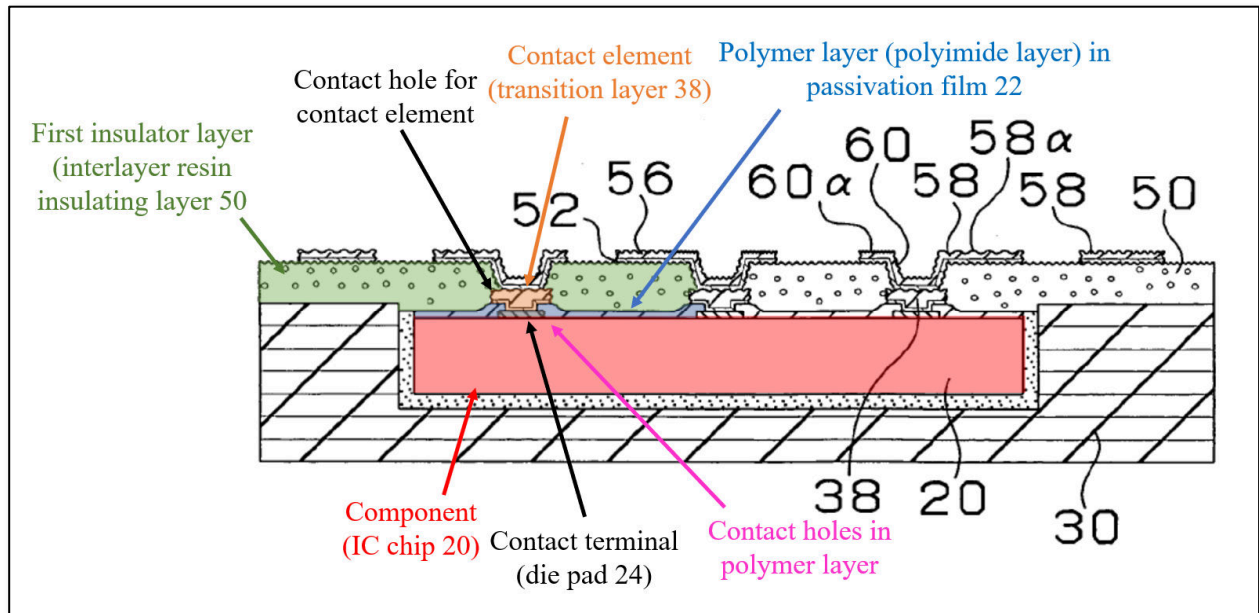


Sakamoto FIG. 4(C)

[15]:

Sakamoto's "polyimide layer" is a "*polymer layer*" satisfying claim 15. APPLE-1003, ¶142. Sakamoto's Background section assumes the presence of a "polyimide layer (or protective layer of the IC)" that is damaged by a laser if "the via diameter is larger than the diameter of the die pad." APPLE-1005, [0012]. As shown below, the polyimide layer 22 would be provided with the passivation film 22, in between layer 50 ("*first insulator layer*") and the IC chip 20 ("*at least one component*"). APPLE-1003, ¶142. The passivation film 22 includes contact holes for the transition layer 38 ("*contact elements*"). APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶142. As such, Sakamoto discloses the presence of a polyimide

layer (“*polymer layer*”) having the arrangement of the passivation film 22 and satisfying claim 15. APPLE-1003, ¶142.



Sakamoto FIG. 4(C)

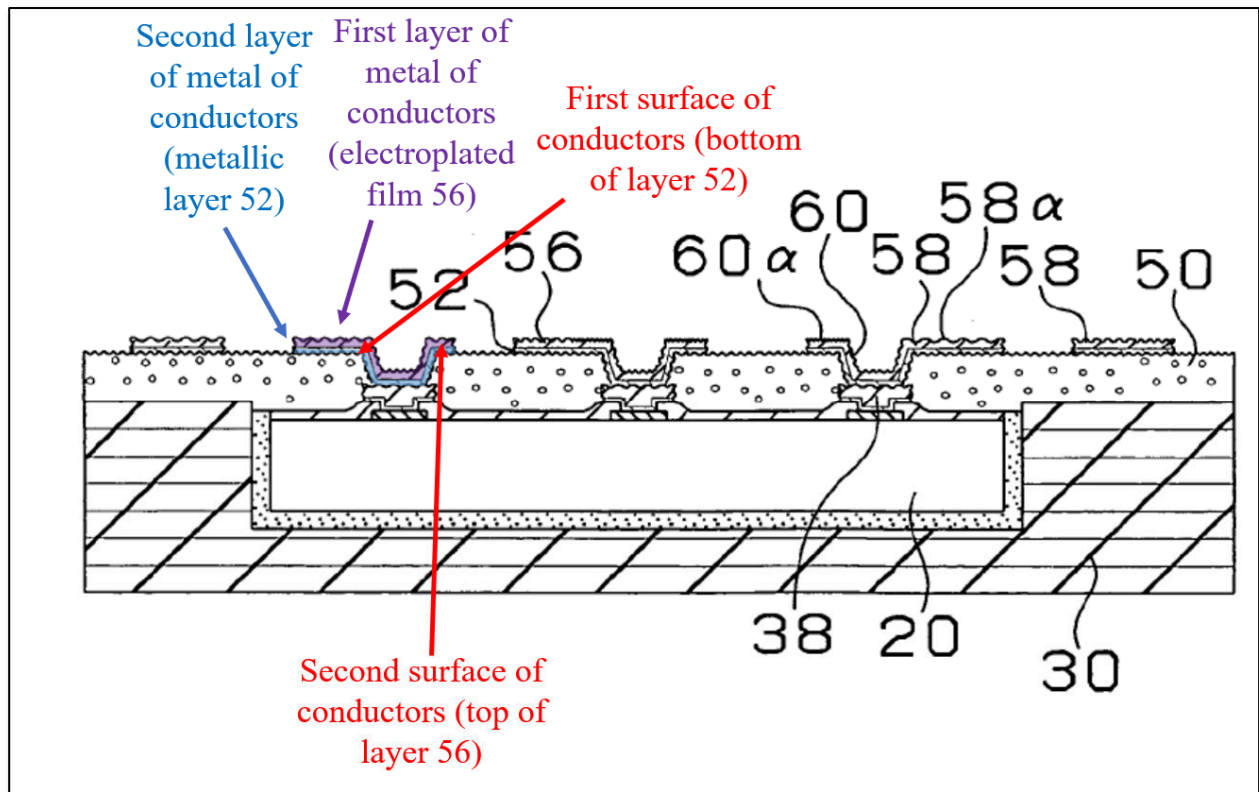
Further, in reference to a “third embodiment,” Sakamoto describes that “[t]he IC chip 420 is covered with an IC protective film (made of passivation+polyimide) 422.” APPLE-1005, [0202]. To the extent the polyimide is not already understood as being present, it would have been obvious to also include the polyimide (a polymer) in the passivation film 22 of the first embodiment in order to achieve the “protective” characteristics that Sakamoto describes are provided by a “polyimide layer,” satisfying claim 15. APPLE-1005, [0012]; APPLE-1003, ¶143.

[17pre]:

See [1pre].

[17a]:

See [1d]. Sakamoto’s “metallic layer 52” and “electroplated film 56,” together applied as “*a conductor layer*” and “*conductors*,” are “*two layers of metal*” between first and second surfaces, as shown below. APPLE-1005, [0121]-[0123]; APPLE-1003, ¶145.

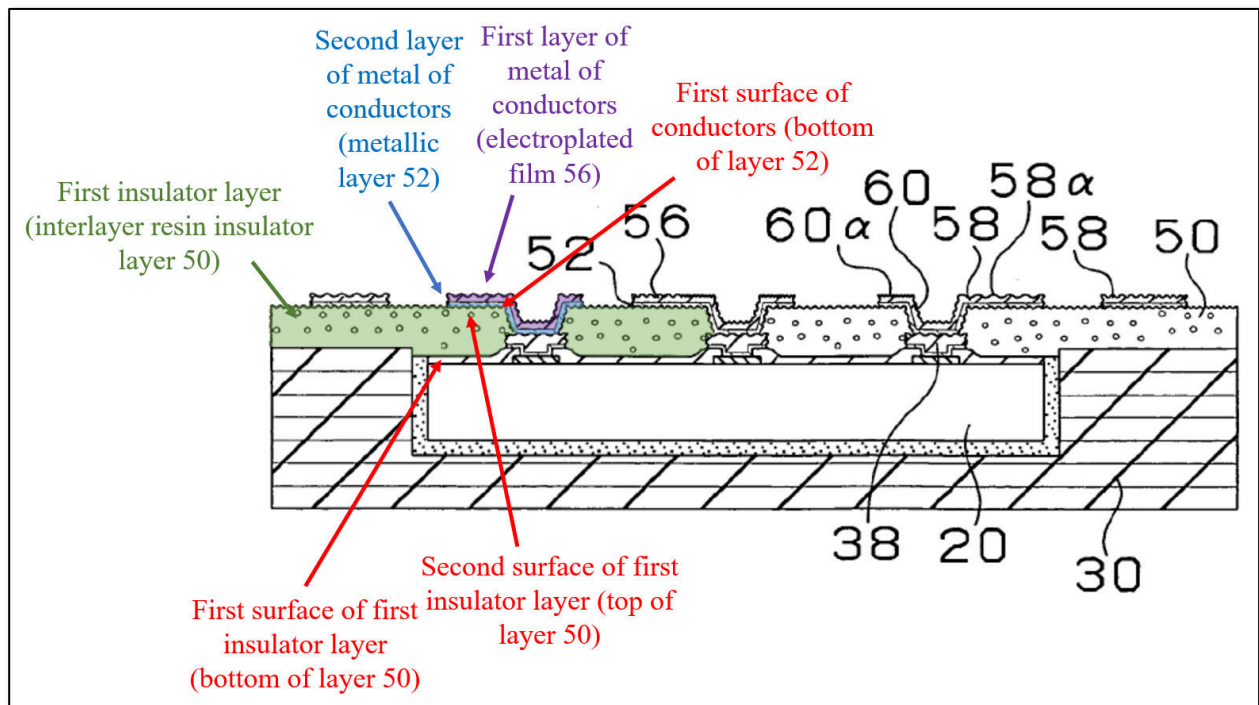


Sakamoto FIG. 4(C)

[17b]:

See [1a]. Sakamoto's interlayer resin insulation layer 50 is a “*first insulator layer*” having a first (bottom) surface and a second (top) surface covering the first

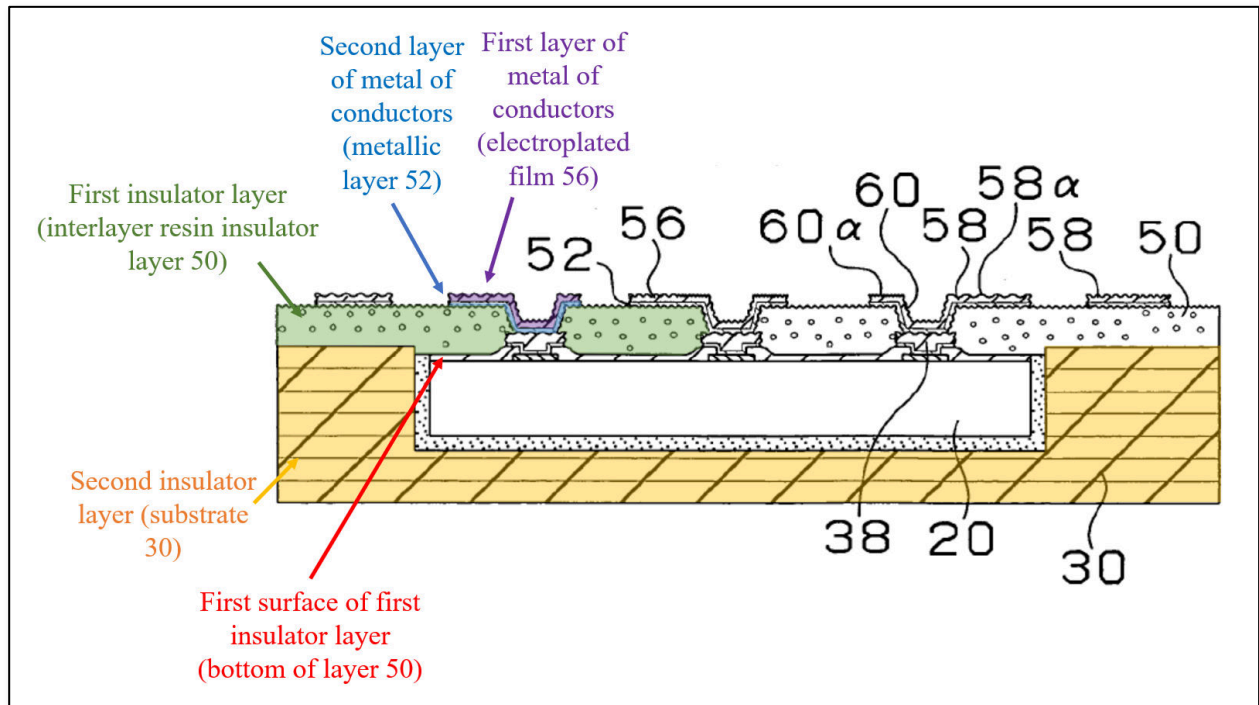
(bottom) surface of the conductors. APPLE-1003, ¶146.



Sakamoto FIG. 4(C)

[17c]:

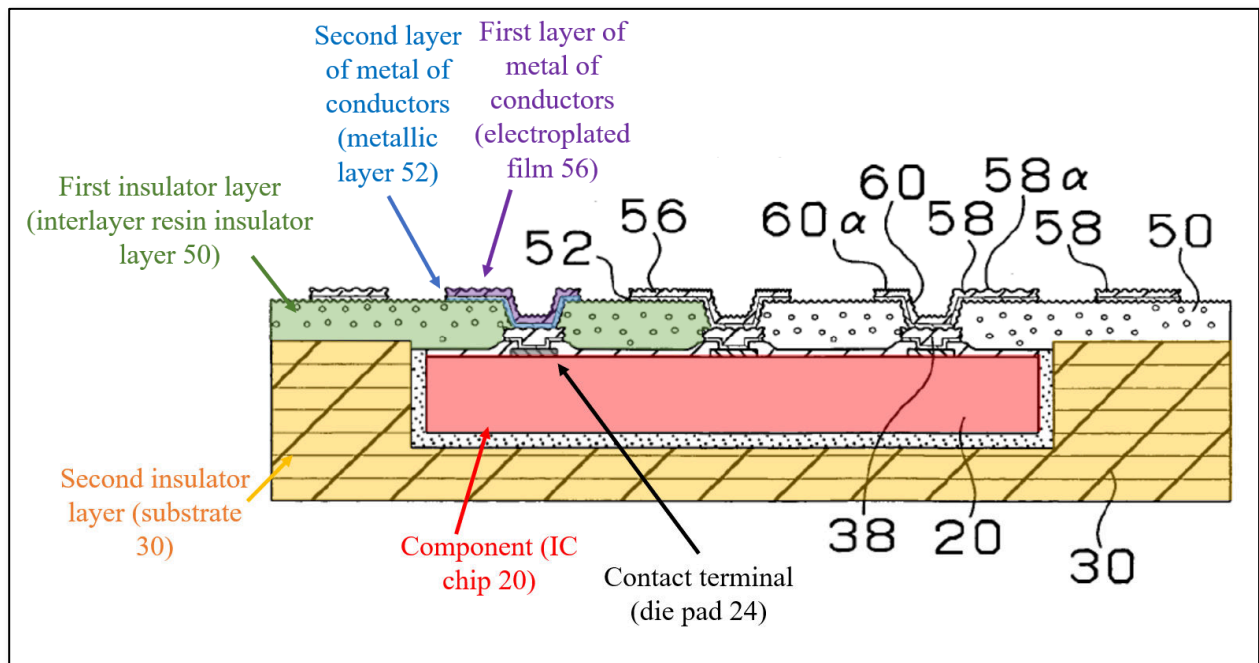
See [1b]. Sakamoto's substrate 30 is a "second insulator layer on the first surface of the first insulator layer." APPLE-1005, [0106]; APPLE-1003, ¶147.



Sakamoto FIG. 4(C)

[17d]:

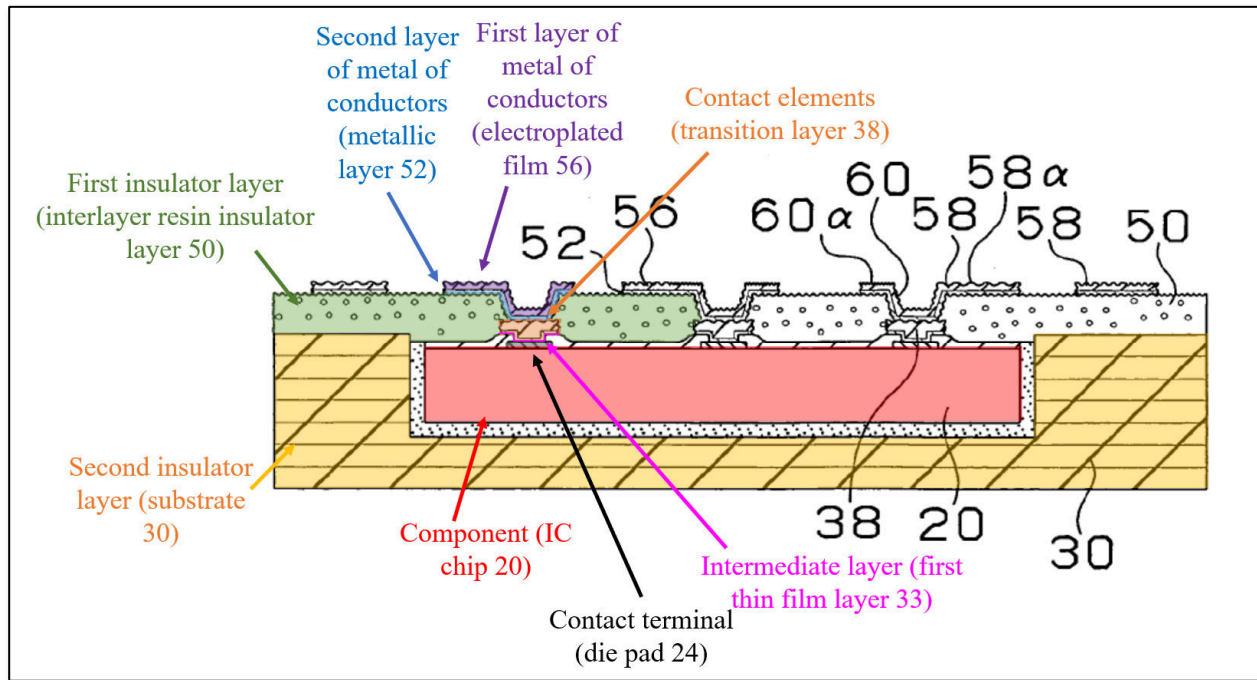
See [1c]. The “IC chip 20” is a “*component*” that is inside the “*second insulator layer*” (substrate 30). APPLE-1005, [0108], FIG. 6; APPLE-1003, ¶148. The IC chip 20 comprises “die pads 24,” which are contact terminals. APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶148. The die pads 24 are composed of aluminum and therefore contain “*at least one layer of metal.*” APPLE-1005, [0051], [0101]; APPLE-1003, ¶148.



Sakamoto FIG. 4(C)

[17e]:

See [1e]. Sakamoto's "transition layer 38," between the "contact terminals" (die pads 24) and the "conductors" (conductor circuits 58 including layer 52 and film 56), constitutes "contact elements." APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶149. The transition layer 38 includes an "intermediate layer" (layer 33) that contains at least one layer of metal, e.g., "tin, chromium, titanium, [], zinc, cobalt, [or] gold." APPLE-1005, [0109]-[0110]; APPLE-1003, ¶149.



Sakamoto FIG. 4(C)

[17f]:

See [1f]. A contact surface area between layer 33 (“*intermediate layer*”) and the die pad 24 (“*contact terminal*”) is less than a surface area of the die pad 24.

APPLE-1005, FIG. 6; APPLE-1003, ¶150.

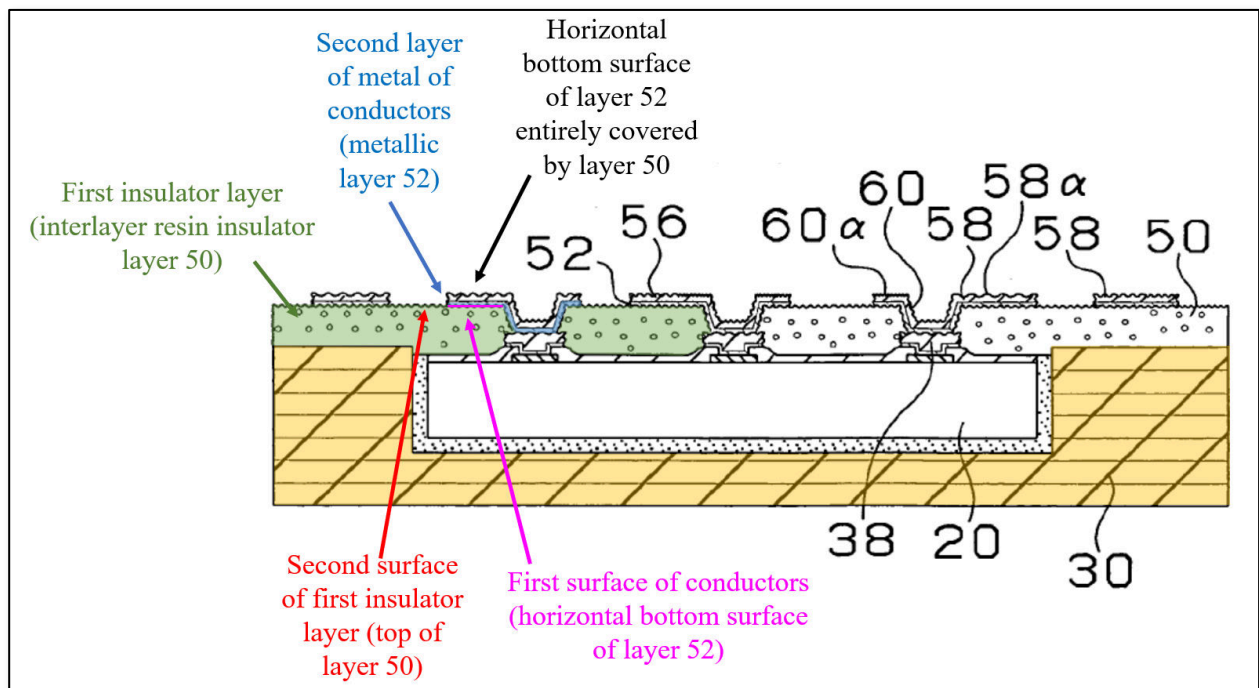
[17g]:

See [1c], [1d], and [1e]. Sakamoto’s die pads 24 (“*contact terminals*”) are composed of **aluminum**, a first metal; layer 52 (included in the “*conductors*”) is composed of **copper** and **nickel**, either of which is a second metal; and layer 33 (“*intermediate layer*”) can be composed of “**tin, chromium, titanium, [] zinc, cobalt, [or] gold.**” APPLE-1005, [0051], [0101], [0109]-[0110], [0123]; APPLE-

1003, ¶151.

[19]:

See claims 1 and 17 above. Claim 19 is identical to claim 17 except for (1) omitting recitation of the first, second, and third metals and (2) reciting “*the second surface of the first insulator layer entirely covering the first surface of the conductors.*” The latter element is satisfied by the top surface of layer 50 (“*first insulator layer*”) entirely covering the bottom horizontal surface of layer 52, the bottom horizontal surface being the “*first surface of the conductors.*” APPLE-1005, FIG. 6; APPLE-1003, ¶152.



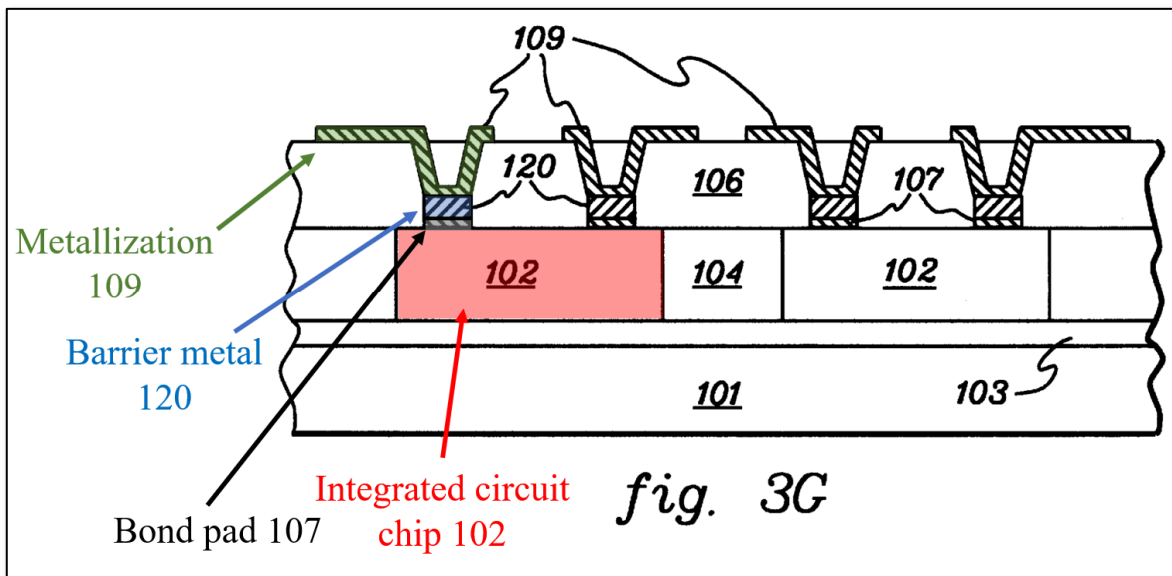
Sakamoto FIG. 4(C)

V. GROUND 1B: Claims 3 and 9-11 are obvious over Sakamoto and Eichelberger

A. Eichelberger

Eichelberger (US 6,396,148) is discussed in the Background of the '324 Patent. APPLE-1001, 2:51-65. Eichelberger describes “first packaging structures and methods of fabrication” that employ “electroless metallizations.” APPLE-1006, Abstract; APPLE-1003, ¶72. For example, Eichelberger describes that an “electroless metal coating” (a “barrier”) can be plated on aluminum contact pads to improve connection reliability and protect against “chemical attack” and corrosion. APPLE-1006, 4:44-61; APPLE-1003, ¶72. Eichelberger discusses that “[c]ertain GaAs IC chips have gold pads” and that “the process described herein will also work with these types of bond pads.” APPLE-1006, 9:40-58.

Eichelberger’s FIG. 3G, reproduced below, shows a similar configuration to that of Sakamoto, including an IC chip 102, a bond pad 107 on the IC chip 102, and multiple metal layers 120, 109 on the bond pad 107. APPLE-1006, 4:9-22, 8:10-13; APPLE-1003, ¶73.



Eichelberger FIG. 3G

Eichelberger is analogous art to the '324 Patent. APPLE-1003, ¶74. Both address the challenges of contacting aluminum bond pads. *See* APPLE-1001, 1:64-2:65, 3:47-63; APPLE-1006, 1:22-26, 2:24-29. Indeed, Eichelberger was recognized as relevant in the Background of the '324 Patent. APPLE-1001, 2:51-65.

B. Analysis of Claims

[3]:

Given Eichelberger, it would have been obvious to have the die pad 24 include gold (instead of or in addition to aluminum), such that the “*first metal*” is gold. APPLE-1003, ¶154. Eichelberger describes that “[c]ertain GaAs IC chips have **gold pads**.” APPLE-1006, 9:42-43. In at least the case where the IC chip 20 of Sakamoto is a GaAs IC chip, it would have been obvious to form the die pad 24

as a gold pad, based on Eichelberger's description that GaAs IC chips have gold pads. APPLE-1006, 9:42-43; APPLE-1005, ¶155-156.

Causing the die pad 24 to contain gold would simply be a selection of one of a finite number of identified, predictable materials for die pads. APPLE-1005, [0051], [0101]; APPLE-1006, 9:38-59; APPLE-1003, ¶156. Indeed, Sakamoto describes that gold may be integrated elsewhere in Sakamoto's circuit board (e.g., as layer 33 or 36), such that the use of gold for the die pad 24 would not constitute the introduction of an entirely new material. APPLE-1005, [0109]-[0111]; APPLE-1003, ¶157.

Further, a POSITA would have been motivated by specific advantages provided by gold. APPLE-1003, ¶158. For example, Sakamoto describes that the oxidation of aluminum pads "causes an increase in the connection resistance of the pad," and a POSITA, based on the common knowledge that gold is resistant to oxidation, would have found it obvious to try using gold to achieve lower connection resistance. APPLE-1005, [0051]; APPLE-1003, ¶158. Indeed, gold was widely known as an effective material to include as, or as part of, contact terminals, providing corrosion resistance and high electrical and thermal conductivity. APPLE-1007, 1; APPLE-1003, ¶158. It would have been obvious for a POSITA to try to realize these well-known advantages by having the die pad 24 contain gold, e.g., as an entirety of the die pad 24 or as a deposited layer of the die

pad 24. APPLE-1003, ¶157-159.

Accordingly, having the die pad 24 contain **gold** as the “*first metal*,” layer 52 contain **copper** as the “*second metal*” (APPLE-1005, [0121]-[0122]), and layer 33 contain **nickel** as the “*third metal*” (APPLE-1005, [0109]) would have been obvious. APPLE-1003, ¶160.

[9]:

Claim 9, besides being taught by Sakamoto, is also obvious over Sakamoto and Eichelberger. APPLE-1003, ¶161. The “Cu/Ni” layer 52 serves as a seed layer for subsequent electroplating of the copper film 56, and the arguments for Ground 1A describe why, in the case where “*layer of copper*” is interpreted as requiring pure copper, it would have been obvious to modify the copper-nickel layer 52 to be pure copper. APPLE-1003, ¶161.

Eichelberger reinforces the obviousness of this modification by directly disclosing the use of an “electroless” “**copper** seed layer 109’ deposited over polymer surface 106.” APPLE-1006, 8:10-11, 8:22; APPLE-1003, ¶162. This is similar to Sakamoto’s layer 52, which is deposited by electroless plating over the surface of the interlayer resin insulating layer 50. APPLE-1005, [0121]; APPLE-1003, ¶162. Layer 109 is then “plated up” on the seed layer 109’, matching Sakamoto’s description that an electroplated copper film 56 is formed on layer 52. APPLE-1006, 8:16-25; APPLE-1005, [0123]; APPLE-1003, ¶162.

Given Eichelberger's corroborating description, it would have been obvious to make the metallic layer 52 and the electroplated film 56 first and second layers of copper, respectively. APPLE-1003, ¶163.

[10]:

See [9] and [10] for Ground 1A and [9] for Ground 1B. For the reasons provided for [9] for Ground 1B, Eichelberger reinforces the obviousness of forming a lower sputtered layer of the metallic layer 52 as a copper layer to be the "*first layer of copper*" and forming an upper layer of the metallic layer 52 as a copper layer to be the "*intermediate layer*," in the case where "*layer of copper*" is interpreted as requiring pure copper. APPLE-1005, [0122], FIG. 6; APPLE-1003, ¶164. The electroplated film 56 is a "*second layer of copper on the surface of the intermediate layer*." APPLE-1005, [0123], FIG. 6; APPLE-1003, ¶164.

[11]:

See [9]-[10] for Grounds 1A and 1B. The upper layer of layer 52, formed by "electroless plating," is an "*intermediate layer*" "*grown by a chemical growing method*" and arranged as recited in claim 11. APPLE-1005, [0122], FIG. 6; APPLE-1003, ¶165. For the reasons provided for [9] for Ground 1B, Eichelberger reinforces the obviousness of having this upper layer be pure copper, in the case where "*layer of copper*" is interpreted as requiring pure copper. APPLE-1003, ¶165-166.

VI. GROUND 1C: Claims 9-11 are obvious over Sakamoto and Chang

A. Chang

Chang is a journal article relating to a “low-temperature integrated electrochemical deposition process for next-generation Cu metallization.” APPLE-1008, 1; APPLE-1003, ¶75. Chang describes a process by which “thin, smooth, conformal Cu seed layers” are used as seed layers for “subsequent electroplating [of copper] to accomplish Cu metallization with good quality.” APPLE-1008, 1-2; APPLE-1003, ¶75-76.

Chang is analogous art to the '324 Patent. APPLE-1003, ¶77. Many embodiments in the '324 Patent, along with claim 11, relate to forming copper layers by electroless plating, and Chang provides experimental methods for the “electroless plating of thin, smooth, conformal Cu seed layers.” APPLE-1001, 17:40-18:7, 19:41-61; APPLE-1008, 1; APPLE-1003, ¶77.

B. Sakamoto-Chang Combination

Chang provides further evidence that, as discussed for [9]-[11] for Grounds 1A-1B, it would have been obvious to make Sakamoto's layer 52 a copper layer rather than a copper-nickel layer, in the case where “*layer of copper*” is interpreted as requiring pure copper. APPLE-1003, ¶168. As discussed for [9] for Ground 1A, the copper-nickel layer 52 functions as a seed layer to permit the subsequent electroplating of film 56. APPLE-1003, ¶168. However, Chang demonstrates that

the use of **copper** seed layers results in “**smooth surfaces** of [subsequently] electrodeposited [electroplated] Cu films” analogous to electroplated film 56 deposited on layer 52. APPLE-1005, [0121]; APPLE-1008, 5; APPLE-1003, ¶168. These electrodeposited Cu films exhibited “high purity, small roughness, low electrical resistivity, low residual stresses, good adhesion to substrates, and excellent superfilling.” APPLE-1008, 7.

As explained further by Dr. Subramanian, it would have been obvious for a POSITA to substitute a pure copper layer for the copper-nickel layer 52, given copper’s recognized suitability for the function of seed layer and the advantages described by Chang. APPLE-1003, ¶169-171.

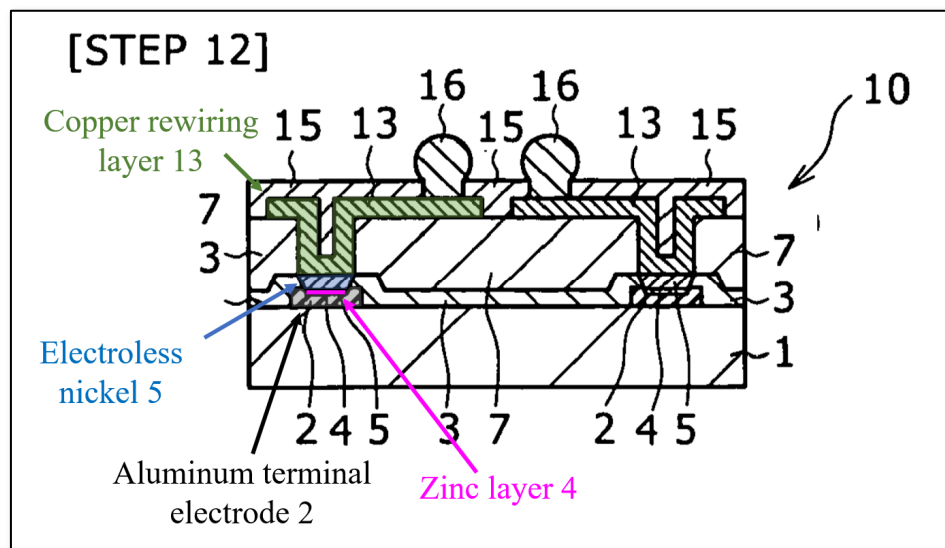
C. Analysis of Claims

[9], [10], [11]: *See* corresponding discussion of claims 9-11 for Ground 1B. For the reasons provided there and in Section VI.B, Chang further evidences the obviousness of making the metallic layer 52 a “*first layer of [pure] copper,*” including, in the case of claim 11, making the lower sputtered layer and upper electroless layer of layer 52 layers of copper. APPLE-1003, ¶172. The reasoning is otherwise identical to that provided for claims 9-11 for Grounds 1A and 1B. APPLE-1003, ¶172.

VII. GROUND 1D: Claims 12, 13, and 15 are obvious over Sakamoto and Ito

A. Ito

Ito describes the manufacture of a “stacked multilayer” contact in which a “metal layer is self-alignedly formed relative to the terminal electrode. This does not need any patterning step thereby forming the contact portion simply and reliably.” APPLE-1012, [0062]; APPLE-1003, ¶78. FIG. 2L of Ito illustrates a structure including an aluminum terminal electrode 2; a zinc layer 4 formed by zincating on the aluminum terminal electrode 2; an electroless-plated nickel layer 5 on the zinc layer 4; and a copper rewiring layer 13 on the nickel layer 5. APPLE-1012, [0082], [0089], [0091], [0094]-[0096]. APPLE-1003, ¶78.



Ito FIG. 2L

Ito is analogous art to the '324 Patent. APPLE-1003, ¶79. Both are directed to contact structures used in conjunction with copper foil-attached insulating resin sheets and disclose that zincation of aluminum contacts, after which electroless

nickel is deposited, represents a solution to challenging in contact aluminum.

APPLE-1001,3:55-4:5, 5:6-46, 17:40-51; APPLE-1012, [0063], [0065], [0073], [0093]; APPLE-1003, ¶79.

B. Zincating

Dr. Subramanian provides an overview of zincating. APPLE-1003, ¶54-55. He describes that “zincating (or zincation) is a ‘widely used process’ for aluminum contact pads. [] ‘Aluminum [] is the dominant material for IC bond pad metallization. [] However, as aluminum instantaneously oxidizes during rinsing or exposure to air, the oxide films will completely suppress metallization or prevent the formation of intermetallic bonds between the EN [electroless nickel] and substrate, resulting in adhesion failure. Zincating of the aluminum pads is a widely used process step that activates the pads for subsequent EN deposition.’ [] ‘Zincation rel[ies] on the electrochemical exchange reaction between zinc ion in solution and aluminum metal to deposit zinc metal at the expense of aluminum dissolution []. Zincation is currently one of the most suitable processes to activate the aluminum surface for electroless technique []. Once this process is performed, aluminum coated with zinc then can be electroless plated by nickel.’ [] This is an ‘essential step to make aluminum pads actives [sic] for subsequent electroless nickel plating.’ [] As a result, a zincated aluminum terminal electrode includes a ‘contact portion’ composed of a ‘zinc layer’ ‘about 0.3 μm ’ thick at the top of the

aluminum electrode.” APPLE-1003, 54.

C. Analysis of Claims

[12]:

It would have been obvious to replace Sakamoto’s first thin film layer 33 with Ito’s zincated zinc layer 4, on Sakamoto’s die pad 24, such that a width of the contact surface between the zinc layer 4 (the “*contact element*”) and the die pad 24 (“*contact terminal*”) is 0-20% less than a greatest width of the zinc layer 4.

APPLE-1003, ¶174.

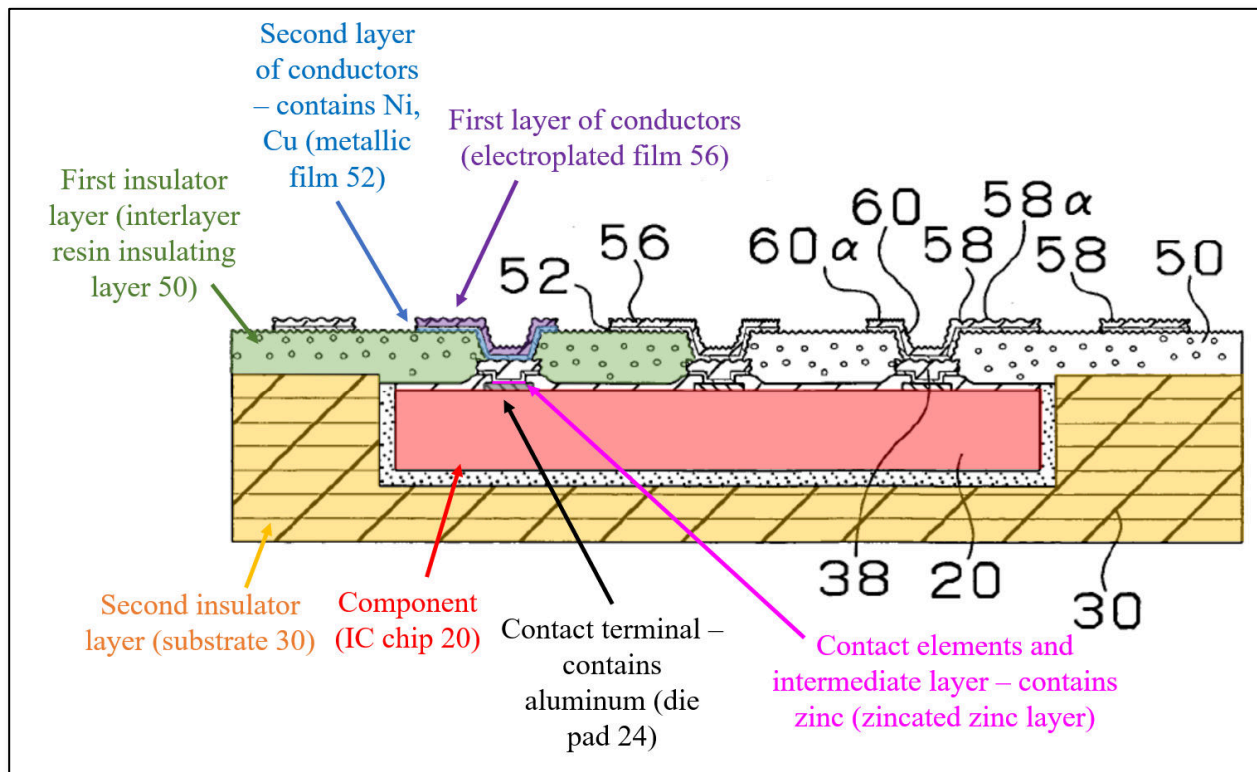
This modification would have been obvious for several reasons. Zincating was a widely-used, conventional first step for forming contact stacks on aluminum pads. APPLE-1003, ¶175. *See* §VII.B. As a POSITA would have recognized, the zinc layer would prevent oxidation of the aluminum die pad 24 and provide a surface for subsequent electroless deposition of the second thin film layer 36. APPLE-1003, ¶175. Indeed, Sakamoto recognizes that oxidation of the aluminum die pad 24 may be problematic. APPLE-1005, [0200], [0206]; APPLE-1003, ¶175. Given Ito’s disclosure that “oxide on the aluminium surface is removed by zincating to form the zinc layer 4,” it would have been obvious for a POSITA to form the zinc layer to remove the oxide film and obtain lower resistances. APPLE-1012, [0093]; APPLE-1003, ¶175.

Further, the zinc layer 4 would be a close structural and functional substitute

for the first thin film layer 33. APPLE-1003, ¶176. The two layers have similar thicknesses (0.3 μm for the zinc layer 4, within the “0.01 to 1.0 μm ” range of layer 33), can both be composed of zinc, are both described as providing improved adhesion to the underlying pad, and are both subsequently covered by a layer that can be electroless nickel. APPLE-1005, [0109]-[0111]; APPLE-1012, [0082], [0091], [0095]; APPLE-1003, ¶176. As such, the simple substitution of the zinc layer 4 for layer 33 would have been obvious. APPLE-1003, ¶17177.

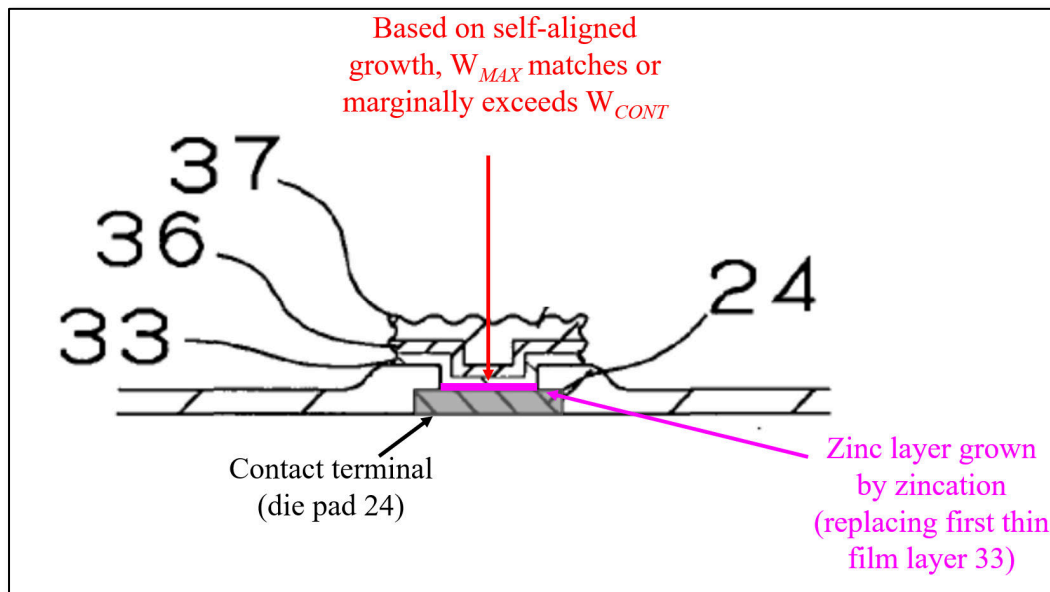
In this modified Sakamoto-Ito circuit board, the zinc layer constitutes the “contact elements” and the “intermediate layer.” APPLE-1003, ¶178. Mappings of the modified Sakamoto-Ito circuit board to the elements of claims 1 and 12, shown in annotated figure and table below, are otherwise identical to those discussed for claim 1 in Ground 1A.

First metal (of die pads 24)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none">• Metallic layer 52 (<i>second layer</i>), and• Electroplated film 56 (<i>first layer</i>)	Cu or Ni	<ul style="list-style-type: none">• Zinc layer 4 (<i>intermediate layer</i>)	Zn



Sakamoto-Ito circuit board based on Sakamoto FIG. 4(C)

Because of the “self-aligned” nature of the zinc growth directly on the aluminum die pad 24 “so that no patterning step is needed,” a width of the contact surface between the zinc layer (*contact elements*) and the die pad 24 (*contact terminal*) is 0-20% less than a greatest width of the zinc layer in the same direction, satisfying claim 11. APPLE-1012, [0096], APPLE-1003, ¶179. That is, the width of the contact surface is substantially equal to (or 0% less than) the greatest width of the zinc layer. APPLE-1003, ¶179.



Sakamoto FIG. 7(A)

[13]:

The zinc layer of the Sakamoto-Ito device – applied as the “*contact element*” as for [12] – has a height $H = “0.3 \mu\text{m}.”$ APPLE- 1012, [0091]. This height is significantly less than the contact element (width of the zinc layer), which is approximately $30 \mu\text{m}$ based on Ito’s opening diameter. APPLE-1012, [0106]; APPLE-1003, ¶180.

[15]:

It would have been obvious to use Ito’s “first passivation layer 101” as, or in, Sakamoto’s “passivation film 22,” such that the first passivation layer 101 is a “*polymer layer*” between the “*first insulator layer*” (layer 50) and the “*component*” (IC chip 20) and includes contact holes for the “*contact elements*” (die pads 24).

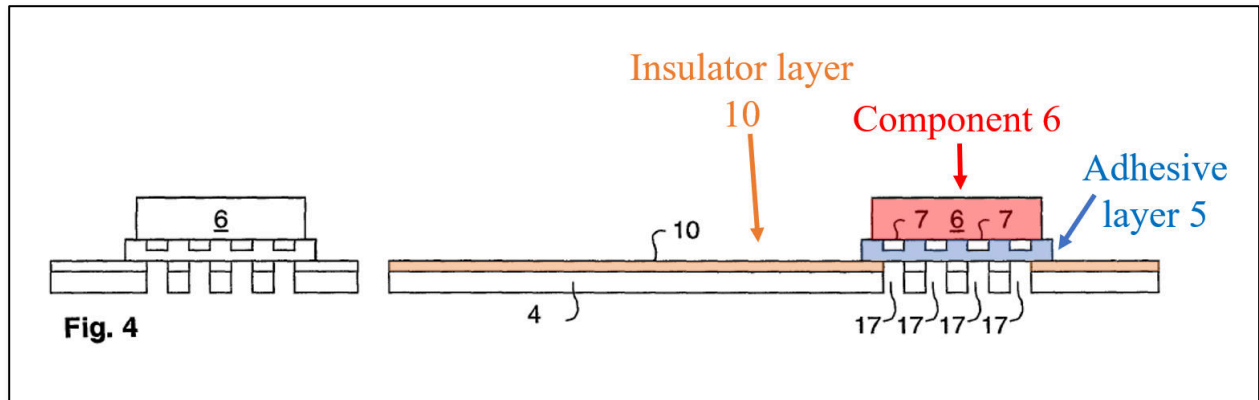
APPLE-1005, FIG. 6; APPLE-1003, ¶181. Ito discloses that a “first passivation layer 101 includes a benzocyclobutene (BCB) resin or a polyimide resin,” both polymers. APPLE-1012, [0010]; APPLE-1003, ¶181. Given Ito’s disclosure that these materials can be used for a “passivation layer,” it would have been obvious to use a layer of one of these polymer materials as, or in, Sakamoto’s “passivation film,” thereby satisfying claim 15. APPLE-1003, ¶182. The obviousness is reinforced by Sakamoto’s explicit disclosure that the passivation film 422 of another embodiment includes “polyimide.” APPLE-1005, [0202]; APPLE-1003, ¶182. It is well-established that selection of a known material based on its suitability for its intended use is *prima facie* obvious. *See, e.g., In re Leshin*, 277 F.2d 197, 125 U.S.P.Q. 416 (C.C.P.A. 1960); *Sinclair Co. v. Interchemical Corp.*, 325 U.S. 327, 335 (1945).

VIII. GROUND 1E: Claims 15-16, 18, and 20 are obvious over Sakamoto and Tuominen

A. Tuominen

Tuominen, which shares two inventors with the ’324 Patent, is directed to “components [] embedded in an installation base and connection to a conductor-pattern structure.” APPLE-1014, 1:5-7; APPLE-1003, ¶80. FIG. 4 illustrates a configuration in which “an adhesive layer 5 is spread on the attachment surface of the insulating layer 10” to attach a component 6 to the insulator layer 10. APPLE-

1014, 6:20-25; APPLE-1003, ¶80.



Tuominen FIG. 4

Tuominen is analogous art to the '324 Patent. APPLE-1003, ¶81. Besides sharing inventors, both relate to similar modules in which a copper foil-based membrane is attached to components that are contacted through contact openings. APPLE-1003, ¶81.

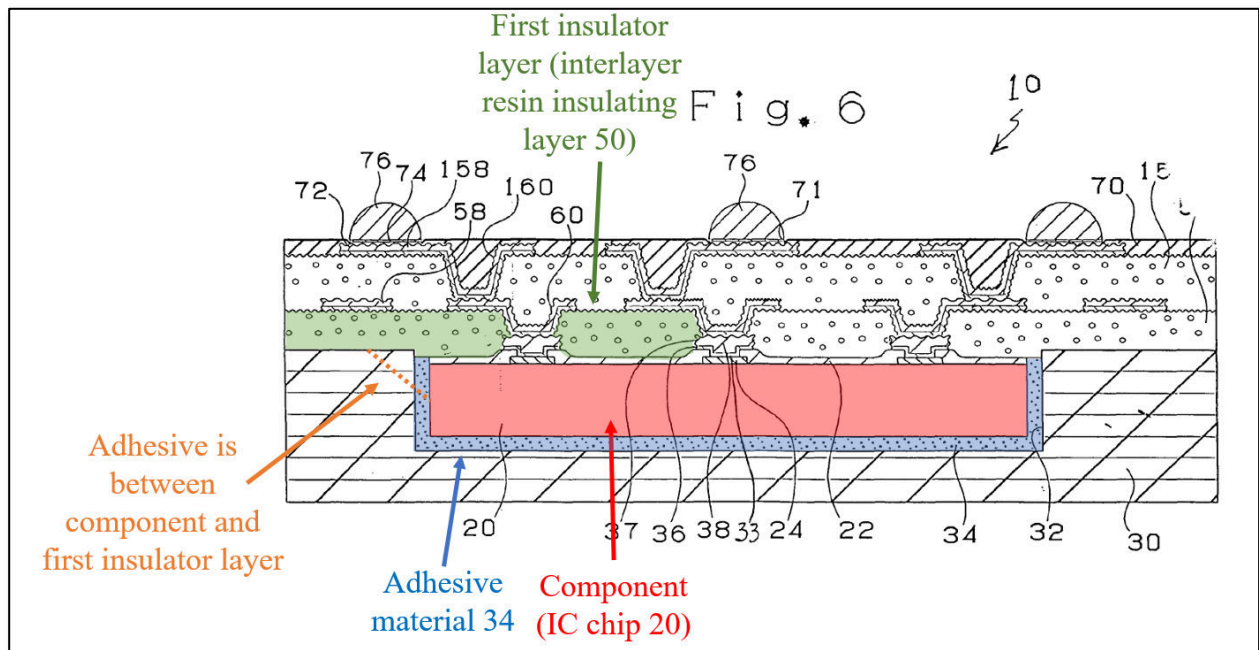
B. Analysis of Claims

[15], [16]:

It would have been obvious to introduce Tuominen's "adhesive 5" in-between Sakamoto's layer 50 and IC chip 20 to attach the layer 50 (which is "vacuum-compression laminated onto the substrate") to the IC chip 20. It would have been obvious to have the adhesive 5 be hardened to better secure the layer to the IC chip 20. APPLE-1003, ¶184. *See* [15]-[16] in Ground 2E.

[18]:

In view of Tuominen, it would have been obvious to harden Sakamoto's "adhesive material 34," thereby satisfying claim 18. As shown below, Sakamoto's "adhesive material 34" is between layer 50 ("first insulator layer") and IC chip 20 ("component"). APPLE-1005, [0106], FIG. 6; APPLE-1003, ¶185.



Sakamoto FIG. 6

Tuominen defines that "[t]he term **adhesive** refers to a material, by means of which the components are attached to the insulator layer 10. [] Another property of the adhesive is that after spreading **the adhesive hardens or can be hardened at least partly, in such a way that the adhesive can hold the component in place.**" APPLE-1014, 7:18-24. Given this disclosure, it would have been obvious to have the adhesive material 34 be "*hardened*," in order to securely "hold" the IC chip 20

to the substrate 30 as taught by Tuominen. APPLE-1003, ¶186.

[20]: See [18].

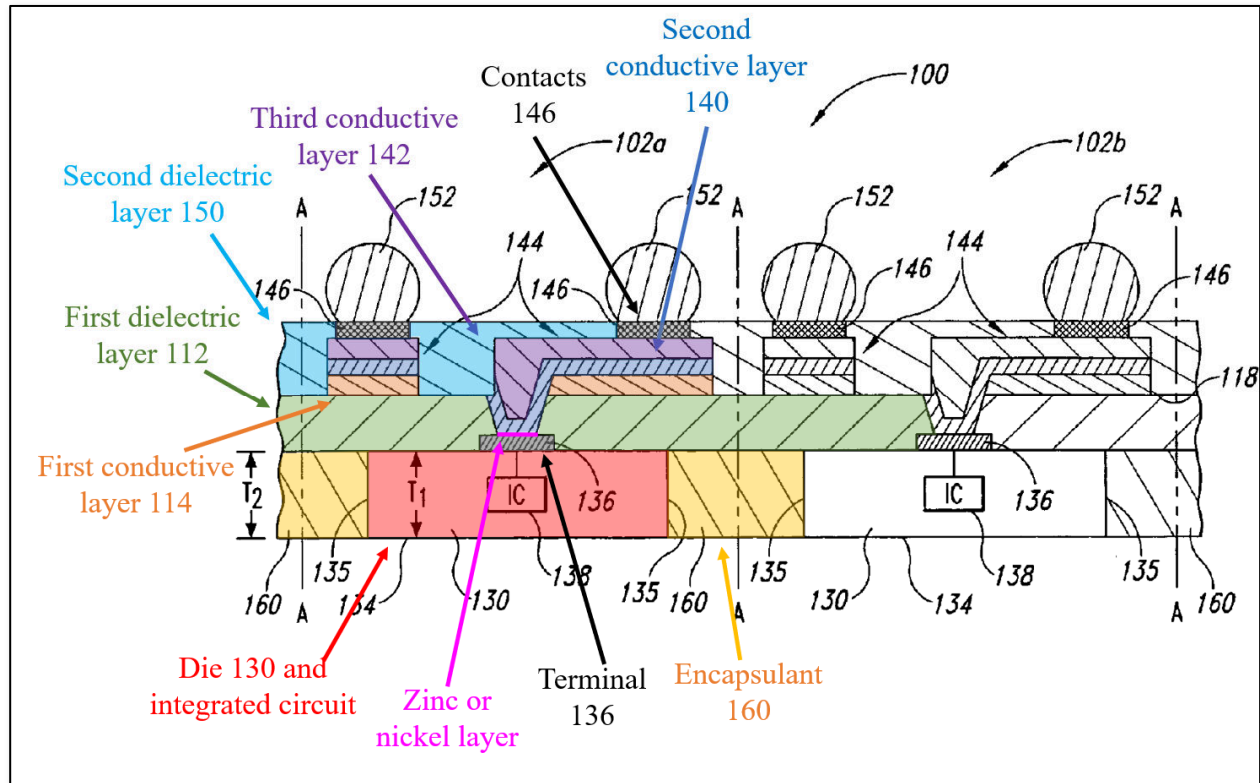
IX. GROUNDS 2A, 2B: Claims 1-2, 4, 6-8, 10-12, and 15-20 are obvious over Lee or Lee and Sakamoto

A. Lee

Lee is directed to microelectronic devices and manufacturing methods that offer improved yield and throughput. APPLE-1015, [0035]; APPLE-1003, ¶82. Like the '324 Patent's, Lee's devices are formed based on a copper foil "first conductive layer 114." APPLE-1015, [0026]; APPLE-1003, ¶82. A contact structure, including a second conductive layer 140, a third conductive layer 142, and contacts 146, is fabricated on terminals 136 of a die 130 exposed in holes in layer 114 and an attached dielectric layer 112. APPLE-1015, [0029]-[0032], FIGS. 1B-1E; APPLE-1003, ¶82. In cases in which "the terminals 136 do not have a surface compatible with electroless plating, additional processes such as zincation, sputtering, and/or plating may be necessary to deposit a compatible conductive protective layer (e.g., a nickel layer) on the terminals 136 before depositing the second conductive layer 140." APPLE-1015, [0030]. As a result, a zinc layer ("zincation") or a "nickel layer" can be provided between the terminals 136 and the second conductive layer 140. APPLE-1003, ¶83.

The resulting structure, with dies 130 encased in an encapsulant 160 and a

second dielectric layer 150 provided on the first dielectric layer 112, is annotated below. APPLE-1015, [0033], FIG. 1E; APPLE-1003, ¶84.



Lee FIG. 1E

Lee is analogous art to the '324 Patent. APPLE-1003, ¶85. Both are in the same field of endeavor of IC manufacture and structure and address the problem of how to contact an IC chip attached to a copper foil by an insulating layer. APPLE-1003, ¶85. Further, both the '324 Patent and Lee address how contact holes can be dimensioned to improve alignment between contact pads and subsequent layers, arriving at the same solution of making the contact area less than the total pad area. APPLE-1003, ¶85.

B. Lee-Sakamoto Combination

In this section, Sakamoto is applied to corroborate the metals of several layers for which Lee does not explicitly disclose a composition. Lee lacks explicit disclosure that the terminals 136 are aluminum, that the second conductive layer 140 is nickel (for claims 7 and 11), or that the third conductive layer 142 is copper (for claims 8 and 10-11), although these compositions are implicitly disclosed or obvious. APPLE-1003, ¶189. Sakamoto provides explicit teaching and motivation for the use of aluminum, nickel, and copper, respectively, for those elements.

Sakamoto is applied in combination with Lee for several other teachings in Section X.

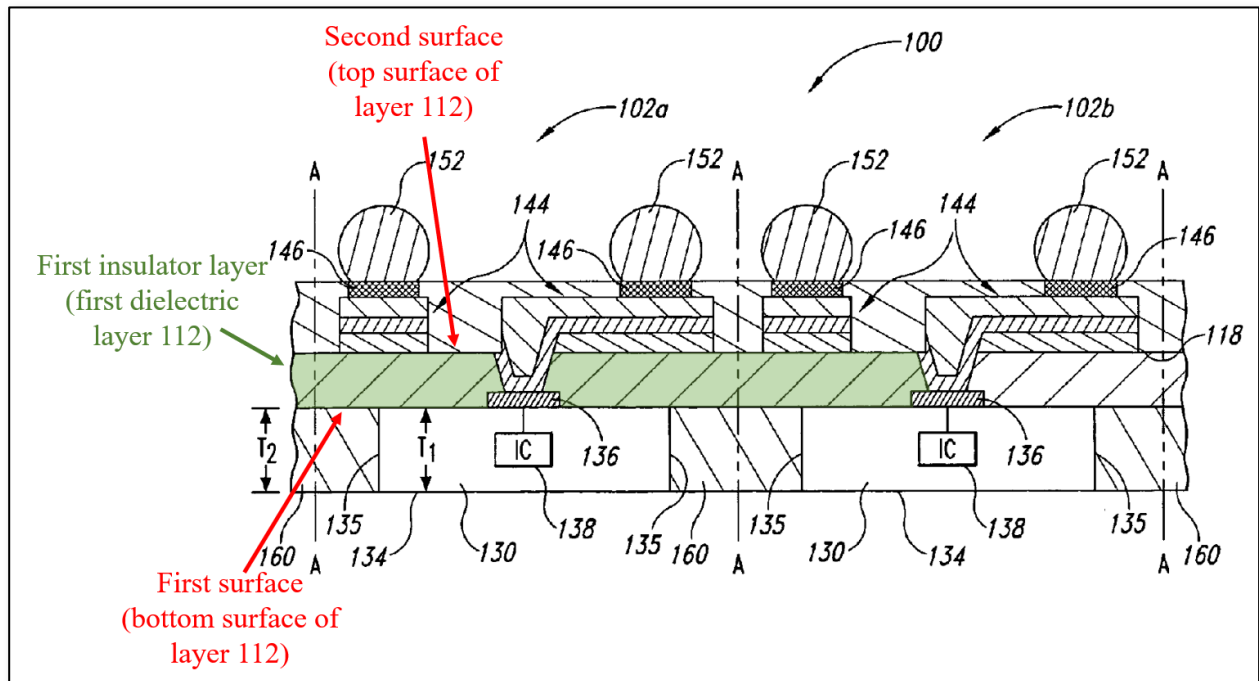
C. Analysis of Claims

[1pre]:

Petitioner does not concede this preamble is limiting. Lee's "microelectronic device assembly 100" is a "*circuit module*." APPLE-1015, [0033]; APPLE-1003, ¶191.

[1a]:

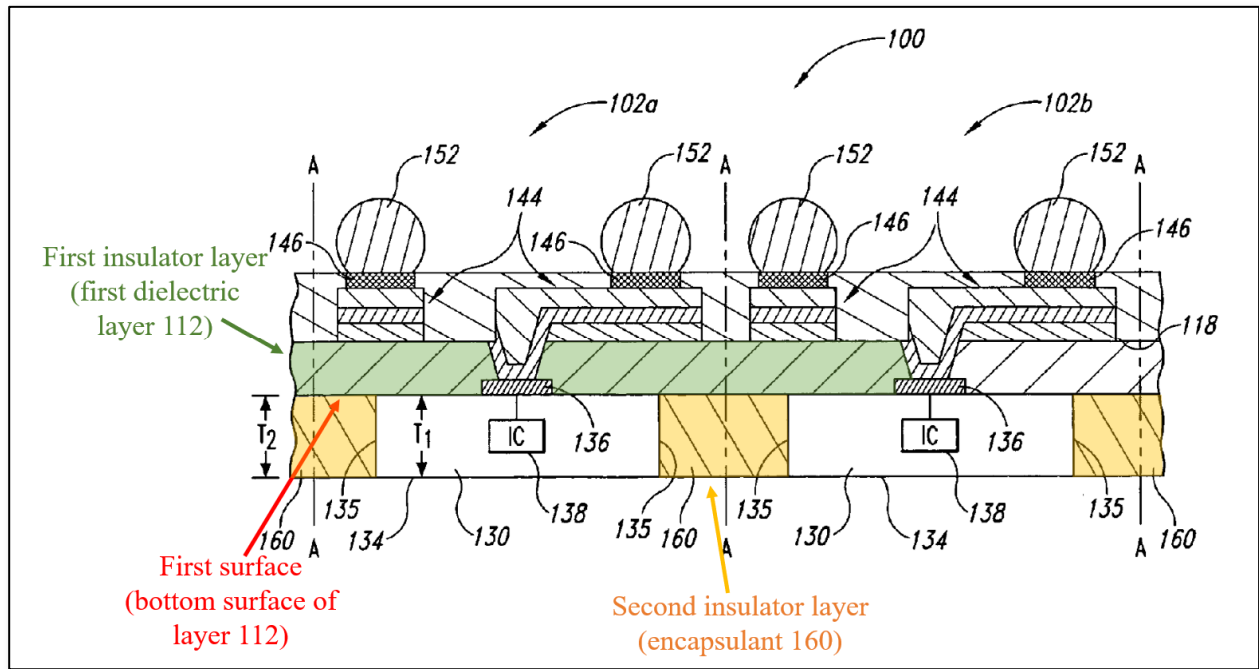
Lee's "first dielectric layer 112," which "can be a resin coated copper (RCC) or pre-preg material with woven fiber cloth embedded in a B-stage resin," is a "*first insulator layer*" and has first and second surfaces, as shown below. APPLE-1015, [0026]; APPLE-1003, ¶192.



Lee FIG. 1E

[1b]:

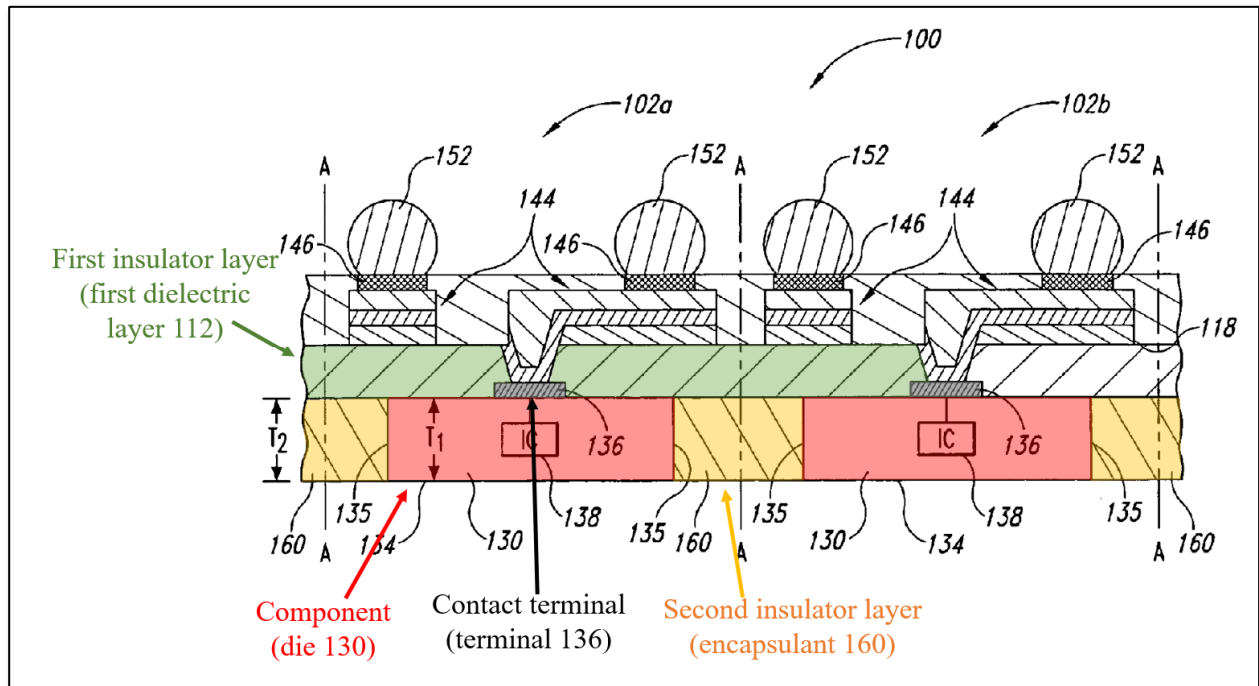
Lee's "encapsulant 160," which is on the bottom ("first") surface of layer 112 ("first insulator layer") is a "second insulator layer." APPLE-1015, [0033], FIG. 1E; APPLE-1003, ¶193.



Lee FIG. 1E

[1c]:

Lee's dies 130, which are inside the encapsulant 160 ("second insulator layer") and have terminals 136 that are "contact terminals," are "at least one component." APPLE-1015, [0029], [0033], FIG. 1E; APPLE-1003, ¶194.



Lee FIG. 1E

Lee does not explicitly disclose the material(s) of the terminals 136.

However, Lee’s disclosure that “zincation” can be performed on the terminals 136 amounts to an implicit disclosure that the terminals 136 are composed of **aluminum**. Dr. Subramanian notes that “for circuit modules in the 2000s, aluminum was the standard material for use in contact terminals, and zincation was a standard process for use on aluminum contact terminals. In the absence of disclosure to the contrary, a POSITA would have generally assumed that, if a terminal were being processed by ‘zincation’ to prepare the terminal for further layer deposition, the terminal would likely be an aluminum terminal.” APPLE-1003, ¶195. *See* Section VII.B.

It would have been obvious to use aluminum for the terminals 136, based on the disclosure of “zincation” and the knowledge that aluminum contacts were common in the field. APPLE-1003, ¶196. Indeed, the ’324 Patent admits in its Technical Field and Background sections that “circuit modules comprise conductors [] through which a component can be connected to become part of a circuit []. **The most common conductor material is aluminium.**” APPLE-1001, 1:9-10, 1:65-66. Accordingly, the use of aluminum for the terminals 136 (as the “*first metal*”) would have been nothing more than the selection of the most common material used for that purpose. APPLE-1003, ¶196.

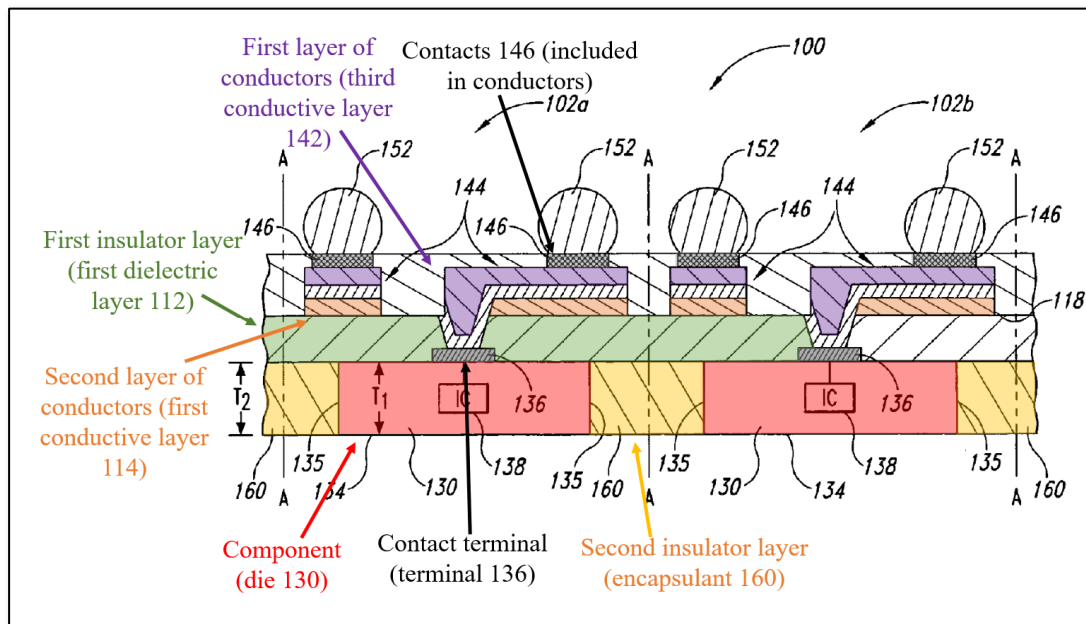
Ground 2B: Lee and Sakamoto render obvious that the terminals 136 are composed of aluminum

The use of aluminum for the terminals 136 is also obvious given Sakamoto. APPLE-1003, ¶197. Sakamoto notes that “the pad of the IC chip is normally formed out of **aluminum** or the like” and describes die pads 24 that are “made of **aluminum.**” APPLE-1005, [0051], [0101]. It would have been obvious to try aluminum based on Sakamoto’s disclosure that aluminum is suitable (and, indeed, “normal”) for this purpose. APPLE-1005, [0051]; APPLE-1003, ¶197. A POSITA would have had a reasonable expectation of success in using aluminum, given that Lee also describes the use of “zincation,” a process known to provide favorable results when applied to aluminum contacts. APPLE-1015, [0029]; APPLE-1003,

¶197.

[1d]:

Lee's first conductive layer 114, third conductive layer 142, and contacts 146 are together “conductors,” of which layers 142 and 114 are examples of the “first layer” and the “second layer,” respectively. APPLE-1015, [0030]-[0033], FIG. 1E; APPLE-1003, ¶198. Layer 114 is on the top surface (*second surface*) of layer 112 (*first insulator layer*). APPLE-1015, FIG. 1E; APPLE-1003, ¶198. Note that the contacts 146 can equally be excluded from the “conductors” without departing from claim 1.

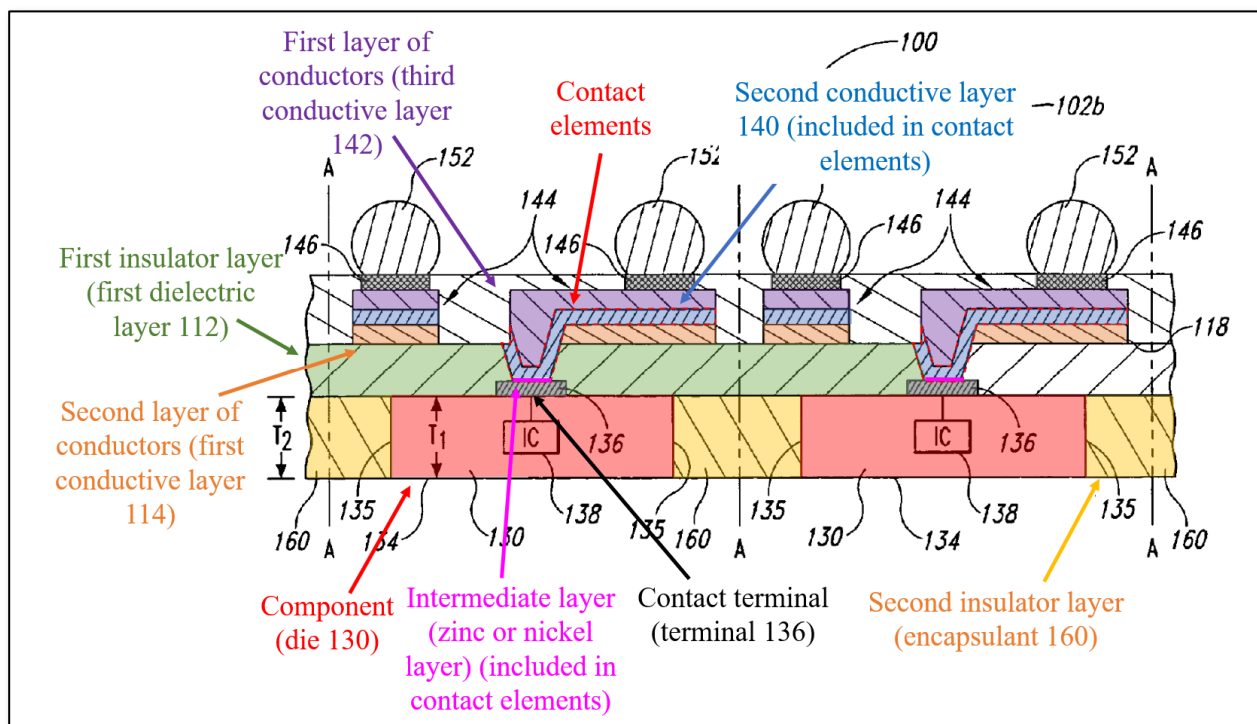


Lee FIG. 1E

Layer 114 (*second layer of the conductors*) can be a “copper foil,” such that the “*second metal*” is **copper**. APPLE-1015, [0026]; APPLE-1003, ¶199.

[1e]:

Lee's zinc or nickel layer and "second conductive layer 140" together are "*contact elements*" that are between the terminals 136 ("*contact terminals*") and layer 142 ("*conductors*"). APPLE-1015, [0030], FIG. 1E; APPLE-1003, ¶200. Of these layers, the zinc or nickel layer is an "*intermediate layer*" on the surface of the contact terminals and containing a "*third metal*," **zinc** or **nickel**. APPLE-1015, [0030], FIG. 6; APPLE-1003, ¶200.

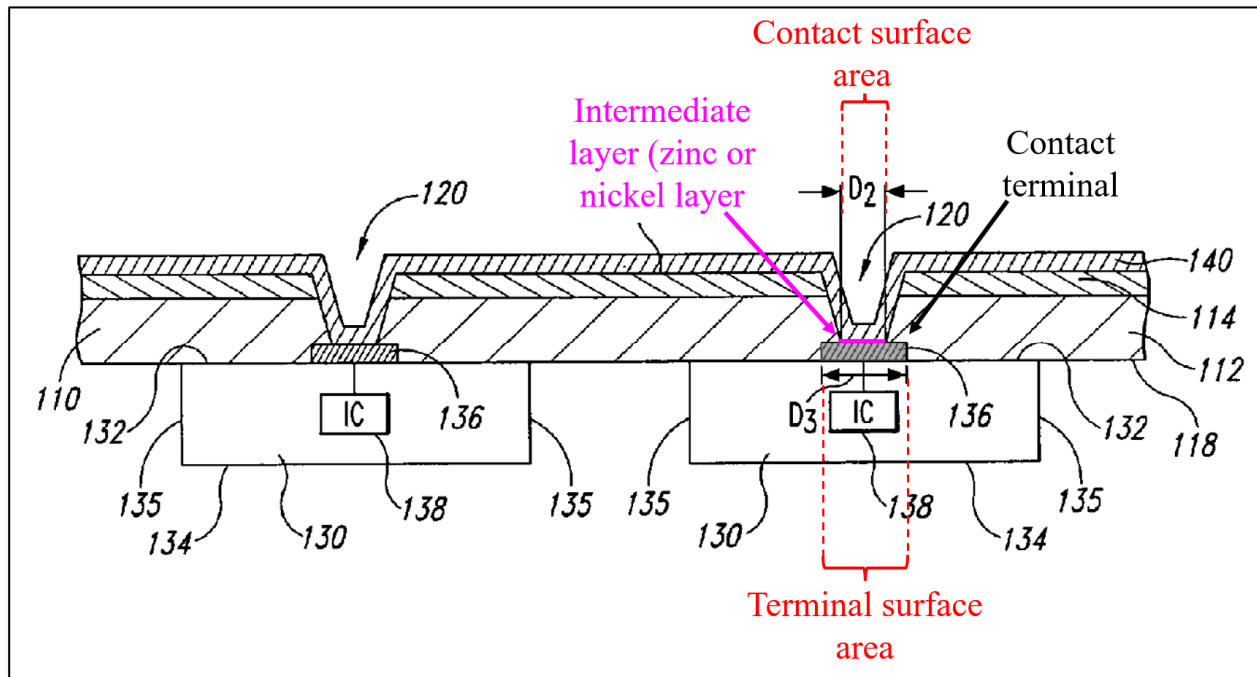


Lee FIG. 1E

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> • First conductive layer 114 (<i>second layer</i>), • Third conductive layer 142 (<i>first layer</i>), and • Contacts 146 	Cu	<ul style="list-style-type: none"> • Zinc or nickel layer (<i>intermediate layer</i>), and • Second conductive layer 140 	Zn or Ni

[1f]:

The contact surface area between Lee's zinc or nickel layer ("*intermediate layer*") and terminal 136 ("*contact terminal*") is less than a surface area of the terminal 136. APPLE-1003, ¶201. Lee describes that "[t]he individual terminals 136 may have a dimension D_3 greater than the second dimension D_2 (FIG. 1A) of the holes 120 to facilitate proper alignment." APPLE-1015, [0029], FIG. 1B. The zinc or nickel layer is formed in the holes 120 "on the terminals 136," e.g., in the case of zincation, would exhibit self-aligned growth on an exposed portion of the terminals 136, as discussed in §§VII.A-VII.C. APPLE-1015, [0030]; APPLE-1003, ¶201. Because the exposed terminal area corresponding to dimension D_2 is less than the total terminal area corresponding to dimension D_3 , a contact surface area between the zinc or nickel layer ("*intermediate layer*") and the terminal 136 ("*contact terminals*") is less than a surface area of the terminal 136, satisfying element [1f]. APPLE-1015, FIG. 1B; APPLE-1003, ¶202.



Lee FIG. 1B

[2]:

Lee or Lee-Sakamoto render obvious that the “*first metal*” of the “*contact terminals*” (terminals 136) is **aluminum**, the “*second metal*” of the “*second layer*” (first conductive layer 114) is **copper**, and the “*third metal*” of the zinc or nickel layer is **zinc** or **nickel**. APPLE-1003, ¶203. See [1c]-[1e]. APPLE-1003, ¶203.

[4]:

Lee’s **zinc** or nickel layer (e.g., formed by “zincation”) is applied as the “*intermediate layer*.” APPLE-1015, [0030]; APPLE-1003, ¶204. See [1e].

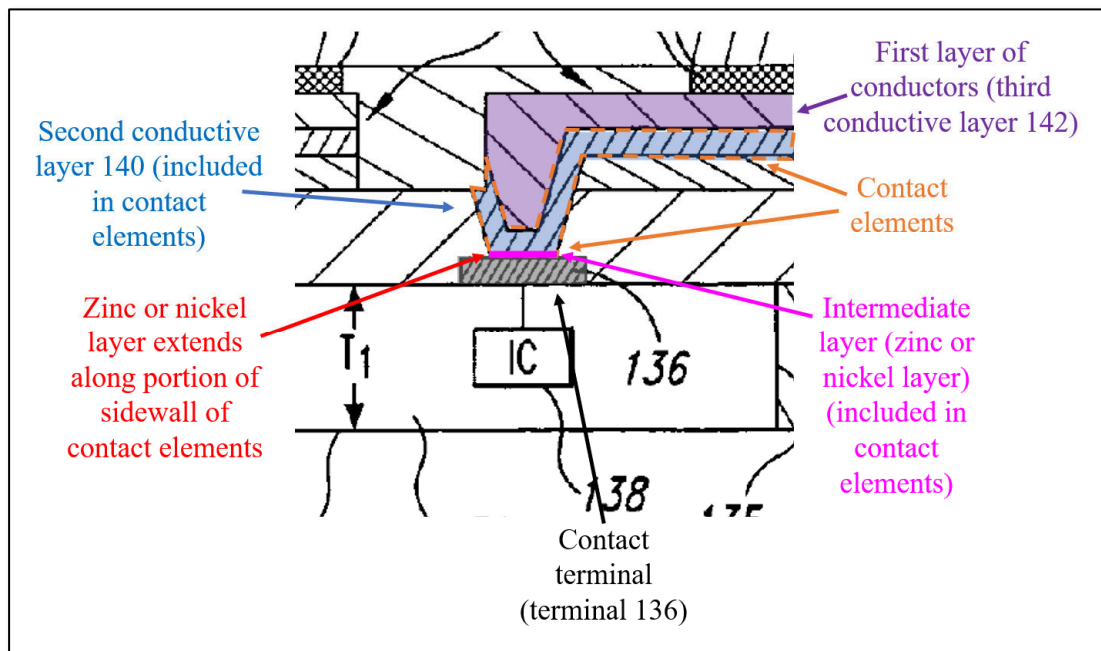
[6]:

Lee’s zinc or **nickel** layer (e.g., “a nickel layer”) is applied as the

“intermediate layer.” APPLE-1015, [0030]; APPLE-1003, ¶205. See [1e].

[7]:

Lee’s zinc or nickel layer and second conductive layer are applied as the “contact elements,” and the zinc or nickel layer is applied as the “intermediate layer.” APPLE-1015, [0030]; APPLE-1003, ¶206. See [1e]. The zinc or nickel layer defines a portion of side walls of the *contact elements*, such that the zinc or nickel layer (“intermediate layer”) “extends along” the side walls. APPLE-1003, ¶206. As shown below, the zinc or nickel layer is between the terminal 136 (“contact terminal”) and layer 142 (“first layer of the conductors”). APPLE-1015, [0030]-[0031], FIG. 1E; APPLE-1003, ¶207.



Portion of Lee FIG. 1E

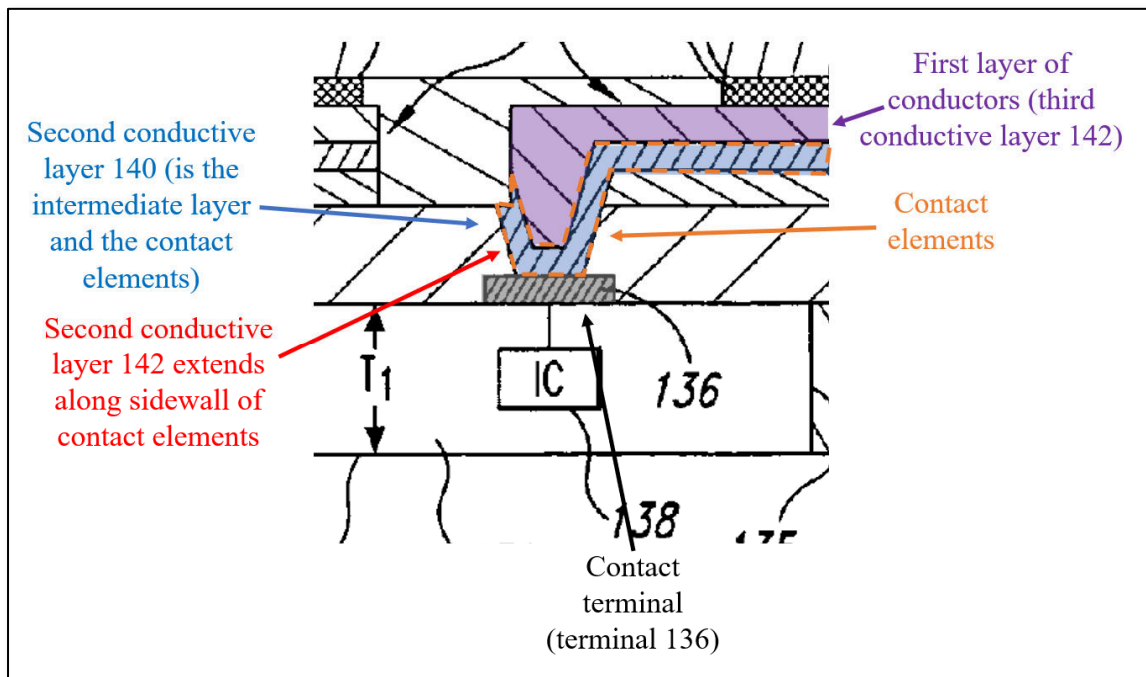
As an alternative teaching of claim 7, in the case where the zinc or nickel

layer is omitted (as Lee teaches is a possibility), the second conductive layer 140 can be applied as the “*intermediate layer*.” APPLE-1015, [0030]; APPLE-1003, ¶208. Layer 140 is on the surface of the terminal 136 (*contact terminal*) as the “*intermediate layer*,” and also forms the “*contact elements*.” APPLE-1003, ¶209.

This mapping is summarized in the table below. As discussed below for [11], it would have been obvious to use nickel for the “*third metal*” of layer 140, e.g., given Lee’s disclosure that it can be formed by “electroless plating,” and/or given Sakamoto. APPLE-1015, [0030]; APPLE-1003, ¶209.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none">• First conductive layer 114 (<i>second layer</i>),• Third conductive layer 142 (<i>first layer</i>), and• Contacts 146	Cu	<ul style="list-style-type: none">• Second conductive layer 140 (<i>intermediate layer</i>)	Ni

Layer 140 extends along (and defines) side walls of the “*contact elements*.” APPLE-1015, FIG. 1E; APPLE-1003, ¶210. Further, layer 140 is between the terminal 136 (“*contact terminal*”) and layer 142 (“*first layer*” of the “*conductors*”). APPLE-1015, [0030]-[0031], FIG. 1E; APPLE-1003, ¶210. Therefore, this alternative mapping also satisfies claim 7.



Portion of Lee FIG. 1E

[8]:

Lee's third conductive layer 142 includes a "*copper core*" that connects continuously to the material of the "*second layer of the conductors*" (third conductive layer 142 above the core). APPLE-1003, ¶211. For claim 1, the first conductive layer 114, contacts 146, and the entirety of layer 142 were together applied as the "*conductors*." However, it is equally valid to apply layer 114, the contacts 146, and the third conductive layer 142 **above the core**, as the "*conductors*," of which layer 114 is applied as the "*first layer*" and layer 142 above the core is applied as the "*second layer*." APPLE-1003, ¶211.

It would have been obvious to use copper for the third conductive layer 142, as copper was the most common material for "electroplating" of a conductive

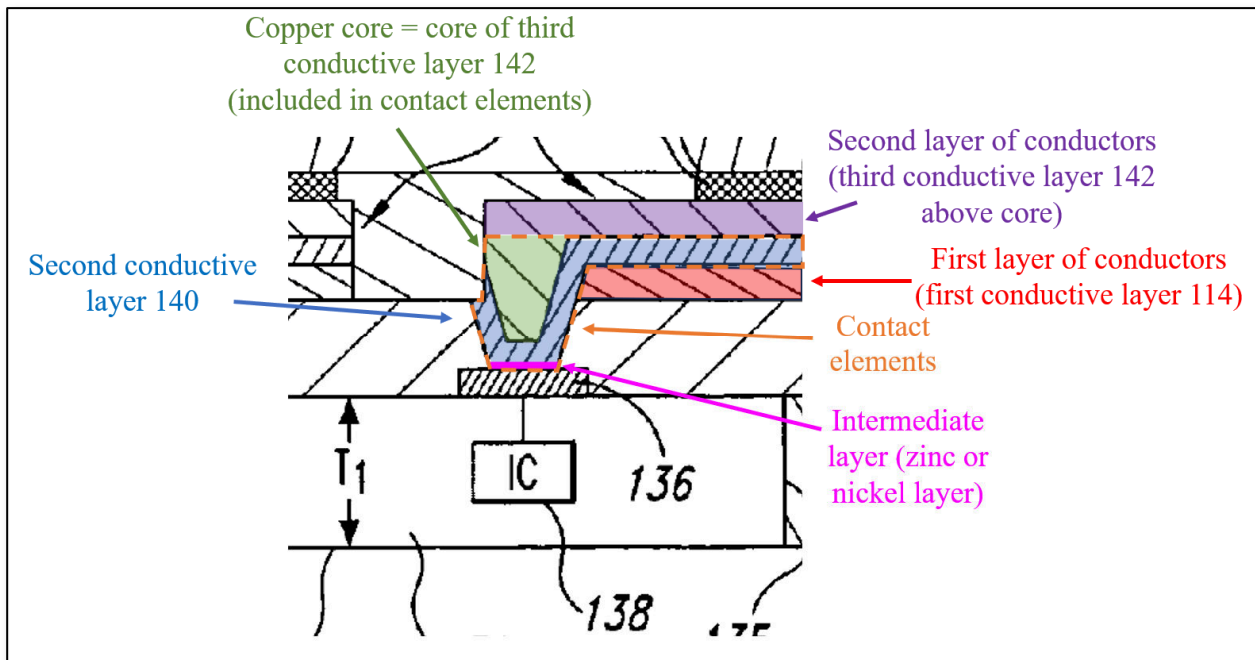
layer, and Lee describes that layer 142 is formed by “electroplating.” APPLE-1015, [0031]; APPLE-1003, ¶212. Therefore, in this mapping, the “*second metal*” of the “*second layer of the conductors*” (the third conductive layer 142 above the core) is **copper**. APPLE-1003, ¶213.

For claim 1, the zinc or nickel layer and layer 140 were together applied as the “*contact elements*.” However, it is equally valid to include each of the zinc or nickel layer, layer 140, **and** the core of layer 142 as the “*contact elements*.” APPLE-1003, ¶214.

The core of the third conductive layer 142 is a “*copper core*” that “*connects continuously*” to the material of the third conductive layer 142 above the core, because these elements are formed in a common, continuous “electroplating” process that, as discussed above, deposits **copper**. APPLE-1015, [0031]; APPLE-1003, ¶215. This mapping is consistent with the ’324 Patent’s description of corresponding elements for the reasons discussed for [8] in §IV.B.

These alternative mappings are shown in the table and annotated FIG. 1E below. APPLE-1003, ¶126.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> First conductive layer 114 (<i>first layer</i>), Third conductive layer 142 above core (<i>second layer</i>), and Contacts 146 	Cu	<ul style="list-style-type: none"> Zinc or nickel layer (<i>intermediate layer</i>), Second conductive layer 140, and Core of third conductive layer 142 	Zn or Ni

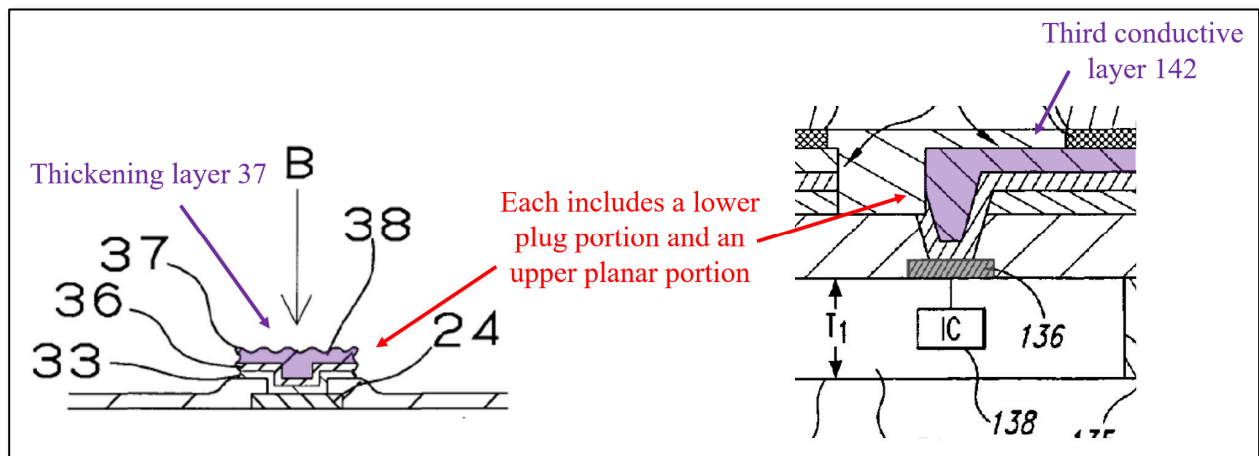


Portion of Lee FIG. 1E

Ground 2B: Lee and Sakamoto render obvious that layer 142 is composed of copper

The use of copper for the third conductive layer 142 is also obvious given Sakamoto. APPLE-1003, ¶217. In selecting a metal to use for layer 142, it would

have been obvious for a POSITA to look to Sakamoto's thickening layer 37, which is similar in several ways to layer 142. APPLE-1003, ¶217. First, both layers are deposited by "electroplating." APPLE-1005, [0114]; APPLE-1015, [0031]. Second, both layers are deposited onto an underlying conductive layer (the "second conductive layer 140" for Lee, and the "metal" layer 36 for Sakamoto). APPLE-1005, [0111], [0114]; APPLE-1015, [0031]. Third, both layers have a similar morphology, including a plug portion and an overlying planar portion, as shown below. APPLE-1005, FIG. 6(A); APPLE-1015, FIG. 1E; APPLE-1003, ¶217. Given the common deposition method, underlying substrate, and layer morphology, it would have been obvious for a POSITA to try using copper for layer 142 with a reasonable expectation of success. APPLE-1003, ¶217-218.



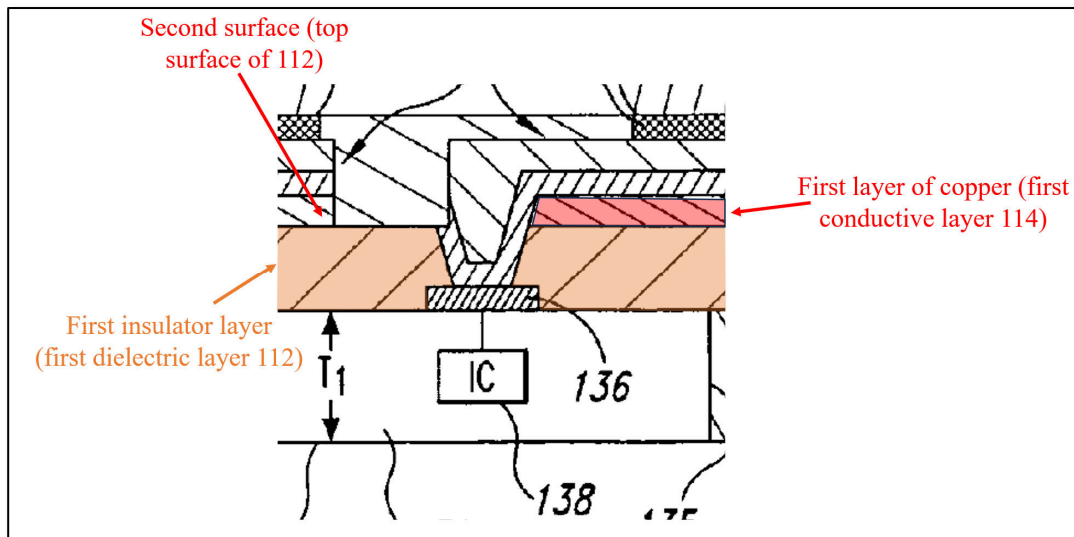
Left: Sakamoto FIG. 6(A); Right: portion of Lee FIG. 1E

[10]:

Lee's conductive layers 114, 140, 142 are respectively a "first layer of copper," "intermediate layer," and "second layer of copper" satisfying claim 10.

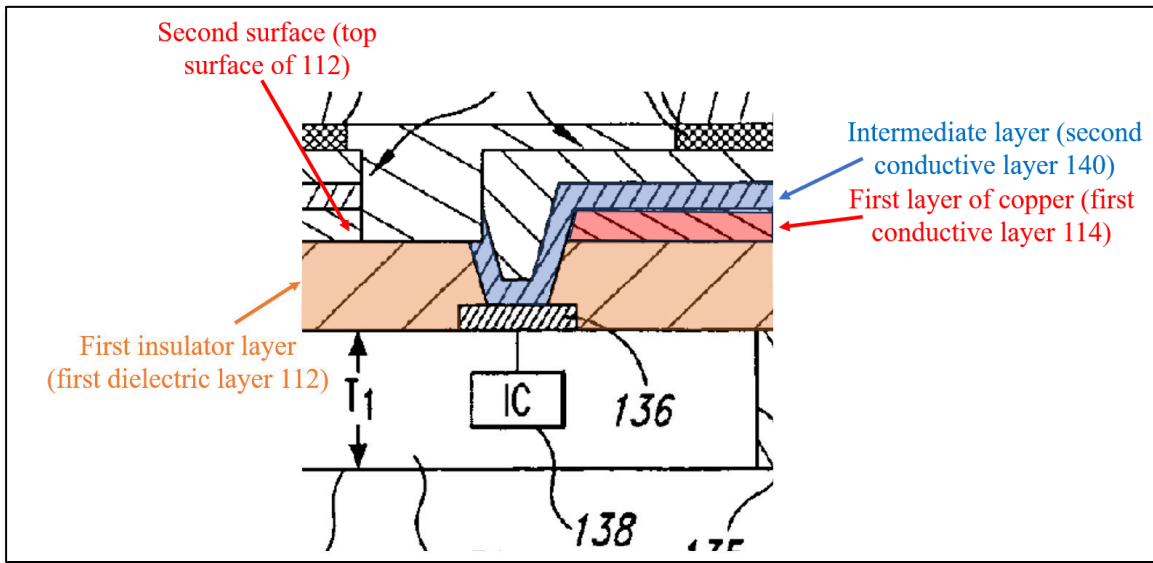
APPLE-1003, ¶219. The “conductors” include Lee’s layer 114, which is “copper foil.” APPLE-1015, [0026]; APPLE-1003, ¶219. See claim 1. Further, layer 114 is on the “second surface” (top surface) of the “first insulator layer” (layer 112).

APPLE-1015, [0026], FIG. 1E; APPLE-1003, ¶219. Therefore, layer 114 is a “first layer of copper” on the second surface of the first insulator layer. APPLE-1003, ¶219.



Portion of Lee FIG. 1E

For claim 1, Lee’s second conductive layer 140 was applied as part of the “contact elements.” However, it is equally valid to layer 140 in the “conductors.” APPLE-1003, ¶220. As shown below, layer 140 is an “intermediate layer” on the surface of the “first copper layer” (layer 114), as recited in claim 10.



Portion of Lee FIG. 1E

Lee's third conductive layer 142 is on the surface of the "*intermediate layer*" (second conductive layer 140). APPLE-1015, FIG. 1E; APPLE-1003, ¶221. As discussed for [8], it would have been obvious to make layer 142 a copper layer. APPLE-1015, [0031]; APPLE-1003, 221. As such, layer 142 is a "*second layer of copper*" on the surface of the "*intermediate layer*" (layer 140) as recited in claim 10.

These mappings are summarized in the table below. APPLE-1003, ¶222.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> • First conductive layer 114 (<i>first layer of copper; “first layer” of claim 1</i>), • Second conductive layer 140 (<i>intermediate layer</i>), • Third conductive layer 142 (<i>second layer of copper; “second layer” of claim 1</i>), and • Contacts 146 	Cu	<ul style="list-style-type: none"> • Zinc or nickel layer (<i>“intermediate layer” of claim 1</i>) 	Zn or Ni

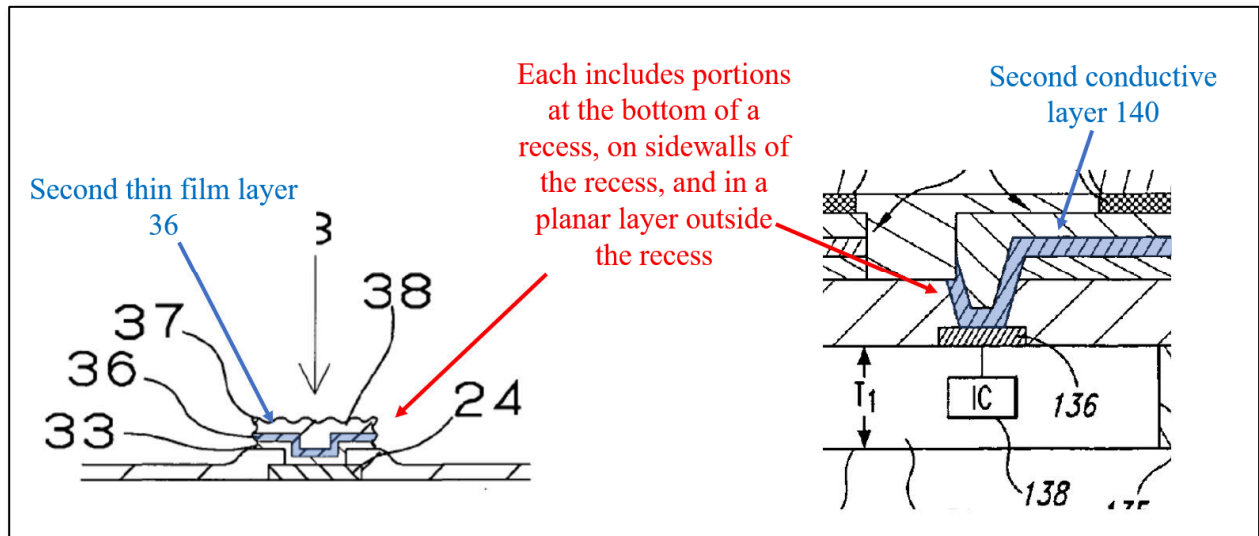
[11]:

The “*intermediate layer*” is Lee’s second conductive layer 140, which “can be formed on the substrate 110 by electroless plating [].” APPLE-1015, [0030]; APPLE-1003, ¶223. *See* [10]. It would have been obvious to have the *intermediate layer* be nickel grown by electroless plating. APPLE-1003, ¶223. *See* Section VII.B, which establishes that zincation of aluminum pads is a common preliminary step to electroless nickel plating. APPLE-1003, ¶223-224.

The electroless nickel layer 140 includes “*nickel grown by a chemical growing method*” and satisfies claim 11. APPLE-1003, ¶225.

Ground 2B: Lee and Sakamoto render obvious that the second conductive layer 140 is electroless copper or electroless nickel

The use of electroless copper or electroless nickel for the second conductive layer 140 is also obvious given Sakamoto. APPLE-1003, ¶226. In selecting a metal to use for layer 140, it would have been obvious to look to Sakamoto's second thin film layer 36, which is similar to layer 140. First, both layers can be deposited by "electroless plating." APPLE-1005, [0021]; APPLE-1015, [0030]. Second, both layers are deposited on an underlying metal layer that can be zinc or nickel (the zinc or nickel layer for Lee, and layer 33 for Sakamoto). APPLE-1005, [0109]; APPLE-1015, [0030]. Third, both layers have similarly morphology, being deposited in a recess, on sidewalls of the recess, and in a planar layer outside the recess, as shown below. APPLE-1005, FIG. 7(A); APPLE-1015, FIG. 1E; APPLE-1003, ¶226. Given the common deposition method, underlying substrate, and layer morphology, it would have been obvious for a POSITA to try using electroless copper or electroless nickel for layer 140, with a reasonable expectation of success. APPLE-1003, ¶226-227.

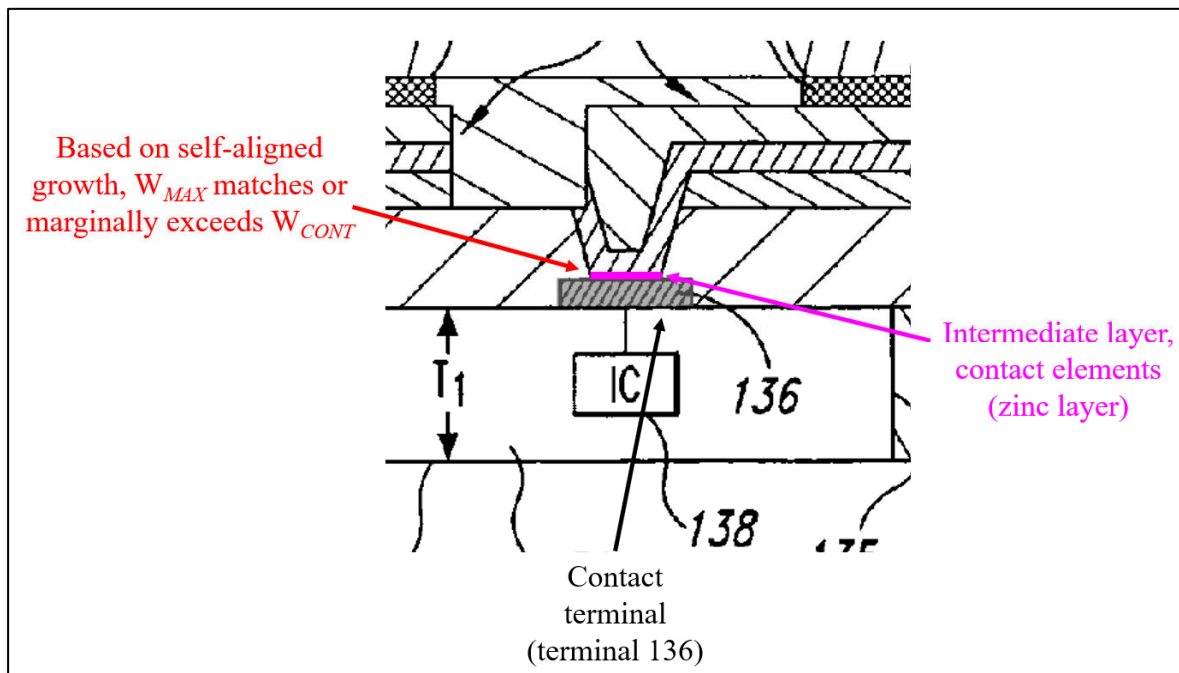


Left: Sakamoto FIG. 6(A); Right: portion of Lee FIG. 1E

[12]:

For claim 1, the “*contact elements*” were mapped to Lee’s zinc or nickel layer and second conductive layer 140. However, it is equally valid to apply only the zinc or nickel layer as the “*contact elements*,” as shown in the chart and figure below, where the zinc or nickel layer is specifically a zinc layer formed by zincation. APPLE-1003, ¶228.

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> • First conductive layer 114 (<i>second layer</i>), • Third conductive layer 142 (<i>first layer</i>), and • Contacts 146 	Cu	<ul style="list-style-type: none"> • Zinc layer (<i>intermediate layer</i>) 	Zn



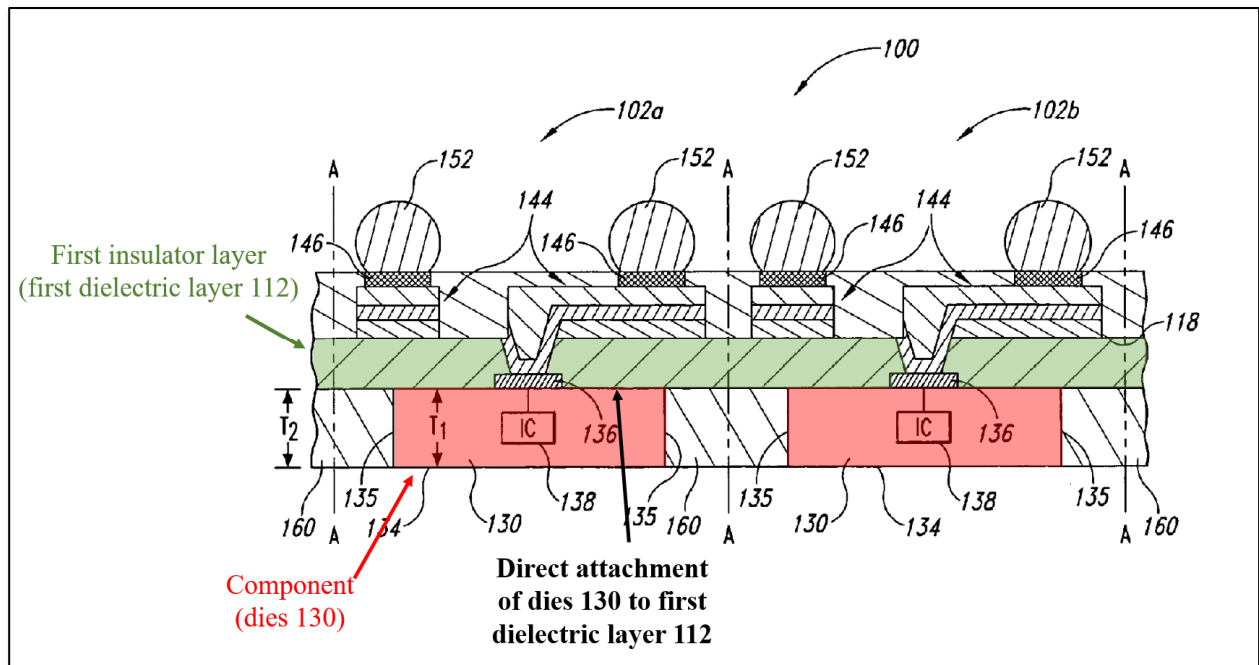
Portion of Lee FIG. 1E

Based on this mapping, claim 12 requires that a width of the contact surface between Lee's zinc layer and Lee's terminal 136 is 0-20% less than a greatest width of the zinc layer in the same direction. APPLE-1003, ¶229. As discussed for [12] at Ground 1D, a zinc layer grown by "zincation" on the terminal 136 (as disclosed by Lee) has a greatest width that essentially matches the width of the contact surface. APPLE-1003, ¶229. Therefore, this arrangement satisfies claim 12.

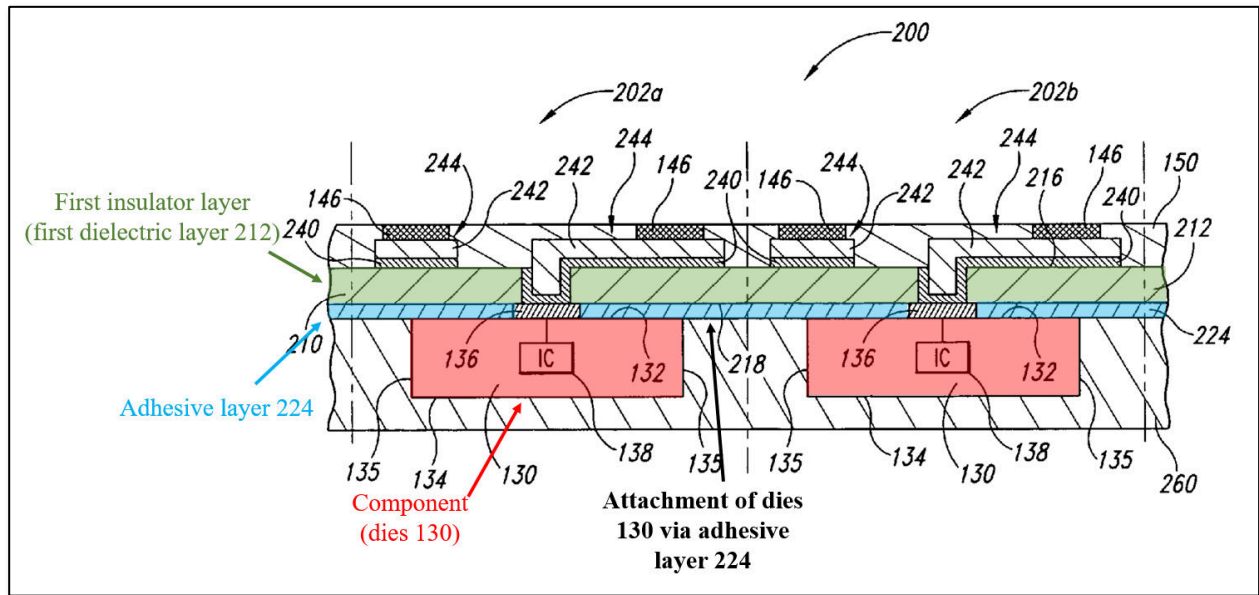
[15]:

Lee's disclosure of an "adhesive layer" teaches claim 15. APPLE-1015, [037]; APPLE-1003, ¶230. While the embodiment of FIG. 1E is "without an adhesive," "in other embodiments, such as the embodiments [of] FIGS. 2A-3B, the

microelectronic device assembly may include an adhesive for attaching the dies 130 to the substrate 110.” APPLE-1015, [0029]. As shown in the comparative figures below, the dies 130 in FIG. 1E are attached directly to the first dielectric layer 112, while the dies 130 in FIG. 2B are attached to a first dielectric layer 212 by an “adhesive layer 224.” APPLE-1015, [0029], [0037]; APPLE-1003, ¶230.



Lee FIG. 1E



Lee FIG. 2B

In an embodiment that “include[s] an adhesive [layer 224] for attaching the dies 130 to the substrate 110” as disclosed by Lee, the adhesive layer 224 would be a “*polymer layer*” between the “*first insulator layer*” (layer 112) and the “*at least one component*” (dies 130). APPLE-1015, [0029]; APPLE-1003, ¶231. For example, Lee describes that the “adhesive layer 224 may be a pre-preg material,” which Lee describes as “woven fiber cloth embedded in a B-stage resin.” APPLE-1015, [0026], [0040]; APPLE-1003, ¶231. A “B-stage resin” is a polymer. APPLE-1003, ¶231. Further, “*contact holes*” for the “*contact elements*” (terminals 136) would be present in the adhesive layer 224, based on Lee’s description that “the adhesive layer 224 includes a plurality of second holes 220b aligned with corresponding first holes 220a in the substrate 210.” APPLE-1015, [0038]; APPLE-1003, ¶232.

To the extent Lee's foregoing description is not interpreted as a direct disclosure of the B-stage resin in the adhesive layer 224 applied to the structure of FIG. 1E, it would have been obvious for a POSITA to include the B-stage resin as a known example of the "pre-preg material" of the adhesive layer 224. APPLE-1015, [0026], [0040]; APPLE-1003, ¶233. For example, in a case where layer 112 may not include an adhesive, the POSITA would have known that the pre-preg material, including the B-stage resin, would be a suitable adhesive to include in the adhesive layer 224. APPLE-1003, ¶233.

[16]:

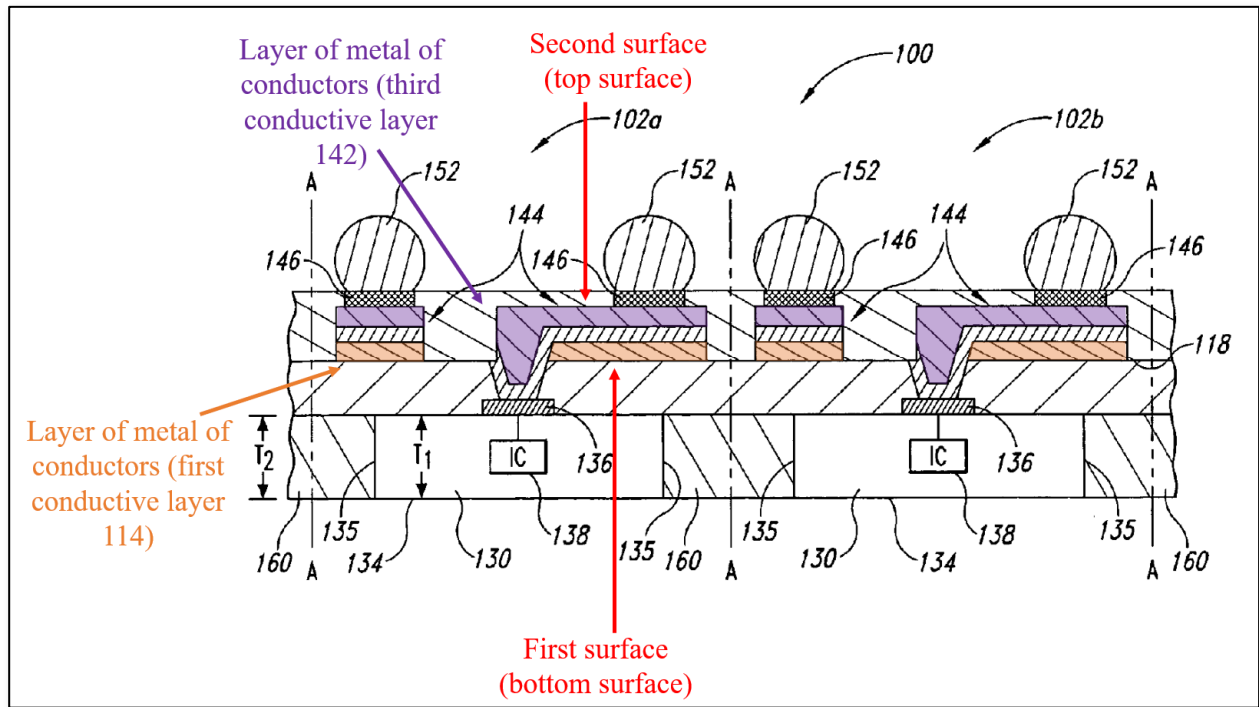
It would have been obvious to cure the B-stage resin included in the adhesive layer 224 ("*polymer layer*") discussed with respect to [15], so that the B-stage resin would become "fully cure[d]" and hardened. APPLE-1015, [0030]; APPLE-1003, ¶234. Although Lee does not explicitly describe that the adhesive layer 224 becomes fully cured, Lee describes curing **another** adhesive material, the "partially cured material in the first dielectric layer 112," so that the material becomes "fully cure[d]." APPLE-1015, [0029]-[0030]; APPLE-1003, ¶234. It would have been obvious to apply this known technique to the B-stage (partially cured) resin of the adhesive layer 224 to predictable obtain a "hardened" resin. APPLE-1003, ¶234.

[17pre]:

See [1pre].

[17a]:

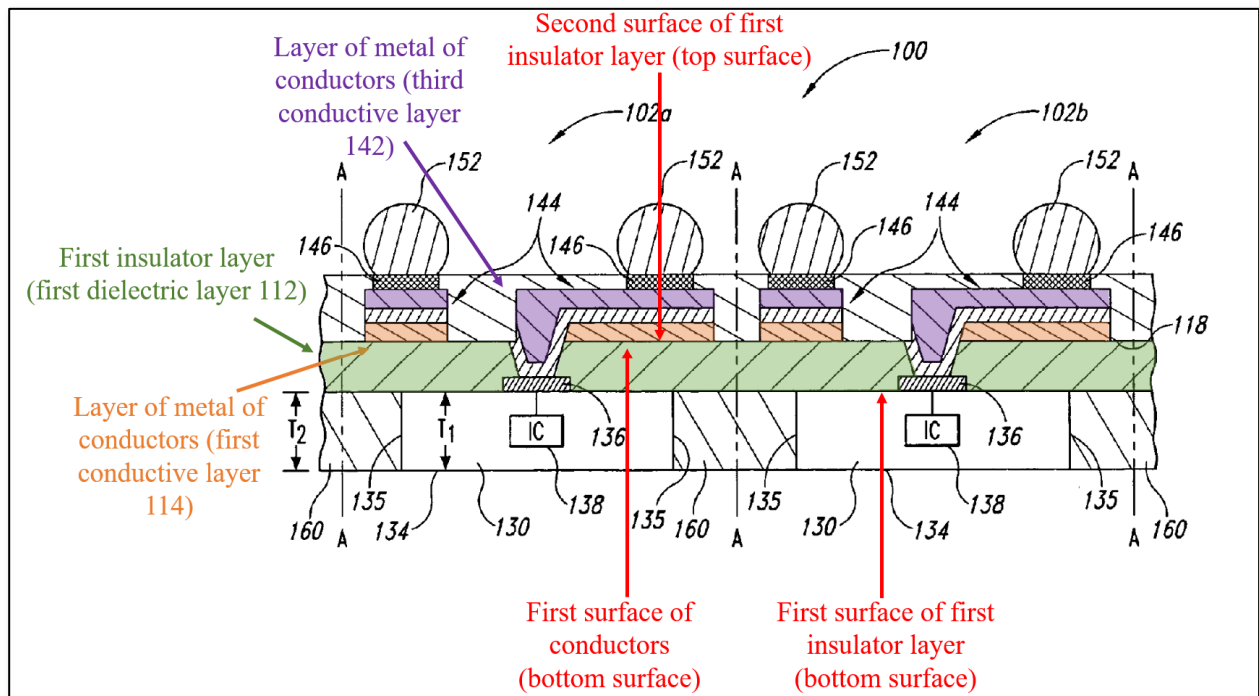
See [1d]. Lee's "first conductive layer 114" and "third conductive layer 142," together applied as "*a conductor layer*" and "*conductors*," are "*two layers of metal*" between first and second surfaces, as shown below. APPLE-1015, [0026]-[0031], FIG. 1E; APPLE-1003, ¶236. E.g., layer 114 is copper foil (a metal), and layer 142, being deposited by "electroplating," is also a metal. APPLE-1015, [0026], [0031]; APPLE-1003, ¶236. See [8] for Grounds 2A/2B above as to why layer 142 is, or obviously is, copper, a metal. APPLE-1003, ¶236. The contacts 146 can optionally be included in the *conductor layer*.



Lee FIG. 1E

[17b]:

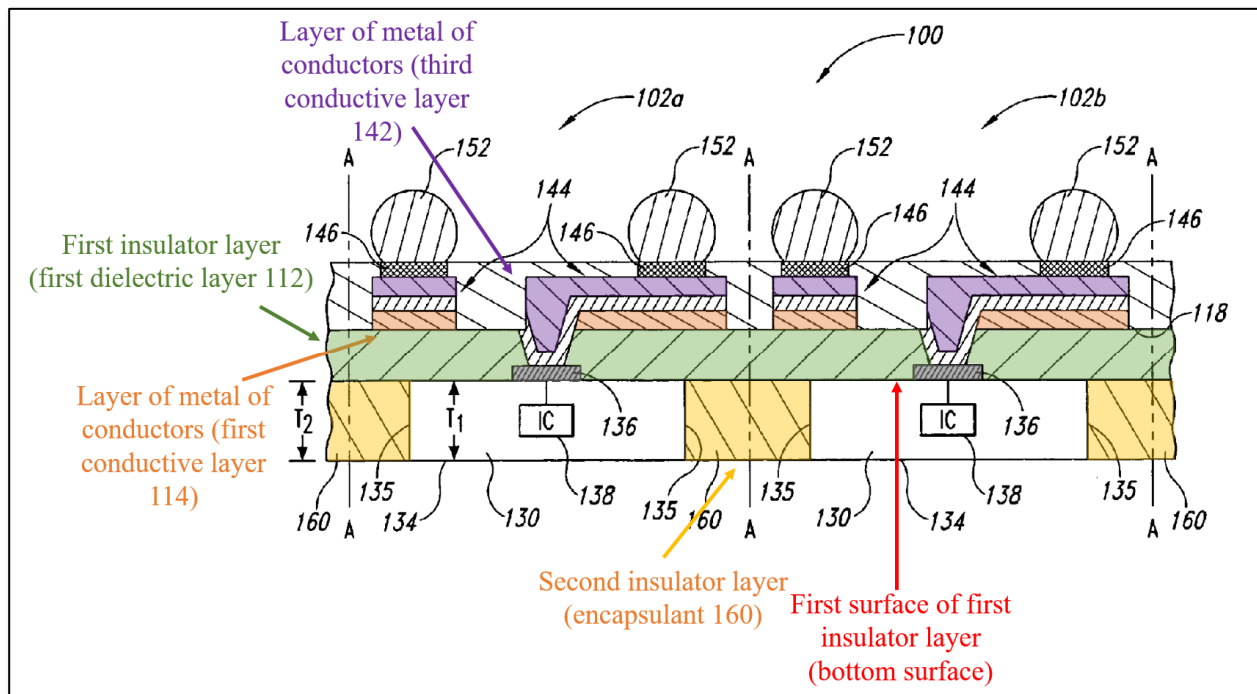
See [1a]. Lee's first dielectric layer 112 is a "first insulator layer" having a first (bottom) surface and a second (top) surface covering the first (bottom) surface of the conductors. APPLE-1015, [0026]; APPLE-1003, ¶237.



Lee FIG. 1E

[17c]:

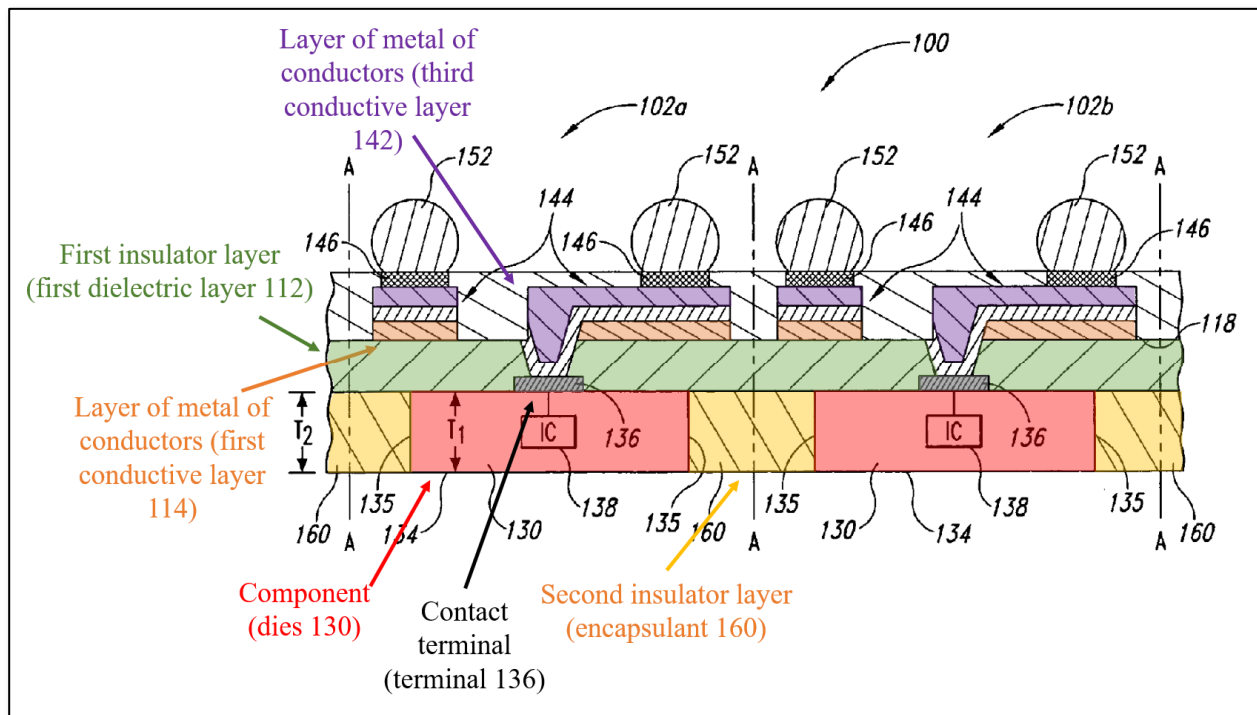
See [1b]. Lee's "encapsulant 160" is a "second insulator layer on the first surface of the first insulator layer." APPLE-1015, [0033]; APPLE-1003, ¶238.



Lee FIG. 1E

[17d]:

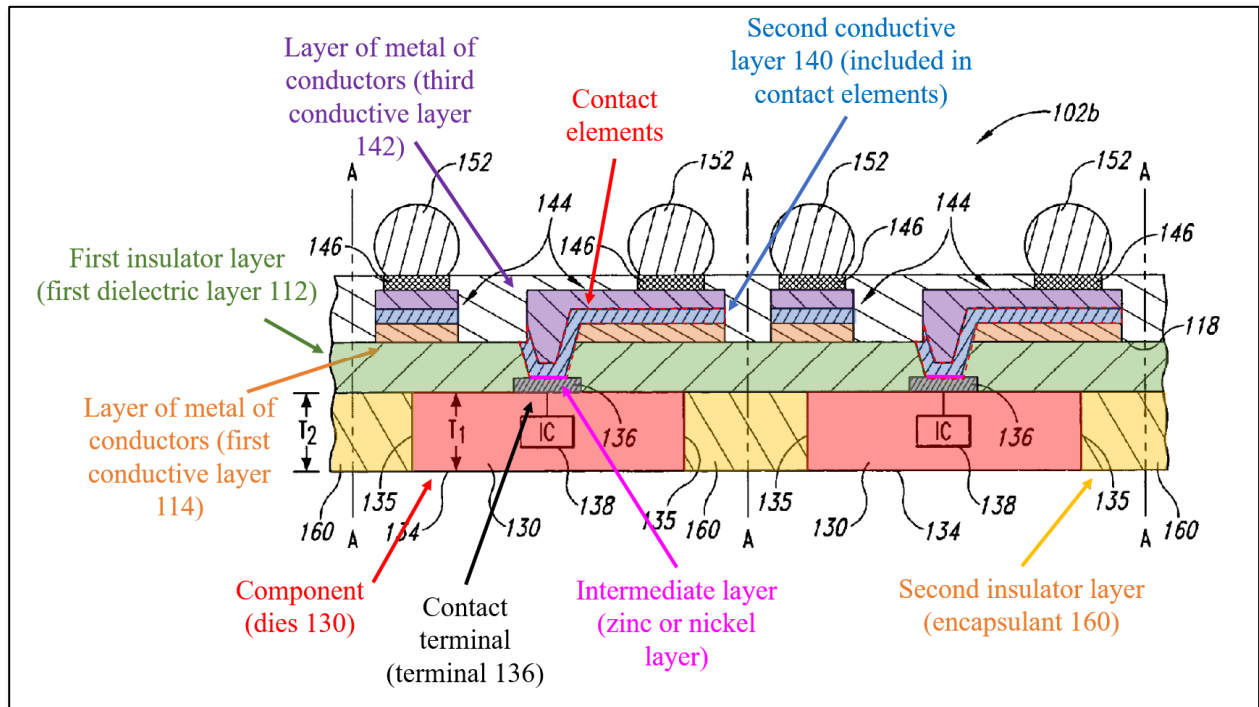
See [1c]. The “dies 130” are components that are inside the *second insulator layer* (encapsulant 160). APPLE-1015, [0029], [0033], FIG. 1E; APPLE-1003, ¶239. The dies 130 comprise “terminals 136” which are “*contact terminals.*” APPLE-1005, [0101], FIG. 6; APPLE-1003, ¶239. The terminals 136 are, or obviously are, composed of aluminum and therefore contain “*at least one layer of metal.*” APPLE-1015, [0030]; APPLE-1003, ¶239. See [1c].



Lee FIG. 1E

[17e]:

See [1e]. Lee’s zinc or nickel layer and second conductor layer 140 are between the “*contact terminals*” (terminals 136) and the *conductors* (e.g., layer 142) and constitute “*contact elements*.” APPLE-1015, [0030], FIG. 3; APPLE-1003, ¶240. The zinc or nickel layer is an “*intermediate layer*” that contains “*at least one layer of metal*,” e.g., the zinc or nickel. APPLE-1015, [0030]; APPLE-1003, ¶240.



Lee FIG. 1E

[17f]:

See [1f]. A contact surface area between the zinc or nickel layer (“*intermediate layer*”) and the terminal 136 (“*contact terminal*”) is less than a surface area of the terminal 136. APPLE-1015, [0027], FIG. 1B; APPLE-1003, ¶241.

[17g]:

See [1c], [1d], and [1e]. Lee’s terminals 136 (“*contact terminals*”) are composed of **aluminum**, a *first metal*; the first conductive layer 114 of the “*conductors*” is composed of **copper**, a *second metal*; and the zinc or nickel layer

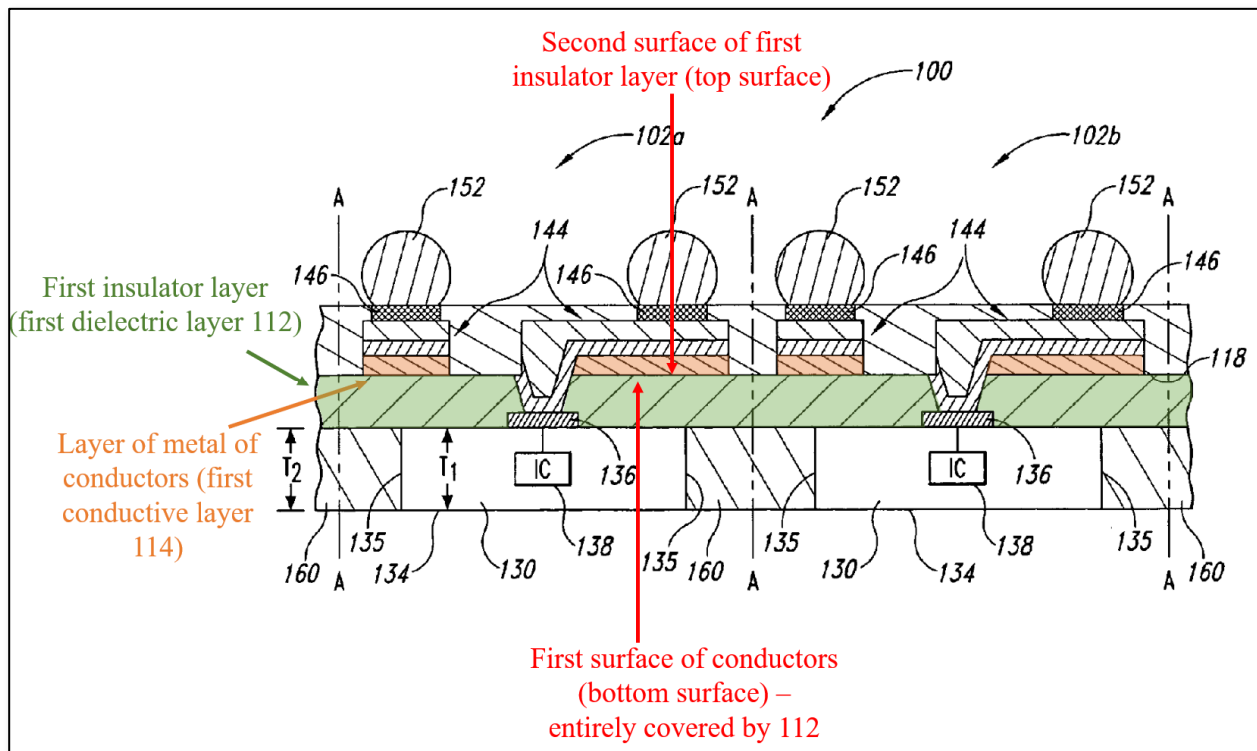
is composed of **zinc or nickel**, a *third metal*. APPLE-1015, [0026], [0030];
APPLE-1003, ¶242.

[18]:

Lee discloses an “adhesive layer 224” between layer 112 (*first insulator layer*) and the dies 130 (*at least one component*). APPLE-1015, [0029], [0038], FIG. 2B; APPLE-1003, ¶243. *See* [15]. It would have been obvious to make this “adhesive layer 224” a “*hardened adhesive*” based on Lee’s disclosure of “fully cur[ing] the partially cured material in the dielectric layer 112” APPLE-1015, [0030]; APPLE-1003, ¶243. *See* [16].

[19]:

See discussion for claims 1 and 17. Claim 19 is identical to claim 17 except for (1) omitting recitation of the first, second, and third metals and (2) reciting “*the second surface of the first insulator layer entirely covering the first surface of the conductors.*” The latter element is satisfied by the top surface of Lee’s first dielectric layer 112 (*first insulator layer*) entirely covering the bottom horizontal surface of the first conductive layer 114, the bottom horizontal surface being the “*first surface of the conductors*” applied for claim 19. APPLE-1015, FIG. 1E; APPLE-1003, ¶244.



Lee FIG. 1E

[20]: See [18] above.

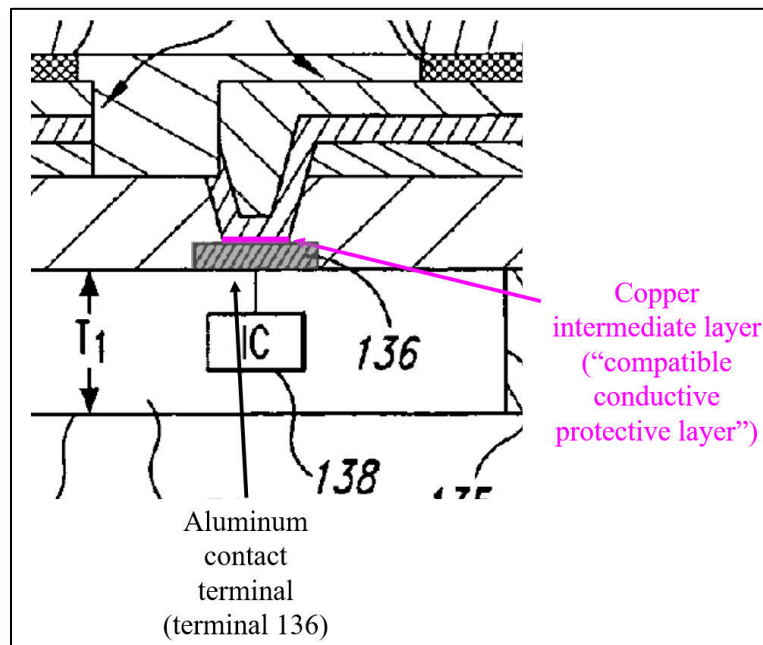
X. GROUND 2B: Claims 5, 9, and 14 are obvious over Lee and Sakamoto

A. Analysis of Claims

[5]:

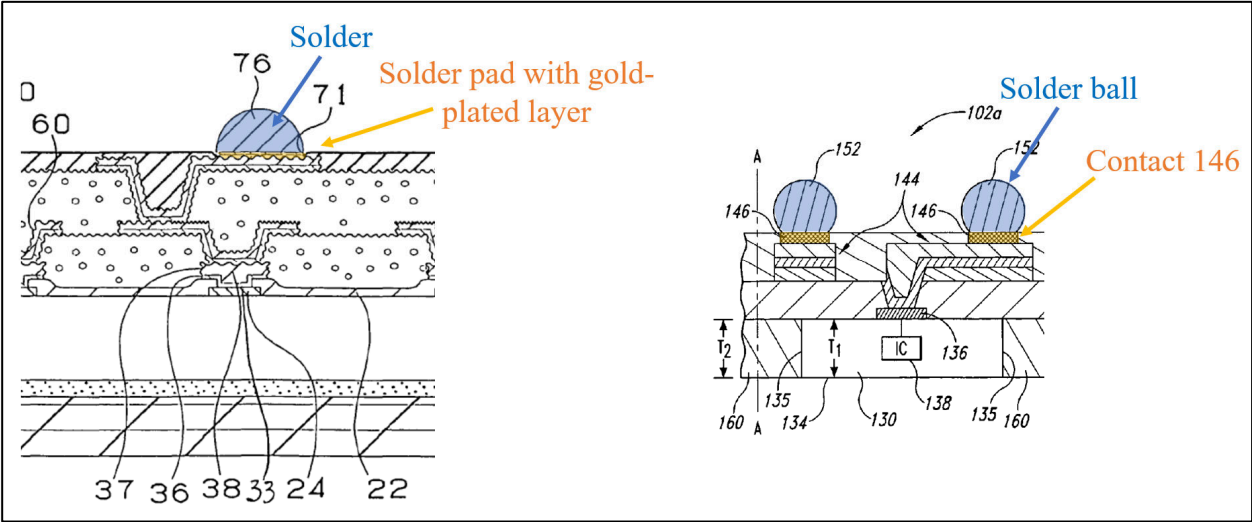
It would have been obvious to use copper in Lee’s “compatible conductive protective layer” (“*intermediate layer*”). APPLE-1003, ¶247. In the mapping discussed for Ground 2A, the “compatible conductive protective layer” was taken as zinc or nickel. APPLE-1015, [0030]. However, Lee does not restrict this layer to zinc or nickel, and, given Sakamoto, it would have been obvious to use **copper** for

this layer, satisfying claim 5. APPLE-1003, ¶247. In selecting a metal to use for the “compatible conductive protective layer,” it would have been obvious for a POSITA to look to Sakamoto’s layer 33, which can be composed of copper and is similar in several ways to the compatible conductive protective layer. APPLE-1005, [0109]; APPLE-1003, ¶247. First, both layers can be deposited by “sputtering.” APPLE-1005, [0109]; APPLE-1015, [0030]. Second, both layers are deposited on an underlying aluminum contact pad. APPLE-1005, [0110]; APPLE-1015, [0030]; APPLE-1003, ¶247. Third, both layers are used as a substrate for subsequent electroless plating or sputtering of another metal layer (layer 140 for Lee, or layer 36 for Sakamoto). APPLE-1005, [0021]; APPLE-1015, [0030]; APPLE-1003, ¶247. Given the common deposition methods and layer arrangements, it would have been obvious for a POSITA to try using, for the compatible conductive protective layer, the metals disclosed by Sakamoto for layer 33, including **copper**, with a reasonable expectation of success, arriving at a **copper** “*third metal*” of the “*intermediate layer*”. APPLE-1003, ¶247-248.



Portion of Lee FIG. 1E

Although, for claim 1, the first conductive layer 114 was applied as the “*second layer*” of the “*conductors*” having the “*second metal*,” it is equally valid to apply the contacts 146 as the “*second layer*” of the “*conductors*.” APPLE-1003, ¶250. Given Sakamoto, it would have been obvious to have the contacts 146 be “gold plated” as described for Sakamoto’s analogous “solder pads 75,” which, like the contacts 146, form an uppermost contact surface on which solder is applied. APPLE-1005, [0130], FIG. 6; APPLE-1015, [0034], FIG. 1E; APPLE-1003, ¶250. Accordingly, the “*second metal*” of the *conductors* can be **gold**.



Left: portion of Sakamoto FIG. 6; Right: portion of Lee FIG. 1E

The mapping applied for claim 5 is summarized in the following table.

APPLE-1003, ¶251.

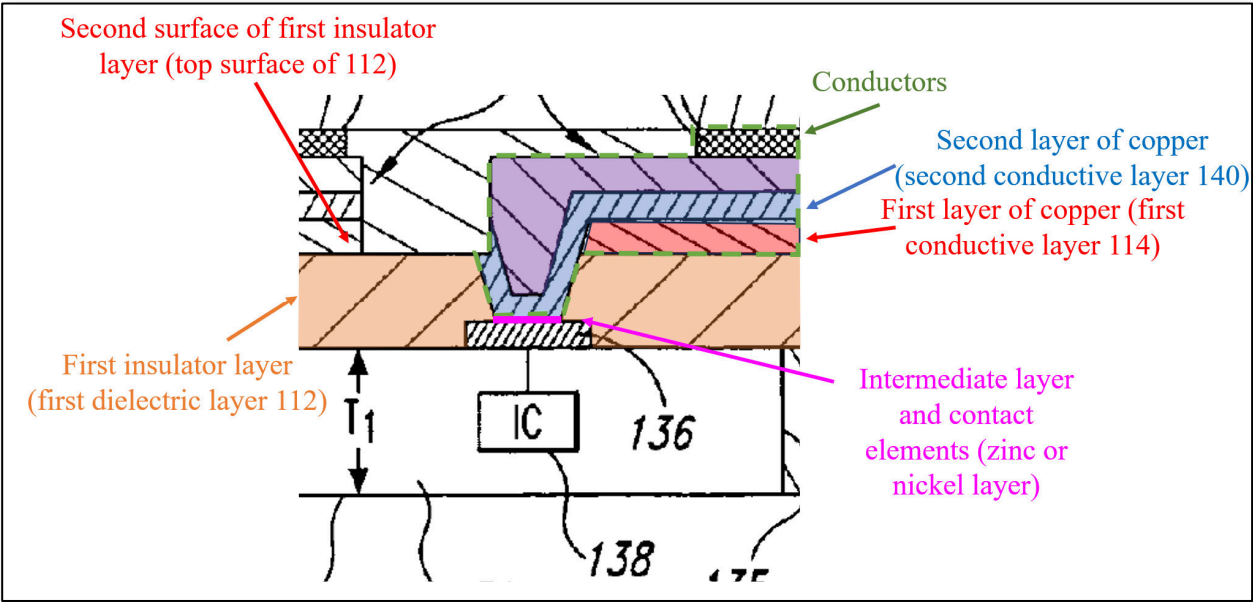
First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none">• First conductive layer 114 (<i>first layer</i>),• Third conductive layer 142, and• Contacts 146 (<i>second layer</i>)	Au	<ul style="list-style-type: none">• “Compatible conductive protective layer” (<i>intermediate layer</i>), and• Second conductive layer 140	Cu

[9]:

See [11] for Ground 2A for why it would have been obvious for layer 140 to be a layer of electroless copper. APPLE-1003, ¶252. Further, although, for claim 1, layer 140 was applied as part of the “*contact elements*,” it is equally valid to apply

layer 140 as a “second layer of copper” of the “conductors.” APPLE-1003, ¶252.

The “copper foil” “first conductive layer 114” is a “first layer of copper on the second surface of the first insulator layer.” Claim 9 is satisfied by the foregoing mappings summarized below. APPLE-1003, ¶253-254.



Portion of Lee FIG. 1E

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none">• First conductive layer 114 (<i>first layer of copper, first layer</i>),• Second conductive layer 140 (<i>second layer of copper, second layer</i>),• Third conductive layer 142, and• Contacts 146	Cu	<ul style="list-style-type: none">• Zinc or nickel layer (<i>intermediate layer</i>)	Zn or Ni

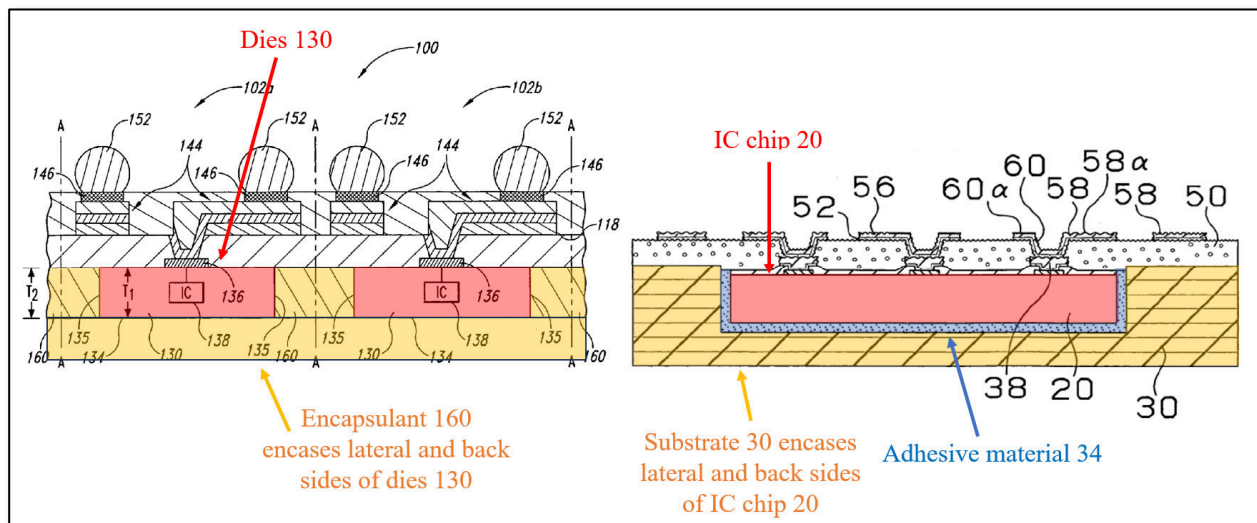
[14]:

It would have been obvious to encapsulate Lee's dies 130 in the substrate 30 of Sakamoto, such that the "*second insulator*" (substrate 30) would contain at least one layer of fibre material and openings in the fibre material for the dies 130.

APPLE-1003, ¶255. Lee discloses that an encapsulant 160 "encases" the dies 130.

APPLE-1015, [0033]; APPLE-1003, ¶255. *See* claim 1. The encapsulant 160 can encase not only the lateral ends 135 of the dies 130 but also the "back sides 134 of the dies." APPLE-1015, [0033]; APPLE-1003, ¶255.

Sakamoto's substrate 30 has a similar configuration, encasing lateral ends and a back side of the IC chip 20 in conjunction with an adhesive material 34, as shown below. APPLE-1005, [0106]-[0108], FIG. 6; APPLE-1003, ¶256.



Left: Lee FIG. 1E; Right: Sakamoto FIG. 6

It would have been obvious, as a matter of design choice, to apply

Sakamoto's configuration to Lee's assembly, for example, by encasing Lee's dies 130 in Sakamoto's substrate 30 and adhesive material 34. APPLE-1003, ¶257. The encapsulant 160 and the substrate 30 serve the same function of encasement (or "contain[ment]") and insulation. APPLE-1005, [0108]; APPLE-1015, [0033]; APPLE-1003, ¶257. Replacing encapsulant 160 with substrate 30 and adhesive material 34 would have been well within the skill of a POSITA with a reasonable expectation of success, especially given Sakamoto's disclosure of the associated materials/manufacturing process. APPLE-1005, [0106]-[0108]; APPLE-1003, ¶257.

As discussed for [14] at Ground 1A, substrate 30 includes "glass cloths" "*contain[ing] at least one layer of fibre material.*" APPLE-1005, [0106]; APPLE-1003, ¶258. Substrate 30, replacing encapsulant 160, would include "*an opening*" in the fibre material for the "*at least one component*" (dies 130), matching the configuration in both Sakamoto's and Lee's structures. APPLE-1005, FIG. 6; APPLE-1015, FIG. 1E; APPLE-1003, ¶258.

XI. GROUND 2C: Claim 3 is obvious over Lee and Eichelberger

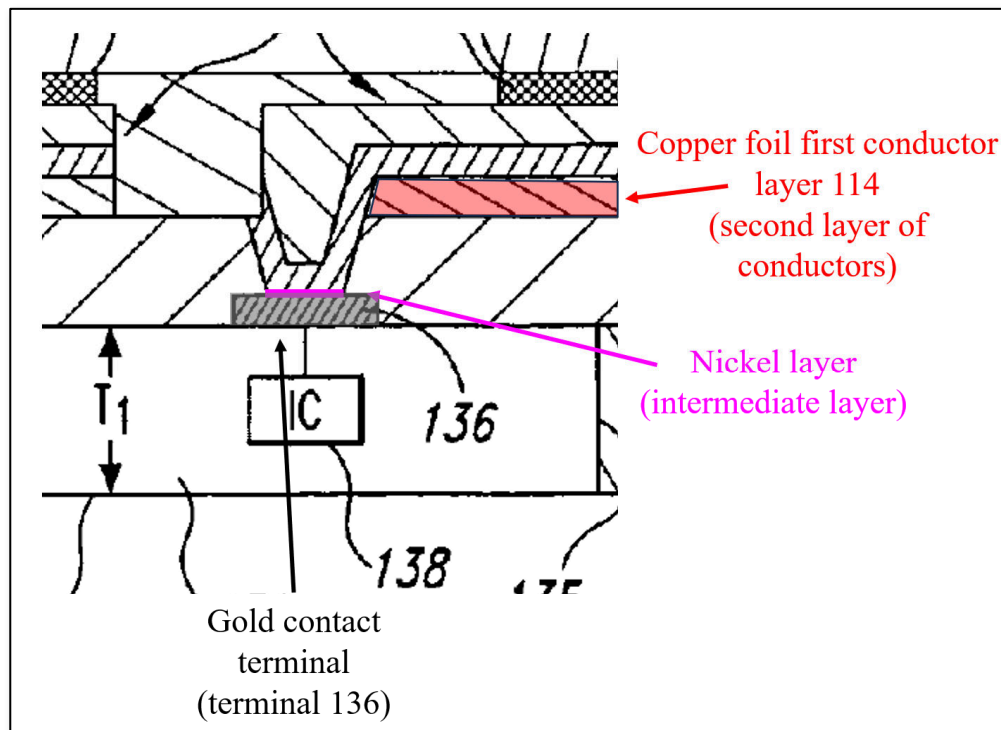
To the extent Sakamoto is found necessary to render obvious the aluminum terminals 136 for claim 1, Sakamoto is included in this ground.

A. Analysis of claim 3

[3]:

It would have been obvious to use gold for Lee's terminals 136, as taught by Eichelberger, such that the terminals contain **gold** as the "*first metal*." APPLE-1003, ¶260-261. Lee does not explicitly disclose a material for the terminals 136 (also referred to as "bond-pads"). APPLE-1015, [0029]; APPLE-1003, ¶260. However, Eichelberger discloses the use of "gold" "bond pads." APPLE-1006, 9:38-58. In selecting a metal for the terminals 136, it would have been obvious for a POSITA to look to Eichelberger's bond pads and to try using the "gold" bond pads disclosed by Eichelberger, for reasons discussed for [3] of Ground 1B. APPLE-1003, ¶260. Having the terminal 136 contain gold would simply be a selection of one of a finite number of identified, predictable materials for bond-pads, and this selection would also provide the advantages discussed for [3] for Ground 1B. APPLE-1006, 9:38-58 APPLE-1003, ¶260.

The copper of Lee's first conductive layer 114 (corresponding to the "*second layer*" of the "*conductors*") is a "*second metal*." See claim 1. Therefore, claim 3 is satisfied based on the *first metal* of the terminals 136 being **gold**, the *second metal* of the "copper foil" first conductive layer 114 being **copper**, and the *third metal* of the "nickel layer" being **nickel**. APPLE-1003, ¶262.



Portion of Lee FIG. 1E

XII. GROUND 2D: Claims 13 and 15 are obvious over Lee and Ito

To the extent Sakamoto is found necessary to render obvious the aluminum terminals 136 for claim 1, Sakamoto is included in this ground.

A. Analysis of Claims

[13]:

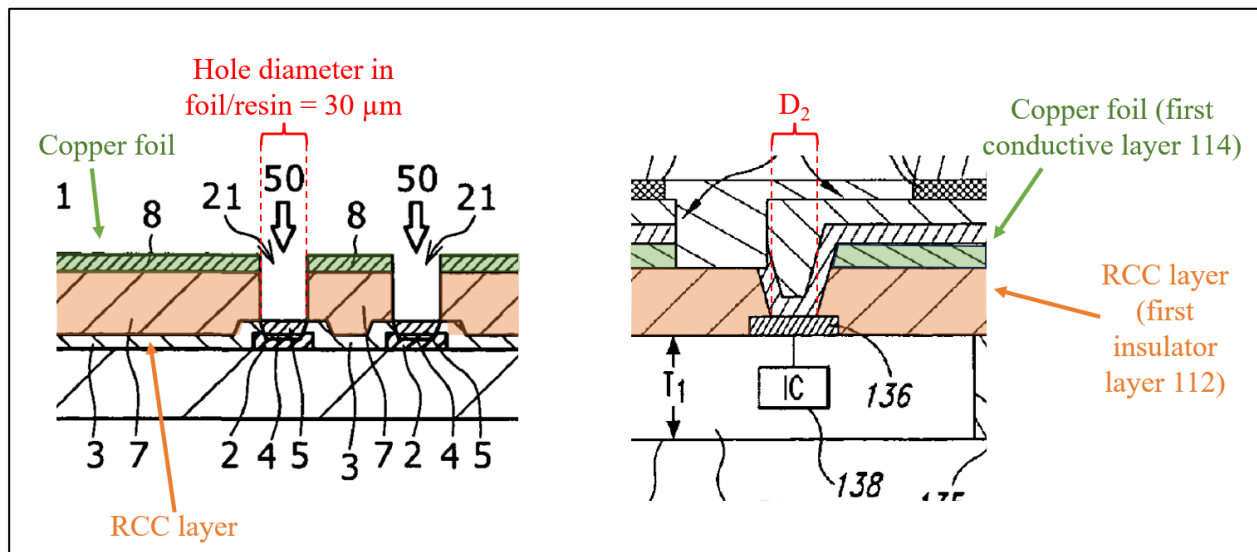
It would have been obvious to apply Ito's element dimensions to Lee's structure, thereby obtaining dimensions satisfying claim 13. APPLE-1003, ¶264. Lee does not disclose dimensions for holes 120, terminals 136, or several layers. It would have been obvious to a POSITA, in selecting these dimensions, to apply Ito's teachings. APPLE-1003, ¶264. First, based on Ito's teaching that "zincating"

on an “aluminum” “terminal electrode” results in “a zinc layer 4 having a thickness of about 0.3 μm ,” it would have been obvious to use the same or a similar thickness for Lee’s “zincation”-formed zinc layer on the “terminals 136.” APPLE-1015, [0030]; APPLE-1012, [0091]; APPLE-1003, ¶265. With the zinc layer applied as the “*contact elements*,” the “*contact elements*” have a height H of about 0.3 μm . APPLE-1003, ¶265.

With respect to width, as discussed in Section VII.C, the “self-aligned” zincation process means that the zinc layer grown by zincation on Lee’s terminal 136 would have a greatest width matching, or effectively matching, the width D_2 (which can be equal to D_1) of the holes 120 in the layers 112/114 that expose the terminals 136. APPLE-1012, [0096]; APPLE-[1015], [0026], [0029]; APPLE-1003, ¶266.

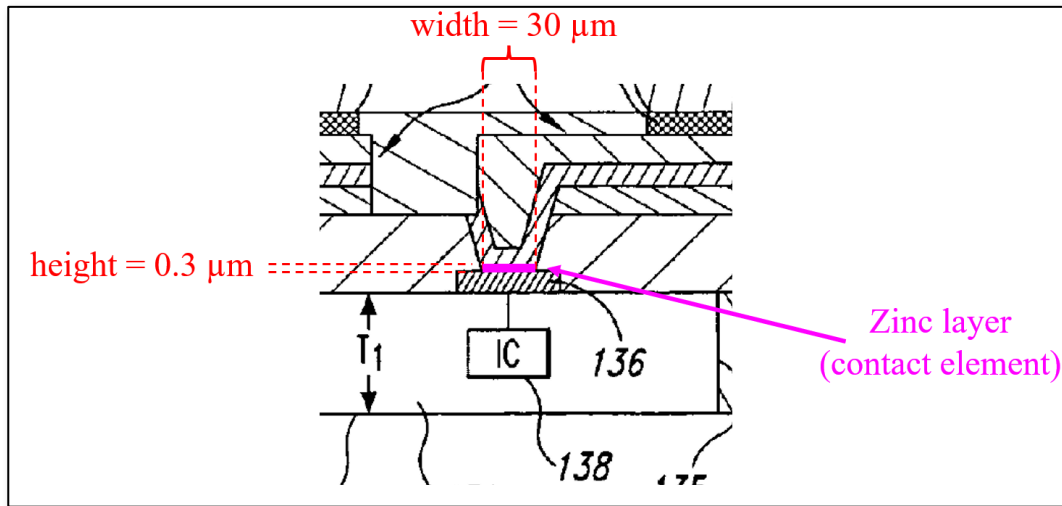
Ito discusses “openings 21” in a combination of an “insulating resin layer 7” and a “copper foil layer 8,” the openings 21 having a “size [] of about 30 μm in diameter.” APPLE-1012, [0138]; APPLE-1003, ¶267. It would have been obvious to apply this or a similar opening size as Lee’s D_1 and D_2 . APPLE-1003, ¶267. Ito’s openings 21 are formed through the same combination of materials as Lee’s holes 120: the openings 21 are through a “resin-coated copper (RCC)” layer 7 and a “copper foil layer 8,” while Lee’s holes 120 are through a “resin coated copper (RCC)” layer 112 and a “copper foil” layer 112. APPLE-1012, [0099], [0107],

[0138]; APPLE-1015, [0026]; APPLE-1003, ¶267. Further, the openings 21 and the holes 120 are both formed using a laser and are used for the same purpose of making contact to underlying terminals. APPLE-1012, [0138]; APPLE-1015, [0028]; APPLE-1003, ¶267-268. This correspondence is illustrated below.



Left: portion of Ito FIG. 4A; Right: portion of Lee FIG. 1E

Therefore, it would have been obvious, as the application of a known technique from Ito to a similar device structure in Lee, to apply Ito's hole size of "about 30 μm" as Lee's diameter D₁ and/or D₂. APPLE-1012, [0138]; APPLE-1003, ¶269. Based on this dimension, Lee's zinc layer (*contact element*) has a height of 0.3 μm and a maximum width of about 30 μm, satisfying claim 13. APPLE-1003, ¶269.



Portion of Lee FIG. 1E

First metal (of terminals 136)	Conductors	Second metal	Contact elements	Third metal
Al	<ul style="list-style-type: none"> • First conductive layer 114 (<i>second layer</i>), • Third conductive layer 142 (<i>first layer</i>), and • Contacts 146 	Cu	<ul style="list-style-type: none"> • Zinc layer (<i>intermediate layer</i>) 	Zn

[15]:

It would have been obvious to provide Ito's "first passivation layer 101" on the top surface of Lee's dies 130, with contact holes for the terminals 136, in order to passivate the surface. APPLE-1003, 270.

XIII. GROUND 2E: Claims 15-16, 18, and 20 are obvious over Lee and Tuominen

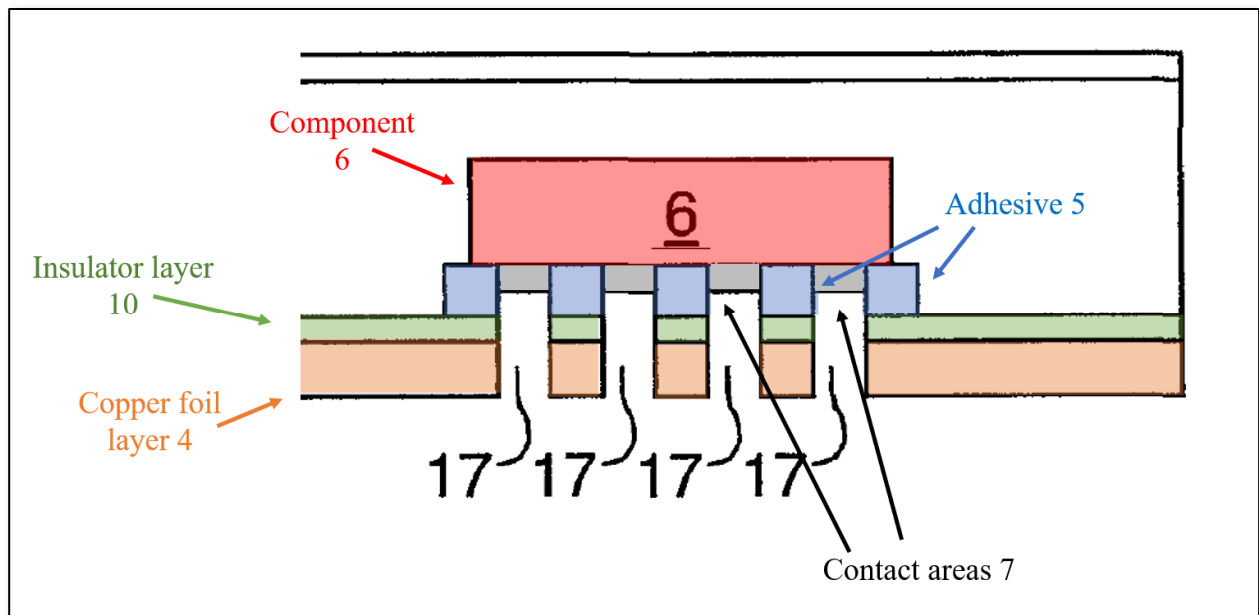
To the extent Sakamoto is found necessary to render obvious the aluminum

terminals 136 for claim 1, Sakamoto is included in this ground.

A. Analysis of Claims

[15]:

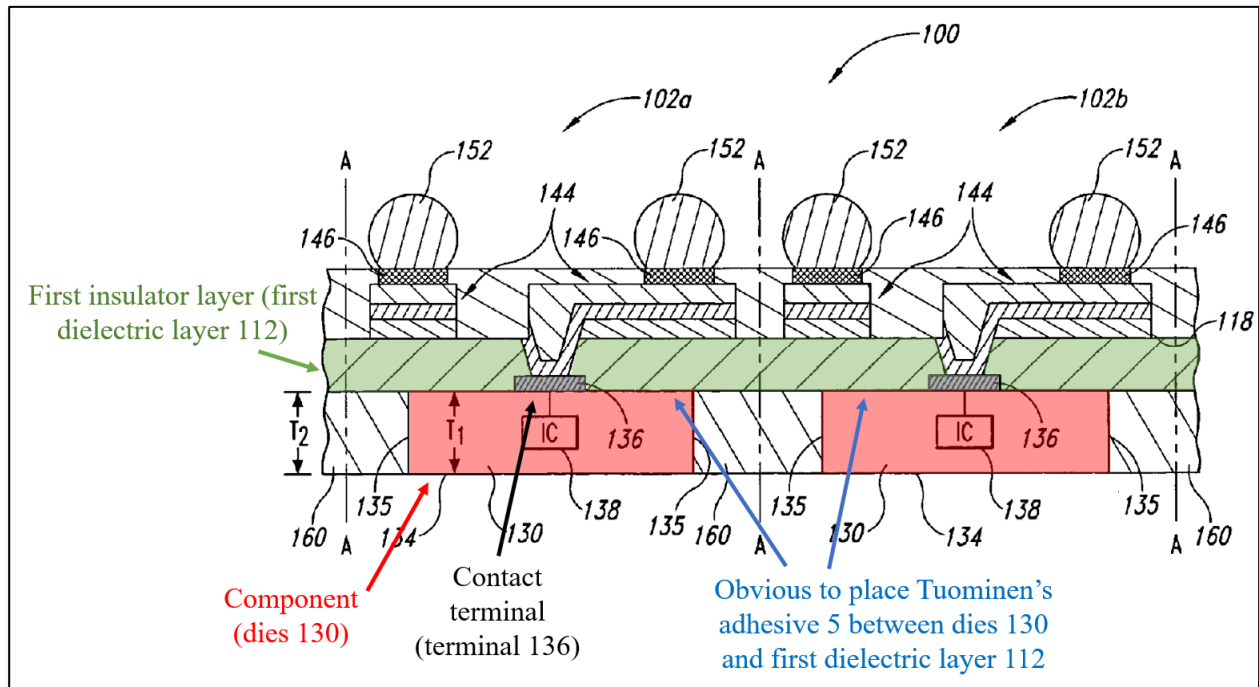
It would have been obvious to use Tuominen's "adhesive 5" (shown in FIG. 9) to attach Lee's dies 130 to Lee's first dielectric layer 112, such that the adhesive (a "*polymer layer*") is between the "*first insulator layer*" (first dielectric layer 112) and the "*at least one component*" (dies 130) and includes "*contact holes*." APPLE-1003, ¶272.



Portion of Tuominen FIG. 9

The structures being attached are essentially the same: Lee attaches dies 130 to a combination of a first dielectric layer 112 and a copper foil 114, whereas Tuominen attaches components 6 to a combination of an insulator layer 10 and a

copper foil layer 4. APPLE-1015, [0026]; APPLE-1014, 5:3-11; APPLE-1003, ¶273. And Lee describes that, although the first dielectric 112 may have adhesive properties that allow attachment “without an adhesive,” “in other embodiments [] the microelectronic device assembly may include an adhesive for attaching the dies 130 to the substrate 110.” APPLE-1015, [0029]; APPLE-1003, ¶273. It would have been obvious, in these “other embodiments,” to apply Tuominen’s known method, including the use of the adhesive 5, to obtain the predictable result of the dies 130 attached to the first dielectric layer 112 by the adhesive 5. APPLE-1003, ¶273.



Lee FIG. 1E

Tuominen’s adhesive 5 is “a thermally hardening epoxy,” a polymer.

APPLE-1014, 8:8; APPLE-1003, ¶274. As a result, when the adhesive 5 is used to

attach Lee's dies 130 to Lee's first dielectric layer 112, the resulting structure would include "*a polymer layer*" (adhesive 5) between the "*first insulator layer*" (dielectric layer 112) and "*the at least one component*" (dies 130). APPLE-1003, ¶274. "*Contact holes for the contact elements*" (terminals 136) would be present in the adhesive to permit electrical connection to the dies 130, matching the configuration of contact holes in Tuominen's adhesive 5 and Lee's first dielectric layer 112. APPLE-1014, FIG. 9; APPLE-1015, FIG. 1E; APPLE-1003, ¶274.

[16]:

It would have been obvious to have Tuominen's adhesive 5, integrated into Lee's structure as discussed with respect to [15], be a "*hardened adhesive*." APPLE-1003, ¶275. Tuominen describes that the adhesive 5 is a "**thermally hardening epoxy**" that can undergo a "*final hardening*." APPLE-1014, 8:8-21. Tuominen also discusses that "*after spreading the adhesive hardens or can be hardened at least partly, in such a way that the adhesive can hold the component in place*." APPLE-1014, 7:18-26. It would have been obvious for a POSITA to harden the adhesive to obtain the predictable, desirable result of securing Lee's first dielectric layer 112 to Lee's dies 130, as taught by Tuominen. APPLE-1003, ¶275.

[18], [20]: See [15] for Ground 2E.

XIV. DISCRETIONARY CONSIDERATIONS

Discretionary denial under *Advanced Bionics* is not warranted. Neither Sakamoto nor Lee was applied/addressed during prosecution, or even listed on the face of the '324 Patent. *See* APPLE-1002.

EP1259103, in the same family as Sakamoto, was cited by the applicant during prosecution of Application No. 12/990,785, the parent application to the '324 Patent. APPLE-1018, 407. However, this reference was not applied in any rejection, or otherwise meaningfully addressed, during prosecution of that application. APPLE-1018, 17-59. Further, the claims considered in the parent application differ substantially from at least the independent claims of the '324 Patent. *See* APPLE-1018, 32-38. As such, part one of the *Advanced Bionics* framework is not satisfied.

Moreover, the examiner's failure to apply EP1259103 during prosecution was erroneous, such that part 2 of the *Advanced Bionics* framework is not satisfied. For example, the examiner failed to appreciate that Sakamoto discloses first, second, and third metals arranged as recited in claim 1, or that Sakamoto FIG. 7(A) directly illustrates the "*surface area*" elements of claim 1. The omission of EP1259103 or Sakamoto from any applied rejection and failure to consider its teachings constitutes material error.

XV. *Fintiv* Factors Weigh in Favor of Institution

The *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. Motion to Transfer to the Northern District of California is pending. While a motion to stay has not been filed, and the PTAB does not infer how the district court would rule, the pending motion at least increases the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11, 10-11 (May 19, 2021).

Factor 2 favors institution. The Board will likely issue its Final Written Decision by about August 2026, several months before the median time-to-trial in WDTX (November 2026, based on median time of 33.1 months). The trial date is uncertain and subject to change due to a number of factors, including the pending transfer motion. APPLE-1036.

Factor 3 favors institution because Petitioner has diligently filed this Petition while the litigation remains in its early stages.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the District Court, which mitigates against duplication of effort and serves efficiency/integrity goals. Same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds.

XVI. PAYMENT OF FEES – 37 C.F.R. §42.103

Petitioner authorizes the Patent and Trademark Office to charge any fees to

Deposit Account No. 06-1050.

XVII. CONCLUSION

The Challenged Claims should be canceled.

XVIII. MANDATORY NOTICES UNDER 37 C.F.R §42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. §42.8(b)(1)

Apple is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. §42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or pending petitions for *inter partes* review for the '324 Patent. The '324 Patent is the subject of: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024; *Samsung Electronics Co., Ltd. et al v. ImberaTek LLC*, IPR2023-00055 (PTAB), filed October 17, 2022; and *ImberaTek LLC v. Samsung Electronics Co., Ltd. et al.*, 2-22-cv-00233 (EDTX), filed June 24, 2022.

C. Lead And Back-Up Counsel Under 37 C.F.R. §42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0197IP1@fr.com.

Respectfully submitted,

Dated: February 6, 2025

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CERTIFICATION UNDER 37 CFR §42.24

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,917 words, which is less than the 14,000 allowed under 37 CFR §42.24.

Dated: February 6, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via USPS Priority Express, to the Patent Owner by serving the correspondence address of record as follows:

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