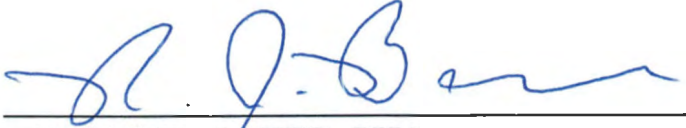


**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent of: Tuominen et al.  
U.S. Patent No.: 11,071,207 Attorney Docket No. 50095-0198IP1  
Issue Date: July 20, 2021  
Appl. Serial No.: 17/005,527  
Filing Date: August 28, 2020  
Title: ELECTRONIC MODULE

**DECLARATION OF DR. R. JACOB BAKER**

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: 2/5/2025 By:   
R. JACOB BAKER, PH.D., P.E.

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I, R. Jacob Baker, Ph.D., P.E., do hereby declare:

1. I am making this declaration at the request of Apple in the matter of *INTER PARTES* REVIEW OF U.S. PATENT No. 11,071,207.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

**I. MATERIALS CONSIDERED**

3. In preparing this Declaration, I considered the following materials:

- U.S. Patent No. 11,071,207 (APPLE-1001), and its accompanying prosecution history (APPLE-1002)
- U.S. Patent No. 5,616,520 to Nishiuma et al. (“Nishiuma”) (APPLE-1004)
- U.S. Publication No. 2002/0149117 to Shibata et al. (“Shibata”) (APPLE-1005)
- U.S. Patent No. 6,555,758 to Stelzl et al. (“Stelzl”) (APPLE-1006)
- U.S. Publication No. 2002/0159242 to Nakatani et al. (“Nakatani”) (APPLE-1007)
- Japanese Patent Publication No. 2001-085473 to Onda with Certified Translation (“Onda”) (APPLE-1008)

- Japanese Patent Publication No. 11-191574 to Matsuda with Certified Translation (“Matsuda”) (APPLE-1009)
- U.S. Patent No. 4,912,844 to Parker (“Parker”) (APPLE-1010)
- U.S. Publication No. 2003/0034557 to Gupta et al. (“Gupta”) (APPLE-1011)
- Johnson et al., *High Speed Digital Design: A Handbook of Black Magic*, Prentice Hall PTR, Englewood Cliffs, New Jersey 07632 © 1993 (APPLE-1012)
- U.S. Patent No. 4,068,022 to Glick (“Glick”) (APPLE-1020)
- J.A. Scarlett, *The Multilayer Printed Circuit Board Handbook*, Electrochemical Publications Limited, 8 Barns Street, Ayr Scotland © 1985 (APPLE-1021)
- J.A. Scarlett, *An Introduction to Printed Circuit Board Technology*, Electrochemical Publication Limited, 8 Barns Street, Ayr Scotland © 1984 (APPLE-1022)
- U.S. Patent No. 6,548,330 (“Murayama”) (APPLE-1023)
- U.S. Patent No. 6,011,313 (“Shangguan”) (APPLE-1024)
- U.S. Publication No. 2021/0037654 (“Tuominen Pub.”) (APPLE-1026)
- U.S. Patent No. 5,060,051 to Usuda (“Usuda”) (APPLE-1034)

- William D. Callister, Jr., *Materials Science and Engineering: An Introduction*, 5<sup>th</sup> Ed., John Wiley & Sons, Inc. © 2000 (APPLE-1035)
- Simon Thomas, *3D-Integration: Trends and Opportunities – An Overview* (Materials Research Society 2003) (APPLE-1036)
- R. Kujala, et. al., *Solderless Interconnection and Packaging Technique for Embedded Active Components* (IEEE 1999) (APPLE-1037)
- U.S. Patent Publication No. 2001/0026010 to Horiuchi (“Horiuchi”) (APPLE-1038)
- U.S. Patent No. 6,038,133 to Nakatani et al. (“Nakatani-II”) (APPLE-1039)
- U.S. Patent No. 5,250,843 to Eichelberger (“Eichelberger”) (APPLE-1040)
- International Patent Application WO1996012296 to Suwa et al. and Certified Translation (“Suwa”) (APPLE-1041)
- Exhibit 17 to Complaint for Patent Infringement – Infringement Claim Chart for ’207 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-17 (APPLE-1105)

## **II. QUALIFICATIONS AND BACKGROUND**

4. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). My curriculum vitae is provided (as Appendix A).

5. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistance Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

6. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera

sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

7. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My more recent industry experience includes working with Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

8. I have taught courses in integrated circuit design (analog, digital, mixed signal, memory circuit design, etc.), linear circuits, microelectronics,

communication systems, power electronics, and fiber optics. I have been the main advisor to over 100 Master's and Doctoral students.

9. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have also authored, or coauthored, more than 100 papers and presentations in the areas of electronic circuit design. I am the named inventor on over 150 granted U.S. patents.

10. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

11. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

12. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University.

13. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

14. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching integrated circuit packaging and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art.

### **III. RELEVANT LEGAL STANDARDS**

15. I have been asked to provide my opinions as to whether claims 1-6 of the '207 Patent would have been obvious to a person of ordinary skill in the art as of the earliest claimed priority date of the '207 patent (February 26, 2003) ("Critical Date").

16. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the '207 patent. In addition, I understand that the following legal principles apply.

17. It is my understanding that, in determining whether claims of the '207 patent are obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the

relevant art. A person of ordinary skill in the art would read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

18. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

19. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

20. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that

one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

21. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

#### **IV. TECHNOLOGY BACKGROUND**

##### **A. Semiconductor Component Modules**

22. Persons of ordinary skill in the art (POSITAs) have continuously looked for solutions to provide multiple component integration into electronic modules to provide higher levels of system functionality without added signal

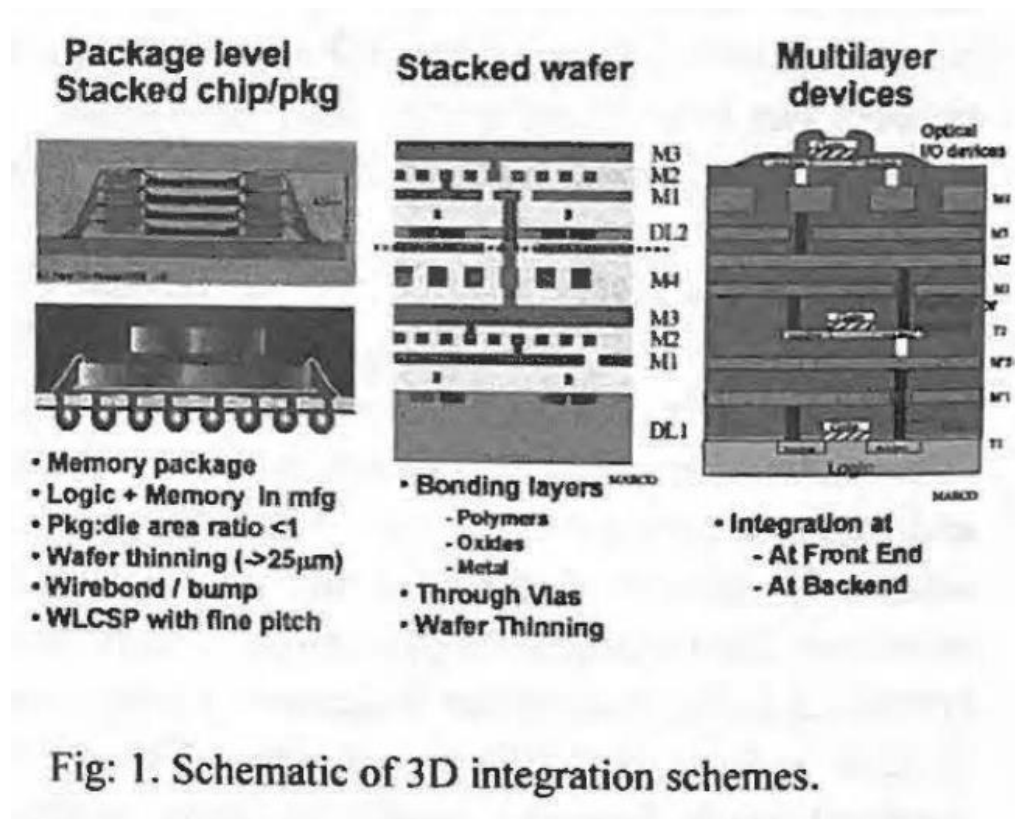
delay and power dissipation in order to integrate components (such as transistors) in integrated circuits in accordance with Moore's law. APPLE-1036, Abstract; *see also generally* APPLE-1021 (describing background of multilayer printed circuit boards). As Simon Thomas explained, "[t]he growth of the semiconductor industry has historically depended on the integration of more components on a chip through transistor and interconnects scaling and manufacturing technology." APPLE-1036, 1. "Three-dimensional integration (3D) of components" including "stacking chips/packages, stacking wafers, and fabrication of multiple device layers on the same wafer" offer pathways toward enhanced integration of components with smaller footprints. *Id.*, 1, 2, 4 (reporting that "stacked chip devices are in production" as of the 2003 publication of the conference proceedings).

23. Thomas describes that functionality has increased through "System-on-Chip (SoC) and System in Package (SiP) approaches." *Id.*

In addition, the increasing drive to integrate diverse component technologies for enhanced SoC functionality, presents a multitude of technical and business challenges. For example, a single chip SoC for a cell phone handset could require GaAs, MEMS, digital, analog, power, and passives technologies. RF circuits integrated with microprocessor in a 3D format, to facilitate wireless communication, has attracted major interest. Another motivation for 3D is the need to reduce footprint of the packaged device, especially for portable applications. There are multiple technology approaches for 3-D integration, currently at varying levels of maturity and each with its own unique strengths and issues. These approaches include [Fig: 1]: - Stacked chips or stacked packages - Stacked wafers through

wafer bonding - Device fabrication in multiple planes on the same wafer.

APPLE-1036, 2.



APPLE-1036, 2

24. Nakatani-II exemplifies how stacking multiple wafers on top of each other was a well-known technique for achieving multiple component integration in a module. For example, Nakatani-II's Figure 4 shows a three layered "built-in module":

Referring to FIG. 4, the circuit component built-in module 400 in Embodiment 4 includes an insulating substrate 401 comprising insulating substrates 401a, 401b and 401c, wiring patterns 402a, 402b, 402c and 402d formed on one principal

plane and in the internal portion of the insulating substrate 401, a circuit component 403 arranged in the internal portion of the insulating substrate 401 and connected to the wiring patterns 402a, 402b or 402c, and an inner via 404 for electrical connection between the wiring patterns 402a, 402b, 402c and 402d.

APPLE-1039, 11:12-22.

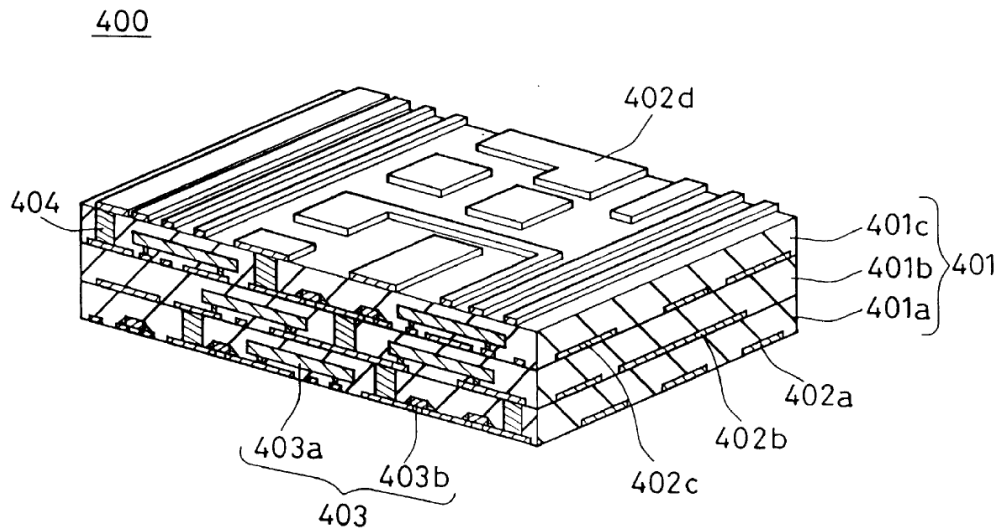


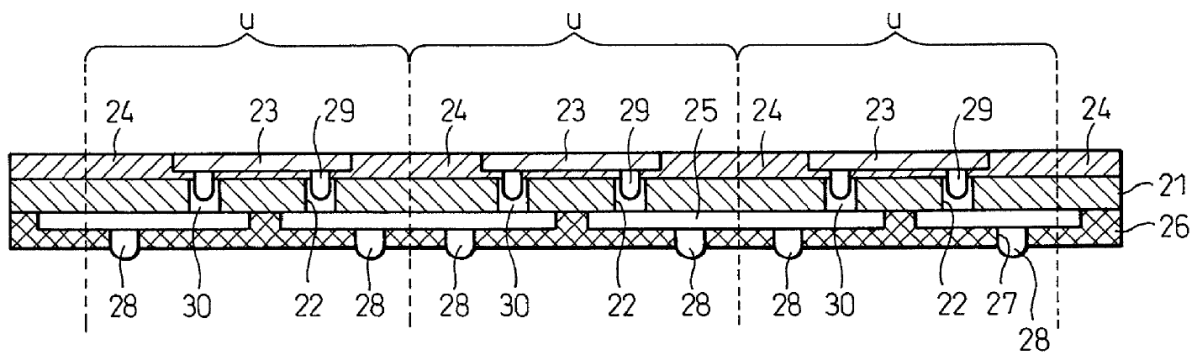
FIG. 4

**APPLE-1039, FIG. 4**

25. “A plurality of semiconductor devices... may be stacked in layers... to form a thin multilayer semiconductor device” in U.S. Patent Application Publication No. 2001/0026010 to Horiuchi et al. (“Horiuchi”). APPLE-1038, [0105]. Horiuchi describes a method including producing an initial structure containing multiple electrical components which are then “cut into semiconductor package units ‘u’... to obtain individual semiconductor devices 20.” *Id.*, [0101],

[0115], [0127], [0143], [0154]. For example, Horiuchi's Figure 9 (reproduced below) shows semiconductor elements 23 which are bonded and mounted to the top surface of tape substrate 21 "by heating the semiconductor elements 23 to a temperature near the melting point of the low melting point metal 30 and pushing the connection terminals 29 into the low melting point metal 30 in the through holes 22." *Id.*, [0094]. "A sealing resin layer 24 covering the top surface of the tape substrate 21" is then ground and polished to a predetermined thickness. *Id.*, [0097]-[0099]. After the grinding and polishing, the external connection terminals 28 are formed and the "assembly is cut into semiconductor package units 'u' at the positions shown by the broken lines in FIG. 9 to obtain individual semiconductor devices." *Id.*, [0100]-[0101].

Fig.9



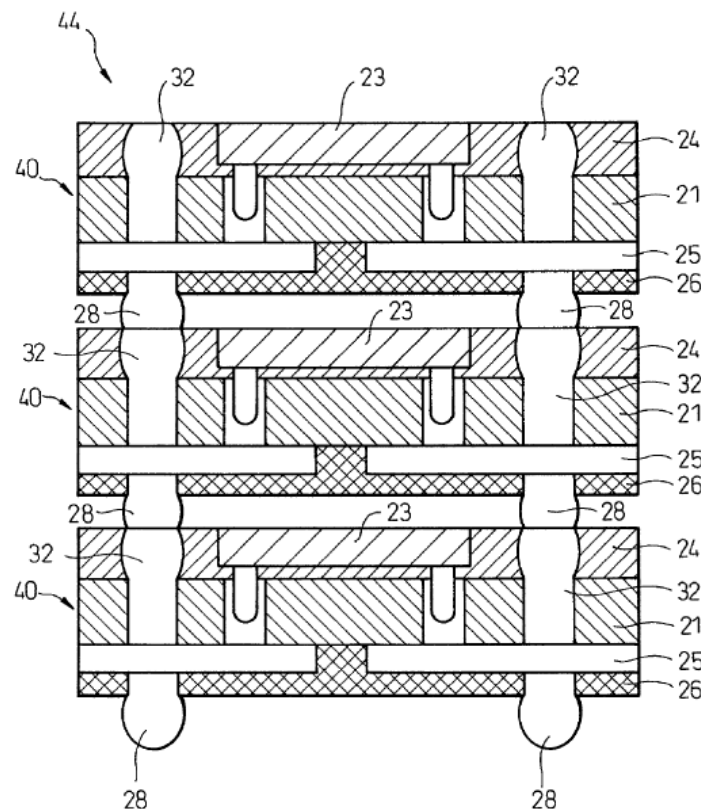
APPLE-1038, FIG. 9

26. Following the cutting procedure, Horiuchi's cut semiconductor devices "may be stacked in layers as shown in FIG. 11 to form a thin multilayer semiconductor device 44" by:

connecting the top ends of the low melting point metal conductors 32 of a bottom semiconductor device 40 and the bottom ends of the external connection terminals 28 of a top semiconductor device 40, a single semiconductor device 4 comprised of an integral circuit including a plurality of semiconductor elements 23 (in this example, three) in a multilayer structure is formed.

APPLE-1038, [0105].

Fig.11



APPLE-1038, FIG. 11

27. As Thomas notes, “[a]nother interesting concept of multilayer device integration is to build active devices within an interconnect level.” APPLE-1036, 6-7. This type of technology had “become increasingly attractive” during the 90’s. APPLE-1037, 1.

28. One way that chip density was increased was by preparing cavities in a circuit board and positioning semiconductor components within the cavities, thereby decreasing a required size of the semiconductor module. For example, in 1999, A. Kujala, R. Tuominen, and J.K. Kivilahti, explained that, “General Electric (GE) introduced high density interconnection technology for embedded chips. HDI technology is a ‘chip first’ solution where active components are placed in cavities formed in a ceramic or embedded into plastic encapsulant.” APPLE-1037, 1. As shown below in Figure 2, the chips are interconnected through laser ablated vias. *Id.*, 2. “The HDI technology enables the fabrication of complex [multi-chip modules] with a very high packaging density and low interconnect impedance” while providing “good protection both mechanically and chemically.” *Id.*

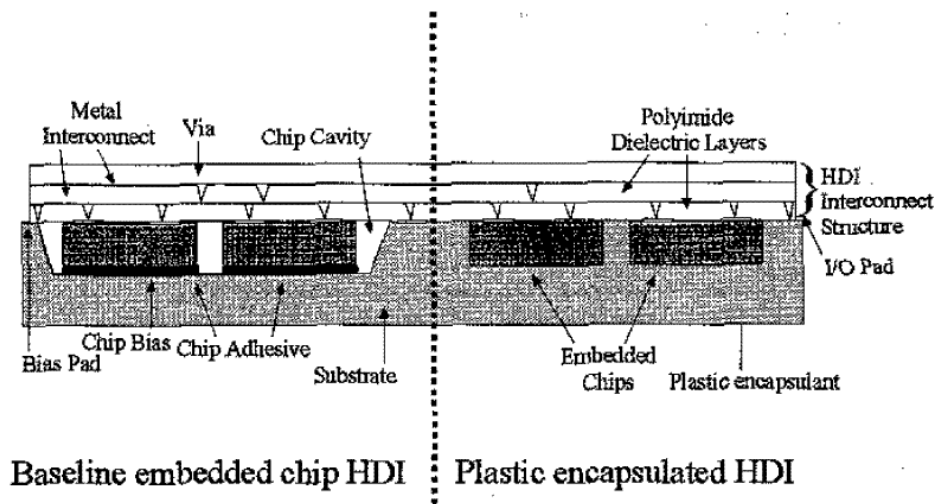
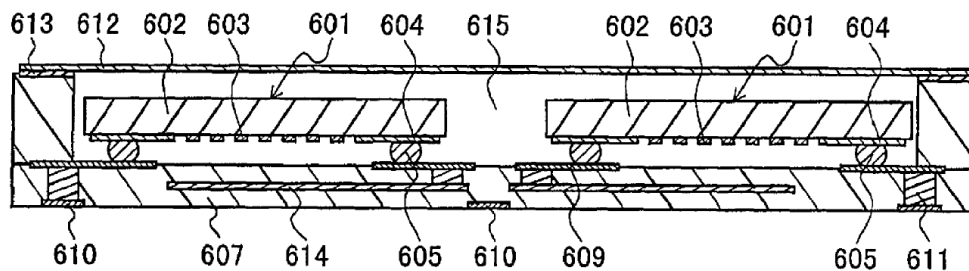


Fig. 2 Schematic presentation of embedded HDI chips [5].

**APPLE-1037, FIG. 2**

29. Kujala et al. further describe that in conventional fabrication methods, “[h]igh interconnection density is achieved with MCM [multi chip module] technology where fine patterned copper layers and dielectric layers are fabricated on various substrates [and] [i]ntegrated circuits are then connected to MCM substrate with wire bond, TAB or flip chip solder bumps.” APPLE-1037, 1. They then describe methods that use “gold bump[s] interconnected to copper wire” for fabrication of MCM components using solderless methods. *Id.*, 3-4.

30. In another example, Nakatani, Eichelberger, Suwa, and Nakatani-II show mounting multiple chips in a single layer. Specifically, due to the increased demand for smaller-sized and higher-density circuit boards, Nakatani discloses “at least two electric elements (203) such as semiconductor chips or surface acoustic



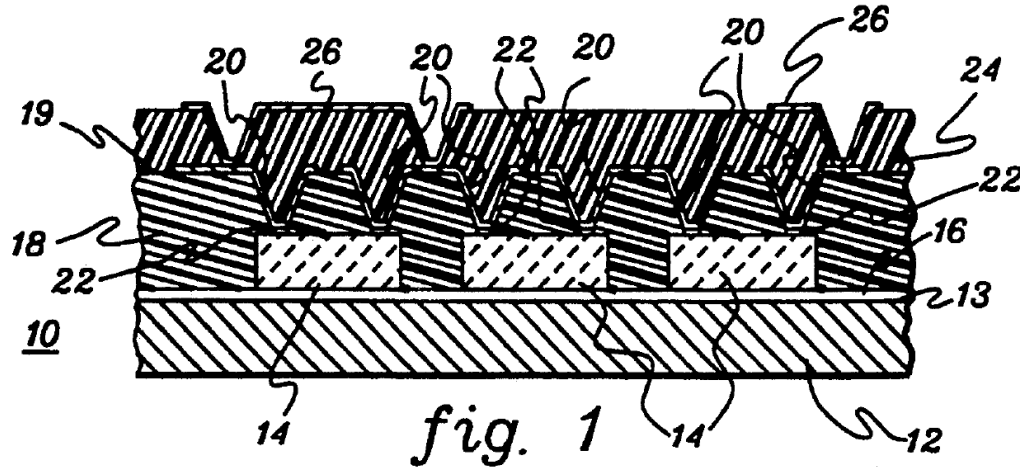
**APPLE-1007, FIG. 7**

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substrate and an electrically conductive material may be disposed in the grooves to communicate with the electrical components.” APPLE-1010, Abstract, 1:49-51, 1:57-66, 2:10-13, FIGS. 1-4. By providing “cavities ... in the printed circuit board to receive electrical components, preferably in a tight-fit relationship in the cavities” space on the printed circuit board can be conserved. *Id.*, 1:49-51, 2:64-3:9, 3:27-42.

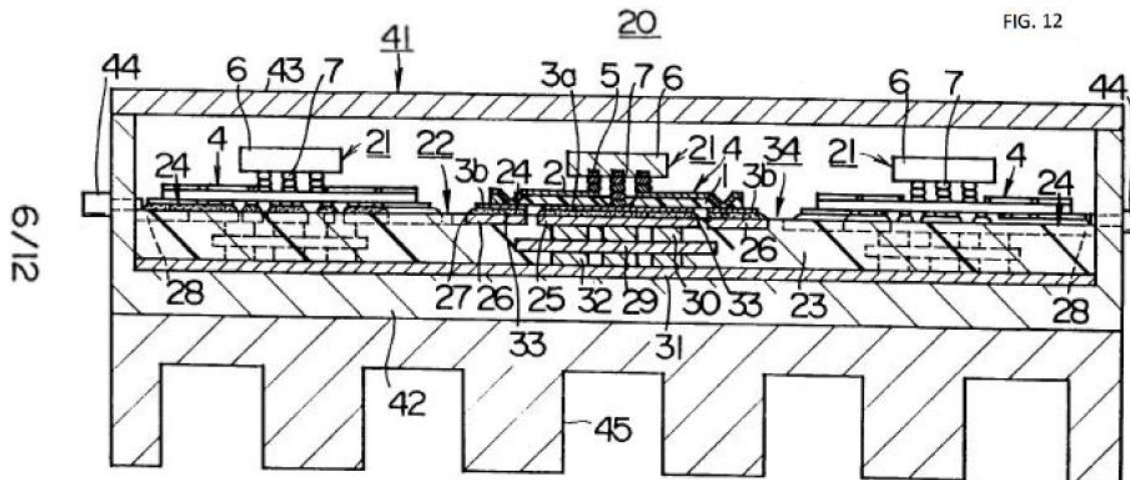
32. Such tight-fit relationships between a cavity and electrical components were conventional for the space-saving reasons described by Parker, and for other reasons including keeping wire bonds short to reduce parasitic effects. APPLE-1011, [0034] (“the cross-sectional dimensions of cavity portion 12... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12”). For example, Gupta describes that in some cases “[t]he height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier.” *Id.*, [0017], [0034], FIGS. 4, 7, 8. Further “[t]he cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.” *Id.*, [0017], [0018], [0038], [0044].

33. Similarly, U.S. Patent No. 5,250,843 to Eichelberger discloses a “multichip integrated circuit package comprises a substrate having a flat upper surface to which is affixed one or more integrated circuit chips having interconnection pads.” APPLE-1040, Abstract. As shown below in Figure 1, Eichelberger’s multichip module includes multiple semiconductor components 14 arranged in one single layer and in a tight-fit relationship with the surrounding insulating polymer encapsulate 18. Eichelberger’s multichip module structure has high I/O capacity with optimal heat removal, has been optimized for speed, and has the ability to incorporate an assortment of components of varying thickness and functions into the module. *Id.*, 1:17-27.



APPLE-1040, FIG. 1

34. International Patent Application WO1996012296 to Suwa et al. (“Suwa”) also discloses a multi-chip module. See APPLE-1041. Suwa’s multi-chip module (MCM) 20 is provided with a plurality of chip assemblies 21 “in



35. As I explained above, Nakatani-II also exemplifies multiple components in a single insulating substrate layer. As shown in Figure 1, Nakatani-II's circuit components 103 are "connected to the wiring pattern 102b and arranged in the insulating substrate 101, and an inner via 104 for electric connection between the wiring patterns 102a and 102b." APPLE-1039, 6:67-7:3.

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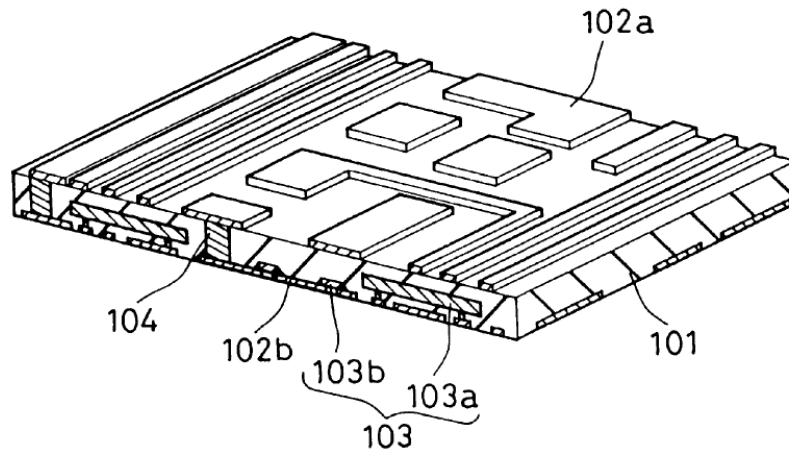


FIG. 1

**APPLE-1039, FIG. 1**

36. In summary, it was well-recognized by POSITAs to mount chips in a cavity of a substrate.

**B. Bonding Techniques**

37. Preparation of a semiconductor package or chip requires that components be electrically connected to wiring patterns on a printed circuit board or other substrate, so that the package or chip can be supplied with power and be grounded, as well as connecting the package or chip to other components. APPLE-1022, 6 (“A printed circuit board is a piece of plastic material on which electronic components can be mounted for mechanical support, and which also electrically

interconnects all the components it supports by means of a pattern of metal tracks on its outer surfaces and sometimes on inside layers”). By the Critical Date, a variety of techniques for bonding components to wiring of printed circuit boards were well known and in use, including solderless techniques including ultrasonic bonding and thermocompression. *See e.g.*, APPLE-1037 (1999 article in IEEE reporting on “Solderless Interconnection and Packaging Technique for Embedded Active Components”). The ’207 patent does not purport to have invented these techniques, and indeed, ultrasonic and thermocompression bonding techniques (i.e., “solderless techniques”) were well-known years before the filing date of the ’207 patent. *Id.*; APPLE-1001, 6:48-50 (“Methods and equipment for ultrasonic bonding are commercially available.”), 6:65-67 (“Methods and equipment for thermo-compression bonding are also commercially available”).

**i. Ultrasonic Bonding**

38. The ’207 patent offers the following description of ultrasonic bonding:

The ultrasonic method then refers to a method, in which two pieces containing metal are pressed against each other while vibration energy at an ultrasound frequency is brought to the area of the joint. Due to the effect of the ultrasound and the pressure created between the surfaces to be joined, the pieces to be joined are bonded metallurgically. Methods and equipment for ultrasonic bonding are commercially available. Ultrasonic bonding has the advantage that a high temperature is not required to form a bond.

APPLE-1001, 6:43-51.

Ultrasonic bonding techniques combine ultrasonic vibrations and heat or pressure to bond two metal components to one another. For example, Matsuda describes a technique that combines ultrasonic methods with thermocompression. Matsuda describes that electrodes 4 of a semiconductor chip are aligned with metal bumps 5 (e.g., Ni or Au) formed on a substrate and then the pieces are “subjected to pressure by a bonding tool while applying ultrasonic vibrations and heat.”

APPLE-1009, [0007], [0006], [0012]. “The bumps 5 are deformed to form an Au/Al alloy on the contact surface, and the chip electrodes 4 and bumps 5 are thermocompressed.” *Id.*, [0007], [0013], FIGS. 2A-B.

## **ii. Thermo-compression Bonding**

39. Similarly, the '207 patent gives the following description related to thermo-compression bonding methods:

The term thermo-compression method refers in turn to a method, in which two pieces containing metal are pressed against each other while thermal energy is brought to the area of the joint. The effect of the thermal energy and the pressure created between the surfaces to be joined cause the pieces to be joined to be bonded metallurgically. Methods and equipment for thermo-compression bonding are also commercially available.

*Id.*, 6:60-67.

40. Glick explains that “[t]hermocompression bonding is a solid-phase bonding technique which forms the bond between two members by inducing a

suitable amount of material flow in one or both members.” APPLE-1020; 3:33-36.

“[M]aterial flow [between the two members] is induced by the application of heat and pressure, which are maintained for a suitable length of time so that adhesion takes place without the presence of a liquid phase.” *Id.*, 3:36-39.

## **V. PERSON OF ORDINARY SKILL IN THE ART**

41. It is my understanding that when interpreting the claims of the '207 patent I must do so based on the perspective of one of ordinary skill in the art at the time of the alleged invention (“POSITA”). For purposes of my analysis in this declaration, I have been asked to assume that the priority date of the '207 patent is February 26, 2003 (“Critical Date”). I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

42. Taking these factors into consideration, it is my opinion that one of ordinary skill in the art would have had at least a Bachelor’s degree in electrical engineering, materials science, applied physics, or a related technical field, and at

least 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. Additional graduate education could substitute for professional experience, or additional professional experience could substitute for formal education.

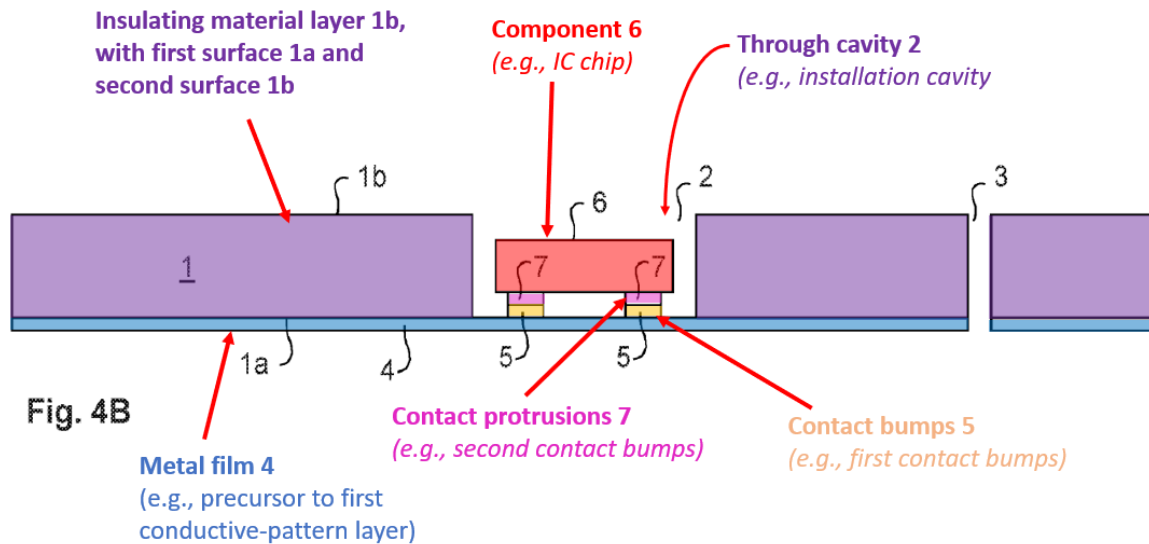
43. I have possessed the qualifications of a POSITA since the Critical Date of the '207 patent, and long before.

## **VI. OVERVIEW OF THE SUBJECT PATENT US11,071,207, “THE '207 PATENT”**

44. The '207 patent is titled Electronic Module. It was filed on August 28, 2020 and is a continuation of U.S. Application No. 16/104,979 (filed on August 20, 2018; now U.S. Patent No. 10,765,606), which is a continuation of U.S. Application No. 14/467,079 (filed on August 25, 2014; now U.S. Patent No. 10,085,345), which is a continuation-in-part of U.S. Application No. 12/603,324 (filed on October 21, 2009; now U.S. Patent No. 8,817,485), which is a continuation-in-part of U.S. Application No. 11,907,795 (filed October 17, 2007; now U.S. Patent No. 7,609,527), which is a continuation of U.S. Application No. 10/546,820 (filed February 25, 2004, now U.S. Patent No. 7,299,546). APPLE-1001, Cover. The '207 patent also claims priority to a Finnish application (20030292) filed on February 26, 2003. *Id.*

45. The '207 patent describes “an electronic module which includes one or more components embedded in an installation base.” APPLE-1001, 1:25-26.

The '207 patent describes a method in which “unpackaged components, such as semiconductor components and particularly microcircuits, can be attached and connected reliably and economically to their installation base.” *Id.*, 3:8-12.



**APPLE-1001, FIG. 4B (annotated)**

46. In an example, the specification describes a method for forming an electronic module such as a circuit board in which “through cavities 2, selected to suit the size of the components 6 to be installed, are made in [an] insulating material layer 1.” *Id.*, 6:14-16. “An unpatterned metal film 4, which acts as the conducting surface of the installation base for the components 6 to be installed and connected is made on the first surface 1a of the insulating substance layer 1.” *Id.*, 6:23-26.

47. “The metal film 4 can be manufactured, for example, by laminating copper (Cu) [or] can also be a surfaced metal film, or some other film including

several layers or several materials.” *Id.*, 6:26-30. “[C]onductive patterns 14 are formed from the conductive layer 4 ... for example, using one of the selective etching methods that are widely used and well known in the circuit-board industry.” *Id.*, 10:32-39, FIGS. 6A-6C. “[T]he connection zones or contact protrusions 7 on the surface of the components 6 are connected to the metal film 4...for example, using the ultrasonic or thermo-compression methods.” *Id.*, 6:38-42. The ’207 patent describes that “[i]n some embodiments, contact bumps 5, to which the connection zones or contact protrusions 7 of the components 6 are connected, are made on top of the conductive film 4.” *Id.*, 7:1-3.

## **VII. PROSECUTION HISTORY OF THE ’207 PATENT**

48. I have reviewed the file history of U.S. Application No. 17/005,527 (“the ’527 application), from which the ’207 patent issued.

49. I understand that the ’207 patent was filed with a single claim that recited first and second conductive-pattern layers with “a flexible insulating-material layer” between the layers, a component with flat contact zones electrically connected to the first conductive-pattern layer by at least one solid contact bump, and “a filler around the component, the filler securing the component mechanically to a flexible sheet.” APPLE-1002, 10.

50. In the only Office Action that was issued during prosecution of the application, the Examiner rejected the originally filed claim as obvious based on

Murayama (APPLE-1023) in view of Shangguan (APPLE-1024). APPLE-1002, 121-127. The Applicant responded by amending claim 1 as shown below and adding dependent claims 2-6. *Id.*, 171-172.

1. (Currently Amended) An electronic module, comprising:

~~[[ - ]]~~ a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface~~[[,]];~~

~~—a second conductive pattern layer having a second surface,~~

~~—a flexible~~ an insulating-material layer ~~between the first surface of the first conductive-pattern layer and the second~~ disposed on the first surface of the second conductive-pattern layer~~[[,]];~~

at least one installation cavity disposed in the insulating-material layer;

~~[[ - ]]~~ a component disposed within the at least one installation cavity, the component comprising ~~having flat contact zones comprising aluminum;~~ between the first surface of the first conductive pattern layer and the second surface of the second conductive pattern layer, at least some of the flat contact zones being electrically connected to the first conductive pattern layer by means of solderless and metallurgical connections, said connections each comprising at least one solid

first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and ~~between the first conductive pattern layer and the respective contact zone, and~~

second contact bumps disposed on the contact zones and electrically connected thereto,

wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials ~~—a filler around the component, the filler securing the component mechanically to a flexible sheet.~~

**APPLE-1002, 171-172**

51. Notably, the amendment to claim 1 removed requirements for the “insulating-material layer” to be “flexible” and located “between” respective surfaces of the first and second conductive-pattern layers. The amendment instead provided that the second conductive-pattern layer is “disposed on” the first conductive pattern layer and added that at least one of the first and second conductive-pattern layers includes “at least two layers of at least two different materials.” *Id.* The Applicant represented in its response that support for the amendments was drawn from paragraphs [0036], [0039], and [0060] of the published application (APPLE-1026)—corresponding to cols. 6:7-35, 6:52-59, and 10:14-21 of the later-issued ’207 patent specification. APPLE-1002, 173. Paragraph [0036] discloses conductive layers disposed on one another as a result of surfacing a first layer (e.g., a copper film) with additional metal(s) (e.g., tin and gold), while paragraph [0039] discloses that various items such as a “metal layer...can naturally also include several metals as layers, accumulations, zones, or metal alloys.” APPLE-1026, [0036], [0039].

52. Shortly after the Applicant filed its response, the Examiner allowed the application and identified a combination of limitations in amended claim 1 in her reasons for allowance. APPLE-1002, 180-184. However, as I will discuss below, all features recited in the Challenged Claims are disclosed in one or more of

Nishiuma, Shibata, Nakatani, Onda, and Parker, and the claimed combinations of these features would have been obvious before the Critical Date.

## VIII. CLAIM CONSTRUCTION

53. I do not believe that any term requires explicit construction. I understand that claim terms in an *inter partes* review proceeding are given their plain and ordinary meaning in light of the specification and file history. For purposes of my analysis in this declaration, I have applied claim interpretations consistent with the patent owner's allegations of infringement against Apple in the parallel district court proceeding. *See* APPLE-1105.

54. For the claim phrase addressed below, I provide my interpretation of the claim term and different ways that it would have been understood by a POSITA. In providing the following interpretation, I have carefully considered and applied the claim construction standard referred to in §III above.

55. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions that are raised in the parallel district court proceeding.

**A. “at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials”**

56. Element [1h] should be interpreted such that ***only one*** of the two conductive-pattern layers must include “at least two layers of at least two different

materials.” A POSITA would have understood the claim phrase as having *no* requirement for *both* the first and second conductive-pattern layers to include at least two layers of at least two different materials. A POSITA, interpreting the phrase “at least one of” would understand that the claim requires only one of the two options but does not require both.

57. This follows because the plain and ordinary meaning of the phrase “at least one of” is “one or more of” and it modifies the listed first conductive-pattern layer and second conductive-pattern layer, thus providing that the criteria for at least two layers of at least two different materials applies only to one or more of—but not necessarily both—the first and second conductive-pattern layers.

58. I understand that in some cases similarly formulated claim language has been interpreted to require at least one of ***each*** item recited in the list when the listed items were categorical (i.e., the listed items were presented as categories containing a variety of examples given in the specification) and the specific context of the specification and claim language in those cases made clear that at least one value from each listed category could be selected to fulfill the claimed criteria. That is not the case here. Instead, here, the recited first and second conductive-pattern layers are discrete items as opposed to categories from which at least one value could be selected from each.

59. Indeed, it would be non-sensical to refer to at least one first conductive-pattern layer and at least one second conductive-pattern layer because there is only one of each conductive-pattern layer recited in the claim. Any requirement to interpret the phrase “at least one of” in this claim as requiring **both** the first and second conductive-pattern layers to include at least two layers of at least two different materials would also violate basic canons of construction by effectively rendering the phrase “at least one” of superfluous.

60. The specification of the '207 patent also never demands two conductive pattern layers that each have at least two layers of different materials, and such features are certainly not essential. During prosecution, the Applicant cited disclosure from the '207 patent specification that allegedly provided support for amendments including the language in element [1h], but this disclosure never mentions any embodiment aligned with the narrow/conjunctive interpretation of element [1h]. See APPLE-1002, 172 (citing APPLE-1026, [0039] (“metal layer...**can** naturally also include several metals as layers, accumulations, zones, or metal alloys”)); *supra*, § III.B.

61. Accordingly, element [1h] only requires that one of the first or second conductive-pattern layers comprises at least two layers of at least two different materials. For example, consistent with the Patent Owner’s own allegations of infringement, element [1h] would be anticipated or rendered obvious by prior art

disclosure of two sub-layers of different materials in either first or second conductive-pattern layers. APPLE-1105, 9-10. Nonetheless, Grounds 1A, 1B and 2A confirm that the Challenged Claims would still have been obvious even if the narrower/conjunctive interpretation applied to require at least two layers of at least two different materials in both the first and second conductive-pattern layers.

## **IX. OVERVIEW OF CONCLUSIONS FORMED**

62. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-6 of the '207 patent are rendered obvious by Nishiuma (APPLE-1004) in view of Shibata (APPLE-1005).
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-6 of the '207 patent are rendered obvious by Nishiuma in view of Shibata and Glick (APPLE-1020).
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 3-4 of the '207 patent are rendered obvious by Nishiuma in view of Shibata and Parker (APPLE-1010).

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-2 and 5-6 of the '207 patent are rendered obvious by Nakatani (APPLE-1007) in view of Onda (APPLE-1008) and Glick.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 3-4 of the '207 patent are rendered obvious by Nakatani in view of Onda, Glick and Parker.

63. Nishiuma, Shibata, Glick, Parker, Nakatani and Onda are all analogous art to the '207 patent in that they are all in the same field of endeavor and/or reasonably pertinent to the problems said to be addressed by the '207 patent. For example, each of the prior art references applied in Grounds 1A-2B below describe techniques for manufacturing and packaging electronic modules. APPLE-1001, 1:24-37 (describing the field of the invention: "The present invention relates to an electronic module... which includes one or more components embedded in an installation base"); APPLE-1004, 1:11-17 ("The present invention relates to a semiconductor integrated circuit device fabrication technique and a semiconductor integrated circuit device obtained by the technique, and particularly to a technique for connecting a semiconductor chip to a printed wiring board by face down bonding of a semiconductor chip to a wiring substrate

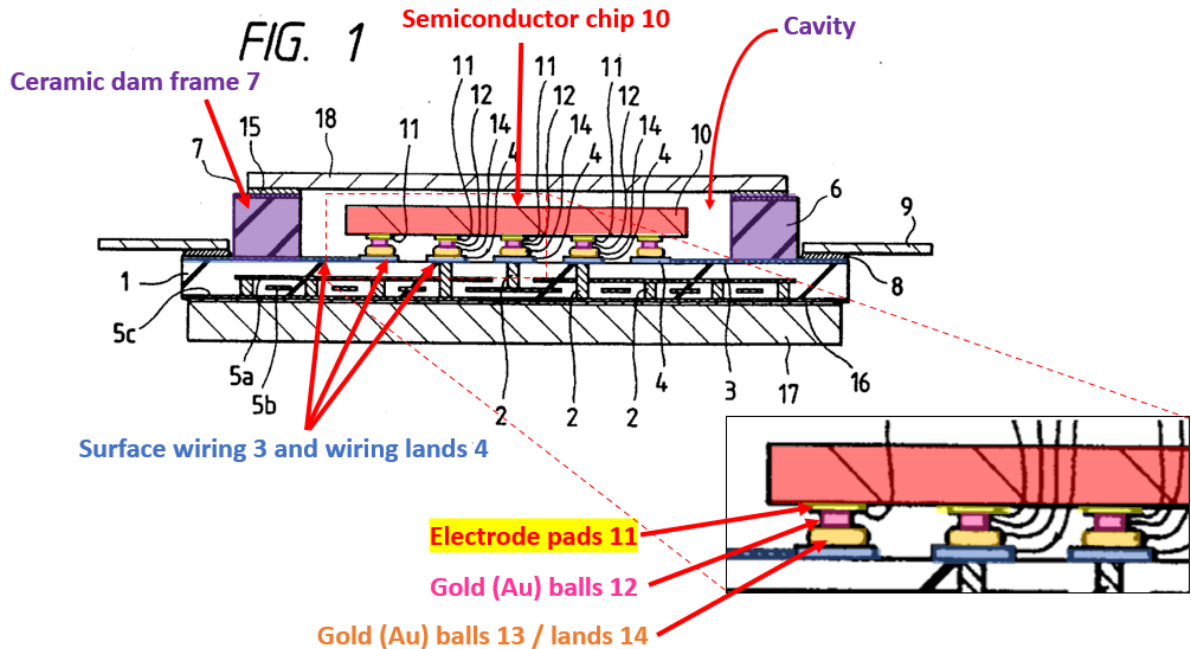
using metallic bumps”); APPLE-1005, [0001] (“The invention relates to a so-called chip-on-chip ... type semiconductor device, in which a plurality of semiconductor chips is electrically interconnected as opposed to each other, and a method for manufacturing the same.”); APPLE-1020, 1:6-10 (“The invention relates to methods for strengthening bonds, and more particularly, to methods for strengthening bonds between thin-film conductors and insulating substrates on which they are formed”); APPLE-1010, 1:5-8 (“This invention relates to printed circuit boards and more particularly relates to methods of making printed circuit boards having grooves for receiving electrical leads and cavities for receiving electrical components”); APPLE-1007, [0001] (“The present invention relates to a module containing electric elements such as semiconductor chips or surface acoustic wave devices... [in particular] an electric element built-in module [and] a method for manufacturing such an electric element built-in module”); APPLE-1008, Title (“Wiring substrate, semiconductor device, electronic devices using these, and manufacturing methods for these”).

**X. GROUND 1A: CLAIMS 1-6 ARE OBVIOUS UNDER 35 U.S.C. § 103  
BASED ON NISHIUMA IN VIEW OF SHIBATA**

**A. Nishiuma Overview (APPLE-1004)**

64. Nishiuma describes a “semiconductor integrated circuit device” formed as “a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.” APPLE-1004, Abstract, 6:66-7:2.

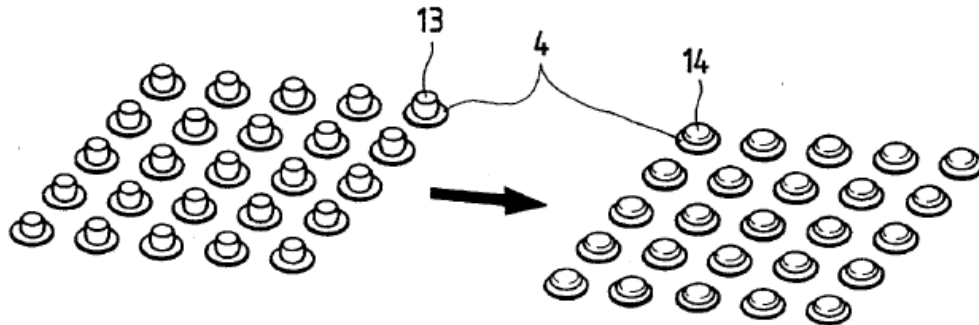
As depicted in FIG. 1, Nishiuma's device includes surface wiring 3 and wiring lands 4 made of "thick films of refractory metal." APPLE-1004, 7:67-8:3.



**APPLE-1004, FIG. 1 (annotated and modified to include excerpt)**

65. Gold (Au) balls 13 are bonded to wiring lands 4 "using heat or ultrasonic energy or both" and flattened to form Au lands 14. *Id.*, 8:18-19, 8:28-29, 9:4-6, FIG. 5(b).

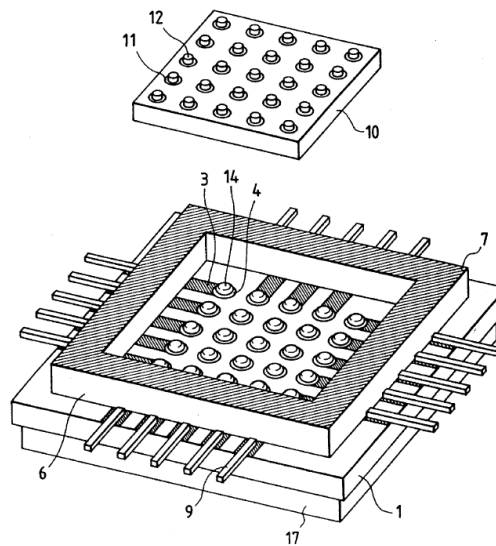
*FIG. 5(b)*



**APPLE-1004, FIG. 5(b)**

66. As shown above in FIG. 1, Nishiuma's "semiconductor chip 10" includes "electrode pads 11" that are "made of [gold] similarly to the integrated circuit wirings." APPLE-1004, 8:10-16. Au balls 12 are "bonded to the electrode pads 11 of the semiconductor chip 10" using "heat or ultrasonic energy or both" and are then bonded to Au lands 14 by "thermocompression bonding" to achieve an electrical connection between the semiconductor chip and the surface wiring. *Id.*, 8:17-19, 9:13-16, 7:43-47. Nishiuma's ceramic "square dam frame 6" "forms a cavity in which the semiconductor chip 10 is mounted." *Id.*, 7:48-54. Nishiuma's "cap 18" is bonded to "the frame 6 through a sealing metallize 7 and brazing filler metal 15." *Id.*, 7:51-55.

FIG. 4



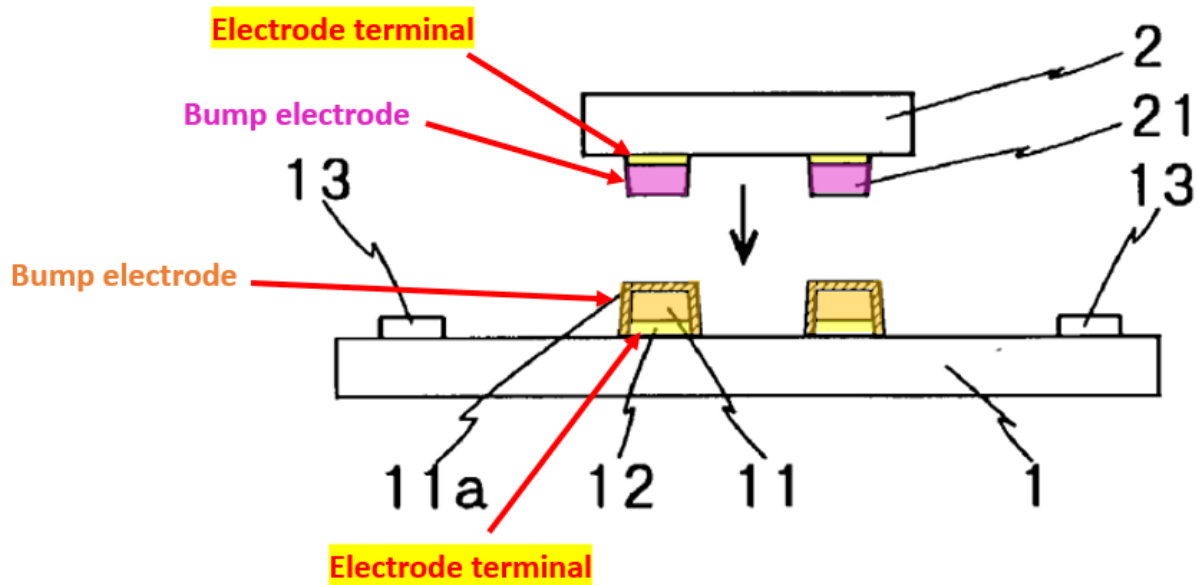
APPLE-1004, FIG. 4

**B. Shibata Overview (APPLE-1005)**

67. Shibata describes a method for coupling semiconductor chips using a bump electrode formed on an electrode terminal of the semiconductor chip.

APPLE-1005, [0011]. Shibata's bump electrodes use metals with a relatively low melting point to alloy one metal with another inside the bump to prevent adverse effects from high temperature on the semiconductor elements. *Id.*

FIG. 1B



APPLE-1005, FIG. 1B (annotated)

68. Shibata's bump electrodes 11 and 21 are formed "on the electrode terminals 12 and 22 made of aluminum." *Id.*, [0052], FIG. 1C.

69. Shibata describes that the first and second bump electrodes 11 and 21 can be joined by "a third metal layer having a lower melting point" which "melts at a relatively low temperature and diffuses into the bump electrode or the electrode terminal to thereby provide diffusive joining." *Id.*, [0014], [0032] ("it is preferable that the metals are made of Au and the low-melting point metal layer is made of Sn or an Au—Sn alloy"), [0082]. For example, in FIG. 1B, above, "[a]n Sn coating 11a is provided on the bump electrode 11 made of Au." *Id.*, [0053].

**C. The Nishiuma-Shibata Combination**

70. Nishiuma discloses that the semiconductor chip 10 includes electrode pads 11 that provide contact zones for electrically connecting the semiconductor chip 10 to the printed wiring board via bonds between Au lands 14 on the wiring board 1 and Au balls 12 on the electrode pads 11. *Supra*, § IV.A; APPLE-1004, 7:43-46. In one embodiment, “electrode pads 11 are made of Au similarly to the integrated circuit wirings.” APPLE-1004, 8:13-16. Nishiuma does not limit the materials of the electrode pads 11, however, and contemplates that metals besides Au would also be suitable for the integrated circuit wirings including for the Au balls 12. *Id.*, 17:15-18, 17:32-42, claims 1 and 15 (not limiting electrode pad material). In this context, a POSITA would have appreciated and found obvious that other metals such as aluminum also would have been obvious to implement Nishiuma’s electrode pads 11, as was conventional by the Critical Date.

71. Recognizing that semiconductor chips commonly included electrode pads formed from materials other than gold, a POSITA would have turned to references such as Shibata to investigate the use of alternate materials for the electrode pads. A POSITA would have appreciated that it was common before the Critical Date to form electrode pads from aluminum. For example, Usuda describes that “[h]eretofore [prior to 1987 filing], in a semiconductor device, copper or copper alloy is used as a bonding wire , and aluminum or aluminum

alloy is used as an electrode pad, which is also known as bonding electrode.”

APPLE-1034, 1:15-18. A POSITA would have been aware of the conventional use of aluminum in electrode pads from references like Usuda and from experience in working with semiconductor devices and chips.

72. Like Nishiuma, Shibata describes techniques for connecting an electronic component having electrode pads to another structure using gold contact bumps—although Shibata’s electrode pads are aluminum. APPLE-1005, [0059], [0051]-[0052]; *supra*, § IV.A.2. Multiple reasons would have motivated a POSITA to implement Nishiuma’s electrode pads using aluminum in accordance with Shibata’s suggestion as described below. APPLE-1004, 8:10-9:16, FIG. 1; APPLE-1005, [0052].

73. First, a POSITA would have been motivated to substitute aluminum, as Shibata suggests, for gold in the electrode pads because aluminum is less costly than gold. For example, in a 2000 Materials Science textbook, aluminum alloys is listed with an associated cost between \$4.40-\$11.65/kg compared to pure gold which is listed as costing between \$9,500-\$10,250 per kg. APPLE-1035, 138-139; *see also* APPLE-1020, 3:67-3:2 (describing a desire to reduce the amount of gold required in bonding semiconductor devices to substrates).

74. Second, a POSITA would have understood that aluminum is easier to work with for producing or coating electrode pads than gold would be and would

have been motivated to substitute aluminum for gold in the electrode pads for ease of manufacturing. A POSITA would have appreciated that aluminum is softer, lighter, and more readily available compared to gold, and that gold often requires alloying with other materials to improve strength which adds complexity to the manufacturing process. See APPLE-1035, 110 (comparing densities of aluminum alloys and gold), 118-119 (comparing yield strength and tensile strength of aluminum alloys and gold). Aluminum is easier to process than many other metals, including gold, and a POSITA would have understood that substituting aluminum for gold in electrode pads would simplify the manufacturing process.

75. Third, a POSITA would have understood that aluminum has superior properties to gold, including better resistivity and a lower coefficient of thermal expansion. A POSITA would have understood that gold and aluminum have similar electrical conductivity (gold having  $4.3 \times 10^7 (\Omega \cdot \text{m})^{-1}$  and Aluminum having  $3.8 \times 10^7 (\Omega \cdot \text{m})^{-1}$  at room temperature). APPLE-1035, 133 (reporting electrical resistivities for aluminum alloys between  $2.9 \times 10^{-8}$  and  $5.22 \times 10^{-8} \Omega \cdot \text{m}$  and electrical resistivity of gold having electrical resistivity between  $4.2 \times 10^{-7}$  –  $5.2 \times 10^{-7} \Omega \cdot \text{m}$ ). Resistivity is the inverse of conductivity, and thus a low resistivity indicates a material that readily allows an electrical current. *Id.*, 133, 12.

76. Additionally, a POSITA would have understood that aluminum has a lower resistivity and lower coefficient of thermal expansion than gold

(commercially pure gold having a coefficient of thermal expansion of  $14.2 \times 10^{-6}$   $(^{\circ}\text{C})^{-1}$  and 99.9% pure aluminum having a coefficient of thermal expansion of  $7.4 \times 10^{-6}$   $(^{\circ}\text{C})^{-1}$ ). APPLE-1035, 124-125. A POSITA would have appreciated that these properties of aluminum are advantageous for use in electrode pads.

77. Fourth, a POSITA would have understood that implementing electrode pads with aluminum in place of gold amounts to simple substitution of one known element for another to obtain predictable results. Indeed, implementing the electrode pads with aluminum in place of gold would have been an obvious design choice to a POSITA to optimize the cost and performance of the electrode pad design. A POSITA, in designing a semiconductor integrated circuit device, as Nishiuma describes would have appreciated that design decisions including materials balance various considerations including cost, electrical conductivity or resistivity, ease of manufacture, and other performance-impacting characteristics of the material. As described above, a POSITA would have appreciated that aluminum electrode pads were commonplace, that aluminum is a suitable material to select for an electrode pad, and that substituting the material of an electrode pad to be aluminum instead of gold would have been straightforward. *See* APPLE-1034, 1:15-18 (describing that aluminum electrode pads were conventional as of 1987). The result of substituting aluminum for gold in an electrode pad would have been predictable—a working electrode pad consistent with conventional

electrode pads at the time. A POSITA would have appreciated this, and it would have been well within the level of skill of the POSITA to make such a substitution.

78. Fifth, coupling a device having aluminum electrode pads to a conductive layer using gold balls in the combination would have been obvious as a predictable application of a known technique for providing electrode pads of a semiconductor device as taught by Shibata to a known system as taught by Nishiuma to achieve entirely predictable results. A POSITA would have been familiar with the use of aluminum in electrode pads of a component, as Shibata teaches, and it would have been simple to implement in Nishiuma's device simply by using aluminum to make the electrode pads of the component (or specifying the electrode pad material of the component during manufacture or purchase). A POSITA would have understood that the use of aluminum for electrode pads was well-known and it would have been straightforward to apply this teaching of Shibata to Nishiuma's device.

79. A POSITA would have had a reasonable expectation of success in implementing electrode pads with aluminum, as Shibata suggests, rather than gold, for a variety of reasons, including that aluminum electrode pads were conventionally used on components at the time of the invention. APPLE-1034, 1:15-18. The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all

the reasons described above and because of the similarities between the teachings of Nishiuma and Shibata. APPLE-1004, 2:60-67, 8:16-9:21; Figs. 1, 39; APPLE-1005, [0051]-[0052], FIG. 1B.

80. For example, Shibata teaches a method for coupling a component to a conductive layer using gold balls, and a POSITA would have understood that such a method is equally applicable to components that have conventional aluminum electrodes pads (as Shibata teaches) as it is to components with gold electrode pads (per Nishiuma). See APPLE-1004, 8:17-19 (“Au balls 12 are bonded to the electrode pads 11 of the semiconductor chip 10”), 8:28-30 (“Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1”); 9:4-6 (“Au lands 14 having a larger diameter are formed by pressing and flattening the Au balls 13”); 9:13-16 (“Au balls 12 of the semiconductor chip 10 are aligned with the corresponding Au lands 14 on the printed wiring board 1 to bond the Au ball 12 with the Au land 14 by thermo-compression bonding”), 8:13-16; APPLE-1005, [0051] (“a semiconductor chip 1 on the surface of which bump electrodes 11 are formed, bump electrodes 21 of a second semiconductor chip 2 are joined” and “[t]he respective bumps electrodes 11 and 21 of these first and second semiconductor chips 1 and 2 are both made of first metal such as Au”), [0052].

81. A POSITA would have understood that Shibata applies a method for connecting a semiconductor chip to a conductive layer that is largely the same as

the method Nishiuma describes—and that Shibata demonstrates that Nishiuma’s teachings can be implemented with conventional components that have aluminum electrodes. See APPLE-1005, FIG. 1B; APPLE-1004, FIG. 1. A POSITA would have had a reasonable expectation of success in making the combination in view of the similarities between the teachings of the references. Because the methods and techniques described by the two references are so similar but for the material of the electrode pads, a POSITA would have understood that the same techniques can be applied with electrode pads of either gold or aluminum materials and would have been motivated to implement the techniques with aluminum pads for all of the reasons explained above.

**D. Claim-by-Claim Analysis**

**i. Claim 1**

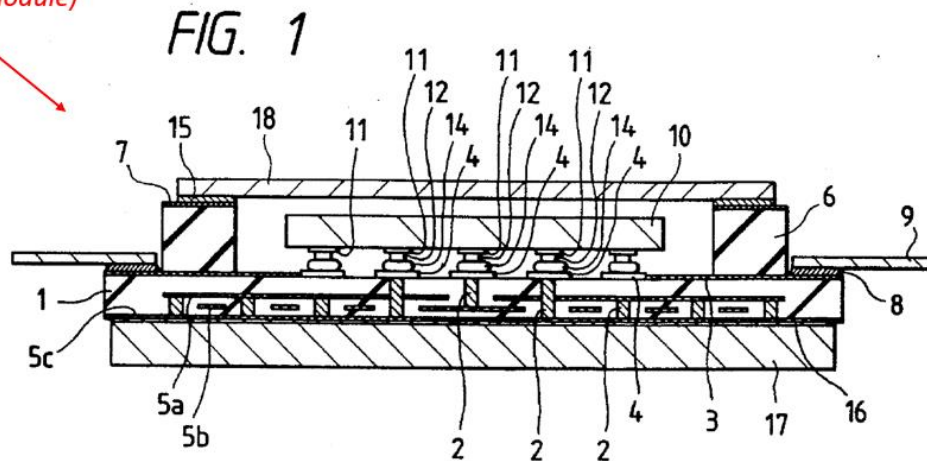
***[1.pre] An electronic module, comprising:***

82. To the extent the preamble is limiting, Nishiuma-Shibata renders [1.pre] obvious. Nishiuma describes a semiconductor integrated circuit device that constitutes an “***electronic module***” as claimed. APPLE-1004, 1:11-17 (“The present invention relates to a semiconductor integrated circuit device fabrication technique and a semiconductor integrated circuit device obtained by the technique, and particularly to a technique for connecting a semiconductor chip to a printed wiring board by face down bonding of a semiconductor chip to a wiring substrate

using metallic bumps”); *cf.* APPLE-1001, 1:24-31 (’207 patent describing that an electronic module “can be a module like a circuit board, which includes several components [such as] semiconductor components”).

83. For example, Nishiuma’s Figure 1 depicts that “the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18.”  
APPLE-1004, 6:66-7:2.

Semiconductor  
integrated circuit device  
(electronic module)



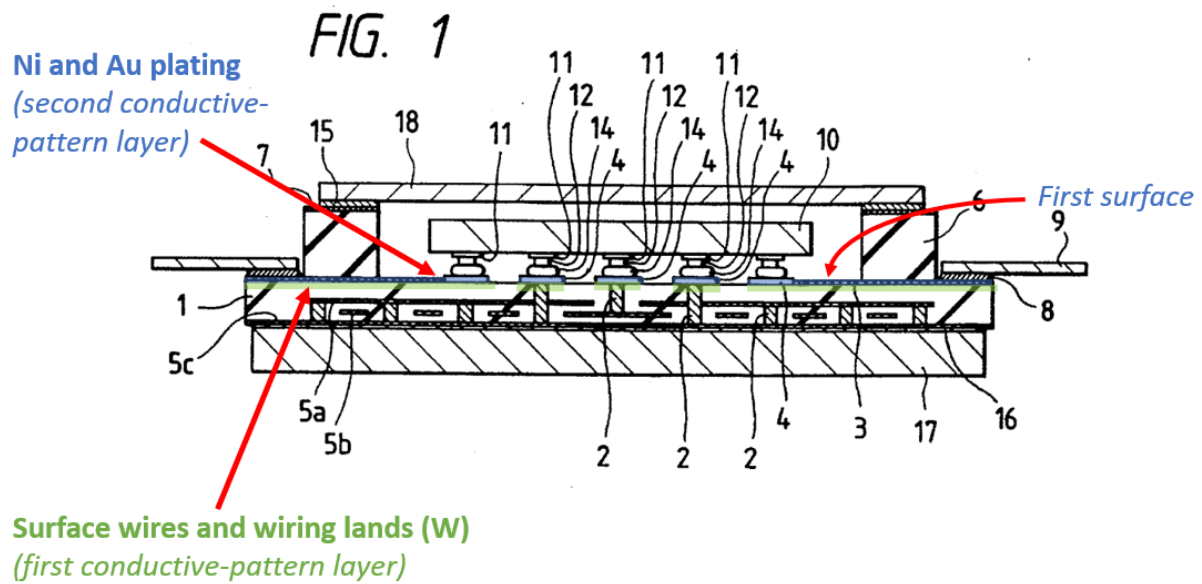
APPLE-1004, FIG. 1 (annotated)

***[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;***

84. Nishiuma's semiconductor device includes a "printed wiring board 1 [] made of ceramic such as alumina or aluminum nitride, on whose surface a plurality of surface wires 3 and a plurality of wiring 1 and electrodes 4 are formed." APPLE-1004, 7:7-10, 7:14-16, FIG. 1. The surface of the printed wiring board 1 including surface wires 3 can further include wiring lands 4. *Id.* Additionally, according to Nishiuma, "[t]he surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au ... ." APPLE-1004, 7:14-16. The underlying surface wires 3 and wiring lands 4 collectively provide the claimed "***first conductive-pattern layer***" while the Ni and Au plated on the surface wires 3 and lands 4 collectively provide the claimed "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. APPLE-1004, 7:14-16; *cf.* APPLE-1001, 6:28-31 ('207 patent describing "surfaced" conductive layers for wiring similar to Nishiuma's), 6:52-59 ('207 patent also describing layers comprised of multiple components); APPLE-1002, 170-173. For example, Nishiuma makes clear that the surface wires and lands are formed from the same materials, and by the same screen-printing technique. For example, Nishiuma describes that "[t]he surface wiring 3 and wiring land 4 of thick films of a refractory metal such as W

plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method.” APPLE-1004, 7:67-8:3; *see also* 7:7-16. From Nishiuma’s description of the common function, materials, and manufacturing process of the surface wiring and lands, a POSITA would have understood that the surface wiring and lands together provide a “**first conductive-pattern layer.**” Similarly, from Nishiuma’s description of the Ni and Au plating layers formed on the refractory metal of the surface wiring and lands, a POSITA would have understood that the plating layers, together, provide a “second conductive-pattern layer.” APPLE-1004, 7:67-8:3.

85. Nishiuma’s surface wires and wiring lands form a pattern on the printed wiring board for establishing connection to components. After forming the wires and the lands on the board, the wires and lands (**first conductive-pattern layer**) would have one surface in contact with the printed wiring board and an opposite surface pointed away from the board which is then plated in Ni and Au so that a surface of the Ni and Au plating (**second conductive-pattern layer**) is pointed away from the board (**a first surface**). *See* APPLE-1004, 7:13-15 (describing that “The surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au in the order from the bottom” implying that the wiring and lands have surfaces.).



**APPLE-1004, FIG. 1 (annotated<sup>1</sup>)**

86. Accordingly, the top of the plated layer of Ni and Au provides the claimed “**first surface**” of the second conductive-pattern layer. APPLE-1004, 7:67-8:3 (“The surface wiring 3 and wiring land 4 of thick films of refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method.”), 7:14-16 (describing an “order from the bottom” implying the existence of a top surface as a first surface).

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<sup>1</sup> FIG. 1 does not specifically depict the plated Ni and Au over the surface wires 3 and wiring lands 4. The size and boundaries of the colored areas are therefore exaggerated to emphasize the existence of two conductive-pattern layers as claimed consistent with the disclosure in Nishiuma.

87. Nishiuma describes that the surface wires 3 and wiring lands 4 together cooperate to form a conductive layer for the transmission of power and information signals. APPLE-1004, 7:16-18; (“The surface wirings 3 are wirings for input/output signals, GND, and power source, one end of each of wirings is connected to one of the wiring lands 4.”), 7:11-14 (“surface wiring 3[ and] lands 4 ... are made of thick films of a refractory metal”); *cf.*, APPLE-1001, 6:52-59 (describing layers that can include “several metals as layers, accumulations, zones, or metal alloys”). Additionally, Nishiuma makes clear that the surface wires and lands are formed from the same materials, and by the same screen-printing technique. For example, Nishiuma describes that “[t]he surface wiring 3 and wiring land 4 of thick films of a refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method.” APPLE-1004, 7:67-8:3; *see also* 7:7-16. The dispersed arrangement of electrodes and contact points provided by the surface wires and wiring lands provide additional forms patterning the conductive layer, as I will discuss further below. From Nishiuma’s description of the common function, materials, and manufacturing process of the surface wiring and lands, a POSITA would have understood that the surface wiring and lands together provide a “***first conductive-pattern layer***.” A POSITA would have similarly understood the Ni and Au plating on the wiring and lands to collectively provide the “second ... layer” as claimed.

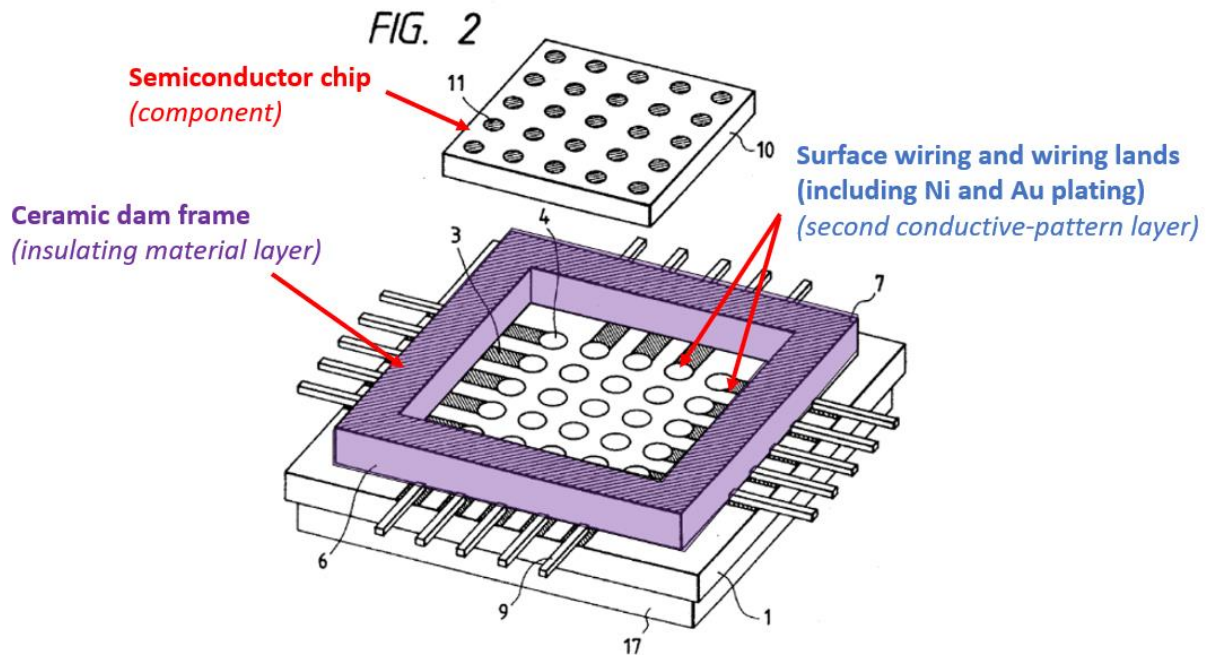
88. Additionally, the surface wires 3, wiring lands 4, and Ni and Au plating, being formed of conductive metals, are electrically conductive. APPLE-1004, 4:31-33 (“it is possible to provide the input/output signal paths of the printed circuit substrate only by forming surface wirings...”); *see also* APPLE-1022, 9 (“A printed circuit board is a piece of plastic material on which electronic components can be mounted for mechanical support, and which also electrically interconnects all the components it supports by means of a pattern of metal tracks on its outer surfaces and sometimes on inner layers.”). Nishiuma describes that the surface wiring and lands are formed from tungsten and plated with nickel and gold—all of these materials being known to be electrically conductive. APPLE-1004, 7:11-16; APPLE-1035, 133. For example, the electrical resistivity of tungsten is about  $5.3 \times 10^{-8} \Omega\text{-m}$ , for nickel it is about  $0.95 \times 10^{-7} \Omega\text{-m}$ , and for gold  $2.35 \times 10^{-8} \Omega\text{-m}$ . *Id.* Resistivity is the inverse of conductivity, and thus a low resistivity indicates a material that readily allows an electrical current. *Id.*, 133,12.

89. The arrangement of individual electrodes and discrete contact points provided by the metal surface wires 3 and wiring lands 4, and Ni and Au plating, form patterning in the conductive layer as claimed. Nishiuma describes that as part of the preparation of the printed wiring board “[t]he surface wiring 3 and wiring land 4 of thick films of a refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing

method.” APPLE-1004, 7:66-8:3. Screen printing the surface wiring and lands enables the creation of a pattern of wires on the printed wiring board to provide connection to devices, such as a semiconductor chip.

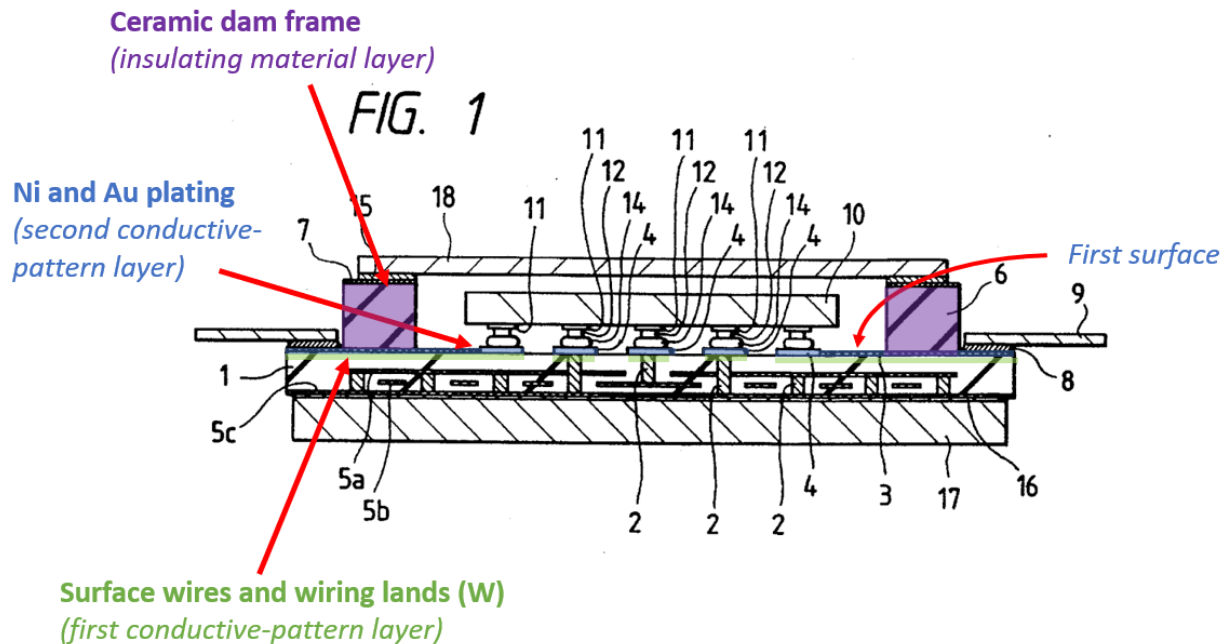
***[1c] an insulating-material layer disposed on the first surface of the second conductive-pattern layer;***

90. Nishiuma-Shibata renders obvious element [1c]. For example, Nishiuma describes that “[a] square dam frame 6 for sealing is formed around the semiconductor chip 10 on the wiring board 1.” APPLE-1004, 7:48-49, 7:53-54 (“The sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted”), 8:5-9. As shown below in FIG. 2, the ceramic dam frame 6 is positioned on the wiring board 1 so that the semiconductor chip 10 can be positioned within the cavity formed by the frame.



**APPLE-1004, FIG. 2**

91. Additionally, as shown below in FIG. 1, the dam frame 6 is disposed on the first surface of the second conductive-pattern layer introduced in the analysis of elements [1a]-[1b.ii] above, so that the component can then be positioned inside the cavity formed by the dam frame 6. *Id.*, 7:53-54, FIGS. 2, 6. Because Nishiuma's dam frame 6 is formed on a top surface of the surface wirings 3 including the Ni and Au plating, the ceramic dam frame is disposed on the first surface of the second-conductive pattern layer.



**APPLE-1004, FIG. 1 (annotated)**

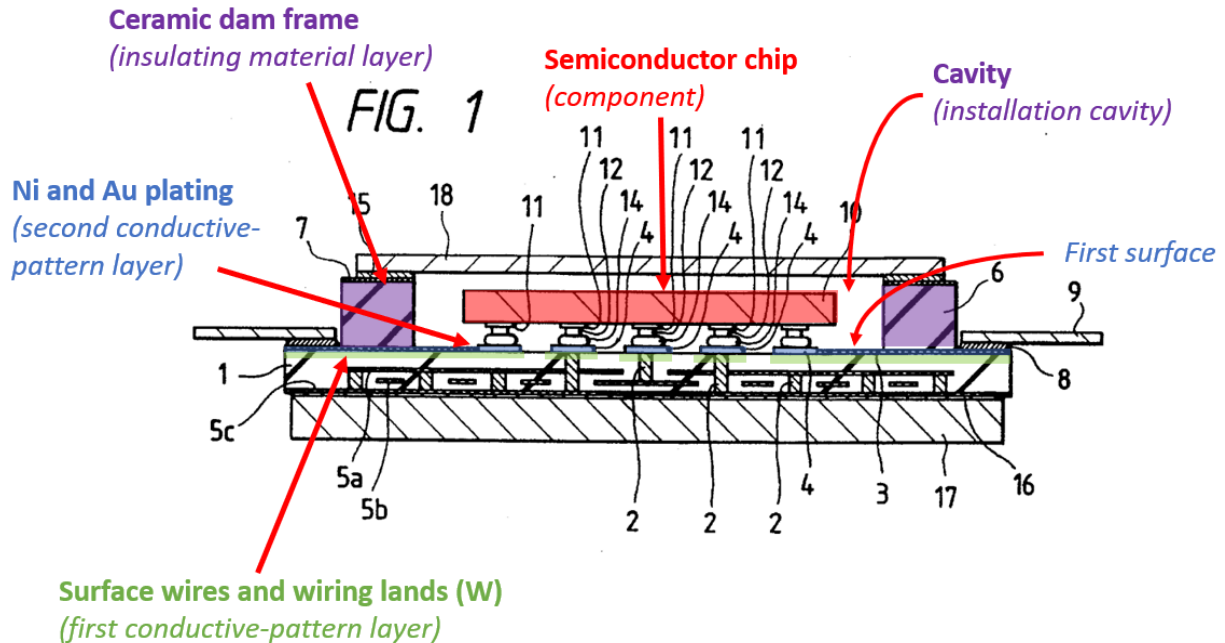
92. Nishiuma further describes that “[t]he dam frame 6 is made of ceramic such as alumina or aluminum nitride,” which are electrical insulators. APPLE-1004, 7:49-51. A POSITA would have recognized that Nishiuma’s ceramic dam frame 6 is an insulator because alumina and aluminum nitride are well-known electronic insulators. *Id.*; APPLE-1035, 43 (“Most polymers and ionic ceramics are insulating materials at room temperature”), 134 (showing high electrical resistivity in a variety of insulators including aluminum oxides (“alumina”)); APPLE-1010, 1:9-17 (describing ceramic as “a suitable electrically insulating material”); APPLE-1011, [0006] (describing chip carrier packages formed from ceramic and alumina insulators). A POSITA would have further

found it obvious to implement Nishiuma's ceramic dam frame as an insulator to prevent electrical signals from wiring 3 from conducting to other components contacted by dam frame 6 or causing undesirable electrical short circuiting.

93. Accordingly, Nishiuma's dam frame provides an “***insulating-material layer***” as claimed.

***[1d]-[1e.i] at least one installation cavity disposed in the insulating-material layer; a component disposed within the at least one installation cavity,***

94. Nishiuma-Shibata renders obvious elements [1d]-[1e.i]. For example, Nishiuma describes that “[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted.” APPLE-1004, 7:53-54, FIGS. 2, 6. As shown in FIG. 1, Nishiuma's device thus provides an “***installation cavity***” disposed within the dam frame (***insulating-material layer***) and includes a semiconductor chip (***component***) disposed within the cavity.



APPLE-1004, FIG. 1 (annotated )

95. As shown above, Nishiuma-Shibata render obvious an installation cavity disposed in the insulating-material layer and a component disposed within the at least one installation cavity.

**[1e.ii] the component comprising contact zones comprising aluminum;**

96. Nishiuma-Shibata renders obvious element [1e.ii]. For example, Nishiuma describes a semiconductor chip (**component**) that includes electrode pads (**contact zones**) for forming electrical connections to external wiring.

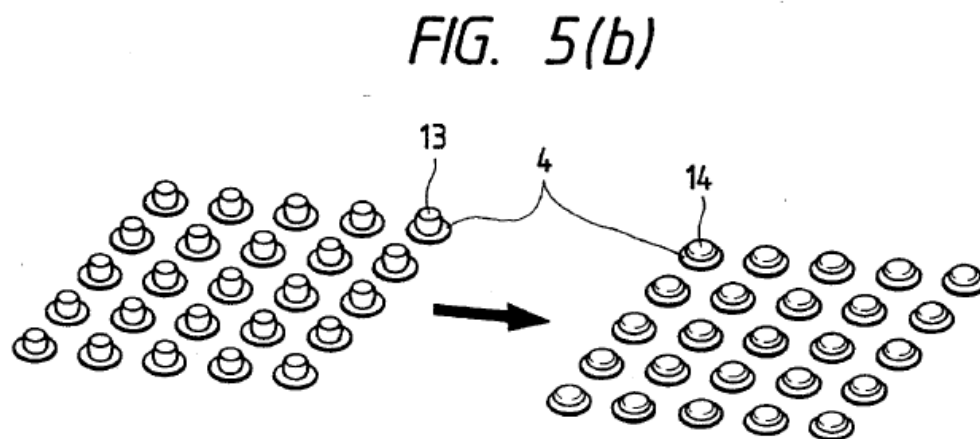
APPLE-1004, Abstract (“electrode pads of a semiconductor chip”), 7:2-6, 7:43-46, 8:13-16, FIGS. 1, 3-4. To the extent Nishiuma does not expressly disclose that the electrode pads can include aluminum, Shibata teaches this conventional option.

APPLE-1005, [0052] (“electrode terminals 12 and 22 made of aluminum”), [0011] (“semiconductor chip having an electrode terminal”), FIGS. 1A-1C.

97. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nishiuma’s electrode pads using aluminum as suggested by Shibata. *Supra* §X.C (Nishiuma-Shibata Combination).

***[1f] first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and***

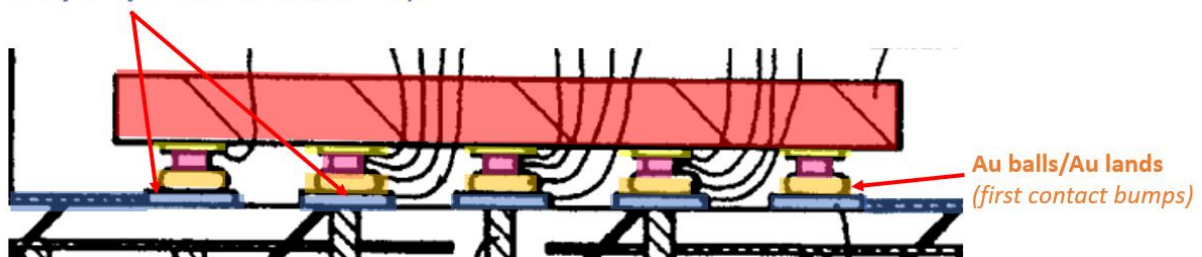
98. Nishiuma-Shibata renders obvious element [1f]. For example, Nishiuma describes that “Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1 ... .” APPLE-1004, 8:28-29. As shown below in FIG. 5B, after bonding the Au balls 13 to the wiring lands 4, “Au lands 14 are formed by pressing and flattening the Au balls 13 ... .” *Id.*, 8:46-48, FIG.5B.



**APPLE-1004, FIG. 5B**

99. The Au balls 13 before pressing/flattening and/or Au lands 14 after pressing/flattening provide “**first contact bumps**” disposed on the first surface of the second conductive-pattern layer as claimed. As described above, the first surface of the second conductive-pattern layer is formed by the top surface of the Ni and Au gold plating, and accordingly, the Au balls 13 and/or Au lands 14 formed on the plated surface wiring 3 and lands 4 are **first contact bumps disposed on the first surface of the second conductive-pattern layer**.

*First surface of the second conductive layer*



**APPLE-1004, FIG. 1 (excerpted, annotated)**

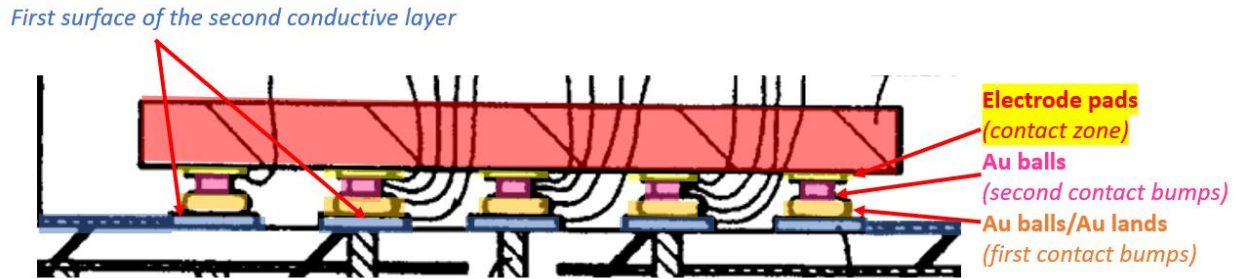
100. In particular, Nishiuma further teaches that the Au balls 13 and Au lands 14 are electrically connected to the first surface of the second conductive-pattern layer (i.e., to the top surface of the plated Ni and Au).

101. For example, Nishiuma explains “[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-

compression bonding.” APPLE-1004, 7:43-47; *see also id.*, 10:34-44. Nishiuma’s bonding of the gold balls to the wiring lands (formed of tungsten and plated with nickel and gold) clearly couples two items formed from conductive materials to electrically connect the gold balls (***first contact bumps***) to the top of the Ni and Au plating (***first surface of the second conductive-pattern layer***). A POSITA also would have understood and found obvious that an electrical connection would be formed by bonding the Au lands 14 to the plated surface of wiring lands 4 since both are electrically conductive. APPLE-1035, 133-134 (describing electrical resistivities of materials including tungsten, nickel and gold – a POSITA would have recognized that electrical conductivity is the reciprocal of electrical resistivity, and thus low electrical resistivities are associated with electrically conductive materials).

***[1g] second contact bumps disposed on the contact zones and electrically connected thereto,***

102. Nishiuma-Shibata renders obvious element [1g]. For example, Nishiuma describes “Au balls 12 having a diameter smaller than that of the Au lands 14 [that] are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10.” APPLE-1004, 7:41-43, 8:17-19. Au balls 12 provide “***second contact bumps***” disposed on the electrode pads 11 (***contact zones***) of the semiconductor chip (***component***) as claimed.



**APPLE-1004, FIG. 1 (excerpted, annotated)**

103. Nishiuma further teaches that “[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding.” APPLE-1004, 7:41-47; *see also id.*, 8:17-27, 10:44-51, 10:57-11:8. Au balls 12 are therefore electrically connected to the electrode pads. *Id.* A POSITA also would have understood and found obvious that an electrical connection would be formed by bonding the Au balls 12 to the electrode pads 11 since both are electrically conductive themselves. *See* APPLE-1035, 133-134 (describing electrical resistivities of materials including aluminum and gold – a POSITA would have recognized that electrical conductivity is the reciprocal of electrical resistivity, and thus low electrical resistivities are associated with electrically conductive materials).

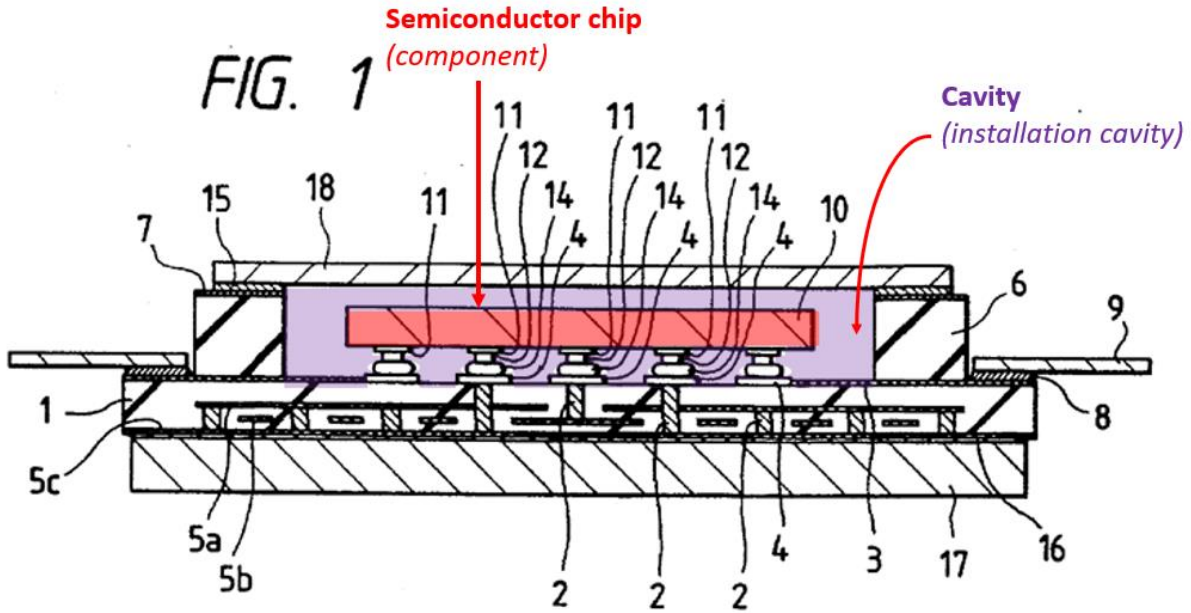
***[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.***

104. Nishiuma-Shibata renders obvious element [1h]. As described above, Nishiuma's underlying surface wires 3 and wiring lands 4 collectively provide the claimed "***first conductive-pattern layer***" while the Ni and Au layers plated on the surface wires 3 and lands 4 collectively provide the claimed "***second conductive-pattern layer***." *Supra*, §X.D.[1a]-[1b.ii]. The second conductive-pattern layer in this example includes layers of "Ni and Au in the order from the bottom" and thus comprises two layers of at least two different materials: (1) a first layer of nickel and (2) a second layer of gold. APPLE-1004, 7:14-16. Accordingly, at least one of the first and second conductive pattern layers (i.e., the second conductive pattern layer) includes two layers of different materials. *Supra* §VIII.A.

**ii. Claim 2**

***[2] The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.***

105. Nishiuma-Shibata renders obvious claim [2]. For example, Nishiuma's FIG. 1 shows that the installation cavity can be thicker than the component. APPLE-1004, FIG. 1; *see also id.*, 7:54-55, claim 2.



**APPLE-1004, FIG. 1 (annotated)**

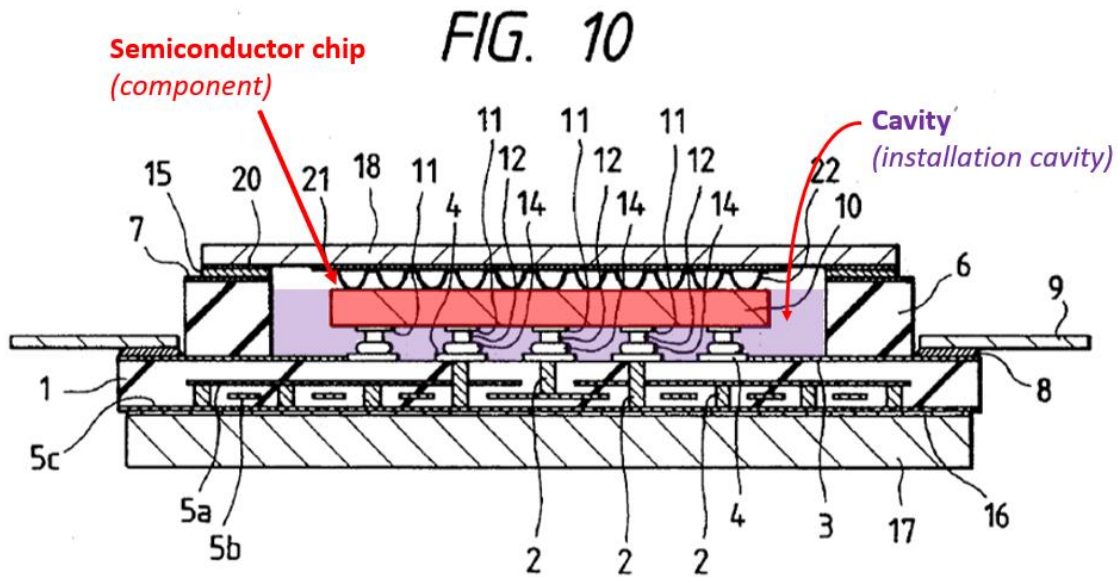
106. In the context of the '207 patent, component thickness refers to or encompasses the height of the component *after installation in the cavity*. Indeed, the patent specifically relates the thickness of the component to the component's protrusion beyond the height or thickness of the installation cavity. *See, e.g.,* APPLE-1001, 7:61-8:5. This understanding comports with the specification's discussion of component thicknesses that are less than, equal to, or greater than the thickness of the installation base or cavity, especially as there would be no reason to distinguish between components of equal or greater absolute/pre-installation thickness when both would protrude from the cavity after installation due to the contact bump / electrode thickness. APPLE-1001, 6:8-17.

107. In this context, Nishiuma's FIG. 1 makes clear that the walls that form the cavity have a larger height than the component, such that the installation cavity is thicker than the component as claimed. Further, a POSITA would have understood that by forming an installation cavity with greater thickness than the component to be installed, the component would not protrude beyond the height of the insulating-layer and could be sealed within the cavity by the positioning of a cap, just as Nishiuma teaches. APPLE-1004, 6:66-7:2, 7:48-60, 9:31-38, 16:38-40.

**iii. Claim 3**

***[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.***

108. Nishiuma-Shibata renders obvious claim [3]. For example, Nishiuma's FIG. 10 embodiment shows that the thickness of the installation cavity can be reduced to match the thickness of the semiconductor chip (***component***) by providing a "a heat conductive media of Au ribbons 22 ... in the space between the back of [the] semiconductor chip 10 ... and the bottom of a cap 18 to cool the semiconductor chip 10 by conducting heat through the cap." APPLE-1004, 11:19-25; *see also id.*, 11:26-41.

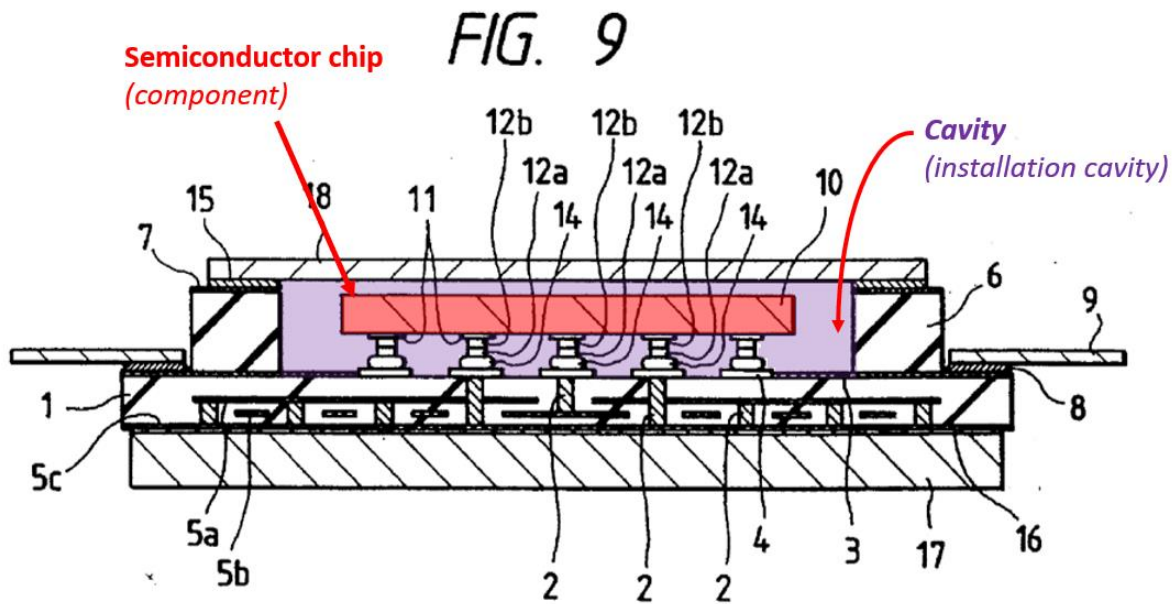


**APPLE-1004, FIG. 10 (annotated)**

109. Even in embodiments that lack Au ribbon 22, Nishiuma confirms that the space between the semiconductor chip 10 and cap 18 can be narrowed relative to the space provided in FIG. 1. See APPLE-1004, FIG. 9. As described above, in the context of the '207 patent, component thickness refers to or encompasses the height of the component *after installation in the cavity*. *Supra* §X.D.i (Claim 2). This is common sense, as it is non-sensical to compare the component thickness to the thickness of the installation cavity to assess protrusion, as discussed in the specification, when other structures such as contact bumps also exist in the cavity after the component is mounted – and in fact underly the component so that a component that is exactly the thickness of the cavity would be forced to protrude to accommodate the underlying structures. Further, while the '207 patent does not

define a tolerance for the “about” modifier in claim 3, it indicates that the thicknesses of the component and installation cavity need not be exactly the same. A POSITA would have understood that a component whose absolute thickness before installation is slightly less than the cavity thickness to accommodate a thickness of contact bumps and similar structures like Nishiuma’s thin Au ribbon would still be *about* equal to the thickness of the cavity since the component otherwise fills the thickness of the cavity without protruding from the cavity. In short, the size of the cavity must be understood to be reduced by components that extend into the cavity, as a component that is sized the same as the cavity would otherwise not fit in view of the additional components.

110. Nishiuma makes clear that the space between the chip 10 and cap 18 is not critical and may be increased or decreased in size. For example, in the FIG. 9 embodiment, an additional Au ball is disposed between the contact pads 11 of chip 10 and wiring lands 4, thereby increasing the installed thickness of the chip 10 and reducing the amount of space between chip 10 and cap 18. APPLE-1004, 10:57-11:18, FIG. 9. The embodiments depicted in FIGS. 9 and 10 demonstrate that Nishiuma does not restrict the installed thickness of the semiconductor chip relative to the thickness of the installation cavity, nor does Nishiuma define any critical/minimum gap that must be maintained between the top of the chip and the bottom of the cap.



**APPLE-1004, FIG. 9 (annotated)**

111. The '207 patent similarly discloses nothing critical or unexpected about the thickness of the installation cavity being about equal to the thickness of the component, but rather confirms that thinner, equally thick, or thicker components are all suitable options. APPLE-1001, 7:58-8:5, 6:8-16. Indeed, a POSITA would have understood that each of the listed options for relative sizing of the installation cavity and component (i.e., thinner, thicker, equal in thickness) would have advantages and disadvantages in different situations and would be suitable in view of differing design objectives. See *supra* §IV.A. The '207 patent also does not define any specific tolerance or range imparted by the modifier “about” in the claim phrase “about equal thickness.” Nishiuma thus discloses the

same general conditions for a cavity with *about* equal thickness as the component as the '207 patent itself, which renders the additional feature recited in claim 3 obvious.

112. Selecting a relative thickness of the component and cavity in the Nishiuma-Shibata combination would have been a simple matter of design choice, and an about equal thickness would predictably be achieved through routine experimentation, e.g., to optimize component stability, minimize size of the semiconductor device, minimize length of the wire bonds, and/or optimize heat dissipation from the chip. See e.g., APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”), 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”); APPLE-1011, [0034] (“the height, h, of cavity portion 12 is also selected based on the height of the semiconductor chip and the location of the wire bonding pads on the chip”), [0017] (“The height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier... [t]he cavity portion is also preferably sized to tightly fit the

chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), [0038], [0044], FIG. 4).

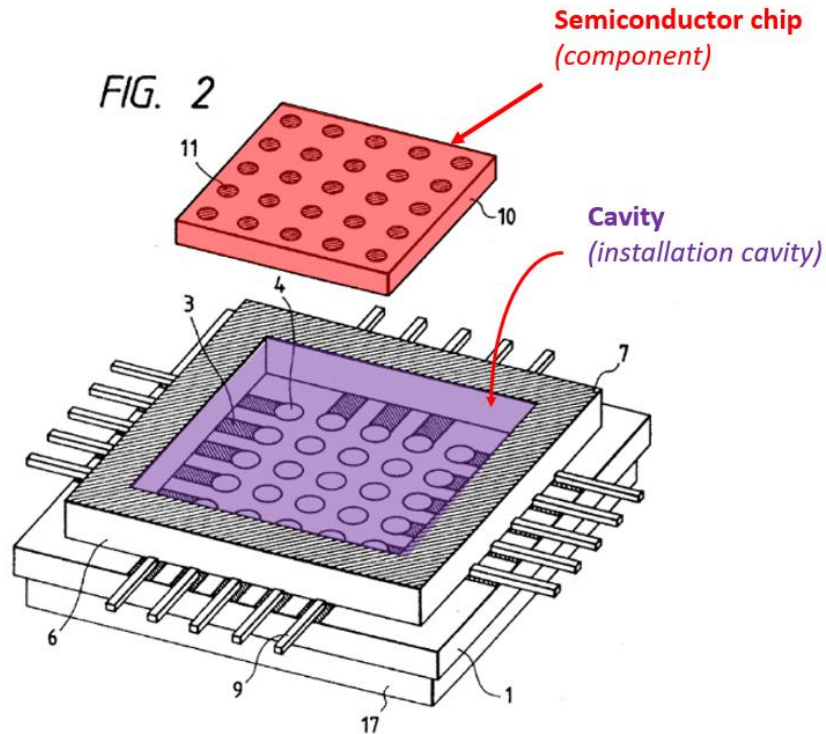
**iv. Claim 4**

***[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.***

113. Nishiuma-Shibata renders obvious claim [4]. As an initial matter and as described above with regard to claim [3], Nishiuma discloses and renders obvious an installation cavity that has about equal thickness as the semiconductor chip (component). *Supra*, §X.D.ii (Claim [3]). When the thickness of Nishiuma’s installation cavity has about the same thickness as the component, it is also dimensioned to the size of the component at least in the thickness dimension. *See* APPLE-1001, 6:14-16 (“through-cavities 2, selected to suit the size of the components 6 to be installed, are made in the insulating material layer”). Claim [4] is thus rendered obvious for at least the same reasons to those described above with regard to claim [3].

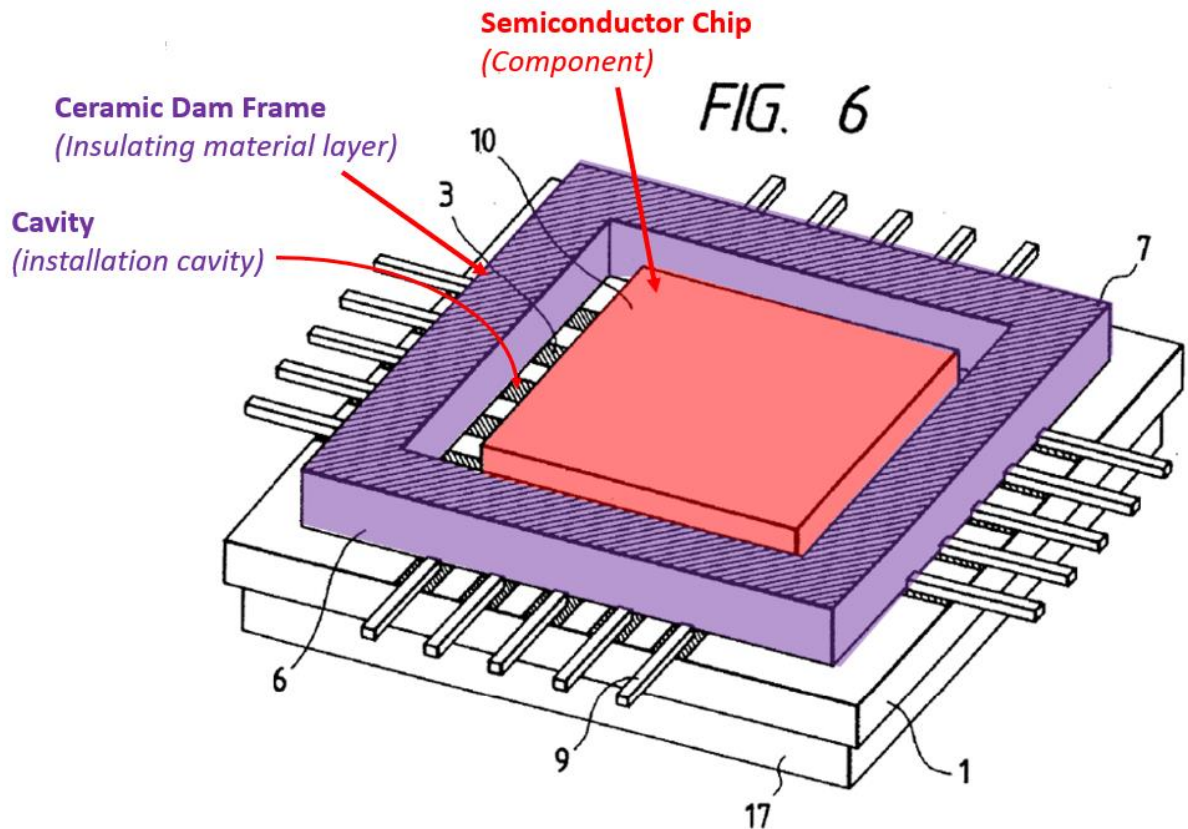
114. Moreover, Nishiuma’s FIG. 2 shows that not only is the thickness of the cavity dimensioned to the size of the component, but so too are its length and width. APPLE-1004, FIG. 2; *see also id.*, FIGS. 3-4, 6. In particular, the length and width of Nishiuma’s cavity are dimensioned to accommodate the footprint of

the semiconductor chip, and the length and width of the cavity bear a clear relationship to the length and width of the semiconductor chip.



**APPLE-1004, FIG. 2 (annotated)**

115. As an example, FIG. 6 shows the semiconductor chip positioned within the cavity formed by the insulating-material. APPLE-1004, 5:1-4, 9:13-25. Note that in FIG. 6 below, the insulating-material is annotated with purple (rather than the cavity formed by the insulating-material), as the component is positioned within the cavity here.



**APPLE-1004, FIG. 6 (annotated)**

116. A POSITA would have understood that sizing the cavity to the component to be fit into the cavity had numerous benefits, including requiring shorter wire bond lengths to minimize parasitic effects and to provide a tighter fit of the component in the cavity. APPLE-1011, [0017] (“The cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”). A POSITA would have understood that the thickness of the cavity and component is only one dimension, and that “the cross-sectional dimensions of [the] cavity portion ... are preferably

customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12.” APPLE-1011, [0034]; see also APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”), 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”). As described above, there are multiple reasons for selecting various relationships in size of the cavity and the component to be positioned therein. For example, in some cases, a larger cavity may be beneficial to provide a component with sufficient air insulation surrounding the component to cool the component. In other cases, a tighter fit between the cavity and component provide a space-saving benefit by allowing for space on the printed circuit board to be maximized. APPLE-1010, 1:49-51, 2:64-3:9, 3:27-42; APPLE-1007, [0002] (“In recent years, with the demand for higher performance and miniaturization of electronic equipment, higher density and higher function for packages in which semiconductor chips are mounted have been desired increasingly”).

v.           **Claim 5**

***[5] The electronic module of claim 1, wherein the first contact bumps comprise tin.***

117. Nishiuma-Shibata renders obvious claim [5]. As described above, Nishiuma describes “Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1” and are later flattened into Au lands 14. APPLE-1004, 8:28-48. Nishiuma does not explicitly describe that the first contact bumps comprise tin, but Shibata describes “an Sn coating is provided on the surface of an Au bump electrode.” APPLE-1005, [0038], [0030]-[0032]. Shibata explains that the addition of a tin coating to a gold bump electrode is beneficial to the bonding process, describing “[a]n Sn coating 11a is provided on the bump electrode 11 made of Au, so that at around a temperature of 230° C., Sn with a melting point of 232° C. or so melts to be alloyed with Au having a melting point of 1064° C. to thereby provide an eutectic alloy and, at around a temperature of 280° C., an alloy layer 3 made of an Au—Sn alloy is formed on the joining surface to permit both the bump electrode 11 and 21 to be melt-adhered to each other.” APPLE-1005, [0053], [0013] (“the bump electrode can be connected at a low heating temperature almost equal to the melting point of the second metal so that by selecting, for example, Sn as the material of the second metal, it is unnecessary to apply such a heating temperature that may affect the circuit elements, thus

avoiding adverse effects on these elements owing to a high temperature.”). Shibata further describes that the use of a Sn alloy material layer may allow self-alignment of the semiconductor chip and the substrate during bonding. *Id.*, [0057]-[0058].

118. I note that the ’207 patent itself does not identify any particular advantages to the use of tin in the first contact bumps. APPLE-1001, 6:58-59 (“Possible metals include particularly copper, aluminum, gold and tin”). The selection of a particular metal, such as tin, for use in the first contact bumps, however, would have been an obvious design choice.

119. It would have been obvious to a POSITA to implement Nishiuma’s Au balls 13 or lands 14 (***first contact bumps***) with a coating of tin to form an alloy that would promote improved bonding with the Au balls of the component (which can also optionally be coated with tin in the Nishiuma-Shibata combination). APPLE-1005, [0053], [0057]-[0058], [0013]; APPLE-1004, 9:13-16, 8:17-19, 8:28-29, 17:19-23. A POSITA would have recognized that the selection of tin for use in the Au balls or lands would have been an obvious design choice, and a POSITA would have been motivated to provide tin in Nishiuma’s Au balls 13/Au lands 14 to enable formation of a eutectic Au-Sn alloy and promote bonding just as Shibata describes. APPLE-1005, [0053], [0057]-[0058], [0026]. A POSITA would have understood that design considerations in the selection of materials for a semiconductor integrated circuit device balance various characteristics of the

materials such as electrical conductivity, thermal conductivity, bonding strength and characteristics, ease of use, and cost, and would have recognized that the use of tin in the formation of the balls and lands would have provided a suitable material for providing electrical connection between the surface wiring and semiconductor device.

120. A POSITA would have reasonably expected success in making the combination at least because the addition of tin to an Au ball would have been well within the skill of a POSITA and because of the similarities between Nishiuma and Shibata's methods in which tin would be applied to coat the same material (Au) in the combination as it is applied in Shibata. *See supra* §X.C (Nishiuma-Shibata Combination).

**vi. Claim 6**

***[6] The electronic module of claim 1, wherein the second contact bumps comprise copper.***

121. Nishiuma-Shibata renders obvious claim [6]. As described above, Nishiuma describes Au balls 12 (***second contact bumps***) "having a diameter smaller than that of the Au lands 14 are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10." APPLE-1004, 7:41-43, 8:17-19. Nishiuma does not explicitly describe that Au balls 12 include copper, but a POSITA would have recognized that the use of copper in contact bumps like

Nishiuma's Au balls 12 was a conventional option before the Critical Date of the '207 patent.

122. For example, Shibata teaches that "bump electrodes 11 and 21 [can be] made of Au, Cu, etc. respectively." APPLE-1005, [0052]. Nishiuma also invites the use of metals in addition to Au to form the balls 12 bonded to electrode pads 11. APPLE-1004, 2:60-64 ("according to the present invention a metal formed of metal other than Pb such as Au is formed using a ball bonding method onto an electrode pad ...").

123. I note that the '207 patent itself does not identify any particular advantages to the use of copper in the second contact bumps. APPLE-1001, 6:58-59 ("Possible metals include particularly copper, aluminum, gold and tin"). The selection of a particular metal, such as copper, for use in the second contact bumps, however, would have been an obvious design choice. For example, a POSITA would have understood that copper has a higher electrical conductivity than gold, and a lower electrical resistance would be expected from a copper contact bump as compared to gold. APPLE-1035, 133. A POSITA would have been motivated to replace some or all of Nishiuma's Au balls 12 with copper for the electrical conductivity advantages associated with the use of copper.

124. A POSITA would have been motivated to implement Nishiuma's balls 12 using copper in accordance with Shibata's teaching to provide an

advantageously low resistive drop between the component and circuit board.

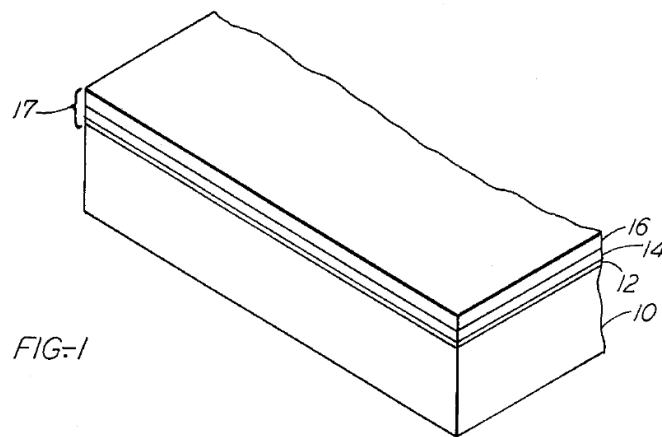
APPLE-1005, [0052] (“on the electrode terminals 12 and 22 made of aluminum are respectively formed barrier metal layer 14 and 24 is a two-layer or three-layer construction... [t]hereon are formed the bump electrodes 11 and 21 made of Au, Cu, etc.”); [0073] (“the barrier metal layer 14 serves to prevent the Al electrode terminal 12 from being oxidized so that it may be connected with the Au wiring 18 at a low resistance”). Accordingly, a POSITA would have been motivated to implement Nishiuma-Shibata’s semiconductor integrated circuit device with Au balls including copper (for example in addition to gold), per Shibata, to achieve the low resistive drop between component and circuit board when they are bonded together. APPLE-1005, [0052], [0073]; APPLE-1012, 152-154 (describing resistance of copper lines). A POSITA would have considered the selection of copper for use in the balls to be an obvious design choice. A POSITA would have understood that design considerations in the selection of materials for a semiconductor integrated circuit device balances various characteristics of the materials such as electrical conductivity, thermal conductivity, bonding strength and characteristics, ease of use, and cost, and would have recognized that the use of copper in the formation of the balls would have provided a suitable material for providing electrical connection between the surface wiring and semiconductor device.

125. A POSITA would have reasonably expected success in making the combination at least because the addition of copper to the Au balls would have been well within the skill of a POSITA and because of the similarities between Nishiuma and Shibata's methods. *See supra* §X.C (Nishiuma-Shibata Combination).

**XI. GROUND 1B: CLAIMS 1-6 ARE OBVIOUS UNDER 35 U.S.C. § 103 BASED ON NISHIUMA IN VIEW OF SHIBATA AND GLICK**

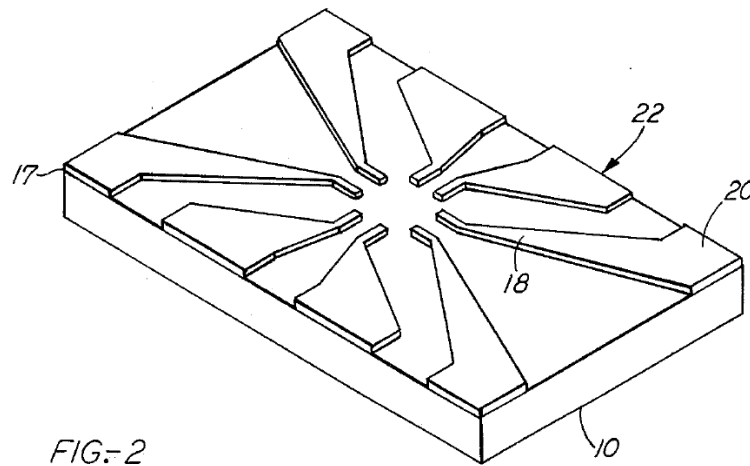
**A. Glick Overview (APPLE-1020)**

126. Glick describes a method “for strengthening bonds between thin-film conductors and insulating substrates on which they are formed.” APPLE-1020, 1:6-10. Glick describes that in Figure 1, “[a] layer of titanium 12 is first deposited on the substrate 10... [n]ext a layer of palladium 14 is deposited on the titanium... [and f]inally, a layer of gold 16 is plated over the palladium.” APPLE-1020, 2:56-66; 1:63-66.



**APPLE-1020, FIG. 1**

127. Glick describes that “[i]f it is desired to reduce the amount of gold, copper may be substituted for most of the gold, i.e., the gold layer may be replaced by a layer of copper plated with gold.” *Id.*, 2:67-3:2. To prevent diffusion of the copper through the gold leading to oxidation of the bonding surface, “[a] barrier of nickel... is placed between the copper and gold.” *Id.*, 3:6-7. Thus, “a conductor layer which includes copper would consist of titanium and palladium sequentially evaporated on the substrate and then copper, nickel, and gold sequentially plated on the palladium.” *Id.*, 3:7-11.



**APPLE-1020, FIG. 2**

128. Following preparation of the composite conductive layers, “film 17 is formed into a pattern 22 of individual conductors 18 and contact pads 20 on the substrate 10,” for example as shown in Figure 2. *Id.*, 3:12-16.

**B. The Nishiuma-Shibata-Glick Combination**

129. Nishiuma discloses that “[t]he surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au in the order from the bottom.” APPLE-1004, 7:14-16. A POSITA would have understood that conductive patterns, such as Nishiuma’s surface wiring and wiring lands, may be plated for a variety of reasons, including to prevent oxidation and improve adherence and conductivity, and that the materials with which a surface wiring and land are plated are not limited to Ni and Au. *See e.g.*, APPLE-1006, 4:65-5:3 (describing deposition of metal layers to provide an advantageous alloy upon melting), 5:4-13 (describing deposition of multiple layers to increase a size of a contact area); *see also* APPLE-1020, 1:50-57 (describing addition of layers for strengthening adherence between the layers and a substrate or for strengthening an external bond made to a layer), 2:67-3:2 (describing addition of layers to reduce the amount of a particular material), 3:3-7 (describing addition of layers to provide an unoxidized bonding surface). In this context, a POSITA would have appreciated and found obvious that additional layers of materials also would have been obvious to implement in Nishiuma’s wiring and lands.

130. Recognizing that having multiple materials coating surface wiring and lands, a POSITA would have turned to references, like Glick, that describe preparing a conductive pattern from multiple layers of materials. APPLE-1020,

2:56-3:11. Like Nishiuma, Glick describes coating conductive patterns with layers of materials, including nickel and gold, although Glick describes additional layers deposited on the conductive patterns to improve adherence and reduce costs.

APPLE-1020, 2:52-3:11. In particular, Glick describes “a conductor layer ...consist[ing] of titanium and palladium sequentially evaporated on the substrate and then copper, nickel and gold sequentially plated on the palladium”). *Id.*, 3:7-11; *supra*, §XI.A. Multiple reasons would have motivated a POSITA to implement Nishiuma’s conductive surface wiring and lands in accordance with Glick’s suggestion to incorporate additional layers of metals as described below. APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:11.

131. First, a POSITA would have been motivated to implement Nishiuma’s surface wiring and lands with additional layers, as Glick suggests, to improve the adherence of the wiring and lands to the underlying substrate. A POSITA would have recognized that it is beneficial for the surface wiring and wiring lands to be strongly attached to the substrate to provide a robust device unlikely to become unattached during manufacture, shipping or use. For example, Glick describes a layered conductor structure including a titanium base layer to improve adherence of the conductor to the substrate, and the layers to one another. APPLE-1020, 2:56-60, 1:50-57, Abstract.

132. Second, a POSITA would have understood that the use of gold in a conductive pattern may be costly and would have been motivated to implement the surface wiring and lands with additional material layers to decrease manufacturing and processing costs. *See* APPLE-1035, 138-139 (describing relative costs of gold compared to materials Glick describes like copper and nickel). For example, a POSITA would have been motivated to implement Nishiuma's surface wiring and lands with the layered conductor structure taught by Glick, including layers of copper, nickel, and gold to minimize the amount of gold needed for the surface wiring. APPLE-1020, 2:67-3:11; APPLE-1035, 138-139.

133. A POSITA would have had a reasonable expectation of success in implementing Nishiuma's surface wiring and lands with additional material layers as Glick suggests for a variety of reasons. For example, the combination would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all the reasons described above and given that the similarities between Nishiuma's teachings of plated surface wirings and Glick's suggestion to add additional wires. APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:11, Figs. 1-2. For example, both Nishiuma and Glick provide examples in which a top layer of the wiring is gold and further describe the use of a nickel layer beneath the gold layer. APPLE-1004, 7:14-16 ("The surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au in the order

from the bottom”), 9:66-10:3; APPLE-1020, 2:56-66 (describing layers of titanium, palladium, and gold), 3:3-11 (describing that “gold is needed to provide a good unoxidized bonding surface” in a layered structure including copper and nickel beneath a gold top layer), 3:12-16, FIGS. 1-2.

134. A POSITA would have had a reasonable expectation of success because the layered conductor structure taught by Glick is complimentary to the layers described by Nishiuma. As described above, both Nishiuma and Glick describe layered structures with a top layer formed from gold. APPLE-1004, 7:14-16; APPLE-1020, 2:56-66, 3:3-16. A POSITA would have recognized that Nishiuma’s nickel and gold layers could be expanded to include the additional layers taught by Glick while maintaining an unoxidized gold bonding surface for connection with the Au balls 13. APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:11.

135. Additionally, a POSITA would have understood that implementing additional conductive material layers on a surface wiring and wiring lands in the combination would have been obvious as a predictable application of a known technique of implementing multiple conductive layers as taught by Glick to a known system as taught by Nishiuma to achieve entirely predictable results. A POSITA would have understood, for example, that the use of multiple material layers in a wiring pattern was conventional and that the use of coating and plating

techniques to provide wiring patterns with more than one layer of material was well-known. A POSITA would have further understood that implementing Nishiuma's conductive surface wiring and wiring lands with multiple layers would have been as simple as plating additional layers on these features – well within the level of skill of the POSITA. A POSITA would have understood that the use of materials such as those that both Nishiuma and Glick discuss, for example, gold, copper, nickel, would have had predictable results of providing a conductive surface wiring with known benefits like improving conductivity, decreasing oxidation, decreasing cost by using a smaller amount of expensive materials like gold, and other similarly well-known advantages. *See e.g.*, APPLE-1020, 2:56-3:11.

**C. Claim-by-Claim Analysis**

**i. Claim 1**

***[1.pre] An electronic module, comprising:***

136. *See supra* §X.D.i (Ground 1A Element [1pre]).

***[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;***

137. The Nishiuma-Shibata-Glick combination discloses and renders obvious elements [1a]-[1b.ii]. As described above, Nishiuma's plurality of surface

[illegible]

89

139. A **first surface** of the second conductive-pattern layer is formed by the top of the gold coating layer of the surface wires and lands.

***[1c]-[1e.i] an insulating-material layer disposed on the first surface of the second conductive-pattern layer; at least one installation cavity disposed in the insulating-material layer; a component disposed within the at least one installation cavity,***

140. See *supra* §X.D.i (Ground 1A Elements [1c]-[1e.i]). In the Nishiuma-Shibata-Glick combination, the ceramic dam frame (“**insulating-material layer**”) is disposed on the first surface of the layered surface wiring and lands (“**second conductive-pattern layer**”).

***[1e.ii]-[1g] the component comprising contact zones comprising aluminum; first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and second contact bumps disposed on the contact zones and electrically connected thereto,***

141. See *supra* §X.D.i (Ground 1A Elements [1c]-[1e.i]). In the Nishiuma-Shibata-Glick combination, the Au balls/lands (“**first contact bumps**”) are formed on the **first surface** of the layered surface wiring and lands (“**second conductive-pattern layer**”).

***[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.***

142. Nishiuma-Shibata-Glick renders obvious element [1h]. *Supra* §XI.C.i (Ground 1B Elements [1a]-[1b.ii]); §VIII.A. As discussed above, in the Nishiuma-Shibata-Glick combination, surface wires and lands comprising titanium and palladium (collectively the “***first conductive-pattern layer***”) are plated in copper, nickel, and gold (collectively the “***second conductive-pattern layer***”). APPLE-1004, 7:7-16; APPLE-1020, 2:52-3:20. The surface wiring and lands layer (***first conductive-pattern layer***) has two sublayers that each comprises a different material: (1) titanium and (2) palladium, and the coatings layer (***second conductive-pattern layer***) has three sublayers that each comprise a different material: (1) copper, (2) nickel, and (3) gold. *Supra* §XI.B (Nishiuma-Shibata-Glick Combination); APPLE-1020, 2:52-3:20. Accordingly, in the Nishiuma-Shibata-Glick combination *both* the first conductive-pattern layer *and* the second conductive-pattern layer each has at least two layers of two different materials.

143. As I described above, the plain meaning of this limitation requires that only one of the two conductive-pattern layers has two layers of two materials – the Nishiuma-Shibata-Glick combination further satisfies the stricter read of the

limitation with both conductive-pattern layers meeting the criteria of having two layers of two different materials. *Supra* §VIII.A.

**ii. Claims 2-6**

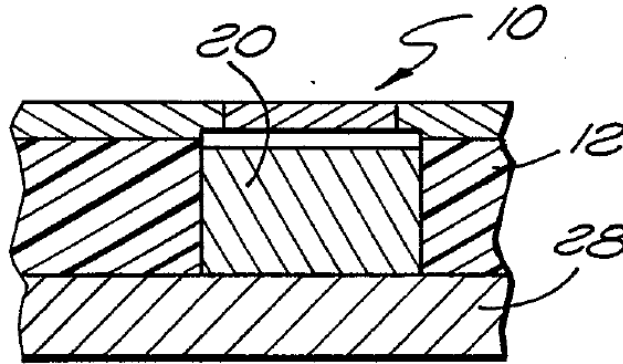
144. *See supra* §§X.D.ii-vi (Ground 1A Claims 2-6).

**XII. GROUND 1C: CLAIMS 3-4 ARE OBVIOUS UNDER 35 U.S.C. § 103  
BASED ON NISHIUMA IN VIEW OF SHIBATA AND PARKER**

**A. Parker Overview (APPLE-1010)**

145. Parker describes “methods of making printed circuit boards having grooves for receiving electrical leads and cavities for receiving electrical components.” APPLE-1010, 1:6-8. Parker describes that “[printed circuit] boards generally include a thin substrate made from a suitable electrically insulating material such as a ceramic or an epoxy-glass composite.” APPLE-1010, 1:10-12.

146. Parker describes that a punch can be used to produce cavities 18 in the substrate 12. *Id.*, 2:5-27; 4:3-19. “Cavities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities.” *Id.*, 1:49-51, 2:64-3:9.



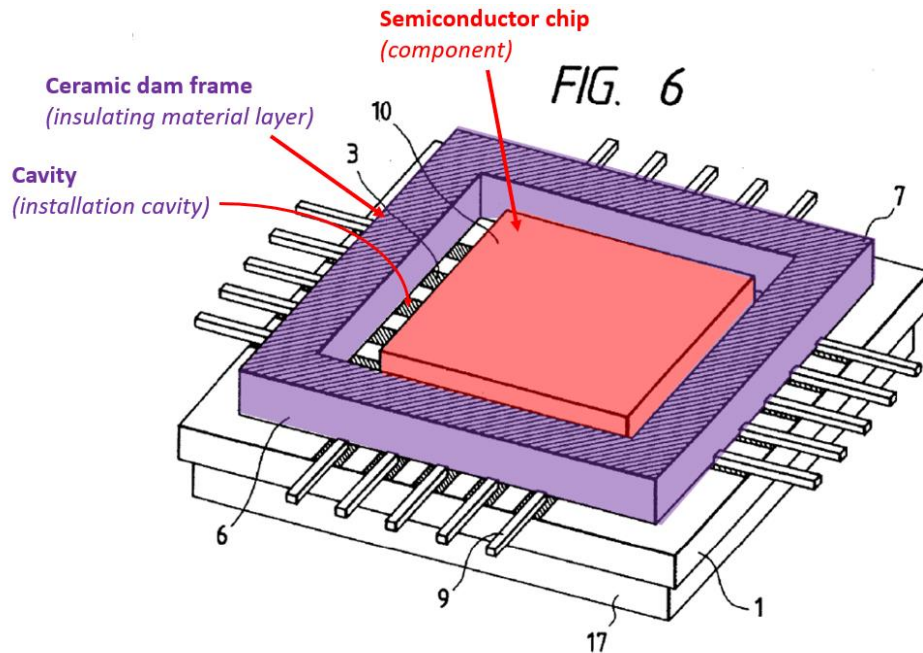
**APPLE-1010, FIG. 2**

147. For example, in Figure 2, reproduced above, a transistor 20 is positioned within a cavity formed in the substrate 12 of the printed circuit board 10. *Id.*, 3:18-22. “A heat sink 28 may be disposed below the transistor [20] in one of the cavities to receive heat from the transistor 20 and thereby prevent the transistor from overheating.” *Id.*

**B. The Nishiuma-Shibata-Parker Combination**

148. Nishiuma describes that “[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted.” APPLE-1004, 7:53-54.

Nishiuma’s FIG. 6 illustrates that the sealing dam frame 6 forms a cavity sized to accept the semiconductor chip 10 within. *Id.*, FIGS. 1, 2, 6, 10.



**APPLE-1004, FIG. 6 (annotated)**

149. A POSITA would have understood that a cavity formed in the circuit board is sized to fit the device intended to be mounted within the cavity, and would have further understood that there are a variety of ways to size the cavity to the device. *See e.g.*, APPLE-1011, [0034] (“the cross-sectional dimensions of cavity portion 12... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12”), [0017] (“[t]he height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier.”), [0038], [0044], FIG. 4; *see also supra* §IV.A. In this context, a POSITA

would have turned to references like Parker that describe sizing considerations for a cavity.

150. For example, Parker describes “[c]avities 18 are [] provided in one or both of the parallel surfaces of the substrate 12” of the printed circuit board.

APPLE-1010, 2:64-65, FIG. 2. “Electrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.” *Id.*, 2:66-3:1. Like Nishiuma, Parker describes mounting a device within a circuit board cavity and additionally provides guidance as to the sizing of the cavity relative to the component to be mounted therein. For example, Parker provides guidance to size the cavity to the dimensions of the component. *See e.g.*, APPLE-1010, 2:64-3:1. A POSITA would have recognized that a cavity would need to be at least large enough to partially accept a component to be installed therein (*see e.g.*, APPLE-1007 describing a concave portion formed “to ensure a space in which the surface acoustic wave devices 601 are mounted”), and further that there are design benefits to sizing the cavity to be larger or smaller relative to the component size and depending on the design objectives of the device.

151. Multiple reasons would have motivated a POSITA to implement Nishiuma’s cavity to be sized to the dimensions of the component in accordance with Parker’s suggestions as described below. APPLE-1010, 1:49-51, 2:64-3:1, FIG. 2.

152. First, a POSITA would have understood that sizing the cavity to have a tight fit with the component optimizes the use of limited space on the printed circuit board. For example, a POSITA would have understood that higher density packages were desirable by the Critical Date and that optimizing use of available space on the circuit board allows for such optimization. *See* APPLE-1011, [0034] (“the cross-sectional dimensions of [the] cavity portion ... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12.”); APPLE-1007, [0002] (“In recent years, with the demand for higher performance and miniaturization of electronic equipment, higher density and higher function for packages in which semiconductor chips are mounted have been desired increasingly”); APPLE-1010, [0017]; APPLE-1036, 1 (“Footprint reduction of the integrated device is an additional need, especially for portable device applications”); *see also supra* §IV.A.

153. Second, to the extent that components are connected to the printed circuit board by wires in addition to contact bumps, positioning a component in a cavity with a tight fit requires shorter wire bond lengths and reduces parasitic effects. APPLE-1010, [0017] (“The cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that]

parasitic effects are minimized.”); FIG. 8; APPLE-1004, 1:18-33 (describing benefits to operating speed with shorter wiring length).

154. Third, a POSITA would have understood that a tight fit between the cavity and the component allows for the component to be easily placed in proper position within the cavity to provide electrical connection between the component and wiring in the cavity. APPLE-1011, [0006] (contrasting with the use of ball grid arrays). For example, Parker describes that transistors may have “a considerabl[e] number of closely spaced electrical terminals such as the pads 26” which must be electrically connected to the circuit board. APPLE-1010, 3:65-4:2. A POSITA would have understood that closely fitted side walls may guide the positioning of the device within the cavity so that electrical connections to the circuit board are aligned during placement of the component. APPLE-1004, 2:34-50; *see also* APPLE-1037, 2 (“the embedded interconnections in the MCM structure provide good protection both mechanically and chemically”).

155. Fourth, a POSITA would have appreciated that there are a limited number of possible size relationships between a cavity and a component sized to fit in the cavity. For example, the '207 patent explains that the component can be shorter, taller, or the same height as the cavity. APPLE-1001, 6:7-16 (describing that the installation base can be thicker than, less thick than, or equally thick as the component). Additionally, a POSITA would have understood that the relationship

between dimensions of the component and cavity other than the height/thickness (i.e., the length and width of the component and cavity) are similarly constrained so that the cavity is closely fitted to the component in length and width or is larger than the component in these respects. It would have been obvious to a POSITA that a cavity intended to receive a component must have dimensions at least sized to allow the component to be placed therein, and can additionally have a height that is shorter than, equal to, or thicker than the height of the component.

156. A POSITA would have found it obvious to try these finite and predictable solutions to sizing the cavity relative to the component and would have had a reasonable expectation of success in implementing them, given that these are conventional methods for mounting a component within a cavity. *See e.g.*, APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”); 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”); APPLE-1011, [0034] (“the height, h, of cavity portion 12 is also selected based on the height of the semiconductor chip and the location of the wire bonding pads on the chip”), [0017] (“The height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor

chip are at approximately the same height as the flange portion of the chip carrier... [t]he cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), [0034], [0038], [0044], FIG. 4.

157. A POSITA would have had a reasonable expectation of success implementing the combination for all the reasons described above and given that Parker describes techniques for disposing components on a printed wiring board and within a cavity, like Nishiuma. APPLE-1004, 7:7-55; APPLE-1010, 1:49-51, 2:5-27, 2:64-3:22. Implementing a semiconductor integrated circuit with a cavity that has a tight fit to the component would have been obvious as a predictable application of a known technique for positioning components in a printed circuit board as taught by Parker to a known system as taught by Nishiuma to achieve entirely predictable results. As described above, a POSITA would have understood that it was conventional to place a component within a cavity of a printed circuit board, and that by providing a tight fit between the component and cavity the space on the circuit board could be optimized. *Supra* §IV.A; APPLE-1010, 1:49-51, 2:64-3:9, 3:27-42. A POSITA would have understood that implementing Nishiuma-Shibata to have a cavity that was a tight fit to the component would have been a straightforward choice during manufacture of the

printed circuit board, just as Parker teaches. APPLE-1010, Abstract, 1:49-51, 1:57-66, 2:10-13, FIGS. 1-4.

**C. Claim-by-Claim Analysis**

**i. Claim 3**

***[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.***

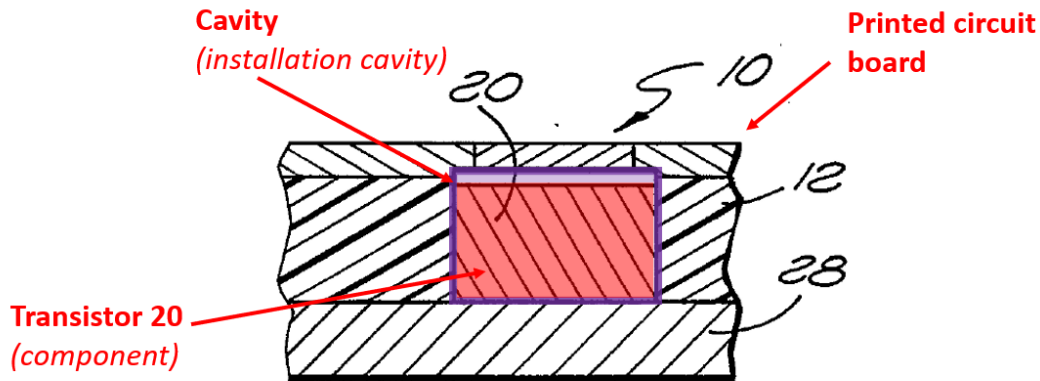
158. Nishiuma-Shibata-Parker renders obvious claim [3]. For example, Nishiuma describes that “[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted.” APPLE-1004, 7:53-54. To the extent Nishuima does not expressly disclose that the installation cavity has about equal thickness as the component, Parker teaches this conventional option. APPLE-1010, 1:49-51 (“[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities”), 2:64-3:11 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”); 3:18-22; APPLE-1004, FIGS. 1, 9, 10.

159. As described above, in the context of the ’207 patent, component thickness refers to or encompasses the height of the component *after installation in the cavity*. *Supra* §X.D.[3] (Ground 1A discussion of claim meaning in Claim [3]).

Indeed, the patent specifically relates the thickness of the component to the component's protrusion beyond the height or thickness of the installation cavity. *See, e.g.*, APPLE-1001, 7:61-8:5. This understanding comports with the specification's discussion of component thicknesses that are less than, equal to, or greater than the thickness of the installation base or cavity, especially as there would be no reason to distinguish between components of equal or greater absolute/pre-installation thickness when both would protrude from the cavity after installation due to the contact bump / electrode thickness. APPLE-1001, 6:8-17.

160. As shown in FIG. 2 below, Parker teaches that the **cavity** formed in the printed circuit board (purple box) **has about equal thickness** as the transistor 20 ("**component**"). APPLE-1010, FIG. 2. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nishiuma's cavity and device with the sizing relationship suggested by Parker so that the installation cavity has about equal thickness as the component as claimed. *Supra* § XIII.B (Nishiuma-Shibata-Parker Combination); *see also* APPLE-1011, [0034] ("the height, h, of cavity portion 12 is also selected based on the height of the semiconductor chip and the location of the wire bonding pads on the chip"), [0017] ("The height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of

the chip carrier... [t]he cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), [0038], [0044], FIG. 4.



APPLE-1010, FIG. 2 (annotated)

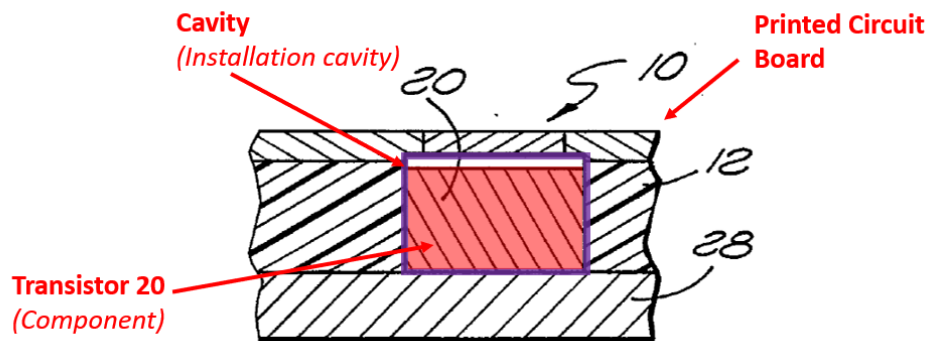
ii. Claim 4

***[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.***

161. Nishiuma-Shibata-Parker renders obvious claim [4]. For example, Parker describes “[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities.”

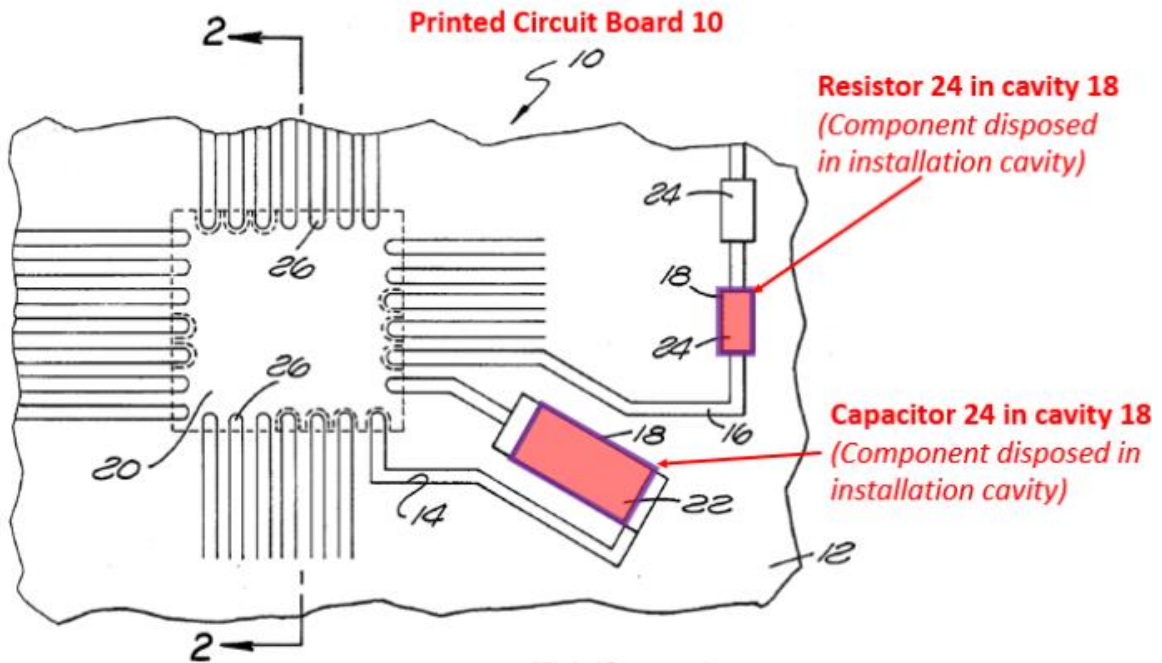
APPLE-1010, 1:49-51, 2:64-3:9. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nishiuma’s cavity and device with the sizing relationship suggested by Parker. *Supra* §XII.B (Nishiuma-Shibata-Parker Combination).

162. As shown in FIG. 2, the **cavity** formed in the printed circuit board (purple box) has a thickness and width (i.e., “dimensions”) about equal to the size of the transistor 20, and thus is “**dimensioned to the size of the component.**” *Id.*, 3:18-22.



APPLE-1010, FIG. 2 (annotated)

163. Additionally, FIG. 1 shows that the **cavities** formed in the printed circuit board are **dimensioned to the size of the components** positioned within the cavities. APPLE-1010, 2:64-3:7, 3:44-53, FIG. 1.



**APPLE-1010, FIG. 1 (annotated)**

164. A POSITA would have understood that sizing the cavity to the component to be fit into the cavity had numerous benefits, including requiring shorter wire bond lengths to minimize parasitic effects and to provide a tighter fit of the component in the cavity. APPLE-1011, [0017] (“The cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”). A POSITA would have understood that the thickness of the cavity and component is only one dimension, and that “the cross-sectional dimensions of [the] cavity portion ... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12.” APPLE-1011, [0034]; see

also APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”), 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”).

165. As described above, there are multiple reasons for selecting various relationships in size of the cavity and the component to be positioned therein. For example, in some cases, a larger cavity may be beneficial to provide a component with sufficient air insulation surrounding the component to cool the component. In other cases, a tighter fit between the cavity and component provide a space-saving benefit by allowing for space on the printed circuit board to be maximized.

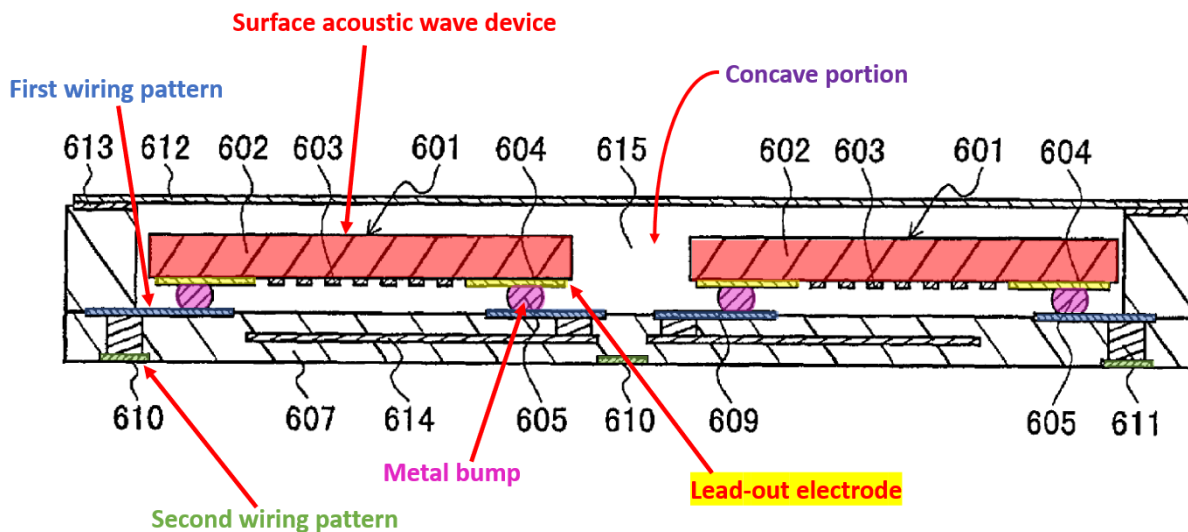
APPLE-1010, 1:49-51, 2:64-3:9, 3:27-42; APPLE-1007, [0002] (“In recent years, with the demand for higher performance and miniaturization of electronic equipment, higher density and higher function for packages in which semiconductor chips are mounted have been desired increasingly”).

### **XIII. GROUND 2A: CLAIMS 1-2 AND 5-6 ARE OBVIOUS UNDER 35 U.S.C. § 103 BASED ON NAKATANI IN VIEW OF ONDA AND GLICK**

#### **A. Nakatani Overview (APPLE-1007)**

166. Nakatani describes “a conventional surface acoustic wave device built-in module.” APPLE-1007, [0016]. Nakatani’s FIG. 7 depicts the

conventional device having a circuit board 607, first wiring patterns 609, second wiring patterns 610, via holes 611, and surface acoustic wave devices 601 positioned within a concave portion 615. APPLE-1007, [0017], [0019].



**APPLE-1007, FIG. 7 (annotated)**

167. Nakatani describes that “[i]n the surface acoustic wave device 601, on one surface of the piezoelectric substrate 602 ... the comb-shaped electrode 603 and the lead-out electrodes 604 formed of a metal film containing aluminum as a main component are formed.” *Id.*, [0018]. “The metal bumps 605 for an electrical connection with an external circuit are formed on the lead out electrodes 604.” *Id.* “After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected [and w]hen gold bumps are used as the metal bumps 605,

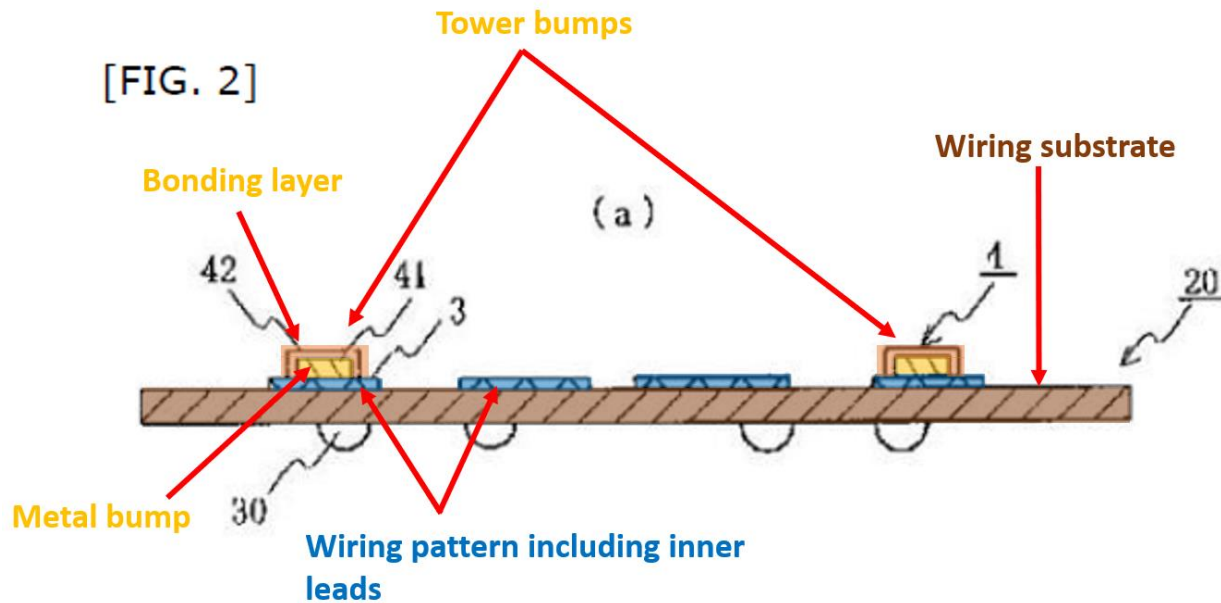
heat and ultrasonic wave are used in combination so as to melt the metal bumps 605 for the connection.” *Id.*, [0020].

168. Nakatani’s FIG. 7 is described as a prior art example of a “conventional surface acoustic wave device built-in module.” APPLE-1007, [0016]. FIG. 7 is thus an example of what was Nakatani recognized as well known in the prior art before the Critical Date. *See supra* §IV.A. Although Nakatani goes on to describe mechanisms for producing “a thinner component built-in module” compared to the prior art device depicted in FIG. 7, this does not detract from the Nakatani’s teachings of common characteristics and features of conventional devices. APPLE-1007, [0023].

**B. Onda Overview (APPLE-1008)**

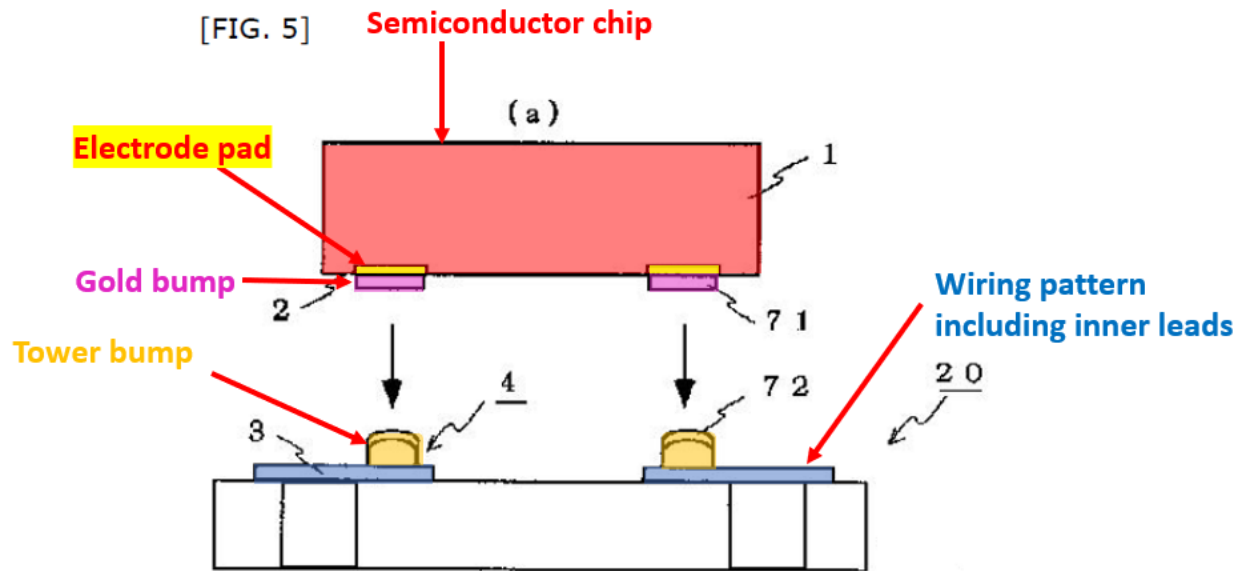
169. Onda describes techniques for connecting a wiring substrate to a semiconductor chip in which “tower bumps 4 are formed on the connecting portions [of the wiring pattern] to connect with the semiconductor chip.” APPLE-1008, [0045]. “The tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to [] electrode pads 2 of the semiconductor chip 1.”

APPLE-1008, [0045].



APPLE-1008, FIG. 2

170. For example, in Figure 5(a), Onda illustrates the process of mounting a “semiconductor chip 1 on the manufactured wiring substrate 20.” *Id.*, [0067]-[0070]. “[A]fter preparing the wiring substrate 20... and aligning the plurality of electrode pads 2 and tower bumps 4 formed on the main surface of the semiconductor chip 1, the semiconductor chip 1 is fixed” to the wiring layer using heat and pressure. *Id.*, [0068]; *see also* [0069]-[0083], [0092]-[0098], Figs. 6(a), 8(a), 9(a) (showing similar manufacturing methods that couple bumps on the semiconductor chip with tower bumps on the wiring layer).



APPLE-1008, FIG. 5

C. The Nakatani-Onda-Glick Combination

i. Nakatani Combined with Onda

171. Nakatani discloses that “lead-out electrodes 604 formed of a metal film containing aluminum as a main component are formed” and metal bumps 605 are formed on the lead-out electrodes. APPLE-1007, [0018]. “After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected.” *Id.*, [0020]; *supra* §XIII.A.

172. In one illustrated embodiment, Nakatani shows the metal bumps 605 connected directly to the wiring patterns 609 of the circuit board. APPLE-1007, FIG. 7. However, Nakatani does not limit the described connection between the

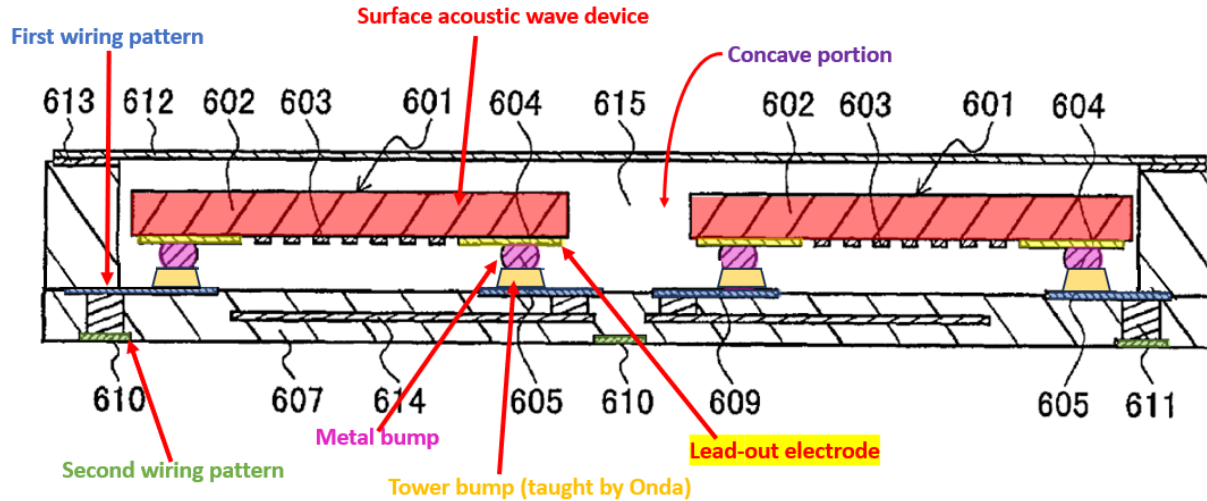
semiconductor and the circuit board to this arrangement, and a POSITA would have understood that other connection schemes would also be suitable for electrically connecting the metal bumps 605 to the first wiring patterns 609. *Id.*, [0016] (“FIG. 7 is a sectional view showing one example of a structure of a conventional surface wave device built-in module...”); [0017]-[0020], [0126] (“In the present embodiment, the gold bumps are used as the metal bumps 505, but the present invention is not limited to them”). A POSITA would have been aware of other conventional solutions for bonding a component to a wiring substrate or circuit board and would have considered other options to achieve known benefits associated with those options.

173. Recognizing that devices commonly are connected to wiring patterns of printed circuit board by conductive contact bumps formed on the device electrode pads and conductive bumps formed on the wiring, a POSITA would have turned to references like Onda to investigate the implementation of pairs of conductive bumps for electrically connecting Nakatani’s surface acoustic wave devices to the circuit board. *See* APPLE-1007, [0016]-[0020], [0072]-[0073], [0078]-[0079], [0086], [0096], [0118], [0122], [0126], [0133], [0147]-[0148], FIGS. 1, 5-7. Like Nakatani, Onda describes techniques for coupling a device’s electrode pads to wiring of a circuit board, although Onda makes the electrical connection using pairs of conductive bumps – conductive bumps formed on the

wiring substrate connected to conductive bumps formed on the electrode pads of the device. APPLE-1008, [0039], [0045]-[0046], [0072]-[0074], [0085]-[0086], [0093]-[0094], [0100]-[0101], [0107]-[0108], [0114]-[0115] FIGS. 5-9.

174. For example, Onda describes that a tower bump is formed on the wiring pattern of the PCB to provide an electrical connection to the semiconductor device and to buffer thermal stresses. *See* APPLE-1008, [0046] (“Alternatively, in the above-described method for manufacturing the electric element built-in module, a bump is formed on the connection electrode of the electric element, and the electric element may be mounted on the wiring pattern by connecting the bump and the wiring pattern in an ultrasonic manner. This makes it possible to reduce a thermal load on the electric element.”).

175. Onda describes that two conductive bumps can be used to couple a device to a wiring substrate: “gold plating (gold bumps) 71 are formed on each electrode pad 2 [of the device and the] wiring layer of the substrate including inner leads 3 is provided with tower bumps 4 consisting of copper bumps 4 consisting of copper bumps (metal bumps 41).” APPLE-1008, [0073].



**APPLE-1007, FIG. 7 (annotated, modified to include Onda’s teaching to use two conductive bumps to electrically couple the device and circuit board)**

176. It would have been obvious to a POSITA to implement the combination of tower bumps and electrode bumps as taught by Onda into Nakatani’s device in place of the single metal bump described by Nakatani for a number of reasons.

177. First, a POSITA would have understood that using electrode bumps (gold bumps) on the device and tower bumps on the circuit board to electrically connect the device to the printed circuit board would improve the ease of making the connection between the component and the wiring pattern. Onda describes that in conventional methods, “bumps in the form of protrusions are formed on the main surface of the semiconductor chip 1 on electrode pads 2 to make connection to the inner lead 3 easier and improve the reliability of the connection.” APPLE-1008, [0005]. Onda’s suggestion of tower bumps formed on the circuit board

would further simplify the method of providing electrical connection between the device and circuit board, because the bumps aid in the alignment of the device with electrical contact points of the printed circuit board.

178. Second, a POSITA would have understood that the addition of a metal tower bump to electrically connect the surface acoustic wave device to the printed circuit board would improve the device's resistance to thermal stresses. APPLE-1008, [0046], [0012], [0041]. For example, Onda describes that "the wiring substrate [is] characterized in that electrical connections of the semiconductor devices and the wiring pattern and tower bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip have been provided on the wiring patterns where the semiconductor chip is mounted on the insulating substrate." *Id.*, [0012]. A POSITA would have understood that the addition of metal balls between the component and substrate would improve resistance to thermal stresses because the metal balls would be able to absorb thermal stresses that would otherwise be on a direct connection between the component and printed board. APPLE-1005, [0060], [0014], [0022], [0084].

179. Onda describes that providing a tower bump on the circuit board for connection to the bumps on the semiconductor chip may "prevent[] cracking of semiconductor chips due to thermal stress." APPLE-1008, [0010]; *see also id.*, [0008]-[0012], [0070]; APPLE-1011, [0004] ("Reliability concerns often arise in

flip-chip-on-board technology; for instance, due to a mismatch between the coefficients of thermal expansion between the semiconductor chip and the substrate, the solder joints may fatigue.”), [0014] (describing thermal mismatch between a conventional substrate and chip carrier).

180. Third, a POSITA would have understood that providing conductive bumps to electrically connect the device and the circuit board would allow for the selection and use of materials that increase the strength of the connection between the device and circuit board. APPLE-1008, [0076]. The selection of materials with high resistance to thermal stresses and which provide strong bonds between the component and printed wiring board could absorb stresses and shocks and provide a more reliable connection between the component and printed wiring board less susceptible to common failures.

181. Fourth, implementing a surface acoustic wave device module electrically coupled to the circuit board by conductive bumps formed on the wiring and on the device electrodes would have been obvious as a predictable application of a known technique for coupling devices to a printed circuit board as taught by Onda to a known system as taught by Nakatani to achieve entirely predictable results. A POSITA would have understood that using two sets of contact bumps (one on the component and one on the substrate) was a well-known method for electrically connecting a component to circuit board by the Critical Date, and a

POSITA would have understood that implementing this conventional method would predictably achieve an electrical connection between the device and substrate wiring, just as Onda teaches.

182. The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all of the reasons above and given the similarities between the connection methods described by Nakatani and the techniques suggested by Onda. APPLE-1007, [0016]-[0021]; APPLE-1008; [0068]-[0083], [0092]-[0098].

**ii. Nakatani-Onda Combined with Glick**

183. Additionally, Nakatani describes that “[a] copper foil can be used as the wiring pattern 201, and a copper foil plated with nickel or gold further is preferable because of its stable electrical connection with the metal bumps 202 on the semiconductor chip 203.” APPLE-1007, [0078]. However, Nakatani does not limit the wiring pattern to a copper foil with nickel or gold plating, and, as described above (§XI.A), a POSITA would have been aware that wiring patterns may be plated for a variety of reasons, including to prevent oxidation and improve adherence and conductivity, and that the materials with which a surface wiring and land are plated are not limited to Ni or Au. *See e.g.*, APPLE-1007, [0091] (“in order to improve the adhesion and prevent oxidation, the surface of the copper plating layer may be treated with the coupling agent or plated with tin, zinc, nickel,

or gold”); APPLE-1006, 4:65-5:3 (describing deposition of metal layers to provide an advantageous alloy upon melting), 5:4-13 (describing deposition of multiple layers to increase a size of a contact area); *see also* APPLE-1020, 1:50-57 (describing addition of layers for strengthening adherence between the layers and a substrate or for strengthening an external bond made to a layer), 2:67-3:2 (describing addition of layers to reduce the amount of a particular material), 3:3-7 (describing addition of layers to provide an unoxidized bonding surface). In this context, a POSITA would have appreciated and found obvious that additional layers of materials also would have been obvious to implement in Nakatani’s surface wiring.

184. For example, as described above (*supra* §XI.A), Glick describes preparing a conductive pattern from multiple layers of materials, including layers of nickel and gold. APPLE-1020, 2:56-3:11. A POSITA would have understood from Nakatani’s disclosure that coated layers on a wiring pattern may be beneficial and would have looked to Glick for details about how to apply coatings to the conductive elements as described by Nakatani. APPLE-1007, [0078]; APPLE-1008, [0012], [0046]-[0048]; APPLE-1020, 2:56-3:11. In particular, Glick describes “a conductor layer ...consist[ing] of titanium and palladium sequentially evaporated on the substrate and then copper, ***nickel and gold*** sequentially plated on the palladium.” *Id.*, 3:7-11; *supra*, §XI.A. Multiple reasons would have motivated

a POSITA to implement Nakatani-Onda's conductive surface wiring and lands in accordance with Glick's suggestion to include layers of **both** nickel and gold on the wiring for the reasons described above with regard to the Nishiuma-Shibata-Glick combination, including to decrease manufacturing and materials costs. *See supra* §XI.B (Reasons for combining Glick with Nishiuma-Shibata to include layers of nickel and gold are equally applicable here to Nakatani-Onda).

185. Additionally, implementing additional conductive material layers in a wiring pattern in the combination would have been obvious as a predictable application of a known technique of implementing multiple conductive layers as taught by Glick to a known system as taught by Nakatani and Onda to achieve entirely predictable results. A POSITA would have understood that implementing Nakatani-Onda's conductive wiring patterns with multiple layers would have been as simple as plating additional layers on these features. A POSITA would have further understood that the use of materials like both Nakatani, Onda and Glick discuss, for example, gold, copper, nickel, would have had predictable results of providing a conductive surface wiring with known benefits like improving conductivity, decreasing oxidation, decreasing cost by using a smaller amount of expensive materials like gold, and other similarly well-known advantages. *See e.g.*, APPLE-1020, 2:56-3:11.

186. Further, a POSITA would have had a reasonable expectation of success in implementing Nakatani-Onda's device with Glick's suggestion to provide multiple layers of coatings to the conductive wiring because of similarities between the teachings of Nakatani and Glick including that the layered conductor structure taught by Glick is complimentary to the layers described by Nakatani. APPLE-1007, [0016]-[0020], [0078]; APPLE-1008, [0012], [0046]-[0048]; APPLE-1020, 2:56-3:11, Figs. 1-2. A POSITA would have recognized that Nakatani's copper foil plated with nickel or gold could be expanded to include layers of both nickel and gold as taught by Glick while maintaining a gold bonding surface for connection with the tower bumps. APPLE-1007, [0078]; APPLE-1008, [0012], [0046]-[0048]; APPLE-1020, 2:56-3:11 (describing that "gold is needed to provide a good unoxidized bonding surface" in a layered structure including copper and nickel beneath a gold top layer).

**D. Claim-by-Claim Analysis**

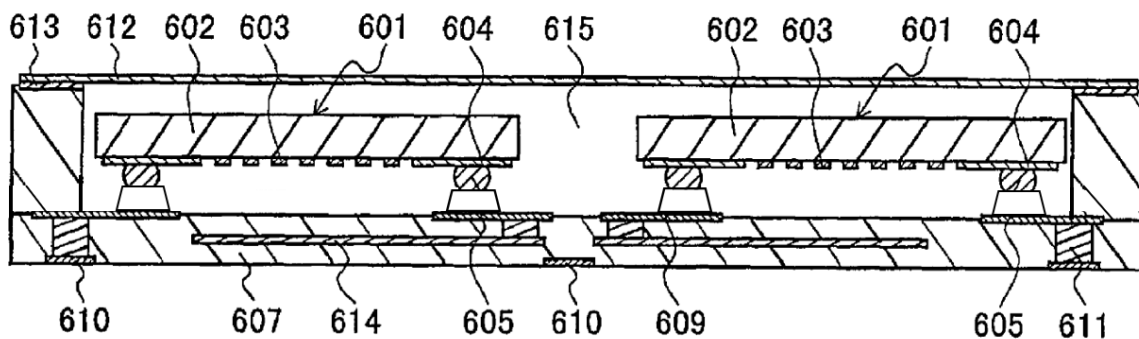
**i. Claim 1**

***[1.pre] An electronic module, comprising:***

187. To the extent the preamble is limiting, Nakatani-Onda-Glick renders [1.pre] obvious. Nakatani describes "a module containing electric elements such as semiconductor chips or surface acoustic wave devices." APPLE-1007, [0001]; *cf.* APPLE-1001, 1:24-31 ('207 patent describing that an electronic module "can be

a module like a circuit board, which includes several components [such as semiconductor components”). For example, Nakatani’s FIG. 7 depicts “a conventional surface acoustic wave device built-in module.” APPLE-1004, [0016].

Surface acoustic wave  
device built-in module  
(electronic module)



**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

188. As described above, Nakatani’s FIG. 7 is an example of an electronic module well-known in the prior art before the Critical Date. APPLE-1006, [0016]; *see supra* §IV.A.

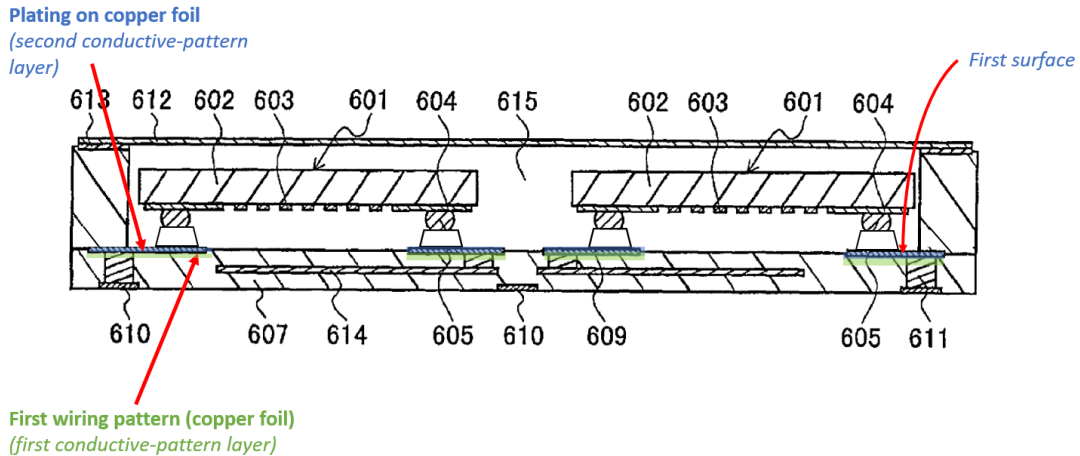
***[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;***

189. The Nakatani-Onda-Glick combination discloses and renders obvious elements [1a]-[1b.ii]. For example, Nakatani describes a surface wave acoustic device module having a circuit board 607 with first wiring patterns 609. APPLE-1007, [0017]; *supra* §XIII.A. “A copper foil can be used as the wiring pattern 201, and a copper foil plated with nickel or gold further is preferable because of its stable electrical connection with the metal bumps 202 on the semiconductor chip 203.” APPLE-1007, [0078]. Accordingly, Nakatani describes that the first wiring pattern formed from copper foil provides a first conductive-pattern layer, and that the copper foil can be coated in nickel or gold, providing a second conductive-pattern layer disposed on the first conductive-pattern layer.

190. To the extent Nakatani does not expressly disclose that the copper foil can be plated with additional layers of materials, Glick teaches this conventional option. APPLE-1007, [0078]; APPLE-1020, 2:56-3:7, 3:7-11 (“a conductor layer which includes copper would consist of titanium and palladium sequentially evaporated on the substrate and then copper, nickel, and gold sequentially plated on the palladium.”), 1:63-66; *see also* APPLE-1004, 7:14-16 (describing that surface wiring is plated in nickel *and* gold). As described above, it would have

been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's copper foil with two or more plated layers (e.g., at least nickel and gold layers) on a top surface of the copper foil, as suggested by Glick. *Supra* §XIII.C.ii (Nakatani-Onda-Glick Combination).

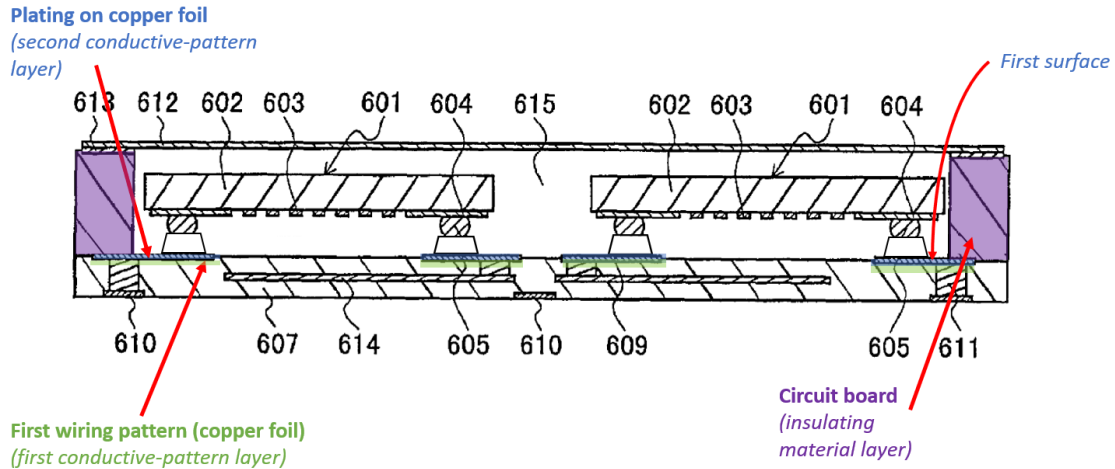
191. The copper foil forming the first wiring pattern 609 provides the claimed “**first conductive-pattern layer**” while the additional layers, as suggested by Glick, plated on the copper foil provide the claimed “**second conductive-pattern layer**” disposed on the first conductive-pattern layer. APPLE-1007, [0078], [0017]-[0020]; *cf.* APPLE-1001, 6:28-31 ('207 patent describing “surfaced” conductive layers for wiring similar to Nakatani's), 6:52-59 ('207 patent also describing layers comprised of multiple components); APPLE-1002, 170-173. The top of the plated layer provides the claimed “**first surface**” of the second conductive-pattern layer. APPLE-1007, [0078], [0016]-[0020]; APPLE-1020, 2:56-3:11, Figs. 1-2.



**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

***[1c] an insulating-material layer disposed on the first surface of the second conductive-pattern layer;***

192. Nakatani-Onda-Glick renders obvious element [1c]. For example, Nakatani describes that “[i]n order to ensure a space in which the surface acoustic wave devices 601 are mounted, the circuit board 607 has the concave portion 615 in its central portion.” APPLE-1007, [0019]. As shown in FIG. 1, Nakatani describes a layer of the circuit board 607 disposed on the first surface of the first wiring pattern coating (second conductive-pattern layer). The layer of the circuit board defines or provides a space (e.g., concave portion 615) so that the device or devices 601 can be inserted into the board.

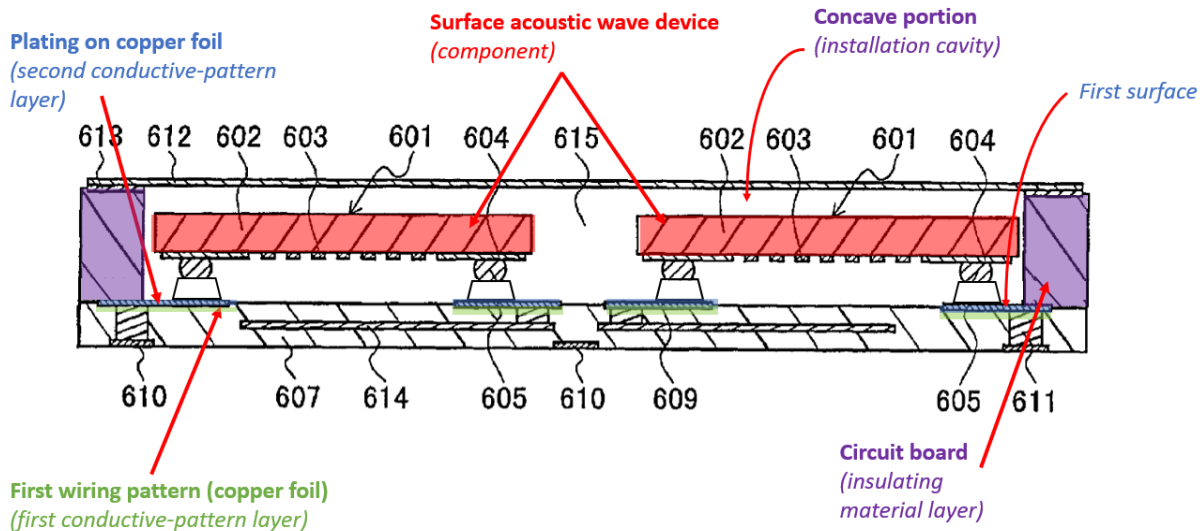


**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

193. Although Nakatani does not describe the material of the layer that forms the concave portion of the circuit board 607, a POSITA would have understood that the material is an insulating material layer, because a POSITA would have been aware that circuit boards generally include layers of insulating material alternating with layers of conductive patterns. For example, a POSITA would have understood that “[p]rinted circuit boards have been in use for decades to provide electrical circuitry [and] generally include a thin substrate made from a suitable electrically insulating material such as a ceramic or an epoxy-glass composite [with t]hin electrical leads [ ]on one or both surfaces.” APPLE-1010, 1:9-17; *see also* APPLE-1012, 212-221 (describing circuit boards and stacked circuit boards); APPLE-1011, [0007]-[0009] (describing mounting semiconductor chips in insulating receptacles); *see generally* §IV.A.

**[1d]-[1e.i] at least one installation cavity disposed in the insulating-material layer; a component disposed within the at least one installation cavity,**

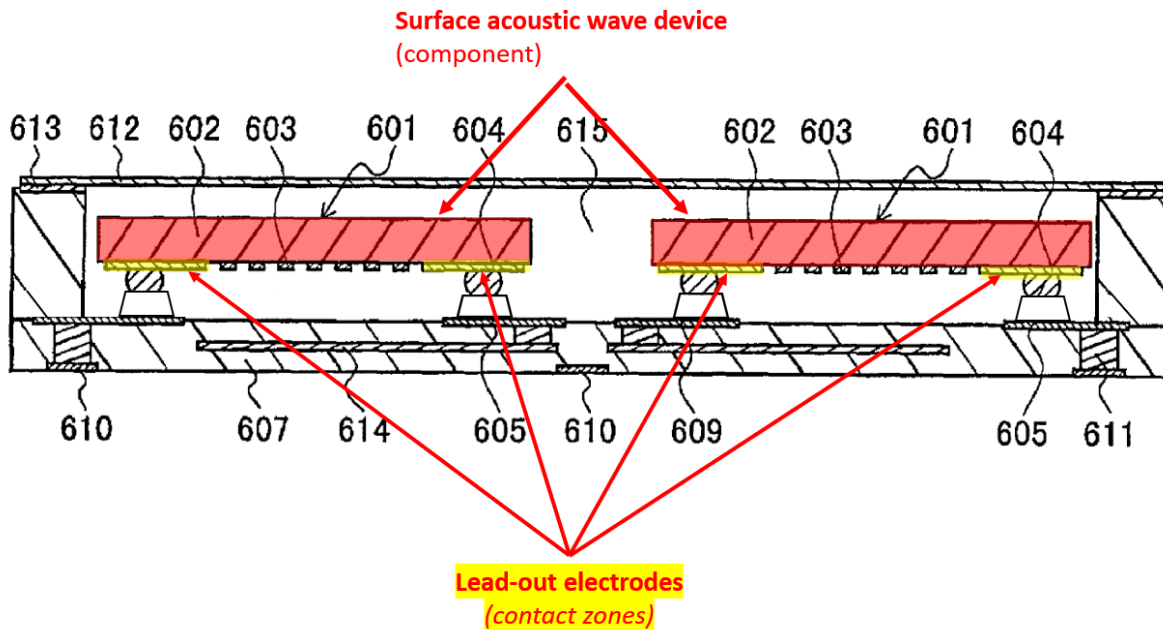
194. Nakatani-Onda-Glick renders obvious elements [1d]-[1e.i]. For example, Nakatani describes that “[i]n order to ensure a space in which the surface acoustic wave devices 601 are mounted, the circuit board 607 has the concave portion 615 in its central portion.” APPLE-1007, [0019]. As shown in FIG. 7, the circuit board includes a concave portion (**installation cavity**) in which the surface acoustic wave devices (**components**) are positioned. *Id.*, [0019], [0021].



**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

***[1e.ii] the component comprising contact zones comprising aluminum;***

195. Nakatani-Onda-Glick renders obvious element [1e.ii]. For example, as shown in FIG. 7, Nakatani describes that the surface acoustic wave device 601 (***component***) includes lead-out electrodes 604. APPLE-1007, [0018] (“In the surface acoustic wave device 601...the lead-out electrodes 604 formed of a metal film containing aluminum as a main component are formed”), FIG. 7; *see also id.*, [0044]-[0046], [0073], [0086], [0118]-[0119]. Nakatani’s lead-out electrodes provide “***contact zones***” on the component. *Id.*, [0018] (“The metal bumps 605 for an electrical connection with an external circuit are formed on the lead-out electrodes 604”), [0020], [0133]. A POSITA would have understood Nakatani’s lead-out electrodes to be contact zones, because Nakatani describes that the lead-out electrodes provide the connection to (and contact with) the metal bumps. *Id.*, [0018].



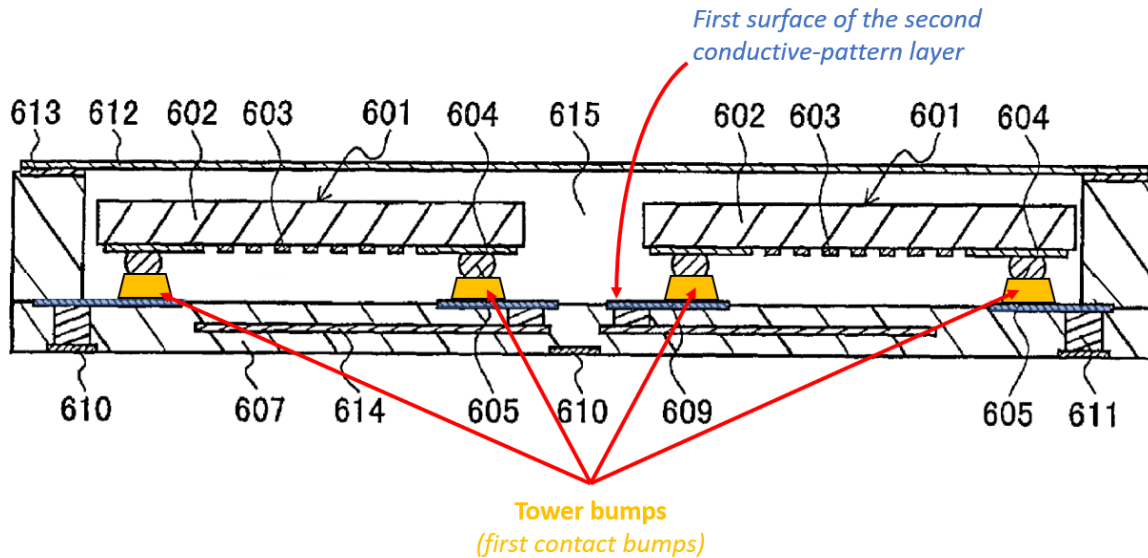
**APPLE-1007, FIG. 7 (annotated and modified to include tower bumps as taught by Onda)**

196. Further, Nakatani describes that “the lead-out electrodes 604 [are] formed of a metal film containing aluminum as a main component.” APPLE-1007, [0018], [0119]. As described above, aluminum electrode pads were well-known by the Critical Date and a POSITA would have appreciated that it was common before the Critical Date to form electrode pads from aluminum, just as Nakatani instructs. *Supra* §X.C. Accordingly, Nakatani-Onda-Glick renders obvious the component comprising contact zones comprising aluminum, as claimed.

***[1f] first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and***

197. Nakatani-Onda-Glick renders obvious element [1f]. For example, Nakatani describes “the first wiring patterns 609 and the metal bumps 605 are electrically connected.” APPLE-1007, [0020]. To the extent Nakatani does not expressly disclose electrically connecting the device to the wiring patterns via the metal bumps and contact bumps formed on the circuit board wiring patterns, Onda teaches this conventional solution for bonding a component to a circuit board. APPLE-1008, [0039], [0045], FIGS. 5-10; *supra* §XIII.B.

198. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani’s device bonded to the circuit board wiring pattern using two conductive bumps, including a tower bump (***first contact bumps***) formed on the top surface of the plated surface wiring of the circuit board (***first surface of the second conductive pattern layer***) as suggested by Onda. *Supra* §XIII.C.i (Nakatani-Onda Combination).



**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

199. As described above, Nakatani teaches that the device is electrically connected to the wiring patterns 609 through the metal bumps 605. APPLE-1007, [0018]-[0020], [0086], [0122]. Further, Onda describes that the pairs of tower bumps and metal bumps of various materials provide an electrical connection between a semiconductor device and a wiring substrate. See APPLE-1008, [0099] (“an example of electrical connection between a semiconductor device and a wiring substrate using gold-gold bonding will be described”), [0014], [0057], [0101]-[0106].

200. A POSITA would have understood that the tower bumps described by Onda are **electrically connected** to the copper foil forming Nakatani’s wiring patterns to couple the device to the wiring of the printed circuit board. APPPLE-

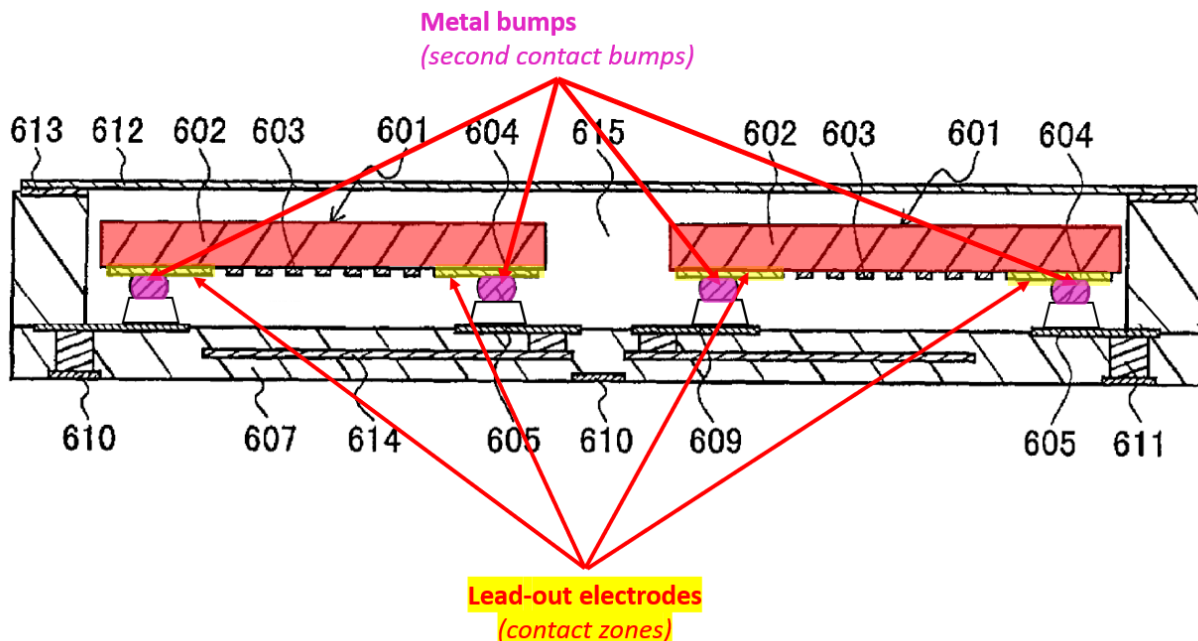
1008, [0039] (“tower bumps 4 are provided in the wiring layer of the substrate including inner leads 3 to connect with the semiconductor chip”). Both Nakatani and Onda make clear that the purpose of metallic bumps between the device and circuit board is an electrical connection, and a POSITA would have understood this as obvious and conventional use of metal bumps. APPLE-1007, [0018]-[0020], [0086], [0122]; APPLE-1008, [0039]; *supra* §IV.A. Accordingly, a POSITA would have understood that the tower bumps (***first contact bumps***) are electrically connected to the plated top surface of the first wiring pattern (***first surface of the second conductive pattern layer***).

***[1g] second contact bumps disposed on the contact zones and electrically connected thereto,***

201. Nakatani-Onda-Glick renders obvious element [1g]. Nakatani describes that “metal bumps 605 for an electrical connection with an external circuit are formed on the lead-out electrodes 604.” APPLE-1007, [0018], [0017], [0020], [0133], FIG. 7. Onda teaches that use of two conductive bumps to electrically connect a semiconductor device to wiring board is a conventional solution for bonding a component to a circuit board. APPLE-1008, [0039], [0045], [0094], [0101]-[0102], FIGS. 5-10; *see supra* §XIII.B.

202. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani’s device bonded

to the circuit board wiring pattern using two conductive bumps, including a metal bump (***second contact bumps***) formed on the electrode pads (***contact zones***) of the device as suggested by Onda. *Supra* §XIII.C.i (Nakatani-Onda Combination).



**APPLE-1007, FIG. 7 (annotated, modified to include tower bumps as taught by Onda)**

203. As described above, Nakatani teaches that the device is electrically connected to the wiring patterns 609 through the metal bumps 605. APPLE-1007, [0018]-[0020], [0086], [0122]. Further, Onda describes that the pairs of tower bumps and metal bumps of various materials for coupling a semiconductor device to a wiring substrate provide an electrical connection. See APPLE-1008, [0101]-[0102] (“gold plating (gold bumps) 71 are formed on each electrode pad

2...[w]hen mounting the semiconductor chip 1 on the wiring substrate 20... the semiconductor chip 1 is placed on the tower bumps formed in the connection portions (tips) of the inner leads 3 on the wiring substrate 20, a connection is established by a gold-gold diffusion reaction with the electrode pads 2”), [0099], [0014], [0057], [0103]-[0106]. A POSITA would have understood that the metal (e.g., gold) bumps described by Onda are **electrically connected** to the electrode pads of Nakatani’s surface acoustic wave device. APPPLE-1008, [0101]-[0102], [0039]. Both Nakatani and Onda make clear that the purpose of metallic bumps between the device and circuit board is an electrical connection, and a POSITA would have understood this as obvious and conventional use of metal bumps. APPLE-1007, [0018]-[0020], [0086], [0122]; APPLE-1008, [0039]; *supra* §IV.A.

204. Accordingly, a POSITA would have understood that the metal bumps (***second contact bumps***) are electrically connected to the electrode pads (***contact zones***).

***[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.***

205. Nakatani-Onda-Glick renders obvious element [1h]. *Supra* XIII.D.i Ground 2A Elements [1a]-[1b.ii].

206. As described above, Nakatani's copper foil forming the first wiring pattern 609 provides the claimed "***first conductive-pattern layer***" while the additional layer or layers, as suggested by Glick, plated on the copper foil provide the claimed "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. *Supra* §XIII.D.i Ground 2A Elements [1a]-[1b.ii]; APPLE-1007, [0078], [0017]-[0020]. The second conductive-pattern layer in this example includes layers of nickel and gold and thus comprises two layers of at least two different materials: (1) a layer of nickel on the copper plating, (2) and a layer of gold. APPLE-1020, 2:56-3:20, 1:63-66. Accordingly, at least one of the first and second conductive-pattern layers (i.e., the second conductive-pattern layer) includes two layers of different materials, satisfying this claim limitation as a POSITA would have understood it. *Supra* §VIII.A.

207. Additionally, although Nakatani describes that the "[a] copper foil can be used as the wiring pattern 201," Nakatani does not limit the wiring pattern to copper materials. APPLE-1007, [0078], [0098] ("Although the above embodiment illustrated the case of using copper as a material for the wiring pattern 201, the present invention is not limited to the above, so metal such as aluminum or nickel may also be used to produce a similar effect"), [0078], [0083], [0091]. A POSITA would have been aware of other conventional materials for forming conductive

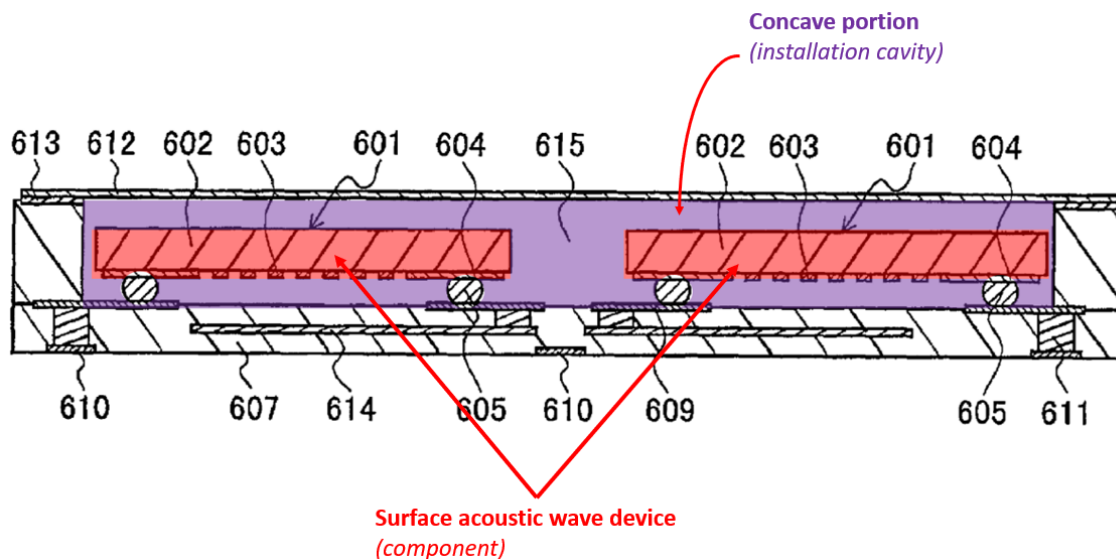
wiring patterns on a circuit board and would have looked to a references like Glick that describe examples of materials used to form conductive patterns.

208. For example, Glick describes that “[a] layer of titanium 12 is first deposited on the substrate 10... [n]ext a layer of palladium 14 is deposited on the titanium... [and f]inally, a layer of gold 16 is plated over the palladium.” APPLE-1020, 2:56-66; 1:63-66. A POSITA would have been motivated to substitute Glick’s suggested titanium and palladium for Nakatani’s copper foil to improve adherence of the wiring pattern to the circuit board. APPLE-1020, 2:56-60 (“A layer of titanium 12 is first deposited on the substrate 10... to increase the adherence of any layer deposited subsequently”); *see also* APPLE-1007, [0091] (describing methods for improving adhesion and preventing oxidation of foil and plating layers). With the use of titanium and palladium layers to form a wiring pattern, the first conductive-pattern layer in this example also comprises two layers of at least two different materials: (1) titanium and (2) palladium. APPLE-1020, 2:56-3:7. In this example, an additional layer of copper may be added between the palladium and nickel as taught by Glick (APPLE-1020, 2:64-3:11), though this does not impact the analysis as to whether the “two layers” are met to satisfy this claim limitation under a narrower read requiring that both first and second conductive-pattern layers include “two layers.” *See supra* §VIII.A.

ii. Claim 2

**[2] The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.**

209. Nakatani-Onda-Glick renders obvious claim [2]. For example, FIG. 7 shows that the concave portion (installation cavity) may be thicker than the component. APPLE-1007, FIG. 7.



**APPLE-1007, FIG. 7 (annotated)**

210. As described above, in the context of the '207 patent, component thickness refers to or encompasses the height of the component *after installation in the cavity*. Indeed, the patent specifically relates the thickness of the component to the component's protrusion beyond the height or thickness of the installation cavity. See, e.g., APPLE-1001, 7:61-8:5. This understanding comports with the specification's discussion of component thicknesses that are less than, equal to, or

greater than the thickness of the installation base or cavity, especially as there would be no reason to distinguish between components of equal or greater absolute/pre-installation thickness when both would protrude from the cavity after installation due to the contact bump / electrode thickness. APPLE-1001, 6:8-17.

211. In this context, Nakatani's FIG. 7 makes clear that the walls that form the concave portion have a larger height than the component, such that the installation cavity is thicker than the component as claimed. Further, a POSITA would have understood that by forming an installation cavity with greater thickness than the component to be installed, the component would not protrude beyond the height of the insulating-layer and could be sealed within the cavity by the positioning of a cover 612, just as Nakatani teaches. APPLE-1007, [0017], [0021], FIG. 7.

**iii. Claim 5**

***[5] The electronic module of claim 1, wherein the first contact bumps comprise tin.***

212. Nakatani-Onda-Glick renders obvious claim [5]. As described above, it would have been obvious and a POSITA would have been motivated for a number of reasons to implement Nakatani's device using two conductive bumps to couple the surface acoustic wave device to the wiring pattern of the circuit board, using materials suggested by Onda. *Supra*, §XIII.C.i.

213. For example, Onda describes that “[t]he tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1 [for example g]old, solder, or tin can be used... in the bonding layer 42.” APPLE-1008, [0045]; [0073] (“The wiring layer of the substrate including inner leads 3 is provided with tower bumps 4 consisting of copper bumps (metal bumps 41) that have been tin plated 72 (bonding layer 42)”), [0074] (“When mounting the semiconductor chip 1 on the wiring substrate 20... the semiconductor chip 1 is placed on the tower bumps 4 formed in the connection portions (tips) of the inner leads 3 on the wiring substrate 20, a connection is established by a gold-tin diffusion reaction with the electrode pads 2”), , FIG. 6A.

214. The selection of tin for use with the tower bumps taught by Onda would have been an obvious design choice for a POSITA to achieve desired electrical, thermal, mechanical, and bonding characteristics for the design. Accordingly, it would have been obvious to a POSITA to implement the Nakatani-Onda-Glick combination with tower bumps (“**first contact bumps**”) including tin, as Onda suggests, to increase the strength of the connection between Nakatani’s first wiring pattern and the device via the bumps by making the connection through gold-tin diffusion. APPLE-1008, [0073]-[0077]. A POSITA would have understood that design considerations in the selection of materials for a surface acoustic wave device built-in module balance various characteristics of the

materials such as electrical conductivity, thermal conductivity, bonding strength and characteristics, ease of use, and cost, and would have recognized that the use of tin in the formation of the tower bumps would have provided a suitable material for providing electrical connection between the surface wiring and semiconductor device. A POSITA would have had a reasonable expectation of success in implementing the combination with the teachings of Onda for all the reasons described above. *Supra* §XIII.C.i.

**iv. Claim 6**

***[6] The electronic module of claim 1, wherein the second contact bumps comprise copper.***

215. Nakatani-Onda-Glick renders obvious claim [6]. As described above, it would have been obvious and a POSITA would have been motivated for a number of reasons to implement Nakatani's device using two conductive bumps to couple the surface acoustic wave device to the wiring pattern of the circuit board, using materials suggested by Onda. *Supra*, §XIII.C.i. For example, Nakatani describes that the metal bumps may be gold bumps that are melted to form the electrical connection to the wiring, or the connection can be made "using an electrically conductive adhesive." APPLE-1007, [0020].

216. Nakatani does not describe the electrically conductive adhesive to be used, however, Onda describes that the pairs of bumps may be bonded with a

bonding layer 42 of a material selected based on the chosen connection method.

APPLE-1008, [0136], [0063], [0042]-[0043]. For example, Onda describes that copper bumps that are metal-plated can be coupled to gold bumps. *Id.*, [0073] (“tower bumps 4 consisting of copper bumps (metal bumps 41) that have been tin plated 72 (bonding layer 42)”), [0074] (“the semiconductor chip 1 is placed on the tower bumps 4... [and] a connection is established by a gold-tin diffusion reaction with the electrode pads 2”), [0075] (“The bonding layer of the gold-tin connection consists of a reactive melted layer of gold and tin at the bonding interface (high melting point layer) and a portion protruding from this (fillet)...”), [0076] (“This gold-tin connection at the first eutectic point, which forms a bonding interface of 10 to 40wt% gold and 60 to 90 wt% tin as mentioned above, increases the strength of the connection at low temperatures”), [0077] (“a gold-tin connection at the first eutectic point is ideal because the bond strength is also high”), [0079] (“This gold-tin connection method is also a low-temperature connection method that can establish connections without adversely affecting the wiring substrate”), [0082], [0083] (“because the connection is established using the first eutectic point of gold-tin, the connection strength is increased and a more reliable connection can be made”), FIG. 6A.

217. A POSITA would have found it to be an obvious design choice to use copper with the metal bumps to achieve desired electrical, thermal, mechanical,

and bonding characteristic for a given design. Accordingly, it would have been obvious to a POSITA to implement the Nakatani-Onda-Glick combination with metal bumps (“***second contact bumps***”) formed from material combinations suggested by Onda, such as copper, to enhance connection between the metal bumps and tower bumps. APPLE-1008, [0073]-[0083]. A POSITA would have understood that design considerations in the selection of materials for a surface acoustic wave device built-in module balance various characteristics of the materials such as electrical conductivity, thermal conductivity, bonding strength and characteristics, ease of use, and cost, and would have recognized that the use of tin in the formation of the metal bumps would have provided a suitable material for providing electrical connection between the surface wiring and semiconductor device. A POSITA would have had a reasonable expectation of success in implementing the metal bumps using copper, given that Onda suggests copper bumps in combination with bumps that are formed from gold (just as Nakatani describes) and plated with tin. APPLE-1008, [0042]-[0043], [0163]; APPLE-1007, [0018], [0017], FIG. 7.

**XIV. GROUND 2B: CLAIMS 3-4 ARE OBVIOUS UNDER 35 U.S.C. § 103  
BASED ON NAKATANI IN VIEW OF ONDA, GLICK, AND  
PARKER**

**A. The Nakatani-Onda-Glick-Parker Combination**

218. Nakatani describes that a circuit board includes a concave portion “to ensure a space in which the surface acoustic wave devices 601 are mounted.” APPLE-1007, [0019]. A POSITA would have understood that a cavity formed in the circuit board is sized to fit the device intended to be mounted within the cavity, and would have further understood that there are a variety of ways to size the cavity to the device. *See e.g.*, APPLE-1011, [0034] (“the cross-sectional dimensions of cavity portion 12... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12”), [0017] (“[t]he height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier.”), [0038], [0044], FIG. 4; *see also supra* §IV.A. In this context, a POSITA would have turned to references like Parker that describe sizing considerations for a cavity.

219. For example, Parker describes that “[c]avities 18 are [] provided in one or both of the parallel surfaces of the substrate 12” of the printed circuit board. APPLE-1010, 2:64-65, FIG. 2. “Electrical components are adapted to be disposed

in the cavities 18, preferably in a tight fit with the walls of the cavities.” *Id.*, 2:66-3:1. Like Nakatani, Parker describes mounting a device within a cavity of a circuit board and additionally provides guidance as to the sizing of the cavity relative to the component to be mounted therein, including sizing the cavity to the dimensions of the component. A POSITA would have recognized that a cavity would need to be at least large enough to partially accept a component to be installed therein (*see e.g.*, APPLE-1007 describing a concave portion formed “to ensure a space in which the surface acoustic wave devices 601 are mounted”), and further that there are design benefits to sizing the cavity to be larger or smaller relative to the component size and depending on the design objectives of the device. Multiple reasons would have motivated a POSITA to implement Nakatani’s cavity to be sized to the dimensions of the component in accordance with Parker’s suggestion as described below. APPLE-1010, 1:49-51, 2:64-3:1, FIG. 2.

220. First, a POSITA would have understood that sizing the cavity to have a tight fit with the component optimizes the use of limited space on the printed circuit board. For example, a POSITA would have understood that higher density packages were desirable by the Critical Date and that optimizing use of available space on the circuit board allows for such optimization. See APPLE-1007, [0002] (“In recent years, with the demand for higher performance and miniaturization of electronic equipment, higher density and higher function for packages in which

semiconductor chips are mounted have been desired increasingly”); APPLE-1011, [0034] (“the cross-sectional dimensions of [the] cavity portion ... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12.”); APPLE-1036, 1 (“Footprint reduction of the integrated device is an additional need, especially for portable device applications”)see also *supra* §IV.A.

221. Second, to the extent that components are connected to the printed circuit board by wires in addition to contact bumps, positioning a component in a cavity with a tight fit requires shorter wire bond lengths and reduces parasitic effects. APPLE-1010, [0017] (“The cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), FIG. 8.

222. Third, a POSITA would have understood that a tight fit between the cavity and the component allows for the component to be easily placed in a proper position within the cavity to provide electrical connection between the component and wiring in the cavity. APPLE-1011, [0006] (contrasting with the use of ball grid arrays). For example, Parker describes that transistors may have “a considerabl[e] number of closely spaced electrical terminals such as the pads 26” which must be electrically connected to the circuit board. APPLE-1010, 3:65-4:2. A POSITA would have understood that closely fitted side walls may guide the

positioning of the device within the cavity so that electrical connections to the circuit board are aligned during placement of the component. *See* APPLE-1037, 2 (“the embedded interconnections in the MCM structure provide good protection both mechanically and chemically”)

223. Fourth, a POSITA would have appreciated that there are a limited number of possible size relationships between a cavity and a component sized to fit in the cavity – the component can be shorter, taller, or the same height as the cavity and the cavity can be the same width/length as the component or larger. APPLE-1001, 6:7-16 (describing that the installation base can be thicker than, less thick than, or equally thick as the component). It would have been obvious to a POSITA that a cavity intended to receive a component must have dimensions at least sized to allow the component to be placed therein, and can additionally have a height that is shorter than, equal to, or thicker than the height of the component.

224. A POSITA would have found it obvious to try these finite and predictable solutions to sizing the cavity relative to the component and would have had a reasonable expectation of success in implementing them, given that these are conventional methods for mounting a component within a cavity. *See e.g.*, APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”); 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel

surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”); APPLE-1011, [0034] (“the height, h, of cavity portion 12 is also selected based on the height of the semiconductor chip and the location of the wire bonding pads on the chip”), [0017] (“The height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier... [t]he cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), [0034], [0038], [0044], FIG. 4.

225. A POSITA would have had a reasonable expectation of success implementing the combination for all the reasons described above and given that Parker describes techniques for disposing components in cavities of a circuit board, like Nakatani. APPLE-1007, [0016]-[0021]; APPLE-1010, 1:49-51, 2:5-27, 2:64-3:22. Implementing a surface acoustic wave device module with a component positioned in a cavity that has a tight fit to the component would have been obvious as a predictable application of a known technique for positioning components in a printed circuit board as taught by Parker to a known system as taught by Nakatani to achieve entirely predictable results. As described above, a POSITA would have understood that it was conventional to place a component

within a cavity of a printed circuit board, and that by providing a tight fit between the component and cavity the space on the circuit board could be optimized. *Supra* §IV.A; APPLE-1010, 1:49-51, 2:64-3:9, 3:27-42. A POSITA would have understood that implementing Nakatani-Onda-Glick to have a cavity that was a tight fit to the component would have been a straightforward choice during manufacture of the printed circuit board, just as Parker teaches. APPLE-1010, Abstract, 1:49-51, 1:57-66, 2:10-13, FIGS. 1-4.

**B. Claim-by-Claim Analysis**

**v. Claim 3**

***[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.***

226. Nakatani-Onda-Glick-Parker renders obvious claim [3]. For example, Nakatani describes that a concave portion in a circuit board provides “a space in which the surface acoustic wave devices 601 are mounted.” APPLE-1007, [0019]. To the extent Nakatani does not expressly disclose that the installation cavity has about equal thickness as the component, Parker teaches this conventional option. APPLE-1010, 1:49-51 (“[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities”), 2:64-3:11 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the

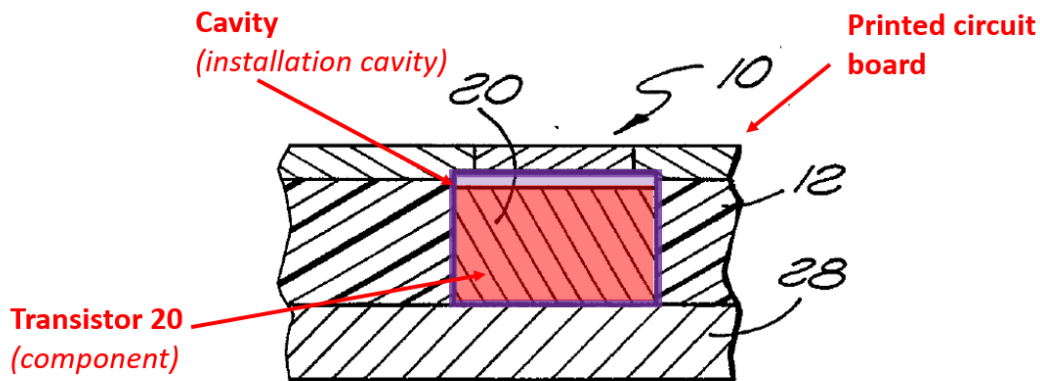
cavities 18, preferably in a tight fit with the walls of the cavities.”); 3:18-22;

APPLE-1004, FIGS. 1, 9, 10.

227. As described above, in the context of the ’207 patent, component thickness refers to or encompasses the height of the component *after installation in the cavity*. *Supra* §X.D.[3] (Ground 1A discussion of claim meaning in Claim [3]). Indeed, the patent specifically relates the thickness of the component to the component’s protrusion beyond the height or thickness of the installation cavity. *See, e.g.*, APPLE-1001, 7:61-8:5. This understanding comports with the specification’s discussion of component thicknesses that are less than, equal to, or greater than the thickness of the installation base or cavity, especially as there would be no reason to distinguish between components of equal or greater absolute/pre-installation thickness when both would protrude from the cavity after installation due to the contact bump / electrode thickness. APPLE-1001, 6:8-17.

228. As shown in FIG. 2 below, Parker teaches that the **cavity** formed in the printed circuit board (purple box) **has about equal thickness** as the transistor 20 (“**component**”). APPLE-1010, FIG. 2. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani’s cavity and device with the sizing relationship suggested by Parker so that the installation cavity has about equal thickness as the component as claimed. *Supra* §XIV.A (Nakatani-Onda-Glick-Parker Combination); *see also*

APPLE-1011, [0034] (“the height, h, of cavity portion 12 is also selected based on the height of the semiconductor chip and the location of the wire bonding pads on the chip”), [0017] (“The height of the cavity portion is selected to keep the length of the wire bonds short, i.e., so that the conductive bonding pads of the semiconductor chip are at approximately the same height as the flange portion of the chip carrier... [t]he cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”), [0038], [0044], FIG. 4.



APPLE-1010, FIG. 2 (annotated)

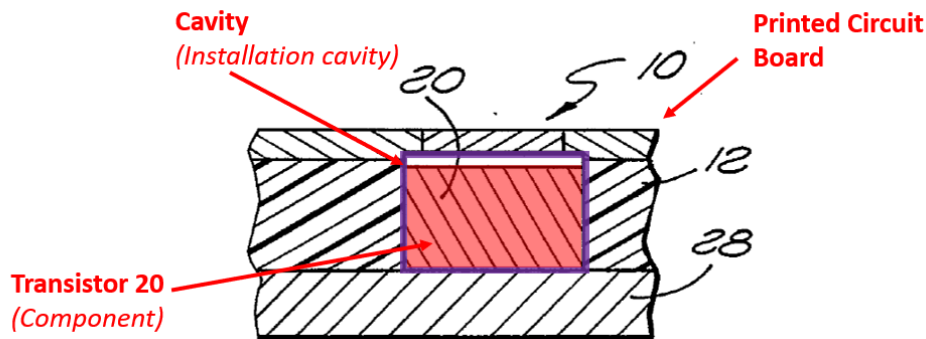
vi. Claim 4

***[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.***

229. Nakatani-Onda-Glick-Parker renders obvious claim [4]. For example, Parker describes “[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities.”

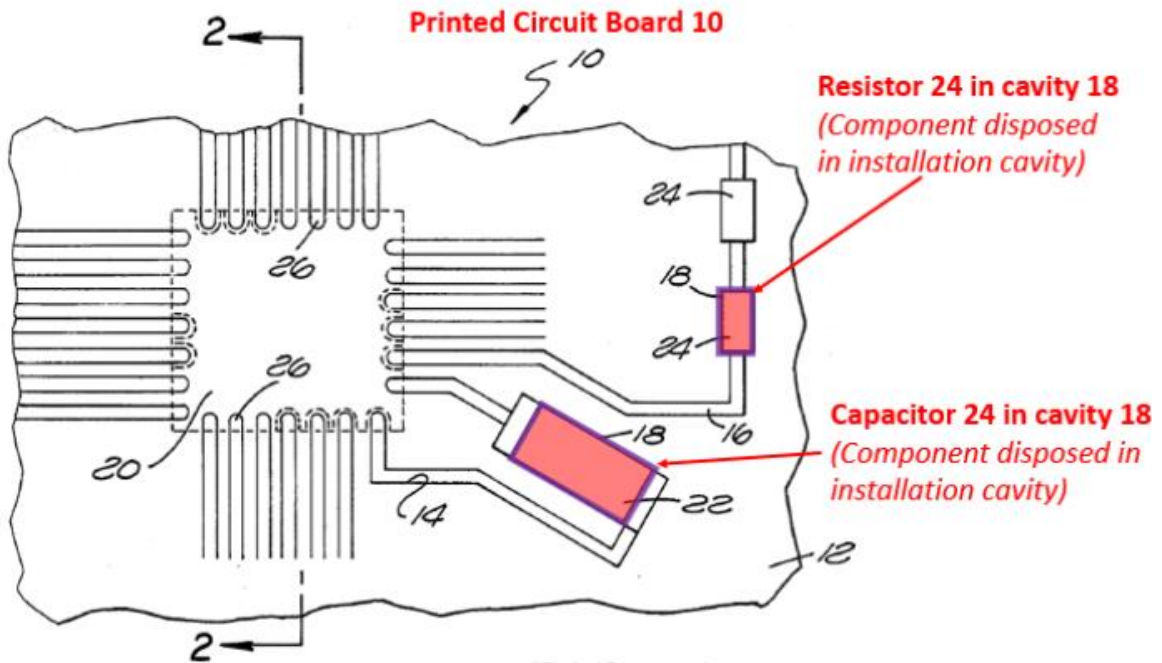
APPLE-1010, 1:49-51, 2:64-3:9. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's cavity and device with the sizing relationship suggested by Parker. *Supra* §XIV.A (Nakatani-Onda-Glick-Parker Combination).

230. As shown in FIG. 2, the **cavity** formed in the printed circuit board (purple box) has a thickness and width (i.e., "dimensions") about equal to the size of the transistor 20, and thus is "***dimensioned to the size of the component.***" *Id.*, 3:18-22.



**APPLE-1010, FIG. 2 (annotated)**

231. Additionally, FIG. 1 shows that the **cavities** formed in the printed circuit board are ***dimensioned to the size of the components*** positioned within the cavities. APPLE-1010, 2:64-3:7, 3:44-53, FIG. 1.



**APPLE-1010, FIG. 1 (annotated)**

232. A POSITA would have understood that sizing the cavity to the component to be fit into the cavity had numerous benefits, including requiring shorter wire bond lengths to minimize parasitic effects and to provide a tighter fit of the component in the cavity. APPLE-1011, [0017] (“The cavity portion is also preferably sized to tightly fit the chip, to further minimize the length of the wire bonds [so that] parasitic effects are minimized.”). A POSITA would have understood that the thickness of the cavity and component is only one dimension, and that “the cross-sectional dimensions of [the] cavity portion ... are preferably customized or selected to provide a relatively tight fit with a desired semiconductor device when the latter is inserted into cavity portion 12.” APPLE-1011, [0034]; see

also APPLE-1010, 1:49-51 (“Cavities are also provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship to the cavities.”), 2:64-3:1 (“Cavities 18 are also provided in one or both of the parallel surfaces of the substrate 12... [e]lectrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities.”). As described above, there are multiple reasons for selecting various relationships in size of the cavity and the component to be positioned therein. For example, in some cases, a larger cavity may be beneficial to provide a component with sufficient air insulation surrounding the component to cool the component. In other cases, a tighter fit between the cavity and component provide a space-saving benefit by allowing for space on the printed circuit board to be maximized. APPLE-1010, 1:49-51, 2:64-3:9, 3:27-42; APPLE-1007, [0002] (“In recent years, with the demand for higher performance and miniaturization of electronic equipment, higher density and higher function for packages in which semiconductor chips are mounted have been desired increasingly”).

## **XV. ADDITIONAL REMARKS**

233. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

## XVI. LISTING OF CLAIMS

| Claim 1 |                                                                                                                                                                       |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1pre]  | An electronic module, comprising:                                                                                                                                     |
| [1a]    | a first conductive-pattern layer and                                                                                                                                  |
| [1b.i]  | a second conductive-pattern layer disposed on the first conductive-pattern layer,                                                                                     |
| [1b.ii] | the second conductive-pattern layer having a first surface;                                                                                                           |
| [1c]    | an insulating-material layer disposed on the first surface of the second conductive-pattern layer;                                                                    |
| [1d]    | at least one installation cavity disposed in the insulating-material layer;                                                                                           |
| [1e.i]  | a component disposed within the at least one installation cavity,                                                                                                     |
| [1e.ii] | the component comprising contact zones comprising aluminum;                                                                                                           |
| [1f]    | first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and                 |
| [1g]    | second contact bumps disposed on the contact zones and electrically connected thereto,                                                                                |
| [1h]    | wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials. |
| Claim 2 |                                                                                                                                                                       |
| [2]     | The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.                                                         |
| Claim 3 |                                                                                                                                                                       |
| [3]     | The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.                                            |

| Claim 4 |                                                                                                                             |
|---------|-----------------------------------------------------------------------------------------------------------------------------|
| [4]     | The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component. |
| Claim 5 |                                                                                                                             |
| [5]     | The electronic module of claim 1, wherein the first contact bumps comprise tin.                                             |
| Claim 6 |                                                                                                                             |
| [6]     | The electronic module of claim 1, wherein the second contact bumps comprise copper.                                         |

# **APPENDIX A**

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## R. JACOB BAKER, PH.D., P.E.

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### PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is [here](#) and his ResearchGate profile is [here](#).

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than [100 graduate students](#).

Dr. Baker has done consulting for over [200 companies](#). His [research/development](#) activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of [online engineering education](#). As a result of this work, he is the named inventor on over [150 US patents](#) and the author of over [100 publications](#).

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over [50 invited talks](#) around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

## INDUSTRY EXPERIENCE

**2008 - present:** Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

**2013 - 2022:** Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

**2017 - 2019:** Worked with Vorpil Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

**2016 - 2019:** Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

**2013 - 2018:** Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonics application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

**2013 - 2015:** Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

**2010 - 2013:** Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

**2013:** Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

**2012:** Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

**2010 - 2012:** Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

**2009 - 2010:** Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

**2009 - 2010:** Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

**1994 - 2008:** Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

**January 2008:** Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

**May 1997 - May 1999:** Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

**Summer 1998:** Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

**Summers 1994 - 1995:** Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

**September - October 1993:** Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

**Summer 1993:** Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

**December 1985 - June 1993:** (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

**Summer 1985:** Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

## ACADEMIC EXPERIENCE

**January 1991 – present:** Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho:** Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

## EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering; May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge.*

## MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)  
Member of the honor societies Eta Kappa Nu and Tau Beta Pi  
Licensed Professional Engineer

## HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

## SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58<sup>th</sup> 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

## ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

## TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., "DRAM Circuit Design: Fundamental and High-Speed Topics", *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., "DRAM Circuit Design: A Tutorial", *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

### **BOOKS, OTHER (edited, chapters, etc.)**

Saxena, V. and Baker, R. J., "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., "CMOS Amplifier Design," chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

### **INVITED TALKS AND SEMINARS**

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMETS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

### **RESEARCH FUNDING**

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, \$120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, \$29,999 (Phase I), \$225,238 (Phase II), and \$79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, \$50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, \$149,998
- Baker, R. Jacob, (2018-2020) "Geiger Mode SiGe Receiver for Long-Range Optical Communications," NASA, \$99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, \$29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, \$29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), \$266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, \$299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, \$299,665

## DOCTORAL STUDENT SUPERVISION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

## MASTERS STUDENT SUPERVISION

91. Jazmine Bloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I/O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikarla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

## GRANTED US PATENTS

152. Baker, R. J., "Quantizing circuits having improved sensing," **10,658,018**, May 19, 2020.
151. Baker, R. J., "Quantizing circuits having improved sensing," **10,403,339**, September 3, 2019.
150. Baker, R. J., "Digital Filters with Memory," **10,366,744**, July 30, 2019.
149. Baker, R. J., "Quantizing circuits having improved sensing," **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., "NMOS regulated voltage reference," **9,753,481**, September 5, 2017.
147. Baker, R. J., "Digital Filters with Memory," **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., "Comparators for delta-sigma modulators," **9,641,193**, May 2, 2017.
144. Baker, R. J., "Quantizing circuits having improved sensing," **9,449,664**, September 20, 2016.
143. Baker, R. J., "Error detection for multi-bit memory," **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,299,423**, March 29, 2016.
141. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **9,299,405**, March 29, 2016.
140. Baker, R. J., "Comparators for delta-sigma modulators," **9,135,962**, September 15, 2015.
139. Baker, R. J., "Resistive memory element sensing using averaging," **9,081,042**, July 14, 2015.
138. Baker, R. J., "Digital Filters with Memory," **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources," **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,878,274**, November 4, 2014.
135. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,854,899**, October 7, 2014.

134. Baker, R. J., "Quantizing circuits with variable parameters," **8,830,105**, September 9, 2014.
133. Baker, R. J., "Integrators for delta-sigma modulators," **8,754,795**, June 17, 2014.
132. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **8,712,249**, April 29, 2014.
130. Baker, R. J., "Resistive memory element sensing using averaging," **8,711,605**, April 29, 2014.
129. Baker, R. J., "Memory with correlated resistance," **8,681,557**, March 25, 2014.
128. Baker, R. J., "Reference current sources," **8,675,413**, March 18, 2014.
127. Baker, R. J., "Methods for sensing memory elements in semiconductor devices," **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., "Dual well read-out integrated circuit (ROIC)," **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, "Resistive memory element sensing using averaging," **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, "Memory with correlated resistance," **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, "Phase splitter using digital delay locked loops," **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, "Subtraction circuits and digital-to-analog converters for semiconductor devices," **8,194,477**, June 5, 2012.
119. Baker, R. J., "Digital Filters for Semiconductor Devices," **8,149,646**, April 3, 2012.
118. Baker, R. J., "Error detection for multi-bit memory," **8,117,520**, February 14, 2012.
117. Baker, R. J., "Integrators for delta-sigma modulators," **8,102,295**, January 24, 2012.
116. Baker, R. J., "Devices including analog-to-digital converters for internal data storage locations," **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., "Multi-resistive integrated circuit memory," **8,093,643**, January 10, 2012.
114. Baker, R. J., "Quantizing circuits with variable parameters," **8,089,387**, January 3, 2012.
113. Baker, R. J., "Reference current sources," **8,068,367**, November 29, 2011.
112. Baker, R. J., "Methods of quantizing signals using variable reference signals," **8,068,046**, November 29, 2011.
111. Baker, R. J., "Systems and devices including memory with built-in self-test and methods of making using the same," **8,042,012**, October 18, 2011.
110. Baker, R. J., "Memory with correlated resistance," **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **7,941,056**, May 10, 2011.
108. Baker, R. J., "K-delta-1-sigma modulator," **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **7,869,249**, January 11, 2011.
104. Baker, R. J., "Subtraction circuits and digital-to-analog converters for semiconductor devices," **7,839,703**, November 23, 2010.
103. Baker, R. J., "Digital Filters with Memory" **7,830,729**, November 9, 2010.
102. Baker, R. J., "Systems and devices including memory with built-in self test and methods of making using the same," **7,818,638**, October 19, 2010.
101. Baker, R. J., "Integrators for delta-sigma modulators," **7,817,073**, October 19, 2010.
100. Baker, R. J., "Digital filters for semiconductor devices," **7,768,868**, August 3, 2010.
99. Baker, R. J., "Quantizing circuits with variable reference signals," **7,733,262**, June 8, 2010.
98. Baker, R. J., "Quantizing circuits for semiconductor devices," **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., "Multi-resistive integrated circuit memory," **7,642,591**, January 5, 2010.
96. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,616,474**, November 10, 2009.
95. Baker, R. J., "Resistive memory element sensing using averaging," **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., "Quantizing circuits with variable parameters," **7,538,702**, May 26, 2009.
93. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,528,877**, May 5, 2009.
92. Baker, R. J., "Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors," **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,495,964**, February 24, 2009.
90. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,489,575**, February 10, 2009.
89. Baker, R. J., "Per column one-bit ADC for image sensors," **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., "Input buffer design using common-mode feedback," **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,421,607**, September 2, 2008.
86. Baker, R. J., "Methods for resistive memory element sensing using averaging," **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., "Method and apparatus for sensing flash memory using delta-sigma modulation," **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor and method of operation," **7,366,003**, April 29, 2008.
83. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,330,390**, February 12, 2008.
82. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., "Method and apparatus providing input buffer design using common-mode feedback," **7,310,018**, December 18, 2007.
80. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., "Method and apparatus for reducing duty cycle distortion of an output signal," **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., "Method of operating a complementary bit resistance memory sensor," **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., "Rewrite prevention in a variable resistance memory," **7,224,632**, May 29, 2007.
73. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **7,151,698**, December 19, 2006.
72. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **7,151,689**, December 19, 2006.
71. Baker, R. J., "Resistive memory element sensing using averaging," **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., "Integrated circuit memory with offset capacitor," **7,109,545**, September 19, 2006.
68. Baker, R. J., "Input and output buffers having symmetrical operating characteristics and immunity from voltage variations," **7,102,932**, September 5, 2006.
67. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **7,095,667**, August 22, 2006.
66. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **7,082,045**, July 25, 2006.
65. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., "Complementary bit resistance memory sensor and method of operation," **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,987,701**, January 17, 2006.

62. Baker, R. J., "Adjusting the frequency of an oscillator for use in a resistive sense amp," **6,985,375**, January 10, 2006.
61. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,954,392**, October 11, 2005.
60. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,391**, October 11, 2005.
59. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., "Phase splitter using digital delay locked loops," **6,950,487**, September 27, 2005.
57. Baker, R. J., "Method and apparatus for measuring current as in sensing a memory cell," **6,930,942**, August 16, 2005.
56. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,917,534**, July 12, 2005.
55. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,914,838**, July 5, 2005.
54. Baker, R. J., "High speed low power input buffer," **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., "Method for stabilizing or offsetting voltage in an integrated circuit," **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,909,656**, June 21, 2005.
51. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., "Skewed sense AMP for variable resistance memory sensing," **6,888,771**, May 3, 2005.
49. Baker, R. J., "Method for reducing power consumption when sensing a resistive memory," **6,885,580**, April 26, 2005.
48. Moore, J. and Baker, R. J., "PCRAM rewrite prevention," **6,882,578**, April 19, 2005.
47. Baker, R. J., "Integrated charge sensing scheme for resistive memories," **6,870,784**, March 22, 2005.
46. Baker, R. J., "Sensing method and apparatus for a resistive memory device," **6,859,383**, February 22, 2005.
45. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,856,564**, February 15, 2005.
44. Baker, R. J., "Offset compensated sensing for a magnetic random access memory," **6,856,532**, February 15, 2005.
43. Baker, R. J., "Dual loop sensing scheme for resistive memory elements," **6,829,188**, Dec. 7, 2004.
42. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,826,102**, Nov. 30, 2004.
41. Baker, R. J., "Resistive memory element sensing using averaging," **6,822,892**, Nov. 23, 2004.
40. Baker, R. J., "System and method for sensing data stored in a resistive memory element using one bit of a digital count," **6,813,208**, Nov. 2, 2004.
39. Baker, R. J., "Wordline driven method for sensing data in a resistive memory array," **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., "Noise resistant small signal sensing circuit for a memory device," **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., "Methods and apparatus for measuring current as in sensing a memory cell," **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., "Complementary bit PCRAM sense amplifier and method of operation," **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., "Method and apparatus for sensing resistance values of memory cells," **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., "Phase detector for all-digital phase locked and delay locked loops," **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., "Producing walking one pattern in shift register," **6,771,249**, August 3, 2004.
31. Baker, R. J., "Sensing method and apparatus for resistance memory device," **6,741,490**, May 25, 2004.
30. Li, W., Schoenfeld, A., and Baker, R. J., "Method and apparatus for providing symmetrical output data for a double data rate DRAM," **6,704,881**, March 9, 2004.
29. Baker, R. J., "Method and system for writing data in an MRAM memory device," **6,687,179**, February 3, 2004.
28. Baker, R. J., "High speed digital signal buffer and method," **6,683,475**, January 27, 2004.
27. Baker, R. J., "High speed low power input buffer," **6,600,343**, July 29, 2003.
26. Baker, R. J., "Offset compensated sensing for magnetic random access memory," **6,597,600**, July 22, 2003.
25. Baker, R. J., "Sensing method and apparatus for resistive memory device," **6,577,525**, June 10, 2003.
24. Baker, R. J., "Method and apparatus for sensing resistance values of memory cells," **6,567,297**, May 20, 2003.

23. Baker, R. J., "High-speed digital signal buffer and method," **6,538,473**, March 25, 2003.
22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
21. Baker, R. J., "Resistive memory element sensing using averaging," **6,504,750**, January 7, 2003.
20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.
18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.
15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
13. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,104,209**, August 15, 2000.
12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
10. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **6,026,050**, February 15, 2000.
9. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **5,953,284**, September 14, 1999.
8. Baker, R. J., "Fully-differential amplifier," **5,953,276**, September 14, 1999.
7. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array", **5,909,201**, June 1, 1999.
6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
5. Baker, R. J., "Adaptively biased voltage regulator and operating method," **5,874,830**, February 23, 1999.
4. Hush, G. Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a Phase-Locked Loop," **5,818,365**, October 1, 1998.
3. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array," **5,638,085**, June 10, 1997.
2. Wilson, A. J., Baker, R. J., and Schoenfeld, A., "Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device," **5,614,856**, March 25, 1997.
1. Hush, G., Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a PLL," **5,598,156**, January 28, 1997.

#### INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a "Nano-Module."
- Baker, R. J., and Campbell, K. A., "Reconfigurable Analog Electronics using the Memristor."
- Baker, R. J., and Saxena, V., "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion."
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
- Baker, R. J., "Delta-Sigma Modulation for Sensing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2004
- Rivera, B. and Baker, R. J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," MURI Review, November, 2001.

## REFEREED JOURNAL PAPERS

26. Lopez, A., Strong, H. N., McGlothen, K. I., Hines, D. J., and Baker, R. J., "A compact avalanche-transistor based pulse generator for transcranial infrared light stimulation (TILS) experiments," *Instruments*, 2022, 6, 20.
25. Senda, D., Strong, H., Hines, D., Hines, R., and Baker, R. J., "A Compact 1200V, 700A, IGBT-Based Pulse Generator for Repetitive Transcranial Magnetic Stimulation In Vivo Laboratory Experiments," *Review of Scientific Instruments*, Vol. 92, Issue 8, August 30, 2021.
24. Wu, W., Baker, R. J., Bikkina, P., Long, Y., Levy, A., and Mikkola, E., "Design and Analysis of a Feedback Time Difference Amplifier with Linear and Programmable Gain," *Analog Integrated Circuits and Signal Processing, Springer*, 16 October, 2017.
23. Moumouni, Y. and Baker, R. J., "Modeling, Simulation, and Implementation of a Solar Thermoelectric Energy Harvesting System," *Journal of Energy and Power Engineering*, vol. 10, pp. 296-312, 2016.
22. Li, Y., Baker, R. J., and Raad, D., "Improving the Performance of Electrowetting on Dielectric Microfluidics Using Piezoelectric Top Plate Control," *Sensors and Actuators B: Chemical*, vol. 229, pp. 63-74, 2016.
21. Li, Y., Li, H., and Baker, R. J., "A Low-Cost and High-Resolution Droplet Position Detector for an Intelligent Electrowetting on Dielectric Device," *Journal of Laboratory Automation*, Vol. 20, No. 6, pp. 663-669, 2015.
20. Moumouni, Y., Ahmad, S., and Baker, R. J., "A System Dynamics Model for Energy Planning in Niger," *International Journal of Power and Energy Engineering*, Vol. 3, No. 6, pp. 308-322, 2014.
19. Estrada, D., Ogas, M. L., Southwick III, R. G., Price, P. M., Baker, R. J., and Knowlton, W. B., *Impact of Single pMOSFET Dielectric Degradation on NAND Circuit Performance*, Microelectronics Reliability, Vol. 48, No. 3, pp 354-363, 2008.
18. Leslie, M. B., and Baker, R. J., "Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 3, pp. 699-704, 2006.
17. Hess, H. L., and Baker, R. J., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices," *IEEE Transactions on Power Electronics*, Vol. 15, No. 5, pp. 923-930, 2000.
16. Lin, F., Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 4, pp. 565-568, 1999.
15. Bruce, J. D., Li, H. W., Dallabetta, M. J., and Baker, R. J., "Analog layout using ALAS!" *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 2, pp. 271-274, 1996.
14. Li, H. W., Dallabetta, M. J., and Baker, R. J., "An interactive impulse response extraction system," *Review of Scientific Instruments* 66(10), 5092-5095, 1995.
13. Ward, S. T., Baker, R. J., and Li, H. W., "A microchannel plate image intensifier gating circuit capable of pulse widths from 30 ns to 10 us," *Measurement Science and Technology*, Vol. 6, No. 11, pp. 1631-1633, 1995.
12. Keeth, B., Baker, R. J., and Li, H. W., "CMOS transconductor VCO with adjustable operating and center frequencies," *Electronics Letters*, 31(17), 1397-98, 1995.
11. Baker, R. J., "Time domain operation of the TRAPATT diode for picosecond-kilovolt pulse generation," *Review of Scientific Instruments*, 65(10), 3286-88, 1994.
10. Baker, R. J. and Ward, S. T., "Designing nanosecond high voltage pulse generators using power MOSFETs," *Electronics Letters*, 30(20), 1634-35, 1994.
9. Baker, R. J. and Johnson, B. P., "Sweep circuit design for a picosecond streak camera," *Measurement Science and Technology*, 5(4). 1994.
8. Baker R. J., Hodder, D. J., Johnson, B. P., Subedi, P. C., and Williams, D. C., "Generation of kilovolt-subnanosecond pulses using a nonlinear transmission line" *Measurement Science and Technology*, 4(8), 893-95, 1993.
7. Baker R. J., and Johnson, B. P., "Series operation of power MOSFETs for high speed, high voltage switching applications," *Review of Scientific Instruments* 65(6), 1993.

6. Baker R. J., and Johnson, B. P., "Applying the Marx bank circuit configuration to power MOSFETs," *Electronics Letters* 29(1), 56-57, 1993.
5. Baker R. J., and Johnson, B. P., "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments*, 63(12), 5799-5801, 1992.
4. Baker R. J., and Johnson, B. P., "A 500 Volt nanosecond pulse generator using cascode connected power MOSFETs," *Measurement Science and Technology*, 3(8), 775-77, 1992.
3. Baker R. J., Perryman, G. T., and Watts, P. W., "A fiber-optically triggered avalanche transistor," *IEEE Transactions on Instrumentation and Measurement*, 40(3), 649-52, 1991.
2. Baker R. J., "High voltage pulse generation using current mode second breakdown in a bipolar junction transistor," *Review of Scientific Instruments*, 62(4), 1031-1036, 1991.
1. Baker R. J., and Pocha, M. D. "Nanosecond switching using power MOSFETs," *Review of Scientific Instruments* 61(8), 2211-2213, 1990.

## REFERRED CONFERENCE PAPERS AND MAGAZINE ARTICLES

85. Strong, H., Senda, D., Baker, R. J., and Hines, D., "Focal Stimulation of Movement Related Cortical Potentials in Mice using a Novel TMS Circuit Design," *Brain Stimulation*, Vol. 14, Issue 6, November, 2021.
84. Arteaga, G., Namboodiri, S. P., Roy, A., and Baker, R. J., "Current Comparator with SiGe BiCMOS Input Stage for Photon-Counting LiDAR Applications," *IEEE 64<sup>th</sup> International Midwest Symposium on Circuits and Systems*, August 9-11, pp. 420-423, 2021.
83. Namboodiri, S. P. and Baker, R. J., "Incorporation of Chopping in Continuous Time K-Delta-1-Sigma Modulator," *IEEE 19th IEEE Interregional NEWCAS Conference*, June 13-16, 2021.
82. Namboodiri, S. P., Arteaga, G., Skelly, J., Mata-carlos, F., Roy, A., and Baker, R. J., "A Current-Mode Photon Counting Circuit for Long-Range LiDAR Applications," *IEEE 63<sup>rd</sup> International Midwest Symposium on Circuits and Systems*, August 9-12, pp. 146-149, 2020.
81. Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Segmented Digital SiPM," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 1118-1121, 2019.
80. Mellott, J. K., Monahan, E., Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Variable Fast Transient Digitizer," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 125-128, 2019.
79. Vinayaka, V., Namboodiri, S. P., Abdalla, Kerstetter, B., Mata-Carlos, F., Senda, D., Skelly, J., Roy, A., and Baker, R. J., "Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 57-62, Tysons Corner, VA, May 9-11, 2019.
78. Woodson, M., Estrella, S., Hay, K., Roy, A., Sun, K., Morgan, J., Beling, A., Baker, R. J., Renner, D., and Mashanovitch, M., "Photodetection at or below 1 micron wavelengths," *Proc. SPIE 10912, Physics and Simulation of Optoelectronic Devices XXVII*, 1091210, March 8, 2019.
77. Buck, K. and Baker, R. J., "Fast Transient Digitizer Chip for Capturing Single-Shot Events," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
76. Wu, W., Baker, R. J., Kumar, P., Garcia, F., and Mikkola, E., "A Linear High Gain Time Difference Amplifier Using Feedback Gain Control," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
75. Moumouni, Y. and Baker, R. J., "Analysis of a Residential 5kW Grid-tied Photovoltaic System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.
74. Moumouni, Y. and Baker, R. J., "LTspice Model of a Solar Thermoelectric Generation System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.
73. Li, Y. and Baker, R. J., "Computer Vision Assisted Measurement of the Displacements of a Bimorph Piezoelectric Cantilever Beam," *Proceedings of the IEEE Biomedical Circuits and Systems (BioCAS 2015) Conference*, October 22-24, 2015.
72. Li, Y. and Baker, R. J., "A Highly Efficient and Reliable Electrowetting on Dielectric Device for Point-of-Care Diagnostics," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
71. Roy, A. and Baker, R. J., "A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
70. Li, Y. and Baker, R. J., "Precise EWOD Top Plate Positioning Using Inverse Preisach Model Based Hysteresis Compensation," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.

69. Moumouni, Y. and Baker, R. J., "Buffer Sizing of Concentrated Photovoltaic Batteries: An Economic Analysis," *IEEE 58<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 704-707, August 2-5, 2015.
68. Moumouni, Y. and Baker, R. J., "Application of Used Electric Vehicle Batteries to Buffer Photovoltaic Output Transients," *IEEE 58<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 700-703, August 2-5, 2015.
67. Roy, A., Meza, M., Yurgelon, J., and Baker, R. J., "An FPGA Based Passive K-Delta-1-Sigma Modulator," *IEEE 58<sup>th</sup> Midwest Symposium on Circuits and Systems*, pp. 121-124, August 2-5, 2015.
66. Moumouni, Y. and Baker, R. J., "Concise Thermal to Electrical Parameters Extraction of Thermoelectric Generator for Spice Modeling," *IEEE 58<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 596-599, August 2-5, 2015.
65. Moumouni, Y. and Baker, R. J., "Improved SPICE Modeling and Analysis of a Thermoelectric Module," *IEEE 58<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 600-603, August 2-5, 2015.
64. Li, Y., Li, H., and Baker, R. J., "Volume and Concentration Identification by Using an Electrowetting on Dielectric Device," *Proceedings of 10<sup>th</sup> IEEE Dallas Circuits and Systems Conference*, October 12-13, 2014.
63. Li, Y., Chen, R., and Baker, R. J., "A Fast Fabricating Electro-wetting Platform to Implement Large Droplet Manipulation," *Proceedings of the IEEE 57<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 326-329, August 3-6, 2014.
62. Roy, A. and Baker, R. J., "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion," *Proceedings of the IEEE 57<sup>th</sup> International Midwest Symposium on Circuits and Systems*, pp. 595-598, August 3-6, 2014.
61. Baker, R. J., "Massive Open Online Courses for Educating Circuit Designers: What Works and What Doesn't," *IEEE Solid-State Circuits Magazine*, Vol. 6, No. 2, pp. 63-65, 2014.
60. Montierth, D., Strand, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process," *IEEE 55<sup>th</sup> International Midwest Symposium on Circuits and Systems*, August 5-8, 2012.
59. VanAckern, G., Baker, R. J., Moll, A. J., and Saxena, V. "On-Chip 3D Inductors using Thru-Wafer Vias," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
58. Yap, K. and Baker, R. J., "Two Techniques to Reduce Gain and Offset Errors in CMOS Image Sensors using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
57. Labaziewicz, A. and Baker, R. J., "A 2 GHz Effective Sampling Frequency K-Delta-1-Sigma Analog-to-Digital Converter," *Proceedings of the IEEE 54<sup>th</sup> International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
56. Saxena, V., Balagopal, S., and Baker, R. J., "Systematic Design of Three-Stage Op-amps using Split Length Compensation," *Proceedings of the IEEE 54<sup>th</sup> International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
55. Harvard, Q. and Baker, R. J., "A Scalable I/O Architecture for Wide I/O DRAM," *Proceedings of the IEEE 54<sup>th</sup> International Midwest Symposium on Circuits and Systems*, August 7-10, 2011.
54. Wald, S., Baker, R. J., Mitkova, M., and Rafla, N., "A Non-Volatile Memory Array Based on Nano-Ionic Conductive Bridge Measurements," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 43-46, April 22, 2011.
53. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," *Proceedings of the IEEE 53<sup>rd</sup> International Midwest Symposium on Circuits and Systems*, August 1-4, 2010.
52. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage Fully-Differential Op-Amps," (invited) *Proceedings of the IEEE 53<sup>rd</sup> International Midwest Symposium on Circuits and Systems*, August 1-4, 2010.
51. Harvard, Q., Baker, R. J., and Drost, R., "Main Memory with Proximity Communication: A Wide I/O DRAM Architecture," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 40-43, April 16, 2010.

50. Yap, K. M. and Baker, R. J., "Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 52-55, April 16, 2010.
49. Gagliano, C. and Baker, R. J., "A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation," *Proceedings (poster) of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 16, 2010.
48. Montierth, D., Yap, K. M., and Baker, R. J., "CMOS Image Sensor using Delta-Sigma Modulation," *4<sup>th</sup> Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
47. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," *4<sup>th</sup> Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
46. Li, K., Saxena, V., Zheng, G., and Baker, R. J., "Full Feed-Forward K-Delta-1-Sigma Modulator," *4<sup>th</sup> Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
45. Bollschweiler, L., English, A., Baker, R. J., Kuang, W., Chang, Z.-C., Shih, M.-H., Knowlton, W.B., Hughes, W.L., Lee, J., Yurke, B., Cockerham, N. S., and Tyree, V. C., "Chip-Scale Nanophotonic Chemical and Biological Sensors using CMOS Process," *Proceedings of the IEEE 52<sup>nd</sup> Midwest Symposium on Circuits and Systems*, pp. 413-416, August 2-5, 2009.
44. Saxena, V., Li, K., Zheng, G., and Baker, R. J., "A K-Delta 1-Sigma Modulator for Wideband Analog to Digital Conversion," *Proceedings of the IEEE 52<sup>nd</sup> International Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009.
43. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," *Proceedings of the IEEE 52<sup>nd</sup> International Midwest Symposium on Circuits and Systems*, pp. 9-12, August 2-5, 2009.
42. Regner, J., Balasubramanian, M., Cook, B., Li, Y., Kassayebetre, H., Sharma, A., Baker, R. J., and Campbell, K. A., "Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 28-31, April, 2009.
41. Gupta, S. Saxena, V., Campbell, K. A., and Baker, R. J., "W-2W Current Steering DAC for Programming Phase Change Memory," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 59-62, April, 2009.
40. Rapole, H., Rajagiri, A., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "Resistive Memory Sensing Using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 63-66, April, 2009.
39. Kassayebetre, H., Regner, J., Rajagiri, A., Sharma, A., Hay, R. R., Baker, R. J., and Campbell, K.A., "Surface Acoustic Wave Device Fabrication using Zinc Oxide and Chalcogenide Thin Films," poster presentation at the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2009.
38. Ande, H. K., Busa, P., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory," *Proceedings of the IEEE 51<sup>st</sup> International Midwest Symposium on Circuits and Systems*, pp. 570-573, August 10-13, 2008.
36. Saxena, V., and Baker, R. J., "Compensation of CMOS Op-Amps using Split-Length Transistors," *Proceedings of the IEEE 51<sup>st</sup> Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008.
36. Saxena, V., and Baker, R. J., "Indirect Compensation Technique for Low-Voltage Op-Amps," *Proceedings of the 3<sup>rd</sup> Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008.
35. Cahoon, C., and Baker, R. J., "Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 16-19, April, 2008.
34. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Hendricks, K., Southwick III, R. G., Henderson, J., Oxford, J., Moll, A., Kuang, W., and Baker, R. J., "Progress Towards a Biomolecular Nanowire Sensor Array for Biomedical Applications," invited talk presented at the 6th Annual INBRE/COBRE Research Conference, Moscow, ID, August 6, 2007
33. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Southwick III, R.G., Oxford, J., Moll, A., Baker, R. J., and Kuang, W., "Development of Biomolecular Nanostructure Sensor Arrays," presented at the Sensors

and Sensor Technology session for the program of the 88th annual meeting of the AAAS, Pacific Division, June 2007, Boise, ID

32. Knowlton, W. B., Kuang, W., Araujo D., Price, P. M., Brotherton, J., Coonse, K. Bollschweiler, L., Southwick, R., Oxford, J. Moll, A., and Baker, R. J., "Nanofabrication of 3D Sensor Arrays for Detection," Advanced Fuel Cycle Workshop, May 8-9, 2007, Boise, ID
31. Loo, S. M., Cole, J., Youngberg, R., Baker, R. J., Gribb, M. M., "Field-programmable gate array in a miniature ion mobility spectrometer sensor system," *Proceedings of the 2006 International Conference on Embedded Systems & Applications*, June 26-29, 2006, Las Vegas, NV.
30. Saxena, V., and Baker, R. J., "Indirect Feedback Compensation of CMOS Op-Amps," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 3-4, April, 2006.
29. Duvvada, K., Saxena, V., and Baker, R. J., High Speed Digital Input Buffer Circuits, *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April, 2006.
28. Saxena, V., Plum, T. J., Jessing, J. R., and Baker, R. J., "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 17-18, April, 2006.
27. Gorseth, T. L., Estrada, D., Kiepert, J., Ogas, M. L., Cheek, B. J., Price, P. M., Baker, R. J., Bersuker, G., and Knowlton, W.B., "Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation," presented at the *Workshop on Microelectronic Devices* (Boise, Idaho; April 14, 2006)
26. Sevier, D., Gribb, M., Plumlee, D., Moll, A. J., Hill, H. H., Hong, F., Baker, R. J., Loo, S. M., Walters, R. and Imonigie, J., "An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone," *Fourth International Conference on Unsaturated Soils (UNSAT '06) Conference, April 2-6, 2006, Carefree, AZ.*
25. Gribb, M., Hill, H. H., Baker, R. J., Loo, S. M., and Moll, A. J., "Ion Mobility Spectrometer (IMS) Sensor Project," presented at the *Environmental & Subsurface Science Symposium*, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
24. Ogas, M. L., Price, P. M., Kiepert J., Baker R. J., Bersuker G., and Knowlton W.B., *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
23. Butler, D. L. and Baker, R. J., *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, *Proceedings of the IEEE 48<sup>th</sup> International Midwest Symposium on Circuits and Systems*, Aug. 7-10, 2005.
22. Cheek, B. J., Southwick III, R. G., Ogas, M. L., Nagler, P. E., Whelchel, D., Kumar, S., Baker, R. J., and Knowlton, W. B., "Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits," poster presentation at *2004 IEEE International Integrated Reliability Workshop*, Oct. 18-21, 2004.
21. Ogas, M., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., "Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra-Thin Oxides," poster presentation at the *Workshop on Microelectronics and Electron Devices*, Boise, Idaho, April 16, 2004.
20. Ogas, M. L., Southwick III, R. G., Cheek, B. J., Baker, R. J., Bersuker, G., and Knowlton, W. B., "Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices," in *Proceedings of the 2004 IEEE International Integrated Reliability Workshop*, pp. 32-36.
19. Cheek, B. J., Stutzke, N., Santosh, K., Baker, R. J., Moll, A. J., and Knowlton, W. B., Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, *2004 IEEE International Reliability Physics Symposium*, April, 25-29.
18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
17. Ogas, M. L., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.

15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)*, IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop*, October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop*, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society Meeting*, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference 2000*, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference*, Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41<sup>st</sup> International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41<sup>st</sup> International Midwest Symposium on Circuits and Systems*, August 9-12, 1998.
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40<sup>th</sup> International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers*, April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

## EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposited 109 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

### Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – MediaTek, Inc. v. Redstone Logics LLC

Case Number – IPR2025-00085. Petition filed on October 22, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

**Baker Botts LLP (Houston, TX)**

Case – Innolux Corporation v. Phenix Longhorn LLC

Case Numbers – IPR2025-00043 and IPR2025-00044. Petitions filed on October 15, 2024.

Case Subject Matter – Systems and methods for outputting “corrected” gamma reference voltages to drive a Liquid Crystal Display (LCD).

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Dority & Manning LLP (San Diego, CA and Greenville, SC)**

Case – LithiumHub, LLC v. Bass Pro Outdoor et. al.

Case Numbers – ITC Investigation No. 337-TA-1421. Complaint filed September 12, 2024.

Case Subject Matter – starting a combustion engine using lithium-based battery cells and solid-state switches.

Work Performed – Provided expert consulting services. Wrote declaration for a claim construction brief.

**Baker Botts LLP (Austin, TX and Houston, TX)**

Case – Silicon Motion Inc. v. K.Mizra, LLC

Case Number – IPR2024-01236. Petition filed on September 10, 2024.

Case Number – IPR2024-01240. Petition filed on August 13, 2024.

Case Number – IPR2024-01241. Petition filed on August 9, 2024.

Case Subject Matter – Calibrating a memory controller for use with DDR (double-data rate) DRAM (dynamic random access memory). Calibrating a communication channel to receive a digital signal. A micro-threaded memory device.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Garlick & Markison, LLC (Phoenix, AZ and Austin, TX)**

Case – Ex Parte Reexamination

Case Number – 90/019612. Request filed on August 6, 2024.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declaration.

**Bookoff McAndrews, PLLC (Washington, DC)**

Case – Lenovo Inc. v. Intellectual Ventures II LLC

Case – Lenovo Inc. v. University of Rochester

Case Numbers – IPR2024-01225 and IPR2024-01226. Petitions filed on August 2, 2024.

Case Subject Matter – Methods for calibrating intra-cycle timing in digital communications. Digital circuits with multiple clock domains.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Wolf, Greenfield & Sacks, P.C. (Washington, D.C., and Boston, MA)**

Case – Infineon Technologies v. Innoscience Technology

Case Numbers – ITC Investigation No. 337-TA-1414. Complaint filed July 26, 2024.

Case Subject Matter – GaN-on-Si semiconductor devices, GaN field effect transistors (FETs), and packaging power transistors.

Work Performed – Provided expert consulting services.

**DLA Piper LLP (Palo Alto, CA and Austin, TX)**

Case – BOE Technology Group Co., Ltd. v. Optronix Sciences LLC

Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024

Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Dentons US LLP (Washington, DC)**

Case – Reolink Digital Technology Co., Ltd. v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Paul Hastings LLP (Washington, DC)**

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reexaminations.

**Banner Witcoff (Chicago, IL and Washington, DC)**

Case – ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd. v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

**Fish & Richardson P.C. (San Diego, CA and Boston, MA)**

Case – Vicor Corporation v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

**Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)**

Case – Redstone Logics LLC v. MediaTek, Inc.

Case Number – Texas, WD (Midland/Odessa) 7:24-cv-00029. Complaint filed January 26, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

**Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)**

Case – RoadRunner Recycling, Inc. v. Recycle Tract Systems

Case Number – California, ND 3:23-cv-04804. Amended complaint filed on January 16, 2024.

Case Subject Matter – Waste and recycling metering technology.

Work Performed – Provided expert consulting services including writing expert report. Was deposed.

**Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)**

Case – Silicon Motion, Inc. v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

**Garlick & Markison, LLC (Austin, TX)**

Case – NXP USA, Inc. v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

**Unified Patents, LLC (Washington, DC)**

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

**Haynes and Boone, LLP (Dallas, TX)**

Case – Western Digital Technologies, Inc. v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

**Paul Hastings LLP (Washington, DC)**

Case – Samsung Electronics Co., Ltd. v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)**

Case – Unification Technologies LLC v. Silicon Motion, Inc.

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

**Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)**

Case – Current Lighting Solutions, LLC d/b/a GE Current v. Jiaying Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

**Faegre Drinker Biddle & Reath LLP (San Francisco, CA, Washington, DC, and Minneapolis, MN)**

Case – CogniPower LLC v. Samsung Electronics

Case Number – Texas, ED (Marshall) 2:23-cv-00160. Complaint filed April 10, 2023.

Case Subject Matter – Power conversion using switching power supplies.

Work Performed – Provided expert consulting services and wrote expert reports.

**Baker Botts LLP (Dallas, TX)**

Case – Lennox Industries Inc. v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Cooley LLP (Palo Alto, CA)**

Case – Nintendo Co., Ltd. and Nintendo of America Inc. v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

**Bracewell LLP (New York, NY and Seattle, WA)**

Case – Kioxia America, Inc. and Kioxia Corporation v. BitMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Bookoff McAndrews, PLLC (Washington, DC)**

Case – Lenovo Inc. and Motorola Mobility LLC v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

**Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)**

Case – Semiconductor Design Technologies LLC v. Cadence Design Systems, Inc.

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

**McDermott Will & Emery LLP (Chicago, IL and Austin, TX)**

Case – Xilinx, Inc. v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

**Willkie Farr & Gallagher LLP (San Francisco, CA)**

Case – Bell Semiconductor, LLC v. Synopsys, Inc.

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

**Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)**

Case – Element Capital Commercial Company PTE. LTD v. BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

**Baker Botts LLP (San Francisco, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)**

Case – Polaris PowerLED, LLC v. Samsung Electronics and Samsung Display

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

**Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)**

Case – Synopsys, Inc. and Cadence Design Systems, Inc. v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

**Paul Hastings LLP (Washington, DC)**

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

**Russ August & Kabat (Los Angeles, CA)**

Case – Resonant Systems, Inc. v. Sony

Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.

Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed.

**Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)**

Case – Bell Semiconductor, LLC v. NXP, SMC, Micron, Nvidia, Advanced Micro Devices (AMD), Acer, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

**O'Melveny & Myers LLP (Los Angeles, CA)**

Case – Daedalus Prime LLC v. Samsung Electronics and Qualcomm Inc.

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

**Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)**

Case – Sonrai Memory LTD. v. Micron Technology, Inc.

Case Numbers – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.

Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

**Russ August & Kabat (Los Angeles, CA and New York, NY)**

Case – NextGen Innovations, LLC v. Infinera, Fujitsu, AT&T, and Nokia

Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.

Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

**DLA Piper (Chicago, IL and Washington, DC)**

Case – Ampt, LLC v. SolarEdge Technologies, Inc.

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

**Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)**

Case – Signify North America Corporation v. Shenzhen Intellirocks Tech Co.

Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.

Case Subject Matter – LED packaging, circuits, and systems.

Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

**Baker Botts LLP (Dallas, TX)**

Case – Rosen Technologies LLC v. Lennox Industries Inc.

Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services.

**Paul Hastings LLP (Austin, TX and Washington, DC)**

Case – Samsung Electronics Co., Ltd. v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)**

Case – Ex Parte Reexaminations

Case Number – 90/015020. Request filed on May 2, 2022.

Case Number – 90/014906. Request filed on November 12, 2021.

Case Number – 90/014899. Request filed on November 10, 2021.

Case Number – 90/014888. Request filed on October 21, 2021.

Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.

Case Number – 90/014885. Request filed on October 19, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging.

Work Performed – Provided expert consulting services and wrote declarations.

**DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)**

Case – SolarEdge Technologies, Inc. v. Fronius International GMBH

Case Number – IPR2022-00849. Petition filed on April 14, 2022.

Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a “rotate-and-lift” feature.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

**Kirkland & Ellis LLP (New York, NY)**

Case – Samsung Electronics Co. v. Sonrai Memory Ltd.

Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.

Case Subject Matter – USB devices and circuits for saving power.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

**Haynes and Boone, LLP (Washington, DC)**

Case – Unified Patents, LLC v. Arigna Technology Limited

Case Number – IPR2022-00285. Petition filed on December 9, 2021.

Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).

Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

**Paul Hastings LLP (Washington, DC)**

Case – Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.

Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021

Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.

Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.

Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.

Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.

Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).

Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

**Haynes and Boone, LLP (Plano, TX)**

Case – Pure Storage, Inc. v. Digital Cache, LLC

Case Number – IPR2022-00121. Petition filed on October 29, 2021.

Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

**Banner Witcoff (Washington, DC)**

Case – SolarEdge Technologies Ltd. v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

**Paul Hastings LLP (Austin, TX and Washington, DC)**

Case – Samsung Electronics Co., Ltd. v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

**Paul Hastings, LLC (Washington, DC)**

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

**Jones Day (San Diego, CA and Pittsburgh, PA)**

Case – SOLiD, Inc. v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

**Unified Patents, LLC (Washington, DC)**

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

**Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)**

Case – Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

**Hill, Kertscher & Wharton, LLP (Atlanta, GA)**

Case – Kaijet Technology v. Sanho Corporation

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

**O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)**

Case – Solas OLED LTD. v. Samsung Electronics Co. LTD.

Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.

Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

**O'Melveny & Myers LLP (San Francisco, CA)**

Case – Super Interconnect Technologies LLC v. Google LLC

Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).

Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).

Work Performed – Provided expert consulting services and wrote expert reports.

**Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)**

Case – Fundamental Innovation Systems International LLC v. Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect

Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

**Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)**

Case – TCT Mobile Inc. and TCL Communication, Inc. v. Fundamental Innovation Systems International LLC

Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.

Case Number – IPR2021-00428. Petition filed on January 13, 2021.

Case Number – IPR2021-00410. Petition filed on January 11, 2021.

Case Number – IPR2021-00395. Petition filed on December 31, 2020.

Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.

Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

**Paul Hastings LLP (Austin, TX and Washington, DC)**

Case – Samsung, Inc. v. Pictos Technologies, Inc.

Case Number – IPR2021-00557. Petition filed on February 18, 2021.

Case Number – IPR2021-00436. Petition filed on January 19, 2021.

Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.

Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

**O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)**

Case – Solas OLED Ltd. v. BOE Technology Group Co. Ltd. and Samsung Electronics

Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.

Case Subject Matter – Active matrix OLED display devices and components

Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

**Paul Hastings LLP (Washington, DC)**

Case – Samsung, Inc. v. Garrity Power Services LLC

Case Number – IPR2021-00389. Petition filed on December 31, 2020.

Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.

Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.