IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Tuominen et al.	
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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 11,071,207 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 11,071,207 ("the '207 patent")
APPLE-1002	File History of U.S. Patent No. 11,071,207
APPLE-1003	Expert Declaration of Dr. R. Jacob Baker, Ph.D., P.E.
APPLE-1004	U.S. Patent No. 5,616,520 to Nishiuma et al. ("Nishiuma")
APPLE-1005	U.S. Publication No. 2002/0149117 to Shibata ("Shibata")
APPLE-1006	U.S. Patent No. 6,555,758 to Stelzl et al. ("Stelzl")
APPLE-1007	U.S. Publication No. 2002/0159242 to Nakatani et al. ("Nakatani")
APPLE-1008	Japanese Patent Publication No. 2001-085473 to Onda with Certified Translation ("Onda")
APPLE-1009	Japanese Patent Publication No. 11-191574 to Matsuda with Certified Translation ("Matsuda")
APPLE-1010	U.S. Patent No. 4,912,844 to Parker ("Parker")
APPLE-1011	U.S. Publication No. 2003/0034557 to Gupta et al. ("Gupta")
APPLE-1012	Johnson et al., *High Speed Digital Design: A Handbook of Black Magic*, Prentice Hall PTR, Englewood Cliffs, New Jersey 07632 © 1993
APPLE-1013-1019	RESERVED
APPLE-1020	U.S. Patent No. 4,068,022 to Glick ("Glick")

APPLE-1021	J.A. Scarlett, *The Multilayer Printed Circuit Board Handbook*, Electrochemical Publications Limited, 8 Barns Street, Ayr Scotland © 1985
APPLE-1022	J.A. Scarlett, *An Introduction to Printed Circuit Board Technology*, Electrochemical Publication Limited, 8 Barns Street, Ayr Scotland © 1984
APPLE-1023	U.S. Patent No. 6,548,330 ("Murayama")
APPLE-1024	U.S. Patent No. 6,011,313 ("Shangguan")
APPLE-1025	RESERVED
APPLE-1026	U.S. Publication No. 2021/0037654 ("Tuominen Pub.")
APPLE-1027-1033	RESERVED
APPLE-1034	U.S. Patent No. 5,060,051 to Usuda ("Usuda")
APPLE-1035	William D. Callister, Jr., Materials Science and Engineering: An Introduction, 5th Ed., John Wiley & Sons, Inc. © 2000
APPLE-1036	Simon Thomas, *3D-Integration: Trends and Opportunities – An Overview* (Materials Research Society 2003)
APPLE-1037	R. Kujala, et. al., *Solderless Interconnection and Packaging Technique for Embedded Active Components* (IEEE 1999)
APPLE-1038	U.S. Patent Publication No. 2001/0026010 to Horiuchi ("Horiuchi")
APPLE-1039	U.S. Patent No. 6,038,133 to Nakatani et al. ("Nakatani-II")
APPLE-1040	U.S. Patent No. 5,250,843 to Eichelberger ("Eichelberger")
APPLE-1041	International Patent Application WO1996012296 to Suwa et al. and Certified Translation ("Suwa")

APPLE-1101	Complaint for Patent Infringement (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1
APPLE-1102	Amended Complaint for Patent Infringement (April 11, 2024), Case No. 1-24-cv-00129 (WDTX), Document 31 (redacted)
APPLE-1103	K. Vidal Memorandum on *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, June 21, 2022
APPLE-1104	*United States District Courts – National Judicial Caseload Profile* (June 2024) (retrieved from https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0630.2024.pdf)
APPLE-1105	Exhibit 17 to Complaint for Patent Infringement – Infringement Claim Chart for ’207 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-17
APPLE-1106	Return of Service (February 8, 2024), Case No. 1-24-cv-00129 (WDTX), Document 8

LISTING OF CLAIMS

Claim 1	
[1pre]	An electronic module, comprising:
[1a]	a first conductive-pattern layer and
[1b.i]	a second conductive-pattern layer disposed on the first conductive-pattern layer,
[1b.ii]	the second conductive-pattern layer having a first surface;
[1c]	an insulating-material layer disposed on the first surface of the second conductive-pattern layer;
[1d]	at least one installation cavity disposed in the insulating-material layer;
[1e.i]	a component disposed within the at least one installation cavity,
[1e.ii]	the component comprising contact zones comprising aluminum;
[1f]	first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and
[1g]	second contact bumps disposed on the contact zones and electrically connected thereto,
[1h]	wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.
Claim 2	
[2]	The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.

Claim 3	
[3]	The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.
Claim 4	
[4]	The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.
Claim 5	
[5]	The electronic module of claim 1, wherein the first contact bumps comprise tin.
Claim 6	
[6]	The electronic module of claim 1, wherein the second contact bumps comprise copper.

I. INTRODUCTION

Apple Inc. ("Apple" or "Petitioner") petitions for *Inter Partes* Review ("IPR") of claims 1-6 ("the Challenged Claims") of U.S. Patent No. 11,071,207 ("the '207 patent").

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Apple certifies that the '207 patent is available for IPR. This Petition is being filed within one year of service of a complaint by ImberaTek, filed February 5, 2024 and served February 6, 2024. *See* APPLE-1101; APPLE-1106.

Petitioner is not barred or estopped from requesting review of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested

Petitioner requests institution of IPR and cancellation of the Challenged Claims based on the following grounds:

Ground	Claims	Basis under 35 U.S.C. § 103
1A	1-6	Nishiuma in view of Shibata
1B	1-6	Nishiuma-Shibata in view of Glick
1C	3-4	Nishiuma-Shibata in view of Parker
2A	1-2, 5-6	Nakatani in view of Onda and Glick
2B	3-4	Nakatani-Onda-Glick in view of Parker

Grounds 1A-2B are further supported by the expert testimony of Dr. Baker. *See* APPLE-1003, ¶¶1-233.

The '207 patent claims priority through several intervening applications to a foreign application filed February 26, 2003. APPLE-1001, Cover (30). Petitioner does not concede that any '207 patent claim is entitled to the benefit of the alleged priority application filing dates, but nonetheless, all references forming the basis of the grounds predate the filing of each of these applications. Petitioner accordingly treats February 26, 2003 as the Critical Date, exclusively for purposes of the analysis in this Petition. APPLE-1003, ¶¶15, 41, 44.

Reference	Filing Date	Publication Date	Pre-AIA Prior Art Status
Nishiuma (APPLE-1004)	12/30/1994	04/01/1997	§§102(a)-(b), (e)
Shibata (APPLE-1005)	07/16/2001	11/17/2002	§§102(a), (e)
Nakatani (APPLE-1007)	11/16/2001	11/31/2002	§§102(a), (e)
Onda[1] (APPLE-1008)	---	03/30/2001	§§102(a)-(b)
Glick (APPLE-1020)	12/10/1974	01/10/1978	§§102(a)-(b), (e)
Parker (APPLE-1010)	08/10/1998	04/03/1990	§§102(a)-(b), (e)

[1] This Petition cites a certified English translation of Onda to identify relevant aspects of the underlying prior art reference. Exhibit APPLE-1008 includes both the English translation and the underlying Japanese reference.

Nishiuma, Shibata, Nakatani, Onda, Glick, and Parker are all analogous art to the ’207 patent in that they are all in the same field of endeavor and/or reasonably pertinent to the problems said to be addressed by the ’207 patent. APPLE-1003, ¶63. For example, like the ’207 patent, each of the prior art references applied in Grounds 1A-2B describes techniques for manufacturing and packaging electronic modules. APPLE-1003, ¶63; APPLE-1001, 1:14-37; *infra*, §IV; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

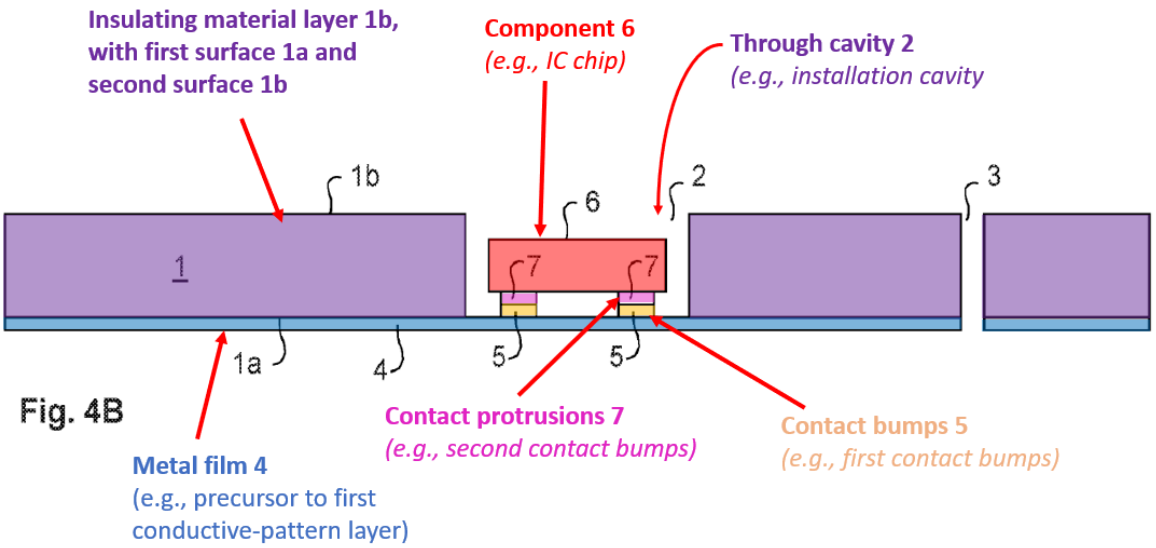
C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art relating to the subject matter of the ’207 patent as of the Critical Date (“POSITA”) would have had a Bachelor’s degree in electrical engineering, materials science, applied physics, or a related technical field, and 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. APPLE-1003, ¶¶41-43. Additional education could substitute for professional experience, and *vice versa*. *Id*.

III. SUMMARY OF THE ’207 PATENT

A. Brief Description

The ’207 patent describes “an electronic module which includes one or more components embedded in an installation base.” APPLE-1001, 1:25-26; APPLE-1003, ¶¶44-47.



APPLE-1001, FIG. 4B (annotated)

In an example, the '207 patent discloses a method for forming an electronic module such as a circuit board that includes "through cavities 2, selected to suit the size of the components 6 to be installed, … made in [an] insulating material layer 1." *Id.*, 6:14-16. "An unpatterned metal film 4, which acts as the conducting surface of the installation base for the components 6 to be installed and connected is made on the first surface 1a of the insulating substance layer 1." *Id.*, 6:23-26. "The metal film 4 can be manufactured… by laminating copper (Cu) [or] can also be a surfaced metal film, ***or some other film including several layers or several materials***." *Id.*, 6:26-30. "[C]onductive patterns 14 are formed from the conductive layer 4 …." *Id.*, 10:32-39, FIGS. 6A-6C. "[T]he connection zones or

contact protrusions 7 on the surface of the components 6 are connected to the metal film." *Id*., 6:38-42. The '207 patent describes that "[i]n some embodiments, contact bumps 5, to which the connection zones or contact protrusions 7 of the components 6 are connected, are made on top of the conductive film 4." *Id*., 7:1-3.

B. Prosecution History

In the only Office Action issued during prosecution, the Examiner rejected the originally-filed claim as obvious based on Murayama (APPLE-1023) in view of Shangguan (APPLE-1024). APPLE-1002, 121-127; *see also id.*, 10; APPLE-1003, ¶¶48-49. Applicant responded by amending claim 1 as shown below and adding dependent claims 2-6. *Id.*, 171-172.

1. (Currently Amended) An electronic module, comprising:

[[-]]a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface[[,]];

~~–a second conductive-pattern layer having a second surface,~~

~~–a flexible~~an insulating-material layer ~~between the first surface of the first conductive-pattern layer and the second~~disposed on the first surface of the second conductive-pattern layer[[,]];

at least one installation cavity disposed in the insulating-material layer;

[[-]]a component disposed within the at least one installation cavity, the component comprising ~~having flat~~ contact zones comprising aluminum;~~between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer, at least some of the flat contact zones being electrically connected to the first conductive-pattern layer by means of solderless and metallurgical connections, said connections each comprising at least one solid~~

first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and~~between the first conductive-pattern layer and the respective contact zone, and~~

second contact bumps disposed on the contact zones and electrically connected thereto,

wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials~~–a filler around the component, the filler securing the component mechanically to a flexible sheet~~.

APPLE-1002, 171-172

The amendment to claim 1 provided that the second conductive-pattern layer is "disposed on" the first conductive-pattern layer and added that at least one of the first and second conductive-pattern layers includes "at least two layers of at least two different materials." *Id.* The applicant contended that support for the amendments was found in paragraphs [0036], [0039], and [0060] of the published application (APPLE-1026), corresponding to cols. 6:7-35, 6:52-59, and 10:14-21 of the later-issued '207 patent, which describe conductive layers disposed on one another as a result of surfacing a first layer with additional metals (APPLE-1026,

[0036]) and further describe a "metal layer…[that] can naturally also include several metals as layers, accumulations, zones, or metal alloys" (APPLE-1026, [0039]). APPLE-1002, 173.

The Examiner allowed the application and identified a collection of limitations in amended claim 1 in her reasons for allowance. APPLE-1002, 180-184. However, as discussed in §IV, the application never should have been allowed. All features recited in the Challenged Claims are disclosed in one or more of Nishiuma, Shibata, Nakatani, Onda, Glick and Parker, and the claimed combinations of these features would have been obvious before the Critical Date. APPLE-1003, ¶¶50-52, 64-233.

C. Claim Construction

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. Petitioner addresses the scope of the claim phrase "at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials" below, but Petitioner submits that formal claim constructions are otherwise presently unnecessary in view of the substantial overlap between the prior art teachings applied in Grounds 1A-2B and

the preferred embodiments of the '207 patent.[2] *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("claim terms need only be construed to the extent necessary to resolve the controversy"); APPLE-1003, ¶¶53-61. This Petition also applies the prior art in a manner consistent with Patent Owner's allegations of infringement before the district court. *See* APPLE-1105.

1. "at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials"

Element [1h] should be interpreted such that ***only one*** of the two conductive-pattern layers must include "at least two layers of at least two different materials." There is no requirement for both the first and second conductive-pattern layers to include at least two layers of at least two different materials. APPLE-1003, ¶¶56-61. It is well established that the plain and ordinary meaning of the phrase "at least one of" is "one or more of," and in Element [1h], "at least one of" modifies "the first conductive-pattern layer and second conductive-pattern layer," thus making clear that the requirement for "at least two layers of at least two different materials" applies only to one or more of—but not necessarily both—the first and

[2] Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

second conductive-pattern layers. *SuperGuide Corp. v. DirecTV Enters., Inc.,* 358 F.3d 870, 886 (Fed. Cir. 2004); *Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999); *Fintiv, Inc. v. PayPal Holdings, Inc.*, IPR2023-00744, paper 29 at 35 (construing claim term "performing one or more of a limit check and a velocity check" as "performing a limit check, a velocity check, or both a limit check and a velocity check"); *Apple, Inc. v. Evolved Wireless LLC*, IPR2016-01177, paper 27 at 9-10 ("Courts have not interpreted *SuperGuide* as setting forth a *per se* rule that the use of 'at least one of' followed by 'and' connotes a conjunctive list…courts have found *SuperGuide* inapplicable when the listed items following 'at least one of' are not categories containing many possible values"); APPLE-1003, ¶¶56-57.

Although similarly formulated claim language has sometimes been interpreted to require at least one of ***each*** item recited in the list, those cases are distinguishable at least because the listed items in those cases were categorical items containing many possible values, and the specific context of the claims and specifications in those cases made clear that at least one value from each listed category could be selected to fulfill the claimed criteria. *See, e.g.*, *SuperGuide*, 358 F.3d at 886-888. Here, by contrast, the recited first and second conductive-pattern layers are discrete items as opposed to categories from which values could be selected from each. APPLE-1003, ¶¶58-59. Indeed, it would be non-sensical to refer to at least one first conductive-pattern layer and at least one second

conductive-pattern layer because there is only one of each conductive-pattern layer. Any requirement for ***both*** the first and second conductive-pattern layers to include at least two layers of at least two different materials would also violate basic canons of construction by effectively rendering the phrase "at least one" of superfluous, especially since the claim drafter could have omitted those words to achieve the same meaning. *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.").

To be sure, the specification of the '207 patent also never demands two conductive-pattern layers that each have at least two layers of different materials, and such features are certainly not essential. APPLE-1003, ¶60. The applicant cited disclosure from the '207 patent specification during prosecution that allegedly provided support for amendments including the language in element [1h], but this disclosure never mentions any embodiment aligned with the narrow/conjunctive interpretation of element [1h]. *See* APPLE-1002, 172 (citing APPLE-1026, [0039] ("metal layer…***can*** naturally also include several metals as layers, accumulations, zones, or metal alloys")); APPLE-1003, ¶60; *supra*, §III.B. Accordingly, element [1h] only requires that one of the first or second conductive-pattern layers comprises at least two layers of at least two different materials. For example, based on Patent Owner's own allegations of infringement, element [1h]

would be anticipated or rendered obvious by prior art disclosure of two sub-layers of different materials in either first or second conductive-pattern layers.[3] APPLE-1105, 9-10; APPLE-1003, ¶¶56-61.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A – Nishiuma-Shibata Renders Obvious Claims 1-6

1. Nishiuma (APPLE-1004)

Nishiuma describes a "semiconductor integrated circuit device" formed as "a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, Abstract, 6:66-7:2; APPLE-1003, ¶¶64-66. As depicted in FIG. 1, Nishiuma's device includes surface wiring 3 and wiring lands 4 made of "thick films of refractory metal." APPLE-1004, 7:67-8:3. Gold (Au) balls 13 (not shown in FIG.1) are bonded to wiring lands 4 "using heat or ultrasonic energy or both" and flattened to form Au lands 14. *Id.*, 8:18-19, 8:28-29, 9:4-6.

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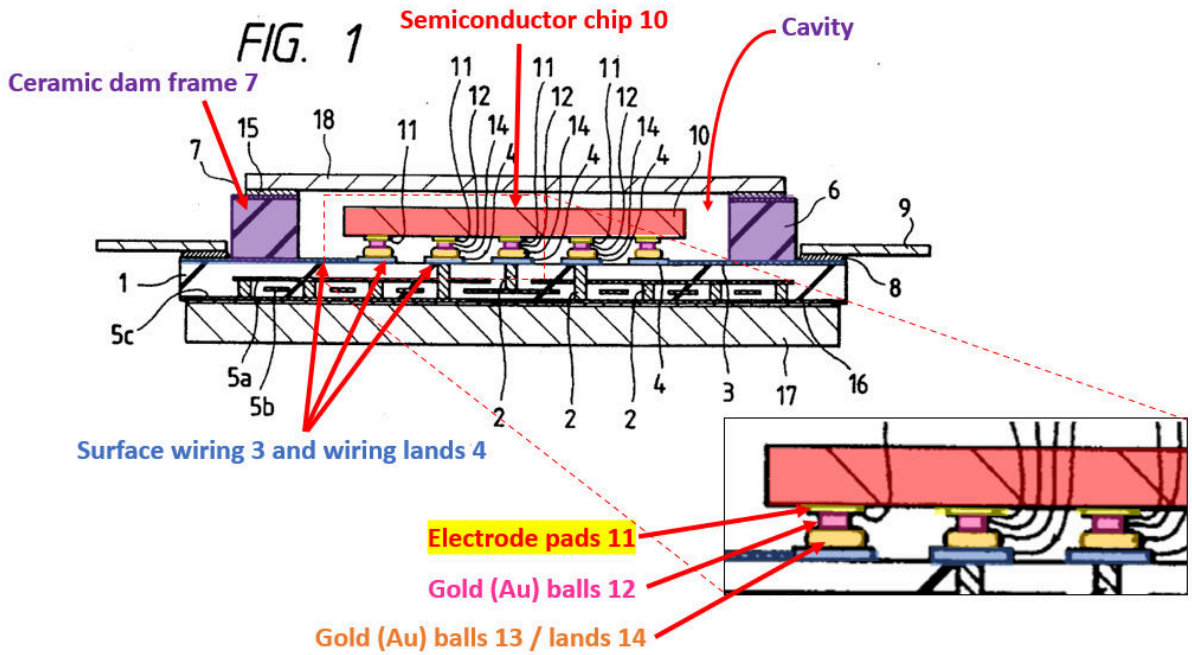
[3] Grounds 1A-2A confirm that the Challenged Claims would still have been obvious even if the narrower/conjunctive interpretation applied to require at least two layers of at least two different materials in both the first and second conductive-pattern layers. APPLE-1003, ¶61.



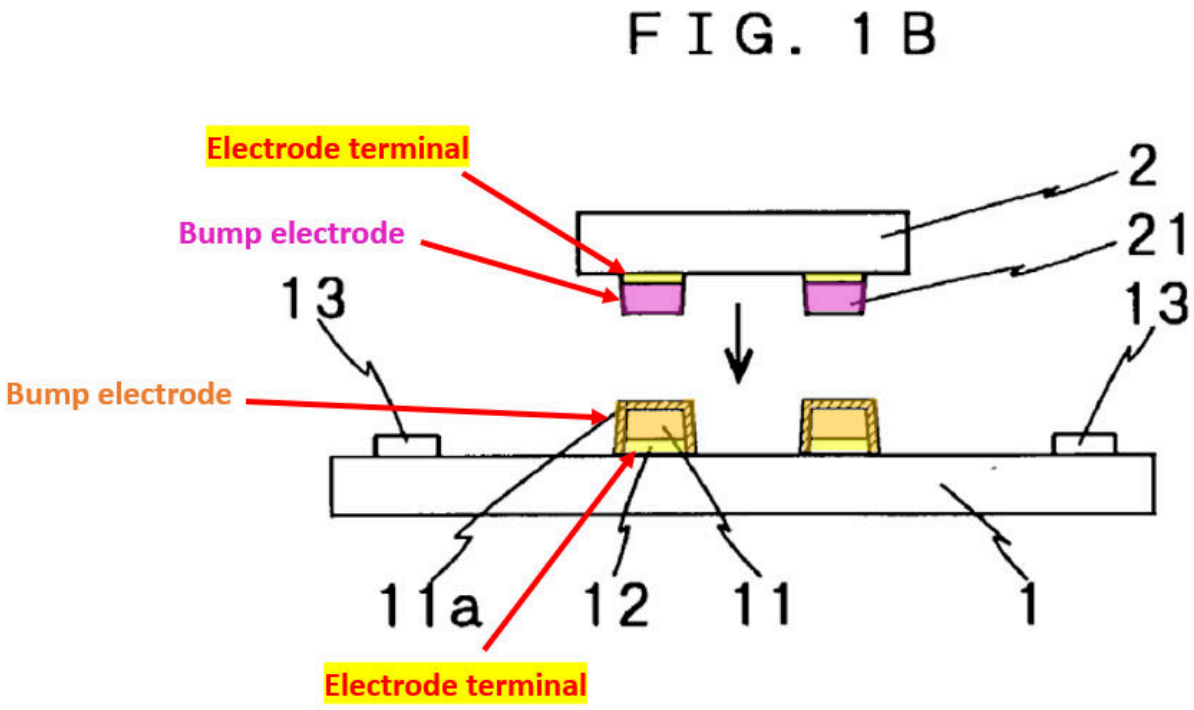
APPLE-1004, FIG. 1 (annotated and modified to include excerpt)

Nishiuma's "semiconductor chip 10" includes "electrode pads 11" that are "made of [gold] similarly to the integrated circuit wirings." APPLE-1004, 8:10-16. Au balls 12 are "bonded to the electrode pads 11 of the semiconductor chip 10" using "heat or ultrasonic energy or both" and are then bonded to Au lands 14 by "thermocompression bonding." *Id.*, 8:17-19, 9:13-16. Nishiuma's ceramic "square dam frame 6" "forms a cavity in which the semiconductor chip 10 is mounted." *Id.*, 7:48-54. Nishiuma's "cap 18" is bonded to "the frame 6 through a sealing metallize 7 and brazing filler metal 15." *Id.*, 7:51-55.

2. Shibata (APPLE-1005)

Shibata describes a method for coupling semiconductor chips using a bump electrode formed on an electrode terminal of the semiconductor chip. APPLE-

1005, [0011]; APPLE-1003, ¶¶67-69. Shibata's bump electrodes use metals with a low melting point to alloy metals inside the bump to prevent adverse effects from high temperature on the semiconductor elements. *Id.*



APPLE-1005, FIG. 1B (annotated)

Shibata's bump electrodes 11 and 21 are formed "on the electrode terminals 12 and 22 made of aluminum." *Id.*, [0052], FIG. 1C.

3. Nishiuma-Shibata Combination

Nishiuma discloses that the semiconductor chip includes electrode pads that provide contact zones for electrically connecting the semiconductor chip to the wiring board via bonds between Au lands on the wiring board and Au balls on the

electrode pads. *Supra*, § IV.A.1; APPLE-1004, 7:43-46. In one embodiment, "electrode pads 11 are made of Au similarly to the integrated circuit wirings." APPLE-1004, 8:13-16. Nishiuma does not limit the electrode pad materials , however, and suggests that metals besides Au would also be suitable for the integrated circuit wirings including for the Au balls. *Id.*, 17:15-18, 17:32-42, claims 1 and 15 (not limiting electrode pad material). In this context, a POSITA would have appreciated that other metals also would have been obvious to use with Nishiuma's electrode pads. APPLE-1003, ¶70.

Recognizing that semiconductor chips commonly included electrode pads formed from various materials, a POSITA would have turned to references like Shibata to investigate the use of alternate electrode pad materials. APPLE-1003, ¶71 (citing APPLE-1034, 1:15-18). Like Nishiuma, Shibata describes techniques for bonding the electrode pads of an electronic component to a structure using gold contact bumps—although Shibata expressly teaches that the electrode pads can be aluminum. APPLE-1005, [0059], [0051]-[0052]; *supra*, §IV.A.2. Multiple reasons would have motivated a POSITA to implement Nishiuma's electrode pads using aluminum in accordance with Shibata's teaching. APPLE-1004, 8:10-9:16, FIG. 1; APPLE-1005, [0052]; APPLE-1003, ¶72.

<u>First</u>, a POSITA would have been motivated to substitute aluminum, as Shibata suggests, for gold in the electrode pads because aluminum is ordinarily less

costly than gold. APPLE-1003, ¶73 (citing APPLE-1035, 138-139).

Second, a POSITA would have understood that the physical properties of aluminum, including its high electrical conductivity, low resistivity, and low coefficient of thermal expansion, make it well suited for use in electrode pads. APPLE-1003, ¶¶75-76; APPLE-1035, 124, 133.

Third, a POSITA would have been motivated to substitute aluminum for gold in the electrode pads because aluminum has properties which are superior to those of gold, including better conductivity, among others. APPLE-1003, ¶74.

Fourth, a POSITA would have understood that implementing electrode pads with aluminum in place of gold amounts to simple substitution of one known element for another to obtain predictable results, and indeed, would have been an obvious design choice to optimize the cost and performance of a particular design. APPLE-1003, ¶77. As described above, a POSITA would have appreciated that aluminum electrode pads were commonplace and substituting the electrode pad material to be aluminum instead of gold would have been straightforward to achieve a predictable result of a working electrode pad consistent with conventional electrode pads at the time. APPLE-1003, ¶¶77, 70-71. The ’207 patent itself merely lists aluminum as one of several “[p]possible” metals that would be suitable for a given design, identifying no particular benefits, challenges, or unpredictable results associated with the use of aluminum as compared to gold

or other metals. APPLE-1001, 6:58-59.

Fifth, coupling a device having aluminum electrode pads to a conductive layer using gold balls in the combination would have been obvious as a predictable application of a known technique as taught by Shibata to a known system as taught by Nishiuma to achieve entirely predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that "simply arranges old elements with each performing the same function it had been known to perform" is obvious); APPLE-1003, ¶78.

A POSITA would have reasonably expected success implementing a semiconductor chip with aluminum electrode pads in the Nishiuma-Shibata device as Shibata suggests, especially since aluminum was commonly used in electrode pads before the Critical Date. APPLE-1003, ¶¶79, 70-71. The similar types of semiconductor devices and constructions described in each of Nishiuma and Shibata underscores the predictability and obviousness of the combination. APPLE-1004, 2:60-67, 8:16-9:21; Figs. 1, 39; APPLE-1005, [0051]-[0052], FIG. 1B; APPLE-1003, ¶¶70-79. Indeed, Shibata confirms that conductive bumps, including gold bumps like those described in Nishiuma, need not be bonded only to gold electrode pads but can also be bonded to aluminum pads. *See* APPLE-1004, 8:17-19 ("Au balls 12 are bonded to the electrode pads 11 of the semiconductor chip 10"), 8:28-30, 9:4-6, 9:13-16, 8:13-16; APPLE-1005, [0051]

("[t]he respective bumps electrodes 11 and 21 of these first and second semiconductor chips 1 and 2 are both made of first metal such as Au"), [0052]; APPLE-1003, ¶¶80-81.

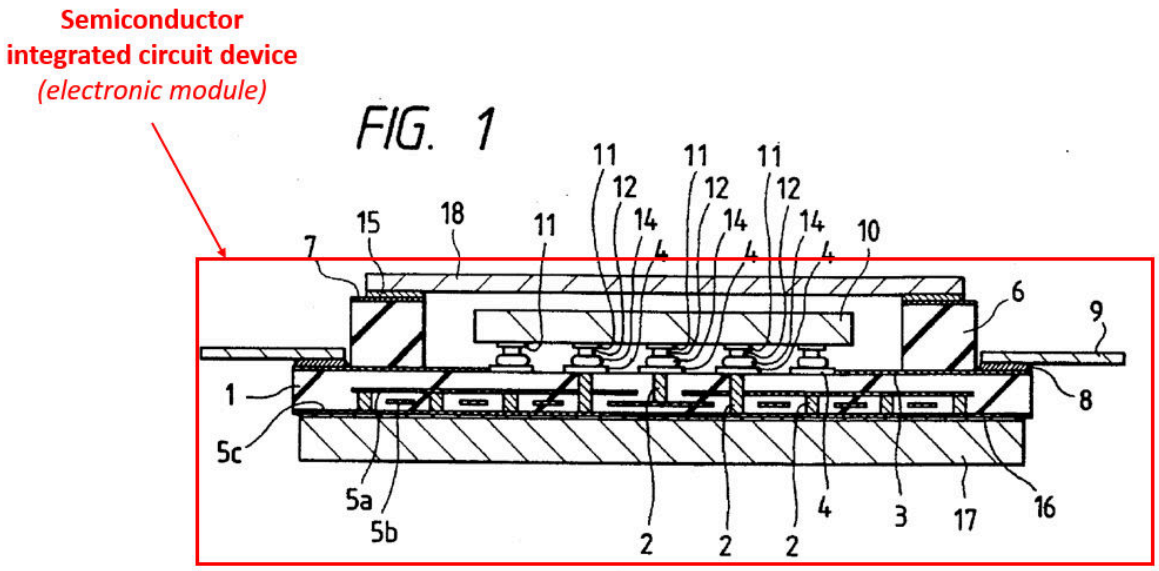
4. Analysis

a) Claim 1

[1.pre] An electronic module, comprising:

To the extent the preamble is limiting, Nishiuma-Shibata renders [1.pre] obvious. APPLE-1003, ¶¶82-83.

Nishiuma describes a semiconductor integrated circuit device that constitutes an "***electronic module.***" APPLE-1004, 1:11-17 ("a semiconductor integrated circuit device … and particularly [a] a technique for connecting a semiconductor chip to a printed wiring board"); *cf.* APPLE-1001, 1:24-31 ('207 patent describing that an electronic module "can be a module like a circuit board, which includes several components [such as] semiconductor components"). Nishiuma's FIG. 1 depicts that "the semiconductor integrated circuit device of this embodiment has a package structure fabricated by sealing a semiconductor chip 10 mounted on a wiring substrate 1 with a cap 18." APPLE-1004, 6:66-7:2; APPLE-1003, ¶¶82-83.



APPLE-1004, FIG. 1 (annotated)

[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;

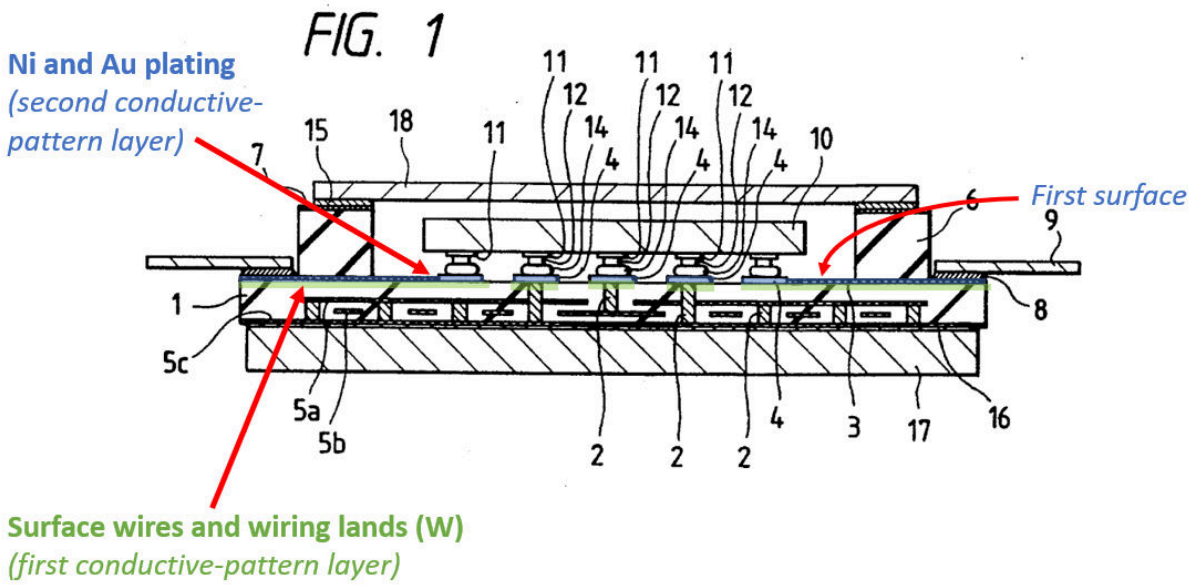
Nishiuma-Shibata discloses and renders obvious elements [1a]-[1b.ii]. APPLE-1003, ¶¶84-89. For example, Nishiuma's semiconductor device includes a "printed wiring board 1 [] made of ceramic such as alumina or aluminum nitride, on whose surface a plurality of surface wires 3 and a plurality of wiring 1 and electrodes 4 are formed." APPLE-1004, 7:7-10, 7:14-16, FIG. 1. Nishiuma further explains that the printed wiring board surface may include wiring lands 4. *Id.* Additionally, according to Nishiuma, "[t]he surfaces of the surface wiring 3 and wiring lands 4 are plated with Ni and Au … ." APPLE-1004, 7:14-16. The underlying surface wires 3 and wiring lands 4 collectively provide the claimed

"***first conductive-pattern layer***" while the Ni and Au plated on the surface wiring 3 and lands 4 collectively provide the claimed "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. APPLE-1003, ¶¶84-85; APPLE-1004, 7:14-16.

Indeed, it would have been obvious to a POSITA that the underlying surface wires 3 and wiring lands 4, described by Nishiuma as formed of the same materials and with the same screen-printing technique, cooperate as a conductive layer to transmit power and information signals. APPLE-1004, 7:16-18 ("The surface wirings 3 are wirings for input/output signals, GND, and power source, one end of each of wirings is connected to one of the wiring lands 4."), 7:11-14 ("surface wiring 3[and] lands 4 … are made of thick films of a refractory metal"), 7:66-8:3 ("surface wiring 3 and wiring land 4…are formed on the surface of the printed wiring board 1 by a known screen printing method"), 2:60-3:10; *cf.*, APPLE-1001, 6:52-59, 14:43-45 ('207 patent likewise describing layers comprised of multiple components); APPLE-1105 (Patent Owner's infringement charts identifying layers comprised of multiple components). Likewise, and similar to conductive coating layers described in the '207 patent, a POSITA would have understood that Nishiuma's Ni and Au plating collectively coat the surface wiring 3 and wiring lands 4, thereby forming a second conductive-pattern layer. APPLE-1001, 6:28-31 ('207 patent describing "surfaced" conductive layers for wiring similar to

Nishiuma's), 6:52-59 ('207 patent also describing layers comprised of multiple components); APPLE-1002, 170-173; *supra*, §III.B.

The top of the plated layer of Ni and Au provides the claimed "***first surface***" of the second conductive-pattern layer. APPLE-1004, 7:67-8:3 ("The surface wiring 3 and wiring land 4 of thick films of refractory metal such as W plated with Ni and Au are formed on the surface of the printed wiring board 1 by a known screen printing method."), 7:14-16 (describing an "order from the bottom" implying the existence of a top surface as a first surface); APPLE-1003, ¶¶85-86. The surface wires 3, wiring lands 4, and Ni and Au plating, being formed of conductive metals, are electrically conductive. APPLE-1003, ¶¶87-89. The dispersed arrangement of electrodes and discrete contact points provided by the surface wires 3 and wiring lands 4, and Ni and Au plating, form patterning in the conductive layer. *Id.*



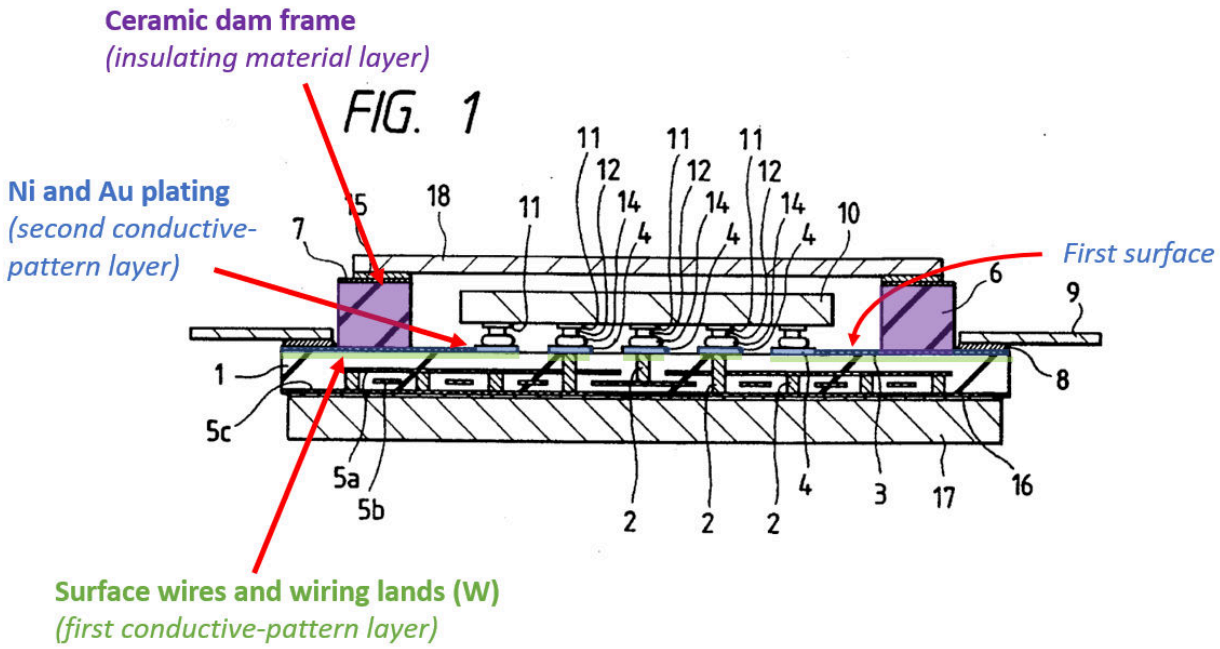
APPLE-1004, FIG. 1 (annotated[4])

[1c] an insulating-material layer disposed on the first surface of the second conductive-pattern layer;

Nishiuma-Shibata renders obvious element [1c]. APPLE-1003, ¶¶90-93. For example, Nishiuma describes that "[a] square dam frame 6 for sealing is formed around the semiconductor chip 10 on the wiring board 1." APPLE-1004, 7:48-49, 7:53-54, 8:5-9, FIGS. 2, 6. As shown in FIG. 1, the dam frame 6 is

[4] FIG. 1 does not specifically depict the plated Ni and Au over the surface wires 3 and wiring lands 4. The size and boundaries of the colorized areas are therefore exaggerated to emphasize the existence of two conductive-pattern layers as claimed consistent with the disclosure in Nishiuma. APPLE-1003, ¶¶85-86.

disposed on the first surface of the second conductive-pattern layer introduced in the analysis of elements [1a]-[1b.ii] above. APPLE-1003, ¶¶90-91.

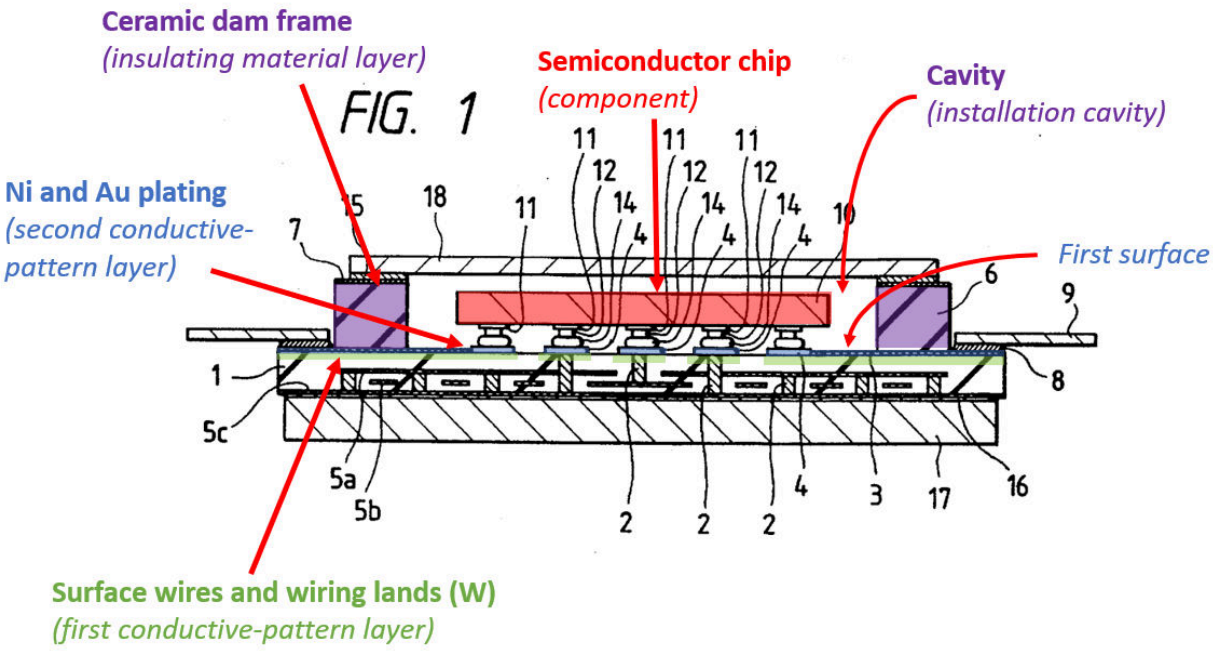


APPLE-1004, FIG. 1 (annotated)

Nishiuma further describes that "[t]he dam frame 6 is made of ceramic such as alumina or aluminum nitride," which a POSITA would have understood to be an electrical insulator, and which would have been obvious to implement as an insulator to prevent electrical signals from wiring 3 from conducting to other components contacted by dam frame 6 or causing undesirable electrical short circuiting. APPLE-1004, 7:49-51; APPLE-1003, ¶¶92-93 (citing APPLE-1010, 1:9-17 (describing ceramic as "a suitable electrically insulating material"); APPLE-1011, [0006] (describing chip carrier packages formed from ceramic and alumina insulators)).

[1d]-[1e.i] at least one installation cavity disposed in the insulating-material layer; a component disposed within the at least one installation cavity,

Nishiuma-Shibata renders obvious elements [1d]-[1e.i]. APPLE-1003, ¶¶94-95. For example, Nishiuma describes that "[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted." APPLE-1004, 7:53-54. As shown in FIG. 1, Nishiuma's device provides an "***installation cavity***" disposed within the dam frame (***insulating-material layer***) and a semiconductor chip (***component***) that is disposed within the cavity. *Id.*, 7:53-54, FIGS. 2-4, 6.



APPLE-1004, FIG. 1 (annotated)

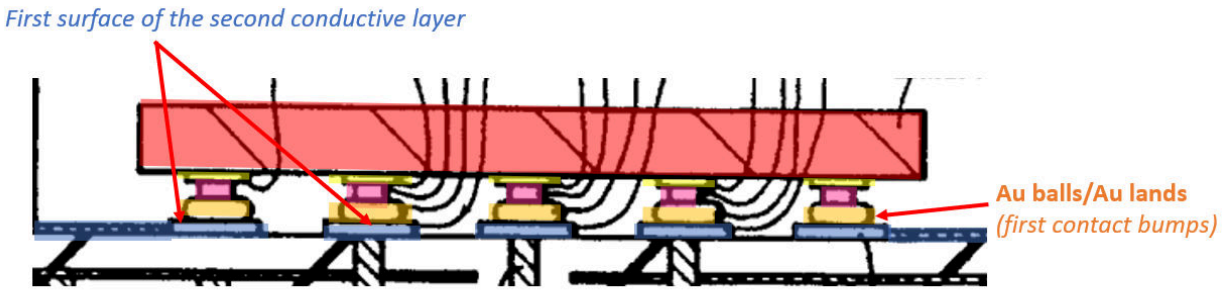
[1e.ii] the component comprising contact zones comprising aluminum;

Nishiuma-Shibata renders obvious element [1e.ii]. APPLE-1003, ¶¶96-97. For example, Nishiuma describes a semiconductor chip (***component***) that includes

electrode pads (***contact zones***) for forming electrical connections to external wiring. APPLE-1004, Abstract ("electrode pads of a semiconductor chip"), 7:2-6, 7:43-46, 8:13-16, FIGS. 1, 3-4. To the extent Nishiuma does not expressly disclose that the electrode pads include aluminum, Shibata teaches this conventional option. APPLE-1005, [0052] ("electrode terminals 12 and 22 made of aluminum"), [0011] ("semiconductor chip having an electrode terminal"), FIGS. 1A-1C. As described above, it would have been obvious and a POSITA would have been motivated to implement Nishiuma's electrode pads using aluminum as suggested by Shibata. *Supra* §IV.A.3 (Nishiuma-Shibata Combination); APPLE-1003, ¶¶96-97, 70-81.

[1f] first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and

Nishiuma-Shibata renders obvious element [1f]. APPLE-1003, ¶¶98-101. For example, Nishiuma describes that "Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1 … ." APPLE-1004, 8:28-29. After bonding the Au balls 13 to the wiring lands 4, "Au lands 14 are formed by pressing and flattening the Au balls 13 … ." *Id.*, 8:46-48. The Au balls 13 before pressing/flattening and/or Au lands 14 after pressing/flattening provide "***first contact bumps***" disposed on the first surface of the second conductive-pattern layer. APPLE-1003, ¶¶98-99.



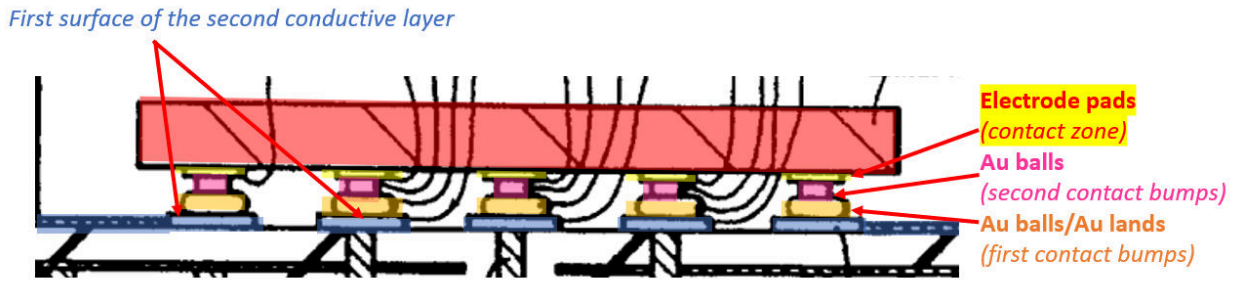
APPLE-1004, FIG. 1 (excerpted, annotated)

Nishiuma further discloses and renders obvoius that the Au balls 13 and Au lands 14 are electrically connected to the first surface of the second conductive-pattern layer (i.e., to the top surface of the plated Ni and Au over the surface wiring 3 and lands 4). APPLE-1003, ¶¶100-101, 84-89; *supra* §§IV.A.4.[1a]-[1b.ii]. For example, Nishiuma explains "[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding." APPLE-1004, 7:43-47; *see also id.*, 10:34-44; APPLE-1003, ¶101. A POSITA also would have understood and found obvious that an electrical connection would be formed by bonding the Au lands 14 to the coated wiring lands 4 since both are electrically conductive. APPLE-1003, ¶101.

[1g] second contact bumps disposed on the contact zones and electrically connected thereto,

Nishiuma-Shibata renders obvious element [1g]. APPLE-1003, ¶¶102-103. For example, Nishiuma describes "Au balls 12 having a diameter smaller than that

of the Au lands 14 [that] are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10." APPLE-1004, 7:41-43, 8:17-19. Au balls 12 provide "***second contact bumps***" disposed on the electrode pads 11 (***contact zones***) of the semiconductor chip. APPLE-1003, ¶102.



APPLE-1004, FIG. 1 (excerpted, annotated)

Nishiuma further teaches that "[t]he wiring lands 4 of the printed wiring board 1 is electrically connected to the electrode pads 11 of the semiconductor chip 10 by bonding the Au lands 14 to the Au balls 12 by a thermo-compression bonding." APPLE-1004, 7:41-47; *see also id.*, 8:17-27, 10:44-51, 10:57-11:8; APPLE-1003, ¶103. Au balls 12 are therefore electrically connected to the electrode pads. *Id.* A POSITA also would have understood and found obvious that an electrical connection would be formed by bonding the Au balls 12 to the electrode pads 11 since both are electrically conductive themselves. APPLE-1003, ¶¶102-103.

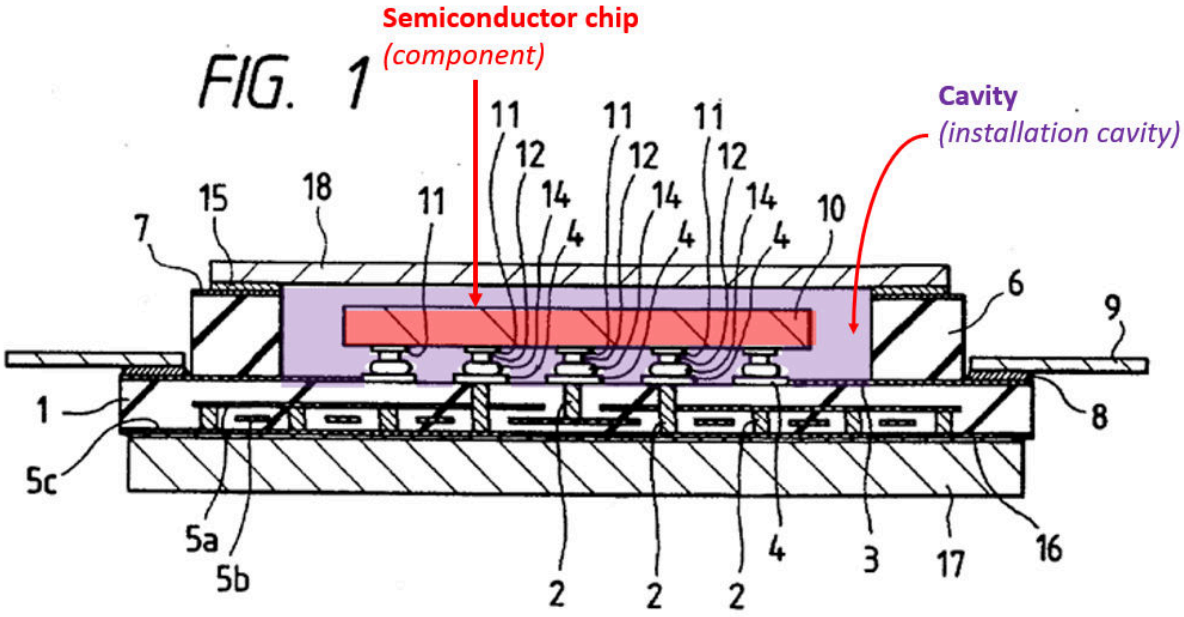
[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.

Nishiuma-Shibata renders obvious element [1h]. APPLE-1003, ¶104. For example, as discussed above, Nishiuma's underlying surface wires 3 and wiring lands 4 provide the claimed "***first conductive-pattern layer***" while the Ni and Au layers plated on the surface wires 3 and lands 4 provide the claimed "***second conductive-pattern layer***." *Supra*, §§IV.A.4.[1a]-[1b.ii]; APPLE-1003, ¶¶104, 84-89. The second conductive-pattern layer includes layers of "Ni and Au in the order from the bottom" and thus comprises two layers of at least two different materials: (1) a first layer of nickel and (2) a second layer of gold. APPLE-1004, 7:14-16; APPLE-1003, ¶104; *cf.*, APPLE-1001, 6:52-59 ('207 patent explaining that "items" such as a "metal layer" can include "several metals as layers"); *supra* §III.C.1.

b) Claim 2

[2] The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.

Nishiuma-Shibata renders obvious claim [2]. APPLE-1003, ¶¶105-107. For example, Nishiuma's FIG. 1 shows that the installation cavity can be thicker than the component. APPLE-1004, FIG. 1; *see also id.*, 7:54-55, claim 2; APPLE-1003, ¶¶105-107.

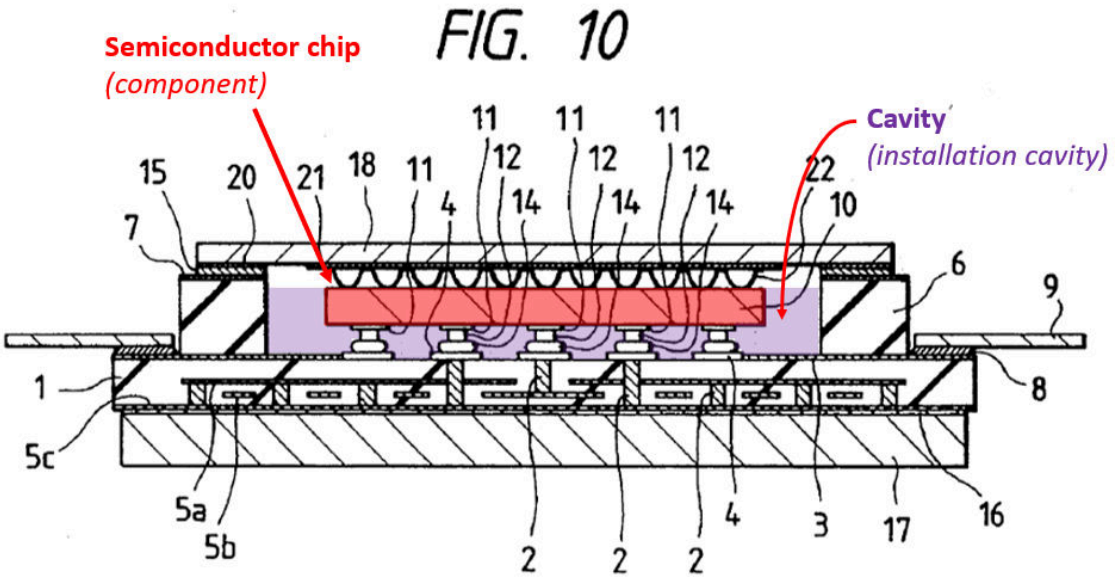


APPLE-1004, FIG. 1 (annotated)

c) Claim 3

[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.

Nishiuma-Shibata renders obvious claim [3]. APPLE-1003, ¶¶108-112. For example, Nishiuma's FIG. 10 embodiment shows that the thickness of the installation cavity can be reduced to match the thickness of the semiconductor chip (***component***) by providing a "a heat conductive media of Au ribbons 22 … in the space between the back of [the] semiconductor chip 10 … and the bottom of a cap 18 to cool the semiconductor chip 10 by conducting heat through the cap." APPLE-1004, 11:19-25; *see also id.*, 11:26-41.



APPLE-1004, FIG. 10 (annotated)

Nishiuma's disclosure aligns with similar descriptions in the '207 patent, which relates component thickness to the height of the component *after installation in the cavity*. APPLE-1003, ¶¶106, 109. To this point, the specification focuses on the component's *protrusion* beyond the height or thickness of the installation cavity as installed as opposed to the absolute thickness of the component in isolation before installation. *See, e.g.*, APPLE-1001, 7:61-8:5. For example, the specification describes how a thickness of the component as installed may be less than, equal to, or greater a thickness of the installation cavity such that the component may or may not protrude from the cavity. APPLE-1001, 6:8-17; APPLE-1003, ¶¶106, 111. Comparing a thickness of the component to the thickness of the installation cavity to assess protrusion, as discussed in the

specification, is non-sensical when other structures such as contact bumps also exist in the cavity after the component is mounted. APPLE-1003, ¶109. Further, while the '207 patent does not define a tolerance for the "about" modifier in claim 3, it indicates that the thicknesses of the component and installation cavity need not be exactly the same. A POSITA would have understood that a component whose absolute thickness before installation is slightly less than the cavity thickness to accommodate a thickness of contact bumps and similar structures like Nishiuma's thin Au ribbon would still be about equal to the thickness of the cavity since the component otherwise fills the thickness of the cavity without protruding from the cavity. APPLE-1003, ¶109.

Even in embodiments that lack Au ribbon 22, Nishiuma confirms that the space between the semiconductor chip 10 and cap 18 can be narrowed relative to the space provided in FIG. 1. APPLE-1003, ¶¶109-110. For example, Nishiuma discloses the option of stacking an additional Au ball between the contact pads 11 of chip 10 and wiring lands 4, thereby increasing the installed thickness of the chip 10 and reducing the amount of space between chip 10 and cap 18. APPLE-1004, 10:57-11:18, FIG. 9 (showing space between semiconductor chip 10 and cap 18 narrowed relative to the space in FIG. 1 that lacks the additional Au ball). These configurations in which the space is narrowed between chip 10 and cap 18 demonstrate that Nishiuma does not restrict the installed thickness of the

semiconductor chip relative to the thickness of the installation cavity, nor does Nishiuma define any critical/minimum gap that must be maintained between the top of the chip and the bottom of the cap. APPLE-1003, ¶110.

The ’207 patent similarly discloses nothing critical or unexpected about the thickness of the installation cavity being about equal to the thickness of the component, but rather confirms that thinner, equally thick, or thicker components are all suitable options. APPLE-1001, 7:58-8:5, 6:8-16; APPLE-1003, ¶111. The ’207 patent also does not define any specific tolerance or range imparted by the modifier “about” in the claim phrase “about equal thickness.” APPLE-1003, ¶111. Nishiuma thus discloses the same general conditions for a cavity with *about* equal thickness as the component as the ’207 patent itself, which renders the additional feature recited in claim 3 obvious. *E.I. du Pont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) (“‘where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation’”). Indeed, it is settled law that a claimed range such as the “about equal thickness” of claim 3 is obvious both when the prior art range overlaps and even when it does not in the absence of criticality or unexpected results. *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003); MPEP § 2144.05. Selecting a relative thickness of the component and cavity in Nishiuma-Shibata would have been a simple matter of design choice, and an about equal

thickness would predictably be achieved through routine experimentation, e.g., to optimize component stability, minimize device size, minimize wire bond length, and/or optimize heat dissipation. APPLE-1003, ¶112 (citing APPLE-1010, 1:49-51, 2:64-3:1; APPLE-1011, [0034], [0017], [0038], [0044], FIG. 4).

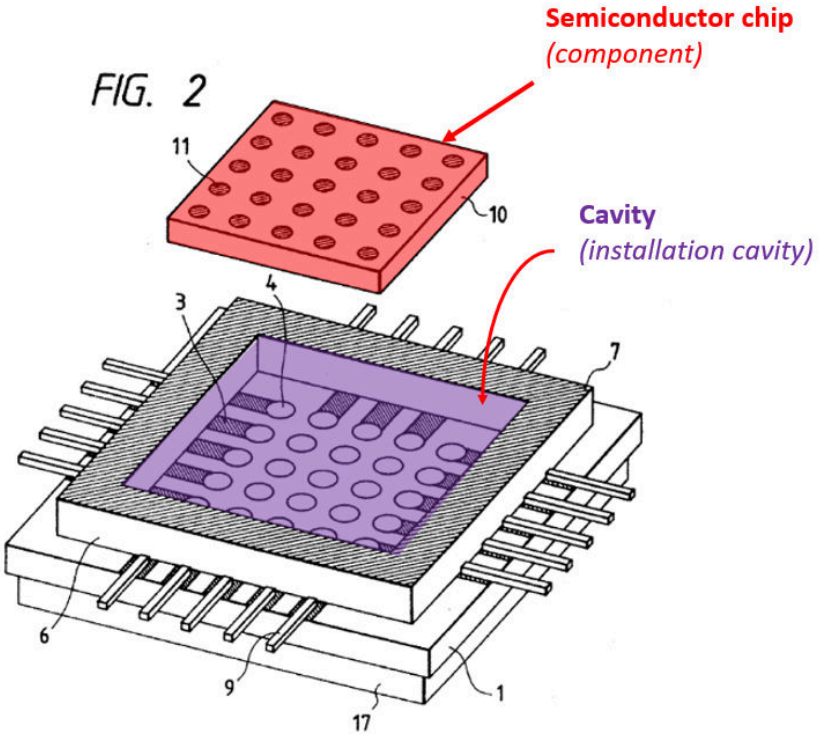
d) Claim 4

[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.

Nishiuma-Shibata renders obvious claim [4]. APPLE-1003, ¶¶113-116. As an initial matter and as described above with regard to claim [3], Nishiuma discloses and renders obvious an installation cavity that has about equal thickness as the semiconductor chip (component). *Supra*, §IV.A.4.[3]; APPLE-1003, ¶¶113, 108-112. When the thickness of Nishiuma's installation cavity has about the same thickness as the component, it is also dimensioned to the size of the component at least in the vertical dimension (thickness). APPLE-1003, ¶113. Claim [4] is thus rendered obvious for at least the same reasons to those described above with regard to claim [3]. *Id.*

Moreover, Nishiuma's FIG. 2 shows that not only is the thickness of the cavity dimensioned to the size of the component, but so too are its length and width. APPLE-1004, FIG. 2; *see also id.*, FIGS. 3-4, 6; APPLE-1003, ¶114. In particular, the length and width of Nishiuma's cavity are dimensioned to

accommodate the footprint of the semiconductor chip, and the length and width of the cavity bear a clear relationship to the length and width of the semiconductor chip. APPLE-1003, ¶¶114-115. Dr. Baker also explains that a POSITA would have understood that sizing the cavity to the component to be fit into the cavity had numerous benefits, including requiring shorter wire bond lengths to minimize parasitic effects and to provide a tighter fit of the component in the cavity. APPLE-1003, ¶116 (citing APPLE-1011, [0017], [0034]; APPLE-1010, 1:49-51, 2:64-3:1; APPLE-1007, [0002]).



APPLE-1004, FIG. 2 (annotated)

e) Claim 5

[5] The electronic module of claim 1, wherein the first contact bumps comprise tin.

Nishiuma-Shibata renders obvious claim [5]. APPLE-1003, ¶¶117-120. As described above, Nishiuma describes "Au balls 13 are bonded to the wiring lands 4 of the printed wiring board 1" and are later flattened into Au lands 14. APPLE-1004, 8:28-48. To the extent Nishiuma does not explicitly describe that the first contact bumps comprise tin, Shibata describes "an Sn coating is provided on the surface of an Au bump electrode." APPLE-1005, [0038]; APPLE-1003, ¶117. Shibata explains that the addition of a tin coating to a gold bump electrode is beneficial to the bonding process, describing "[a]n Sn coating 11*a* is provided on the bump electrode 11 made of Au, so that at around a temperature of 230° C., Sn with a melting point of 232° C. or so melts to be alloyed with Au having a melting point of 1064° C. to thereby provide an eutectic alloy and, at around a temperature of 280° C., an alloy layer 3 made of an Au—Sn alloy is formed on the joining surface to permit both the bump electrode 11 and 21 to be melt-adhered to each other." APPLE-1005, [0053]; APPLE-1003, ¶117.

It would have been obvious to a POSITA to implement Nishiuma's Au balls 13 or lands 14 (***first contact bumps***) with a coating of tin to form an alloy that would promote improved bonding with the Au balls of the component (which can

also optionally be coated with tin in Nishiuma-Shibata). APPLE-1005, [0053]; APPLE-1004, 9:13-16, 8:17-19, 8:28-29, 17:19-23; APPLE-1003, ¶¶118-120. A POSITA would have considered the selection of tin to be an obvious design choice and would have been motivated to provide tin in Nishiuma's Au balls 13/Au lands 14 to enable formation of a eutectic Au-Sn alloy and promote bonding as expressly described in Shibata. APPLE-1005, [0053]; APPLE-1003, ¶¶118-120. A POSITA would have reasonably expected success in making the combination at least because the addition of tin to an Au ball would have been well within the skill of a POSITA and because of the similarities between Nishiuma and Shibata's methods in which tin would be applied to coat the same material (Au) in the combination as it is applied in Shibata. *See supra* §IV.A.3 (Nishiuma-Shibata Combination); APPLE-1003, ¶¶120, 70-81.

f) Claim 6

[6] The electronic module of claim 1, wherein the second contact bumps comprise copper.

Nishiuma-Shibata renders obvious claim [6]. APPLE-1003, ¶¶121-125. As described above, Nishiuma describes Au balls 12 (***second contact bumps***) "having a diameter smaller than that of the Au lands 14 are bonded to the electrode pads 11 on the element forming surface of the semiconductor chip 10." APPLE-1004, 7:41-43, 8:17-19. Nishiuma does not explicitly describe its second contact bumps

(e.g., balls 12) include copper, but a POSITA would have recognized that the use of copper in second contact bumps like Nishiuma's was a conventional option before the Critical Date of the '207 patent. APPLE-1003, ¶121. For example, Shibata teaches that "bump electrodes 11 and 21 [can be] made of Au, Cu, etc. respectively." APPLE-1005, [0052]. Nishiuma also invites the use of metals in addition to Au to form the balls 12 bonded to electrode pads 11. APPLE-1004, 2:60-64 ("according to the present invention a metal formed of metal other than Pb such as Au is formed using a ball bonding method onto an electrode pad …").

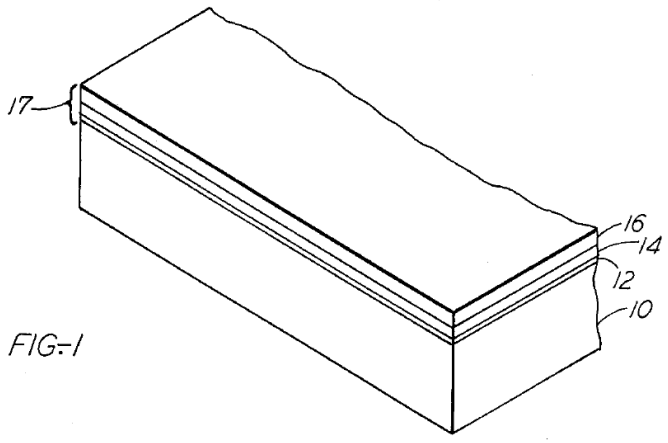
A POSITA would have been motivated to implement Nishiuma's second contact bumps (e.g., balls 12) using copper with or in addition to gold in accordance with Shibata's teaching to provide an advantageously low resistive drop between the component and circuit board. APPLE-1003, ¶¶121-124 (citing APPLE-1012, 152-154). Accordingly, a POSITA would have considered the selection of copper to be an obvious design choice and would have been motivated to implement Nishiuma-Shibata's semiconductor integrated circuit device with second contact bumps including copper, per Shibata, to achieve the low resistive drop between component and circuit board when they are bonded together. APPLE-1005, [0052]; APPLE-1003, ¶¶124-125. A POSITA would have reasonably expected success making the combination at least because the use of copper in electrodes and contact bumps was well-established before the Critical

Date. *See supra* §IV.A.3 (Nishiuma-Shibata Combination); APPLE-1003, ¶¶125, 70-81.

B. GROUND 1B – Nishiuma-Shibata-Glick Renders Obvious Claims 1-6

1. Glick (APPLE-1020)

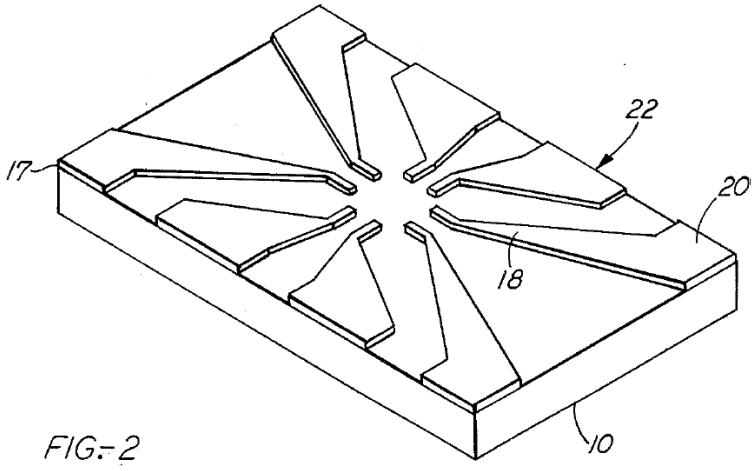
Glick describes a method "for strengthening bonds between thin-film conductors and insulating substrates on which they are formed." APPLE-1020, 1:6-10; APPLE-1003, ¶¶126-128. Glick describes that in FIG. 1, "[a] layer of titanium 12 is first deposited on the substrate 10… [n]ext a layer of palladium 14 is deposited on the titanium… [and f]inally, a layer of gold 16 is plated over the palladium." APPLE-1020, 2:56-66, 1:63-66.



APPLE-1020, FIG. 1

"If it is desired to reduce the amount of gold, copper may be substituted for most of the gold, i.e., the gold layer may be replaced by a layer of copper plated

with gold." *Id.*, 2:67-3:2. A nickel layer can be used to prevent diffusion of the copper through the gold leading to oxidation of the bonding surface, such that "a conductor layer which includes copper would consist of titanium and palladium sequentially evaporated on the substrate and then copper, nickel, and gold sequentially plated on the palladium." *Id.*, 3:6-11.



APPLE-1020, FIG. 2

Following preparation of the composite conductive layers, "film 17 is formed into a pattern 22 of individual conductors 18 and contact pads 20." *Id.*, 3:12-16, FIG. 2.

2. Nishiuma-Shibata-Glick Combination

Nishiuma discloses that "[t]he surfaces of the surface wiring 3 and wiring

lands 4 are plated with Ni and Au in the order from the bottom." APPLE-1004, 7:14-16. A POSITA would have understood that conductive patterns, such as Nishiuma's surface wiring and wiring lands, may be plated for a variety of reasons, including to prevent oxidation and improve adherence and conductivity, and that the plating materials are not limited to Ni and Au. APPLE-1003, ¶129. In this context, a POSITA would have appreciated that additional material layers would have been obvious to implement in Nishiuma's wiring and lands. APPLE-1003, ¶129.

Recognizing that having multiple materials coating wiring and lands, a POSITA would have turned to references, like Glick, that describe preparing a conductive pattern from multiple layers of materials. APPLE-1020, 2:56-3:11; APPLE-1003, ¶130. Like Nishiuma, Glick describes coating conductive patterns with layers of materials, including nickel and gold, although Glick describes additional layers to the conductive patterns to improve adherence and reduce costs. APPLE-1020, 2:52-3:11; APPLE-1003, ¶¶130, 126-128; *supra*, § IV.B.1. Multiple reasons would have motivated a POSITA to implement Nishiuma's conductive surface wiring and lands in accordance with Glick's suggestion. APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:11; APPLE-1003, ¶¶130-135.

First, a POSITA would have been motivated to implement Nishiuma's surface wiring and lands with additional layers of material forming the wiring and

lands themselves, as Glick suggests, to improve the adherence of the wiring and lands to the underlying substrate. APPLE-1003, ¶131; APPLE-1020, 2:56-60, 1:50-57, Abstract.

Second, a POSITA would have understood that the use of gold in a conductive pattern may be costly and would have been motivated to implement the surface wiring and lands with additional material layers to decrease manufacturing and processing costs, for example, including layers of copper, nickel, and gold to minimize the amount of gold needed for the plating of the surface wiring. APPLE-1020, 2:67-3:11; APPLE-1003, ¶132 (citing APPLE-1035).

A POSITA would have reasonably expected success implementing Nishiuma's surface wiring and lands with additional material layers as Glick suggests for a variety of reasons, including all the reasons described above and given that the layered conductor structure taught by Glick is complementary to the layers described by Nishiuma. APPLE-1003, ¶¶133-135 (explaining that both Nishiuma and Glick provide examples in which a top layer of the wiring is gold); APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:11, FIGS. 1-2.

Additionally, a POSITA would have understood that implementing additional conductive material layers on a surface wiring and wiring lands in the combination would have been obvious as a predictable application of a known technique of implementing multiple conductive layers as taught by Glick to a

known system as taught by Nishiuma to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶135.

3. Analysis

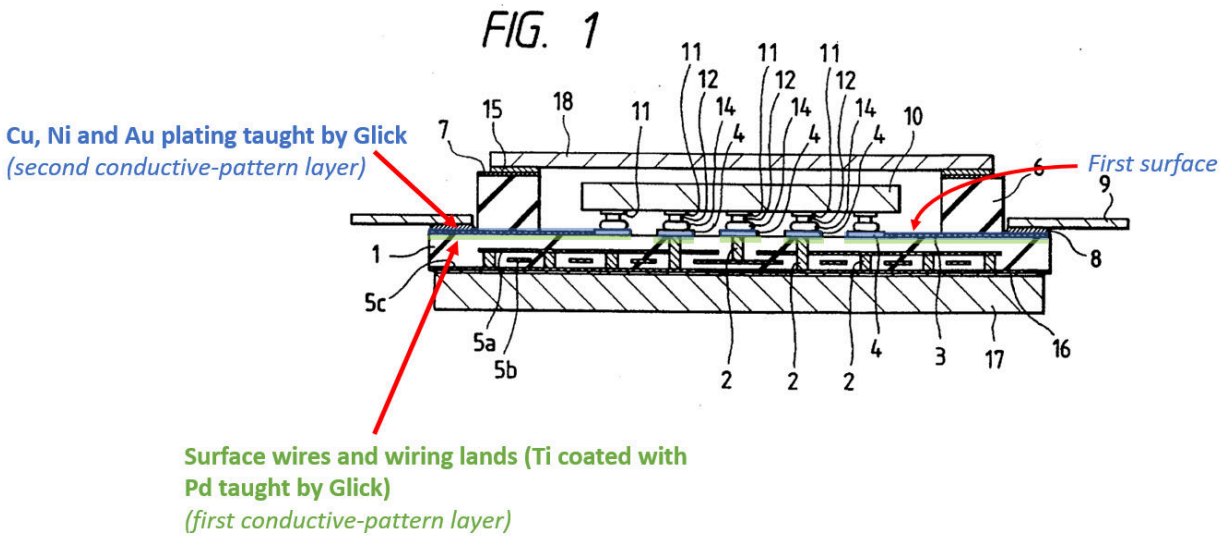
a) Claim 1

[1.pre]

See supra §IV.A.4.[1pre]; APPLE-1003, ¶¶136, 82-83.

[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;

Nishiuma-Shibata-Glick discloses and renders obvious elements [1a]-[1b.ii]. APPLE-1003, ¶¶137-139. For example, as described above, Nishiuma's surface wires and lands provide the "***first conductive-pattern layer***" and one or more coatings of the surface wires/lands provide the "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. APPLE-1003, ¶¶137, 84-89; *supra*, Ground 1A, [1a]. In Nishiuma-Shibata-Glick, the surface wires and lands are formed from multiple material layers including titanium and palladium (***first conductive-pattern layer***) which are further coated in copper, nickel and gold (***second conductive-pattern layer***). APPLE-1004, 7:7-10, 7:14-16; APPLE-1020, 2:56-3:20, Figs. 1-2; APPLE-1003, ¶¶138-139.



APPLE-1004, FIG. 1 (annotated)

Accordingly, in Nishiuma-Shibata-Glick, Nishiuma's surface wires and lands are formed from layers of titanium and palladium (second conductive-pattern layer) and are plated in layers of copper, nickel, and gold (first conductive-pattern layer). *Supra* §IV.B.2; APPLE-1020, 2:52-3:20; APPLE-1004, 7:7-16; APPLE-1003, ¶¶137-139, 129-135.

[1c]-[1e.i]

See supra §§IV.A.4.[1c]-[1e.i]; APPLE-1003, ¶¶140, 90-95. In Nishiuma-Shibata-Glick, the ceramic dam frame (***insulating-material layer***) is disposed on the first surface of the layered surface wiring and lands (***second conductive-pattern layer***). APPLE-1003, ¶¶140, 129-135.

[1e.ii]-[1g]

See supra §§IV.A.4.[1e.ii]-[1g]; APPLE-1003, ¶¶141, 96-103. In Nishiuma-Shibata-Glick, the Au balls/lands (***first contact bumps***) are formed on the ***first surface*** of the layered surface wiring and lands (***second conductive-pattern layer***). APPLE-1003, ¶¶141, 129-135.

[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.

Nishiuma-Shibata-Glick renders obvious element [1h]. APPLE-1003, ¶¶142-143, 137-139*; supra* §§IV.B.3.[1a]-[1b.ii]. For example, as discussed above, in Nishiuma-Shibata-Glick, surface wires and lands comprising titanium and palladium (collectively the "***first conductive-pattern layer***") are plated in copper, nickel, and gold (collectively the "***second conductive-pattern layer***"). APPLE-1004, 7:7-16; APPLE-1020, 2:52-3:20; APPLE-1003, ¶¶142. The surface wiring and lands layer (***first conductive-pattern layer***) has two sublayers that each comprises a different material: (1) titanium and (2) palladium, and the coating (***second conductive-pattern layer***) has three layers that each comprise a different material: (1) copper, (2) nickel, and (3) gold. *Supra* §IV.B.2; §III.C.1; APPLE-1020, 2:52-3:20; APPLE-1003, ¶¶142, 129-135.

Accordingly, both the surface wiring and lands (***second conductive-pattern layer***) and the plated metal layers formed on the wiring/lands (***first conductive***

pattern layer) includes ***at least two layers of at least two different materials*** in the Nishiuma-Shibata-Glick combination, thus meeting the second interpretation of limitation [1e]. APPLE-1004, 7:14-16; APPLE-1020, 2:52-3:11; APPLE-1003, ¶¶142-143, 56-61.

b) Claims 2-6

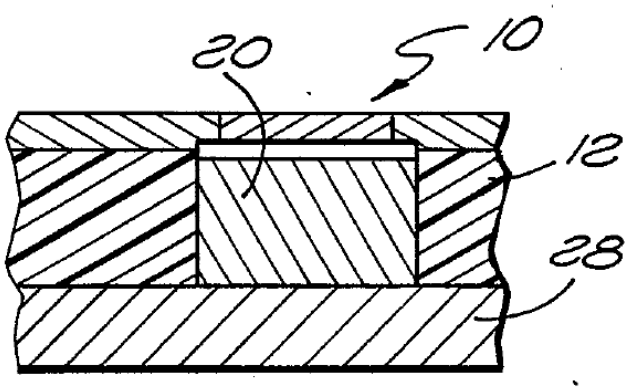
See supra §§IV.A.4.[2]-[6]; APPLE-1003, ¶¶144, 105-125.

C. GROUND 1C – Nishiuma-Shibata-Parker Renders Obvious Claims 3-4

1. Parker (APPLE-1010)

Parker describes "methods of making printed circuit boards having grooves for receiving electrical leads and cavities for receiving electrical components." APPLE-1010, 1:6-8; APPLE-1003, ¶¶145-147.

Parker describes that a punch can be used to "[c]avities … provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities." *Id.*, 1:49-51, 2:64-3:9; 2:5-27; 4:3-19, 1:10-12.

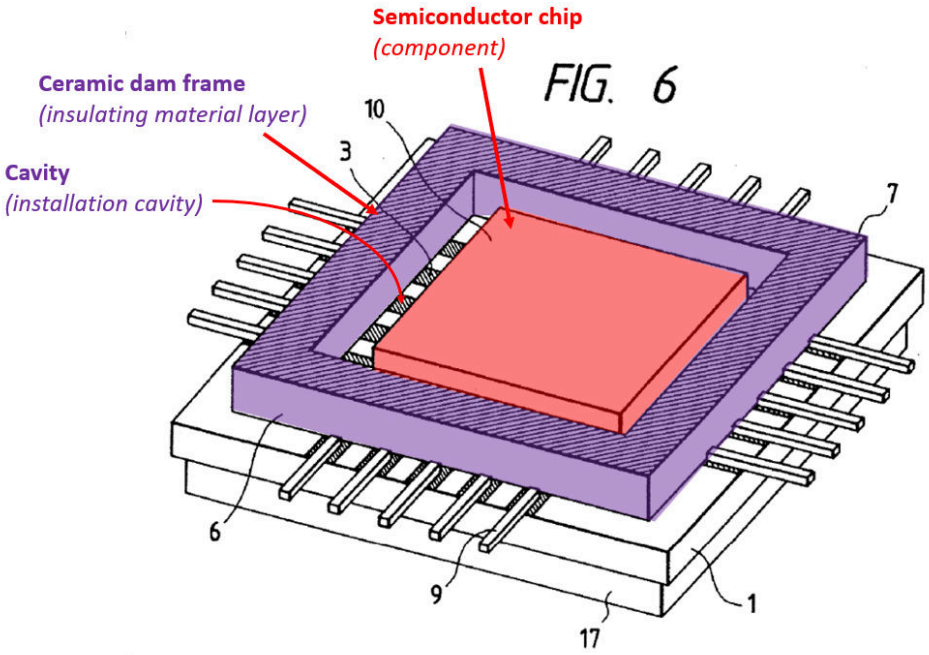


APPLE-1010, FIG. 2

For example, in FIG. 2, a transistor 20 is positioned within a cavity formed in the substrate 12 of the printed circuit board 10. *Id.*, 3:18-22.

2. Nishiuma-Shibata-Parker Combination

Nishiuma describes that "[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted." APPLE-1004, 7:53-54. Nishiuma's FIG. 6 illustrates that the sealing dam frame 6 forms a cavity sized to accept the semiconductor chip 10 within. *Id.*, FIGS. 1, 2, 6, 10.



APPLE-1004, FIG. 6 (annotated)

A POSITA would have understood that a cavity is sized to fit the device intended to be mounted therein and would have further understood that there are a variety of ways to size the cavity to the device. APPLE-1003, ¶¶148-149 (citing APPLE-1011, [0034], [0017], [0038], [0044], FIG. 4). In this context, a POSITA

would have turned to references like Parker that describe sizing considerations for a cavity. APPLE-1003, ¶¶148-149.

For example, Parker describes "[c]avities 18 are [] provided in one or both of the parallel surfaces of the substrate 12" of the printed circuit board. APPLE-1010, 2:64-65, FIG. 2. "Electrical components are adapted to be disposed in the cavities 18, preferably in a tight fit with the walls of the cavities." *Id.*, 2:66-3:1; APPLE-1003, ¶150. Like Nishiuma, Parker describes mounting a device within a circuit board cavity and provides additional cavity sizing guidance. APPLE-1003, ¶150. Multiple reasons would have motivated a POSITA to implement Nishiuma's cavity to be sized to the dimensions of the component in accordance with Parker's suggestion. APPLE-1010, 1:49-51, 2:64-3:1, FIG. 2; APPLE-1003, ¶¶148-157.

First, a POSITA would have understood that sizing the cavity to have a tight fit with the component optimizes the use of limited space on the printed circuit board. APPLE-1003, ¶¶152, 22-36 (citing APPLE-1007, [0002]; APPLE-1011, [0034]).

Second, to the extent that components are connected to the printed circuit board by wires in addition to contact bumps, positioning a component in a cavity with a tight fit requires shorter wire bond lengths and reduces parasitic effects. APPLE-1010, [0017]; APPLE-1004, 1:18-33 (describing benefits to operating speed with shorter wiring length); APPLE-1003, ¶153.

Third, a POSITA would have understood that a tight fit between the cavity and the component allows for the component to be easily placed in proper position within the cavity to provide electrical connection between the component and wiring in the cavity. APPLE-1003, ¶154 (citing APPLE-1011, [0006]); APPLE-1010, 3:654:2; APPLE-1004, 2:34-50.

Fourth, a POSITA would have appreciated that there are a limited number of possible size relationships between a cavity and a component sized to fit in the cavity. APPLE-1003, ¶155; APPLE-1001, 6:7-16 (describing that the installation base can be thicker than, less thick than, or equally thick as the component). A POSITA would have found it obvious to try these finite and predictable solutions to sizing the cavity relative to the component and would have had a reasonable expectation of success in implementing them, given that these are conventional methods for mounting a component within a cavity. APPLE-1003, ¶¶155-156.

A POSITA would have had a reasonable expectation of success implementing the combination for all the reasons described above and given that Parker describes techniques for disposing components on a printed wiring board and within a cavity, like Nishiuma. APPLE-1004, 7:7-55; APPLE-1010, 1:49-51, 2:5-27, 2:64-3:22; APPLE-1003, ¶¶157, 145-147. Implementing a semiconductor integrated circuit with a cavity that has a tight fit to the component would have been obvious as a predictable application of a known technique for positioning

components in a printed circuit board as taught by Parker to a known system as taught by Nishiuma to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶¶148-157.

3. Analysis

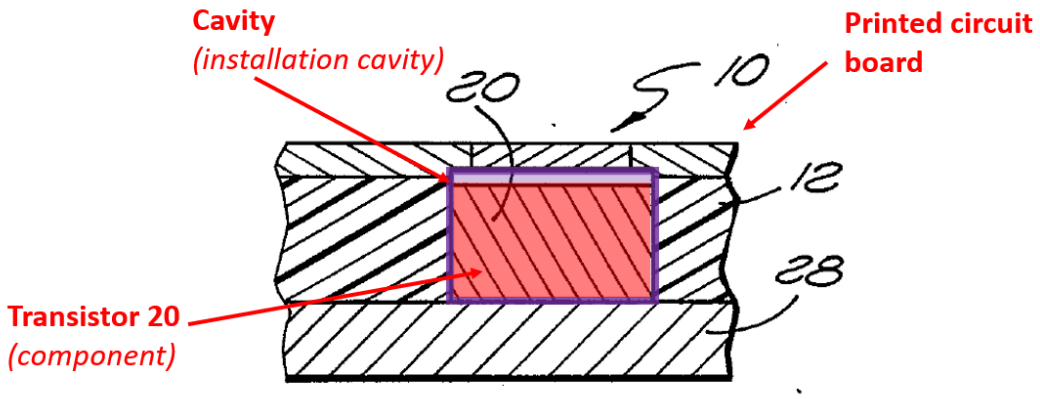
a) Claim 3

[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.

Nishiuma-Shibata-Parker renders obvious claim [3]. APPLE-1003, ¶¶158-160, 109. For example, "[t]he sealing dam frame 6 forms a cavity in which the semiconductor chip 10 is mounted." APPLE-1004, 7:53-54. To the extent Nishiuma does not expressly disclose an installation cavity of equal thickness as the component, Parker teaches this conventional option, and it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nishiuma's cavity and device with the sizing relationship suggested by Parker. *Supra* §IV.D.2; APPLE-1010, 1:49-51 ("[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities"), 2:64-3:9; 3:18-22; APPLE-1004, FIGS. 1, 9, 10; APPLE-1003, ¶¶158-159 (citing APPLE-1011, [0034], [0017], [0038]-[0044], FIG. 4).

As shown in Parker's FIG. 2, the ***cavity*** formed in the printed circuit board (purple box) ***has about equal thickness*** as the transistor 20 ("***component***"). *Id.*,

APPLE-1003, ¶160.



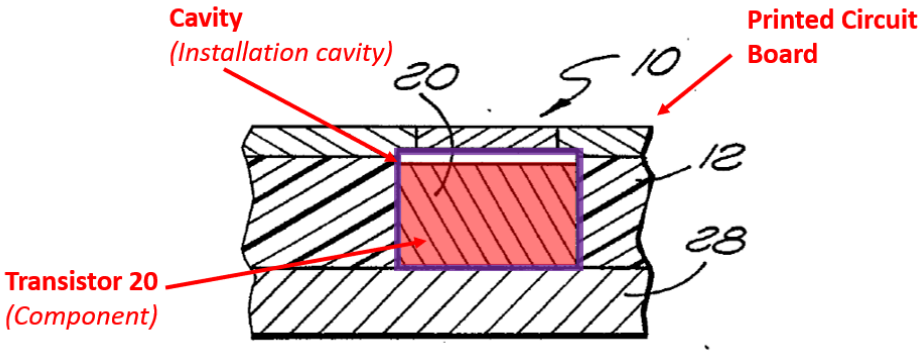
APPLE-1010, FIG. 2 (annotated)

b) Claim 4

[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.

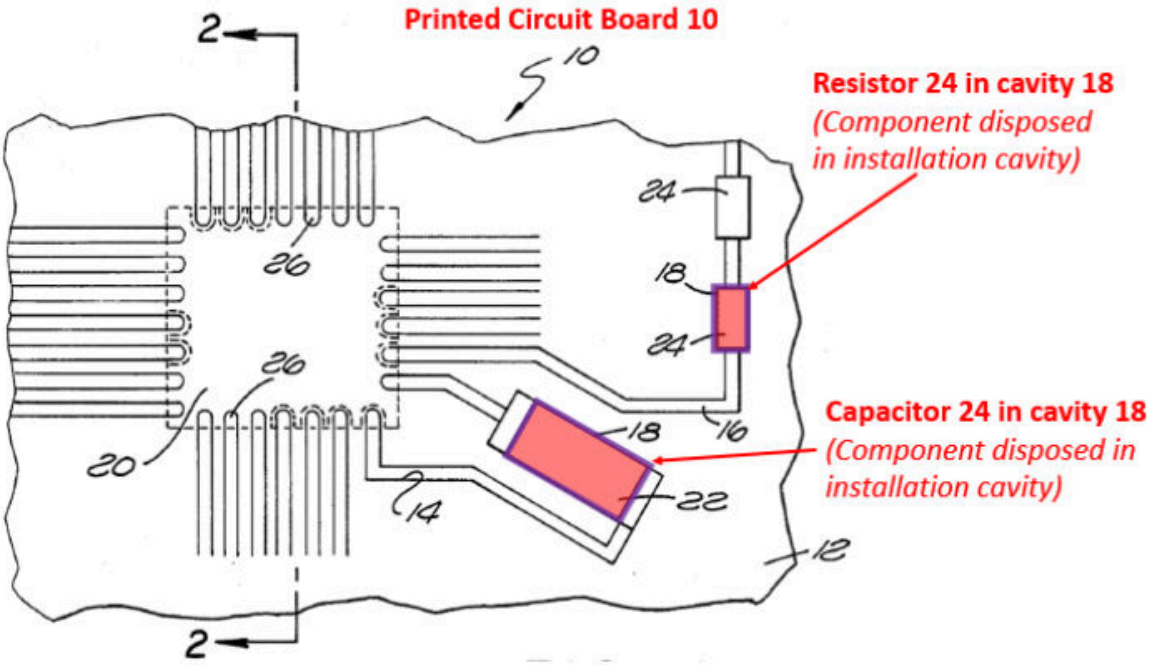
Nishiuma-Shibata-Parker renders obvious claim [4]. APPLE-1003, ¶¶161-164. As described above in Claim [3], it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nishiuma's cavity and device with the sizing relationship suggested by Parker. *Supra* §IV.C.3.[3]; APPLE-1010, 1:49-51 ("electrical components [are] preferably in a tight fit relationship in the cavities."), 2:64-3:9; APPLE-1003, ¶¶161-165, 148-160.

As shown in FIG. 2, the ***cavity*** formed in the printed circuit board (purple box) has a thickness and width (i.e., "dimensions") about equal to the size of the transistor 20, and thus is "***dimensioned to the size of the component***." APPLE-1010, 3:18-22; APPLE-1003, ¶162.



APPLE-1010, FIG. 2 (annotated)

Additionally, FIG. 1 shows that ***cavities*** formed in the printed circuit board are ***dimensioned to the size of the components*** positioned within the cavities. APPLE-1010, 2:64-3:7, 3:44-53, FIG. 1; APPLE-1003, ¶163.

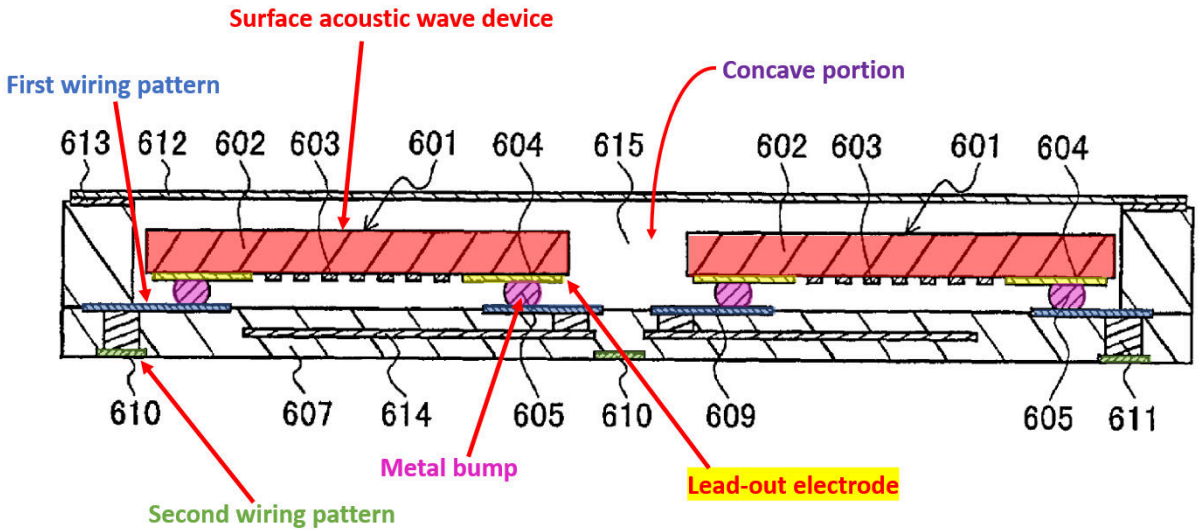


APPLE-1010, FIG. 1 (annotated)

D. GROUND 2A –Nakatani-Onda-Glick Renders Obvious Claims 1-2 and 5-6

1. Nakatani (APPLE-1007)

Nakatani describes "a conventional surface acoustic wave device built-in module." APPLE-1007, [0016]; APPLE-1003, ¶¶166-168. Nakatani's FIG. 7 depicts the conventional device having a circuit board 607, first wiring patterns 609, second wiring patterns 610, via holes 611, and surface acoustic wave devices 601 positioned within a concave portion 615. APPLE-1007, [0017], [0019].



APPLE-1007, FIG. 7 (annotated)

Nakatani describes that "[i]n the surface acoustic wave device 601, on one surface of the piezoelectric substrate 602 … the lead-out electrodes 604 formed of a metal film containing aluminum as a main component are formed." *Id.*, [0018]. "The metal bumps 605 for an electrical connection with an external circuit are

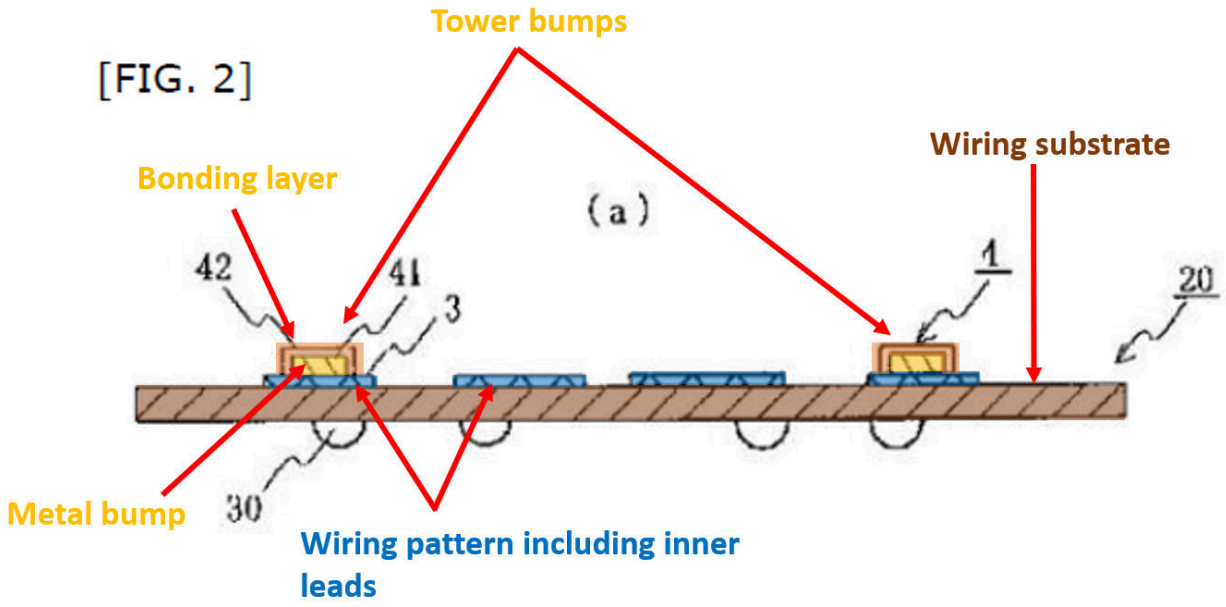
formed on the lead out electrodes 604." *Id.* "After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected [and w]hen gold bumps are used as the metal bumps 605, heat and ultrasonic wave are used in combination so as to melt the metal bumps 605 for the connection." *Id.*, [0020].

Nakatani's FIG. 7 is described as a prior art example of a "conventional surface acoustic wave device built-in module." APPLE-1007, [0016]. FIG. 7 is thus an example of what Nakatani recognized as well-known in the prior art before the Critical Date. APPLE-1003, ¶168. Although Nakatani goes on to describe mechanisms for producing "a thinner component built-in module" compared to the FIG. 7 prior art device, this does not detract from Nakatani's teachings of common characteristics and features of conventional devices. APPLE-1007, [0023]; *In re Heck*, 699 F.2d 1331, 1332-33 (Fed. Cir. 1983) ("The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain.").

2. Onda (APPLE-1008)

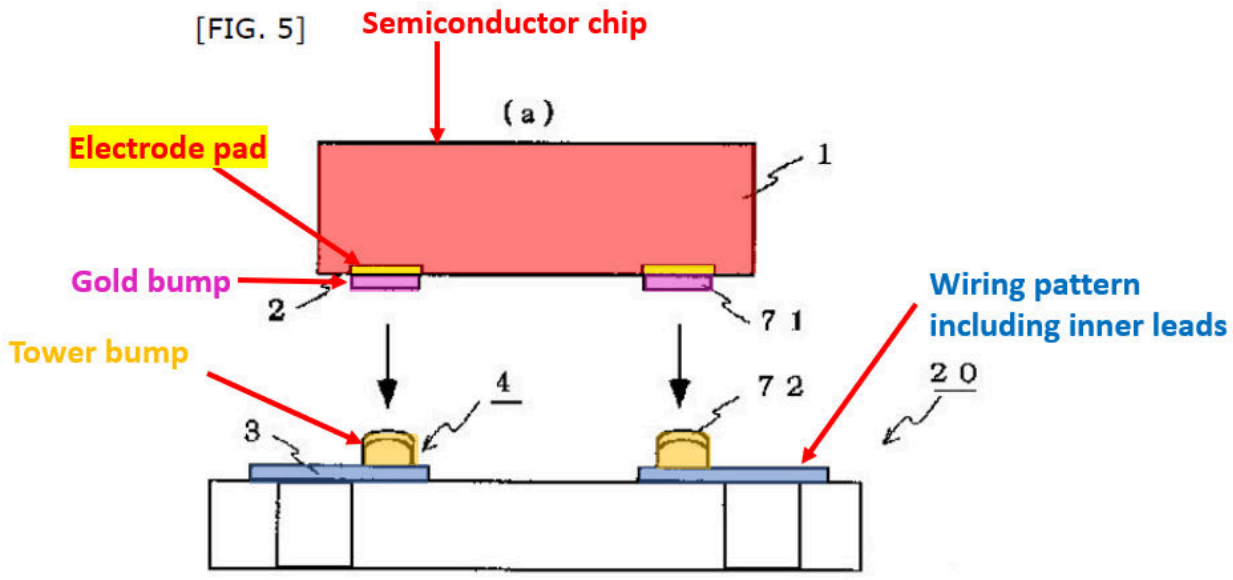
Onda describes techniques for connecting a wiring substrate to a semiconductor chip in which "tower bumps 4 are formed on the connecting portions [of the wiring pattern] to connect with the semiconductor chip." APPLE-

1008, [0045]; APPLE-1003, ¶¶169-170. "The tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to [] electrode pads 2 of the semiconductor chip 1." APPLE-1008, [0045].



APPLE-1008, FIG. 2

For example, in FIG. 5, Onda illustrates the process of mounting a "semiconductor chip 1 on the manufactured wiring substrate 20" via bumps on the semiconductor chip and tower bumps on the substrate. *Id.*, [0067]; *see also id.*, [0068]-[0083], [0092]-[0098], Figs. 6(a), 8(a), 9(a) (showing methods that couple bumps on the semiconductor chip with tower bumps on the wiring layer).



APPLE-1008, FIG. 5

3. Nakatani-Onda-Glick Combination

Nakatani discloses that "lead-out electrodes 604 formed of a metal film containing aluminum as a main component are formed" and metal bumps 605 are formed on the lead-out electrodes. APPLE-1007, [0018]. "After the surface acoustic wave devices 601 are positioned and placed on the circuit board 607, the first wiring patterns 609 and the metal bumps 605 are electrically connected." *Id.*, [0020]; *supra* §IV.D.1. In one illustrated embodiment, Nakatani shows the metal bumps 605 connected directly to the wiring patterns 609 of the circuit board. APPLE-1007, FIG. 7.

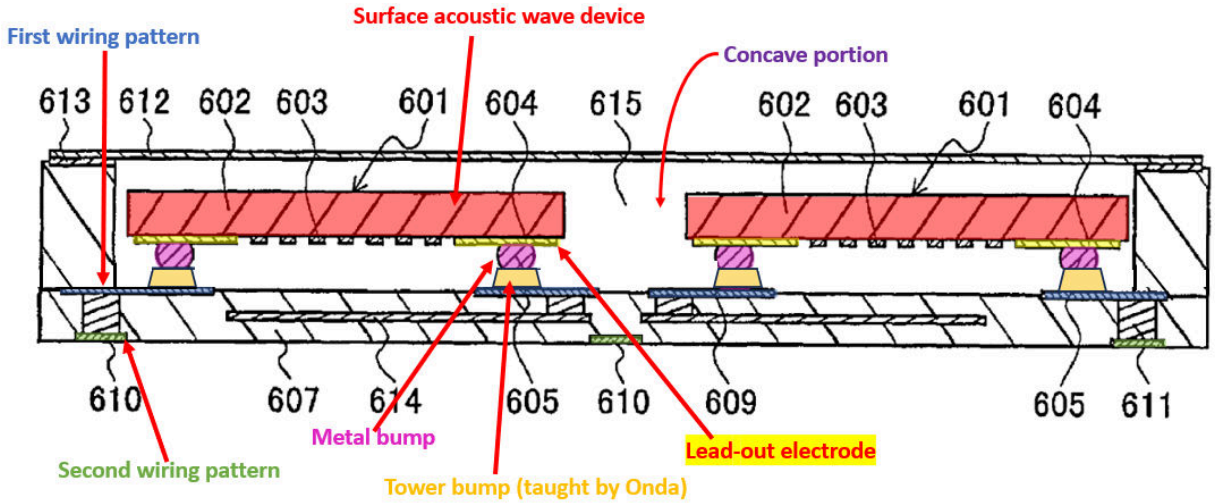
However, Nakatani does not limit the semiconductor-circuit board connection to this arrangement, and a POSITA would have understood that other

connection schemes would also be suitable for electrically connecting the metal bumps 605 to the first wiring patterns 609. *Id.*, [0016], [0017]-[0020]; APPLE-1003, ¶¶171-172. A POSITA would have been aware of other conventional solutions for bonding a component to a wiring substrate and would have considered other options to achieve known benefits associated with those options.

Recognizing that devices commonly are connected to wiring patterns of a printed circuit board by conductive contact bumps formed on the device electrode pads and wiring, a POSITA would have turned to references like Onda to investigate the implementation of pairs of conductive bumps for electrically connecting Nakatani's surface acoustic wave devices to the circuit board. APPLE-1003, ¶¶169-173. Like Nakatani, Onda describes techniques for coupling a device's electrode pads to circuit board wiring, although Onda makes the electrical connection using conductive bumps formed on the wiring substrate and on the electrode pads of the device. APPLE-1008, [0039], [0045]-[0046], [0072]-[0074], [0085]-[0086], [0093]-[0094], [0100]-[0101], [0107]-[0108], [0114]-[0115], FIGS. 5-9; APPLE-1003, ¶¶173, 166-170.

For example, Onda describes that a tower bump is formed on the wiring pattern of the PCB to provide an electrical connection to the semiconductor device and to buffer thermal stresses. *See* APPLE-1008, [0046]; APPLE-1003, ¶¶174-175. Onda describes that two conductive bumps can be used to couple a device to

a wiring substrate: "gold plating (gold bumps) 71 are formed on each electrode pad 2 [of the device and the] wiring layer of the substrate including inner leads 3 is provided with tower bumps 4 consisting of copper bumps 4 consisting of copper bumps (metal bumps 41)." APPLE-1008, [0073].



APPLE-1007, FIG. 7 (annotated, modified to include Onda's teaching to use two conductive bumps to electrically couple the device and circuit board)[5]; APPLE-1003, ¶¶174-176.

It would have been obvious to a POSITA to implement the combination of tower bumps and electrode bumps as taught by Onda into Nakatani's device in place of the single metal bump described by Nakatani for many reasons. APPLE-

[5] Nakatani's FIG. 7 as modified here to include Onda's teaching is used throughout Ground 2A to show the Nakatani-Onda-Glick combination.

1003, ¶¶171-182.

First, a POSITA would have understood that using device electrode bumps and circuit board tower bumps to electrically connect the device to the printed circuit board would provide a simple and reliable mechanism for establishing an electrical connection between the device and circuit board. APPLE-1003, ¶177; APPLE-1008, [0005] ("bumps in the form of protrusions are formed on the main surface of the semiconductor chip 1 on electrode pads 2 to make connection to the inner lead 3 easier and improve the reliability of the connection.").

Second, a POSITA would have understood that the addition of a metal tower bump to electrically connect the surface acoustic wave device to the printed circuit board would have been beneficial to improve the device's resistance to thermal stresses. APPLE-1003, ¶¶178-179; APPLE-1008, [0046], [0012] ("tower bumps that buffer the thermal stress generated between the insulating substrate and the semiconductor chip have been provided on the wiring patterns"), [0010] (describing that circuit board tower bumps may "prevent[] cracking of semiconductor chips due to thermal stress."), [0041], [0008]-[0012], [0070]; APPLE-1011, [0004], [0014].

Third, a POSITA would have understood that providing conductive bumps to electrically connect the device and the circuit board would allow for the selection and use of materials that increase the strength of the connection between

the device and circuit board. APPLE-1008, [0076]; APPLE-1003, ¶180.

Fourth, implementing a semiconductor chip such as a surface acoustic wave device module electrically coupled to the circuit board by conductive bumps formed on the wiring and on the device electrodes would have been obvious as a predictable application of a known technique for coupling devices to a printed circuit board as taught by Onda to a known system as taught by Nakatani to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶181.

The combination further would have been obvious and a POSITA would have had a reasonable expectation of success implementing the combination for all of the reasons above and given the similarities between the connection methods described by Nakatani and the techniques suggested by Onda. APPLE-1007, [0016]-[0021]; APPLE-1008; [0068]-[0083], [0092]-[0098]; APPLE-1003, ¶¶171-182.

Additionally, Nakatani describes that "[a] copper foil can be used as the wiring pattern 201, and a copper foil plated with nickel or gold further is preferable because of its stable electrical connection with the metal bumps 202 on the semiconductor chip 203." APPLE-1007, [0078]; APPLE-1003, ¶183. However, Nakatani does not limit the wiring pattern to a copper foil with plating by only one metal such as nickel ***or*** gold, and, as described above (§IV.B.2), a POSITA would have been aware that wiring patterns may be plated for a variety of

reasons, including to prevent oxidation and improve adherence and conductivity, and that the materials with which a surface wiring and land are plated are not limited to Ni or Au. APPLE-1003, ¶¶183, 126-128 (citing APPLE-1006; APPLE-1004). In this context, a POSITA would have appreciated and found obvious that additional layers of materials also would have been obvious to use in coating Nakatani's surface wiring. APPLE-1003, ¶183.

For example, Glick describes preparing a conductive-pattern from multiple layers of materials, including layers of nickel and gold. APPLE-1020, 2:56-3:11. A POSITA would have understood from Nakatani's disclosure that coated layers on a wiring pattern are beneficial and would have looked to Glick for details about how to apply coatings to the conductive elements as described by Nakatani. APPLE-1007, [0078]; APPLE-1008, [0012], [0046]-[0048]; APPLE-1020, 2:56-3:11; APPLE-1003, ¶¶184, 126-128. Multiple reasons would have motivated a POSITA to implement Nakatani-Onda's conductive surface wiring and lands in accordance with Glick's suggestion to include layers of ***both*** nickel and gold on the wiring for the reasons described above with regard to Nishiuma-Shibata-Glick, including to decrease manufacturing and materials costs. *Supra* §IV.B.2; APPLE-1003, ¶¶184, 130-135.

Additionally, implementing additional conductive material layers in a wiring pattern in the combination would have been obvious as a predictable application of

a known technique of implementing multiple conductive layers as taught by Glick to a known system as taught by Nakatani and Onda to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶¶183-185.

Further, a POSITA would have had a reasonable expectation of success in implementing Nakatani-Onda's device with Glick's suggestion to provide multiple layers of coatings to the conductive wiring because of similarities between the teachings of Nakatani and Glick including that the layered conductor structure taught by Glick is complimentary to the layers described by Nakatani. APPLE-1003, ¶¶186, 183-184, 126-128; APPLE-1007, [0016]-[0020], [0078]; APPLE-1008, [0012], [0046]-[0048]; APPLE-1020, 2:56-3:11, Figs. 1-2.

4. Analysis

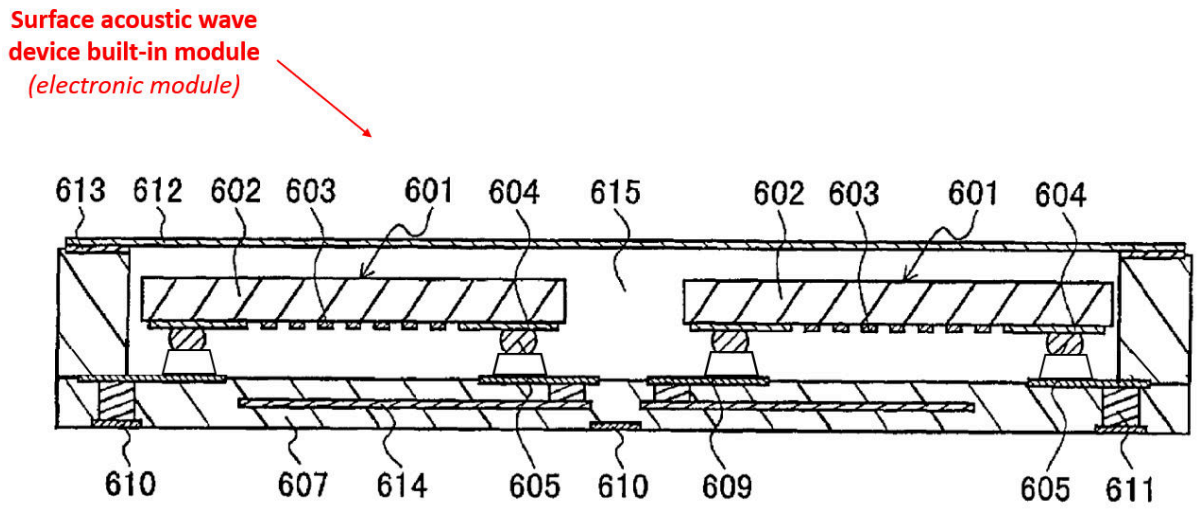
a) Claim 1

[1.pre] An electronic module, comprising:

To the extent the preamble is limiting, Nakatani-Onda-Glick renders [1.pre] obvious. APPLE-1003, ¶¶187-188.

Nakatani describes "a module containing electric elements such as semiconductor chips or surface acoustic wave devices." APPLE-1007, [0001]; *cf.* APPLE-1001, 1:24-31 ('207 patent describing that an electronic module "can be a module like a circuit board, which includes several components [such as] semiconductor components"). For example, Nakatani's FIG. 7 depicts "a

conventional surface acoustic wave device built-in module." APPLE-1004, [0016]; APPLE-1003, ¶¶187-188.



APPLE-1007, FIG. 7 (annotated, modified to show the combination)

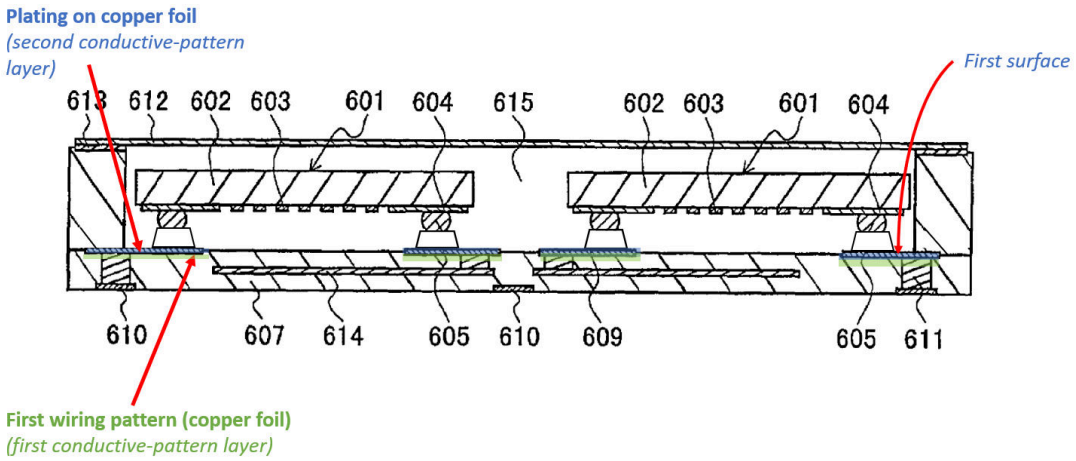
[1a]-[1b.ii] a first conductive-pattern layer and a second conductive-pattern layer disposed on the first conductive-pattern layer, the second conductive-pattern layer having a first surface;

Nakatani-Onda-Glick discloses and renders obvious elements [1a]-[1b.ii]. APPLE-1003, ¶¶189-191. For example, Nakatani describes a surface wave acoustic device module having a circuit board 607 with first wiring patterns 609. APPLE-1007, [0017]; APPLE-1003, ¶¶189, 166-168. "A copper foil can be used as the wiring pattern 201, and a copper foil plated with nickel or gold further is preferable because of its stable electrical connection with the metal bumps 202 on the semiconductor chip 203." APPLE-1007, [0078]; APPLE-1003, ¶189.

To the extent Nakatani does not expressly disclose that the copper foil can be plated with additional layers of materials, Glick teaches this conventional option. APPLE-1007, [0078]; APPLE-1020, 2:56-3:7, 3:7-11 ("a conductor layer which includes copper would consist of titanium and palladium sequentially evaporated on the substrate and then copper, nickel, and gold sequentially plated on the palladium."), 1:63-66; APPLE-1003, ¶¶190, 126-128. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's copper foil with two or more plated layers (e.g., nickel and gold layers) on a top surface of the copper foil, as Glick suggests. *Supra* §IV.D.3 (Nakatani-Onda-Glick Combination); APPLE-1003, ¶¶190, 183-184.

The copper foil forming the first wiring pattern 609 corresponds to a "***first conductive-pattern layer***" as claimed while the additional metals plated on the copper foil, as suggested by Glick, corresponds to a "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. APPLE-1007, [0078], [0017]-[0020]; APPLE-1003, ¶¶189-191; *cf.* APPLE-1001, 6:28-31 ('207 patent describing "surfaced" conductive layers for wiring similar to Nakatani's), 6:52-59 ('207 patent also describing layers comprised of multiple components); APPLE-1002, 170-173. The top of the plated layer provides the claimed "***first surface***" of the second conductive-pattern layer. APPLE-1007, [0078], [0016]-[0020];

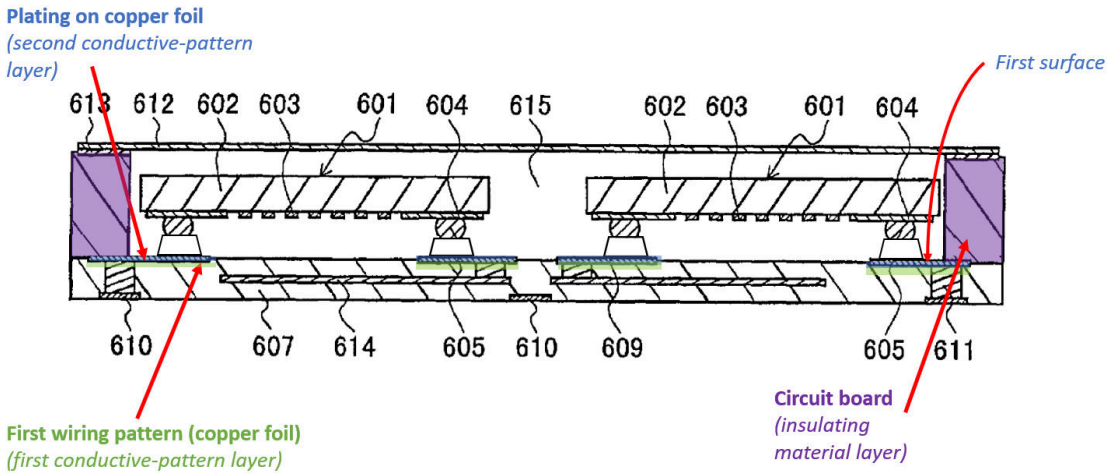
APPLE-1020, 2:56-3:11, Figs. 1-2; APPLE-1003, ¶191.



APPLE-1007, FIG. 7 (annotated, modified to show the combination)

[1c] an insulating-material layer disposed on the first surface of the second conductive-pattern layer;

Nakatani-Onda-Glick renders obvious element [1c]. APPLE-1003, ¶¶192-193. For example, Nakatani describes that "[i]n order to ensure a space in which the surface acoustic wave devices 601 are mounted, the circuit board 607 has the concave portion 615 in its central portion." APPLE-1007, [0019]. As shown in FIG. 1, Nakatani describes a layer of the circuit board 607 disposed on the first surface of the first wiring pattern (***second conductive-pattern layer***) coating. APPLE-1003, ¶192.



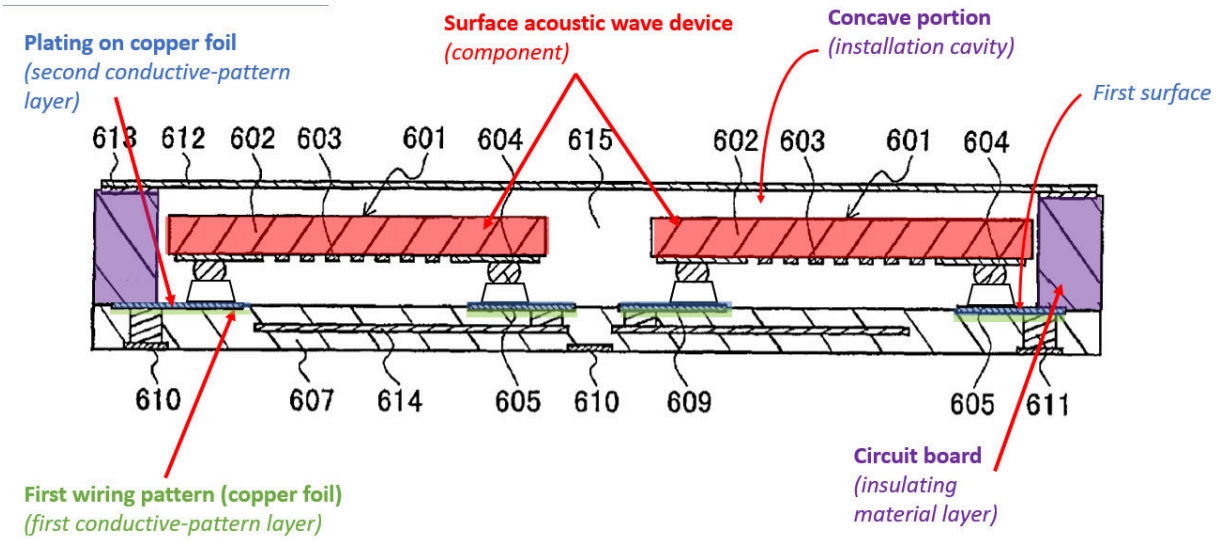
APPLE-1007, FIG. 7 (annotated, modified to show the combination)

To the extent Nakatani does not specifically identify the material of the layer that forms the concave portion of the circuit board 607, a POSITA would have known that circuit boards conventionally employ an insulating material between conductive layers that serves to electrically isolate the conductive layers, and would thus have understood the layer of Nakatani's board that forms the concave portion to be an insulating material, or would have found it obvious to implement it with an insulating material to electrically isolate the conductive layers beneath and above sidewalls. APPLE-1003, ¶¶193, 22-36 (citing APPLE-1010, 1:9-17 ("Printed circuit boards have been in use for decades to provide electrical circuitry [and] generally include a thin substrate made from a suitable electrically insulating

material such as a ceramic or an epoxy-glass composite"); APPLE-1012, 212-221; APPLE-1011, [0007]-[0009]).

[1d]-[1e.i] at least one installation cavity disposed in the insulating-material layer; a component disposed within the at least one installation cavity,

Nakatani-Onda-Glick renders obvious elements [1d]-[1e.i]. APPLE-1003, ¶194. For example, Nakatani describes that "[i]n order to ensure a space in which the surface acoustic wave devices 601 are mounted, the circuit board 607 has the concave portion 615 in its central portion." APPLE-1007, [0019]. As shown in FIG. 7, the circuit board includes a concave portion (***installation cavity***) in which the surface acoustic wave devices (***component***) are positioned. *Id*., [0019], [0021]; APPLE-1003, ¶194.

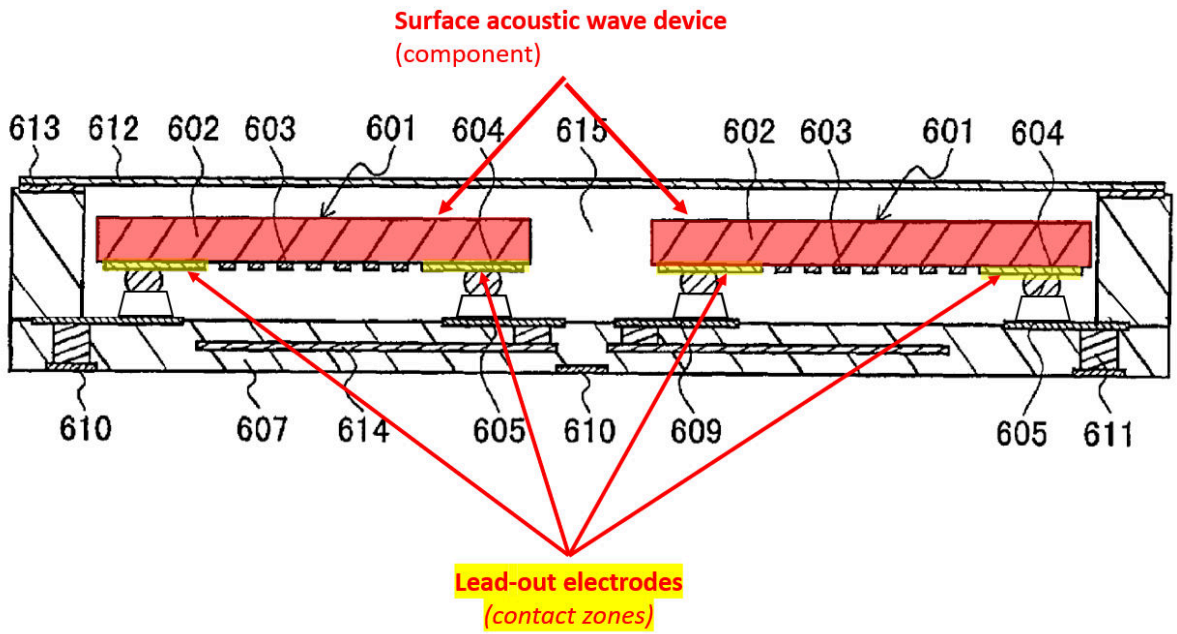


APPLE-1007, FIG. 7 (annotated, modified to show the combination)

[1e.ii] the component comprising contact zones comprising aluminum;

Nakatani-Onda-Glick renders obvious element [1e.ii]. APPLE-1003, ¶¶195-

196. For example, as shown in FIG. 7, Nakatani describes that the surface acoustic wave device 601 (***component***) includes lead-out electrodes 604. APPLE-1007, [0018], FIG. 7; APPLE-1003, ¶195. Nakatani's lead-out electrodes provide "***contact zones***" on the component. APPLE-1003, ¶195.



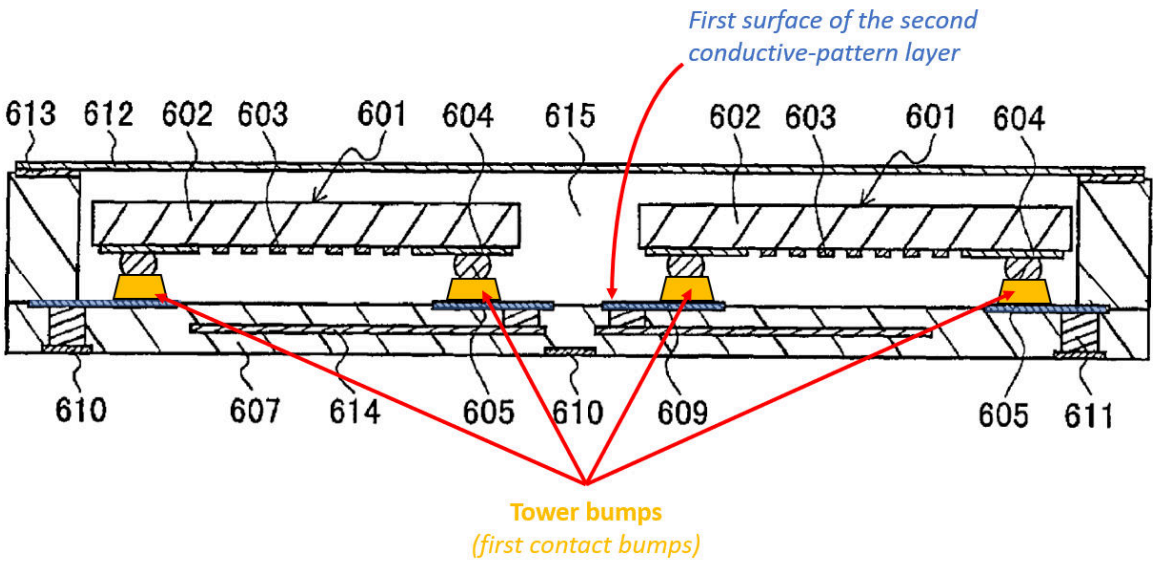
APPLE-1007, FIG. 7 (annotated, modified to show the combination)

Further, Nakatani describes that "the lead-out electrodes 604 [are] formed of a metal film containing aluminum as a main component." APPLE-1007, [0018]; APPLE-1003, ¶196.

[1f] first contact bumps disposed on the first surface of the second conductive-pattern layer, the first contact bumps electrically connected thereto; and

Nakatani-Onda-Glick renders obvious element [1f]. APPLE-1003, ¶¶197-200. For example, Nakatani describes "the first wiring patterns 609 and the metal

bumps 605 are electrically connected." APPLE-1007, [0020]. To the extent Nakatani does not expressly disclose electrically connecting the device to the wiring patterns via the metal bumps and contact bumps formed on the circuit board wiring patterns, Onda teaches this conventional solution for bonding a component to a circuit board. APPLE-1008, [0039], [0045], FIGS. 5-10; APPLE-1003, ¶¶197-200. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's device bonded to the circuit board wiring pattern using two conductive bumps, including a tower bump (***first contact bumps***) formed on the surface wiring of the circuit board (***first surface of the second conductive-pattern layer***) as suggested by Onda. *Supra* §IV.D.3 (Nakatani-Onda-Glick Combination); APPLE-1003, ¶¶197-198, 183-186.



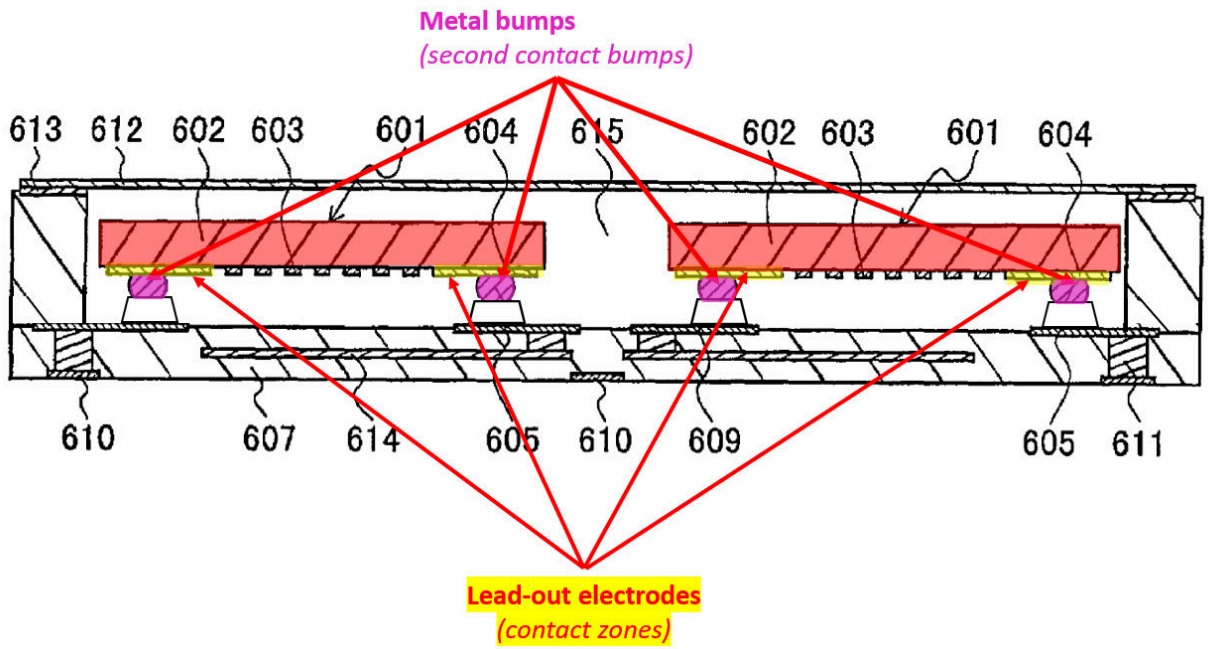
APPLE-1007, FIG. 7 (annotated, modified to show the combination)

As described above, Nakatani teaches that the device is electrically connected to the wiring patterns 609 through the metal bumps 605. APPLE-1007, [0020]. Further, Onda describes that the pairs of tower bumps and metal bumps of various materials for coupling a semiconductor device to a wiring substrate provide an electrical connection. *See* APPLE-1008, [0099], [0014], [0057], [0101]-[0106]. A POSITA would have understood that the tower bumps described by Onda are ***electrically connected*** to the copper foil forming Nakatani's wiring patterns to couple the device to the wiring of the printed circuit board. APPPLE-1008, [0039] ("tower bumps 4 are provided in the wiring layer of the substrate including inner leads 3 to connect with the semiconductor chip"); APPLE-1003, ¶¶199-200. Accordingly, a POSITA would have understood that the tower bumps

(***first contact bumps***) are electrically connected to the plated surface of the first wiring pattern (***first surface of the second conductive pattern-layer***). APPLE-1003, ¶¶197-200.

[1g] second contact bumps disposed on the contact zones and electrically connected thereto,

Nakatani-Onda-Glick renders obvious element [1g]. APPLE-1003, ¶¶201-204. Nakatani describes that "metal bumps 605 for an electrical connection with an external circuit are formed on the lead-out electrodes 604." APPLE-1007, [0018], [0017], FIG. 7. Onda teaches that use of two conductive bumps to electrically connect a semiconductor device to wiring board is a conventional solution for bonding a component to a circuit board. APPLE-1008, [0039], [0045], [0094], [0101]-[0102], FIGS. 5-10; APPLE-1003, ¶¶201, 169-170. As described above, it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's device bonded to the circuit board wiring pattern using two conductive bumps, including a metal bump (***second contact bumps***) formed on the electrode pads (***contact zones***) of the device as suggested by Onda. *Supra* §IV.D.3 (Nakatani-Onda-Glick Combination); APPLE-1003, ¶¶202, 183-186.



APPLE-1007, FIG. 7 (annotated, modified to show the combination)

As described above, Nakatani teaches that the device is electrically connected to the wiring patterns 609 through the metal bumps 605. APPLE-1007, [0020]. Further, Onda describes that the pairs of tower bumps and metal bumps of various materials for coupling a semiconductor device to a wiring substrate provide an electrical connection. *See* APPLE-1008, [0101]-[0102] ("gold plating (gold bumps) 71 are formed on each electrode pad 2…[w]hen mounting the semiconductor chip 1 on the wiring substrate 20… the semiconductor chip 1 is placed on the tower bumps formed in the connection portions (tips) of the inner leads 3 on the wiring substrate 20, a connection is established by a gold-gold diffusion reaction with the electrode pads 2"), [0099], [0014], [0057], [0103]-

[0106]. A POSITA would have understood that the metal (e.g., gold) bumps described by Onda are ***electrically connected*** to the electrode pads of Nakatani's surface acoustic wave device. APPPLE-1008, [0101]-[0102], [0039]; APPLE-1003, ¶203. Accordingly, a POSITA would have understood that the metal bumps (***second contact bumps***) are electrically connected to the electrode pads (***contact zones***). APPLE-1003, ¶¶201-204.

[1h] wherein at least one of the first conductive-pattern layer and the second conductive-pattern layer comprises at least two layers of at least two different materials.

Nakatani-Onda-Glick renders obvious element [1h]. APPLE-1003, ¶¶205-208. For example, as described above, Nakatani's copper foil forming the first wiring pattern 609 provides the claimed "***first conductive-pattern layer***" while the additional layer or layers, as suggested by Glick, plated on the copper foil provide the claimed "***second conductive-pattern layer***" disposed on the first conductive-pattern layer. *Supra*, §§IV.D.4.[1a]-[1b.ii]; APPLE-1007, [0078], [0017]-[0020]; APPLE-1003, ¶¶206, 189-191. The second conductive-pattern layer thus includes layers of nickel and gold and thus comprises two layers of at least two different materials: (1) nickel on the copper plating, and (2) gold. APPLE-1020, 2:56-3:20, 1:63-66; APPLE-1003, ¶¶205-206, 56-61; *supra* §III.C.1.

Additionally, although Nakatani describes that the "[a] copper foil can be used as the wiring pattern 201," Nakatani does not limit the wiring pattern to

copper materials. APPLE-1007, [0078]; APPLE-1003, ¶207. A POSITA would have been aware of other conventional materials for forming conductive wiring patterns on a circuit board and would have looked to a references like Glick that describe examples of materials used to form conductive patterns. APPLE-1003, ¶¶207, 126-128, 183-186. For example, Glick describes that "[a] layer of titanium 12 is first deposited on the substrate 10… [n]ext a layer of palladium 14 is deposited on the titanium…." APPLE-1020, 2:56-66; 1:63-66. A POSITA would have been motivated to substitute Glick's suggested titanium and palladium for Nakatani's copper foil to improve adherence of the wiring pattern to the circuit board. APPLE-1020, 2:56-60 ("A layer of titanium 12 is first deposited on the substrate 10… to increase the adherence of any layer deposited subsequently"); APPLE-1003, ¶208. With the use of titanium and palladium layers to form a wiring pattern, the first conductive-pattern layer in this example also comprises two layers of at least two different materials: (1) titanium and (2) palladium[6] such that both the first and second conductive-pattern layers comprises at least two

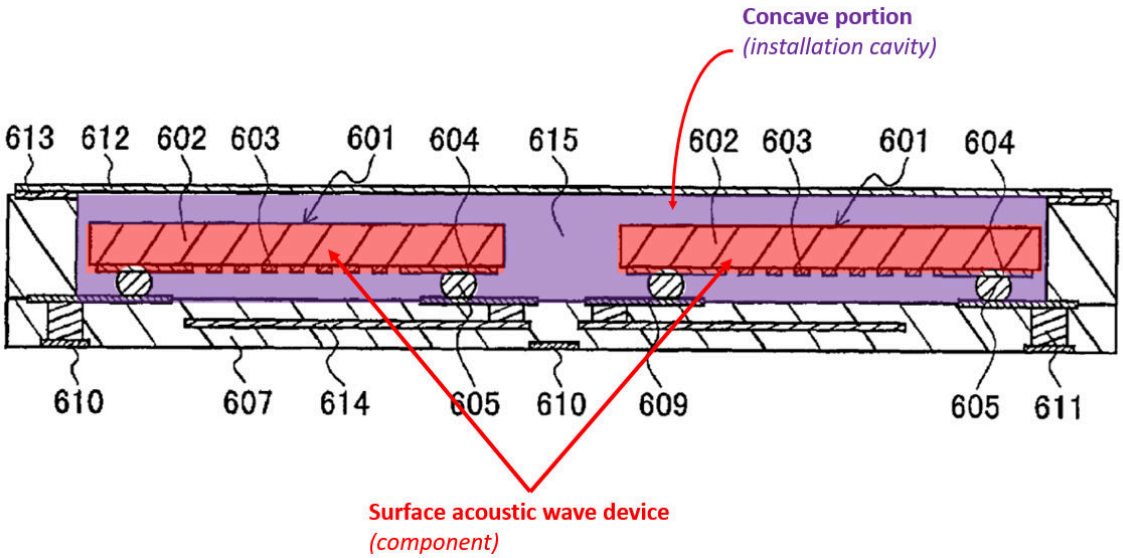
[6] In this example, an additional layer of copper may be added between the palladium and nickel as taught by Glick (APPLE-1020, 2:64-3:11), though this does not impact the analysis as to whether the "two layers" are met. APPLE-1003, ¶208.

layers of at least two different materials as claimed. *Supra* §III.C.1; APPLE-1020, 2:56-3:7; APPLE-1003, ¶¶207-208, 56-61.

b) Claim 2

[2] The electronic module of claim 1, wherein the at least one installation cavity is thicker than the component.

Nakatani-Onda-Glick renders obvious claim [2]. APPLE-1003, ¶¶209-211. For example, FIG. 7 shows that the concave portion (installation cavity) may be thicker than the component. APPLE-1007, FIG. 7; APPLE-1003, ¶¶209-211.



APPLE-1007, FIG. 7 (annotated)

c) Claim 5

[5] The electronic module of claim 1, wherein the first contact bumps comprise tin.

Nakatani-Onda-Glick renders obvious claim [5]. APPLE-1003, ¶¶212-214. As described above, it would have been obvious and a POSITA would have been

motivated for several reasons to implement Nakatani's device using two conductive bumps to couple the device to the circuit board wiring pattern, using materials suggested by Onda. *Supra*, §IV.D.3; APPLE-1003, ¶¶212, 171-182. For example, Onda describes that "[t]he tower bumps 4 are composed of a metal bump 41 and a bonding layer 42 that bonds to the electrode pads 2 of the semiconductor chip 1 [for example g]old, solder, or tin can be used… in the bonding layer 42." APPLE-1008, [0045]; [0073]-[0074], FIG. 6A; APPLE-1003, ¶¶212-213.

The choice of tin would have been an obvious design choice to achieve desired electrical, thermal, mechanical, and bonding characteristic for a given design, and it would have been obvious to a POSITA to implement Nakatani-Onda-Glick with tower bumps (***first contact bumps***) including tin, as Onda suggests, to increase the strength of the bond between Nakatani's first wiring pattern and the device by making the connection through gold-tin diffusion. APPLE-1008, [0073]-[0077]; APPLE-1003, ¶¶214, 171-182. A POSITA would have had a reasonable expectation of success in implementing the combination for all the reasons described above. *Supra* §IV.D.3; APPLE-1003, ¶¶212-214, 171-182.

d) Claim 6

[6] The electronic module of claim 1, wherein the second contact bumps comprise copper.

Nakatani-Onda-Glick renders obvious claim [6]. APPLE-1003, ¶¶215-217. As described above, it would have been obvious and a POSITA would have been motivated for many reasons to implement Nakatani's device using two conductive bumps to couple the device to the circuit board wiring pattern, using materials suggested by Onda. *Supra*, §IV.D.3; APPLE-1003, ¶¶215, 171-182. For example, Nakatani describes that gold bumps may be melted to form the electrical connection to the wiring, or the connection can be made "using an electrically conductive adhesive." APPLE-1007, [0020]. Nakatani does not describe the electrically conductive adhesive to be used, however, Onda describes that the pairs of bumps may be bonded with a bonding layer 42 of a material selected based on the chosen connection method. APPLE-1008, [0136], [0063], [0042]-[0043]. For example, Onda describes that copper bumps that are metal-plated can be coupled to gold bumps. *Id.*, [0073]-[0077], FIG. 6A; APPLE-1003, ¶¶215-216.

The choice of copper would have been an obvious design choice to achieve desired electrical, thermal, mechanical, and bonding characteristic for a given design, and it would have been obvious to a POSITA to implement Nakatani-Onda-Glick with metal bumps (***second contact bumps***) formed from material

combinations suggested by Onda, such as copper, to enhance connection between the metal bumps and tower bumps. APPLE-1003, ¶217. A POSITA would have had a reasonable expectation of success in implementing the metal bumps using copper, given that Onda suggests copper bumps in combination with bumps that are formed from gold and plated with tin. APPLE-1008, [0042]-[0043], [1063]; APPLE-1003, ¶¶214-217, 171-182.

E. GROUND 2B – Nakatani-Onda-Glick-Parker Renders Obvious Claims 3 and 4

1. Nakatani-Onda-Glick-Parker Combination

Nakatani describes that a circuit board includes a concave portion "to ensure a space in which the surface acoustic wave devices 601 are mounted." APPLE-1007, [0019]. A POSITA would have understood that a cavity is sized to fit the device intended to be mounted therein, and would have further understood that there are a variety of ways to size the cavity to the device. APPLE-1003, ¶¶218, 22-36 (citing APPLE-1011, [0034], [0017], [0038], [0044], FIG. 4). In this context, a POSITA would have turned to references like Parker that describe sizing considerations for a cavity. APPLE-1003, ¶¶218-219.

For example, Parker describes "[c]avities 18 are [] provided in one or both of the parallel surfaces of the substrate 12" of the printed circuit board. APPLE-1010, 2:64-65, FIG. 2. "Electrical components are adapted to be disposed in the

cavities 18, preferably in a tight fit with the walls of the cavities." *Id.*, 2:66-3:1; APPLE-1003, ¶¶219, 145-147. Like Nakatani, Parker describes mounting a device within a circuit board cavity and provides additional cavity sizing guidance. APPLE-1003, ¶219. Multiple reasons would have motivated a POSITA to implement Nakatani's cavity to be sized to the dimensions of the component in accordance with Parker's suggestion, many of the reasons similar to those reasons discussed above with regard to the Nishiuma-Shibata-Parker combination (§IV.C.2). APPLE-1010, 1:49-51, 2:64-3:1, FIG. 2; APPLE-1003, ¶¶218-225.

First, a POSITA would have understood that sizing the cavity to have a tight fit with the component optimizes the use of limited space on the printed circuit board. APPLE-1003, ¶220 (citing APPLE-1007, [0002]; APPLE-1011, [0034]).

Second, to the extent that components are connected to the printed circuit board by wires in addition to contact bumps, positioning a component in a cavity with a tight fit requires shorter wire bond lengths and reduces parasitic effects. APPLE-1010, [0017]; APPLE-1003, ¶221.

Third, a POSITA would have understood that a tight fit between the cavity and the component allows for the component to be easily placed in proper position within the cavity to provide electrical connection between the component and wiring in the cavity. APPLE-1003, ¶222 (citing APPLE-1011, [0006]); APPLE-1010, 3:654:2.

Fourth, a POSITA would have appreciated that there are a limited number of possible size relationships between a cavity and a component sized to fit in the cavity. APPLE-1003, ¶223; APPLE-1001, 6:7-16 (describing that the installation base can be thicker than, less thick than, or equally thick as the component). A POSITA would have found it obvious to try these finite and predictable solutions to sizing the cavity relative to the component and would have had a reasonable expectation of success in implementing them, given that these are conventional methods for mounting a component within a cavity. APPLE-1003, ¶¶223-224;

A POSITA would have had a reasonable expectation of success implementing the combination for all the reasons described above and given that Parker describes techniques for disposing components in circuit board cavities, like Nakatani. APPLE-1007, [0016]-[0021]; APPLE-1010, 1:49-51, 2:5-27, 2:64-3:22; APPLE-1003, ¶¶218-225. Implementing a surface acoustic wave device module with a cavity that has a tight fit to the component would have been obvious as a predictable application of a known technique for positioning components in a printed circuit board as taught by Parker to a known system as taught by Nakatani to achieve entirely predictable results. *KSR*, 550 U.S. at 417; APPLE-1003, ¶¶225, 22-36.

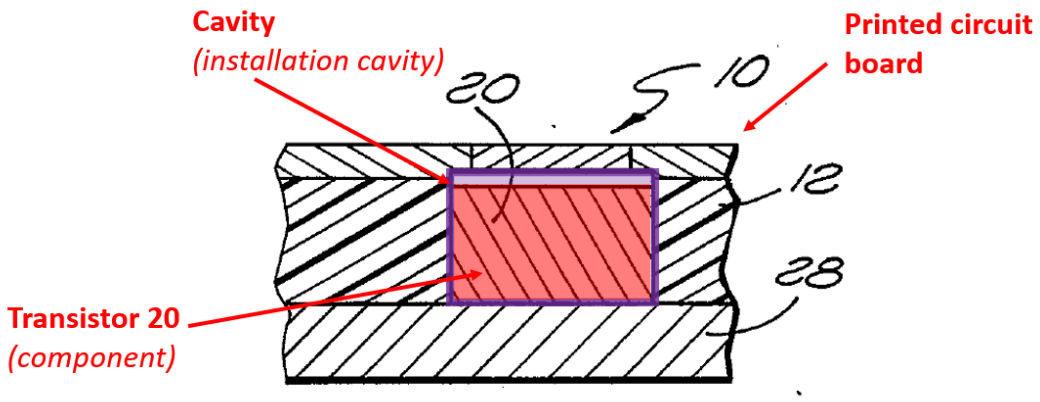
2. Analysis

a) Claim 3

[3] The electronic module of claim 1, wherein the at least one installation cavity has about equal thickness as the component.

Nakatani-Onda-Glick-Parker renders obvious claim [3]. APPLE-1003, ¶¶226-228, 109. For example, Nakatani describes that a concave portion provides "a space in which the surface acoustic wave devices 601 are mounted." APPLE-1007, [0019]. To the extent Nakatani does not expressly disclose an installation cavity of equal thickness as the component, Parker teaches this conventional option, and it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's cavity and device with the sizing relationship suggested by Parker. *Supra* §IV.E.1; APPLE-1010, 1:49-51 ("[c]avities are [] provided in the printed circuit board to receive electrical components, preferably in a tight fit relationship in the cavities"), 2:64-3:9; 3:18-22; APPLE-1004, FIGS. 1, 9, 10; APPLE-1003, ¶¶226-227 (citing APPLE-1011, [0034], [0017], [0038]-[0044], FIG. 4).

As shown in FIG. 2, the ***cavity*** formed in the printed circuit board (purple box) ***has about equal thickness*** as the transistor 20 ("***component***"). *Id.*, APPLE-1003, ¶¶227-228.



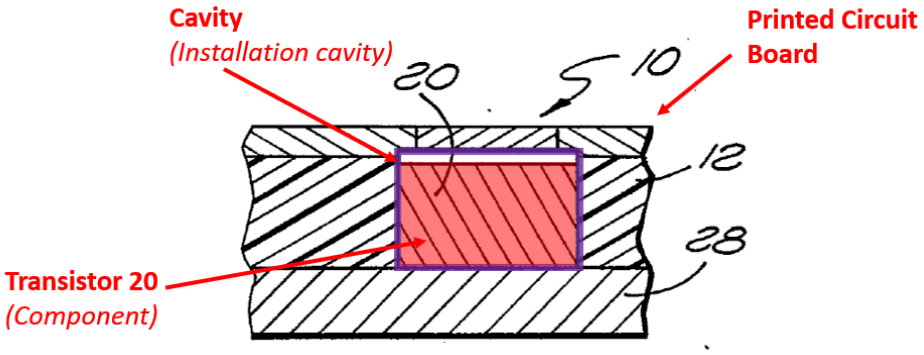
APPLE-1010, FIG. 2 (annotated)

b) Claim 4

[4] The electronic module of claim 3, wherein the at least one installation cavity is dimensioned to the size of the component.

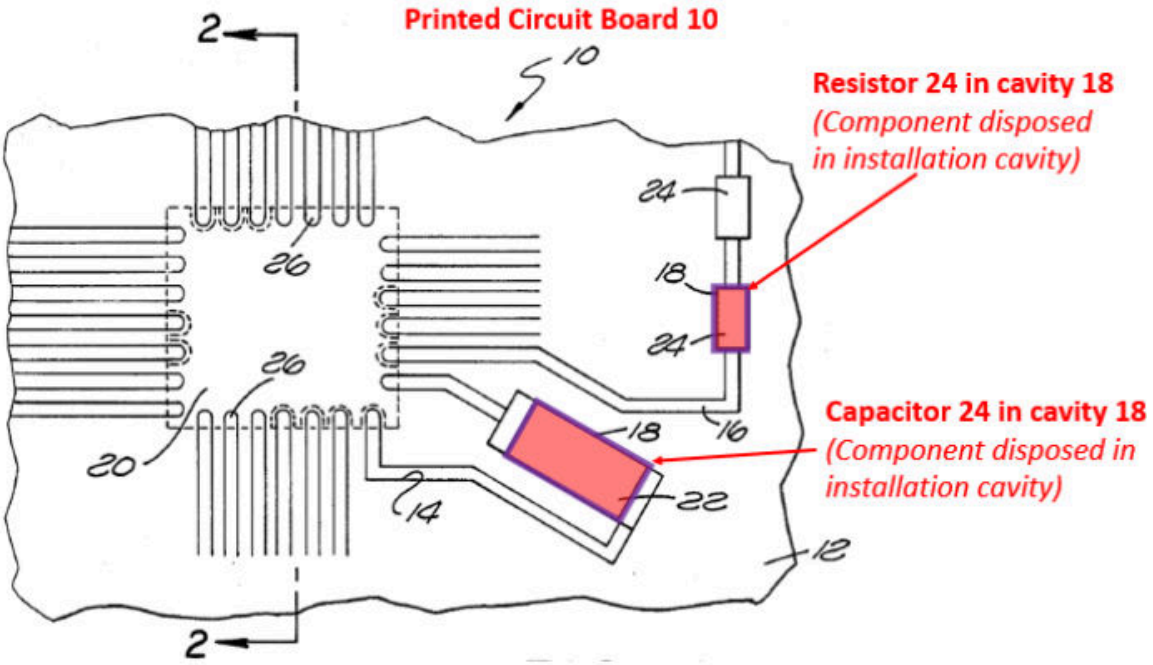
Nakatani-Onda-Glick-Parker renders obvious claim [4]. APPLE-1003, ¶¶229-232. As described above in Claim [3], it would have been obvious and a POSITA would have been motivated by multiple reasons to implement Nakatani's cavity and device with the sizing relationship suggested by Parker. *Supra* §IV.E.1; APPLE-1010, 1:49-51 ("electrical components [are] preferably in a tight fit relationship in the cavities."), 2:64-3:9; APPLE-1003, ¶¶228-232, 218-225.

As shown in FIG. 2, the ***cavity*** formed in the printed circuit board (purple box) has a thickness and width (i.e., "dimensions") about equal to the size of the transistor 20, and thus is "***dimensioned to the size of the component***." APPLE-1010, 3:18-22; APPLE-1003, ¶230.



APPLE-1010, FIG. 2 (annotated)

Additionally, FIG. 1 shows that ***cavities*** formed in the printed circuit board are ***dimensioned to the size of the components*** positioned within the cavities. APPLE-1010, 2:64-3:7, 3:44-53, FIG. 1; APPLE-1003, ¶231.



APPLE-1010, FIG. 1 (annotated)

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. Section 325(d)

None of Nishiuma, Shibata, Onda, Parker or Glick were considered by the Office during prosecution. APPLE-1001, Cover (56); APPLE-1002. The U.S. patent corresponding to Nakatani (U.S.6,798,121) was submitted in an IDS filed 8/31/2020 and initialed by the Examiner as considered on 11/06/2020 – the same day the Examiner performed the search for initial examination of the claims. APPLE-1002, 55, 132, 129. Nakatani (and Nishiuma, Shibata, Onda, Glick and Parker) were not cited in any rejection of the claims.

Because the ’207 patent’s prosecution did not involve any discussion between the applicant and Examiner regarding the teachings of the prior art applied in this Petition, the invalidity challenge asserted here is not the same as, or substantially similar to, art and arguments previously presented to the Office in connection with the ’207 patent. *See, generally,* APPLE-1002; *supra* §III.B. Moreover, even if any of these references were somehow considered cumulative, the prosecution history never examined any of the claims in view of the prior art combinations applied in this Petition.

Accordingly, neither condition of the *Advanced Bionics* framework first prong is met, and there is no need to reach the second prong to resolve against

discretionary denial under §325(d). *See*, *e.g.*, *Oticon Medical AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential). To the extent file history contains prior art teachings or arguments cumulative to those presented in this Petition, the Examiner erred in not recognizing the significance of those teachings or arguments in relation to the unpatentability of claims 1-6—particularly after the Applicant heavily amended the claims relative to the claimed subject matter initially examined.

B. Section 314(a)

The *Fintiv* factors weigh against exercising discretionary denial.

Factor 1 is neutral or favors institution. A motion to transfer to the Northern District of California is pending. While a motion to stay has not been filed, even without inferring how the district court would rule, the pending motions at least increase the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. Even if the district court proceeding is not transferred, the Board will likely issue its final written decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is also uncertain and subject to change due to a number of factors.

Factor 3 favors institution because Petitioner has diligently filed this Petition while the litigation remains in its early stages.

Factor 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the district court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein.

VI. CONCLUSION AND FEES

The Challenged Claims are unpatentable. Please charge fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple Inc. is the petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or IPR petitions for the '207 Patent. The '207 patent is the subject of civil action: *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
W. Karl Renner, Reg. No. 41,265 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR50095-0198IP1@fr.com	Nicholas W. Stephens, Reg. No. 74,320 Kiersten Batzli, Reg. No. 75,476 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR50095-0198IP1@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0198IP1@fr.com.

Respectfully submitted,

Dated: February 6, 2025

/W. Karl Renner/

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Attorneys for Petitioner

CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,957 words, which is less than the 14,000 allowed under 37 C.F.R. § 42.24.

Dated: February 6, 2025

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Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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