

3D-INTEGRATION: TRENDS AND OPPORTUNITIES - AN OVERVIEW

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ABSTRACT

The drive to maintain the rate of component integration in integrated circuits continues while numerous technical challenges are looming on the horizon. From the interconnect view, signal delay and power dissipation resulting from long global interconnects are serious concerns. A continuing trend is in integrating a diversity of device technologies on silicon, to provide even higher levels of system functionality. Footprint reduction of the integrated device is an additional need, especially for portable device applications. Two-dimensional integration on a single chip to satisfy all the demands is not viable. Three-dimensional integration (3D) of components is an approach which could address some of these needs. There are three broad approaches in 3D integration: stacking chips/packages, stacking wafers, and fabrication of multiple device layers on the same wafer. Stacked chip devices are already in production, while the stacked wafers and multi layer device approach are still under development. There is increasing acceptance of the 3D approach as a viable means of integration, although the concept has been in existence for many years. An overview of the approaches, the challenges and opportunities is given in this presentation.

INTRODUCTION

The growth of the semiconductor industry has historically depended on the integration of more components on a chip through transistor and interconnects scaling and manufacturing technology. Much of the current technology development thrust is to sustain the historical rate of doubling component density every eighteen months and to surmount the technical impediments ahead. Integration of components and functions continues to be pushed for increased functionality through the System-on-Chip (SoC) and System in Package (SiP) approaches. System-on-chip integration methodology has received much deserved credit for many products, and is technologically attractive from a silicon implementation view. Future SOC, however, may entail higher costs in design and manufacturing, because multiple divergent functionalities are difficult to integrate together in the same silicon, and they can be performance-constrained when mixed functionalities are integrated. While the preferred approach in many situations, SoC has several limitations that must be understood in order to make intelligent judgement in system design. When development times and cost are considered, it is not possible to regard a monolithic single chip as the ideal in all cases. To complement the SoC approach, multicomponent integration through SiP is being currently pursued with great expectations. With many anticipated challenges in continuing to reduce individual chip area (i.e., the X and Y dimensions), and in 2D multichip packaging, interest in three

dimensional (3D) integration as a means of increasing component density is mounting [1-5].

There are many drivers for the 3D integration approach. One of the key enablers for integration through SoC or SiP, is the appropriate interconnect technology. Although individual device dimensions and interconnect widths have shrunk, chip size has continued to increase and has resulted in longer global interconnects. In SoC integration, signal delay and power dissipation from long global interconnects have become serious concerns [6-8]. To overcome this issue, the drive is to keep the interconnect length short through 3D integration [9]

In addition, the increasing drive to integrate diverse component technologies for enhanced SoC functionality, presents a multitude of technical and business challenges. For example, a single chip SoC for a cell phone handset could require GaAs, MEMS, digital, analog, power, and passives technologies. RF circuits integrated with microprocessor in a 3D format, to facilitate wireless communication, has attracted major interest. Another motivation for 3D is the need to reduce footprint of the packaged device, especially for portable applications. There are multiple technology approaches for 3-D integration, currently at varying levels of maturity and each with its own unique strengths and issues. These approaches include [Fig: 1]:

- Stacked chips or stacked packages
- Stacked wafers through wafer bonding
- Device fabrication in multiple planes on the same wafer

By leveraging an approach appropriate for the application, a 3-D integrated device can be fabricated with optimal cost/performance. Products based on stacked chips and stacked packages have been in production for a few years. Technology capabilities of this approach continue to be improved for wider product applications. The stacked chips in a package have a much higher package integration ratio. In addition, only one package has to be tested, and the established IC assembly methods can be used.

Wafer bonding, while not a new idea, is being adapted for 3-D applications. Many groups are exploring wafer bonding using bonding layers of silicon oxide, metals, or polymers and the needed interconnect technology. The concept of fabricating devices on recrystallized silicon layers or epitaxial overgrowth has been around for many years. This approach is being revisited based on the emerging needs and with newer approaches.

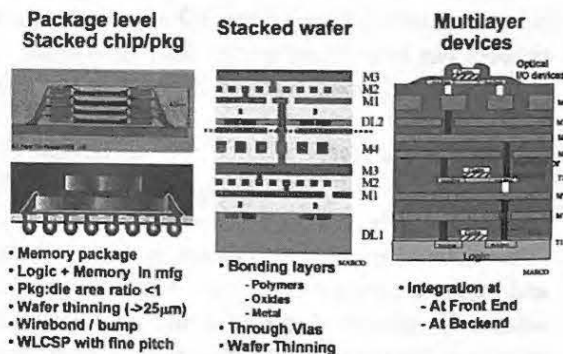


Fig: 1. Schematic of 3D integration schemes.

STACKED CHIPS/ STACKED PACKAGES

Early adoption of 3D stacking was with devices packaged first in ultra-thin packages, and stacked vertically using conventional packaging and interconnects technology. This is a mature technology offered by many assembly houses. This approach is driven by the need for foot print reduction and is a very high yield process committing only tested good devices in packages. In principle, many packages can be stacked without undue difficulty. However, this approach offers minimal enhancement in interconnect performance expected from 3D integration nor exploits the opportunity in cost reduction in packaging.

Stacking of chips, in which two or more ICs are attached one die on top of the other in a single package, is an approach gaining acceptance. Chips are stacked using epoxy adhesives. The memory industry has realized this opportunity to minimize package size and cost and has implemented this in products. The mature option uses wire bonds to interconnect between chips and wire bonds to the package substrate.

The chips have to be of appropriate graduated sizes so one can be wire bonded to the next. Two and three chip stacks are already in production while stacking of eight chips has been reported by (Fujitsu) [10].

To stay within the standard package heights, the stacked chips need to be thinned. The backgrinding process is more widely used to reduce the die thickness to the range of 50 -125 μm on 200-mm wafers. Wafer thinning and handling have emerged as key enablers which need special attention, especially as the process is extended to 300mm-wafer size. Mechanically thinning wafers down to thickness of 25 microns has been reported.

In the stacked chip option, only tested known good die (KGD) are committed for stacking. Therefore, it can realize high yield and lower cost of packaging. Flexibility in the selection of chip size and mixed technology devices is offered. Many of the needed processes and tool capabilities exist, although much opportunity exists for further enhancement.

The stacked chip-on-chip option is extended further with the integration of flip chip attachment of the top chip with area array solder bumps directly to the bottom chip, offering shorter chip to chip interconnects. Bump pitch can be reduced further from the typical 150µm C4 pitch currently in production to only a few tens of microns and can potentially make chip to chip interconnect comparable to that within a single chip.

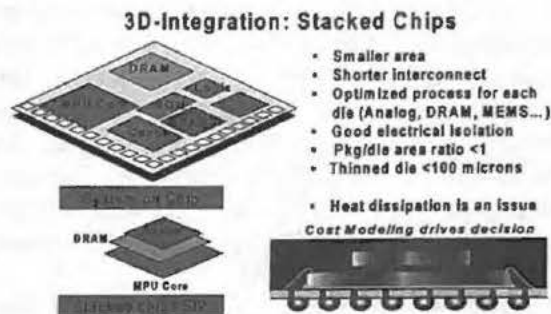


Fig: 2 Stacked chips

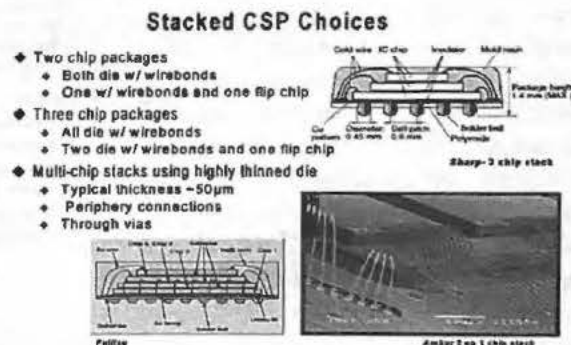


Fig: 3 Stacked chips wire bonded

Another interesting approach of flip chip solder bonding was recently announced by Infineon Technologies [11]. The technique named "SOLID" (Solid Liquid Inter Diffusion) bonding technique joins ICs face-to-face to form a "sandwich" chip system. The upper and lower sides of the "sandwich" chips are coated with a $\sim 5\mu\text{m}$ layer of copper redistribution layer and patterned to form via pads. The copper metal on the top wafer is coated with tin of $\sim 3\mu\text{m}$ thickness. Both chips are soldered together at a temperature of 270°C and 3 bar of pressure to create a permanent bond. Wire bonds from the bottom chip connect the combined stack to the package. The wafers are thinned to $\sim 60\mu\text{m}$ so the combined chips meet the package thickness requirements.

While stacked chip devices are in production, many technology enablers are being developed for wider product applications and performance enhancements. These include wafer level chip size package (WL CSP) process, ultra-thin wafer-process, re-distribution metallization, and high precision placement technology. While WL CSP has been pursued as a low cost packaging technology, this offers additional capabilities for stacked chips. Device-protecting passivation technology, and area array bump formation technology can be leveraged for stacked chips. A WL CSP with high-density area array interconnects with 12000 I/O /cm², dubbed "sea of leads" capability has been demonstrated [12]. This technology offers a capability amenable to stacked flip chips, providing high interconnect density, passivation protection and cost leverage.

Adopting the principle of embedding thinned chips in organic build-up dielectric layers further extends the stacked chip approach. This approach drives technology enablers such as wafer thinning, redistribution interconnects, inter-chip planarization, precision placement etc. Fraunhofer IZM's Chip in Polymer (CIP)[13] and Fujitsu's Chip Size Module™ (CSM) are examples. A schematic of Fujitsu's CSM is shown in fig 4. This approach drives wafer thinning and redistribution interconnection capability.

With the focus on SoC, the importance of integrating passive components such as capacitors, resistors, and inductors is easily overlooked. Individual component reduction requirements are growing more stringent for portable communication devices. The SiP approach offers capability for integrating passive components in 3D. In contrast to the standard integration techniques in which discrete passive components are mounted onto the surface of the PCB, opportunity exists for these components to be embedded in package substrates or in the inter-chip planarization layer in the stacked chip configuration. Equivalent or superior electronics functionality can be achieved by this integration approach and offers significant advantages in size, performance, cost and manufacturability. Multilayer ceramic technology with low temperature cofired ceramic or multilayer organic board technology is used for embedding these passives. Stacked chips are attached to these substrates to provide more integrated system functionality. An emerging approach is to embed passives in the CSM or CIP mentioned above. Opportunities exist in developing new materials and processes for passives compatible with 3D integration and which provide improved performance, especially for systems for portable communication.

Stacked Die Technology Trends

- ◆ Embed thin, stacked die in polymer build up layers
(eg: Chip in Polymer (CIP) Fraunhofer IZM, Chip Size Module™ (CSM) Fujitsu —)
- ◆ Stacked chip memory device
- ◆ Extending to logic devices
- ◆ Combining:
 - ◆ Wafer level chip size package (WL CSP) processes
 - ◆ Wafer thinning: thickness $\rightarrow 50\mu\text{m} \rightarrow 25\mu\text{m}$
 - ◆ High precision placement technology
 - ◆ Interchip planarization
 - ◆ Re-distribution interconnects
 - ◆ Embedded passive components

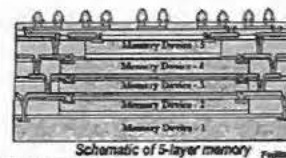


Fig: 4. 3D stacked chip module

In view of the worsening interconnect delay issues in future ICs with Cu/low k, exploratory work is ongoing in optical interconnects applied to on-chip and chip-to-chip communication. While progress is being made in optical component technologies of microlasers, optical detectors with silicon CMOS, waveguides, etc many hurdles exist in integrating these in a 2D silicon IC. It is generally believed that the first integration will be using a hybrid approach involving 3D. Free-Space Optical Interconnect (FSOI) that relies on flip-chip bonded VCSEL arrays and detectors, on CMOS circuits for chip-to-chip communication [14, 15,16] is being explored. While this may appear within reach of implementation, huge challenges remain in developing a cost effective, manufacturable process for high volume production.

3D STACKED WAFERS

3D integration by wafer bonding and through silicon interconnect is a promising approach being explored currently [17,18,19]. Processed wafers are aligned and bonded using dielectric polymer such as BCB, either wafers face to face or back to face. High aspect ratio vias are etched through the thinned top silicon wafer followed by copper fill and CMP. Wafers being bonded have to be of the same size and chips of same size on both wafers, which could be a constraint. Four key process challenges

need to be tackled: wafer alignment, bonding, wafer thinning and handling and deep via through multilayer structures. However, all these processes are compatible with back end processes. While wafer-bonding technology has been studied for decades, the knowledge needs to be adapted to the present situation. While alignment capability needs to be improved, 0.5 μm capability has been demonstrated. Wafer thinning and handling is a generic need in many applications and progress is being made. Through-silicon-via process is a major challenge with all the requirements associated with copper processing. Forming and maintaining the electrical isolation layer between the through-silicon copper and the silicon substrate is critical to the success of the manufacturing process-flow. The stacked wafer 3D approach is attractive from the standpoint of its capability in fine pitch interconnects between wafers and compatibility with wafer fabrication infrastructure, although additional process complexity is involved. Die size restriction, and cumulative yield of the wafer stack (the product of the individual wafer yields) are deterrents.

An alternate approach to dielectric polymer bonding is to use copper metal to metal bonding of two wafers [20,21]. The primary distinction is in the choice of the bonding layer, while the majority of process requirements, constraints and issues are common to both approaches. Bonding of 200mm wafers is difficult but has been demonstrated using Cu to Cu bonding at temperature of $\sim 400^\circ\text{C}$. The copper bonding layer, in addition to serving as chip to chip interconnect, could potentially be used as a thermal spreader and as a ground plane to provide

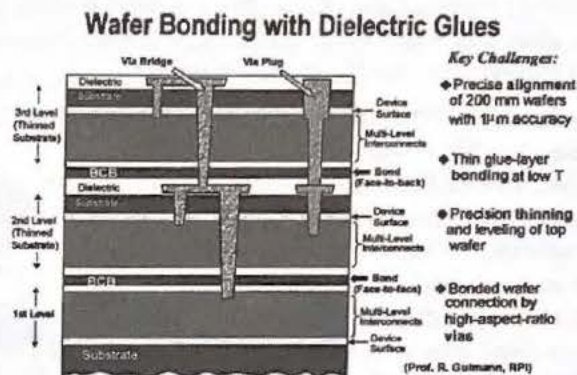


Fig: 5 Stacked wafers

substrate coupled noise isolation. The effects of thermal stress on copper via due to the thermal mismatch between copper and silicon need to be evaluated in assessing system reliability.

3D MULTILAYER DEVICES

Integration in the front end

3D CMOS devices built on multiple layers of silicon are attractive from the point of view of fabrication on the same wafer. Low temperature selective epitaxial growth (SEG) and epitaxial lateral overgrowth (ELO), coupled with CMP planarization could offer multiple silicon layers of device quality. The material and process technology for SEG and ELO has been under investigation for decades. There is renewed interest in the material technology and CMOS/BiCMOS devices grown on such material for 3D integration [22,23,24]. Using ELO, multiple layers of silicon-on-insulator devices can be fabricated on top of substrate devices on the same die. Devices on different planes are interconnected using buried refractory metals compatible with the 'front end' processes.

In spite of the extensive knowledge base in SEG and ELO, issues of selectivity of SEG and crystallographic defectivity remain. Other issues to be considered for a manufacturable technology include thermal budget in fabricating different planes of silicon, additional silicon area required for the SEG seed connection to the substrate, implant anneals, junction formation, high resistivity interconnects in the device planes, increased mask counts, epitaxy /CMP cost, thermal dissipation, etc.

Heteroepitaxial integration of III-V materials on Si to combine silicon devices and III-V devices has been a long lasting aspiration for researchers. Such a capability, if realized, would open up vast new opportunities in 3D integrated circuits and applications. Such heterogeneous integration could provide performance and capabilities that exceed the chip stacking approaches.

Specifically, integration of optoelectronic devices and high frequency RF devices, and overcoming scaled

CMOS limits, based on integrated materials, appear to be of great interest. Research in the materials integration continues and a number of research concepts hold promise for creating the material technology. An approach for growth of III-V on Si is to use a buffer layer between the grown layers and the silicon substrate to accommodate the lattice mismatch. The key step

Multi-Level SOI for 3D Integrated Circuits

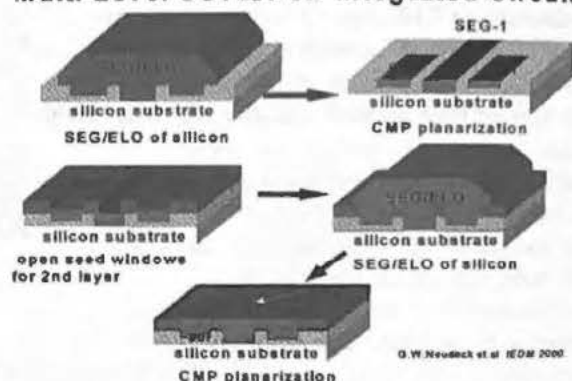


Fig: 6 3D devices on multilayer SOI

Heterogeneous Integration

- ◆ Heteroepitaxial Integration of III-V materials on Si
- ◆ Combine the unique strengths of each in electrical and optical performance

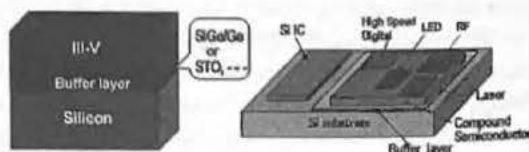


Fig: 7. Integration of III-V devices

appears to be in tailoring the buffer layer for defect free epitaxy. Two buffer layer systems which reportedly have given encouraging results in high quality III-V heteroepitaxy, are SiGe/Ge [25] and strontium titanate (STO) [26]. GaAs layer grown on SiGe/Ge has given epitaxial layer of 'acceptable defectivity' [25]. In addition to material integration of this system, a monolithically integrated laser/detector has been fabricated on the stacked layer. This shows promise for monolithically integrating optical interconnects and optodevices.

Integration in backend

Another interesting concept of multilayer device integration is to build active devices within an interconnect level. An obvious requisite is the ability to fabricate transistors that can be embedded in metal/dielectric levels with low temperature processing below $\sim 400^\circ\text{C}$. Such a 3-D architecture potentially offers interconnect performance and routing advantages. Devices built on recrystallized polysilicon (e.g.: laser recrystallized) have been a topic of study in the past. With pulsed laser recrystallization, polysilicon grains of a few microns have been fabricated with acceptable mobility. MOS transistors incorporating gate oxide formed at $\sim 100^\circ\text{C}$ also have been reported. New crystallization method using Ni or Ge seeding induced silicon crystallization and grain growth shows promise [27].

Another approach being explored is a low temperature Ge transistor fabrication and incorporating a high k gate dielectric. Excellent transistor properties and electrical stress reliability have been demonstrated with a low temperature ($<400^\circ\text{C}$) process. Such a transistor could be integrated in the backend [28].

Another group of devices that can be integrated between metal layers is memory components. Matrix Semiconductor, INC., Santa Clara, CA., announced a write-once 3D-memory device where the memory elements of diode and antifuse are integrated between metal layers while the access transistors are built on the substrate [29]. Many of the emerging memory elements under development such as MRAM, polymer memory, etc use low temperature processing and will be integrated between backend metallization layers.

CHALLENGES AND OPPORTUNITIES

While much attention is placed on developing process technologies for 3D integration, device reliability aspects are only beginning to be addressed. Of particular need is to understand the mechanical stability of the integrated system, especially for the emerging wafer bonded approaches. The bond integrity and through-silicon-via stability on large wafers subjected to thermal stressing need to be understood. A major concern generic to all 3D approaches is the heat removal capabilities. Both total power dissipation and heat removal need to be assessed at a system level. Thermal modeling of 3D ICs is receiving good attention and the results have indicated that chip temperature increases in general, in the 3D approach [30,31]. The specific layout of different device layers in the stack can have a significant impact on the increase in temperature. New approaches are being explored in heat removal, such as spray cooling, microchannel cooling combined with electrokinetic pumping and thermoelectric cooling devices. Integration of such devices with 3D ICs amenable to high volume manufacturability will be of keen interest.

While multiple approaches are being pursued for 3D integration, each has its own strengths and issues. A comparison of these is made in Table 1. The choice of an approach for product implementation will depend on the application and cost/ performance attributes.

To fully exploit the potential benefits from 3D integration, a system level design methodology is needed. Assembling a few 'off-the-shelf chips' in a stack does

not do justice to the potential benefits that could be derived from 3D integration.

A methodology needs to be developed for partitioning different device layers and interconnects from a system performance standpoint. In addition to reducing die area by partitioning functions like memory, logic, and analog into separate layers, changes to the interface circuitry can produce a more efficient chip layout and superior performance. The design methodology should invoke chip and package together as an integrated system. This partitioning methodology must incorporate cost factors in addition to performance criteria. Together with the methodology, design tools for 3D integration need to be developed. A library of packaging and chip level interconnects capable of 'mix and match' in order to integrate a diversity of components and technologies must be available. Lastly, simulation, test and evaluation tools at the system level need development, which enable a much higher level of confidence that the design to be implemented will result in a fully functional system. It is also essential that as technology elements are integrated, organizational disciplines need to collaborate to provide a system solution.

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3D Approaches -- A Comparison (partial)

	Stacked Die	Stacked wafers	Multilayer devices
Strengths	• Mature process/tools • Each die optimized for cost/ performance • Die size flexibility • Commit only tested good die • Mixed device technologies • Heterogeneous integration • Faster System redesign	• Integrated Wafer processing • Fine pitch via/interconnects • Each wafer optimized for performance • Mixed device technologies	• Integrated wafer processing • Processes on same wafer • Self aligned / capable • Shorter interconnects • Mixed device technologies
Challenges	• Wafer thinning/ handling • Thermal management • Mechanical stability • Moderate interconnect pitch	• Process complexity • Same size die • Stacked wafer yield ($(\eta_1 \times \eta_2 \times \dots)$) • Wafer thinning/handling • Aggressive alignment target • Bond integrity • Si active area reduction • Thermal management	• Frontend / backend mix • Device 'good enough'? • Mask cost • Thermal process budget • Yield • Crystalline defects (ELO) • Epitaxy cost (ELO) • Thermal management

Table 1. 3D approaches: a comparison

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