IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Iihola et al.	
U.S. Patent No.:	11,716,816	Attorney Docket No. 50095-0199IP1
Issue Date:	August 1, 2023	
Appl. Serial No.:	17/364,593	
Filing Date:	June 30, 2021	
Title:	METHOD FOR MANUFACTURING AN ELECTRONIC MODULE AND ELECTRONIC MODULE	

DECLARATION OF DR. R. JACOB BAKER

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: 2/5/2025 By: _____

R. JACOB BAKER, PH.D., P.E.

APPLE 1003

Table of Contents

I. Materials Considered 5
II. Qualifications And Background 7
III. Relevant Legal Standards 10
IV. Technology Background 13
A. Semiconductor Components for Multi-chip Modules 13
B. Bonding Techniques 24
i. Ultrasonic Bonding 25
ii. Thermo-compression Bonding 26
V. Person of Ordinary Skill in the Art 26
VI. Overview of the Subject Patent US 11,716,816, "The '816 Patent" 28
VII. Prosecution History of the '816 Patent 30
VIII. Claim Construction 32
IX. Overview of Conclusions Formed 33
X. GROUND 1A – Tsubosaki010 in View of Tsubosaki405 Renders Obvious Claims 1-14 33
A. Tsubosaki010 Overview (APPLE-1005) 33
B. Tsubosaki405 Overview (APPLE-1011) 36
C. The Tsubosaki010-Tsubosaki405 Combination Overview 38
D. Analysis 43
i. Claim 1 43
ii. Claim 2 58
iii. Claim 3 59
iv. Claim 4 60

v. Claim 5 61

vi. Claim 6 62

vii. Claim 7 63

viii. Claim 8 64

ix. Claim 9 69

x. Claim 10 69

xi. Claim 11 70

xii. Claim 12 71

xiii. Claim 13 71

xiv. Claim 14 72

XI. GROUND 1B: Tsubosaki010 Renders Obvious Claims 1-14 74

XII. GROUND 2: Oya in View of Shugg Renders Obvious Claims 1, 3-4, 6-8, 10-11, and 13-14 75

A. Oya Overview 75

B. Shugg Overview 77

C. The Oya-Shugg Combination Overview 78

D. Analysis 81

i. Claim 1 81

ii. Claim 3 94

iii. Claim 4 95

iv. Claim 6 96

v. Claim 7 98

vi. Claim 8 99

vii. Claim 10 113

viii. Claim 11 115

ix. Claim 13 117

x. Claim 14 120

XIII. Additional Remarks 122

XIV. Listing of Claims 123

I, R. Jacob Baker, Ph.D., P.E., do hereby declare:

1. I have been engaged by Fish & Richardson P.C. ("Fish") on behalf of Apple, Inc. ("Apple" or "Petitioner") to provide my independent analysis of issues relating to the patentability of claims of U.S. Patent No. 11,716,816.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation in no way depends on the outcome of this proceeding or the content of my testimony.

I. MATERIALS CONSIDERED

3. In preparing this Declaration, I considered the following materials:

APPLE-1001	U.S. Patent No. 11,716,816 (the "'816 Patent")
APPLE-1002	Excerpts from the Prosecution History of the '816 Patent
APPLE-1004	U.S. Pub. 2004/0000710 A1 ("Oya")
APPLE-1005	U.S. Pub. 2002/0180010 A1 ("Tsubosaki010")
APPLE-1006	Shugg, W. Tillar, HANDBOOK OF ELECTRICAL AND ELECTRONIC INSULATING MATERIALS, 2nd Edition, Wiley-IEEE Press, 1995 ("Shugg")
APPLE-1007	U.S. Pub. 2003/0102572 A1 ("Nathan 1")
APPLE-1008	Scarlett, J.A., AN INTRODUCTION TO PRINTED CIRCUIT BOARD TECHNOLOGY, Electromechanical Publication Limited, 1984 ("Scarlett 1")

APPLE-1009	Scarlett, J.A., MULTILAYER PRINTED CIRCUIT BOARD HANDBOOK, Electromechanical Publication Limited, 1985 ("Scarlett 2")
APPLE-1010	Farr, I. V., "SYNTHESIS AND CHARACTERIZATION OF NOVEL POLYIMIDE GAS SEPARATION MEMBRANE MATERIAL SYSTEMS," Dissertation submitted to the Virginia Polytechnic Institute and State University (Jul 26, 1999).
APPLE-1011	U.S. Patent No. 5,714,405 ("Tsubosaki405")
APPLE-1016	Yu et al., "Surface characterizations of potassium-hydroxide-modified Upilex-S® polyimide at an elevated temperature," European Polymer Journal, Vol. 37, Issue 9, September 2001, pp. 1791-1799
APPLE-1019	Yamamoto et al., *A Composite Electrical Insulation in Superconducting Magnets*, 44 Advances in Cryogenic Eng'g (Materials) 239 (1998) ("Yamamoto")
APPLE-1020	U.S. Patent No. 6,709,897 ("Cheng")
APPLE-1022	U.S. Patent No. 11,071,207 ("Tuominen207")
APPLE-1024	U.S. Publication No. 2002/0159242 to Nakatani et al. ("Nakatani")
APPLE-1025	Japanese Patent Publication No. 1999-191574 to Matsuda with Certified Translation ("Matsuda")
APPLE-1026	U.S. Patent No. 4,068,022 to Glick ("Glick")
APPLE-1028	Simon Thomas, *3D-Integration: Trends and Opportunities – An Overview* (Materials Research Society 2003)

APPLE-1029	R. Kujala, et. al., *Solderless Interconnection and Packaging Technique for Embedded Active Components* (IEEE 1999)
APPLE-1030	U.S. Patent Publication No. 2001/0026010 to Horiuchi ("Horiuchi")
APPLE-1031	U.S. Patent No. 6,038,133 to Nakatani et al. ("Nakatani-II")
APPLE-1032	U.S. Patent No. 5,250,843 to Eichelberger ("Eichelberger")
APPLE-1033	International Patent Application WO1996012296 to Suwa et al. and Certified Translation ("Suwa")
APPLE-1034	U.S. Patent No. 7,609,527 ("Tuominen527")
APPLE-1105	Exhibit 18 to Complaint for Patent Infringement – Infringement Claim Chart for '816 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-17

II. QUALIFICATIONS AND BACKGROUND

4. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). My curriculum vitae is provided (as Appendix A).

5. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor of Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

6. I received a Bachelor of Science and Master of Science degrees in Electrical Engineering from UNLV, in 1986 and 1988, respectively. In 1993, I also received a Ph.D. in Electrical Engineering from the University of Nevada, Reno. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada Test Site. During this time, I designed, and oversaw the fabrication and manufacture of over 30 electronic and electronic-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics.

7. From 1997 to 1999, I served as a Consultant for Tower Semiconductor, in the design of CMOS integrated circuit cells for various modem chips, interfaces, and serial buses, including charging circuits based upon power up-down circuits using an MOS or bandgap reference, pre-amplifiers, and comparators. I was also a Senior Designer at Micron Technology from 1994 to 2008, working on the development of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, CMOS Image Sensors (CISs), and power supply design. My more recent industry experience includes working with

Freedom Photonics on the integration, fabrication, and design of optoelectronics with CMOS integrated circuits, including the design of compact optical transceiver for range finding applications, Geiger mode SiGe receiver for long-range communications, and packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies. I have worked as a consultant at other companies designing electronic circuits, including Sun, Oracle, Contour Semiconductor, Lockheed-Martin, and OmniVision.

8. I have taught courses in integrated circuit design (analog, digital, mixed signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, power electronics, and fiber optics. I have been the main advisor to over 100 Master's and Doctoral students.

9. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have also authored, or coauthored, more than 100 papers and presentations in the areas of electronic circuit design. I am the named inventor on over 150 granted U.S. patents.

10. I have received numerous awards for my work, including the Frederick Emmons Terman (the "Father of Silicon Valley") Award. The Terman

Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession.

11. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

12. I have received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University.

13. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award four of the years I have been at UNLV.

14. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching integrated circuit packaging and my knowledge of electrical circuit design and fabrication and electrical engineering fundamentals. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person having ordinary skill in the art.

III. RELEVANT LEGAL STANDARDS

15. I have been asked to provide my opinions as to whether claims 1-14 of the '816 Patent would have been obvious to a person of ordinary skill in the art

as of the earliest claimed priority date of the '816 patent, which I understand is September 18, 2003 ("Critical Date").

16. I am an engineer by training and profession. The opinions I express in this declaration involve the application of my technical knowledge and experience to the evaluation of certain prior art with respect to the '816 patent. In addition, I understand that the following legal principles apply.

17. It is my understanding that, in determining whether claims of the '816 patent are obvious in this proceeding, the claim terms are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the relevant art. A person of ordinary skill in the art would read the claim terms in the context of the entire patent specification in which they appear, as well as the prosecution history of the patent.

18. It is my understanding that a claim is unpatentable under 35 U.S.C. § 103 if the claimed subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the alleged invention. I also understand that an obviousness analysis takes into account the scope and content of the prior art, the differences between the claimed subject matter and the prior art, and the level of ordinary skill in the art at the time of the invention.

19. In determining the scope and content of the prior art, it is my understanding that a reference is considered relevant prior art if it falls within the field of the inventor's endeavor. In addition, a reference is prior art if it is reasonably pertinent to the particular problem with which the inventor was involved. A reference is reasonably pertinent if it logically would have commended itself to an inventor's attention in considering his problem. If a reference relates to the same problem as the claimed invention, that supports use of the reference as prior art in an obviousness analysis.

20. To assess the differences between prior art and the claimed subject matter, it is my understanding that 35 U.S.C. § 103 requires the claimed invention to be considered as a whole. This "as a whole" assessment involves showing that one of ordinary skill in the art at the time of invention, confronted by the same problems as the inventor and with no knowledge of the claimed invention, would have selected the elements from the prior art and combined them in the claimed manner.

21. It is my further understanding that several rationales may be applied for combining references or modifying a reference to show obviousness of claimed subject matter. These rationales include: combining prior art elements according to known methods to yield predictable results; simple substitution of one known

element for another to obtain predictable results; a predictable use of prior art elements according to their established functions; applying a known technique to a known device (method or product) ready for improvement to yield predictable results; choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify a prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. TECHNOLOGY BACKGROUND

A. Semiconductor Components for Multi-chip Modules

22. Persons of Ordinary Skill In The Art (POSITAs) have continuously looked for solutions to provide multiple component integration into electronic modules to provide higher levels of system functionality without added signal delay and power dissipation in order to integrate components (such as transistors) in integrated circuits in accordance with Moore's law. APPLE-1036, Abstract. As Simon Thomas explained, "[t]he growth of the semiconductor industry has historically depended on the integration of more components on a chip through transistor and interconnects scaling and manufacturing technology." Thomas describes that functionality has increased through "System-on-Chip (SoC) and System in Package (SiP) approaches." *Id*.

In addition, the increasing drive to integrate diverse component technologies for enhanced SoC functionality, presents a multitude of technical and business challenges. For example, a single chip SoC for a cell phone handset could require GaAs, MEMS, digital, analog, power, and passives technologies. RF circuits integrated with microprocessor in a 3D format, to facilitate wireless communication, has attracted major interest. Another motivation for 3D is the need to reduce footprint of the packaged device, especially for portable applications. There are multiple technology approaches for 3-D integration, currently at varying levels of maturity and each with its own unique strengths and issues. These approaches include [Fig: 1]: - Stacked chips or stacked packages - Stacked wafers through wafer bonding - Device fabrication in multiple planes on the same wafer.

APPLE-1036, 2.

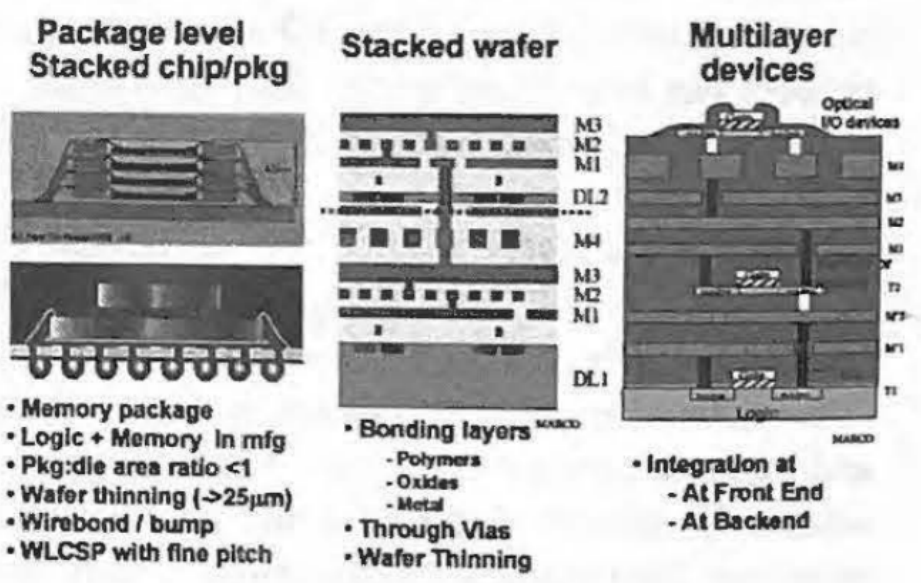


Fig: 1. Schematic of 3D integration schemes.

APPLE-1036, 2

23. Nakatani-II exemplifies how stacking multiple wafers on top of each other was a well-known technique for achieving multiple component integration in a module. For example, Nakatani-II's Figure 4 shows a three-layered "built-in module":

> Referring to FIG. 4, the circuit component built-in module 400 in Embodiment 4 includes an insulating substrate 401 comprising insulating substrates 401a, 401b and 401c, wiring patterns 402a, 402b, 402c and 402d formed on one principal plane and in the internal portion of the insulating substrate 401, a circuit component 403 arranged in the internal portion of the insulating substrate 401 and connected to the wiring patterns 402a, 402b or 402c, and an inner via 404 for electrical connection between the wiring patterns 402a, 402b, 402c and 402d.

APPLE-1039, 11:12-22.

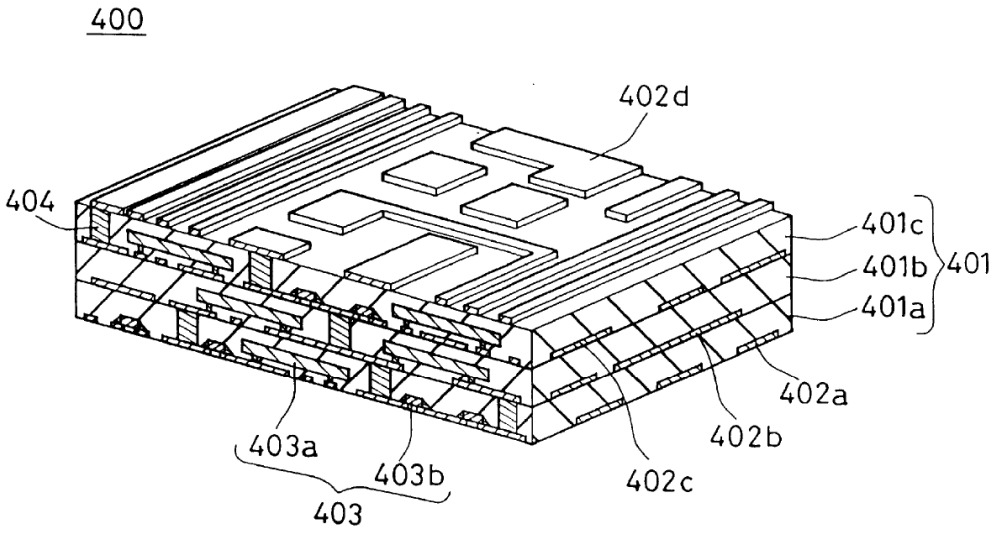
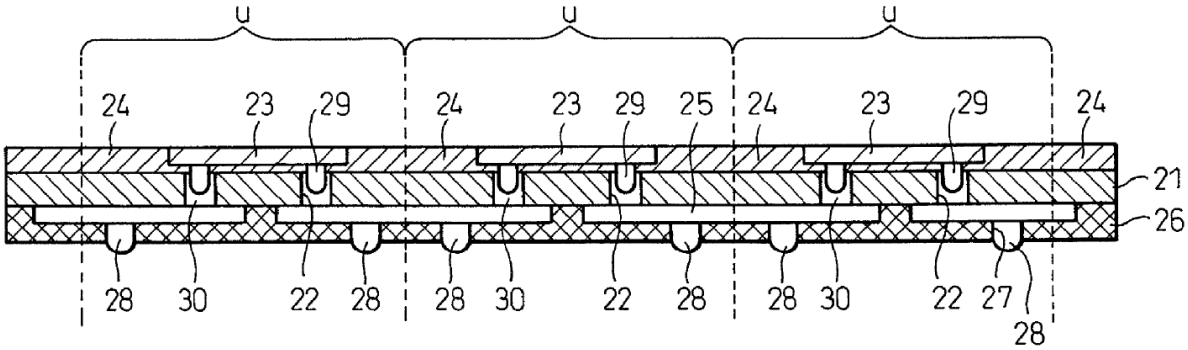


FIG. 4

APPLE-1039, FIG. 4

24. "A plurality of semiconductor devices… may be stacked in layers… to form a thin multilayer semiconductor device" in U.S. Patent Application Publication No. 2001/0026010 to Horiuchi et al. ("Horiuchi"). APPLE-1038, [0105]. Horiuchi describes a method including producing an initial structure containing multiple electrical components which are then "cut into semiconductor package units 'u'… to obtain individual semiconductor devices 20." *Id*., [0101], [0115], [0127], [0143], [0154]. For example, Horiuchi's Figure 9 (reproduced below) shows semiconductor elements 23 which are bonded and mounted to the top surface of the tape substrate 21 "by heating the semiconductor elements 23 to a temperature near the melting point of the low melting point metal 30 and pushing the connection terminals 29 into the low melting point metal 30 in the through holes 22." *Id*., [0094]. "A sealing resin layer 24 covering the top surface of the tape substrate 21" is then ground and polished to a predetermined thickness. *Id*., [0097]-[0099]. After the grinding and polishing, the external connection terminals 28 are formed and the "assembly is cut into semiconductor package units 'u' at the positions shown by the broken lines in FIG. 9 to obtain individual semiconductor devices." *Id*., [0100]-[0101].

Fig.9



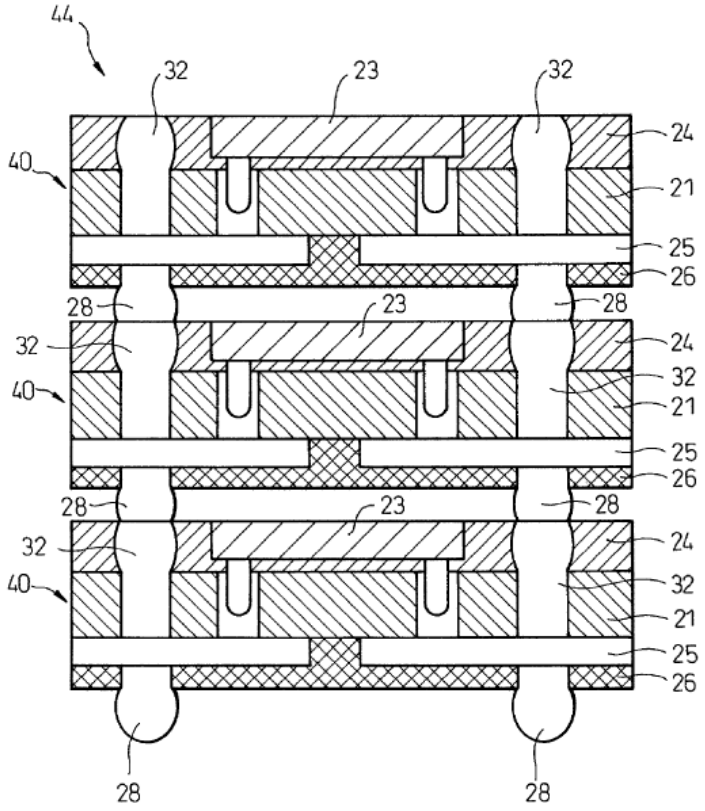
APPLE-1038, FIG. 9

25. Following the cutting procedure, Horiuchi's cut semiconductor devices "may be stacked in layers as shown in FIG. 11 to form a thin multilayer semiconductor device 44" by:

> connecting the top ends of the low melting point metal conductors 32 of a bottom semiconductor device 40 and the bottom ends of the external connection terminals 28 of a top semiconductor device 40, a single semiconductor device 4 comprised of an integral circuit including a plurality of semiconductor elements 23 (in this example, three) in a multilayer structure is formed.

APPLE-1038, [0105].

Fig.11



APPLE-1038, FIG. 11

26. As Thomas notes, "[a]nother interesting concept of multilayer device integration is to build active devices within an interconnect level." APPLE-1036, 6-7. This type of technology had "become increasingly attractive" during the 90's. APPLE-1029, 1. For example, in 1999, A. Kujala, R. Tuominen, and J.K. Kivilahti, explained that, "General Electric (GE) introduced high density interconnection technology for embedded chips. HDI technology is a 'chip first' solution where active components are placed in cavities formed in a ceramic or

embedded into plastic encapsulant." APPLE-1037, 1. As shown below in Figure 2, the chips are interconnected through laser ablated vias. *Id*., 2. "The HDI technology enables the fabrication of complex [multi-chip modules] with a very high packaging density and low interconnect impedance" while providing "good protection both mechanically and chemically." *Id*.

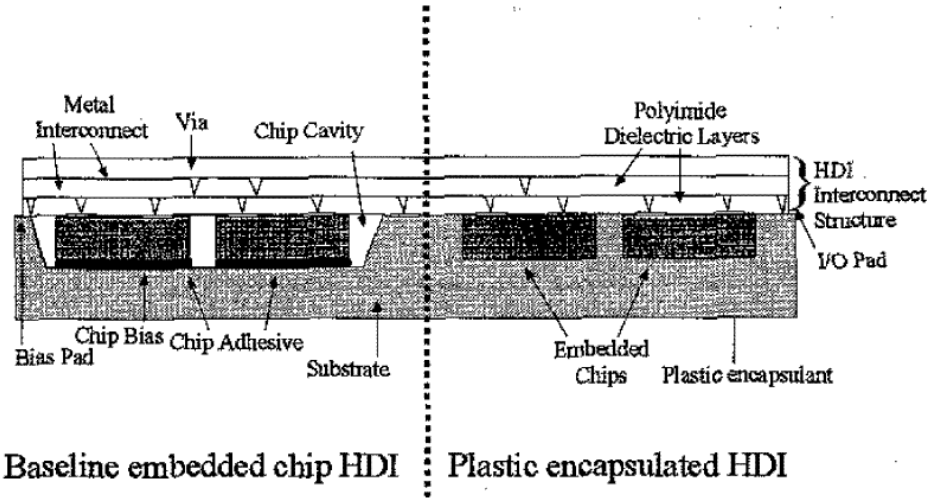


Fig. 2 Schematic presentation of embedded HDI chips [5].

APPLE-1037, FIG. 2

27. For example, Nakatani, Eichelberger, Suwa, and Nakatani-II show mounting multiple chips in a single layer. Specifically, due to the increased demand for smaller-sized higher-density circuit boards, Nakatani discloses "at least two electric elements (203) such as semiconductor chips or surface acoustic wave devices … mounted on wiring patterns." APPLE-1007, Abstract, [0003], [0017]

("In FIG. 7, numeral 601 denotes surface acoustic wave devices…"), [0127]; *see also infra* §X.A. Nakatani's "first wiring patterns 609 and [] metal bumps 605 are electrically connected" using "heat and ultrasonic wave[s]" to melt the metal bumps 605 for the connection of the components (surface acoustic wave devices 601) with the circuit board. *Id.*, [0016], [0020], [0125]. Nakatani describes that by including a plurality of components in a single layer, the semiconductor package's thickness is improved by having the multiple thin chips successfully mounted on a thinner substrate. *Id.*, [0011]-[0012].

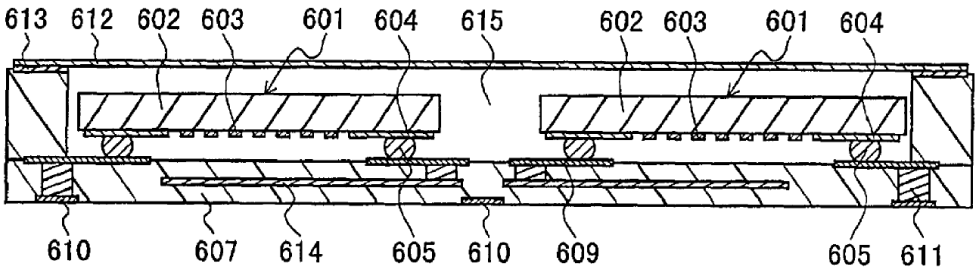
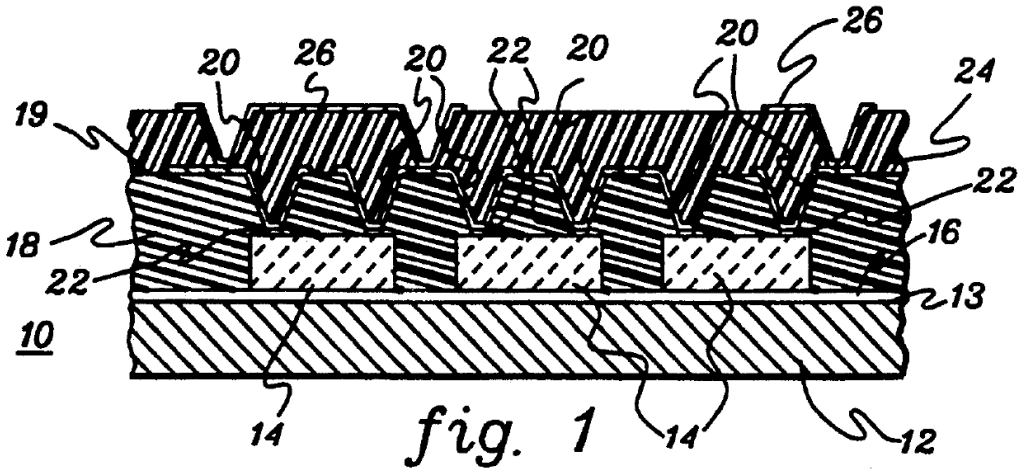


FIG . 7
PRIOR ART

APPLE-1007, FIG. 7

28. Similarly, U.S. Patent No. 5,250,843 to Eichelberger discloses a "multichip integrated circuit package comprises a substrate having a flat upper surface to which is affixed one or more integrated circuit chips having

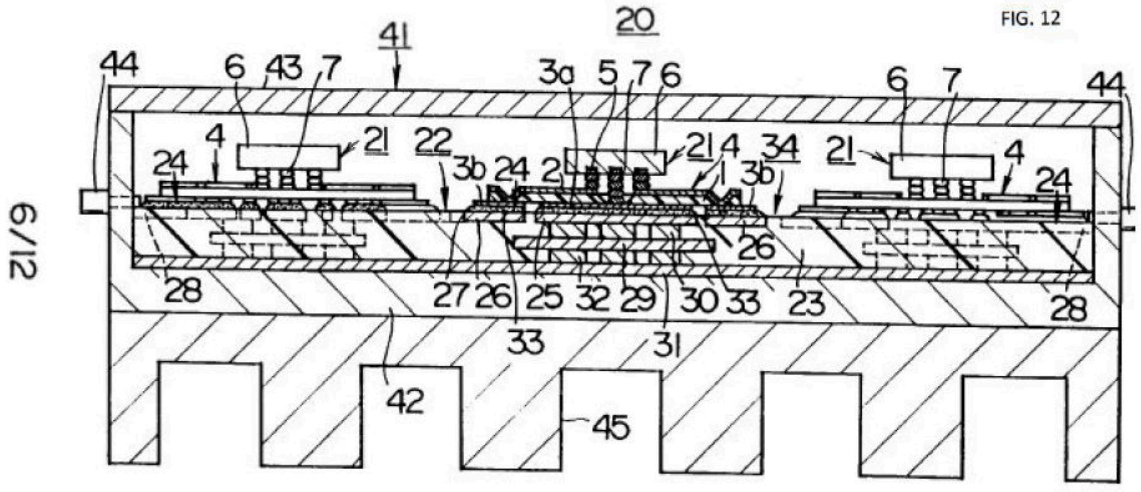
interconnection pads." APPLE-1040, Abstract. As shown below in Figure 1, Eichelberger's multichip module includes multiple semiconductor components 14 arranged in one single layer. Eichelberger's multichip module structure has high I/O capacity with optimal heat removal, has been optimized for speed, and has the ability to incorporate an assortment of components of varying thickness and functions into the module. *Id.*, 1:17-27.



APPLE-1040, FIG. 1

29. International Patent Application WO1996012296 to Suwa et al. ("Suwa") also discloses a multi-chip module. *See* APPLE-1041. Suwa's multi-chip module (MCM) 20 is provided with a plurality of chip assemblies 21 "in which the IC chip 6 is facedown-bonded to the tape 4." *Id.*, 12. "A plurality (four in the illustrated example) of the chip assemblies 21 is used in the MCM 20, and

passive elements and active elements are incorporated into each chip assembly 21." *Id.*, 12-13.



APPLE-1041, FIG. 12

30. Suwa describes that since the IC chips 6, are "mounted on the wiring board 22 via the tape 4 with a thickness of approximately 50 μm, the level difference between the wiring board 22 and the IC chip 6 can be extremely minimalized, and therefore a drop in the impedance can be suppressed when a high-speed signal is transmitted, and impedance matching of the highspeed signal line 2b can be easily ensured." APPLE-1041, 16. Furthermore, Suwa describes that since "IC chip 6 is surface-mounted in the wiring board 22 in the chip assembly 21, no cavity needs to be formed in the wiring board 22, and therefore

the manufacturing costs of the wring board 22 as well as of the MCM 20 can be reduced." *Id*.

31. As I explained above, Nakatani-II also exemplifies multiple components in a single insulating substrate layer. As shown in Figure 1, Nakatani-II's circuit components 103 are "connected to the wiring pattern 102b and arranged in the insulating substrate 101, and an inner via 104 for electric connection between the wiring patterns 102a and 102b." APPLE-1039, 6:67-7:3.

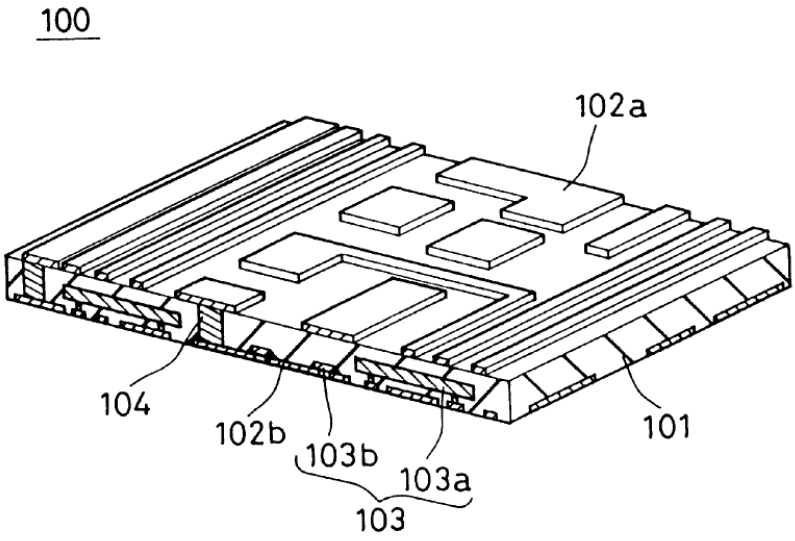


FIG. 1

APPLE-1039, FIG. 1

32. In summary, it was well-recognized by POSITAs to mount a plurality of chips on a substrate, and further to stack a plurality of chip modules accordingly.

B. Bonding Techniques

33. Preparation of a semiconductor package or chip requires that components be electrically connected to wiring patterns on a printed circuit board or other substrate, so that the package or chip can be supplied with power and be grounded, as well as connecting the package or chip to other components. APPLE-1022, 1 ("A printed circuit board is a piece of plastic material on which electronic components can be mounted for mechanical support, and which also electrically interconnects all the components it supports by means of a pattern of metal tracks on its outer surfaces and sometimes on inside layers"). By the Critical Date, a variety of techniques for bonding components to wiring of printed circuit boards were well known and in use, including solderless techniques including ultrasonic bonding and thermocompression. *See e.g.,* APPLE-1037 (1999 article in IEEE reporting on "Solderless Interconnection and Packaging Technique for Embedded Active Components"). The '816 patent does not purport to have invented these techniques, and indeed, ultrasonic and thermocompression bonding techniques (*i.e.,* "solderless techniques") were well-known years before the filing date of the '816 patent. *Id.*; APPLE-1001, 6:46-48 ("Methods and devices for creating

ultrasound joints (ultrasonic bonding) are commercially available."), 6:63-65 (Methods and devices for making thermo-compressed joints (thermo-compression bonding) are also commercially available").

i. Ultrasonic Bonding

34. The Tuominen patent offers the following description of ultrasonic bonding:

> The ultrasonic method then refers to a method, in which two pieces containing metal are pressed against each other while vibration energy at an ultrasound frequency is brought to the area of the joint. Due to the effect of the ultrasound and the pressure created between the surfaces to be joined, the pieces to be joined are bonded metallurgically. Methods and equipment for ultrasonic bonding are commercially available. Ultrasonic bonding has the advantage that a high temperature is not required to form a bond.

APPLE-1034, 6:41-49.

35. Ultrasonic bonding techniques combine ultrasonic vibrations and heat or pressure to bond two metal components to one another. For example, Matsuda describes a technique that combines ultrasonic methods with thermocompression. Matsuda describes that electrodes 4 of a semiconductor chip are aligned with metal bumps 5 (*e.g.,* Ni or Au) formed on a substrate and then the pieces are "subjected to pressure by a bonding tool while applying ultrasonic vibrations and heat." APPLE-1009, [0007], [0006], [0012]. "The bumps 5 are deformed to form an

Au/Al alloy on the contact surface, and the chip electrodes 4 and bumps 5 are thermocompressed." *Id.*, [0007], [0013], FIGS. 2A-B.

ii. Thermo-compression Bonding

36. Similarly, the '816 patent gives the following description related to thermo-compression bonding methods:

> The term thermo-compression method refers in turn to a method, in which two pieces containing metal are pressed against each other while thermal energy is brought to the area of the joint. The effect of the thermal energy and the pressure created between the surfaces to be joined cause the pieces to be joined to be bonded metallurgically. Methods and equipment for thermo-compression bonding are also commercially available.

Id., 6:58-65.

37. Glick explains that " [t]hermocompression bonding is a solid-phase bonding technique which forms the bond between two members by inducing a suitable amount of material flow in one or both members." APPLE-1020; 3:33-36. "[M]aterial flow [between the two members] is induced by the application of heat and pressure, which are maintained for a suitable length of time so that adhesion takes place without the presence of a liquid phase." *Id.*, 3:36-39.

V. PERSON OF ORDINARY SKILL IN THE ART

38. It is my understanding that when interpreting the claims of the '816 patent I must do so based on the perspective of the POSITA. For purposes of my

analysis in this declaration, as noted above, I have been asked to assume that the priority date of the '816 patent is September 18, 2003 ("Critical Date"). I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

39. Taking these factors into consideration, it is my opinion that one of ordinary skill in the art would have had a Bachelor's degree in electrical engineering, materials science, applied physics, or a related technical field, and 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. Additional graduate education could substitute for professional experience, or additional professional experience could substitute for formal education.

40. I possessed the qualifications of a POSITA since the Critical Date of the '816 patent, and long before.

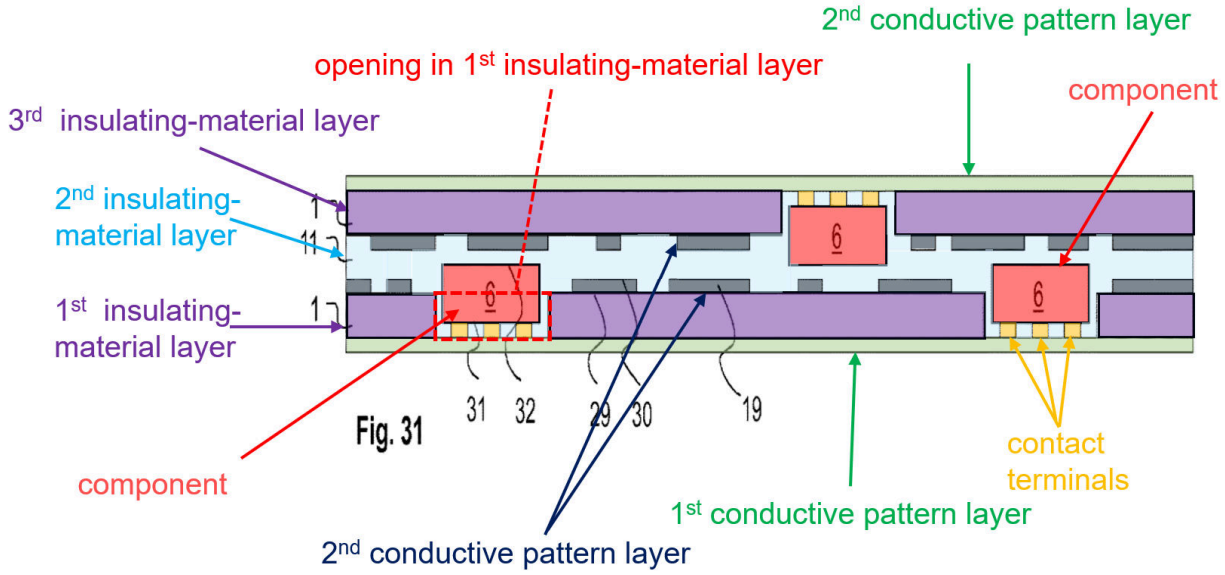
VI. OVERVIEW OF THE SUBJECT PATENT US 11,716,816, "THE '816 PATENT"

41. The '816 patent is titled Method for manufacturing an electronic module and electronic module, filed as U.S. Application No. 17/364,593 (the " '593 application"). It was filed on June 30, 2021 as a continuation of U.S. Application No. 16/788,701 (filed on February 12, 2020, which is a Continuation of U.S. patent application Ser. No. 14/580,257, filed on Dec. 23, 2014, which is a Continuation-in-Part of U.S. patent application Ser. No. 10/572,340, filed on Sep. 15, 2004). APPLE-1001, Cover. Although not listed on the cover of the '816 patent, the U.S. priority application was filed as a U.S. national stage entry of PCT/FI2004/000053 (filed September 15, 2004). APPLE-1002, 53. The '816 application also claims priority to Finnish Application No. 20030167, filed on April 2, 2003. *Id.*

42. The '816 Patent generally describes techniques for fabricating "electronic modules" containing a semiconductor chip, or other component, embedded in an installation base such as a circuit board. APPLE-1001, 1:28-33. The specification explains that "[e]mbodiments of the invention are based on commencing manufacture [of the electronic module] from an insulating board, which is surfaced on at least one side with a conductive layer." APPLE-1001, 3:21-23. "After this, a recess or opening is made in the insulation, which opens

onto one surface of the board, but does not penetrate the conductive layer on the opposite surface of the board." *Id.*, 3:23-26. "A component is attached to the recess or opening and electrical contacts are formed between the conductive layer and the contact areas, or contact protrusions of the component." *Id.*, 3:26-29. "After the attachment of the component, conductive patterns are formed from this conductive layer, which become part of the circuit-board structure, or other electronic module." *Id.*, 3:29-32; *see also id.*, 3:16-4:9 (discussing alleged advantages of the designs disclosed in the '816 Patent).

43. By way of example, FIG. 31 depicts one embodiment of an electronic module disclosed in the '816 Patent:



APPLE-1001, FIG. 31 (annotated)[1]

44. As shown above, the disclosed module includes a first insulating material layer 1 toward a bottom portion of the module, a second insulating material layer 11 around a middle portion of the module, and a third insulating material layer 1 toward a top portion of the module. APPLE-1001, 13:3-61; *see also id.*, 5:20-26, FIGS. 30-31. First and second conductive pattern layers are formed on opposite sides of the first and third insulating material layers, respectively. *Id.* The first and third insulating material layers further include openings sized to receive components 6 (*e.g.,* semiconductor chips), thereby permitting electrical connection of the contact terminals of the components 6 to the first or second conductive pattern layers. *Id.*

VII. PROSECUTION HISTORY OF THE '816 PATENT

45. I have reviewed the file history of U.S. Application No. 17/364,593 ("the '593 application), from which the '816 patent issued.

46. I understand that the application was rejected only one time during prosecution. In the only Office Action issued during prosecution of the

[1] While the metal conductive layers (shaded green) are shown as continuous surfaced material in FIG. 30, they are later patterned to form the first and second conductive pattern layers according to the processes described in the '816 Patent. APPLE-1001, 13:3-61; *see also id.*, FIGS. 36-38.

application, the Examiner The office action rejected each of the independent claims and most dependent claims pending at the time as anticipated by Cheng (APPLE-1020). APPLE-1002, 19-25. Two dependent claims were identified as reciting allowable subject matter, however. APPLE-1002, 25-26. These claims recited that "the first conductive pattern layer and the second conductive pattern layer are each substantially planar." *Id.* The applicant responded to the action by amending the independent claims to incorporate language based on the features recited in the allowable dependent claims:

> 1. (currently amended) An electronic module, comprising:
>
> a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
>
> at least one opening in the first insulating-material layer that extends through the first insulating-material layer;
>
> a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;
>
> a second insulating-material layer disposed on the first insulating-material layer; and
>
> a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers,
>
> wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

APPLE-1002, 2-3; *generally id.*, 11-16.

47. Following the applicant's response, the examiner agreed to allow the application in a notice of allowance dated March 13, 2023. APPLE-1002, 3-10. As Grounds 1A-2 of this Petition demonstrate, however, the '816 Patent never should have been allowed. The conventional features recited in the Challenged

Claims—including "substantially planar" conductive pattern layers—were all well known in the prior art before the alleged invention, and the claims fail to recite these features in any innovative or non-obvious arrangement.

48. However, as I will discuss below, all features recited in the Challenged Claims are disclosed in one or more of Tsubosaki, Oya, and Shugg, none of which were considered by the Office or cited in the Office Action, and the claimed combinations of these features would have been obvious before the Critical Date.

VIII. CLAIM CONSTRUCTION

49. I do not believe that any term requires explicit construction. I understand that claim terms in an *inter partes* review proceeding are given their plain and ordinary meaning in light of the specification and file history. For purposes of my analysis in this declaration, I have applied claim interpretations consistent with the patent owner's allegations of infringement against Apple in the parallel district court proceeding. *See* APPLE-1105.

50. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions that are raised in the parallel district court proceeding.

IX. OVERVIEW OF CONCLUSIONS FORMED

51. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-14 of the '816 patent are rendered obvious by Tsubosaki010 in view of Tsubosaki405.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-14 of the '816 patent are rendered obvious by Tsubosaki010.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1, 3-4, 6-8, 10-11, and 13-14 of the '816 patent are rendered obvious by Oya in View of Shugg.

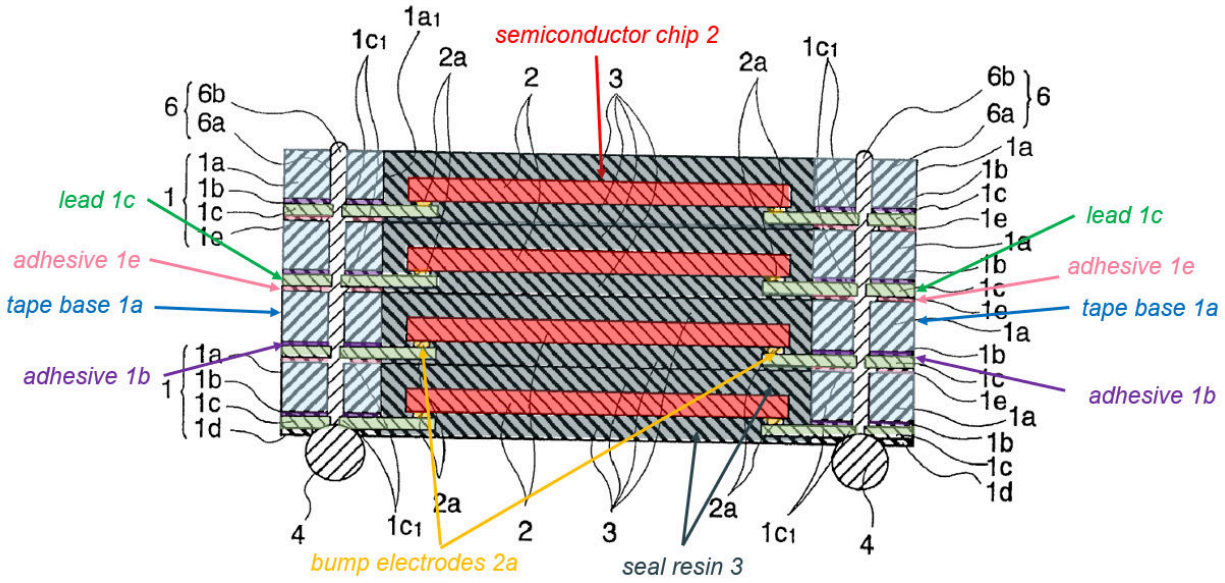
X. GROUND 1A – TSUBOSAKI010 IN VIEW OF TSUBOSAKI405 RENDERS OBVIOUS CLAIMS 1-14

A. Tsubosaki010 Overview (APPLE-1005)

52. Tsubosaki010's disclosure "relates generally to semiconductor devices and manufacturing methodology thereof, and more particularly to technologies usefully applicable to high-density mountable semiconductor devices

with tape carrier package (TCP) structures along with fabrication methods thereof." Tsubosaki010, ¶[0011]. "The TCP is a package structured including a tape carrier having a plurality of conductive leads formed thereon in a repeated pattern, wherein a semiconductor chip is placed on or in the tape carrier with its electrode pads lamination-contacted with corresponding ones of the carrier leads for electrical interconnection therebetween, the semiconductor chip being sealed by a sealing resin or the like." Tsubosaki010, ¶[0003]. For example, a unitary TCP can include "a semiconductor chip 2 [] disposed within a device hole [1a1] as formed in a tape base material 1a of a tape carrier 1, which chip is less in thickness than the tape base material 1a." Tsubosaki010, Abstract; *see also id.*, ¶[0062].

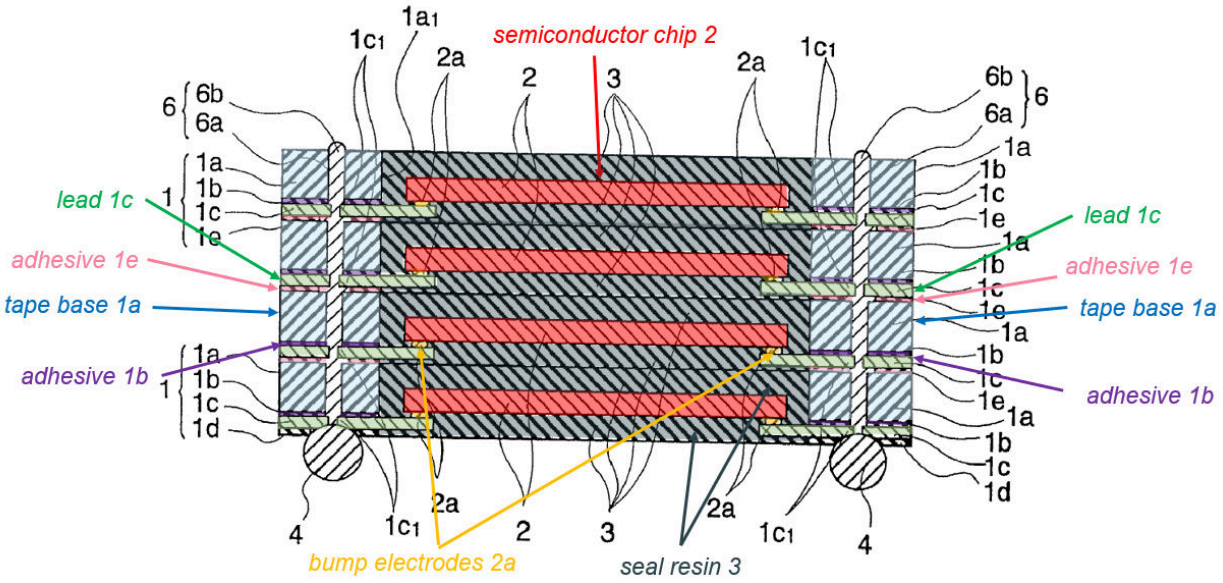
53. With reference to FIGS. 14-21, Tsubosaki010 describes techniques for manufacturing "a multi-layered TCP structure" comprising a stack of unitary TCPs laminated atop each other. *See* Tsubosaki010, FIGS. 14-21, ¶¶[0108]-[0130]. The multi-layered TCP structure allows multiple unitary TCPs to be formed into a larger module comprising multiple semiconductor chips 2 with outbound leads that connect electrical terminals of the chips 2 to other circuit components and wiring. *Id.*, ¶¶[0108]-[0114].



APPLE-1005, FIG. 14

54. Tsubosaki010 explains that each TCP in the multi-layered structure includes a device hole 1a1 formed in a tape base 1a and adhesive layer 1b. *Id.*, ¶[[0116]. Copper film is bonded to the tape base 1a by the adhesive1b. The copper film is later etched to form a patterned layer comprising conductive leads 1c. *Id.*, ¶¶[0116]-[0117]; FIGS. 16-17. A semiconductor chip 2 is placed within the device hole 1a1 of the tape base 1a. *Id.*, ¶[0120]. The semiconductor chip 2's bump electrodes 2a and leads1c of the TCP are aligned and bonded to form an electrical connection. *Id.*, ¶[0120]. A layer of adhesive 1e that coats the top surface of the tape base 1a secures the stacked TCPs to each other to form the multi-layer TCP structure shown in FIG. 14 (sectional view) and FIG. 15 (plan view). *Id.* ¶¶[0111], ¶¶[0124]-[0125]; *see also id.*, ¶¶[0141]-[0154] & FIGS. 27-30

(describing option for sealing the semiconductor chips 2 in sealing resin 3 using a single molding process for the entire stacked structure). Tsubosaki010's Fifth and Seventh embodiments include substantially similar structures that map to the Challenged Claims in a generally equivalent manner.



APPLE-1005, FIG. 14

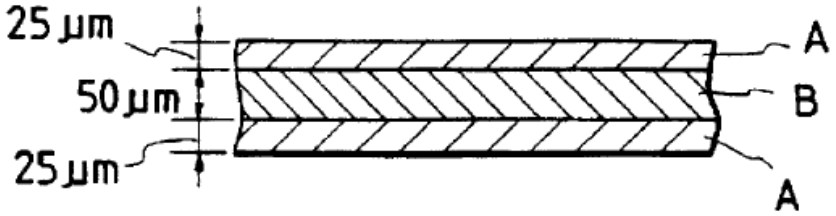
B. Tsubosaki405 Overview (APPLE-1011)

55. Like Tsubosaki010, Tsubosaki405 describes structures and uses of conventional carrier tapes for electronic packaging.[2] Tsubosaki405, Abstract. For example, Tsubosaki405 discloses "insulating adhesive films (tapes) 2, 7 … in the form of a tape having a thermosetting or thermoplastic single layer (an adhesive

[2] The first-named inventor on both Tsubosaki010 and Tsubosaki405 is Kunihiro Tsubosaki.

material only), or a double adhesive layer (not less than three layer construction)." Tsubosaki405, 7:33-41. "In the case of a three-layer insulating adhesive film 27 shown in FIG. 5, for instance, it is multilayer in construction, having a base B interposed between adhesive layers A, and composed of, *e.g.*, polyetheramideimide 25 μm/captone 50 μm/polyetheramideimide 25 μm." *Id.*, 7:35:40: *see also id.*, 7:40-41 ("In this case, any other polyimide film may replace the captone.").[3]

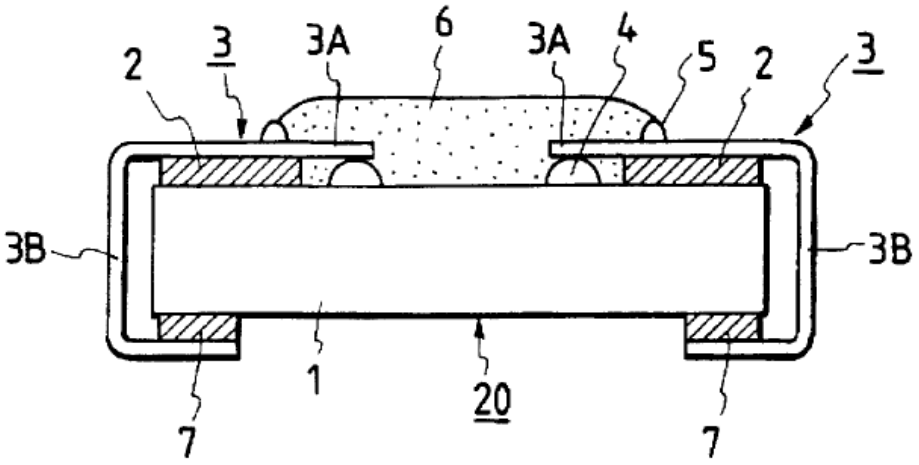
FIG. 5



APPLE-1011, FIG. 5

[3] Tsubosaki405 makes clear that its adhesive film is composed of insulating materials, including materials that it identifies as polyetheramideimide and captone. APPLE-1011, 7:35-41. To the extent Tsubosaki405 suggests that the adhesive film can also be constructed from layers of polyester amide imide / Kapton / polyester amide imide, a POSITA would have understood that these materials are likewise electrically insulative. Kapton tape is commonly used in electronics and printed circuits boards.

56. Tsubosaki405's insulating adhesive films are used for bonding structures to circuitry leads 3 made from thin metal films such as iron or copper. *See, e.g.*, Tsubosaki405, 1:65-2:22, 6:44-48 ("[T]he insulating adhesive films 2, 3 are bonded to the leadframe in position. The lead 3 is in the form of a sheet or foil of Fe (42 Ni-Fe material) or Cu …"), FIGS. 1-2.



APPLE-1011, FIG. 2

C. The Tsubosaki010-Tsubosaki405 Combination Overview

57. As discussed above, Tsubosaki010 discloses a tape base 1a of a tape carrier 1 that can be "made of polyimide resin or other similar suitable materials." Tsubosaki010, ¶[0064]; *see also id.*, ¶¶[0111], [0118]. A thin copper film patterned to form leads 1c is bonded to the tape base 1a by an adhesive 1b. *Id.*, ¶[0116]-[0117], [0063]. "Adjacent ones of the laminated unitary TCPs are bonded together by adhesive 1e," which can be "made of a thermally deformable polyimide resin material." *Id.*, ¶[0111]; *see also id.*, [0118], FIG. 18.

58. To the extent Tsubosaki010 does not expressly disclose that the tape base layer 1a and adhesive layers 1b and 1e are made from insulating materials, it would have been obvious to a POSITA to use insulating materials for these components based on the teachings of Tsubosaki405. Recall, for example, that Tsubosaki405 describes conventional carrier tapes in which both the base member and adhesives on either side of the base member are insulating materials. Tsubosaki405, 7:33-41 (describing "a three-layer insulating adhesive film 27 … having a base B interposed between adhesive layers A"), FIG. 5. Applying Tsubosaki405's teachings to Tsubosaki010, tape base 1a, adhesive 1b, and adhesive 1e would each predictably be made of insulating materials in a manner analogous to the three-layer adhesive film disclosed in Tsubosaki405. In the combination, in some examples, base 1a may include "captone" or "any other polyimide film," adhesive 1b may include "polyetheramideimide," and adhesive 1e may be an insulating "thermally deformable polyimide resin" based on the teachings of Tsubosaki405 and Tsubosaki010. *See, e.g.*, Tsubosaki405, 7:33-41; Tsubosaki010, ¶¶[0064], [0111], [0116]-[0118]. Other suitable insulating materials may also be used.

59. A POSITA would have been motivated to implement Tsubosaki010's tape base 1a and adhesives 1b and 1e with insulating materials based on the teachings of Tsubosaki405 for multiple reasons.

60. *First*, a POSITA would have implemented Tsubosaki010's tape base 1a and adhesives 1b and 1e as insulating materials to ensure that different conductive leads 1c within each TCP in the stack and/or conductive leads 1c from different TCPs in the stack are electrically isolated from each other. As FIG. 15 of Tsubosaki010 shows, each TCP 1 can include dozens of leads 1c that function as separate power and/or signal lines delivering power and/or signals to respective terminals of the semiconductor chip 2. Tsubosaki010, FIG. 15; *see also id.*, ¶[0017]-[0022], [0062], [0110]. Because the tape base 1a and adhesives 1b, 1e are situated between conductive leads within and between TCPs of Tsubosaki010's multi-layer structure, a POSITA would have sought to implement these components with insulating materials to ensure the leads are electrically isolated and to reduce the risk of a short circuit due to undesired connections between different leads and conductors in the module. *See id.*, APPLE-1008, 556.

61. *Second*, a POSITA would have appreciated that due to power and electrical signals being connected with conductive leads 1c to the semiconductor chip 2, no need exists for the tape base 1a or adhesives 1b and 1e to similarly be

conductive to deliver power or signals either to chip 2 or any other module component. Indeed, neither tape base 1a nor adhesives 1b and 1e are electrically connected to the terminals of semiconductor chip 2, and they are therefore neither intended nor able to practicably serve as power or signal lines for the chip 2 or other components in Tsubosaki 010's module. *See, e.g.*, Tsubosaki010, FIGS. 14-21. A POSITA therefore would have had no reason to implement conductive materials for the tape base 1a or adhesives 1b or 1e, and it would have been obvious to instead choose insulating materials given that conductive materials would serve no evident purpose.

62. *Third*, a POSITA would have found insulating materials for the tape base 1a and adhesives 1b and 1e obvious to try. There exist a finite number of classes of materials that could be used to implement tape base 1a and adhesives 1b and 1e—namely, insulating materials or conductive materials—and a POSITA would have had ample reason to try insulating materials for each of the reasons described herein (*e.g.,* to promote electrical isolation between leads 1c, semiconductor chips 2, and other components of the module).

63. *Fourth*, a POSITA would have understood that insulators such as the polyimide-based materials suggested in Tsubosaki405 were commonly used in electronic devices before the Critical Date. These and similar materials (*e.g.,*

polyamides) were known to be useful in "prevent[ing] cross-talk between conducting vias, and as adhesives between polymer-polymer and polymer-metal interface." APPLE-1010, 42. Such materials can also provide "excellent performance at elevated temperatures" and exhibit beneficial "corrosion resistance." APPLE-1010, 42.

64. *Fifth*, a POSITA would have found insulating materials such as the polyimides described in Tsubosaki405 obvious and desirable to use when implementing Tsubosaki010's tape base 1a and adhesives 1b and 1e to gain the benefit of their low dielectric constants and other favorable properties. Polyimides were "used as dielectric layers in a variety of microelectronic applications since they have good processability, low dielectric constant, high thermal stability, low moisture absorption, and good mechanical properties." APPLE-1016, Intro..

65. *Sixth*, implementing tape base 1a and adhesives 1b and 1e with insulating materials would have been obvious as a predictable application of Tsubosaki405's known materials to Tsubosaki010's known structures to achieve merely predictable results.

66. A POSITA would have reasonably expected success implementing the tape base 1a and adhesives 1b and 1e in the Tsubosaki010-Tsubosaki405 combination. Insulating materials were commonly used with adhesive films in

tape carriers before the ’816 Patent, and Tsubosaki010 and Tsubosaki405 both contemplated the use of similar polyimide-based materials for similar tape base member and adhesive structures. *Id.* Indeed, Tsubosaki 010 notes that tape base 1a and adhesive 1e can each be made of polyimide materials, although Tsubosaki010 does not disclose the same specificity as Tsubosaki405. *Id.*; Tsubosaki010, ¶¶[0064], [0111], [0118]. Tsubosaki010 and Tsubosaki405 are both also analogous art in that they are both in the same field of endeavor and/or reasonably pertinent to the problem faced by the inventors of the ’816 Patent. For example, like the ’816 Patent, Tsubosaki010 and Tsubosaki405 both describe techniques for manufacturing and packaging electronic modules. APPLE-1001, 1:17-39; *supra*, §§X.A-B; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

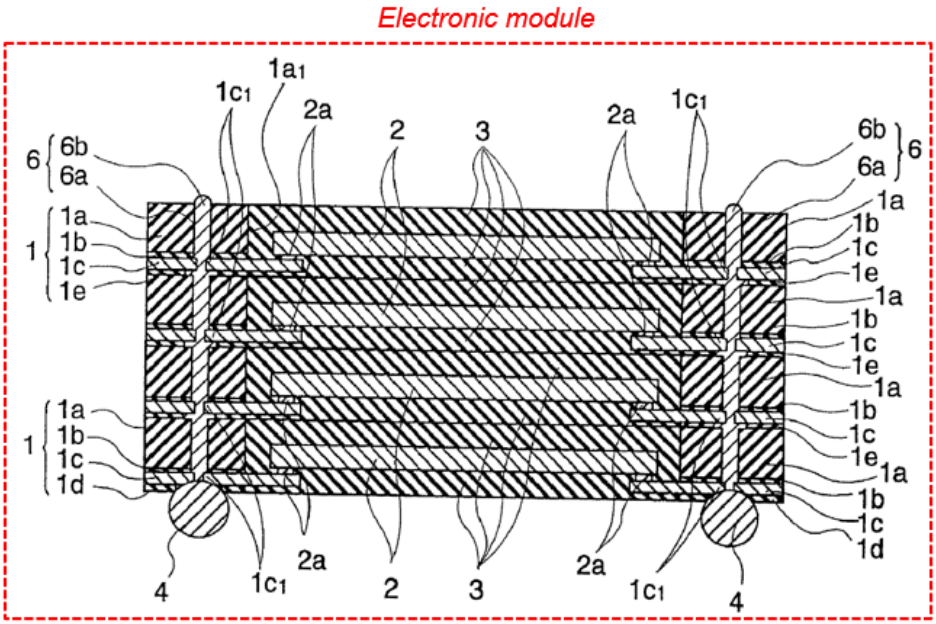
D. Analysis

i. Claim 1

[1pre] An electronic module, comprising:

67. To the extent the preamble is limiting, the Tsubosaki010-Tsubosaki405 combination renders it obvious. For example, Tsubosaki010 discloses that “a plurality of TCPs … are laminated on one another to constitute a multi-layered TCP structure” that corresponds to an “***electronic module***” as claimed. Tsubosaki010, ¶[0110]; *generally id.*, ¶¶[0108]-[0130], FIGS. 14-21. Tsubosaki010’s modules are “adaptable for use with a semiconductor device as

built in electronic equipment—such as computers, portable or mobile radiotelephone handsets, video cameras or the like—or integrated circuit (IC) cards or memory cards; for example, the semiconductor device is arranged to have a tape carrier package (TCP) structure which includes a semiconductor chip 2 disposed within a device hole 1a1 of a tape carrier 1" Tsubosaki010, ¶[0062].

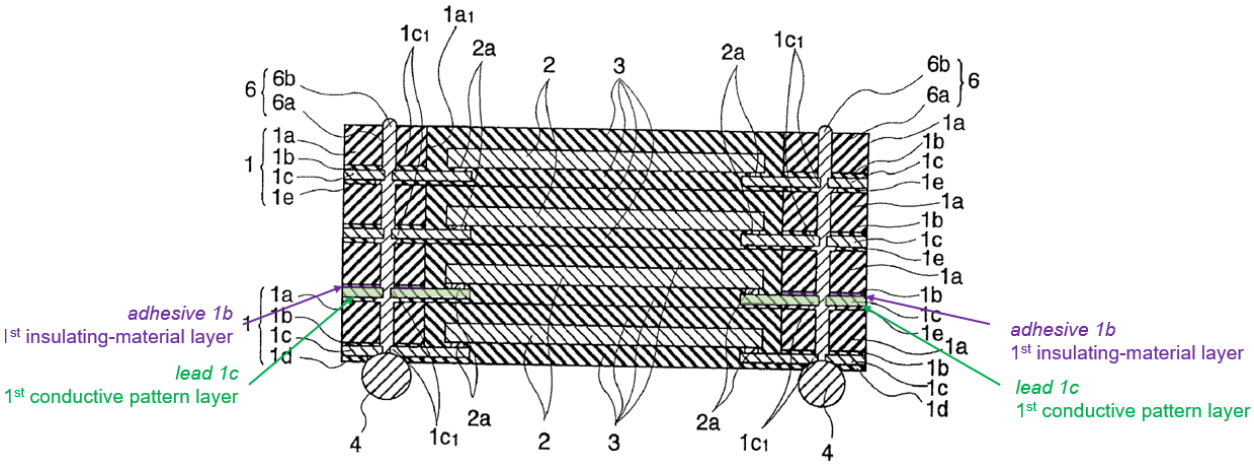


APPLE-1005, FIG. 14 (annotated)

[1a] a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;

68. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1a]. For example, in the combination, leads 1c from a given one of the TCPs in the stacked TCP module corresponds to a "***first conductive pattern layer***" and adhesive layer 1b from the same TCP corresponds to a "***first insulating-***

material layer" arranged on at least one surface (*i.e.,* a top surface) of the leads 1c as claimed. Tsubosaki010, ¶¶[0116]-[0117] ("a tape base 1a with ***adhesive 1b bonded to its one surface***"; "***bond a Cu thin-film*** for example to one surface of the tape base 1a by using the adhesive 1b attached thereto; thereafter, ***pattern the Cu thin film*** by etching methods or the like to thereby ***form a plurality of leads 1c*** …")[4], FIGS. 14, 16-17, 21; *see also id.*, ¶¶[0063], [0066], [0068].



APPLE-1005, FIG. 14 (annotated)

69. To the extent Tsubosaki010 does not expressly disclose that adhesive layer 1b is made from an insulating material, Tsubosaki405 discloses "***insulating*** adhesive films … in the form of a tape" having insulative adhesive such as polyetheramideimide" bonded between a lead and a tape base member in a semiconductor package similar to Tsubosaki010's adhesive layer 1b.

---

[4] All emphasis added unless indicated otherwise.

Tsubosaki405, 7:33-41, FIG. 5; *supra*, §X.B. It would have been obvious based on Tsubosaki405 to implement Tsubosaki010's adhesive layer 1b as an insulating-material layer for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §X.C.

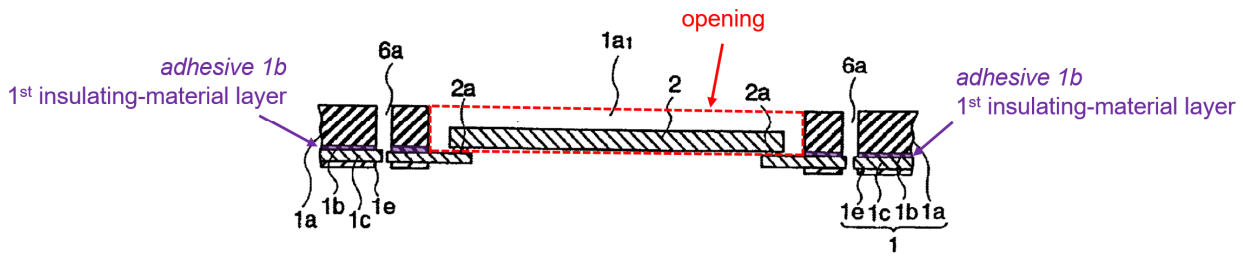
[1b] at least one opening in the first insulating-material layer that extends through the first insulating-material layer;

70. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1b]. For example, Tsubosaki010 discloses a device hole 1a1 (***at least one opening***) formed in tape base 1a and adhesive layer 1b (***first insulating-material layer***), where the device hole 1a1 extends through the entire thickness of the adhesive layer 1b (***first insulating-material layer***). Tsubosaki010, ¶[0116] ("form by mechanical die-punching techniques a device hole 1a1"), ¶[0120] ("place a semiconductor chip 2 within the device hole 1a1"), FIGS. 16-19; *see also id.*, Abstract ("A semiconductor chip 2 is disposed within a device hole as formed in a tape base material 1a of a tape carrier 1 …"), ¶¶[0062]-[0065], FIGS. 14, 21.[5]

---

[5] Nothing in the plain language of Element [1c] requires that a thickness of the "at least one opening" be coterminous with the thickness of first insulating-material layer. Even if this were required, however, the portion of device hole 1a1 that spans the space between adhesive layer 1b, to the exclusion of the portion of

71. FIG. 19 shows the hole 1a1 (***at least one opening***) formed in the tape base 1a and adhesive layer 1b at an intermediate stage of manufacturing the electronic module:



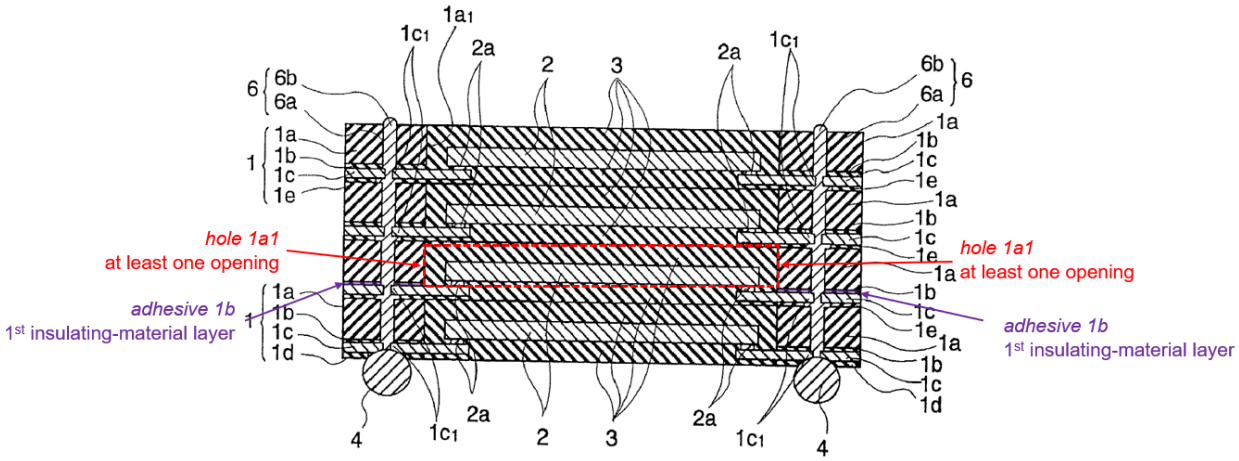
APPLE-1005, FIG. 19 (annotated)

72. FIG. 14 shows a sectional view of the finished electronic module in which hole 1a1 is filled with a sealing resin 3 around semiconductor chip 2:[6]

---

device hole 1a1 that spans the space between tape base 1a, provides an alternative mapping to the claimed "at least one opening."

[6] Like Tsubosaki010, the '816 Patent also discloses that after forming the opening in the first insulating-material layer and mounting the component (e.g., chip) in the opening, the opening can then be filled in the finished module with resin material. '816 Patent, 13:47-53 ("[P]repreg can be used as the second insulating-material layer 11. … With the aid of the prepreg, excellent filling is achieved in the space between the elements, as shown in the example of FIG. 29."), 12:54-54-63 ("As can be seen from FIG. 28, the resin contained in the prepreg fills the space between the component 6 and its surroundings."), FIGS. 28-31.



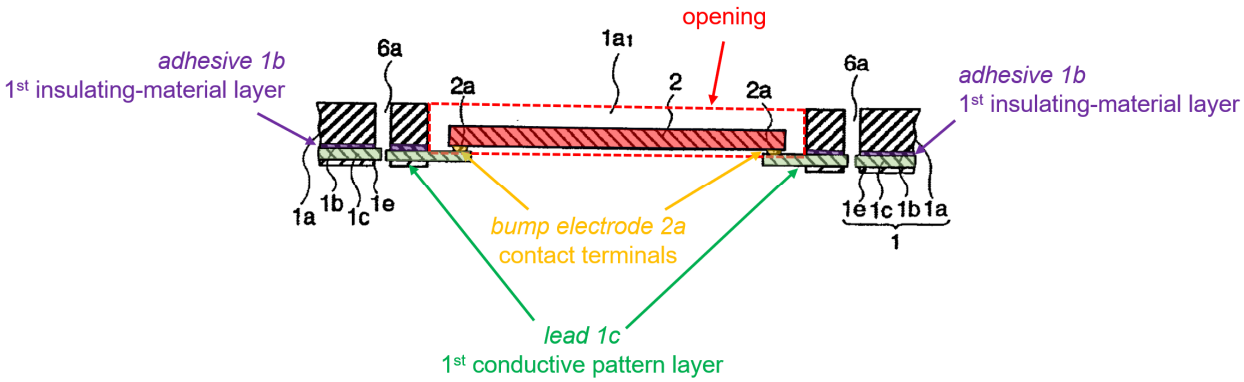
APPLE-1005, FIG. 14 (annotated)

[1c] a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;

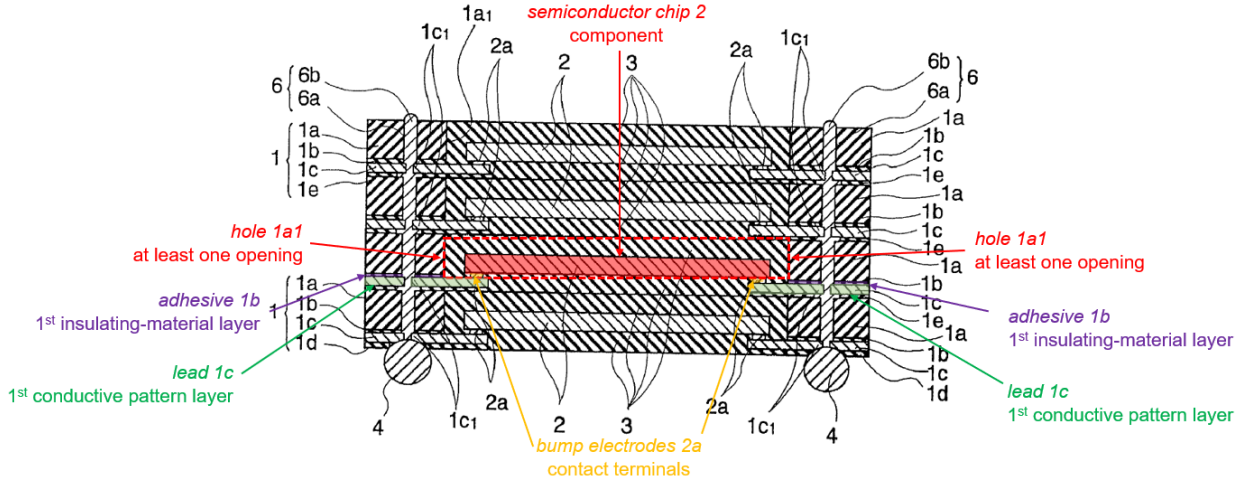
73. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1c]. For example, Tsubosaki010 discloses a semiconductor chip 2 (***component***) comprising bump electrodes 2a (***contact terminals***) being arranged at least partially within device hole 1a1 (***opening***), the bump electrodes 2a (***contact terminals***)[7] electrically connected to leads 1c (***first conductive pattern layer***) of the TCP in which the chip 2 is disposed. Tsubosaki010, ¶[0120] ("Subsequently, place

[7] The semiconductor chip 2's bonding pads 2b or the combination of bonding pads 2b and bump electrodes 2a provide alternative mappings to the claimed "***contact terminals***" and likewise render the challenged claimed features obvious. *See* Tsubosaki010, [0068], [0072]-[0073], [0160]-[0163], FIG. 32.

a semiconductor chip 2 within the device hole 1a1 of the tape base 1a. Then, perform position alignment between the semiconductor chip 2's bump electrodes 2a and leads 1c. Thereafter, contact the bump electrodes 2a with leads 1c by all-at-once inner-lead bonding techniques as shown in FIG. 19."), FIGS. 19-21; *see also id.*, ¶¶[0068] ("The distal end of each lead 1c is electrically connected via bump electrode 2a to the semiconductor chip 2. This bump electrode 2a is made for example of Au … . Accordingly, the bump electrode 2a and its associated lead 1c are in contact with each other by Au-Au junction or the like."), [0062] ("chip 2 disposed within a device hole 1a1 of a tape carrier 1[] … while causing electrodes of the semiconductor chip 2 to be externally drawn via bump electrodes 4 associated therewith"), [0069], [0072]-[0073], [0081], [0094], Abstract, FIG. 14.



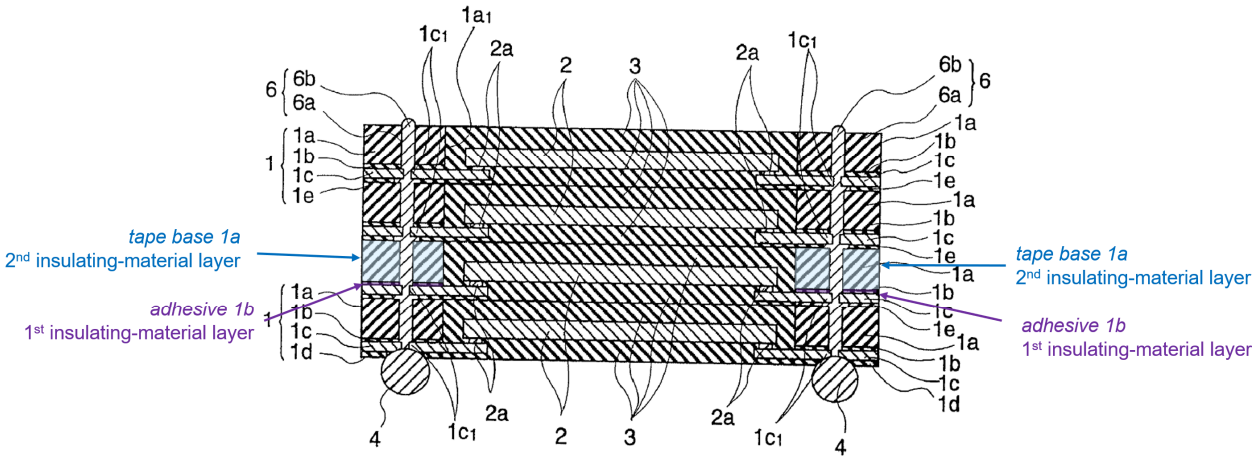
APPLE-1005, FIG. 19 (annotated)



APPLE-1005, FIG. 14 (annotated)

[1d] a second insulating-material layer disposed on the first insulating-material layer, and;

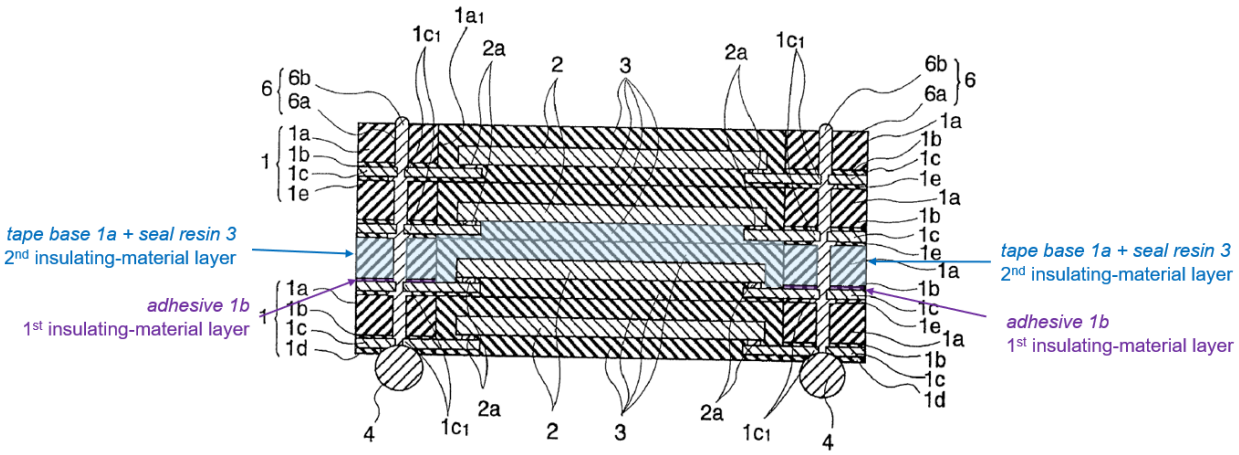
74. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1d]. For example, in a first mapping, Tsubosaki010 discloses a tape base 1a that, in the combination, provides a "***second insulating-material layer***" disposed on adhesive layer 1b (***first insulating-material layer***) as claimed. Tsubosaki010, ¶¶[0110], [0116], FIGS. 14, 16, 19, 21; *see also id.*, [0063], [0064] ("tape base 1a is made of polyimide resin or other suitable materials"), [0068].



APPLE-1005, FIG. 14 (annotated) – First Mapping

75. Alternatively, in the combination, Tsubosaki010's tape base 1a together with seal resin 3 collectively provide a "***second insulating-material layer***" disposed on adhesive layer 1b (***first insulating-material layer***) as claimed. Tsubosaki010, [0110], [0116], FIGS. 14, 16, 19, 21; *see also id.*, [0063]-[0064], [0068]. Tsubosaki010 explains that seal resin 3 is formed by injection molding, in some examples. Tsubosaki010, [0121] ("Thereafter place the tape carrier 1 mounting thereon the semiconductor chip 2 within a molding die 5 as shown in FIG. 8; then, inject a molten seal resin material, which has been fed to inside a runner 5b of the molding die 5, into a cavity as formed of the tape base 1a's device hole 1a1 and the molding die 5 through a subrunner 5c and a gate 5a as well as a seal resin injection port 1a2 of the tape base 1a."), [0065]-[0067], [0082], FIG. 8; *see also id.*, [0141]-[0154] & FIGS. 28-31 (describing a technique for "[i]ntegral

molding of the seal resin 3 of the multilayer TCP" such that there are "no gaps [] formed between layers of seal resin 3").[8]



APPLE-1005, FIG. 14 (annotated) – Second Mapping

76. To the extent Tsubosaki010 does not expressly disclose that tape base 1a is made from an insulating material, Tsubosaki405 discloses "***insulating***

---

[8] Petitioner maps tape base 1a and seal resin 3 collectively to the claimed "second insulating-material layer" under Patent Owner's broader application of the term "layer" as reflected in Patent Owner's infringement charts in the related district court litigation. *See* APPLE-1105, 3-7, 9-11 (pointing to portions of Petitioner's product that encompass multiple strata of materials as the claimed first and second insulating-material layers, respectively). The '816 Patent likewise refers to a "two-layered insulation layer" made of multiple materials. APPLE-1001, 2:22-26; *see also* APPLE-1022, 14:43-45 (claim 1) (Patent Owner claiming a first or second conductive-pattern layer that "comprises ***at least two layers*** of at least two different materials" in a related patent asserted against Petitioner).

adhesive films … in the form of a tape" having an insulative tape base member made from captone or other suitable polyimide film. Tsubosaki405, 7:33-41, FIG. 5; *supra*, §X.A; Tsubosaki010, [0064] ("tape base 1a is made of polyimide resin or other suitable materials"). It would have been obvious based on Tsubosaki405 to implement Tsubosaki010's tape base 1a as an insulating-material for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §X.C.

77. A POSITA also would have understood and found it obvious to implement Tsubosaki010's seal resin 3 as an insulating material, especially as seal resin 3 fills the space between different leads, electrodes, and semiconductor dies in the multi-layered TCP structure, and an insulating-material would be important to electrically isolate these structures while preventing short circuits. For example, Tsubosaki010 explains that the seal resin 3 can be made of an epoxy-based resin, which a POSITA would have understood to ordinarily be an insulating material. Tsubosaki, ¶[0076]; *see also id.*, APPLE-1006, 250 ("since 1947, [epoxy resins] are second in usage in insulation varnishes only to polyesters"), 8 ("[e]poxies are noted for their excellent dielectric properties"), 185-186, 271, 360. At minimum, and even if the insulative properties of Tsubosaki010's epoxy-based seal resin 3 are not expressly disclosed, a POSITA would have been motivated to use an

insulating seal resin 3 in the Tsuboaski010-Tsubosaki405 combination to ensure different conductive components in the TCP structure were electrically isolated. In this manner, the seal resin 3 and tape base 1a cooperate to form a layer that supports and electrically isolate disparate conductive components in the TCP stack of the Tsubosaki010-Tsubosaki405 combination.[9] *Id.*

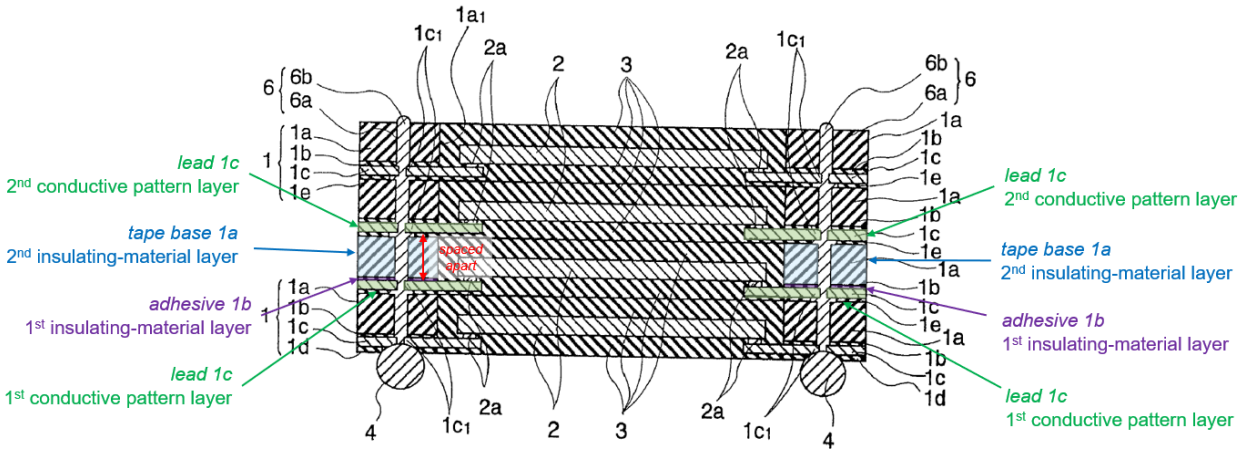
[1e] a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers;

78. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1e]. For example, Tsubosaki010 discloses that the multi-layered TCP structure includes a second set of leads 1c (***second conductive-pattern layer***) of a second tape carrier 1 (*i.e.,* an upper tape carrier) positioned above a first tape carrier 1 (*i.e.,* a lower tape carrier) containing a first set of leads 1c (***first conductive-pattern layer***). Tsubosaki010, ¶¶[0108]-[0114], FIGS. 14, 21, 31; *see also id.*, ¶¶[0116]-[0117] ("Subsequently, ***bond a Cu thin-film*** for example to one surface of the tape base 1a by using the adhesive 1b attached thereto; thereafter, ***pattern the Cu thin film*** by etching methods or the like to thereby ***form a plurality of leads 1c*** …"), [0063], [0066], [0068], FIGS. 16-17.

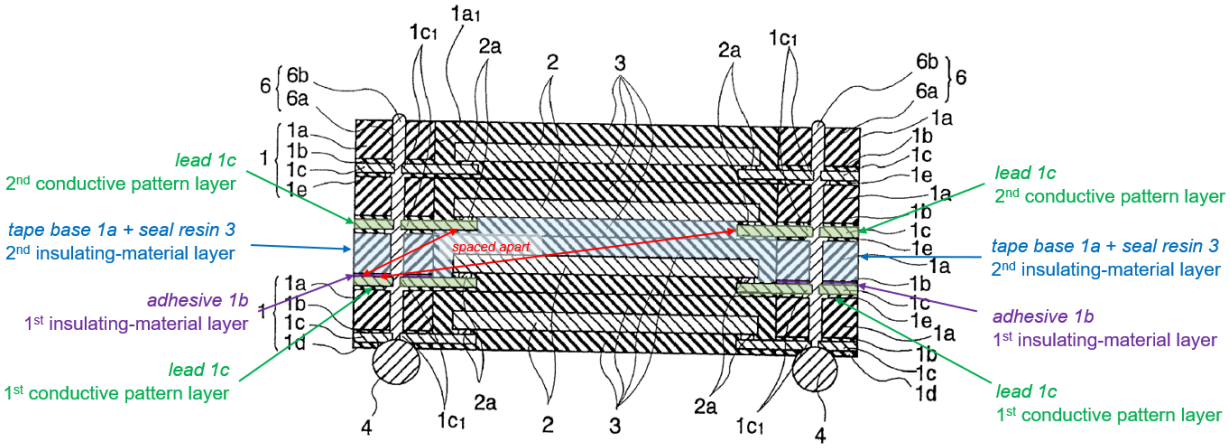
---

[9] *Supra*, Footnote 11.

79. For both the first and second alternative mappings of the "***second insulating-material layer***" described above in connection with Element [1d], the upper set of leads 1c (***second conductive-pattern layer***) is spaced apart from the lower set of leads 1c (***first conductive-pattern layer***) by at least the adhesive layer 1b (***first insulating-material layer***) and tape base 1a (***second insulating-material layer*** (first mapping) or tape base 1a together with seal resin 3 (***second insulating-material layer*** (second mapping).



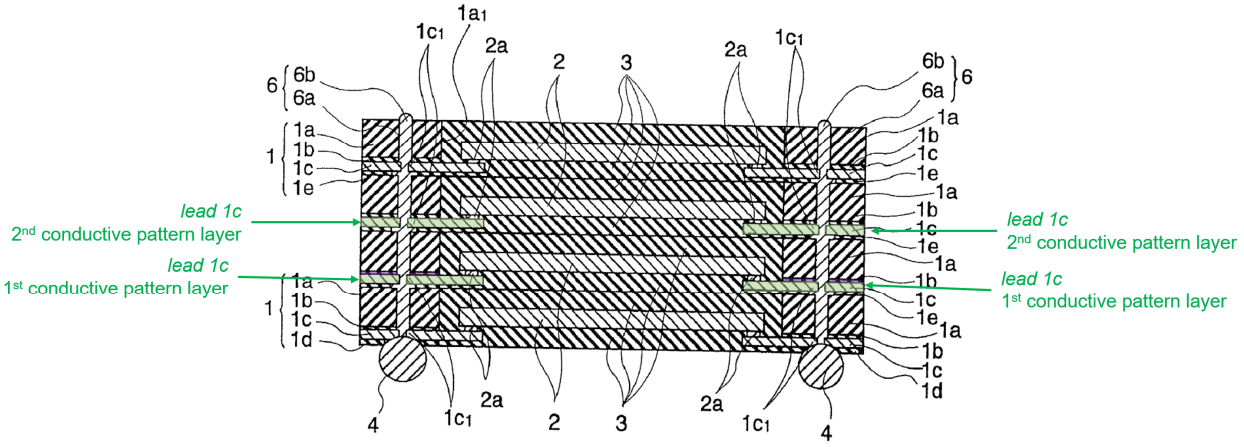
APPLE-1005, FIG. 14 (annotated) – First Mapping



APPLE-1005, FIG. 14 (annotated) – Second Mapping

[1f] wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

80. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1f]. Tsubosaki describes techniques for forming sets of leads 1c including a lower set (***first conductive-pattern layer***) and an upper set (***second conductive-pattern layer***) in the multi-layered TCP structure that are each substantially planar. *See, e.g.*, Tsubosaki010, [0114], [0118], FIGS. 14-21. The substantially planar leads 1c are shown in FIG. 14, for example:



APPLE-1005, FIG. 14 (annotated)

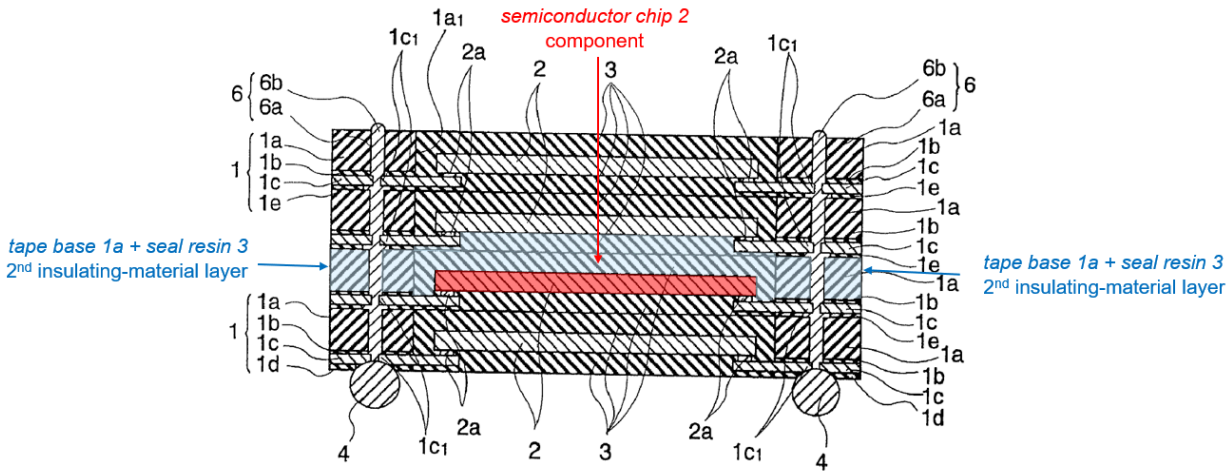
81. That leads 1c of the first and second conductive-pattern layers are substantially planar also would have been obvious to a POSITA based on Tsubosaki010's descriptions of how the leads 1c are formed. For instance, Tsubosaki010 discloses that tape base 1a with its hole 1a1 have a "planar rectangular shape" and that the copper (or other suitable metal) film that is patterned to form leads 1c is bonded to the tape base 1a via adhesive 1b. Tsubosaki, ¶¶[0064], [0116]-[0117]. Tsubosaki010 also describes a "stress neutral plane A [that] is the plane parallel to the principal surface of the semiconductor chip 2, which is a specific plane on which the stress applied to the semiconductor chip 2 becomes neutral in the direction along the thickness of the semiconductor chip 2." Tsubosaki010, ¶[0075], FIG. 1; *see also id.*, ¶¶[0074], [0088], [0094]-[0095], [0098]-[0099], [0106] (referring to stress neutral planes A and A1). Even where portions of the tape carrier 1 may be subjected to stress, Tsubosaki010

describes techniques to mitigate resulting deformation. For example, Tsubosaki010 teaches that "[i]n cases where the stress neutral plane A1 of the semiconductor chip 2 and the stress neutral plane A of the TCP as a whole are little deviated from each other due to any possible thickness differences among respective constituent parts or components of the TCP, such deviation is corrected by adjustment of the bending amount of the lead 1 c." Tsubosaki010, ¶[0098].

ii. Claim 2

[2] The electronic module of claim 1, wherein the second insulating-material layer directly contacts the component.

82. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [2]. For example, Tsubosaki010 discloses that seal resin 3 (*i.e.,* a component of the ***second insulating-material layer*** according to the second mapping discussed above in Element [1d]) directly contacts the semiconductor chip 2 (***component***). Tsubosaki010, ¶[0120]-[0123] ("both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3"), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d].

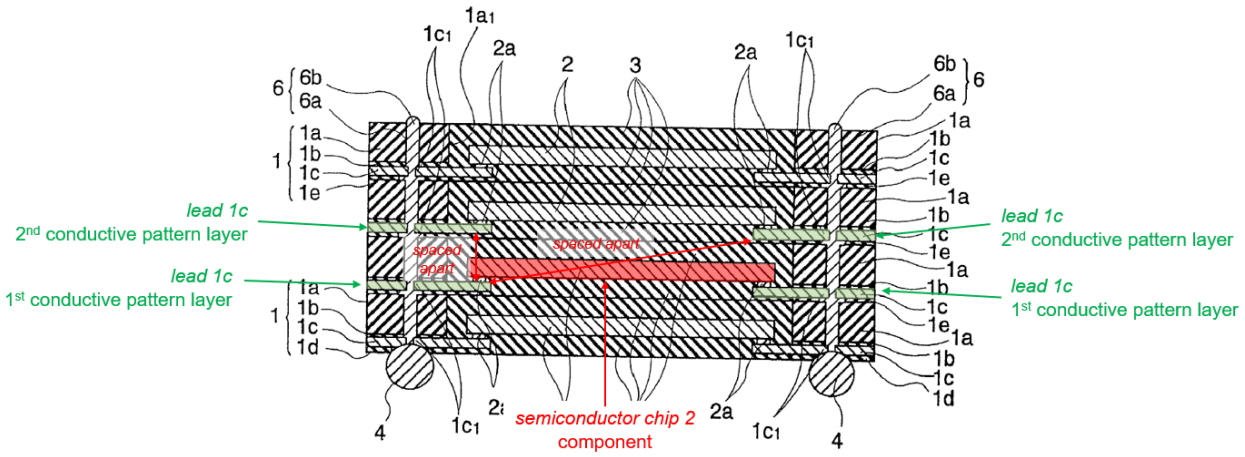


APPLE-1005, FIG. 14 (annotated) – Second Mapping

iii. Claim 3

[3] The electronic module of claim 1, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.

83. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [3]. For example, Tsubosaki010 discloses that the second (upper) set of leads 1c (***second conductive-pattern layer***) is spaced apart from the first (lower) set of leads 1c (***first conductive-pattern layer***) by the semiconductor chip 2 (***component***). Tsubosaki010, ¶¶[0108]-[0126], FIG. 14.

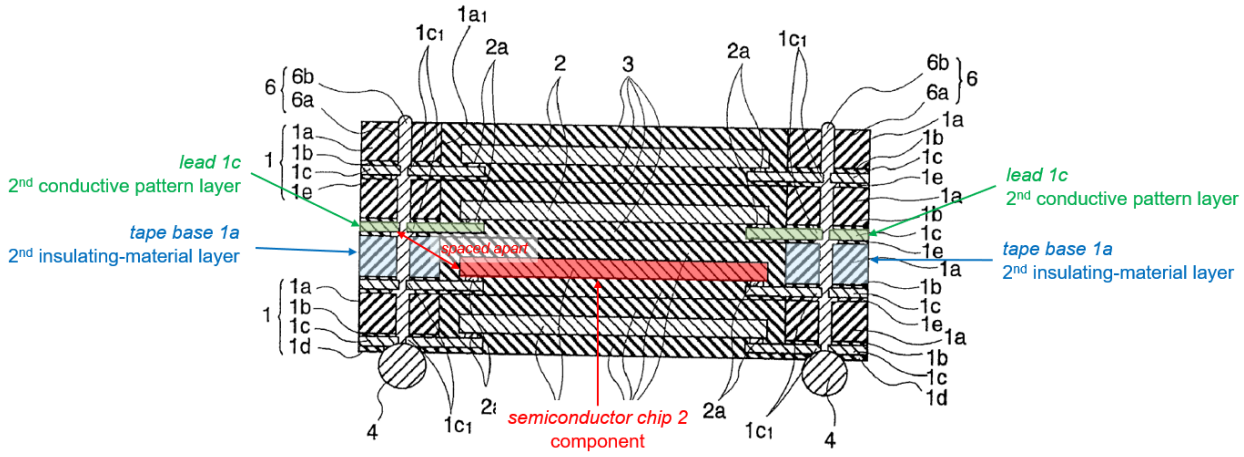


APPLE-1005, FIG. 14 (annotated)

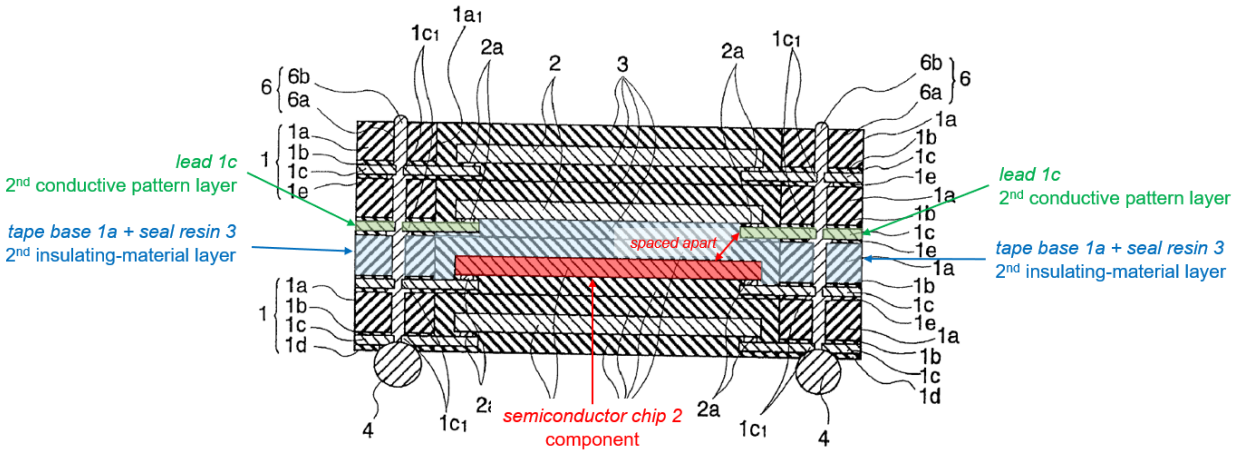
iv. Claim 4

[4] The electronic module of claim 3, wherein the second conductive pattern layer is spaced apart from the component by the second insulating-material layer.

84. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [4]. For example, Tsubosaki010 discloses that the second (upper) set of leads 1c (***second conductive-pattern layer***) is spaced apart from the semiconductor chip 2 (***component***) by the tape base 1a or the tape base 1a together with seal resin 3 (***second insulating-material layer***). *See* Tsubosaki010, ¶¶[0120]-[0123] ("both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3"), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d]; *generally id.*, Tsubosaki010, [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated) – First Mapping



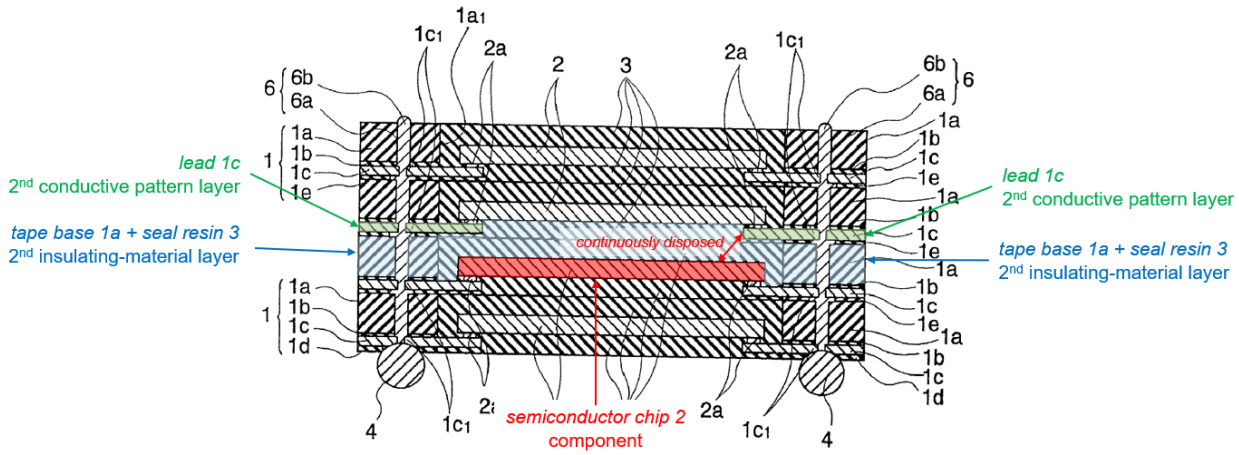
APPLE-1005, FIG. 14 (annotated) – Second Mapping

v. Claim 5

[5] The electronic module of claim 4, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.

85. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [5]. For example, Tsubosaki010 discloses that seal resin 3 (*i.e.,* a component of the ***second insulating-material layer*** according to the second mapping discussed

above in Element [1d]) is continuously disposed between the upper set of leads 1c (***second conductive-pattern layer***) and the semiconductor chip 2 (***component***). Tsubosaki010, ¶[0120]-[0123] ("both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3"), [0140] ("no gaps are formed between layers of seal resin 3"), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d]; *generally* Tsubosaki010, [0108]-[0126], FIGS. 14-21 & [0139]-[0154], FIGS. 27-30.



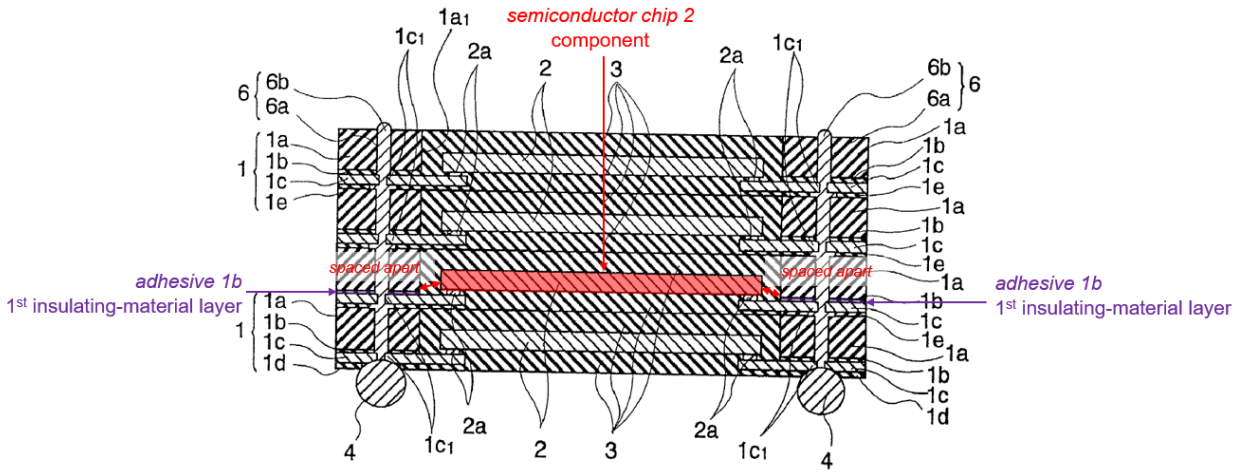
APPLE-1005, FIG. 14 (annotated) – Second Mapping

vi. Claim 6

[6] The electronic module of claim 1, wherein the first insulating-material layer is spaced apart from the component.

86. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [6]. For example, Tsubosaki010 discloses that the adhesive layer 1b (***first insulating-material layer***) is spaced apart from the semiconductor chip 2

(***component***). Tsubosaki010's seal resin 3 surrounds the semiconductor chip 2 thus separating the semiconductor chip 2 from the adhesive layer 1b. Tsubosaki010, ¶¶[0065], [0082]-[0085]; *see also id.*, ¶[0092] ("the thickness D1 of the seal resin 3 [can] be equal to the thickness D2 of tape carrier 1"), [0063], [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated)

vii. Claim 7

[7] The electronic module of claim 1, wherein the first insulating-material layer comprises a different material than a material of the second insulating-material layer.

87. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [7]. As discussed above, in the Tsubosaki010-Tsubosaki405 combination, adhesive layer 1b provides a "***first insulating-material layer***," tape base 1a provides a "***second insulating-material layer***" according to a first mapping, and

tape base 1a together with seal resin 3 provides a "***second insulating-material layer***" according to a second mapping. *Supra*, Element [1a], [1d]. In the combination, Tsubosaki405 demonstrates that it would have been obvious to implement adhesive layer 1b as an adhesive film such as polyetheramideimide and to implement tape base 1a as another suitable polyimide film such as captone (sic) that lacks the same adhesive properties. Tsubosaki405, 7:32-41, FIG. 5; *supra*, §§X.B-C. Tsubosaki010 further discloses that seal resin 3 can be an epoxy-based resin. Tsubosaki010, [0076]. Accordingly, in the combination, the first insulating-material layer comprises a different material (*e.g.,* polyetheramideimide or another adhesive film) than a material of the second insulating-material layer (*e.g.,* captone or another non-adhesive polyimide film and/or epoxy-based resin).

viii. Claim 8

[8pre] An electronic module, comprising:

88. *Supra*, Element [1pre].

[8a] a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;

89. *Supra*, Element [1a].

[8b] an opening in the first insulating-material layer that extends through the first insulating-material layer;

90. *Supra*, Element [1b].

[8c] a component comprising contact terminals, the component being arranged at least partially within the opening, the contact terminals electrically connected to the first conductive pattern layer;

91. *Supra*, Element [1c].

[8d] a second insulating-material layer disposed on the first insulating-material layer;

92. *Supra*, Element [1d].

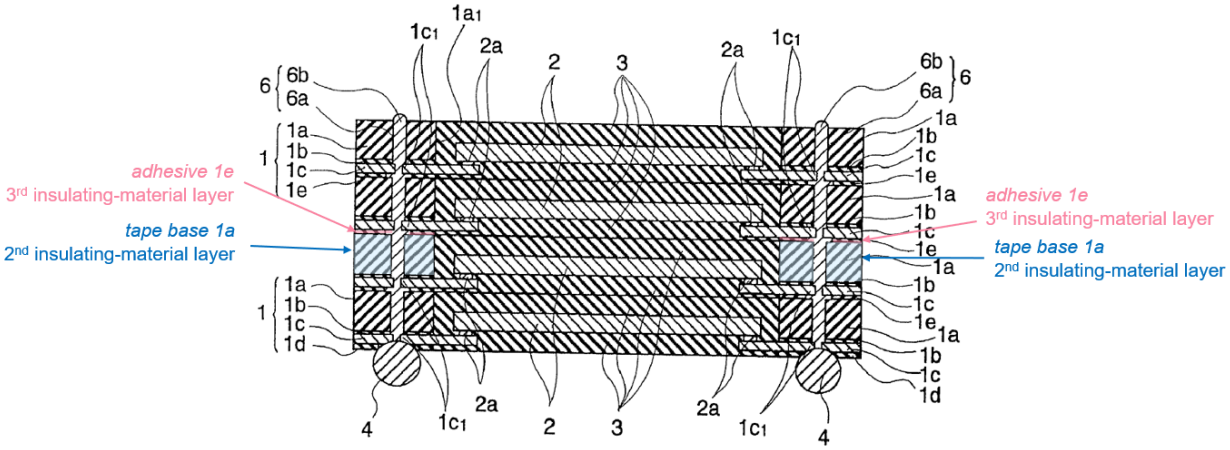
[8e] a third insulating-material layer disposed on the second insulating-material layer; and

93. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [8e]. For example, Tsubosaki010 discloses an adhesive layer 1e (***third insulating-material layer***) disposed on the tape base 1a (***second insulating-material layer***).[10] Tsubosaki010, [0111] ("Adjacent ones of the laminated unitary TCPs are bonded together by adhesive 1e. This adhesive 1e is a member for constituting part of the unitary TCP's tape carrier 1; for example, it is made of a thermally deformable polyimide resin material."), [0118] ("Thereafter, as shown in FIG. 18, provide adhesive le made of for example thermally deformable polyimide

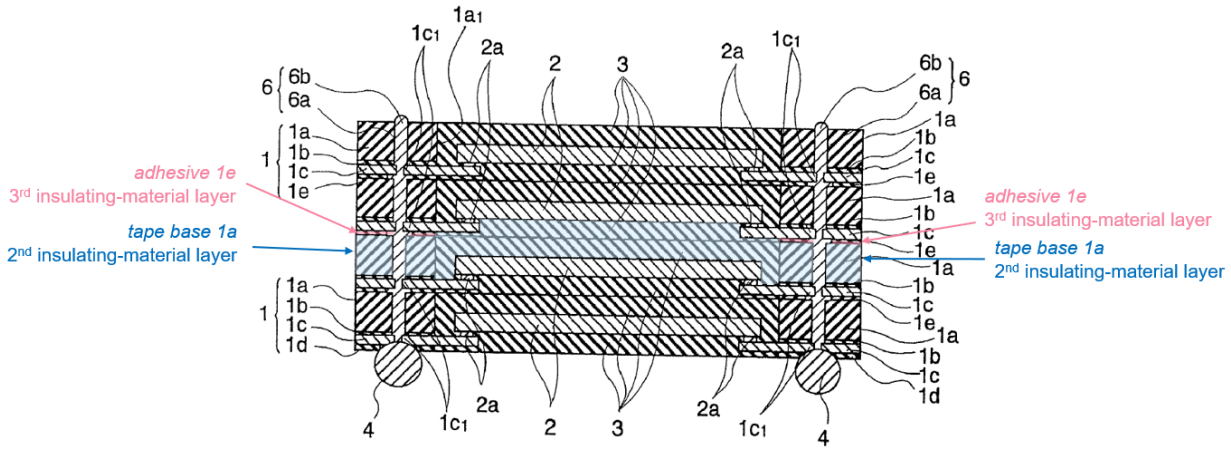
---

[10] Tape base 1a corresponds to the "second insulating-material layer" according to a first mapping of Tsubosaki010's structures to the claimed features. Tape base 1a is a component of the "second insulating-material layer" along with seal resin 3 according to a second mapping of Tsubosaki010's structures to the claimed features. *Supra*, Element [1d].

resin on the side of the copper thin film; then, remove part of such adhesive 1 e so that the bump underlayer pattern 1 c 1 portion of lead 1 c and a projected inner lead portion 1 c are exposed."), [0125] ("Thereafter, use the adhesive 1e sandwiched between adjacent ones of the unitary TCPs to contact the unitary TCPs together by thermo-compression methods thereby forming the intended multilayer TCP. To make long story short, as multiple unitary TCPs are stacked or laminated on one another by use of the adhesive 1e that is formed during fabrication of a unitary TCP, it becomes possible to manufacture the multilayer TCP without increasing production process steps required."), [0143] ("after lamination of a plurality of tape carriers 1 each mounting thereon its semiconductor chip 2 as shown in FIG. 28, use the adhesive 1 e between tape carriers 1"), [0130], FIGS. 14-21, 27-31.



APPLE-1005, FIG. 14 (annotated) – First Mapping

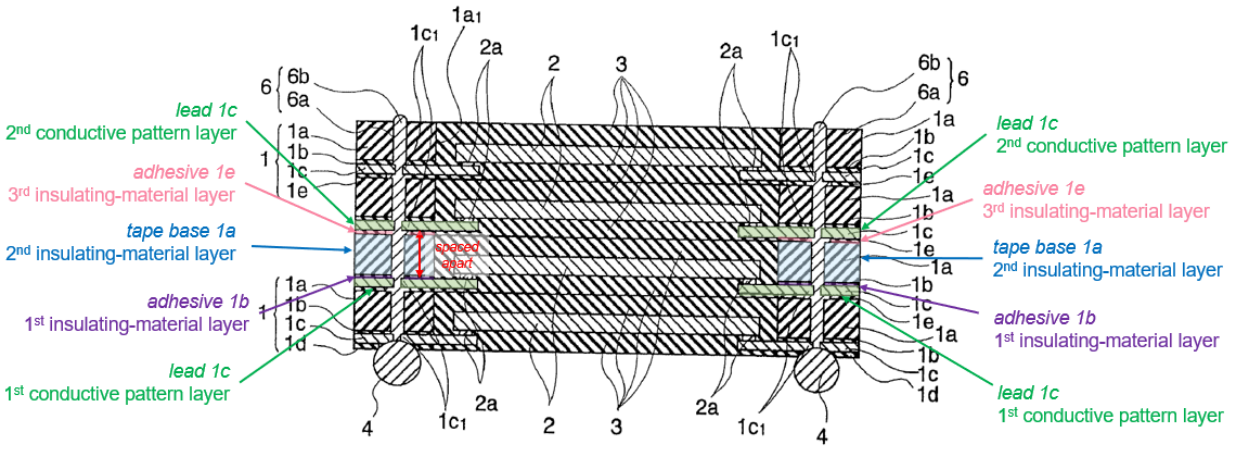


APPLE-1005, FIG. 14 (annotated) – Second Mapping

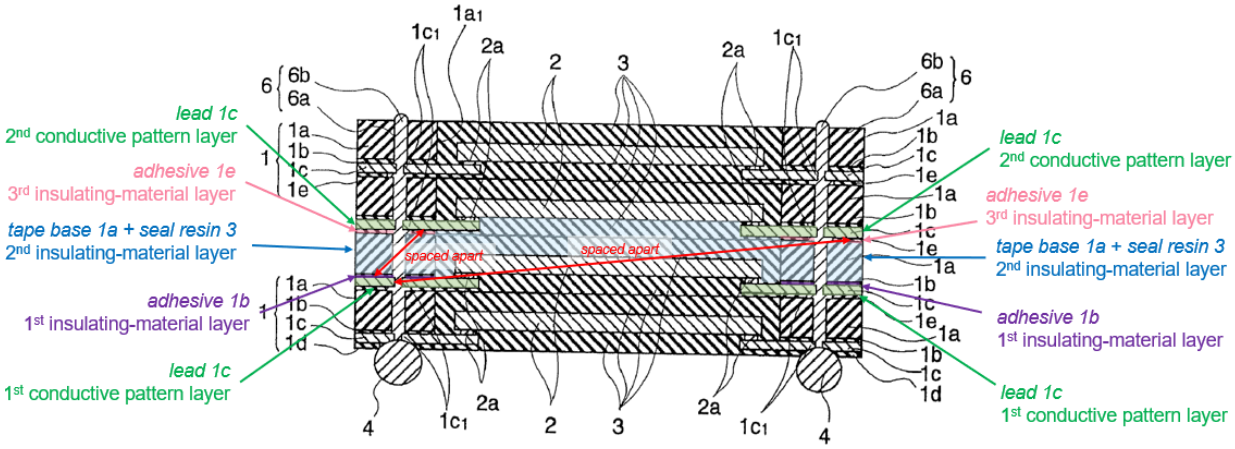
94. Tsubosaki010 teaches that adhesive 1e can be made of a "thermally deformable polyimide resin material." Tsubosaki010, ¶¶[0111], [0118]. To the extent Tsubosaki010 does not expressly disclose that adhesive layer 1e is an insulating material, Tsubosaki405 discloses "***insulating*** adhesive films … in the form of a tape" having insulative adhesive such as polyetheramideimide bonded between a lead and a tape base member in a semiconductor package similar to Tsubosaki010's adhesive layer 1e. Tsubosaki405, 7:33-41, FIG. 5; *supra*, §X.B. It would have been obvious based on Tsubosaki405 to implement Tsubosaki010's adhesive layer 1e as an insulating-material layer for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §X.C.

[8f] a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first, second, and third insulating-material layers,

95. The Tsubosaki010-Tsubosaki405 combination renders obvious Element [8f]. As described above in connection with Element [1e], Tsubosaki010 discloses that an upper set of leads 1c (***second conductive-pattern layer***) in the multi-layered TCP structure is spaced apart from a lower set of leads 1c (***first conductive pattern layer***) by at least the adhesive layer 1b (***first insulating-material layer***) and the tape base 1a or tape base 1a in connection with seal resin 3 (***second insulating-material layer***). *Supra*, Element [1e]. Tsubosaki010 further discloses that the upper set of leads 1c (***second conductive-pattern layer***) is spaced apart from the lower set of leads 1c (***first conductive-pattern layer***) additionally by the adhesive layer 1e (***third insulating-material layer***). Tsubosaki010, [0108]-[0126], [0143], FIGS. 14-21, 27-31.



APPLE-1005, FIG. 14 (annotated) – First Mapping



APPLE-1005, FIG. 14 (annotated) – Second Mapping

[8g] wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

96. *Supra*, Element [1f].

ix. Claim 9

[9] The electronic module of claim 8, wherein the second insulating-material layer directly contacts the component.

97. *Supra*, Claim [2].

x. Claim 10

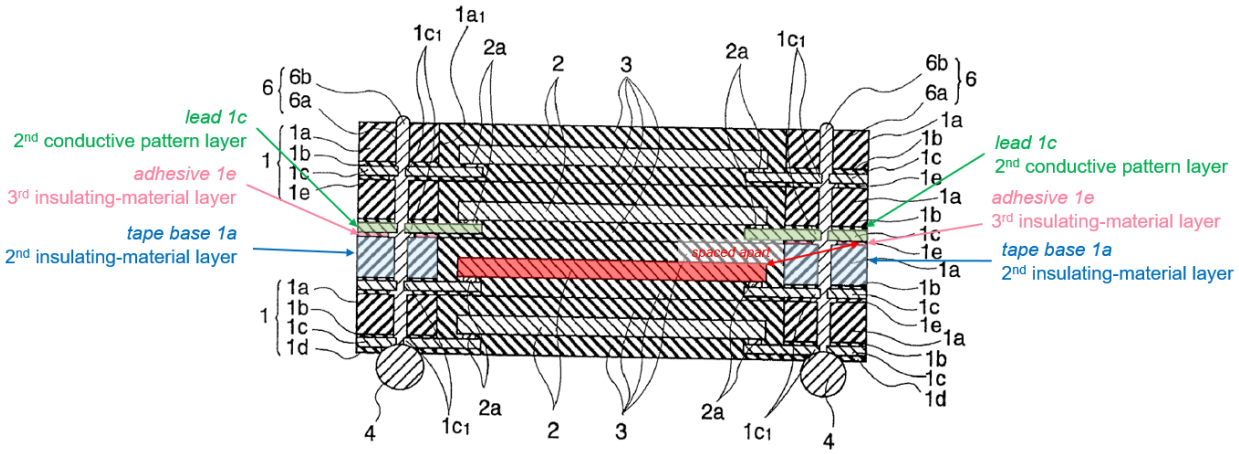
[10] The electronic module of claim 8, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.

98. *Supra*, Claim [3].

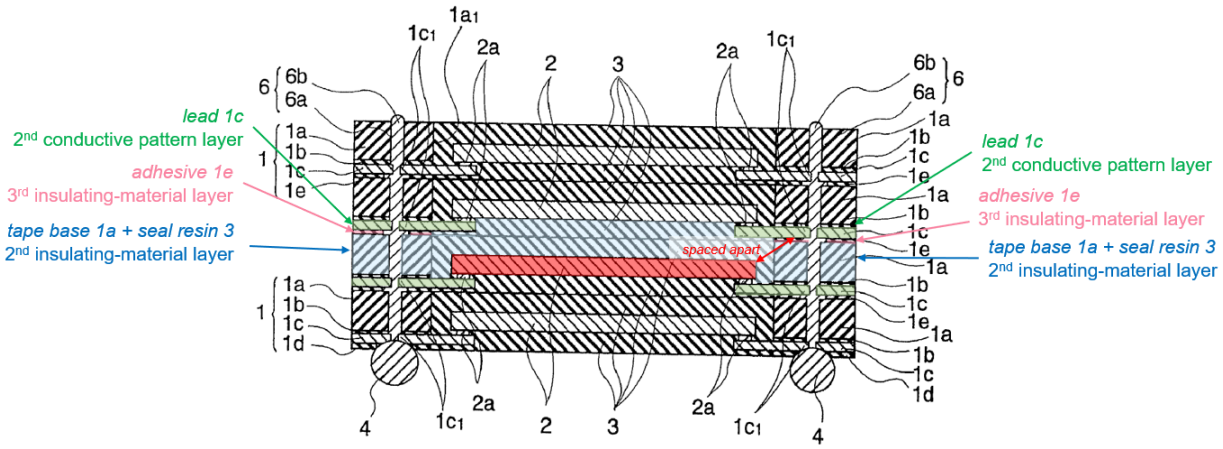
xi. Claim 11

[11] The electronic module of claim 10, wherein the second conductive pattern layer is spaced apart from the component by the second and third insulating-material layers.

99. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [11]. For example, Tsubosaki010 discloses that the upper set of leads 1c (***second conductive-pattern layer***) is spaced apart from the semiconductor chip 2 (***component***) by (i) the tape base 1a or the tape base 1a together with seal resin 3 (***second insulating-material layer***) and (ii) the adhesive layer 1e (***third insulating-material layer***). *See* Tsubosaki010, ¶¶[0120]-[0123] ("both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3"), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d] and Claim [4]; *generally id.*, [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated) – First Mapping



APPLE-1005, FIG. 14 (annotated) – Second Mapping

xii. Claim 12

[12] The electronic module of claim 11, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.

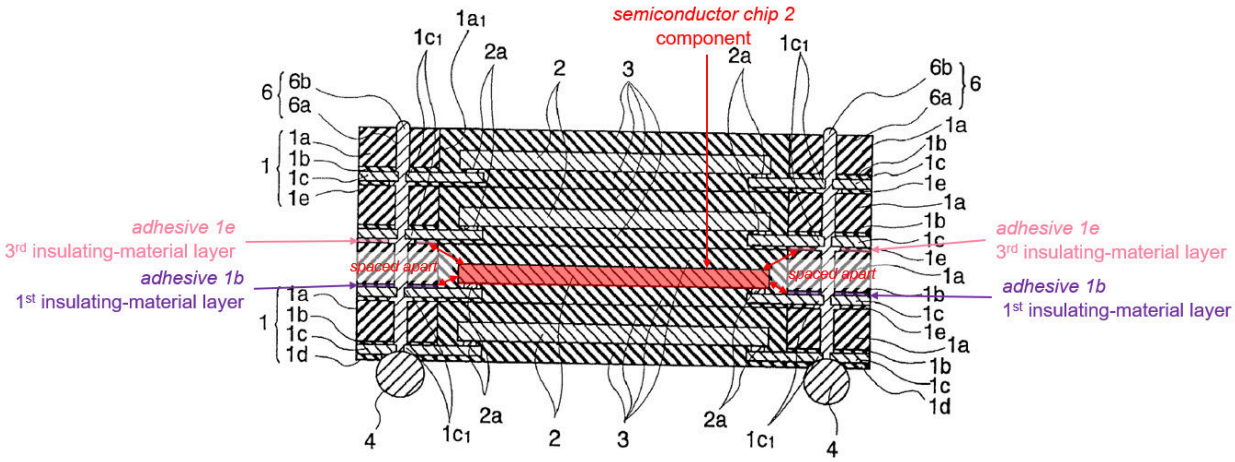
100. *Supra*, Claim [5].

xiii. Claim 13

[13] The electronic module of claim 8, wherein the first and third insulating-material layers are spaced apart from the component.

101. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [13]. For example, Tsubosaki010 discloses that the adhesive layer 1b (***first insulating-material layer***) and the adhesive layer 1e (***third insulating-material layer***) are both spaced apart from the semiconductor chip 2 (***component***). Tsubosaki010's seal resin 3 surrounds the semiconductor chip 2 thus separating the semiconductor chip 2 from the adhesive layers 1b and 1e. Tsubosaki010,

¶¶[0065], [0082]-[0085]; *see also id.*, ¶[0092] ("the thickness D1 of the seal resin 3 [can] be equal to the thickness D2 of tape carrier 1"), [0063], [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated)

xiv. Claim 14

[14] The electronic module of claim 8, wherein the first and third insulating-material layers comprise a first material, the second insulating-material layer comprises a second material, the first material being different than the second material.

102. The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [14]. As discussed above, in the Tsubosaki010-Tsubosaki405 combination, adhesive layer 1b provides a "***first insulating-material layer***," tape base 1a provides a "***second insulating-material layer***" according to a first mapping, tape base 1a together with seal resin 3 provides a "***second insulating-material layer***" according to a second mapping, and adhesive layer 1e provides a "***third insulating-***

material layer." *Supra*, Elements [1a], [1d], [8e]. In the combination, Tsubosaki405 renders obvious implementing adhesive layers 1b and 1e with an adhesive film such as polyetheramideimide and implementing tape base 1a as another suitable polyimide film such as captone that lacks similar adhesive properties. Tsubosaki405, 7:32-41, FIG. 5; *supra*, §§X.B-C; *see also* Tsubosaki010, [0111] (adhesive 1e "made of a thermally deformable polyimide resin material"). Tsubosaki010 further discloses that seal resin 3 can be an epoxy-based resin. Tsubosaki010, [0076].

103. Accordingly, in the combination, the first insulating-material layer 1b and third-insulating material layer 1e comprise a first material (*e.g.,* polyetheramideimide or another adhesive film) that is different than a second material of the second insulating-material layer from tape base 1a or seal resin 3 (*e.g.,* captone or another non-adhesive polyimide film and/or epoxy-based resin). Tsubosaki405 also demonstrates the known option of using the same adhesive material on either side of a tape base member, and it would have been obvious to implement Tsubosaki010's adhesive layers 1b and 1e to include at least a same first material as taught in Tsubosaki405 to simplify the construction and minimize the number of different adhesives used in constructing the multi-layered TCP. Tsubosaki405, 7:32-41, FIG. 5. A POSITA would have reasonably expected

success using a same thermally deformable polyimide resin or other suitable insulating material for both adhesives 1b and 1e given that both adhesive layers perform a similar function of binding the tape base member 1a to a lead 1c in the multi-layered TCP structure.

XI. GROUND 1B: TSUBOSAKI010 RENDERS OBVIOUS CLAIMS 1-14

104. As I addressed above in Ground 1A, a POSITA would have found it obvious based on Tsubosaki405 to implement Tsubosaki010's tape base 1a and adhesive layers 1b and 1e with insulating materials. But the teachings of Tsubosaki405 would not have been necessary to be applied in combination for a POSITA to have been prompted to use insulating materials for each of tape base 1a and adhesive layers 1b and 1e in Tusbosaki010's device. The general background knowledge of a POSITA also would have rendered the use of insulating materials for these components obvious, especially as the use of insulating materials for adhesives and tape bases was well known before the Critical Date and polyimide materials that Tsubosaki010 discloses for the tape base and adhesive are commonly insulating materials. *Id.* (citing corroborating exhibits APPLE-1011, XX; APPLE-1006, 8 ("[e]poxies are noted for their excellent dielectric properties"); APPLE-1005, [0064], [0111], [0118]; *see also id*., APPLE-1017, 81, Abstract; APPLE-1018, Abstract; APPLE-1019, 239. A POSITA would have been motivated and would have reasonably expected success using insulating materials for the tape

base 1a and adhesives 1b, 1e for substantially the same reasons that I addressed above in Ground 1A. The resulting version of Tsubosaki010's device would have provided all elements of claims 1-14 based on the mappings described above in Ground 1A. *Id.*

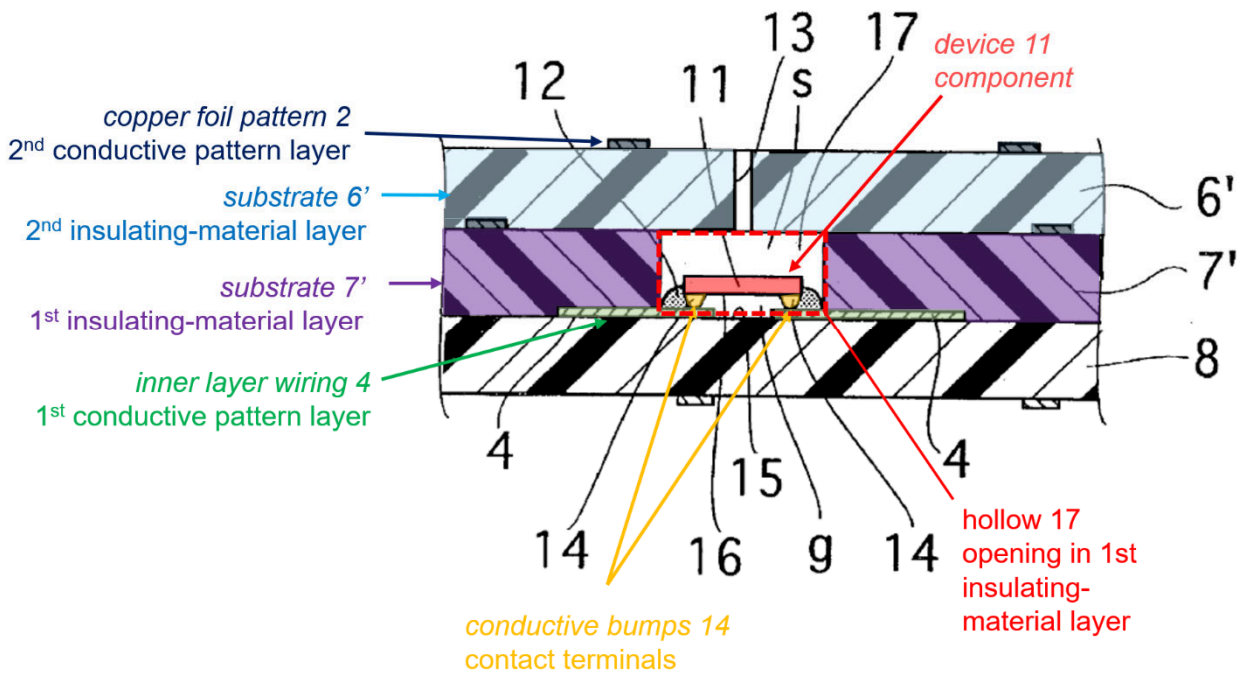
XII. GROUND 2: OYA IN VIEW OF SHUGG RENDERS OBVIOUS CLAIMS 1, 3-4, 6-8, 10-11, AND 13-14

A. Oya Overview

105. Oya discloses a multi-layered printed circuit board ("PCB") 1 adapted to house a semiconductor component having a "functional surface" such as a surface acoustic wave (SAW) device or a micro electromechanical system (MEMS). Oya, Abstract, ¶¶[0005], [0012], [0042]-[0043], [0070], FIG. 1. According to the Abstract, Oya's PCB "is capable of air-tightly sealing a function surface of a device and of preventing excessive stress from acting on the device itself …." *Id.*.

106. In an embodiment illustrated by FIG. 7, semiconductor device 11 is disposed within a hollow 17 of a PCB substrate 7'. Oya, ¶¶ [0067]-[0071]. Another substrate 6' is attached to a top surface of substrate 7', while a substrate 8 is attached to a bottom surface of substrate 7'. *Id.*, ¶[0067]. "[D]evice 11 [is first disposed] on the substrate 8." Id. 67. "[S]ubstrate 7' having a through-hole formed therein may be stacked [on the substrate 8]." *Id.* The "substrate 6' may be

stacked further [on the substrate 7] so as to cover the through-hole so as to form the hollow 17." *Id.*



APPLE-1004, FIG. 7 (annotated)

107. Oya's PCB 1 includes two outer layer wirings 2 and 3 and two inner layer wirings 4 and 5. Oya, ¶[0039], FIGS. 1, 7. As shown in FIG. 7, the inner layer wiring 4 is disposed between the substrate 8 and substrate 7', and the inner layer wiring 5 is shown between substrate 7' and substrate 6'. In one implementation, Oya teaches that outer layer wirings 2, 3 can be disposed on surfaces of the substrate 6' and substrate 8, as illustrated in FIGS. 7. A functional surface 16 of the device 11 is mounted face down in the hollow 17. *Id.*, ¶[0040].

108. Oya's device 11 is electrically connected to the inner layer wiring 4 by a set of conductive bumps 14. APPLE-1004, ¶ [0040]. The set of conductive bumps 14, on the functional surface 16 side of the device 11, are formed "in correspondence with" the electrode pads 22 and 25. APPLE-1004, ¶[0048]. Oya's electrode pads 22 and 25 are electrically connected to the wiring 4 via the conductive bumps 14. APPLE-1004, ¶[0048]. A sealing member 12 covers the conductive bumps 14, protecting the conductive bumps 14 and the functional surface 16 of the device 11. APPLE-1004, ¶[0057]. Like embodiments disclosed in the '816 Patent, Oya utilizes conventional materials in the formation of PCB 1. *See* APPLE-1004, ¶¶[0055], [0051]. For example, Oya's outer layer wirings 2 and 3 can be formed from copper, the substrate 7'can be formed of an epoxy resin, and the substrates 6' and 8 can be made of prepregs. *See* Oya, ¶¶[0055], [0051].

B. Shugg Overview

109. Shugg's Handbook of Electrical and Electronic Insulating Materials, published in 1995, describes various "properties, uses, standards, and specifications of electrical insulating materials" commonly used in manufacturing electronics. *See* APPLE-1006, xxi. Among the materials disclosed as suitable for use in electronics are prepregs, epoxy resins, and polyimide. *See, e.g.*, APPLE-1006, 228-229 (polyimide), 126-127 (epoxy resins), 217-276 (prepregs).

C. The Oya-Shugg Combination Overview

110. Oya discloses that its substrates, *e.g.,* substrates 6, 7', and 8', can be made from an epoxy resin and can include "prepreg" material (*e.g.,* a "pre-impregnated" composite material that includes a fabric). APPLE-1004, ¶¶ [0051], [0060]. Shugg demonstrates that epoxy resin and prepregs were commonly implemented as insulating materials in electronic devices. Shugg, 144, 151-152, 199-200, 205-208, 244, 269-270, 290-291, 301-304, 306-308. To the extent Oya does not expressly disclose that the substrate layers of its printed circuit board are made from insulating materials, it would have been obvious to use insulating materials for this purpose based on the teachings of Shugg. *See* APPLE-1006, 126-127 (epoxy resins); id., 217-276 (prepregs). Multiple reasons would have prompted a POSITA to combine Oya and Shugg to implement insulating substrate layers in Oya's PCB.

111. *First*, a POSITA would have used insulators as the substrates to ensure the wiring and conductive leads disposed between different layers of the substrates are electrically isolated. The conductive pathways in Oya's device would predictably carry power and/or information signals to and from various electrical components. Insulators, having a higher resistivity to the flow of electrical current, are known to be useful in confining electrical signals to the electrical conductors. By confining the signals to their respective conductive

pathways, the insulators would advantageously isolate conductive elements, thus facilitating the proper routing of the electrical signals. A POSITA would have recognized that failing to separate signals would dimmish the performance of an electrical device. *See* APPLE-1008, 2, 78, 104, 110, 112, 117, 120, 122, 126, 155, 183 (discussing prepregs); *see* also id., 28, 78, 107, 115, 127, 129, 146, 148, 159, 179 (discussing epoxide resin or epoxy resin). For example, failing to separate electrical signals within a circuit can produce short circuit, cross-talk, reduce signal quality, cause overheating, and performance degradation. An insulator would have been recognized by a POSITA as a well-known solution to these well-known problems.

112. *Second*, a POSITA would have been prompted to implement the substrate layers in Oya's PCB with insulating materials to reduce signal loss in the conductive layers of the multi-layered semiconductor. Loss of signal quality is a known problem in electronic device. Insulators are known to have a higher resistivity to the flow of electrical current than electrical conductors. Surrounding electrical conductors with an insulator, having higher resistivity than air or other electrical conductors, facilitates the transmission of the signal along the electrical conductor.

113. *Third*, a POSITA would have been prompted to implement the substrate layers in Oya's PCB with insulating materials to reduce the risk of known hazards that can be caused by conductors that touch or are too close to one another. A POSITA would have understood that electrical conductors that are inadvertently contacted or electrically coupled can produce cross-talk, short circuits, and electrical hazards. Insulators would have been known to the POSITA for their ability to form barriers between energized parts (*e.g.,* electrical conductors) of an electric circuit within a semiconductor device. A POSITA would have known that insulators were useful for confining the flow of current along a desired path.

114. *Fourth*, a POSITA would have found the use of insulating materials for Oya's substrates to be obvious to try. There exist a finite number of classes of materials that could be used to implement the substrates—namely, either insulating materials or conductive materials—and a POSITA would have had ample reason to try insulating materials for each of the reasons described herein (*e.g.,* to promote electrical isolation between electrical conductors within the PCB).

115. *Fifth*, implementing Oya's substrates with insulating materials would have been obvious as a predictable application of known insulating materials as taught by Shugg to known structures as taught by Oya to achieve merely predictable results.

116. A POSITA would have had a reasonable expectation of success implementing Oya's substrate layers with insulating materials, especially since insulating substrate materials were well known before the '816 Patent. *See also* APPLE-1004, ¶[0051]; APPLE-1008, 61; APPLE-1009, 78, 79-81. Oya and Shugg are both also analogous art in that they are both in the same field of endeavor and/or reasonably pertinent to the problem faced by the inventors of the '816 Patent. For example, like the '816 Patent, Oya and Shugg both describe techniques for manufacturing and packaging electronic modules.

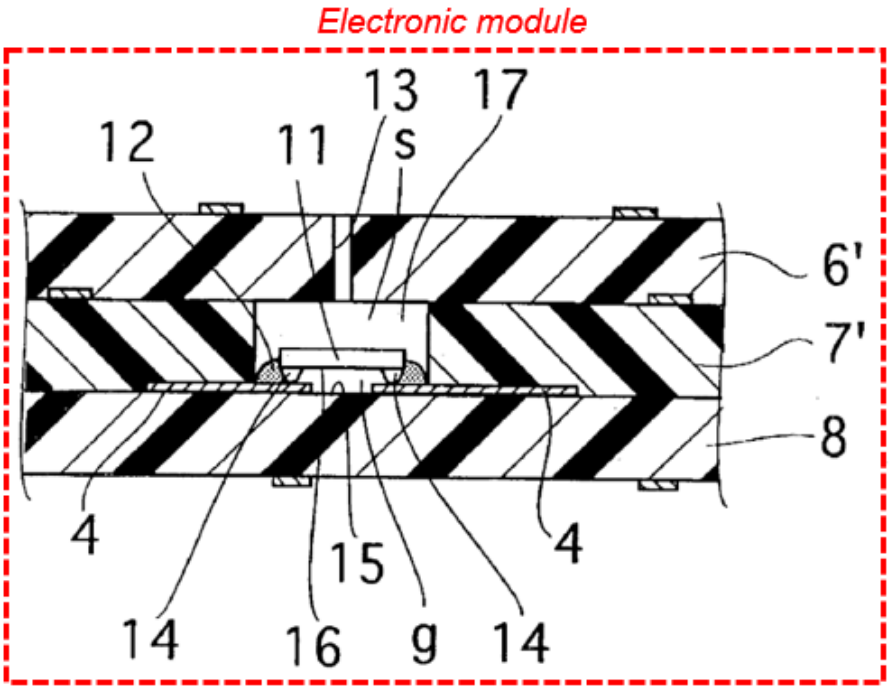
D. Analysis

i. Claim 1

[1pre] An electronic module, comprising:

117. To the extent the preamble is a limitation, the Oya-Shugg combination renders it obvious. For example, Oya discloses a printed circuit board (PCB) 1 that provides an "***electronic module***" as recited in [1pre]. Oya, ¶[0003] ("The present invention relates to a ***printed circuit board*** having a structure in which a device is embedded in a cavity in a wiring board and a fabrication process thereof"); *see also id.*, Abstract ("The present invention provides a printed circuit board which is capable of air-tightly sealing a functional surface of a device and of preventing excessive stress from acting on the device itself or a conductive bump conjugating the device with a wiring board and a method of fabricating the printed circuit

board.”), [0013]-[0015], [0024], FIG. 7; *cf.* APPLE-1001, 1:23-27 (’816 Patent similarly explaining that an “electronic module … can be a module like a circuit board, which includes several components, which are connected to each other electrically”).



APPLE-1004, FIG. 7 (annotated)

[1a] a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;

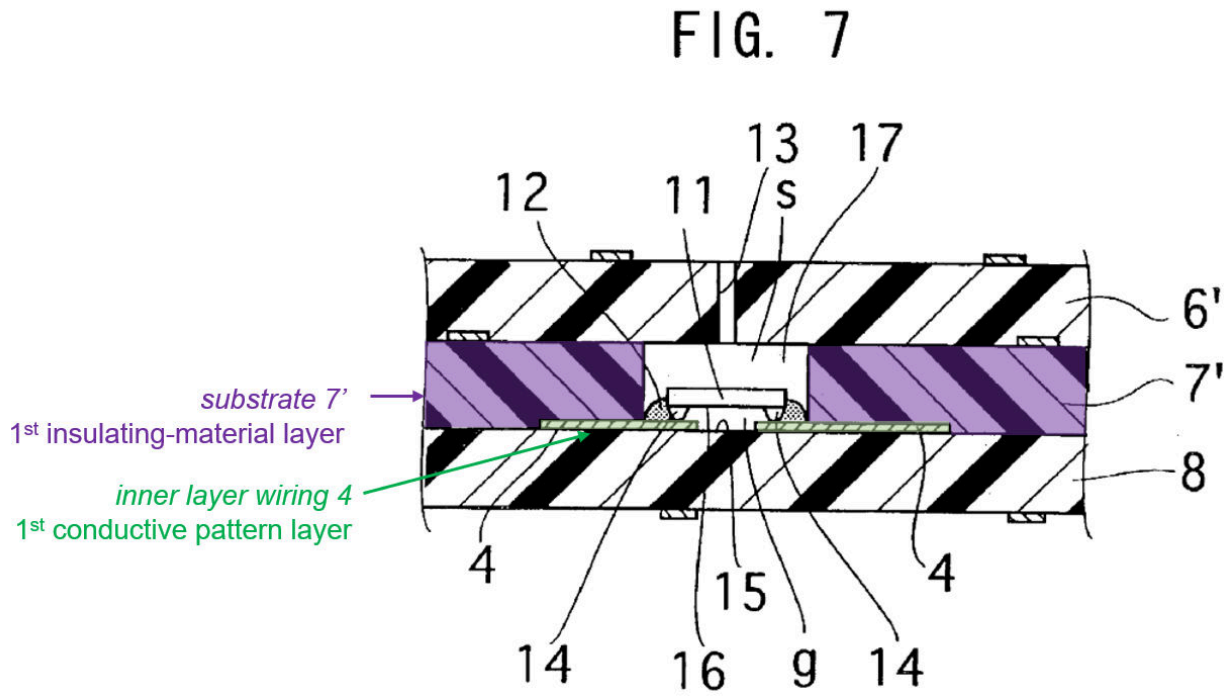
118. The Oya-Shugg combination renders Element [1a] obvious. For example, in the combination, Oya discloses an inner layer wiring 4 that corresponds to a “***first conductive pattern layer***” and a substrate 7’ that corresponds to a “***first insulating-material layer***” as claimed. Oya, FIG. 7. As

shown in FIG. 7 (reproduced and annotated below), Oya's substrate 7' is arranged on at least one surface (*e.g.,* a top surface) of the inner wiring layer 4. Oya, ¶[0067] ("As shown in FIG. 7, after mounting the device 11 on the substrate 8, a substrate 7 having a through-hole formed therein may be stacked thereon …"), [0066] ("Alternatively, different from the above-mentioned fabrication process, after preparing a multilayer printed circuit board having a preliminarily provided recess, a device may be mounted in the recess, …"); *see also id.*, [0045]-[0047] & FIG. 2 (describing an etching process for forming wiring layer 4).

119. I note that the '816 Patent describes that the opening is first formed in the first insulating-material layer and the component is subsequently placed in the opening to form an electrical connection with the first conductive pattern layer. *Supra*, §XII.A. Oya's disclosure at paragraph [0066] aligns with these techniques as described in the '816 Patent and confirms that the option of first forming an opening before mounting the component would have been an obvious design choice that would have simplified construction of Oya's device in some cases. My opinions regarding Oya's disclosure are not based on the specific processing steps described in paragraph [0067] of Oya.

120. Oya teaches that the substrates of the wiring board, *e.g.,* substrate 7', can be "prepreg" and "composed of an epoxy resin or the like." Oya, ¶¶[0045],

[0051]. For the reasons described above, it would have been obvious to a POSITA based on Shugg to implement Oya's substrates including substrate 7' as an insulator such that substrate layer 7' would be a "***first insulating-material layer***" arranged on at least one surface of the inner wiring layer 4 (***first conductive pattern layer***) as claimed. *Supra*, §XII.C.



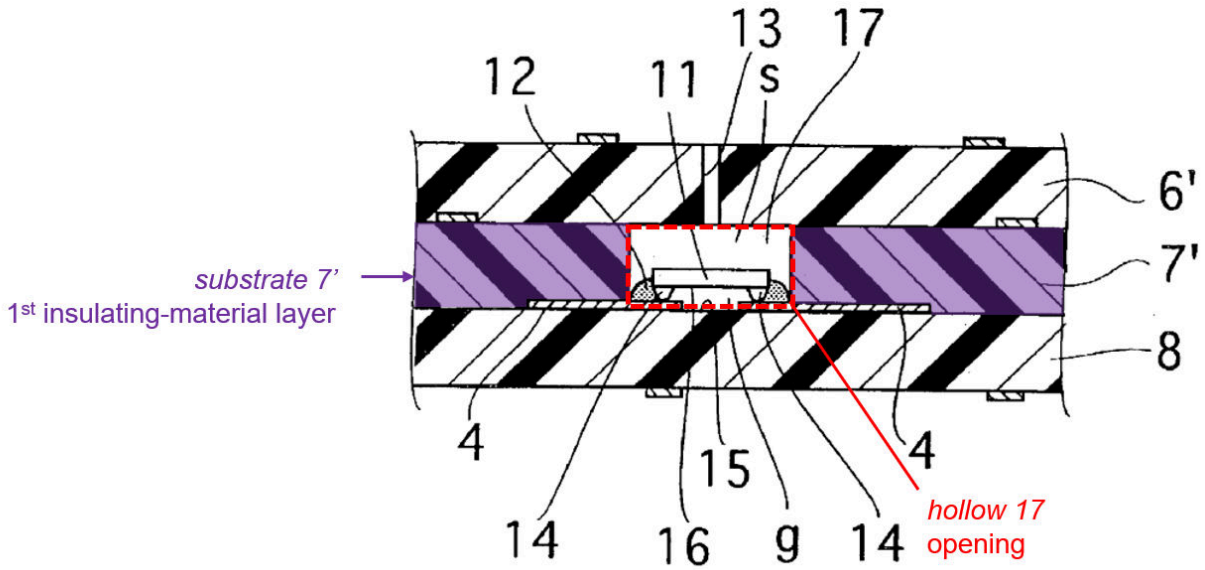
APPLE-1004, FIG. 7 (annotated)

[1b] at least one opening in the first insulating-material layer that extends through the first insulating-material layer;

121. The Oya-Shugg combination renders Element [1b] obvious. For example, Oya discloses a "through-hole," "recess," or "hollow 17" that forms an "***opening***" in and that extends through the substrate 7' (***first insulating-material***

layer). Oya, ¶¶[0067] ("As shown in FIG. 7, after mounting the device 11 on the substrate 8, a substrate 7 having a through-hole formed therein may be stacked thereon and a substrate 6 may be stacked further thereon so as to cover the through-hole so as to form the hollow 17."), [0066] ("after preparing a multilayer printed circuit board having a preliminarily provided recess, a device may be mounted in the recess"), FIG. 7; *see also id.*, [0014] ("The printed circuit board of the present invention has a device mounted in a hollow formed in a wiring board"), [0040] ("hollow 17 formed in the substrate 6"), [0052] ("recess 26 forms a hollow 17 for accommodating the device 11"), [0053].

FIG. 7



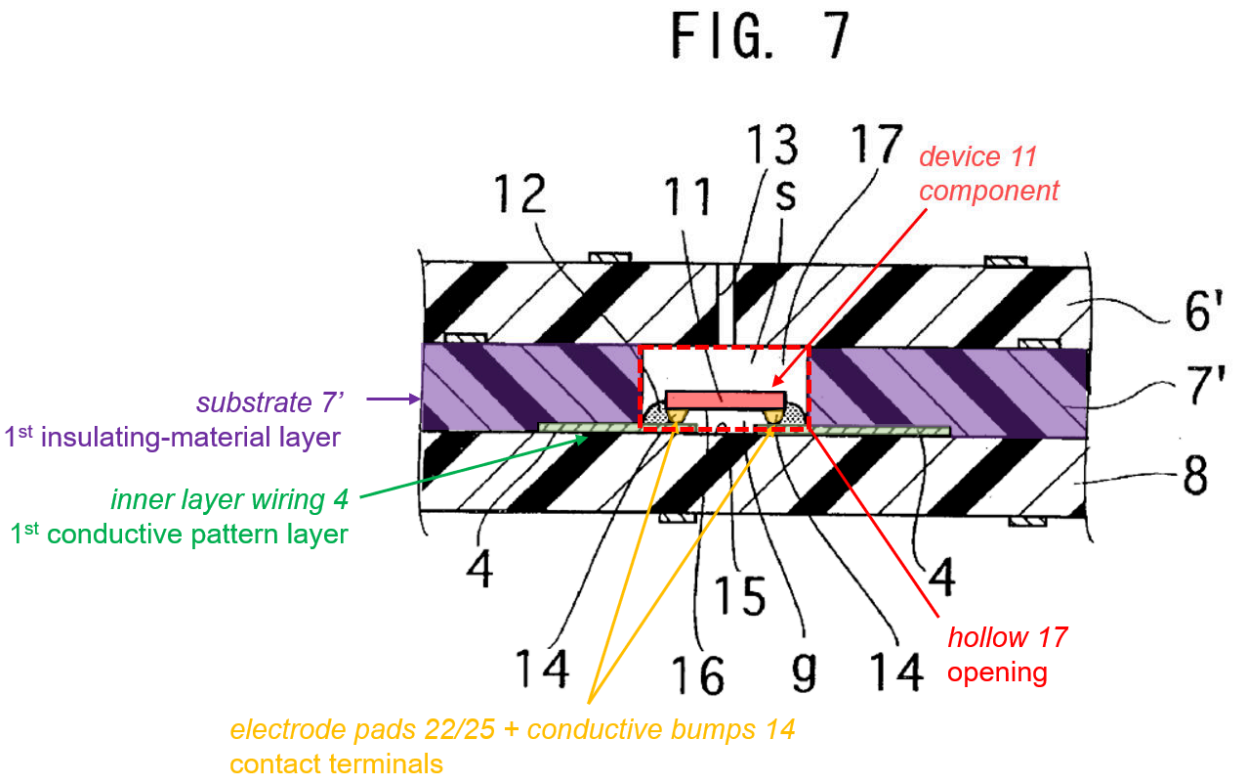
APPLE-1004, FIG. 7 (annotated)

[1c] a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;

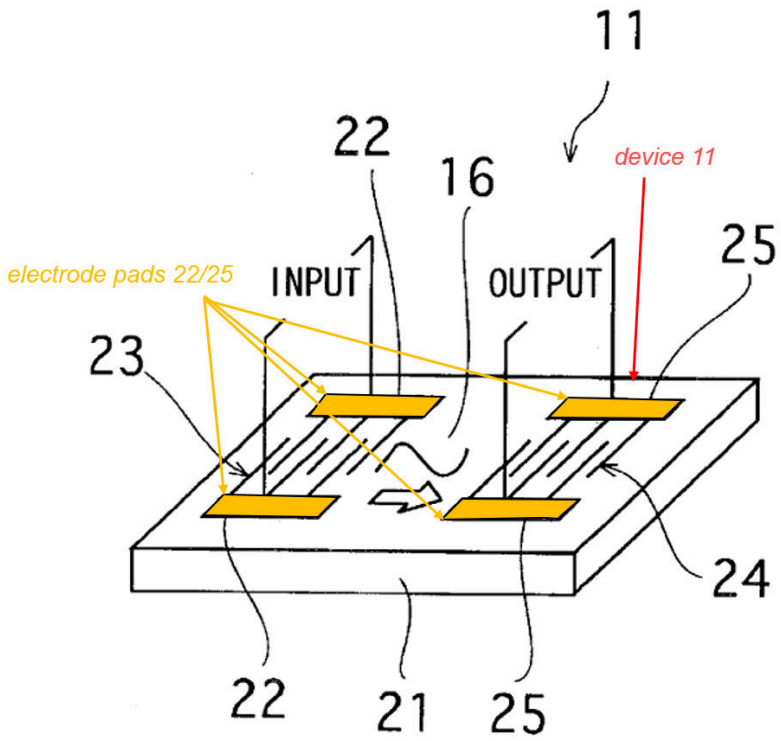
122. The Oya-Shugg combination renders Element [1c] obvious. For example, Oya discloses a device 11 (***component***) arranged at least partially within the hollow 17 (also referred to in Oya as a recess or through-hole) of the substrate 7' (***first insulating-material layer***). Oya discloses that the device 11 can be a surface acoustic wave (SAW) device, a Micro Electro Mechanical Systems (MEMS), or other device that has a functional surface in different embodiments. Oya, ¶¶[0039]-[0043], [0070], FIG. 9; *see also id.*, [0005]-[0014], Abstract. The device 11 can be arranged in the opening by "preparing a multilayer printed circuit board having a preliminarily provided recess, [in which] a device may be mounted in the recess, side surfaces of the device sealed with a resin and the recess may be covered with another substrate so as to obtain a hollow having the device sealed therein." *Id.*, ¶[0066]; *see also id.*, [0067].

123. Oya also discloses that the device 11 (***component***) comprises a set of electrode pads, *e.g.,* electrode pads 22, 25. Oya, ¶¶[0043], [0048], FIG. 9. "On the functional surface 16 side [of device 11], a plurality of conductive bumps 14 are formed in correspondence with the electrode pads 22 and 25" and "[b]y bonding these conductive bumps 14 after positioning them on the wiring 4, the electrode

pads 22 and 25 are electrically connected to the wiring 4 through the conductive bumps 14." *Id.*, [0048]. "The conductive bumps 14 may include a solder bump, a gold stud bump, and the like." *Id.*, [0040]. The electrode pads of the device 11 (***component***), the conductive bumps, and the electrode pads together with the conductive bumps provide alternative mappings to the claimed "***contact terminals***" of the device 11 electrically connected to the wiring 4 (***first conductive-pattern layer***).



APPLE-1004, FIG. 7 (annotated)



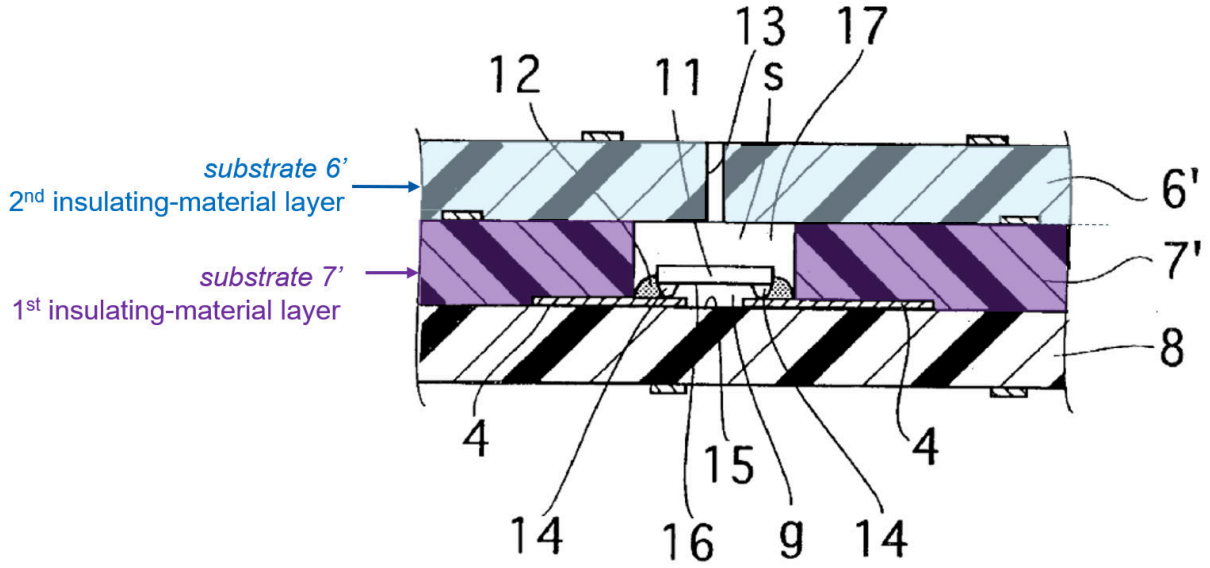
APPLE-1004, FIG. 9 (annotated)

[1d] a second insulating-material layer disposed on the first insulating-material layer, and;

124. The Oya-Shugg combination renders Element [1d] obvious. For example, Oya discloses a substrate layer 6' disposed on the substrate layer 7' (***first insulating-material layer***). Oya, ¶[0067] ("a substrate 7' having a through-hole formed therein may be stacked thereon and a substrate 6' may be stacked further thereon so as to cover the through-hole so as to form the hollow 17"), FIG. 7; *see also id.*, [0066], [0051] ("the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7 … [t]hen, the substrates are sandwiched between heater plates and are pressed and heated").

125. Oya teaches that the substrates of the wiring board, *e.g.,* substrate 6', can be "prepreg" and "composed of an epoxy resin or the like." Oya, ¶¶[0045], [0051]. For the reasons described above, it would have been obvious to a POSITA based on the teachings of Shugg to implement Oya's substrates including substrate 6' as an insulator such that substrate layer 6' would be a "***second insulating-material layer***" disposed on the substrate layer 7' (***first insulating-material layer***) as claimed. *Supra*, §XII.C; *see also* Oya, ¶¶[0040], [0051]-[0053], [0060], [0067].

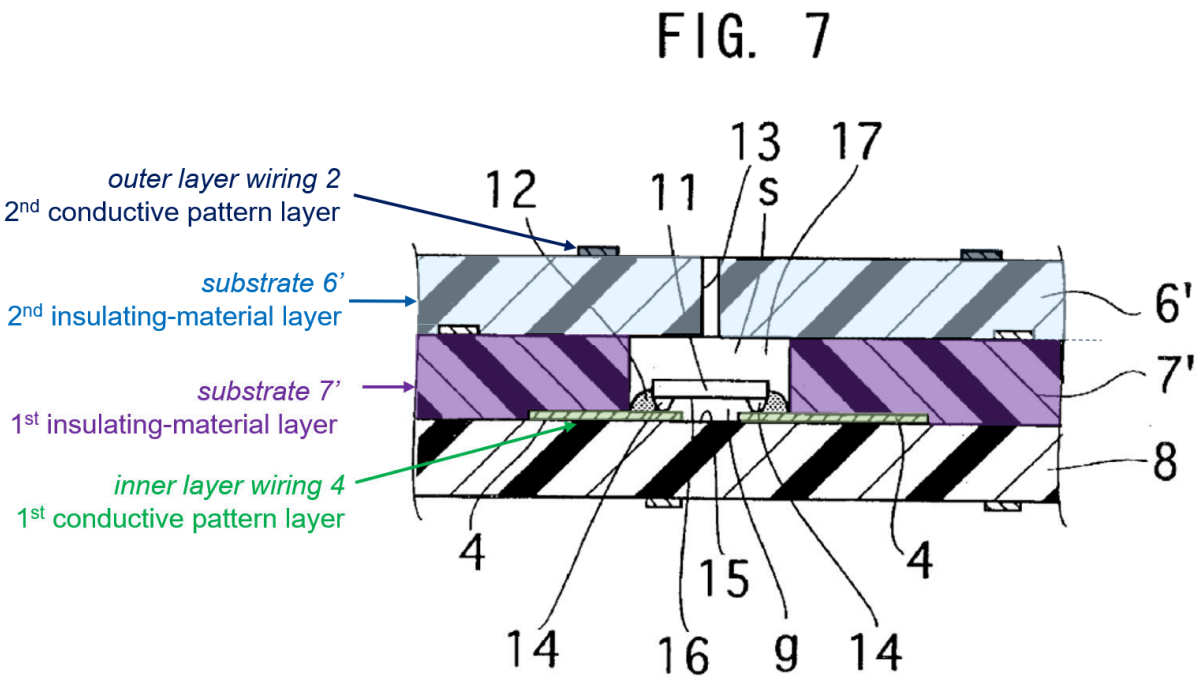
FIG. 7



APPLE-1004, FIG. 7 (annotated)

[1e] a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers;

126. The Oya-Shugg combination renders Element [1e] obvious. For example, Oya discloses an outer layer wiring 2 that provides a "***second conductive pattern layer***" as claimed. Oya, ¶[0067], FIG. 7; *see also id.*, ¶¶[0039] ("The wiring board 10 is a multilayer printed circuit board having two outer layer wirings 2 and 3 and two inner layer wirings 4 and 5."). The outer layer wiring 2 is also referred to as a "copper foil pattern 2." Oya, ¶[0055] ("copper foil patterns 2 and 3."), [0051] ("the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7, respectively, and a copper foil is stacked on each of the substrates 6 and 8"). As shown in FIG. 7, the outer layer wiring 2 is disposed directly on substrate 6' and is spaced apart from the inner layer wiring 4 (***first conductive pattern layer***) by at least the substrate layer 7' (***first insulating-material layer***) and the substrate layer 6'(***second insulating-material layer***). *Id.*.



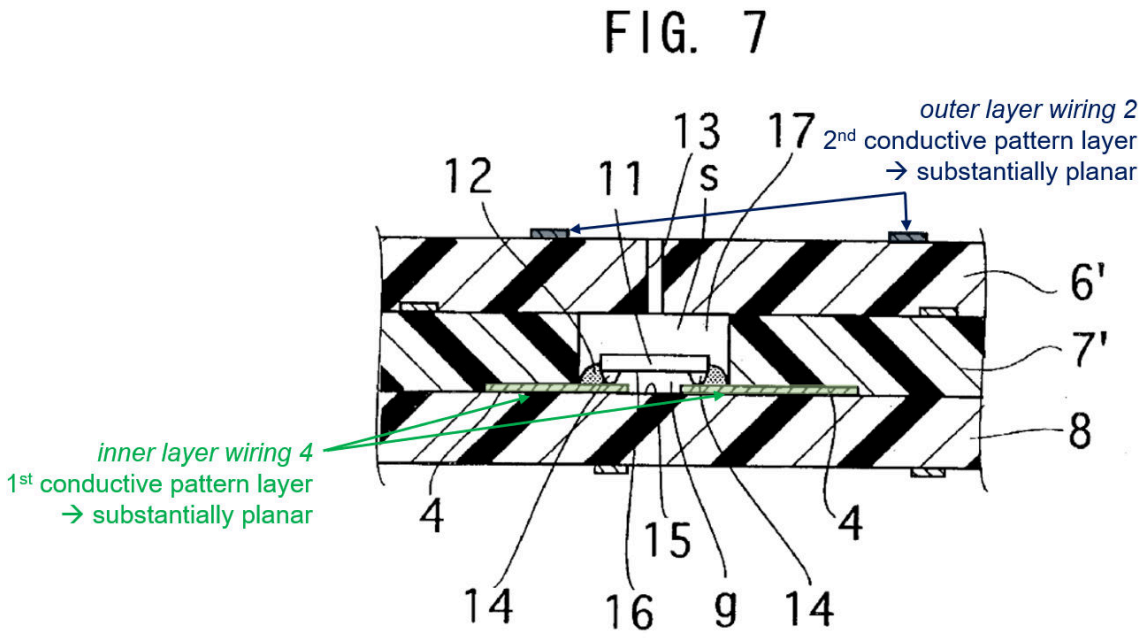
APPLE-1007, FIG. 7 (annotated)

[1f] wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

127. The Oya-Shugg combination renders Element [1f] obvious. In the combination, Oya's inner layer wiring 4 (***first conductive pattern layer***) and outer layer wiring 2 (***second conductive pattern layer***) are each substantially planar. Oya, ¶¶[0051], [0039], [0054]-[0055], [0066]-[0067]; *see also id.*, FIGS. 1, 7-8. For example, when forming the inner layer wiring 4, Oya teaches that a copper foil or a copper plating is disposed directly "on both surfaces of the substrate 7." Oya, ¶[0045]. After a dry film is disposed on the copper foil, a mask having a circuit pattern is thereon disposed. *Id.*, ¶[0046]. Using the dry film as a mask, the copper foil is wet-etched and the wirings 4 and 5 are formed. *Id.*, ¶¶[0046]-[0047]. A

POSITA would have understood and it would have been obvious from these teachings, including the fact that the inner layer wiring 4 is formed on the surface of a substantially planar substrate 8, that the inner layer wiring 4 is substantially planar.

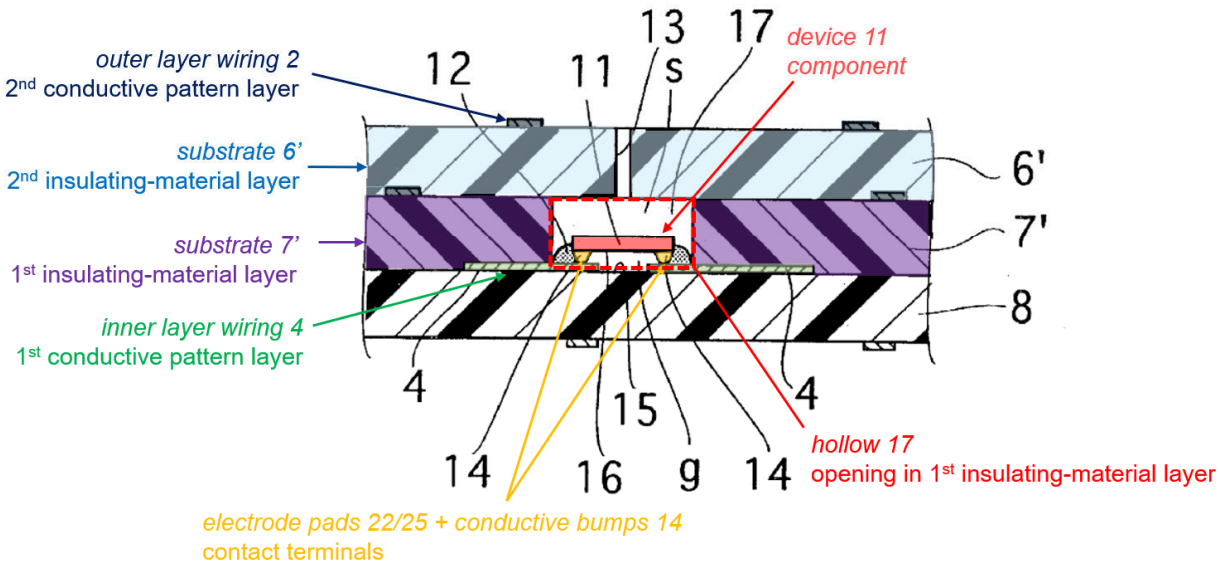
128. Furthermore, as illustrated in FIG. 7, Oya's outer layer wiring 2 is formed on substrate 6', thereby providing a second conductive pattern layer that is substantially planar. Oya, ¶[0067], FIG. 7, *see also id.*, [0051] ("a copper foil is stacked on each of the substrates 6 and 8"), [0054]-[0055] ("[A]fter sticking a dry film on the copper foil stuck on each of the surfaces of the substrates 6 and 8…. According to this processing, desired copper foil patterns 2 and 3 can be obtained."). Accordingly, a POSITA would have understood and it would have been obvious from Oya's teachings, including the fact that the outer layer wiring 2 is formed on the surface of a substantially planar substrate 6', that the outer layer wiring 2 is also substantially planar.



APPLE-1007, FIG. 7 (annotated)

129. The following version of FIG. 7 further illustrates representative mappings of various structures from Oya's electronic module to corresponding structures recited in claim 1:

FIG. 7

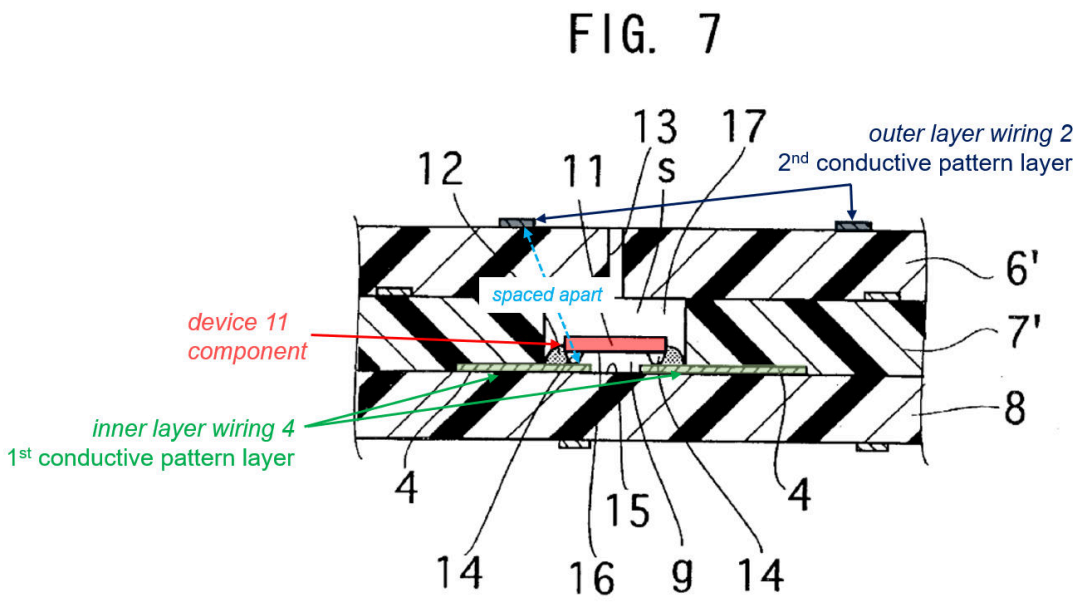


APPLE-1007, FIG. 7 (annotated)

ii. Claim 3

[3] The electronic module of claim 1, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.

130. The Oya-Shugg combination renders Claim [3] obvious. For example, Oya discloses that the outer layer wiring 2 (***second conductive pattern layer***) is spaced apart from the inner layer wiring 4 (***first conductive pattern layer***) by the device 11 (***component***). *Id.* This configuration is illustrated in FIG. 7:



APPLE-1004, FIG. 7 (annotated)

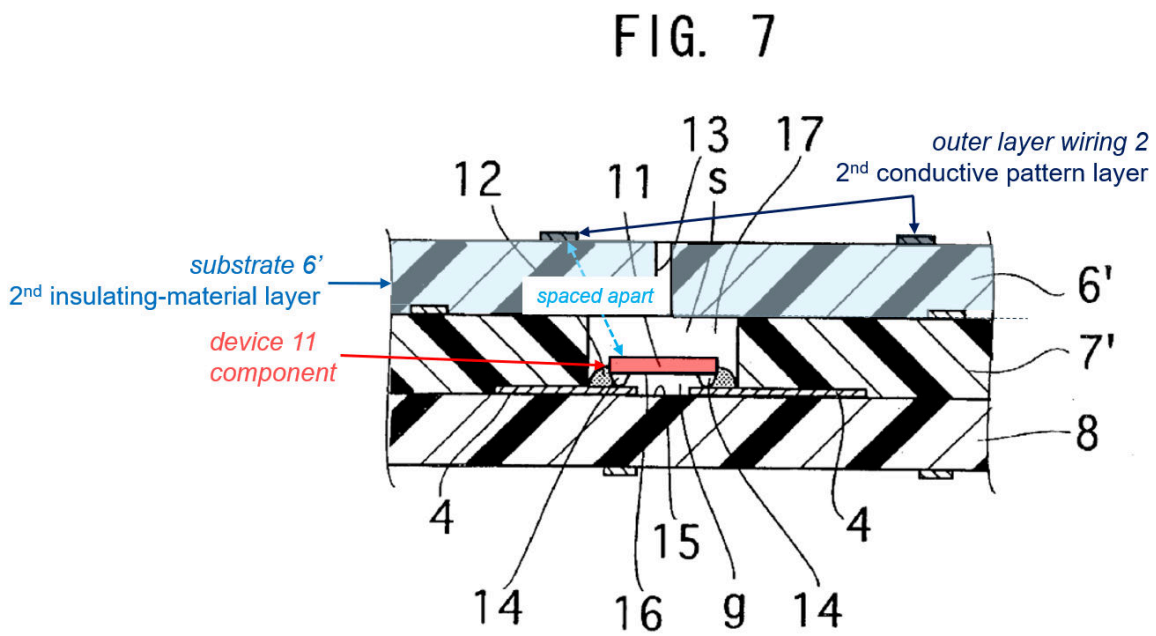
131. *See also id.*, ¶40 (describing a gap of "several tens of μm" between an inner surface 15 of the hollow 17 and the functional surface 16 of the device 11), [0066]-[0067].

iii. Claim 4

[4] The electronic module of claim 3, wherein the second conductive pattern layer is spaced apart from the component by the second insulating-material layer.

132. The Oya-Shugg combination renders Claim [4] obvious. For example, Oya discloses that the outer layer wiring 2 (***second conductive pattern layer***) is disposed on a top surface of the substrate 6' (***second insulating-material layer***), as shown in FIG. 7. Oya, ¶¶[0066]-[0067], FIG. 7. The device 11 (***component***) is disposed within the hollow 17 fashioned inside the substrate 7'. *Id.*

The substrate 7' is disposed below the substrate 6'. *Id.* Oya discloses that "the device 11 [is disposed] on the substrate 8." *Id.*, [0067]. The "substrate 7' having a through-hole formed therein may be stacked [on the substrate 8]." *Id.* The "substrate 6' may be stacked further [on the substrate 7] so as to cover the through-hole so as to form the hollow 17." *Id.* As such, Oya's outer layer wiring 2 (***second conductive pattern layer***) is spaced apart from the device 11 (***component***) by the substrate 6' (***second insulating-material layer***). *Id.*.

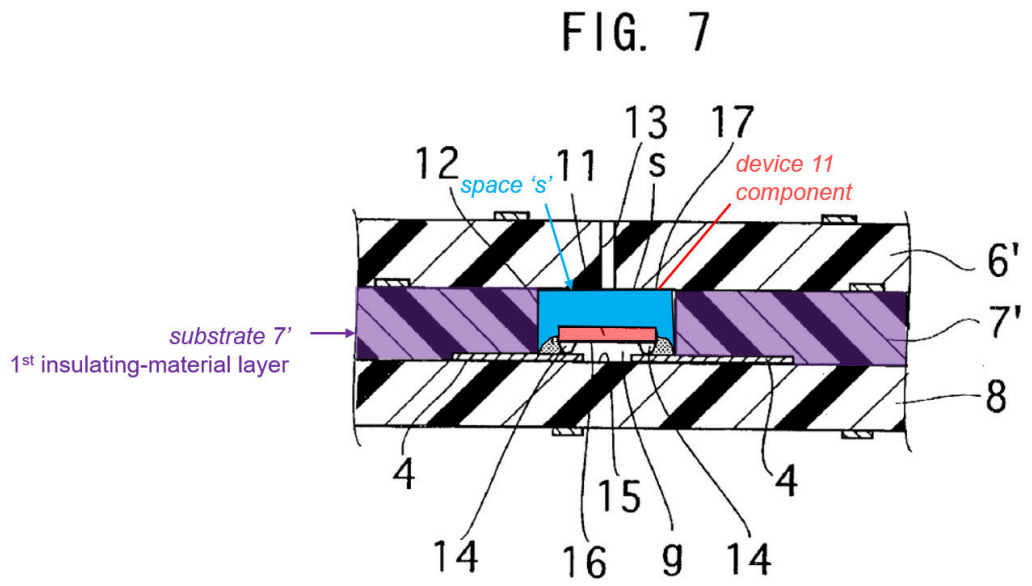


APPLE-1004, FIG. 7 (annotated)

iv. Claim 6

[6] The electronic module of claim 1, wherein the first insulating-material layer is spaced apart from the component.

133. The Oya-Shugg combination renders Claim [6] obvious. For example, Oya discloses that the substrate 7' (***first insulating-material layer***) is spaced apart from the device 11 (***component***). *Id.* Oya's device 11 is mounted within a hollow 17 formed by the substrate 6' and the substrate 7'. Oya, ¶¶[0066]-[0067], FIG. 7; *see also id.*, ¶¶52-56. Oya further discloses that "the device 11 faces the wiring board 10 in ***non-contact having the gap g therebetween***, and the other surface of the device 11 faces the wiring board 10 in ***non-contact having the space s*** therebetween." *Id.*, ¶57. Accordingly, a POSITA in possession of Oya would have understood from the figures and description that the substrate 7' (***first insulating-material layer***) is spaced apart from the device 11 (***component***) at least by the space s provided between the device 11 and the substrate 7'.



APPLE-1004, FIG. 7 (annotated)

v. Claim 7

[7] The electronic module of claim 1, wherein the first insulating-material layer comprises a different material than a material of the second insulating-material layer.

134. The Oya-Shugg combination renders Claim [7] obvious. As discussed above, Oya teaches that the substrates of its wiring board, *e.g.,* substrates 6' and 7', can be "prepreg" and "composed of an epoxy resin or the like." Oya, ¶¶[0045], [0051]. A POSITA would have known that "prepreg" was a composite material commonly used for circuit board substrates made of pre-impregnated fibers mixed with a partially cured resin. Shugg, 289-290 ("The basic materials for making industrial laminates are called *prepregs*. A prepreg is composed of a substrate, usually paper, cotton, or glass fabric, impregnated with a thermosetting resin, generally phenolic, epoxy, or melamine."), 291 ("Epoxy resin glass-reinforced laminates … are used extensively as substrates for printed circuits."), 303-304; *see also* APPLE-1019, 239 ("[g]lass-fiber cloth pre-impregnated with epoxy-resin [was] … widely used as a composite electrical insulation in various electrical industrial products"). Consistent with this conventional understanding of prepreg, Oya explicitly confirms that the substrates can be "composed of glass fiber impregnated with a resin." Oya, ¶[0060]. Because prepreg is a composite material that is itself composed of multiple materials, substrate 7' (***first insulating-material layer***) comprises *a* material that is different than *a* material of substrate 6' (***second***

insulating-material layer) as claimed.[11] For example, substrate 7' comprises a glass fiber material that is different from a resin material of substrate 6'. *Id.* Alternatively, substrate 7' comprises a resin material that is different from a glass fiber material of substrate 6.' *Id.*

vi. Claim 8

[8pre] An electronic module, comprising:

135. *Supra*, Element [1pre].

[8a] a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;

---

[11] I understand that the term"comprise[s]" is an open-ended transition word. In the phrase "the first insulating-material layer *comprises* a different material than a material of the second insulating-material layer," claim 7 is clear that the first insulating-material layer need only *include* a material that is different from a material of the second insulating-material layer—but it need not consist only of material that is different from any/all material of the second insulating-material layer. The plain language of claim 7 is met by Oya's disclosure of one material in the first insulating-material layer that is different than another material in the second insulating-material layer. *Id.* The specification of the '816 Patent likewise confirms that "the insulating-material layer 1 can equally well be manufactured from more than one part" and "[i]t is then also possible to proceed in such a way that the insulating-material layer 1 is ***formed of more than one insulating material***." APPLE-1001, 12:36-40.

136. *Supra*, Element [1a].

[8b] an opening in the first insulating-material layer that extends through the first insulating-material layer;

137. *Supra*, Element [1b].

[8c] a component comprising contact terminals, the component being arranged at least partially within the opening, the contact terminals electrically connected to the first conductive pattern layer;

138. *Supra*, Element [1c].

[8d] a second insulating-material layer disposed on the first insulating-material layer;

139. The Oya-Shugg combination renders Element [8d] obvious. As addressed above in connection with Element [1d], Oya discloses a substrate layer 6' disposed on the substrate layer 7'. Oya, ¶[0067] ("a substrate 7' having a through-hole formed therein may be stacked thereon and a substrate 6' may be stacked further thereon so as to cover the through-hole so as to form the hollow 17"), FIG. 7; *see also id.*, [0066], [0051] ("the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7 … [t]hen, the substrates are sandwiched between heater plates and are pressed and heated"); *supra*, Element [1d].

140. Oya discloses that "[t]he wiring board 10 is a multilayer printed circuit board." Oya, ¶[0039]; *see also id.*, ¶[0066] ("preparing a multilayer printed circuit board"). Shugg further describes well-known techniques for constructing multilayer printed circuit boards like Oya's. Shugg, 307. According to Shugg,

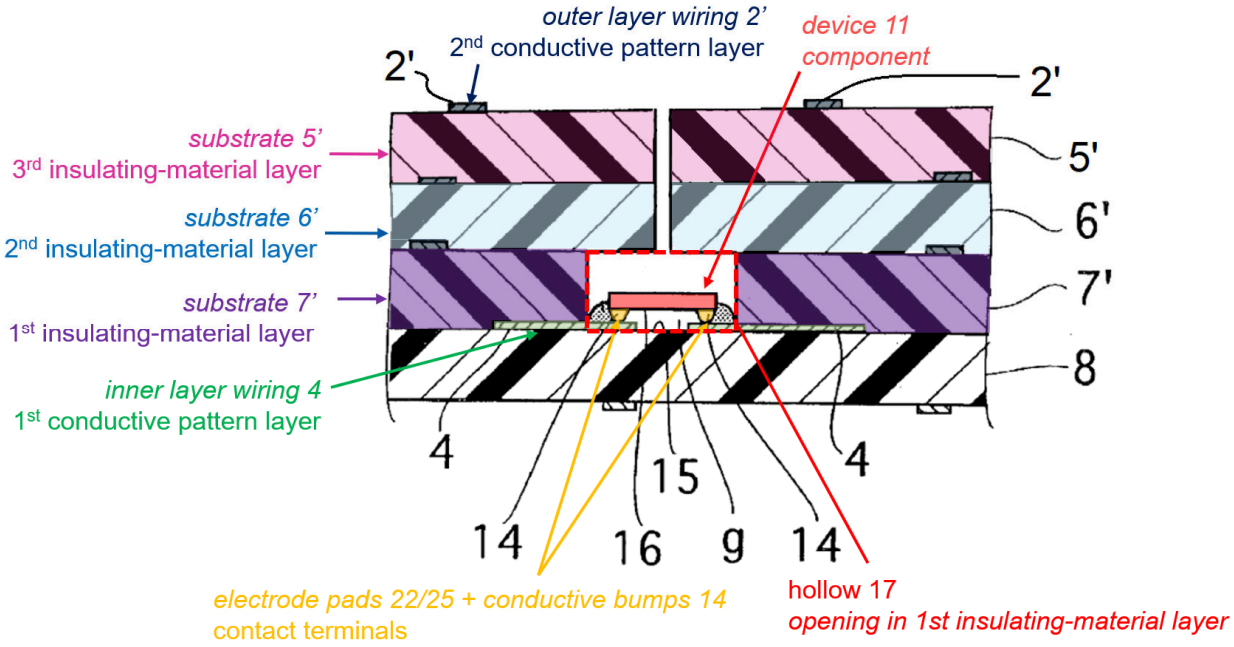
"[p]rinted circuit materials, usually of epoxy or polyimide types, may be layered to form multilayer circuits." *Id.* "Circuits may have up to 40 layers" and "[t]hese high-density constructions[] … offer significant savings in size and weight." *Id.* A POSITA considering the teachings of Shugg would have understood that, although Oya only explicitly depicts a few wiring and substrate layers in its multilayer PCB 10, it would have been obvious to implement Oya's PCB 10 with additional wiring and/or substrate layers. A POSITA would have done so to achieve at least the known benefits explicitly discussed in Shugg, including to provide a "high[er]-density construction[]" and to gain "significant savings in size and weight." Shugg, 307. Indeed, adding layers to Oya's multilayer PCB 10 would beneficially yield additional wiring layers that could be used to establish additional electrical connections between electronic components of the PCB 10 (*e.g.,* connections between device 11 and other components mounted on or embedded in the PCB 10) without a significant increase in the footprint of the PCB 10 that would ordinarily otherwise be necessary to accommodate the additional wiring on existing layers.

141. Reducing the size of the PCB would also be beneficial to reduce the length of the wiring on the PCB and between connection endpoints, which a POSITA would have sought to do to reduce electrical resistance through the wiring, minimize power loss due to internal resistance in the wire (which is

proportional to the path length), improve signal integrity, and minimize heat generation. To be sure, the addition of layers to Oya's multilayer PCB as taught in Shugg would have been entirely obvious as it involves the mere application of a known technique (*e.g.,* forming additional layers in a multilayer PCB) to a known device (*e.g.,* Oya's PCB 10) that was ready for improvement to yield merely predictable results (*e.g.,* a multilayer PCB 10 with additional layers beyond those explicitly depicted in Oya's FIG. 7). A POSITA would have reasonably expected success modifying Oya's PCB 10 to include additional layers since multilayer PCBs with more than three or four substrate layers were well known before the '816 Patent and Oya already contemplated that its electronic module should be implemented as a multilayer PCB. *See* Oya, ¶¶[0039], [0066]; Shugg, 307 ("up to 40 layers"); *see also* Oya, ¶[0071] (Oya acknowledging that "obviously many changes and variations are possible" and "[i]t is … to be understood that the present invention may be practiced otherwise than as specifically described herein").

142. The following figure shows a first predictable implementation of Oya's PCB 10 modified in accordance with Shugg's teachings to include an additional substrate layer (labeled as substrate 5') over substrate 6' and an outer

wiring layer 2' formed on the top surface of substrate 5', thereby providing an additional inner wiring layer between substrates 5' and 6':

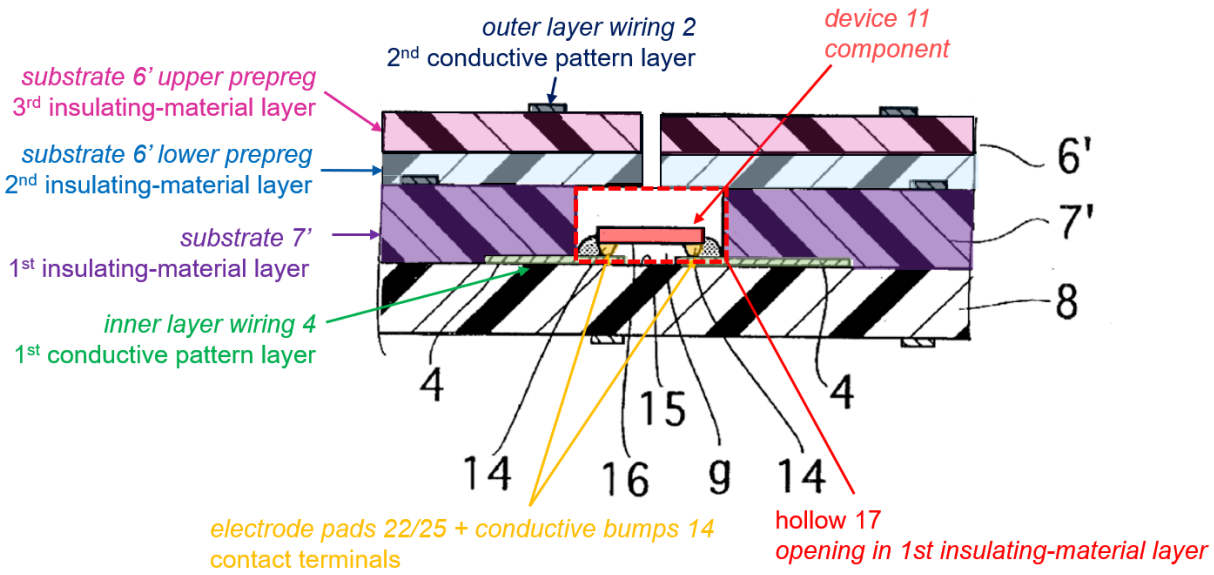


First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

143. As another example, based on Shugg's teaching to provide "two or three bonding layers of prepreg between circuit layers," it would have been obvious to provide not just one but two prepreg substrate layers between the inner wiring layer on substrate 7' and the outer wiring layer on substrate 6' as shown below. Shugg, 307. A POSITA would have sought to substitute Oya's single substrate 6' with two substrate layers to achieve a desired thickness, increase stability and rigidity of the PCB 10, and to increase separation between wiring

layers that can be beneficial to reduce both RF interference and thermal interaction between the wiring layers. The following figure illustrates an alternative implementation of the Oya-Shugg combination according to the modification described here:



Second Alternative Implementation of the Oya-Shugg Combination

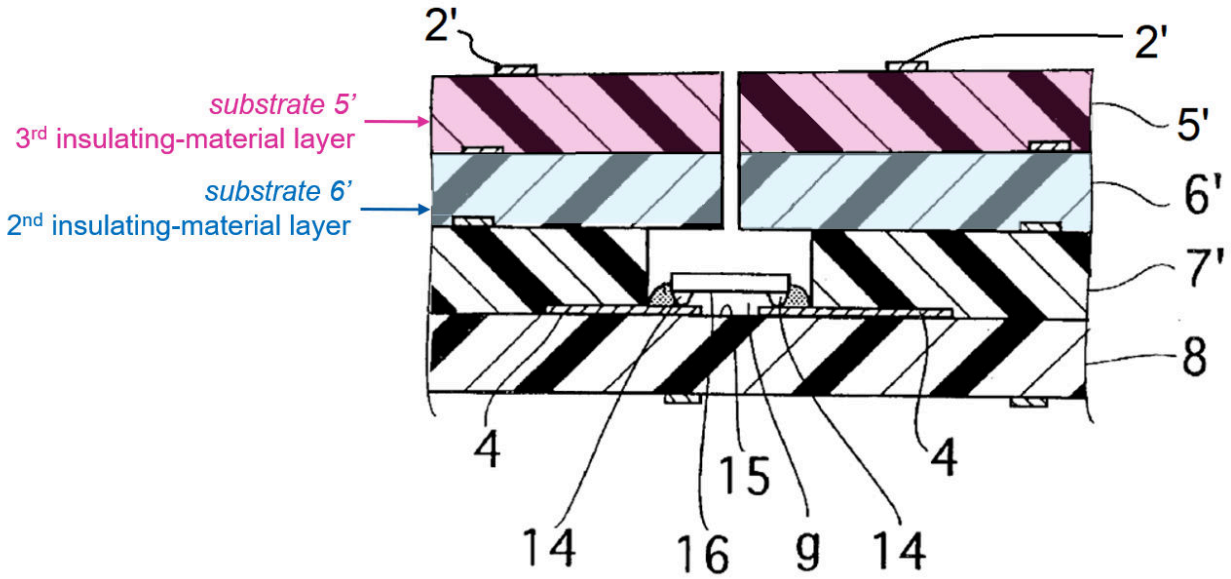
(APPLE-1004, FIG. 7 (modified and annotated))

144. Oya teaches that its substrate layers can be "prepreg" and "composed of an epoxy resin or the like." Oya, ¶¶[0045], [0051]. For each of the reasons described above, it would have been obvious to a POSITA based on Shugg to implement the substrate layers in the Oya-Shugg combination as insulators such that substrate layer 6' in the first alternative implementation and the substrate 6' lower prepreg in the second alternative implementation would each be a "***second***

insulating-material layer" disposed on the substrate layer 7' (***first insulating-material layer***) as claimed. *Supra*, §XII.C; *see also* Oya, ¶¶[0040], [0051]-[0053], [0060], [0067].

[8e] a third insulating-material layer disposed on the second insulating-material layer; and

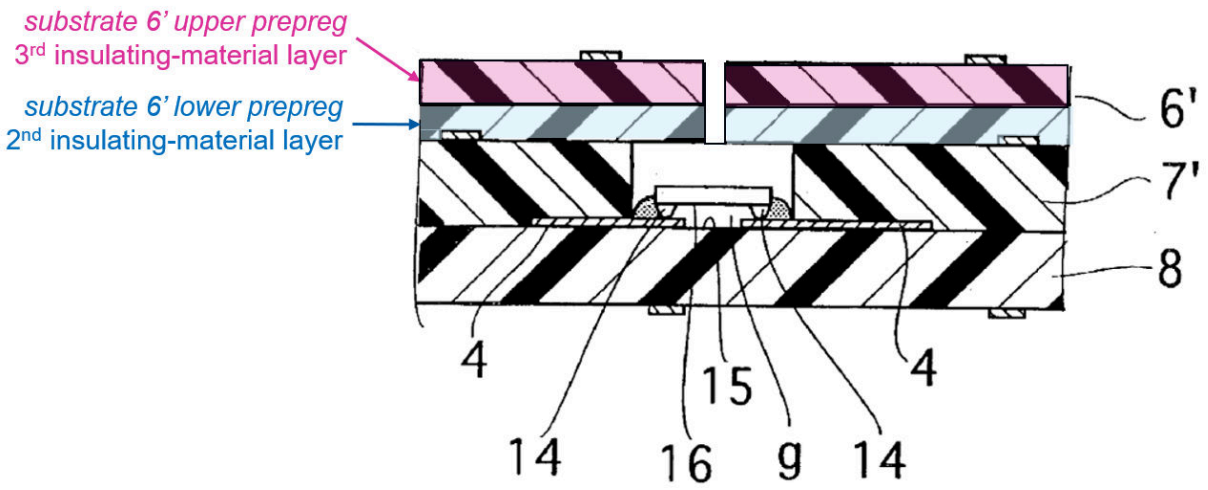
145. The Oya-Shugg combination renders Element [8e] obvious. As described above in connection with Element [8d], it would have been obvious based on Shugg to extend Oya's multilayer PCB 10 to include additional prepreg or other insulating-material layers above substrate 7'. *Supra*, Element [8d]. In the first alternative implementation of the Oya-Shugg combination, substrate 5' (***third insulating-material layer***) is disposed on substrate 6' (***second insulating-material layer***). *Id.*



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

146. Likewise, in the second alternative implementation of the Oya-Shugg combination, substrate 6' upper prepreg (***third insulating-material layer***) is disposed on substrate 6' lower prepreg (***second insulating-material layer***).



Second Alternative Implementation of the Oya-Shugg Combination

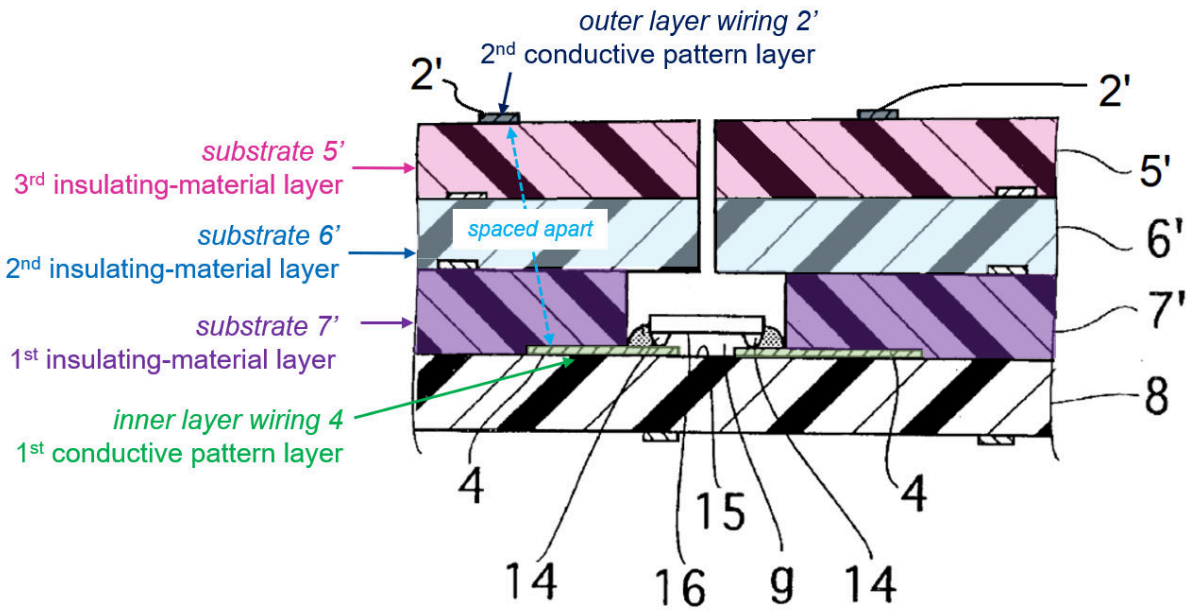
(APPLE-1004, FIG. 7 (modified and annotated))

[8f] a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first, second, and third insulating-material layers,

147. The Oya-Shugg combination renders Element [8f] obvious. For example, Oya discloses an outer layer wiring 2. Oya, ¶[0067], FIG. 7; *see also id.*, ¶¶[0039] ("The wiring board 10 is a multilayer printed circuit board having two outer layer wirings 2 and 3 and two inner layer wirings 4 and 5."). The outer layer wiring 2 is also referred to as a "copper foil pattern 2." Oya, ¶[0055] ("copper foil patterns 2 and 3."), [0051] ("the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7, respectively, and a copper foil is stacked on each of the substrates 6 and 8"). The outer layer wiring 2 is disposed directly on substrate 6'

and is spaced apart from the inner layer wiring 4 by at least the substrate layer 7' and the substrate layer 6'. Oya, FIG. 7; *supra*, Element [1e].

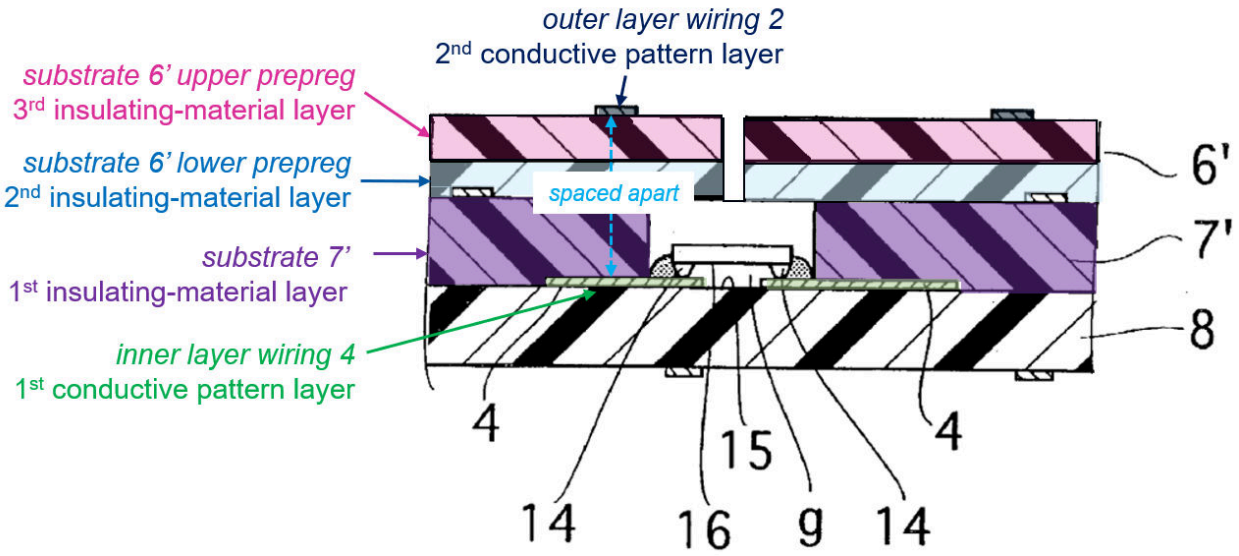
148. Moreover, as described above in connection with Element [8d], it would have been obvious based on Shugg to extend Oya's multilayer PCB 10 to include additional wiring and/or substrate layers. *Supra*, Element [8d]. In the first alternative implementation of the Oya-Shugg combination, an outer wiring layer 2' (***second conductive pattern layer***) is spaced apart from the inner wiring layer 4 (***first conductive pattern layer***) by substrate 7' (***first insulating-material layer***), substrate 6' (***second insulating-material layer***), and substrate 5' (***third insulating-material layer***). *Id.*



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

149. Likewise, in the second alternative implementation of the Oya-Shugg combination, outer wiring layer 2 (***second conductive pattern layer***) is spaced apart from the inner wiring layer 4 (***first conductive pattern layer***) by substrate 7' (***first insulating-material layer***), substrate 6' lower prepreg (***second insulating-material layer***), and substrate 6' upper prepreg (***third insulating-material layer***).



Second Alternative Implementation of the Oya-Shugg Combination

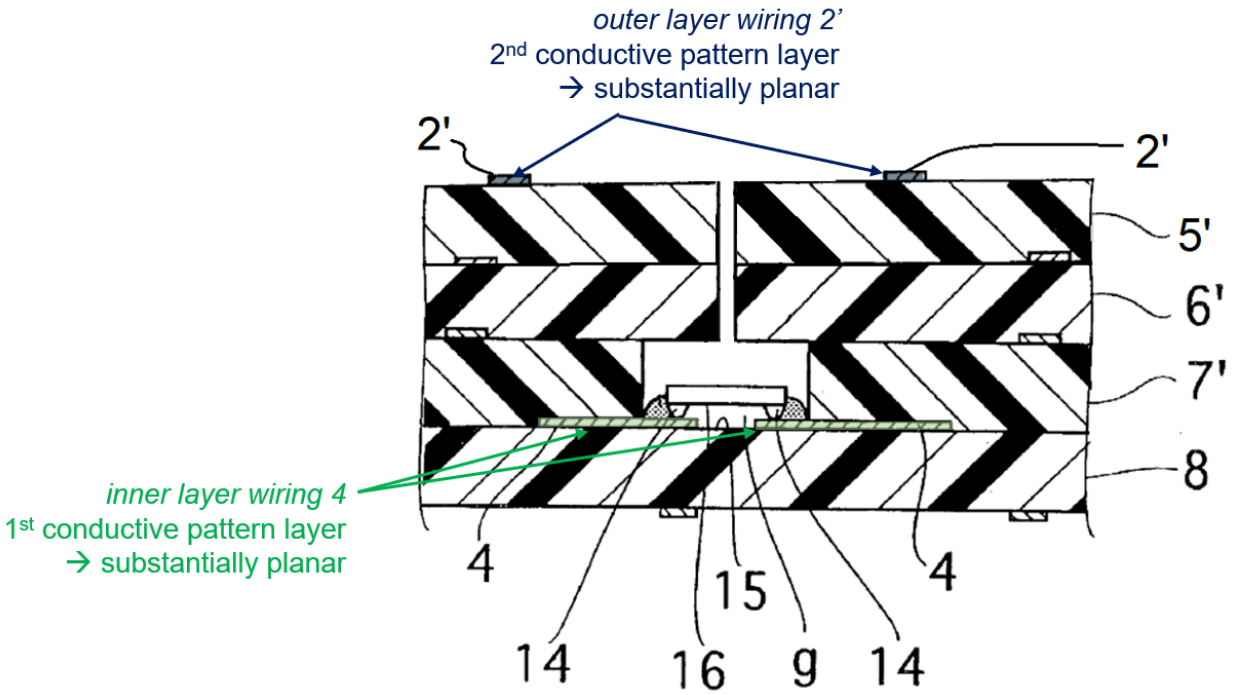
(APPLE-1004, FIG. 7 (modified and annotated))

[8g] wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

150. The Oya-Shugg combination renders Element [8g] obvious. For example, Oya teaches that its wiring layers including inner layer wiring 4 and outer layer wiring 2 are each substantially planar. Oya, ¶¶[0051], [0039], [0054]-[0055], [0066]-[0067]; *see also id.*, FIGS. 1, 7-8. According to Oya, when forming the inner layer wiring 4, a copper foil or a copper plating is disposed directly "on both surfaces of the substrate 7." Oya, ¶[0045]. After a dry film is disposed on the copper foil, a mask having a circuit pattern is thereon disposed. *Id.*, ¶[0046]. Using the dry film as a mask, the copper foil is wet-etched and the wirings 4 and 5 are formed. *Id.*, ¶¶[0046]-[0047]. A POSITA would have understood and it would

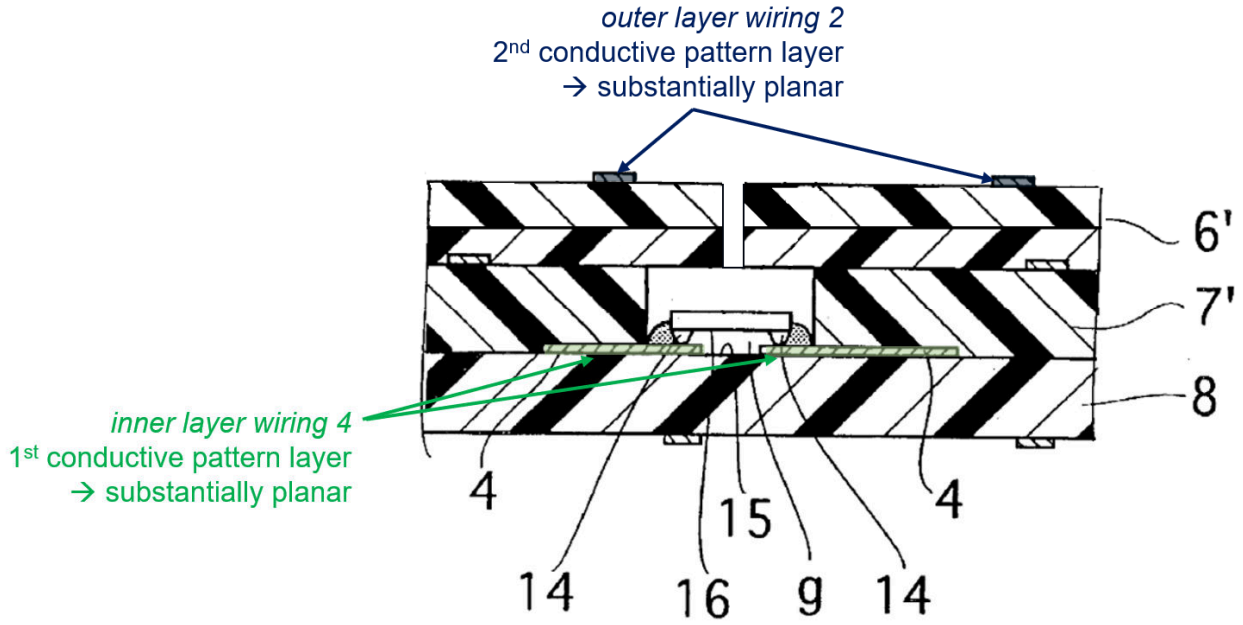
have been obvious from these teachings, including the fact that the inner layer wiring 4 is formed on the surface of a substantially planar substrate 8, that the inner layer wiring 4 is substantially planar.

151. Furthermore, as illustrated in FIG. 7, Oya's outer layer wiring 2 is formed on substrate 6', thereby providing a second conductive pattern layer that is substantially planar. Oya, ¶[0067], FIG. 7, *see also id.*, [0051] ("a copper foil is stacked on each of the substrates 6 and 8"), [0054]-[0055] ("[A]fter sticking a dry film on the copper foil stuck on each of the surfaces of the substrates 6 and 8…. According to this processing, desired copper foil patterns 2 and 3 can be obtained."). Accordingly, a POSITA would have understood and it would have been obvious from Oya's teachings, including the fact that the outer layer wiring 2 is formed on the surface of a substantially planar substrate 6', that the outer layer wiring 2 is also substantially planar, and that the outer layer wiring 2' in the first alternative implementation of the Oya-Shugg combination would be substantially planar.



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



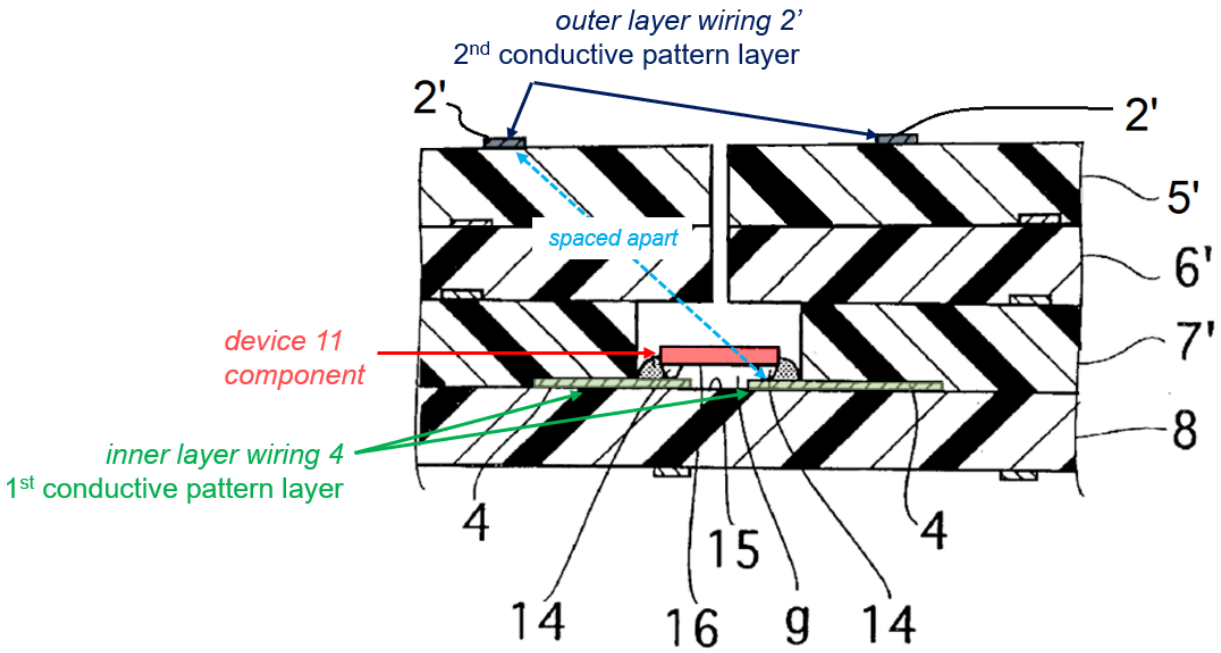
Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

vii. Claim 10

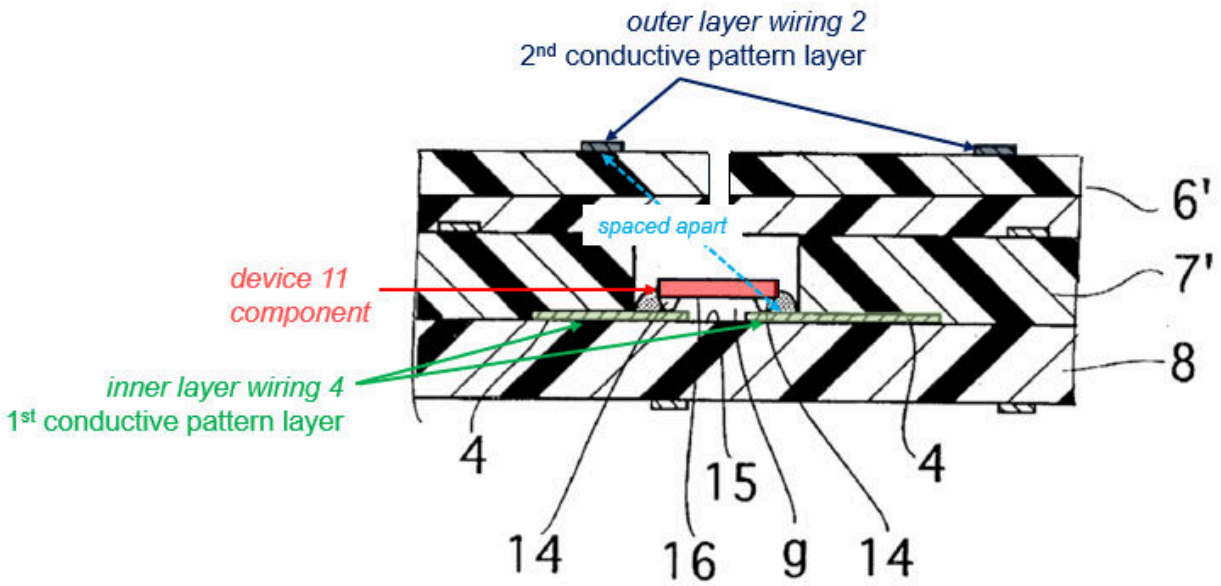
[10] The electronic module of claim 8, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.

152. The Oya-Shugg combination renders Claim [10] obvious. For example, in the combination, Oya discloses that the outer layer wiring 2 or 2' (***second conductive pattern layer***) is spaced apart from the inner layer wiring 4 (***first conductive pattern layer***) by the device 11 (***component***). Oya, FIG. 7; *see also id.*, [0066]-[0067].



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

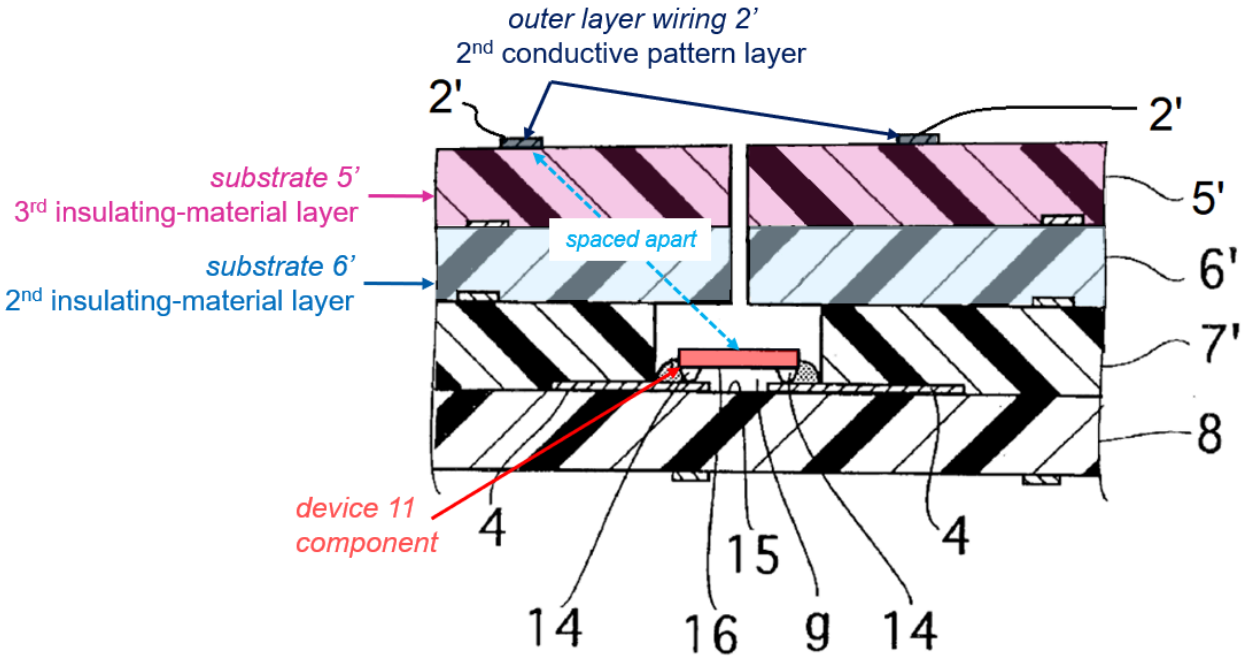
See also id., ¶40 (describing a gap of "several tens of μm" between an inner surface 15 of the hollow 17 and the functional surface 16 of the device 11), [0066]-[0067].

viii. Claim 11

[11] The electronic module of claim 10, wherein the second conductive pattern layer is spaced apart from the component by the second and third insulating-material layers.

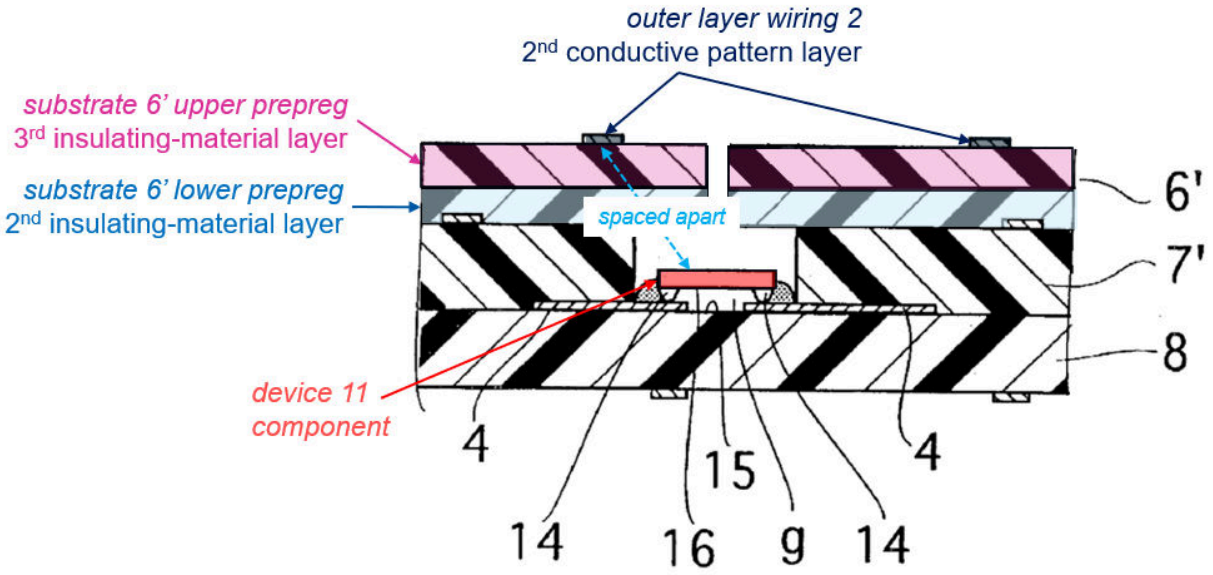
153. The Oya-Shugg combination renders Claim [11] obvious. For example, in the combination, the outer layer wiring 2 or 2' (***second conductive pattern layer***) is disposed on a top surface of the substrate 5' or on a top surface of the substrate 6' upper prepreg (***third insulating-material layer***). Oya, ¶¶[0066]-[0067], FIG. 7; *supra*, Element [8d]. The device 11 (***component***) is disposed within the hollow 17 fashioned inside the substrate 7'. *Id.* The substrate 7' is disposed below the substrate 6'. *Id.* Oya discloses that "the device 11 [is disposed] on the substrate 8." *Id.*, [0067]. The "substrate 7' having a through-hole formed therein may be stacked [on the substrate 8]." *Id*. The "substrate 6' may be stacked further [on the substrate 7] so as to cover the through-hole so as to form the hollow 17." *Id*. In the combination, outer layer wiring 2' (***second conductive pattern layer***) in the first alterative implementation is spaced apart from the device 11 (***component***) by the substrates 5' and 6' (***third and second insulating-material layers***), and outer layer wiring 2 (***second conductive pattern layer***) in the second

alternative implementation is spaced apart from the device 11 (***component***) by the substrate 6' upper and lower prepregs (***third and second insulating-material layers***) in the second alternative implementation. *Id.*.



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

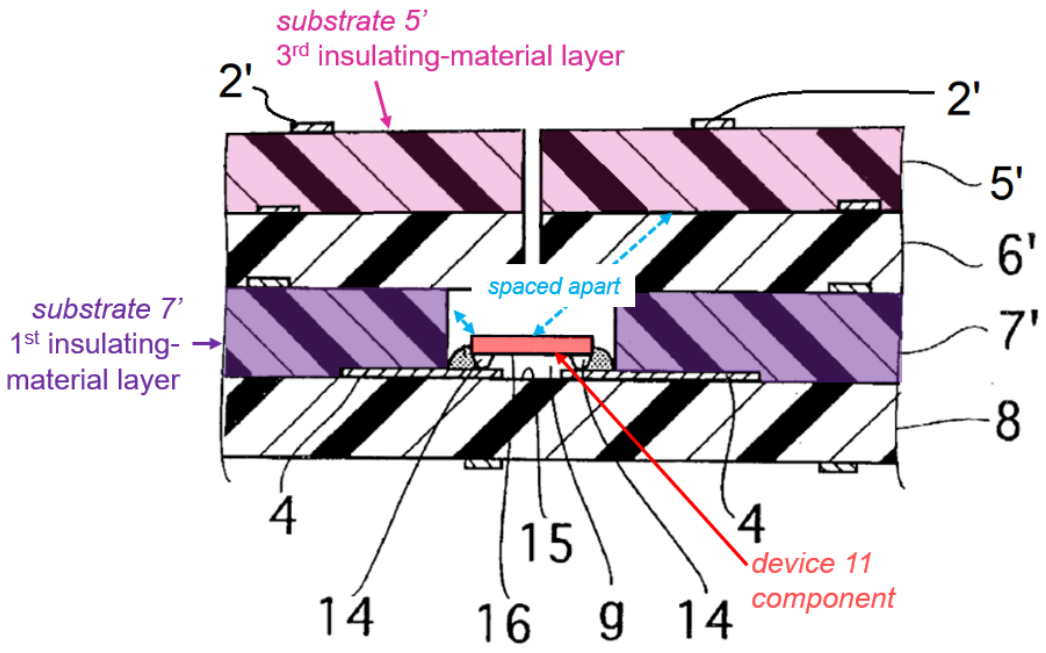
ix. Claim 13

[13] The electronic module of claim 8, wherein the first and third insulating-material layers are spaced apart from the component.

154. The Oya-Shugg combination renders Claim [13] obvious. To start, Oya discloses that the substrate 7' (***first insulating-material layer***) is spaced apart from the device 11 (***component***). *Id.* Oya's device 11 is mounted within a hollow 17 formed by the substrate 6' and the substrate 7'. Oya, ¶¶[0066]-[0067], FIG. 7; *see also id.*, ¶¶52-56. Oya further discloses that "the device 11 faces the wiring board 10 in ***non-contact having the gap g therebetween***, and the other surface of the device 11 faces the wiring board 10 in ***non-contact having the space s***

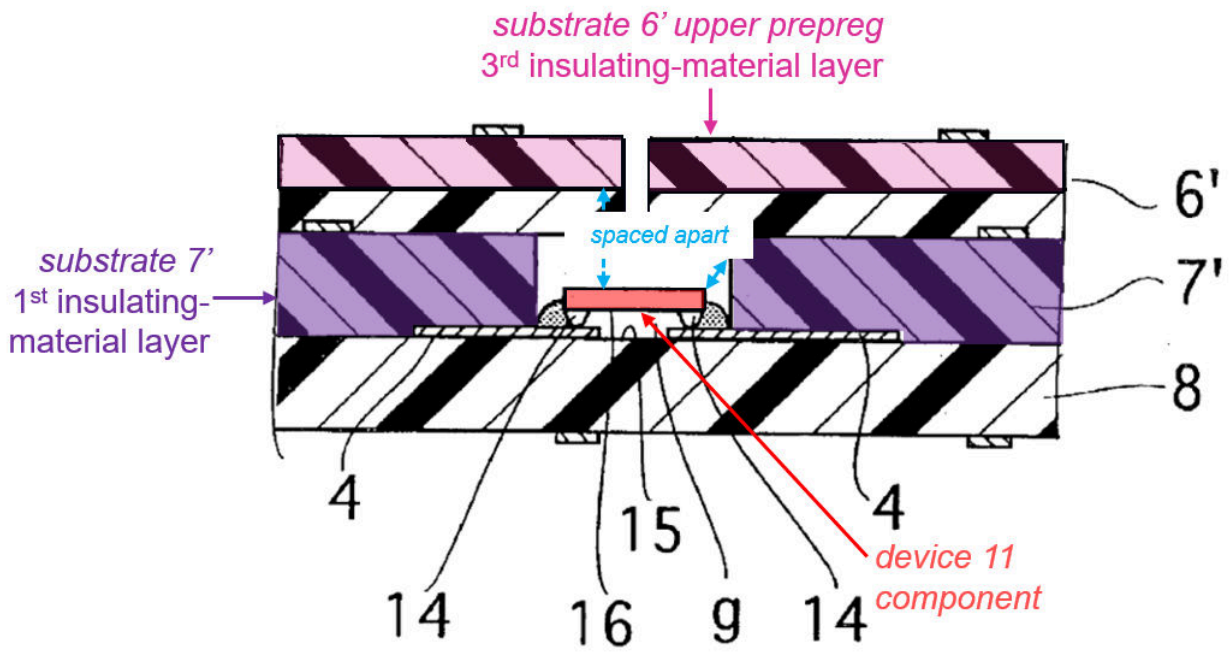
therebetween." *Id.*, ¶57. Accordingly, a POSITA in possession of Oya would have understood from the figures and description that the substrate 7' (***first insulating-material layer***) is spaced apart from the device 11 (***component***) at least by the space s provided between the device 11 and the substrate 7'.

155. Additionally, as described above in connection with Element [8d], it would have been obvious based on Shugg to implement a "***third insulating-material layer***" in Oya's PCB 10 as either substrate 5' in the first alternative implementation of the Oya-Shugg combination or as substrate 6' upper prepreg in the second alternative implementation of the Oya-Shugg combination. *Supra*, Element [8d]. In both implementations, the "***third insulating-material layer***" (*i.e.,* substrate 5' or substrate 6' upper prepreg) is also spaced apart from the device 11 (***component***).



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

x. Claim 14

[14] The electronic module of claim 8, wherein the first and third insulating-material layers comprise a first material, the second insulating-material layer comprises a second material, the first material being different than the second material.

156. The Oya-Shugg combination renders Claim [14] obvious. As discussed above, Oya teaches that the substrates of its wiring board, *e.g.,* substrates 6' and 7', can be "prepreg" and "composed of an epoxy resin or the like." Oya, ¶¶[0045], [0051]. A POSITA would have known that "prepreg" was a composite material commonly used for circuit board substrates made of pre-impregnated fibers mixed with a partially cured resin. Shugg, 289-290 ("The basic materials for

making industrial laminates are called *prepregs*. A prepreg is composed of a substrate, usually paper, cotton, or glass fabric, impregnated with a thermosetting resin, generally phenolic, epoxy, or melamine."), 291 ("Epoxy resin glass-reinforced laminates … are used extensively as substrates for printed circuits."), 303-304; *see also* APPLE-1019, 239 ("[g]lass-fiber cloth pre-impregnated with epoxy-resin [was] … widely used as a composite electrical insulation in various electrical industrial products"). Consistent with the conventional understanding of prepreg, Oya explicitly confirms that the substrates can be "composed of glass fiber impregnated with a resin." Oya, ¶[0060]. In the combination, it would have been obvious for the second and third insulating material layers to be prepreg based on Shugg's teachings as well. *See, e.g.,* 289 ("bonding layers of prepreg between circuit layers"); *supra*, Element [8d]. Because prepreg is a composite material that is itself composed of multiple materials, substrate 7' (***first insulating-material layer***) and the "***third insulating-material layer***" (*e.g.,* substrate 5' in the first alternative implementation of the combination or substrate 6' upper prepreg in the second alternative implementation of the combination) both comprise a first material such as glass fiber that is different than a second material such as resin of the ***second insulating-material layer*** (*e.g.,* substrate 6' in the first alternative

implementation of the combination or substrate 6' lower prepreg in the second alternative implementation of the combination) as claimed.[12]

XIII. ADDITIONAL REMARKS

157. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

---

[12] I understand that the term "comprise[s]" is an open-ended transition word. In the phrases "the first and third insulating-material layers *comprise* a first material and "the second insulating-material layer comprises a second material," claim 14 is clear that the first and third insulating-material layers need only *include* a first material that is different from a second material included in the second insulating-material layer—although the first and third insulating-material layers need not consist only of material that is different from any/all material of the second insulating-material layer. The plain language of claim 14 is met Oya and Shugg's teachings of one material in the first and third insulating-material layers that is different than another material in the second insulating-material layer. *Id.* The specification of the '816 Patent likewise confirms that "the insulating-material layer 1 can equally well be manufactured from more than one part" and "[i]t is then also possible to proceed in such a way that the insulating-material layer 1 is ***formed of more than one insulating material***." APPLE-1001, 12:36-40.

XIV. LISTING OF CLAIMS

Claim 1	
[1pre]	An electronic module, comprising:
[1a]	a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
[1b]	at least one opening in the first insulating-material layer that extends through the first insulating-material layer;
[1c]	a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;
[1d]	a second insulating-material layer disposed on the first insulating-material layer; and
[1e]	a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers,
[1f]	wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.
Claim 2	
[2]	The electronic module of claim 1, wherein the second insulating-material layer directly contacts the component.
Claim 3	
[3]	The electronic module of claim 1, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.
Claim 4	

[4]	The electronic module of claim 3, wherein the second conductive pattern layer is spaced apart from the component by the second insulating-material layer.
Claim 5	
[5]	The electronic module of claim 4, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.
Claim 6	
[6]	The electronic module of claim 1, wherein the first insulating-material layer is spaced apart from the component.
Claim 7	
[7]	The electronic module of claim 1, wherein the first insulating-material layer comprises a different material than a material of the second insulating-material layer.
Claim 8	
[8pre]	An electronic module, comprising:
[8a]	a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
[8b]	an opening in the first insulating-material layer that extends through the first insulating-material layer;
[8c]	a component comprising contact terminals, the component being arranged at least partially within the opening, the contact terminals electrically connected to the first conductive pattern layer;
[8d]	a second insulating-material layer disposed on the first insulating-material layer;
[8e]	a third insulating-material layer disposed on the second insulating-material layer; and

[8f]	a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first, second, and third insulating-material layers,
[8g]	wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.
Claim 9	
[9]	The electronic module of claim 8, wherein the second insulating-material layer directly contacts the component.
Claim 10	
[10]	The electronic module of claim 8, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.
Claim 11	
[11]	The electronic module of claim 10, wherein the second conductive pattern layer is spaced apart from the component by the second and third insulating-material layers.
Claim 12	
[12]	The electronic module of claim 11, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.
Claim 13	
[13]	The electronic module of claim 8, wherein the first and third insulating-material layers are spaced apart from the component.
Claim 14	
[14]	The electronic module of claim 8, wherein the first and third insulating-material layers comprise a first material, the second insulating-material layer comprises a second material, the first material being different than the second material.

APPENDIX A

R. JACOB BAKER, PH.D., P.E.

professor emeritus of electrical and computer engineering

6775 Agave Azul Court
Las Vegas, NV 89120

(208) 850-0517 (Cell)

Email: rjacobbaker@gmail.com
Website: http://CMOSedu.com/jbaker/jbaker.htm

PROFESSIONAL SUMMARY

Russel Jacob Baker (R. Jacob Baker), Ph.D., P.E. (IEEE Student Member 1983, Member 1988, Senior Member 1997, and Fellow 2013) was born in Ogden, Utah, on October 5, 1964. He received the B.S. and M.S. degrees in electrical engineering from the University of Nevada, Las Vegas (UNLV) in 1986 and 1988. He received the Ph.D. degree in electrical engineering from the University of Nevada, Reno (UNR) in 1993. His Google Scholar profile is here and his ResearchGate profile is here.

From 1981-1987 he served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division). From 1985-1993 he worked for E. G. & G. Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapons tests at the Nevada Test Site. During this time he designed, and oversaw the fabrication and the electrical/mechanical manufacture of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame- and bit-syncs for high-speed imaging, data converters, streak-camera sweep circuits, Pockels cell drivers, micro-channel plate gating circuits, and analog oscilloscope electronics. From 1991-1993 he was an adjunct faculty member in the Departments of Electrical Engineering at UNLV and UNR. From 1993-2000 he served on the faculty in the Department of Electrical Engineering at the University of Idaho (UI), first as an untenured assistant professor and then from 1998 as a tenured associate professor. In 2000 he joined a new electrical and computer engineering (ECE) program at Boise State University (BSU) where he was promoted to professor in 2002. He then served as the ECE department chair from 2004-2007. At BSU he helped establish graduate programs in ECE including, in 2006, the university's second PhD degree. In 2012 he rejoined the faculty at UNLV as a tenured full professor of ECE. During his tenure at the UI, BSU, and UNLV he has been the major professor to more than 100 graduate students.

Dr. Baker has done consulting for over 200 companies. His research/development activities are in: photonics, circuit design for wireless and wired communications, analog-to-digital/digital-to-analog data conversion and transmission, optoelectronics (imagers, displays, LIDARs, APDs, SiPMs, and associated electronics), analog and digital integrated circuit design and fabrication, design of diagnostic electrical and electro-optic instrumentation for scientific research, integrated electrical/biological circuits and systems, array (memory, imagers, and displays) fabrication and design, design of digital processors for signal processing, CAD tool development and online tutorials, low-power interconnect and packaging (electrical and optical) techniques, design of wired/wireless communication and interface circuits, circuit design for the use and storage of renewable energy, power electronics and power supply design, and the delivery of online engineering education. As a result of this work, he is the named inventor on over 150 US patents and the author of over 100 publications.

He is a member of the honor societies Eta Kappa Nu and Tau Beta Pi, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the 2000 Best Paper Award from the IEEE Power Electronics Society,

the 2007 Frederick Emmons Terman Award, the 2011 IEEE Circuits and Systems Education Award, and the 2021 Wiley-IEEE Press Textbook Award for the 4th Edition of his book CMOS Circuit Design, Layout, and Simulation.

His service activities include the IEEE Press Editorial Board (1999-2004), editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), Distinguished Lecturer for the SSCS (2012-2015), Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the IEEE Solid-State Circuits Magazine, IEEE Kirchhoff Award Committee (2020-2023), and advisor for the student branch of the IEEE at UNLV (2013-2024).

INDUSTRY EXPERIENCE

2008 - present: Expert witness in intellectual property disputes in electrical, electro-optic, and computer engineering matters for: 1) district court and ITC patent disputes, 2) inter partes reviews at the PTAB, and 3) arbitrations and mediations.

2013 - 2022: Worked with Freedom Photonics, Santa Barbara, CA, on the integration, fabrication and design, of optoelectronics with CMOS integrated circuits. Work includes the design of compact optical transceivers for range finding applications, high-efficiency integrated silicon avalanche photodetectors for quantum key receivers, Geiger mode SiGe receivers for long-range communications, cryptography, and the fabrication of near-infrared focal plane arrays. Packaging and testing of numerous chips fabricated in both CMOS and SiGe technologies using LEDs, ILDs, PIN, APDs, and ROICs.

2017 - 2019: Worked with Vorpal Research Systems, Las Vegas, NV on the design of integrated circuit electronics and optoelectronics for optical transceivers used in LIDARs/LADARs.

2016 - 2019: Worked with Attollo Engineering on the design of transient digitizers for the capture of high-speed signals for range finders using LEDs and lasers in compact optical transceivers.

2013 - 2018: Working with Mission Support and Test Services, LLC (MSTS, formerly National Security Technologies, LLC, [NSTec]) on the Design and Fabrication of Integrated electrical/photonic application specific integrated circuit (ASIC) design for use in the implementation of diagnostic instrumentation.

2013 - 2015: Consultant for OmniVision. Working on integrating CMOS image sensors (CIS) with memory for very high-speed consumer imager products. Design specialty DRAM, high-speed interfaces between CIS and DRAM, packaging techniques to pair the CIS with DRAM.

2010 - 2013: Worked with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2013: Cirque, Inc. Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

2012: Consultant at Lockheed-Martin Santa Barbara Focal Plane Array. CMOS circuit design and fabrication for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, high-speed interfaces between image processors and imaging systems, and infrared imaging systems.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodetectors in standard CMOS.

2009 - 2010: Sun Microsystems, Inc. (and then Oracle) VLSI research group. Provided consulting on memory circuit design/fabrication and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power, 3D packaging, for memory modules and controllers implemented with FPGAs and custom ASICs.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

1994 - 2008: Affiliate faculty (Senior Designer), Micron Technology. Designed CMOS circuits for DRAMs including DLLs, PLLs for embedded processors, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), SRAMs, RFIDs, CMOS active pixel imagers and sensors, power supply design (linear and switching), input buffers, etc. Worked on a joint research project

between Micron and HP labs in magnetic memory fabrication and design using the MTJ memory cell. Worked on numerous technologies ranging from LED lighting to medical imaging using CMOS image sensors (too many to list) resulting in numerous US patents (see following list). Considerable experience working with product engineering to ensure high-yield from the production line from fabrication to test. Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging. Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing.

January 2008: Consultant for Nascentric located in Austin, TX. Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

May 1997 - May 1999: Consultant for Tower Semiconductor, Haifa, Israel. Designed CMOS integrated circuit cells for various modem chips, interfaces, and serial buses including USB circuits, charging circuits based upon power up/down circuits using an MOS or bandgap reference, pre-amplifiers, comparators, etc.

Summer 1998: Consultant for Amkor Wafer Fabrication Services, Micron Technology, and Rendition, Inc., Design PLLs and DLLs for custom ASICs and processors.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television. Worked on the fabrication and design of video peripheral circuits for these displays.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns rise-time and 8 ns fall-time for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

December 1985 - June 1993: (from July 1992 to June 1993 employed as a consultant while finishing up my Ph.D.), E.G.&G. Energy Measurements Inc., Nevada, Senior Electronics Design Engineer. Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing and fabricating over 30 electronic and electro-optic instruments including: CCD camera design, communication networks, fiber optic transmitters employing high speed laser drive electronics, receivers employing envelop tracking for DC voltage restoration and regeneration of received information, receiver low noise amplifier design, frame synchronizers for re-assembling transmitted images, high-speed SRAM memory system design with battery back-up, calibration equipment design such as a tunnel diode pulse generator for testing compensation of oscilloscopes and DAC design for calibrating CCD readout electronics, power supply and battery charger designs, sweep circuits for streak cameras, Pockel's cell drive electronics, vertical amplifier design using HBTs for analog oscilloscopes used at the Nevada Test Site, and 10 kV ramp designs using a planar triode to name some of the designs.

This position provided considerable fundamental grounding in EE with a broad exposure ranging from the design of PC boards to, for example, the design of cable equalizers. Summarizing, gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuit fabrication and design, GaAs (high speed logic and HBTs), Mach-Zehnder interferometers, Pockels cells, krytrons, power MOSFETs, microwave techniques, power supplies, fiber optic transmitters/receivers, etc.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and trouble-shooting electric motors on mining equipment.

ACADEMIC EXPERIENCE

January 1991 – present: Professor of Electrical and Computer Engineering at the **University of Nevada, Las Vegas** from August 2012 to present. From January 2000 to July 2012 held various positions at **Boise State University** including: Professor (2003 – 2012), Department Chair (2004 - 2007), and tenured Associate Professor (2000 - 2003). From August 1993 to January 2000 was a tenured/tenure track faculty member at the **University of Idaho**: Assistant Professor (1993 - 1998) and then tenured Associate Professor (1998 - 2000). Lastly, from January 1991 to May 1993 held adjunct faculty positions in the departments of Electrical Engineering at the University of Nevada, Las Vegas and Reno. Additional details:

- Research is focused on analog and mixed-signal integrated circuit fabrication and design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.) on projects that have been funded by EPA, DARPA, NASA, Army, DMEA, Navy, and the AFRL.
- Current and past research and development interests are:
  - Design and packaging of electrical/optical systems (e.g., LiDARs/LADARs) using LEDs, semiconductor lasers, lens for focusing and directing light, integrated circuits, and associated control and communication systems/circuits.
  - Capacitive sensing techniques using delta-sigma modulation and interfacing to sensors
  - Design of high-voltage and energy switching circuits
  - Circuit design and fabrication for the control, use, and storage of renewable energy using thermoelectric generators
  - Design of electrical/biological/optical circuits and systems using electrowetting on dielectric for automating and controlling biological experiments
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g., FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories, memory modules, and digital systems using custom and non-custom (e.g., FPGAs) implementations
  - Analog and mixed-signal circuit fabrication and design for communication systems, synchronization, energy storage, data conversion, and interfaces
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g., magnetic, chalcogenide)
  - Reconfigurable electronics design and fabrication using nascent memory technologies such as the memristor to implement FPGAs
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Power electronics circuit design for consumers and consumer electronics including power management and adaptive control to reduce power consumption
  - Design of bandpass delta-sigma modulators for IQ demodulation in wireless communication systems in OFDM, WiFi, 802.11, Bluetooth, 3G, 4G, etc.
  - University prototyping, fabricating, and packaging of integrated circuits
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and ABET accreditation visits.
- Worked with established and start-up companies to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI design and fabrication, fiber optics, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

EDUCATION

- Ph.D. in Electrical Engineering; December 1993; University of Nevada, Reno, GPA 4.0/4.0. Dissertation Title: *Applying power MOSFETs to the design of electronic and electro-optic instrumentation.*
- M.S. and B.S. in Electrical Engineering: May 1986 and May 1988; University of Nevada, Las Vegas. Thesis Title: *Three-dimensional simulation of a MOSFET including the effects of gate oxide charge*.

MEMBERSHIPS IN PROFESSIONAL AND SCHOLARLY ORGANIZATIONS

IEEE (student, 1983; member, 1988; senior member, 1997; Fellow, 2013)
Member of the honor societies Eta Kappa Nu and Tau Beta Pi
Licensed Professional Engineer

HONORS AND AWARDS

- Consolidated Students of the University of Nevada, Las Vegas (CSUN) Faculty Award, 2017
- Tau Beta Pi UNLV Outstanding Professor of the Year in 2013, 2014, 2015 and 2016
- UNLV ECE Department Distinguished Professor of the Year in 2015
- IEEE Fellow for contributions to the design of memory circuits - 2013
- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2012 - 2015
- IEEE Circuits and Systems (CAS) Education Award - 2011
- Twice elected to the Administrative Committee of the Solid-State Circuits Society, 2011 - 2016
- Frederick Emmons Terman Award from the American Society of Engineering Education - 2007
- President's Research and Scholarship Award, Boise State University - 2005
- Honored Faculty Member - Boise State University Top Ten Scholar/Alumni Association 2003
- Outstanding Department of Electrical Engineering faculty, Boise State 2001
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99
- University of Idaho, College of Engineering Outstanding Young Faculty award, 1996-97

SERVICE

Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Reviewer for the National Institutes of Health. Technology editor and then Editor-in-Chief for the Solid-State Circuits Magazine.

Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Master's graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

Also currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong University, as a Distinguished Lecturer for the SSCS (2012-2015), as the Technical Program Chair for the IEEE 58th 2015 International Midwest Symposium on Circuits and Systems, MWSCAS 2015, as advisor for the student branch of the IEEE at UNLV (2013-2023), and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for the *IEEE Solid-State Circuits Magazine*, and IEEE Kirchhoff Award Committee (2020-2023).

ARMED FORCES

From 1981 to 1987 served in the United States Marine Corps (from September of 1982 in the Reserves, Fox Company, 2nd Battalion, 23rd Marines, 4th Marine Division), Honorable Discharge. Military Occupational Specialty (MOS) was Machine Gunner (MOS 0331)

TEXTBOOKS AUTHORED

Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Fourth Edition" *Wiley-IEEE Press*, 1234 pages. ISBN 9781119481515 (2019) **Over 50,000 copies of this book in print.** (Third Edition published in 2010, Revised Second Edition published in 2008, and Second Edition Published in 2005)

Baker, R. J., “CMOS Mixed-Signal Circuit Design,” *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 9780471227540 (First Edition published in 2002)

Keeth, B., Baker, R. J., Johnson, B., and Lin, F., “DRAM Circuit Design: Fundamental and High-Speed Topics”, *Wiley-IEEE*, 2008, 201 pages. ISBN: 9780470184752

Keeth, B. and Baker, R. J., “DRAM Circuit Design: A Tutorial”, *Wiley-IEEE*, 2001, 201 pages. ISBN 0780360141

Baker, R. J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 9780780334168

BOOKS, OTHER (edited, chapters, etc.)

Saxena, V. and Baker, R. J., “Analog and Digital VLSI,” chapter in the CRC Handbook on Industrial Electronics, edited by J. D. Irwin and B. D. Wilamowski, *CRC Press*, 2009 second edition.

Baker, R. J., “CMOS Analog Circuit Design,” (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 2000. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)

Baker, R. J., “CMOS Digital Circuit Design,” (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 2000. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Li, H.W., Baker, R. J., and Thelen, D., “CMOS Amplifier Design,” chapter 22 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)

INVITED TALKS AND SEMINARS

Have given over 50 invited talks and seminars at the following locations: AMD (Fort Collins), AMI semiconductor, Arizona State University, Beijing Jiaotong University, Boise State University, Carleton University, Carnegie Mellon, Columbia University, Dublin City University (Ireland), E.G.&G. Energy Measurements, Foveon, the Franklin Institute, Georgia Tech, Gonzaga University, Hong Kong University of Science and Technology, ICSEng Keynote, ICySSS keynote, IEEE Computing and Communication Workshop (CCWC), IEEE Electron Devices Conference (NVMTS), IEEE Workshop on Microelectronics and Electron Devices (WMED), Indian Institute of Science (Bangalore, India), Instituto de Informatica (Brazil), Instituto Tecnológico y de Estudios Superiores de Monterrey (ITESM, Mexico), Iowa State University, Lawrence Livermore National Laboratory, Lehigh University, Lockheed-Martin, Micron Technology, Nascentric, National Semiconductor, Princeton University, Rendition, Saintgits College (Kerala, India), Southern Methodist University, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Temple University, Texas A&M University, Tower Semiconductor (Israel), University of Alabama (Tuscaloosa), University of Arkansas, University of Buenos Aires (Argentina), University of Houston, University of Idaho, University of Illinois (Urbana-Champaign), Université Laval (Québec City, Québec), University of Macau, University of Maryland, Université de Montréal (École Polytechnique de Montréal), Xilinx (Ireland), University of Nevada (Las Vegas), University of Nevada (Reno), University of Toronto, University of Utah, Utah State University, and Yonsei University (Seoul, South Korea).

RESEARCH FUNDING

In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

- Baker, R. J., (2023-2024) "Silicon Germanium (SiGe) Avalanche Photo Diode (APD) Chip," Department of Energy, Mission Support and Test Services (MSTS), LLC, $120,000
- Baker, R. Jacob, (2017-2023) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit," NASA, $29,999 (Phase I), $225,238 (Phase II), and $79,697 (Phase IIE)
- Goldman, J., Menezes, J., and Baker, R. J., (2021-2022) "Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling," UNLV Sports Research & Innovation Initiative. Proof of Concept Grant Program, $50,000
- Baker, R. Jacob, (2019-2021) "Dual-Mode, Extended Near-Infrared, Focal Plane Arrays Fabricated with CMOS Compatible GeSiSn Alloy Materials," DARPA, $149,998
- Baker, R. Jacob, (2018-2020) “Geiger Mode SiGe Receiver for Long-Range Optical Communications,” NASA, $99,996

- Baker, R. Jacob, (2019) "Improved Quantum Efficiency Photo-Detector," Navy, $29,999
- Baker, R. Jacob, (2018-2019) "Tiled Silicon Photomultiplier Array Read-Out Integrated Circuit – Phase I," NASA, $29,999
- Baker, R. Jacob, (2017-2019) "Quantum Cryptography Detector Chip," Defense MicroElectronics Activity (DMEA), $266,029
- Baker, R. Jacob, (2017-2019) "Advanced Printed Circuit Board Design Methods for Compact Optical Transceiver," U.S. Army/DOD, $299,605
- Baker, R. Jacob, (2016-2018) "High-Sensitivity Monolithic Silicon APD and ROIC," U.S. Air Force/DOD, $299,665

DOCTORAL STUDENT SUPERVSION

10. Sachin Namboodiri – A Multi-channel MCP-PMT based Readout Integrated Circuit for LiDAR Applications (2020)
9. Wenlan Wu – High-Speed Radhard Mega-Pixel CIS Camera for High-Energy Physics (2019)
8. Kostas Moutafis – A Highly-Sensitive Global-Shutter CMOS Image Sensor with On-Chip Memory for Hundreds of kilo-frames per second Scientific Experiments (2019)
7. Yiyan Li – Portable High Throughput Digital Microfluidics and On-Chip Bacteria Cultures (2016)
6. Yacouba Moumouni – Designing, Building, and Testing a Solar Thermoelectric Generation, STEG, for Energy Delivery to Remote Residential Areas in Developing Regions (2015)
5. Qawi IbnZayd Harvard – Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design (2011)
4. Vishal Saxena – K-Delta-1-Sigma Modulators for Wideband Analog-to-Digital Conversion (2010)
3. Robert Russell Hay – Digitally-Tunable Surface Acoustic Wave Resonator (2009)
2. Xiangli Li (the first Boise State University College of Engineering PhD graduate) – MOSFET Modulated Dual Conversion Gain CMOS Image Sensors (2008)
1. Feng Lin, Research and Design of Low Jitter, Wide Locking-Range Phase-Locked and Delay-Locked Loops (2000)

MASTERS STUDENT SUPERVISION

91. Jazmine Boloor – Survey of how Irregular Pathways in the Electrical System of the Human Heart Link to Different Heart Arrhythmias (2023)
90. Abraham Lopez – An Avalanche-Transistor-Based Pulse Generator Design For Infrared Laser Applications (2023)
89. David Santiago – Development of an Automated GPIB System for Characterization of SiGe Avalanche Photodiodes (2023)
88. Minsung Cho – Studies of Forward Projection Algorithms and Implementation on PC and FPGA (2023)
87. Armani Alvarez – A Control Integrated Circuit for a Hysteretic Flyback Power Converter (2022)
86. Francisco Mata-carlos – A Wearable Electronic Monitoring Device for Low Pressure Garment Applications and Temperature Analysis for Prevention of Ulceration and Infection (2022)
85. Daniel Senda – Designs and Outcomes of Transcranial Magnetic Stimulation (TMS) and Repetitive Transcranial Magnetic Stimulation (rTMS) Circuits (2021)
84. James Skelly – Monitored Compression Therapy: Using Smart Technology to Optimize the Treatment of Lower Extremity Swelling (2021)
83. Gonzalo Arteaga – Current-mode photon-counting circuit with SiGe BiCMOS input stage (2020)
82. Jason Silic – Design and Fabrication of a 6-bit Current-Mode ADC for Lidar and High-Speed Applications (2020)
81. Brandon Wade (2020)
80. Mario Valles Montenegro – Front-End CMOS Transimpedance Amplifiers on a Silicon Photomultiplier Resistant to Fast Neutron Fluence (2020)
79. Jonathan DeBoy (2018)
78. Dane Gentry – Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process (2018)
77. James Mellot – Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for Processing Fast Signals and Pulses (2018)
76. Eric Monahan – High Speed Fast Transient Digitizer Design and Simulation (2018)
75. Shada Sharif – Design and Analysis of First and Second Order K-Delta-1-Sigma Modulators in Multiple Fabrication Processes (2018)
74. Vikas Vinayaka – Analysis and Design of Analog Front-End Circuitry for Avalanche Photodiodes (APD) and Silicon Photo-Multipliers (SiPM) in Time-of-Flight Applications (2018)

73. Claire Tsagkari – Design, Fabrication and Testing of a Capacitive Sensor Using Delta-Sigma Modulation (2017)
72. Kevin Buck – Fast Transient Digitizer and PCB Interface (2015)
71. Marzieh Sharbat Maleki (2015)
70. Angsuman Roy – Design, Fabrication and Testing of Monolithic Low-Power Passive Sigma-Delta Analog-to-Digital Converters (2015)
69. Daniel Anderson – Design and Implementation of an Instruction Set Architecture and Instruction Execution Unit for the RZ9 Coprocessor System (2014)
68. Jared Gordon – Design and Fabrication of an Infrared Optical Pyrometer ASIC (2013)
67. Justin Butterfield (2012)
66. Adam Johnson – Methods and Considerations for Testing Resistive Memories (2012)
65. Ben Millemon – CMOS Characterization, Modeling, and Circuit Design in the Presence of Random Local Variation (2012)
64. Justin Wood (2012)
63. Chamunda Ndinawe Chamunda (2011)
62. Gary VanAckern – Design Guide for CMOS Process On-Chip 3D Inductors using Thru-Wafer Vias (2011)
61. Lucien Jan Bissey – High-Voltage Programmable Delta-Sigma Modulation Voltage-Control Circuit (2010)
60. Kaijun Li (2010)
59. Yingting Li (co-supervised with Maria Mitkova) (2010)
58. Lael Matthews (co-supervised with Said Ahmed-Zaid) (2010)
57. Priyanka Mukeshbhai Parikh (2010)
56. Todd Plum (co-supervised with Jeff Jessing) – Design and Fabrication of a Chemicapacitive Sensor for the Detection of Volatile Organic Compounds (2010)
55. Rahul Srikonda (2010)
54. Avani Falgun Trivedi (2010)
53. Kuang Ming Yap – Gain and Offset Error Correction for CMOS Image Sensors using Delta-Sigma Modulation (2010)
52. Mahesh Balasubramanian – Phase Change Memory - Array Development and Sensing Circuits using Delta-Sigma Modulation (2009)
51. Lincoln Bollschweiler (2009)
50. Shantanu Gupta (2009)
49. Qawi Harvard – Wide I_O DRAM Architecture Utilizing Proximity Communication (2009)
48. Avinash Rajagiri (2009)
47. Ramya Ramarapu (2009)
46. Harikrishna Rapole (2009)
45. Aruna Vadla (2009)
44. Hemanth Ande (2008)
43. Curtis Cahoon – Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References (2008)
42. Prashanth Busa (2008)
41. John McCoy III (2008)
40. Dennis Montierth – Using Delta-Sigma-Modulation for Sensing in a CMOS Imager (2008)
39. Rudi Rashwand (2008)
38. Barsha Shrestha (co-supervised with Zhu Han) – Wireless Access in Vehicular Environments using Bit Torrent and Bargaining (2008)
37. Eric Becker – Design of an Integrated Half-Cycle Delay Line Duty Cycle Corrector Delay Locked Loop (2007)
36. Matthew Leslie – Noise-Shaping Sense Amplifier for Cross-Point Arrays (2007)
35. Jose Monje (2007)
34. Sanghyun Park (2007)
33. Vishal Saxena – Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers (2007)
32. Meshack Appikatla (2006)
31. Eric Booth – Wide Range, Low Jitter Delay-Locked Loop Using a Graduated Digital Delay Line and Phase Interpolator (2006)

30. Sucheta Das (2006)
29. Krishna Duvvada – High Speed Digital CMOS Input Buffer Design (2006)
28. Krishnamraju Kurra (2006)
27. Soumya Narasimhan (2006)
26. Roger Porter (2006)
25. David Butler – Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes (2005)
24. Dragos Dimitriu (2005)
23. Surendranath Eruvuru – Sensing Circuit Design for an Ion Mobility Spectrometer (2005)
22. Sandhya Sandireddy (2005)
21. Harish Singidi (2005)
20. Indira Vemula – Delta-Sigma Modulator Used in CMOS Imagers (2005)
19. Bhavana Kollimarla – A 1-Bit Analog-to-Digital Converter Using Delta Sigma Modulation for Sensing in CMOS Imagers (2004)
18. Sandeep Pemmaraju – High Voltage Charge Pump Circuit for an Ion Mobility Spectrometer (2004)
17. Ravindra Puthumbaka – Circuit Design for an Ion Mobility Spectrometer (2004)
16. Brandon Roth – Comparison of Asynchronous vs. Synchronous Design Technologies using a 16-bit Binary Adder (2004)
15. Jennifer Taylor – Reading and Writing Flash Memory Using Delta-Sigma Modulation (2004)
14. Jing Plaisted – Methods for Memory Testing (2003)
13. Murugesh Subramaniam – Flash Memory Sensing Using Averaging (2003)
12. Brian Johnson – Application of an Asynchronous FIFO in a DRAM Data Path (2002)
11. Scott Ward – Electrostatic Discharge (ESD) Protection in CMOS (2002)
10. Tyler Gomm – Design of a Delay-Locked Loop with a DAC-Controlled Analog Delay Line (2001)
9. Gexin Huang (2001)
8. Chris Atkins (2000)
7. Thaddeus Black (2000)
6. Zuxu Qin (2000)
5. Hao Chen (1999)
4. Doug Hackler (co-supervised with Steve Parke) – TMOS: A Novel Design for MOSFET Technology (1999)
3. Song Liu – Design of a CMOS 6-bit Folding and Interpolating Analog-to-Digital Converter (1999)
2. Ben Ba (1997)
1. Brent Keeth – A Novel Architecture for Advanced High Density Dynamic Random Access Memories (1996)

GRANTED US PATENTS

152. Baker, R. J., “Quantizing circuits having improved sensing,” **10,658,018**, May 19, 2020.
151. Baker, R. J., “Quantizing circuits having improved sensing,” **10,403,339**, September 3, 2019.
150. Baker, R. J., “Digital Filters with Memory,” **10,366,744**, July 30, 2019.
149. Baker, R. J., “Quantizing circuits having improved sensing,” **10,127,954**, November 13, 2018.
148. Baker, R. J. and Parkinson, W., “NMOS regulated voltage reference,” **9,753,481**, September 5, 2017.
147. Baker, R. J., “Digital Filters with Memory,” **9,734,894**, August 15, 2017.
146. Baker, R. J. and Keeth, B., "Optical interconnect in high-speed memory systems," **9,697,883**, July 7, 2017
145. Baker, R. J., “Comparators for delta-sigma modulators,” **9,641,193**, May 2, 2017.
144. Baker, R. J., “Quantizing circuits having improved sensing,” **9,449,664**, September 20, 2016.
143. Baker, R. J., “Error detection for multi-bit memory,” **9,336,084**, May 10, 2016.
142. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **9,299,423**, March 29, 2016.
141. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **9,299,405**, March 29, 2016.
140. Baker, R. J., “Comparators for delta-sigma modulators,” **9,135,962**, September 15, 2015.
139. Baker, R. J., “Resistive memory element sensing using averaging,” **9,081,042**, July 14, 2015.
138. Baker, R. J., “Digital Filters with Memory,” **9,070,469**, June 30, 2015.
137. Baker, R. J., "Reference current sources,” **8,879,327**, November 4, 2014.
136. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,878,274**, November 4, 2014.
135. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,854,899**, October 7, 2014.

134. Baker, R. J., “Quantizing circuits with variable parameters,” **8,830,105**, September 9, 2014.
133. Baker, R. J., “Integrators for delta-sigma modulators,” **8,754,795**, June 17, 2014.
132. Baker, R. J., “Methods of quantizing signals using variable reference signals,” **8,717,220**, May 6, 2014.
131. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **8,712,249**, April 29, 2014.
130. Baker, R. J., “Resistive memory element sensing using averaging,” **8,711,605**, April 29, 2014.
129. Baker, R. J., “Memory with correlated resistance,” **8,681,557**, March 25, 2014.
128. Baker, R. J., “Reference current sources,” **8,675,413**, March 18, 2014.
127. Baker, R. J., “Methods for sensing memory elements in semiconductor devices,” **8,582,375**, November 12, 2013.
126. Linder, L. F., Renner, D., MacDougal, M., Geske, J., and Baker, R. J., “Dual well read-out integrated circuit (ROIC),” **8,581,168**, November 12, 2013.
125. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **8,516,292**, August 20, 2013.
124. Baker, R. Jacob, “Resistive memory element sensing using averaging,” **8,441,834**, May 14, 2013.
123. Qawi, Q. I., Drost, R. J., and Baker, R. Jacob, "Increased DRAM-array throughput using inactive bitlines," **8,395,947**, March 12, 2013.
122. Baker, R. Jacob, “Memory with correlated resistance,” **8,289,772**, October 16, 2012.
121. Lin, F. and Baker, R. Jacob, “Phase splitter using digital delay locked loops,” **8,218,708**, July 10, 2012.
120. Baker, R. Jacob, “Subtraction circuits and digital-to-analog converters for semiconductor devices,” **8,194,477**, June 5, 2012.
119. Baker, R. J., “Digital Filters for Semiconductor Devices,” **8,149,646**, April 3, 2012.
118. Baker, R. J., “Error detection for multi-bit memory,” **8,117,520**, February 14, 2012.
117. Baker, R. J., “Integrators for delta-sigma modulators,” **8,102,295**, January 24, 2012.
116. Baker, R. J., “Devices including analog-to-digital converters for internal data storage locations,” **8,098,180**, January 17, 2012.
115. Baker, R. J. and Beigel, K. D., “Multi-resistive integrated circuit memory,” **8,093,643**, January 10, 2012.
114. Baker, R. J., “Quantizing circuits with variable parameters,” **8,089,387**, January 3, 2012.
113. Baker, R. J., “Reference current sources,” **8,068,367**, November 29, 2011.
112. Baker, R. J., “Methods of quantizing signals using variable reference signals,” **8,068,046**, November 29, 2011.
111. Baker, R. J., “Systems and devices including memory with built-in self-test and methods of making using the same,” **8,042,012**, October 18, 2011.
110. Baker, R. J., “Memory with correlated resistance,” **7,969,783**, June 28, 2011.
109. Baker, R. J. and Keeth, B., “Optical interconnect in high-speed memory systems,” **7,941,056**, May 10, 2011.
108. Baker, R. J., “K-delta-1-sigma modulator,” **7,916,054**, March 29, 2011.
107. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,877,623**, January 25, 2011.
106. Lin, F. and Baker, R. J., “Phase splitter using digital delay locked loops,” **7,873,131**, January 18, 2011.
105. Hush, G. and Baker, R. J., “Complementary bit PCRAM sense amplifier and method of operation,” **7,869,249**, January 11, 2011.
104. Baker, R. J., “Subtraction circuits and digital-to-analog converters for semiconductor devices,” **7,839,703**, November 23, 2010.
103. Baker, R. J., “Digital Filters with Memory” **7,830,729**, November 9, 2010.
102. Baker, R. J., “Systems and devices including memory with built-in self test and methods of making using the same,” **7,818,638**, October 19, 2010.
101. Baker, R. J., “Integrators for delta-sigma modulators,” **7,817,073**, October 19, 2010.
100. Baker, R. J., “Digital filters for semiconductor devices,” **7,768,868**, August 3, 2010.
99. Baker, R. J., “Quantizing circuits with variable reference signals,” **7,733,262**, June 8, 2010.
98. Baker, R. J., “Quantizing circuits for semiconductor devices,” **7,667,632**, February 23, 2010.
97. Baker, R. J., and Beigel, K. D., “Multi-resistive integrated circuit memory,” **7,642,591**, January 5, 2010.
96. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **7,616,474**, November 10, 2009.
95. Baker, R. J., “Resistive memory element sensing using averaging,” **7,577,044**, Aug. 18, 2009.

94. Baker, R. J., “Quantizing circuits with variable parameters,” **7,538,702**, May 26, 2009.
93. Baker, R. J., “Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors,” **7,528,877**, May 5, 2009.
92. Baker, R. J., “Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors,” **7,515,188**, April 7, 2009.
91. Taylor, J. and Baker, R. J., “Method and apparatus for sensing flash memory using delta-sigma modulation,” **7,495,964**, February 24, 2009.
90. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **7,489,575**, February 10, 2009.
89. Baker, R. J., “Per column one-bit ADC for image sensors,” **7,456,885**, November 25, 2008.
88. Staples, T. and Baker, R. J., “Input buffer design using common-mode feedback,” **7,449,953**, November 11, 2008.
87. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,421,607**, September 2, 2008.
86. Baker, R. J., “Methods for resistive memory element sensing using averaging,” **7,372,717**, May 13, 2008.
85. Taylor, J. and Baker, R. J., “Method and apparatus for sensing flash memory using delta-sigma modulation,” **7,366,021**, April 29, 2008.
84. Hush, G. and Baker, R. J., “Method of operating a complementary bit resistance memory sensor and method of operation,” **7,366,003**, April 29, 2008.
83. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **7,330,390**, February 12, 2008.
82. Baker, R. J., “Input and output buffers having symmetrical operating characteristics and immunity from voltage variations,” **7,319,620**, January 15, 2008.
81. Staples, T. and Baker, R. J., “Method and apparatus providing input buffer design using common-mode feedback,” **7,310,018**, December 18, 2007.
80. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **7,286,428**, October 23, 2007.
79. Baker, R. J., and Cowles, T. B., “Method and apparatus for reducing duty cycle distortion of an output signal,” **7,271,635**, September 18, 2007.
78. Baker, R. J., and Cowles, T. B., “Method and apparatus for reducing duty cycle distortion of an output signal,” **7,268,603**, September 11, 2007.
77. Hush, G., Baker, R. J., and Moore, J., “Skewed sense AMP for variable resistance memory sensing,” **7,251,177**, July 31, 2007.
76. Hush, G. and Baker, R. J., “Method of operating a complementary bit resistance memory sensor,” **7,242,603**, July 10, 2007.
75. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **7,237,136**, June 26, 2007.
74. Moore, J. and Baker, R. J., “Rewrite prevention in a variable resistance memory,” **7,224,632**, May 29, 2007.
73. Baker, R. J., “Integrated charge sensing scheme for resistive memories,” **7,151,698**, December 19, 2006.
72. Baker, R. J., “Adjusting the frequency of an oscillator for use in a resistive sense amp,” **7,151,689**, December 19, 2006.
71. Baker, R. J., “Resistive memory element sensing using averaging,” **7,133,307**, Nov. 7, 2006.
70. Lin, F. and Baker, R. J., “Phase detector for all-digital phase locked and delay locked loops,” **7,123,525**, October 17, 2006.
69. Baker, R. J., and Beigel, K. D., “Integrated circuit memory with offset capacitor,” **7,109,545**, September 19, 2006.
68. Baker, R. J., “Input and output buffers having symmetrical operating characteristics and immunity from voltage variations,” **7,102,932**, September 5, 2006.
67. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **7,095,667**, August 22, 2006.
66. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **7,082,045**, July 25, 2006.
65. Baker, R. J., “System and method for sensing data stored in a resistive memory element using one bit of a digital count,” **7,009,901**, March 7, 2006.
64. Hush, G. and Baker, R. J., “Complementary bit resistance memory sensor and method of operation,” **7,002,833**, February 21, 2006.
63. Lin, F. and Baker, R. J., “Phase detector for all-digital phase locked and delay locked loops,” **6,987,701**, January 17, 2006.

62. Baker, R. J., “Adjusting the frequency of an oscillator for use in a resistive sense amp,” **6,985,375**, January 10, 2006.
61. Baker, R. J., “Method for reducing power consumption when sensing a resistive memory,” **6,954,392**, October 11, 2005.
60. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,954,391**, October 11, 2005.
59. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,954,390**, October 11, 2005.
58. Lin, F. and Baker, R. J., “Phase splitter using digital delay locked loops,” **6,950,487**, September 27, 2005.
57. Baker, R. J., “Method and apparatus for measuring current as in sensing a memory cell,” **6,930,942**, August 16, 2005.
56. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **6,917,534**, July 12, 2005.
55. Baker, R. J., “Dual loop sensing scheme for resistive memory elements,” **6,914,838**, July 5, 2005.
54. Baker, R. J., “High speed low power input buffer,” **6,914,454**, July 5, 2005.
53. Baker, R. J., and Beigel, K. D., “Method for stabilizing or offsetting voltage in an integrated circuit,” **6,913,966**, July 5, 2005.
52. Moore, J. and Baker, R. J., “PCRAM rewrite prevention,” **6,909,656**, June 21, 2005.
51. Baker, R. J., “Integrated charge sensing scheme for resistive memories,” **6,901,020**, May 31, 2005.
50. Hush, G., Baker, R. J., and Moore, J., “Skewed sense AMP for variable resistance memory sensing,” **6,888,771**, May 3, 2005.
49. Baker, R. J., “Method for reducing power consumption when sensing a resistive memory,” **6,885,580**, April 26, 2005.
48. Moore, J. and Baker, R. J., “PCRAM rewrite prevention,” **6,882,578**, April 19, 2005.
47. Baker, R. J., “Integrated charge sensing scheme for resistive memories,” **6,870,784**, March 22, 2005.
46. Baker, R. J., “Sensing method and apparatus for a resistive memory device,” **6,859,383**, February 22, 2005.
45. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,856,564**, February 15, 2005.
44. Baker, R. J., “Offset compensated sensing for a magnetic random access memory,” **6,856,532**, February 15, 2005.
43. Baker, R. J., “Dual loop sensing scheme for resistive memory elements,” **6,829,188**, Dec. 7, 2004.
42. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,826,102**, Nov. 30, 2004.
41. Baker, R. J., “Resistive memory element sensing using averaging,” **6,822,892**, Nov. 23, 2004.
40. Baker, R. J., “System and method for sensing data stored in a resistive memory element using one bit of a digital count,” **6,813,208**, Nov. 2, 2004.
39. Baker, R. J., “Wordline driven method for sensing data in a resistive memory array,” **6,809,981**, Oct. 26, 2004.
38. Baker, R. J., “Noise resistant small signal sensing circuit for a memory device,” **6,798,705**, Sept. 28, 2004.
37. Baker, R. J., “Methods and apparatus for measuring current as in sensing a memory cell,” **6,795,359**, Sept. 21, 2004.
36. Hush, G. and Baker, R. J., “Complementary bit PCRAM sense amplifier and method of operation,” **6,791,859**, Sept. 14, 2004.
35. Baker, R. J., “Method and apparatus for sensing resistance values of memory cells,” **6,785,156**, August 31, 2004.
34. Lin, F. and Baker, R. J., “Phase detector for all-digital phase locked and delay locked loops,” **6,779,126**, August 17, 2004.
33. Baker, R. J., and Lin, F. "Digital dual-loop DLL design using coarse and fine loops," **6,774,690**, August 10, 2004.
32. Hush, G., Baker, R. J., and Voshell, T., “Producing walking one pattern in shift register,” **6,771,249**, August 3, 2004.
31. Baker, R. J., “Sensing method and apparatus for resistance memory device,” **6,741,490**, May 25, 2004.
30. Li, W., Schoenfeld, A., and Baker, R. J., “Method and apparatus for providing symmetrical output data for a double data rate DRAM,” **6,704,881**, March 9, 2004.
29. Baker, R. J., “Method and system for writing data in an MRAM memory device,” **6,687,179**, February 3, 2004.
28. Baker, R. J., “High speed digital signal buffer and method,” **6,683,475**, January 27, 2004.
27. Baker, R. J., “High speed low power input buffer,” **6,600,343**, July 29, 2003.
26. Baker, R. J., “Offset compensated sensing for magnetic random access memory,” **6,597,600**, July 22, 2003.
25. Baker, R. J., “Sensing method and apparatus for resistive memory device,” **6,577,525**, June 10, 2003.
24. Baker, R. J., “Method and apparatus for sensing resistance values of memory cells,” **6,567,297**, May 20, 2003.

23. Baker, R. J., “High-speed digital signal buffer and method,” **6,538,473**, March 25, 2003.
22. Baker, R. J. and Beigel, K. D., "Electronic device with interleaved portions for use in integrated circuits," **6,509,245**, January 21, 2003.
21. Baker, R. J., "Resistive memory element sensing using averaging," **6,504,750**, January 7, 2003.
20. Baker, R. J., "High-speed digital signal buffer and method," **6,483,347**, November 19, 2002.
19. Baker, R. J., and Lin, F., "Digital dual-loop DLL design using coarse and fine loops," **6,445,231**, September 3, 2002.
18. Baker, R. J., "Method and apparatus for receiving synchronous data," **6,424,684**, July 23, 2002.
17. Baker, R. J. and Beigel, K. D., "Comb-shaped capacitor for use in integrated circuits," **6,410,955**, June 25, 2002.
16. Baker, R. J., "High-speed, low-power input buffer," **6,407,588**, June 18, 2002.
15. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,316,976**, Nov. 13, 2001.
14. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,256,234**, July 3, 2001.
13. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,104,209**, August 15, 2000.
12. Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "Method and apparatus for improving the performance of digital delay locked loop circuits," **6,069,506**, May 30, 2000.
11. Keeth, B. and Baker, R. J., "Low skew differential receiver with disable feature," **6,026,051**, February 15, 2000.
10. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **6,026,050**, February 15, 2000.
9. Baker, R. J., and Manning, T. A., "Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same," **5,953,284**, September 14, 1999.
8. Baker, R. J., "Fully-differential amplifier," **5,953,276**, September 14, 1999.
7. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array". **5,909,201**, June 1, 1999.
6. Hush, G. and Baker, R. J., "Field emission display having pulsed capacitance current control," **5,894,293**, April 13, 1999.
5. Baker, R. J., "Adaptively biased voltage regulator and operating method," **5,874,830**, February 23, 1999.
4. Hush, G. Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a Phase-Locked Loop," **5,818,365**, October 1, 1998.
3. Hush, G., Baker, R. J., and Voshell, T., "Timing Control for a Matrixed Scanned Array," **5,638,085**, June 10, 1997.
2. Wilson, A. J., Baker, R. J., and Schoenfeld, A., "Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device," **5,614,856**, March 25, 1997.
1. Hush, G., Baker, R. J., and Voshell, T., "Serial to Parallel Conversion with a PLL," **5,598,156**, January 28, 1997.

INVITED TALKS (PARTIAL LISTING)

- Harvard, Q. I. and Baker, R. J., “Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design,” a presentation covering semiconductor packaging, DRAM architectures, and I/O circuits. The goal of this work is to investigate replacing the currently used dual in-line memory modules (DIMMs) with a smaller and a lower power memory module, a “Nano-Module.”
- Baker, R. J., and Campbell, K. A., “Reconfigurable Analog Electronics using the Memristor.”
- Baker, R. J., and Saxena, V., “A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion.”
- Li, K., Saxena, V., and Baker, R. J., "The Baker ADC: An Overview,"
- Saxena, V., and Baker, R. J., "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs,"
- Baker, R. J., "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive."
- Baker, R. J., Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
- Baker, R. J., "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
- Baker, R. J. and Saxena, V., "Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes."
- Baker, R. J., "Sensing Circuits for Resistive Memory."
- Hadrick, M. and Baker, R. J., "Sensing in CMOS Imagers using Delta-Sigma Modulation."

- Baker, R. J., "Design of High-Speed CMOS Op-Amps for Signal Processing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2005
- Baker, R. J., "Delta-Sigma Modulation for Sensing," IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), April, 2004
- Rivera, B. and Baker, R. J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," MURI Review, November, 2001.

REFEREED JOURNAL PAPERS

26. Lopez, A., Strong, H. N., McGlothen, K. I., Hines, D. J., and Baker, R. J., "A compact avalanche-transistor based pulse generator for transcranial infrared light stimulation (TILS) experiments," *Instruments*, 2022, 6, 20.
25. Senda, D., Strong, H., Hines, D., Hines, R., and Baker, R. J., "A Compact 1200V, 700A, IGBT-Based Pulse Generator for Repetitive Transcranial Magnetic Stimulation In Vivo Laboratory Experiments," *Review of Scientific Instruments*, Vol. 92, Issue 8, August 30, 2021.
24. Wu, W., Baker, R. J., Bikkina, P., Long, Y., Levy, A., and Mikkola, E., "Design and Analysis of a Feedback Time Difference Amplifier with Linear and Programmable Gain," Analog Integrated Circuits and Signal Processing, *Springer*, 16 October, 2017.
23. Moumouni, Y. and Baker, R. J., "Modeling, Simulation, and Implementation of a Solar Thermoelectric Energy Harvesting System," *Journal of Energy and Power Engineering*, vol. 10, pp. 296-312, 2016.
22. Li, Y., Baker, R. J., and Raad, D., "Improving the Performance of Electrowetting on Dielectric Microfludics Using Piezoelectric Top Plate Control," *Sensors and Actuators B: Chemical*, vol. 229, pp. 63-74, 2016.
21. Li, Y., Li, H., and Baker, R. J., "A Low-Cost and High-Resolution Droplet Position Detector for an Intelligent Electrowetting on Dielectric Device," *Journal of Laboratory Automation*, Vol. 20, No. 6, pp. 663-669, 2015.
20. Moumouni, Y., Ahmad, S., and Baker, R. J., "A System Dynamics Model for Energy Planning in Niger," *International Journal of Power and Energy Engineering*, Vol. 3, No. 6, pp. 308-322, 2014.
19. Estrada, D., Ogas, M. L., Southwick III, R. G., Price, P. M., Baker, R. J., and Knowlton, W. B., *Impact of Single pMOSFET Dielectric Degradation on NAND Circuit Performance*, Microelectronics Reliability, Vol. 48, No. 3, pp 354-363, 2008.
18. Leslie, M. B., and Baker, R. J., "Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays," *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 3, pp. 699-704, 2006.
17. Hess, H. L., and Baker, R. J., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices," *IEEE Transactions on Power Electronics,* Vol. 15, No. 5, pp. 923-930, 2000.
16. Lin, F., Miller, J., Schoenfeld, A., Ma, M., and Baker, R. J., "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 4, pp. 565-568, 1999.
15. Bruce, J. D., Li, H. W., Dallabetta, M. J., and Baker, R. J., "Analog layout using ALAS!" *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 2, pp. 271-274, 1996.
14. Li, H. W., Dallabetta, M. J., and Baker, R. J., "An interactive impulse response extraction system," *Review of Scientific Instruments* 66(10), 5092-5095, 1995.
13. Ward, S. T., Baker, R. J., and Li, H. W., "A microchannel plate image intensifier gating circuit capable of pulse widths from 30 ns to 10 us," *Measurement Science and Technology*, Vol. 6, No. 11, pp. 1631-1633, 1995.
12. Keeth, B., Baker, R. J., and Li., H. W., "CMOS transconductor VCO with adjustable operating and center frequencies," *Electronics Letters,* 31(17), 1397-98, 1995.
11. Baker, R. J., "Time domain operation of the TRAPATT diode for picosecond-kilovolt pulse generation," *Review of Scientific Instruments,* 65(10), 3286-88, 1994.
10. Baker, R. J. and Ward, S. T., "Designing nanosecond high voltage pulse generators using power MOSFETs," *Electronics Letters,* 30(20), 1634-35, 1994.
9. Baker, R. J. and Johnson, B. P., "Sweep circuit design for a picosecond streak camera," *Measurement Science and Technology,* 5(4). 1994.
8. Baker R. J., Hodder, D. J., Johnson, B. P., Subedi, P. C., and Williams, D. C., "Generation of kilovolt-subnanosecond pulses using a nonlinear transmission line" *Measurement Science and Technology,* 4(8), 893-95, 1993.
7. Baker R. J., and Johnson, B. P., "Series operation of power MOSFETs for high speed, high voltage switching applications," *Review of Scientific Instruments* 65(6), 1993.

6. Baker R. J., and Johnson, B. P., "Applying the Marx bank circuit configuration to power MOSFETs," *Electronics Letters* 29(1), 56-57. 1993.
5. Baker R. J., and Johnson, B. P., "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments,* 63(12), 5799-5801, 1992.
4. Baker R. J., and Johnson, B. P., "A 500 Volt nanosecond pulse generator using cascode connected power MOSFETs," *Measurement Science and Technology,* 3(8), 775-77, 1992.
3. Baker R. J., Perryman, G. T., and Watts, P. W., "A fiber-optically triggered avalanche transistor," *IEEE Transactions on Instrumentation and Measurement,* 40(3), 649-52, 1991.
2. Baker R. J., "High voltage pulse generation using current mode second breakdown in a bipolar junction transistor," *Review of Scientific Instruments,* 62(4), 1031-1036, 1991.
1. Baker R. J., and Pocha, M. D. "Nanosecond switching using power MOSFETs," *Review of Scientific Instruments* 61(8), 2211-2213, 1990.

REFERRED CONFERENCE PAPERS AND MAGAZINE ARTICLES

85. Strong, H., Senda, D., Baker, R. J., and Hines, D., "Focal Stimulation of Movement Related Cortical Potentials in Mice using a Novel TMS Circuit Design," *Brain Stimulation*, Vol. 14, Issue 6, November, 2021.
84. Arteaga, G., Namboodiri, S. P., Roy, A., and Baker, R. J., "Current Comparator with SiGe BiCMOS Input Stage for Photon-Counting LiDAR Applications," *IEEE 64th International Midwest Symposium on Circuits and Systems*, August 9-11, pp. 420-423, 2021.
83. Namboodiri, S. P. and Baker, R. J., "Incorporation of Chopping in Continuous Time K-Delta-1-Sigma Modulator," IEEE 19th IEEE Interregional NEWCAS Conference, June 13-16, 2021.
82. Namboodiri, S. P., Arteaga, G., Skelly, J., Mata-carlos, F., Roy, A., and Baker, R. J., "A Current-Mode Photon Counting Circuit for Long-Range LiDAR Applications," *IEEE 63rd International Midwest Symposium on Circuits and Systems*, August 9-12, pp. 146-149, 2020.
81. Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Segmented Digital SiPM," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 1118-1121, 2019.
80. Mellott, J. K., Monahan, E., Vinayaka, V., Namboodiri, S. P., Roy, A., and Baker, R. J., "Variable Fast Transient Digitizer," *IEEE 62nd International Midwest Symposium on Circuits and Systems*, August 4-7, pp. 125-128, 2019.
79. Vinayaka, V., Namboodiri, S. P., Abdalla, Kerstetter, B., Mata-Carlos, F., Senda, D., Skelly, J., Roy, A., and Baker, R. J., "Monolithic 8x8 SiPM with 4-bit Current-Mode Flash ADC with Tunable Dynamic Range," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 57-62, Tysons Corner, VA, May 9-11, 2019.
78. Woodson, M., Estrella, S., Hay, K., Roy, A., Sun, K., Morgan, J., Beling, A., Baker, R. J., Renner, D., and Mashanovitch, M., "Photodetection at or below 1 micron wavelengths," *Proc. SPIE 10912, Physics and Simulation of Optoelectronic Devices XXVII*, 1091210, March 8, 2019.
77. Buck, K. and Baker, R. J., "Fast Transient Digitizer Chip for Capturing Single-Shot Events," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
76. Wu, W., Baker, R. J., Kumar, P., Garcia, F., and Mikkola, E., "A Linear High Gain Time Difference Amplifier Using Feedback Gain Control," *Proceedings of 12th IEEE Dallas Circuits and Systems Conference*, October 9-10, 2016.
75. Moumouni, Y. and Baker, R. J., "Analysis of a Residential 5kW Grid-tied Photovoltaic System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.
74. Moumouni, Y. and Baker, R. J., "LTspice Model of a Solar Thermoelectric Generation System," *Proceedings of the 2016 Clemson University Power Systems Conference*, March 8-11, 2016.
73. Li, Y. and Baker, R. J., "Computer Vision Assisted Measurement of the Displacements of a Bimorph Piezoelectric Cantilever Beam," Proceedings of the IEEE Biomedical Circuits and Systems (BioCAS 2015) Conference, October 22-24, 2015.
72. Li, Y. and Baker, R. J., "A Highly Efficient and Reliable Electrowetting on Dielectric Device for Point-of-Care Diagnostics," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
71. Roy, A. and Baker, R. J., "A Low-Power Switched-Capacitor Passive Sigma-Delta Modulator," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.
70. Li, Y. and Baker, R. J., "Precise EWOD Top Plate Positioning Using Inverse Preisach Model Based Hysteresis Compensation," *Proceedings of 11th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2015.

69. Moumouni, Y. and Baker, R. J., "Buffer Sizing of Concentrated Photovoltaic Batteries: An Economic Analysis," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 704-707, August 2-5, 2015.
68. Moumouni, Y. and Baker, R. J., "Application of Used Electric Vehicle Batteries to Buffer Photovoltaic Output Transients," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 700-703, August 2-5, 2015.
67. Roy, A., Meza, M., Yurgelon, J., and Baker, R. J., "An FPGA Based Passive K-Delta-1-Sigma Modulator," *IEEE 58th Midwest Symposium on Circuits and Systems*, pp. 121-124, August 2-5, 2015.
66. Moumouni, Y. and Baker, R. J., "Concise Thermal to Electrical Parameters Extraction of Thermoelectric Generator for Spice Modeling," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 596-599, August 2-5, 2015.
65. Moumouni, Y. and Baker, R. J., "Improved SPICE Modeling and Analysis of a Thermoelectric Module," *IEEE 58th International Midwest Symposium on Circuits and Systems*, pp. 600-603, August 2-5, 2015.
64. Li, Y., Li, H., and Baker, R. J., "Volume and Concentration Identification by Using an Electrowetting on Dielectric Device," *Proceedings of 10th IEEE Dallas Circuits and Systems Conference*, October 12-13, 2014.
63. Li, Y., Chen, R., and Baker, R. J., "A Fast Fabricating Electro-wetting Platform to Implement Large Droplet Manipulation," *Proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 326-329, August 3-6, 2014.
62. Roy, A. and Baker, R. J., "A Passive 2nd-Order Sigma-Delta Modulator for Low-Power Analog-to-Digital Conversion," *Proceedings of the IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 595-598, August 3-6, 2014.
61. Baker, R. J., "Massive Open Online Courses for Educating Circuit Designers: What Works and What Doesn't," IEEE Solid-State Circuits Magazine, Vol. 6, No. 2, pp. 63-65, 2014.
60. Montierth, D., Strand, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process," *IEEE 55th International Midwest Symposium on Circuits and Systems*, August 5-8, 2012.
59. VanAckern, G., Baker, R. J., Moll, A. J., and Saxena, V. "On-Chip 3D Inductors using Thru-Wafer Vias," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
58. Yap, K. and Baker, R. J., "Two Techniques to Reduce Gain and Offset Errors in CMOS Image Sensors using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.
57. Labaziewicz, A. and Baker, R. J., "A 2 GHz Effective Sampling Frequency K-Delta-1-Sigma Analog-to-Digital Converter," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**
56. Saxena, V., Balagopal, S., and Baker, R. J., "Systematic Design of Three-Stage Op-amps using Split Length Compensation," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**
55. Harvard, Q. and Baker, R. J., "A Scalable I/O Architecture for Wide I/O DRAM," *Proceedings of the IEEE 54th International Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**
54. Wald, S., Baker, R. J., Mitkova, M., and Rafla, N., "A Non-Volatile Memory Array Based on Nano-Ionic Conductive Bridge Measurements," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 43-46, April 22, 2011.
53. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," *Proceedings of the IEEE 53rd International Midwest Symposium on Circuits and Systems*, August 1-4, 2010**.**
52. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage Fully-Differential Op-Amps," (invited) *Proceedings of the IEEE 53rd International Midwest Symposium on Circuits and Systems*, August 1-4, 2010**.**
51. Harvard, Q., Baker, R. J., and Drost, R., "Main Memory with Proximity Communication: A Wide I/O DRAM Architecture," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 40-43, April 16, 2010.

50. Yap, K. M. and Baker, R. J., "Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 52-55, April 16, 2010.
49. Gagliano, C. and Baker, R. J., "A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation," *Proceedings* (poster) *of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 16, 2010.
48. Montierth, D., Yap, K. M., and Baker, R. J., "CMOS Image Sensor using Delta-Sigma Modulation," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
47. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
46. Li, K., Saxena, V., Zheng, G., and Baker, R. J., "Full Feed-Forward K-Delta-1-Sigma Modulator," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
45. Bollschweiler, L., English, A., Baker, R. J., Kuang, W., Chang, Z.-C., Shih, M.-H., Knowlton, W.B., Hughes, W.L., Lee, J., Yurke, B., Cockerham, N. S., and Tyree, V. C., "Chip-Scale Nanophotonic Chemical and Biological Sensors using CMOS Process," *Proceedings of the IEEE 52nd Midwest Symposium on Circuits and Systems*, pp. 413-416, August 2-5, 2009**.**
44. Saxena, V., Li, K., Zheng, G., and Baker, R. J., "A K-Delta 1-Sigma Modulator for Wideband Analog to Digital Conversion," *Proceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009**.**
43. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," *Proceedings of the IEEE 52nd International Midwest Symposium on Circuits and Systems*, pp. 9-12, August 2-5, 2009**.**
42. Regner, J., Balasubramanian, M., Cook, B., Li, Y., Kassayebetre, H., Sharma, A., Baker, R. J., and Campbell, K. A., "Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 28-31, April, 2009.
41. Gupta, S. Saxena, V., Campbell, K. A., and Baker, R. J., "W-2W Current Steering DAC for Programming Phase Change Memory," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 59-62, April, 2009.
40. Rapole, H., Rajagiri, A., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "Resistive Memory Sensing Using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 63-66, April, 2009.
39. Kassayebetre, H., Regner, J., Rajagiri, A., Sharma, A., Hay, R. R., Baker, R. J., and Campbell, K.A., "Surface Acoustic Wave Device Fabrication using Zinc Oxide and Chalcogenide Thin Films**,"** poster presentation at the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2009.
38. Ande, H. K., Busa, P., Balasubramanian, M., Campbell, K. A., and Baker, R. J., "A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory," *Proceedings of the IEEE 51st International Midwest Symposium on Circuits and Systems*, pp. 570-573, August 10-13, 2008**.**
36. Saxena, V., and Baker, R. J., "Compensation of CMOS Op-Amps using Split-Length Transistors," *Proceedings of the IEEE 51st Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008**.**
36. Saxena, V., and Baker, R. J., "Indirect Compensation Technique for Low-Voltage Op-Amps," *Proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008**.**
35. Cahoon, C., and Baker, R. J., "Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 16-19, April, 2008.
34. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Hendricks, K., Southwick III, R. G., Henderson, J., Oxford, J., Moll, A., Kuang, W., and Baker, R. J., "Progress Towards a Biomolecular Nanowire Sensor Array for Biomedical Applications," invited talk presented at the 6th Annual INBRE/COBRE Research Conference, Moscow, ID, August 6, 2007
33. Knowlton, W. B., Araujo, D., Price, P.M., Brotherton, J., Coonse, K., Southwick III, R.G., Oxford, J., Moll, A., Baker, R. J., and Kuang, W., "Development of Biomolecular Nanostructure Sensor Arrays," presented at the Sensors

and Sensor Technology session for the program of the 88th annual meeting of the AAAS, Pacific Division, June 2007, Boise, ID

32. Knowlton, W. B., Kuang, W., Araujo D., Price, P. M., Brotherton, J., Coonse, K. Bollschweiler, L., Southwick, R., Oxford, J. Moll, A., and Baker, R. J., "Nanofabrication of 3D Sensor Arrays for Detection," Advanced Fuel Cycle Workshop, May 8-9, 2007, Boise, ID
31. Loo, S. M., Cole, J., Youngberg, R., Baker, R. J., Gribb, M. M., "Field-programmable gate array in a miniature ion mobility spectrometer sensor system," *Proceedings of the 2006 International Conference on Embedded Systems & Applications*, June 26-29, 2006, Las Vegas, NV.
30. Saxena, V., and Baker, R. J., "Indirect Feedback Compensation of CMOS Op-Amps," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 3-4, April, 2006.
29. Duvvada, K., Saxena, V., and Baker, R. J., High Speed Digital Input Buffer Circuits, *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 11-12, April, 2006.
28. Saxena, V., Plum, T. J., Jessing, J. R., and Baker, R. J., "Design and Fabrication of a MEMS Capacitive Chemical Sensor System," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 17-18, April, 2006.
27. Gorseth, T. L., Estrada, D., Kiepert, J., Ogas, M. L., Cheek, B. J., Price, P. M., Baker, R. J., Bersuker, G., and Knowlton, W.B., "Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation," presented at the *Workshop on Microelectronic Devices* (Boise, Idaho; April 14, 2006)
26. Sevier, D., Gribb, M., Plumlee, D., Moll, A. J., Hill, H. H., Hong, F., Baker, R. J., Loo, S. M., Walters, R. and Imonigie, J., "An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone," *Fourth International Conference on Unsaturated Soils* (*UNSAT '06*) *Conference, April 2-6, 2006, Carefree, AZ.*
25. Gribb, M., Hill, H. H., Baker, R. J., Loo, S. M., and Moll, A. J., "Ion Mobility Spectrometer (IMS) Sensor Project," presented at the *Environmental & Subsurface Science Symposium*, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
24. Ogas, M. L., Price, P. M., Kiepert J., Baker R. J., Bersuker G., and Knowlton W.B., *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
23. Butler, D. L. and Baker, R. J., *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, *Proceedings of the IEEE 48th International Midwest Symposium on Circuits and Systems*, Aug. 7-10, 2005.
22. Cheek, B. J., Southwick III, R. G., Ogas, M. L., Nagler, P. E., Whelchel, D., Kumar, S., Baker, R. J., and Knowlton, W. B., "Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits," poster presentation at *2004 IEEE International Integrated Reliability Workshop*, Oct. 18-21, 2004.
21. Ogas, M., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., "Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra-Thin Oxides," poster presentation at the *Workshop on Microelectronics and Electron Devices*, Boise, Idaho, April 16, 2004.
20. Ogas, M. L., Southwick III, R. G., Cheek, B. J., Baker, R. J., Bersuker, G., and Knowlton, W. B., "Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices," in *Proceedings of the 2004 IEEE International Integrated Reliability Workshop*, pp. 32-36.
19. Cheek, B. J., Stutzke, N., Santosh, K., Baker, R. J., Moll, A. J., and Knowlton, W. B., Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, *2004 IEEE International Reliability Physics Symposium*, April, 25-29.
18. Stutzke, N., Cheek, B. J., Wiscombe, M., Lowman, T., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
17. Ogas, M. L., Southwick, R. G., Cheek, B. J., Lawrence, C. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
16. Baker, R. J., *Mixed-Signal Design in the Microelectronics Curriculum,* IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.

15. Hartman, J. A., Baker, R. J., Gribb, M., Hill, H. H., Jessing, J., Moll, A. J., Prouty, and Russell, D., *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
14. Lawrence, C.E., Cheek, B. J., Lawrence, T. E., Kumar, S., Haggag, A., Baker, R. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003.
13. Cheek, B., Lawrence, C., Lawrence, T., Gomez, J., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs),* IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25, 2002.
12. Lawrence, C., Cheek, B., Caldwell, T., Lawrence, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop,* October 21-24, 2002.
11. Cheek, B., Lawrence, C., Lawrence, T., Caldwell, T., Kiri, D., Kumar, S., Baker, R. J., Moll, A. J., and Knowlton, W. B., Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at the IEEE International Integrated Reliability Workshop, October 21-24, 2002.
10. Baker, R. J., "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
9. Rivera, B., Baker, R. J., Melngailis, J., "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
8. Hess, H. and Baker, R. J., "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
7. Baker, R. J., and Hess, H., "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference,* Seattle, Washington, May 1999, pp. 673-676.
6. Baker, R. J., "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
5. Chen, H. and Baker, R. J., "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
4. Liu, S. and Baker, R. J., "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st International Midwest Symposium on Circuits and Systems, August 9-12, 1998.*
3. Boyce, D.E. and Baker, R. J., "A Complete Layout System for the PC," *IEEE 40th International Midwest Symposium on Circuits and Systems*, 1997.
2. Baker, R. J., and Blair, J. J., "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers,* April 3-4, Las Vegas, Nevada, 1991.
1. Baker, R. J., "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10, 1990.

EXPERT WITNESS EXPERIENCE

The law firms and clients (underlined) whom I have provided expert witness services in electrical and computer engineering are listed below. I have been deposed 109 times, given expert testimony at 14 trials (7 USITC, 2 D. Del., 1 Arbitr., 1 S.D. Cal., 1 N.D. Ga., 1 D. Ore., and 1 E.D. Tex.), and participated in 1 mediation.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – *MediaTek, Inc.* v. Redstone Logics LLC

Case Number – IPR2025-00085. Petition filed on October 22, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Baker Botts LLP (Houston, TX)

Case – *Innolux Corporation* v. Phenix Longhorn LLC

Case Numbers – IPR2025-00043 and IPR2025-00044. Petitions filed on October 15, 2024.

Case Subject Matter – Systems and methods for outputting "corrected" gamma reference voltages to drive a Liquid Crystal Display (LCD).

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dority & Manning LLP (San Diego, CA and Greenville, SC)

Case – *LithiumHub, LLC* v. Bass Pro Outdoor et. al.

Case Numbers – ITC Investigation No. 337-TA-1421. Complaint filed September 12, 2024.

Case Subject Matter – starting a combustion engine using lithium-based battery cells and solid-state switches.

Work Performed – Provided expert consulting services. Wrote declaration for a claim construction brief.

Baker Botts LLP (Austin, TX and Houston, TX)

Case – *Silicon Motion Inc.* v. K.Mizra, LLC

Case Number – IPR2024-01236. Petition filed on September 10, 2024.

Case Number – IPR2024-01240. Petition filed on August 13, 2024.

Case Number – IPR2024-01241. Petition filed on August 9, 2024.

Case Subject Matter – Calibrating a memory controller for use with DDR (double-data rate) DRAM (dynamic random access memory). Calibrating a communication channel to receive a digital signal. A micro-threaded memory device.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Garlick & Markison, LLC (Phoenix, AZ and Austin, TX)

Case – Ex Parte Reexamination

Case Number – 90/019612. Request filed on August 6, 2024.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services and wrote declaration**.**

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc.* v. Intellectual Ventures II LLC

Case – *Lenovo Inc.* v. University of Rochester

Case Numbers – IPR2024-01225 and IPR2024-01226. Petitions filed on August 2, 2024.

Case Subject Matter – Methods for calibrating intra-cycle timing in digital communications. Digital circuits with multiple clock domains.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Wolf, Greenfield & Sacks, P.C. (Washington, D.C., and Boston, MA)

Case – *Infineon Technologies* v. Innoscience Technology

Case Numbers – ITC Investigation No. 337-TA-1414. Complaint filed July 26, 2024.

Case Subject Matter – GaN-on-Si semiconductor devices, GaN field effect transistors (FETs), and packaging power transistors.

Work Performed – Provided expert consulting services.

DLA Piper LLP (Palo Alto, CA and Austin, TX)

Case – *BOE Technology Group Co., Ltd.* v. Optronic Sciences LLC

Case Numbers – IPR2024-01130, IPR2024-01133, and IPR2024-01134. Petitions filed on July 5, 2024

Case Subject Matter – Imaging pixels, layout, and fabrication. Light emitting devices, including packaging, covers, and structures.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Dentons US LLP (Washington, DC)

Case – *Reolink Digital Technology Co., Ltd.* v. KT Imaging US, LLC

Case Numbers – IPR2024-01154 and IPR2024-01155. Petitions filed on July 3, 2024

Case Subject Matter – Image sensor structure and package with integrated lens module for digital image products such as digital cameras, camera phones, video phones, fingerprint readers and so on.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/019,560, 90/019,962, and 90/019,964. Requests filed on July 1, 2024

Case Numbers – 90/019,556, 90/019,557, and 90/019,558. Requests filed on June 28, 2024.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for ex parte reexaminations.

Banner Witcoff (Chicago, IL and Washington, DC)

Case – *ZF Friedrichshafen AG, ZF Active Safety and Electronics US LLC, and Nissan Motor Company, Ltd.* v. Foras Technologies, Ltd.

Case Number – IPR2024-00969. Petition filed on June 24, 2024.

Case Subject Matter – Detecting loss of lockstep between pairs of processors and loss of lockstep recovery

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Fish & Richardson P.C. (San Diego, CA and Boston, MA)

Case – *Vicor Corporation* v. Delta Electronics, Inc.

Case Numbers – IPR2024-00704, IPR2024-00705, IPR2024-00706, and IPR2024-00715. Petitions filed on March 25, 2024.

Case Subject Matter – Power converters including design, packaging, heatsinking and manufacturing. Resonant converters with overcurrent protection.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Pillsbury Winthrop Shaw Pittman LLP (San Francisco, CA)

Case – Redstone Logics LLC v. *MediaTek, Inc.*

Case Number – Texas, WD (Midland/Odessa) 7:24-cv-00029. Complaint filed January 26, 2024.

Case Subject Matter – multi-core processors with voltage and clock scaling functionality and related communications/control signaling.

Work Performed – Provided expert consulting services including writing declaration for claim construction.

Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C. (Boston, MA)

Case – RoadRunner Recycling, Inc. v. *Recycle Tract Systems*

Case Number – California, ND 3:23-cv-04804. Amended complaint filed on January 16, 2024.

Case Subject Matter – Waste and recycling metering technology.

Work Performed – Provided expert consulting services including writing expert report. Was deposed.

Winston & Strawn LLP (Los Angeles, CA and Redwood City, CA)

Case – *Silicon Motion, Inc.* v. Unification Technologies LLC

Case Number – IPR2024-00199. Petition filed on December 18, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Garlick & Markison, LLC (Austin, TX)

Case – *NXP USA, Inc.* v. Bell Semiconductor, LLC

Case Numbers – IPR2024-00167 and IPR2024-00168. Petitions filed on November 9, 2023.

Case Subject Matter – Semiconductor manufacturing processes, fabrication and packaging of integrated circuits, layout and routing of signal lines.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019288. Request filed on October 20, 2023.

Case Subject Matter – Power conversion device to drive an alternating-current motor for an electric vehicle.

Work Performed – Provided expert consulting services and wrote declaration.

Haynes and Boone, LLP (Dallas, TX)

Case – *Western Digital Technologies, Inc.* v. Longitude Licensing LTD.

Case Number – IPR2023-01200. Petition filed on July 14, 2023.

Case Subject Matter – Communications between a memory controller and memory.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Mojo Mobility, Inc.

Case Numbers – IPR2023-01094, IPR2023-01095, IPR2023-01096, IPR2023-01097, IPR2023-01098, IPR2023-01099, IPR2023-01100, and IPR2023-01124. Petitions filed on June 30, 2023.

Case Numbers – IPR2023-01101 and IPR2023-01102. Petitions filed on June 29, 2023.

Case Numbers – IPR2023-01091, IPR2023-01092, and IPR2023-01093. Petitions filed on June 28, 2023.

Case Numbers – IPR2023-01086, IPR2023-01087, IPR2023-01088, IPR2023-01089, and IPR2023-01090. Petitions filed on June 27, 2023.

Case Subject Matter – Wireless charging systems, power sources, and inductive receivers for charging mobile devices.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Winston & Strawn LLP (Los Angeles, CA, Redwood City, CA, Chicago, IL, and Houston, TX)

Case – Unification Technologies LLC v. *Silicon Motion, Inc.*

Case Number – Texas, ED (Marshall) 2:23-cv-00267. Complaint filed June 2, 2023.

Case Subject Matter – Memory controller, solid-state drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services.

Norton Rose Fulbright LLP (Austin, TX and Dallas, TX)

Case – *Current Lighting Solutions, LLC d/b/a GE Current* v. Jiaxing Super Lighting Electric Appliance Co., Ltd.

Case Numbers – IPR2023-00979 and IPR2023-00980. Petitions filed on May 31, 2023.

Case Number – IPR2023-00270. Petition filed on December 19, 2022.

Case Number – IPR2023-00271. Petition filed on December 14, 2022.

Case Subject Matter – LED lighting, lamps, tube lamps, assembly, and associated circuits and electronics.

Work Performed – Provided expert consulting services and wrote declarations for inter partes review.

Faegre Drinker Biddle & Reath LLP (San Francisco, CA, Washington, DC, and Minneapolis, MN)

Case – CogniPower LLC v. *Samsung Electronics*

Case Number – Texas, ED (Marshall) 2:23-cv-00160. Complaint filed April 10, 2023.

Case Subject Matter – Power conversion using switching power supplies.

Work Performed – Provided expert consulting services and wrote expert reports.

Baker Botts LLP (Dallas, TX)

Case – *Lennox Industries Inc.* v. Rosen Technologies LLC

Case Numbers – IPR2023-00715, IPR2023-00716, IPR2023-00717, IPR2023-00718, and IPR2023-00719. Petitions filed on March 29, 2023.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Cooley LLP (Palo Alto, CA)

Case – *Nintendo Co., Ltd. and Nintendo of America Inc.* v. Polaris PowerLED Technologies, LLC

Case Number – IPR2023-00778. Petition filed on March 28, 2023.

Case Subject Matter – Visual displays, circuit design, and related technologies.

Work Performed – Provided expert consulting services, wrote declaration for inter partes review, and was deposed.

Bracewell LLP (New York, NY and Seattle, WA)

Case – *Kioxia America, Inc. and Kioxia Corporation* v. BiTMICRO LLC

Case Numbers – IPR2023-00741, IPR2023-00742, and IPR2023-00743. Petitions filed on March 23, 2023.

Case Subject Matter – Solid-state storage devices utilizing multi-profile memory controllers. Optimizing memory operations in a memory system suitable for use in an electronic storage device. Supplying energy to a cache memory using a super capacitor.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Bookoff McAndrews, PLLC (Washington, DC)

Case – *Lenovo Inc. and Motorola Mobility LLC* v. Theta IP, LLC

Case Numbers – IPR2023-00694, IPR2023-00697, and IPR2023-00698. Petitions filed on March 7, 2023.

Case Subject Matter – Power in wireless communication circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA)

Case – Semiconductor Design Technologies LLC v. *Cadence Design Systems, Inc.*

Case Number – California, ND 3:23-cv-01001. Complaint filed March 6, 2023.

Case Subject Matter – Semiconductor design support device/method and manufacturing method for semiconductor integrated circuit.

Work Performed – Provided expert consulting services.

McDermott Will & Emery LLP (Chicago, IL and Austin, TX)

Case – *Xilinx, Inc.* v. Polaris Innovations Limited

Case Numbers – IPR2023-00513 and IPR2023-00514. Petitions filed on February 6, 2023.

Case Subject Matter – Methods for terminating a memory chip with various termination resistances and output drivers for integrated circuits.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed**.**

Willkie Farr & Gallagher LLP (San Franciso, CA)

Case –Bell Semiconductor, LLC. v. *Synopsys, Inc.*

Case Number – California, SD 3:22-cv-00594. Complaint filed on January 31, 2023.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services and wrote expert reports.

Fish & Richardson P.C. (Washington, DC, Atlanta, GA, and Boston, MA)

Case – Element Capital Commercial Company PTE. LTD v. *BOE Technology Group Co. LTD and Motorola (Wuhan) Mobility*

Case Number – Texas, ED (Marshall) 2:22-cv-00118. Complaint filed January 11, 2023.

Case Subject Matter – Display technology, layout, circuit design, pixel design and fabrication.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Baker Botts LLP (San Franciso, CA and New York, NY) and O'Melveny & Myers LLP (Los Angeles, CA)

Case – Polaris PowerLED, LLC v. *Samsung Electronics and Samsung Display*

Case Number – Texas, ED (Marshall) 2:22-cv-00469. Complaint filed December 12, 2022.

Case Subject Matter – active matrix organic light-emitting diode (AMOLED) displays, controlling the intensity of light-emitting diodes in backlights of displays, control circuits for adjusting current delivery based upon temperature.

Work Performed – Provided expert consulting services including writing a declaration for claim construction.

Arnold & Porter (Los Angeles and Palo Alto, CA) and Willkie Farr & Gallagher LLP (San Franciso, CA)

Case – *Synopsys, Inc. and Cadence Design Systems, Inc.* v. Bell Semiconductor, LLC.

Case Number – Delaware, 1:22-cv-01512. Complaint filed on November 18, 2022.

Case Subject Matter – Integrated circuit design computer-aided design (CAD) tools for routing, design rule checking, layout versus schematic, electrical checking, dummy fill, reducing capacitance.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Paul Hastings LLP (Washington, DC)

Case – Ex Parte Reexaminations

Case Numbers – 90/015155 and 90/015156. Requests filed on November 7, 2022.

Case Number – 90/015134. Request filed on October 14, 2022.

Case Number – 90/015130. Request filed on September 30, 2022.

Case Subject Matter – Packaging and fabrication of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declaration.

Russ August & Kabat (Los Angeles, CA)

Case – *Resonant Systems, Inc.* v. Sony

Case Number – Texas, ED (Marshall) 2:22-cv-00424. Complaint filed on October 26, 2022.

Case Subject Matter – Linear vibration modules and linear-resonant vibration modules.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed.

Sheppard, Mullin, Richter & Hampton LLP (Menlo Park, CA and San Diego, CA) and Willkie Farr & Gallagher LLP (San Francisco, CA)

Case – Bell Semiconductor, LLC v. *NXP*, SMC, Micron, Nvidia, *Advanced Micro Devices (AMD)*, *Acer*, Infineon, Qualcomm, Motorola Mobility, and Western Digital

Case Number – ITC Investigation No. 337-TA-1340. Complaint filed October 6, 2022.

Case Subject Matter – Electronic devices, semiconductor devices, and components.

Work Performed – Provided expert consulting services.

O'Melveny & Myers LLP (Los Angeles, CA)

Case – Daedalus Prime LLC v. *Samsung Electronics* and Qualcomm Inc.

Case Number – ITC Investigation No. 337-TA-1335. Complaint filed September 12, 2022.

Case Subject Matter – Semiconductor devices, mobile devices, and components.

Work Performed – Provided expert consulting services.

Fish & Richardson P.C. (Boston, MA, Houston, TX, and Washington, DC)

Case – Sonrai Memory LTD. v. *Micron Technology, Inc.*

Case Numbers – Texas, WD (Waco) 6:22-cv-00855 and Texas, WD (Waco) 1:23-cv-01407. Complaint filed August 16, 2022.

Case Subject Matter – Portable RAM drive and variable charge pump circuit with dynamic load.

Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Russ August & Kabat (Los Angeles, CA and New York, NY)

Case – *NextGen Innovations, LLC* v. Infinera, Fujitsu, AT&T, and Nokia

Case Number – Texas, ED (Marshall) 2:22-cv-00306, Texas, ED (Marshall) 2:22-cv-00307, Texas, ED (Marshall) 2:22-cv-00308, and Texas, ED (Marshall) 2:22-cv-00309. Complaints filed on August 9, 2022.

Case Subject Matter – optical transmission systems including optical components for encoding, transmission (fiber optic transmitters and receivers), and decoding of data and related standards and concepts.

Work Performed – Provided expert consulting services, wrote claim construction disclosure, wrote expert reports, and was deposed twice.

DLA Piper (Chicago, IL and Washington, DC)

Case – Ampt, LLC v. *SolarEdge Technologies, Inc.*

Case Number – ITC Investigation No. 337-TA-1327. Complaint filed July 28, 2022.

Case Subject Matter – Solar power optimizers, inverters, and components.

Work Performed – Provided expert consulting services including writing declarations for claim construction, expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Signify North America Corporation v. *Shenzhen Intellirocks Tech Co.*

Case Number – Texas, WD (Waco) 6:22-cv-00760. Complaint filed on July 8, 2022.

Case Subject Matter – LED packaging, circuits, and systems.

Work Performed – Provided expert consulting services including writing declaration for claim construction. Was deposed.

Baker Botts LLP (Dallas, TX)

Case – Rosen Technologies LLC v. *Lennox Industries Inc.*

Case Number – Texas, ND (Dallas) 3:22-cv-00732. Complaint filed on June 7, 2022.

Case Subject Matter – Thermostat system communications, programming, and displays.

Work Performed – Provided expert consulting services.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Scramoge Technology Ltd.

Case Numbers – IPR2022-01052, IPR2022-01053, and IPR2022-01058. Petitions filed on May 26, 2022.

Case Numbers – IPR2022-01054, IPR2022-01055, IPR2022-01056, and IPR2022-01057. Petitions filed on May 24, 2022.

Case Number – IPR2022-00939. Petition filed on April 29, 2022.

Case Subject Matter – An antenna that supports wireless charging using switching power supplies such as flyback converters.

Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – Ex Parte Reexaminations
Case Number – 90/015020. Request filed on May 2, 2022.
Case Number – 90/014906. Request filed on November 12, 2021.
Case Number – 90/014899. Request filed on November 10, 2021.
Case Number – 90/014888. Request filed on October 21, 2021.
Case Numbers – 90/014886 and 90/014887. Requests filed on October 20, 2021.
Case Number – 90/014885. Request filed on October 19, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging.
Work Performed – Provided expert consulting services and wrote declarations**.**

DLA Piper (Chicago, IL, Austin, TX, and Washington, DC)

Case – *SolarEdge Technologies, Inc.* v. Fronius International GMBH
Case Number – IPR2022-00849. Petition filed on April 14, 2022.
Case Subject Matter – Mechanical assembly and enclosure whereby an upper housing part is detached from a lower housing part using a "rotate-and-lift" feature.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Kirkland & Ellis LLP (New York, NY)

Case – *Samsung Electronics Co.* v. Sonrai Memory Ltd.
Case Numbers – IPR2022-00305 and IPR2022-00306. Petitions filed on December 10, 2021.
Case Subject Matter – USB devices and circuits for saving power.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews.

Haynes and Boone, LLP (Washington, DC)

Case – *Unified Patents, LLC* v. Arigna Technology Limited
Case Number – IPR2022-00285. Petition filed on December 9, 2021.
Case Subject Matter – High voltage driver circuit for driving power devices such as insulated gate bipolar transistors (IGBTs).
Work Performed – Provided expert consulting services, wrote declaration for inter partes review and was deposed.

Paul Hastings LLP (Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. Lynk Labs, Inc.
Case Numbers – IPR2022-00149 and IPR2022-00150. Petitions filed on November 12, 2021
Case Numbers – IPR2022-00100 and IPR2022-00101. Petitions filed on October 28, 2021.
Case Numbers – IPR2022-00051, IPR2022-00052, and IPR2022-00098. Petitions filed on October 27, 2021.
Case Numbers – IPR2021-01575 and IPR2021-01576. Petitions filed on October 1, 2021.
Case Numbers – IPR2021-01299, IPR2021-01300, IPR2021-01345, IPR2021-01346, and IPR2021-01347. Petitions filed on September 7, 2021.
Case Subject Matter – Circuit design, including switching power supply design (e.g., flyback), rectifiers, power factor correction, etc. for lighting and displays using light emitting diodes (LEDs).
Work Performed – Provided expert consulting services, wrote declarations, and was deposed ten times.

Haynes and Boone, LLP (Plano, TX)

Case – *Pure Storage, Inc.* v. Digital Cache, LLC
Case Number – IPR2022-00121. Petition filed on October 29, 2021.
Case Subject Matter – Non-volatile memory (NVM) devices capable of retaining stored data in case of a power failure.
Work Performed – Provided expert consulting services and wrote declaration for inter partes review.

Banner Witcoff (Washington, DC)

Case – *SolarEdge Technologies Ltd.* v. Koolbridge Solar, Inc.

Case Numbers – IPR2022-00007, IPR2022-00008, IPR2022-00009, IPR2022-00010, IPR2022-00011, and IPR2022-00012. Petitions filed on October 11, 2021.

Case Numbers – IPR2022-00013, IPR2022-00014, and IPR2022-00015. Petitions filed on October 8, 2021.

Case Subject Matter – DC-to-AC converters using full-bridges, multi-level conversion for power systems, and other electronics for harvesting solar energy.

Work Performed – Provided expert consulting services, wrote declarations for inter partes reviews, and was deposed.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung Electronics Co., Ltd.* v. LED Wafer Solutions LLC

Case Number – IPR2021-01554. Petition filed on September 20, 2021.

Case Number – IPR2021-01526. Petition filed on September 10, 2021.

Case Number – IPR2021-01506. Petition filed on September 7, 2021.

Case Number – IPR2021-01491. Petition filed on September 3, 2021.

Case Subject Matter – Packaging of light emitting diodes (LEDs).

Work Performed – Provided expert consulting services and wrote declarations.

Paul Hastings, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/014,846. Request filed on August 30, 2021.

Case Subject Matter – Wireless power transmission and ways to wirelessly charge and/or discharge a battery.

Work Performed – Provided expert consulting services and wrote declaration.

Jones Day (San Diego, CA and Pittsburgh, PA)

Case – *SOLiD, Inc.* v. CommScope Technologies LLC

Case Numbers – IPR2021-01390, IPR2021-01391, IPR2021-01392, IPR2021-01393, and IPR2021-01394. Petitions filed on August 12, 2021.

Case Subject Matter – Digital antenna system that enables extension of radio frequency (RF) analog signals from base stations to areas (e.g., inside of buildings) where access to such signals is inhibited.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declaration.

Unified Patents, LLC (Washington, DC)

Case – Ex Parte Reexamination

Case Number – 90/019,015. Request filed on July 20, 2021.

Case Subject Matter – Voltage-controlled oscillator (VCO) temperature compensation.

Work Performed – Provided expert consulting services and wrote declaration.

Winston & Strawn LLP (Dallas, TX and Palo Alto, CA)

Case – *Micron Technology, Inc.; Micron Semiconductor Products, Inc.; Micron Technology Texas LLC* v. Unification Technologies LLC

Case Numbers – IPR2021-00940, IPR2021-00941, and IPR2021-00942. Petitions filed on June 4, 2021.

Case Subject Matter – Solid-State Drive (SSD), flash non-volatile memory management, memory controller operation and addressing.

Work Performed – Provided expert consulting services for inter partes reviews and wrote declarations.

Hill, Kertscher & Wharton, LLP (Atlanta, GA)

Case – Kaijet Technology v. *Sanho Corporation*

Case Number – IPR2021-00886. Petition filed on April 30, 2021.

Case Subject Matter – Port extension apparatus for headphone jack, USB (Universal Serial Bus or Type-C ports), and video ports such as VGA (Video Graphics Array), DVI (Digital Visual Interface), HDMI (High-Definition Multimedia Interface), DP (Display Port), and mini-DP.

Work Performed – Provided expert consulting services for inter partes review, wrote declaration, was deposed.

O'Melveny & Myers LLP (Los Angeles, CA and New York, NY)

Case – Solas OLED LTD. v. *Samsung Electronics Co. LTD.*
Case Number – Texas, ED (Marshall) 2:21-cv-00105. Complaint filed March 22, 2021.
Case Subject Matter – Touch-sensors for gesture recognition and signal processing for capacitive touch displays.
Work Performed – Provided expert consulting services including writing declaration for claim construction.

O'Melveny & Myers LLP (San Francisco, CA)

Case – Super Interconnect Technologies LLC v. *Google LLC*
Case Number – Texas, ED (Marshall) 2:18-cv-00463 (complaint filed November 2, 2018) and Texas, WD (Waco) 6:21-cv-00259 (complaint filed March 15, 2021).
Case Subject Matter – Transmission of data and clock signals. Serial signals such as transition minimized differential signaling. Communications between processors and non-volatile storage such as Universal Flash Storage (UFS) and embedded MultiMedia Controller (eMMC).
Work Performed – Provided expert consulting services and wrote expert reports.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, and Irvine, CA)

Case – Fundamental Innovation Systems International LLC v. *Anker Innovations and Fantasia Trading LLC d/b/a Ankerdirect*
Case Number – Delaware, 1:21-cv-00339. Complaint filed on March 5, 2021.
Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.
Work Performed – Provided expert consulting services, wrote expert reports, and was deposed.

Orrick, Herrington & Sutcliffe LLP (Houston, TX, Irvine, CA, and Menlo Park, CA)

Case – *TCT Mobile Inc. and TCL Communication, Inc.* v. Fundamental Innovation Systems International LLC
Case Numbers – IPR2021-00597, IPR2021-00598, and IPR2021-00599. Petitions filed on February 26, 2021.
Case Number – IPR2021-00428. Petition filed on January 13, 2021.
Case Number – IPR2021-00410. Petition filed on January 11, 2021.
Case Number – IPR2021-00395. Petition filed on December 31, 2020.
Case Subject Matter – Universal Serial Bus (USB) for charging mobile devices.
Work Performed – Provided expert consulting services including writing declarations for inter partes reviews. Was deposed twice.

Paul Hastings LLP (Austin, TX and Washington, DC)

Case – *Samsung, Inc.* v. Pictos Technologies, Inc.
Case Number – IPR2021-00557. Petition filed on February 18, 2021.
Case Number – IPR2021-00436. Petition filed on January 19, 2021.
Case Numbers – IPR2021-00437 and IPR2021-00438. Petitions filed on January 15, 2021.
Case Subject Matter – Solid-state imaging devices including red, green, and blue pixels, data conversion circuits, and interpolation circuits. CMOS imagers including fabrication and design, active pixels, and semiconductor physics.
Work Performed – Provided expert consulting services and wrote declarations for inter partes reviews.

O'Melveny & Myers LLP (San Francisco, CA) and DLA Piper (New York, NY)

Case – Solas OLED Ltd. v. *BOE Technology Group Co. Ltd. and Samsung Electronics*
Case Number – ITC Investigation No. 337-TA-1243. Complaint filed January 5, 2021.
Case Subject Matter – Active matrix OLED display devices and components
Work Performed – Provided expert consulting services, wrote expert reports, was deposed, and testified at trial.

Paul Hastings LLP (Washington, DC)

Case – *Samsung, Inc.* v. Garrity Power Services LLC
Case Number – IPR2021-00389. Petition filed on December 31, 2020.
Case Subject Matter – Power electronics including full-bridge PWM modules for wireless power transmission using magnetic coupling via antennas and transformers. Design of inductors and coils.
Work Performed – Provided expert consulting services and wrote declaration for inter partes reviews.