

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Iihola et al.
U.S. Patent No.: 11,716,816 Attorney Docket No. 50095-0199IP1
Issue Date: August 1, 2023
Appl. Serial No.: 17/364,593
Filing Date: June 30, 2021
Title: METHOD FOR MANUFACTURING AN ELECTRONIC
MODULE AND ELECTRONIC MODULE

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 11,716,816 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

APPLE-1001	U.S. Patent No. 11,716,816 (the “’816 Patent”)
APPLE-1002	Excerpts from the Prosecution History of the ’816 Patent
APPLE-1003	Expert Declaration of Dr. R. Jacob Baker, Ph.D., P.E.
APPLE-1004	U.S. Pub. 2004/0000710 A1 (“Oya”)
APPLE-1005	U.S. Pub. 2002/0180010 A1 (“Tsubosaki010”)
APPLE-1006	Shugg, W. Tillar, HANDBOOK OF ELECTRICAL AND ELECTRONIC INSULATING MATERIALS, 2nd Edition, Wiley-IEEE Press, 1995 (“Shugg”)
APPLE-1007	U.S. Pub. 2003/0102572 A1 (“Nathan 1”)
APPLE-1008	Scarlett, J.A., AN INTRODUCTION TO PRINTED CIRCUIT BOARD TECHNOLOGY, Electromechanical Publication Limited, 1984 (“Scarlett 1”)
APPLE-1009	Scarlett, J.A., MULTILAYER PRINTED CIRCUIT BOARD HANDBOOK, Electromechanical Publication Limited, 1985 (“Scarlett 2”)
APPLE-1010	Farr, I. V., “SYNTHESIS AND CHARACTERIZATION OF NOVEL POLYIMIDE GAS SEPARATION MEMBRANE MATERIAL SYSTEMS,” Dissertation submitted to the Virginia Polytechnic Institute and State University (Jul 26, 1999).
APPLE-1011	U.S. Patent No. 5,714,405 (“Tsubosaki405”)
APPLE-1012-1015	RESERVED

APPLE-1016	Yu et al., “Surface characterizations of potassium-hydroxide-modified Upilex-S® polyimide at an elevated temperature,” European Polymer Journal, Vol. 37, Issue 9, September 2001, pp. 1791-1799
APPLE-1017, -1018	RESERVED
APPLE-1019	Yamamoto et al., A Composite Electrical Insulation in Superconducting Magnets, 44 Advances in Cryogenic Eng’g (Materials) 239 (1998) (“Yamamoto”)
APPLE-1020	U.S. Patent No. 6,709,897 (“Cheng”)
APPLE-1021	RESERVED
APPLE-1022	U.S. Patent No. 11,071,207 (“Tuominen207”)
APPLE-1023	Declaration of June Munford
APPLE-1024	U.S. Publication No. 2002/0159242 to Nakatani et al. (“Nakatani”)
APPLE-1025	Japanese Patent Publication No. 11-191574 to Matsuda with Certified Translation (“Matsuda”)
APPLE-1026	U.S. Patent No. 4,068,022 to Glick (“Glick”)
APPLE-1027	RESERVED
APPLE-1028	Simon Thomas, <i>3D-Integration: Trends and Opportunities – An Overview</i> (Materials Research Society 2003)
APPLE-1029	R. Kujala, et. al., <i>Solderless Interconnection and Packaging Technique for Embedded Active Components</i> (IEEE 1999)
APPLE-1030	U.S. Patent Publication No. 2001/0026010 to Horiuchi (“Horiuchi”)

APPLE-1031	U.S. Patent No. 6,038,133 to Nakatani et al. (“Nakatani-II”)
APPLE-1032	U.S. Patent No. 5,250,843 to Eichelberger (“Eichelberger”)
APPLE-1033	International Patent Application WO1996012296 to Suwa et al. and Certified Translation (“Suwa”)
APPLE-1034	U.S. Patent No. 7,609,527 (“Tuominen527”)
APPLE-1035-1100	RESERVED
APPLE-1101	Complaint for Patent Infringement (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1
APPLE-1102	Amended Complaint for Patent Infringement (April 11, 2024), Case No. 1-24-cv-00129 (WDTX), Document 31 (redacted)
APPLE-1103	K. Vidal Memorandum on <i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> , June 21, 2022
APPLE-1104	<i>United States District Courts – National Judicial Caseload Profile</i> (June 2024) (retrieved from https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile0630.2024.pdf)
APPLE-1105	Exhibit 18 to Complaint for Patent Infringement – Infringement Claim Chart for ’816 Patent (February 5, 2024), Case No. 1-24-cv-00129 (WDTX), Document 1-17
APPLE-1106	Return of Service (February 8, 2024), Case No. 1-24-cv-00129 (WDTX), Document 8

LISTING OF CHALLENGED CLAIM ELEMENTS

Claim 1	
[1pre]	An electronic module, comprising:
[1a]	a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
[1b]	at least one opening in the first insulating-material layer that extends through the first insulating-material layer;
[1c]	a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;
[1d]	a second insulating-material layer disposed on the first insulating-material layer; and
[1e]	a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers,
[1f]	wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.
Claim 2	
[2]	The electronic module of claim 1, wherein the second insulating-material layer directly contacts the component.
Claim 3	
[3]	The electronic module of claim 1, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.
Claim 4	
[4]	The electronic module of claim 3, wherein the second conductive pattern layer is spaced apart from the component by the second insulating-material layer.

Claim 5	
[5]	The electronic module of claim 4, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.
Claim 6	
[6]	The electronic module of claim 1, wherein the first insulating-material layer is spaced apart from the component.
Claim 7	
[7]	The electronic module of claim 1, wherein the first insulating-material layer comprises a different material than a material of the second insulating-material layer.
Claim 8	
[8pre]	An electronic module, comprising:
[8a]	a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
[8b]	an opening in the first insulating-material layer that extends through the first insulating-material layer;
[8c]	a component comprising contact terminals, the component being arranged at least partially within the opening, the contact terminals electrically connected to the first conductive pattern layer;
[8d]	a second insulating-material layer disposed on the first insulating-material layer;
[8e]	a third insulating-material layer disposed on the second insulating-material layer; and
[8f]	a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first, second, and third insulating-material layers,

[8g]	wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.
Claim 9	
[9]	The electronic module of claim 8, wherein the second insulating-material layer directly contacts the component.
Claim 10	
[10]	The electronic module of claim 8, wherein the second conductive pattern layer is spaced apart from the first conductive pattern layer by the component.
Claim 11	
[11]	The electronic module of claim 10, wherein the second conductive pattern layer is spaced apart from the component by the second and third insulating-material layers.
Claim 12	
[12]	The electronic module of claim 11, wherein the second insulating-material layer is continuously disposed between the second conductive pattern layer and the component.
Claim 13	
[13]	The electronic module of claim 8, wherein the first and third insulating-material layers are spaced apart from the component.
Claim 14	
[14]	The electronic module of claim 8, wherein the first and third insulating-material layers comprise a first material, the second insulating-material layer comprises a second material, the first material being different than the second material.

I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for *inter partes* review (IPR) of claims 1-14 (“Challenged Claims”) of U.S. Patent No. 11,716,816 (“the ’816 Patent”).

II. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing Under 37 C.F.R. § 42.104(a)

Apple certifies that the ’816 Patent is available for IPR. The present Petition is being filed within one year of service of a complaint by ImberaTek, filed February 5, 2024 and served February 6, 2024. *See* APPLE-1101; APPLE-1106.

Petitioner is not barred or estopped from requesting this review challenging the Challenged Claims on the grounds identified below.

B. Challenge and Relief Requested

Petitioner requests institution of IPR and cancellation of the Challenged Claims based on the following grounds:

Ground	Claims	Basis under 35 U.S.C. § 103
1A	1-14	Tsubosaki010 in view of Tsubosaki405
1B	1-14	Tsubosaki010
2	1, 3-4, 6-8, 10-11, 13-14	Oya in view of Shugg

Grounds 1A-2 are further supported by the expert testimony of Dr. R. Jacob Baker, Ph.D., and the additional supporting evidence cited throughout this Petition and Dr. Baker's declaration. *See* APPLE-1003, ¶¶15-157.

The '816 Patent claims priority through several intervening applications to a foreign application filed September 18, 2003. APPLE-1001, Cover (30). As shown below, each prior art reference that forms the basis of Grounds 1A-2 of this Petition pre-dates the '816 Patent's earliest claimed priority date (September 18, 2003). APPLE-1003, ¶41. Petitioner does not concede that the Challenged Claims are entitled to the benefit of priority to the earlier filing dates of any of the applications listed in its priority chain, but this Petition nonetheless treats September 18, 2003 as the Critical Date for purposes of analyzing the issues addressed herein. APPLE-1003, ¶¶38-40.

Reference	Filing Date	Publication Date	Pre-AIA Prior Art Status
Tsubosaki010 (APPLE-1005)	11/21/1996	12/5/2002	§§102(a), (e)
Tsubosaki405 (APPLE-1011)	9/26/1996	2/3/1998	§§102(a)-(b), (e)
Oya (APPLE-1004)	6/12/2003	1/1/2004	§102(e)
Shugg ¹	---	1995	§§102(a)-(b)

¹ Shugg is a textbook published by IEEE Press in 1995. *See* APPLE-1006, 1-5.

The declaration of Ms. June Munford addresses evidence that confirms Shugg was

(APPLE-1006)			
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III. SUMMARY OF THE '816 PATENT

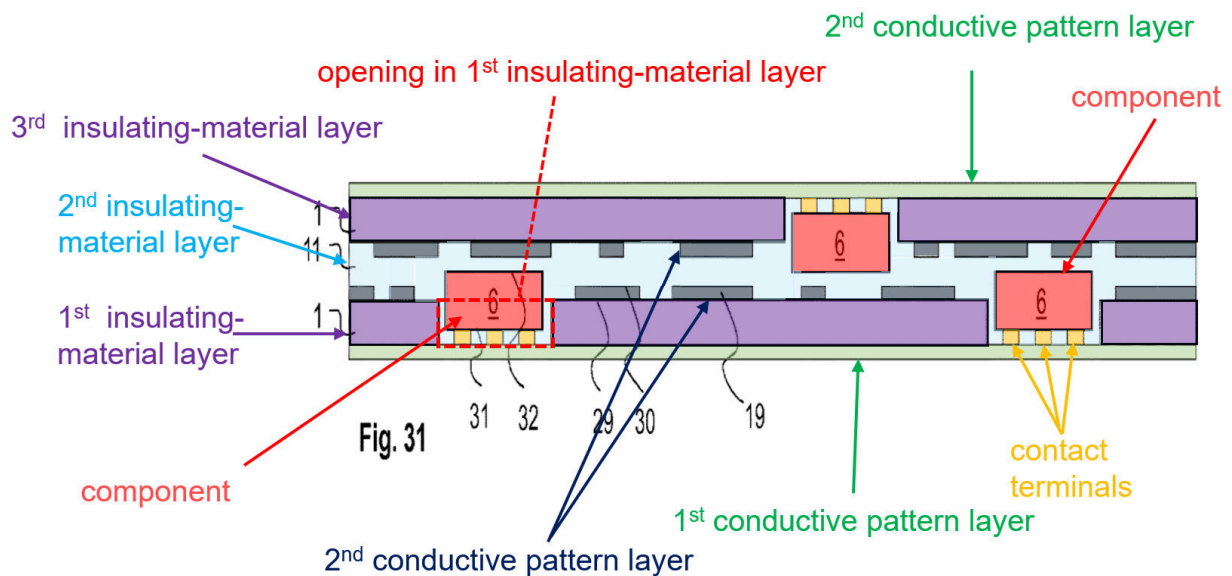
A. Brief Description

The '816 Patent generally describes techniques for fabricating “electronic modules” containing a semiconductor chip, or other component, embedded in an installation base such as a circuit board. APPLE-1001, 1:28-33; APPLE-1003, ¶¶41-42. The specification explains that “[e]mbodiments of the invention are based on commencing manufacture [of the electronic module] from an insulating board, which is surfaced on at least one side with a conductive layer.” APPLE-1001, 3:21-23. “After this, a recess or opening is made in the insulation, which opens onto one surface of the board, but does not penetrate the conductive layer on the opposite surface of the board.” *Id.*, 3:23-26. “A component is attached to the recess or opening and electrical contacts are formed between the conductive layer and the contact areas, or contact protrusions of the component.” *Id.*, 3:26-29. “After the attachment of the component, conductive patterns are formed from this

published years before the Critical Date of the '816 Patent. APPLE-1023. Ms. Munford presents evidence, for example, that Shugg was publicly accessible and disseminated to the public when it was shelved at a public library in 1995. *Id.*

conductive layer, which become part of the circuit-board structure, or other electronic module.” *Id.*, 3:29-32; *see also id.*, 3:16-4:9 (discussing alleged advantages of the designs disclosed in the ’816 Patent).

By way of example, FIG. 31 depicts one embodiment of an electronic module disclosed in the ’816 Patent (APPLE-1003, ¶43):



APPLE-1001, FIG. 31 (annotated)²

As shown above, the disclosed module includes a first insulating material

² While the metal conductive layers (shaded green) are shown as continuous surfaced material in FIG. 30, they are later patterned to form the first and second conductive pattern layers according to the processes described in the ’816 Patent. APPLE-1001, 13:3-61; *see also id.*, FIGS. 36-38.

layer 1 toward a bottom portion of the module, a second insulating material layer 11 around a middle portion of the module, and a third insulating material layer 1 toward a top portion of the module. APPLE-1001, 13:3-61; *see also id.*, 5:20-26, FIGS. 30-31; APPLE-1003, ¶44. First and second conductive pattern layers are formed on opposite sides of the first and third insulating material layers, respectively. *Id.* The first and third insulating material layers further include openings sized to receive components 6 (e.g., semiconductor chips), thereby permitting electrical connection of the contact terminals of the components 6 to the first or second conductive pattern layers. *Id.*

B. Prosecution History

The examiner issued just a single office action during original examination of the '816 Patent. APPLE-1002, 17-27; APPLE-1003, ¶¶45-48; *see also, id.*, 49-50. The office action rejected each of the independent claims and most dependent claims pending at the time as anticipated by Cheng (APPLE-1020). APPLE-1002, 19-25; APPLE-1003, ¶46. Two dependent claims were identified as reciting allowable subject matter, however. APPLE-1003, ¶43, n. 1. These claims recited that “the first conductive pattern layer and the second conductive pattern layer are each substantially planar.” *Id.* The applicant responded to the action by amending the independent claims to incorporate language based on the features recited in the allowable dependent claims:

1. (currently amended) An electronic module, comprising:
a first conductive pattern layer, and a first insulating-material layer arranged on at least one surface of the first conductive pattern layer;
at least one opening in the first insulating-material layer that extends through the first insulating-material layer;
a component comprising contact terminals, the component being arranged at least partially within the at least one opening, the contact terminals electrically connected to the first conductive pattern layer;
a second insulating-material layer disposed on the first insulating-material layer; and
a second conductive pattern layer spaced apart from the first conductive pattern layer by at least the first and second insulating-material layers,
wherein the first conductive pattern layer and the second conductive pattern layer are each substantially planar.

APPLE-1002, 2-3; *generally id.*, 11-16.

Following the applicant’s response, the examiner agreed to allow the application in a notice of allowance dated March 13, 2023. APPLE-1002, 3-10.

As Grounds 1A-2 of this Petition demonstrate, however, the ’816 Patent never should have been allowed. The conventional features recited in the Challenged Claims—including “substantially planar” conductive pattern layers—were all well known in the prior art before the alleged invention, and the claims fail to recite these features in any innovative or non-obvious arrangement. APPLE-1003, ¶47; *see also id.*, ¶48.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art relating to the subject matter of the ’816 patent as of the Critical Date (“POSITA”) would have had a Bachelor’s degree in electrical engineering, materials science, applied physics, or a related technical

field, and 2-3 years of experience in the research, design, development, or testing of circuit board or microcircuit components, or the equivalent. APPLE-1003, ¶¶38-40. Additional education could substitute for professional experience, and *vice versa*. *Id*; *see also*, APPLE-1003, ¶¶22-37.

D. Claim Construction

All claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. Here, Petitioner submits that formal claim constructions are presently unnecessary in view of the substantial overlap between the prior art teachings applied in Grounds 1A-2 and the preferred embodiments of the '816 Patent.³ *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“claim terms need only be construed to the extent necessary to resolve the controversy”); APPLE-1003, ¶49. This Petition also applies the prior art in a manner consistent with Patent Owner’s allegations of infringement before the district court. *See* EX1105.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A: Tsubosaki010 in View of Tsubosaki405 Renders Obvious Claims 1-14

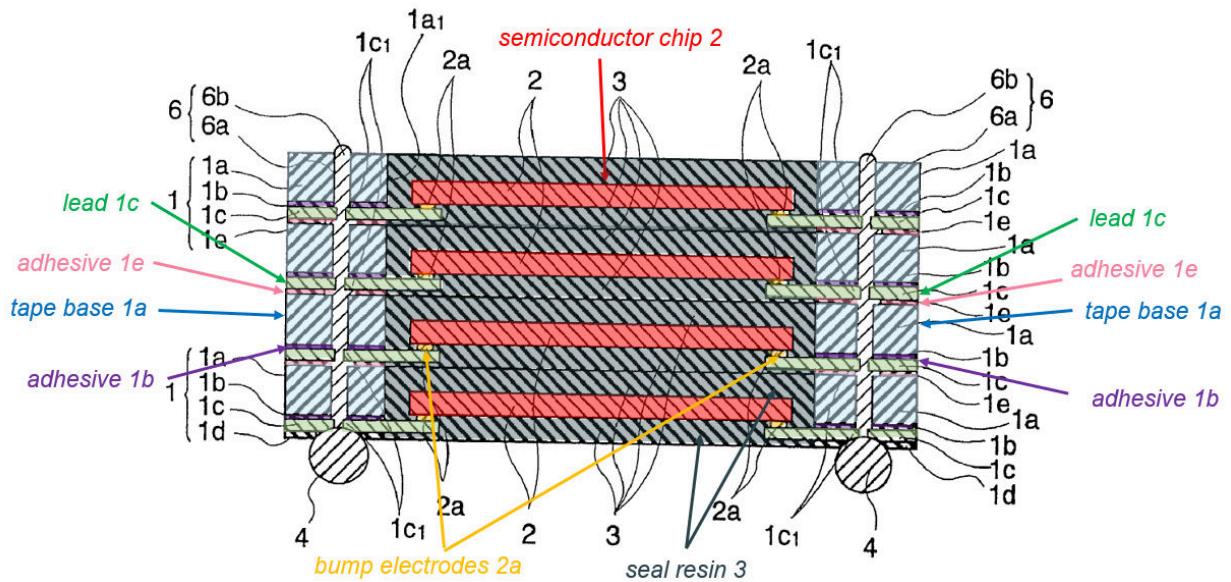
³ Petitioner is not conceding that each claim satisfies all statutory requirements, nor waiving any arguments concerning claim scope or grounds that can only be raised in district court.

1. Overview of Tsubosaki010

Tsubosaki010's disclosure "relates generally to semiconductor devices and manufacturing methodology thereof, and more particularly to technologies usefully applicable to high-density mountable semiconductor devices with tape carrier package (TCP) structures along with fabrication methods thereof." APPLE-1005, ¶[0011]; APPLE-1003, ¶52. "The TCP is a package structured including a tape carrier having a plurality of conductive leads formed thereon in a repeated pattern, wherein a semiconductor chip is placed on or in the tape carrier with its electrode pads lamination-contacted with corresponding ones of the carrier leads for electrical interconnection therebetween, the semiconductor chip being sealed by a sealing resin or the like." APPLE-1005, ¶[0003]. For example, a unitary TCP can include "a semiconductor chip 2 [] disposed within a device hole [1a1] as formed in a tape base material 1a of a tape carrier 1, which chip is less in thickness than the tape base material 1a." APPLE-1005, Abstract; *see also id.*, ¶[0062].

With reference to FIGS. 14-21, Tsubosaki010 describes techniques for manufacturing "a multi-layered TCP structure" comprising a stack of unitary TCPs laminated atop each other. *See* APPLE-1005, FIGS. 14-21, ¶¶[0108]-[0130]. The multi-layered TCP structure allows multiple unitary TCPs to be formed into a larger module comprising multiple semiconductor chips 2 with outbound leads that connect electrical terminals of the chips 2 to other circuit components and wiring.

Id., ¶¶[0108]-[0114]; APPLE-1003, ¶53.



APPLE-1005, FIG. 14

Tsubosaki010 explains that each TCP in the multi-layered structure includes a device hole 1a1 formed in a tape base 1a and adhesive layer 1b. *Id.*, ¶[[0116]. Copper film is bonded to the tape base 1a by the adhesive 1b. The copper film is later etched to form a patterned layer comprising conductive leads 1c. *Id.*, ¶¶[0116]-[0117]; FIGS. 16-17. A semiconductor chip 2 is placed within the device hole 1a1 of the tape base 1a. *Id.*, ¶[0120]. The semiconductor chip 2's bump electrodes 2a and leads 1c of the TCP are aligned and bonded to form an electrical connection. *Id.*, ¶[0120]. A layer of adhesive 1e that coats the top surface of the tape base 1a secures the stacked TCPs to each other to form the multi-layer TCP structure shown in FIG. 14 (sectional view) and FIG. 15 (plan view). *Id.*, ¶¶[0111],

¶¶[0124]-[0125]; *see also id.*, ¶¶[0141]-[0154] & FIGS. 27-30 (describing option for sealing the semiconductor chips 2 in sealing resin 3 using a single molding process for the entire stacked structure).⁴

2. Overview of Tsubosaki405

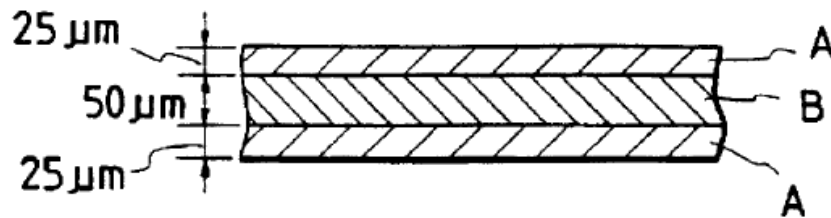
Like Tsubosaki010, Tsubosaki405 describes structures and uses of conventional carrier tapes for electronic packaging.⁵ APPLE-1011, Abstract; APPLE-1003, ¶55. For example, Tsubosaki405 discloses “insulating adhesive films (tapes) 2, 7 ... in the form of a tape having a thermosetting or thermoplastic single layer (an adhesive material only), or a double adhesive layer (not less than three layer construction).” APPLE-1011, 7:33-41. “In the case of a three-layer insulating adhesive film 27 shown in FIG. 5, for instance, it is multilayer in construction, having a base B interposed between adhesive layers A, and composed of, e.g., polyetheramideimide 25 μm/captone 50 μm/polyetheramideimide 25 μm.” *Id.*, 7:35:40; *see also id.*, 7:40-41 (“In this case, any other polyimide film may

⁴ Tsubosaki010’s Fifth and Seventh embodiments include substantially similar structures that map to the Challenged Claims in a generally equivalent manner. APPLE-1003, 54.

⁵ The first-named inventor on both Tsubosaki010 and Tsubosaki405 is Kunihiro Tsubosaki. APPLE-1003, 55, n. 2.

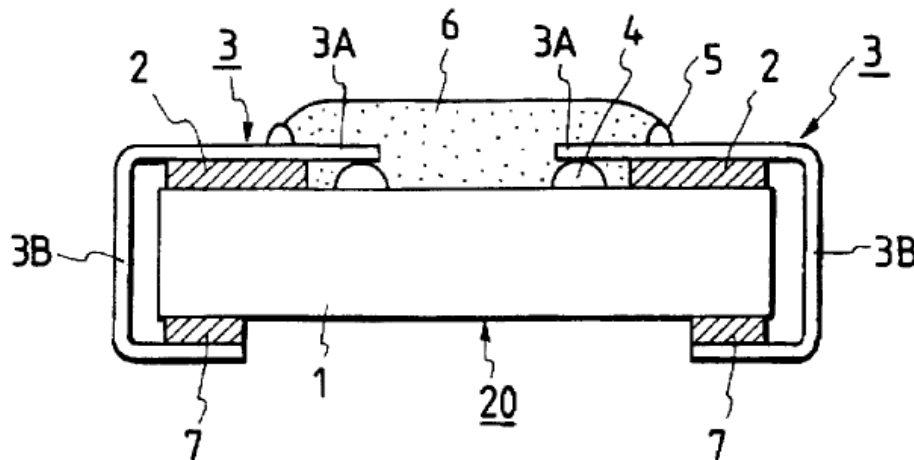
replace the captone.”).

FIG. 5



APPLE-1011, FIG. 5

Tsubosaki405's insulating adhesive films are used for bonding structures to circuitry leads 3 made from thin metal films such as iron or copper. *See, e.g.,* APPLE-1011, 1:65-2:22, 6:44-48 (“[T]he insulating adhesive films 2, 3 are bonded to the leadframe in position. The lead 3 is in the form of a sheet or foil of Fe (42 Ni-Fe material) or Cu ...”), FIGS. 1-2; APPLE-1003, ¶56.



APPLE-1011, FIG. 2

3. Predictable Combination of Tsubosaki010 and Tsubosaki405

As discussed above, Tsubosaki010 discloses a tape base 1a of a tape carrier 1 that can be “made of polyimide resin or other similar suitable materials.” APPLE-1005, ¶[0064]; *see also id.*, ¶¶[0111], [0118]; APPLE-1003, ¶57. A thin copper film patterned to form leads 1c is bonded to the tape base 1a by an adhesive 1b. *Id.*, ¶[0116]-[0117], [0063]. “Adjacent ones of the laminated unitary TCPs are bonded together by adhesive 1e,” which can be “made of a thermally deformable polyimide resin material.” *Id.*, ¶[0111]; *see also id.*, [0118], FIG. 18.

To the extent Tsubosaki010 does not expressly disclose that the tape base layer 1a and adhesive layers 1b and 1e are made from insulating materials, it would have been obvious to a POSITA to use insulating materials for these components based on the teachings of Tsubosaki405. APPLE-1003, ¶58. Recall, for example, that Tsubosaki405 describes conventional carrier tapes in which both the base member and adhesives on either side of the base member are insulating materials. APPLE-1011, 7:33-41 (describing “a three-layer insulating adhesive film 27 ... having a base B interposed between adhesive layers A”), FIG. 5. Applying Tsubosaki405’s teachings to Tsubosaki010, tape base 1a, adhesive 1b, and adhesive 1e would each predictably be made of insulating materials in a manner analogous to the three-layer adhesive film disclosed in Tsubosaki405. APPLE-1003, ¶58. In the combination, in some examples, base 1a may include “captone” or “any other polyimide film,” adhesive 1b may include “polyetheramideimide,”

and adhesive 1e may be an insulating “thermally deformable polyimide resin” based on the teachings of Tsubosaki405 and Tsubosaki010. *See, e.g.*, APPLE-1011, 7:33-41; APPLE-1005, ¶¶[0064], [0111], [0116]-[0118]; APPLE-1003, ¶58. Other suitable insulating materials may also be used. APPLE-1003, ¶58.

A POSITA would have been motivated to implement Tsubosaki010’s tape base 1a and adhesives 1b and 1e with insulating materials based on the teachings of Tsubosaki405 for multiple reasons. APPLE-1003, ¶59.

First, a POSITA would have implemented Tsubosaki010’s tape base 1a and adhesives 1b and 1e as insulating materials to ensure that different conductive leads 1c within each TCP in the stack and/or conductive leads 1c from different TCPs in the stack are electrically isolated from each other. APPLE-1003, ¶60. As FIG. 15 of Tsubosaki010 shows, each TCP 1 can include dozens of leads 1c that function as separate power and/or signal lines delivering power and/or signals to respective terminals of the semiconductor chip 2. APPLE-1005, FIG. 15; *see also id.*, ¶[0017]-[0022], [0062], [0110]. Because the tape base 1a and adhesives 1b, 1e are situated between conductive leads within and between TCPs of Tsubosaki010’s multi-layer structure, a POSITA would have sought to implement these components with insulating materials to ensure the leads are electrically isolated and to reduce the risk of a short circuit due to undesired connections between different leads and conductors in the module. APPLE-1003, ¶60; *see also id.*,

APPLE-1008, 556.

Second, a POSITA would have appreciated that due to power and electrical signals being conducted to the semiconductor chip 2 by leads 1c, no need exists for the tape base 1a or adhesives 1b and 1e to similarly be conductive to deliver power or signals either to chip 2 or any other module component. APPLE-1003, ¶61. Indeed, neither tape base 1a nor adhesives 1b and 1e are electrically connected to the terminals of semiconductor chip 2, and they are therefore neither intended nor able to practicably serve as power or signal lines for the chip 2 or other components in Tsubosaki 010's module. *See, e.g.*, APPLE-1005, FIGS. 14-21; APPLE-1003, ¶61. A POSITA therefore would have had no reason to implement conductive materials for the tape base 1a or adhesives 1b or 1e, and it would have been obvious to instead choose insulating materials given that conductive materials would serve no evident purpose. APPLE-1003, ¶61.

Third, a POSITA would have found insulating materials for the tape base 1a and adhesives 1b and 1e obvious to try. APPLE-1003, ¶62. There exist a finite number of classes of materials that could be used to implement tape base 1a and adhesives 1b and 1e—namely, insulating materials or conductive materials—and a POSITA would have had ample reason to try insulating materials for each of the reasons described herein (e.g., to promote electrical isolation between leads 1c, semiconductor chips 2, and other components of the module). APPLE-1003, ¶62.

Fourth, a POSITA would have understood that insulators such as the polyimide-based materials suggested in Tsubosaki405 were commonly used in electronic devices before the Critical Date. APPLE-1003, ¶63. These and similar materials (e.g., polyamides) were known to be useful in “prevent[ing] cross-talk between conducting vias, and as adhesives between polymer-polymer and polymer-metal interface.” APPLE-1010, 42; APPLE-1003, ¶63. Such materials can also provide “excellent performance at elevated temperatures” and exhibit beneficial “corrosion resistance.” APPLE-1010, 42; APPLE-1003, ¶63.

Fifth, a POSITA would have found insulating materials such as the polyimides described in Tsubosaki405 obvious and desirable to use when implementing Tsubosaki010’s tape base 1a and adhesives 1b and 1e to gain the benefit of their low dielectric constants and other favorable properties. APPLE-1003, ¶64. Polyimides were “used as dielectric layers in a variety of microelectronic applications since they have good processability, low dielectric constant, high thermal stability, low moisture absorption, and good mechanical properties.” APPLE-1016, Intro.; APPLE-1003, ¶64.

Sixth, implementing tape base 1a and adhesives 1b and 1e with insulating materials would have been obvious as a predictable application of Tsubosaki405’s known materials to Tsubosaki010’s known structures to achieve merely predictable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed

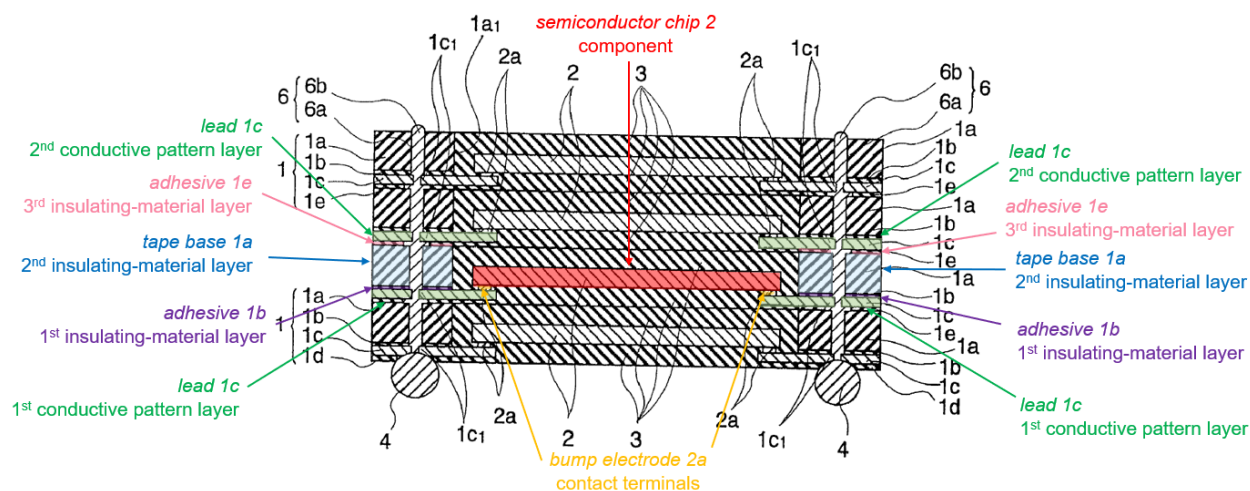
invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious); APPLE-1003, ¶65.

A POSITA would have reasonably expected success implementing the tape base 1a and adhesives 1b and 1e in the Tsubosaki010-Tsubosaki405 combination. APPLE-1003, ¶66. Insulating materials were commonly used with adhesive films in tape carriers before the '816 Patent, and Tsubosaki010 and Tsubosaki405 both contemplated the use of similar polyimide-based materials for similar tape base member and adhesive structures. *Id.* Indeed, Tsubosaki 010 notes that tape base 1a and adhesive 1e can each be made of polyimide materials, although Tsubosaki010 does not disclose the same specificity as Tsubosaki405. *Id.*; APPLE-1005, ¶¶[0064], [0111], [0118]. Tsubosaki010 and Tsubosaki405 are both also analogous art in that they are both in the same field of endeavor and/or reasonably pertinent to the problem faced by the inventors of the '816 Patent. For example, like the '816 Patent, Tsubosaki010 and Tsubosaki405 both describe techniques for manufacturing and packaging electronic modules. APPLE-1003, ¶66; APPLE-1001, 1:17-39; *supra*, §§IV.A.1-2; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

4. Application to Challenged Claims

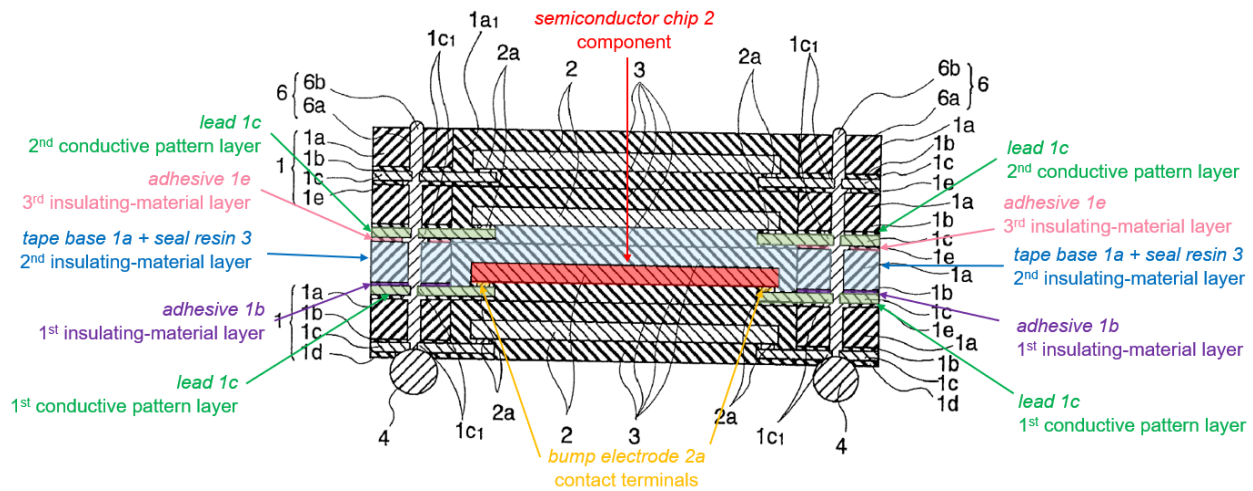
The Tsubosaki010-Tsubosaki405 combination renders the Challenged Claims and each recited claim element obvious for the reasons addressed in detail

in the element-by-element analysis that follows below. The following annotated figures depict an overview of two alternative mappings of the prior art to the Challenged Claims consistent with the detailed analysis below.⁶ APPLE-1003, ¶¶51, 52-103.



APPLE-1005, FIG. 14 (annotated) – First Mapping

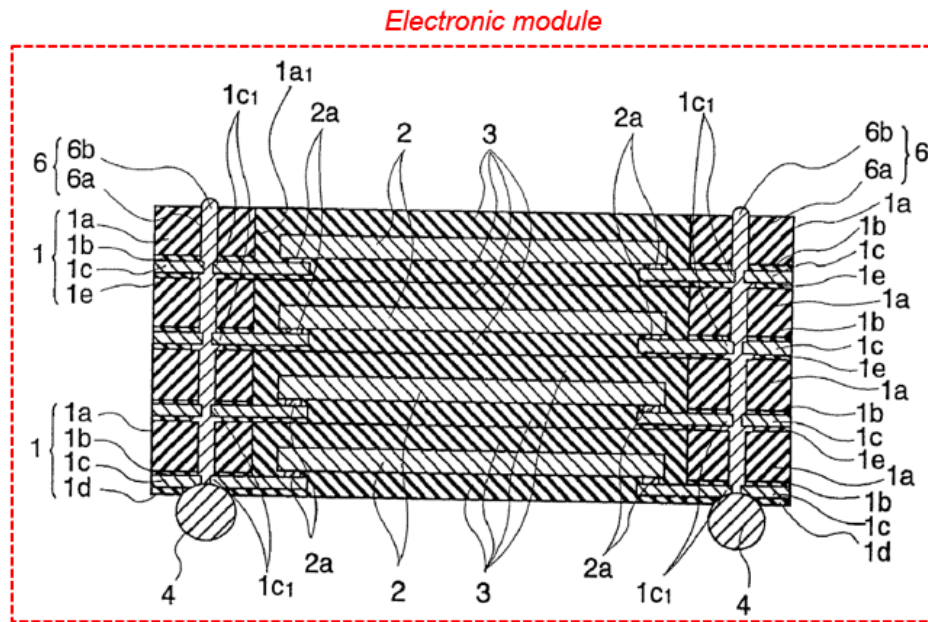
⁶ As explained in the analysis of Element [1d], tape base 1a alone provides the claimed “second insulating-material layer” according to a first mapping of the Tsubosaki010-Tsubosaki405 combination to the Challenged Claims. Tape base 1a together with seal resin 3 provides the claimed “second insulating-material layer” according to a second (alternative) mapping. *Infra*, Element [1d]; APPLE-1003, 68, 74, 93, n. 1, 145. The first and second mappings are otherwise the same (*i.e.*, apart from the mappings for the second insulating-material layer).



APPLE-1005, FIG. 14 (annotated) – Second Mapping

Element [1pre]

To the extent the preamble is limiting, the Tsubosaki010-Tsubosaki405 combination renders it obvious. APPLE-1003, ¶67. For example, Tsubosaki010 discloses that “a plurality of TCPs ... are laminated on one another to constitute a multi-layered TCP structure” that corresponds to an “*electronic module*” as claimed. APPLE-1005, ¶[0110]; *generally id.*, ¶¶[0108]-[0130], FIGS. 14-21. Tsubosaki010’s modules are “adaptable for use with a semiconductor device as built in electronic equipment—such as computers, portable or mobile radiotelephone handsets, video cameras or the like—or integrated circuit (IC) cards or memory cards; for example, the semiconductor device is arranged to have a tape carrier package (TCP) structure which includes a semiconductor chip 2 disposed within a device hole 1 a 1 of a tape carrier 1.” APPLE-1005, ¶[0062].

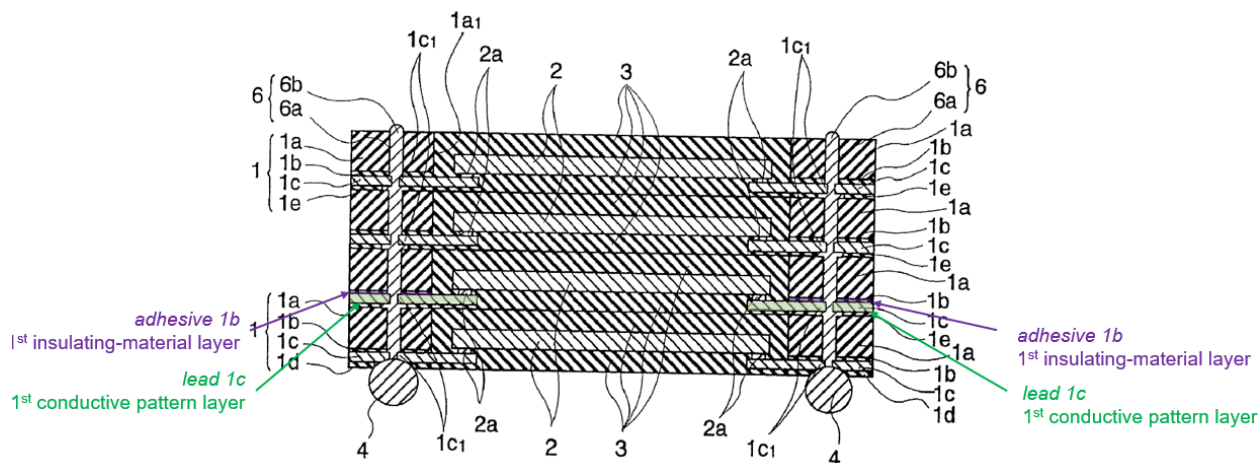


APPLE-1005, FIG. 14 (annotated)

Element [1a]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1a]. APPLE-1003, ¶68. For example, in the combination, leads 1c from a given one of the TCPs in the stacked TCP module corresponds to a “*first conductive pattern layer*” and adhesive layer 1b from the same TCP corresponds to a “*first insulating-material layer*” arranged on at least one surface (*i.e.*, a top surface) of the leads 1c as claimed. APPLE-1005, ¶¶[0116]-[0117] (“a tape base 1a with *adhesive 1b bonded to its one surface*”; “*bond a Cu thin-film* for example to one surface of the tape base 1a by using the adhesive 1b attached thereto; thereafter,

of leads 1c ...)⁷, FIGS. 14, 16-17, 21; *see also id.*, ¶¶[0063], [0066], [0068].



APPLE-1005, FIG. 14 (annotated)

To the extent Tsubosaki010 does not expressly disclose that adhesive layer 1b is made from an insulating material, Tsubosaki405 discloses “*insulating* adhesive films ... in the form of a tape” having insulative adhesive such as polyetheramideimide bonded between a lead and a tape base member in a semiconductor package similar to Tsubosaki010’s adhesive layer 1b. APPLE-1011, 7:33-41, FIG. 5; *supra*, §IV.A.2. It would have been obvious based on Tsubosaki405 to implement Tsubosaki010’s adhesive layer 1b as an insulating-material layer for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §IV.A.3; APPLE-1003, ¶69.

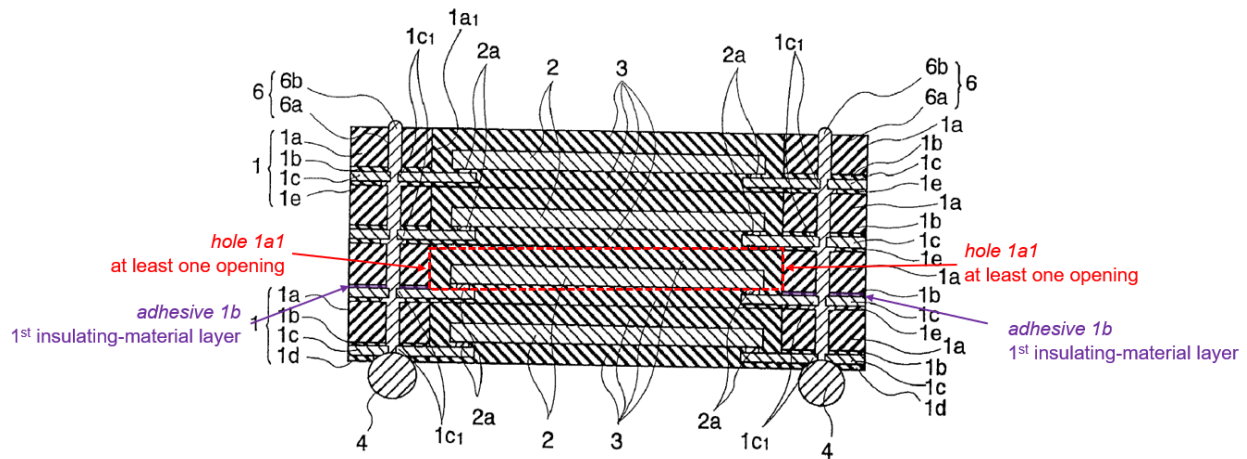
⁷ All emphasis added unless indicated otherwise.

Element [1b]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1b]. APPLE-1003, ¶70. For example, Tsubosaki010 discloses a device hole 1a1 (*at least one opening*) formed in tape base 1a and adhesive layer 1b (*first insulating-material layer*), where the device hole 1a1 extends through the entire thickness of adhesive layer 1b (*first insulating-material layer*). APPLE-1005, ¶[0116] (“form by mechanical die-punching techniques a device hole 1a1”), ¶[0120] (“place a semiconductor chip 2 within the device hole 1a1”), FIGS. 16-19; *see also id.*, Abstract (“A semiconductor chip 2 is disposed within a device hole as formed in a tape base material 1a of a tape carrier 1 ...”), ¶¶[0062]-[0065], FIGS. 14, 21.⁸

FIG. 19 shows the hole 1a1 (*at least one opening*) formed in the tape base

⁸ Nothing in the plain language of Element [1c] requires that a thickness of the “at least one opening” be coterminous with the thickness of first insulating-material layer. APPLE-1003, 70, n. 5. Even if this were required, however, the portion of device hole 1a1 that spans the space between adhesive layer 1b, to the exclusion of the portion of device hole 1a1 that spans the space between tape base 1a, provides an alternative mapping to the claimed “at least one opening.” APPLE-1003, 70, n. 5.



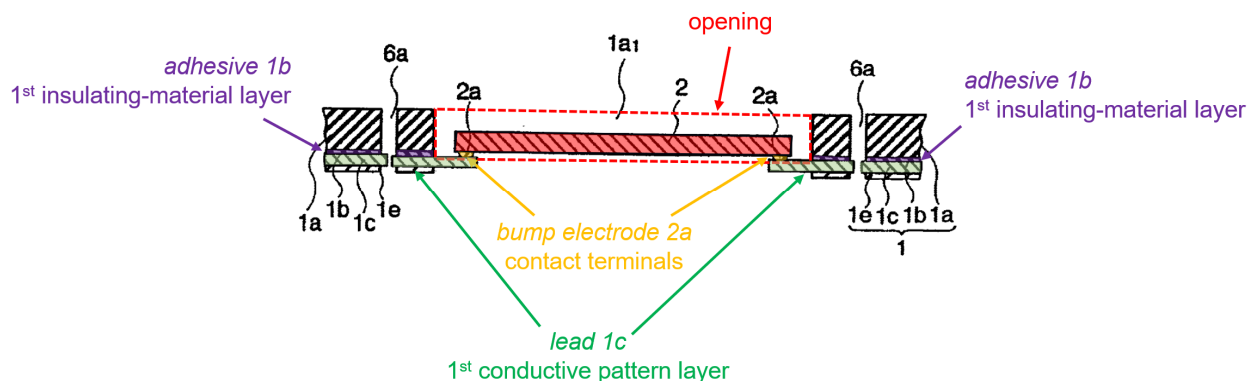
APPLE-1005, FIG. 14 (annotated)

Element [1c]

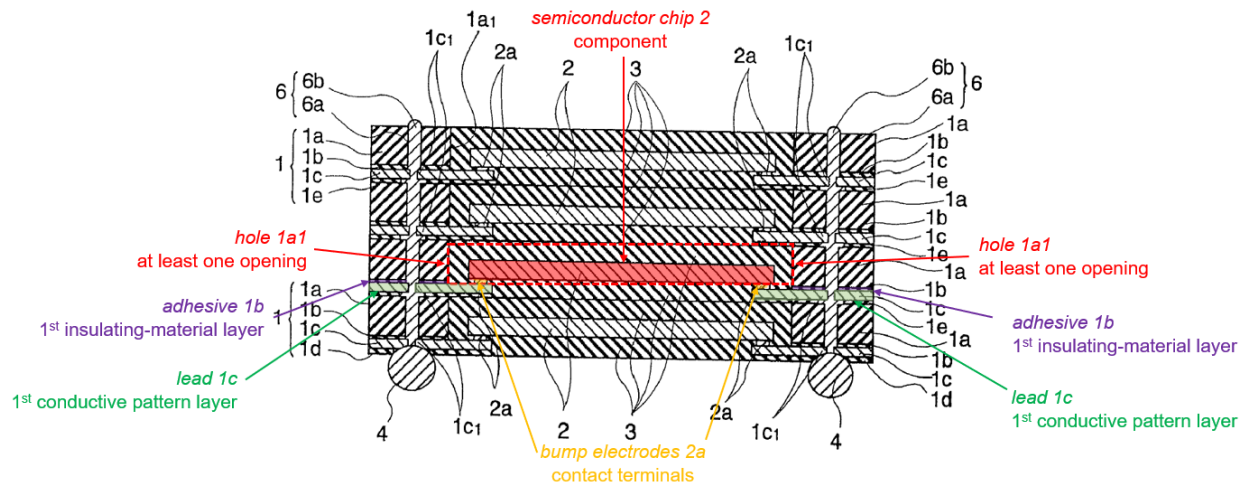
The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1c]. APPLE-1003, ¶73. For example, Tsubosaki010 discloses a semiconductor chip 2 (*component*) comprising bump electrodes 2a (*contact terminals*) being arranged at least partially within device hole 1a1 (*opening*), the bump electrodes 2a (*contact terminals*)¹⁰ electrically connected to leads 1c (*first conductive pattern layer*) of the TCP in which the chip 2 is disposed. APPLE-1005, ¶[0120]

¹⁰ The semiconductor chip 2's bonding pads 2b or the combination of bonding pads 2b and bump electrodes 2a provide alternative mappings to the claimed "*contact terminals*" and likewise render the challenged claimed features obvious. See APPLE-1005, [0068], [0072]-[0073], [0160]-[0163], FIG. 32; APPLE-1003, 73, n. 7.

(“Subsequently, place a semiconductor chip 2 within the device hole 1a1 of the tape base 1a. Then, perform position alignment between the semiconductor chip 2’s bump electrodes 2a and leads 1c. Thereafter, contact the bump electrodes 2a with leads 1c by all-at-once inner-lead bonding techniques as shown in FIG. 19.”), FIGS. 19-21; *see also id.*, ¶¶[0068] (“The distal end of each lead 1c is electrically connected via bump electrode 2a to the semiconductor chip 2. This bump electrode 2a is made for example of Au Accordingly, the bump electrode 2a and its associated lead 1c are in contact with each other by Au-Au junction or the like.”), [0062] (“chip 2 disposed within a device hole 1a1 of a tape carrier 1[] ... while causing electrodes of the semiconductor chip 2 to be externally drawn via bump electrodes 4 associated therewith”), [0069], [0072]-[0073], [0081], [0094], Abstract, FIG. 14.



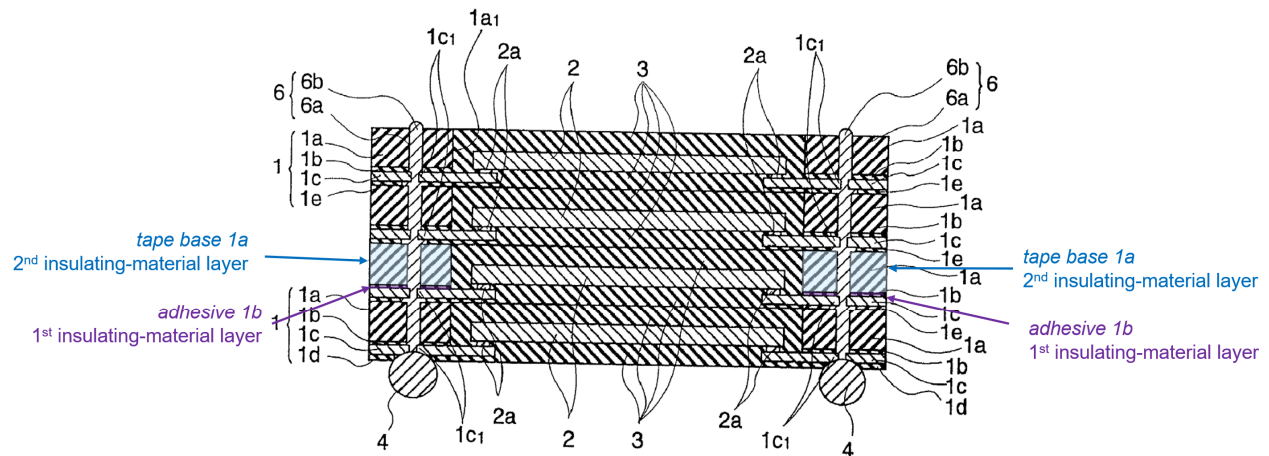
APPLE-1005, FIG. 19 (annotated)



APPLE-1005, FIG. 14 (annotated)

Element [1d]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1d]. APPLE-1003, ¶74. For example, in a first mapping, Tsubosaki010 discloses a tape base 1a that, in the combination, provides a “*second insulating-material layer*” disposed on adhesive layer 1b (*first insulating-material layer*) as claimed. APPLE-1005, ¶¶[0110], [0116], FIGS. 14, 16, 19, 21; *see also id.*, [0063], [0064] (“tape base 1a is made of polyimide resin or other suitable materials”), [0068].

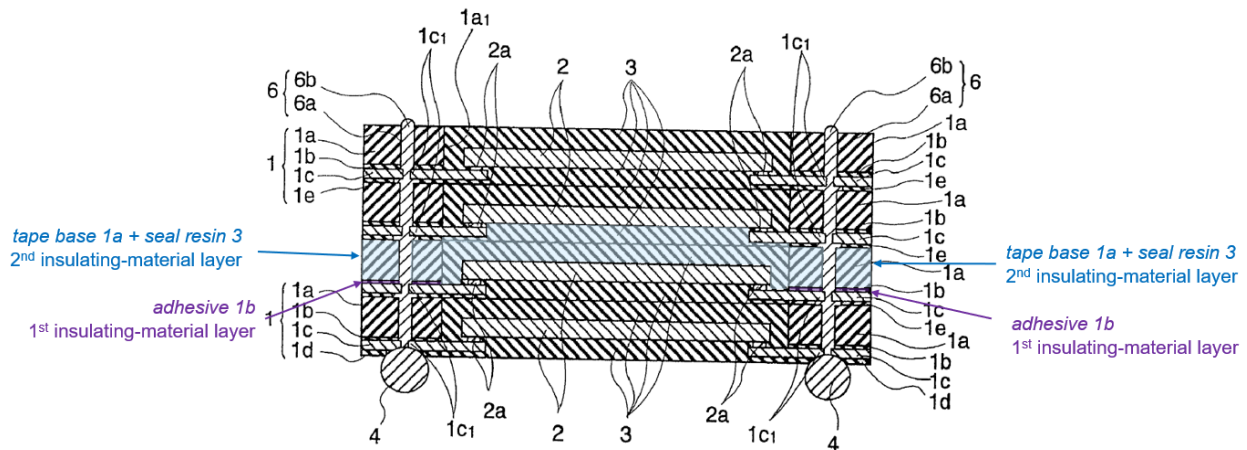


APPLE-1005, FIG. 14 (annotated) – First Mapping

Alternatively, in the combination, Tsubosaki010's tape base 1a together with seal resin 3 collectively provide a "***second insulating-material layer***" disposed on adhesive layer 1b (***first insulating-material layer***) as claimed. APPLE-1005, [0110], [0116], FIGS. 14, 16, 19, 21; *see also id.*, [0063]-[0064], [0068]. APPLE-1003, ¶75. Tsubosaki010 explains that seal resin 3 is formed by injection molding, in some examples. APPLE-1005, [0121] ("Thereafter place the tape carrier 1 mounting thereon the semiconductor chip 2 within a molding die 5 as shown in FIG. 8; then, inject a molten seal resin material, which has been fed to inside a runner 5b of the molding die 5, into a cavity as formed of the tape base 1a's device hole 1a1 and the molding die 5 through a subrunner 5c and a gate 5a as well as a seal resin injection port 1a2 of the tape base 1a."), [0065]-[0067], [0082], FIG. 8; *see also id.*, [0141]-[0154] & FIGS. 28-31 (describing a technique for "[i]ntegral molding of the seal resin 3 of the multilayer TCP" such that there are "no gaps []

formed between layers of seal resin 3”).¹¹

¹¹ Petitioner maps tape base 1a and seal resin 3 collectively to the claimed “second insulating-material layer” under Patent Owner’s broader application of the term “layer” as reflected in Patent Owner’s infringement charts in the related district court litigation. *See* APPLE-1105, 3-7, 9-11 (pointing to portions of Petitioner’s product that encompass multiple strata of materials as the claimed first and second insulating-material layers, respectively); APPLE-1003, 75, n. 8. The ’816 Patent likewise refers to a “two-layered insulation layer” made of multiple materials. APPLE-1001, 2:22-26; *see also* APPLE-1022, 14:43-45 (claim 1) (Patent Owner claiming a conductive-pattern layer that “comprises *at least two layers* of at least two different materials” in a related patent asserted against Petitioner), 6:52-59 (describing a layer comprised of “several metals as layers, accumulations, zones, or metal alloys”).



APPLE-1005, FIG. 14 (annotated) – Second Mapping

To the extent Tsubosaki010 does not expressly disclose that tape base 1a is made from an insulating material, Tsubosaki405 discloses “*insulating* adhesive films ... in the form of a tape” having an insulative tape base member made from captone or other suitable polyimide film. APPLE-1011, 7:33-41, FIG. 5; *supra*, §IV.A.2; APPLE-1005, [0064] (“tape base 1a is made of polyimide resin or other suitable materials”). It would have been obvious based on Tsubosaki405 to implement Tsubosaki010’s tape base 1a as an insulating-material for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §IV.A.3; APPLE-1003, ¶76.

A POSITA also would have understood and found it obvious to implement Tsubosaki010’s seal resin 3 as an insulating material, especially as seal resin 3 fills the space between different leads, electrodes, and semiconductor dies in the multi-layered TCP structure, and an insulating-material would be important to

electrically isolate these structures while preventing short circuits. APPLE-1003, ¶77. For example, Tsubosaki010 explains that the seal resin 3 can be made of an epoxy-based resin, which a POSITA would have understood to ordinarily be an insulating material. Tsubosaki, ¶[0076]; APPLE-1003, ¶77; *see also id.*, APPLE-1006, 250 (“since 1947, [epoxy resins] are second in usage in insulation varnishes only to polyesters”), 8 (“[e]poxies are noted for their excellent dielectric properties”), 185-186, 271, 360. At minimum, and even if the insulative properties of Tsubosaki010’s epoxy-based seal resin 3 are not expressly disclosed, a POSITA would have been motivated to use an insulating seal resin 3 in the Tsubosaki010-Tsubosaki405 combination to ensure different conductive components in the TCP structure were electrically isolated. APPLE-1003, ¶77. In this manner, the seal resin 3 and tape base 1a cooperate to form a layer that supports and electrically isolates disparate conductive components in the TCP stack of the Tsubosaki010-Tsubosaki405 combination.¹² *Id.*

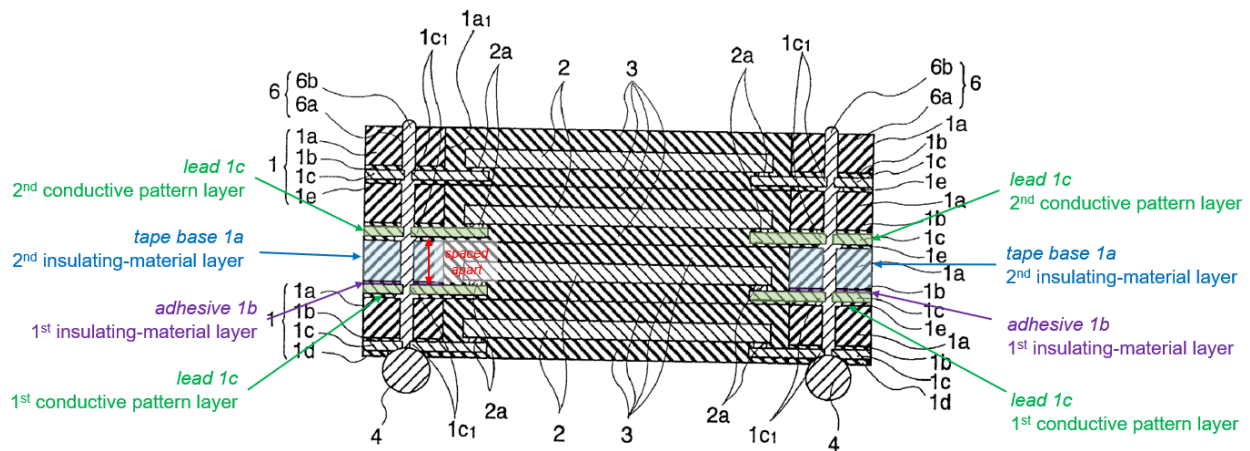
Element [1e]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1e]. APPLE-1003, ¶78. For example, Tsubosaki010 discloses that the multi-layered TCP structure includes a second set of leads 1c (*second conductive-pattern*

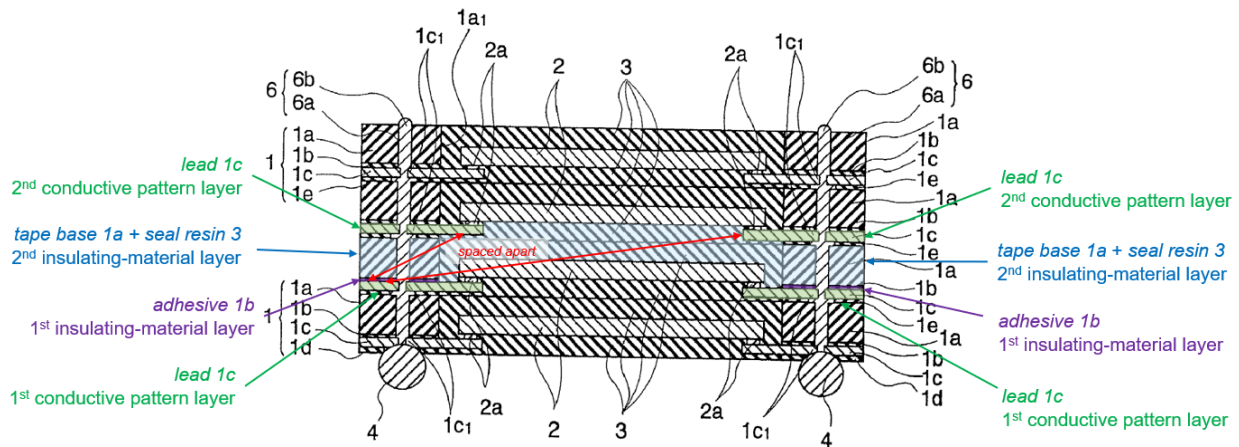
¹² *Supra*, Footnote 11.

layer) of a second tape carrier 1 (i.e., an upper tape carrier) positioned above a first tape carrier 1 (i.e., a lower tape carrier) containing a first set of leads 1c (*first conductive-pattern layer*). APPLE-1005, ¶¶[0108]-[0114], FIGS. 14, 21, 31; *see also id.*, ¶¶[0116]-[0117] (“Subsequently, *bond a Cu thin-film* for example to one surface of the tape base 1a by using the adhesive 1b attached thereto; thereafter, *pattern the Cu thin film* by etching methods or the like to thereby *form a plurality of leads 1c ...*”), [0063], [0066], [0068], FIGS. 16-17.

For both the first and second alternative mappings of the “*second insulating-material layer*” described above in connection with Element [1d], the upper set of leads 1c (*second conductive-pattern layer*) is spaced apart from the lower set of leads 1c (*first conductive-pattern layer*) by at least the adhesive layer 1b (*first insulating-material layer*) and tape base 1a (*second insulating-material layer* (first mapping)) or tape base 1a together with seal resin 3 (*second insulating-material layer* (second mapping)). APPLE-1003, ¶79.



APPLE-1005, FIG. 14 (annotated) – First Mapping



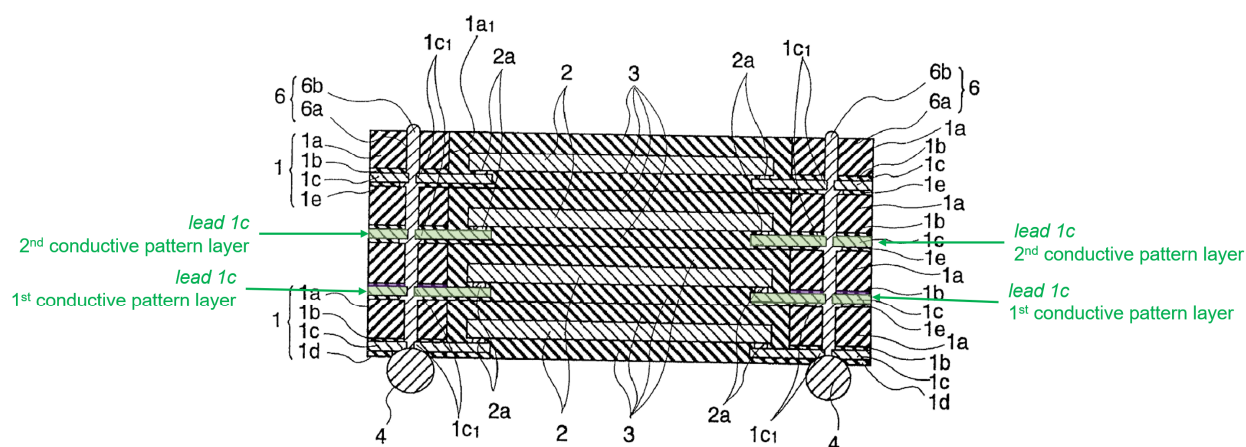
APPLE-1005, FIG. 14 (annotated) – Second Mapping

Element [1f]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [1f].

APPLE-1003, ¶80. Tsubosaki describes techniques for forming sets of leads 1c including a lower set (*first conductive-pattern layer*) and an upper set (*second conductive-pattern layer*) in the multi-layered TCP structure that are each substantially planar. *See, e.g.*, APPLE-1005, [0114], [0118], FIGS. 14-21. The

substantially planar leads 1c are shown in FIG. 14, for example:



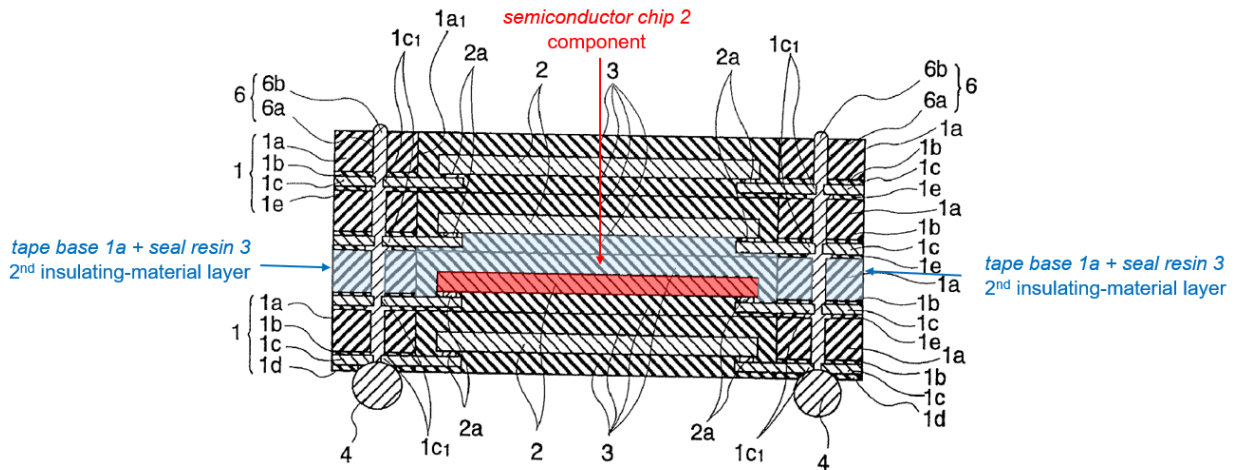
APPLE-1005, FIG. 14 (annotated)

That leads 1c of the first and second conductive-pattern layers are substantially planar also would have been obvious to a POSITA based on Tsubosaki010's descriptions of how the leads 1c are formed. APPLE-1003, ¶81. For instance, Tsubosaki010 discloses that tape base 1a with its hole 1a1 have a "planar rectangular shape" and that the copper (or other suitable metal) film that is patterned to form leads 1c is bonded to the tape base 1a via adhesive 1b. Tsubosaki, ¶¶[0064], [0116]-[0117]. Tsubosaki010 also describes a "stress neutral plane A [that] is the plane parallel to the principal surface of the semiconductor chip 2, which is a specific plane on which the stress applied to the semiconductor chip 2 becomes neutral in the direction along the thickness of the semiconductor chip 2." APPLE-1005, ¶[0075], FIG. 1; *see also id.*, ¶¶[0074], [0088], [0094]-[0095], [0098]-[0099], [0106] (referring to stress neutral planes A and A1). Even

where portions of the tape carrier 1 may be subjected to stress, Tsubosaki010 describes techniques to mitigate resulting deformation. For example, Tsubosaki010 teaches that “[i]n cases where the stress neutral plane A1 of the semiconductor chip 2 and the stress neutral plane A of the TCP as a whole are little deviated from each other due to any possible thickness differences among respective constituent parts or components of the TCP, such deviation is corrected by adjustment of the bending amount of the lead 1 c.” APPLE-1005, ¶[0098].

Claim [2]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [2]. APPLE-1003, ¶82. For example, Tsubosaki010 discloses that seal resin 3 (*i.e.*, a component of the *second insulating-material layer* according to the second mapping discussed above in Element [1d]) directly contacts the semiconductor chip 2 (*component*). APPLE-1005, ¶[0120]-[0123] (“both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3”), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d]; APPLE-1003, ¶82.

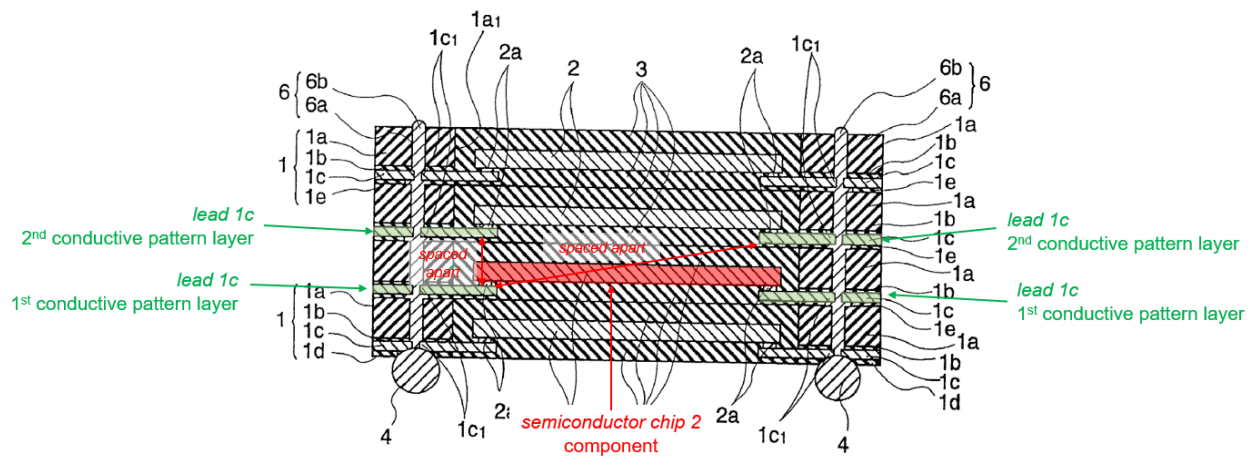


APPLE-1005, FIG. 14 (annotated) – Second Mapping

Claim [3]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [3].

APPLE-1003, ¶83. For example, Tsubosaki010 discloses that the second (upper) set of leads 1c (*second conductive-pattern layer*) is spaced apart from the first (lower) set of leads 1c (*first conductive-pattern layer*) by the semiconductor chip 2 (*component*). APPLE-1005, ¶¶[0108]-[0126], FIG. 14; APPLE-1003, ¶83.

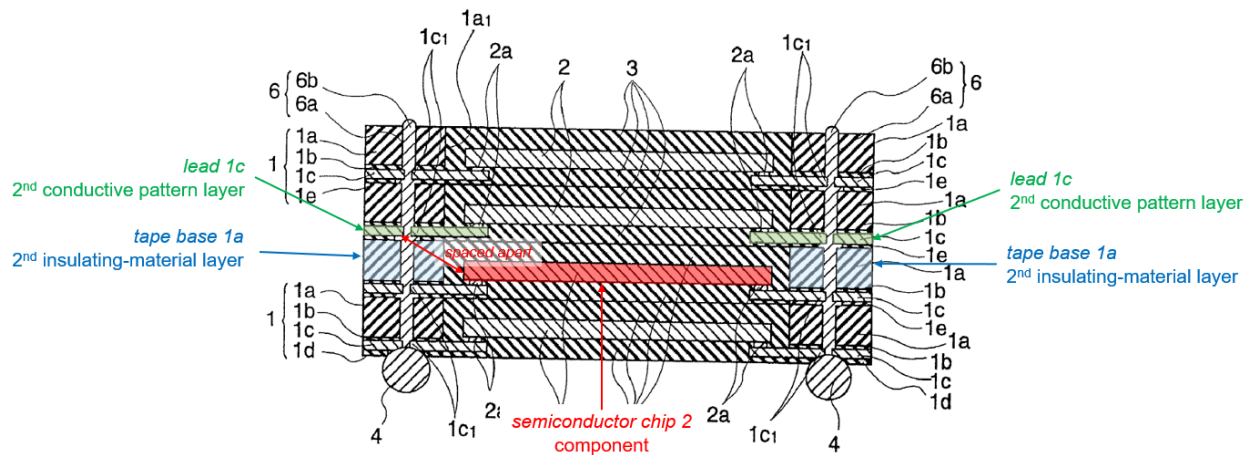


APPLE-1005, FIG. 14 (annotated)

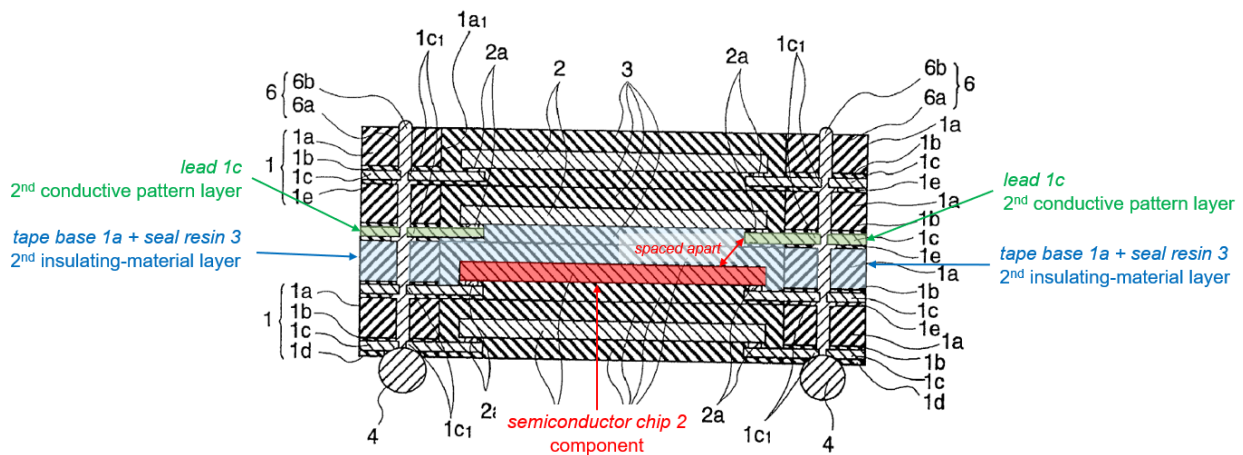
Claim [4]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [4].

APPLE-1003, ¶84. For example, Tsubosaki010 discloses that the second (upper) set of leads 1c (*second conductive-pattern layer*) is spaced apart from the semiconductor chip 2 (*component*) by the tape base 1a or the tape base 1a together with seal resin 3 (*second insulating-material layer*). See APPLE-1005, ¶¶[0120]-[0123] (“both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3”), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d]; *generally id.*, APPLE-1005, [0108]-[0126], FIGS. 14-21; APPLE-1003, ¶84.



APPLE-1005, FIG. 14 (annotated) – First Mapping

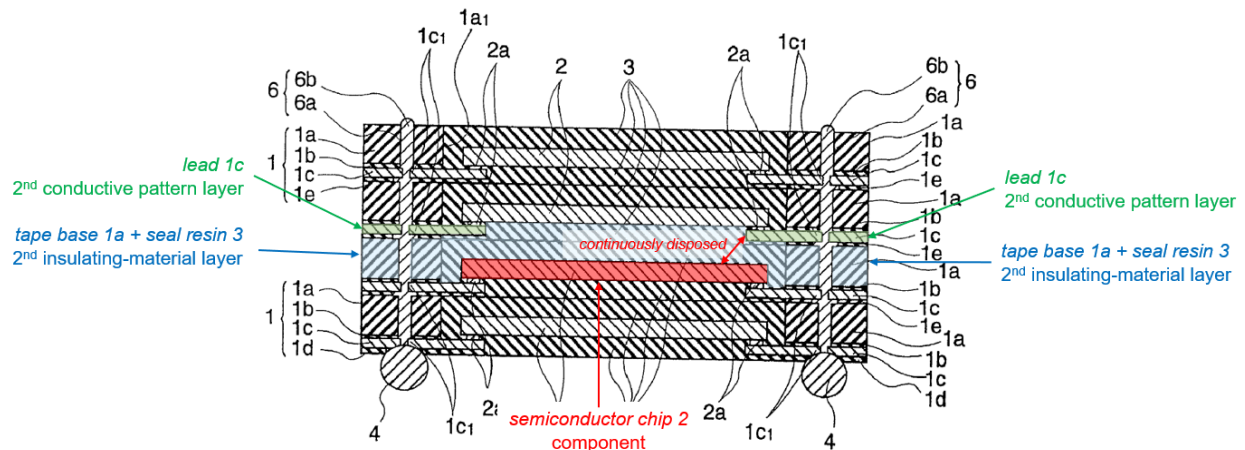


APPLE-1005, FIG. 14 (annotated) – Second Mapping

Claim [5]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [5].

APPLE-1003, ¶85. For example, Tsubosaki010 discloses that seal resin 3 (*i.e.*, a component of the **second insulating-material layer** according to the second mapping discussed above in Element [1d]) is continuously disposed between the upper set of leads 1c (**second conductive-pattern layer**) and the semiconductor chip 2 (**component**). APPLE-1005, ¶[0120]-[0123] (“both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3”), [0140] (“no gaps are formed between layers of seal resin 3”), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d]; APPLE-1003, ¶85; *generally* APPLE-1005, [0108]-[0126], FIGS. 14-21 & [0139]-[0154], FIGS. 27-30.

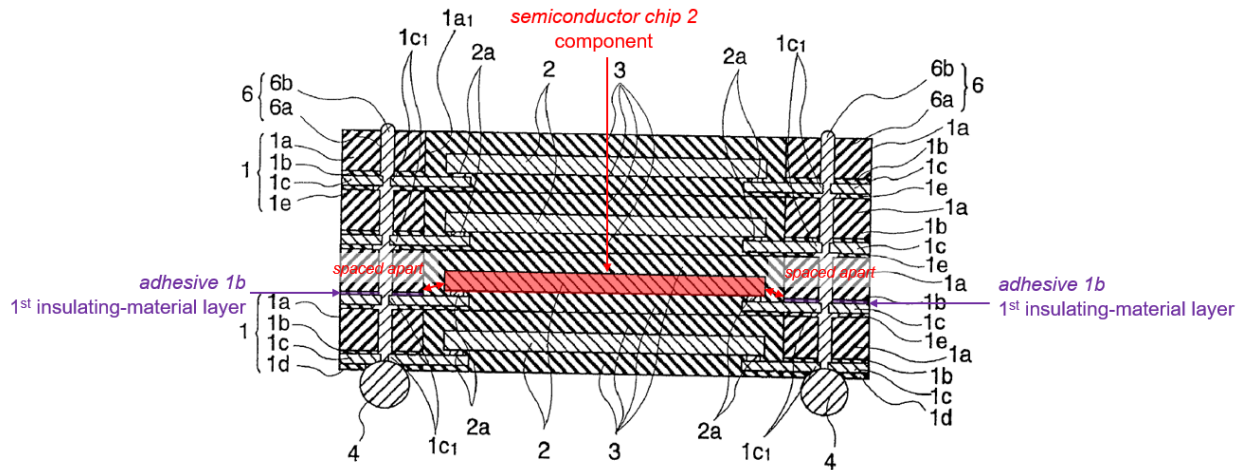


APPLE-1005, FIG. 14 (annotated) – Second Mapping

Claim [6]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [6].

APPLE-1003, ¶86. For example, Tsubosaki010 discloses that the adhesive layer 1b (*first insulating-material layer*) is spaced apart from the semiconductor chip 2 (*component*). Tsubosaki010's seal resin 3 surrounds the semiconductor chip 2 thus separating the semiconductor chip 2 from the adhesive layer 1b. APPLE-1005, ¶¶[0065], [0082]-[0085]; *see also id.*, ¶[0092] (“the thickness D1 of the seal resin 3 [can] be equal to the thickness D2 of tape carrier 1”), [0063], [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated)

Claim [7]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [7].

APPLE-1003, ¶87. As discussed above, in the Tsubosaki010-Tsubosaki405 combination, adhesive layer 1b provides a “*first insulating-material layer*,” tape base 1a provides a “*second insulating-material layer*” according to a first mapping, and tape base 1a together with seal resin 3 provides a “*second insulating-material layer*” according to a second mapping. *Supra*, Element [1a], [1d]. In the combination, Tsubosaki405 demonstrates that it would have been obvious to implement adhesive layer 1b as an adhesive film such as polyetheramideimide and to implement tape base 1a as another suitable polyimide film such as captone that lacks the same adhesive properties. APPLE-1011, 7:32-41, FIG. 5; *supra*, §§V.A.2-3; APPLE-1003, ¶87. Tsubosaki010 further discloses that seal resin 3 can be an epoxy-based resin. APPLE-1005, [0076]. Accordingly,

in the combination, the first insulating-material layer comprises a different material (e.g., polyetheramideimide or another adhesive film) than a material of the second insulating-material layer (e.g., captone or another non-adhesive polyimide film and/or epoxy-based resin). APPLE-1003, ¶87.

Element [8pre]

Supra, Element [1pre]; APPLE-1003, ¶88.

Element [8a]

Supra, Element [1a]; APPLE-1003, ¶89.

Element [8b]

Supra, Element [1b]; APPLE-1003, ¶90.

Element [8c]

Supra, Element [1c]; APPLE-1003, ¶91.

Element [8d]

Supra, Element [1d]; APPLE-1003, ¶92.

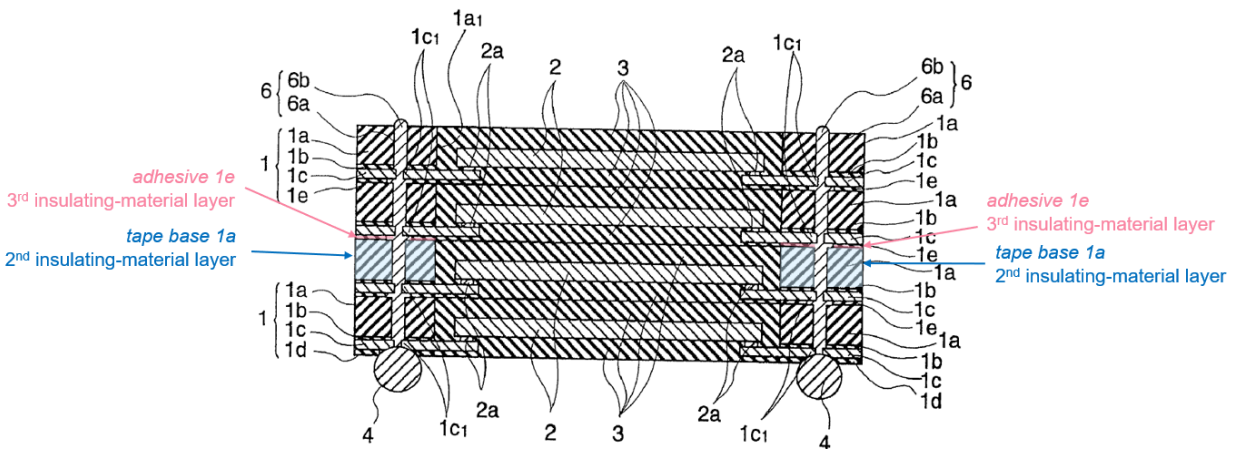
Element [8e]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [8e]. APPLE-1003, ¶93. For example, Tsubosaki010 discloses an adhesive layer 1e (*third insulating-material layer*) disposed on the tape base 1a (*second*

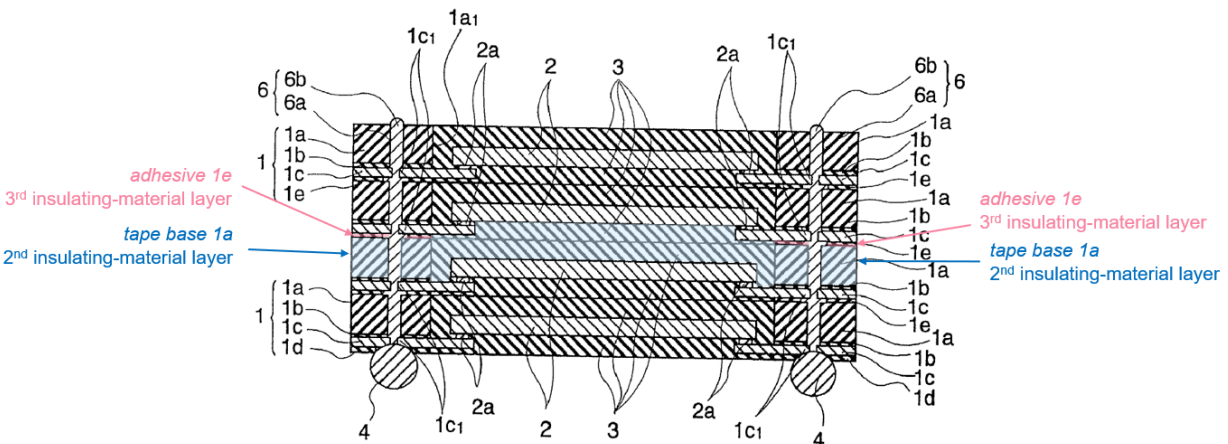
insulating-material layer).¹³ APPLE-1005, [0111] (“Adjacent ones of the laminated unitary TCPs are bonded together by adhesive 1e. This adhesive 1e is a member for constituting part of the unitary TCP’s tape carrier 1; for example, it is made of a thermally deformable polyimide resin material.”), [0118] (“Thereafter, as shown in FIG. 18, provide adhesive 1e made of for example thermally deformable polyimide resin on the side of the copper thin film; then, remove part of such adhesive 1e so that the bump underlayer pattern 1c1 portion of lead 1c and a projected inner lead portion 1c are exposed.”), [0125] (“Thereafter, use the adhesive 1e sandwiched between adjacent ones of the unitary TCPs to contact the unitary TCPs together by thermo-compression methods thereby forming the intended multilayer TCP. To make long story short, as multiple unitary TCPs are stacked or laminated on one another by use of the adhesive 1e that is formed during fabrication of a unitary TCP, it becomes possible to manufacture the multilayer TCP without increasing production process steps required.”), [0143]

¹³ Tape base 1a corresponds to the “second insulating-material layer” according to a first mapping of Tsubosaki010’s structures to the claimed features. Tape base 1a is a component of the “second insulating-material layer” along with seal resin 3 according to a second mapping of Tsubosaki010’s structures to the claimed features. *Supra*, Element [1d]; APPLE-1003, 93, n. 10.

(“after lamination of a plurality of tape carriers 1 each mounting thereon its semiconductor chip 2 as shown in FIG. 28, use the adhesive 1 e between tape carriers 1”), [0130], FIGS. 14-21, 27-31.



APPLE-1005, FIG. 14 (annotated) – First Mapping



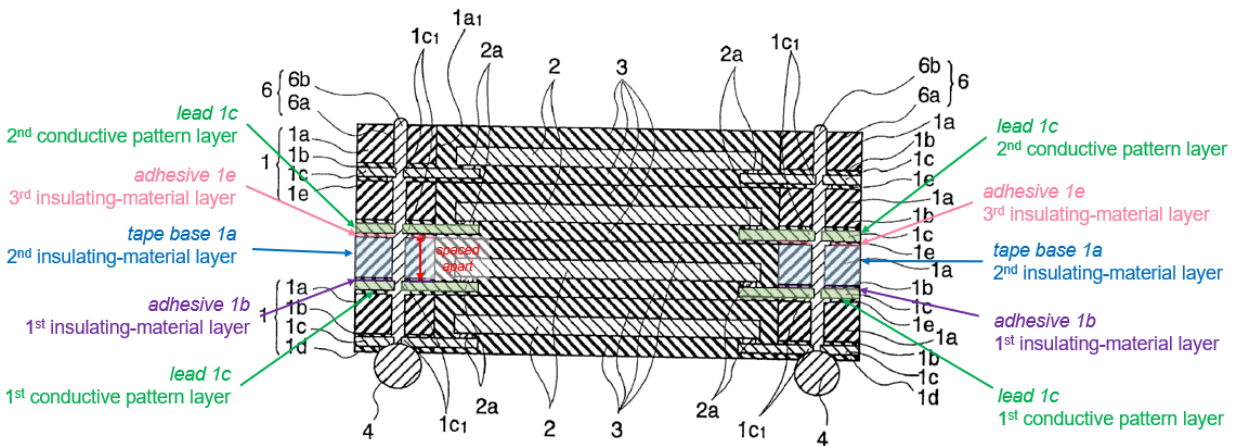
APPLE-1005, FIG. 14 (annotated) – Second Mapping

Tsubosaki010 teaches that adhesive 1e can be made of a “thermally deformable polyimide resin material.” APPLE-1005, ¶¶[0111], [0118]; APPLE-1003, ¶94. To the extent Tsubosaki010 does not expressly disclose that adhesive

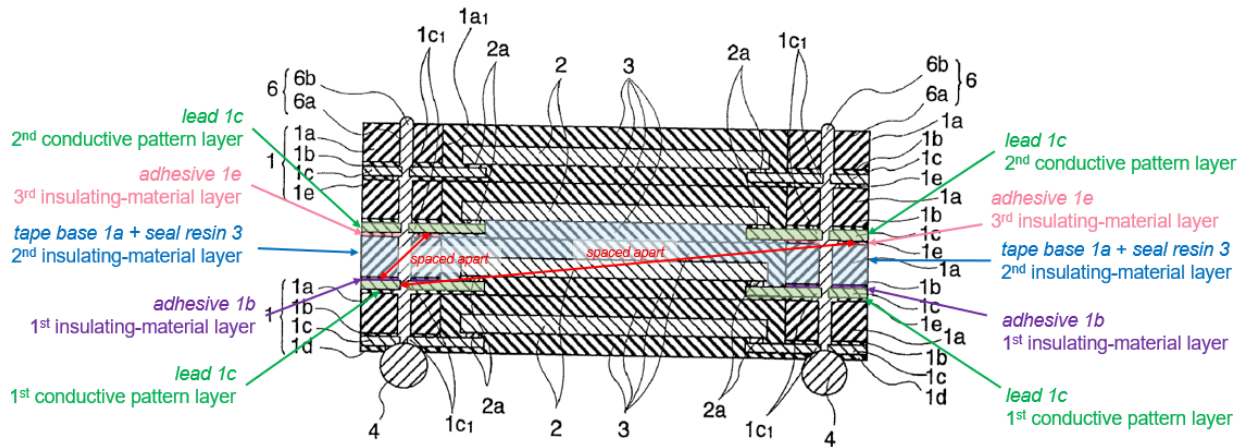
layer 1e is an insulating material, Tsubosaki405 discloses “*insulating* adhesive films ... in the form of a tape” having insulative adhesive such as polyetheramideimide bonded between a lead and a tape base member in a semiconductor package similar to Tsubosaki010’s adhesive layer 1e. APPLE-1011, 7:33-41, FIG. 5; *supra*, §IV.A.2. It would have been obvious based on Tsubosaki405 to implement Tsubosaki010’s adhesive layer 1e as an insulating-material layer for each of the reasons described above in the overview of the Tsubosaki010-Tsubosaki405 combination. *Supra*, §IV.A.3; APPLE-1003, ¶94.

Element [8f]

The Tsubosaki010-Tsubosaki405 combination renders obvious Element [8f]. APPLE-1003, ¶95. As described above in connection with Element [1e], Tsubosaki010 discloses that an upper set of leads 1c (*second conductive-pattern layer*) in the multi-layered TCP structure is spaced apart from a lower set of leads 1c (*first conductive pattern layer*) by at least the adhesive layer 1b (*first insulating-material layer*) and the tape base 1a or tape base 1a in connection with seal resin 3 (*second insulating-material layer*). *Supra*, Element [1e]. Tsubosaki010 further discloses that the upper set of leads 1c (*second conductive-pattern layer*) is spaced apart from the lower set of leads 1c (*first conductive-pattern layer*) additionally by the adhesive layer 1e (*third insulating-material layer*). APPLE-1005, [0108]-[0126], [0143], FIGS. 14-21, 27-31.



APPLE-1005, FIG. 14 (annotated) – First Mapping



APPLE-1005, FIG. 14 (annotated) – Second Mapping

Element [8g]

Supra, Element [1f]; APPLE-1003, ¶96.

Claim [9]

Supra, Claim [2]; APPLE-1003, ¶97.

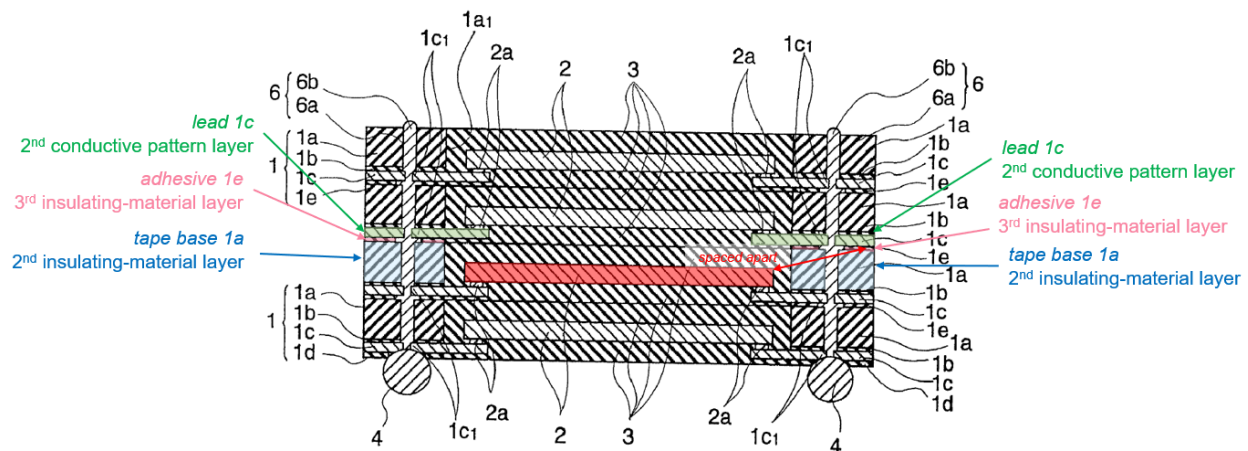
Claim [10]

Supra, Claim [3]; APPLE-1003, ¶98.

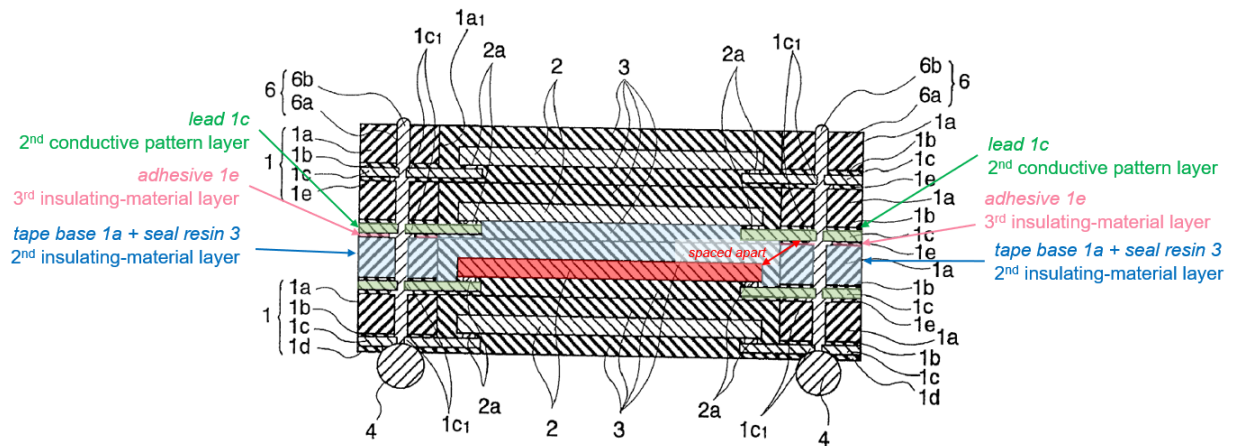
Claim [11]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [11].

APPLE-1003, ¶99. For example, Tsubosaki010 discloses that the upper set of leads 1c (*second conductive-pattern layer*) is spaced apart from the semiconductor chip 2 (*component*) by (i) the tape base 1a or the tape base 1a together with seal resin 3 (*second insulating-material layer*) and (ii) the adhesive layer 1e (*third insulating-material layer*). See APPLE-1005, ¶¶[0120]-[0123] (“both of the principal surface and back surface of the semiconductor chip 2 are coated with the seal resin 3”), [0011], [0062]-[0063], [0065]-[0066], FIG. 14; *supra*, Element [1d] and Claim [4]; APPLE-1003, ¶99; *generally id.*, [0108]-[0126], FIGS. 14-21; APPLE-1003, ¶99.



APPLE-1005, FIG. 14 (annotated) – First Mapping



APPLE-1005, FIG. 14 (annotated) – Second Mapping

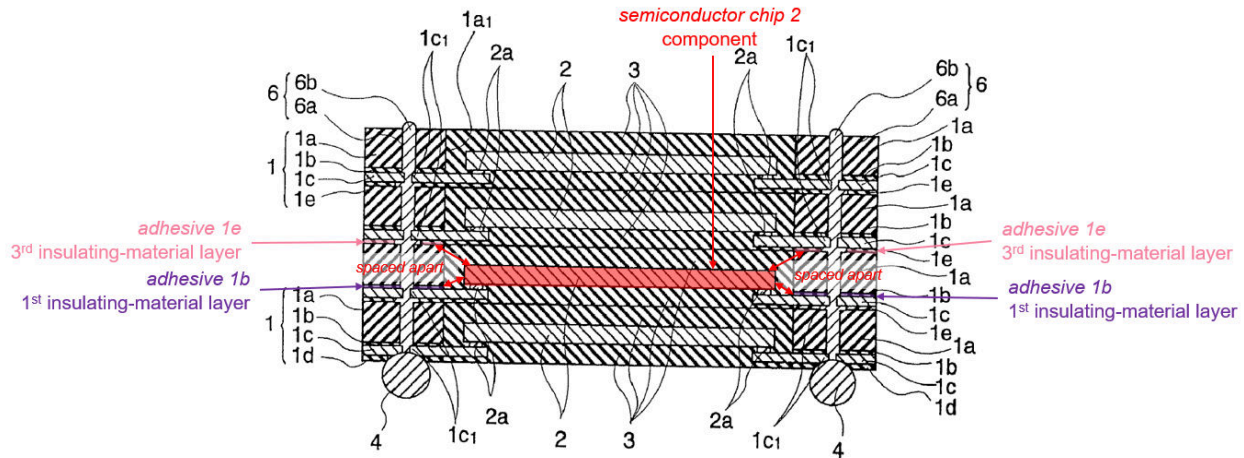
Claim [12]

Supra, Claim [5]; APPLE-1003, ¶100.

Claim [13]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [13].

APPLE-1003, ¶101. For example, Tsubosaki010 discloses that the adhesive layer 1b (*first insulating-material layer*) and the adhesive layer 1e (*third insulating-material layer*) are both spaced apart from the semiconductor chip 2 (*component*). Tsubosaki010's seal resin 3 surrounds the semiconductor chip 2 thus separating the semiconductor chip 2 from the adhesive layers 1b and 1e. APPLE-1005, ¶¶[0065], [0082]-[0085]; *see also id.*, ¶[0092] (“the thickness D1 of the seal resin 3 [can] be equal to the thickness D2 of tape carrier 1”), [0063], [0108]-[0126], FIGS. 14-21.



APPLE-1005, FIG. 14 (annotated)

Claim [14]

The Tsubosaki010-Tsubosaki405 combination renders obvious Claim [14].

APPLE-1003, ¶102. As discussed above, in the Tsubosaki010-Tsubosaki405 combination, adhesive layer 1b provides a “*first insulating-material layer*,” tape base 1a provides a “*second insulating-material layer*” according to a first mapping, tape base 1a together with seal resin 3 provides a “*second insulating-material layer*” according to a second mapping, and adhesive layer 1e provides a “*third insulating-material layer*.” *Supra*, Elements [1a], [1d], [8e]. In the combination, Tsubosaki405 renders obvious implementing adhesive layers 1b and 1e with an adhesive film such as polyetheramideimide and implementing tape base 1a as another suitable polyimide film such as captone that lacks similar adhesive properties. APPLE-1011, 7:32-41, FIG. 5; *supra*, §§V.A.2-3; *see also* APPLE-1005, [0111] (adhesive 1e “made of a thermally deformable polyimide resin

material”); APPLE-1003, ¶102. Tsubosaki010 further discloses that seal resin 3 can be an epoxy-based resin. APPLE-1005, [0076].

Accordingly, in the combination, the first insulating-material layer 1b and third-insulating material layer 1e comprise a first material (e.g., polyetheramideimide or another adhesive film) that is different than a second material of the second insulating-material layer from tape base 1a or seal resin 3 (e.g., captone or another non-adhesive polyimide film and/or epoxy-based resin). APPLE-1003, ¶103. Tsubosaki405 also demonstrates the known option of using the same adhesive material on either side of a tape base member, and it would have been obvious to implement Tsubosaki010’s adhesive layers 1b and 1e to include at least a same first material as taught in Tsubosaki405 to simplify the construction and minimize the number of different adhesives used in constructing the multi-layered TCP. APPLE-1011, 7:32-41, FIG. 5; APPLE-1003, ¶103. A POSITA would have reasonably expected success using a same thermally deformable polyimide resin or other suitable insulating material for both adhesives 1b and 1e given that both adhesive layers perform a similar function of binding the tape base member 1a to a lead 1c in the multi-layered TCP structure. APPLE-1003, ¶103.

B. GROUND 1B: Tsubosaki010 Renders Obvious Claims 1-14

As discussed in Ground 1A, a POSITA would have found it obvious based on Tsubosaki405 to implement Tsubosaki010’s tape base 1a and adhesive layers

1b and 1e with insulating materials. *Supra*, §IV.A.3. But the teachings of Tsubosaki405 would not have been necessary to be applied in combination for a POSITA to have been prompted to use insulating materials for each of tape base 1a and adhesive layers 1b and 1e in Tsubosaki010's device. APPLE-1003, ¶104. The general background knowledge of a POSITA also would have rendered the use of insulating materials for these components obvious, especially as the use of insulating materials for adhesives and tape bases was well known before the Critical Date and polyimide materials that Tsubosaki010 discloses for the tape base and adhesive are commonly insulating materials. *Id.* (citing corroborating exhibits APPLE-1011, 7:32-41, 6:18-22, FIG. 5; APPLE-1006, 8 (“[e]poxies are noted for their excellent dielectric properties”); APPLE-1005, [0064], [0111], [0118]; *see also id.*, APPLE-1017, 81, Abstract; APPLE-1018, Abstract; APPLE-1019, 239. A POSITA would have been motivated and would have reasonably expected success using insulating materials for the tape base 1a and adhesives 1b, 1e for substantially the same reasons described above in §IV.A.3; APPLE-1003, ¶104. The resulting version of Tsubosaki010's device would have provided all elements of claims 1-14 as described above in Ground 1A. *Id.*

**C. GROUND 2: Oya in View of Shugg Renders Obvious
Claims 1, 3-4, 6-8, 10-11, and 13-14**

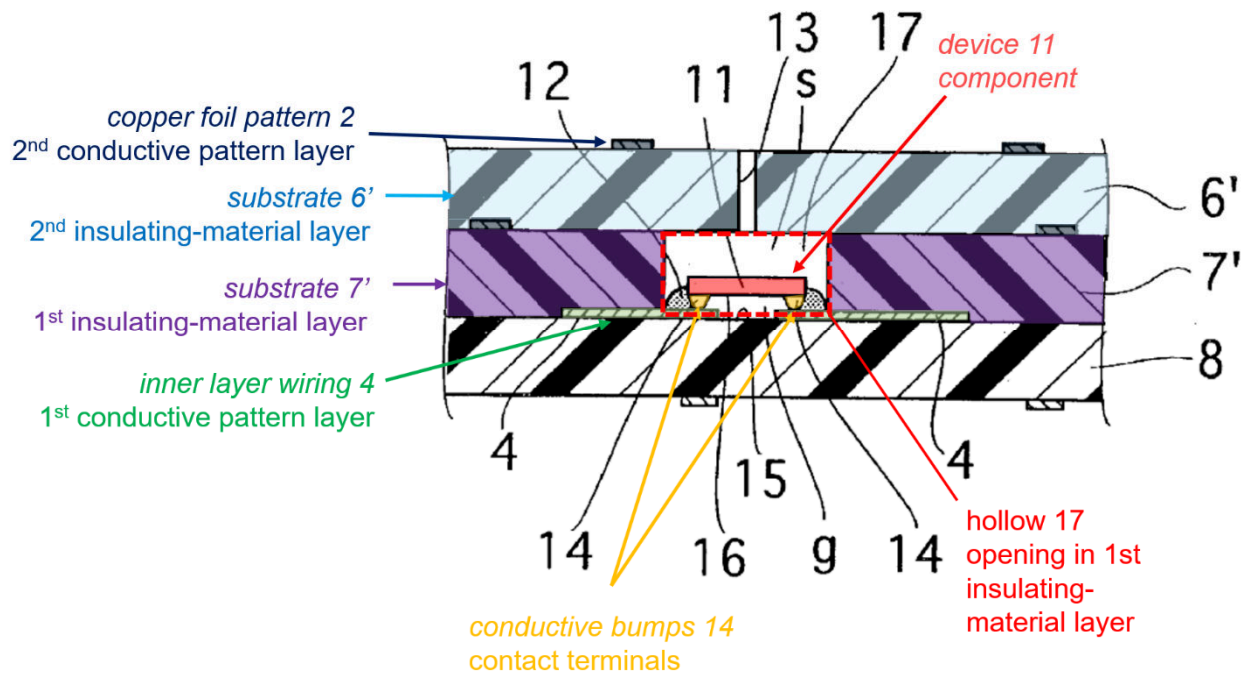
1. Overview of Oya

Oya discloses a multi-layered printed circuit board (“PCB”) 1 adapted to house a semiconductor component having a “functional surface” such as a surface acoustic wave (SAW) device or a micro electromechanical system (MEMS).

APPLE-1004, Abstract, ¶¶[0005], [0012], [0042]-[0043], [0070], FIG. 1.

According to the Abstract, Oya’s PCB “is capable of air-tightly sealing a function surface of a device and of preventing excessive stress from acting on the device itself” *Id.*; APPLE-1003, ¶105.

In an embodiment illustrated by FIG. 7, semiconductor device 11 is disposed within a hollow 17 of a PCB substrate 7’. APPLE-1004, ¶¶[0067]-[0071]; APPLE-1003, ¶106. Another substrate 6’ is attached to a top surface of substrate 7’, while a substrate 8 is attached to a bottom surface of substrate 7’. *Id.*, ¶[0067]. “[D]evice 11 [is first disposed] on the substrate 8.” *Id.* 67. “[S]ubstrate 7’ having a through-hole formed therein may be stacked [on the substrate 8].” *Id.* The “substrate 6’ may be stacked further [on the substrate 7] so as to cover the through-hole so as to form the hollow 17.” *Id.*; APPLE-1003, ¶106.



APPLE-1004, FIG. 7 (annotated)

Oya's PCB 1 includes two outer layer wirings 2 and 3 and two inner layer wirings 4 and 5. APPLE-1004, ¶[0039], FIGS. 1, 7; APPLE-1003, ¶107. As shown in FIG. 7, the inner layer wiring 4 is disposed between the substrate 8 and substrate 7', and the inner layer wiring 5 is shown between substrate 7' and substrate 6'. In one implementation, Oya teaches that outer layer wirings 2, 3 can be disposed on surfaces of the substrate 6' and substrate 8, as illustrated in FIGS. 7. A functional surface 16 of the device 11 is mounted face down in the hollow 17. *Id.*, ¶[0040]; APPLE-1003, ¶107. Oya's device 11 is electrically connected to the inner layer wiring 4 by a set of conductive bumps 14. APPLE-1004, ¶[0040], [0048], [0051], [0055]. APPLE-1003, ¶108.

2. Overview of Shugg

Shugg's Handbook of Electrical and Electronic Insulating Materials, published in 1995, describes various "properties, uses, standards, and specifications of electrical insulating materials" commonly used in manufacturing electronics. *See* APPLE-1006, xxi. Among the materials disclosed as suitable for use in electronics are prepregs, epoxy resins, and polyimide. *See, e.g.*, APPLE-1006, 144, 151-152, 199-200, 205-208, 228-229, 244, 269-270, 290-291 (polyimide), 126-127 (epoxy resins), 217-276, 301-304, 306-308 (prepregs); APPLE-1003, ¶109.

3. Predictable Combination of Oya and Shugg

Oya discloses that its substrates, e.g., substrates 6, 7', and 8', can be made from an epoxy resin and can include "prepreg" material (*e.g.*, a "pre-impregnated" composite material that includes a fabric). APPLE-1004, ¶¶[0051], [0060]. Shugg demonstrates that epoxy resin and prepregs were commonly implemented as insulating materials in electronic devices. APPLE-1006, 144, 151-152, 199-200, 205-208, 244, 269-270, 290-291, ("epoxy/epoxies") 301-304, 306-308 ("prepreg"). To the extent Oya does not expressly disclose that the substrate layers of its printed circuit board are made from insulating materials, it would have been obvious to use insulating materials for this purpose based on the teachings of Shugg. APPLE-1003, ¶110; *see* APPLE-1006, 126-127 (epoxy resins); *id.*, 217-276 (prepregs).

Multiple reasons would have prompted a POSITA to combine Oya and Shugg to implement insulating substrate layers in Oya's PCB. APPLE-1003, ¶110.

First, a POSITA would have used insulators as the substrates to ensure the wiring and conductive leads disposed between different layers of the substrates are electrically isolated. APPLE-1003, ¶111. The conductive pathways in Oya's device would predictably carry power and/or information signals to and from various electrical components. APPLE-1003, ¶111. Insulators, having a higher resistivity to the flow of electrical current, are known to be useful in confining electrical signals to the electrical conductors. APPLE-1003, ¶111. By confining the signals to their respective conductive pathways, the insulators would advantageously isolate conductive elements, thus facilitating the proper routing of the electrical signals. APPLE-1003, ¶111. A POSITA would have recognized that failing to separate signals would diminish the performance of an electrical device. APPLE-1003, ¶111; *see also* APPLE-1008, 2, 78, 104, 110, 112, 117, 120, 122, 126, 155, 183 (discussing prepregs); *see also id.*, 28, 78, 107, 115, 127, 129, 146, 148, 159, 179 (discussing epoxide resin or epoxy resin). For example, failing to separate electrical signals within a circuit can produce short circuit, cross-talk, reduce signal quality, cause overheating, and performance degradation. APPLE-1003, ¶111. An insulator would have been recognized by a POSITA as a well-known solution to these well-known problems. APPLE-1003, ¶111.

Second, a POSITA would have been prompted to implement the substrate layers in Oya's PCB with insulating materials to reduce signal loss in the conductive layers of the multi-layered semiconductor. APPLE-1003, ¶112. Loss of signal quality is a known problem in electronic device. APPLE-1003, ¶112. Insulators are known to have a higher resistivity to the flow of electrical current than electrical conductors. APPLE-1003, ¶112. Surrounding electrical conductors with an insulator, having higher resistivity than air or other electrical conductors, facilitates the transmission of the signal along the electrical conductor. APPLE-1003, ¶112.

Third, a POSITA would have been prompted to implement the substrate layers in Oya's PCB with insulating materials to reduce the risk of known hazards that can be caused by conductors that touch or are too close to one another. APPLE-1003, ¶113. A POSITA would have understood that electrical conductors that are inadvertently contacted or electrically coupled can produce cross-talk, short circuits, and electrical hazards. APPLE-1003, ¶113. Insulators would have been known to the POSITA for their ability to form barriers between energized parts (e.g., electrical conductors) of an electric circuit within a semiconductor device. APPLE-1003, ¶113. A POSITA would have known that insulators were useful for confining the flow of current along a desired path. APPLE-1003, ¶113.

Fourth, a POSITA would have found the use of insulating materials for

Oya's substrates to be obvious to try. APPLE-1003, ¶114. There exist a finite number of classes of materials that could be used to implement the substrates—namely, either insulating materials or conductive materials—and a POSITA would have had ample reason to try insulating materials for each of the reasons described herein (e.g., to promote electrical isolation between electrical conductors within the PCB). APPLE-1003, ¶114.

Fifth, implementing Oya's substrates with insulating materials would have been obvious as a predictable application of known insulating materials as taught by Shugg to known structures as taught by Oya to achieve merely predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious); APPLE-1003, ¶115.

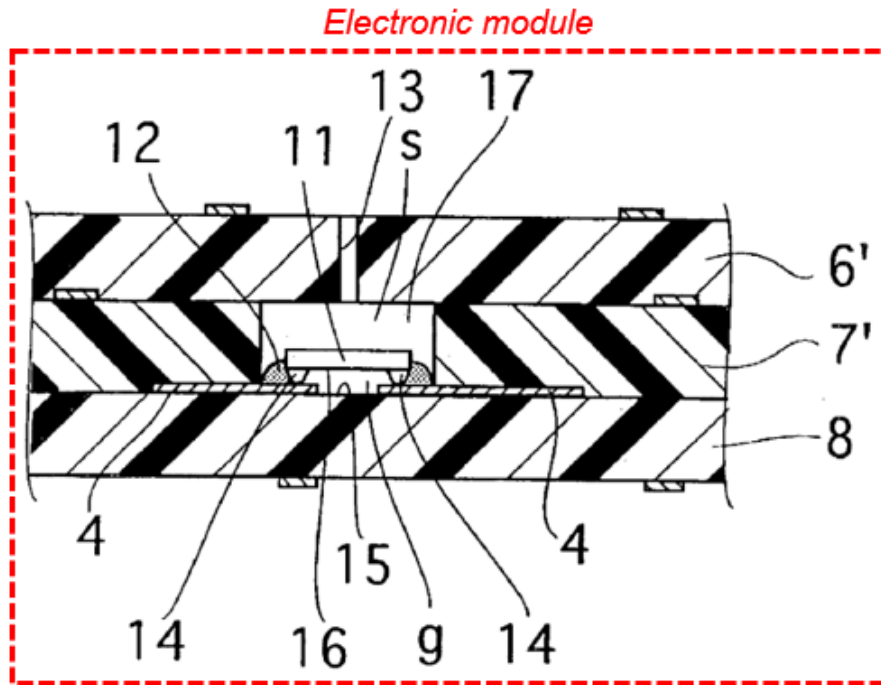
A POSITA would have had a reasonable expectation of success implementing Oya's substrate layers with insulating materials, especially since insulating substrate materials were well known before the '816 Patent. APPLE-1003, ¶116; *see also* APPLE-1004, ¶[0051]; APPLE-1008, 61; APPLE-1009, 78, 79-81. Oya and Shugg are both also analogous art in that they are both in the same field of endeavor and/or reasonably pertinent to the problem faced by the inventors of the '816 Patent. For example, like the '816 Patent, Oya and Shugg both describe techniques for manufacturing and packaging electronic modules. APPLE-

1003, ¶116; APPLE-1001, 1:17-39; *supra*, §§IV.B.1-2; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

4. Application to Challenged Claims

Element [1pre]

To the extent the preamble is a limitation, the Oya-Shugg combination renders it obvious. APPLE-1003, ¶117. For example, Oya discloses a printed circuit board (PCB) 1 that provides an “*electronic module*” as recited in [1pre]. APPLE-1004, ¶[0003] (“a *printed circuit board* having a structure in which a device is embedded in a cavity in a wiring board and a fabrication process thereof”); *see also id.*, Abstract, [0013]-[0015], [0024], FIG. 7; *cf.* APPLE-1001, 1:23-27 (’816 Patent similarly explaining that an “electronic module ... can be a module like a circuit board, which includes several components, which are connected to each other electrically”); APPLE-1003, ¶117.



APPLE-1004, FIG. 7 (annotated)

Element [1a]

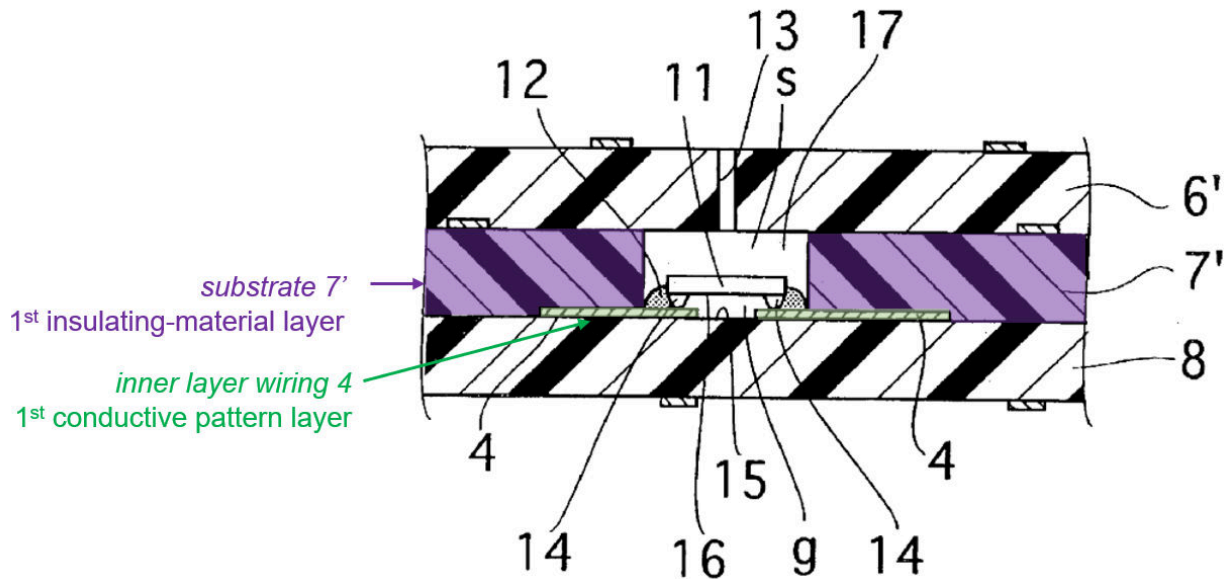
The Oya-Shugg combination renders Element [1a] obvious. APPLE-1003, ¶118. For example, in the combination, Oya discloses an inner layer wiring 4 that corresponds to a “*first conductive pattern layer*” and a substrate 7’ that corresponds to a “*first insulating-material layer*” as claimed. APPLE-1004, FIG. 7. As shown in FIG. 7 (reproduced and annotated below), Oya’s substrate 7’ is arranged on at least one surface (e.g., a top surface) of the inner wiring layer 4. APPLE-1004, ¶[0067] (“As shown in FIG. 7, after mounting the device 11 on the substrate 8, a substrate 7 having a through-hole formed therein may be stacked thereon ...”), [0066] (“Alternatively... after preparing a multilayer printed circuit

board having a preliminarily provided recess, a device may be mounted in the recess, ...”¹⁴; *see also id.*, [0045]-[0047] & FIG. 2 (describing an etching process for forming wiring layer 4); APPLE-1003, ¶¶119-120.

Oya teaches that the substrates of the wiring board, e.g., substrate 7’, can be “prepreg” and “composed of an epoxy resin or the like.” APPLE-1004, ¶¶[0045], [0051]. For the reasons described above, it would have been obvious to a POSITA based on Shugg to implement Oya’s substrates including substrate 7’ as an insulator such that substrate layer 7’ would be a “*first insulating-material layer*” arranged on at least one surface of the inner wiring layer 4 (*first conductive pattern layer*) as claimed. *Supra*, §IV.C.3; APPLE-1003, ¶120.

¹⁴ The ’816 Patent describes that the opening is first formed in the first insulating-material layer and the component is subsequently placed in the opening to form an electrical connection with the first conductive pattern layer. *Supra*, §III.A. Oya’s disclosure at paragraph [0066] aligns with these techniques as described in the ’816 Patent and confirms that the option of first forming an opening before mounting the component would have been an obvious design choice to simplify construction of Oya’s device in certain applications. APPLE-1003, 119. The specific processing steps described in paragraph [0067] of Oya are thus not essential or relied upon in this Petition. *Id.*

FIG. 7



APPLE-1004, FIG. 7 (annotated)

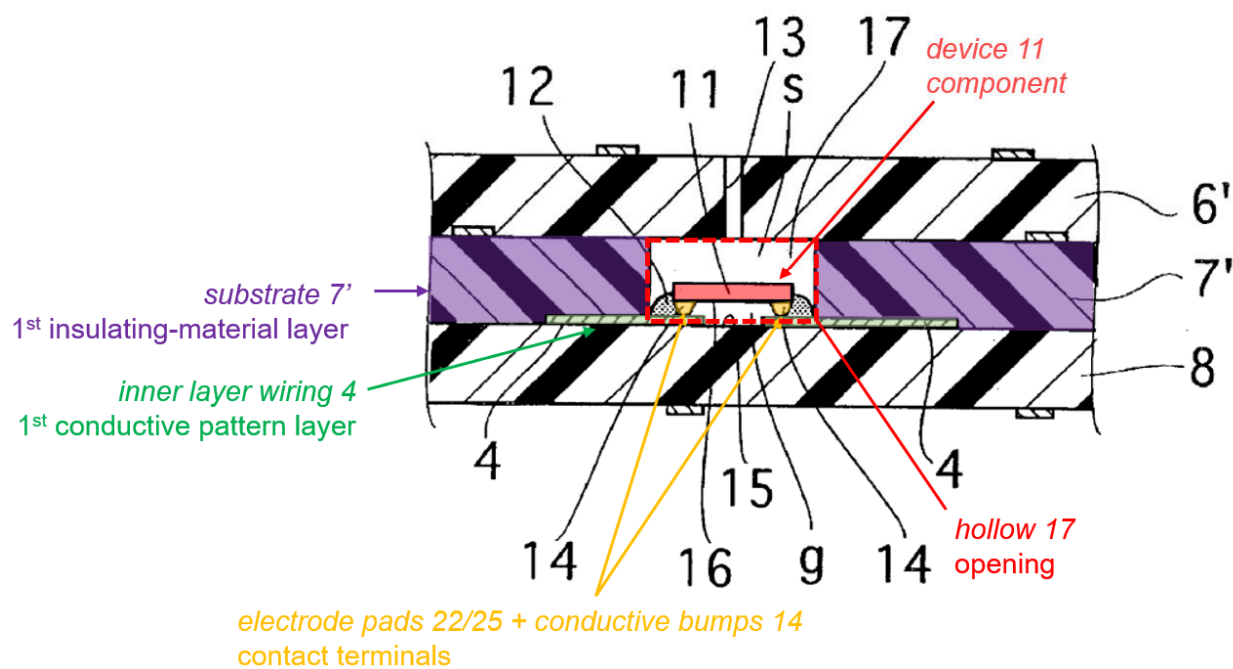
Element [1b]

The Oya-Shugg combination renders Element [1b] obvious. APPLE-1003, ¶121. For example, Oya discloses a “through-hole,” “recess,” or “hollow 17” that forms an “*opening*” in and that extends through the substrate 7’ (*first insulating-material layer*). APPLE-1004, ¶¶[0067] (“As shown in FIG. 7, after mounting the device 11 on the substrate 8, a substrate 7 having a through-hole formed therein may be stacked thereon and a substrate 6 may be stacked further thereon so as to cover the through-hole so as to form the hollow 17.”), [0066] (“after preparing a multilayer printed circuit board ... a device may be mounted in the recess”), FIG. 7; *see also id.*, [0014], [0040] (“hollow 17 formed in the substrate 6”), [0052],

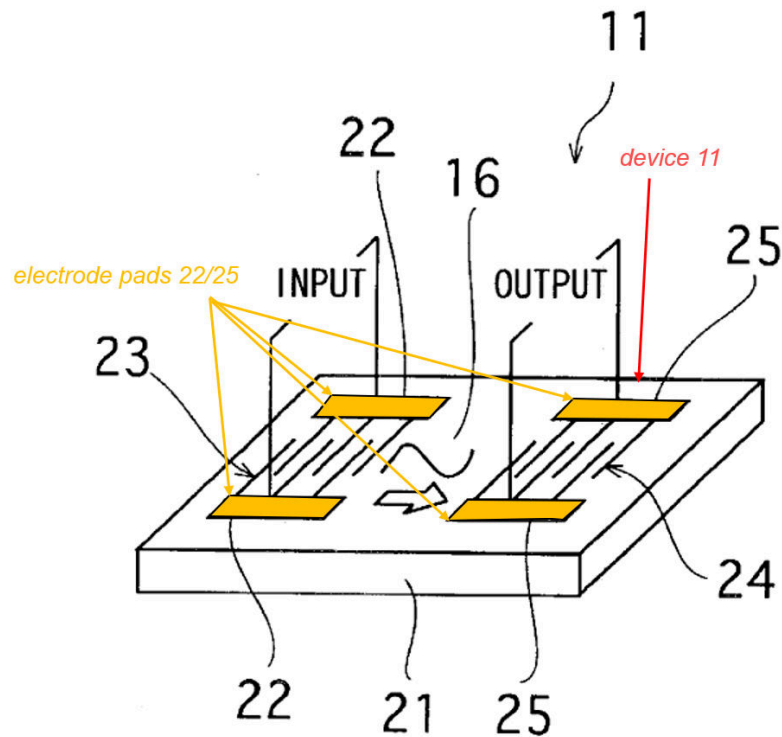
multilayer printed circuit board having a preliminarily provided recess, [in which] a device may be mounted in the recess, side surfaces of the device sealed with a resin and the recess may be covered with another substrate so as to obtain a hollow having the device sealed therein.” *Id.*, ¶[0066]; *see also id.*, [0067].

Oya also discloses that the device 11 (***component***) comprises a set of electrode pads, e.g., electrode pads 22, 25. APPLE-1004, ¶¶[0043], [0048], FIG. 9. “On the functional surface 16 side [of device 11], a plurality of conductive bumps 14 are formed ... with the electrode pads 22 and 25” and “[b]y bonding these conductive bumps 14 ... the electrode pads 22 and 25 are electrically connected to the wiring 4 through the conductive bumps 14.” *Id.*, [0048]. “The conductive bumps 14 may include a solder bump, a gold stud bump, and the like.” *Id.*, [0040]. The electrode pads of the device 11 (***component***), the conductive bumps, and the electrode pads together with the conductive bumps provide alternative mappings to the claimed “***contact terminals***” of the device 11 electrically connected to the wiring 4 (***first conductive-pattern layer***). APPLE-1003, ¶123.

FIG. 7



APPLE-1004, FIG. 7 (annotated)



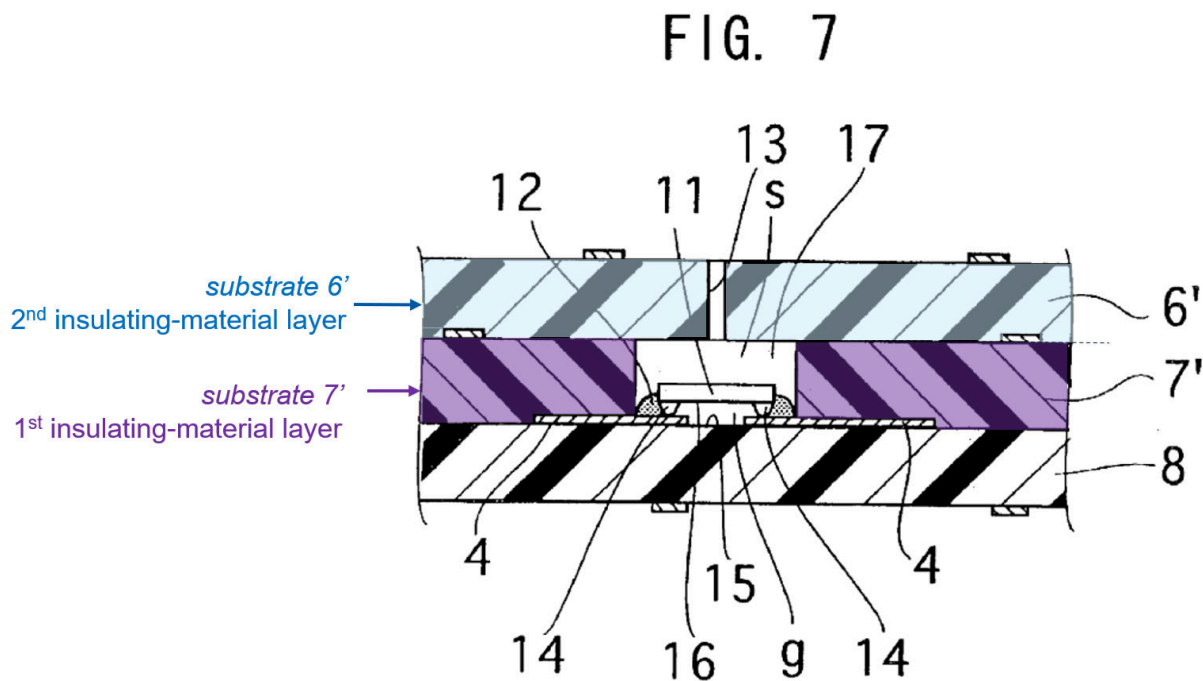
APPLE-1004, FIG. 9 (annotated)

Element [1d]

The Oya-Shugg combination renders Element [1d] obvious. APPLE-1003, ¶124. For example, Oya discloses a substrate layer 6' disposed on the substrate layer 7' (*first insulating-material layer*). APPLE-1004, ¶[0067] (“a substrate 7' having a through-hole formed therein may be stacked thereon and a substrate 6' may be stacked further thereon so as to cover the through-hole so as to form the hollow 17”), FIG. 7; *see also id.*, [0066], [0051] (“the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7 ... [t]hen, the substrates are sandwiched between heater plates and are pressed and heated.”).

Oya teaches that the substrates of the wiring board, e.g., substrate 6', can be

“pregreg” and “an epoxy resin or the like.” APPLE-1004, ¶¶[0045], [0051]. For the reasons described above, it would have been obvious to a POSITA based on the teachings of Shugg to implement Oya’s substrates including substrate 6’ as an insulator such that substrate layer 6’ would be a “*second insulating-material layer*” disposed on the substrate layer 7’ (*first insulating-material layer*) as claimed. *Supra*, §IV.C.3; *see also* APPLE-1004, ¶¶[0040], [0051]-[0053], [0060], [0067]; APPLE-1003, ¶125.

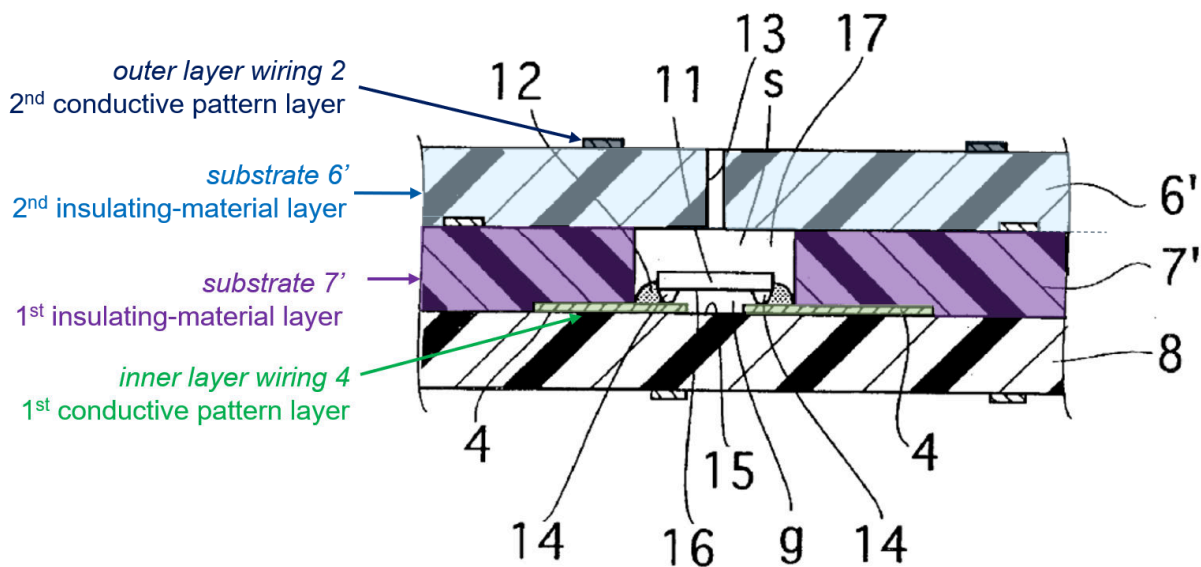


Element [1e]

The Oya-Shugg combination renders Element [1e] obvious. APPLE-1003, ¶126. For example, Oya discloses an outer layer wiring 2 that provides a “*second*

conductive pattern layer” as claimed. APPLE-1004, ¶[0067], FIG. 7; *see also id.*, ¶¶[0039] (“The wiring board 10 is a multilayer printed circuit board having two outer layer wirings 2 and 3 and two inner layer wirings 4 and 5.”). The outer layer wiring 2 is also referred to as a “copper foil pattern 2.” APPLE-1004, ¶[0055] (“copper foil patterns 2 and 3.”), [0051] (“the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7, respectively, and a copper foil is stacked on each of the substrates 6 and 8”). As shown in FIG. 7, the outer layer wiring 2 is disposed directly on substrate 6’ and is spaced apart from the inner layer wiring 4 (*first conductive pattern layer*) by at least the substrate layer 7’ (*first insulating-material layer*) and the substrate layer 6’ (*second insulating-material layer*). *Id.*; APPLE-1003, ¶126.

FIG. 7



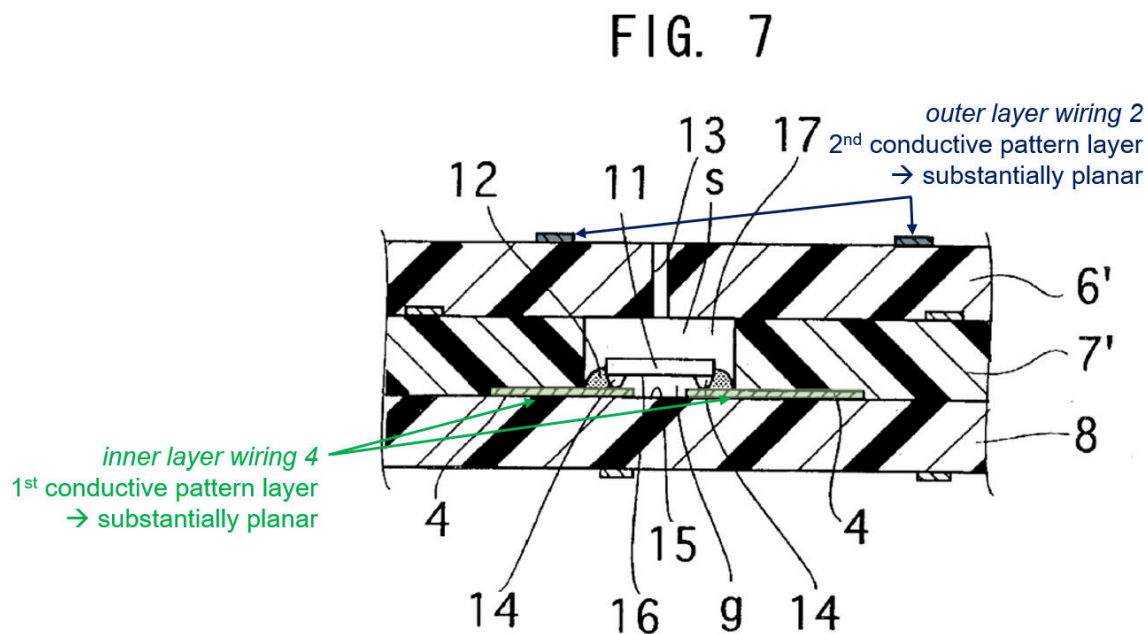
APPLE-1007, FIG. 7 (annotated)

Element [1f]

The Oya-Shugg combination renders Element [1f] obvious. APPLE-1003, ¶127. In the combination, Oya's inner layer wiring 4 (*first conductive pattern layer*) and outer layer wiring 2 (*second conductive pattern layer*) are each substantially planar. APPLE-1004, ¶¶[0051], [0039], [0054]-[0055], [0066]-[0067]; *see also id.*, FIGS. 1, 7-8. For example, when forming the inner layer wiring 4, Oya teaches that a copper foil or a copper plating is disposed directly "on both surfaces of the substrate 7." APPLE-1004, ¶[0045]. After a dry film is disposed on the copper foil, a mask having a circuit pattern is thereon disposed. *Id.*, ¶[0046]. Using the dry film as a mask, the copper foil is wet-etched and the wirings 4 and 5 are formed. *Id.*, ¶¶[0046]-[0047]. A POSITA would have understood and it would have been obvious from these teachings, including the fact that the inner layer wiring 4 is formed on the surface of a substantially planar substrate 8, that the inner layer wiring 4 is substantially planar. APPLE-1003, ¶127.

Furthermore, as illustrated in FIG. 7, Oya's outer layer wiring 2 is formed on substrate 6', thereby providing a second conductive pattern layer that is substantially planar. APPLE-1004, ¶[0067], FIG. 7, *see also id.*, [0051] ("a copper foil is stacked on each of the substrates 6 and 8"), [0054]-[0055] ("[A]fter sticking

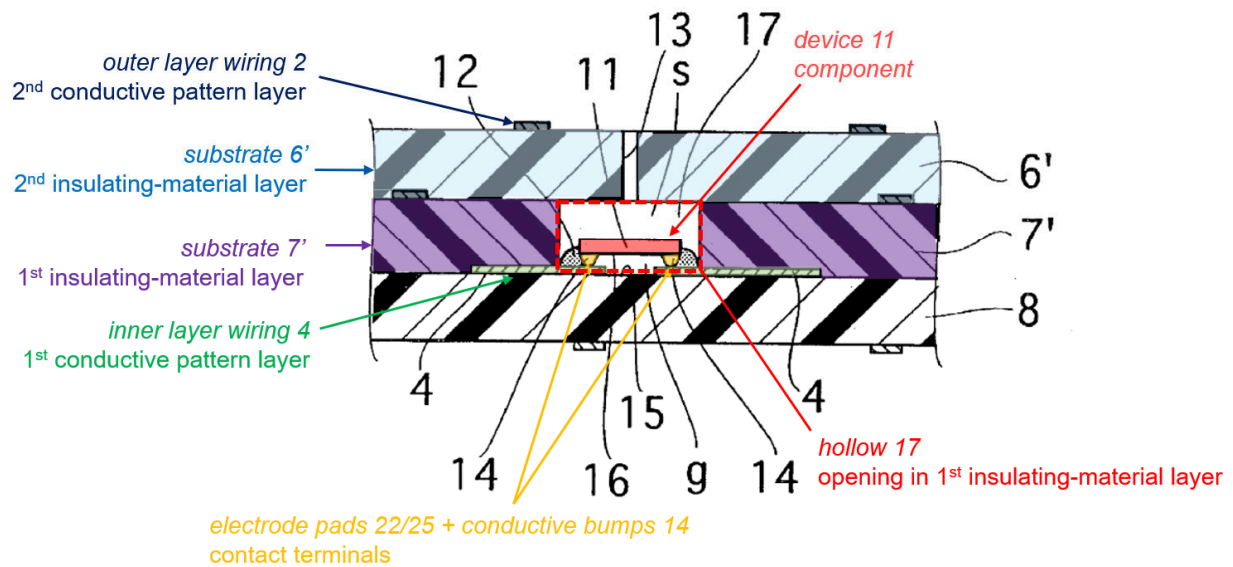
a dry film on the copper foil stuck on each of the surfaces of the substrates 6 and 8.... [A] desired copper foil patterns 2 and 3 can be obtained.”). Accordingly, a POSITA would have understood and it would have been obvious from Oya’s teachings, including the fact that the outer layer wiring 2 is formed on the surface of a substantially planar substrate 6’, that the outer layer wiring 2 is also substantially planar. APPLE-1003, ¶128.



APPLE-1007, FIG. 7 (annotated)

The following version of FIG. 7 further illustrates representative mappings of various structures from Oya’s electronic module to corresponding structures recited in claim 1 (APPLE-1003, ¶129):

FIG. 7

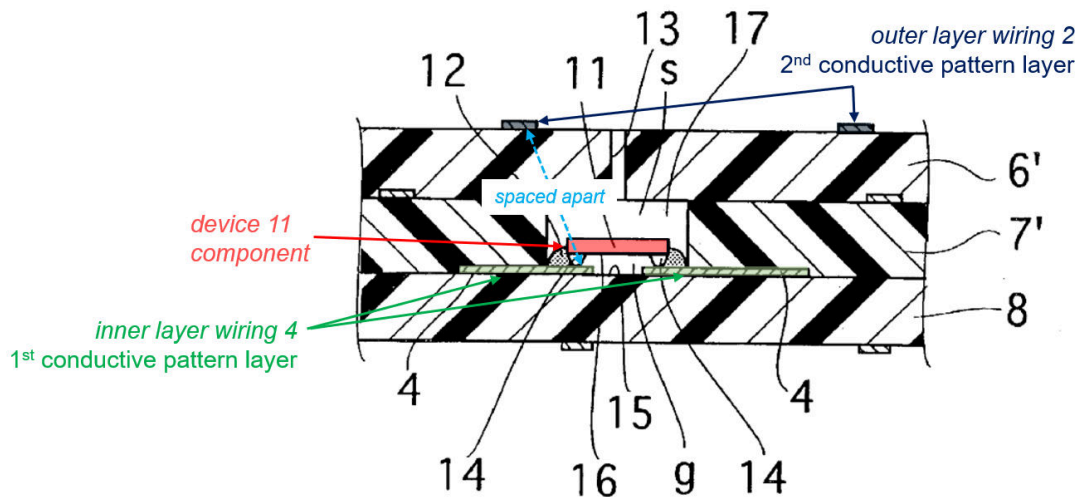


APPLE-1007, FIG. 7 (annotated)

Claim [3]

The Oya-Shugg combination renders Claim [3] obvious. APPLE-1003, ¶130. For example, Oya discloses that the outer layer wiring 2 (*second conductive pattern layer*) is spaced apart from the inner layer wiring 4 (*first conductive pattern layer*) by the device 11 (*component*). *Id.* This configuration is illustrated in FIG. 7:

FIG. 7



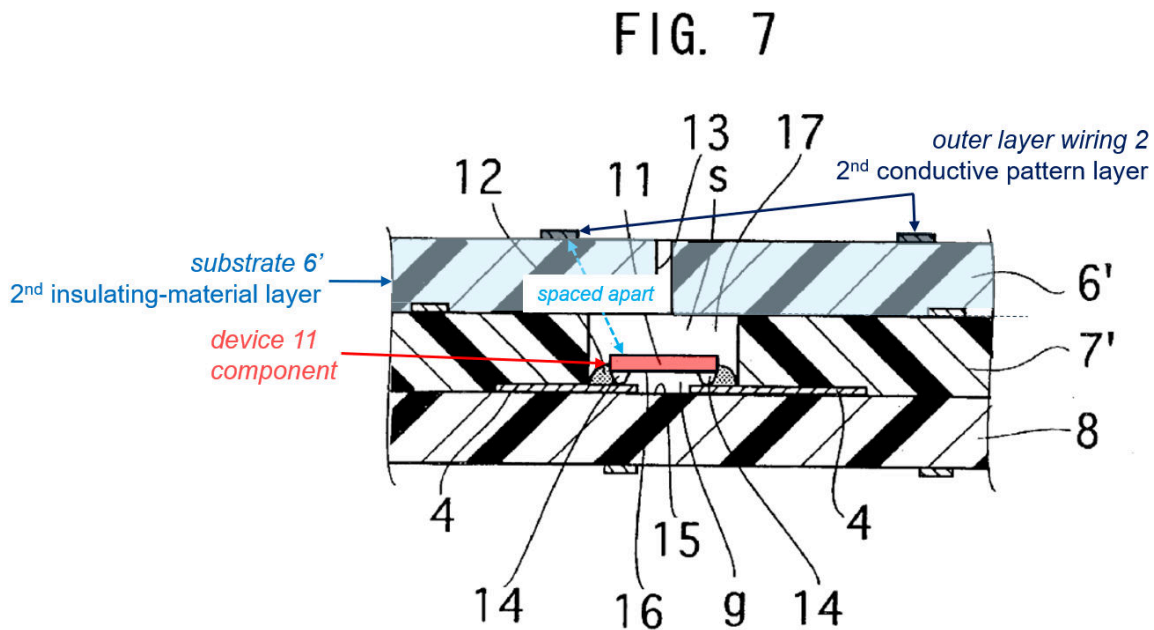
APPLE-1004, FIG. 7 (annotated)

See also *id.*, ¶40 (describing a gap of “several tens of μm ” between an inner surface 15 of the hollow 17 and the functional surface 16 of the device 11), [0066]-[0067]; APPLE-1003, ¶131.

Claim [4]

The Oya-Shugg combination renders Claim [4] obvious. APPLE-1003, ¶132. For example, Oya discloses that the outer layer wiring 2 (*second conductive pattern layer*) is disposed on a top surface of the substrate 6' (*second insulating-material layer*), as shown in FIG. 7. APPLE-1004, ¶¶[0066]-[0067], FIG. 7. The device 11 (*component*) is disposed within the hollow 17 fashioned inside the substrate 7'. *Id.* The substrate 7' is disposed below the substrate 6'. *Id.* Oya discloses that “the device 11 [is disposed] on the substrate 8.” *Id.*, [0067]. The

“substrate 7’ having a through-hole formed therein may be stacked [on the substrate 8].” *Id.* The “substrate 6’ may be stacked further [on the substrate 7’] so as to cover the through-hole [and] form the hollow 17.” *Id.* As such, Oya’s outer layer wiring 2 (*second conductive pattern layer*) is spaced apart from the device 11 (*component*) by the substrate 6’ (*second insulating-material layer*). *Id.*; APPLE-1003, ¶132.

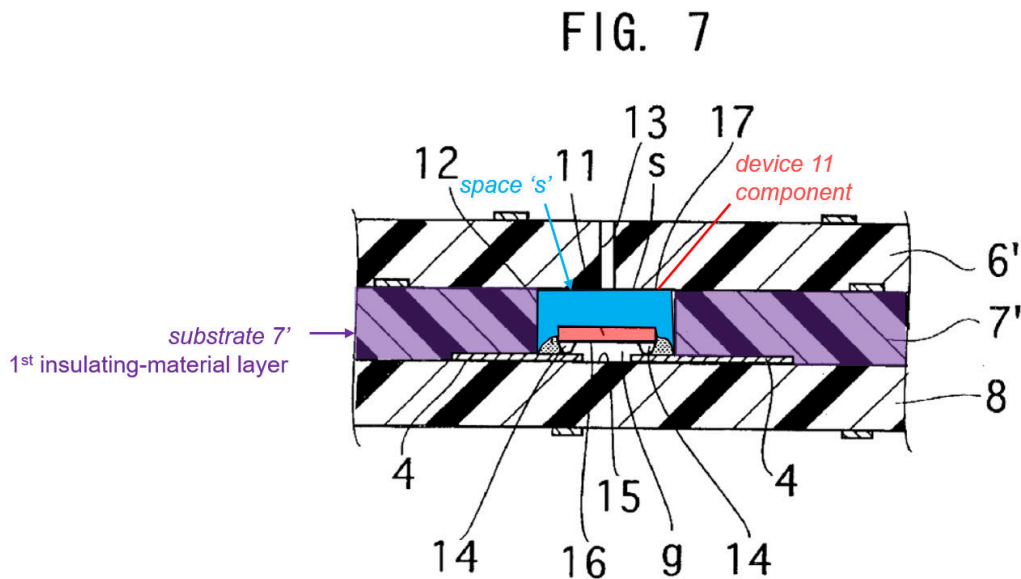


APPLE-1004, FIG. 7 (annotated)

Claim [6]

The Oya-Shugg combination renders Claim [6] obvious. APPLE-1003, ¶133. For example, Oya discloses that the substrate 7’ (*first insulating-material layer*) is spaced apart from the device 11 (*component*). *Id.* Oya’s device 11 is mounted within a hollow 17 formed by the substrate 6’ and the substrate 7’.

APPLE-1004, ¶¶[0066]-[0067], FIG. 7; *see also id.*, ¶¶52-56. Oya further discloses that “the device 11 faces the wiring board 10 in *non-contact having the gap g therebetween*, and the other surface of the device 11 faces the wiring board 10 in *non-contact having the space s therebetween*.” *Id.*, ¶57. Accordingly, a POSITA in possession of Oya would have understood from the figures and description that the substrate 7' (*first insulating-material layer*) is spaced apart from the device 11 (*component*) at least by the space s provided between the device 11 and the substrate 7'. APPLE-1003, ¶133.



APPLE-1004, FIG. 7 (annotated)

Claim [7]

The Oya-Shugg combination renders Claim [7] obvious. APPLE-1003, ¶134. As discussed above, Oya teaches that the substrates of its wiring board, e.g.,

substrates 6' and 7', can be "prepreg" and "an epoxy resin." APPLE-1004, ¶¶[0045], [0051]. A POSITA would have known that "prepreg" was a composite material commonly used for circuit board substrates made of pre-impregnated fibers mixed with a partially cured resin. APPLE-1006, 289-290 ("The basic materials for making industrial laminates are called *prepregs*. A prepreg is composed of a substrate, usually paper, cotton, or glass fabric, impregnated with a thermosetting resin...."), 291 ("Epoxy resin glass-reinforced laminates ... are used extensively as substrates for printed circuits."), 303-304; APPLE-1003, ¶134; *see also* APPLE-1019, 239 ("[g]lass-fiber cloth pre-impregnated with epoxy-resin [was] ... widely used as a composite electrical insulation in various electrical industrial products"). Consistent with this conventional understanding of prepreg, Oya explicitly confirms that the substrates can be "composed of glass fiber impregnated with a resin." APPLE-1004, ¶[0060]. Because prepreg is a composite material that is itself composed of multiple materials, substrate 7' (*first insulating-material layer*) comprises *a* material that is different than *a* material of substrate 6' (*second insulating-material layer*) as claimed.¹⁵ APPLE-1003, ¶134.

¹⁵ Through use of the open-ended transition word "comprises" in the phrase "the first insulating-material layer *comprises* a different material than a material of the

For example, substrate 7' comprises a glass fiber material that is different from a resin material of substrate 6'. *Id.* Alternatively, substrate 7' comprises a resin material that is different from a glass fiber material of substrate 6.' *Id.*

Element [8pre]

Supra, Element [1pre]; APPLE-1003, ¶135.

Element [8a]

Supra, Element [1a]; APPLE-1003, ¶136.

second insulating-material layer,” claim 7 is clear that the first insulating-material layer need only *include* a material that is different from a material of the second insulating-material layer—but it need not consist only of material that is different from any/all material of the second insulating-material layer. APPLE-1003, 134, n. 11. The plain language of claim 7 is met by Oya’s disclosure of one material in the first insulating-material layer that is different than another material in the second insulating-material layer. *Id.* The specification of the ’816 Patent likewise confirms that “the insulating-material layer 1 can equally well be manufactured from more than one part” and “[i]t is then also possible to proceed in such a way that the insulating-material layer 1 is *formed of more than one insulating material*.” APPLE-1001, 12:36-40.

Element [8b]

Supra, Element [1b]; APPLE-1003, ¶137.

Element [8c]

Supra, Element [1c]; APPLE-1003, ¶138.

Element [8d]

The Oya-Shugg combination renders Element [8d] obvious. APPLE-1003, ¶139. As addressed above in connection with Element [1d], Oya discloses a substrate layer 6' disposed on the substrate layer 7'. APPLE-1004, ¶[0067], FIG. 7; *see also id.*, [0066], [0051] (“the substrates (prepregs) 6 and 8 are stacked on both surfaces of the substrate 7”); *supra*, Element [1d].

Oya discloses that “[t]he wiring board 10 is a multilayer printed circuit board.” APPLE-1004, ¶[0039]; *see also id.*, ¶[0066] (“preparing a multilayer printed circuit board”); APPLE-1003, ¶140. Shugg further describes well-known techniques for constructing multilayer printed circuit boards like Oya’s. APPLE-1006, 307. According to Shugg, “[p]rinted circuit materials, usually of epoxy or polyimide types, may be layered to form multilayer circuits.” *Id.* “Circuits may have up to 40 layers” and “[t]hese high-density constructions[] ... offer significant savings in size and weight.” *Id.* A POSITA considering the teachings of Shugg would have understood that, although Oya only explicitly depicts a few wiring and substrate layers in its multilayer PCB 10, it would have been obvious to implement

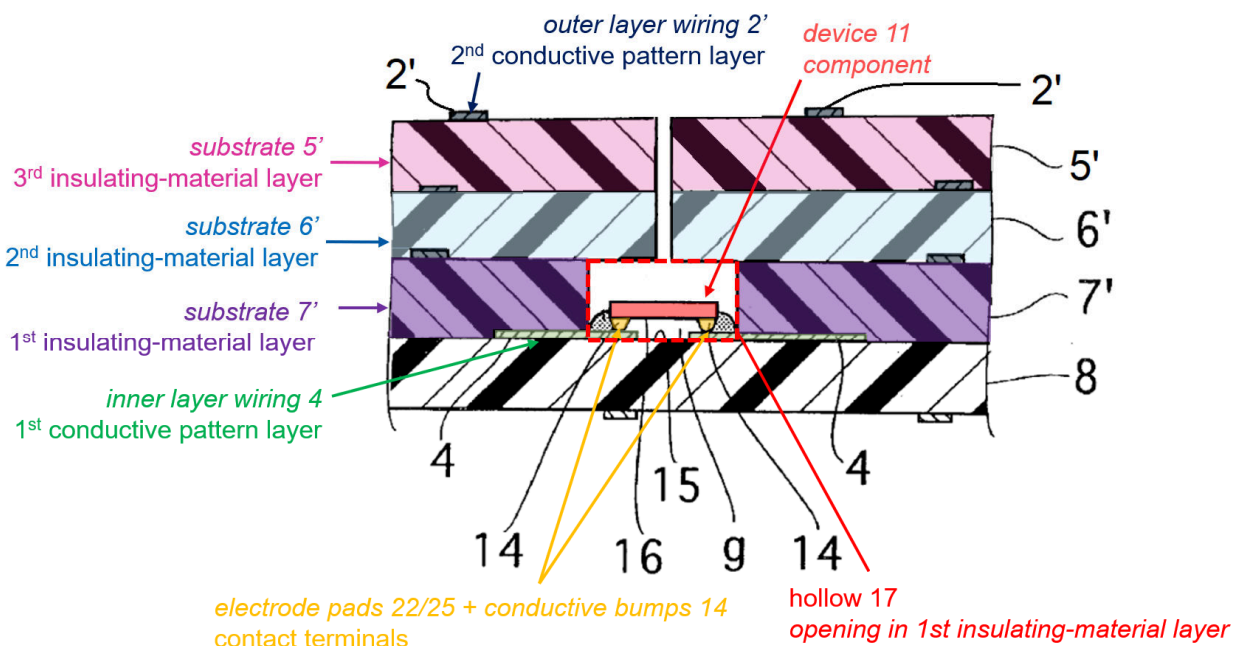
Oya's PCB 10 with additional wiring and/or substrate layers. APPLE-1003, ¶140.

A POSITA would have done so to achieve at least the known benefits explicitly discussed in Shugg, including to provide a "high[er]-density construction[]" and to gain "significant savings in size and weight." APPLE-1006, 307; APPLE-1003, ¶140. Indeed, adding layers to Oya's multilayer PCB 10 would beneficially yield additional wiring layers that could be used to establish additional electrical connections between electronic components of the PCB 10 (e.g., connections between device 11 and other components mounted on or embedded in the PCB 10) without a significant increase in the footprint of the PCB 10 that would ordinarily otherwise be necessary to accommodate the additional wiring on existing layers. APPLE-1003, ¶140.

Reducing the size of the PCB would also be beneficial to reduce the length of the wiring on the PCT and between connection endpoints, which a POSITA would have sought to do to reduce electrical resistance through the wiring, minimize power loss due to internal resistance in the wire (which is proportional to the path length), improve signal integrity, and minimize heat generation. APPLE-1003, ¶141. To be sure, the addition of layers to Oya's multilayer PCB as taught in Shugg would have been entirely obvious as it involves the mere application of a known technique (e.g., forming additional layers in a multilayer PCB) to a known device (e.g., Oya's PCB 10) that was ready for improvement to yield merely

predictable results (e.g., a multilayer PCB 10 with additional layers beyond those explicitly depicted in Oya's FIG. 7). *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (“[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.”); APPLE-1003, ¶141. A POSITA would have reasonably expected success modifying Oya's PCB 10 to include additional layers since multilayer PCBs with more than three or four substrate layers were well known before the '816 Patent and Oya already contemplated that its electronic module should be implemented as a multilayer PCB. *See* APPLE-1004, ¶¶[0039], [0066]; APPLE-1006, 307 (“up to 40 layers”); *see also* APPLE-1004, ¶[0071].

The following figure shows a first predictable implementation of Oya's PCB 10 modified in accordance with Shugg's teachings to include an additional substrate layer (labeled as substrate 5') over substrate 6' and an outer wiring layer 2' formed on the top surface of substrate 5', thereby providing an additional inner wiring layer between substrates 5' and 6' (APPLE-1003, ¶142):

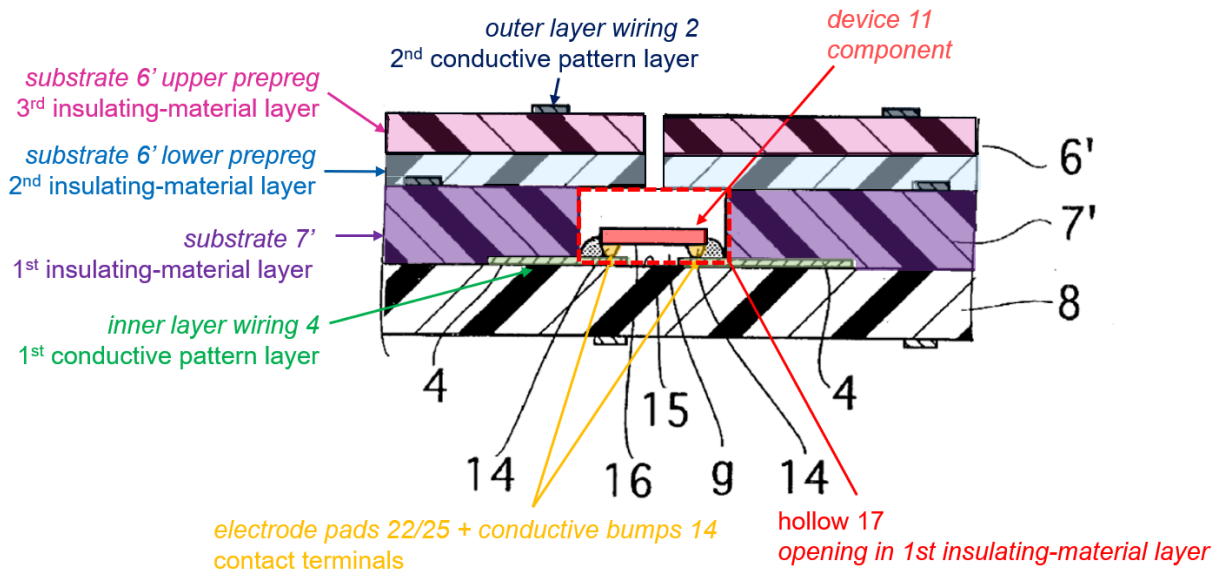


First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

As another example, based on Shugg's teaching to provide "two or three bonding layers of prepreg between circuit layers," it would have been obvious to provide not just one but two prepreg substrate layers between the inner wiring layer on substrate 7' and the outer wiring layer on substrate 6' as shown below. APPLE-1006, 307; APPLE-1003, ¶143. A POSITA would have sought to substitute Oya's single substrate 6' with two substrate layers to achieve a desired thickness, increase stability and rigidity of the PCB 10, and to increase separation between wiring layers that can be beneficial to reduce both RF interference and thermal interaction between the wiring layers. *KSR*, 550 U.S. at 417; APPLE-1003, ¶143. The following figure illustrates an alternative implementation of the

Oya-Shugg combination according to the modification described here:



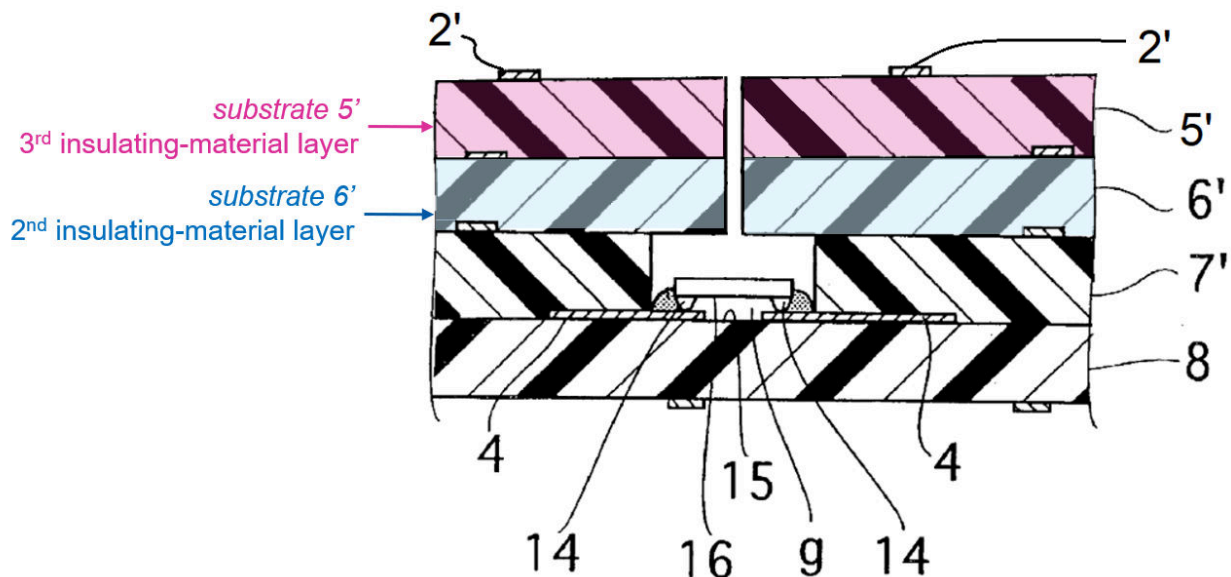
Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

Oya teaches that its substrate layers can be “prepreg” and “an epoxy resin or the like.” APPLE-1004, ¶¶[0045], [0051]. For each of the reasons described above, it would have been obvious to a POSITA based on Shugg to implement the substrate layers in the Oya-Shugg combination as insulators such that substrate layer 6' in the first alternative implementation and the substrate 6' lower prepreg in the second alternative implementation would each be a “*second insulating-material layer*” disposed on the substrate layer 7' (*first insulating-material layer*) as claimed. *Supra*, §IV.C.3; *see also* APPLE-1004, ¶¶[0040], [0051]-[0053], [0060], [0067]; APPLE-1003, ¶144.

Element [8e]

The Oya-Shugg combination renders Element [8e] obvious. APPLE-1003, ¶145. As described above in connection with Element [8d], it would have been obvious based on Shugg to extend Oya's multilayer PCB 10 to include additional prepreg or other insulating-material layers above substrate 7'. *Supra*, Element [8d]; APPLE-1003, ¶145. In the first alternative implementation of the Oya-Shugg combination, substrate 5' (*third insulating-material layer*) is disposed on substrate 6' (*second insulating-material layer*). *Id.*

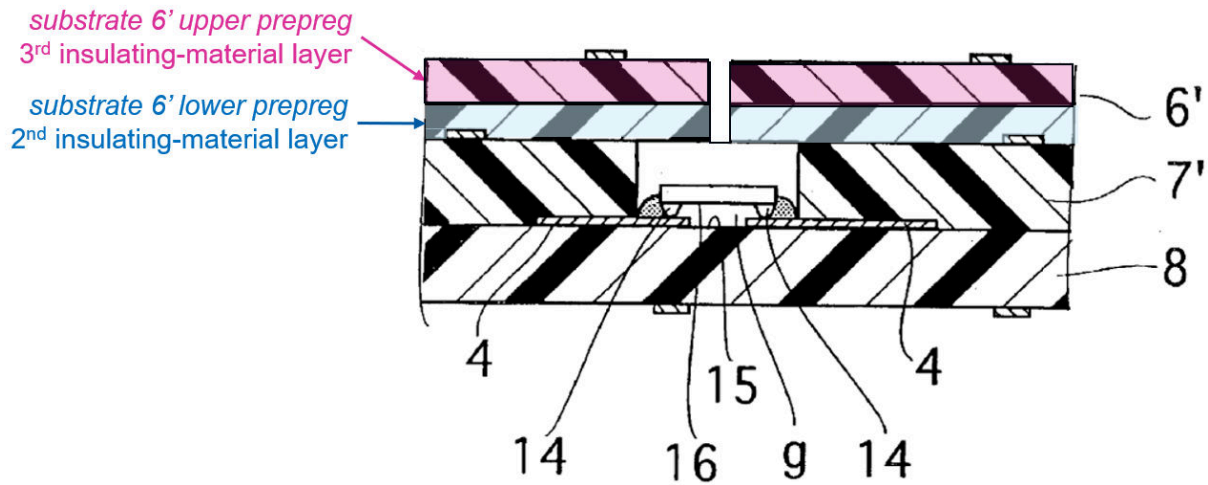


First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

Likewise, in the second alternative implementation of the Oya-Shugg combination, substrate 6' upper prepreg (*third insulating-material layer*) is disposed on substrate 6' lower prepreg (*second insulating-material layer*).

APPLE-1003, ¶146.



Second Alternative Implementation of the Oya-Shugg Combination

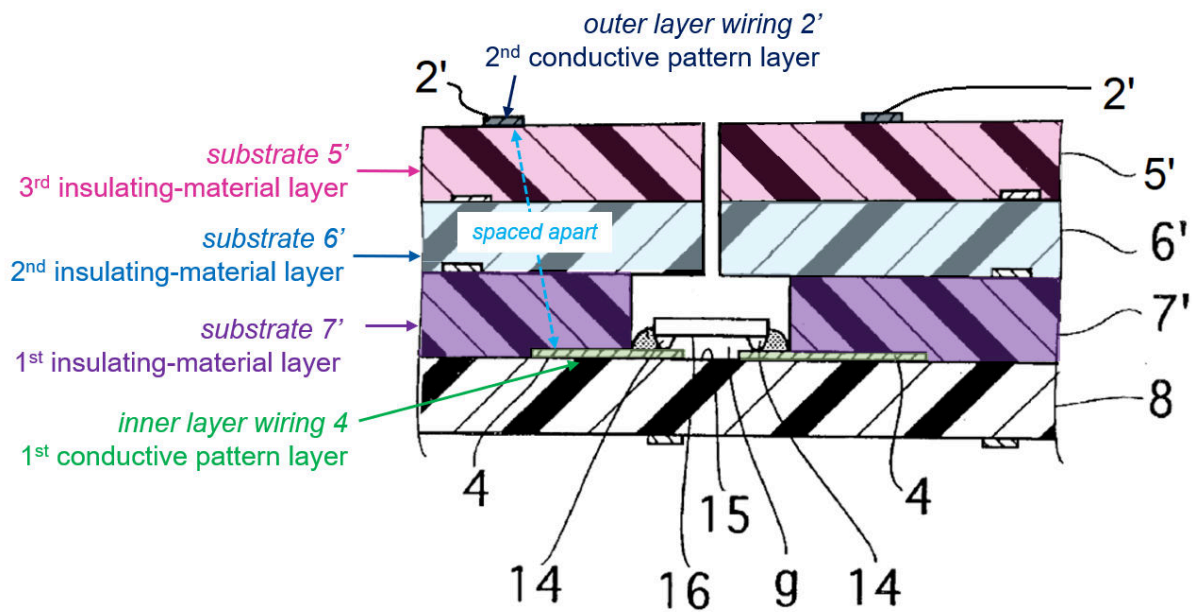
(APPLE-1004, FIG. 7 (modified and annotated))

Element [8f]

The Oya-Shugg combination renders Element [8f] obvious. APPLE-1003, ¶147. For example, Oya discloses an outer layer wiring 2. APPLE-1004, ¶[0067], FIG. 7; *see also id.*, ¶[0039]. The outer layer wiring 2 is also referred to as a “copper foil pattern 2.” APPLE-1004, ¶[0055] (“copper foil patterns 2 and 3.”), [0051] (“the substrates (prepregs) 6 and 8 are stacked on ... the substrate 7... and a copper foil is stacked on each of the substrates 6 and 8”). The outer layer wiring 2 is disposed directly on substrate 6' and is spaced apart from the inner layer wiring 4 by at least the substrate layer 7' and the substrate layer 6'. APPLE-1004, FIG. 7; APPLE-1003, ¶147; *supra*, Element [1e].

Moreover, as described above in connection with Element [8d], it would

have been obvious based on Shugg to extend Oya's multilayer PCB 10 to include additional wiring and/or substrate layers. *Supra*, Element [8d]; APPLE-1003, ¶148. In the first alternative implementation of the Oya-Shugg combination, an outer wiring layer 2' (*second conductive pattern layer*) is spaced apart from the inner wiring layer 4 (*first conductive pattern layer*) by substrate 7' (*first insulating-material layer*), substrate 6' (*second insulating-material layer*), and substrate 5' (*third insulating-material layer*). *Id.*



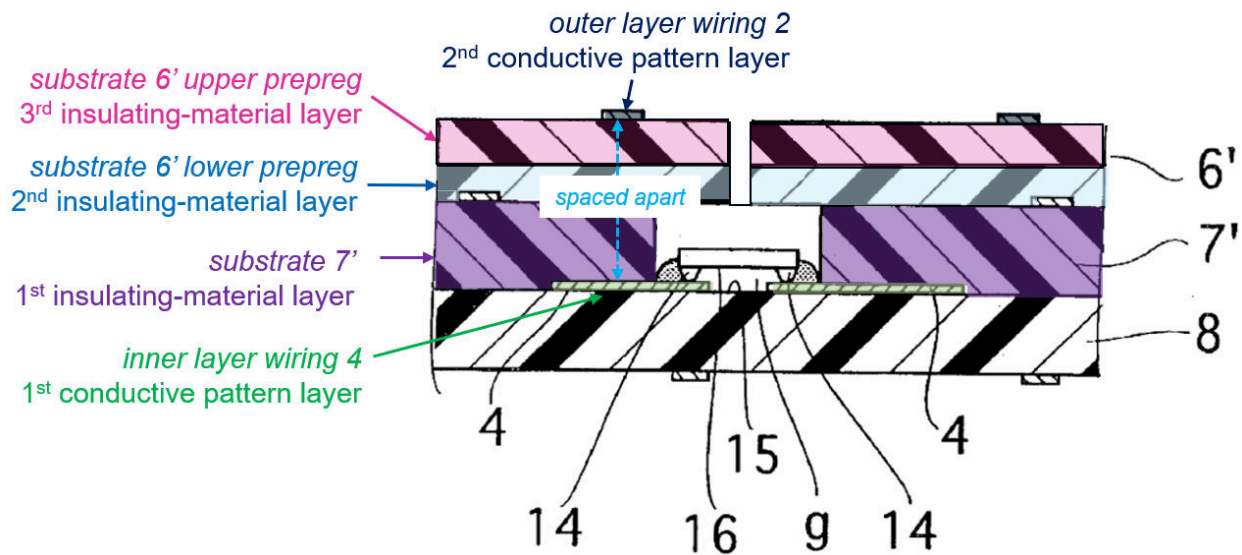
First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

Likewise, in the second alternative implementation of the Oya-Shugg combination, outer wiring layer 2 (*second conductive pattern layer*) is spaced apart from the inner wiring layer 4 (*first conductive pattern layer*) by substrate 7'

(*first insulating-material layer*), substrate 6' lower prepreg (*second insulating-material layer*), and substrate 6' upper prepreg (*third insulating-material layer*).

APPLE-1003, ¶149.



Second Alternative Implementation of the Oya-Shugg Combination

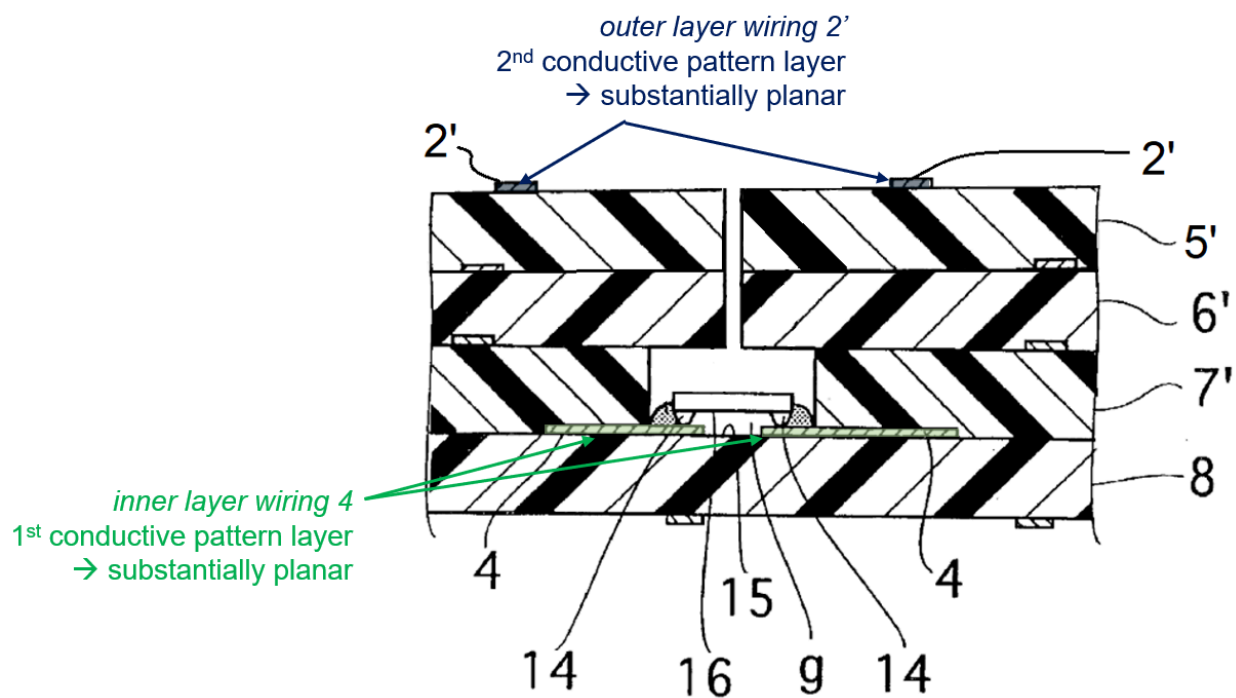
(APPLE-1004, FIG. 7 (modified and annotated))

Element [8g]

The Oya-Shugg combination renders Element [8g] obvious. APPLE-1003, ¶150. For example, Oya teaches that its wiring layers including inner layer wiring 4 and outer layer wiring 2 are each substantially planar. APPLE-1004, ¶¶[0051], [0039], [0054]-[0055], [0066]-[0067]; *see also id.*, FIGS. 1, 7-8. According to APPLE-1004, when forming the inner layer wiring 4, a copper foil or a copper plating is disposed directly “on both surfaces of the substrate 7.” APPLE-1004, ¶[0045]. After a dry film is disposed on the copper foil, a mask having a circuit

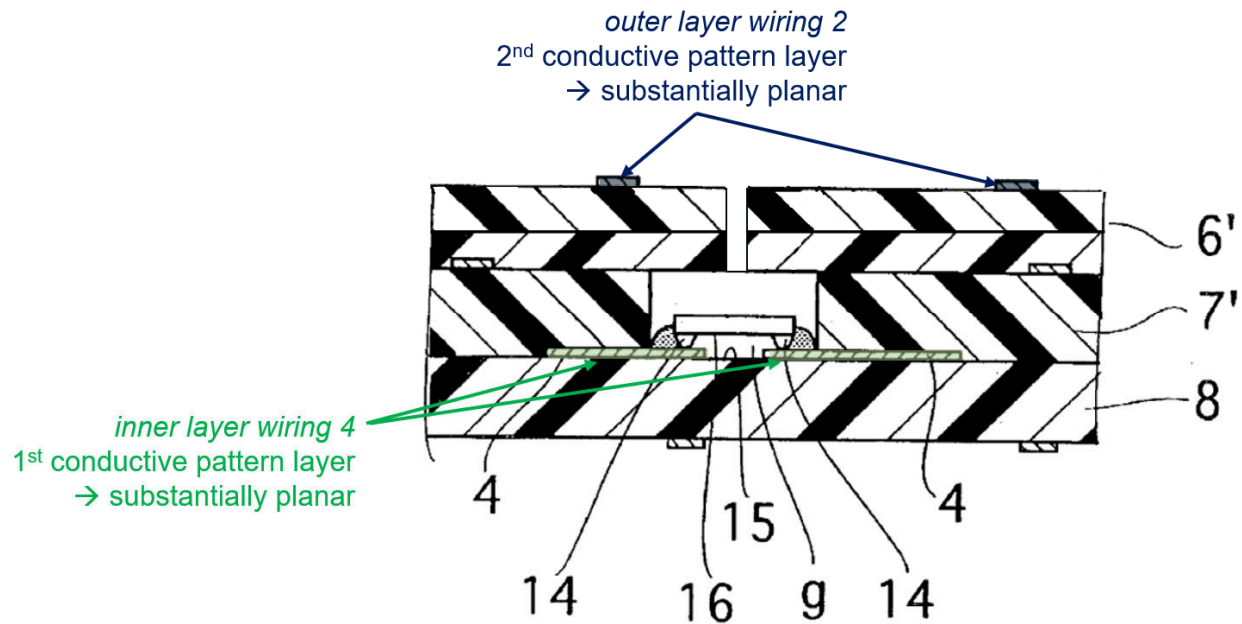
pattern is thereon disposed. *Id.*, ¶[0046]. Using the dry film as a mask, the copper foil is wet-etched and the wirings 4 and 5 are formed. *Id.*, ¶¶[0046]-[0047]. A POSITA would have understood and it would have been obvious from these teachings, including the fact that the inner layer wiring 4 is formed on the surface of a substantially planar substrate 8, that the inner layer wiring 4 is substantially planar. APPLE-1003, ¶150.

Furthermore, as illustrated in FIG. 7, Oya's outer layer wiring 2 is formed on a substantially planar substrate 6', thereby providing a second conductive pattern layer that is likewise substantially planar. APPLE-1004, ¶[0067], FIG. 7, *see also id.*, [0051] ("a copper foil is stacked on each of the substrates 6 and 8"), [0054]-[0055]. Accordingly, a POSITA would have understood and it would have been obvious from Oya's teachings, including the fact that the outer layer wiring 2 is formed on the surface of a substantially planar substrate 6', that the outer layer wiring 2 is also substantially planar, and that the outer layer wiring 2' in the first alternative implementation of the Oya-Shugg combination would be substantially planar. APPLE-1003, ¶151.



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

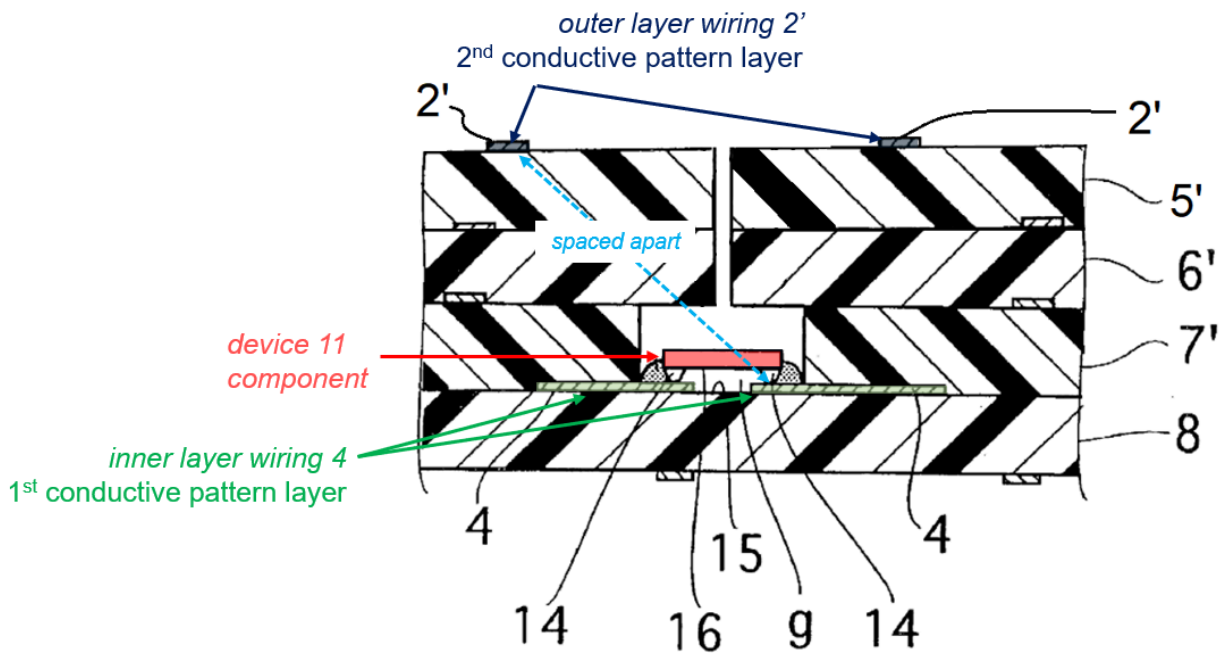


Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

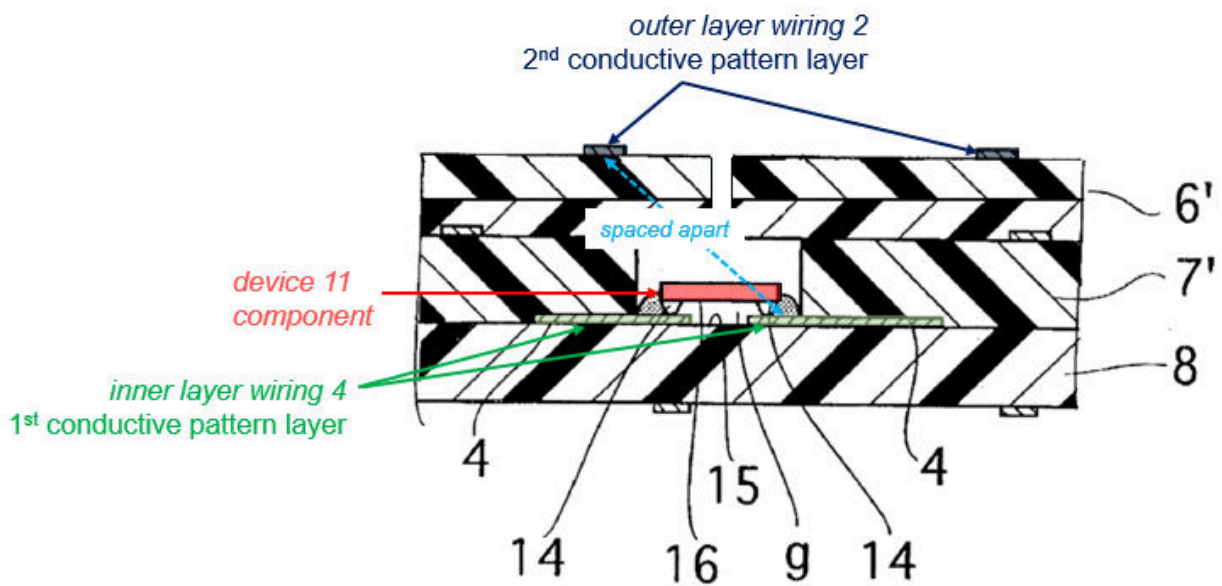
Claim [10]

The Oya-Shugg combination renders Claim [10] obvious. APPLE-1003, ¶152. For example, in the combination, Oya discloses that the outer layer wiring 2 or 2' (*second conductive pattern layer*) is spaced apart from the inner layer wiring 4 (*first conductive pattern layer*) by the device 11 (*component*). APPLE-1004, FIG. 7; *see also id.*, [0066]-[0067].



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

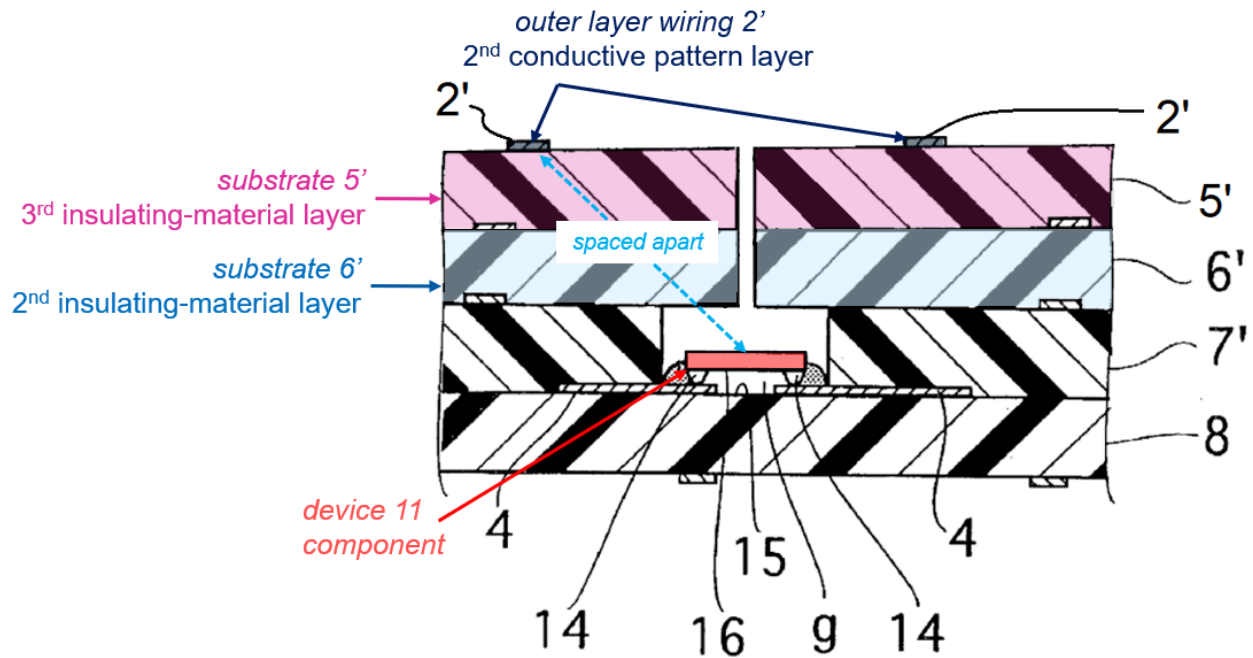
See also id., ¶40 (describing a gap of “several tens of μm ” between an inner surface 15 of the hollow 17 and the functional surface 16 of the device 11), [0066]-[0067].

Claim [11]

The Oya-Shugg combination renders Claim [11] obvious. APPLE-1003, ¶153. For example, in the combination, the outer layer wiring 2 or 2' (*second conductive pattern layer*) is disposed on a top surface of the substrate 5' or on a top surface of the substrate 6' upper prepreg (*third insulating-material layer*). APPLE-1004, ¶¶[0066]-[0067], FIG. 7; *supra*, Element [8d]. The device 11 (*component*) is disposed within the hollow 17 fashioned inside the substrate 7'. *Id.* The substrate 7' is disposed below the substrate 6'. *Id.* Oya discloses that “the device 11 [is disposed] on the substrate 8.” *Id.*, [0067]. The “substrate 7' having a through-hole formed therein may be stacked [on the substrate 8].” *Id.* The “substrate 6' may be stacked further [on the substrate 7] so as to cover the through-hole so as to form the hollow 17.” *Id.* In the combination, outer layer wiring 2' (*second conductive pattern layer*) in the first alternative implementation is spaced apart from the device 11 (*component*) by the substrates 5' and 6' (*third and second insulating-material layers*), and outer layer wiring 2 (*second conductive pattern layer*) in the second alternative implementation is spaced apart from the device 11 (*component*) by the substrate 6' upper and lower prepreps (*third and*

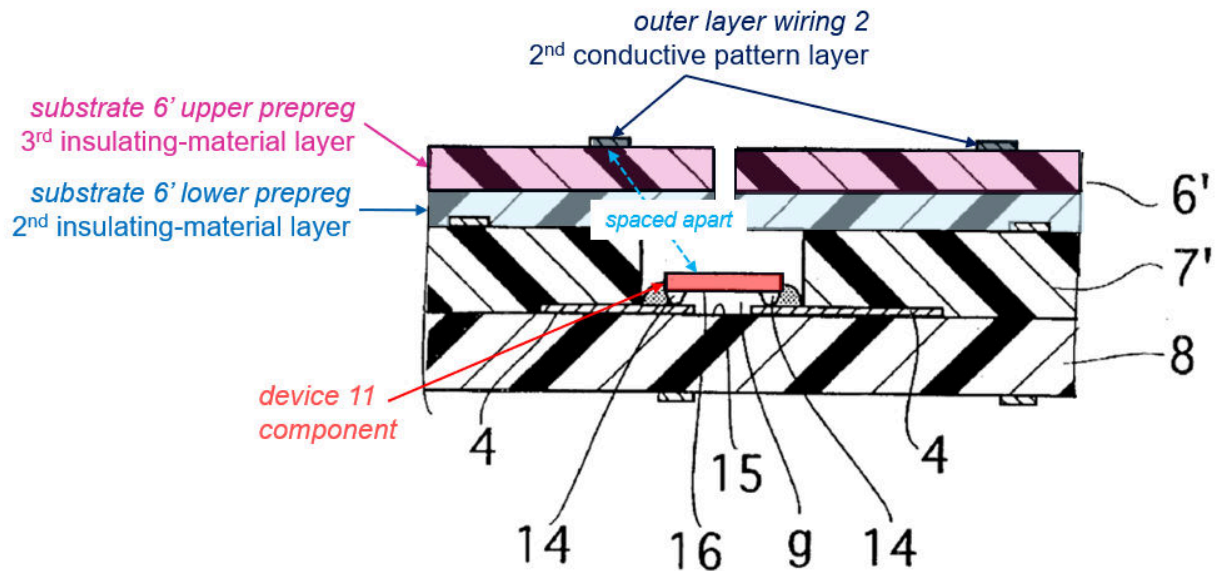
second insulating-material layers) in the second alternative implementation. *Id.*;

APPLE-1003, ¶153.



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

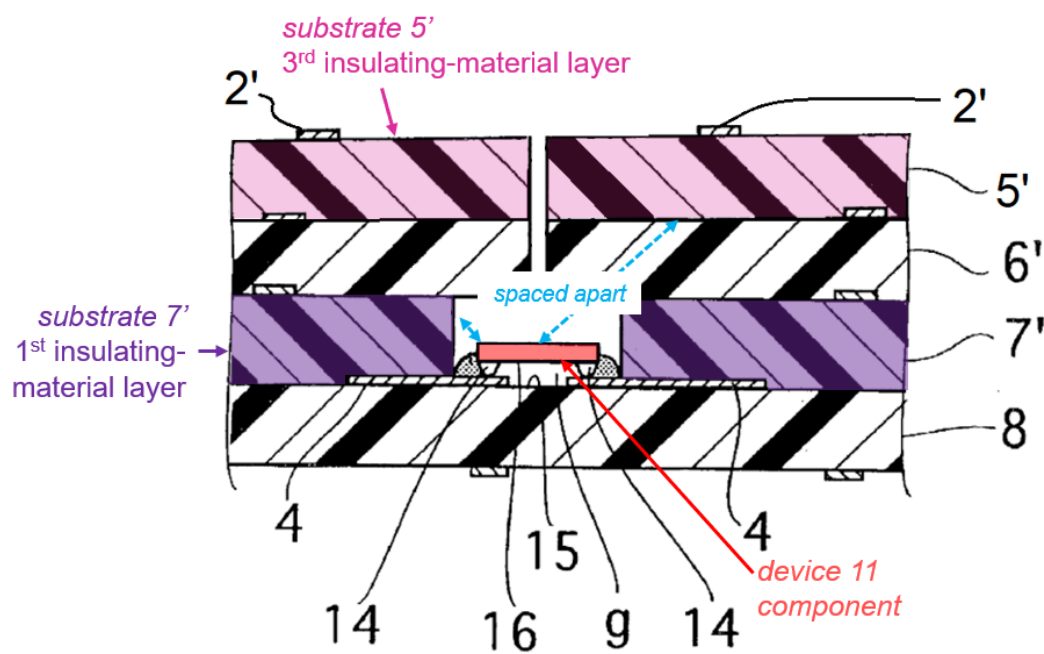
(APPLE-1004, FIG. 7 (modified and annotated))

Claim [13]

The Oya-Shugg combination renders Claim [13] obvious. APPLE-1003, ¶154. To start, Oya discloses that the substrate 7' (*first insulating-material layer*) is spaced apart from the device 11 (*component*). *Id.* Oya's device 11 is mounted within a hollow 17 formed by the substrate 6' and the substrate 7'. APPLE-1004, ¶¶[0066]-[0067], FIG. 7; *see also id.*, ¶¶52-56. Oya further discloses that "the device 11 faces the wiring board 10 in *non-contact having the gap g therebetween*, and the other surface of the device 11 faces the wiring board 10 in *non-contact having the space s therebetween*." *Id.*, ¶57. Accordingly, a POSITA in possession of Oya would have understood from the figures and description that

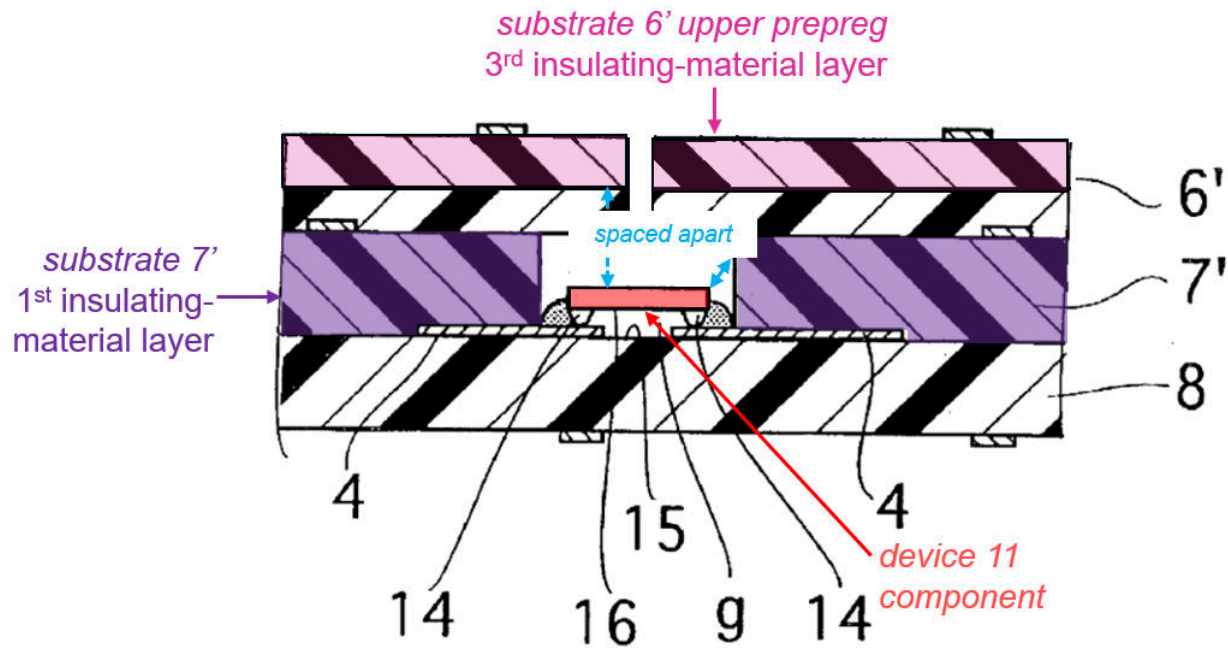
the substrate 7' (*first insulating-material layer*) is spaced apart from the device 11 (*component*) at least by the space s provided between the device 11 and the substrate 7'. APPLE-1003, ¶154.

Additionally, as described above in connection with Element [8d], it would have been obvious based on Shugg to implement a “*third insulating-material layer*” in Oya’s PCB 10 as either substrate 5’ in the first alternative implementation of the Oya-Shugg combination or as substrate 6’ upper prepreg in the second alternative implementation of the Oya-Shugg combination. *Supra*, Element [8d]; APPLE-1003, ¶155. In both implementations, the “*third insulating-material layer*” (i.e., substrate 5’ or substrate 6’ upper prepreg) is also spaced apart from the device 11 (*component*).



First Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))



Second Alternative Implementation of the Oya-Shugg Combination

(APPLE-1004, FIG. 7 (modified and annotated))

Claim [14]

The Oya-Shugg combination renders Claim [14] obvious. APPLE-1003, ¶156. As discussed above, Oya teaches that the substrates of its wiring board, e.g., substrates 6' and 7', can be “prepreg” and “an epoxy resin.” APPLE-1004, ¶¶[0045], [0051]. A POSITA would have known that “prepreg” was a composite material commonly used for circuit board substrates made of pre-impregnated fibers mixed with a partially cured resin. APPLE-1006, 289-290 (“The basic materials for making industrial laminates are called *prepregs*. A prepreg is composed of a substrate, usually paper, cotton, or glass fabric, impregnated with a

thermosetting resin, generally phenolic, epoxy, or melamine.”), 291 (“Epoxy resin glass-reinforced laminates ... are used extensively as substrates for printed circuits.”), 303-304; APPLE-1003, ¶156; *see also* APPLE-1019, 239 (“[g]lass-fiber cloth pre-impregnated with epoxy-resin [was] ... widely used as a composite electrical insulation in various electrical industrial products”). Consistent with the conventional understanding of prepreg, Oya explicitly confirms that the substrates can be “composed of glass fiber impregnated with a resin.” APPLE-1004, ¶[0060]. In the combination, it would have been obvious for the second and third insulating material layers to be prepreg based on Shugg’s teachings as well. *See, e.g.*, 289 (“bonding layers of prepreg between circuit layers”); *supra*, Element [8d]; APPLE-1003, ¶156. Because prepreg is a composite material that is itself composed of multiple materials, substrate 7’ (***first insulating-material layer***) and the “***third insulating-material layer***” (e.g., substrate 5’ in the first alternative implementation of the combination or substrate 6’ upper prepreg in the second alternative implementation of the combination) both comprise a first material such as glass fiber that is different than a second material such as resin of the ***second insulating-material layer*** (e.g., substrate 6’ in the first alternative implementation of the combination or substrate 6’ lower prepreg in the second alternative implementation

of the combination) as claimed.¹⁶ APPLE-1003, ¶156, 157.

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. Section 325(d)

This Petition does not present a situation where “the same or substantially the same prior art or arguments” were previously considered by the Office to warrant denial under § 325(d). None of Tsubosaki010, Tsubosaki405, or Shugg were cited to the Office during prosecution of the ’816 Patent. Although Oya was cited in an IDS during prosecution, and is therefore one of dozens of references listed on the face of the ’816 Patent, Oya was never substantively addressed in any office action or remarks in connection with original examination of the ’816 Patent. APPLE-1001, Cover; EX1002; *supra*, §III.B. Nor was Oya considered in combination with Shugg as set forth in Ground 2. For this reason alone, such

¹⁶ *Supra*, Footnote 15. For reasons similar to those discussed above with respect to claim 7, claim 14 is clear that the first and third insulating-material layers need only *include* a first material that is different from a second material included in the second insulating-material layer—although the first and third insulating-material layers need not consist only of material that is different from any/all material of the second insulating-material layer. APPLE-1003, 156, n. 12.

“new, noncumulative prior art asserted in the Petition” weighs against discretionary denial. *Oticon Medical AB v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (Oct. 16, 2019 (§§II.B and II.C precedential)). Even if the Examiner had considered any prior art containing teachings cumulative to the teachings of the references cited in this Petition, the compelling merits of this Petition demonstrate that the Examiner would have committed material error in allowing the Challenged Claims over such references. These circumstances all counsel against denial under §325(d).

B. Section 314(a)

This Petition’s merits are compelling, and the evidence presented herein is substantial, counseling against discretionary denial under *Fintiv*. SAMSUNG-1101 4-5. Moreover, the *Fintiv* factors counsel against denial. The *Fintiv* factors weigh against exercising discretionary denial. This Petition’s merits are compelling, and the evidence presented herein is substantial, counseling against discretionary denial under *Fintiv*. The related litigation remains in its infancy.

Factor 1 is neutral or favors institution. A motion to transfer to the Northern District of California is pending. While a motion to stay has not been filed, even without inferring how the district court would rule, the pending motions at least increase the likelihood of a stay. *Hulu LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Factor 2 favors institution. Even if the district court proceeding is not transferred, the Board will likely issue its final written decision by about August 2026, several months before the median time-to-trial in WDTX (November, 2026, based on median time of 33.1 months). The trial date is also uncertain and subject to change due to a number of factors, including Apple's pending motion to transfer.

Factor 3 favors institution because Petitioner has diligently filed this Petition while the litigation remains in its early stages. As noted above, Apple's motion to transfer remains pending.

Factors 4 and 5 are neutral or favor institution. Resolution is expected well before a decision in the district court, which mitigates against duplication of effort and serves efficiency and integrity goals. The same parties are in the co-pending litigation.

Factor 6 favors institution because this Petition's merits are compelling for the reasons described herein, demonstrating unpatentability based on multiple independent grounds. The strength of the merits alone outweigh any inefficiencies borne of parallel litigation.

VI. PAYMENT OF FEES – 37 C.F.R. § 42.103

Petitioner authorizes the Patent and Trademark Office to charge any fees to Deposit Account No. 06-1050.

VII. CONCLUSION

The Challenged Claims are unpatentable based on Grounds 1A-2. The Board should institute IPR and cancel all Challenged Claims.

VIII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Apple, Inc. is the Petitioner and the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates, or petitions for *inter partes* review for the '816 Patent. The '816 Patent is the subject of a civil action in *ImberaTek LLC v. Apple Inc.*, 1-24-cv-00129 (WDTX), filed February 5, 2024.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR50095-0199IP1@fr.com.

Respectfully submitted,

Dated: 2/6/2025

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F: 877-769-7945

(Control No. IPR2025-00584)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,983 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: 2/6/2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 6, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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