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POLYSILICON EMITTERS FOR SILICON CONCENTRATOR SOLAR CELLS

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ABSTRACT

Polysilicon emitters with a thermally grown interfacial oxide are examined in great detail. Both J_o and ρ_c are measured for the polysilicon emitter (contact) which is annealed under various conditions. $J_o \leq 5 \times 10^{-14}$ A/cm^2 and $\rho_c \sim 1 \times 10^{-5}$ Ω-cm^2 are obtained for both n- and p-type polysilicon emitters. The results also indicate that the interfacial oxide is only broken by a very small fraction in order to have $\rho_c \sim 1 \times 10^{-5}$ Ω-cm^2. Under such a condition, J_o is primarily dominated by the recombination at the oxide interface.

INTRODUCTION

Polysilicon emitters, because of their important applications in high speed bipolar transistors, have been widely studied. It was found that, between the polysilicon and the substrate, there always exists a very thin oxide (interfacial oxide), which can be as a by-product of the cleaning process or is grown intentionally [1,2,3,4,5,6,7]. In either case, the oxide is not thermally stable; *i.e.*, it tends to break up during high temperature anneals [1,2,3,4,5,6,7]. The breakup of the interfacial oxide has direct impact on both majority and minority carrier transport in the polysilicon emitter. This can be seen from the dependence of the specific contact resistivity (ρ_c) [6] and the the emitter saturation current density (J_o) [1,2,3,4,5,6,7] upon either the anneal condition or the oxide integrity. When the effect of the interfacial oxide is negligible, such as when the interfacial oxide loses its integrity in high temperature anneals, the ρ_c is low ($\sim 2 \times 10^{-7}$ Ω-cm^2) [6] and the J_o is high ($\sim 1 \times 10^{-12}$) [1,3]. Conversely, when both carriers are mostly blocked by the interfacial oxide, like for an intact chemical oxide ($\sim$15 Å), the ρ_c is high and the J_o is low. Typically, $\rho_c \geq 1 \times 10^{-4}$ Ω-cm^2, and the corresponding $J_o \sim 1 \times 10^{-14}$ A/cm^2 have been observed on the n-type polysilicon emitter [1,5,6].

With the extent of the oxide breakup between these two extremes, various combinations of ρ_c and J_o can be obtained. It is of particular interest to know the ρ_c and the corresponding J_o when only a small fraction of the interfacial oxide is broken. For silicon solar cells operated under high concentrated sunlight, the emitter recombination is one of the main recombination that limit the solar cell performance [8]. This is because the diffused-emitter, which is formed with dopant diffusion into the base (substrate), has high J_o ($=4.5 \times 10^{-13}$ A/cm^2). Consequently, the cell performance can be improved if the diffused-emitter is replaced with the polysilicon emitter, of which the J_o is less than 4.5×10^{-13} A/cm^2 and the ρ_c is low enough.

In this paper, detailed calibrations for the polysilicon emitter with a thermally grown interfacial oxide is presented. Compared with the the chemical oxide, the thermal oxide appears to be more robust to the high temperature anneal. Consequently, this lends more controllability on the oxide breakup process. In addition, two separate anneal steps were used in order to avoid any possible interference from the dopant diffusion. It has been reported that the interfacial oxide tends to break up more rapidly with the existence of dopant [3,5]. Moreover, J_o also depends on the surface dopant concentration and the emitter depth [9]. In order to see the effect of the oxide breakup on J_o and ρ_c alone, it is therefore desirable to separate these two processes. The first-step anneal, which serves to break the oxide, was performed at higher temperature than that for the second-step anneal which aims for the dopant drive-in.

EXPERIMENTAL

Procedures

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In this work, the J_o and ρ_c were measured independently for each type of polysilicon emitter (or contact). J_o was measured with photoconductivity decay method which has been reported elsewhere [10]. Because high bulk lifetime is needed for such a measurement, the samples were prepared with high resistivity (>100 Ω-cm) FZ wafers. In contrast, ρ_c was measured on devices made on CZ wafers of which resistivity is 0.28 and 0.5 Ω-cm for p- and n- type respectively. The device for ρ_c-measurement is shown in Fig. 1 schematically. Except for the pattern-definition steps which were not required for J_o-measurement samples, the two sets of wafers were always processed together. The process sequence is shown as followings:

1. Field oxidation (2000 Å)*.
2. Polysilicon-substrate contact opening*.
3. Thin thermal oxide growth at 800 °C*. (10-minute oxygen flow)
4. Polysilicon deposition (6000 Å) and first-step anneal (1050 °C)*.
5. First-step anneal *.
6. Polysilicon finger definition.
7. Undoped glass deposition (2000 Å).
8. Metal-polysilicon and metal-substrate contact opening.
9. Doped glass deposition on both sides of the wafer*.
10. Drive-in; 900-1000 °C*.
11. Doped glass stripping and Al-1% Si alloy deposition.
12. Metal finger definition.

Note that the steps marked with "*" are the steps for J_o-measurement samples. In addition, the J_o-samples are divided into two sets; one set of samples had an additional 400 °C-30 min forming gas anneal (FGA), the other did not. The growth of thin oxide was carried out with 200 sccm oxygen and 5 slm argon mixture. Typically, oxide thickness less than 20 Å was measured with ellipsometer. In step 2, a series of square contacts of size between 1 and 64 μm are opened for polysilicon-substrate contacts.

ρ_c Measurement

As shown in Fig. 1, the voltage difference, V_{ab}, between probe A and B is caused by several components of the series resistance along the current loop. They are the resistance imposed by the bulk of the polysilicon and the wafer, the metal-polysilicon contact resistance, and the polysilicon-substrate contact resistance. The potential drop across the polysilicon film is conceivably negligible because the film is heavily doped and very thin. The metal-polysilicon contact resistance is actually measured on the similar device (four-terminal resistor [11]) next to the device shown in the figure. Typically, the ρ_c of the metal-polysilicon contact is less than 1×10^{-6} Ω-cm^2. With such low ρ_c and large contact area between the metal and the polysilicon, the metal-polysilicon contact resistance can be ignored as well. As a result, the series resistance derived from V_{ab}/I is essentially determined by two terms; the bulk resistance of the silicon substrate and the polysilicon-substrate contact resistance. Such a series resistance can be expressed as a function of the size of the polysilicon-substrate square contact.

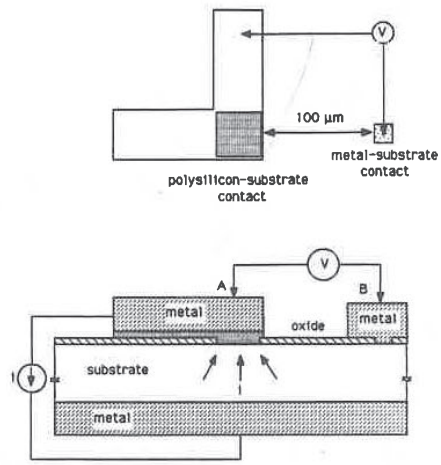

Figure 1: The device structure for the specific contact resistivity measurement.

$$R = C\frac{\rho}{d} + \frac{\rho_c}{d^2}, \quad (1)$$

or

$$R_c = R \times d^2 = \rho_c + C\rho\, d; \quad (2)$$

where C is a constant that accounts for the contact geometry factor, ρ is the substrate resistivity, d is the width of the square contact, and ρ_c is the specific contact resistivity of the polysilicon-substrate contact. The contact size dependence of the last term in Eqn. (2) results from the crowding effect as the current flows toward the polysilicon-substrate contact. It is obvious that, from Eqn. (2), the ρ_c can be derived from the plot of R_c versus d which is obtained by measuring the series resistance of contacts of different sizes.

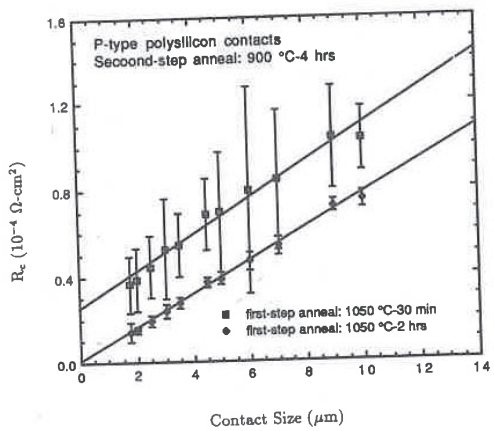

Figure 2: The R_c versus the contact size for p-type polysilicon contacts of different first-step anneals.

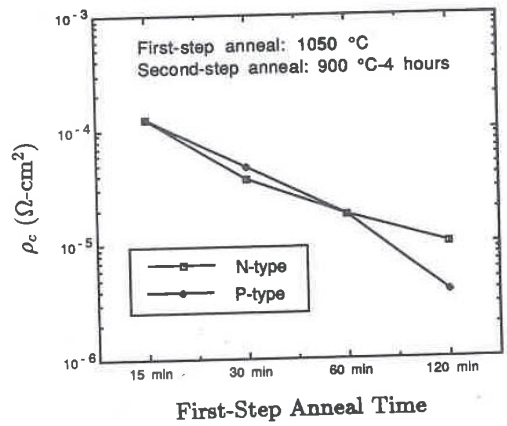

Figure 3: ρ_c of both n- and p- type polysilicon-substrate contacts is shown as a function of the time of the first-step anneal.

RESULTS AND DISCUSSIONS

Fig. 2 shows two R_c-plots for the p-type polysilicon contacts. One has the first-step anneal at 1050 °C for 30 minutes, the other has 1050 °C for 2 hours. Each data point is the average of 16 measurements across the wafer and the error bar is drawn with 4 standard deviations. Since devices were made on the wafers of about the same resistivity, the slopes of the linear-fit lines are almost identical. Note that, the devices that received a 30-minute first-step anneal have higher intercepts than those that received a 2-hour first-step anneal. This indicates that more oxide breakup occurs when the anneal time increases. Another characteristic of the interfacial oxide breakup can also be seen from the spread in the data (the length of the error bar). The magnitude of the error bar is not due to the measurement uncertainty; instead, it results from the random distribution of the oxide breakup. When only a very small fraction of the interfacial oxide is broken, it is possible that the interfacial oxide on each contact may not be broken equally. Consequently, this gives rise to the fluctuation of the resistance measured. On the other hand, the fluctuation will be subdued when more oxide is broken. This explains the different appearance of error bars observed between these two sets of data.

To see how the J_o and the ρ_c is affected by the first-step anneal, one set of samples (and device wafers) were first annealed at 1050 °C for various lengths of time (first-step anneal). After the doped-glass deposition, they were all annealed at 900 °C for 4 hours. The ρ_c measured from the device and the J_o measured from the photoconductivity decay are presented in the following figures.

In Fig. 3, ρ_c is plotted against the time of the first-step anneal for both types. Note that the ρ_c decreases as the anneal time increases. In addition, ρ_c measured from both n- and p- type devices are more or less the same, except those annealed with 120 minutes. The similarity of ρ_c between the n- and the p- type contact also indicates that the interaction between the dopant and the interfacial oxide is negligible; since such an interaction, if exists, would cause the ρ_c of the p-type to be lower [6].

The effects of the first-step anneal on J_o are presented in Fig. 4 and 5 for the n-type and the p-type polysilicon emitters respectively. In each figure, two sets of data are shown: the one with an FGA, and the one without. For the samples with an FGA, the J_o is significantly less than that without FGA for the same anneal condition. This indicates that the recombination

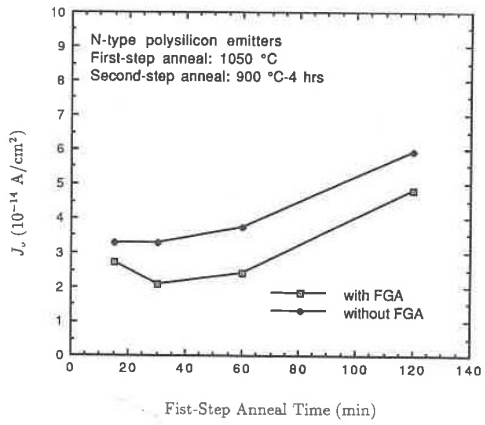

Figure 4: The J_o versus the first-step anneal time for n-type polysilicon emitters.

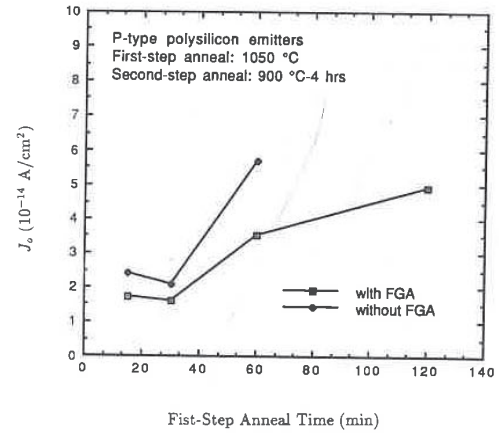

Figure 5: The J_o versus the first-step anneal time for p-type polysilicon emitters.

at the oxide interface is, at least, one of the dominant mechanisms for the emitter recombination. It is also important to note that the J_o of the p-type polysilicon emitter (Fig 5) appears to be much lower than what has been previously reported [1]. This may have to do to the use of thermal oxide as the interfacial layer in our samples. Either the thermal oxide is most robust during the high temperature anneal or the thermal oxide has lower interface defect state density (D_{it}) compared to the chemical oxide. Another interesting thing in these figures is that the J_o of the sample that received a 15-minute anneal is higher than the sample that received a 30-minute anneal. Moreover, such a behavior occurs in both the n- and the p- type samples. The possible explanation is that the interfacial oxide quality is improved by the high temperature anneal. This is not too surprising because the oxide was grown around 800 °C, in which higher D_{it} is expected [12,13]. Other than that, the J_o of both types appears to increase slowly with the anneal time. In addition, because the dominant recombination is likely at the oxide interface, it implies that the oxide must only be broken by very a small fraction, which is in consistent with what was observed in Fig. 2.

The effect of the second-step anneal (dopant drive-in) on both the J_o and the ρ_c were also investigated. All samples (and devices) received a first-step anneal at 1050 °C for one hour, followed with various treatments in the second-step anneal. The results are summarized in Table 1. The label on the right most column represents the second-step anneal condition of that sample. As shown in the table, the J_o increases with the temperature and time of the second-step anneal. In the meantime, the ρ_c decreases as the drive-in temperature increases. Considering the significant increase of J_o caused by increasing the drive-in temperature from 900 to 1000 °C, it is beneficial to use the two-step anneal to optimize J_o.

In Fig. 3, the decrease of ρ_c with the anneal time is what would be expected from the gradual breakup of the interfacial oxide. This is in consistent with the increase of J_o shown in Fig. 4 and Fig. 5, since J_o depends on the oxide integrity in the opposite way. This is especially clear when both ρ_c and J_o are plotted together. Fig. 6 is the ρ_c versus J_o plot for all the results obtained in this experiment. The inset is the list of the label

Table 1: The effect of the second-step anneal on J_o and ρ_c.

	N-type		P-type	
	$J_{o,e}$ ($\times 10^{-14}$ A/cm^2)	ρ_c ($\mu\Omega$-cm^2)	$J_{o,e}$ ($\times 10^{-14}$ A/cm^2)	ρ_c ($\mu\Omega$-cm^2)
900 °C-4 hour	2.4	18	3.5	18
1000 °C-30 min	4.5	~ 6	8.2	3.8
1000 °C-60 min	7.9		10.5	

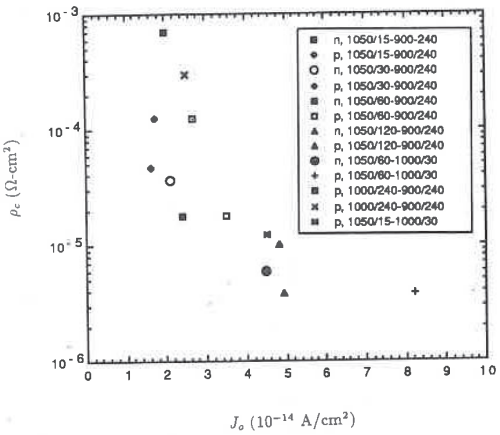

Figure 6: ρ_c-J_o of this work.

for each point. It specifies the type of polysilicon emitter, the first-step anneal (temperature/minute), and the second-step anneal (temperature/minute). As shown in the figure, the data runs from the upper-left corner to the lower-right corner which is similar to that reported by Crabbé [6] and is the typical trend when both ρ_c and J_o are regulated by the extent of oxide breakup. Nevertheless, from left to right, two distinct regimes are shown in the figure. In one regime, J_o is almost constant while ρ_c drops drastically. In the other regime, ρ_c decreases very slowly and J_o increases in much faster pace. In the first regime, that the J_o is inert to the oxide breakup is because the extent of the oxide breakup is very small such that the J_o is still dominated by the recombinations at the oxide interface and in the singly-crystal outdiffusion. On the other hand, the drastic change of the ρ_c can be attributed to the transition of the majority carrier transport from the tunneling to the channel resistance. When the interfacial oxide is intact, tunneling is the only process available for the majority carriers to pass through the interfacial oxide. This usually results in a high contact resistance because of low tunneling probability. As the oxide starts to break up, additional highly conductive channels are created due to the intimate contacts formed between the polysilicon and the substrate in the broken regions [3,4,5]. A drastic change of ρ_c is observed when more currents flow through those channels. In the other regime, J_o starts to increase because the recombination in the polysilicon becomes comparable to the recombination mentioned previously. On the other hand, the slow decrease of the ρ_c in this regime is because the majority carrier transport is completely dominated by the channel resistance. The increase of the oxide breakup can be thought as more parallel resistors added together; consequently, a significant change of ρ_c will not be observed.

The data shown in Fig. 6 are quite useful for silicon solar cells. First, most of J_o are below 5×10^{-14} A/cm^2 which is about one order magnitude lower than that of diffused-emitters. Second, most of ρ_c are also lower than 5×10^{-5} Ω-cm^2. This means that the potential drop across the contact is negligible as long as the current density is less than 100 A/cm^2. It is interesting to see how much of the cell efficiency can be improved with polysilicon emitters of characteristics given here. With the cell modeling, which is similar to the one reported by Sinton [8], more than one absolute percent of the cell efficiency is obtained for a backside contact solar cell with polysilicon emitters with characteristics shown here (J_o=2×10^{-14} A/cm^2 for the n-type, J_o=3.5×10^{-14} A/cm^2 for the p-type, and ρ_c=1×10^{-5} Ω-cm^2 for both types).

CONCLUSIONS

To conclude, we showed that polysilicon emitters with low J_o and ρ_c can be obtained with a very small fraction of interfacial oxide breakup. Typically, $\rho_c \sim 1 \times 10^{-5}$ Ω-cm^2 and $J_o \leq 5 \times 10^{-14}$ A/cm^2 are obtained for both n- and p- type polysilicon emitters. From the cell modeling, polysilicon emitters with these qualities can be quite useful for silicon concentrator solar cells. Because only small fraction of interfacial oxide is broken, the J_o is primarily dominated by the recombination at the oxide interface and in the single-crystal diffusion region. Consequently, an interfacial oxide of good quality is important to obtain low J_o. Our results also indicates that ρ_c drops drastically when the oxide starts to breakup. This is explained by the transition of the dominant majority-carrier transport from the tunneling to the channel resistance.

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