Handbook of Photovoltaic Science and Engineering

Edited by

Antonio Luque
Instituto de Energía Solar, Universidad Politécnica de Madrid, Spain

and

Steven Hegedus
Institute of Energy Conversion, University of Delaware, USA



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The FF is a function of V_{OC} (equation 3.134), so

$$\eta^{\text{Xsuns}} = \eta^{\text{1sun}} \left(\frac{FF^{\text{Xsuns}}}{FF^{\text{1sun}}} \right) \left(1 + \frac{\dfrac{kT}{q} \ln \text{X}}{V_{\text{OC}}^{\text{1sun}}} \right). \tag{3.165}$$

Both factors multiplying the 1 sun efficiency increase as the illumination concentration increases. Therefore, the efficiency of concentrator cells increases as the illumination concentration increases, as shown in Figure 3.25.

Of course, there are many obstacles to achieving this. Concentrator cells must be cooled, since an increase in operating temperature reduces V_{OC}, and hence the cell efficiency. The FF^{Xsuns} eventually decreases with increasing X and current due to the parasitic series resistance. Concentrator solar cells are discussed in more detail in Chapter 11.

3.5.6 High-level Injection

In high-level injection, the excess carrier concentrations greatly exceed the doping in the base region, so $\Delta p \approx \Delta n \approx n \approx p$ if the carriers are moving generally in the same direction. This occurs with back-contact solar cells, such as the silicon point-contact solar

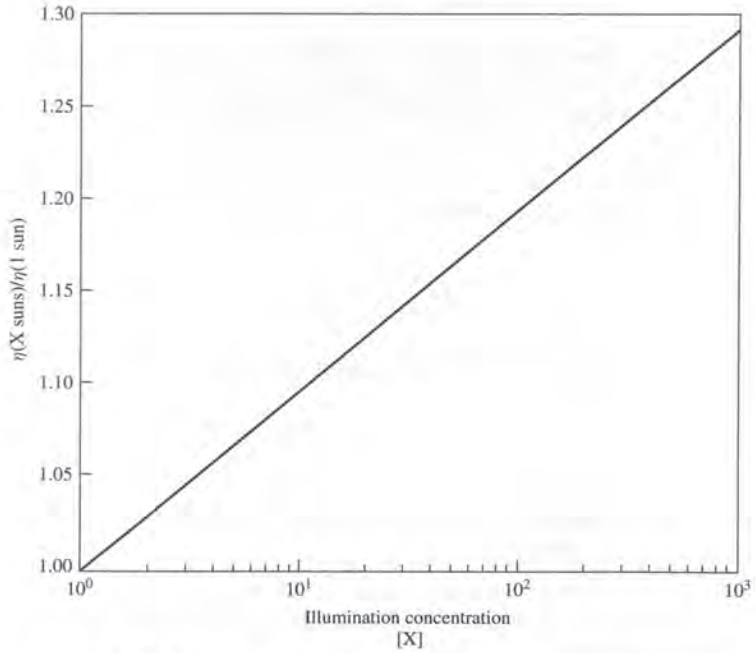


Figure 3.25 Relative efficiency as a function of illumination concentration

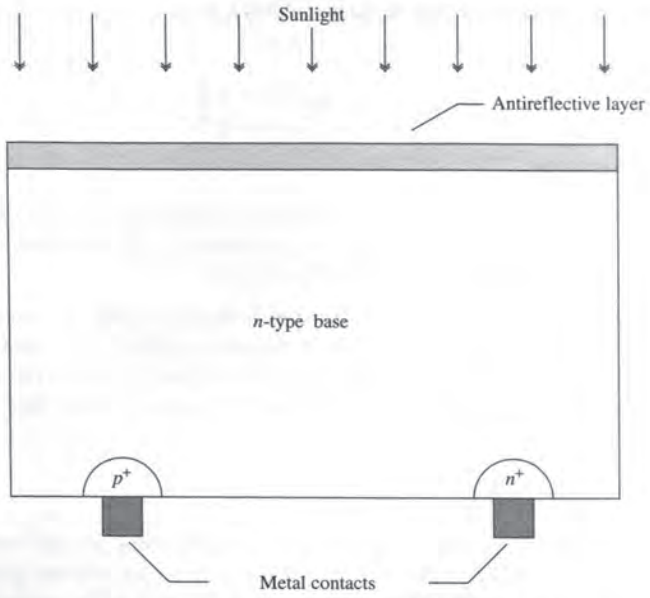


Figure 3.26 Schematic of a back-contact solar cell

cell [22], as illustrated in Figure 3.26. Since both electrical contacts are on the back, there is no grid shadowing. These cells are typically used in concentrator application and high-level injection conditions pervade. Assuming high-level injection, a simple analysis is possible.

Returning to equations (3.76) and (3.77), it can be seen that in high-level injection, the electric field can be eliminated (it is not necessarily zero), resulting in the ambipolar diffusion equation

$$D_a \frac{d^2 p}{dx^2} - \frac{p}{\tau_n + \tau_p} = -G(x), \tag{3.166}$$

where the ambipolar diffusion coefficient is given by

$$D_a = \frac{2D_n D_p}{D_n + D_p}. \tag{3.167}$$

The ambipolar diffusion coefficient is always less than the larger diffusion coefficient and greater than the smaller one.

In silicon, where $D_n/D_p \approx 3$ over a wide range of doping, the ambipolar diffusion coefficient is $D_a \approx 3/2D_p \approx 1/2D_n$ and, if we also assume $\tau_p \approx \tau_n$, the ambipolar diffusion length is

$$L_a \approx \sqrt{3} L_p \approx L_n. \tag{3.168}$$

Thus, the increased high-injection lifetime (see equation 3.40) offsets the reduced ambipolar diffusion coefficient.

It is crucial that the front surface of a back-contacted cell be well passivated, so we will assume that $S_F = 0$. We will further assume that optical generation is uniform throughout the base region. At open circuit, with these assumptions, $d^2p/dx^2 = 0$ and therefore

$$V_{OC} = \frac{2kT}{q} \ln\left[\frac{G(\tau_n + \tau_p)}{n_i}\right]. \tag{3.169}$$

The short-circuit current (with $p \simeq 0$ at the back of the cell) is

$$I_{SC} = qAL_aG \sinh(W_B/L_a) \tag{3.170}$$

which, when $L_a \gg W_B$, becomes

$$I_{SC} = qAW_BG. \tag{3.171}$$

3.5.7 *p-i-n* Solar Cells

The *p-i-n* solar cell takes advantage of the fact that in many semiconductor materials, especially direct band gap semiconductors (i.e. large absorption coefficient), most of the electron–hole pairs are created very near the surface. If an intrinsic (undoped) layer is placed between the (very thin) *n* and *p* regions, the depletion region thickness is the most significant fraction of the total solar cell thickness, as illustrated in Figure 3.27. Carrier collection is now aided by the electric field in the depletion region, which helps offset the low lifetimes in some materials, such as amorphous silicon (see Chapter 12). The $I-V$ characteristic of a *p-i-n* solar cell can be described with minor modifications to the previously derived expressions. The most significant modification is to equation (3.129) where the depletion width is now written as

$$W_D = \chi_N + W_I + \chi_P \tag{3.172}$$

where W_I is the thickness of the intrinsic layer. Since χ_N and χ_P are very thin, short-base approximations are in order for equations (3.127) and (3.128). Also, there is no BSF ($S_{BSF} \to \infty$).

3.5.8 Detailed Numerical Modeling

While analytic solutions such as those discussed thus far in this chapter provide an intuitive understanding of solar cell performance and are therefore very important, they are limited in their accuracy due to the many simplifying assumptions that must be made in order to obtain them. It is rather straightforward to solve the semiconductor equations numerically without the need to make so many simplifications. Several computer codes have been written that solve the semiconductor equations for the explicit purpose of modeling solar cells – PC-1D [23], AMPS [24], ADEPT [25], and its predecessors [16, 26, 27], for example. The basic design of these computer programs is very similar. The semiconductor

7

Crystalline Silicon Solar Cells and Modules

Ignacio Tobías[1], Carlos del Cañizo[1] and Jesús Alonso[2]

[1]*Universidad Politécnica de Madrid, Madrid, Spain,* [2]*Isofotón S.A., Málaga, Spain*

7.1 INTRODUCTION

Crystalline silicon solar cells and modules have dominated photovoltaic (PV) technology from the beginning. They constitute more than 85% of the PV market today, and although their decline in favor of other technologies has been announced a number of times, they presumably will retain their leading role for a time, at least for the next decade.

One of the reasons for crystalline silicon to be dominant in photovoltaics is the fact that microelectronics has developed silicon technology greatly. On the one hand, not only has the PV community benefited from the accumulated knowledge but also silicon feedstock and second-hand equipment have been acquired at reasonable prices. On the other hand, Microelectronics has taken advantage of some innovations and developments proposed in Photovoltaics.

For several decades, the terrestrial PV market has been dominated by *p*-type Czochralski silicon substrates. Continuous improvements in performance, yields and reliability have allowed an important cost reduction and the subsequent expansion of the PV market. Because of the lower cost of mc-Si wafers, multicrystalline (MC) silicon cells emerged in the 1980s as an alternative to single-crystal ones. However, their lower quality precluded the achievement of similar efficiencies to those of Cz, so that the figure of merit \$ W^{-1} has been quite similar for both technologies over a long time (see Table 7.1).

Deeper understanding of the physics and optics of the mc-Si material led to improved device design, which allowed a wider spread of the technology. A combination

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Table 7.1 Breakdown of costs of fabrication of single-crystalline (SX) and multicrystalline (MC) solar cells (corresponding to year 1990) [1]

Item	SX	MC
Pure Si	38	38
Ingot formation	115	35
Sawing	77	77
Wafer cost	**230**	**150**
Cell fabrication	80	80
Total components	310	230
Yield	0.95	0.9
Cell cost	**326**	**256**
Module assembling	75	75
Lamination	75	75
Module cost (Euro m^{-2})	**476**	**406**
Efficiency	0.14	0.12
Module cost (Euro Wp^{-1})	**3.40**	**3.38**

Table 7.2 Market share of monocrystalline and multicrystalline solar cells [2]

Year	Cz-Si solar cells		MC-Si solar cells	
	Output [MW]	Market share [%]	Output [MW]	Market share [%]
1996	48.7	55	28.4	32
2000	92.0	32	146.7	51

of improved material quality and material processing has allowed higher efficiencies at a still lower cost, increasing the share of MC in the PV market, well ahead of monocrystalline. Recent evolution of the market can be seen in Table 7.2 [2].

This chapter offers an overview of silicon solar cell and module technology. First, Si properties justifying its use as photovoltaic material are presented. Then, design of Si solar cells is reviewed, highlighting the benefits and limits of different approaches. Manufacturing processes are described, paying special attention to technologies that are currently implemented at the industrial level, mostly based on screen-printing metallization technology. Considerations of ways of improving solar cell technology are also specified. Peculiarities of multicrystalline material are explained in Section 7.6, while other approaches that are already in industrial production are also described briefly. Next, crystalline Si modules are reviewed, pertaining to electrical performance, fabrication sequence and reliability concerns.

7.2 CRYSTALLINE SILICON AS A PHOTOVOLTAIC MATERIAL

7.2.1 Bulk Properties

Crystalline silicon has a fundamental indirect band gap $E_G = 1.17$ eV and a direct gap above 3 eV [3] at ambient temperature. These characteristics determine the variation of optical properties of Si with wavelength, including the low absorption coefficient for carrier generation for near band gap photons [4]. At short ultraviolet (UV) wavelengths in the solar spectrum, the generation of two electron–hole pairs by one photon seems possible, though quantitatively this is a small effect [5]; at the other extreme of the spectrum parasitic free-carrier absorption competes with band-to-band generation [6]. The intrinsic concentration is another important parameter related to the band structure; it links carrier disequilibrium with voltage [7].

At high carrier densities, doping- or excitation-induced, the band structure is altered leading to an increase in the effective intrinsic concentration: this is one of the so-called heavy doping effects that degrade the PV quality of highly doped regions [8].

Recombination in Si is usually dominated by recombination at defects, described with Shockley–Read–Hall (SRH) lifetimes. The associated lifetime τ (which can also be described in terms of diffusion length L) increases for good quality materials. Auger recombination, on the contrary, is a fundamental process that becomes important at high-carrier concentration [9]. The Auger coefficients are reported to be higher at moderate carrier densities due to excitonic effects [10]. Band-to-band direct recombination is also a fundamental process but quantitatively negligible (it is instructive, however, to notice that record-efficiency solar cells have such extraordinarily low SRH recombination levels that they perform as 1%-efficient light-emitting diodes, that is, radiative recombination is significant [11]).

At low and moderate doping, electrons present mobilities about three times higher than holes, both limited by phonon scattering. Impurity scattering dominates for higher doping densities [12, 13]. Carrier–carrier scattering affects transport properties in highly injected material [14].

7.2.2 Surfaces

7.2.2.1 Contacts

Contacts are structures built on a semiconductor surface that allow charge carriers to flow between the semiconductor and the external circuit. In solar cells, contacts are required to extract the photogenerated carriers from the absorbing semiconductor substrate. They should be selective, that is, should allow one type of carrier to flow from Si to metal without energy loss while blocking the transport of carriers of the opposite type.

Direct Si-metal contacts, in general, do not behave this way. As an exception, good hole contacts to highly doped p-Si substrates with aluminum are possible. But the

most used approach is to create heavily doped regions under the metal, p-type for hole extraction and n-type for electron extraction. Majority carriers in this region can flow through the contact with low voltage loss. The transport of minority carriers is described by a surface recombination velocity (SRV), S. Although the SRV is high, limited only by thermal diffusion so that $S \cong 10^6$ cm·s^{-1} [15], the concentration of minority carriers, for a given pn product, is suppressed by the high doping and the flow is reduced.

As will be seen later on, the contact for the minority carriers is usually placed at the front (illuminated) face of the substrate, and the corresponding heavily doped layer is usually called *emitter*. The doped region under the majority carrier contact at the back is called a *Back Surface Field* (BSF).

Recombination at these heavily doped regions is described by the saturation current density J_0 that includes volume and true contact recombination. Their thickness w should be much higher than the minority-carrier diffusion length L so that few excess carriers reach the contact, and the doping level must be very high to decrease contact resistance and the minority-carrier concentration, although heavy doping effects may limit the doping level advisable for such regions. The recombination activity of BSF layers is often described in terms of an effective SRV instead of the saturation current density.

Typical 10^{-13} to 10^{-12} A·cm^{-2} J_0 values are achieved [16, 17]. Diffused phosphorus is used for n-contacts. Aluminum alloying has the advantages over boron for p-contacts that very thick p^+ layers can be formed in a short time at moderate temperatures and that gettering action is achieved [18]. As a shortcoming, the p^+ layer is nonhomogeneous and can even be locally absent; the obtained J_0 is larger than expected for a uniform layer. In comparison to aluminum, boron offers higher doping levels because of a larger solubility [19] and transparency to light so that it can also be used at illuminated surfaces.

Other structures have been tested to obtain selective contacts: metal-insulator-semiconductor (MIS) contacts [20], polysilicon contacts [21] and heterojunction to a-Si or other wide band gap material [22].

7.2.2.2 Noncontacted surfaces

Because of the severe alteration of the bonding of Si atoms, a large number of band gap states exist at a bare Si surface which, acting as SRH recombination centers, make the SRV very large, around 10^5 cm·s^{-1} [23, 24]. In order to reduce surface recombination, two main approaches are followed [25].

In the first one, the density of electron surface states in the gap is decreased. This is accomplished by depositing or growing a layer of an appropriate material that partially restores the bonding environment of surface Si atoms. This material must be an insulator.

Thermal SiO_x is grown in an oxygen-rich atmosphere at the expense of substrate Si atoms at high temperatures around 1000°C. SiN_x is deposited by plasma-enhanced chemical vapor deposition (PECVD) [26] at low temperatures between 300 and 400°C range. The quality of both techniques is very sensitive to subsequent treatments, with hydrogen playing a major role in obtaining low SRV values below 100 cm·s^{-1}.

As a general rule, S increases with the doping of the substrate [23, 24]. It also depends on the injection level and doping type, because the interfaces contain positive

charges that affect the number of carriers at the surface, and because the capture probability for electrons and holes is different [27]. N-type or intrinsic surfaces are usually better than p-type ones. Stability under UV exposure is another fundamental concern.

In the second approach, the excess carrier density at the interface is decreased relative to the bulk. This effect has already been commented upon with respect to contacts and results in a reduced effective SRV at the bulk edge of the corresponding space charge region. It can be produced by charges in the surface layer, by the electrostatics associated to a MOS structure [28] or by doping.

The surface layer can be accumulated or inverted, or, correspondingly, doped with the same or the opposite type of the substrate. Its recombination activity is better described by a constant saturation current density, J_0, whose minimization follows the same rules as mentioned for the contacts if S at the surface is high. On the contrary, if S is low when compared to D/L for minority carriers (with D the diffusion constant and L the diffusion length in the substrate) in the surface layer, it is better for it to be thin or "transparent" to minority-carrier flow ($w < L$). The optimum doping level is a compromise between reduction of the excess carriers, and heavy doping effects and the increase of the SRV with doping. Moderate doping levels are favored in this case. Under passivated surfaces, J_0 values around 10^{-14} A·cm^{-2} are achievable, with phosphorus-doped substrates giving better results than boron-doped ones [16, 17].

In conclusion, recombination at a noncontacted surface can be made much smaller than at a metallized one, and this has a deep influence in the evolution of Si solar cell design.

7.3 CRYSTALLINE SILICON SOLAR CELLS

7.3.1 Cell Structure

Several studies have been carried out to find the limiting efficiency and the optimum structure of a-Si solar cell [29–31]. All avoidable losses are assumed to be suppressed:

1. no reflection losses and maximum absorption as achieved by ideal light-trapping techniques,
2. minimum recombination: SRH and surface recombination are assumed avoidable and only Auger recombination remains,
3. the contacts are ideal: neither shading nor series resistance losses,
4. no transport losses in the substrate: the carrier profiles in the substrate are flat so that recombination is the minimum possible for a given voltage.

The optimum cell should use intrinsic material, to minimize Auger recombination and free-carrier absorption, and should be around 80-μm thick, the result of the trade-off between absorption and recombination. It could attain nearly 29% efficiency at one sun AM1.5 Global, 25°C [30].

This ideal case does not tell us where to put the contacts. To realize Condition 4 mentioned above, the contacts should be located at the illuminated or the front face, closest to photogeneration (Figure 7.1a). Because of metal shading losses this threatens

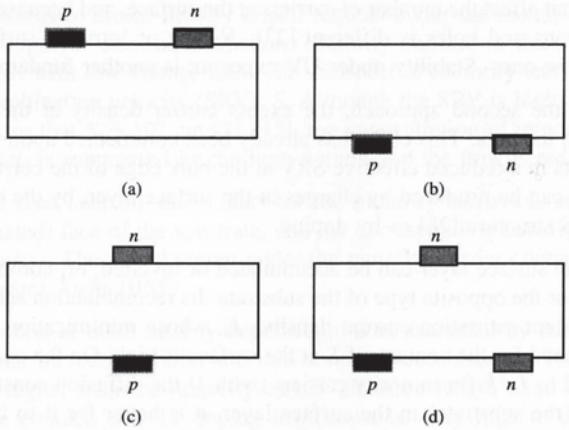


Figure 7.1 Contacting structures: (a) both contacts at the front; and (b) at the back; (c) both faces contacted; and (d) one carrier extracted at both faces. The structures with interchanged *n*- and *p*-types are also possible

Condition 3 mentioned above. This solution is being considered for concentration [32]. Putting both contacts at the back works the other way round (Figure 7.1b). Back-contacted cells exhibit record efficiencies under concentration and demonstrate very high values near 23% at one sun [33].

In most cells, each contact is placed on a different face, which is technologically simpler (Figure 7.1c). Minority carriers in the substrate are usually collected at the front since their extraction is more problematic because of their low density. The diffusion length describes the maximum distance from where they can be collected. Majority carriers can drift to the back contact with low loss. Several designs extract minority carriers both at the front and at the back (Figure 7.1d) [34], thus increasing the volume of profitable photogeneration.

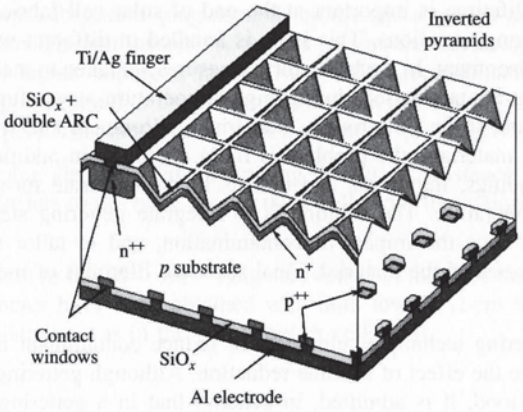
Bifacial cells are designed to collect light incident at both faces, which allows a boost in output power if there is a significant albedo component. They can be implemented with any structure in Figure 7.1 on the condition that both surfaces allow light through [35].

Both 24.7% record-efficiency laboratory solar cells [36] (Figure 7.2a) and mass-produced industrial devices (Figure 7.2b), typically 15% efficient, display the contacting structure in Figure 7.1(c). They will be described in the paragraphs that follow with the aim of illustrating the amplitude and the reasons for the performance gaps between the ideal and the best Si cell, and between this cell and industrial cells.

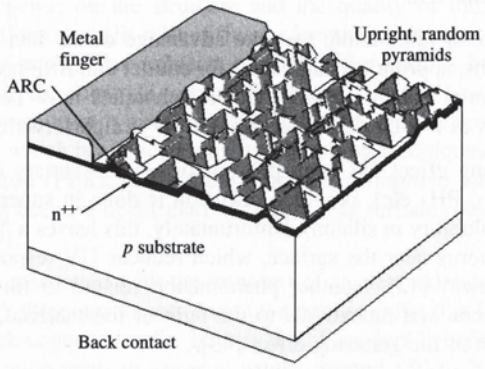
7.3.2 Substrate

7.3.2.1 Materials and processing

Highest efficiencies are achieved with monocrystalline float zone (FZ-Si) material, which in addition to extreme crystalline perfection shows the lowest contamination levels of both



(a)



(b)

Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

metallic and light (O, C, N) impurities. This translates into the longest post-processing SRH lifetimes in the millisecond range, but still shorter than the Auger limit. Magnetic Czochralski (MCz) material contains much less oxygen than conventional Czochralski and also allows very high efficiencies to be obtained [36].

Industrial cells use Czochralski (Cz-Si) wafers because of their availability. Cz wafers are also perfect crystals but they contain a high concentration of oxygen that affects lifetime in several ways [37]. Some commercial devices are made on multicrystalline (mc-Si) substrates grown in blocks or ribbons with procedures specially developed for photovoltaics. In addition to crystal defects, such as grain boundaries and dislocations, the potential content of metallics is higher because of lower segregation to the melt during the faster solidification process. As a result, the lifetime of mc-Si is lower.

But lifetime is important at the end of solar cell fabrication during which it can undergo strong variations. This issue is handled in different ways in a laboratory and a factory environment. In the laboratory, measures are taken to maintain long initial lifetimes by avoiding contamination during high-temperature steps: furnace cleaning, ultra pure chemicals and so on. In a rough, industrial environment and with defect-containing (Cz- and mc-Si) materials, the problem is more complex: in addition to contamination from the surroundings, impurities and defects in the substrate move, interact and transform at high temperature. The solution is to integrate gettering steps [38] in the fabrication flow that reduce the impact of contamination, and to tailor the thermal treatments to the peculiarities of the material. Final substrate lifetimes of industrial cells range from 1 to 10 μs.

Gettering techniques eliminate or reduce contaminant impurities in a wafer, and so neutralize the effect of lifetime reduction. Although gettering processes are not always well understood, it is admitted, in general, that in a gettering process a sink region is formed, which is able to accommodate the lifetime-killing impurities in such a way that they are not harmful to the device being manufactured, or at least they are where they can be easily removed.

In solar cell fabrication, we take advantage of the fact that phosphorus and aluminum diffusions, appropriate candidates for emitter and BSF layers, respectively, produce gettering in certain conditions [39]. Other techniques have been explored [40, 41], but their integration in a solar cell process is not so straightforward.

P gettering effect has been proved for a wide variety of P diffusion techniques (spin-on, $POCl_3$, PH_3 etc), provided diffusion is done in supersaturation conditions (i.e. over its solid solubility in silicon). Unfortunately, this leaves a "dead layer" of electrically inactive phosphorus near the surface, which reduces UV response of the cells in case it is not etched away [42]. Another phenomenon related to this supersaturated P is the injection of silicon self-interstitials to the bulk of the material, which is responsible for an enhancement of the gettering effect [43].

When Al is deposited on Silicon (by different techniques such as sputtering, vacuum evaporation or screen printing) and annealed over the eutectic temperature (577°C), a liquid Al-Si layer is formed, where impurities tend to segregate because of their enhanced solubility [44]. They will remain in this gettering layer while cooling, so that bulk lifetime will improve after the process.

Another approach to improve material quality is "bulk passivation", a treatment with hydrogen, for example, during SiN_x deposition, to which some defected materials respond very well [45].

7.3.2.2 Doping level and type

Both laboratory record-efficiency and industrial cells use boron-doped substrates. Rather than fundamental advantages [46], there are practical (properties of P diffusion, easiness of Al alloying) and historical reasons for this preference [47]. However, the situation may change once the role of boron in the degradation of Cz-Si cells under illumination has been established [48].

The optimum substrate doping depends on the cell structure and dominant recombination mechanism. Though intrinsic substrates present the advantage of highest Auger-limiting lifetimes, higher doping is favored when SRH recombination is present, since recombination is proportional to the excess density that decreases, for a given voltage, as doping increases [29]. This is balanced with a reduction of the lifetime itself.

A high doping also helps in minimizing the series resistance losses associated to the transport of carriers to the back face in thick cells with the majority carrier contact at the back.

Doping levels in the 10^{16} cm^{-3} range are found in the substrate of industrial cells. Very high efficiencies have been obtained with both low (1 Ω·cm for PERL cells) and high substrate resistivities, as in the point-contact cells [33].

7.3.2.3 Thickness

From the point of view of electrical performance, the choice of the optimum substrate thickness also depends on the structure and the quality of the materials and involves several considerations. In cells with diffusion lengths longer than the thickness, the most important issue is surface recombination: if S at the back is higher than D/L for the minority carriers in the substrate (around 250 $cm \cdot s^{-1}$ for the best cells), thinning the cell increases recombination at a given voltage, and vice versa. Thinner cells always absorb less light as well, which is attenuated by light-trapping techniques. Passivated emitter and rear locally diffused (PERL) cells were reported to improve when going from 280- to 400-μm thickness because of a (relatively) high rear surface recombination and nonideal light-trapping [49].

The losses associated with the transport of carriers extracted at the nonilluminated face decrease with thinning: in conventional structure cells; this leads to decreased series resistance. In back-contacted cells, both types of carriers benefit from thinning and the trade-off in absorption leads to lower w values, around 150 to 200 μm.

The diffusion length of industrial cells (around 100 μm) is generally lower than thickness. These cells are rather insensitive to thinning because they collect only the generation near the contact and are not affected by rear surface recombination. The driving criteria are cost and fabricability. A thickness in the 200- to 300-μm range is usually employed but there is a clear trend toward thinner wafers for saving expensive silicon material [47], and advanced wafering techniques and procedures to process very thin, large-area substrates without breaking are being developed: light-trapping and back recombination will become increasingly important.

7.3.3 The Front Surface

7.3.3.1 Metallization techniques

Metal grids are used at the front face to collect the distributedly photogenerated carriers. The compromise between transparency and series resistance requires metallization technologies able to produce very narrow but thick and highly conductive metal lines with

a low contact resistance to Si. Laboratory cells use photolithography and evaporation to form 10- to 15-μm metal fingers. Ti/Pd/Ag structures combine low contact resistance to *n*-Si and high bulk conductivity. These processes are not well suited to mass production that relies on thick-film technologies. Ag pastes are screen printed, resulting in over 100-μm wide lines with higher bulk and contact resistance. Laser-grooved buried-grid (LGBG) industrial cells implement a finer metallization technology [50], which will be presented in Section 7.7.3.

Coarser metallization techniques imply higher shading and resistance losses, and restrict the efficiency enhancement that could be achieved by internal cell design.

7.3.3.2 Homogeneous emitters

Under the metal lines, the substrate must be heavily doped to make the contact selective. Usually the doped region, the emitter, extends all across the front surface, acting as a "transparent electrode" by offering minority carriers in the substrate a low resistance path to the metal lines.

When the exposed surface is not passivated (Figure 7.3a), the emitter should be as thin as possible, because the high SRV makes the light absorbed in this region poorly collected, and also highly doped to decrease recombination. On the other hand, a sufficient low-sheet resistance is to be achieved. The solution is to make very thin and highly doped emitters.

If the surface is passivated (Figure 7.3b), the collection efficiency of the emitter can be raised by lowering the doping level thus avoiding heavy doping and other detrimental

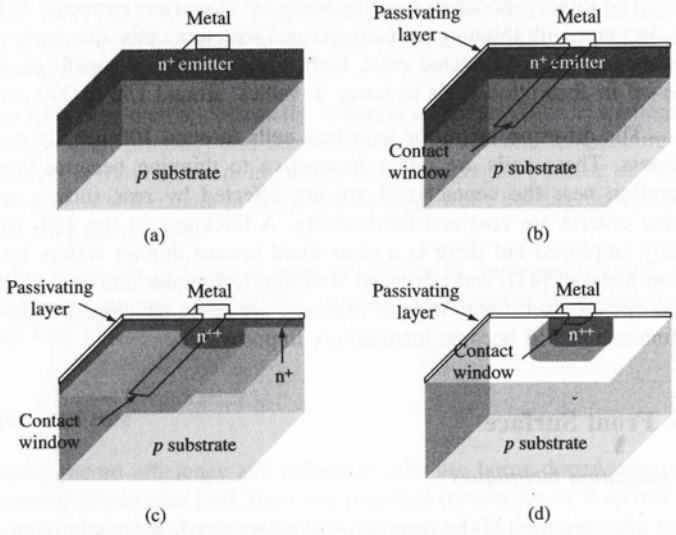


Figure 7.3 Different emitter structures: (a) homogenous emitter without surface passivation; (b) homogenous emitter with surface passivation; (c) selective emitter; and (d) localized emitter

effects. This must be balanced with contact resistance. Etching off of the passivating layer before metallization is usually needed (not in screen-printed cells). To maintain low sheet resistance and diminish recombination at the metallized fraction, the emitter is deep (around 1 μm). Note that the collection of carriers near the surface implies that the emitter is thin in terms of the minority-carrier diffusion length ($w < L$) and so it is very sensitive to surface recombination. Recombination is further reduced, by making the contact window narrower than the finger width, as illustrated in Figure 7.3 [51].

Control of both the surface concentration and the depth of the emitter, is achieved by depositing, in a thermal step, the desired amount of phosphorus or boron (predeposition) and then diffusing it into the substrate (drive-in) during subsequent furnace steps. The MIS solar cell, on the contrary, uses no diffusion for the n region, which is electrostatically induced by charges on top of the surface [20].

The J_0 of the emitter is the average, weighted by the contacted area, of the J_0 of contacted and noncontacted portions.

7.3.3.3 Selective and point emitters

A further improvement involves making separate diffusions for the different regions since the requirements are so different (Figure 7.3c) [52]: a heavily doped and thick region under the contacts, a thin and lowly doped region under the passivating layer. These structures, known as "selective emitters", come at the expense of more complicated processing usually involving photolithographic delineation and alignment of the diffusions (not in LGBG cells to be seen later).

If a very low SRV is possible, it would be best to have no emitter at all since doping always degrades bulk lifetime (Figure 7.3d). Examples are the back point-contact solar cell and the point-emitter design with bifacial contact [53], originally designed for concentration but capable of very high one-sun efficiency as well.

With localized contacts, surface recombination decreases with the penalty of an increase in transport losses in the substrate: deeper gradients for minority carriers, or increased series resistance for majority carriers, because of current crowding near the contacts. The trading is more favorably solved as the contact size shrinks [54]. Light and/or localized diffusions also have the drawback of decreased gettering action.

7.3.3.4 Industrial cells

Screen printing drastically affects the design of the emitter: it must be very highly doped to decrease the high-contact resistance and not very shallow so that it is not perforated during paste firing, which would short-circuit the junction [55]. Besides, the wide metal lines must be placed well apart; and in order to keep shading losses moderate, the emitter lateral conductance must be high, which also advises deep and highly doped regions. These characteristics are good to decrease recombination at the contacts, but are far from optimum at the exposed surface.

Industrial phosphorus emitters, typically, feature surface concentrations over 10^{20} cm^{-3} and 0.4-μm depth, and result in a sheet resistance around 40 Ω. As already

mentioned, the very highly doped region exhibits almost no photovoltaic activity due to the presence of precipitates ("dead layer"). As a result, the collection of short-wavelength light is very poor and the J_0 large, irrespective of a hypothetical surface passivation is therefore not implemented. The advantage is that heavy phosphorus diffusions produce very effective gettering. Some ways of incorporating selective emitters to screen-printed cells are being considered, SiN_x appearing very well suited for surface passivation [55]. This, however, must be accompanied by a decrease in the finger width so that lower sheet resistances are tolerated.

7.3.4 The Back Surface

The majority carrier, back p-contact of industrial solar cells is usually made by printing, and subsequently, firing an aluminum-containing Ag-conducting paste.

The p^+ layer would be useful in decreasing contact recombination, as explained, but this is immaterial to the electrically thick ($w > L$) present industrial cells and it is not optimized for this purpose.

For high-efficiency cells, contact passivation is essential. A BSF is a first step (Figure 7.4a). Localized contacts, as shown in Figure 7.4(b), further reduce recombination. This structure is presented by some of the bifacial cells [56].

If the surface passivation is good, the BSF is restricted to point contacts, some microns in size, as in PERL and similar cells (Figure 7.4c) [57]. The back face of bifacial cells passivated with SiN_x is shown in Figure 7.4(d).

A shallow and light diffusion helps in decreasing surface recombination (Figure 7.4e). The diffusion can be the same type of the substrate, or the opposite one: so-called PERT (Passivated emitter rear totally diffused) [36] and PERF (Passivated emitted rear floating junction) [58] cells demonstrate these concepts. The latter structure benefits from the lower J_0 values of n^+ layers, and it is essential that no electron flow is injected from the n region to the p contact: the junction must be in open-circuit (a "floating" junction). Note that this structure has nothing to do with structures sometimes found at the back of industrial cells (Figure 7.4f) where a coarse metal mesh is fired through the parasitic n^+ layer formed during front diffusion. A mesh is preferred to a continuous layer for mechanical reasons. The junction is shorted and presents to the substrate a high SRV.

7.3.5 Size Effects

Substrate edges are highly recombining surfaces that adversely affect cell performance, especially for small size, large diffusion length devices. For laboratory cells, efficiency is defined on the basis of a design area. The emitter is limited to it by planar masking or mesa etching. The true edge is thus placed far away from the cell limit, and then recombination is reduced. For real applications, on the contrary, only the substrate area counts, and edge optimization is more complex. Advanced passivation schemes such as edge diffusions are being considered [59, 60]. In large industrial cells, this recombination is much less important.

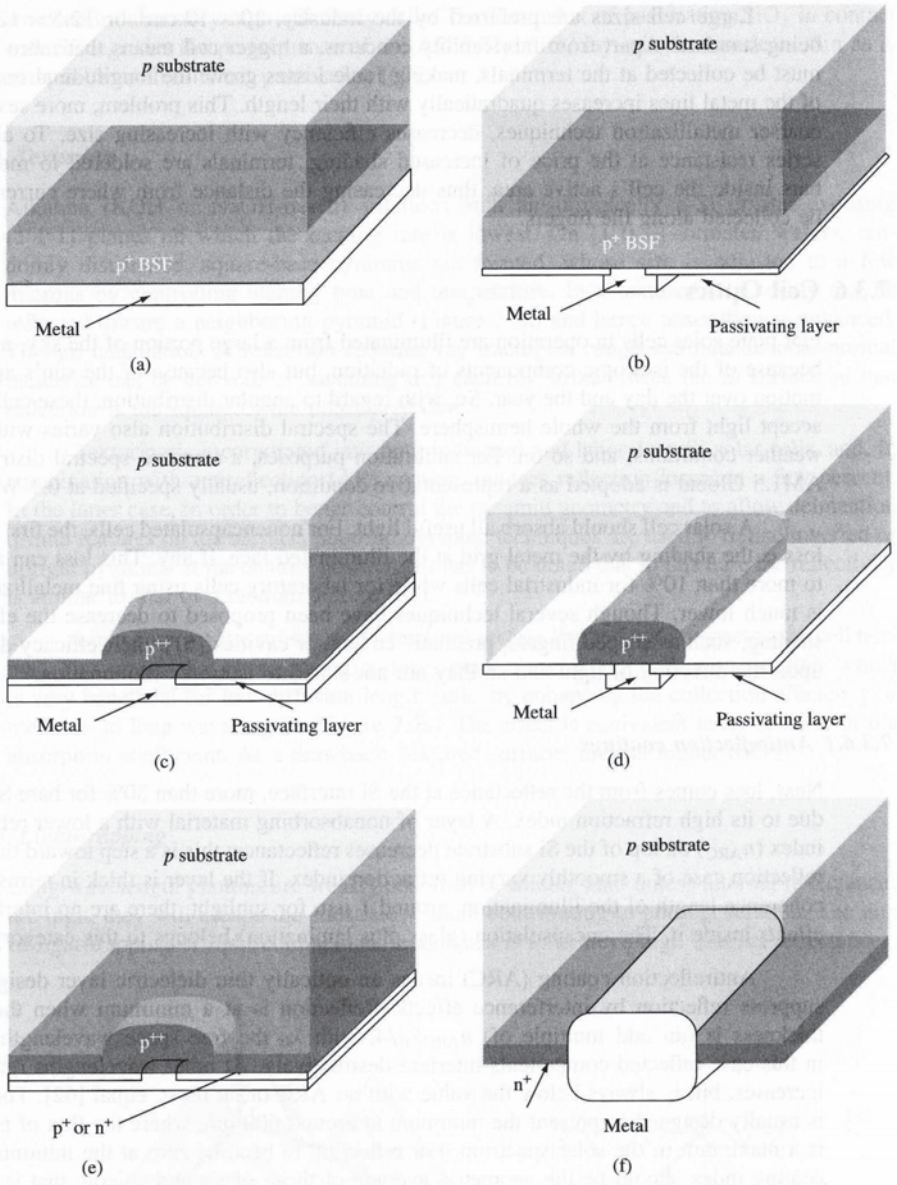


Figure 7.4 Rear contact structures: (a) continuous BSF; (b) bifacial cell; (c) local BSF; (d) local BSF, bifacial cell; (e) selective emitter or floating junction passivation; and (f) shorted junction at the back face of industrial cells

Large cell sizes are preferred by the industry, 10×10 cm^2 or 12.5×12.5 cm^2 being standard. Apart from fabricability concerns, a bigger cell means that more current must be collected at the terminals, making Joule losses grow: the longitudinal resistance of the metal lines increases quadratically with their length. This problem, more severe for coarser metallization techniques, decreases efficiency with increasing size. To alleviate series resistance at the price of increased shading, terminals are soldered to metal bus bars inside the cell's active area, thus decreasing the distance from where current must be collected along the fingers.

7.3.6 Cell Optics

Flat plate solar cells in operation are illuminated from a large portion of the sky, not only because of the isotropic components of radiation, but also because of the sun's apparent motion over the day and the year. So, with regard to angular distribution, these cells must accept light from the whole hemisphere. The spectral distribution also varies with time, weather conditions, and so on. For calibration purposes, a standard spectral distribution AM1.5 Global is adopted as a representative condition, usually specified at 0.1 W·cm^{-2}.

A solar cell should absorb all useful light. For nonencapsulated cells, the first optical loss is the shading by the metal grid at the illuminated face, if any. This loss can amount to more than 10% for industrial cells while for laboratory cells using fine metallization it is much lower. Though several techniques have been proposed to decrease the effective shading, such as shaped fingers, prismatic covers, or cavities [61], their efficacy depends upon the direction of light and so they are not suited to isotropic illumination.

7.3.6.1 Antireflection coatings

Next, loss comes from the reflectance at the Si interface, more than 30% for bare Si in air due to its high refraction index. A layer of nonabsorbing material with a lower refraction index (n_{ARC}) on top of the Si substrate decreases reflectance: this is a step toward the zero-reflection case of a smoothly varying refraction index. If the layer is thick in terms of the coherence length of the illumination, around 1 μm for sunlight, there are no interference effects inside it. The encapsulation (glass plus lamination) belongs to this category.

Antireflection coating (ARC) means an optically thin dielectric layer designed to suppress reflection by interference effects. Reflection is at a minimum when the layer thickness is (an odd multiple of) $n_{ARC}\lambda_0/4$, with λ_0 the free space wavelength, since in this case reflected components interfere destructively. At other wavelengths reflection increases, but is always below the value with no ARC or, at most, equal [62]. The ARC is usually designed to present the minimum at around 600 nm, where the flux of photons is a maximum in the solar spectrum. For reflection to become zero at the minimum, the coating index should be the geometric average of those of air and silicon, that is, 2.4 at 600 nm for nonencapsulated cells.

The industry uses TiO_x deposited by chemical vapor deposition (CVD). PECVD SiN_x is very interesting since it also serves as a passivating layer, as explained earlier.

By using double layer coatings with $\lambda/4$ design, with growing indices from air to silicon, the minimum in reflection is broader in wavelength. Evaporated SZn and MgF_2

are used in laboratory high-efficiency cells. The low index of passivating SiO_x in contact with Si degrades the performance of the ARC. The SiO_x layer is then made as thin as is compatible with efficient passivation [63].

7.3.6.2 Texturing

Alkaline (KOH or NaOH-based) solutions etch anisotropically a-Si crystal exposing {1 1 1} planes on which the etching rate is lowest. On [1 0 0]–oriented wafers, randomly distributed, square-base pyramids are formed, whose size is adjusted to a few microns by controlling etching time and temperature. In a textured face, a ray can be reflected toward a neighboring pyramid (Figure 7.5a) and hence absorption is enhanced. Though calculation of reflection requires ray tracing, a rough estimate of near-normal incidence can be derived, by assuming that each ray strikes twice the Si surface so that reflection is the square of the untextured case.

Texturing is incorporated into both industrial and laboratory Si solar cells, and, in combination with antireflection (AR) coating, reduces reflection losses to a few percent. In the latter case, in order to better control the pyramid geometry and to allow delineation of fine features on the surface, photolithographic techniques are used to define inverted or upright pyramids at the desired positions. It has to be noted that in this case the reflectivity is similar to that of a random texture [64].

Light entering the substrate at a textured surface is tilted with respect to the cell normal. This means that photogeneration takes place closer to the collection junction, which is very beneficial for low-diffusion length cells, by enhancing the collection efficiency of medium- to long wavelengths (Figure 7.5a). The effect is equivalent to an increase of the absorption coefficient. As a drawback, textured surfaces present higher SRVs.

7.3.6.3 Light-trapping

Long-wavelength photons are weakly absorbed in silicon, and, unless internal reflectances are high, they will escape the substrate without contributing to photogeneration. The aim of light-trapping or light confinement techniques is to achieve high internal reflectances.

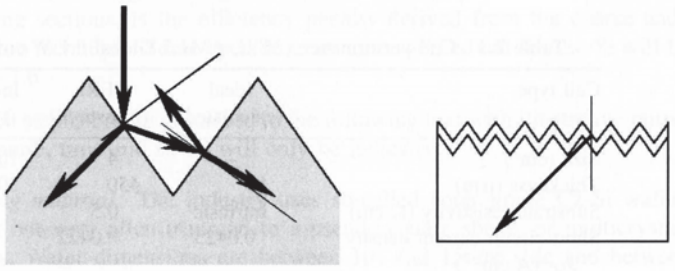


Figure 7.5 Effects of surface texturing: (a) decreased reflection; and (b) increased photogeneration in the base

Practical back mirrors that are fully compatible with the cell electrical design, can be implemented, such as those schematized in Figure 7.4. A metal can make a good reflector, but Al, especially after heat treatment, gives low reflectance. The Si-oxide-metal structure in Figure 7.4(c) can present a high reflectance by capitalizing on interference effects [65].

At the front, the metal mirror is not applicable because the ray paths must be kept open for the entering light. Still, high front reflectance can be achieved because of total internal reflection [61]. Rays striking the surface at angles larger than the critical air-Si one are totally reflected. Texturing one or both surfaces with macroscopic or microscopic features serves this purpose by tilting the rays. Even in the case of geometric texturing with well-defined surface orientations, after a few internal reflections, the direction of rays inside the wafer is randomly distributed: this is the lambertian case, useful analytic approximation to light-trapping. Bifacial structures in Figure 7.4 can, for the same reason, be very efficient at confining the light [66].

Light-trapping increases the effective thickness of the wafer for absorption. In the geometrical optics regime, it has been shown that for one-side isotropic illumination the maximum enhancement factor (though perhaps not realizable) is 4 $(n_{Si}/n_{air})^2$, that is, each ray traverses 50 times the cell thickness before escaping [67]. The corresponding enhancement in photogeneration will be lower because of the competition of the absorption by free carriers at long wavelength.

Light-trapping is essential for thin cells. Even in the thick PERL design it can suppose around 1 mA·cm^{-2} enhancement in short-circuit current with respect to the case where the internal reflectances were zero.

7.3.7 Performance Comparison

For illustration purposes, Table 7.3 collects relevant parameters of the Auger-limited ideal Si solar cell [30], the best one-sun PERL cell [36] and a typical screen-printed, industrial cell on Cz-Si. The different concepts behind each set of data must be accounted for when comparing the figures. For instance, the ideal cell is assumed as being isotropically illuminated, while measurements are made for near-normal incidence.

Table 7.3 Cell performance (25°C, AM1.5 Global 0.1 W·cm^{-2})

Cell type	Ideal (calculated)	PERL (measured)	Industrial (typical)
Size (cm^2)	–	4	100
Thickness (μm)	80	450	300
Substrate resistivity (Ω·cm)	Intrinsic	0.5	1
Short-circuit current density, J_{SC} (A·cm^{-2})	0.0425	0.0422	0.034
Open-circuit voltage, V_{OC} (V)	0.765	0.702	0.600
Fill factor, *FF*	0.890	0.828	0.740
Efficiency, η (%)	28.8	24.7	15.0

The most striking difference between the best and the ideal solar cell is the difference in design: thick and low injection *versus* thin and high injection. The PERL cell is surely the best design for the currently achievable levels of surface recombination, which limit open-circuit voltage and shift the optimum thickness to high values. The low resistivity follows then from transport considerations for the chosen structure. The very high fill factor of the ideal cell is characteristic of high injection, Auger-limited operation.

Reduction of surface recombination in the best laboratory cells relies on surface passivation and the restriction of very heavily doped regions to a minimum. In the end, this is possible because of the possibility of defining and aligning very small features on the surfaces.

The very heavily doped emitter, along with lower substrate lifetimes, is responsible for the reduced short-circuit current and open-circuit voltage in the industrial cell. The fill factor is affected by the large device area in conjunction with the limitations of the metallization technique, which further reduces the current because of shading.

Continuous improvement in material quality and cost-driven thinning of the substrates will increase the need for industrial cells to implement surface passivation schemes. This will require the refinement of the metallization technique; another issue is that substrate lifetimes in an industrial environment depend on the gettering action of very heavy diffusions, which are not compatible with optimum surface performance. The PERL approach – high-temperature processes and delineation of fine features – is the most successful path to high efficiency, but it is not the only one that can inspire the forthcoming developments in industrial cells. It is worth noting, in this respect, that heterojunction with intrinsic thin-layer (HIT) solar cells have entered the exclusive club of more than 20% efficiency with a different approach (see Section 7.7.2).

7.4 MANUFACTURING PROCESS

7.4.1 Process Flow

Figure 7.6 shows the main steps of a simple process for solar cell fabrication based on screen printing. With more or less minor modifications, this process is currently used by many manufacturers. The main virtues of this 30-year-old PV technology are easy automation, reliability, good usage of materials and high yield. The drawback, as explained in preceding sections, is the efficiency penalty derived from the coarse and aggressive metallization technique. Some specific treatments worked out for mc-Si will be explained in Section 7.6.

Each step is briefly described in the following text with illustrative purposes: values of temperature, time and so on will only be indicative.

1. *Starting material*: The industry uses so-called solar grade Cz-Si wafers, round in origin but very often trimmed to a pseudo-square shape, or multicrystalline square wafers. Wafer dimensions are between 10- and 15-cm side and between 200- and 350-μm thickness. Doping is *p*-type (boron) to a resistivity of around 1 Ω·cm.
2. *Saw damage removal*: The sawing operation leaves the surfaces of "as cut" wafers with a high degree of damage. This presents two problems: the surface region is of

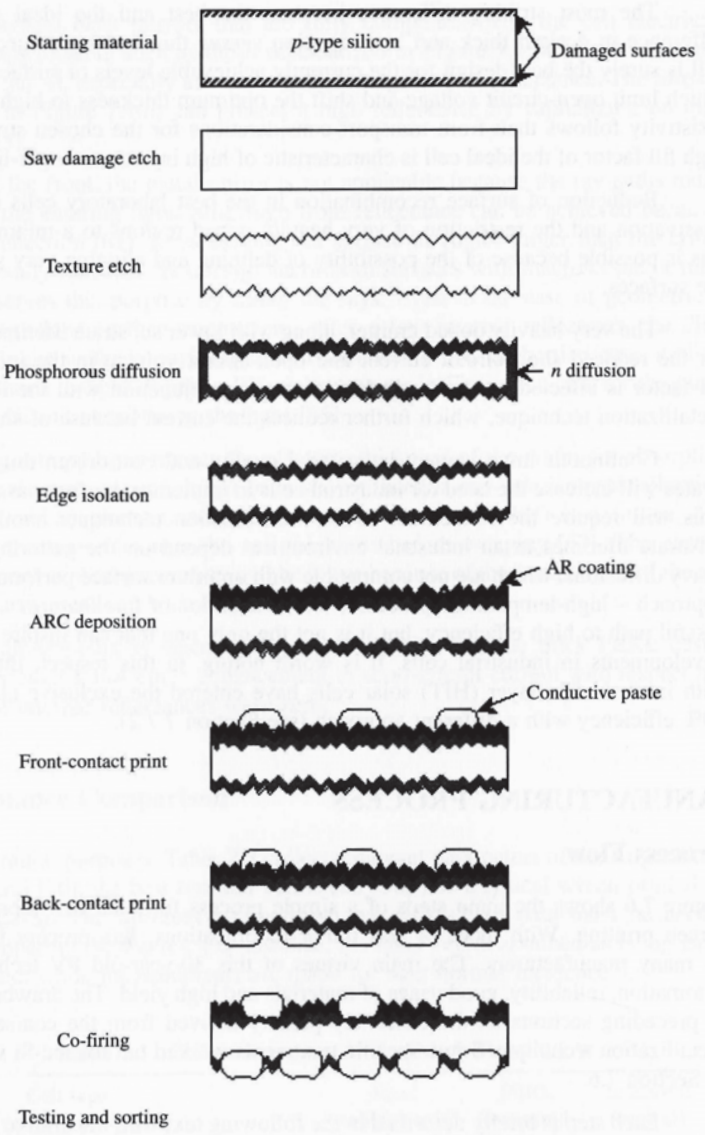


Figure 7.6 A typical processing sequence with schematic illustrations of the resulting structures

a very bad quality and the defects can lead to wafer fracture during processing [68]. For this reason, about ten microns are etched off from each face in alkaline or acid solutions. The wafers, in Teflon cassettes, are immersed in tanks containing the solution under temperature and composition control. Alkaline etches are preferred to acid solutions due to considerations of waste disposal.

3. *Texturization*: NaOH etching leading to microscopic pyramids is commonly employed. Their size must be optimized, since very small pyramids lead to high reflection, while very large ones can hinder the formation of the contacts. To ensure complete texturing coverage and adequate pyramid size, the concentration, the temperature and the agitation of the solution and the duration of the bath must be controlled (in fact NaOH at a higher concentration and at a higher temperature is commonly used as an isotropic etch for saw damage removal). Alcohol is added to improve homogeneity through an enhancement of the wettability of the silicon surface. Typical parameters are 5% NaOH concentration, 80°C and 15 min [69].
   Texturing alternatives for multicrystalline material are presented in Section 7.6.
4. *Phosphorus diffusion*: Phosphorus is universally used as the *n*-type dopant for silicon in solar cells. Since solid-state diffusion demands high temperature, it is very important that the surfaces are contamination-free before processing. To this end, after the texturing the wafers are subjected to acid etch to neutralize alkaline remains and eliminate adsorbed metallic impurities.
   The industry uses a number of procedures to perform the phosphorus diffusion. The following classification is based on the type of furnace in which the high-temperature step takes place:
   Quartz furnaces: The cells to be diffused, loaded in quartz boats, are placed in a quartz tube with resistance heating and held at the processing temperature (Figure 7.7a). The cells enter and exit the furnace through one end, while gases are fed through the opposite one. Phosphorus itself can be supplied in this way, typically by bubbling nitrogen through liquid $POCl_3$ before injection into the furnace. Solid dopant sources are also compatible with furnace processing. Five to fifteen minutes at temperatures in the range from 900 to 950°C can be considered representative. As suggested in Figure 7.6, both surfaces and the edges of the wafer will be diffused.

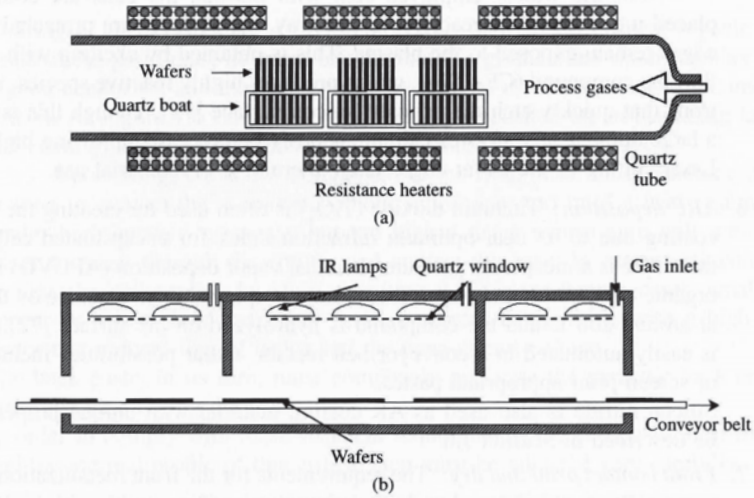


Figure 7.7 (a) A quartz furnace; and (b) a belt furnace for the diffusion of phosphorus

Belt furnaces: In this case, solid phosphorus sources are used: screen printed, spun-on or CVD pastes containing phosphorus compounds are applied on one wafer face and, after drying, placed in a conveyor belt passing through the furnace (Figure 7.7b). The temperature inside it can be adjusted in several zones and, though the furnace is open, gases can be supplied. The temperature cycle undergone by the wafer will mimic the temperature profile along the furnace with the time scale set by the advancing speed of the belt. A cycle begins with several minutes at around 600°C with clean air to burn off the organic materials of the paste, followed by the diffusion step in nitrogen at 950°C for 15 min. Only one face of the wafer is diffused, but the parasitic junction formed at the edges is also present in this technique due to diffusion from the gas phase. Resistance or infrared heating can be employed, the latter offering the possibility of faster heating–cooling rates of the wafer.

The main benefit of the quartz furnace is cleanliness, since no metallic elements are hot and no air flows into the tube. Though this is a batch step, high throughput can be achieved since many wafers can be simultaneously diffused in each tube, commercial furnaces consisting of stacks of four tubes. In a belt furnace, the ambient air can get into the furnace and the hot conveyor belt is a source of metallic impurities. The assets of belt furnaces are found in automation and in-line production, throughput and the ability to implement temperature profiles. New designs try to reconcile the advantages of both types of equipment [70].

After diffusion, an amorphous glass of phospho-silicates remains at the surface that is usually etched off in diluted HF because it can hinder subsequent processing steps.

5. *Junction isolation*: The *n*-type region at the wafer edges would interconnect the front and back contacts: the junction would be shunted by this path translating into a very low shunt resistance. To remove this region, dry etching, low temperature procedures are used.

   For the widely employed etch with plasma, the cells are coin-stacked and placed into barrel-type reactors. In this way, the surfaces are protected and only the edges remain exposed to the plasma. This is obtained by exciting with an RF field a fluorine compound (CF_4, SF_6), which produces highly reactive species, ions and electrons that quickly etch the exposed silicon surface [71]. Though this is a batch step, a large number of wafers can simultaneously be processed allowing high throughput. Laser cutting of the wafer edges is an alternative in industrial use.

6. *ARC deposition*: Titanium dioxide (TiO_2) is often used for creating the antireflecting coating due to its near-optimum refraction index for encapsulated cells. A popular technique is atmospheric pressure chemical vapor deposition (APCVD) from titanium organic compounds and water: the mixture is sprayed from a nozzle on the wafer held at around 200°C and the compound is hydrolyzed on the surface [72]. This process is easily automated in a conveyor-belt reactor. Other possibilities include to spin-on or screen print appropriate pastes.

   Silicon nitride is also used as AR coating material with unique properties that will be described in Section 7.6.

7. *Front contact print and dry*: The requirements for the front metallization are low contact resistance to silicon, low bulk resistivity, low line width with high aspect ratio, good mechanical adhesion, solderability and compatibility with the encapsulating

materials. Resistivity, price and availability considerations make silver the ideal choice as the contact metal. Copper offers similar advantages, but it does not qualify for screen printing because subsequent heat treatments are needed during which its high diffusivity will produce contamination of the silicon wafer.

Screen printing compares very unfavorably with vacuum evaporation in the first three requirements. It has been already commented how this affects the cell design and leads to a significant efficiency gap between laboratory and commercial cells. But throughput and cost compensate for it.

Screen printing will be described in more depth in the following section. It is used to stick a paste containing silver powder to the front face of the wafer in the comblike (fingers plus bus bars) pattern. Automatic screen printers are available that are capable of in-line, continuous operation with high throughput. These machines accept wafers from packs, cassettes or a belt line, place them with sufficient accuracy under the screen and deliver the printed wafers to the belt line. The paste is a viscous liquid due to the solvents it contains; these are evaporated in an in-line furnace at 100 to 200°C. The dried paste is apt for subsequent processing.

8. *Back contact print and dry*: The same operations are performed on the backside of the cell, except that the paste contains both silver and aluminum and the printed pattern is different.

   Aluminum is required because silver does not form ohmic contacts to p-Si, but cannot be used alone because it cannot be soldered. The low eutectic temperature of the Al-Si system means that some silicon will be dissolved and then recrystallize upon cooling in a p-type layer.

   Though in principle a continuous contact will give better electrical performance (lower resistance), most commercial wafers feature a back contact with a mesh structure: apart from paste-saving considerations, this is preferred to a continuous layer because the different expansion coefficients would produce warp of the cell during the subsequent thermal step.

9. *Cofiring of metal contacts*: A high-temperature step is still needed: organic components of the paste must be burnt off, the metallic grains must sinter together to form a good conductor, and they must form an intimate electric contact to the underlying silicon. As Figure 7.6 shows, the front paste is deposited on an insulating layer (the AR coating) and the back contact on the parasitic n-type rear layer.

   Upon firing, the active component of the front paste must penetrate the ARC coating to contact the n-emitter without shorting it: too mild a heat treatment will render high contact resistance, but too high a firing temperature will motivate the silver to reach through the emitter and contact the base. In extreme situations, this renders the cell useless by short-circuiting it. In more benign cases, small shunts appear as a low shunt resistance or dark current components with a high ideality factor that reduces the fill factor and the open-circuit voltage.

   The back paste, in its turn, must completely perforate the parasitic back emitter to reach the base during the firing.

   In order to comply with these stringent requirements, the composition of the pastes and the thermal profile of this critical step must be adjusted very carefully.

10. *Testing and sorting*: The illuminated $I-V$ curve of finished cells is measured under an artificial light source with a spectral content similar to sunlight (a sun simulator)