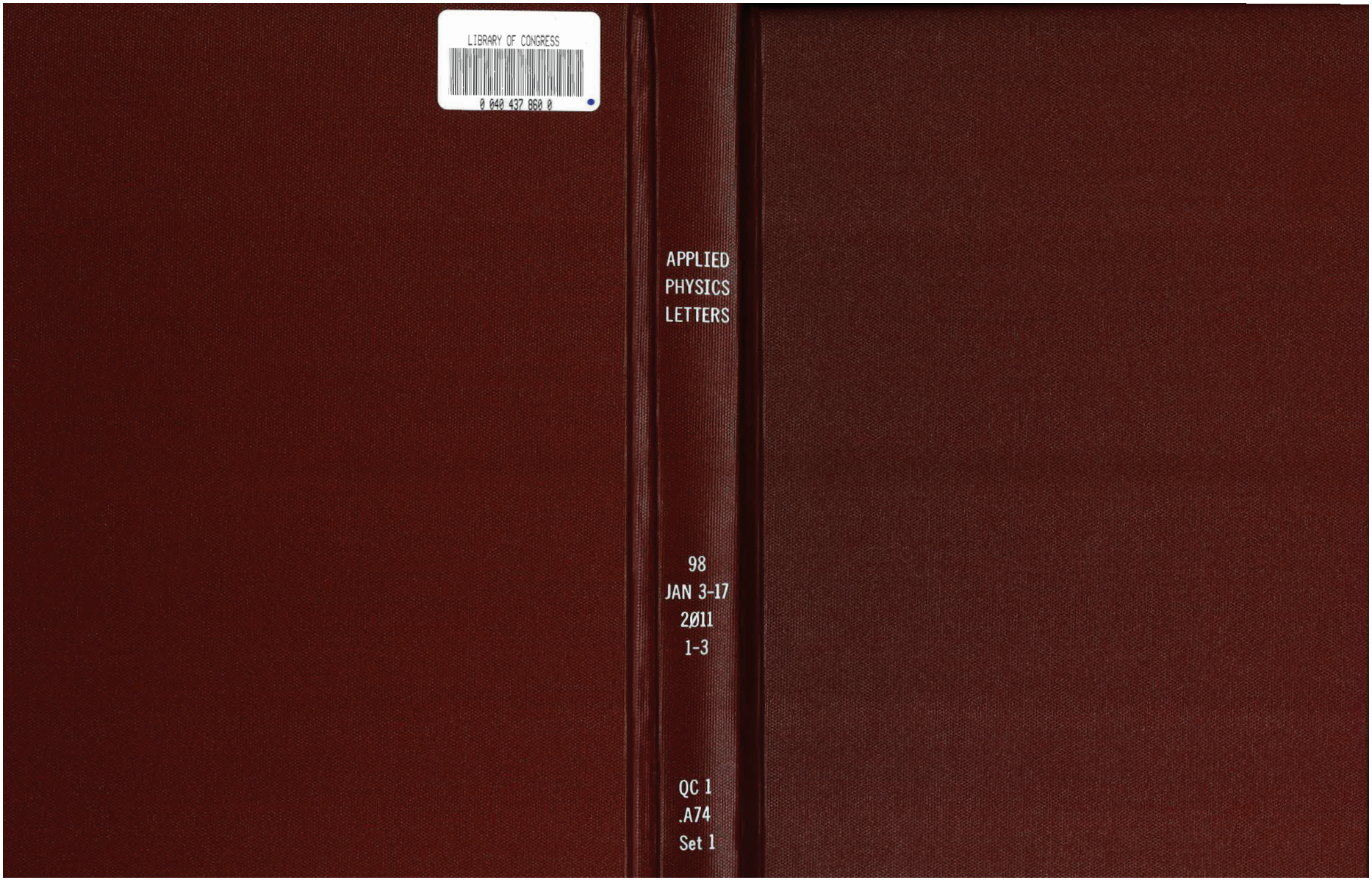
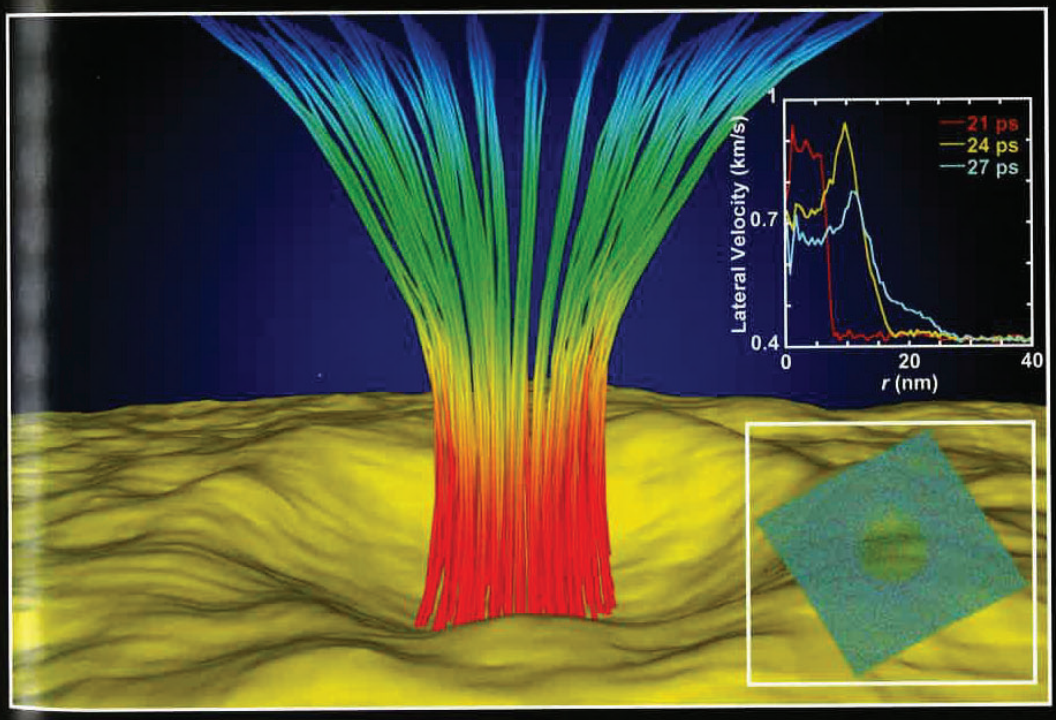

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Simultaneous gettering and emitter formation in multicrystalline-Si wafers by annealing phosphorus doped amorphous silicon compounds

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We demonstrate gettering of metal impurities in p-type multicrystalline silicon (mc-Si) wafers by annealing wafers that are surface passivated by double layers of amorphous silicon-based compounds acting as gettering sites. As inner layer we use a phosphorus-doped amorphous silicon-carbon-nitrogen alloy, providing surface passivation and acting as dopant source for the emitter formation during subsequent anneal. The outer layer is silicon nitride with antireflective properties. Anneals are done at 750, 800, and 850 °C for 30 and 60 min. The gettering effect is as good as for a conventional $POCl_3$ diffusion followed by extended gettering at low temperature, and it is weakly influenced by the temperature step chosen. In the range explored, the sheet resistances of the emitters and the junction depths lay between 3000 to 60 Ω/sq. and 100–300 nm, respectively. © *2011 American Institute of Physics*. [doi:10.1063/1.3535616]

Multicrystalline silicon wafers are commonly used in the solar industry for the production of wafer-based solar cells. Metal impurities such as iron are present in the wafers due to the manufacturing process of the multicrystalline silicon (mc-Si) ingots and reduce the carrier bulk lifetime. These metal impurities are gettered during the formation of the emitter, conventionally done by diffusion at 800–900 °C in $POCl_3$ atmosphere to form an n^+-type emitter on a p-type substrate.[1] After that, a HF dip is necessary to remove the phosphosilicate glass (PSG) grown on the wafer surface. The emitter is subsequently passivated by amorphous silicon nitride (SiN), serving at the same time as antireflective coating.

In this work we suggest an alternative way of emitter formation and gettering for p-type mc-Si solar cells. It consists of the deposition of double layers of phosphorus-doped amorphous silicon-based compounds followed by annealing. Gettering of metal impurities from deposited amorphous silicon (a-Si) was already reported in patents[2–4] and in a publication.[5] Emitter diffusion from phosphorus doped amorphous layers was demonstrated[6] without analyzing the gettering performance. Our process provides the simultaneous formation of an emitter and getters metallic impurities and will eventually also provide antireflection properties.[7] As an additional advantage, a posterior HF dip to remove the PSG is not necessary. This paper concentrates on the gettering performance and the sheet resistance of the emitter. Surface passivation and optical properties will be discussed elsewhere.

Neighboring p-type mc-Si wafers with 1.3 ± 0.1 Ω cm resistivity are selected from middle positions of a mc-Si ingot. We select two different regions A and B on each wafer to explore the dependence of gettering on the grain size. Region A has a grain size that is around five times that of region B.

Etching for 3 min in an acidic CP4 solution removes the saw damage. The final wafer thickness is 155 μm. Afterwards we perform a RCA cleaning and an HF dip. Then we split the wafers in three groups: the first for depositing doped a-Si double layers that are annealed, the second for reference $POCl_3$ diffusions, and the third to be well passivated with silicon nitride for measuring the bulk lifetime before gettering.

Amorphous silicon films are deposited by means of a RF parallel plate plasma enhanced chemical vapor deposition at a frequency of 13.27 MHz. The process temperature is 400 °C and the total gas pressure 0.4 bar. We coat both surfaces of each wafer symmetrically with double layers.

The first and inner layer is a phosphorus-doped silicon-carbon-nitrogen alloy [SiCN(n)] that is rich in silicon and has a refractive index of 3.7–4.0 and a thickness of 50 nm. This layer is the phosphorus source for the emitter formation during the subsequent annealing. We use silane [SiH_4, 28 SCCM (SCCM denotes cubic centimeter per minute at STP)], methane (CH_4, 21 SCCM), molecular nitrogen (N_2, 32 SCCM), and phosphine (PH_3, 1.5 SCCM) as precursor gases. These deposition parameters demonstrated excellent surface passivation for p-type[8] and n-type[9] crystalline silicon. The presence of carbon in phosphorus-doped amorphous silicon films reduces drastically the surface recombination when compared to films without carbon deposited at identical conditions.[10] It also permits to work at deposition temperatures almost two times higher than those for a-Si films and consequently reduce the content of hydrogen.

The second and outer layer is nominally intrinsic (not doped) silicon nitride with a refractive index of 2.1 and a thickness of 70–80 nm. This layer is conceived to provide the antireflection properties and to prevent the out-diffusion of phosphorus. We use silane (SiH_4, 15 SCCM) and ammonia (NH_3, 18 SCCM) as precursor gases.

We anneal samples at 750, 800, and 850 °C for 30 and 60 min, respectively, in a conventional tube furnace under N_2 atmosphere. In order to facilitate slow effusion of hydrogen out of the amorphous films without producing blistering, we

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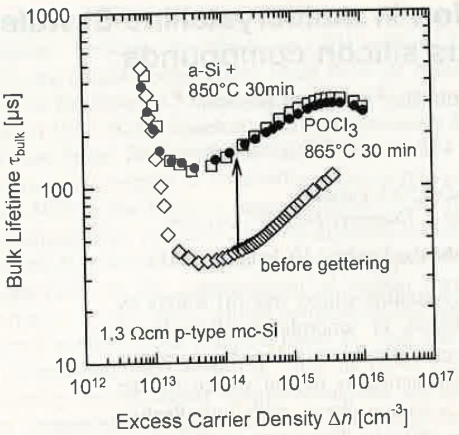


FIG. 1. Demonstration of gettering in region A after annealing a-Si stacks at 850 °C for 30 min. Once the wafer is annealed, bulk lifetime increases from around 55 μs (before gettering) to around 220 μs (after gettering) at $\Delta n = 5\times10^{14}$ cm^{-3}. The corresponding neighboring wafer with $POCl_3$ reference process reaches similar values.

introduce a preannealing at 500 °C for 30 min. Scanning electron microscope images show that both outer and inner layer remain after annealing as distinct films on the wafer surface.

As a reference for the gettering experiments, we diffuse a 70 Ω/sq. phosphorus emitter under $POCl_3$ atmosphere at 865 °C during 30 min, followed by further extended gettering[11] step at 500 °C during 1.5 h under N_2 atmosphere. We perform an HF dip to remove the silicon nitride outer layer of the samples with an annealed a-Si compounds and to remove the PSG from the $POCl_3$-diffused samples. Afterwards we etch off 6 μm of Si with a CP4 solution to fully remove the inner layer and the diffused emitter. Then we RCA-clean the samples and deposit passivating SiN on both sides.

We determine the gettering quality by measuring the minority carrier lifetimes before and after annealing applying the steady state photoconductance technique.[12] Infrared light

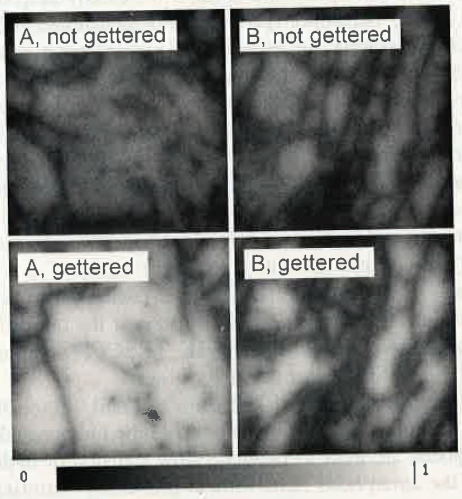


FIG. 2. Spatially resolved PL image of two passivated, emitter-free mc-Si neighboring wafers before and after annealing at 850 °C for 30 min.

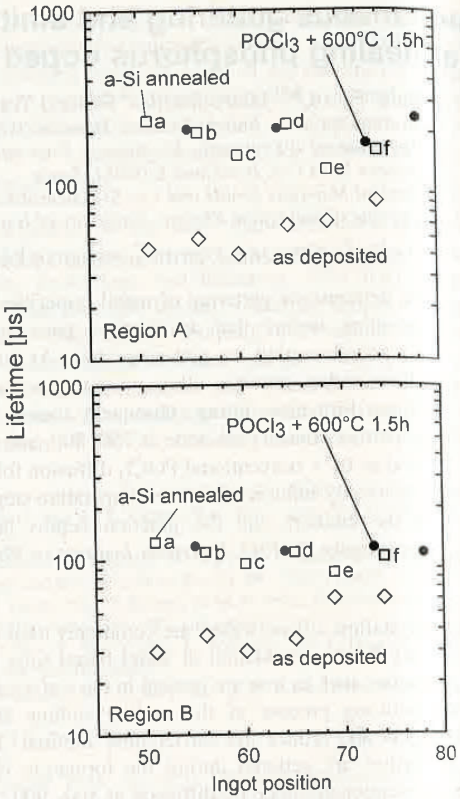


FIG. 3. Measured lifetime at $\Delta n = 5\times10^{14}$ cm^{-3} for mc-Si samples as a function of the ingot position. Labels for squares indicate the annealings as follows: (a) 750 °C, 30 min, (b) 750 °C, 60 min, (c) 800 °C, 30 min, (d) 850 °C, 30 min, (e) 850 °C, 60 min, and (f) 800 °C, 60 min. Variation (d) corresponds to samples used in Figs. 1 and 2.

illuminates the sample to ensure a close to uniform charge carrier generation rate in the wafers.

Figure 1 shows the injection dependences of the carrier lifetime for region A that we annealed at 850 °C for 30 min. Also shown is the $POCl_3$-diffused reference that experienced a postdiffusion low-temperature anneal.

Both annealing treatments enhance the lifetime by about a factor 4 at an excess carrier density of $\Delta n = 10^{14}$–10^{15} cm^{-3}. This reflects a reduction of Shockley–Read–Hall recombination in the bulk since (i) the emitter is etched and the surface is repassivated, (ii) Auger recombination[13] is negligible, and (iii) lifetime artifacts due to trapping[14] or depletion region modulation[15–17] are present only at lower injection densities.

Figure 2 shows spatially resolved photoluminescence images of neighboring wafers before and after annealing the amorphous double layer with the annealing conditions used in Fig. 1. The image is taken once the emitter is etched-off and the surface is repassivated. The signal, proportional to the carrier lifetime, enhances at the grain boundaries and in the volume of the crystal grains. The same enhancement seems to occur either for big grains, like in region A, or for small grains observed in region B. This suggest a mechanism involving the presence of gettering sites produced by the phosphorus emitter[18] and uniformly distributed, rather than a internal gettering[19] produced by the migration of impurities to already existing gettering sites.

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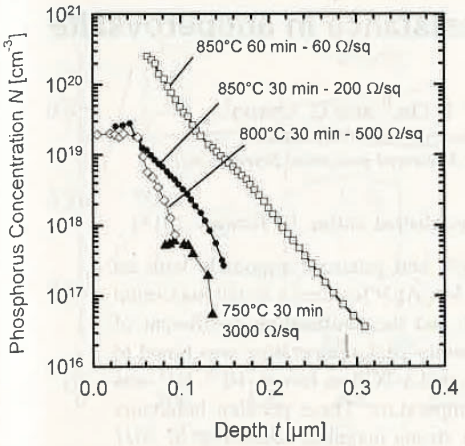


FIG. 4. Phosphorus profiles measured with ECV for annealed samples. Measurements are done after etching the SiN outer layer with HF solution.

Figure 3 displays the lifetimes (taken at $\Delta n = 5 \times 10^{14}$ cm^{-3}) of the bulk mc-Si wafers before and after gettering processes as a function of the ingot position for both regions A and B. Efficient gettering is achieved, yielding equivalent final bulk lifetime level regardless of the process performed (annealing of a-Si compounds or $POCl_3$ diffusion), or the region analyzed. This indicates that metallic impurities are effectively gettered and that the final lifetime in region B is limited by crystallographic defects. To support this hypothesis, we determine the interstitial iron concentration from lifetime measurements in the dissociate and associate states of the Fe–B pairs as described in Ref. 20. Samples not gettered contain interstitial iron concentrations of around 10^{11} cm^{-3}, while the measured values are below the detection limit (10^{10} cm^{-3}) in gettered samples from a-Si and from $POCl_3$ diffusion.

Figure 4 shows the electrically active phosphorus profiles determined by electrochemical capacitance voltage (ECV) technique. Prior to this measurement it is necessary to etch off the nonconducting SiN outer layer with HF solution. We measure then the sheet resistances with a four point probe directly on the crystallized inner layer. ECV measurements allow us to determine junction depths of 100–300 nm and sheet resistances between 3000 and 60 Ω/sq. for the samples with lowest and highest thermal budget explored, respectively.

In conclusion, in this work we have demonstrated a method of gettering impurities in multicrystalline silicon wafers. It is based on depositing amorphous silicon carbide-nitride/silicon nitride double layers, the inner ones being phosphorus-doped, and annealing them between 750 and 850 °C during 30 or 60 min. The gettering effect is as good as for the $POCl_3$ diffusion when the latter is followed by extended gettering at 500 °C. Besides gettering, emitter formation with attractive sheet resistances was demonstrated.

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