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Polysilicon: a versatile material for microsystems

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Abstract

The initial attraction of polysilicon was the ability to deposit semiconductor layers on a wide range of substrates. This leads to the development of polysilicon gate MOS, polysilicon emitters and a range of passive devices. In the field of sensors and actuators, the strain sensors, based on piezoresistive effect, was one of the first successful applications. However, it was probably the development of surface micromachining, which received the most attention. The ability to deposit polysilicon on oxide meant that free-standing structures could be fabricated and this has lead to a wide range of successful devices. Polysilicon has a structure comprising small single-crystal grains with many orientations separated by thin grain boundaries. The size of these grains is highly dependent upon processing and therefore a wide range of electrical and mechanical properties can be achieved. This yields greater flexibility but this sensitivity to process parameters can lead to problems in obtaining a stable process. This paper will look back at the development of polysilicon, its structure, fabrication and both mechanical and electrical properties. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Polysilicon; Sensors and actuators; Piezoresistive effect; Micromachining

1. Introduction

Polycrystalline silicon (polysilicon) comprises small grains of single-crystal silicon separated by thin grain boundaries. At the grain boundaries, the grains of different orientations meet resulting in an extremely thin amorphous layer. These boundaries create electrical barriers and therefore have a significant influence on the mechanical properties. The basic structure can be small random grains or columnar (Fig. 1). These structures are highly dependent on processing making it difficult to give exact recipes which can be applied to other deposition systems. Values given in this paper are therefore simply examples for a given system.

The applications for polysilicon can be traced back to the 1960s with the realisation that it could be used for gates in MOS technologies to enable further reduction in dimensions [1]. It was also useful since p–n junctions can be avoided [2], which lead to an expansion in the studies on the electrical properties of the material [3,4]. Its applications were further expanded into crossovers, interconnects and capacitors. In the 1970s, it was found to be a useful material for a piezoresistive element [5–10]. Since no p–n junction was required, these devices could operate at higher temperatures. In the 1980s, the potential of polysilicon as a mechanical material was realised.

At the grain boundaries two crystal orientations meet and therefore dangling bonds are created. When the films are doped, the doping atoms can occupy these sites rendering them electrically inactive and thus a barrier is created. This barrier is similar to a Schottky barrier, through which transport can be through thermionic emission or tunnelling. This paper examines development of polysilicon, its structure, fabrication, both mechanical and electrical properties, and applications such as piezoresistive devices and micromechanics are discussed.

2. Deposition and structure

Polysilicon can be deposited using chemical vapour deposition. This can be at atmospheric pressure (APCVD) or at low pressure (LPCVD). Plasma enhanced (PECVD) is also used although this yields an amorphous structure. In general, the low pressure systems are used for polysilicon. There are a number of gasses available and the most common are silane and dichlorosilane. Silane is used in most LPCVD systems although for higher temperature depositions, such as epitaxy, dichlorosilane is used. The reaction for silane is given by

$$SiH_4 \rightarrow Si + 2H_2$$

The deposition rate is strongly dependent upon the pressure, flow and temperature. An example of deposition rate as a function of temperature is given in Fig. 2. This is a typical temperature range for LPCVD.

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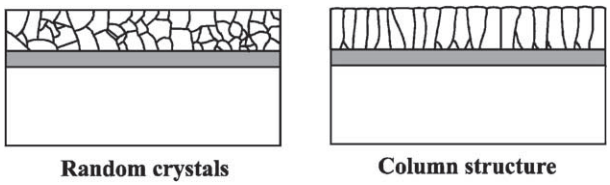

Fig. 1. Two polysilicon structures: (left) a random structure; (right) column structure.

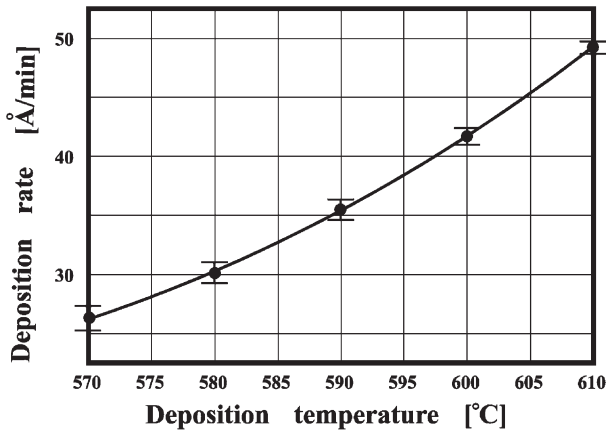

Fig. 2. Deposition rate as a function of temperature.

The system used in this case was a horizontal LPCVD system, similar to that shown in Fig. 3, with a 15 cm diameter tube. The pressure was 150 mTorr and the silane flow 45 sccm.

In recent years there has been increased interest in epi-poly. This is polysilicon deposited in an epitaxial reactor. This has the advantage of having a deposition rate in the range of 1 μm/min instead of 30–50 Å, found with LPCVD.

As we sweep through the temperature, we find two deposition regimes separated by a transition temperature. Below a certain temperature, the deposited films are not truly polysilicon but an amorphous film containing single-crystal grains. When the temperature is reduced, the grain

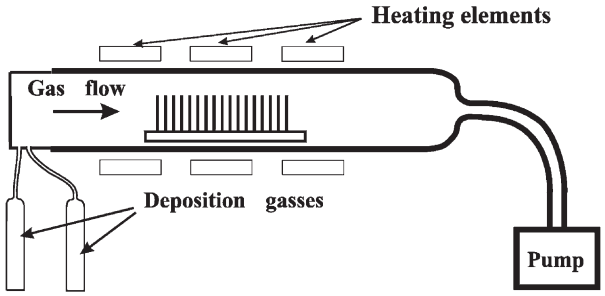

Fig. 3. Example of a horizontal LPCVD system.

size is not affected but the thickness of the amorphous layer between the grains increases. This amorphous layer readily takes the crystal orientation of adjacent grains with anneal temperatures below 1000 °C, until the amorphous layer is consumed and only a thin grain boundary is left. Anneal temperatures above this are needed for further grain growth. For depositions above the critical temperature, the grain boundaries are already formed and thus anneals above 1000 °C are required to achieve grain growth. The structure grain amorphous layer around the grains is shown in Fig. 4. The grain size in both cases is about 600 Å, but the grain density is quite different.

Fig. 5 shows an example of measured grain size as a function of deposition temperature after a 1000 °C anneal. For the lower temperature depositions, the amorphous layer surrounding the grain has been crystallised to form a full polycrystalline structure with larger grains.

3. Electrical and mechanical properties

As mentioned above, the material comprises small crystallites of single-crystal silicon separated by grain boundaries. These grain boundaries have a significant influence on the electrical properties of the material. In micromachined structures, the intrinsic stress in the material is an important

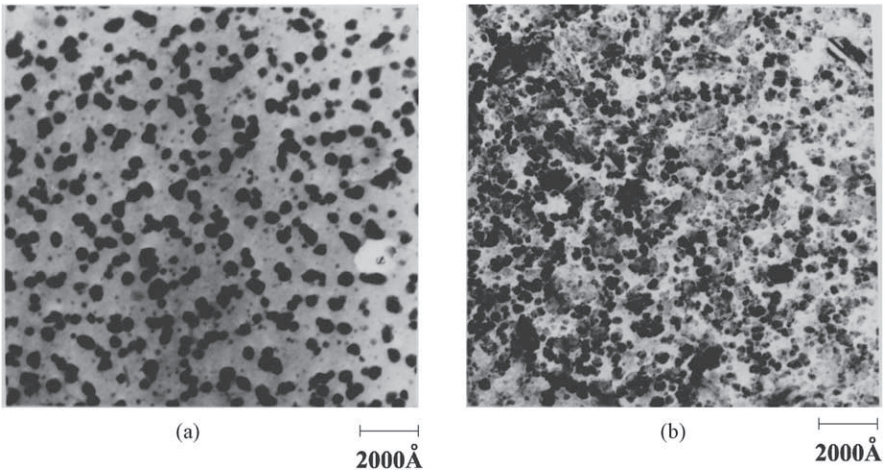

Fig. 4. Examples of two films deposited at (a) 560 °C and (b) 601 °C. In both cases, the grain size was approximately 600 Å.

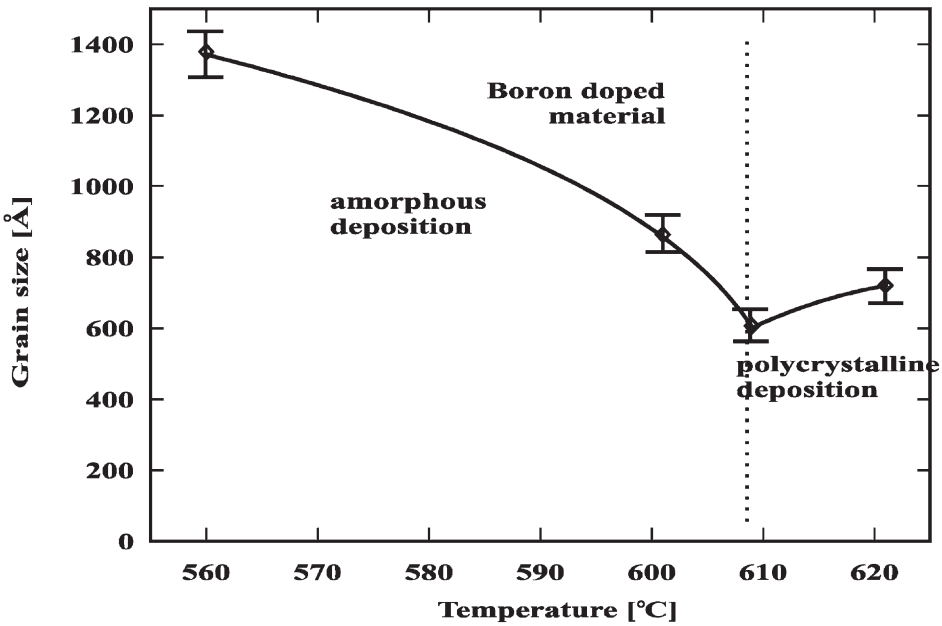

Fig. 5. Grain size as a function of deposition temperature. After deposition, samples were implanted with boron and annealed at 1000 °C for 30 min.

consideration; here too the grain boundaries can play an important role.

3.1. Electrical properties

Polysilicon can be modelled as a series of resistors, as shown in Fig. 6. Resistivity is also strongly affected by the grain boundary. The grain boundary can be considered as a Schottky barrier [11] with a semiconductor on both sides, leading to the model shown in Fig. 7. There have been a number of models to describe the carrier transport through the barrier. These usually involve two mechanisms, thermionic emission [12,13], where carriers have sufficient energy to pass over the barrier and tunnelling or diffusion through the barrier. The idea of thermionic emission combined with quantum tunnelling was suggested by Tarng [14], which had previously been used for Schottky barriers [15]. This was further developed for polysilicon grain boundaries [16,17]. A further model combining thermionic emission and diffusion was suggested by Singh et al. [13] based on a model for metal semiconductor barriers [11]. In normal operation, the voltage drop across each grain boundary is small. The boundary can thus be treated as a linear resistor and thus in a simplified form, assuming a linear resistor, the resistivity, ρ, of a polysilicon film can therefore be defined by

$$\rho = \left[\frac{L-(2w+\delta)}{L}\right]\rho_{\mathrm{g}} + \left[\frac{2w+\delta}{L}\right]\rho_{\mathrm{b}}$$

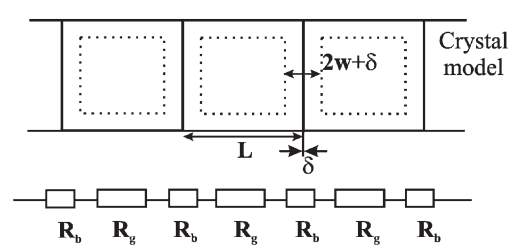

Fig. 6. Simple electrical model for polysilicon.

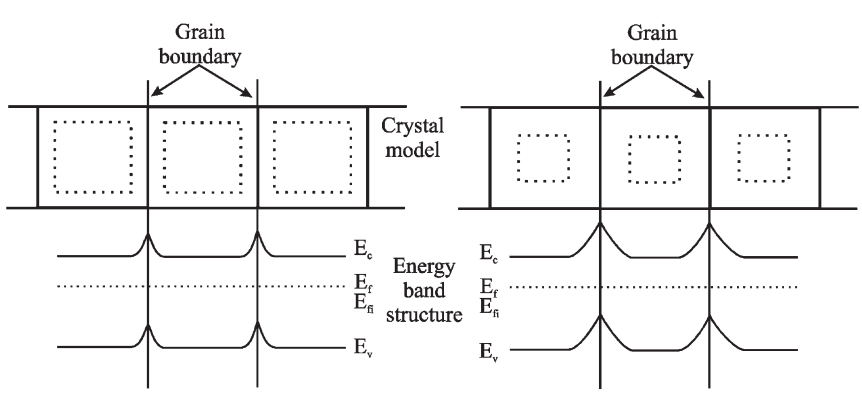

Fig. 7. Model structure showing the band bending due to the barrier: (left) high doping; (right) low doping.

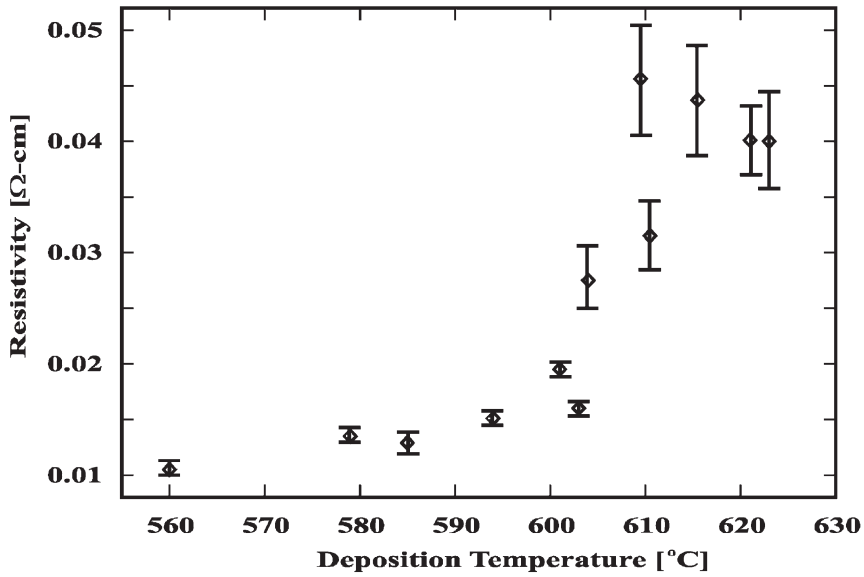

Fig. 8. Resistance as a function of deposition temperature. Layers were ion implanted in phosphorus to a dose of 1×10^{15} cm^{-2} and annealed at 1000 °C for 30 min. Taken from [18].

where L, w and δ are as defined in Fig. 6, and ρ_g and ρ_b are the grain and barrier resistivity, respectively.

It has been shown that forming the grain boundary at deposition leads to a higher number of traps and therefore a higher barrier and a greater width, as shown in Fig. 7. This shows that the grain size is the same in each case but the difference in barrier height leads to a greater proportion of the film being grain boundary. Since ρ_b is larger than ρ_g, this results in higher film resistance. Therefore a step in resistance can be found corresponding to the critical temperature. This is illustrated in Fig. 8.

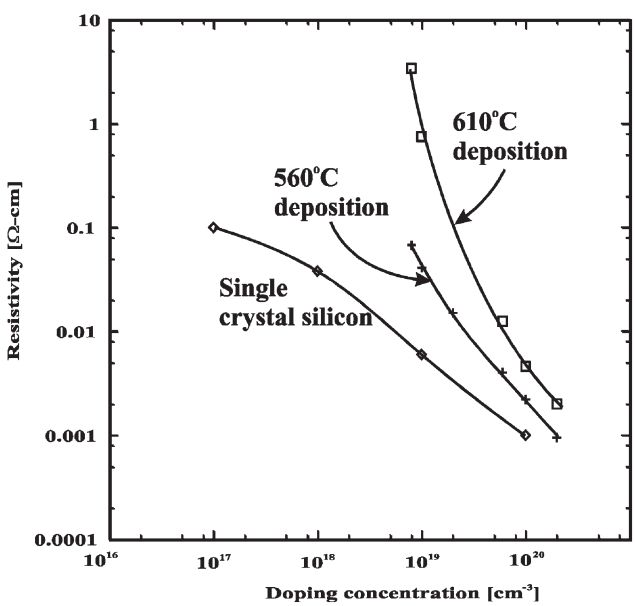

Fig. 9. Resistivity as a function of doping concentration for single crystal and polycrystalline silicon [18].

The effect of the grain boundary can also be seen in the sharp fall in resistance with increasing doping level, as shown in Fig. 9. The influence of the grain boundary can also be seen in the temperature coefficient or resistance. Around room temperature single-crystal silicon has a positive TCR, whereas the grain boundary has a negative TCR, similar to a Schottky barrier. The influence of the two regions is shown in Fig. 10. It can also be seen that the 609 °C deposited films have a higher negative value. This is again due to the fact that grain boundaries formed at deposition have higher trap densities and thus a greater grain boundary contribution.

3.2. Mechanical properties

Young's modulus of silicon is highly dependent upon crystal orientation. The value for polysilicon has been found to fall between the maximum and minimum crystalline values [19], which indicates that the grain boundary does not have a significant effect. This is illustrated in Fig. 11.

The intrinsic stress, on the other hand, has been found to be highly dependent upon how the grain boundaries are formed. High stress levels in films on the surface of the silicon wafer can cause significant problems in devices below. For micromachining it is also extremely important, even when at relatively low levels. When polysilicon is in compressive stress double clamped structures will tend to buckle. Only structures under a critical length will remain flat [20]. The ideal for most applications is low tensile stress. This will ensure that the mechanical structures are pulled into the correct shape, although high tensile stress will lead to breakage. The second consideration for stress is the stress profile. Although the films are generally less than 1 μm thick, a difference in stress between the upper and lower

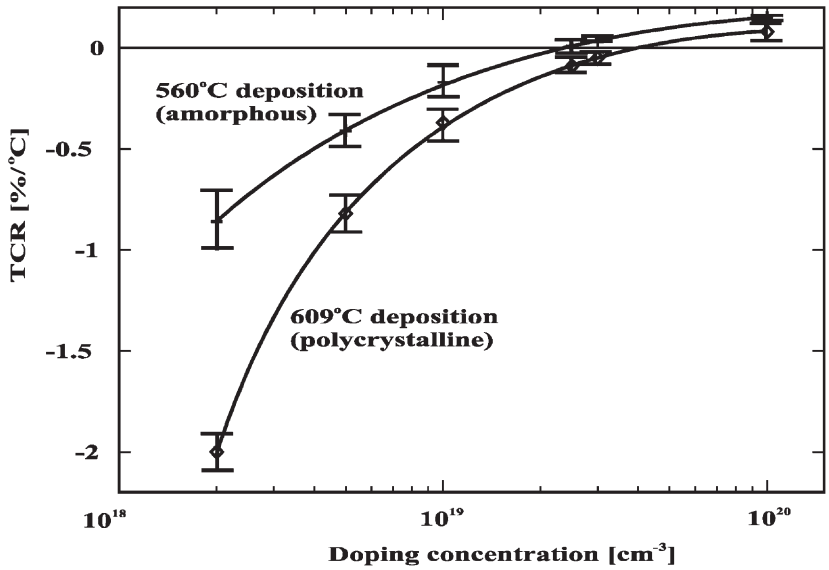

Fig. 10. TCR as a function of boron doping concentration. Taken from [18].

surfaces can cause severe bending of structures. In general, polysilicon deposited in polycrystalline form is in compressive stress [21] but this can be removed using a high-temperature anneal. This effect is shown in Fig. 12.

However, this is not always possible if the devices are integrated with other devices. The solution has been found to be depositing below the critical temperature, and therefore without forming the grain boundaries. If these samples are given an anneal, even as low as 600 °C [22–24], the amorphous regions around the crystallites will be crystallised until the grain boundaries are formed. Since the crystalline form has a smaller volume than the amorphous form, the shrinking of the material shifts the stress from compressive to tensile. This is also achieved when the samples are annealed after ion implantation. This effect is illustrated in Fig. 13.

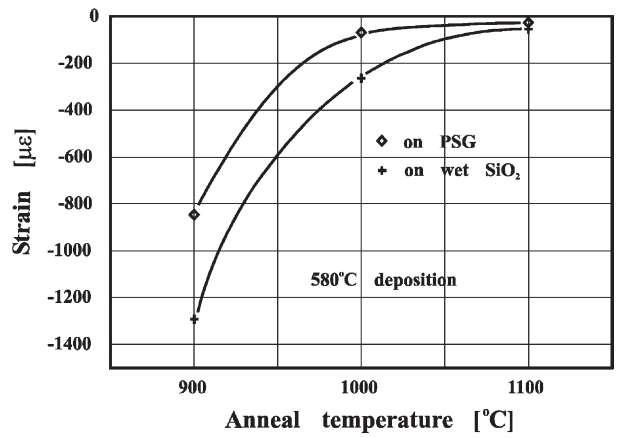

Fig. 12. Measured strain in polysilicon as a function of anneal temperature, for two underlying layers. Redrawn from [20].

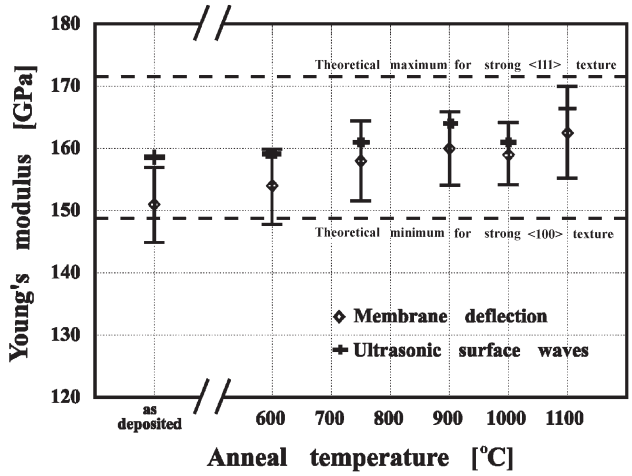

Fig. 11. Young's modulus of LPCVD polysilicon as a function of annealing temperature, measured using two techniques. The anneal time in each case was 2 h. Redrawn from [19].

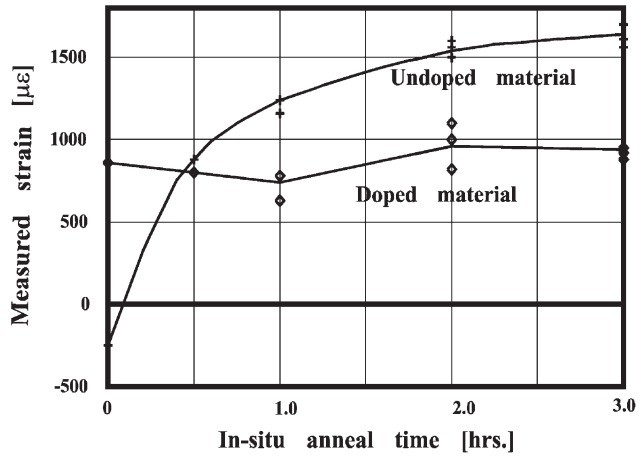

Fig. 13. Intrinsic strain as a function of in situ annealing at 600 °C. The doped samples were ion implanted with boron and then annealed at 850 °C for 30 min. Taken from [24].

4. Applications

Polysilicon has found a wide range of applications for microsystem. The following sections will concentrate on piezoresistive devices and surface micromachining.

4.1. Piezoresistive devices

Piezoresistance is the change in resistivity of a material due to mechanical stress. Simple resistors, often used in the form of a Wheatstone bridge, can be used for stress sensors. The sensitivity of the material is usually given as the gauge factor, which is defined and the relative change in resistance, R, per unit strain, by

$$G = \frac{\Delta R}{R\varepsilon} = 1 + 2v + \frac{\Delta\rho}{\rho\varepsilon}$$

where v is Poisson's ratio, ρ the resistivity and ε the applied strain.

This was one of the first sensor applications for polysilicon [5–10]. It was found to have a considerably higher sensitivity than metal-based films and although not as high as single-crystal silicon it had the advantage of being able to deposit on a range of insulating layers. In this application, the grain structure has been found to be highly significant. There are two aspects. The first is the crystal orientation of individual grain and the second is the contribution of the grain boundary. Considering the first aspect. The piezoresistive coefficient of polysilicon grain is estimated by taking the average value for each grain. In some polysilicon structures there is a texture, which means that a small number crystal orientations, whereas other films have been found to have a totally random structure. Grain orientations quoted in the literature include (1 0 0), (1 1 0), (3 1 1), (3 3 1) and (1 1 1) [25]. As shown in Table 1, this can have a significant effect on the magnitude of the gauge factor.

The piezoresistive coefficient is defined as the change in resistivity per unit stress and therefore the gauge factor is defined by

$$G = \frac{\Delta R}{R\varepsilon} = 1 - 2\frac{S_{ij}}{S_{ii}} + \frac{\pi}{S_{ii}}$$

The second aspect is the influence of the grain boundary on piezoresistance. As shown in Fig. 6, the films can be considered as a series resistor string and thus both types of resistor contribute to the piezoresistive effect. It has been shown that the coefficient of the grain boundary is low and this limits the values obtainable. The change in resistivity of polysilicon can be found by differentiating yielding

$$\frac{\Delta\rho}{\rho} = \frac{[L - (2w + \delta)]}{L}\frac{\Delta\rho_g}{\rho\varepsilon} + \left[\frac{2w + \delta}{L}\right]\frac{\Delta\rho_b}{\rho\varepsilon}$$

As with resistivity a sharp step is found when films are deposited around the critical temperature. This effect is shown in Fig. 14. Films deposited at below the transition temperature have a smaller barrier.

Plotting the gauge factor as a function of doping concentration also reveals the effect of the barrier. Fig. 15 shows the gauge factors over a range of doping concentrations.

The fall for high concentration is due to the high doping effects, also found in single-crystal silicon [26] whereas the fall for lower doping levels is due to the domination of the grain boundary. The values here can be compared to maximum achievable values for single-crystal silicon of more than 100.

4.2. Micromachining

Basic surface micromachining is shown in Fig. 16. The two layer types are a mechanical layer and a sacrificial layer, which is removed to form the free-standing structure. Polysilicon has been shown to be suitable for both applications, although its role as a mechanical material has received more attention.

Since the first demonstrations of moving polysilicon parts surface micromachining has received considerable attention. As shown above, it is important to optimise the processing to

Table 1
Piezoresistive coefficients, π, gauge factors, G, Young's modulus, E, and Poisson's ratio, v_{ij}, averaged for a number of polysilicon textures[a]

		Texture					
		(1 0 0)	(1 1 1)	(3 1 1)	(1 1 0)	(3 3 1)	Random
π'_l	n-Type	−68.0	−31.6	−56.9	−40.9	−38.2	−55.8
G_l	n-Type	−97.2	−53.4	−85.7	−61.4	+59.4	−82.1
π'_l	p-Type	+39.4	+72.8	+49.5	+64.2	+66.7	+53.1
G_l	p-Type	+61.5	+122.9	+77.7	+111.7	+114.5	+87.5
π'_l	n-Type	+18.5	+30.1	+24.1	+27.4	+28.3	+37.0
G_t	n-Type	+24.0	+50.9	+35.0	+43.1	+45.3	+55.5
π'_l	p-Type	−33.8	−23.1	−28.7	−25.6	−24.9	−18.1
G_t	p-Type	−53.3	−39.1	−45.9	−44.4	−42.8	−30.3
E	$1/S_{ii}$	+1.5	+1.71	+1.56	+1.67	+1.68	+1.60
v_{ij}	$-S_{ij}/S_{ii}$	+0.25	+0.21	+0.23	+0.22	+0.22	+0.27

[a] Subscripts l and t denote longitudinal (stress parallel to current flow) and transverse (stress perpendicular to flow). All values are defined for tensile stress.

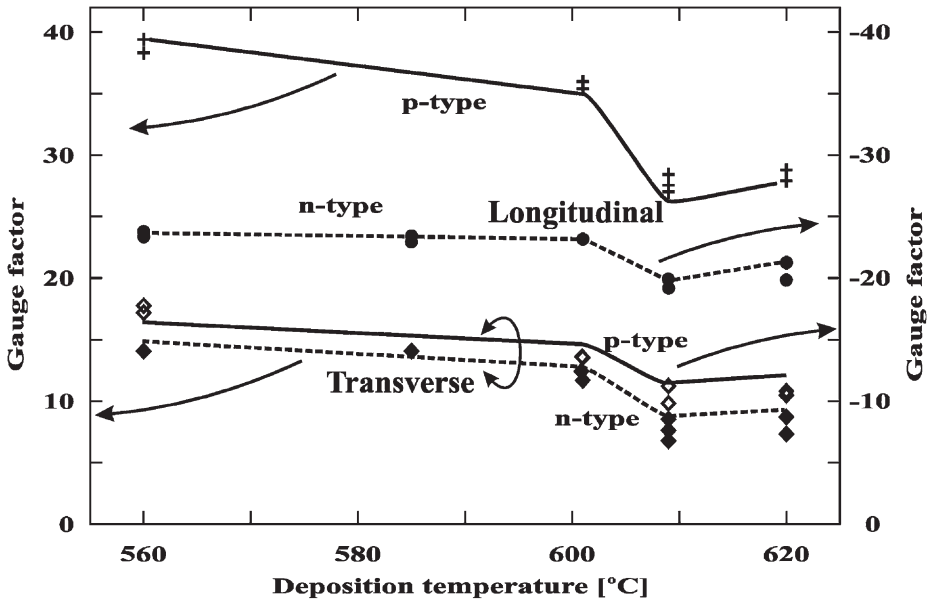

Fig. 14. Gauge factor as a function of deposition temperature. All films were annealed at 1000 °C after implantation.

achieve the desired mechanical properties. If this is done polysilicon is highly suitable for micromechanics often with silicon dioxide as the sacrificial layer. Both LPCVD and epi-poly have been successfully applied. Examples of LPCVD and epi-poly structures are given in Fig. 17. The epi-poly structure in this case is 4 μm thick and shows part of a lateral accelerometer. The LPCVD structure was fabricated in the Sandia Labs using a 5-layer polysilicon process.

With polysilicon there are a number of process options to integrate with electronics. This can be:

- pre-processing;
- integrated processing;
- using existing layers;
- post-processing.

All of these options have issues which much be addressed. In the first option, polysilicon microstructures are formed in etched pits before processing. The pits are then filled and the wafer planarised. The wafers can then be treated as normal process wafers and only after processing the structures can be released [29]. This maintains totally standard electronics processing, although the processing of the polysilicon has to be adjusted to ensure the correct mechanical properties after a long thermal treatment [30]. In the second approach, the polysilicon for the micromachining is integrated into the

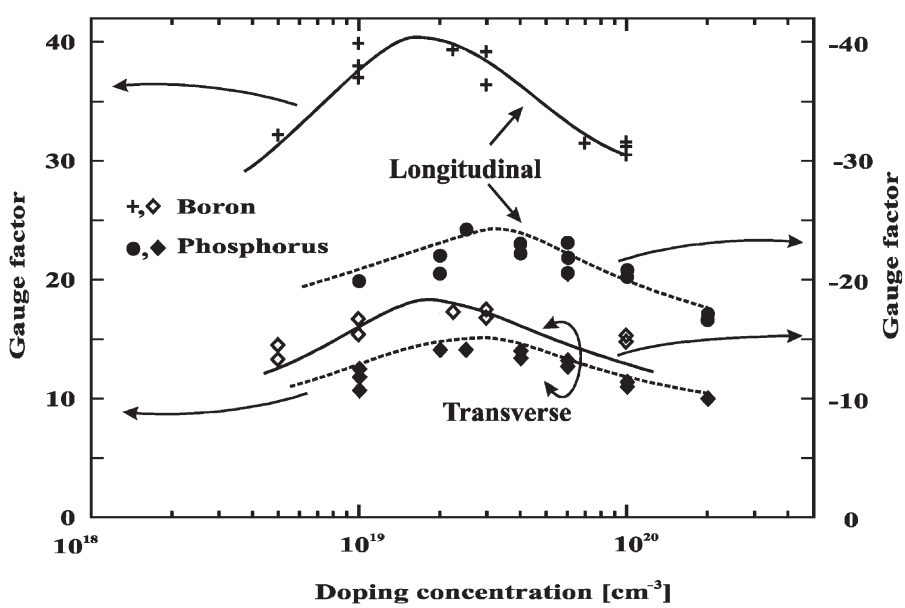

Fig. 15. Graph of gauge factor as a function of doping concentration for both boron- and phosphorus-doped material. All films were deposited at 560 °C.

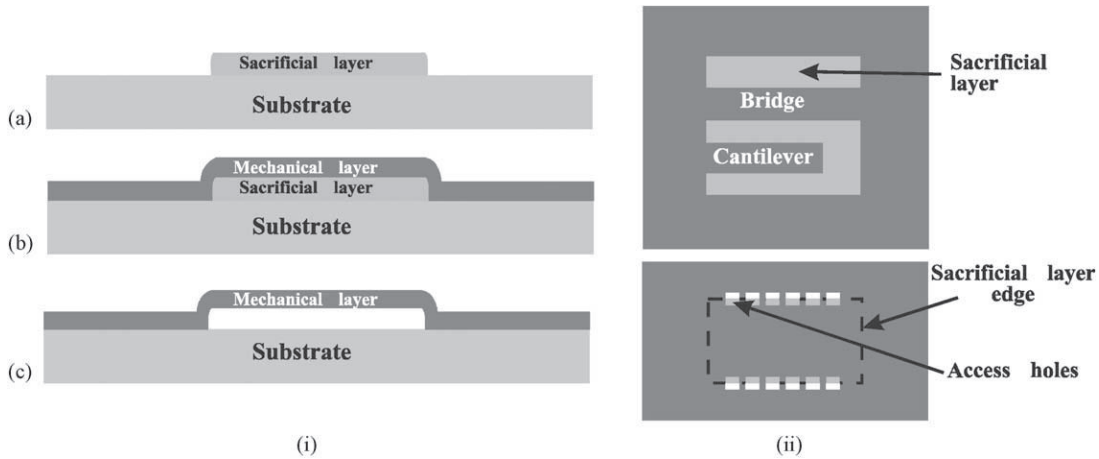

Fig. 16. Basic surface micromachining process: (i) cross-sectional view; (ii) planar view of simple structure.

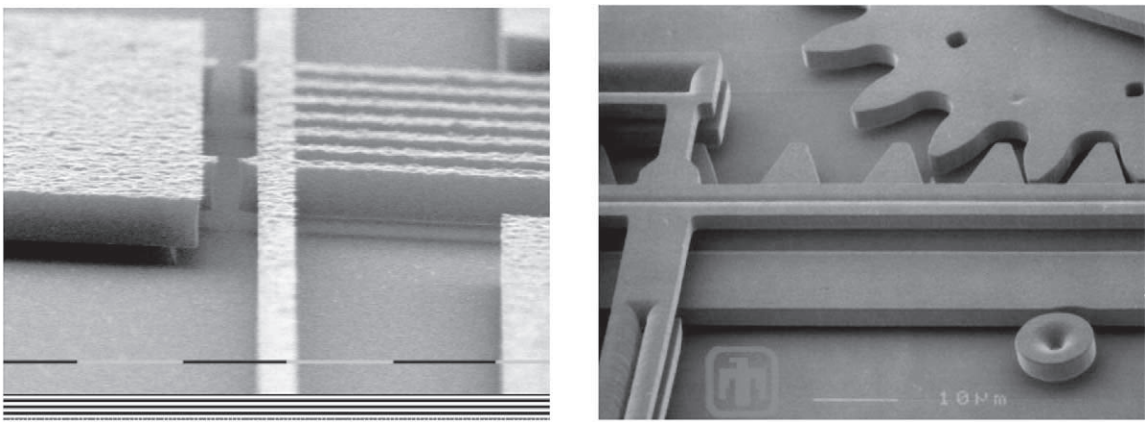

Fig. 17. (Left) close up of an epi-poly structure (reproduced with kind permission of Gennissen [27]) and (right) mechanical structure fabricated in the Sandia multi-level polyprocess (reproduced with kind permission of Sandia labs [28]).

standard process as additional processing steps, after the main thermal treatment but before aluminium. An example of this approach is given in Fig. 18 [31]. The approach limits the thermal budget of the micromachining, but does allow optimisation of the mechanical layers. However, this does require access to the process line.

An alternative approach is to use existing polysilicon layers. Many IC processes use polysilicon and this can be

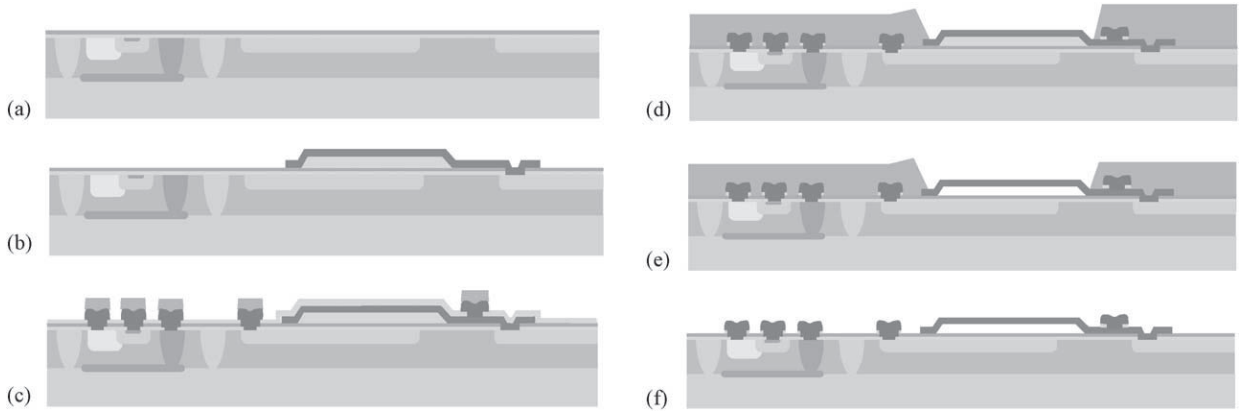

Fig. 18. Integrated approach: (a) end of bipolar thermal process; (b) LPCVD; (c) aluminium; (d) resist protection of the circuitry; (e) sacrificial etching; (f) removal of resist.

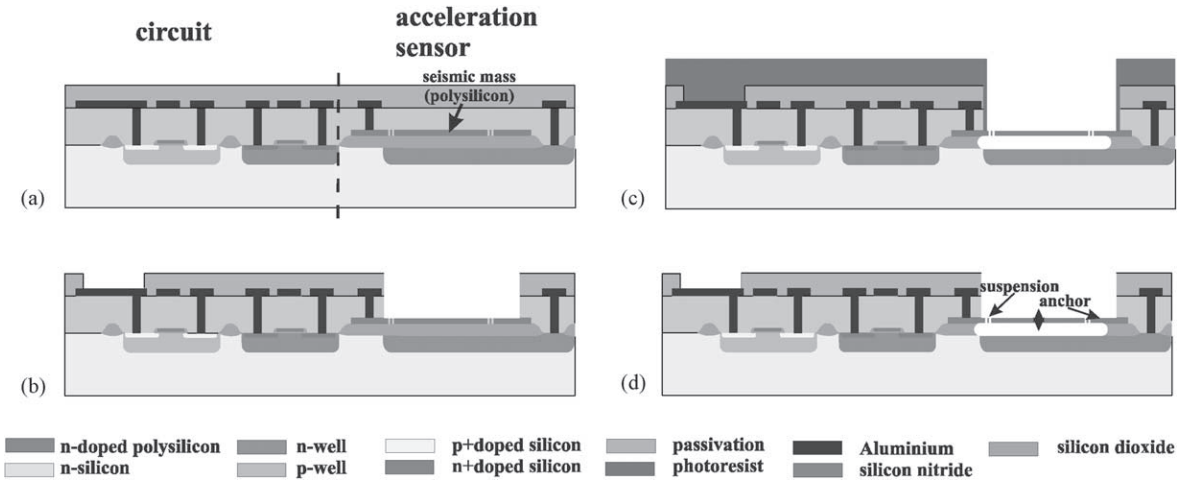

Fig. 19. Surface micromachining using gate poly as the mechanical layer [32].

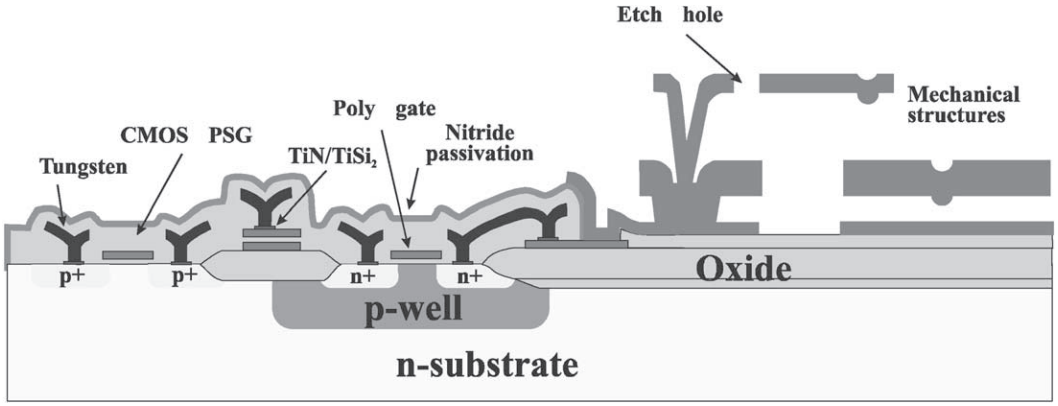

Fig. 20. Cross-section of polysilicon-based surface micromachined structure using post-processing micromachining. Redrawn from [33].

used as a mechanical layer, as shown in Fig. 19 [32]. This process, developed at Siemens, uses the polysilicon gate as the mechanical layer and the field oxide as the sacrificial layer. In all these processes, the problems arise that the layers in CMOS or bipolar are not design for mechanics and often have compressive mechanical stress. Therefore stress compensation has to be introduced through design. However, in the case where access to the line is possible processing can be adjusted which gives the desired mechanical properties without a detrimental effect on the electronics.

Post-processing places greater constraints on the thermal budget. If aluminium is used the thermal processing is limited to 400 °C, which is below the LPCVD temperature. This means that only PECVD can be used. An alternative approach is to use a metal which can survive the higher temperatures. Bustillo et al. [33] used tungsten as the metallisation where after processing a protection layer was deposited over the wafer followed by standard surface micromachining. A cross-sectional view of one of these structures is given in Fig. 20.

Polysilicon can also be used as a sacrificial layer either using TMAH or KOH [34] or by making it porous and then removing the porous layer [35].

5. Conclusions

Polysilicon has been shown to be a highly flexible material for microsystem applications. From the early days as interconnect, gates and capacitors, it has expanded to mechanical sensors and actuators with the help of micromachining techniques. The piezoresistive effect in polysilicon is lower than that of single-crystal silicon. However, it has the advantage of not requiring a p–n junction as isolation and has greater flexibility since there is no single-crystal orientation. In micromachining, polysilicon has been found highly suitable as a mechanical and sacrificial layer, although the role as a mechanical material has received more attention. Since the 1980s, polysilicon has been widely used for micromechanical structure in both sensor and actuator applications.

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