

UNITED STATES PATENT AND TRADEMARK
OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMPHENOL CORP.,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

Case No. IPR2025-00607
Patent No. 11,495,898

DECLARATION OF SHUKRI SOURI, Ph.D.
IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO.
11,495,898

~~UNDER 35 U.S.C. §§311-319 AND 37 C.F.R. §42.1 et seq~~

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Other Authorities

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~~Proceedings Before the Patent Trial and Appeal Board,~~

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EXHIBIT LIST I. INTRODUCTION

A. Engagement

1. I am a salaried employee of Exponent, Inc. (“Exponent”). Exponent charges \$925 per hour for my time plus expenses for work performed in connection with this matter. I have received no additional compensation for work in this case, and my compensation does not depend upon the contents of this report, any testimony I may provide, or the ultimate outcome of the case.

2. Exponent is an engineering and science consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025. I am a Principal and a Corporate Vice President at Exponent. I am based in, and Director of, Exponent’s New York office. I am also the Director of Exponent’s Electrical Engineering and Computer Science practice.

3. Exponent has been retained by Counsel for Amphenol in this matter to provide independent technical expert consulting services. I, Shukri Sourì, am the investigator for the subject matter in this report.

B. Background and Qualifications

4. My curriculum vitae (“CV”) detailing my educational background, professional experience, and list of publications is provided as Exhibit 1004

(EX1004). Some of my background and experience that qualifies me to offer the opinions in this Declaration as an expert in the technical issues in this case are as follows.

5. I received my B.A. (Honors) and M.A. in Engineering Science from Oxford University in the UK; my Master's degree in Electrical Engineering from Stanford University, California; and my Ph.D. in Electrical Engineering, also from Stanford University, California.

6. Before returning to Stanford for my Ph.D., I was a member of the staff at Raychem's Corporate Research and Development Laboratories, where I researched and built electronic systems to target reliable and safe operation of commercial and industrial equipment. My work resulted in patents awarded by the United States, European, Japanese, and World Intellectual Property Organization patent offices.

7. My Ph.D. work at Stanford was generally in the area of 3-dimensional design and fabrication of Integrated Circuits ("ICs"). My contributions included novel electrical interconnect architectures to enable Giga Scale Integration ("GSI") and enhanced speeds in ICs.

8. Since joining Exponent, my professional activities have included working with industry members to understand failure modes of their products, whether such failures occur in the field after deployment, during manufacturing

and quality assurance, or even earlier in the design and modeling phase. The knowledge acquired during such root cause investigations is typically fed back into the manufacturer's product life cycle for purposes of improving yield, quality, reliability, safety and lifetime of the same or new product.

9. I also work with government institutions to advise on technological investigations and challenges. For example, I was selected to United States National Academy of Engineering Frontiers of Engineering Symposium to help address future technological challenges facing society; and I also advised members of the United States Congress in their Investigation into Instances of Sudden Unintended Acceleration in Toyota Made Vehicles, as instituted by the Committee on Energy and Commerce in the House of Representatives.

10. My experience with electrical connectors and relevant electrical/electronic materials spans over 25 years. During this time, I have worked on research and manufacturing of electrically insulating materials; non-linear electrically conducting polymeric materials; and investigated design, manufacturing and assembly issues related to failures of electrical connectors. This included analyses of connector failures on Printed Circuit Boards ("PCBs") due to issues related to design, manufacturing, quality and assembly.

11. By way of example, as a Scientist at Raychem in the mid- to late90's, I began my research in, and developed, electrical material systems and devices

based on conductive polymeric materials. Such material systems and devices can exhibit Positive Temperature Coefficient of Resistance (PTC-R) effects: whether due to externally applied or active Joule heating, the thermal expansion of the loaded matrix causes a disruption in the conductive network, increasing electrical resistance. Products based on PTC-R materials have been deployed for various applications, including self-regulated heating, resettable fuses, and thermal sensors, as examples. As a Research Engineer at Raychem, now part of TE Connectivity, my research encompassed designing and working with connector components including for Printed Circuit Boards (“PCBs”), fiber optics cables, high frequency applications, automotive and telecom industries.

12. Over the years, and particularly for electrical connectors, I have led several investigations at Exponent to identify the root cause of failures involving connectors on PCBs. As examples, such failures have involved backplanes and mainboards in applications for data centers or high-reliability computing. These failures were occurring in field-deployed devices as well as during accelerated lifetime tests as performed by my teams at Exponent. Our work with industry resulted in efforts to address manufacturing practices to minimize the risk of failures, whether during testing or in the field. My experience with electrical connectors has also crossed various industry boundaries, including IT, automotive, industrial controls and healthcare applications, also as examples. I have also been

admitted as an expert in several litigation matters and offered opinions related to electrical connectors for various industries, including small form factor pluggable type connectors for high-speed electrical interconnections, such as QSFP, QSFPDD and OSFP, among others.

13. I am currently a Senior Member of the Institute of Electrical and Electronics Engineers. Additional details about my background and expertise, including publications, are further described in my professional resume, which is attached as Exhibit K to this report. This resume includes a list of all publications I have authored within the preceding ten years. It also includes a list of cases in which I have testified as an expert at trial or by deposition within the preceding four years.

14. In forming my opinions, I have relied upon the materials listed below, my education, training, and knowledge of connector technologies, electrical and electronic materials, and related experience.

C. Bases of My Opinions and Materials Considered

15. I have reviewed the '898 patent, its prosecution history, and the prior art and other documents and materials cited herein. For ease of reference, the full list of documents that I have considered is in the exhibit list below. I have also considered the documents cited and referenced herein, even if not included in the exhibit list below. Each of these materials is a type of document that experts in

my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent office and/or well-known libraries, conferences, publications, organizations, and websites in the field as further discussed herein.

16. My opinions, as explained below, are based on my years of education, research, experience, and background in the field of microelectronics and computing systems, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section III below. In forming my opinions, I have studied and considered the materials identified in the list below.

Exhibit	Description
1001	U.S. Patent No. 11,495,898 (“the ’898 patent”)
1002	Prosecution History of U.S. Patent No. 11,495,898
1003	Declaration of Dr. Shukri Sourì (“Sourì”)
1004	Curriculum Vitae of Dr. Shukri Sourì
1005	U.S. Patent Application Publication No. 2020/0194911 (“Ayzenberg”)
1006	U.S. Patent Application Publication No. 2013/0280955 (“Alden”)
1007	U.S. Patent No. 9,882,706 (“Lugthart”)
1008	Andy Turudic, et al., <i>Pre-Emphasis and Equalization Parameter Optimization with Fast, Worst-Case/Multibillion-Bit Verification</i> (DesignCon 2007) (“Turudic”)
1009	U.S. Patent No. 9,887,496 (“Janssen”)
1010	QSFP-DD Hardware Rev 5.0 (Jul. 9, 2019)
1011	Pages from Newton’s Telecom Dictionary (30th ed. 2016)
<u>Exhibit</u>	<u>Description</u>

1012	Pages from R. Horak, <i>Webster's New World Telecom Dictionary</i> (2008)
1013	'898 Patent Claim Limitation Comparison Chart
1014	U.S. Patent No. 11,228,123 ("Ayzenberg-123")
1015	U.S. Provisional Patent Application No. 62/780,504
1016	Ayzenberg Claim Limitation Comparison Chart
1017	TE connectivity, <i>QSFP-DD Connectors & Cable Assemblies: High Speed 400G Pluggable I/O Solutions</i> (2019)
1018	U.S. Patent No. 7,498,523
Exhibit	Description
1019	Redline Comparison Of Ayzenberg (EX1005) Specification To EX1015 Specification
1020	Griffiths, D.J., INTRODUCTION TO ELECTRODYNAMICS (4th ed. 2013).

~~MANDATORY NOTICES~~

~~A. — Real Party In Interest~~

~~Petitioner is the Real Party in Interest.~~

~~B. — Related Matters~~

~~U.S. Patent No. 11,495,898 issued D.~~ MY UNDERSTANDING OF PATENT LAW

17. In developing my opinions, I discussed various relevant legal principles with Petitioner’s attorneys. Though I do not purport to have prior knowledge of such principles, I understood them when they were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

18. I understand that “*inter partes* review” (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent’s claims based on prior art patents and printed publications.

19. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the ’898 patent are unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

20. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSA”) in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification’s special definition controls. If a claim element is expressed as a “means” for performing a specified function, I understand that it covers the corresponding structure described in the specification and equivalents of the described structure. I have applied these standards in preparing the opinions in this declaration.

21. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application’s filing date. I understand that a disclosure that merely renders the claimed invention obvious is

not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

22. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (novel—*i.e.*, not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

1. Anticipation

23. I understand that, for a patent claim to be “anticipated” by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA’s knowledge and experience.

24. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

2. Obviousness

25. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior art reference or a combination of prior art references.

26. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

x the scope and content of the prior art; x the differences between the prior art and the claims at issue; x the knowledge of a person of ordinary skill in the pertinent art; and x if present, objective factors indicative of non-obviousness, sometimes referred to as “secondary considerations.” To my knowledge, the Patent Owner has not asserted any such secondary considerations with respect to the '898 patent.

27. I understand that in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior art references (or for altering a single prior art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

28. I further understand that in determining whether a prior art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

x combining prior art elements according to known methods to yield predictable results; x simple substitution of one known element for another to obtain predictable results; x use of a known technique to improve similar devices in the same way; x applying a known technique to a known device ready for improvement to yield predictable results; x applying a technique or approach that would have been “obvious to try,” i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.

x known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;

x some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed

invention. I understand that this teaching, suggestion or motivation may come from a prior art reference or from the knowledge or common sense of one of ordinary skill in the art.

29. I understand that for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

3. Claim Interpretation

30. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the claim. In this section, I discuss the interpretations I have applied to certain claim terms in my analysis.

31. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification and the prosecution history (i.e., the intrinsic record).

32. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the

context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

33. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the time of the alleged invention. This can be useful for technical terms whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic

evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

34. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Declaration, I apply the above standards to the terms in the challenged claims. The meanings of specific terms are discussed below in connection with evaluating the disclosure in the priority documents.

II. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

35. I have reviewed the '898 patent (EX1001) and its prosecution history (EX1002).

36. I understand that the '898 patent issued from U.S. Patent Application No. 17/146,350, which claims priority to foreign patent ("the '350 application No. CN"), filed on January 11, 2021. EX1001, codes (21), (22).

37. I understand that the '350 application relates to Chinese Patent Application No. 202010149136.4, which was filed on March 5, 2020. -EX1001, code (30).

C. — Counsel and Service Information — 37 C.F.R. §§42.8(b)(3) and (4)

<u>Lead Counsel</u>	<u>Adam R. Wichman, Reg. No. 43,988</u>
<u>Backup Counsel</u>	<u>Michael S. Parsons, Reg. No. 58,767—</u>

Service Information	<u>E-mail: AWichman-PTAB@WolfGreenfield.com</u> <u>MParsons-PTAB@WolfGreenfield.com</u> <u>Post and hand delivery: Wolf, Greenfield & Sacks, P.C.</u> <u>600 Atlantic Avenue</u> <u>Boston, MA 02210-2206</u> <u>Telephone: 617-646-8000</u> <u>Facsimile: 617-646-8646</u>
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~~A power of attorney is submitted with the Petition. Counsel for Petitioner consents to service of all documents via electronic mail.~~

Amphenol Corporation (“Petitioner”) requests *inter partes* review and cancellation of claims 1-20 (the “Challenged Claims”) of U.S. Patent No. 11,495,898 (EX1001, “the ’898 patent”).

I. INTRODUCTION

38. I have been instructed by counsel to assume the relevant timeframe for my analysis of the prior art in this Declaration is on or before March 5, 2020.

39. Based on my review of this material, I believe that the relevant field for the purposes of the ’898 patent is high-speed interconnects.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

40. I have been informed and understand that for purposes of assessing whether prior art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date.

41. I have been informed and understand that various factors may be considered in assessing the level of a POSA, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. I have also been

informed and understand that not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. I have further been informed and understand that these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. I have applied this standard throughout my declaration.

42. The '898 patent involves technology in the field of connector paddle card designs. I have been asked to provide my opinions as to the state of the art in this field by early 2020. I use this timeframe because the face of the '898 patent indicates an earliest claimed priority date of March 5, 2020. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '898 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the early 2020 timeframe, even if I do not say so specifically in each case.

43. In the context of the '898 patent and the prior art, it is my opinion that the POSA to whom the patent is addressed, before March 5, 2020, would have had a Bachelor's degree in computer or electrical engineering or a related scientific field and two years of experience with interconnects for high-speed communications. A POSA would have had a working knowledge of signal integrity and how it is affected by various PCB and cable designs, as well as

industry standards such as QSFP-DD (EX1010) governing cable assemblies and connections for high-speed communication. A POSA would have understood the technology surrounding mounting a cable to another structure, such as a PCB. More education could substitute for experience, and vice versa. A POSA would have been capable of understanding and applying the teachings of the '898 patent and the prior-art references discussed in this declaration.

44. The basis for my familiarity with the level of ordinary skill is my own technical experience and my interaction with students and professionals in the field of high-speed interconnects who were at this level of skill as of March 5, 2020. I am well aware of the knowledge that a POSA would have had at the time this patent was written as I have been actively consulting, teaching, and carrying out research with such students and/or professionals for approximately 25 years prior to March 5, 2020.

45. My opinion identifying the POSA's level of ordinary skill is consistent with the problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field. This is shown, among other things, by the prior art references described in the Grounds below.

46. For example, POSAs were aware that cables for “high frequency signals” use various components (e.g., signal wires terminated to PCBs) that “impact signal propagation.” EX1005, [0003]-[0005]. “Non-uniformities on a signal path... created by changes in shape or material of the components, give rise to changes in impedance or promote mode conversion, which reduce signal integrity, as these effects are manifested as insertion loss, crosstalk or other undesirable effects.” *Id.*, [0005]. As early as 2012, market demand for smaller and higher-performance cables motivated POSAs to explore various improvements to these components, and how they connect, to overcome these undesirable effects. *See, e.g.*, EX1006, [0003]-[0004]. Ayzenberg and Alden found that crosstalk can be decreased in such high-speed cables when the electrodes on a PCB terminating the cable’s signal wires are staggered across two rows. EX1005, [0045], Fig. 4A; EX1006, [0025], [0039], Fig. 1. Lugthart found that including an active transceiver at each cable end “permit[s] communication over longer distance... with a thinner cable,” as well as “decreas[ing] jitter, noise, and/or ISI [(intersymbol interference)]. EX1007, 15:5-10. POSAs were thus aware of various problems that arise in designing smaller and higher-speed cables, and were actively designing various solutions prior to March 5, 2020 to mitigate undesirable effects caused by cable component design and assembly.

47. As summarized above with regards to my qualifications and experience, I possessed at least the level of skill of a POSA at the time of the alleged invention of the '898 patent.

48. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill in and around March 2020. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above.

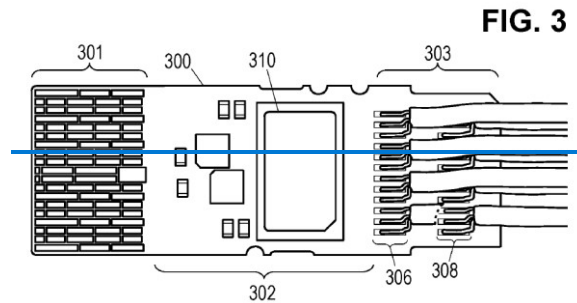
49. Except as noted below whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the '898 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the March 2020 timeframe, even if I do not say so specifically in each case.

IV. THE '898 PATENT¹

~~The '898 patent concerns printed circuit boards (“PCB”) called “paddle cards” that terminate shielded signal wires in a data cable. Modular connectors—described in well-known industry standards—conventionally enclose the PCBs and~~

¹ AllThroughout this Declaration when I quote language from a reference all emphasis in the Petition is added unless otherwise indicated.

physically connect with matched receiving sockets to provide electrical connection to attached signal wires. Data cables terminated with such connectors routinely interconnect electronic devices.



Exemplary '898 paddle card

The '898 patent purports to have invented staggering signal wire solder contacts along an edge of the PCB, and providing a recess that receives sheathing surrounding signal wires to leave the wire leads flush against the PCB surface. The '898 patent issued with no meaningful examination.

The claims should never have issued. The '898 patent's alleged invention was well known and described in patent documents filed by industry practitioners long before the '898 patent was filed. Industry standards described paddle cards connecting networked devices via an edge connector that passes signals received over copper signal wire. A PCB with staggered signal wires connections pads and a recess for the signal wire sheathing enclosed by connectors comporting with industry standards was well known.

~~**Ground 1** shows that Ayzenberg, an Amphenol patent application, anticipates and/or renders obvious independent claims 1, 9, and 16, and dependent claims 2, 10, and 18.~~

~~**Ground 2** shows that Ayzenberg in view of Lugthart renders obvious claims 3, 11, and 17—requiring an IC on the PCB. **Ground 3** shows that Ayzenberg in view of Janssen renders obvious claims 4-8, 12-15, and 19-20—requiring a recess on the PCB for the wire sheathing.~~

~~Alden also taught the alleged invention before PO filed the '898 patent. **Ground 4** shows that Alden anticipates or renders obvious independent claims 1, 9, and 16, and dependent claims 2, 10, and 18. **Ground 5** shows that adding staggered signal wire leads, as in Alden, to Lugthart's PCB with an IC, renders obvious claims 3, 11, and 17. **Ground 6** shows that adding staggered signal wire leads of Alden to Janssen's PCB renders obvious claims 4-8, 12-15, and 19-20.~~

~~Accordingly, Petitioner requests that the Board institute IPR and cancel the Challenged Claims.~~

~~II.—STANDING CERTIFICATION~~

~~Petitioner certifies that the '898 patent is available for IPR. Petitioner is neither barred nor estopped from requesting IPR. 37 C.F.R. §42.104(a).~~

III. UNPATENTABILITY GROUNDS

Petitioner relies on these references. The AIA applies because the '898 patent's effective filing date is after March 16, 2013. EX1001, code (22), (30).

Name	Provisional Date	Filing Date	Issue/Pub. Date	Basis
Ayzenberg (EX1005)	2018-12-17	2019-12-16	2020-06-18	102(a)(2)
Alden (EX1006)		2012-04-24	2013-10-24	102(a)(1)
Lugthart (EX1007)		2016-12-28	2018-01-30	102(a)(1)
Janssen (EX1009)		2016-06-13	2018-02-06	102(a)(1)

Ayzenberg issued as U.S. Patent No. 50. The '898 patent is titled "Connector Paddle Card with Improved Wiring Connection Geometry." Its Abstract says it provides 11,228,123 (EX1014, "Ayzenberg123"). Ayzenberg is entitled to the filing date of its provisional application No. 62/780,504 (EX1015) because Ayzenberg meets the "ministerial requirements" of 35 U.S.C. §119. *Penumbra v. RapidPulse*, IPR2021-01466, Paper 34, 32-34 (Mar. 10, 2023) (precedential as to §II.E.3), appeal pending. Ayzenberg claims priority to and was co-pending with its provisional (EX1005, codes (22), (60), [0001]), both share common inventors (EX1005, code (72); EX1015, 6-8), and both describe the

same subject matter. 35 U.S.C. §§102(a)(2), 102(a)(d)(2), 119; EX1019 (redline showing changes in the text of Ayzenberg (EX1005) compared to its provisional (EX1015)); EX1003, Declaration of Dr. Shukri Sourì (“Sourì”), ¶¶60-62.

Ayzenberg is also entitled to its provisional filing date because the provisional application’s written description supports the invention claimed in Ayzenberg 123. *Dynamic Drinkware v. National Graphics*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). For example, application claim 5 recites each limitation in Ayzenberg 123, claim 1. Compare EX1015, 31-32 (application claims 1, 5) with EX1014, claim 1; EX1016, 1. Petitioner respectfully requests that the Board find the Challenged Claims unpatentable, and cancel them as follows. 37 C.F.R. §42.104(b).

Ground	Reference(s)	Claims	Basis
1	Ayzenberg	1-2, 9-10, 16, 18	102/103
2	Ayzenberg+Lugthart	3, 11, 17	103
3	Ayzenberg+Janssen	4-8, 12-15, 19-20	103
4	Alden	1-2, 9-10, 16, 18	102/103
5	Lugthart+Alden	3, 11, 17	103
6	Janssen+Alden	4-8, 12-15, 19-20	103

40.

~~IV. THE '898 PATENT~~²

~~The '898 patent concerns~~ connector paddle cards “with “an improved wiring connection geometry that reduces impedance mismatch.” EX1001, Abstract.

A. Described Embodiments

51. According to the '898 patent, a “paddle card” is “a specialized type of daughter card that functions as an adapter, typically having a minimal number of electronic components that couple signals from the edge connector to external

system components.” EX1001, ~~Id.~~ 1:27-31.- In the '898 patent, the paddle card is a printed circuit board (“PCB”) “used as part of a cable connector,” where “signal wires” in the cable are “soldered to terminals along one edge of the card.” *-Id.*, 1:35-39, 1:46-51.

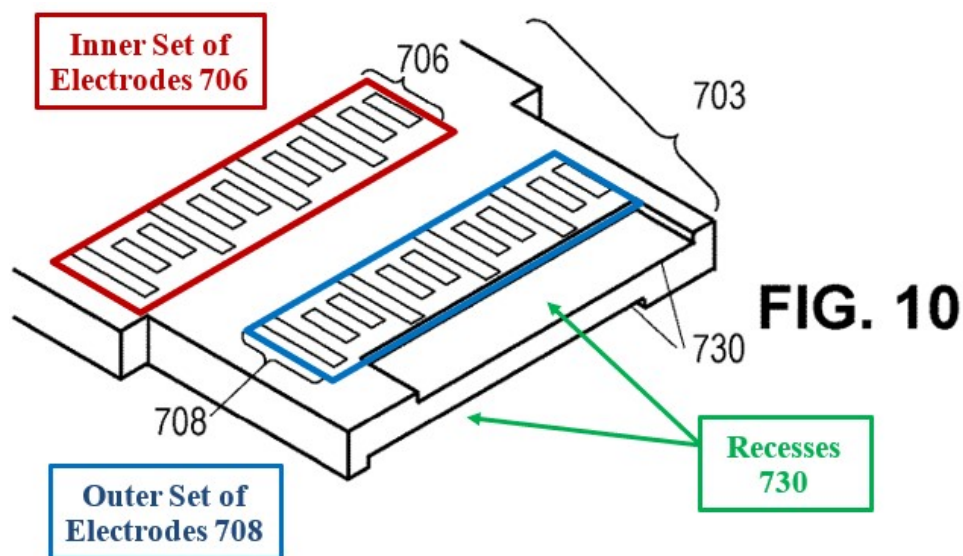
52. The '898 patent arranges solder terminals or “electrodes” on the PCB in two rows (an “inner set” and an “outer set”), where “the electrodes in the inner set” are “staggered relative to the electrodes in the outer set.” *-Id.*, 1:50-59, Fig. 10 (annotated below). ~~The~~As also shown in Figure 10, the paddle card ~~also~~ includes a “recess 730” that “extends along the path of the outer wire from the edge of the

²~~All Throughout this Declaration when I quote language from a reference all emphasis in the Petition is added unless otherwise indicated.~~

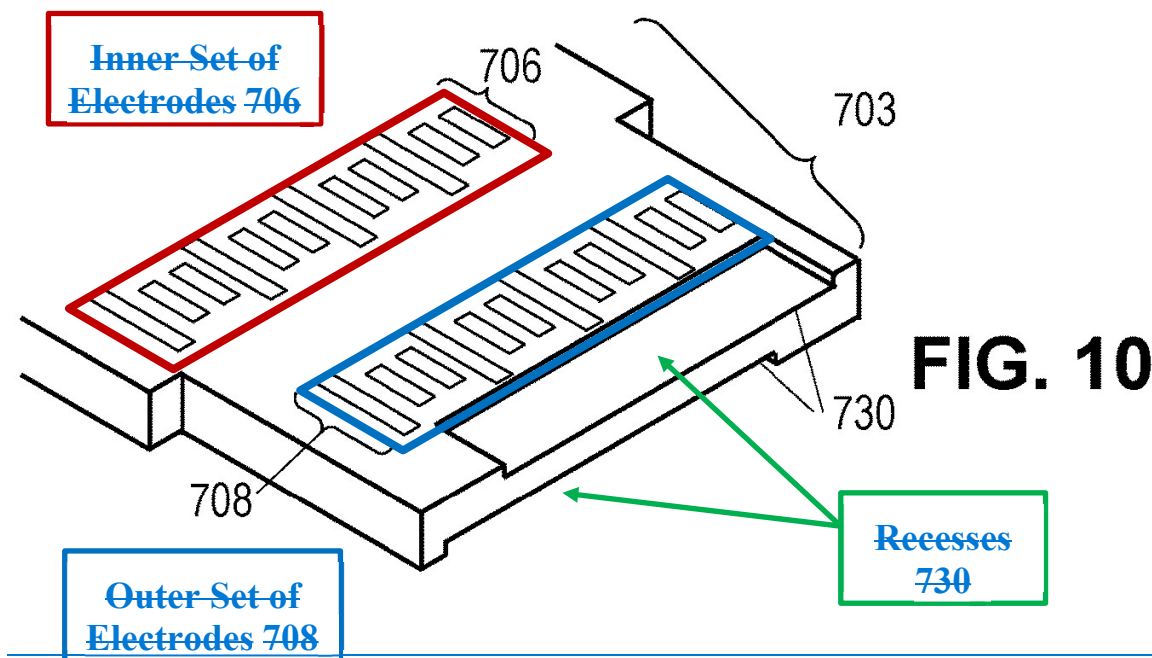
paddle card toward the outer electrode to accommodate the outer wire's sheath."

Id., 5:~~62-65~~, Fig. 10:~~62~~65. The recess allows the exposed end of the wire "to be attached to the outer electrode while remaining parallel to the" surface of the paddle card. *Id.*, 5:65-67 and "~~preferably has a~~ The recess thus "~~preferably has a depth at least equal~~" to the thickness of the sheath surrounding the signal wire's conductor. *Id.*, 6:1-2.

~~depth at least equal" to the thickness of the sheath surrounding the signal wire's conductor.~~



EX1001, Fig. 10 (annotated)~~*Id.*, 5:65-67, 6:1-2.~~



53. The '898 patent also describes the paddle card having an integrated circuit ("IC") ~~with~~ that "includes a powered transceiver that performs clock and data recovery (CDR) and ~~remodulation~~ re-modulation of data streams." *Id.*, 3:19-22, 4:11-18. -The IC is arranged on the paddle card to "couple[s]" together" the edge connector traces and the rows of electrodes "for receiving and redriving signals in each direction" ~~and~~ while optionally providing protocol and signal format conversion." *Id.*, 4:11-18.

~~*Id.*, 4:11-18.~~

~~A.~~ B. **Prosecution History of the '898 Patent**

54. The '898 patent issued without any substantive examination. The

Examiner's first action was a Notice of Allowance allowing all the claims without meaningful explanation. EX1002, 40, 44-45. Applicants then filed an RCE

(EX1002, 28) with an IDS listing 10 new references. ~~EX1002, 28-32.~~

~~The~~ Thereafter the Examiner issued another Notice of Allowance repeating the positions from the previous Notice of

~~Allowance's positions.~~ Allowance. EX1002, 8, 12-13.

C. The ~~B.~~ **Challenged Claims**

55. The '898 patent has 20 claims. Claims 1, 9, and 16 are independent. A ~~claim list is appended. *Supra* §0.~~

56. Claim 1 recites a "printed circuit board" ("PCB") ([1PRE]) having "edge connector traces" along a "first edge" that are "for contacting conductors in a socket connector" ([1A]), and an "inner" ([1C]) and "outer" ([1B]) set of electrodes "for attaching" exposed signal wire leads in a cable, wherein the sets are parallel to a "second edge" and "staggered" relative to each other ([1D]) .

57. Claim 9 recites a "cable" ([9PRE]) comprising "sheathed wires" terminated at each end by a "connector" ([9A]) that includes the PCB ([9B])

described in claim 1 ([9B1])-(9B4)). Claim 16 recites a “cable manufacturing method” ([16PRE]) comprising “*providing* first and second” PCBs ([16A]) described in claim 1 ([16A1])-(16A4)), “*soldering*” signal wires leads to electrodes on the PCB ([16B]), and “*packaging*” the PCBs in connectors that “fit into a socket.” ([16C]).

~~PCB ([16B]), and “*packaging*” the PCBs in connectors that “fit into a socket.” ([16C]).~~

Dependent claims add limitations on electrode spacing (claim 2), an integrated circuit (“IC”) on the PCB (claim 3), and a recess in the PCB that receives cable sheathing so as to dispose a signal wire lead parallel to and in contact with a PCB surface (claims 4-

58. 8). Dependent claims 10-15 and 17-20 largely repeat limitations from claims 2-7.

V. PRIOR ART REFERENCES

59. I briefly introduce in this Section, various prior art references discussed in this declaration.

A. Ayzenberg

~~C. POSA~~

~~A person of ordinary skill in the art (“POSA”) would have had a bachelor’s degree in computer or electrical engineering or a related scientific field and two years of experience with interconnects for high-speed communication. Souri, ¶¶40-49. A POSA would have had a working knowledge of signal integrity and how various PCB and cable designs affect it, as well as industry standards such as QSFP-DD (EX1010) governing cable assemblies and connections for high-speed communication. A POSA also would have understood the technology surrounding mounting a cable to another structure, such as a PCB. Souri, ¶¶40-49. (EX1005)~~

60. Ayzenberg is titled “High Performance Cable Termination.”

Ayzenberg is directed to “[a] cable assembly comprising a connector with a termination that enables high density and high signal integrity” and “[s]hields of cables are terminated to a paddle card via a conductive structure attached to a surface of the paddle card.” Ayzenberg, Abstract.

Ayzenberg (EX1005) was issued as U.S. Patent ~~More education could substitute for experience, and vice versa. *Id.*~~

~~V. CLAIM INTERPRETATION~~

~~The Board construes claim terms using ordinary meaning in light of the specification and prosecution history. 37 C.F.R. §42.100(b). The Board need only construe terms to the extent needed to resolve disputes. *Nidec Motor v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 83 Fed. Reg. 51340, 51353.~~

61. No. 11,228,123 claim term requires that the Board reach

(EX1014, “Ayzenberg-123”). According to the face of the document, Ayzenberg (EX1005) is a United States patent application published on June 18, 2020 as Publication No. 2020/0194911 from an exact outer boundary construction because the application filed on December 16, 2019 as Application No. 16/716,176. That application claimed priority to a provisional application filed on December 17, 2018 as Provisional Application No. 62/780,504 (EX1015). I have been informed by counsel that Ayzenberg is entitled to the December 17, 2018 filing date of its provisional application. I have been informed by counsel that Ayzenberg qualifies as prior art ~~meets~~to the ’898 patent based on Ayzenberg’s filing date. See also *infra* §VI.A.1 (additional discussion of Ayzenberg).

62. I have also compared the provisional application of Ayzenberg (EX1015) to the ~~claims under~~U.S. publication of Ayzenberg (EX1005). I have observed that the provisional application describes the same subject matter as Ayzenberg. EX1019 (redline comparison showing changes in the text of the Ayzenberg (EX1005) specification compared to its provisional (EX1015)). In particular, EX019 provides a redline comparison of the published application EX1005 to the provisional application EX1015. In EX1019, the provisional application EX1015 is the reference for the comparison, so that any ~~reasonable interpretation. changes in~~ the published application EX1005 text from the provisional EX1015 text are shown

in conventional redline formatting with a line-out denoting a deletion and underline denoting addition. For example, as EX1019 makes clear, the published application adds a paragraph [0001] concerning cross-references to related applications and the published application thus increments the remaining paragraph numbering by one from the paragraph numbering in the provisional application EX1015.

B. Alden (EX1006)

63.Alden is titled “Circuit Board and Wire Assembly.” Alden is directed to “[a]n electrical connector includ[ing] a circuit board having an internal ground plane that defines at least a portion of an internal layer of the circuit board” and “bodies [] engaged with the internal ground plane of the circuit board to electrically connect the ground shields to the internal ground plane.”

Alden,

Abstract.

64.According to the face of the document, Alden (EX1006) is a United States patent application published on October 24, 2013 as Publication No. 2013/0280955 from an application filed on April 24, 2012 as Application No. 13/454,556. I have been informed by counsel that Alden qualifies as prior art to the '898 patent based on Alden's publication date. See also *infra* §VI.D.1 (additional discussion of Alden).

C. VI. ~~GROUND 1: AYZENBERG ANTICIPATES AND/OR~~
~~RENDERS OBVIOUS CLAIMS 1-2, 9-10, 16, AND 18~~

~~A.~~ ~~Ayzenberg~~ Lugthart (EX1007)

65. Lugthart is titled “High Speed Transceiver.” Lugthart is directed to “[s]ystems and methods for high speed communications” that “include innovative transceiver architectures and techniques for re-timing, multiplexing, demultiplexing and transmitting data.” Lugthart, Abstract.

66. According to the face of the document, Lugthart (EX1007) is a United States patent issued on January 30, 2018 as Patent No. 9,882,706 from an application filed on December 28, 2016 as Application No. 15/392,244. I have been informed by counsel that Lugthart qualifies as prior art to the ’898 patent based on Lugthart’s issuance date. See also infra §VI.B.1 (additional discussion of Lugthart).

D. Janssen (EX1009)

67. Janssen is titled “Contact Connecting of Shielded Data Lines to a Board and Method for Contacting a Number of Shielded Data Lines with a Board.” Janssen is directed to “a contact connecting of preferably a number of shielded conductor pairs to a board in particular of a plug for high-speed data connections.” Janssen, Abstract.

68. According to the face of the document, Janssen (EX1009) is a United States patent issued on February 6, 2018 as Patent No. 9,887,496 from

an application filed on June 13, 2016 as Application No. 15/180,244. I have been informed by counsel that Janssen qualifies as prior art to the '898 patent based on

Janssen's issuance date. See also *infra* §VI.C.1 (additional discussion of Janssen).

E. QSFP-DD Specification (EX1010)

69. The '898 patent describes paddle cards designed to operate according to a standard such as the “quad small form-factor pluggable double density” (“QSFP-DD”) specification. EX1001, 1:7-22. Version 5.0 of this specification (EX1010) was in effect when the '898 patent was first filed, as indicated by the QSFP-DD organization's website (see <http://www.qsfp-dd.com/specification/>). See also EX1010, 1 (indicating a publication date of July, 9, 2019). It is my opinion that a POSA would have been aware of and utilized this specification in designing compliant electrical connectors using the teachings in the prior art.

70. The QSFP-DD specification defines “a high density 8-channel (8x) module, cage and connector system” including “[d]imensions, mounting and insertion requirements” so that the “cable plug, cage and connector system on a circuit board” are “mechanically interchangeable.” *Id.*, 7-8, Fig. 9 (“2x1 stacked cage and module”). Although Figure 9 shows a “2x1 stacked” cage and module, it was understood that this is merely exemplary, and it was well-known and conventional to provide a single cage (such as shown in QSFP-DD Figure 10

below) receiving a single module (such as shown in QSFP-DD Figure 11 below).

The cage and module are designed so that when the module is plugged into the cage the mating connections on a paddle card (enclosed by the pluggable module) are disposed in electrical contact with corresponding or matched connections within the cage.

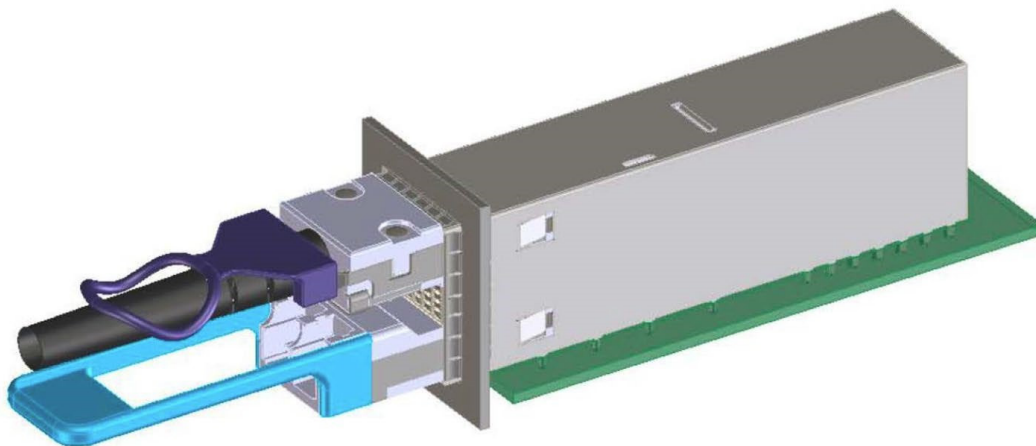


Figure 9: 2x1 stacked cage and module

71. The pluggable module includes “a single paddle card” and is designed to “mate to the connectors and cages defined in [the] specification.” *Id.*, 9, 28, Fig. 11 (below).

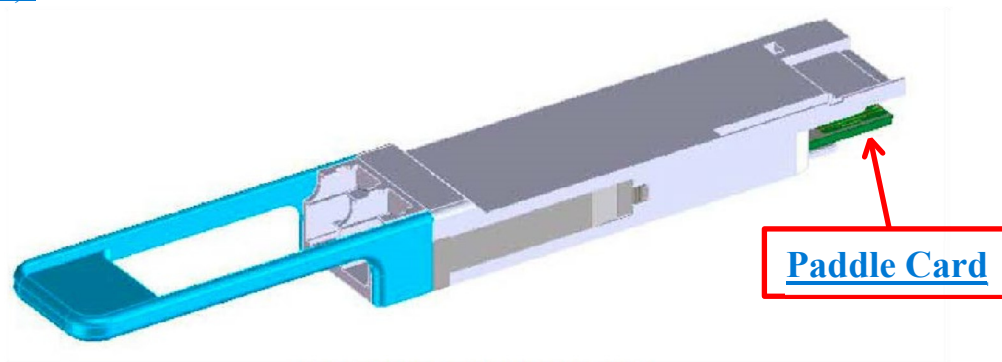


Figure 11: Type 1 Pluggable module

The cage and connector are a *socket* that receives the “pluggable module.” *Id.*, 2829, 32, Fig. 10 (below).

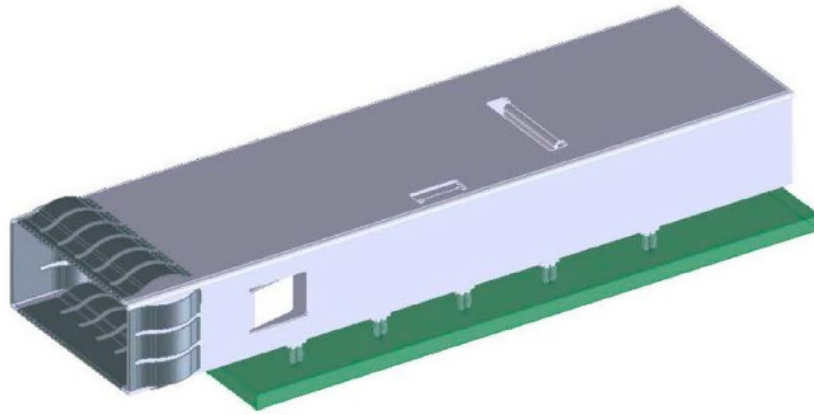


Figure 10: Press fit cage for surface mount (SMT) connector

As noted above the cage encloses a connector that mates with contacts on the paddle card in the pluggable module. For example, QSFP-DD Figure 30 (below) shows a cutaway of a cage exposing the mating connector—in this example called a “SMT connector”—within it.

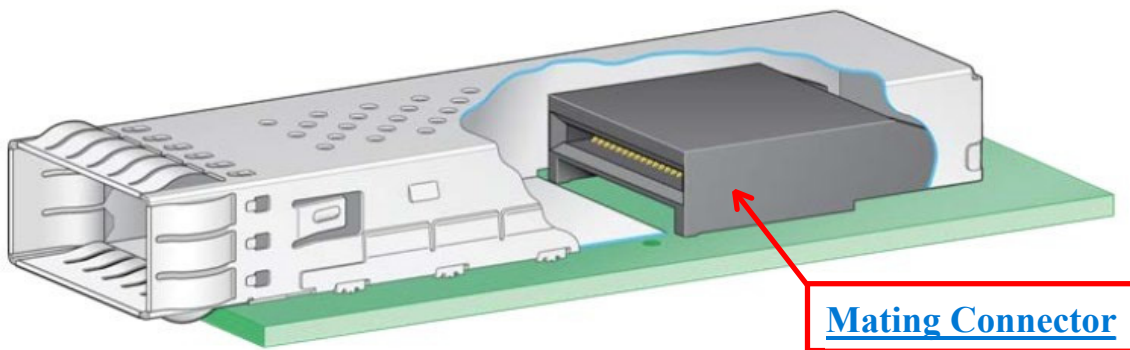


Figure 30: SMT connector in 1xn cage

72. It is my opinion that POSAs would have recognized that the paddle cards described in the '898 patent and the prior art, when applied to the QSFP-DD

specification, would have been included in a “pluggable module” designed to mate with the connector inside a corresponding “cage.”

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE IN LIGHT OF THE PRIOR ART

73. I have been asked to provide my opinion concerning whether claims 1-20 of the '898 patent are anticipated or would have been obvious to a POSA in light of the prior art references discussed below. For the reasons explained below, it is my opinion that each of claims 1-20 is anticipated and/or would have been obvious to a POSA. The following table summarizes the Grounds I discuss in the sections below (independent claims have been indicated in **bold** in the table below). I use “+” as a shorthand for “in view of,” so that, *e.g.*, by “Ayzenberg+Lugthart” I mean the combination of Ayzenberg in view of Lugthart as explained in the grounds below.

<u>Ground</u>	<u>Reference(s)</u>	<u>Claims</u>	<u>Basis</u>
<u>1</u>	<u>Ayzenberg (EX1005)</u>	<u>1-2, 9-10, 16, 18</u>	<u>Anticipates and/or Obvious</u>
<u>2</u>	<u>Ayzenberg+Lugthart (EX1007)</u>	<u>3, 11, 17</u>	<u>Obvious</u>
<u>3</u>	<u>Ayzenberg+Janssen (EX1009)</u>	<u>4-8, 12-15, 19-20</u>	<u>Obvious</u>
<u>4</u>	<u>Alden (EX1006)</u>	<u>1-2, 9-10, 16, 18</u>	<u>Anticipates and/or Obvious</u>
<u>5</u>	<u>Lugthart+Alden</u>	<u>3, 11, 17</u>	<u>Obvious</u>
<u>6</u>	<u>Janssen+Alden</u>	<u>4-8, 12-15, 19-20</u>	<u>Obvious</u>

**A. Ground 1: Ayzenberg Anticipates and/or Renders Obvious Claims
1-2, 9-10, 16, and 18**

74. As explained in this section below, in my opinion claims 1-2, 9-10, 16, and 18 of the '898 patent would have been anticipated and/or rendered obvious over Ayzenberg (EX1005).

1. Discussion of Ayzenberg (EX1005)

75.

Amphenol's patent application Ayzenberg (~~EX1005~~) concerns high performance cable terminations. EX1005, code (54), (73). Ayzenberg discloses a "cable assembly" comprising a paddle card where "signal conductors of the cables are terminated to pads" located on each surface of the paddle card. EX1005, Abstract, [0058]. The paddle card can be designed "having a width and/or other aspects/dimensions as defined in the~~....~~ QSFP-DD standards." *Id.*, [0044]; ~~Souri,~~ ~~¶supra~~^{75.}

~~contact pads 406~~
~~rows 420A, 420B~~

**solder pads 410:
inner row 422B**

**solder pads 410:
outer row 422A**

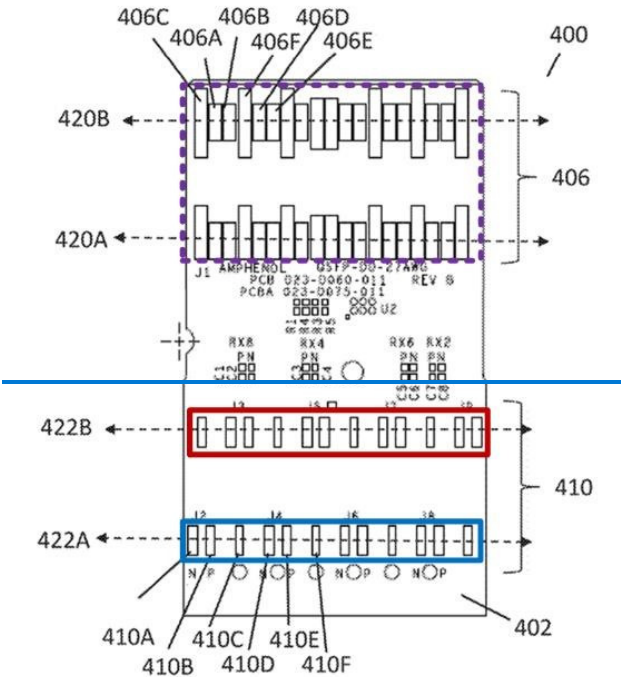


FIG. 4A

[§V.E; EX1010 \(defining the QSFP-DD standard\).](#)

**contact pads 406
rows 420A, 420B**

**solder pads 410:
inner row 422B**

**solder pads 410:
outer row 422A**

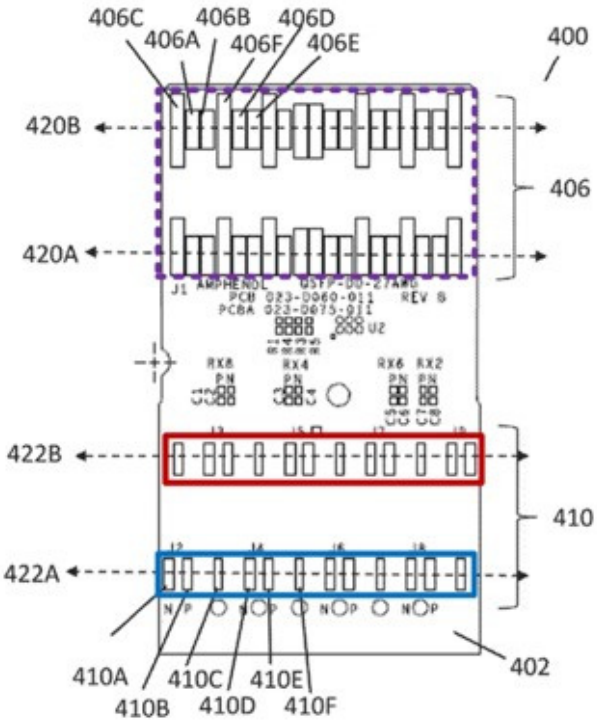


FIG. 4A

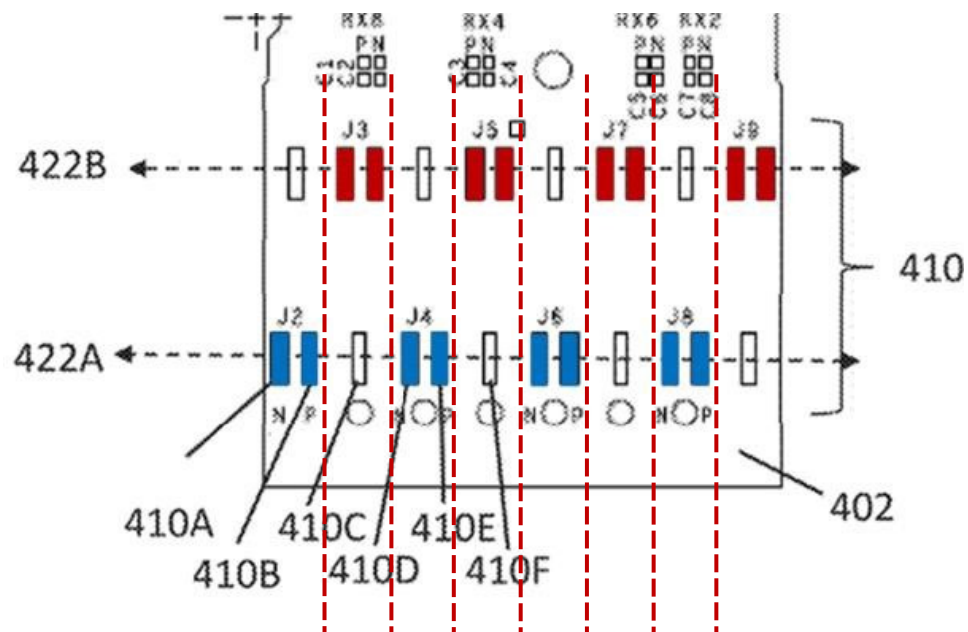
Each surface of Ayzenberg's paddle card includes "contact pads" and "solder pads." *Id.*, [0059], Fig. 4A (top surface, annotated above), Fig. 4B (bottom surface with contact pads 408 in rows 424A/~~424B~~, B and solder pads 412 in rows

76. ~~426A/426B~~, B). The contact pads are "in electrical communication with the solder pads" to "facilitate connection of the signals" from the cable "to corresponding contacts of a mating connector." *Id.*, [0062]-[0063]. ~~The~~One such mating connector is a "receptacle connector" that is "mounted on a printed circuit board (PCB) in an electronic device." *Id.*, [0077].

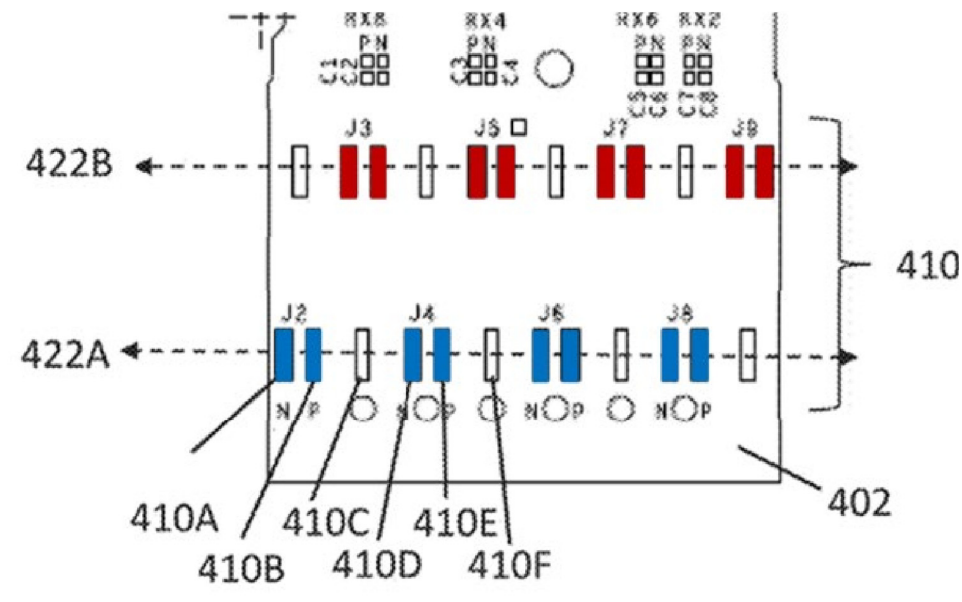
~~"receptacle connector... mounted~~Focusing on a ~~[PCB]~~ in an electronic device."the top ~~*Id.*, [0077].~~

77. ~~The~~ surface of first side 402 in ~~Figure~~Fig. 4A ~~shows that, the~~ solder pads "are arranged along two rows shown by dotted arrows 422A and 422B." *Id.*, [0060]. Each row includes signal solder pad pairs (e.g., pads 410A/410B, 410D/410E) "to electrically and physically connect to the n and p signal wires" of a

cable with multiple wires. *Id.*, [0060], [0047], Fig. 4A (pairs J2-[to](#) J9), Figs. 9A, 9B.³



³ The remaining solder pads in rows 422A/422B (e.g., 410C, 410F, unshaded in annotated Fig. 4A) are ground connections. E.g., EX1005, [0060].



Ayzenberg, Fig. 4A (excerpted, annotated)

The dashed red lines As shown in annotated Figure 4A (above) show that

Ayzenberg staggers the signal solder pad pairs (e.g., J2 to J9) in each solder pad row (e.g.,

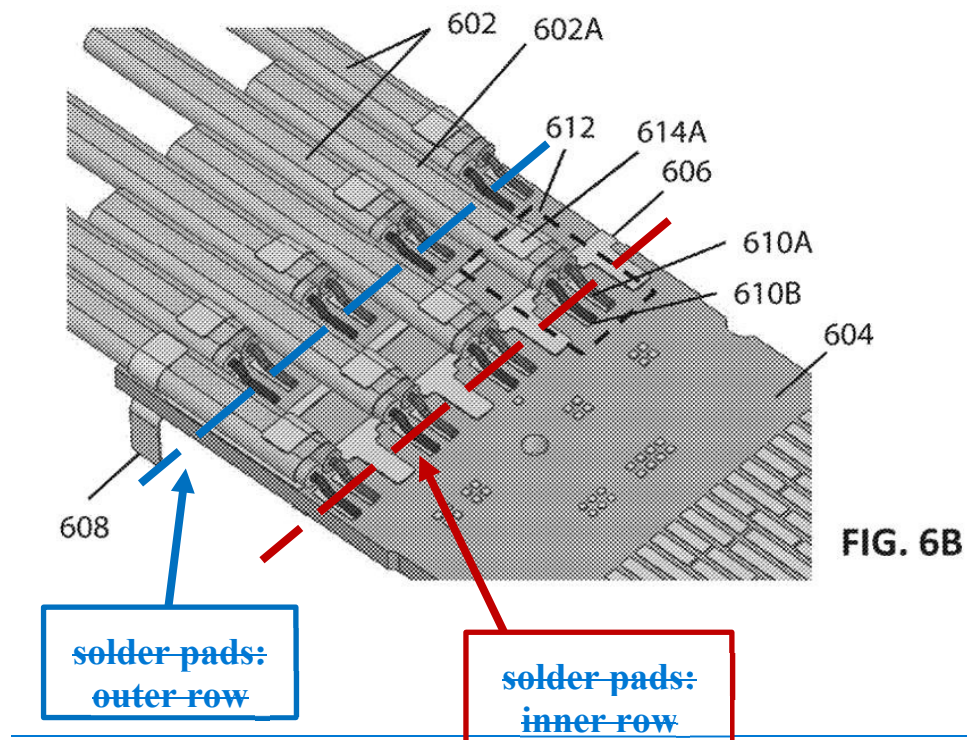
78. 422B, 422A).

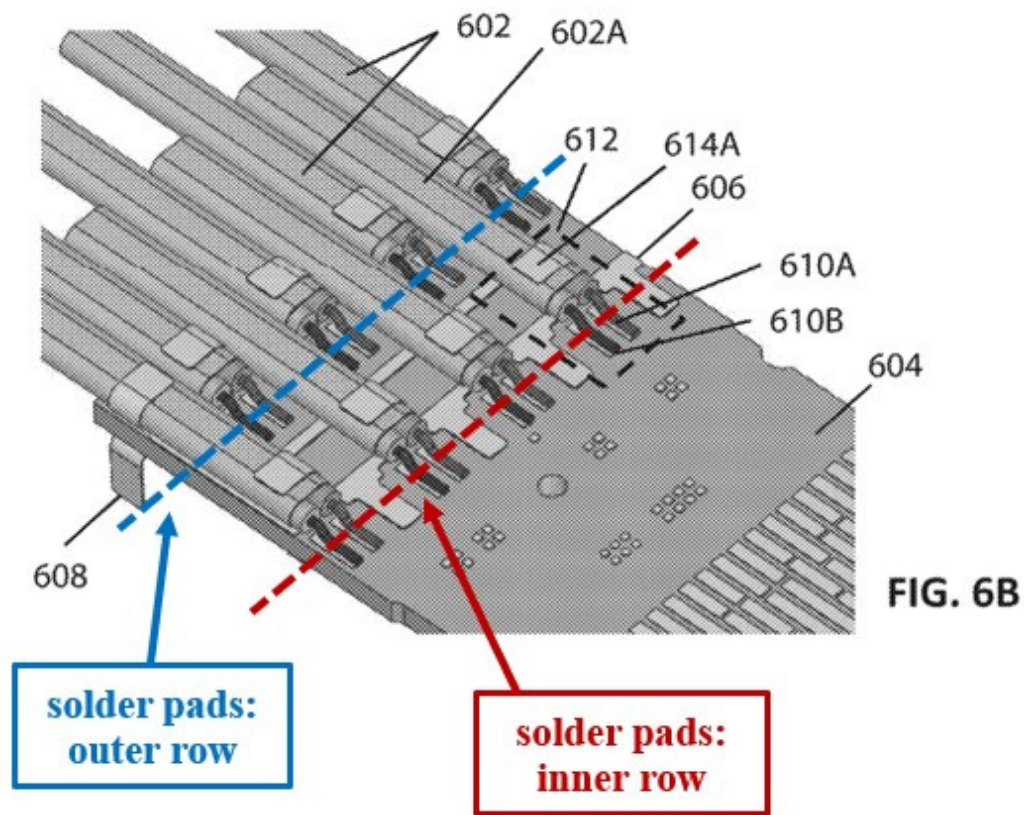
Id., [0060]-], Figs. 4A (above, annotated), 4B.

Ayzenberg Figure 6B rotates and angles the orientation is an isometric view of thea cable assembly which includes a paddle card (such as that depicted in

Figure 4A), and shows cables 602 with signal wire leads (e.g., 610A), 610B)

79. soldered to signal solder pads (partly visible beneath wire leads in Figure 6B). *Id.*, [0073], Fig. 6B. Figure 6B shows that staggering the solder pad placement in each row permits wires connected to the inner row of pads (on red dashed line below) to pass between the wires connected to the outer row of pads (on blue dashed line below).





Ayzenberg, [Fig. 6B \(annotated\)](#)

80. [Ayzenberg](#) states that [while active components are “not shown,”](#)

“active components can be attached to the paddle card... in the space between the row 420A... and the row 422B of contact pads [in FIG 4A.](#)” *Id.*, [0065], [Fig. 4A.](#)].

Exemplary active components include “[filters, amplifiers,](#) transceivers, and/or the like” [that.](#)” *Id.* [Such active components on the paddle card 400 can](#) “convert between different communication protocols... such that a different protocol is provided to a mating connector.” *Id.*

B. Analysis

2. Mapping of Ayzenberg ~~anticipates and/or renders obvious~~to claims 1-2, 9-10, 16, and 18. ~~“It is well settled that a disclosure that anticipates under §102 also renders the claim invalid under §103, for anticipation is the epitome of obviousness.”~~ *Realtime*

Data v. Iancu, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (cleaned up).

_____ 1 _____ a. Claim 1

_____ ai. Preamble [1PRE]

[1PRE]: A [PCB] that comprises at least one surface having:

81. Ayzenberg meets [1PRE] because it teaches a “*printed circuit board*” (PCB) in the form of a “paddle card.” EX1005, [0039] (“PCB may be a paddle card of a connector[.]”), [0058]-[0059]; *cf.* EX1001, 1:21-22 (describing connector PCB as a paddle card); ~~Souri, ¶81.~~ The paddle card has a “*surface*” on each side. EX1005, [0058]-[0059], Figs. 4A (side 402), Fig. 4B (side 404); ~~Souri, ¶81.~~ For simplicity, ~~this~~my analysis focuses on side 402 (“*at least one surface*”). As I will discuss below, it is my opinion that Ayzenberg meets all the limitations of claim 1.

ii.

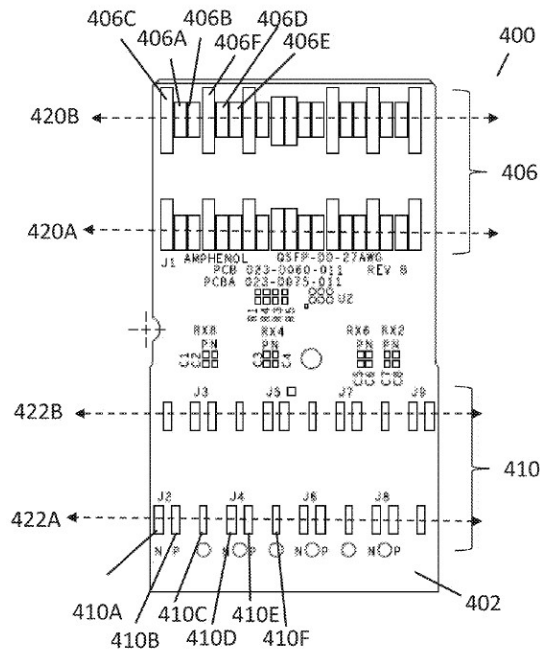


FIG. 4A

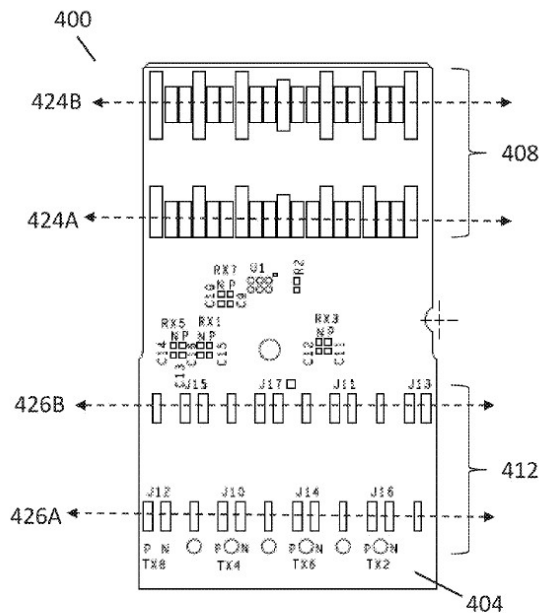


FIG. 4B

b. Limitation [1A]

[1A]: edge connector traces arranged along a first edge for contacting electrical conductors in a socket connector;

i. (1) “edge connector traces arranged along a first edge”

82. Ayzenberg meets [1A] because its paddle card includes “contact pads 406” (i.e., “edge connector traces”) ~~arranged along the card’s edge (i.e., “first edge”)~~ that “are in electrical communication with the solder pads 410... through the interior of the paddle card.” -EX1005, [0062], Fig.. Figure 4A (annotated below);

406
(i.e.,

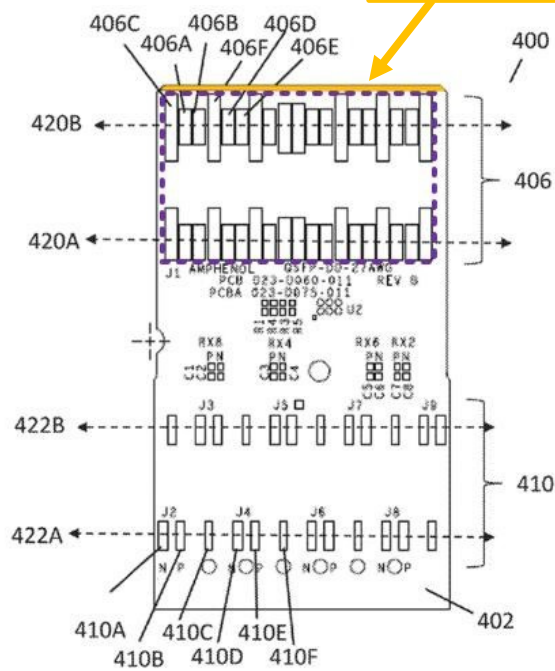


FIG. 4A

Souri, ¶82, shows contact pads arranged along the card's edge "first edge").

contact pads 406
"edge connector traces"

the claim because such statements usually do no more than define a context in which the invention operates.”).

84. Regardless, it is my opinion that Ayzenberg’s contact pads 406 ~~meet~~meets the language “for contacting…” language. Souri, ¶84. electrical conductors in a socket connector”. The ’898 patent does not define “*socket connector*” but describes “packaging” PCBs in “connectors adapted to fit standard-compliant *socket*” (EX1001, 6:48-52) and having “corresponding electrical conductors” that electrically couple to edge connector traces on a PCB when a connector enclosing a PCB is “seated within an edge connector socket.” *Id.*, 4:19-26; ~~Souri, ¶84. The. It is my opinion that the~~ plain meaning confirms this usage. POSAs knew that in QSFP-DD, the mating cage (i.e., “*socket*”) that receives the pluggable module comprises a connector inside the cage providing the functionality described in the ’898 specification, which POSAs would have understood was a “*socket connector*” as claimed. E.g., EX1010, 53 (surface mount “QSFP-DD Connector is a 76-contact, right angle connector”), Fig. ~~30; Souri, ¶¶69-72, 84.~~

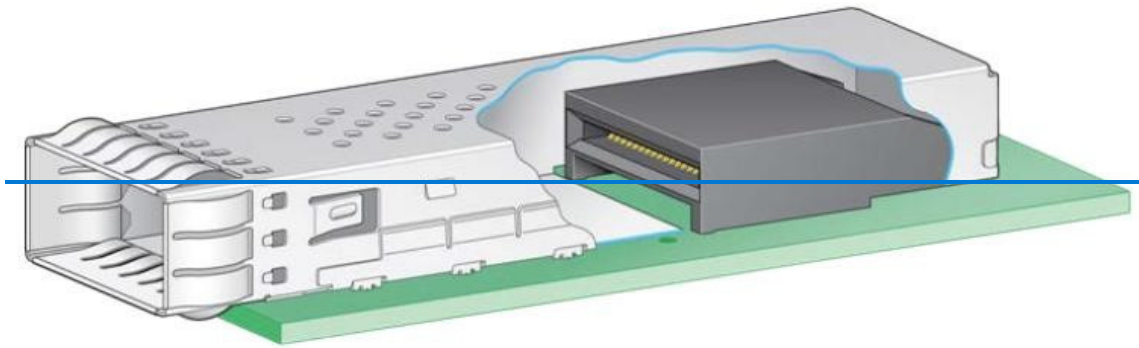


Figure 30: SMT connector in 1xn cage

[30; supra §V.E.](#)

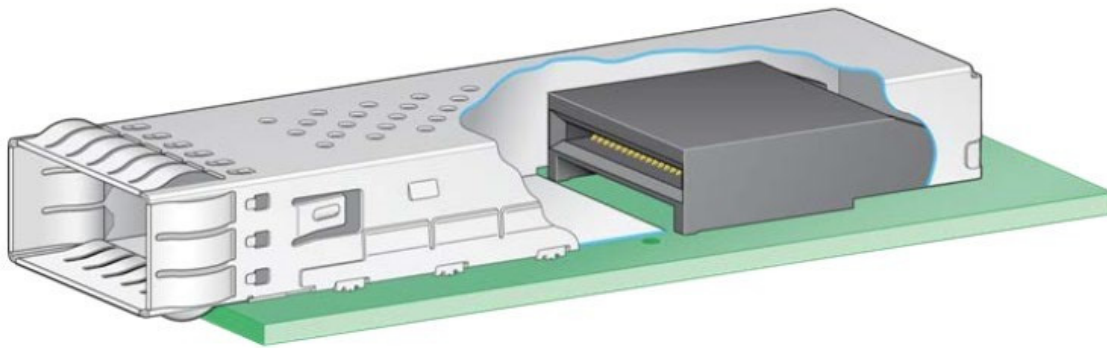


Figure 30: SMT connector in 1xn cage

Ayzenberg describes contact pads 406 [as](#) located “at the mating interface” [to](#)

[85. .” EX1005, \[0058\]. Contact pads 406](#) “facilitate connection of the signals from the associated cable to corresponding contacts of a mating connector.”

[EX1005, \[0058\], *Id.*, \[0063\], \[0077\]](#) (“[. “The plug of cable assembly 700 may mate with *a receptacle connector*\[-.\]”](#)” [Id., \[0077\]](#) (emphasis added). POSAs would have understood that Ayzenberg’s “mating-[connector](#)” / “receptacle connector” interchangeably refer to a “*socket connector*” because it receives Ayzenberg’s PCB and comprises

contacts that electrically connect to contact pads 406 and pass electrical signals, as described in the '898 patent. ~~Souri, ¶85; see EX1005; See id.~~, [0063], [0076]; EX1001, 4:19-26. This usage was consistent with the QSFP-DD connector standards cited in Ayzenberg and the '898 patent. EX1005, Abstract, [0044]-[0045], [0057];]; EX1001, 1:16-20; ~~Souri, ¶85.~~

86. The QSFP-DD gives examples of a “cage” with a connector (e.g., *socket*) for receiving a “pluggable module” (e.g., the connector enclosing the paddle card ~~terminating~~that terminates the signal wires). Supra §V.E; see e.g., EX1010, ~~28-29~~2829, 32, Fig. 9 (“2x1 stacked cage and module”), Fig. 11 (showing a QSFP-DD “pluggable module”), Fig. 10 (cage_ for receiving pluggable module); *cf.* EX1005, [0075], Fig. 7 (exploded cable assembly (e.g., connector) 700 enclosing paddle card 708); ~~Souri, ¶¶69-72, 86.~~

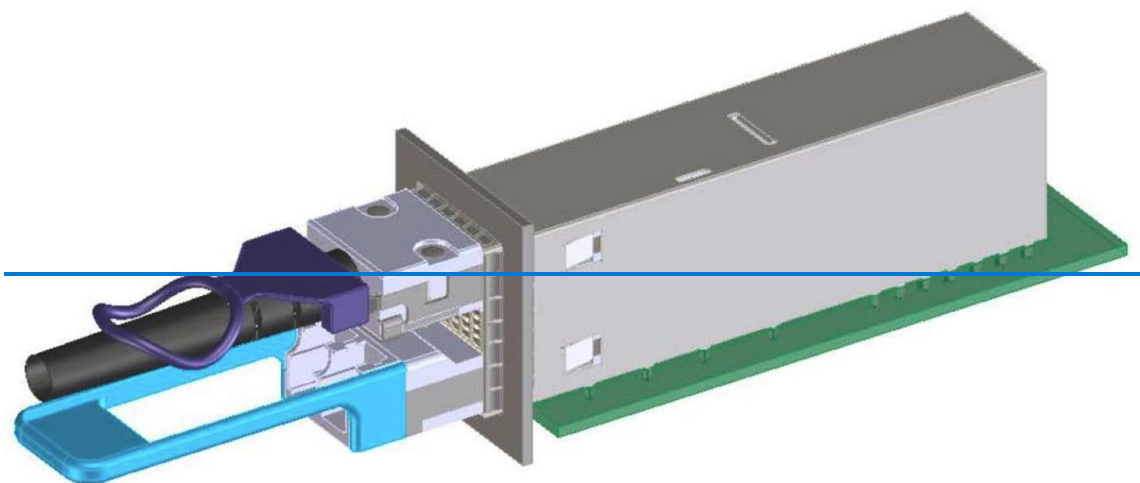


Figure 9: 2x1 stacked cage and module

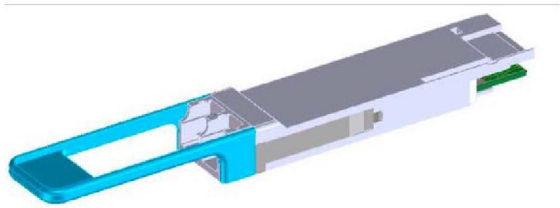


Figure 11: Type 1 Pluggable module

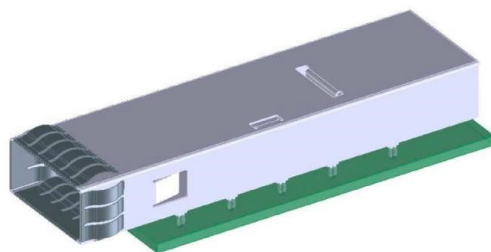


Figure 10: Press fit cage for surface mount (SMT) connector

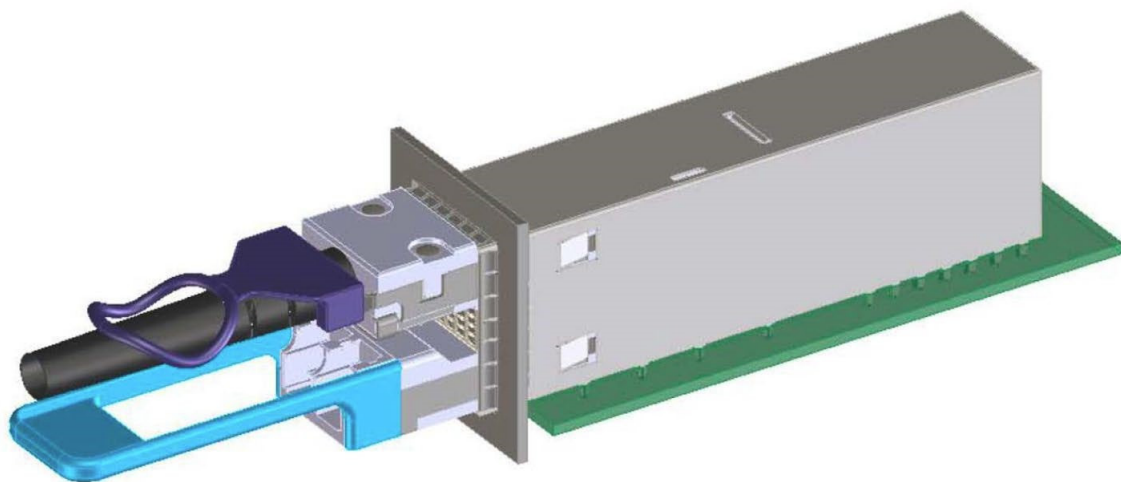


Figure 9: 2x1 stacked cage and module

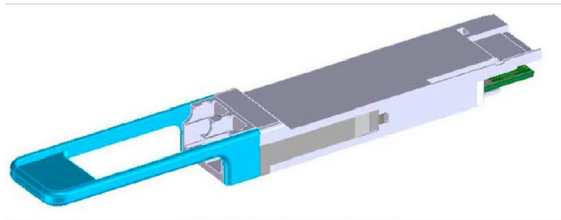


Figure 11: Type 1 Pluggable module

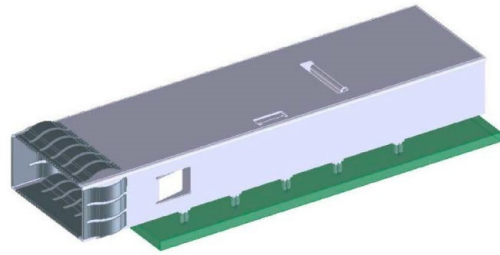


Figure 10: Press fit cage for surface mount (SMT) connector

87. POSAs would have recognized that Ayzenberg’s “receptacle” is a connector of a “*socket*” that Ayzenberg’s plug housing and paddle card are designed to “*fit into*” and, by mating with contact portions in the socket’s connector, “to connect any suitable electronic device to any other suitable device.”

~~EX1005, [0077]; See,~~

~~EX1005, [0077]; See, e.g., EX1001, 1:23-31 (describing paddle cards generally); Souri, ¶¶69-72, 87.).~~

88. Like the ’898 ~~patent~~^{spatent} paddle cards, Ayzenberg’s paddle cards are designed for housing in QSFP-DD standard connectors. *Compare* EX1005, [0044]-[0045] with EX1001, 1:16-22; ~~Souri, ¶88.~~ POSAs would have recognized Ayzenberg’s paddle cards—like the edge connector traces on paddle cards described in the ’898 patent—were designed for contact pads 406 to mate with a connector in a corresponding *socket*. ~~Souri, ¶88.~~

89. ———eThus, it is my opinion that Ayzenberg meets Limitation [1A].

iii. **Limitation [1B]**

[HB]: an outer set of electrodes arranged parallel to a second edge for attaching exposed ends of sheathed wires in a cable (“outer wires”);

i. (1) Terms

(~~4~~1) “outer set”

90. The specification describes “outer set of electrodes 308” as disposed closer to a PCB edge than “inner set of electrodes 306.” EX1001, Fig. 3, 4:51-59 (“The terms ‘inner’ and ‘outer’ are used solely to indicate the electrode position relative to the edge of the paddle card”); Souri, ¶90.—”).

(2ii) “*cable*” / “*sheathed wires*”

91. A “*cable*” is “[a] group or bundle of conductors, fibers, or wires, or bound together, sharing a common protective sheath or jacket[.]” EX1012, 77; Souri, ¶91. An “outer jacket (usually metal or plastic) surrounding copper... cables” is a “*sheath*.”

~~“sheath.”~~ EX1011, 1134; ~~Souri, ¶91.~~

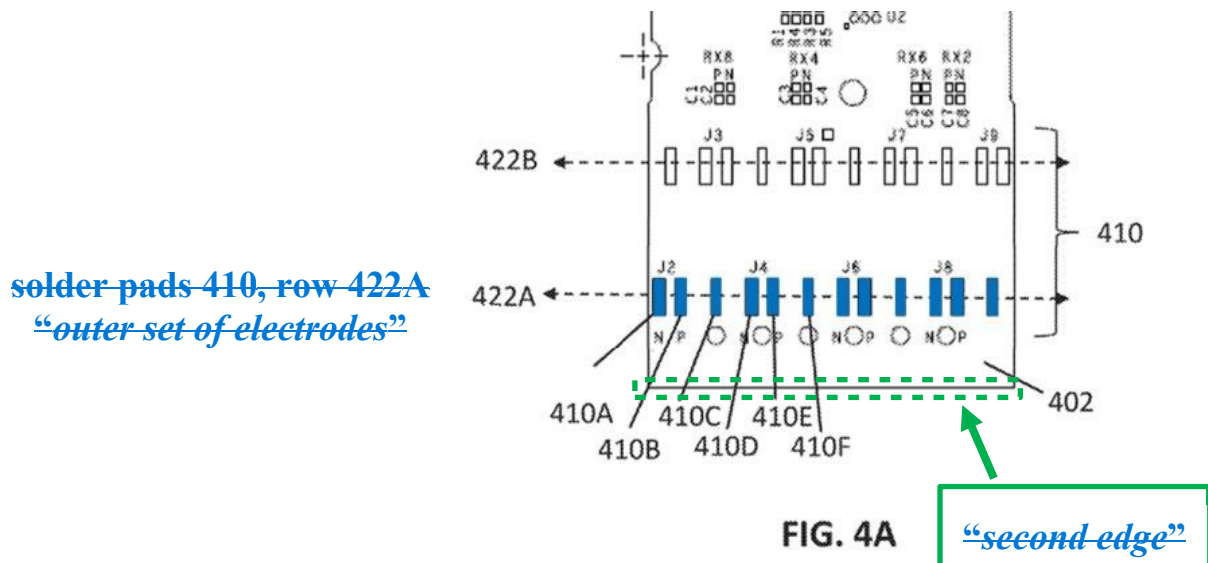
(3iii) “for attaching...”

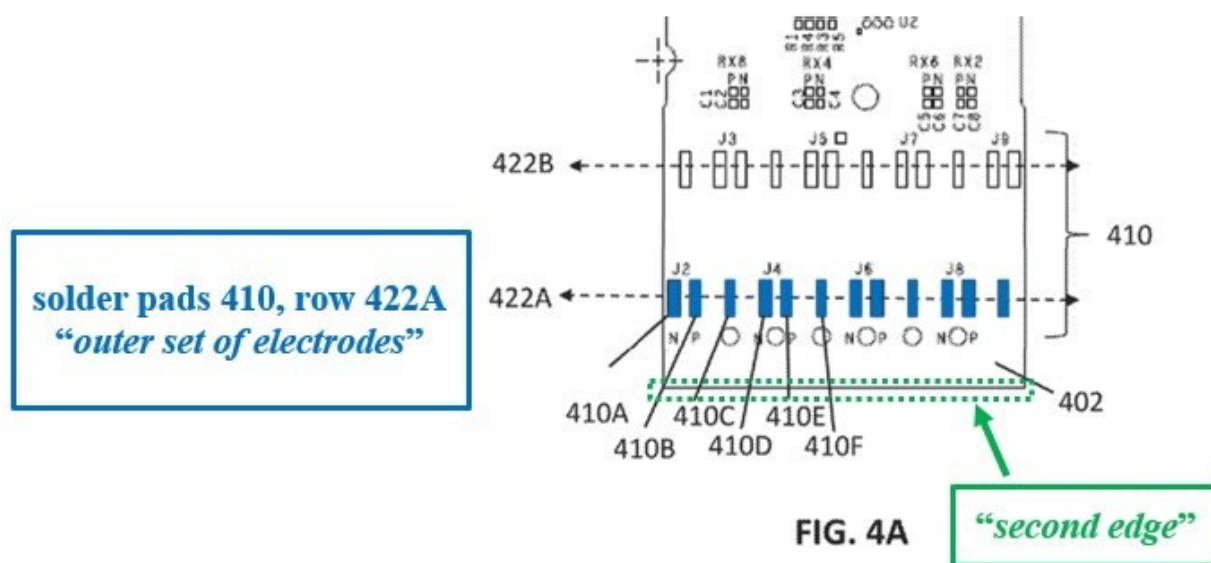
92. Like I have been informed by counsel that, like “for contacting...” in [1A], the “for attaching...” language in [1B] is a ~~nonlimiting~~non-limiting statement of intended use. Supra §VI.B.1.b.ii; Boehringer, 320 F.3d at 1345. Regardless, if

it is construed as limiting, then it is my opinion that Ayzenberg meets “for attaching...”it as shown below. Souri, ¶92.

ii. (2) Analysis

93. Ayzenberg meets [1B] because solder pads 410 in row 422A are “*an outer set of electrodes arranged parallel to a second edge*” of the paddle card. as shown in annotated Fig. 4A below. EX1005, [0060], Fig. 4A (annotated below); Souri, ¶93. 4A.

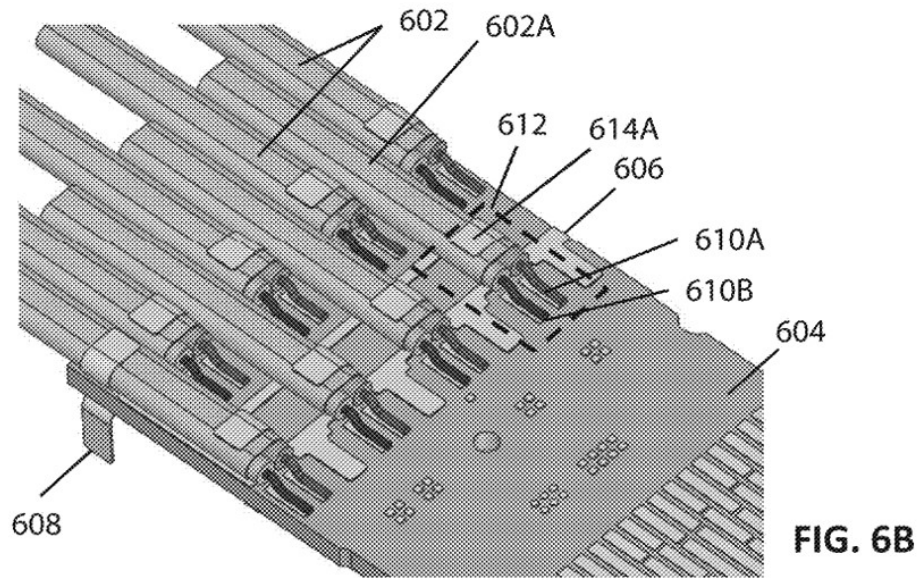




Ayzenberg, Fig. 4A (excerpted, annotated)

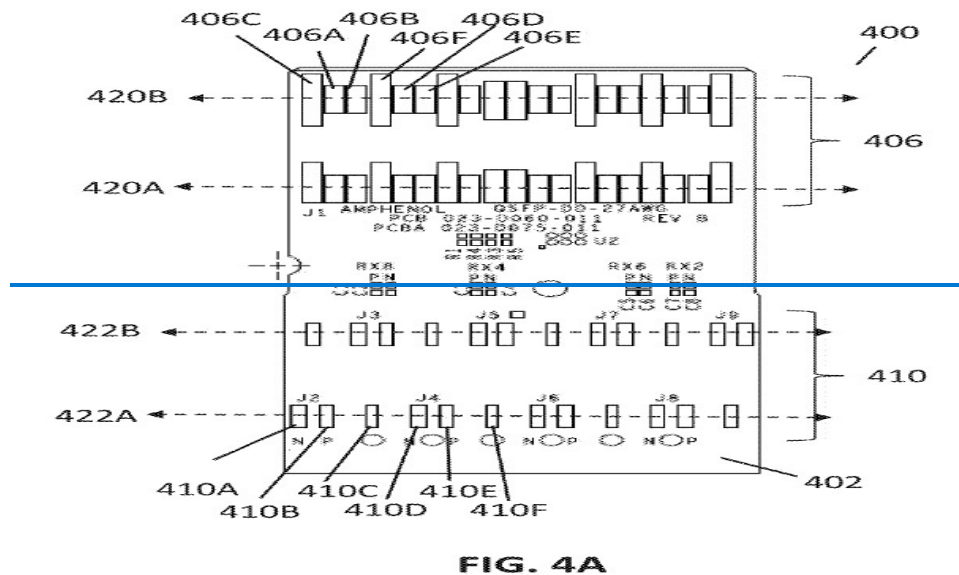
94. In Ayzenberg, solder pads 410 are used *"for attaching exposed ends of sheathed wires in a cable,"* as solder pads 410 "are used to electrically and physically connect to the pair of signal wires... of an associated transmit *cable*."

EX1005, [0060], [0069], Fig. (emphasis added), [0069], Fig. 6B (showing signal wires 610A and 610B connected to solder pads).



Ayzenberg, Fig. 6B (showing

95. The signal wires 610A/610B connected to solder pads); Souri, ¶94.



The cable's signal wires in the transmit cable soldered to each solder pad are

“*exposed ends of sheathed wires*” because Ayzenberg discloses using “[a] known

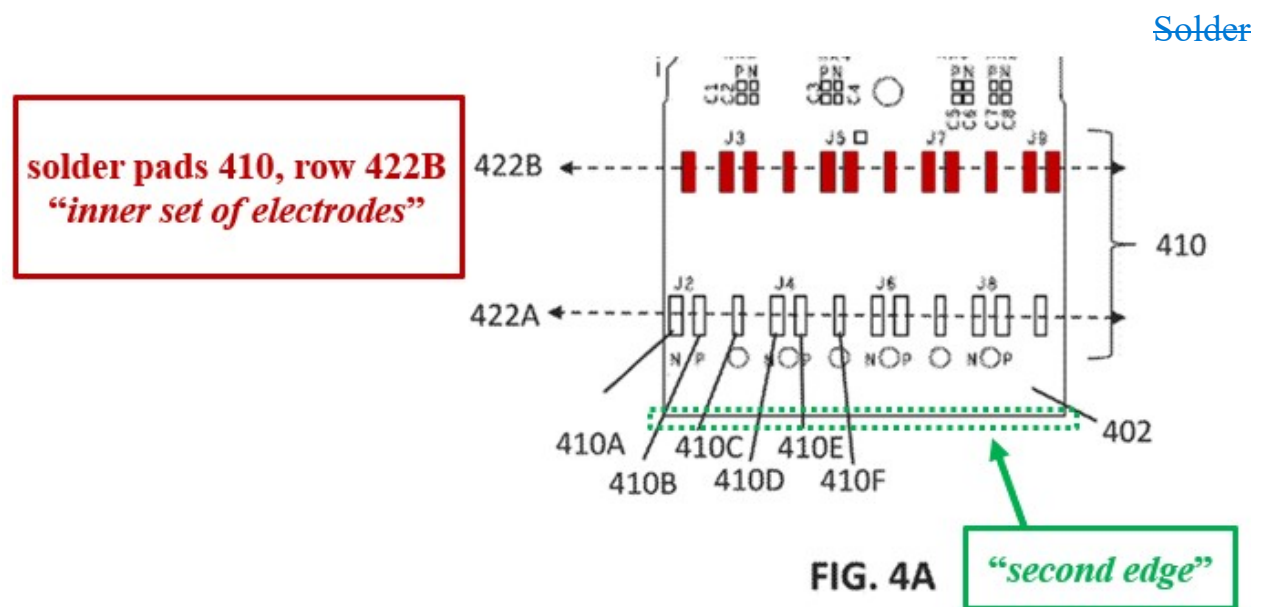
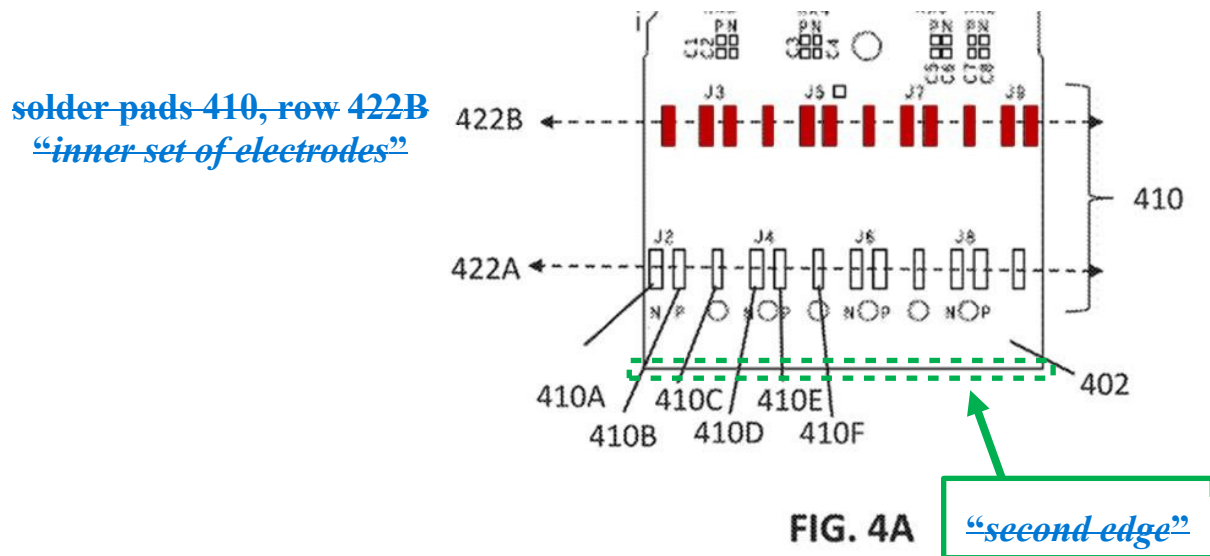
technique for terminating a cable” by “strip[ping] away” ~~components~~, at the end of the cable

, components of the cable (e.g., “dielectric material 906A, 906B, conductive foil 908 and outer coating”) ~~“to expose the signal conductors.”~~ EX1005, [0049], [0091], [0069] (“~~[T]he~~In order to connect cables to the paddle card (e.g., at the solder pads), the layers of the cable... (e.g., the conductive layer and the dielectric coatings on the signal wires) are removed so that the signal wire terminations can be connected (e.g., soldered) to the paddle card.”); ~~Souri, ¶95.~~ The wires having exposed ends attached to solder pads 410 in row 422A are thus ~~“(outer wires)”~~ meeting [1B]. ~~Souri, ¶95.~~ 96. Thus, it is my opinion that Ayzenberg meets
Limitation [1B].

~~div.~~ **Limitation [1C]**

~~[1C]~~: and an inner set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed wires in a cable (“inner wires”), ”

97. Ayzenberg meets [1C] because solder pads 410 in row 422B are “an inner set of electrodes arranged parallel to a second edge” of the paddle card, e.g., parallel to the bottom edge in Fig. 4A. EX1005, [0060], Fig. ~~4A (annotated below);~~
~~Souri, ¶974A.~~



Ayzenberg, Fig. 4A (excerpted, annotated)

98. Ayzenberg meets [1C] because solder pads 410 on row 422B “are used to electrically and physically connect to the pair of signal wires.” *Supra* §VI.B.1.c ({A.2.a.iii (Limitation [1B]); EX1005, [0060], [0069]; ~~Souri, ¶98.~~}. The exposed ends of signal wires soldered to each solder pad 410 in row 422B are

“*exposed ends of sheathed wires*” as explained for [1B]. *Supra* §VI.A.2.a.iii (Limitation [1B]); EX1005, [0049], [0069]. The wires soldered to pads 410 in row 422B are “(inner wires)” meeting [1C]. EX1001, Fig. 3, 4:51-59.

Supra §VI.B.1.c ([1B]); EX1005, [0049], [0069]; Souri, ¶98. The wires soldered to pads 410 in row 422B are “inner wires” meeting [1C]. EX1001, Fig. 3, 4:51-59;

Souri, ¶98.

99. ———eThus, it is my opinion that Ayzenberg meets Limitation [1C].

v. Limitation [1D]

<u>[1D]:</u> with the electrodes in the inner set being staggered relative to the electrodes in the outer set.

100. Ayzenberg meets [1D] because—as the dashed red lines in annotated Figure

Fig. 4A (below) make clear—Ayzenberg staggers the signal solder pad pairs (e.g., J2J9J2 to J9) and ground contacts (shaded green) in row 422B (“inner set”)

“relative to the electrodes” for the signal solder pad pairs and ground contacts in row 422A (“outer set”). *Supra* §VI.A; EX1005, [0060], Fig. 4A; Souri, ¶100. In Figure 4A no pad in row 422B has the same lateral displacement from the left side of the paddle card as a pad in row 422A. Souri, ¶100.

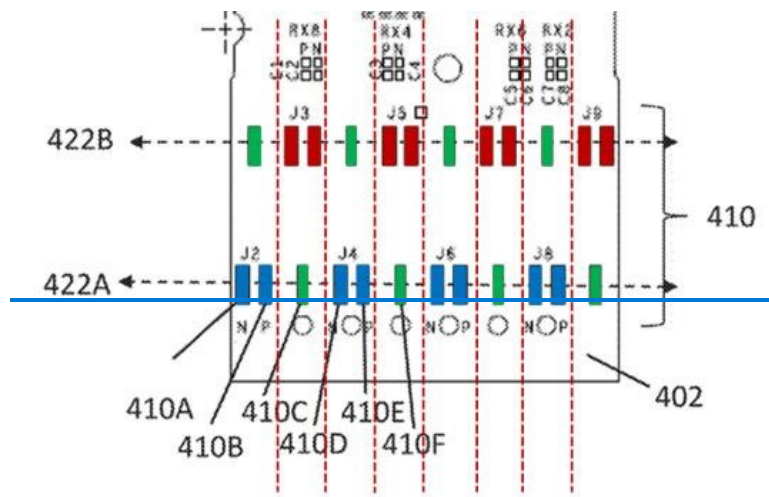


FIG. 4A

(“outer set”). *Supra* §§VI.A.2.a.iii (Limitation [1B]), VI.A.2.a.iv (Limitation [1C]); EX1005, [0060], Fig. 4A. No pad in row 422B has the same lateral displacement from the left side of the paddle card in Fig. 4A as a pad in row 422A.

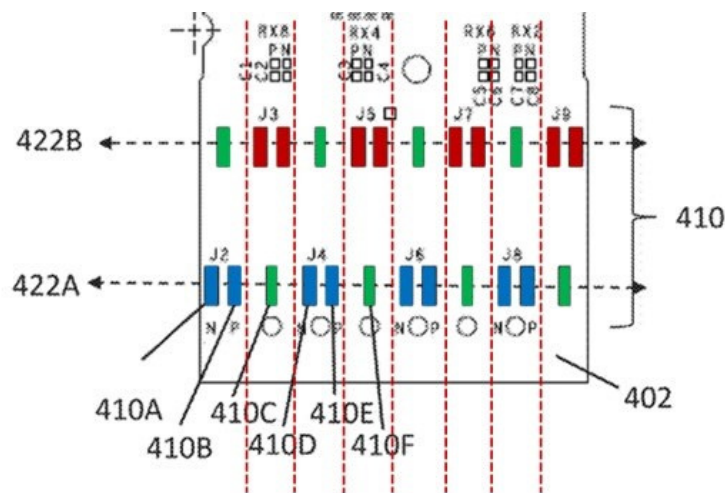


FIG. 4A

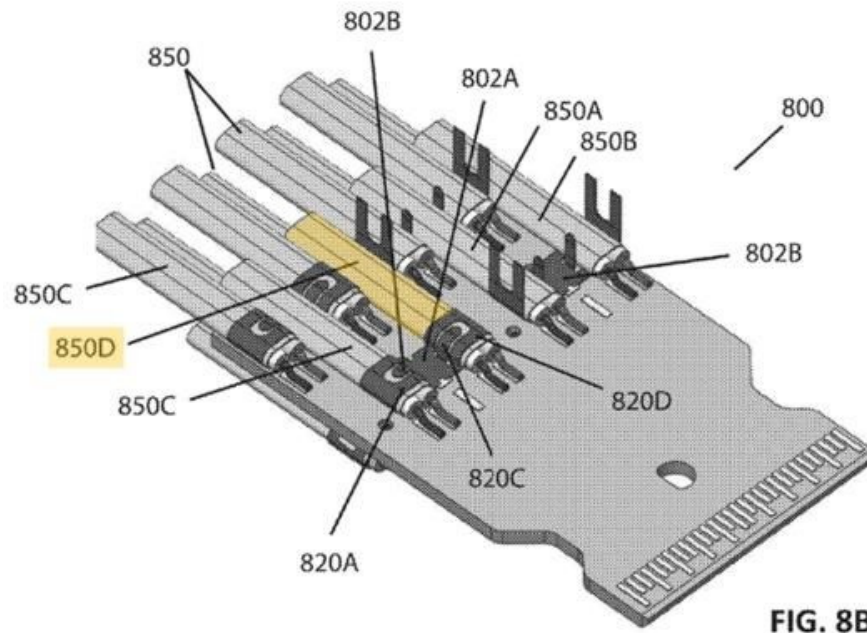
Ayzenberg, Fig. 4A (excerpted, annotated)

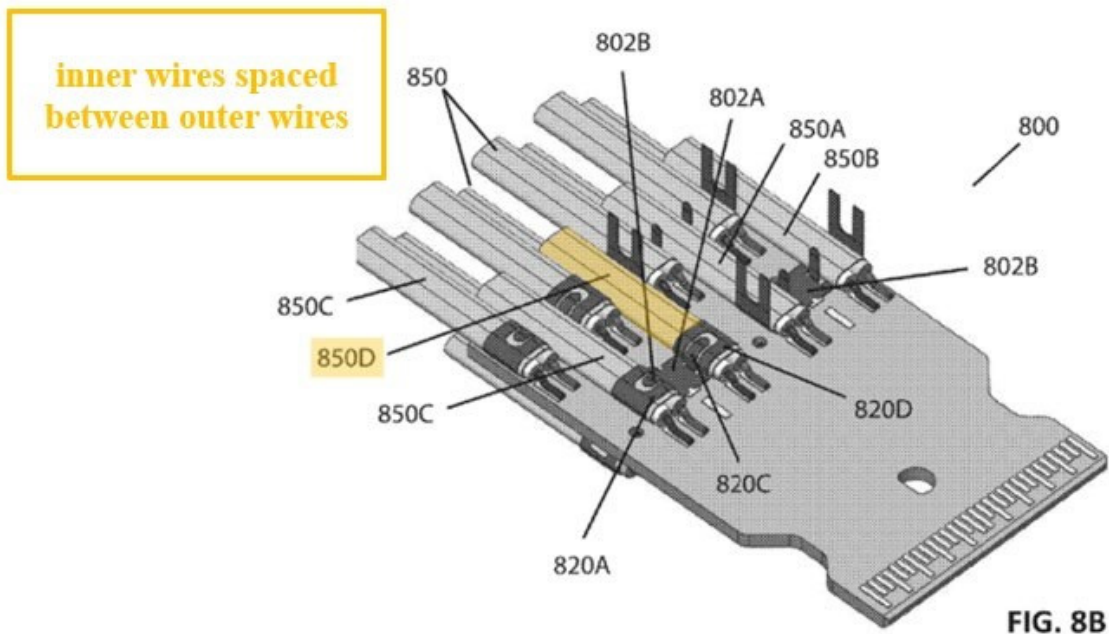
101. Staggering the electrodes allows wires connected to the inner set of electrodes to pass between the wires connected to the outer set of electrodes:

The cables may be electrically and physically mounted to the PCB *in different rows along the PCB, so that connections for neighboring cables are staggered along the width of the PCB.*

EX1005,
[0043],
(emphasis
added), Figs. 6B,
8B; *supra*
§VI.A; *Souri*,
¶101.

inner-wires
spaced
between
outer-wires





Ayzenberg, Fig. 8B (annotated)

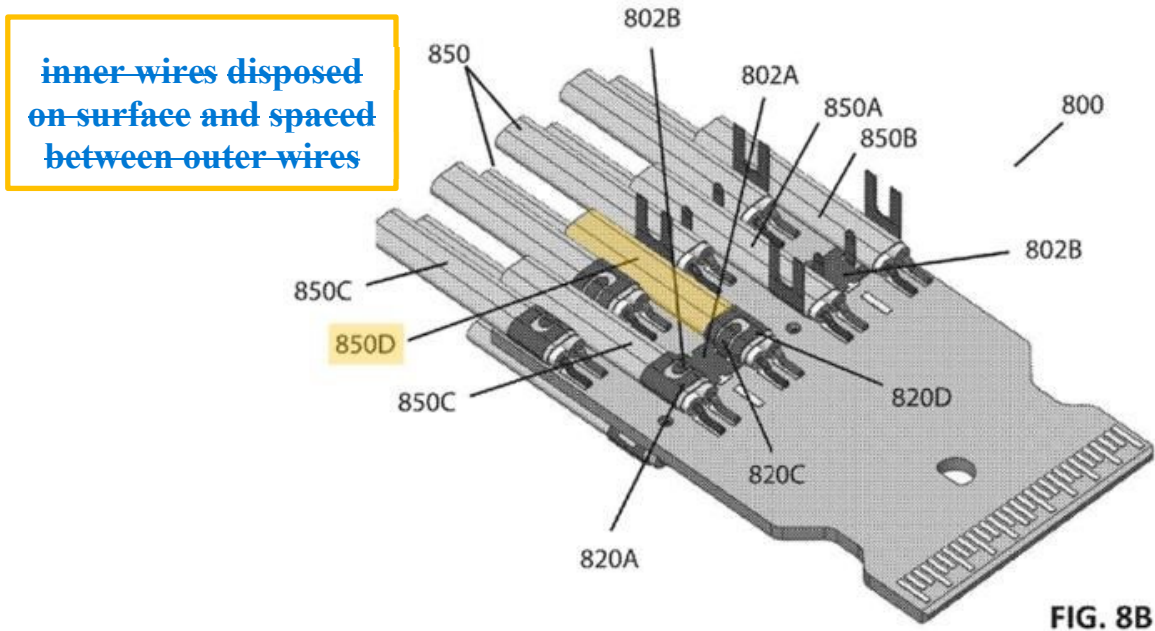
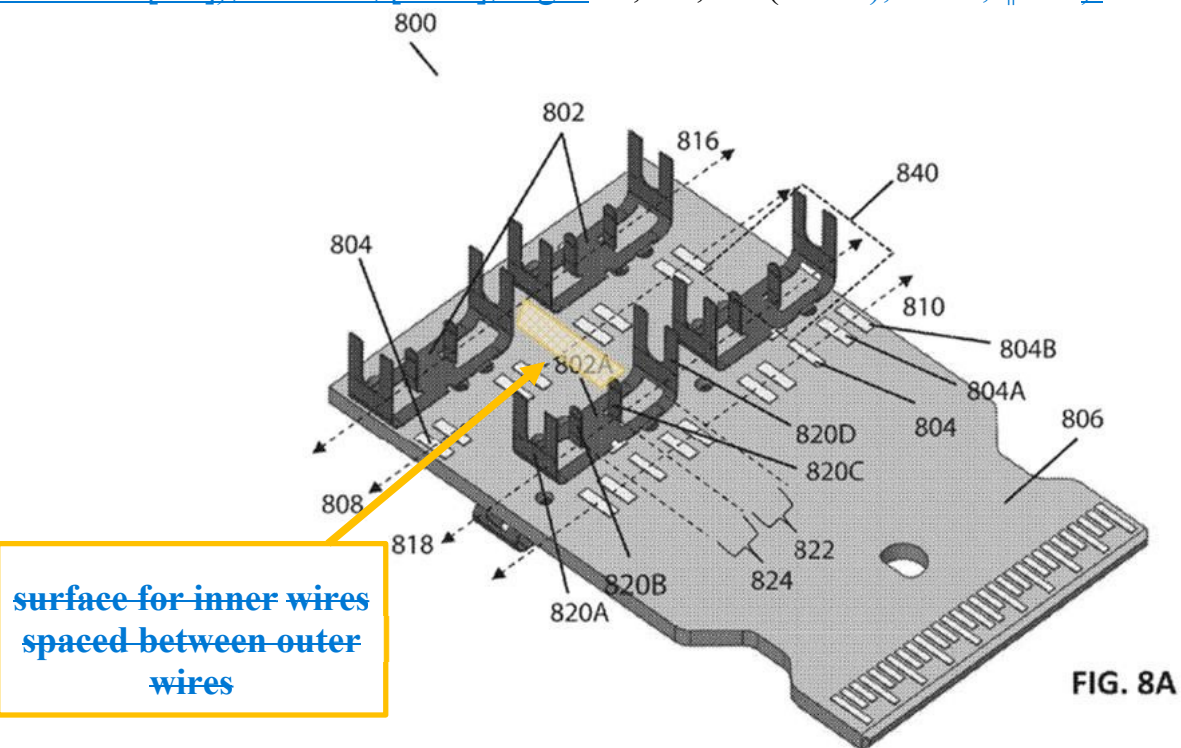
102. Thus, it is my opinion that Ayzenberg meets Limitation [1D].

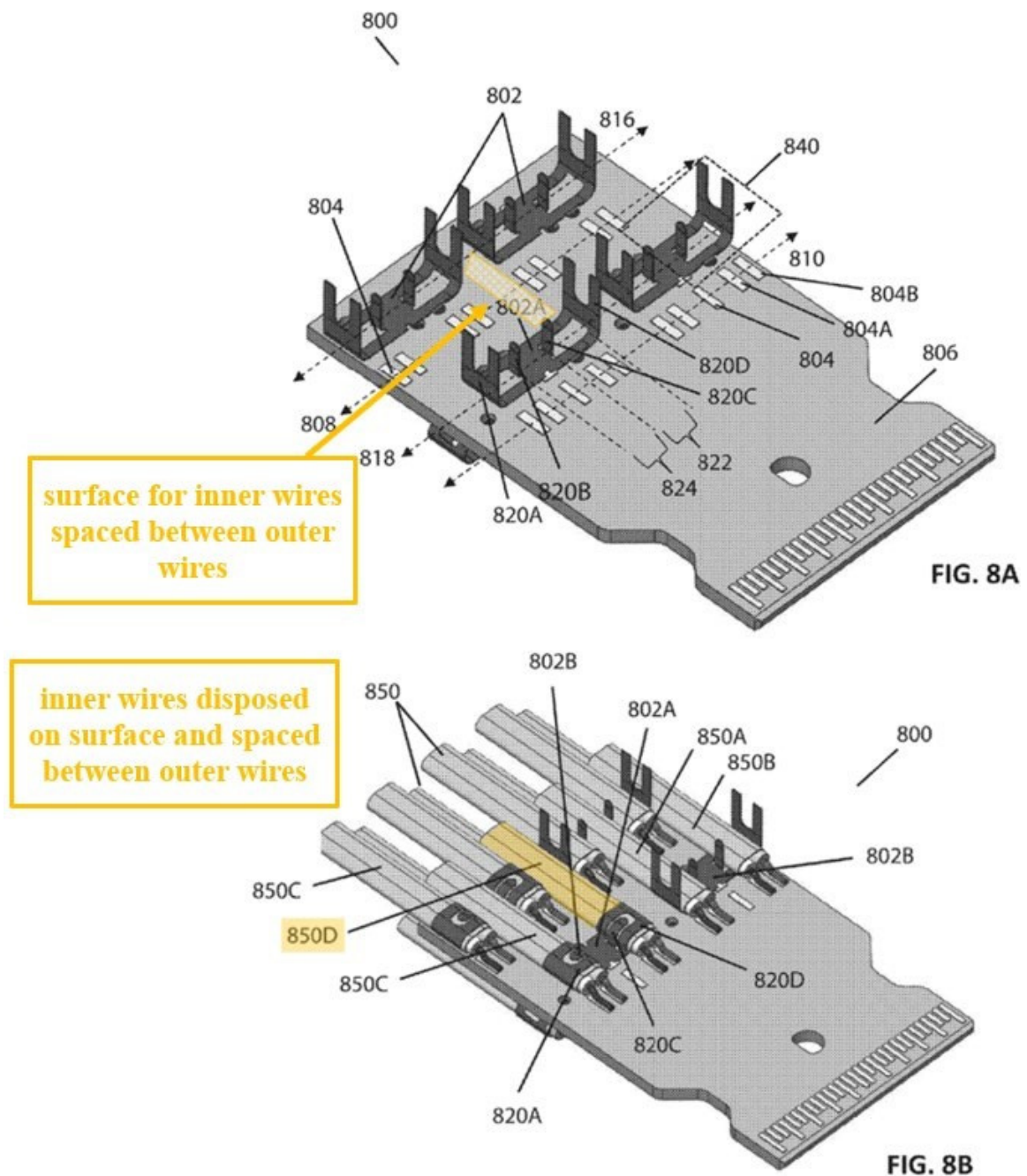
Claim 2

b. : The [PCB] of claim 1, with the electrodes in each of the inner and outer sets being spaced to enable the inner wires to pass between the outer wires while maintaining contact with the at least one surface.

103. Ayzenberg meets claim 2 because the “outer” and “inner” rows of Ayzenberg’s solder pads are “spaced” such that wires connected to the “outer set” pass between the wires connected to the “inner set.” *Supra* §VI.B.1.e ([1D]); EX1005, [0043], Figs. A.2.a.v

(Limitation [1D]); EX1005, [0043], Figs. 6B, 8A, 8B (below); Sourin, ¶103.).





Ayzenberg, Figs. 8A (annotated, excerpted), 8B (annotated)

104. Figure 8B (above) shows that “inner wires” 850D pass between adjacent “outer wires” 850 while disposed flush against (“maintaining contact with”) the PCB surface (“the at least one surface”). ~~Souri, ¶104.~~

Regardless, POSAs would have had reasons to connect inner wires to

105. Ayzenberg's paddle card by disposing them so that they "*maintain contact*" with the surface of the PCB asbecause this would have facilitated uniform positioning of the signal wire leads for soldering to the solder pads (as shown in Fig. 6B) and because Ayzenberg teaches that the wires are both "*physically* and electrically *mounted... side-by-side to the PCB.*" EX1005, Fig. 6B, [0043] ("Cables with a plurality of conductors may be physically and electrically mounted to the PCB, with the conductors for a particular cable mounted side-by-side on the PCB."). on the PCB." EX1005, Fig. 6B, [0043]; Souri, ¶105.

106. ~~3.~~ Thus, it is my opinion that Ayzenberg meets claim 2.

c. **Claim 9**

ai. **Preamble [9PRE]**

[9PRE]: **A cable that comprises:**

107. Ayzenberg meets [9PRE] because it is titled "High Performance Cable Termination" and teaches "[a] cable assembly comprising a connector with a termination that enables high density and high signal integrity" for use with data cables. EX1005, code (54), Abstract, Figs. 9A, 10A (cable bundles), [0042] ("cable assembly may include a plurality of cables"), [0043] (describing "cables with a

plurality of conductors”); ~~Souri, ¶107.~~). Ayzenberg’s cable assembly comprises “a cable” and meets claim 9 as shown below. EX1005, ~~Fig. 9A, [0087].~~

~~Fig. 9A, [0087]; Souri, ¶107.~~

~~bii.~~ **Limitation [9A]**

~~[9A].~~ **sheathed wires extending between a first connector and a second connector,**

108. Ayzenberg meets [9A] because cable bundle 900 includes cables 902, each comprising a pair of signal conductor “wires” 904. EX1005, Fig. 9A, ~~[0087]; Souri, ¶108.]~~. Each signal conductor is a “*sheathed wire*[]” because “[e]ach signal conductor is surrounded by a dielectric material” 906. EX1005, [0088]-[0089], Figs. ~~9A, 9B; Souri, ¶108. The dielectric material surrounding each wire is a sheath. EX1011, 1134; Souri, ¶108. 9A, 9B.~~

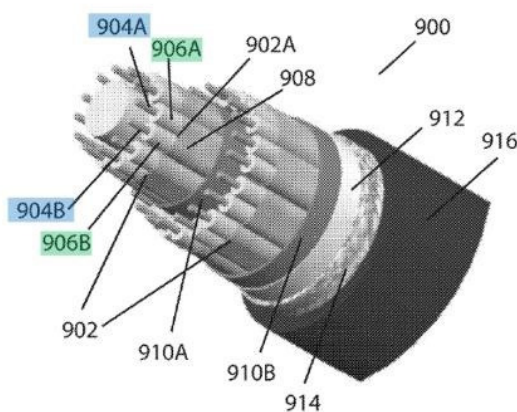


FIG. 9A

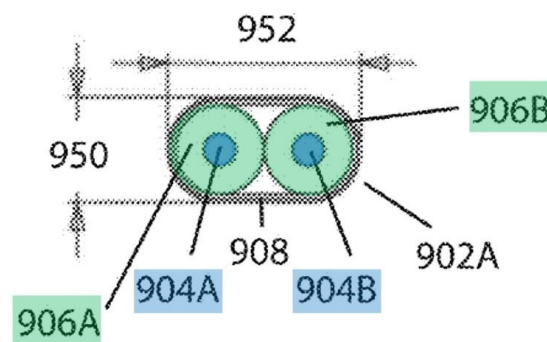


FIG. 9B

~~The dielectric material surrounding each wire is a sheath. EX1011, 1134.~~

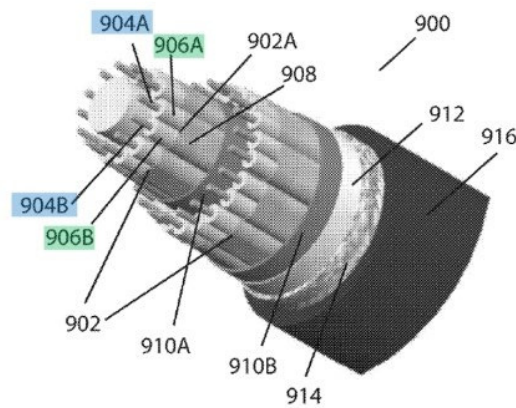


FIG. 9A

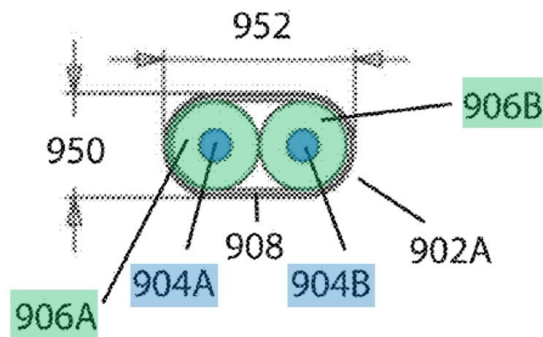


FIG. 9B

109. Ayzenberg—entitled “High Performance Cable Termination”—describes terminating each end of a signal conductor, in each wire, at solder pads on a paddle card, in a connector. EX1005, Abstract, [0002]-[0003] (“Cables are often terminated *at their ends* with electrical connectors that mate with corresponding connectors on the electronic devices....”), enabling quick interconnection of the electronic devices.” (emphasis added), [0009] (“wires may be attached to a terminating structure, such as *a paddle card of a connector*”), (emphasis added), [0039] (“PCB may be a paddle card *of a connector*”); [.]” (emphasis added)); Figs. ~~6A, 6B~~; ~~Souri, ¶109.~~ POSAs would have understood from Ayzenberg’s description that Ayzenberg’s PCBs would have 6A, 6B. A POSA would have understood from Ayzenberg’s description that Ayzenberg’s PCB would have terminated both ends of a eable’s cable comprising signal wires. ~~Souri, ¶109.~~

~~Te~~It is my opinion that, to the extent ~~the Board disagrees with that~~ Ayzenberg ~~does not~~ literally ~~meeting~~meet [9A], ~~POSA~~Asa POSA would have known that the conventional and obvious way to terminate a signal wire was to terminate each end in a paddle card enclosed in a connector. ~~Souri, ¶110.~~ The same reasons that Ayzenberg describes terminating a sheathed ~~wires to~~wire in a PCB would have motivated POSAs to terminate each end of

110. Ayzenberg's "*sheathed wires*" at a paddle card ~~for use, each of which~~ being used in a ~~mating~~ connector, meeting [9A]. EX1005, [0003], [0009]; EX1017, 1 (showing cable terminated ~~by~~in a connector at each end); EX1007, 6:65-67 (describing "a cable and a pair of transceivers provided at respective ends of the cable"); EX1001, 1:3-22 (admitting known to use paddle card in connector). ~~housing paddle cards in connectors was known); Souri, ¶110.~~

111. ~~_____e~~Thus, it is my opinion that Ayzenberg meets Limitation [9A].

iii. **Limitation [9B]**

~~[9B]~~]: each of the first and second connectors including a [PCB] with at least one surface having:

112. Ayzenberg meets [9B] because its paddle card is a "*a [PCB] with at least one surface.*" EX1005, [~~0057~~][0058], Fig. 4A; *supra* §VI.~~B.1A.2.a~~(f.i
(Preamble

~~[1PRE]; Souri,~~

~~¶112.])~~ Ayzenberg describes using a paddle card in a “connector.” *Supra* §
VI.~~B.3.b~~ (~~A.2.a.ii~~ (Limitation [9A]); EX1005, Abstract, [0002]-[0003], [0009]
 (“[W]ires may be attached to... a terminating structure, such as a paddle card of a
connector.

The signal wires may be attached to *conductive elements serving as mating*
contacts in the connector.”),” (emphasis added), [0039]; ~~Souri, ¶112.—]~~.

113. As ~~explained~~ I discussed above with respect to Limitation [9A] (*supra*
§VI.~~B.3.b~~ (~~[9A]~~), A.2.a.ii), Ayzenberg describes a cable assembly terminated at
each end with connectors. A connector encloses the paddle card at each cable end,
meeting the “*first and second connectors*” in [9B], so that the cable can connect
electronic devices (e.g., servers, routers, and switches) to each other to “enable low
loss cable assemblies” and “reduce crosstalk across cables.” EX1005, [0045],
[0057], [0075]-[0077], [0002]-[0003]; ~~Souri, ¶113.—]~~.

114. ~~—~~ Thus, it is my opinion that Ayzenberg meets Limitation [9B].

iv. **Limitations [9B1]-[9B4]**

Ayzenberg meets ~~limitations~~ Limitations [9B1]-[9B4] for the reasons that it
meets the corresponding limitations ~~[1A]-[1D]~~ as shown in claim 1 below. EX1013,
1; ~~Souri, ¶115.~~

. The “*some of the sheathed wires*” in [9B2] are the “*outer wires*” in [1B], while the

115. “others of the sheathed wires” in [9B3] are the “inner wires” in [1C].
~~Souri, ¶115.~~

Limitation	Corresponding limitation	Discussion <i>supra</i>
[9B1]	[1A]	§ VI. ~~B.1.b~~ <u>A.2.a.ii</u>
[9B2]	[1B]	§ VI. ~~B.1.e~~ <u>A.2.a.iii</u>
[9B3]	[1C]	§ VI. ~~B.1.d~~ <u>A.2.a.iv</u>
[9B4]	[1D]	§ VI. ~~B.1.e~~ <u>A.2.a.v</u>

116. ~~_____4._____~~ Thus, it is my opinion that Ayzenberg meets Limitations
[9B1]-[9B4].

d. **Claim 10-: The cable of claim 9, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.**

117. Ayzenberg meets the additional limitations in claim 10 for the reasons
it meets claim 2. ~~Supra §VI.B.2; Souri, ¶117.~~

118. ~~_____5._____~~ Thus, it is my opinion that Ayzenberg meets claim 10.

e. **Claim 16**

~~_____aj.~~ **Preamble [16PRE]**

<u>[16PRE]:</u> A cable manufacturing method that comprises:

119. If [16PRE] is limiting, Ayzenberg meets it because it describes a cable
assembly and “a cable manufacturing method” for producing it that meets [16A]
~~[16C]~~ as shown below. ~~Souri, ¶119.~~

120. Regardless, as shown below, POSAs would have had reasons to make

Ayzenberg's cable following the "providing...", "soldering...", and

"packaging..." steps in [16A]

[16C] in order to achieve a cable terminated at each end with Ayzenberg's cable assembly having connectors enclosing Ayzenberg's PCB at each end because this was the conventional and obvious way to make a high-performance cable using Ayzenberg's PCB. ~~Souri, ¶120; infra §§VI.B.5.b-VI.B.5.e.~~

~~bii.~~ Limitation [16A]

[16A]: providing first and second [PCBs] each having:

121. Ayzenberg meets [16A] because it teaches—and POSAs would have had reasons to provide—a PCB terminating each end of a cable. *Supra* §§VI.B.1A.2.a (claim 1), VI.B.3A.2.c (~~{.iii (Limitation [9B]); Souri, ¶121.}~~). The "first and second connectors" in [9B] are associated, respectively, with "first and second PCBs" meeting [16A]. *Supra*

§§VI.B.1 (claim 1), VI.B.3.c (~~{[9B]; Souri, ¶121.}~~) are associated, respectively, with "first and second PCBs" meeting [16A]. *Id.*

As shown for [9B], Ayzenberg describes a cable having a connector, comprising a PCB, at each end cable. *Supra* §VI.B.3.c (~~{A.2.c.iii (Limitation [9B]); Souri,~~

~~¶121.]).~~ Regardless, it is my opinion that POSAs would have found it conventional to terminate each end of a cable ~~that~~ a connector comprising Ayzenberg's PCB. *Supra* §VI.~~B.3~~A.2.c(~~.iii~~ (Limitation [9B]); ~~Souri, ¶121.]).~~

122. Ayzenberg's PCB ~~terminating at~~ each ~~cable~~ end of the cable meets [16A1]-[16A4] as shown below.~~—Souri, ¶122.~~ Thus, a POSA would have understood that implementing Ayzenberg's teachings required "*providing*" the PCBs because the PCBs would have had to have been "*provid[ed]*" before they could be attached to each end of the cable.

~~PCBs would have had to have been "*provid[ed]*" before they could be attached to the ends of a cable. Souri, ¶122.~~

123. ~~_____c._____Limitations~~ Thus, it is my opinion that Ayzenberg meets Limitation [16A].

iii. Limitation [16A1]-[16A4]

124. Ayzenberg meets Limitations [16A1]-[16A4] for the reasons that it meets the corresponding limitations ~~[1A]-[1D] as shown in claim 1~~ below. EX1013, 2; ~~Souri, ¶124.~~

Limitation	Corresponding limitation	Discussion <i>supra</i>
[16A1]	[1A]	§VI. ~~B.1.b~~ <u>A.2.a.ii</u>
[16A2]	[1B]	§VI. ~~B.1.c~~ <u>A.2.a.iii</u>
[16A3]	[1C]	§VI. ~~B.1.d~~ <u>A.2.a.iv</u>
[16A4]	[1D]	§VI. ~~B.1.e~~ <u>A.2.a.v</u>

125. ~~i.~~ Thus, it is my opinion that Ayzenberg meets Limitations [16A1]-

[16A4].

(1) Limitation [16A1]: “for contacting electrical conductors when the [PCB] is inserted in a matching socket”

The I have been informed by counsel that the “for contacting...” language is non limiting. *Supra* §VI.B.1.b.A.2.a.ii ((Limitation [1A]);

126. ~~Boehringer, 320 F.3d at 1345.].~~ Regardless, if it is construed as limiting, then Ayzenberg meets it as shown below.

127. Ayzenberg’s contact pads 406 would conventionally have “contact[ed] electrical conductors” in a “mating connector” (“socket connector”) within a cage (i.e., “socket”) that the QSFP-DD standard describes as receiving a pluggable module comprising a connector enclosing a PCB like Ayzenberg’s: EX1005, [0063]; E.g., EX1010, 28-29, 53 (surface mount “QSFP-DD Connector is a 76contact, right angle connector”), Fig. 30 (below); *supra* §VI.B.1.b ((1A)); *Souri*, ¶¶69-72, 127. PCB.

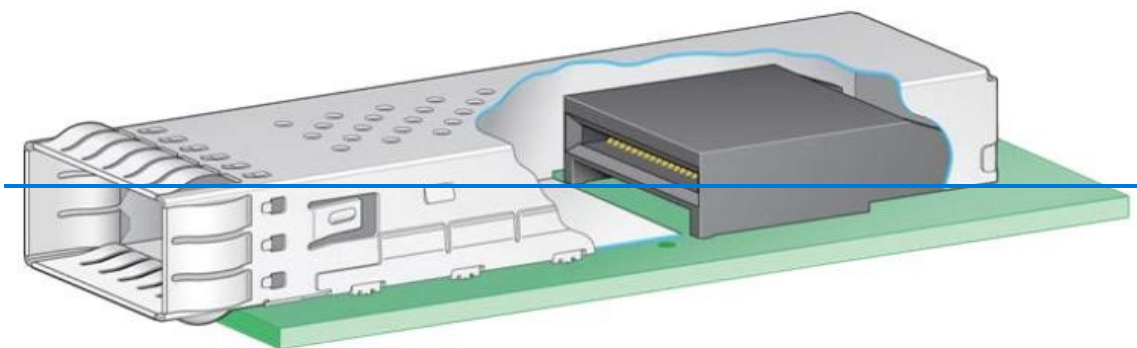


Figure 30: SMT connector in 1xn cage

EX1005, [0063]; *supra* §V.E; see e.g., EX1010, 28-29, 53 (surface mount “QSFPDD Connector is a 76-contact, right angle connector”), Fig. 30 (below); *supra* §VI.A.2.a.ii (Limitation [1A]).

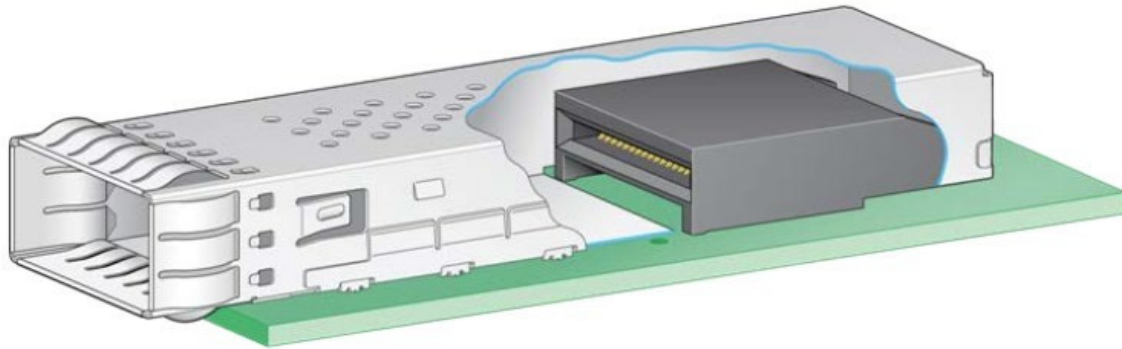


Figure 30: SMT connector in 1xn cage

The '898 specification explains that “[v]arious standard cable connectors *and connection ports* are provided including, e.g., QSFP-DD... connectors, which are designed to house small [PCBs] with integrated transceiver electronics.”

128. EX1001, 1:3-34. POSAs would have understood that Ayzenberg’s “mating connector” (“*socket connector*”) and the claimed “*matching socket*” ~~([16A1])~~ are ([16A1]) are “connection ports” for receiving the connectors like those including Ayzenberg’s PCB, as recited in Limitation [16C] below. EX1010, 28-29; ~~Souri~~, ¶128.

129. ~~ii.~~ Thus, it is my opinion that Ayzenberg meets Limitation [16A1].

(2) Limitations [16A2]-[16A3]: “*certain...wires*” /

“other...wires”

130. The “*certain sheathed wires*” in [16A2] are the “*outer wires*” in [1B], while the “*other sheathed wires*” in [16A3] are the “*inner wires*” in [1C]. ~~Souri,~~
~~¶130.~~

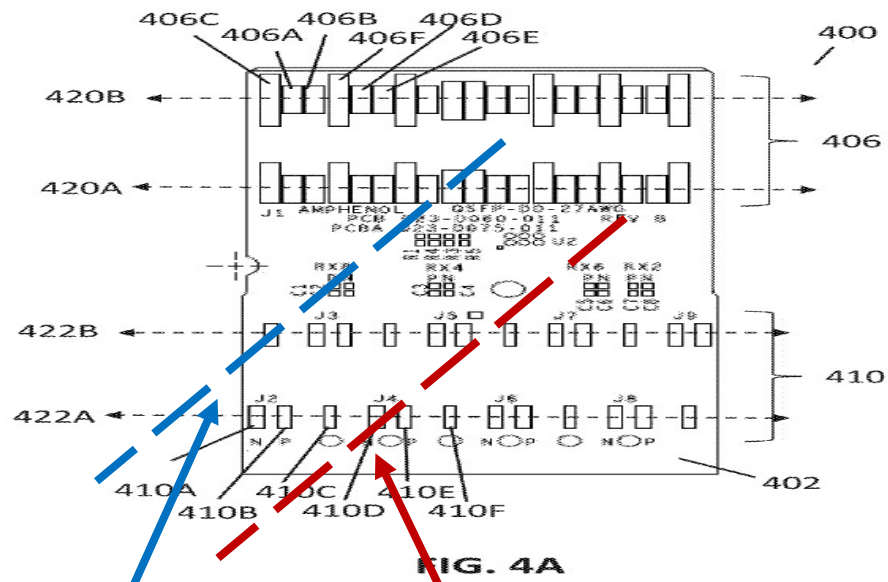
131. ———~~d~~ Thus, it is my opinion that Ayzenberg meets Limitations [16A2]-
[16A3].

iv. Limitation [16B]

<u>[16B]:</u> soldering unsheathed ends of the sheathed wires to the electrodes in the inner and outer set;
--

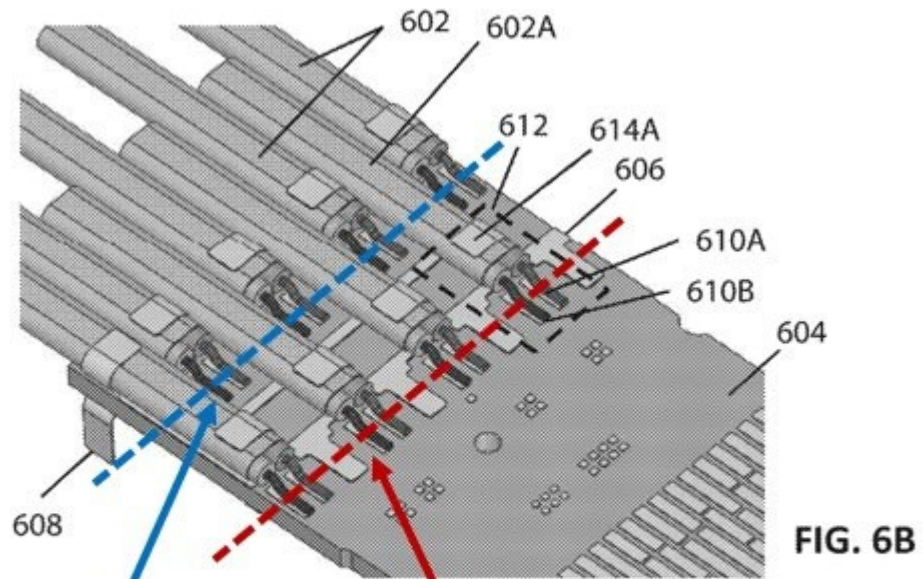
Ayzenberg meets [16B] because it teaches soldering unsheathed signal wire leads (“*unsheathed ends of the sheathed wires*”) to the ~~PCB’s~~ “*outer*” (*supra* §VI.~~B.1.c~~ (~~{~~A.2.a.iii (Limitation [1B])) and “*inner*” (*supra* §VI.~~B.1.d~~ (~~{~~A.2.a.iv (Limitation [1C])) ~~sets~~set of solder pads 410

132. (“*electrodes*”.) on the PCB. EX1005, [0073] (“[f]or each cable, the ends of the signal wires are soldered to respective signal solder pads”), Fig. 6B (annotated below showing signal wire ends soldered to “*inner*” and “*outer*” solder pads); ~~Souri,~~ ~~¶132.~~).



solder pads:
outer row

solder pads:
inner row



solder pads:
outer row

solder pads:
inner row

Ayzenberg, Fig. 6B (annotated)

133. Thus, it is my opinion that Ayzenberg meets Limitation [16B].

y. **Limitation [16C]**

~~[16C]~~: and packaging the first and second printed circuit boards into connectors adapted to fit into a socket.

Ayzenberg meets [16C] because it describes using its paddle card

134. (“first”/“second PCB”) in “standards based connectors (e.g., for QSFP-DD)” that were affixed to each end of a cable and known to be “*adapted to fit into a socket.*”

EX1005, [0057]; EX1010, 28-29; *Suprasupra* §VI.B.5.b (~~[A.2.e.ii (Limitation [16A]); Souri, ¶134.]~~).

135. Ayzenberg teaches “*packaging*” the PCB because it describes “cable assembly 700 [that] includes outer portions 702 and 704 of a plug housing” that “*surround[s] the paddle card 708.*” EX1005, [0075], Fig. 7 (below).

~~“surround[s] the paddle card 708.” EX1005, [0075], Fig. 7 (below); Souri, ¶135.~~

136. Furthermore, ~~POSA~~sa POSA would have recognized that a conventional and obvious way to achieve ~~Ayzenberg’s~~the connector that ~~encloses~~Ayzenberg describes as enclosing the PCB would have required “*packaging...[... [the PCBs] into connectors.*” ~~POSA~~s” and a POSA would have had reasons to “*package*” the PCB this way to achieve what Ayzenberg describes.

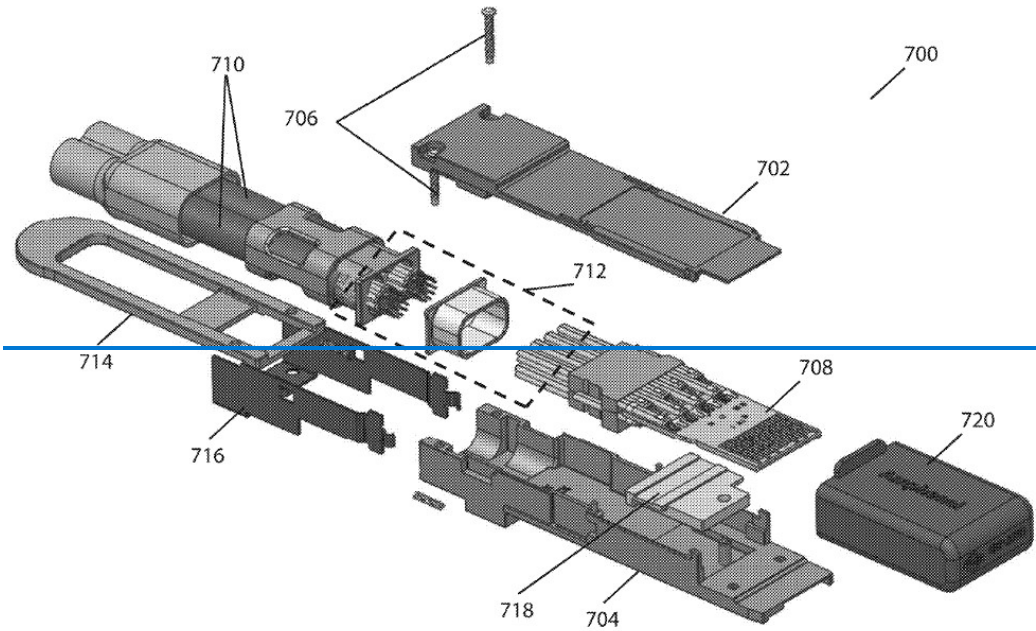


FIG. 7

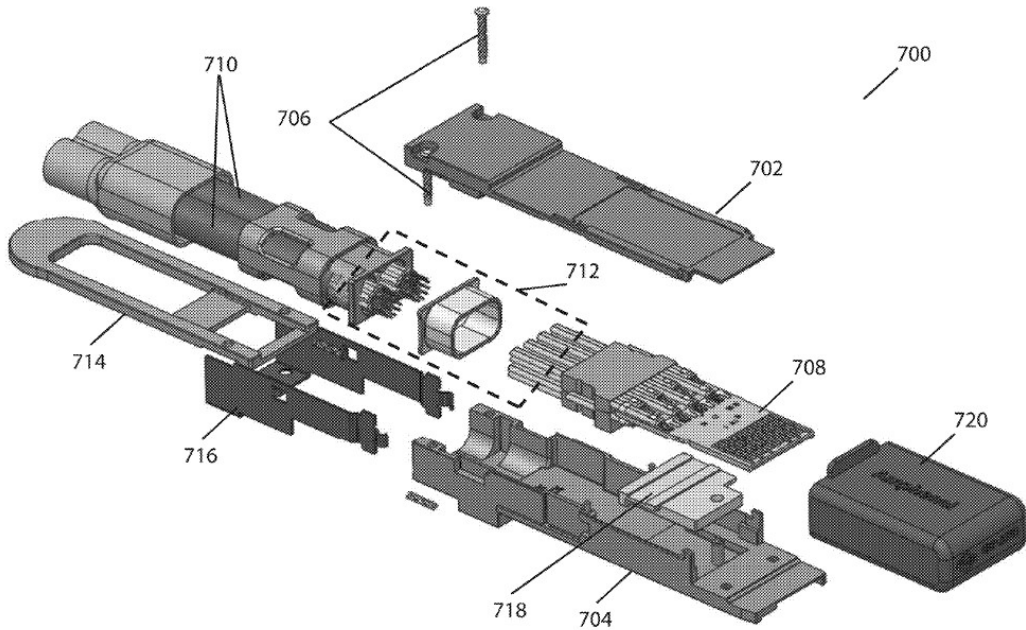


FIG. 7

Ayzenberg, Fig. 7

137. The plug housing (enclosing PCB 708) forms “connectors adapted to fit into a socket” because it allows the cable to “mate with a receptacle connector mounted in an electronic device” such that “the mating contact portions ... at the end of the paddle card” are “configured to mate with mating contact portions in a receptacle” (e.g., a “socket”). EX1005, [0076]-[0077]. As discussed *supra* § VI.A.2.a.iii (Limitation [1B]), POSAs would have recognized that Ayzenberg’s

“socket”). EX1005, [0076]-[0077]; ~~Souri, ¶137. As discussed *supra* § VI.B.1.e ([1B]), POSAs would have recognized that Ayzenberg’s~~ “receptacle” is a “socket.” EX1005, [0077].

~~EX1005, [0077]; Souri, ¶137.~~

138. ~~6. Claim 18~~ Thus, it is my opinion that Ayzenberg meets Limitation [16C].

f. Claim 18: The method of claim 16, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.

139. Ayzenberg meets the additional limitations in claim 18 for the reasons it meets claim 2. *Supra* § VI.B.A.2; ~~Souri, ¶139.b.~~

140. ~~VII. GROUND~~ Thus, it is my opinion that Ayzenberg meets claim 18.

B. Ground 2: AYZENBERG+LUGTHART RENDERS OBVIOUS CLAIMS The Combination of Ayzenberg and Lugthart Renders Obvious Claims 3, 11, AND 17

1. Discussion of ~~A.~~ Lugthart (EX1007)

141. Lugthart teaches a “high-speed communication link” in the form of “a cable and a pair of transceivers provided at respective ends of the cable.” EX1007, 6:656765-67. Lugthart’s transceivers comprise “a single integrated circuit (IC)” having “a host side for facing an electronic device and a line side for facing the cable.” EX1007, Id., 15:25-34, 19:46-48, Fig. 4A; Souri, ¶141. The transceivers thus have a transmit path “configured to transport signals from an electronic device towards the cable 205” and a receive path “configured to transport signals from the cable 205 to the electronic device.” EX1007, Id., 15:25-34, 19:52-56; Souri, ¶141.

142. The Each of the transmit and receive paths include clock and data recovery (CDR) circuits and digital signal processors (DSP). EX1007, 7:66-8:7, 21:33-38; Souri, Id., 7:66-8:7, 21:33-38. POSAs thus would have recognized Lugthart’s transceivers to be in ICs in a cable that perform data recovery and remodulation of the signals sent or received via the cable.

¶142. POSAs thus would have recognized Lugthart’s transceivers to be ICs in a cable that perform data recovery and remodulation 2. Discussion of signals transferred over the cable. Souri, ¶142.

~~B.~~ ~~Ayzenberg+Lugthart~~ Combination

143. As noted *supra* §§VI.A.1 (Ayzenberg), ~~VI.B.1~~VII.A (Lugthart), both Ayzenberg and Lugthart teach a cable assembliesassembly integrating PCBsa PCB for interfacing signals passed by wires in the cable between electronic devices.

~~1a.~~ **Reasons to Combine**

144. Ayzenberg teaches that ~~the~~the paddle cards terminating the ends of the cable may include “active components,”~~e.g.,~~such as “transceivers ... attached to the paddle card,” but does not describe the specifics of such ~~transeeivers are not described~~a transceiver. EX1005, [0065]; ~~Souri, ¶144.~~ Thus, POSAsa POSA would ~~have looked~~look to combine Ayzenberg with transceiver technologies such as those taught in Lugthart. ~~Souri, ¶144.~~ POSAsFurther, a POSA would have been motivated to look to specific transceiver technologies which aid in the development of a “high performance cable,” as ~~indicated by Ayzenberg’s described in the~~to support the provisioning of Ayzenberg, such that it supported the provision of “low insertion loss and low cross talk.” EX1005, Abstract; ~~Souri, ¶144.~~ Lugthart discloses ~~transeeivers that~~a transceiver which includes ability to “compensate for transmission line losses on the line side...[...][and] on the host side” ~~to achievesuch~~that it achieves “reliable high-speed point-to-point communication.” EX1007, 6:58-64, 9:10-15; ~~Souri, ¶144.~~

145. Lugthart explains that a transceiver “operates as a re-timer” that “can re-time and re-transmit” received signals “to generate one or more transmit signals”

~~which~~so as to “reduce[s] or remove[s] high-frequency jitter in the signals, thereby improving signal fidelity and/or permitting communication over longer distances.”

~~EX1007, 12:58-67, Fig. 2a; Sourì, ¶145. The re-timing works with signals received from a~~

~~Id., 12:58-67, Fig. 2a. The re-timing works with signals received from a~~ “host”

(e.g., electronic device 101) and transmitted to the “line” (e.g., cable 111), or ~~vice-versa. EX1007, viceversa. Id., 12:58-67, Fig. 2a; Sourì, ¶145.~~ Lugthart describes

incorporating such transceivers ~~on~~in a “transceiver assembly” terminating each ~~end~~
~~of a data~~ cable ~~end~~ “for improving performance of the cable.” ~~EX1007, Id., Fig. 2a~~

(transceivers 107a, 107b), 14:29-42; ~~Sourì, ¶145.~~ Lugthart explains that “at a

given bit rate” such ~~an~~ active ~~cables permit~~cable permits “communication over

longer distance and/or with a thinner cable” and “can decrease jitter, noise, and/or

ISI [intersymbol interference]” compared to a “passive cable” (e.g., a cable ~~with~~

~~cable assembly~~ lacking active components). ~~EX1007, 15:5-13; Sourì, ¶145. Id.,~~

~~POSAs 15:5-13.~~

146. Thus, in my opinion, a POSA would have had reasons to combine

Lugthart’s transceiver teachings with Ayzenberg to provide an active cable with

~~transceivers~~circuitry on ~~the PCBs that a PCB to~~ recover and remodulate ~~signals~~a

signal in order to achieve ~~improved high-speed~~the highspeed communication

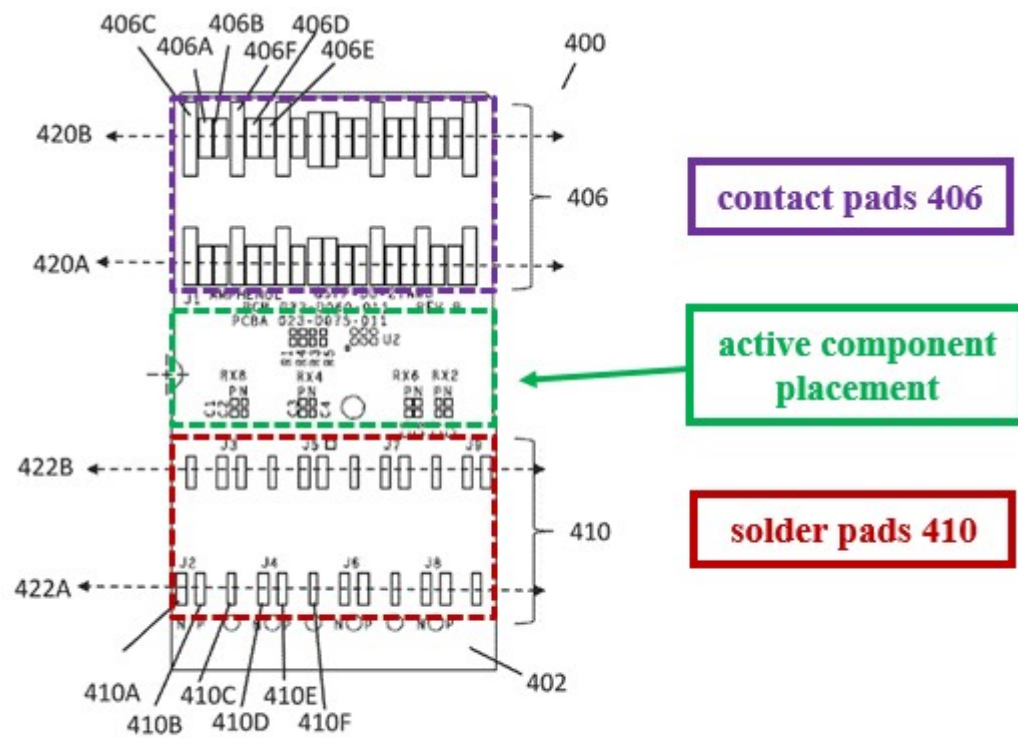
improvements that Lugthart describes. ~~Sourì, ¶146.~~ The combination would have

used known components (Ayzenberg's ~~PCBs in~~PCB and QSFP-DD compliant connectors, Lugthart's transceiver) and techniques (e.g., re-timing), according to their conventional uses, with predictable results. ~~Souri, ¶146; KSR Int'l v. Teleflex, 550 U.S. 398, 416-417 (2007).~~ The combination also would have simply ~~implemented~~substituted Ayzenberg's active transceiver with Lugthart's active transceiver to obtain the predictable result of Ayzenberg's paddle card with ~~Lugthart's transceiver. Souri, ¶146; KSR, 550 U.S.~~ ~~at 416-417. This~~Lugthart's active transceiver. I further reference this combination ~~is as~~

"Ayzenberg+Lugthart."

2b. Reasonable Expectation of Success

147. ~~A~~In my opinion, a POSA would have ~~reasonably expected~~had a reasonable expectation that Ayzenberg+Lugthart would work because Ayzenberg describes mounting transceivers such as Lugthart's on its ~~PCBs~~PCB "in the space between the row 420A of contact pads and the row 422B of contact pads shown in FIG. 4A." EX1005, ~~[0065], Fig. 4A (annotated below); Souri, ¶147.~~ [0065], Fig. 4A (annotated below).



Ayzenberg, Fig. 4A (excerpted, annotated)

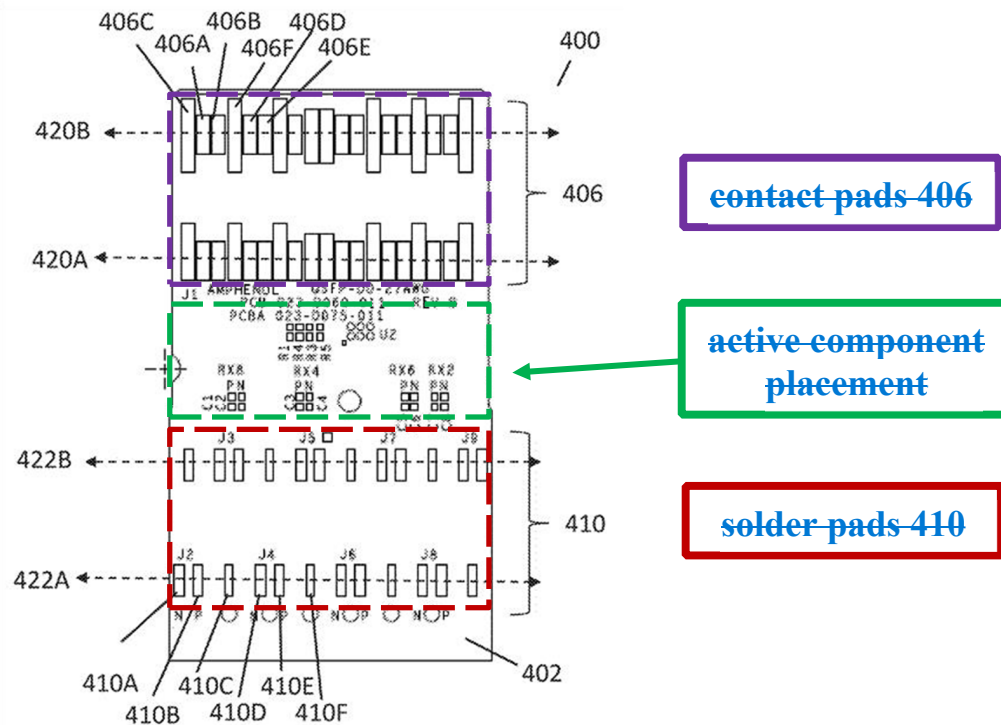


FIG. 4A

148.

Furthermore, both Ayzenberg and Lugthart describe enclosing a PCB including a transceiver in standards-compliant connectors. EX1005, Abstract, [0044]-[0045], [0057], [0087]; EX1007, 15:36-52.

~~[0044]-[0045], [0057], [0087]; EX1007, 15:36-52; Souri, ¶13.~~
Mapping of the Ayzenberg+Lugthart Combination to
Claims 3, 11, and 17

~~148.~~

C. Analysis

149. Ayzenberg+Lugthart renders obvious claims 3, 11, and 17.

~~1.~~ a. Claim 3

: The [PCB] of claim 1, further comprising an [IC] that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

150. Ayzenberg+Lugthart meets claim 1 for the same reasons as Ayzenberg alone. *Supra* §VI.~~B.1~~A.2.a (claim 1); ~~Souri, ¶150.~~

i. ~~a.~~ “recovers and remodulates signals”

151. The ’898 patent does not ~~define~~explain what an IC that “*recovers and remodulates signals,*” is but describes “a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams” by, such as ~~“convert[ing] between PAM4 and NRZ signaling.”~~ EX1001, 3:19-21, 3:65-67; Sourì, ¶151.

“convert[ing] between PAM4 and NRZ signaling.” EX1001, 3:19-21, 3:65-67.
b. — Ayzenberg+Lugthart renders claim 3 obvious.

152. Ayzenberg+Lugthart renders obvious claim 3 because Ayzenberg’s paddle card 400 (“[PCB]”) includes Lugthart’s active transceiver (“*an [IC]*”), which provides the same signal recovery and re-modulation functionality described in the ’898 specification. *Supra* §~~VH~~VI.B; ~~Souri, ¶152.~~2. Specifically, the transceiver is an *IC* mounted to the paddle card that processes “*signals passing between*” the mating contact pads on the host side (i.e., “*edge connector traces*”)

and the staggered solder pads on the line side (i.e., “*electrodes...*”) for transmission over a cable in a desired modulation format. EX1005, [0065] (active transceiver “convert[s] from the communication protocol being used on the cable to a different communication protocol... provided to a mating connector”); EX1007, 8:50-60 (describing the transceiver converting dual NRZ signals “on the host side” to a single PAM-4 signal “for transmission to the line side over the cable” and vice-versa), 15:31-34 (describing the transceiver as a single integrated circuit), Figs. 2A (device 101, cable 111), 6A (step 305) and 6B (step 355), 13:13:48 (describing the transceiver performing various remodulation formats between PAM4 and NRZ), 14:29-42 (describing host electronic device 101 and line cable 111); [Souri, ¶152.](#)

The transceiver “*recovers and remodulates signals passing between*” the host-[side](#) and [the](#) line-~~sides~~-[side](#), and thus receives and transmits signals on both [the host and line](#) sides. *E.g.*,

[153.](#) EX1007, Figs. 1A, 4A; [Souri, ¶153.](#)

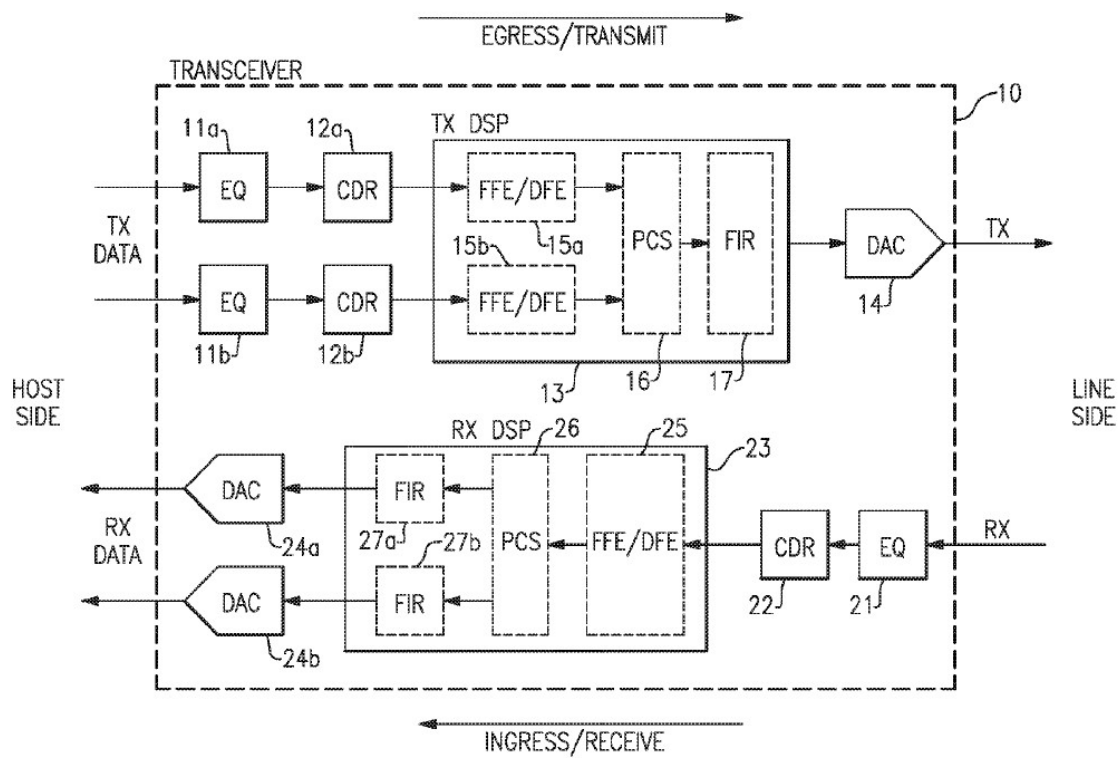


FIG. 1A

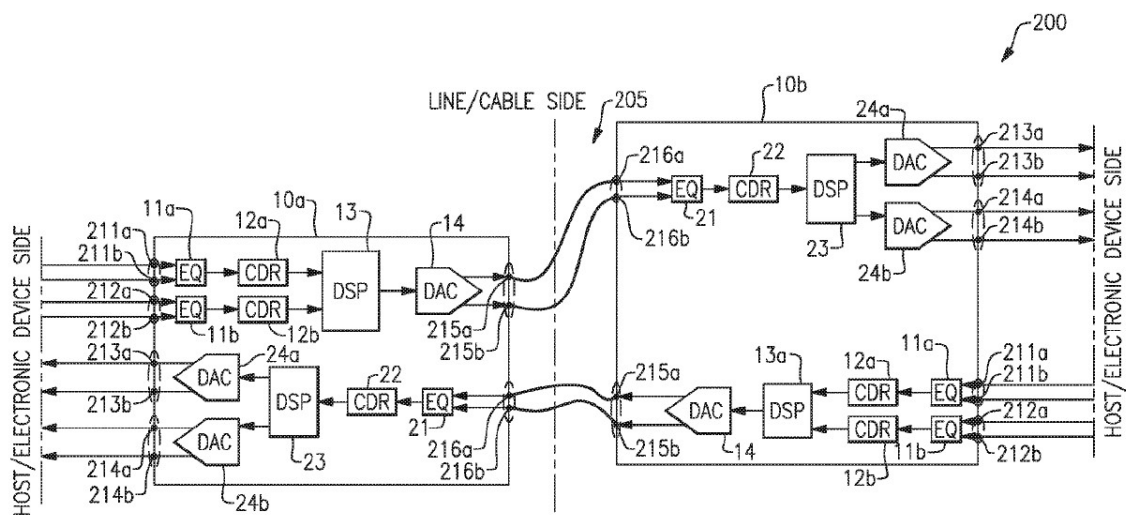


FIG. 4A

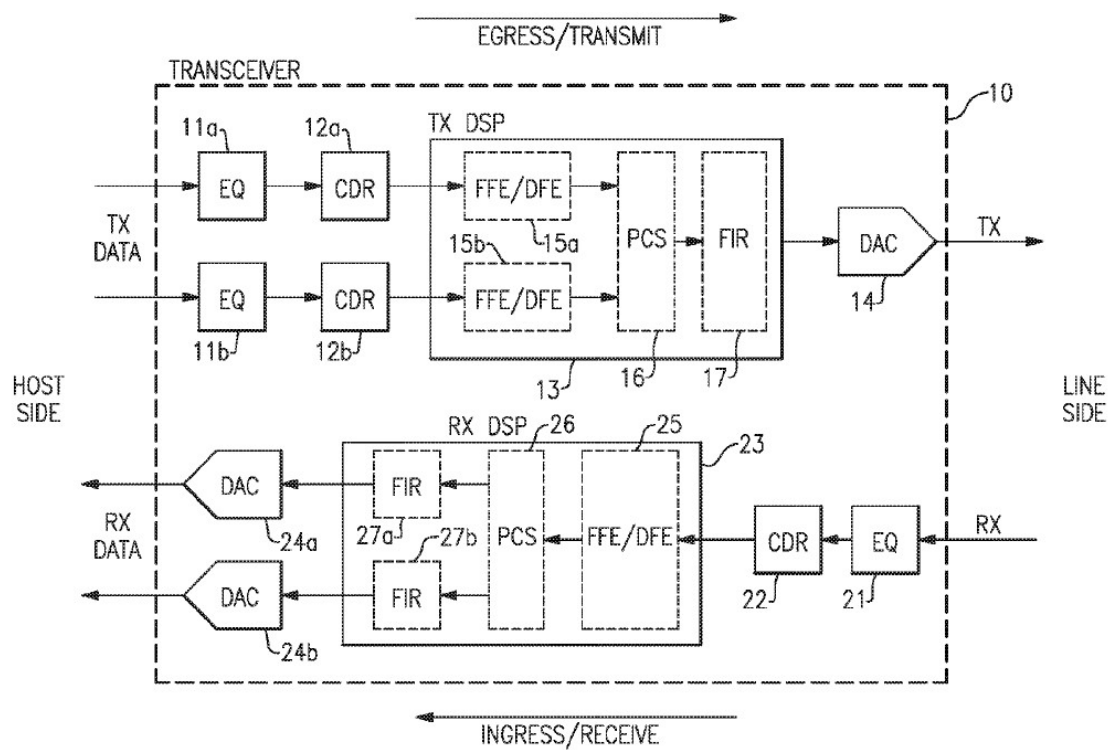


FIG.1A

Lugthart, Fig. 1A

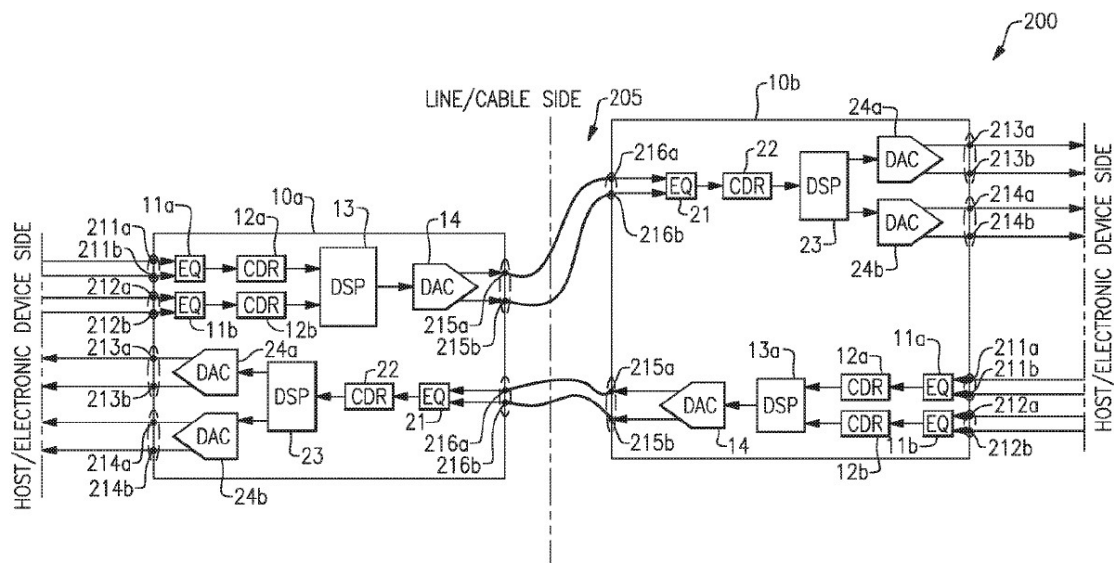


FIG.4A

Lugthart, Fig. 4A

154. Specifically, the transceiver—comprising clock and data recovery (“CDR”) circuits 12 and 22—recovers, remodulates, and transmits signals received from a cable (line) to a host, and ~~signal~~signal received from a host to a cable. *Supra* §~~VII.A~~VI.B.1; EX1007, 7:66-8:7, 21:33-38, 22:40-43, 23:10-23, Fig. 4B; ~~Souri, ¶154.~~ The CDR circuits digitize the incoming analog signals and provide “timing recovery to recover a clock and a data signal” from ~~both~~the host (EX1007, 21:43-52) and the line (EX1007, 22:50-59).~~Souri, ¶154.~~

155. The transceiver receives signals modulated with NRZ, PAM-4, or other modulation schemes, from both a *host* (EX1007, 19:65-20:15) and a line (~~EX1007,~~
~~(EX1007, 21:4-30).~~~~Souri, ¶155.~~ The transceiver likewise transmits signals modulated with NRZ, PAM-4, or other modulation schemes, to ~~both~~the *line* (EX1007, 20:61-21:3) and the *host* (EX1007, 20:29-32).~~Souri, ¶155.~~

The transceiver thus “*remodulates*” signals between host and line sides—

156. ~~i.e.g.~~, “*signals passing between the edge connector traces and the electrodes of the inner and outer sets*”—because the transceiver (when mounted as an active component on the paddle card) receives signals from the line side (via “electrodes of the inner and outer set”) having “a data rate higher than the data rate... outputted” to the host side- (via “the edge connector traces”). EX1007,

21:4-20; ~~Souri, ¶156.~~ Furthermore, Lugthart expressly describes active cables wherein a transceiver sends/receives host-side signals with NRZ modulation and sends/receives line-side signals with PAM4 modulation, where the transceiver converts between NRZ and PAM4 modulation. EX1007, 54:26-55:45; ~~Souri,~~ Converting data signals between NRZ and PAM4 modulations is “remodulation.” Accord EX1001, 3:19-21, 3:65-67.

~~¶156. Converting data signals between NRZ and PAM4 modulations is~~

157. “remodulation.” Souri, ¶¶156; accord Thus, it is my opinion that Ayzenberg+Lugthart meets claim 3.

~~bEX1001, 3:19-21, 3:65-67.~~

2. Claims 11, 17

~~11. The cable of claim 9, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.~~

~~17. The method of claim 16, further comprising equipping each of the first and second printed circuit boards with an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.~~

Claim 11: The cable of claim 9, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

Claim 17: The method of claim 16, further comprising equipping each of the first and second printed circuit

boards with an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

158. Claim 11 depends from claim 9, while claim 17 depends from claim

16. Ayzenberg+Lugthart meets claims 9 and 16 for the same reasons as Ayzenberg alone. ~~Supra §§VI.B.3 (claim 9), VI.B.5 (claim 16); Souri, ¶158.~~

Ayzenberg alone. Supra §§VI.A.2.c (claim 9), VI.A.2.e (claim 16).

159. Ayzenberg+Lugthart meets the remaining limitations in claims 11 and

17 for the same reasons it meets additional limitations in claim 3. *Supra*

§VII.C.1 (claim

VI.B.3); Souri, ¶159. a (claim 3). For claim 17, POSAs would have “*equip[ped]*”

each of

Ayzenberg’s paddle card with Lugthart’s transceiver because Ayzenberg+Lugthart

comprises a transceiver as taught by Lugthart. *Supra* §VII.B; Souri, ¶159.

~~VIII. GROUND~~ 160. Thus, it is my opinion that Ayzenberg+Lugthart meets claims 11 and

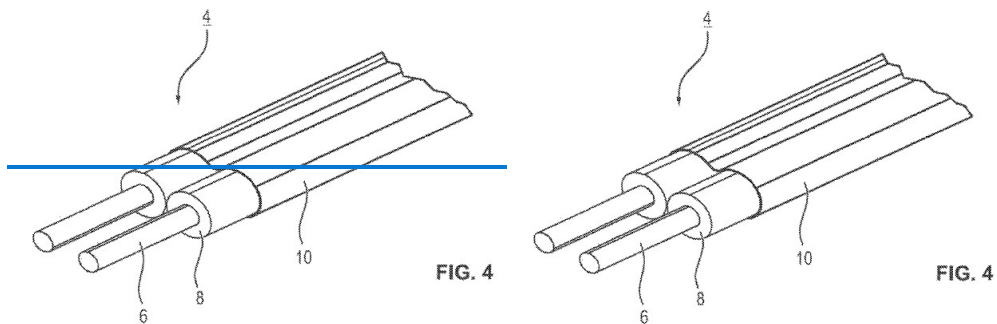
17.

C. Ground 3: AYZENBERG+JANSSEN RENDERS OBVIOUS CLAIMS The Combination of Ayzenberg and Janssen Renders Obvious Claims 4-8, 12-15, AND 19-20

A. 1. Discussion of Janssen (EX1009)

161.

Janssen describes connecting “a number of shielded conductor pairs to a board”—such as paddle cards for QSFP connectors—for high-speed data connections. EX1009, Abstract, 1:38-58, 2:39-42; ~~Souri, ¶161.~~ Like Ayzenberg, Janssen describes signal lines comprising “shielded pair[s] of insulated wires 4” wherein ~~“insulation 8” surrounds “data conductors 6.”~~ *Id.*, 5:63-65, Figs. 2, 4. “insulation 8” surrounds “data conductors 6.” *Id.*, 5:63-65, Figs. 2, 4. “[S]hielding 10” comprising “a metal layer (aluminum) and a plastics layer” surrounds each pair of insulated wires. *Id.*, Figs. 2, 4, 5:65-6:2; ~~Souri, ¶161.~~



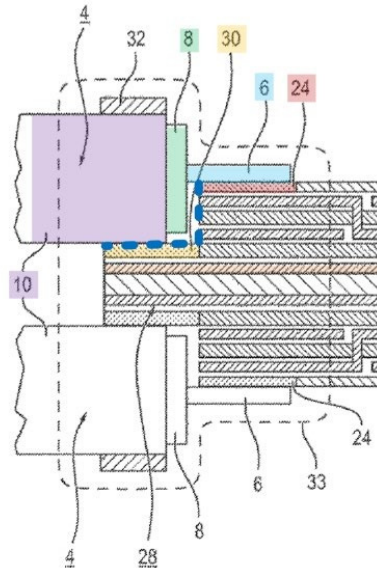
Janssen, Fig. 4

162.

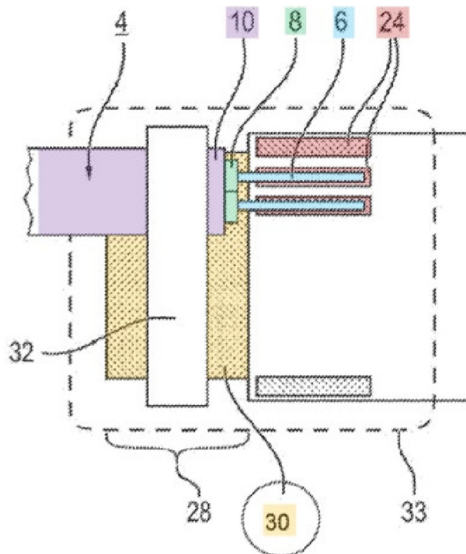
At “high transmission frequency, reliable shielding” and “reliably connect[ing]” such shielding to the board—e.g., reliably grounding the shielding—has “crucial importance.” *Id.*, 1:59-2:1. To reliably connect and ground the

shielding, Janssen teaches a PCB having a “ground contact zone 28” that “projects, in a tongue-like manner, towards the connected conductor pairs.” *Id.*, Figs. 1, 2,

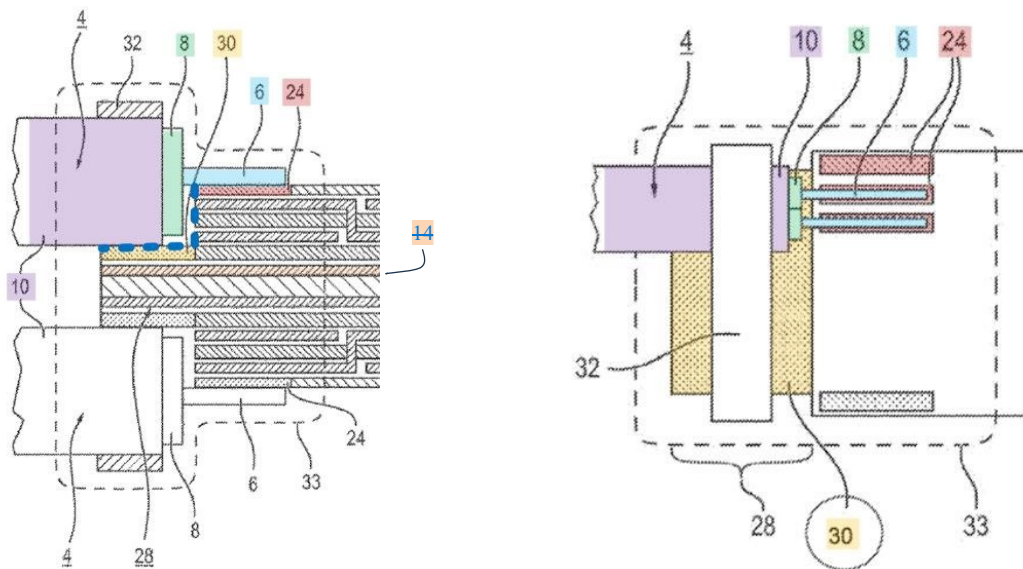
[Abstract, 6:31-33, 6:52-63.](#)



[Abstract, 6:31-33, 6:52-63; Souri,](#)



~~162~~



_____ Janssen, Fig. 1 (excerpt) _____ Janssen, left, excerpted/annotated, Fig. 2 (excerpt)

right, excerpted, annotated) 163. The tongue-like projection defines a recess relative to the PCB surface

(dashed blue line in Fig. 1 profile above) so that “[t]he respective pair of insulated wires 4 rests by the pair shielding 10 on this ground contact zone 28 in a contacting manner” that grounds shielding 10 against metal layer 30 on ground conductor 14. *Id.*, Fig. 1, 6:52-7:18; Souri, ¶163. This disposes the exposed end of “data conductor 6” against connection pad 24, when where it is soldered. *Id.*, Fig. 1, 6:41-44, 7:29-32. 32; Souri, ¶163.

_____ **B.** _____ **2. Discussion of the Ayzenberg+Janssen Combination**

164. Ayzenberg and Janssen both teach connecting multiple shielded wire pairs in a cable to a paddle eardscard used for QSFP connectors.connections

[between electrical devices](#). EX1005, [0045], [0057], [0060], [0087]; EX1009, 7:64-8:16; *supra*

§§VI.A.1 (Ayzenberg), ~~VIII.A~~[VI.C.1](#) (Janssen); ~~Souri,~~

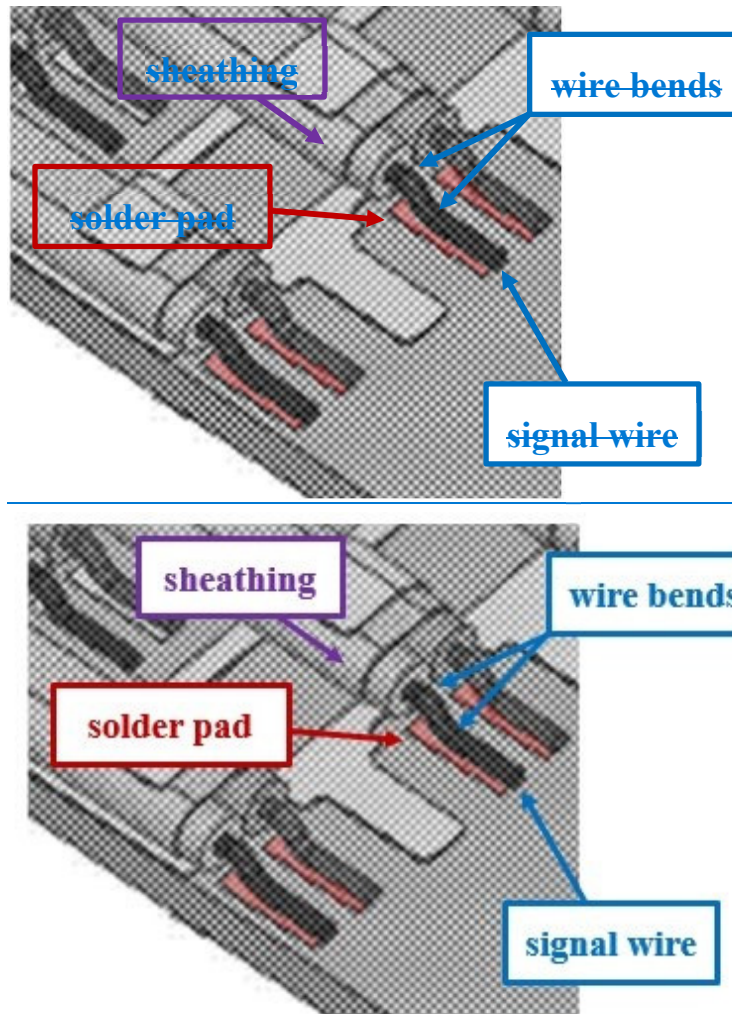
~~¶164.~~

~~_____~~¹ **a. Reasons to Combine**

[165.](#) POSAs would have had several reasons to modify Ayzenberg to use Janssen’s teachings (hereinafter “Ayzenberg+Janssen”). ~~Souri, ¶165.~~

[166.](#) *First*, Ayzenberg teaches placing ~~sheathed~~ cables [with their sheathing](#) on the paddle card surface, ~~which requires bending~~[so that soldering](#) the exposed signal wire ~~when soldered~~ to the PCB [solder pads requires bending the signal wire lead twice](#)—first near the sheathing (e.g., dielectric 906 and shielding 908, *supra* §VI.~~B.3.b~~ (~~{~~[A.2.c.ii \(Limitation \[9A\]\)](#)~~}~~)), and second near the solder pad—to accommodate vertical displacement of the wire from the surface of the solder pad due to the sheathing thickness. E.g., EX1005, [Figs. 6B \(annotated excerpt below\), 9B.](#)

~~Figs. 6B (annotated excerpt below), 9B; Souri, ¶166.~~



Ayzenberg, Fig. 6B
(excerpted, annotated)

POSAs knew that bending the signal wire lead had undesirable effects on signal propagation. E.g., EX1008, 10 (“When discontinuities are introduced in the signal path, taking the form of... bends ..., destructive resonances are introduced. ... [R]esonances can be largely eliminated by design practices[.]”); EX1018, 1:[5245-21](#), 1:60-67 (transitions between electrical conductors like a signal wire to

conductive trace can introduce “impedance... mismatch[]” and “conductor bends to connect to the trace on the PCB... may result in a characteristic mismatch”—e.g., impedance, insertion loss, return loss, or crosstalk—that affects “signal quality”); ~~Souri, ¶167.~~). Notably, these undesirable effects are in part due to the geometry of the bend of the signal wire lead affecting total impedance, in which the loop formed by the wire is subject to Faraday’s law: (i.e., a larger loop area captures more magnetic flux, thus higher inductance and therefore impedance). EX1020, 312-327; ~~Souri, ¶167.~~

167. . In my opinion, POSAs would have used Janssen’s ground contact ~~zone~~pad and connection methodology with Ayzenberg’s outer solder pad ~~rows~~row 422A/ (and 426A-), supra §VI.B.1.e ({A.2.a.v [1D]}), in order to connect signal wire leads to the PCB—e.g., at Ayzenberg solder pad 410/Janssen connection pad 24—without bending the leads, thus mitigating signal discontinuities, “destructive resonances,” and other adverse effects on signal quality from a “characteristic mismatch” introduced by Ayzenberg’s bends. EX1018, 1:5-21, 1:60-67; EX1009, Fig. 1; EX1008, 10; ~~Souri, ¶167.~~

Second, grounding the cable shielding to the paddle card by pressing exposed shields against a ground plane of the paddle card exposed ~~by~~in Janssen’s recess would have simplified Ayzenberg’s manufacture and assembly steps by eliminating the need to provide “ground solder pads 410C” alongside “signal solder pads 410A

and 410B” and any need to physically connect cable grounds to such ground pads for the outer wires. EX1005, [0060] (describing grounds pads);

168. EX1009, 3:1-19 (“use of a ground wire is omitted”), 7:13-18 (simple connection with clamping element 32); ~~Souri, ¶168.~~ In my opinion, POSAs would have known that Janssen’s removing ~~the~~ need to individually contact ground wires “significantly reduced” the “outlay on manufacturing and connection” PCBspaddle boards while increasing “manufacturing reliability” by avoiding common prior art problems with “ground wire short circuits.” EX1009, 2:22-24 (“contact connection is simple to manufacture and... constructed compactly”), 2:43-54; ~~Souri, ¶168.~~

Third, Ayzenberg+Janssen would have combined known components 169. (Ayzenberg’s PCB with Janssen’s recesses and ground contact zone), according to their conventional uses, with predictable results. ~~KSR, 550 U.S. at 416-417; Sourì, ¶169.~~ The combination also would have used Janssen’s known techniques for grounding wires in a recess to improve the grounding of the outer wires on Ayzenberg’s paddle card in the same way. ~~KSR, 550 U.S. at 416-417; Sourì, ¶169.~~

2b. Reasonable Expectation of Success

170. In my opinion, POSAs would have reasonably expected success in applying Janssen’s cable connection teachings to Ayzenberg for the same reasons

they worked in Janssen, and because both Ayzenberg and Janssen are concerned with grounding wires in the same type of high-speed connectors with predictable results. EX1005, [0057]; EX1005, [0057]; EX1009, 2:39-42 (Janssen “suitable” for “all... connectors... equipped with ‘paddle cards’”), 7:64-8:16.

EX1009, 2:39-42 (3. Mapping of Ayzenberg+Janssen “suitable” for “all... connectors... equipped with ‘paddle cards’”), 7:64 to Claims 4-8:16; Souri, ¶, 12-15, and 19-20~~170.~~

C. Analysis

171. Ayzenberg+Janssen renders obvious claims 4-8, 12-15, and 19-20.

a. 1. Claim 4

ai. Limitation [4A]

[4A]: The [PCB] of claim 1, wherein the outer wires each have a sheath with a given thickness adjacent to the exposed end,

Ayzenberg+Janssen meets claim 1 for the same reasons as Ayzenberg alone.

172. *Supra* §VI.B.1; Souri, ¶172.A.2.a.

Ayzenberg+Janssen meets [4A] because both Ayzenberg and Janssen teach that the wires connecting to the PCB—including the “*outer wires*”—“*have a sheath with a given thickness adjacent to*” the signal conductors at “*the exposed end,*” as

shown in Ayzenberg Figs. 9A, 9B and Janssen Fig. 4. *Supra* §VI.B.3.b (A.2.c.ii (Limitation [9A])); EX1005, Figs. 9A, 9B, [0088]-[0089] (“Each signal conductor is surrounded by a dielectric material” which is then “surrounded by a conductive foil.”); EX1009, Fig. 4,

173. 5:63-6:2 (“shielded pair[s] of insulated wires 4” with “data conductors 6 which are in each case surrounded by insulation 8” and “common pair shielding 10.”); Souri, ¶173.”).

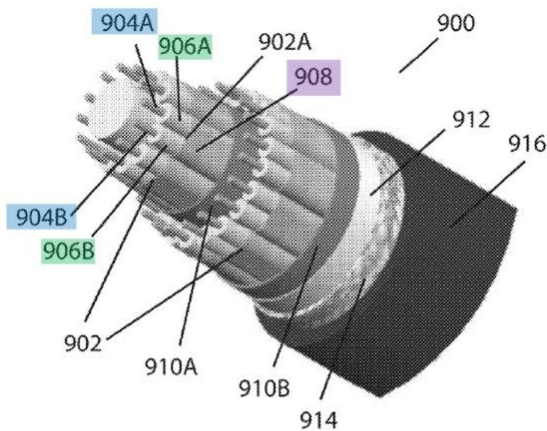


FIG. 9A

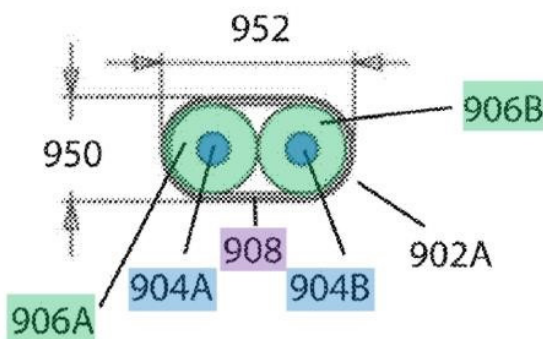


FIG. 9B

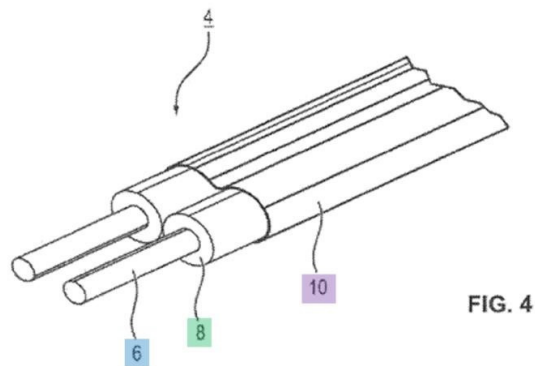


FIG. 4

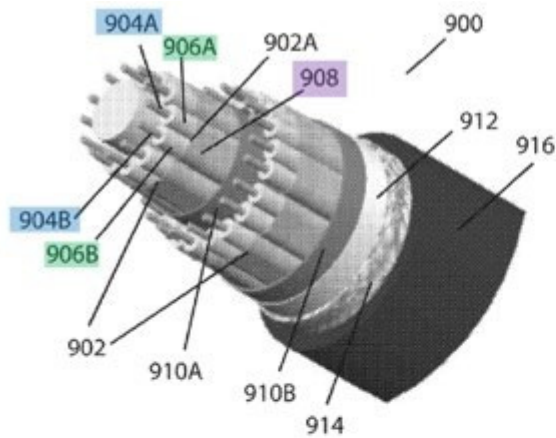


FIG. 9A

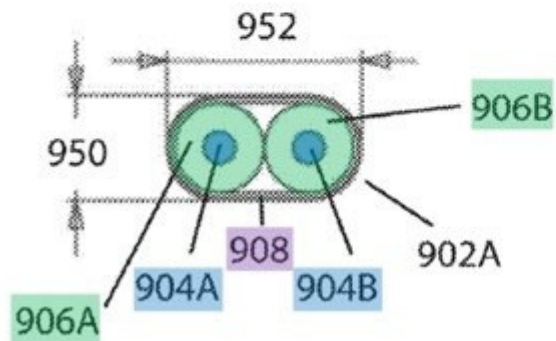


FIG. 9B

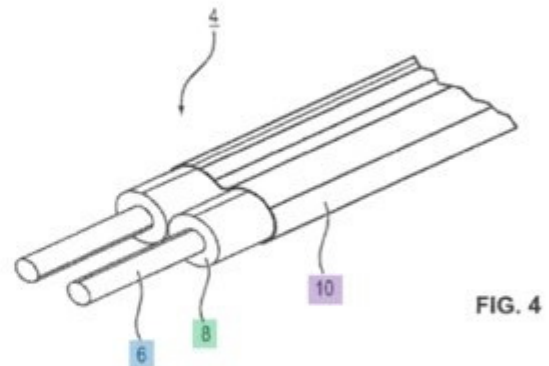


FIG. 4

Ayzenberg, Figs. 9A, 9B (annotated)

Janssen, Fig. 4 (annotated)

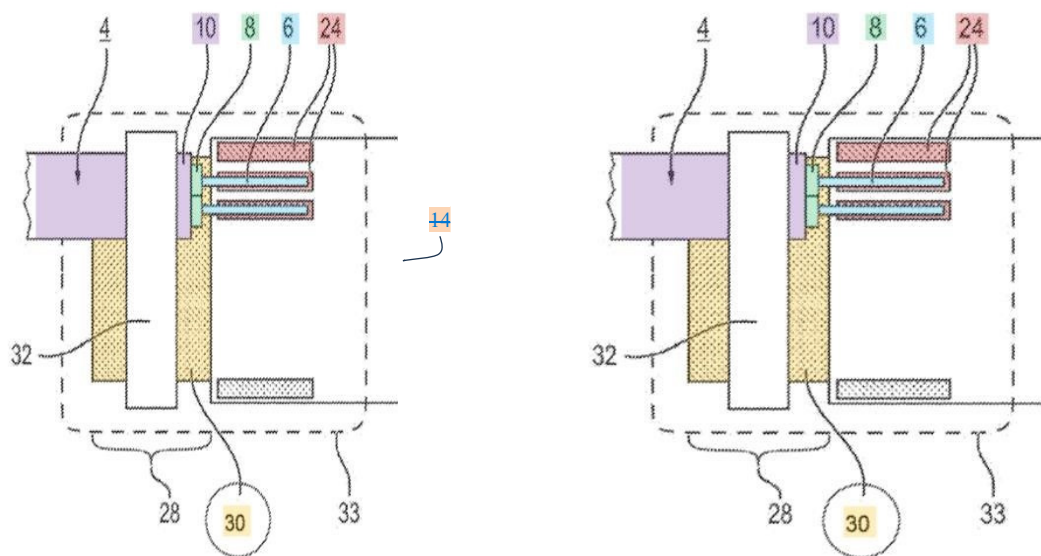
174. Thus, in my opinion, Ayzenberg+Janssen meets Limitation [4A].

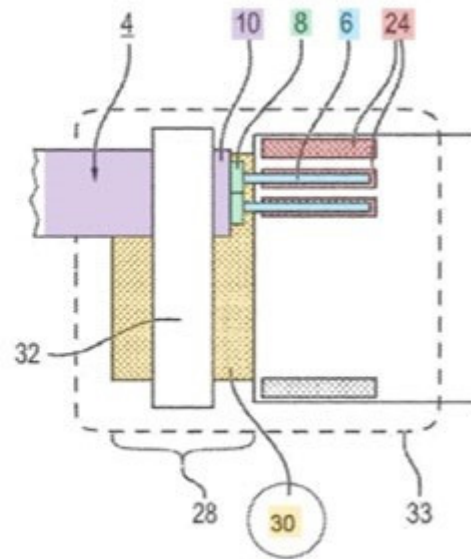
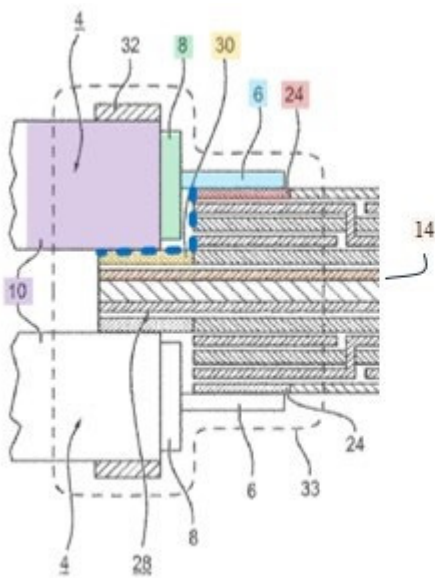
ii. **Limitation [4B]**

[4B]: and wherein the [PCB] further comprises one or more recesses in the at least one surface along each outer wire sheath's path between the second edge and the outer set of electrodes.

Ayzenberg+Janssen meets [4B] because it modifies Ayzenberg's PCB with

175. Janssen's teaching of a "ground contact zone 28" that "projects, in a ~~tongue-like~~tonguelike manner, towards the connected conductor pairs," which forms a "recess" (blue dashed line in Janssen Fig. 1 below)—e.g., "one or more recesses"—in "at least one surface" of Ayzenberg's PCB "along each outer wire sheath's path between the second edge" of Ayzenberg's PCB (*supra* §VI.~~B.1.e~~ ~~(A.2.a.iii (Limitation [1B]))~~ "and the outer set of electrodes" (e.g., solder pads 410 in Ayzenberg row 422A (*id.*)), which accommodates the thickness of the connecting wires' sheaths. *Supra* §~~VIII.A~~VI.C.1 (Janssen); EX1009, Figs. 1, 2, Abstract, 6:31-33, 6:52-7:18; ~~Souri~~, ¶175. Metal 30 provides a surface in the recess that electrically contacts and supports wire shielding 10. *Id.*





Janssen, Fig. 1 (~~excerpt~~)—excerpted, annotated Janssen, Fig. 2 (~~excerpt~~)—excerpted, annotated

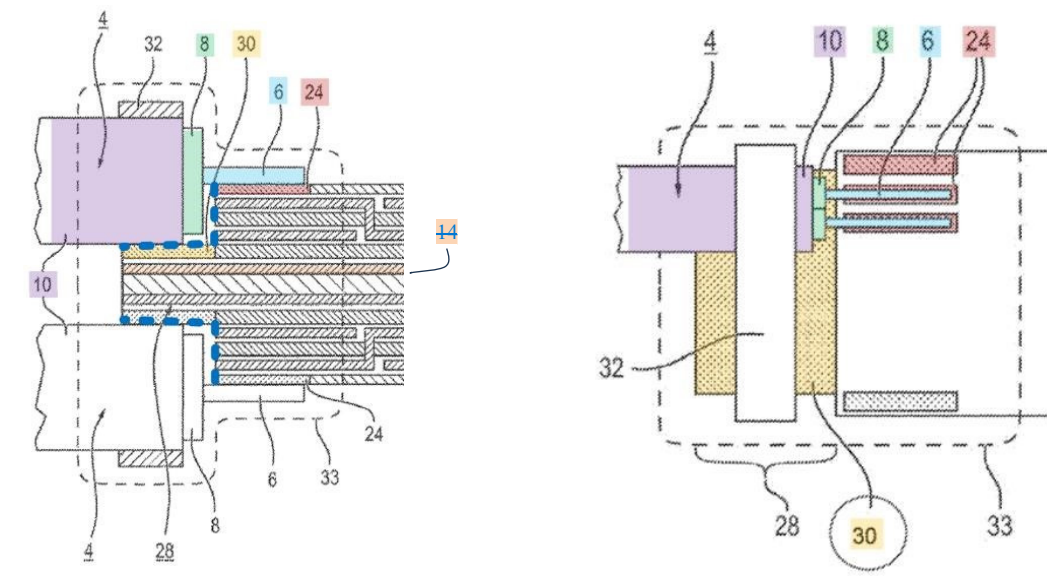
176. Janssen’s Figure 1 shows that ground contact zone 28 is *recessed* in the board “*in the at least one surface along each outer wire sheath’s path between the second edge and the outer set of electrodes*” (i.e., connection pads 24) since “the carrier 12 is extended in a rearward region of the board 2, which region is oriented toward the pairs of insulated wires 4, beyond the rest of the layer structure such that a type of projecting tongue is formed.” EX1009, 6:52-56; ~~Souri,~~ ¶176.

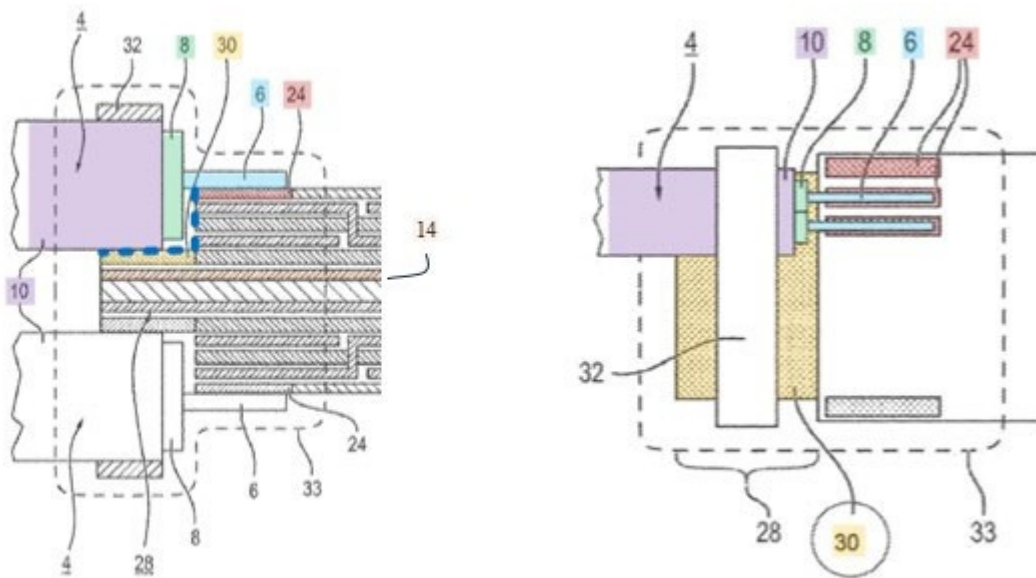
177. —2.— Thus, in my opinion, Ayzenberg+Janssen meets
Limitation [4B].

Claim 5

b. : The [PCB] of claim 4, wherein the one or more recesses each accommodates sheathes of multiple outer wires.

178. Ayzenberg+Janssen renders obvious claim 5 because Janssen describes a “*recess[]*” (dashed blue lines Fig. 1 below) that “*accommodates sheathes of multiple... wires*” (e.g., “a total of eight pairs of insulated wires”) on each side of the PCB, such as, e.g.,—for one surface in Fig. 1—a single wire pair shown in the planar view in Fig. 2. EX1009, 8:8-10; Figs. 1, 2; ~~Souri, ¶178.~~ In Ayzenberg+Janssen each recess accommodates Ayzenberg’s “*outer wires*” as described *supra* §§VI.B.1.c (~~{A.2.a.iii (Limitation [1B])~~), ~~VIII.VI.C.43.a ({i (Limitation [4A])~~). ~~Souri, ¶178.~~





Janssen, Fig. 1 (excerpt) — 1 (excerpted, annotated) Janssen, Fig. 2 (excerpt) 2 (excerpted, annotated) 179. Furthermore, Ayzenberg teaches four “outer wire” pairs (J2, J4, J6, J8) on surface 402 (and pairs J12, J10, J14, J16 on surface 404), and the combination provides a recess accommodating the sheathes of each such wire.

Supra §§VI.B.1.e (A.2.a.iii (Limitation [1B]), VIII.B.VI.C.2 (Ayzenberg+Janssen), VIII.VI.C.1.b (3.a.ii (Limitation [4B])); EX1005, Figs. 4A, 4B; *see also* EX1009, 7:64-8:16 (recess accommodates multiple pairs of insulated wires);).
Souri, ¶179.

180. — 3. — Thus, it is my opinion that Ayzenberg+Janssen meets claim 5.

Claim 6

∴ The [PCB]printed circuit board of claim 4, wherein each outer wire has a corresponding one of the one or more recesses.

c.

181. Ayzenberg+Janssen renders obvious claim 6 because Janssen describes a recess spanning the width of a board surface wherein metal 30 is disposed ~~to support~~ and supports and electrically ~~contact~~ contacts each “outer wire” pair shielding 10.

Supra §§~~VIII~~VI.C.1.b (~~3.a.ii (Limitation [4B])~~), ~~VIII~~VI.C.23.b (claim 5); EX1009, Fig. 2; ~~Souri, ¶181~~2. The “each outer wire” in this embodiment “correspond[s]” to the “recess” because each “outer wire” is disposed in the recess. ~~Souri, ¶181~~. The ’898 patent’s Fig. 10 shows a similar configuration wherein a single recess accommodates multiple wires. EX1001, Fig. 10, 6:17-22 (“[T]he (“In some embodiments, the recesses 730 are broadened as shown in FIG. 10 so that each recess can accommodate sheathes from multiple outer wires. If desired, the recess may extend across the full width of the paddle card to provide a stepped profile next to the outer set of electrodes.”); ~~Souri, ¶181~~.”).

182. Furthermore, ~~POSA~~ in my opinion, a POSA would have known that another predictable design choice was to form a “recess” for each “outer wire” in order to reduce impedance mismatch by controlling the signal characteristics at the transition from signal wire to PCB. ~~Souri, ¶182 (discussing EX1018, Figs. 2, 5, 7, 8, 2:13-44, 2:63-3:5, 3:38-53, 3:644:5). Impedance~~ As stated previously, impedance is directly dependent on the geometry of the bend of the signal wire. ~~Souri, ¶182;~~ in which the loop formed by the wire is subject to Faraday’s law (i.e., a larger loop

area captures more magnetic flux, thus higher inductance and therefore impedance). EX1020, 312-327. For example, Miller (EX1018) teaches that a signal wire's transition from being surrounded by its sheathing to being exposed and attached to a PCB can "result[] in characteristic mismatches that can degrade signal quality" if "not controlled or managed in any of these transitions." EX1018, 2:1-12. Rather than use a single recess as in Janssen, Miller teaches separate recesses (i.e., notches) in a PCB for each wire attached at the edge to control this transition. See, e.g., id., Figs. 2, 5, 7, 8, 2:13-44 ("A notch...has been formed in the substrate, such that the coaxial cable can be positioned to control the signal characteristics in the conductor 22."), 2:63-3:5, 3:38-53, 3:64-4:5. This predictable variation of providing a recess per "*outer wire*" also renders claim 6 obvious. Souri, ¶182. KSR, 550 U.S. at 417 ("If a [POSA] can implement a predictable variation, §103 likely bars its patentability."), 421 (when design need has a finite number of identified predictable solutions using such a predictable solution is obvious); Uber Techs. v. X One, 957 F.3d 1334, 1340-1341 (Fed. Cir. 2020) (simple design choice for desired outcome bars the patentability of each variation).

183. ———4.—— Thus, it is my opinion that Ayzenberg+Janssen meets claim 6.

Claim 7

d. : The [PCB] claim 4, wherein each of the one or more recesses is deep enough to accommodate the given thickness of the sheath, enabling each of the exposed

ends of the outer wires to contact the ~~electrodes in the outer set while remaining parallel to the at least one surface.~~

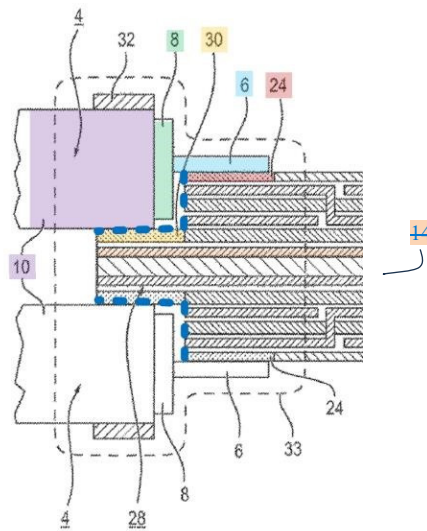
electrodes in the outer set while remaining parallel to the at least one surface.

Ayzenberg+Janssen renders obvious claim 7 because Janssen's tongue-like protrusion forms a "recess" on each surface of the PCB (dashed blue lines in Fig. 1 below). EX1009, Fig. 1; *supra* §§~~VIII~~VI.C.13.a-~~(i~~(Limitation [4A]), ~~VIII~~VI.C.13.a.ii ([4B]), ~~VIII~~VI.C.2

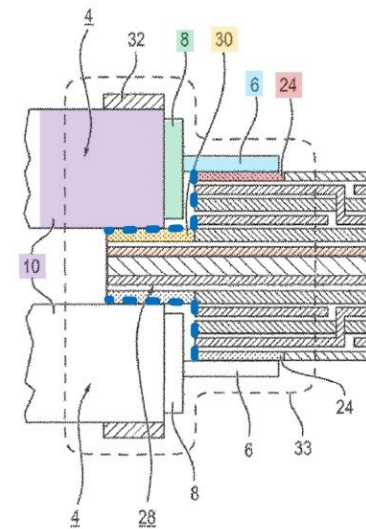
184. 3.b (claim 5); ~~Souri, ¶184.~~). Janssen shows that each recess "*is deep enough to accommodate the given thickness of the sheath*" for each signal wire (e.g., ~~insulator~~insulator 8 and shielding 10) so that the wire lead ("*exposed end of the outer wires*") of each "data conductor 6" is disposed against connection pad 24, where it is soldered. *Id.*, Fig. 1, 6:41-44, 7:29-32; EX1009, Fig. 1; *supra* §VI.C.1 (Janssen).

~~8 and shielding 10) so that the wire lead ("*exposed end of the outer wires*") of each "data conductor 6" is disposed against connection pad 24, where it is soldered.~~

~~EX1009, Fig. 1, 6:41-44, 7:29-32; *supra* §VIII.A (Janssen); Sourì, ¶184.~~



Janssen, Fig. 1 (excerpt)



Janssen, Fig. 1 (excerpted, annotated)

185. Janssen Fig. 1 shows that exposed lead 6 “*remain[s] parallel to the at least one surface*” of the PCB and connection pad 24, disposed in the PCB, to which lead 6 is soldered. ~~Souri, ¶185.~~ Janssen, Fig. 1.

186. Regardless, in my opinion, POSAs would have had reasons to size each recess in order to receive the cable sheathing and dispose the wire lead parallel

to the board surface in order to avoid imparting bends in the wire when contacting the board's solder pad—as shown in Ayzenberg—which were known to introduce undesirable electrical effects. Supra §VI.C.2 (Ayzenberg+Janssen); EX1018, 2:1-26, 3:64-4:5.

187. §VIII.B.1 (Thus, it is my opinion that Ayzenberg+Janssen); EX1018, 2:1-26, 3:64-4:5; Souri, ¶186. meets claim 7.

5e. Claim 8

ai. Preamble [8PRE] and Limitation [8A]

~~[8PRE] The [PCB] of claim 7, further comprising a second surface having:~~

~~[8A] a second outer set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed outer wires;~~

i. [8PRE]: The [PCB] of claim 7, further comprising

[8A]: a second surface having: a second outer set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed outer wires;

(1) “for attaching...”

188. The I have been informed by counsel that the “for attaching...”

language in [8A] is non-limiting. Supra §§VI.B.1-bA.2.a.ii ((Limitation [1A])),

VI.B.1.c.i(3) (A.2.a.iii

(Limitation [1B]); Boehringer, 320 F.3d at 1345.]). Regardless, if it is construed as limiting, then

Ayzenberg+Janssen meets or suggests it as shown below. [Souri, ¶188.](#)

ii. (2) Analysis

189. Ayzenberg+Janssen meets [8PRE] because it renders obvious claim 7

(*supra*

[§VIII§VI.C.43.d](#)) and, as discussed *supra* [1B], Ayzenberg's paddle card has surfaces on each side (i.e., "*a second surface*"). *Supra* [§VI.B.1.c](#) ([\[1B\]](#)); [EX1005, Figs. 4A, A.2.a.iii \(Limitation](#)

[\[1B\]](#)); [EX1005, Figs. 4A and 4B](#), [0058] ("FIG. 4A is a plan view of a first side 402 of an exemplary paddle card 400, and FIG. 4B is a plan view of the opposite side 404 of the exemplary paddle card 400."); [Souri, ¶189.](#)).

The second surface of Ayzenberg's paddle card has "*a second outer set of electrodes*" (as recited in [8A]) for signal wire pairs J12, J10, J14, and J16 in row

190. 426A that are
"*arranged parallel to the second edge for attaching exposed ends of sheathed outer wires.*" *Supra*

[§VI.B.1.c](#) ([\[A.2.a.iii \(Limitation \[1B\]\)](#)]; [EX1005,](#)

[Fig. 4B](#), [0060]; [Souri, ¶190.](#)].

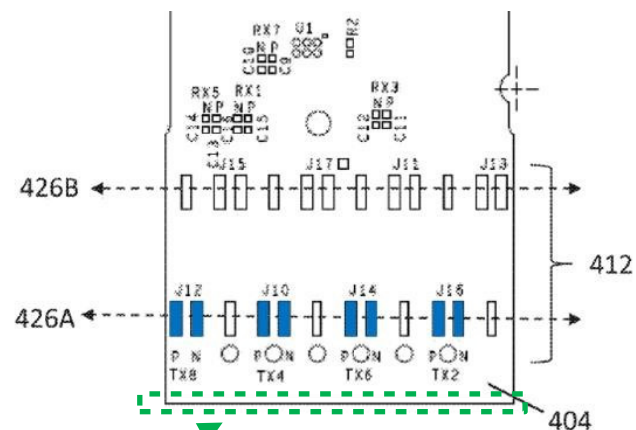
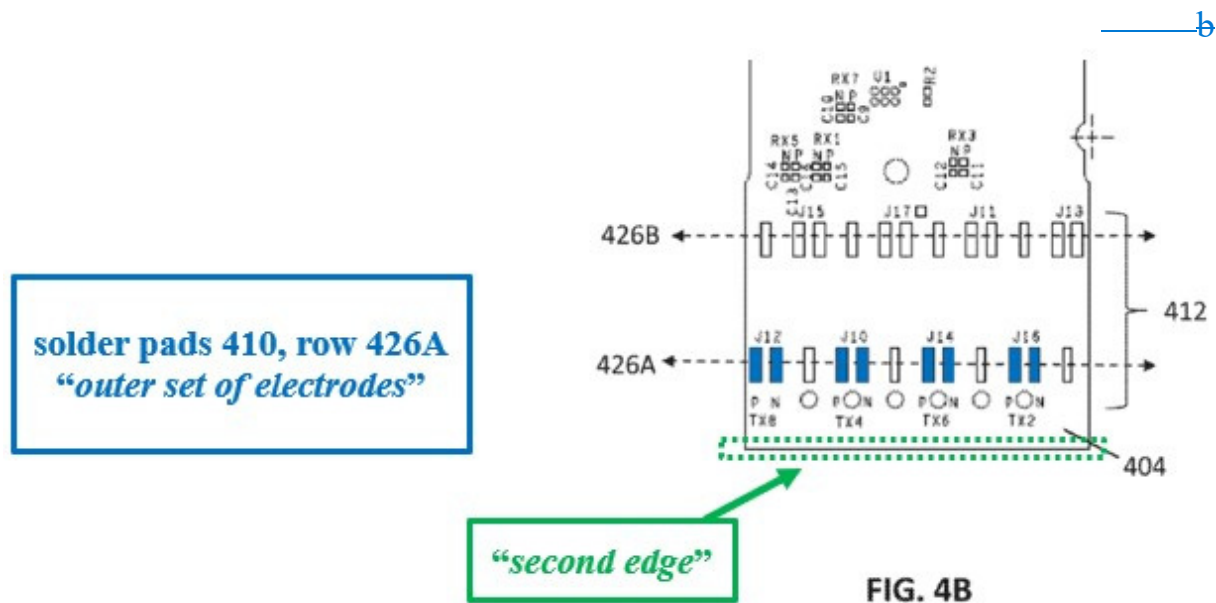


FIG. 4B

solder pads 410, row 426A "*outer set of electrodes*"



Ayzenberg, Fig. 4B (excerpted and annotated) 191. Thus, it is my

opinion that Ayzenberg+Janssen meets Preamble

[8PRE] and Limitation [8A].

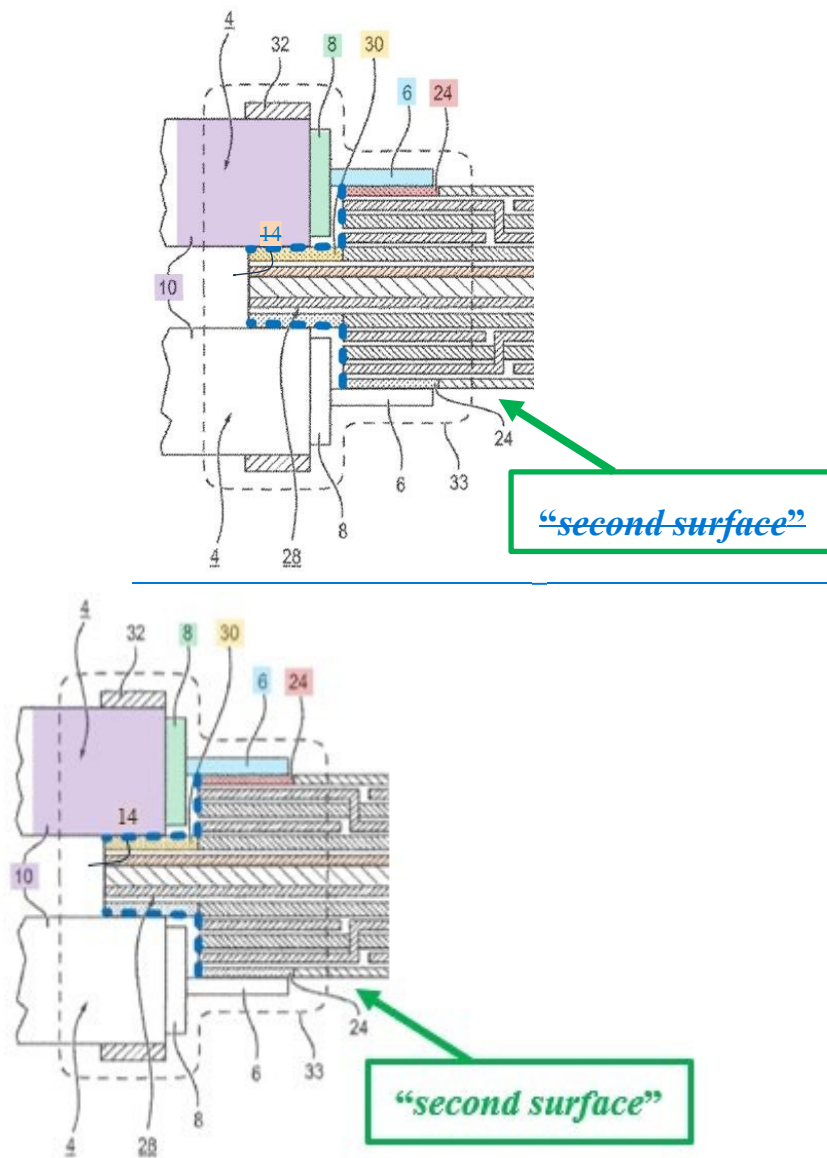
ii. **Limitation [8B]**

[8B]: and one or more recesses in the second surface extending along a path of each sheathed outer wire's sheath between the second edge and the second outer set of electrodes.

192.

Ayzenberg+Janssen meets [8B] because Janssen teaches a recess (bordered by dashed blue outline below) on each side of a PCB—e.g., on a “second surface” of the PCB—including the surface of contact 24 that is recessed flush in the PCB as shown in Figure 1 (below). *Supra* §§~~VIII.C.1.b~~ (~~VI.A.2.a.iii~~ (Limitation [4B])), ~~VIII~~VI.C.23.b (claim 5);

EX1009, 6:57-60 (“The carrier 12 forms a ground plane 26 with the ground conductor 14. The projecting partial region forms a ground contact zone 28 of the ground plane 26.”); [Souri, ¶.192](#).



Janssen, Fig. 1 (excerpt)

Janssen, Fig. 1 ([excerpt](#))
[excerpted and annotated](#))

When Janssen’s ground contact zone (i.e., recess) teachings are applied to

193. Ayzenberg’s paddle card, ~~POSA~~ Asa POSA would have recognized that, as discussed *supra* § ~~VIII~~ VI.C.1.b (~~{3.a.ii~~ (Limitation [4B])), the “*recess[] in the second surface extend[s] along a path of each sheathed outer wire's sheath between the second edge and the second outer set of electrodes.*” ~~Souri, ¶193.~~

194. ~~_____~~ 6 Thus, it is my opinion that Ayzenberg+Janssen meets Limitation [8B].

_____ **f. Claims 12 and 19**

Claim 12: The cable of claim 9, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes.

Claim 19: The method of claim 18, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes, each of the recesses being deep enough to accommodate a full thickness of the sheath near the unsheathed end.

195. Claims 12 and 19 depend from claims 9 and 18, respectively.

196. Ayzenberg+Janssen meets claims 9 and 18 for the reasons that Ayzenberg alone meets claims 9 (*supra* § VI.B.3A.2.c) and 18 (*supra* § VI.B.6A.2.f), respectively. ~~Souri, ¶196.~~

197. The additional limitations in claims 12 and 19 are similar to the additional limitations in claim 7 and [4B]. EX1013, 3; ~~Souri, ¶197.~~

Ayzenberg+Janssen meets the remaining limitations in claims 12 and 19 for reasons that Ayzenberg+Janssen meets claim 7 (depending on claim 4). *Supra*

§§~~VIII~~VI.C.~~43~~d (claim 7), ~~VIII~~VI.C.~~43~~a (claim 4); ~~Souri, ¶197.~~.

Ayzenberg+Janssen further meets the additional limitations in claims 12 and 19,

and renders each claim obvious, because Ayzenberg teaches soldering signal wire

leads to the outer row of signal solder pads 410 on surface 402~~/~~ and 406

(e.g., providing “*sheathed wires attached to the outer set of electrodes*”). EX1005,

Figs. 6A, 6B, [0073] (“[T]he ends of the signal wires are soldered to respective

signal solder pads.”); ~~Souri, ¶197.~~”).

7198. Thus, it is my opinion that Ayzenberg+Janssen meets claims 12 and 19.

g. **Claims 13-15 and 20**

Claim 13: The cable of claim 12, wherein the one or more recesses each accommodates sheathes of multiple sheathed wires.

Claim 14: The cable of claim 12, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more recesses.

Claim 15: The cable of claim 12, wherein each of the one or more recesses is deep enough to accommodate a full thickness of the sheath near the unsheathed end, enabling each of the unsheathed ends of the wires attached to the outer set of electrodes to contact those electrodes while remaining parallel to the at least one surface.

Claim 20: The method of claim 19, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more recesses. 199. Claims 13-15 depend from claim 12, and claim 20 depends from claim 19. Ayzenberg+Janssen meets claims 12 and 19. *Supra* §~~VIII~~VI.C.6; ~~Souri~~, ¶1993.f.

200. Ayzenberg+Janssen meets the additional limitations in claims 13-15 and 20, and renders those claims obvious, for the reasons it meets the corresponding limitations in claims 5-7 as shown below. EX1013, 4-5; ~~Souri~~, ¶200.

Claim	Corresponding claim	Discussion <i>supra</i>
13	5	§ ~~VIII~~ <u>VI</u> .C.23.b
14, ~~20~~	6	§ ~~VIII~~ <u>VI</u> .C.3.c
15	7	§ ~~VIII~~ <u>VI</u> .C.43.d
<u>20</u>	<u>6</u>	§ <u>VI</u> .C.3.c

201. ~~IX. GROUND~~ Thus, it is my opinion that Ayzenberg+Janssen meets claims 13-15 and 20.

D. Ground 4: ALDEN ANTICIPATES AND/OR RENDERS OBVIOUS CLAIMS Alden Anticipates and/or Renders Obvious Claims 1, 2, 9, 10, 16, ~~AND~~and 18

A. ———— 1. Discussion of Alden (EX1006)

202. Alden (EX1006) concerns an “electrical connector ~~include[ing]~~[that] includes a circuit board” and specifically to “an electrical connector within which the circuit board and wire assembly” are used in “a high-speed input/output (I/O) connector.” EX1006, Abstract, [0016]. The circuit board includes “a mating region 60 that defines a portion of the card edge that mates with the complementary



FIG. 3

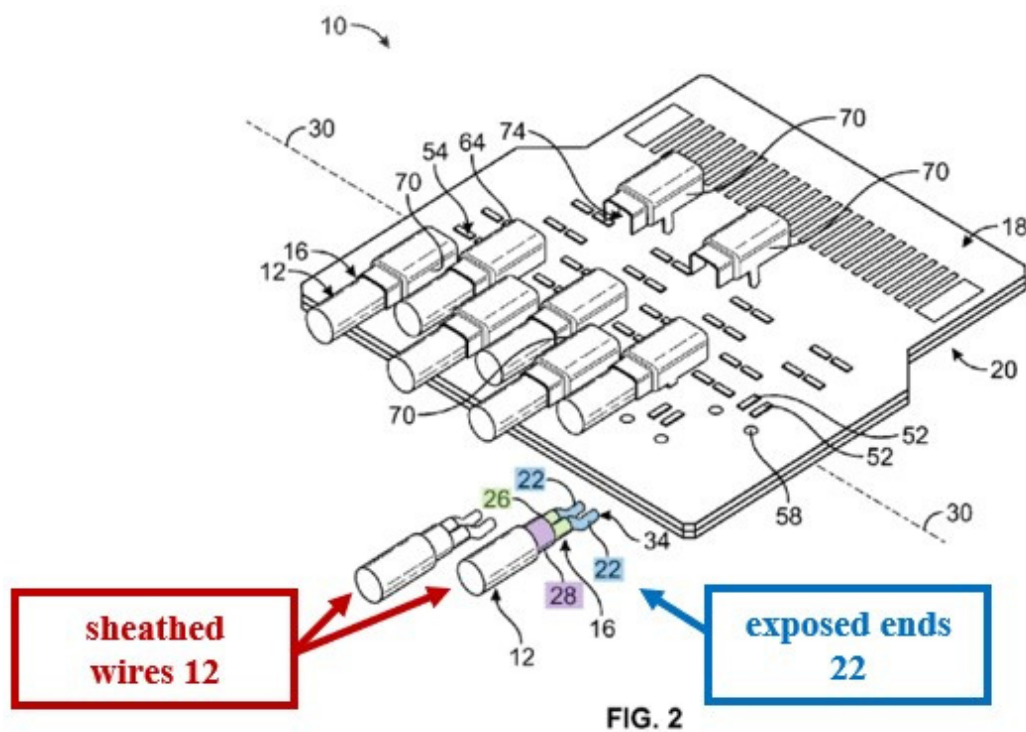
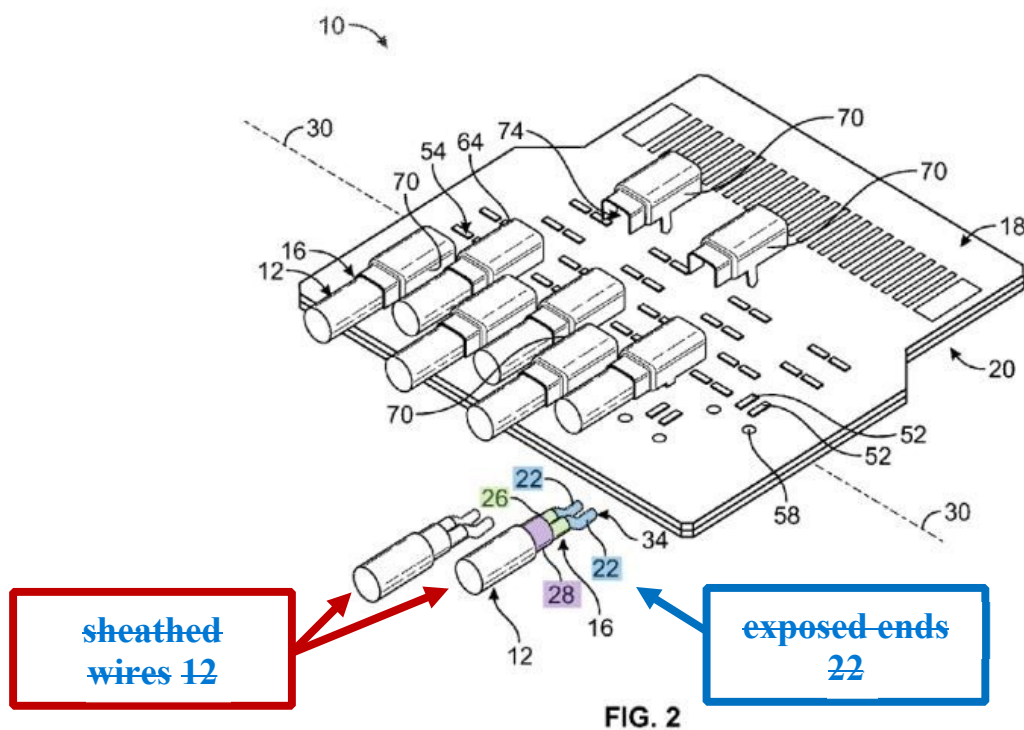


FIG. 3

Alden, Fig. 3 (annotated)

end segment 34 of a signal conductor 22” that are exposed from sheathing

~~“insulating members 26” and “ground conductor 28” (e.g., shielding). *Id.*, [0018], [0029], Fig. 2; Sourin, ¶¶202-2032.~~



Alden, Fig. 2 (annotated)

204. The signal conductors are included in “electrical wires 12” ~~(e.g.,” such as, for example,~~ wires in a twin axial cable~~),~~ where “each electrical wire “12 includes a differential signal pair of signal conductors 22.” *Id.*, [0017]. Each signal conductor is sheathed, ~~e.g.,for example,~~ surrounded by an “insulating member 26” ~~and,” which is also surrounded by~~ “a ground conductor 28 that extends around the insulating member.” *Id.*, [0018], Fig. 2; ~~Souri,~~ ¶204.

B. Analysis2. Mapping of Alden to claims 1, 2, 9, 10, 16, and 18

Alden anticipates and/or renders obvious claims 1-2, 9-10, 16, and 18.

Realtime Data, 912 F.3d at 1373.

~~1.~~ ~~a.~~ **Claim 1**

~~i.~~ ~~a.~~ **Preamble [1PRE]: A printed circuit board that comprises at least one surface having:**

205. Alden meets [1PRE] because it teaches “a circuit board 14” (a PCB) “that terminates ends 16 of electrical wires 12.” EX1006, [0016], Fig. ~~4;~~ ~~Souri,~~ ¶2051.

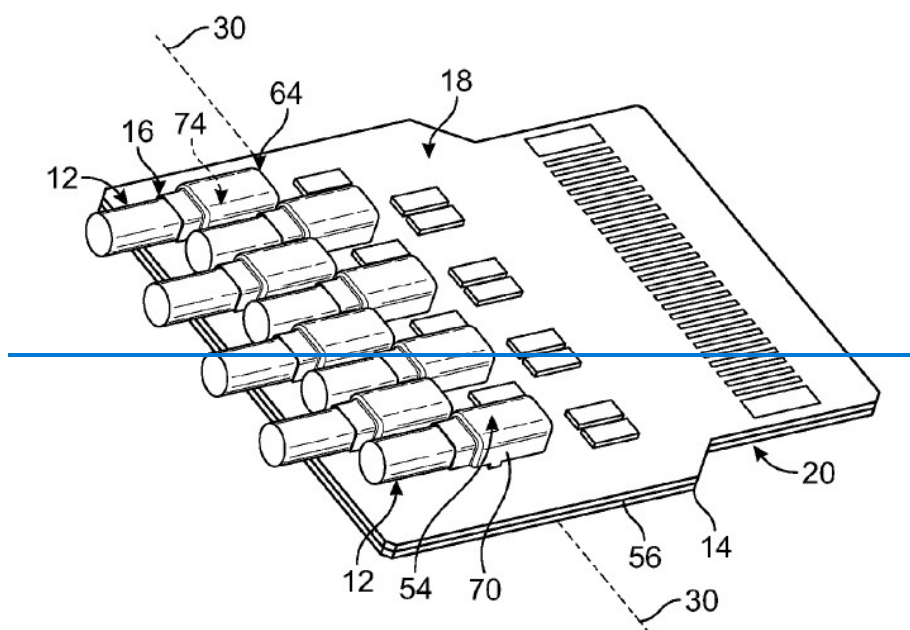


FIG. 1

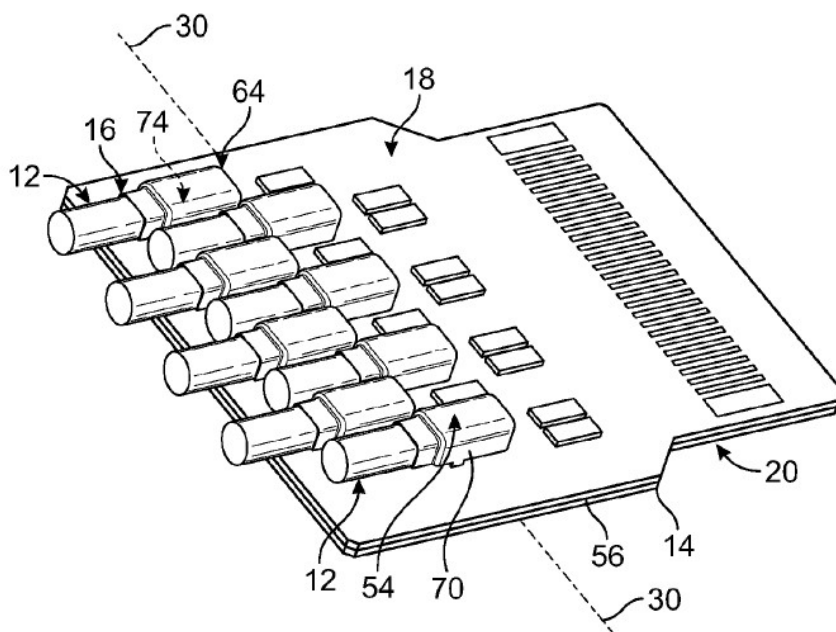


FIG. 1

[Alden, Fig. 1](#)

206. Circuit board 14 “*comprises at least one surface*” because it “includes the exterior sides 18 and 20.” EX1006, [0020], Fig. ~~1~~; ~~Souri, ¶2061.~~

~~—— b. Limitation [1A]~~ **ii. Limitation [1A]: edge connector traces arranged along a first edge for contacting electrical conductors in a socket connector;**

207. Alden meets [1A] because circuit board 14 includes “*edge connector traces*” represented as “a mating region 60 that defines a portion of the card edge that mates with the complementary mating connector.” EX1006, [0025]; ~~Souri, ¶207.1.~~

208. While the intended use “*for contacting electrical conductors in a socket connector*” is not limiting (*supra* §VI.~~B.1.b~~A.2.a.ii (Ground 1, Limitation [1A])),

Alden nonetheless meets it because mating region 60 includes mating pads 62 that “mate with corresponding mating contacts (not shown) of the complementary mating connector to establish an electrical connection between the circuit board 14 and the complementary mating connector.” EX1006, [0025]; ~~Souri, ¶208.1.~~

209. In my opinion, POSAs would have recognized from the shape of mating region 60, Alden’s description of its function (EX1006, [0025]) and use in high speed I/O connectors (EX1006, [0016])—which were known to mate with socket connectors—that the mating pads 62 are “*for contacting electrical*

conductors in a socket connector.” ~~Souri, ¶209.~~ Regardless, ~~POSA~~ in my opinion, a POSA would have understood that the conventional and obvious use of Alden’s high-speed I/O connectors was to contact electrical conductors in a socket connector.” ~~Supra §VI.B.1.b (Ground 1, A.2.a.ii (Limitation [1A], discussing “socket connector”); Souri, ¶209.)~~.

The mating region 60 is “*arranged along a first edge*,” i.e., mating end 42,

210. “wherein the circuit board 14 mates with a mating connector (not shown).”

EX1006, [0020], [0025], Fig. 3 (annotated below); ~~Souri, ¶210.~~

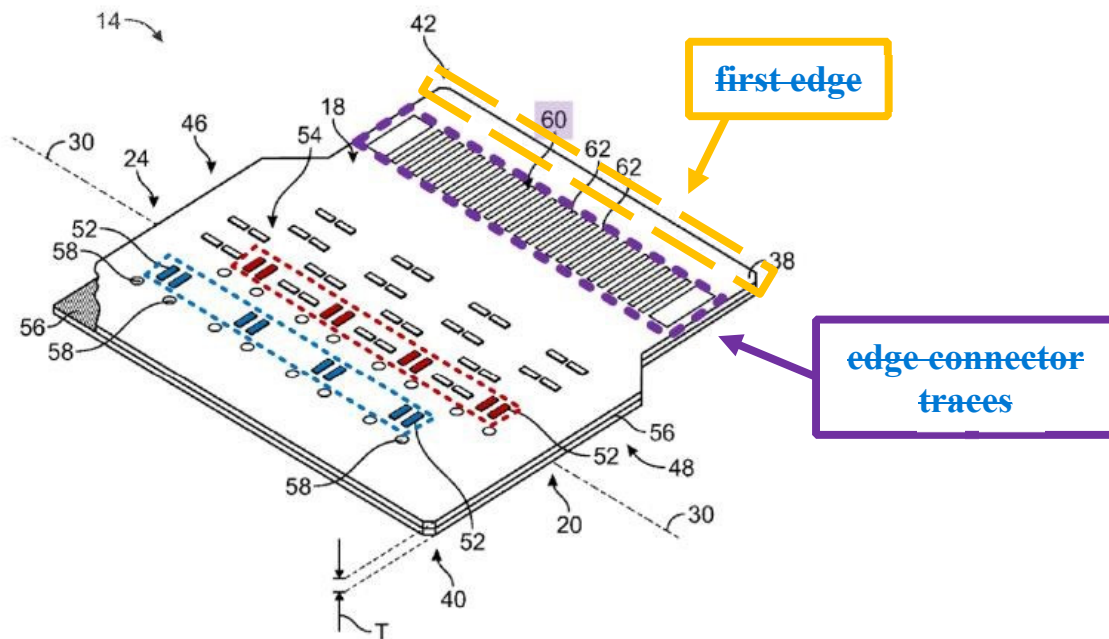
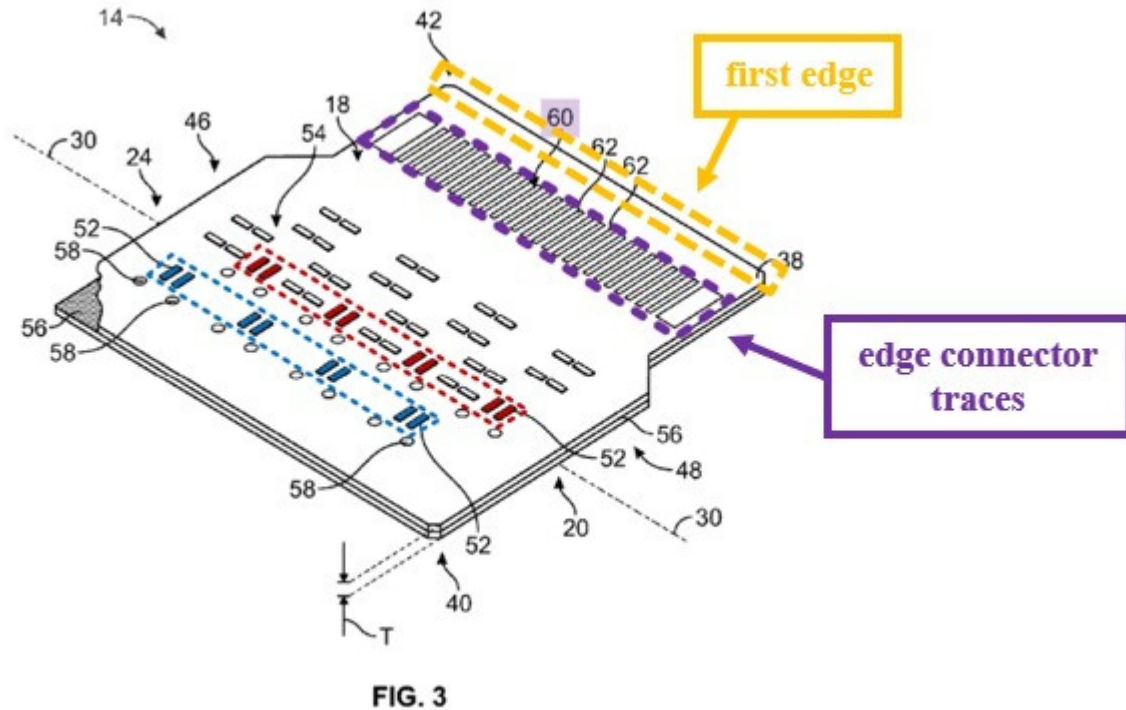


FIG. 3



Alden, Fig. 3 (annotated)

211. Thus, it is my opinion that Alden meets Limitation [1A].

iii. Limitation [1B]: an outer set of electrodes arranged parallel to a second edge for attaching exposed ends of sheathed wires in a cable (“outer wires”);

Alden meets [1B] because circuit board 14 includes a “set of electrodes arranged parallel to a second edge” represented in ~~Figure~~Fig. 3 as “mounting pads 52 to which the electrical wires 12 are terminated.” EX1006, [0021]; ~~Souri, ¶212.~~]. The mounting pads 52 on Alden’s circuit board “are arranged in a row 24 that extends a length along a row axis

215. Alden describes wires 12 “*in a cable*” comprising “two signal conductors 22... that are arranged side-by-side, such that each electrical wire 12 is what is commonly referred to as a ‘twinax cable’ or a ‘twinaxial cable’.” EX1006, [0017]. The wires in Alden’s twinaxial cables are “*sheathed*.” EX1006, Fig. 2, [0018]-[0019] (insulator 26, conductor 28); ~~see e.g.,~~ EX1001, 3:14-17 (~~describing that twinaxial cables have~~ “(“The electrical conductors may be individually and (optionally) collectively shielded, having grounded conductive sheaths... like coaxial or twinaxial cables to reduce signal crosstalk”); ~~Souri, ¶215.~~”).

216. Alden further teaches that mounting pads 52 are used for “*attaching exposed ends*” of electrical wires 12. EX1006, [0019] (“The exposed end segments 34 enable the electrical wires 12, and specifically the electrical signal conductors 22, to be mounted to mounting pads 52 of the circuit board 14.”); ~~Souri, ¶216.~~”).

217. Thus, Alden teaches “an outer set of electrodes arranged parallel to a second edge for attaching exposed ends of sheathed wires in a cable (‘outer wires’).” ~~wires’).” Souri, ¶217.~~

218. ~~—d.—~~ ~~Limitation [1C]~~ Thus, it is my opinion that Alden meets Limitation [1B].

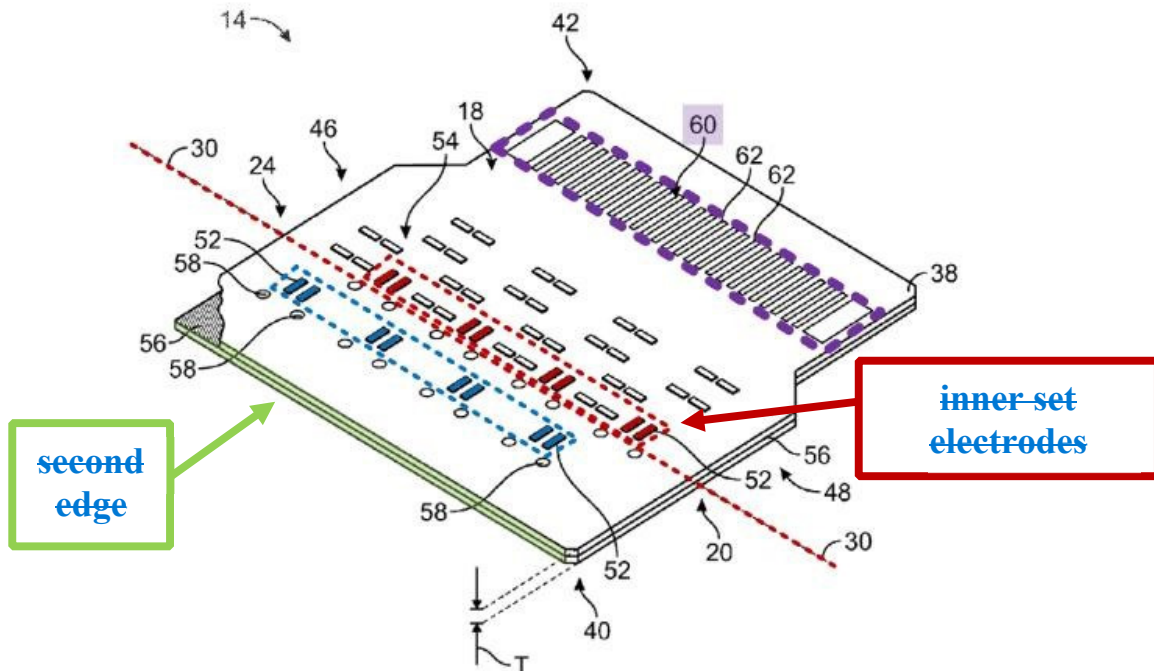
iv. Limitation [1C]: and an inner set of electrodes arranged parallel to the second edge for attaching

exposed ends of sheathed wires in a cable (“inner wires”).

219. Alden meets [1C] because circuit board 14 includes a “set of electrodes arranged parallel to the second edge” shown in Fig. 3 as “mounting pads 52.” EX1006, [0021]; *supra* §IX.B.1.e ([1B]); ~~Souri, ¶219.~~ VI.D.2.a.iii (Limitation [1B]).

220. The “mounting pads 52 within the row 24”—which “are staggered on” the side “of the row axis 30” (EX1006, [0021]) closer to the mating end 42—are an “inner set of electrodes.” *Supra* §IX.B.1.e (~~VI.D.2.a.iii (Limitation [1B])~~); EX1001, 4:51-59, Fig. 3 (inner set 306); ~~Souri, ¶220.~~

4:51-59, Fig.



3 (inner set 306).

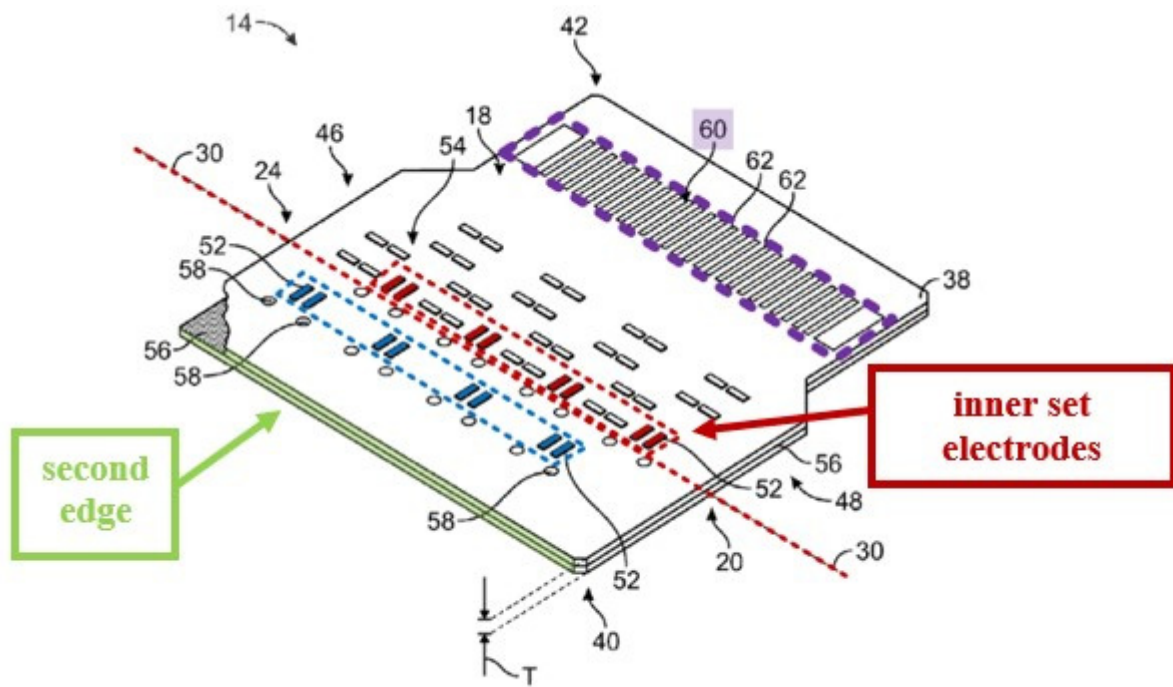


FIG. 3

Alden, Fig. 3 (annotated)

Like the “outer set” *supra* §IX.B.1.e (VI.D.2.a.iii (Limitation [1B])), the “inner set” of mounting pads 52 are used for the non-limiting intended purpose of “attaching exposed ends of sheathed wires in a cable.”

221. EX1006, [0017], [0019], Fig. 8; Souri, ¶221.

Fig. 8.

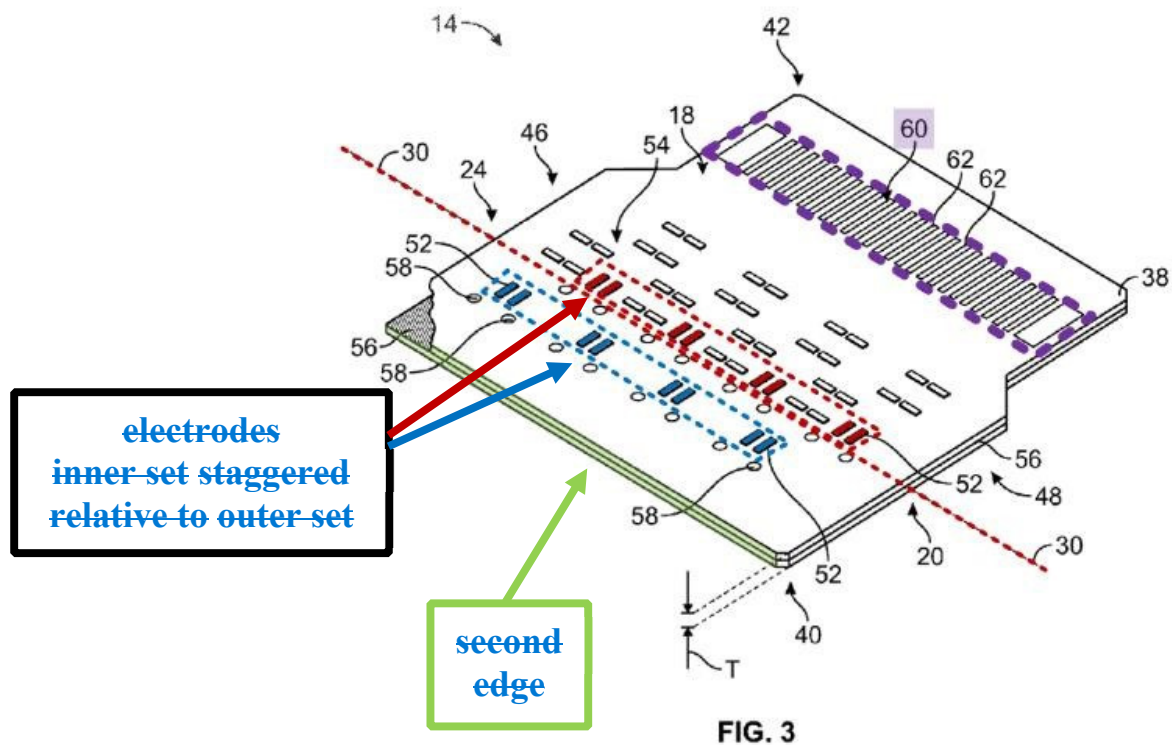
222. Thus, it is my opinion that Alden meets Limitation [1C].

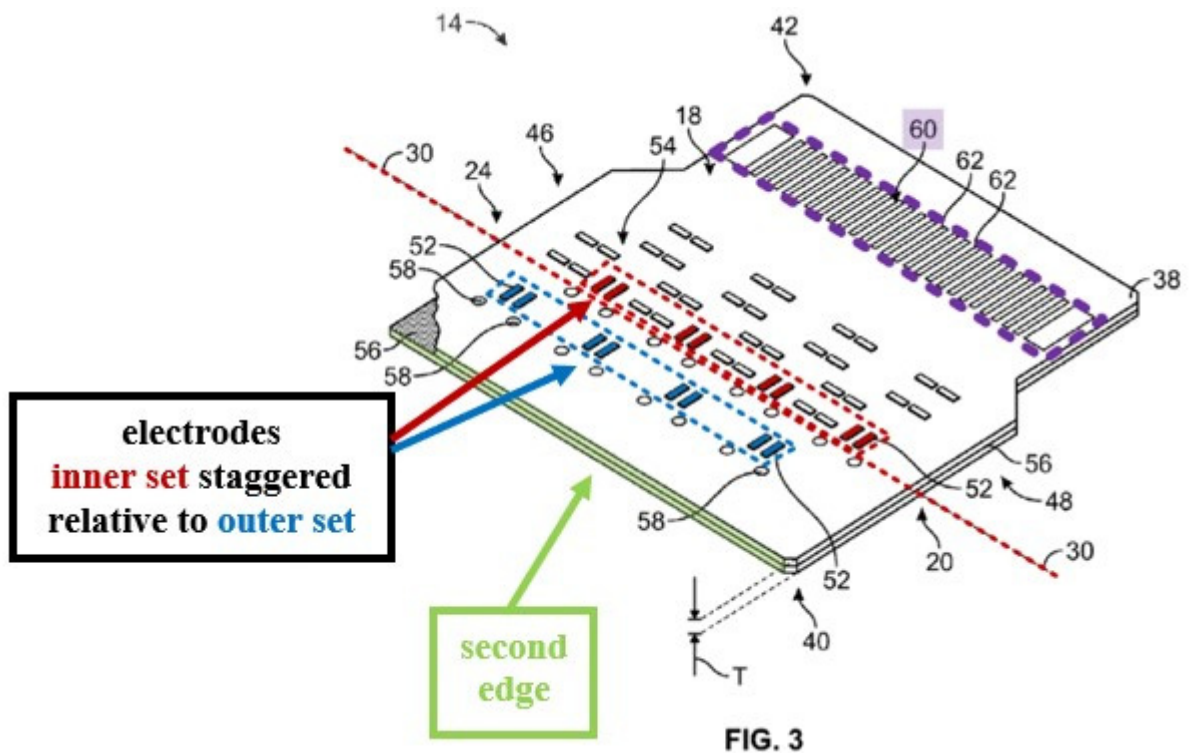
v. Limitation [1D]: with the electrodes in the inner set being staggered relative to the electrodes in the outer set.

223. Alden meets [1D] because Alden teaches *outer* and *inner sets* of electrodes represented in Figure Fig. 3 (annotated below) as “adjacent pairs of

mounting pads 52 within the row 24 [that] are *staggered on respective opposite sides of the row axis 30.*" EX1006, [0021]; *supra* §§VI.D.2.a.iii (Limitation [1B]), VI.D.2.a.iv (Limitation [1C]).

~~30."~~ EX1006, [0021]; ~~*supra* §§IX.B.1.c ([1B]), IX.B.1.d ([1C]); Sourin, ¶223.~~





Alden, Fig. 3 (annotated)

224. Thus, Alden teaches mounting pads 52 “in the inner set being staggered relative to the electrodes in the outer set.” Souri, ¶224.

225. ———2Thus, it is my opinion that Alden meets Limitation [1D].

b. **Claim 2-: The printed circuit board of claim 1, with the electrodes in each of the inner and outer sets being spaced to enable the inner wires to pass between the outer wires while maintaining contact with the at least one surface.**

226. Alden meets claim 2 because Alden’s *outer* and *inner* mounting pads

52 are *staggered relative* to each other as shown *supra* §IX.B.VI.D.2 (f.a.v (Limitation [1D])). Souri, ¶226.

Alden, Fig. 2

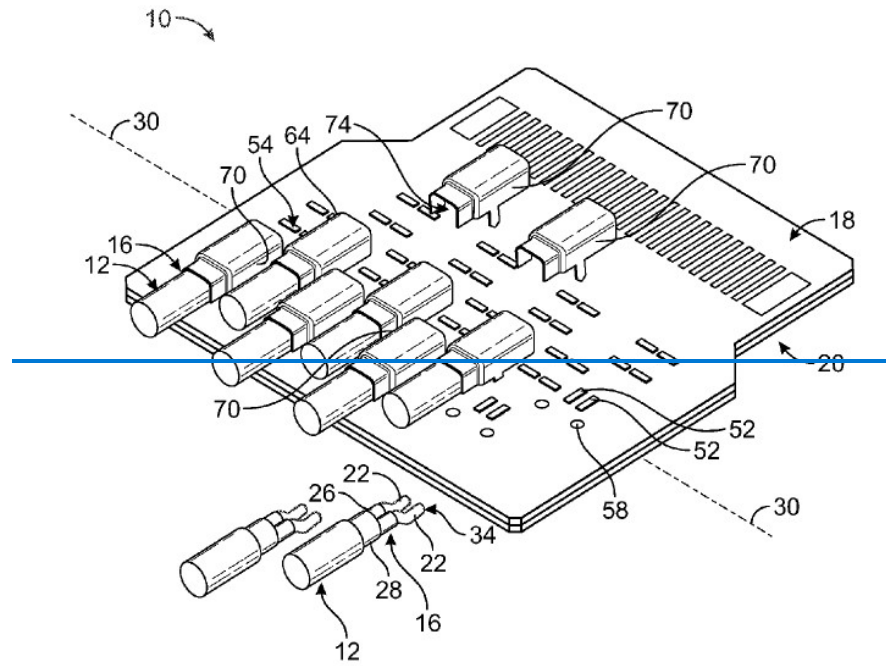
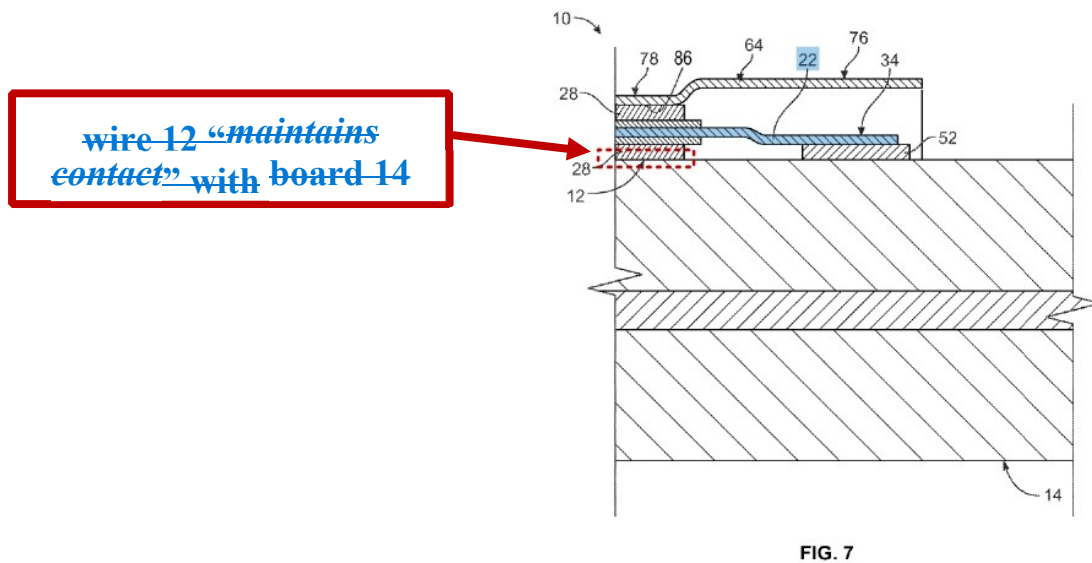


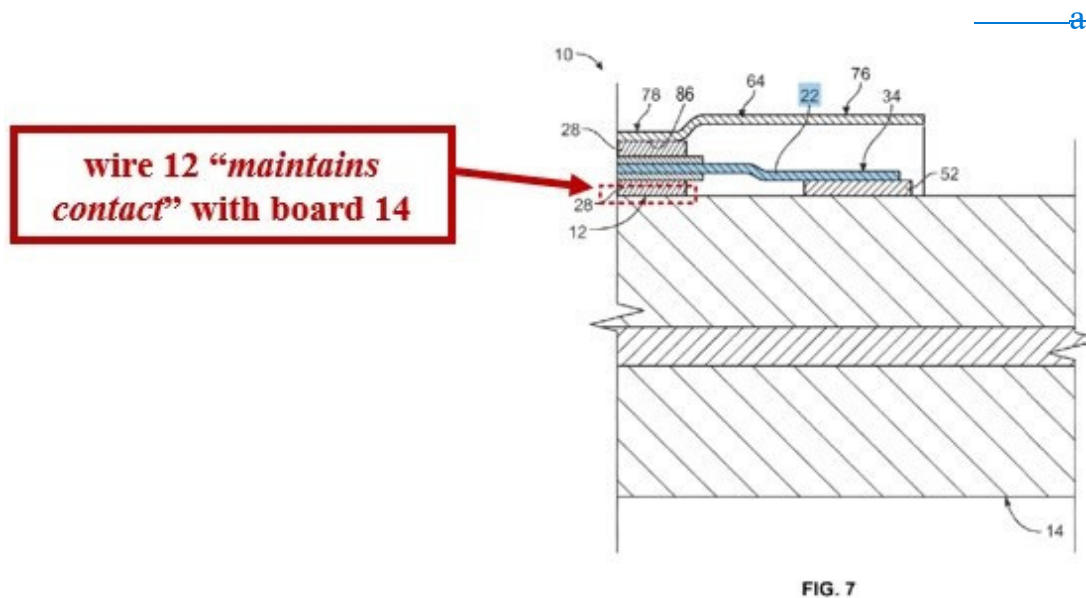
FIG. 2

227.

Figure 7 (below) shows Alden's wire 12 *maintaining contact* with the surface of circuit board 14, wherein the exposed wire end 34 is slightly bent and mounted to mounting pad 52 while wire 12 maintains contact with the surface of the circuit board 14. ~~Souri, ¶227.~~



3. Claim 9



Alden, Fig. 7 (annotated)

228. Thus, it is my opinion that Alden meets claim 2.

c. Claim 9

i. Preamble [9PRE]-]: A cable that comprises:

229. Alden meets [9PRE] because it teaches “two or more electrical wires... grouped together in a cable” wherein the cable’s electrical wires are terminated on PCB 14 enclosed in connector 100. EX1006, Fig. 8 (connector 100), [0002], [0005], [0007], [0016], [0035], [0037] (“electrical wires 12 are... twinax cables”).

~~PCB 14 enclosed in connector 100. EX1006, Fig. 8 (connector 100), [0002], [0005], [0007], [0016], [0035], [0037] (“electrical wires 12 are... twina~~x cables”);

~~Souri, ¶229.~~

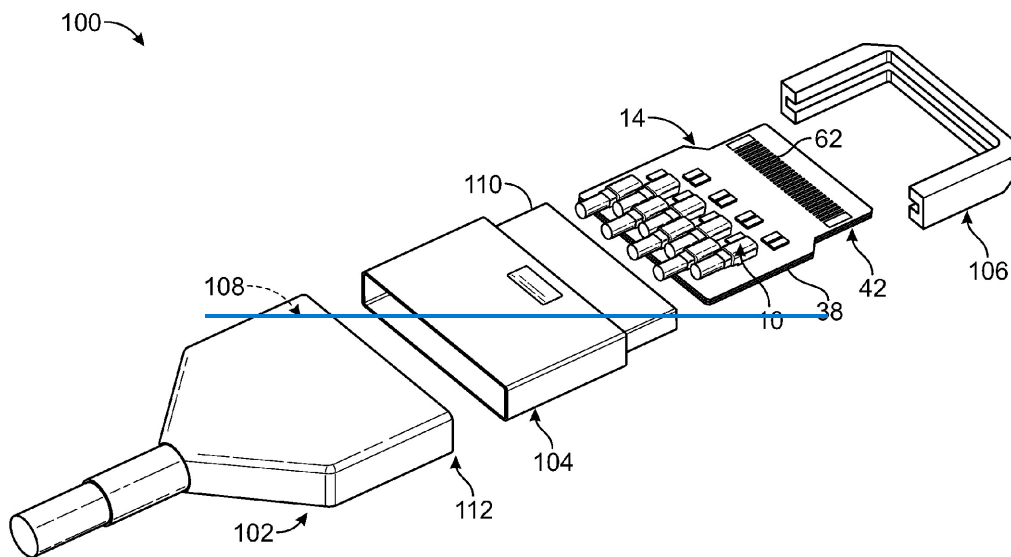


FIG. 8

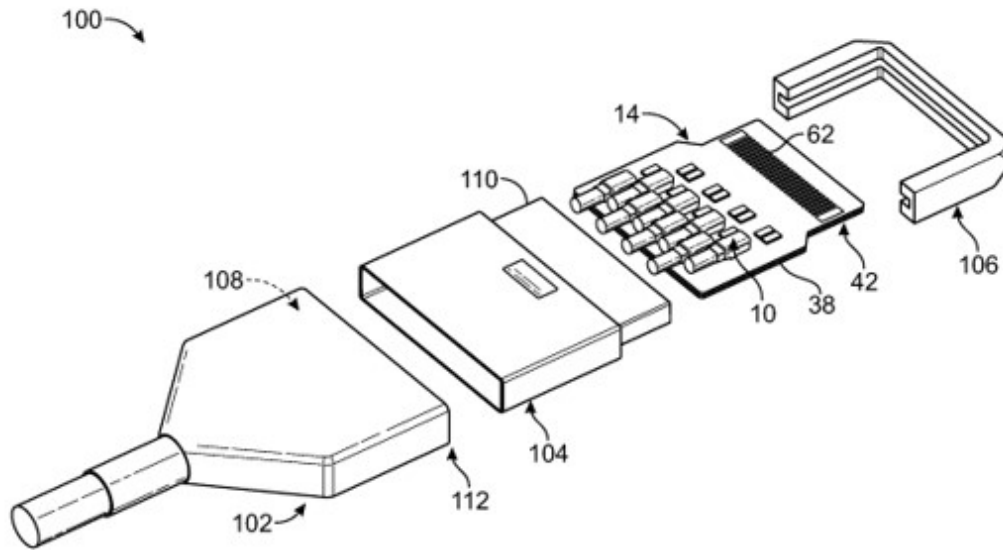


FIG. 8

b

Alden, Fig. 8

ii. **Limitation [9A]**

]: sheathed wires extending between a first connector and a second connector, 230. As discussed *supra* §IX.B.3.a (~~[VI.D.2.c.i (Preamble [9PRE])~~), Alden teaches a cable assembly as I/O connector 100. EX1006, Fig. 8, [0016], [0035]. The I/O connector 100 includes “a wire assembly 10” (e.g., “*sheathed wires*”) *extending* from circuit board 14 (i.e., “*a first connector*”). EX1006, [0035] (“an electrical connector 100 with which the circuit board and wire assembly 10 may be used”); ~~Souri, ¶230.~~). As discussed *supra* §IX.B.1.e (~~[VI.D.2.a.iii (Limitation [1B])~~), Alden’s wire assembly comprises *sheathed wires*, *e.g., for example*, a ~~twinaxial~~twin axial cable as described in the ’898 patent. EX1006, [0017]; EX1001, 3:14-17; ~~Souri, ¶230.~~

231. Although Alden does not describe the component at a second end of electrical wires 12, in my opinion, POSAs would have had reasons to include a second connector as in FIG. 8, which Alden calls an I/O connector. EX1006, [0016]; ~~Souri, ¶231.~~ Such a cable assembly would enable interconnecting two devices each having a mating connector (EX1006, [0025]), which was a known use of I/O connectors.

~~Such cable assemblies would enable interconnecting two devices, each having a mating connector (EX1006, [0025]), which was a known use of I/O connectors. Souri, ¶231.~~

232. ———eThus, in my opinion, Alden meets Limitation [9A].

iii. **Limitations [9B], [9B1]-[9B4]**

233. Alden meets Limitations [9B] and [9B1]-[9B4] for the reasons that it meets the corresponding limitations shown below. EX1013, 1; ~~Souri, ¶233.~~ The “*some of the sheathed wires*” in [9B2] are the “*outer wires*” in [1B], while the “*others of the sheathed wires*” in [9B3] are the “*inner wires*” in [1C]. ~~Souri, ¶233.~~

Limitation	Corresponding limitation	Discussion <i>supra</i>
[9B]	[1PRE]	§ ~~IX.B.1~~ <u>VI.D.2.a.i</u>
[9B1]	[1A]	§ ~~IX.B.1.b~~ <u>VI.D.2.a.ii</u>
[9B2]	[1B]	§ ~~IX.B.1.c~~ <u>VI.D.2.a.iii</u>
[9B3]	[1C]	§ ~~IX.B.1.d~~ <u>VI.D.2.a.iv</u>
[9B4]	[1D]	§ ~~IX.B.1.e~~ <u>VI.D.2.a.v</u>

4. **Claim 10**

234. Thus, it is my opinion that Alden meets Limitations [9B] and [9B1]-

[9B4].

- d. Claim 10: The cable of claim 9, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.**

235. Alden meets the additional limitations in claim 10 for the reasons it meets claim 2. *Supra* §IX.B.VI.D.2; ~~Souri, ¶235.—b.~~

236. —5.— Thus, it is my opinion that Alden meets claim 10.

e. Claim 16

- ~~—ai.~~ **Preamble [16PRE+]: A cable manufacturing method that comprises:**

237. If [16PRE] is limiting, Alden renders obvious “*a cable manufacturing method*” and its “*providing*” ([16A]), “*soldering*” ([16B]), and “*packaging*” ([16C]) steps as shown below. ~~Souri, ¶237.~~

bii. Limitations [16A], [16A1]-[16A4]

Alden meets Limitations [16A] and [16A1]-[16A4] for the reasons that it meets the corresponding limitations shown below. EX1013, 2; ~~Souri, ¶238. A~~

238. . In my opinion, a POSA would have “*provid[ed]*” the first and second PCB in [16A] in order to provide a cable assembly with connectors at each end of the cable. ~~Souri, ¶238.~~

Limitation	Corresponding limitation	Discussion <i>supra</i>
[16A]	[9A]-[9B]	§§IX.B.3.b- VI.B.3D.2.c.ii- <u>VI.D.2.c.iii</u>

[16A1]	[1A]	~~§IX.B.1.b~~ <u>VI.D.2.a.ii</u>
[16A2]	[1B]	~~§IX.B.1.e~~ <u>VI.D.2.a.iii</u>
[16A3]	[1C]	~~§IX.B.1.d~~ <u>VI.D.2.a.iv</u>
[16A4]	[1D]	~~§IX.B.1.e~~ <u>VI.D.2.a.v</u>

239. ~~_____e._____~~ ~~Limitation [16B]~~ Thus, it is my opinion that Alden meets Limitations [16A] and [16A1]-[16A4].

iii. Limitation [16B]: soldering unsheathed ends of the sheathed wires to the electrodes in the inner and outer set;

240. Alden meets [16B] because it describes “mounting” the “exposed end segments 34” of signal wires to the “corresponding mounting pad 52... using solder.” EX1006, [0029]; ~~Souri, ¶240. Alden’s mounting pads 52 are arranged in “inner” and~~ Alden’s mounting pads 52 are arranged in “inner” and ~~“outer sets of electrodes” on circuit board 14 and the exposed end segments 34 are “unsheathed ends of sheathed wires.” Supra §§IX.B.1.c ([1B]), IX.B.1.d ([1C]); EX1006, [0019]; Souri, ¶240. This teaches “soldering unsheathed ends of the sheathed wires to the electrodes in the inner and outer set.” Souri, ¶¶.~~ “outer sets of electrodes” on circuit board 14 and the exposed end segments 34 are ~~d.~~ “unsheathed ends of sheathed wires.” Supra §§VI.D.2.a.iii (Limitation [1B]), VI.D.2.a.iv (Limitation [1C]); EX1006, [0019]. This teaches “soldering unsheathed ends of the sheathed wires to the electrodes in the inner and outer set.”

241. Thus, it is my opinion that Alden meets Limitation [16B].

iv. Limitation [16C]: and packaging the first and second printed circuit boards into connectors adapted to fit into a socket.

Alden meets [16C] because it teaches a PCB 14 enclosed in I/O connector

242. 100. EX1006, Fig. 8 (exploded view), [0016], [0035]-[0036]; ~~Souri,~~

~~¶242. A]. In my opinion, a~~ POSA would have understood that PCB 14 is

“packag[ed]” in I/O connector 100.

~~Souri, ¶242.~~

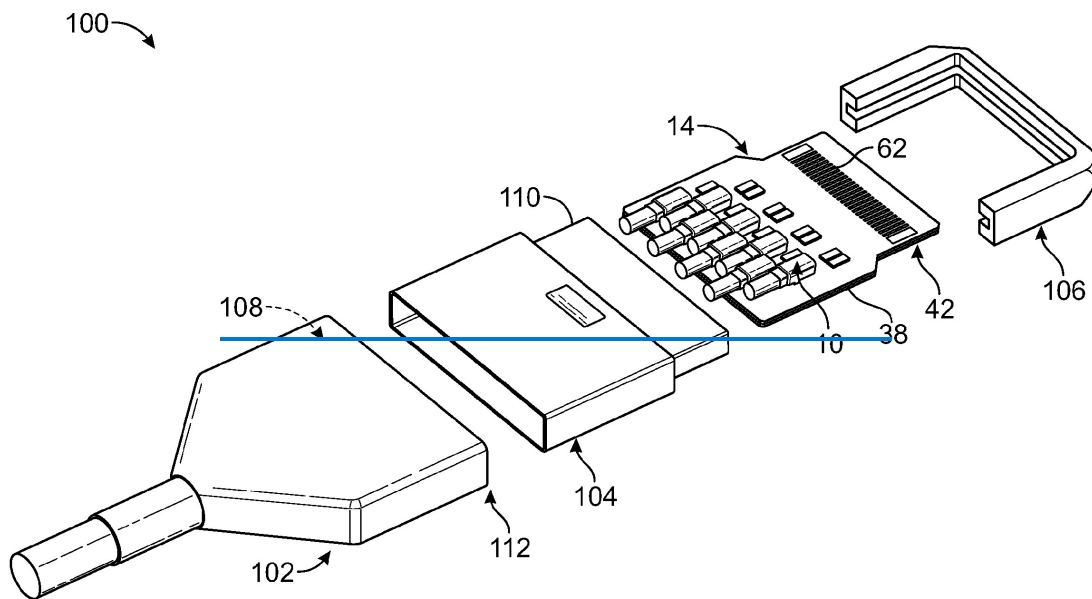


FIG. 8

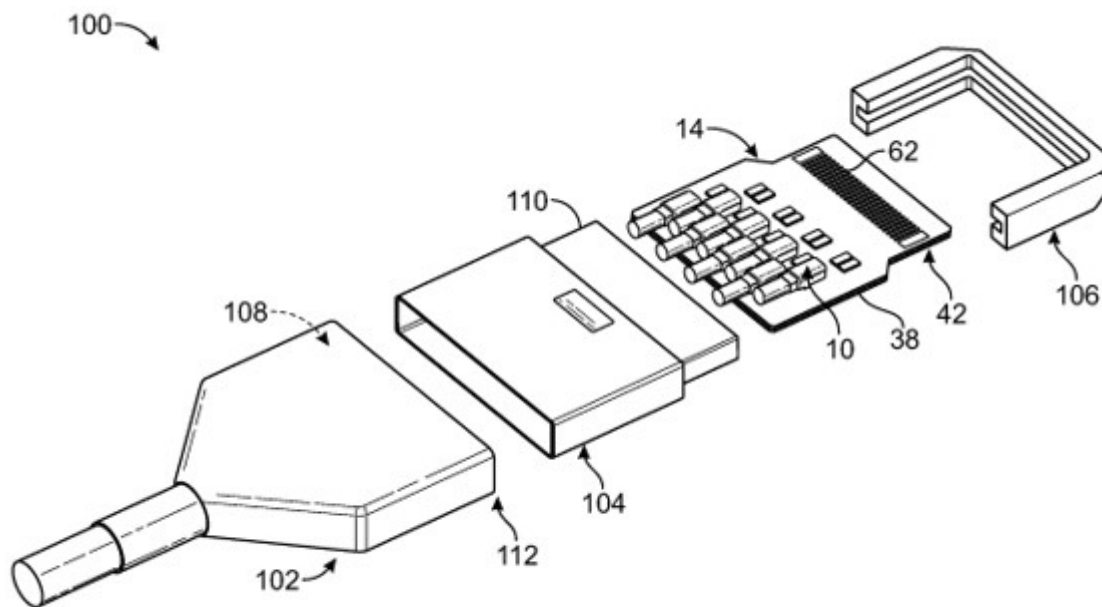


FIG. 8

Alden, Fig. 8

Regardless, in my opinion, a POSA would have found it conventional and obvious to

243. “*packag[e]*” the PCB in a connector in order to achieve the connector assembly that Alden describes. ~~Souri, ¶243.~~

244. In my opinion, POSAs would have recognized that Alden’s I/O connector in ~~Figure~~Fig. 8 is designed to adapt the circuit board 14 to mate with a “*socket*” because “insert 104 holds the circuit board 14 such that the end 42 of the substrate 38 extends within the extension 110 for mating with a complementary mating connector (not shown).” EX1006, [0036]; ~~Souri, ¶244.~~ The “complementary mating connector” is a “*socket*.” *Supra* §~~IX.B.1.b~~ (~~VI.D.2.a.ii~~

(Limitation [1A]); ~~Souri, ¶244.~~ For example, “the end 42 of the substrate 38 defines a card edge that is configured to mate with the complementary mating connector” such that “the mating pads 62 that mate with corresponding mating contacts (not shown) of the complementary mating connector to establish an electrical connection between the electrical connector 100 and the complementary mating connector.” EX1006, [0036], [0025]; ~~Souri, ¶244.~~ Once the PCB is “packaged,” the connectors on the ends of the PCB are positioned so that they can be inserted into a socket, such as sockets according to the QSFP-DD standard. ~~Souri, ¶¶69-72, 244; *supra* §~~*Supra* §§V.E (QSPF-DD Standard), VI.B.1.bA.2.a.ii (Ground 1, ~~[1A])~~. Limitation 6[1A]).

245. Thus, it is my opinion that Alden meets Limitation [16C].

f. Claim 18:- The method of claim 16, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.

246. Alden renders obvious claim 18 because it renders obvious claim 16 (*supra* §~~IX.B.5~~VI.D.2.e) and meets the additional limitations in claim 18 for the same reasons it meets claim 2 (*supra* §~~IX.B.2~~). ~~Souri, ¶246.~~VI.D.2.b).

247. ~~X.~~ ~~GROUND~~ Thus, it is my opinion that Alden meets claim 18.

E. Ground 5: LUGTHART+ALDEN RENDERS OBVIOUS CLAIMS The Combination of Lugthart and Alden Renders Obvious Claims 3, 11, ANDand 17

A. _____ 1. Discussion of the Lugthart+Alden Combination

As discussed *supra* §~~VII.A~~,VI.B.1 (Lugthart), Lugthart teaches a “~~high-speed~~highspeed communication link” in the form of “a cable and a pair of transceivers provided at respective ends of the cable.” EX1007, 6:65-67;~~Souri,~~
¶~~248.~~ Like Alden, Lugthart’s cable includes

248. “one or more pairs of... conductors” that attach to a PCB (e.g., transceiver assemblies 105a/105b). EX1007, 7:1-3, 15:14-24, 18:29-32, Figs. 2A,
~~3B~~;~~Souri,~~

¶~~248.~~

~~43B.~~

_____ a. Reasons to Combine

249. Lugthart’s cable 110 “is an active cable including actively powered componentry for improving performance of the cable 110.” *Id.*, 14:29-31;~~Souri,~~
¶~~249.~~ The cable is terminated at each end by attaching the cable’s “conductive lines 111” to the “line side” of a transceiver assembly 105. ~~EX1007,Id.,~~ 14:29-42. The transceiver assembly 105 at each cable end includes a transceiver 107 implemented “in a single integrated circuit (IC).” ~~EX1007,Id.,~~ 15:25-34;~~Souri,~~
¶~~249.~~ This provides an active cable. ~~EX1007,Id.,~~ 14:29-31;~~Souri,~~¶~~249.~~ The

transceiver assembly's "host side" is configured to interface with a host device (e.g., "electronic device"). *Id.*, Figs. 2A (below), 4A, 14:31-34, 15:552.

EX1007, Figs. 2A (below), 4A, 14:31-34, 15:5-52; *Souri*, ¶249.

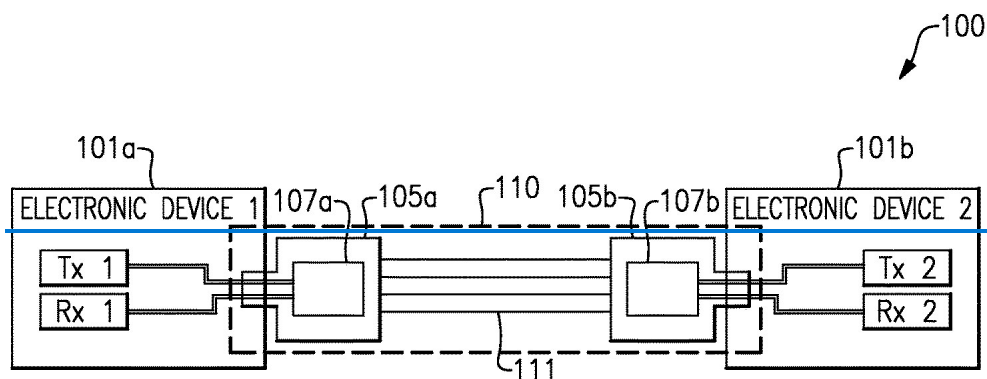


FIG. 2A

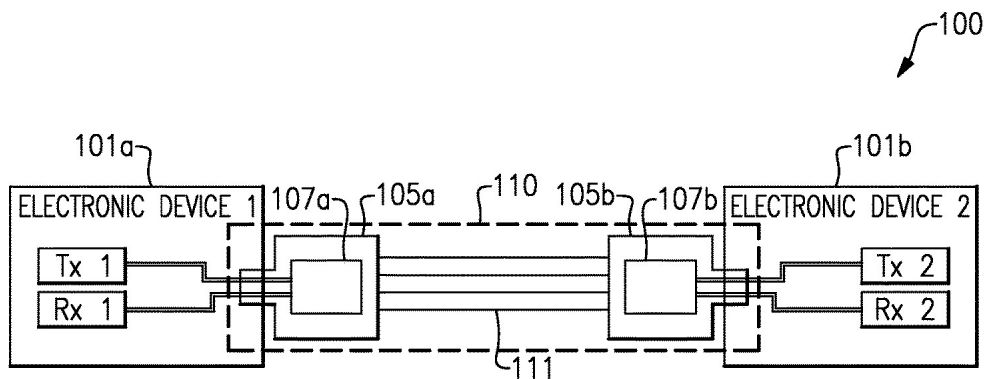


FIG. 2A

A In my opinion, a POSA would have had reasons to implement Lugthart's

transceiver assemblies using the staggered electrode design in Alden's circuit board to reduce crosstalk on the "line side" of theLugthart's transceiver assembly. ~~*Souri*~~, ¶250. Alden recognizes that "[c]ompetition and market demands have continued the trend toward smaller and higher performance (e.g., faster) electronic systems" that

would benefit from “a circuit board and wire ~~assembly~~assembl[ies] that experiences less crosstalk between electrical wires that are terminated to the same side of a circuit board.”

EX1006, [0003]-[0004]. Since Alden’s circuit board is not limited to the “[d]imensions” or “orientations,” “number,” and “positions of the various components” (EX1006, [0040]), POSAs would have found it beneficial to apply Alden’s circuit board teachings to Lugthart’s transceiver assemblies, that connect wires to a circuit board for interfacing with an electronic device, to also reduce crosstalk between ~~adjacent~~ electrodes connecting wires of the cable on the same side of the PCB. ~~Souri, ¶250.~~

~~POSAs~~In my opinion, a POSA would have had reason to use the staggered electrode design of Alden’s

PCB with Lugthart’s transceiver assemblies to ~~improve~~get the improved performance of

250. Lugthart’s active cable with Alden’s low crosstalk. ~~Souri, ¶250.~~

251. When using Alden’s PCB design to form an active cable as illustrated in Lugthart Figure 2A, the transceiver assemblies would carry the egress/transmit ingress/receive signals processed/generated by Lugthart’s transceiver chip between

the staggered electrodes (as in Alden) ~~on the line side~~ and the contacts on the ~~host side~~ host-side that

connect to an electrical device. ~~Souri, ¶251~~ Thus, a POSA would have arranged the electrodes on the transceiver assembly that connect to the cable (e.g., conductive lines 111 in Fig. 2A) according to Alden to connect the transceiver assembly to the desired signal paths within the assembly. In Lugthart, the signals forming the egress/transmit, ingress/receive signals pass between the traces/electrodes as claimed, such that a POSA would have connected the cable to the transceiver assembly to pass these signals between ~~electrical~~ electronic devices.

~~Souri,~~

~~¶251.~~

252. The combination of Lugthart in view of Alden (“Lugthart+Alden”) would have included staggered rows of electrodes, to achieve the low crosstalk of Alden, and the transceiver of Lugthart to recover and remodulate transmitted and received signals. ~~Souri, ¶252.~~

253. Lugthart’s cable including transceiver assemblies that apply Alden’s circuit board design (hereinafter “Lugthart+Alden”) is thus the predictable use of prior art elements according to their established functions. ~~Souri, ¶253; KSR, 550 U.S. at 416-417.~~

2 **b. Reasonable Expectation of Success**

254. In my opinion, POSAs would have reasonably expected success in applying Alden's circuit board teachings to Lugthart's transceiver assemblies because it was known to implement a cable assembly with the same form factor for either a passive or active cable. EX1010, 15-16 (Figs. 4, 5); ~~Souri, ¶254.~~ Both Lugthart and Alden are directed to high-speed connectors that use a PCB in connectors terminating a cable providing an interface between electronic devices. EX1006, [0025]; EX1007, 14:7-15; ~~Souri, ¶254.~~ Mounting a cable to a PCB to connect an IC on the PCB ~~was conventional~~ is a common practice and Lugthart describes that its transceiver assembly is suitable for mounting wires in a cable. ~~Souri, ¶254.~~ The combination thus uses known components and design methods in known ways in a predictable art. ~~Souri, ¶254.~~

B. Analysis

1. 2. Mapping of the Lugthart+Alden Combination to claims 3, 11, and 17

255. Lugthart+Alden renders obvious claims 3, 11 and 17.

a. Claim 3: The printed circuit board of claim 1, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

256. Lugthart+Alden meets claim 1 for the same reasons as Alden alone.

Supra

~~§IX.B.1; Souri, ¶256.~~ §VI.D.2.a.

As discussed *supra* §§~~VII.A~~ VI.B.1 (Lugthart), ~~VII.C.1.b~~ VI.B.3.a (Ground 2, claim 3),

Lugthart teaches that its transceiver is an ~~integrated circuit~~ included on a transceiver assembly

257. PCB. ~~Souri, ¶257. —POSAs~~ In my opinion, a POSA would have understood that Lugthart+Alden teaches a PCB having a host-side (i.e., “*edge connector traces*”) for connecting to an electrical device and a line-side (i.e., *electrodes*) connected to ~~signal wires in~~ a cable. *Supra* §§~~IX.B.1.b-IX.B.1.d~~ (VI.D.2.a.ii-VI.D.2.a.iv (Limitations [1A]-[1C])); cf. EX1007, ~~15:25-34, 19:46-48, Fig. 4A; Souri, ¶257.~~

15:25-34, 19:46-48, Fig. 4A.

258. As discussed *supra* §§~~VII.C.1.b~~ VI.B.3.a, Lugthart’s transceiver “*recovers... signals passing between*” the host-side (i.e., *edge connector traces*) and the ~~line-side~~ lineside (i.e., *electrodes...*) via a CDR circuit that digitizes the incoming analog signals and provides “timing recovery to recover a clock and a data signal” from the host

(EX1007, 21:43-52) and the line (EX1007, 22:50-59). ~~Souri, ¶258;~~ E.g., EX1007,

Figs. 1A, 4A. As also discussed *supra* §~~VII.C.1.b~~VI.B.3.a, Lugthart's transceiver "remodulates" these recovered signals by sending/receiving host-side signals with NRZ modulation and sending/receiving line-side signals with PAM4 modulation, where the transceiver converts between NRZ and PAM4 modulation. EX1007, 54:26-55:45; accord
54:26-55:45; Souri, ¶258; accord EX1001, 3:19-21, 3:65-67.

259. ——— 2. ——— Thus, it is my opinion that Lugthart+Alden meets claim 3.

b. Claims 11, 17

Claim 11: The cable of claim 9, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

Claim 17: The method of claim 16, further comprising equipping each of the first and second printed circuit boards with an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

260. Claim 11 depends from claim 9, while claim 17 depends from claim 16. Lugthart+Alden meets claims 9 and 16 for the same reasons as Alden alone.

Supra §§IX.B.3VI.D.2.c (claim 9), IX.B.5VI.D.2.e (claim 16); Souri, ¶260.

261. Lugthart+Alden meets the remaining limitations in claims 11 and 17 for the same reasons it meets additional limitations in claim 3. *Supra* §X.B.1; *Souri*, ¶261. *Supra* §VI.E.2.a. In my opinion, for claim 17, POSAs would have “equip[ped]” each of Lugthart’s paddle card with a transceiver because Lugthart teaches PCB having transceivers.

~~For claim 17, POSAs would have “equip[ped]” each of Lugthart’s transceiver assemblies with a transceiver because Lugthart teaches PCBs having transceivers.~~

Lugthart+Alden thus renders obvious claims 11 and 17.

262. Thus, it is my opinion that Lugthart+Alden meets claims 11 and 17. ~~*Souri*, ¶261.~~

~~**XI. GROUND.**~~ **Ground 6: JANSSEN+ALDEN RENDERS OBVIOUS CLAIMS** The Combination of Janssen and Alden Renders Obvious Claims 4-8, 12-15, AND and 19-20

~~**A.**~~ **1. Discussion of the Janssen+Alden Combination**

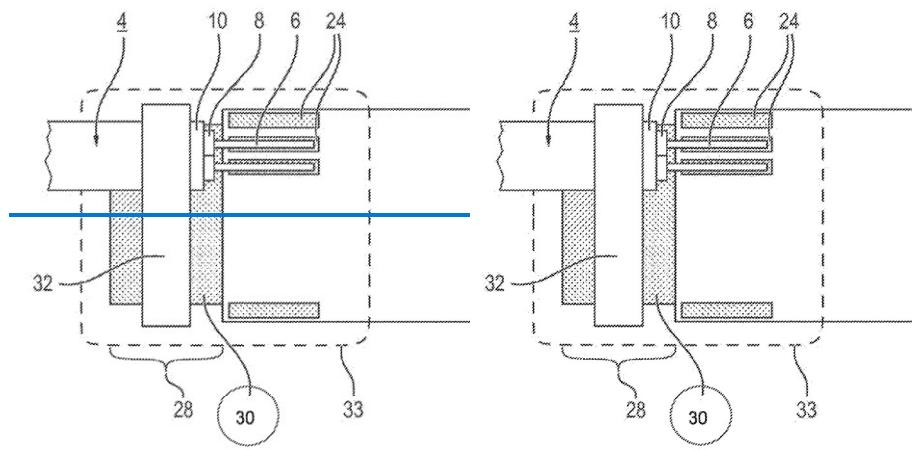
263. Janssen and Alden both teach connecting multiple shielded wire pairs in a cable to a printed circuit board (PCB) used for connections between electrical devices. EX1009, 7:64-8:16; EX1006, [0002], [0005], [0016], [0029], [0036]; *supra* §§~~VIII.A~~VI.C.1 (Janssen), ~~IX.A~~VI.D.1 (Alden); ~~*Souri*, ¶263.~~

~~**1a.**~~ **Reasons to Combine**

264. In my opinion, POSAs would have had several reasons to modify Janssen to use Alden’s teachings (hereinafter “Janssen+Alden”). ~~*Souri*, ¶264.~~

265. Janssen describes connecting “a number of shielded conductor pairs to a board”—such as ~~a paddle cards for QSFP connector’s paddle card connectors~~—for high-speed data connections. EX1009, Abstract, 1:38-58, 2:39-42. ~~POSAs knew that minimizing crosstalk was~~ In order to facilitate a highspeed data connection, it is important to facilitate high-speed interconnects. ~~Souri, ¶265. minimize crosstalk.~~

However, while Janssen teaches soldering cables on the PCB surface, wherein each wire is mounted to contact pads arranged in a single row (e.g., “outer” row) on one edge of the PCB (EX1009, Fig. 2 (in part below)), ~~Janssen~~ it does not describe mitigating crosstalk between signal cables by taking advantage of other geometric layouts, such as when using a second (“inner”) row of signal wire contacts. ~~Souri, ¶265.~~



Janssen, FIG. 2 (excerpted)

Alden recognized that arranging the contact pads for adjacent wires in a single row lead had undesirable effects on signal propagation such as crosstalk. E.g.,

266. EX1006, [0003] (“[E]lectrical wires that are mounted to a circuit board may experience crosstalk with adjacent electrical wires that are mounted to the same side of the circuit board.”); Souri, ¶266.”). POSAs would have had reasons to use Janssen’s ground contact pad and connection methodology with the staggered inner and outer solder pad rows in Alden (*supra* §~~IX.B.1.e~~VI.D.2.a.v Limitation [1D]) in order to connect signal wire leads to the PCB, thus mitigating crosstalk between the adjacently-adjacent wires mounted wires-on the same side of the board. EX1006, Fig. 2, [0002]-[0003], [0039]; Souri, ¶266.—] (“The embodiments described and/or illustrated herein may provide a circuit board and wire assembly that experiences less crosstalk between electrical wires that are terminated to the circuit board.”).

Second, Janssen+Alden would have combined known components (Janssen’s PCB with Alden’s staggered contact pads), according to their conventional uses, with predictable results. KSR, 550 U.S. at 416-417; Souri,

~~267. ¶267.~~ The combination also would have used Alden's known technique of staggered contact pads to reduce crosstalk between wires to improve Janssen's PCB in the same way.

~~PCB in the same way. KSR, 550 U.S. at 416-417; Souri, ¶267.~~

~~_____2_____~~ **b. Reasonable Expectation of Success**

268. POSAs would have reasonably expected success in applying Alden's contact pad teachings to Janssen for the same reasons they worked in Alden, and because Janssen is "suitable" for "all... connectors... equipped with 'paddle cards'." EX1009, 2:39-42. Alden describes such a connector.

2. Mapping of the ~~Janssen is "suitable" for "all... connectors... equipped with 'paddle cards'."~~

~~EX1009, 2:39-42; Souri, ¶268.~~ Alden describes such a connector. ~~Souri, ¶268.~~

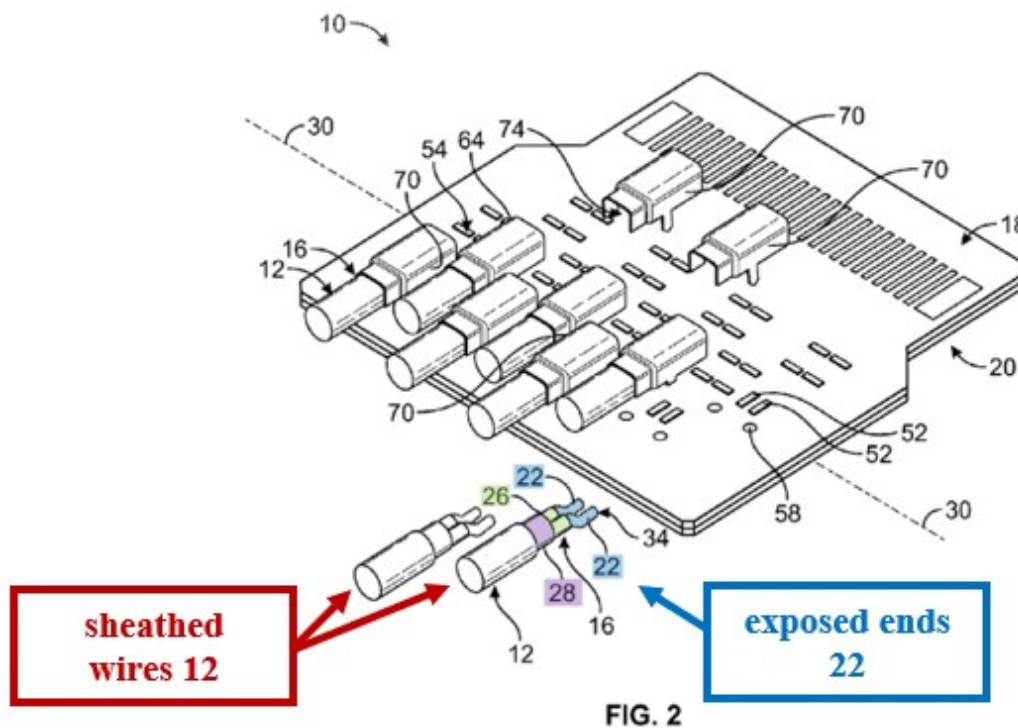
~~_____B. Analysis~~ Combination to claims 4-8, 12-15, and 19-20

269. Janssen+Alden renders obvious claims 4-8, 12-15, and 19-20.

1a. **Claim 4**

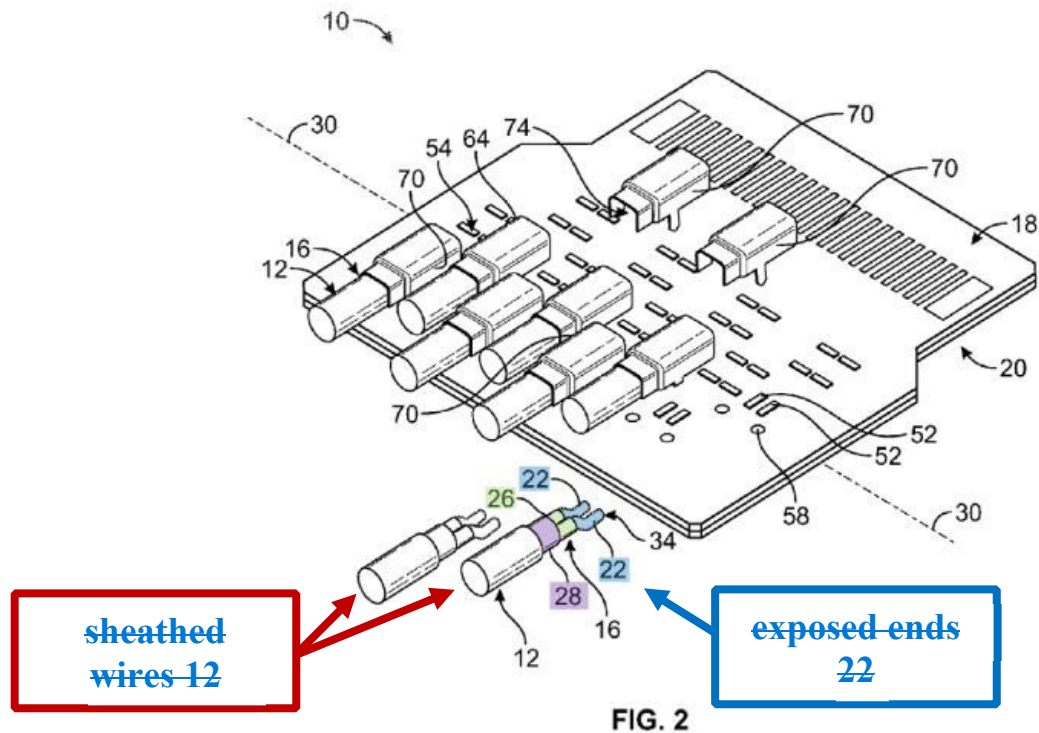
~~_____ai.~~ Limitation [4A]: The printed circuit board of claim 1, wherein the outer wires each have a sheath with a given thickness adjacent to the exposed end,

Janssen+Alden meets [4A] because Alden teaches that the wires connecting to its circuit board “*have a sheath with a given thickness adjacent to*” the signal conductors at “*the exposed end,*” as shown in Fig. 2 (below). *Supra* §IX.B.1.e 270. (VI.D.2.a.iii (Limitation [1B])); EX1006, [0019] (“At the ends 16 of the electrical wires 12, the signal conductors 22 include *exposed end segments 34* that extend lengths outward from ends of the *insulating members 26*.”); *Souri*, ¶270.”).

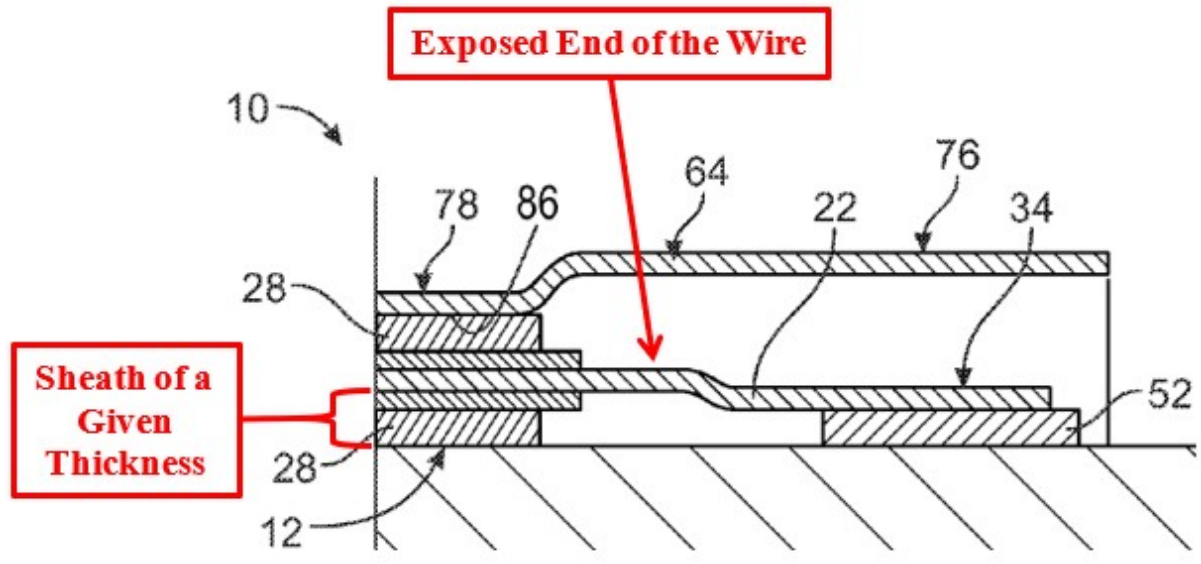
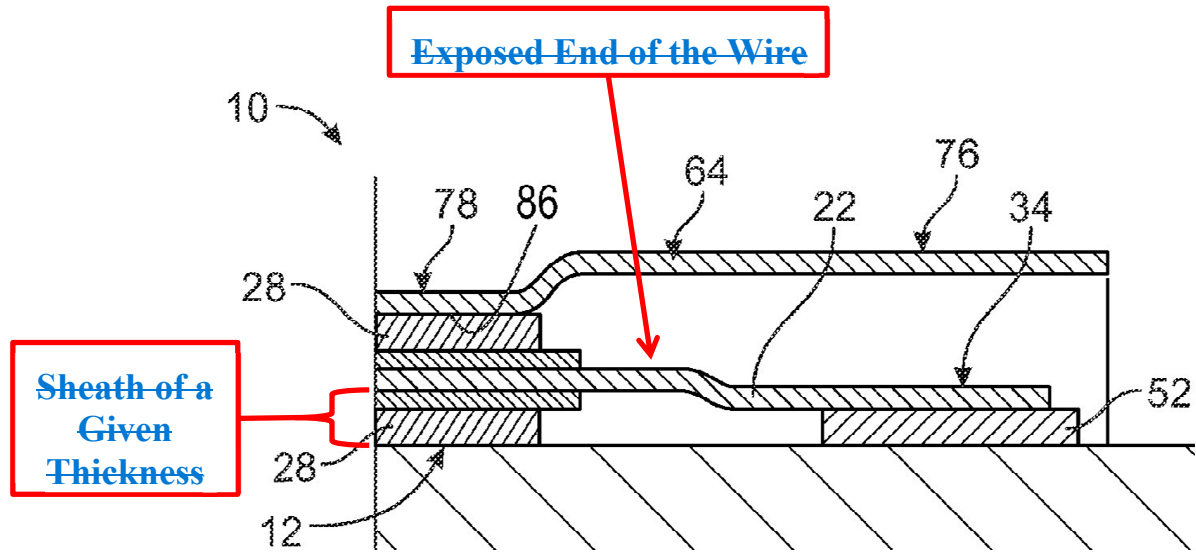


[Alden, Fig. 2 \(annotated\)](#)

271.



Alden Figure 2 shows the “insulating member 26... may be two discrete members that surround corresponding signal conductors 22 of the electrical wire 12” and may also include “a ground conductor 28 [that] extends around the insulating member 26 of one or more of the electrical wires 12.” [EX1006, \[0018\]](#); [Souri, ¶EX1006, \[0018\].271.](#) Annotated Figure 7 (excerpted below) shows the insulating member 26 and ground conductor 28 comprise “a sheath with a given thickness” that surrounds the *exposed end* segment 34 of wire 12. [Souri, ¶271.](#)



Alden, Fig. 7 (excerpted and annotated)

272. Janssen+Alden also meets [4A] because Janssen teaches wires that

“each have a sheath with a given thickness adjacent to the exposed end.”

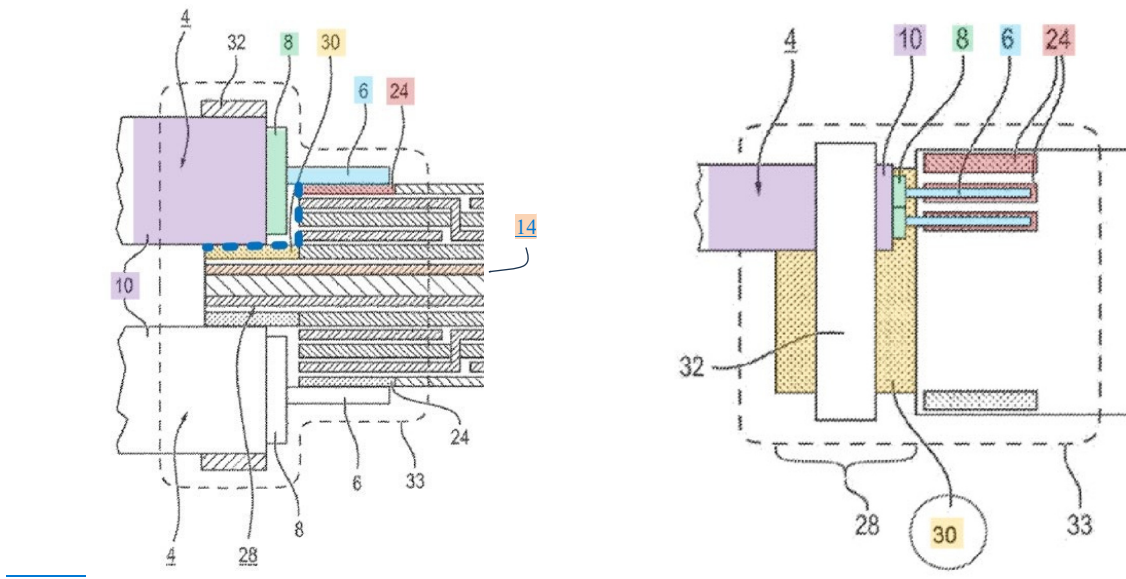
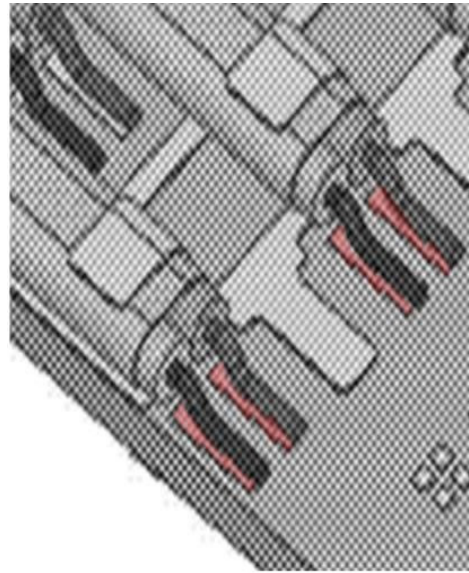
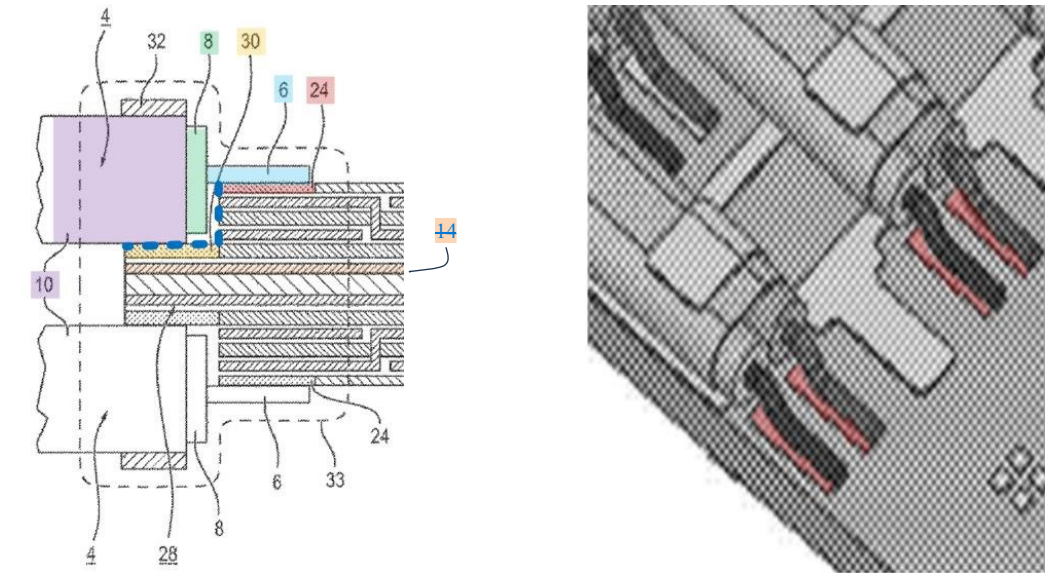
EX1009, 5:63-

6:2 (“shielded pair[s] of insulated wires 4” with “data conductors 6 which are in each case surrounded by insulation 8” and “common pair shielding 10.”); ~~Souri, ¶272.~~”).

273. ~~_____ b. _____ Limitation [4B]~~ Thus, in my opinion, Janssen+Alden meets Limitation [4A].

ii. Limitation [4B]: and wherein the printed circuit board further comprises one or more recesses in the at least one surface along each outer wire sheath’s path between the second edge and the outer set of electrodes.

274. Janssen+Alden meets [4B] because Janssen teaches “ground contact zone 28” that “projects, in a tongue-like manner, towards the connected conductor pairs,” which forms a “*recess*” (blue dashed line in Janssen Fig. 1 below)—e.g., “*one or more recesses*”—in “*at least one surface*” of the PCB “*along each outer wire sheath’s path between the second edge*” of the PCB (*supra* §~~IX.B.1.e~~ (~~VI.D.2.a.iii~~ (Limitation [1B])) “*and the outer set of electrodes*,” which accommodates the thickness of the connecting wires’ sheaths. *Supra* §§~~VIII.A.VI.C.1~~ (Janssen), ~~XI.A.VI.F.1~~ (Janssen+Alden); EX1009, Figs. 1, 2, Abstract, 6:31-33, 6:52-7:18; ~~Souri, ¶274.~~ Metal 30 provides a surface in the recess that electrically contacts and supports wire shielding 10. *Id.*



Janssen, Fig. 1 (~~excerpt~~excerpted, annotated)

Janssen, Fig. 2 (~~excerpt~~excerpted, annotated)

275. Janssen's Figure 1 shows that ground contact zone 28 is *recessed* in the board “*in the at least one surface along each outer wire sheath's path between the second edge and the outer set of electrodes*” (i.e., connection pads 24) since “the carrier 12 is extended in a rearward region of the board 2, which region is

oriented toward the pairs of insulated wires 4, beyond the rest of the layer structure such that a type of projecting tongue is formed.” EX1009, 6:52-56; ~~Souri, ¶275.~~

~~276. ——— 2. ——— Claim 5 Thus, in my opinion, Janssen+Alden meets Limitation [4B].~~

b. Claim 5: The printed circuit board of claim 4, wherein the one or more recesses each accommodates sheathes of multiple outer wires.

~~277. Janssen+Alden renders obvious claim 5 because Janssen describes a “recess[]” (dashed blue lines Fig. 1 below) that “accommodates sheathes of multiple... wires” (e.g., “a total of eight pairs of insulated wires”) on each side of the PCB, such as, e.g.,—for one surface in Fig. 1—a single wire pair shown in the planar view in Fig. 2. EX1009, 8:8-10; Figs. 1, 2; ~~Souri, ¶277.~~ Each recess accommodates “~~outer wires~~” as described ~~supra~~ §§IX.B.1.c ([1B]), XI.B.1.a ([4A]). ~~Souri, ¶277.~~~~

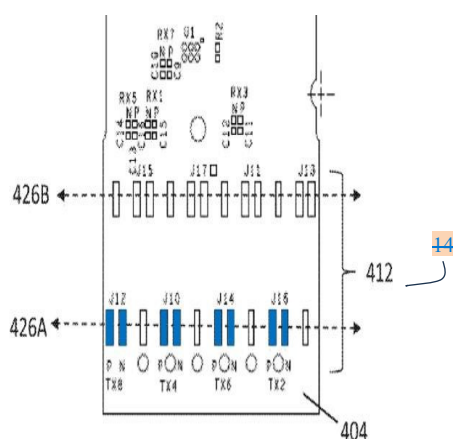
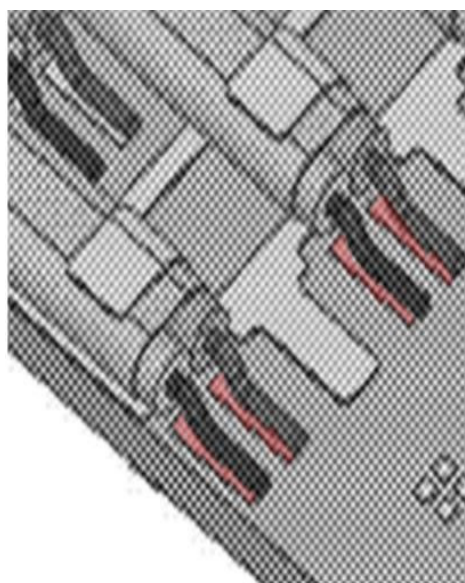
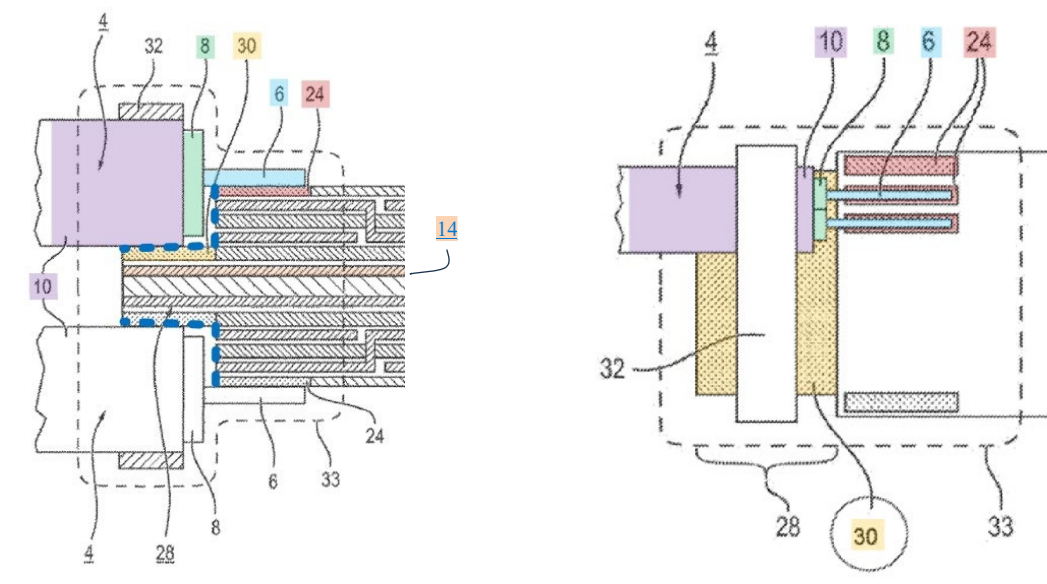


FIG. 4B



“outer wires” as described *supra* §§VI.D.2.a.iii (Limitation [1B]), VI.F.2.a.i (Limitation [4A]).



**Janssen, Fig. 1 (~~exeerpt~~-excerpted,
(excerpted, annotated)**

**Janssen, Fig. 2 (~~exeerpt~~)2
annotated)**

278. Janssen+Alden provides a recess accommodating the sheathes of each “outer wire.” *Supra* §~~XI.B.1.b~~ (VI.F.2.a.ii (Limitation [4B]); EX1009, 7:64-8:16 (recess accommodates multiple pairs of insulated wires); ~~Souri, ¶278.—~~).

279. ——— 3. ——— ~~Claim 6~~ Thus, in my opinion, Janssen+Alden meets claim 5.

c. Claim 6: The printed circuit board of claim 4, wherein each outer wire has a corresponding one of the one or more recesses.

280. Janssen+Alden renders obvious claim 6 because Janssen describes a recess spanning the width of a board surface wherein metal 30 is disposed to

~~support and supports~~ and electrically ~~contact~~contacts each “outer wire” pair shielding 10. ~~Supra §XI.B.1.b~~ (~~§§VI.F.2.a.ii (Limitation [4B])~~, ~~XI.B.VI.F.2.b~~ (claim 5, recess supports multiple outer wires); EX1009, Fig. 2; ~~Souri, ¶280~~. The “each outer wire” in this embodiment “correspond[s]” to the “recess” because each “outer wire” is disposed in the recess. ~~Souri, ¶280~~. The ’898 patent’s Fig. 10 shows a similar configuration wherein a single recess accommodates multiple wires. EX1001, Fig. 10, 6:17-22; ~~Souri, ¶280~~.

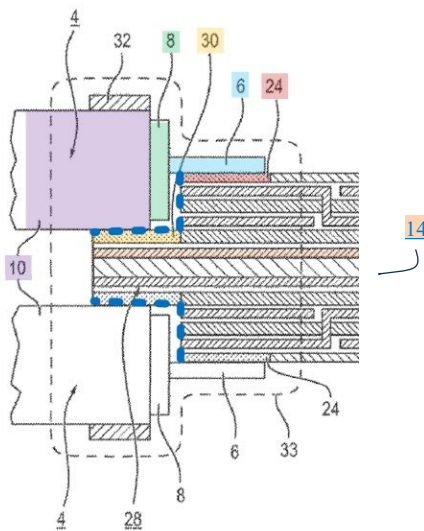
281. Furthermore, in my opinion, a POSA would have known that another predictable design choice was to form a “recess” for each “outer wire” as explained ~~supra §VIII.VI.C.3.-c~~ (Ground 1, claim 6).

~~Souri, ¶281.~~

282. ~~4.~~ ~~Claim 7~~ Thus, in my opinion, Janssen+Alden meets claim 6.

d. Claim 7: The printed circuit board of claim 4, wherein each of the one or more recesses is deep enough to accommodate the given thickness of the sheath, enabling each of the exposed ends of the outer wires to contact the electrodes in the outer set while remaining parallel to the at least one surface.

Janssen+Alden renders obvious claim 7 because Janssen’s tongue-like protrusion forms a “recess” on each surface of the PCB (dashed blue lines in Fig. 1 below). EX1009, Fig. 1; ~~supra §§VIII.C.1.VI.F.2.a~~ (~~¶.i (Limitation [4A])~~, ~~VIII.C.1.b~~ (~~¶VI.F.2.a.ii (Limitation [4B])~~), ~~VIII.C.VI.F.2~~



Janssen, Fig. 1 (excerpted and annotated)

284. Janssen Fig. 1 shows that exposed lead 6 “*remain[s] parallel to the at least one surface*” of the PCB and connection pad 24, disposed in the PCB, to which lead 6 is soldered. Janssen, Fig. 1; ~~Souri, ¶284.1.~~

285. When Janssen’s circuit board is modified to have staggered contact pads as taught in Alden, POSAs would have recognized that the sheathes of the wires connected to Janssen’s *outer set of electrodes* would have been accommodated in the recess so that the conductors likewise remain parallel with the surfaces of the circuit board. ~~Souri, ¶285.~~

286. ~~5.~~ Thus, in my opinion, Janssen+Alden meets claim 7.

e. Claim 8

~~ai.~~ **Preamble [8.PRE] and 8PRE]: The printed circuit board of claim 7, further comprising a second surface having:**

Limitation [8A]

~~[8PRE]~~ The printed circuit board of claim 7, further comprising a second surface having:

~~[8A]~~ a second outer set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed outer wires;

: a second outer set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed outer wires;

As I discussed *supra* §VI.D.2.a.iii (Limitation [1B]), Alden teaches that its circuit board 14 includes *a surface* (i.e., exterior side 18) having *an outer set of electrodes arranged parallel to a second edge for attaching exposed ends of sheathed outer wires*. EX1006, [0020]-[0021], [0029], Fig. 3. Alden also teaches that its circuit board 14 includes exterior side 20 (i.e., “*a second surface*”) on the opposite side of the circuit board.

EX1006, [0020] (“The circuit board 14 includes a substrate 38 that includes the exterior sides 18 and 20.”); ~~Souri, ¶287.~~). Like exterior side 18, exterior side 20 also has “*a second outer set of electrodes*” for connecting wires of a cable. EX1006, [0017] (“[T]he assembly 10 also includes electrical wires 12 that are terminated to an exterior side 20 of the circuit board 14 that is opposite the exterior side 18.”).

Based on these teachings and ~~because that~~ Alden is directed toward reducing ~~cross-talk~~ crosstalk from adjacent wires connected on the same side of the circuit board

(EX1006, [0003]-[0004]), POSAs would have recognized that, like exterior side

287. 18, exterior side 20 of Alden's circuit board also includes "*an outer set of electrodes*" that are "*arranged parallel to the second edge for attaching exposed ends of sheathed outer wires.*" ~~Souri, ¶287.~~

288. ———~~b~~ Thus, in my opinion, Janssen+Alden meets Preamble [8PRE] and

Limitation [8A].

ii. **Limitation [8B]**

[8B]: and one or more recesses in the second surface extending along a path of each sheathed outer wire's sheath between the second edge and the second outer set of electrodes.

289. As I discussed ~~supra~~ above with respect to Limitation [4B], Janssen teaches a recess on each side of a PCB represented as ground contact zone 28, as shown in Figure 1 (below). EX1009,

6:57-60 ("The carrier 12 forms a ground plane 26 with the ground conductor 14. The projecting partial region forms a ground contact zone 28 of the ground plane 26.").

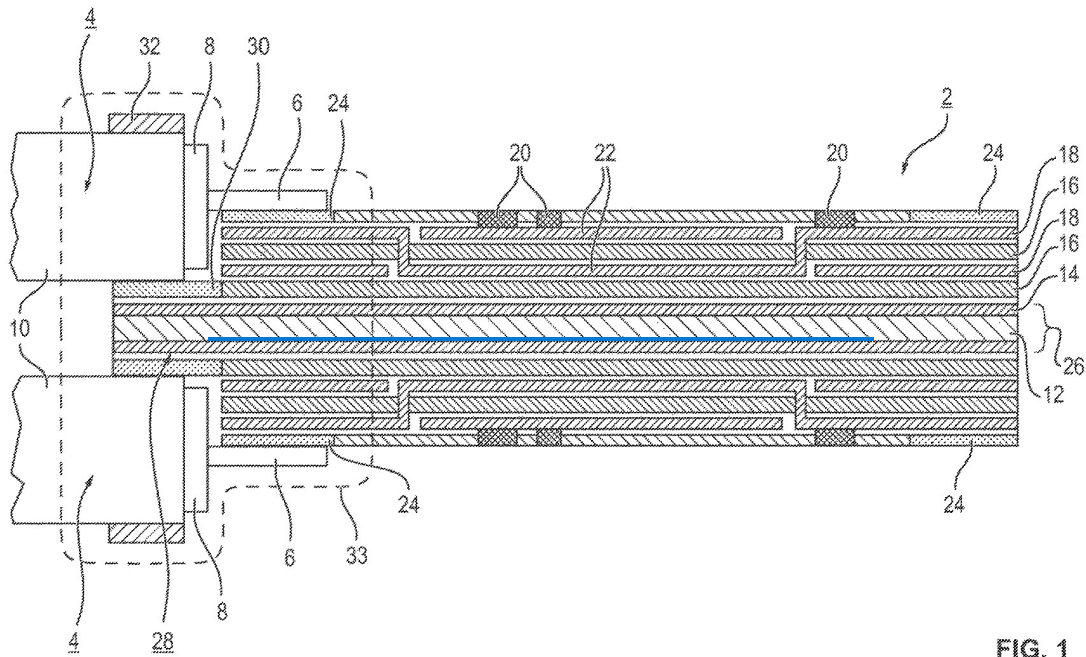


FIG. 1

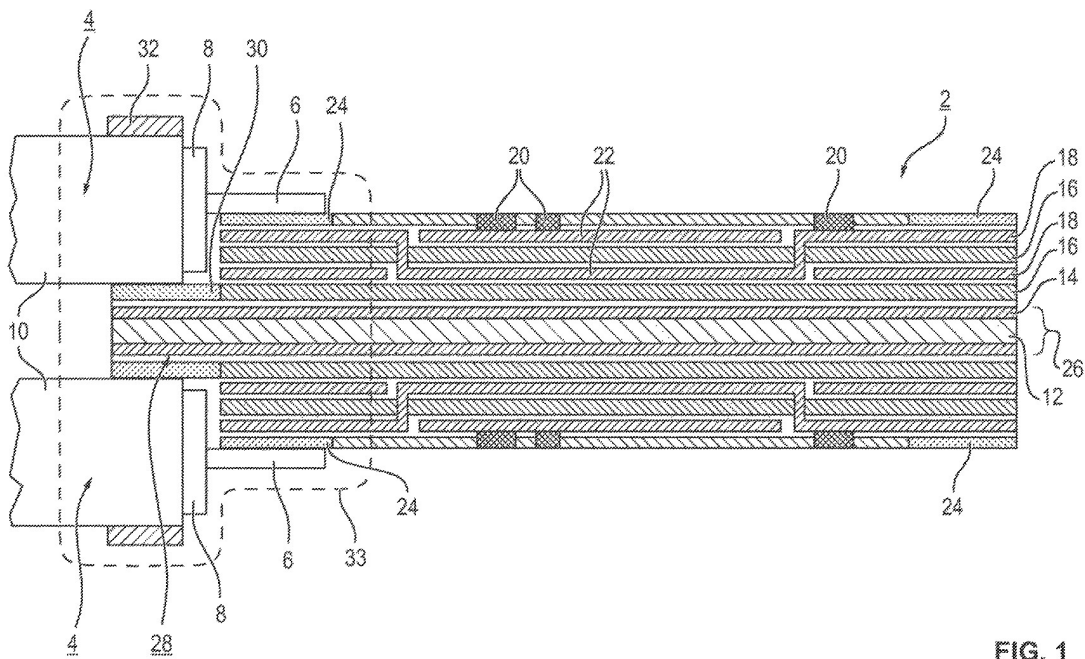


FIG. 1

Janssen, Fig. 1

290. When Alden's staggered contact pad teaching is applied to Janssen's PCB, POSAs would have recognized that, as I discussed supraabove with respect to

Limitation [4B], the “*recess[] in the second surface extend[s] along a path of each sheathed outer wire’s sheath between the second edge and the second outer set of electrodes.*” ~~Souri, ¶¶289-290.~~

291. ~~6.~~ Thus, in my opinion, Janssen+Alden meets Limitation [8B].

f. **Claims 12 and 19**

Claim 12: The cable of claim 9, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes.

Claim 19: The method of claim 18, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes, each of the recesses being deep enough to accommodate a full thickness of the sheath near the unsheathed end.

292. Claims 12 and 19 depend from claims 9 and 18, respectively.

Janssen+Alden meets claims 9 and 18 for the reasons that Alden alone meets claims 9 (*supra* §~~IX.B.3~~VI.D.2.c) and 18 (*supra* §~~IX.B.6~~VI.D.2.f), respectively. ~~Souri, ¶292.~~

293. The additional limitations in claims 12 and 19 are similar to the additional limitations in claim 7 and [4B]. EX1013, 3; ~~Souri, ¶293.~~ Janssen+Alden meets the remaining limitations in claims 12 and 19 for reasons that Janssen+Alden

meets claim 7 (depending on claim 4). *Supra* §§~~XI.B.1~~VI.F.2.a (claim 4),
~~XI.B.4~~VI.F.2.d (claim 7); ~~Souri, ¶293.~~ Janssen+Alden further meets the
additional limitations in claims 12 and 19, and renders each claim obvious, because
Janssen teaches soldering signal wire leads (e.g., “individual data conductors 6”) to
the “outer row” of “connection pads 24” (e.g., providing “*sheathed wires attached*
to the outer set of electrodes”). EX1009,
EX1009, 7:29-32; Souri, ¶293.

294. ——— 7. ——— Thus, in my opinion, Janssen+Alden meets claims 12 and
19.

g. **Claims 13-15 and 20**

Claim 13: The cable of claim 12, wherein the one or more recesses each accommodates sheathes of multiple sheathed wires.

Claim 14: The cable of claim 12, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more recesses.

Claim 15: The cable of claim 12, wherein each of the one or more recesses is deep enough to accommodate a full thickness of the sheath near the unsheathed end, enabling each of the unsheathed ends of the wires attached to the outer set of electrodes to contact those electrodes while remaining parallel to the at least one surface.

Claim 20: The method of claim 19, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more

recesses. 295. Claims 13-15 depend from claim 12, and claim 20 depends from claim 19.

Janssen+Alden meets base claims 12 and 19. *Supra* §~~XI.B.6~~; ~~Souri, ¶VI.F.2.f.295.~~

296. Janssen+Alden meets the additional limitations in claims 13-15 and 20, and renders those claims obvious, for the reasons it meets the corresponding limitations in claims 5-7 as shown below. EX1013, 4-5; ~~Souri, ¶296.~~

Claim	Corresponding claim	Discussion <i>supra</i>
13	5	§ ~~XI.B~~ <u>VI.F.2.b</u>
14, ~~20~~	6	§ ~~XI.B.3~~ <u>VI.F.2.c</u>
15	7	§ ~~XI.B.4~~ <u>VI.F.2.d</u>
<u>20</u>	<u>6</u>	<u>§VI.F.2.c</u>

297. Thus, in my opinion, Janssen+Alden meets claims 13-15 and 20.

VII.XII. DISCRETIONARY DENIAL IS UNWARRANTED

A. Section 314(a)

Section 314(a) discretionary denial is inapplicable. The '898 patent has not previously been challenged in IPR, so the *General Plastic* analysis⁴ does not apply. There is no parallel litigation involving the '898 patent, so the *Fintiv* analysis⁵ does not apply. Regardless, the Petition provides compelling evidence of unpatentability that favors institution.

B. Section 325(d)

There is no basis for discretionary denial under §325(d). *Advanced Bionics v. MED-EL Elektromedizinische Geräte*, IPR2019-01469, Paper 6 (Feb. 13, 2020)

⁴ *General Plastic Industries v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sep. 6, 2017) (precedential).

⁵ *Apple v. Fintiv*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).

(precedential).

1. ~~Grounds fail *Advanced Bionics* step one.~~

~~The Grounds rely on references—Ayzenberg,~~ DECLARATION

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

~~Alden, Lugthart, and Janssen that were never considered or cited during prosecution. E.g., EX1001, code (56). Specifically, none of references of record rely on Ayzenberg's or Alden's teachings of a PCB having two rows of staggered electrodes for connecting wires in a cable. See EX1002, 45-48; EX1017, 48-51. And none of the references of record rely on a combination of Ayzenberg or Alden with either Lugthart or Janssen, as discussed above. The Examiner allowed the claims without rejection over U.S. 7,655,869 ("Kawaguchi") because Kawaguchi did not teach a~~

PCB “with the electrodes in the inner set being staggered relative to the electrodes in the outer set” (EX1002, 45). But both Ayzenberg and Alden teach this. *Supra* §§VI.B.1.e (Ayzenberg), IX.B.1.e (Alden).

Accordingly, the prior art presented in the Grounds are not cumulative to prior art presented to the Office during prosecution. Thus, this Petition presents new art and arguments not previously considered and fails *Advanced Bionics* step one. *Advanced Bionics*, Paper 6, at 8-9; *PLR Worldwide Sales v. Flip Phone Games*, IPR2024-00209, Paper 9, 17 (May 10, 2024) (refusing discretionary denial because none of the references applied in the Petition were cited during prosecution).

2. — Grounds fail *Advanced Bionics* step two.

There is no basis for reaching *Advanced Bionics* step 2 because the Petitions fails *Advanced Bionics* step one. Regardless, the Petition also fails any reasonable step 2 analysis because the Examiner did not analyze or apply any of the references cited during prosecution in a rejection.

XIII. CONCLUSION

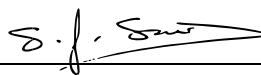
The Board should institute review and cancel claims 1-20.

Respectfully submitted,

Amphenol Corp.

Dated: _____ April 1, 2025

By: /Adam R. Wichman/



~~Adam R. Wichman, Reg. No. 43,988~~

~~WOLF, GREENFIELD & SACKS, P.C.~~

Shukri Sourì, Ph.D.

APPENDIX A: U.S. PATENT NO. 11,495,898 CLAIM LIST

The following claim listing assigns element labels (e.g., [1A], [1B], ...) to certain claims for clarity.

Claim 1
[1PRE] A printed circuit board that comprises at least one surface having:
[1A] edge connector traces arranged along a first edge for contacting electrical conductors in a socket connector;
[1B] an outer set of electrodes arranged parallel to a second edge for attaching exposed ends of sheathed wires in a cable (“outer wires”);
[1C] and an inner set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed wires in a cable (“inner wires”),
[1D] with the electrodes in the inner set being staggered relative to the electrodes in the outer set.
Claim 2
The printed circuit board of claim 1, with the electrodes in each of the inner and outer sets being spaced to enable the inner wires to pass between the outer wires while maintaining contact with the at least one surface.
Claim 3
The printed circuit board of claim 1, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.
Claim 4
[4A] The printed circuit board of claim 1, wherein the outer wires each have a sheath with a given thickness adjacent to the exposed end,
[4B] and wherein the printed circuit board further comprises one or more recesses in the at least one surface along each outer wire sheath’s path between the second edge and the outer set of electrodes.
Claim 5

The printed circuit board of claim 4, wherein the one or more recesses each accommodates sheathes of multiple outer wires.

Claim 6

The printed circuit board of claim 4, wherein each outer wire has a corresponding one of the one or more recesses.

Claim 7

The printed circuit board of claim 4, wherein each of the one or more recesses is deep enough to accommodate the given thickness of the sheath, enabling each of the exposed ends of the outer wires to contact the electrodes in the outer set while remaining parallel to the at least one surface.

Claim 8

[8PRE] The printed circuit board of claim 7, further comprising a second surface having:

[8A] a second outer set of electrodes arranged parallel to the second edge for attaching exposed ends of sheathed outer wires;

[8B] and one or more recesses in the second surface extending along a path of each sheathed outer wire's sheath between the second edge and the second outer set of electrodes.

Claim 9

[9PRE] A cable that comprises:

[9A] sheathed wires extending between a first connector and a second connector,

[9B] each of the first and second connectors including a printed circuit board with at least one surface having:

[9B1] edge connector traces arranged along a first edge for contacting electrical conductors when the connector is inserted in a socket;

[9B2] an outer set of electrodes arranged parallel to a second edge for attaching unsheathed ends of some of the sheathed wires;

[9B3] and an inner set of electrodes arranged parallel to the second edge for attaching unsheathed ends of others of the sheathed wires,

[9B4] with the electrodes in the inner set being staggered relative to the electrodes in the outer set.

Claim 10

The cable of claim 9, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.

Claim 11

The cable of claim 9, further comprising an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

Claim 12

The cable of claim 9, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes.

Claim 13

The cable of claim 12, wherein the one or more recesses each accommodates sheathes of multiple sheathed wires.

Claim 14

The cable of claim 12, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more recesses.

Claim 15

The cable of claim 12, wherein each of the one or more recesses is deep enough to accommodate a full thickness of the sheath near the unsheathed end, enabling each of the unsheathed ends of the wires attached to the outer set of electrodes to contact those electrodes while remaining parallel to the at least one surface.

Claim 16

[16PRE] A cable manufacturing method that comprises:

[16A] providing first and second printed circuit boards each having:

[16A1] edge connector traces arranged along a first edge for contacting electrical conductors when the printed circuit board is inserted in a matching socket;

[16A2] an outer set of electrodes arranged parallel to a second edge for attaching unsheathed ends of certain sheathed wires in a cable;

[16A3] and an inner set of electrodes arranged parallel to the second edge for attaching unsheathed ends of other sheathed wires in the cable,

[16A4] with the electrodes in the inner set being staggered relative to the electrodes in the outer set;

[16B] soldering unsheathed ends of the sheathed wires to the electrodes in the inner and outer set;

[16C] and packaging the first and second printed circuit boards into connectors adapted to fit into a socket.

Claim 17

The method of claim 16, further comprising equipping each of the first and second printed circuit boards with an integrated circuit that recovers and remodulates signals passing between the edge connector traces and the electrodes of the inner and outer sets.

Claim 18

The method of claim 16, wherein the electrodes in each of the inner and outer sets are spaced to enable the sheathed wires attached to the inner set to maintain contact with the at least one surface while passing between the sheathed wires attached to the outer set.

Claim 19

The method of claim 18, wherein each printed circuit board further comprises one or more recesses in the at least one surface between the second edge and the outer set of electrodes to accommodate sheathes of the sheathed wires attached to the outer set of electrodes, each of the recesses being deep enough to accommodate a full thickness of the sheath near the unsheathed end.

Claim 20

The method of claim 19, wherein each sheathed wire attached to the outer set of electrodes has a corresponding one of the one or more recesses.

~~CERTIFICATE OF SERVICE UNDER 37 C.F.R. §42.6(e)(4)~~

~~I certify that on April 1, 2025, a copy of the foregoing document, including any exhibits or appendices filed therewith, is being served via *Overnight FedEx* at the following correspondence address of record for the patent:~~

~~_____ Ramey LLP~~

~~5020 Montrose Blvd.
Suite 800~~

~~Houston, TX 77006~~

~~Date: April 1, 2025 _____ /Dara Del Rosario/~~

~~_____ Dara Del Rosario~~

~~_____ Paralegal~~

~~_____ WOLF, GREENFIELD & SACKS, P.C.~~

~~_____
_____~~

~~CERTIFICATE OF WORD COUNT~~

~~Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,987 words excluding a table of contents, a table of authorities, Mandatory Notices under §42.8, a certificate of service or word count, or appendix of exhibits or claim listing. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.~~

~~Date: April 1, 2025~~

~~/Dara Del Rosario/~~

~~Dara Del Rosario~~

~~Paralegal~~

~~WOLF, GREENFIELD & SACKS, P.C.~~