PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/136,343	Filing Date 12/29/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	12/29/2020	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 67	Minus	** 20	= 47		x $50 =	2350
	Independent (37 CFR 1.16(h))	* 7	Minus	*** 3	= 4		x $240 =	960
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	3310

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LDRC
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EVA V GILLIS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/50 (10-17)
Approved for use through 01/31/2020. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE PATENT APPLICATION TRANSMITTAL

Address to:

Mail Stop Reissue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.	NRLA-001US04
First Named Inventor	Anatoli Gorchechnikov
Original Patent Number	9,189,828
Original Patent Issue Date (Month/Day/Year)	11/17/2015
Priority Mail Express® Label No.	

APPLICATION FOR REISSUE OF:
(*Check applicable box*) ☑ Utility Patent ☐ Design Patent ☐ Plant Patent

APPLICATION ELEMENTS (37 CFR 1.173)

1. ☐ **Fee Transmittal Form** (PTO/SB/56)
2. ☑ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification and Claims** in double column copy of patent format (*amended, if appropriate*)
5. ☑ **Drawing(s)** (*proposed amendments, if appropriate*)
6. ☑ **Reissue Oath/Declaration or Substitute Statement** (37 CFR 1.175) (PTO/AIA/05, 06, or 07)
7. ☑ **Application Data Sheet** **NOTE:** Benefit claims under 37 CFR 1.78 and foreign priority claims under 37 CFR 1.55 MUST be set forth in an Application Data Sheet (ADS).
8. ☑ **Original U.S. Patent currently assigned?** ☑ Yes ☐ No
(*If Yes, check applicable box(es)*)
   - ☑ Written Consent of all Assigness (PTO/AIA/53)
   - ☑ 37 CFR 3.73(c) Statement (PTO/AIA/96)
9. ☐ **CD-ROM or CD-R** in duplicate, Computer Program (*Appendix*) or large table
   - ☐ Landscape Table on CD
10. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   - a. ☐ Computer Readable Form (CRF)
   - b. ☐ Specification Sequence Listing on:
     - i. ☐ CD -ROM (2 copies) or CD-R (2 copies); **or**
     - ii. ☐ Paper
   - c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

11. ☑ **Statement of status and support for all changes to the claims.** See 37 CFR 1.173(c).
12. ☑ **Power of Attorney**
13. ☐ **Information Disclosure Statement (IDS)** PTOSB/08 or PTO-1449
   - ☐ Copies of citations attached
14. ☐ **English translation of Reissue Oath/Declaration** (*if applicable*)
15. ☐ **Return Receipt Postcard** (MPEP § 503) (Should be specifically itemized)
16. ☑ **Preliminary Amendment** (37 CFR 1.173; MPEP § 1453)
17. ☐ **Other:** The statement of status and support for all changes to the the claims appears in the remarks section of the preliminary amendment. The claims presented in this continuation reissue application correct an error that was identified in the original reissue declarations but not corrected in the original reissue application, namely, the lack of claims to user interaction streams, and so the original reissue declarations are included here.

☑ This is a continuation reissue or divisional reissue application (*i.e.*, a second or subsequent reissue application for the same issued patent). (*Check box if applicable.*)

18. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 149890 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone			
Email					

Signature	/Christopher Max Colice/	Date	12/29/2020
Name (Print/Type)	Christopher Max Colice	Registration No.	65634

This collection of information is required by 37 CFR 1.173. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Reissue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Neurala, Inc.

Application No./Patent No.: 9,189,828 Filed/Issue Date: 11-17-2015

Titled: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Neurala, Inc. (Name of Assignee), a corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. [x] The assignee of the entire right, title, and interest.

2. [ ] An assignee of less than the entire right, title, and interest (check applicable box):

   [ ] The extent (by percentage) of its ownership interest is _____ %). Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   [ ] There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. [ ] The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. [ ] The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____ , Frame _____ , or for which a copy thereof is attached.

B. [x] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: Neurala LLC
   The document was recorded in the United States Patent and Trademark Office at
   Reel 032138 , Frame 0737 , or for which a copy thereof is attached.

2. From: Neurala LLC To: Neurala, Inc.
   The document was recorded in the United States Patent and Trademark Office at
   Reel 032166 , Frame 0594 , or for which a copy thereof is attached.

153829963 v1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

4. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

5. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

6. From: _____ To: _____
   The document was recorded in the United States Patent and Trademark Office at
   Reel _____ , Frame _____ , or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Christopher Max Colice/	November 9, 2017
Signature	Date
Christopher Max Colice	65,634
Printed or Typed Name	Title or Registration Number

Doc Code: PA.
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 149890

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Neurala, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Heather Ames Vercoe		
Title	COO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Anatoli		Gorchetchnikov	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Newton	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1			
Address 2			
City	Newton	State/Province	MA
Postal Code		Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Heather	Marie	Ames	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Milton	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	13 Myers Lane		
Address 2			
City	Milton	State/Province	MA
Postal Code	02186	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Massimiliano		Versace	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

City	Milton	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	13 Myers Lane		
Address 2			
City	Milton	State/Province	MA
Postal Code	02186	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Fabrizio		Santini	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Jamaica Plain	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1			
Address 2			
City	Jamaica Plain	State/Province	MA
Postal Code		Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	149890		
Email Address	docketing@smithbaluch.com	Add Email	Remove Email

Application Information:

Title of the Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD		
Attorney Docket Number	NRLA-001US04	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	3

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	149890		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15808201	2017-11-09

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15808201	reissued of	14147015	2014-01-03	9189828	2015-11-17
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14147015	Continuation of	11860254	2007-09-24	8648867	2014-02-11
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
11860254	Claims benefit of provisional	60826892	2006-09-25		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
	reissued of	14147015	2014-01-03	9189828	2015-11-17

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Neurala, Inc.		
Mailing Address Information For Applicant:			
Address 1			
Address 2			
City	Boston	**State/Province**	MA
Country	US	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Christopher Max Colice/			Date (YYYY-MM-DD)	2020-12-29
First Name	Christopher	Last Name	Colice	Registration Number	65634

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NRLA-001US04
	Application Number	
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04

Filed as Small Entity

Filing Fees for Reissue (Utility)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY REISSUE BASIC	2014	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Electronic Acknowledgement Receipt

EFS ID:	41509304
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice
Filer Authorized By:	
Attorney Docket Number:	NRLA-001US04
Receipt Date:	29-DEC-2020
Filing Date:	
Time Stamp:	12:55:51
Application Type:	Reissue (Utility)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	E2020BSC57174197
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	NRLA-001US04_Specification.pdf	453495 cc5d6bd9dc967ec48756c767562d2e842f653c24	no	7
Warnings:					
Information:					
2	Drawings-only black and white line drawings	NRLA-001US04_Drawings.pdf	397794 41e7eb322695cdd63ed9f5b259b4738bf12bd36f	no	5
Warnings:					
Information:					
3	Claims	NRLA-001US04_Claims.pdf	133360 b60889e1063afeba0d581c9aa6b308bfe357893a	no	2
Warnings:					
Information:					
4	Consent of Assignee accompanying the declaration	NRLA-001US04_aia0053.pdf	272529 4ce18546eb06e73740d45addc9c4d26c0baa7f2b	no	2
Warnings:					
Information:					
5		NRLA-001US04_Preliminary_Amendment_20201229.pdf	287029 dad52a3e674128a30f080c2476c830dbe32b30a9	yes	15

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Specification	2	2
Claims	3	14

	Applicant Arguments/Remarks Made in an Amendment		15	15	
Warnings:					
Information:					
6	Transmittal Reissue Application	NRLA-001US04_aia0050.pdf	294406 1049357723b5218b614025664d0daee86bda6bd4	no	2
Warnings:					
Information:					
7	Assignee showing of ownership per 37 CFR 3.73	NRLA-001US04_373c_Statement.pdf	74940 185dc9214ef692f15e86535fde5d502658809172	no	2
Warnings:					
Information:					
8	Power of Attorney	Neurala__Inc__-_General_POA_-_EXECUTED.pdf	1790359 81e902bb741ffe0a2a42df18950cfab10a917ceb	no	1
Warnings:					
Information:					
9	Reissue dec filed in accordance with MPEP 1414	NRLA-001US04_Reissue_Application_Declarations.pdf	1574989 0e9c54fc1cbe3b97192082fd55b81cae380fd9d9	no	11
Warnings:					
Information:					
10	Application Data Sheet	NRLA-001US04_USPTO_AIA14_20201229_125201.pdf	1874458 5cb24231b4320d29103dd766df0235ecf06768ac	no	10
Warnings:					
Information:					
11	Fee Worksheet (SB06)	fee-info.pdf	29706 2c9102631adc76bf4a86c7d8b7b247261b8ee713	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	7183065		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

RELATED APPLICATIONS

The present application claims a priority benefit, under 35 U.S.C. §120, as a continuation of U.S. application Ser. No. 11/860,254, now U.S. Pat. No. 8,648,867 B2, filed Sep. 24, 2007, entitled "Graphic Processor Based Accelerator System and Method," which claims the priority benefit, under 35 U.S.C. §119(e), of U.S. Application No. 60/826,892, filed Sep. 25, 2006. Each of the above-identified applications is incorporated herein by reference in its entirety.

BACKGROUND

Graphics Processing Units (GPUs) are found in video adapters (graphic cards) of most personal computers (PCs), video game consoles, workstations, etc. and are considered highly parallel processors dedicated to fast computation of graphical content. With the advances of the computer and console gaming industries, the need for efficient manipulation and display of 3D graphics has accelerated the development of GPUs.

In addition, manufacturers of GPUs have included general purpose programmability into the GPU architecture leading to the increased popularity of using GPUs for highly parallelizable and computationally expensive algorithms outside of the computer graphics domain. When implemented on conventional video card architectures, these general purpose GPU (GPGPU) applications are not able to achieve optimal performance, however. There is overhead for graphics-related features and algorithms that are not necessary for these non-video applications.

SUMMARY

Numerical simulations, e.g., finite element analysis, of large systems of similar elements (e.g. neural networks, genetic algorithms, particle systems, mechanical systems) are one example of an application that can benefit from GPGPU computation. During numerical simulations, disk and user input/output can be performed independently of computation because these two processes require interactions with peripheral hardware (disk, screen, keyboard, mouse, etc) and put relatively low load on the central processing unit/system (CPU). Complete independence is not desirable, however; user input might affect how the computation is performed and even interrupt it if necessary. Furthermore, the user output and the disk output are dependent on the results of the computation. A reasonable solution would be to separate input/output into threads, so that it is interacting with hardware occurs in parallel with the computation. In this case whatever CPU processing is required for input/output should be designed so that it provides the synchronization with computation.

In the case of GPGPU, the computation itself is performed outside of the CPU, so the complete system comprises three "peripheral" components: user interactive hardware, disk hardware, and computational hardware. The central processing unit (CPU) establishes communication and synchronization between peripherals. Each of the peripherals is preferably controlled by a dedicated thread that is executed in parallel with minimal interactions and dependencies on the other threads.

A GPU on a conventional video card is usually controlled through OpenGL, DirectX, or similar graphic application

programming interfaces (APIs). Such APIs establish the context of graphic operations, within which all calls to the GPU are made. This context only works when initialized within the same thread of execution that uses it. As a result, in a preferred embodiment, the context is initialized within a computational thread. This creates complications, however, in the interaction between the user interface thread that changes parameters of simulations and the computational thread that uses these parameters.

A solution as proposed here is an implementation of the computational stream of execution in hardware, so that thread and context initialization are replaced by hardware initialization. This hardware implementation includes an expansion card comprising a printed circuit board having (a) one or more graphics processing units, (b) two or more associated memory banks that are logically or physically partitioned, (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the CPU is freed from this function and is dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

In general, according to one aspect, the invention features a computer system. This system comprises a central processing unit, main memory accessed by the central processing unit, and a video system for driving a video monitor in response to the central processing unit as is common. The computer system further comprises an accelerator that uses input data from and provides output data to the central processing unit. This accelerator comprises at least one graphics processing unit, accelerator memory for the graphic processing unit, and an accelerator controller that moves the input data into the at least one graphics processing unit and the accelerator memory to generate the output data.

In the preferred, the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit. Preferably, the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit. The use of the separate controller enables data transfer during execution such that the accelerator controller transfers output data from the accelerator memory to main memory of the central processing unit.

In the preferred embodiment, the accelerator controller comprises an interface controller that enables the accelerator to communicate over a bus of the computer system with the central processing unit.

In general according to another aspect, the invention also features an accelerator system for a computer system, which comprises at least one graphics processing unit, accelerator memory for the graphic processing unit and an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory.

In general according to another aspect, the invention also features a method for performing numerical simulations in a computer system. This method comprises a central processing unit loading input data into an accelerator system from main memory of the central processing unit and an accelera-

tor controller transferring the input data to a graphics processing unit with instructions to be performed on the input data. The accelerator controller then transfers output data generated by the graphic processing unit to the central processing unit as output data.

The above and other features of the invention including various novel details of construction and combinations of parts, and other advantages, will now be more particularly described with reference to the accompanying drawings and pointed out in the claims. It will be understood that the particular method and device embodying the invention are shown by way of illustration and not as a limitation of the invention. The principles and features of this invention may be employed in various and numerous embodiments without departing from the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings, reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale; emphasis has instead been placed upon illustrating the principles of the invention. Of the drawings:

FIG. **1** is a schematic diagram illustrating a computer system including the GPU accelerator according to an embodiment of the present invention;

FIG. **2** is block diagram illustrating the architecture for the GPU accelerator according to an embodiment of the present invention;

FIG. **3** is a block/flow diagram illustrating an exemplary implementation of the top level control of the GPU accelerator system;

FIG. **4** is a flow diagram illustrating an exemplary implementation of the bottom level control of the GPU accelerator system that is used to execute the target computation; and

FIG. **5** is an example population of nine computational elements arranged in a 3×3 square and a potential packing scheme for texture pixels, according to an implementation of the present invention.

DETAILED DESCRIPTION

FIG. **1** shows a computer system **100** that has been constructed according to the principles of the present invention.

In more detail, the computer system **100** in one example is a standard personal computer (PC). However, this only serves as an example environment as computing environment **100** does not necessarily depend on or require any combination of the components that are illustrated and described herein. In fact, there are many other suitable computing environments for this invention, including, but not limited to, workstations, server computers, supercomputers, notebook computers, hand-held electronic devices such as cell phones, mp3 players, or personal digital assistants (PDAs), multiprocessor systems, programmable consumer electronics, networks of any of the above-mentioned computing devices, and distributed computing environments that including any of the above-mentioned computing devices.

In one implementation the GPU accelerator is implemented as an expansion card **180** includes connections with the motherboard **110**, on which the one or more CPU's **120** are installed along with main, or system memory **130** and mass/non volatile data storage **140**, such as hard drive or redundant array of independent drives (RAID) array, for the computer system **100**. In the current example, the expansion card **180** communicates to the motherboard **110** via a local bus **190**. This local bus **190** could be PCI, PCI Express, PCI-X, or any other functionally similar technology (depending upon the availability on the motherboard **110**). An external version GPU accelerator is also a possible implementation. In this example, the external GPU accelerator is connected to the motherboard **110** through USB-2.0, IEEE 1394 (Firewire), or similar external/peripheral device interface.

The CPU **120** and the system memory **130** on the motherboard **110** and the mass data storage system **140** are preferably independent of the expansion card **180** and only communicate with each other and the expansion card **180** through the system bus **200** located in the motherboard **110**. A system bus **200** in current generations of computers have bandwidths from 3.2 GB/s (Pentium 4 with AGTL+, Athlon XP with EV6) to around 15 GB/s (Xeon Woodcrest with AGTL+, Athlon 64/Opteron with Hypertransport), while the local bus has maximal peak data transfer rates of 4 GB/s (PCI Express 16) or 2 GB/s (PCI-X 2.0). Thus the local bus **190** becomes a bottleneck in the information exchange between the system bus **200** and the expansion card **180**. The design of the expansion card and methods proposed herein minimizes the data transfer through the local bus **190** to reduce the effect of this bottleneck.

The system memory **130** is referred to as the main random-access memory (RAM) in the description herein. However, this is not intended to limit the system memory **130** to only RAM technology. Other possible computer storage media include, but are not limited to ROM, EEPROM, flash memory, or any other memory technology.

In the illustrated example, the GPU accelerator system is implemented on an expansion card **180** on which the one or more GPU's **240** are mounted. It should be noted that the GPU accelerator system GPU **240** is separate from and independent of any GPU on the standard video card **150** or other video driving hardware such as integrated graphics systems. Thus the computations performed on the expansion card **180** do not interfere with graphics display (including but not limited to manipulation and rendering of images).

Various brand of GPU are relevant. Under current technology, GPU's based on the GeForce series from NVIDIA Corporation or the Catalyst series from ATI/Advanced Micro Devices, Inc.

The output to a video monitor **170** is preferably through the video card **150** and not the GPU accelerator system **180**. The video card **150** is dedicated to the transfer of graphical information and connects to the motherboard **110** through a local bus **160** that is sometimes physically separate from the local bus **190** that connects the expansion card **180** to the motherboard **110**.

FIG. **2** is a block diagram illustrating the general architecture of the GPU accelerator system and specifically the expansion card **180** in which at least one GPU **240** and associated memories **210** and **250** are mounted. Electrical (signal) and mechanical coupling with a local bus **190** provides signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI, PCI-X, PCI Express, or functionally similar technology).

The GPU accelerator further preferably comprises one specifically designed accelerator controller **220**. Depending upon the implementation, the accelerator controller **220** is field programmable gate array (FPGA) logic, or custom built application-specific (ASIC) chip mounted in the expansion card **180**, and in mechanical and signal coupling with the GPU **240** and the associated memories **210** and **250**. During initial design, a controller can be partially or even fully implemented in software, in one example.

The controller **220** commands the storage and retrieval of arrays of data (on a conventional video card the arrays of data are represented as textures, hence the term 'texture' in this document refers to a data array unless specified otherwise and each element of the texture is a pixel of color information), execution of GPU programs (on a conventional video card these programs are called shaders, hence the term 'shader' in this document refers to a GPU program unless specified otherwise), and data transfer between the system bus **200** and the expansion card **180** through the local bus **190** which allows communication between the main CPU **120**, RAM **130**, and disk **140**.

Two memory banks **210** and **250** are mounted on the expansion card **180**. In some example, these memory banks separated in the hardware, as shown, or alternatively implemented as a single, logically partitioned memory component.

The reason to separate the memory into two partitions **210** **250** stems from the nature of the computations to which the GPU accelerator system is applied. The elements of computation (computational elements) are characterized by a single output variable. Such computational elements often include one or more equations. Computational elements are same or similar within a large population and are computed in parallel. An example of such a population is a layer of neurons in an artificial neural network (ANN), where all neurons are described by the same equation. As a result, some data and most of the algorithms are common to all computational elements within population, while most of the data and some algorithms are specific for each equation. Thus, one memory, the shader memory bank **210**, is used to store the shaders needed for the execution of the required computations and the parameters that are common for all computational elements and is coupled with the controller **220** only. The second memory, the texture memory bank **250**, is used to store all the necessary data that are specific for every computational element (including, but not limited to, input data, output data, intermediate results, and parameters) and is coupled with both the controller **220** and the GPU **240**.

The texture memory bank **250** is preferably further partitioned into four sections. The first partition **250** a is designed to hold the external input data patterns. The second partition **250***b* is designed to hold the data textures representing internal variables. The third partition **250***c* is designed to hold the data textures used as input at a particular computation step on the GPU **240**. The fourth partition **250***d* holds the data textures used to accommodate the output of a particular computational step on the GPU **240**. This partitioning scheme can be done logically, does not require hardware implementation. Also the partitioning scheme is also altered based on new designs or needs of the algorithms being employed. The reason for this partitioning is further explained in the Data Organization section, below.

A local bus interface **230** on the controller **220** serves as a driver that allows the controller **220** to communicate through the local bus **190** with the system bus **200** and thus the CPU **120** and RAM **130**. This local bus interface **230** is not intended to be limited to PCI related technology. Other drivers can be used to interface with comparable technology as a local bus **190**.

Data Organization

Each computational element discussed above has output variables that affect the rest of the system. For example in the case of a neural network it is the output of a neuron. A computational element also usually has several internal variables that are used to compute output variables, but are not exposed to the rest of the system, not even to other elements of the same population, typically. Each of these variables is represented as a texture. The important difference between output variables and internal variables is their access.

Output variables are usually accessed by any element in the system during every time step. The value of the output variable that is accessed by other elements of the system corresponds to the value computed on the previous, not the current, time step. This is realized by dedicating two textures to output variables—one holds the value computed during the previous time step and is accessible to all computational elements during the current time step, another is not accessible to other elements and is used to accumulate new values for the variable computed during the current time step. In-between time steps these two textures are switched, so that newly accumulated values serve as accessible input during the next time step, while the old input is replaced with new values of the variable. This switch is implemented by swapping the address pointers to respective textures as described in the System and Framework section.

Internal variables are computed and used within the same computational element. There is no chance of a race condition in which the value is used before it is computed or after it has already changed on the next time step because within an element the processing is sequential. Therefore, it is possible to render the new value of internal variable into the same texture where the old was read from in the texture memory bank. Rendering to more than one texture from a single shader is not implemented in current GPU architectures, so computational elements that track internal variables would have to have one shader per variable. These shaders can be executed in order with internal variables computed first, followed by output variables.

Further savings of texture memory is achieved through using multiple color components per pixel (texture element) to hold data. Textures can have up to four color components that are all processed in parallel on a GPU. Thus, to maximize the use of GPU architecture it is desirable to pack the data in such a way that all four components are used by the algorithm. Even though each computational element can have multiple variables, designating one texture pixel per element is ineffective because internal variables require one texture and output variables require two textures. Furthermore, different element types have different numbers of variables and unless this number is precisely a multiple of four, texture memory can be wasted.

A more reasonable packing scheme would be to pack four computational elements into a pixel and have separate textures for every variable associated with each computational element. In this case the packing scheme is identical for all textures, and therefore can be accessed using the same algorithm. Several ways to approach this packing scheme are outlined here. An example population of nine computational elements arranged in a 3×3 square (FIG. **5***a*) can be packed by element (FIG. **5***b*), by row (FIG. **5***c*), or by square (FIG. **5***d*).

Packing by element (FIG. **5***b*) means that elements **1**,**2**,**3**,**4** go into first pixel; **5**,**6**,**7**,**8** go into second pixel; **9** goes into third pixel. This is the most compact scheme, but not convenient because the geometrical relationship is not preserved during packing and its extraction depends on the size of the population.

Packing by row (column; FIG. **5***c*) means that elements **1**,**2**,**3** go into pixel (**1**,**1**); **3**,**4**,**5** go into pixel (**2**,**1**), **7**,**8**,**9** go into pixel (**3**,**1**). With this scheme the element's y coordinate in the population is the pixel's y coordinate, while the element's x coordinate in the population is the pixel's x coordinate times four plus the index of color component. Five by five populations in this case will use 2×5 texture, or 10 pixels. Five of these pixels will only use one out of four components, so it

wastes 37.5% of this texture. 25×1 population will use 6×1 texture (six pixels) and will waste 12.5% of it.

Packing by square (FIG. **5***d*) means that elements **1**,**2**,**4**,**5** go into pixel (**1**,**1**); **3**,**6** go into pixel (**1**,**2**); **7**,**8** go into pixel (**2**,**1**), and **9** goes into pixel (**2**,**2**). Both the row and the column of the element are determined from the row (column) of the pixel times two plus the second (first) bit of the color component index. Five by five populations in this case will use 3×3 texture, or 9 pixels. Four of these pixels will only use two out of four components, and one will only use one component, so it wastes 34.4% of this texture. This is more advantageous than packing by row, since the texture is smaller and the waste is also lower. 25×1 population on the other hand will use 13×1 texture (thirteen pixels) and waste >50% of it, which is much worse than packing by row.

In order to eliminate waste altogether the population should have even dimensions in the square packing, and it should have a number of columns divisible by four in row packing. Theoretically, the chances are approximately equivalent for both of these cases to occur, so the particular task and data sizes should determine which packing scheme is preferable in each individual case.

The System and Framework

FIG. **3** shows an exemplary implementation of the top level system and method that is used to control the computation. It is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented in the invention described herein and so the implementation is not intended to be limited to the following description and accompanying figure.

The method presented herein includes two execution streams that run on the CPU **120**—User Interaction Stream **302** and Data Output Stream **301**. These two streams preferably do not interact directly, but depend on the same data accumulated during simulations. They can be implemented as separate threads with shared memory access and executed on different CPUs in the case of multi-CPU computing environment. The third execution stream—Computational Stream **303**—runs on the GPU accelerator of the expansion card **180** and interacts with the User Interaction Stream **302** through initialization routines and data exchange in between simulations. The Computational Stream **303** interacts with the User Interaction Stream and the Data Output Stream through synchronization procedures during simulations.

The crucial feature of the interaction between the User Interaction Stream **302** and the Computational Stream **303** is the shift of priorities. Outside of the simulation, the system **100** is driven by the user input, thus the User Interaction Stream **302** has the priority and controls the data exchange **304** between streams. After the user starts the simulation, the Computational Stream **303** takes the priority and controls the data exchange between streams until the simulation is finished or interrupted **350**.

The user starts **300** the framework through the means of an operating system and interacts with the software through the user interaction section **305** of the graphic user interface **306** executed on the CPU **120**. The start **300** of the implementation begins with a user action that causes a GUI initialization **307**, Disk input/output initialization **308** on the CPU **120**, and controller initialization **320** of the GPU accelerator on the expansion card **180**. GUI initialization includes opening of the main application window and setting the interface tools that allow the user to control the framework. Disk I/O initialization can be performed at the start of the framework, or at the start of each individual simulation.

The user interaction **305** controls the setting and editing of the computational elements, parameters, and sources of external inputs. It specifies which equations should have their output saved to disk and/or displayed on the screen. It allows the user to start and stop the simulation. And it performs standard interface functions such as file loading and saving, interactive help, general preferences and others.

The user interaction **305** directs the CPU **120** to acquire the new external input textures needed (this includes but is not limited to loading from disk **140** or receiving them in real time from a recording device), parses them if necessary **309**, and initializes their transfer to the expansion card **180**, where they are stored **325** in the texture memory bank **250** by the controller **220**. The user interaction **305** also directs the CPU **120** to parse populations of elements that will be used in the simulation, convert them to GPU programs (shaders), compile them **310**, and initializes their transfer to the expansion card **180**, where they are stored **326** in the shader memory bank **210** by the controller **220**. This operation is accompanied by the upload **309** of the initial data into the input partition of the texture memory bank **250**, and stores the shader order of execution in the controller **220**. The user can perform operations **309** and **310** as many times as necessary prior to starting the simulation or between simulations.

The editing of the system between simulations is difficult to accomplish without the hardware implementation of the computational thread suggested herein. The system of equations (computational elements) is represented by textures that track variables plus shaders that define processing algorithms. As mentioned above, textures, shaders and other graphics related constructs can only be initialized within the rendering context, which is thread specific. Therefore textures and shaders can only be initialized in the computational thread.

Network editing is a user-interactive process, which according to the scheme suggested above happens in the User Interaction Stream **302**. The simulation software thus has to take the new parameters from the User Interaction Stream **302**, communicate them to the Computational Stream **303** and regenerate the necessary shaders and textures. This is hard to accomplish without a hardware implementation of the Computational Stream **303**. The Computational Stream **303** is forked from the User Interaction Stream and it can access the memory of the parent thread, but the reverse communication is harder to achieve. The controller **220** allows operations **309** and **310** to be performed as many times as necessary by providing the necessary communication to the User Interaction Stream **302**.

After execution of the input parser texture generation **309** and population parser shader generator and compiler **310** are performed at least once, the user has the option to initialize the simulation **311**. During this initialization the main control of the framework is transferred to the GPU accelerator system's accelerator controller **220** and computation **330** is started (see FIG. **4**; **420**). The user retains the ability to interrupt the simulation, change the input, or to change the display properties of the framework, but these interactions are queued to be performed at times determined by the controller-driven data exchange **314** and **316** to avoid the corruption of the data.

The progress monitor **312** is not necessary for performance, but adds convenience. It displays the percentage of completed time steps of the simulation and allows the user to plan the schedule using the estimates of the simulation wall clock times. Controller-driven data exchange **314** updates the display of the results **313**. Online screen output for the user selected population allows the user to monitor the activity and evaluate the qualitative behavior of the network. Simulations with unsatisfactory behavior can be terminated early to change parameters and restart. Controller-driven data

exchange **314** also drives the output of the results to disk **317**. Data output to disk for convenience can be done on an element per file basis. A suggested file format includes a leftmost column that displays a simulated time for each of the simulation steps and subsequent columns that display variable values during this time step in all elements with identical equations (e.g. all neurons in a layer of a neural network).

Controller-driven data exchange or input parser texture generator **316** allows the user to change input that is generated on the fly during the simulation. This allows the framework monitoring of the input that is coming from a recording device (video camera, microphone, cell recording electrode, etc) in real time. Similar to the initial input parser **309**, it preprocesses the input into a universal format of the data array suitable for texture generation and generates textures. Unlike the initial parser **309**, here the textures are transferred to hardware not whenever ready but upon the request of the controller **220**.

The controller **220** also drives the conditional testing **315** and **318** informs the CPU-bound streams whether the simulation is finished. If so, the control returns to the User Interaction Stream. The user then can change parameters or inputs (**309** and **310**), restart the simulation (**311**) or quit the framework (**390**).

SANNDRA (Synchronous Artificial Neuronal Network Distributed Runtime Algorithm; http://www.kinness.net/Docs/SANNDRA/html) was developed to accelerate and optimize processing of numerical integration of large non-homogenous systems of differential equations. This library is fully reworked in its version 2.x.x to support multiple computational backends including those based on multicore CPUs, GPUs and other processing systems. GPU based backend for SANNDRA-2.x.x can serve as an example practical software implementation of the method and architecture described above and pictorially represented in FIG. **3**.

To use SANNDRA, the application should create a TSimulator object either directly or through inheritance. This object will handle global simulation properties and control the User Interaction Stream, Data Output Stream, and Computational Stream. Through TSimulator::timestep( ), TSimulator::outfileInterval( ), and TSimulator::outmode( ), the application can set the time step of the simulation, the time step of disk output, and the mode of the disk output. The external input pattern should be packed into a TPattern object and bound to the simulation object through TSimulator::resetInputs( ) method. TSimulator::simLength( ) sets the length of the simulation.

The second step is to create at least one population of equations (Tpopulation object). Population holds one equation object TEquation. This object contains only a formula and does not hold element-specific data, so all elements of the population can share single TEquation.

The TEquation object is converted to a GPU program before execution. GPU programs have to be executed within a graphical context, which is stream specific. TSimulator creates this context within a Computational Stream, therefore all programs and data arrays that are necessary for computation have to be initialized within Computational Stream. Constructor of TPopulation is called from User Interaction Stream, so no GPU-related objects can be initialized in this constructor.

TPopulation::fillElements( ) is a virtual method designed to overcome this difficulty. It is called from within the Computational Stream after TSimulator::networkCreate( ) is called in the User Interaction Stream. A user has to override TPopulation::fillElements( ) to create TEquation and other computation related objects both element independent and element-specific. Element independent objects include subcomponents of TEquation and objects that describe how to handle interdependencies between variables implemented through derivatives of TGate class.

Element-specific data is held in TElement objects. These objects hold references to TEquation and a set of TGate objects. There is one TElement per population, but the size of data arrays within this object corresponds to population size. All TElement objects have to be added to the TSimulator list of elements by calling TSimulator::addUnit( ) method from TPopulation::fillElements( ).

Finally, TPopulation::fillElements( ) should contain a set of TElement::add*Dependency( ) calls for each element. Each of these calls sets a corresponding dependency for every TGate object. Here TGate object holds element independent part of dependency and TElement::add*Dependency( ) sets element-specific details.

System provided TPopulation handles the output of computational elements, both when they need to exchange the data and when they need to output it to disk. User implementation of TPopulation derivative can add screen output.

Listing 1 is an example code of the user program that uses a recurrent competitive field (RCF) equation:

Listing 1

```
uint16_t w = 3, h = 3;
static float m_compet = 0.5;
static float m_persist = 1.0;
class TCablePopRCF : public TPopulation
{
TEq_RCF* m_equation;
TGate* m_gatel;
TGate* m_gate2;
void createGatingStructure( )
{
m_gatel = new TGate(0);
m_gate2 = new TGate(1);
};
void createUnitStructure(TBasicUnit* u)
{
u->addO2OPInputDependency(m_gatel, 0., 0., 0.004, 0., 0, 0);
u->addFullDependency(m_gate2, population( ));
}
public: TCablePopRCF( ) : TPopulation("compCPU RCF", w, h, true) { };
~TCablePopRCF( ) {if(m_equation) delete m_equation;
   if(m_gatel) delete m_gatel;
   if(m_gate2) delete m_gate2;};
bool fillElements(TSimulator* sim);
};
bool TCablePopRCF::fillElements(TSimulatior* sim)
{
m_equation = new TEq_RCF(this, m_compet, m_persist);
createGatingStructure( );
for(size_t i = 0; i < xSize( ); ++i)
for(size_t j = 0; j < ySize( ); ++j)
{
TElement* u = new TCPUElement(this, m_equation, i, j);
sim->addUnit(u);
createUnitStructure(u);
}
Return true;
}
int
main( )
{
// Input pattern generation (309 in FIG.3)
uint32_t* pat = new uint32_t[w*h];
TRandom<float> randGen (0);
for(uint32_t I = 0; I < w*h; ++i)
pat[i] = randGen.random( );
Tpattern* p = new Tpattern(pat, w, h);
// Setting up the simulation
TSimulator* cableSim = new TSimulator("data"); //(308 and 320 in
FIG. 3)
```

-continued

Listing 1

```
cableSim->timestep(0.05); //(320 in FIG. 3)
cableSim->resetInputs(p); //(325 in FIG. 3)
cableSim->outfileInterval(0.1); //(308 in FIG. 3)
cableSim->outmode(SANNDRA::timefunc); //(308 in FIG. 3)
cableSim->simLength(60.0); //(320 in FIG. 3)
// Preparing the population
TPopulation* cablePop = new TCablePopRCF( ); //(310 in FIG. 3)
cableSim->networkCreate( ); //(326 in FIG. 3)
uint16_t user= 1;
while(user)
{
if(! cableSim->simulationStart(true, 1)) //(311 in FIG. 3)
exit(1);
std::cout<<"Repeat?\n"; //(305 in FIG. 3)
std::cin>>user; //(305 in FIG. 3)
if(user == 1)
cableSim->networkReset( ); //(305 in FIG. 3)
{
If(cableSim)
Delete cableSim; //Also deletes cablePop and its internals
exit(0);
};
```

FIG. **4** is a detailed flow diagram illustrating a part of an exemplary implementation of the bottom level system and method performed during the computation on the GPU accelerator of the expansion card **180** and is a more detailed view of the computational box **330** in FIG. **3**. FIG. **4** is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented.

With systems of equations that have complex interdependencies it is likely that the variable in some equation from a previous time step has to be used by some other equation after the new values of this variable are already computed for new time step. To avoid data confusion, the new values of variables should be rendered in a separate texture. After the time step is completed for all equations, these new values should be copied over old values so that they are used as input during the next time step. Copying textures is an expensive operation, computationally, but since the textures are referred to by texture IDs (pointers), swapping these pointers for input and output textures after each time step achieves the same result at a much lesser cost.

In the hardware solution suggested herein, ID swapping is equivalent to swapping the base memory address for two partitions of the texture memory bank **250**. They are swapped **485** during synchronization (**485**, **430**, and **455**) so that data transfer **445** and the computation **435**-**487** proceeds immediately and in parallel with data transfer as shown in FIG. **4**. A hardware solution allows this parallelism through access of the controller **220** to the onboard texture memory bank **250**.

The main computation and data exchange are executed by the controller **220**. It runs three parallel substreams of execution: Computational Substream **403**, Data Output Substream **402**, and Data Input Substream **404**. These streams are synchronized with each other during the swap of pointers **485** to the input and output texture memory partitions of the texture memory bank **250** and the check for the last iteration **487**. Algorithmically, these two operations are a single atomic operation, but the block diagram shows them as two separate blocks for clarity.

The Computational Substream **403** performs a computational cycle including a sequential execution of all shaders that were stored in the shader memory bank **210** using the appropriate input and output textures. To begin the simulation the controller **220** initializes three execution substreams **403**, **402**, and **404**. On every simulation step, the Computational Substream **403** determines which textures the GPU **240** will need to perform the computations and initiates the upload **435** of them onto the GPU **240**. The GPU **240** can communicate directly with the texture memory bank **250** to upload the appropriate texture to perform the computations. The controller **220** also pulls the first shader (known by the stored order) from the shader memory bank **210** and uploads **450** it onto the GPU **240**.

The GPU **240** executes the following operations in this order: performs the computation (execution of the shader) **470**; tells the controller **220** that it is done with the computations for the current shader; and after all shaders for this particular equation are executed sends **480** the output textures to the output portion of the texture memory bank **250**. This cycle continues through all of the equations based on the branching step **482**.

An example shader that performs fourth order Runge-Kutta numerical integration is shown in Listing 2 using GLSL notation;

Listing 2

```
uniform sampler2DRect Variable;
uniform float integration_step;
float halfstep = integration_step*0.5;
float fl_6step = integration_step/6.0;
vec4 output = texture2DRect(Variable, gl_TexCoord[0].st);
// define equation( ) here
vec4 rungekutta4(vec4 x)
{
const vec4 kl = equation(x);
const vec4 k2 = equation(x + halfstep*kl);
const vec4 k3 = equation(x + halfstep*k2);
const vec4 k4 = equation(x + integration step*k3);
return fl_6step*(k1 + 2.0*(k2 + k3) + k4);
}
Void main(void)
{
output += rungekutta4(output);
gl_FragColor = output;
}
```

The shader in Listing 2 can be executed on conventional video card. Using the controller **220** this code can be further optimized, however. Since the integration step does not change during the simulation, the step itself as well as the halfstep and ⅙ of the step can be computed once per simulation, and updated in all shaders by a shader update procedures **310**, **326** discussed above.

After all of the equations in the computational cycle are computed the main execution substream **403** on the controller **220** can switch **485** the reference pointers of the input and output portions of the texture memory bank **250**.

The two other substreams of execution on the controller **220** are waiting (blocks **430** and **455**, respectively) for this switch to begin their execution. The Data Input Substream **404** is controlling **440** the input of additional data from the CPU **120**. This is necessary in cases where the simulation is monitoring the changing input, for example input from a video camera or other recording device in the real time. This substream uploads new external input from the CPU **120** to the texture memory bank **250** so it can be used by the main computational substream **403** on the next computational step and waits for the next iteration **475**. The Data Output Substream **445** controls the output of simulation results to the CPU **120** if requested by the user. This substream uploads the results of the previous step to the main RAM **130** so that the CPU **120** can save them on disk **140** or show them on the results display **313** and waits for the next iteration **460**.

Since the Computational Substream **403** determines the timing of input **440** and output **445** data transfers, these data transfers are driven by the controller **220**. To further reduce the data transfer overhead (and disk **140** overhead also) the controller **220** initiates transfer only after selected computational steps. For example, if the experimental data that is simulated was recorded every 10 milliseconds (msec) and the simulation for better precision was computed every 1 msec, then only every tenth result has to be transferred to match the experimental frequency.

This solution stores two copies of output data, one in the expansion card texture memory bank **250** and another in the system RAM **130**. The copy in the system RAM **130** is accessed twice: for disk I/O and screen visualization **313**. An alternative solution would be to provide CPU **120** with a direct read access to the onboard texture memory bank **250** by mapping the memory of the hardware onto a global memory space. The alternative solution will double the communication through the local bus **190**. Since the goal discussed herein is reducing the information transfer through the local bus **190**, the former solution is favored.

The main substream **403** determines if this is the last iteration **487**. If it is the last iteration, the controller **220** waits for the all of the execution substreams to finish **490** and then returns the control to the CPU **120**, otherwise it begins the next computational cycle.

This repeats through all of the computational cycles of the simulation.

CONCLUSION

This GPU accelerator system offers the following potential advantages:

1. Limited computations on the CPU **120**. The CPU **120** is only used for user input, sending information to the controller **220**, receiving output after each computational cycle (or less frequently as defined by the user), writing this output to disk **140**, and displaying this output on the monitor **170**. This frees the CPU **120** to execute other applications and allows the expansion card to run at its full capacity without being slowed down by extensive interactions with the CPU **120**.

2. Minimizing data transfer between the expansion card **180** and the system bus **200**. All of the information needed to perform the simulations will be stored on the expansion card **180** and all simulations will take place on it. Furthermore, whatever data transfer remains necessary will take place in parallel with the computation, thus reducing the impact of this transfer on the performance.

3. New way to execute GPU programs (shaders). Previously, the CPU **120** had full control over the order of shader's execution and was required to produce specific commands on every cycle to tell the GPU **240** which shader to use. With the invention disclosed herein, shaders will initially be stored on the shader memory bank **210** on the expansion card **180** and will be sent to the GPU **240** for execution by the general purpose controller **220** located on the expansion card.

4. Multiple parallelisms. The GPU **240** is inherently parallel and is well suited to perform parallel computations. In parallel with the GPU **240** performing the next calculation, the controller **220** is uploading the data from the previous calculation into main memory **130**. Furthermore, the CPU **120** at the same time uses uploaded previous results to save them onto disk **140** and to display them on the screen through the system bus **200**.

5. Reuse of existing and affordable technology. All hardware used in the invention and mentioned here-in are based on currently available and reliable components. Further advance of these components will provide straightforward improvements of the invention.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. A computer system, comprising:

a central processing unit to receive input data;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the first memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one graphics processing unit to perform a sequence of computations on the at least a portion of the input data so as to generate output data, intermediate computations in the sequence of computations yielding intermediate results; and

accelerator memory, operably coupled to the graphic processing unit, to store the results of the plurality of sequential computations; and

a controller, operably coupled to the at least one graphics processing unit and the accelerator memory, to transfer the at least a portion of the input data into the accelerator memory, and to transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the sequence of computations by the at least one graphic processing unit.

2. The computer system of claim **1**, wherein the central processing unit is configured to receive the input data in response to a user interaction.

3. The computer system of claim **1**, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one graphics processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

4. The computer system of claim **1**, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

5. The computer system of claim **1**, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

6. The computer system of claim **1**, wherein accelerator memory comprises:

a first memory bank to store parameters common to all of the computations in the sequence of computations; and

a second memory bank to store data specific to at least one computation in the sequence of computations.

7. The computer system of claim **1**, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

8. The computer system of claim **1**, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one graphics processing unit has begun to perform another sequence of computations.

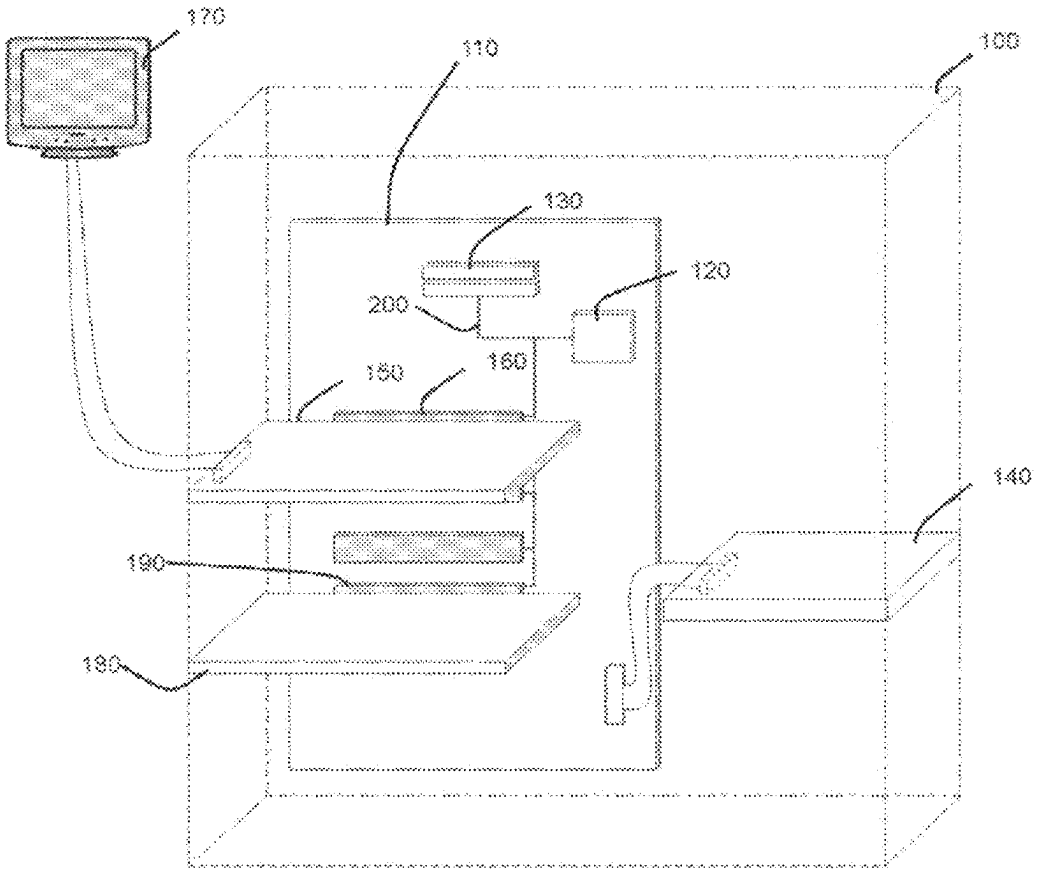


FIG. 1

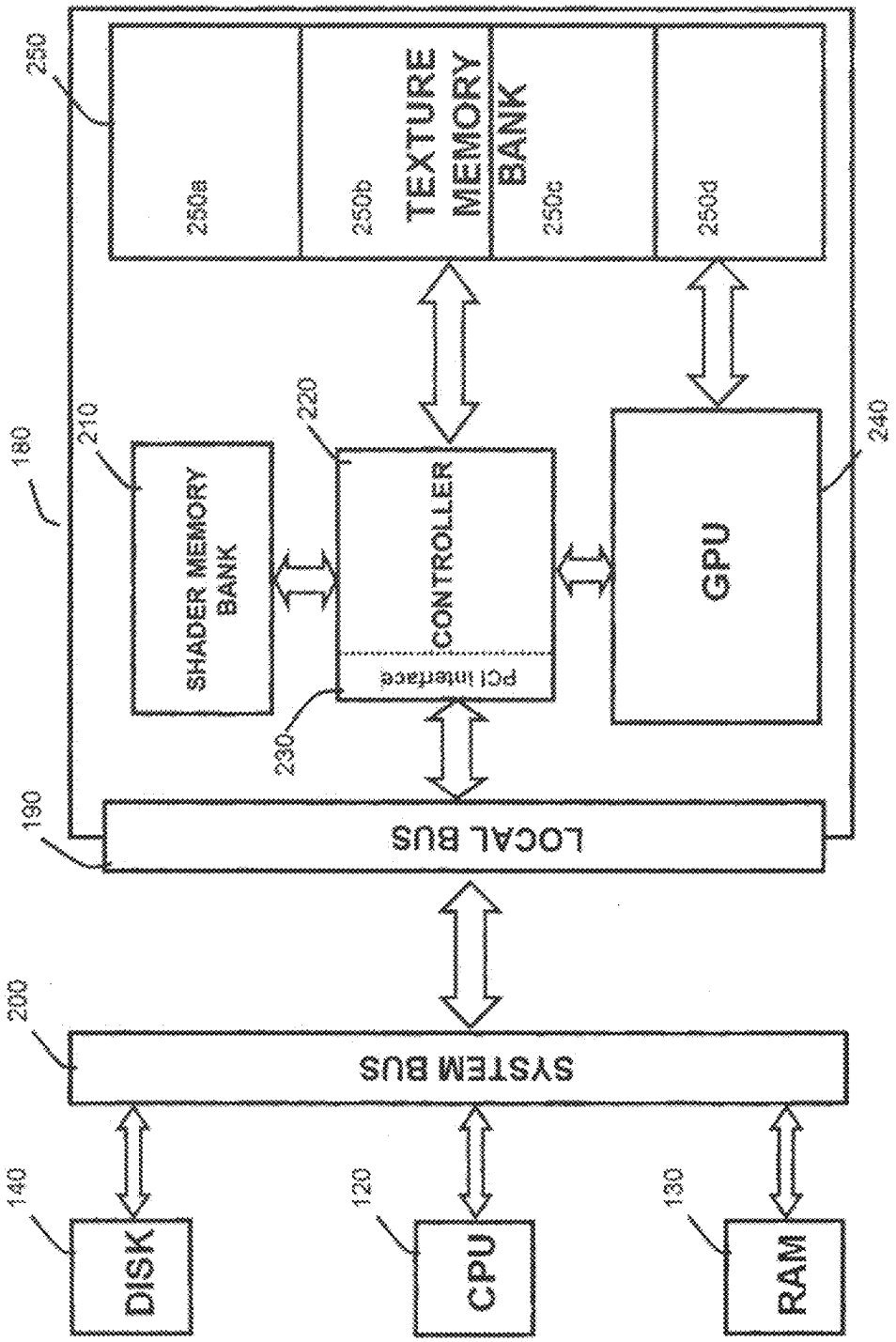

250a
250b
TEXTURE MEMORY BANK
250c
250d
250
SHADER MEMORY BANK
210
CONTROLLER
220
PCI interface
230
GPU
240
180
LOCAL BUS
190
SYSTEM BUS
200
DISK
140
CPU
120
RAM
130

FIG. 2

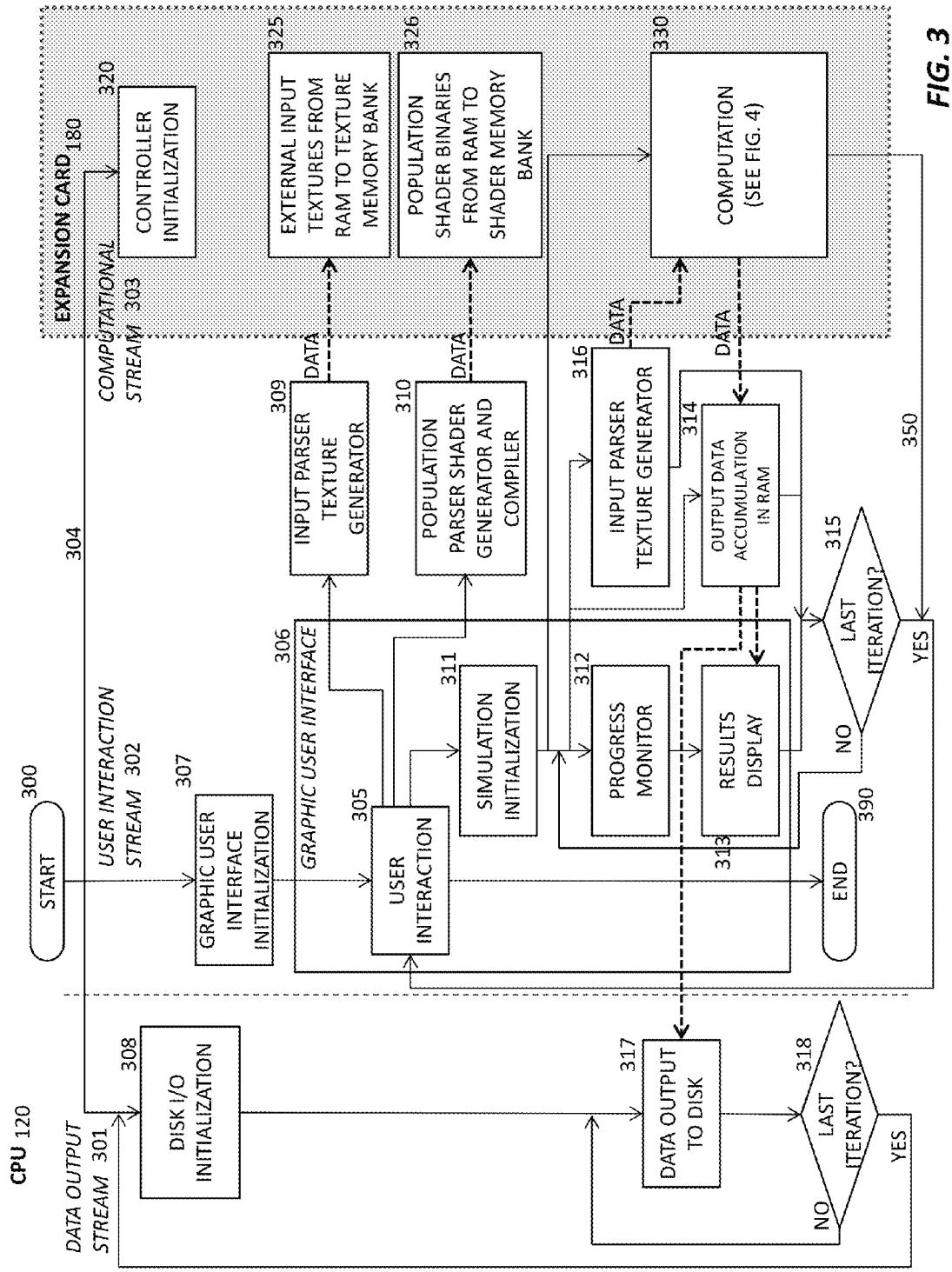

EXPANSION CARD 180
CONTROLLER INITIALIZATION
320
EXTERNAL INPUT TEXTURES FROM RAM TO TEXTURE MEMORY BANK
325
POPULATION SHADER BINARIES FROM RAM TO SHADER MEMORY BANK
326
COMPUTATION (SEE FIG. 4)
330
COMPUTATIONAL STREAM 303
DATA
INPUT PARSER TEXTURE GENERATOR
309
POPULATION PARSER SHADER GENERATOR AND COMPILER
310
INPUT PARSER TEXTURE GENERATOR
316
OUTPUT DATA ACCUMULATION IN RAM
314
350
304
LAST ITERATION?
315
YES
NO
GRAPHIC USER INTERFACE
306
SIMULATION INITIALIZATION
311
PROGRESS MONITOR
312
RESULTS DISPLAY
313
USER INTERACTION STREAM 302
START
300
GRAPHIC USER INTERFACE INITIALIZATION
307
USER INTERACTION
305
END
390
CPU 120
DISK I/O INITIALIZATION
308
DATA OUTPUT STREAM 301
DATA OUTPUT TO DISK
317
LAST ITERATION?
318
YES
NO

FIG. 3

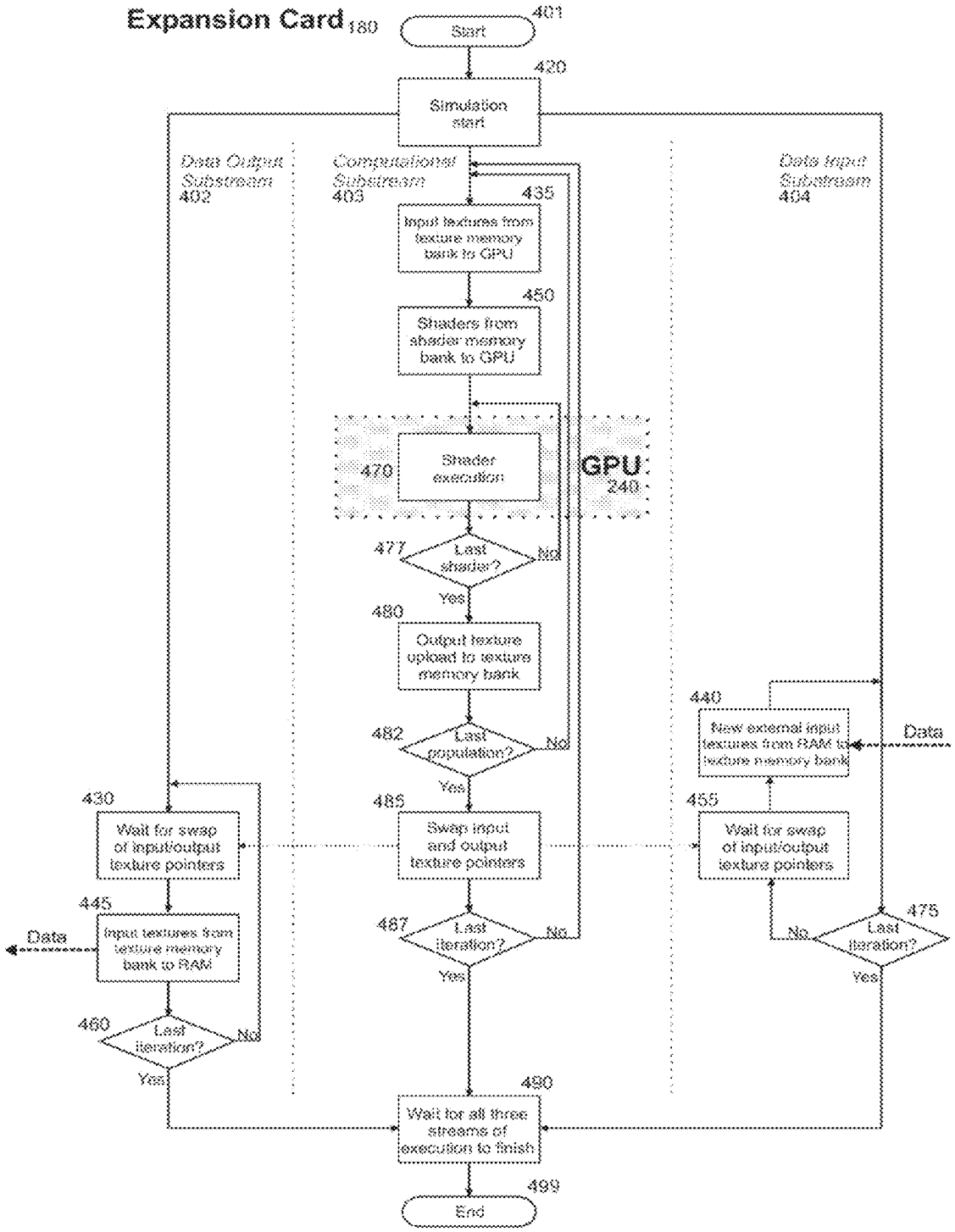
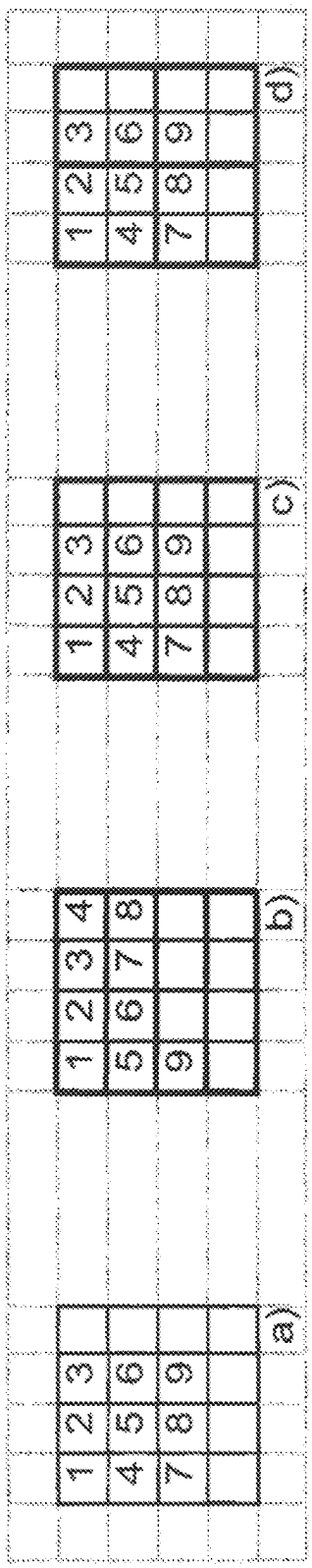

Expansion Card 180
Start
401
420
Simulation start
Data Output Substream 402
Computational Substream 403
Data Input Substream 404
435
Input textures from texture memory bank to GPU
450
Shaders from shader memory bank to GPU
470
Shader execution
GPU 240
477
Last shader?
No
Yes
480
Output texture upload to texture memory bank
482
Last population?
No
Yes
440
New external input textures from RAM to texture memory bank
Data
430
Wait for swap of input/output texture pointers
485
Swap input and output texture pointers
455
Wait for swap of input/output texture pointers
445
Input textures from texture memory bank to RAM
Data
467
Last iteration?
No
Yes
475
Last iteration?
No
Yes
460
Last iteration?
No
Yes
490
Wait for all three streams of execution to finish
499
End

FIG 4



Bold lines show the packing of data into pixels with four color components.

FIG. 5

Since the Computational Substream **403** determines the timing of input **440** and output **445** data transfers, these data transfers are driven by the controller **220**. To further reduce the data transfer overhead (and disk **140** overhead also) the controller **220** initiates transfer only after selected computational steps. For example, if the experimental data that is simulated was recorded every 10 milliseconds (msec) and the simulation for better precision was computed every 1 msec, then only every tenth result has to be transferred to match the experimental frequency.

This solution stores two copies of output data, one in the expansion card texture memory bank **250** and another in the system RAM **130**. The copy in the system RAM **130** is accessed twice: for disk I/O and screen visualization **313**. An alternative solution would be to provide CPU **120** with a direct read access to the onboard texture memory bank **250** by mapping the memory of the hardware onto a global memory space. The alternative solution will double the communication through the local bus **190**. Since the goal discussed herein is reducing the information transfer through the local bus **190**, the former solution is favored.

The main substream **403** determines if this is the last iteration **487**. If it is the last iteration, the controller **220** waits for the all of the execution substreams to finish **490** and then returns the control to the CPU **120**, otherwise it begins the next computational cycle.

This repeats through all of the computational cycles of the simulation.

CONCLUSION

This GPU accelerator system offers the following potential advantages:

1. Limited computations on the CPU **120**. The CPU **120** is only used for user input, sending information to the controller **220**, receiving output after each computational cycle (or less frequently as defined by the user), writing this output to disk **140**, and displaying this output on the monitor **170**. This frees the CPU **120** to execute other applications and allows the expansion card to run at its full capacity without being slowed down by extensive interactions with the CPU **120**.

2. Minimizing data transfer between the expansion card **180** and the system bus **200**. All of the information needed to perform the simulations will be stored on the expansion card **180** and all simulations will take place on it. Furthermore, whatever data transfer remains necessary will take place in parallel with the computation, thus reducing the impact of this transfer on the performance.

3. New way to execute GPU programs (shaders). Previously, the CPU **120** had full control over the order of shader's execution and was required to produce specific commands on every cycle to tell the GPU **240** which shader to use. With the invention disclosed herein, shaders will initially be stored on the shader memory bank **210** on the expansion card **180** and will be sent to the GPU **240** for execution by the general purpose controller **220** located on the expansion card.

4. Multiple parallelisms. The GPU **240** is inherently parallel and is well suited to perform parallel computations. In parallel with the GPU **240** performing the next calculation, the controller **220** is uploading the data from the previous calculation into main memory **130**. Furthermore, the CPU **120** at the same time uses uploaded previous results to save them onto disk **140** and to display them on the screen through the system bus **200**.

5. Reuse of existing and affordable technology. All hardware used in the invention and mentioned here-in are based on currently available and reliable components. Further advance of these components will provide straightforward improvements of the invention.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. A computer system, comprising:

a central processing unit to receive input data;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the first memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one graphics processing unit to perform a sequence of computations on the at least a portion of the input data so as to generate output data, intermediate computations in the sequence of computations yielding intermediate results; and

accelerator memory, operably coupled to the graphic processing unit, to store the results of the plurality of sequential computations; and

a controller, operably coupled to the at least one graphics processing unit and the accelerator memory, to transfer the at least a portion of the input data into the accelerator memory, and to transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the sequence of computations by the at least one graphic processing unit.

2. The computer system of claim **1**, wherein the central processing unit is configured to receive the input data in response to a user interaction.

3. The computer system of claim **1**, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one graphics processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

4. The computer system of claim **1**, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

5. The computer system of claim **1**, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

6. The computer system of claim **1**, wherein accelerator memory comprises:

a first memory bank to store parameters common to all of the computations in the sequence of computations; and

a second memory bank to store data specific to at least one computation in the sequence of computations.

7. The computer system of claim **1**, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

8. The computer system of claim **1**, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one graphics processing unit has begun to perform another sequence of computations.

9. The computer system of claim **8**, wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one graphics processing unit.

10. The computer system of claim **1**, wherein the controller is configured to control execution of the sequence of computations by the at least one graphics processing unit.

11. The computer system of claim **1**, further comprising:

at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central processor unit, to acquire the input data in real time.

12. A method of performing a sequence of computations on a computer system comprising a central processing unit (CPU), a main memory operably coupled to the central processing unit via a bus, an accelerator operably coupled to the CPU and the main memory via the bus, the accelerator comprising a graphics processing unit (GPU) and an accelerator memory, the method comprising:

(A) performing, by the GPU, the sequence of computations on a first portion of the input data so as to generate a first portion of the output data, intermediate computations in the sequence of computations yielding intermediate results;

(B) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the input data from the main memory to the accelerator via the bus; and

(C) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the output data from the accelerator memory to the main memory via the bus.

13. The method of claim **12**, further comprising:

storing the input data in the main memory in response to a user interaction.

14. The method of claim **12**, further comprising:

receiving the input data at a first rate; and

wherein (A) comprises performing the sequence of computations at a second rate different than the first rate.

15. The method of claim **12**, wherein (A) comprises:

generating an output representative of an output of at least one neuron in an artificial neural network.

16. The method of claim **12**, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory without transferring any of the intermediate results of the plurality of sequential computations from the accelerator memory to the main memory so as to reduce data transfer via the bus.

17. The method of claim **12**, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory after the GPU has begun to perform another sequence of computations.

18. The method of claim **17**, wherein (C) further comprises:

initiating transfer of the second portion of the output data in parallel with performance of at least one computation in the other sequence of computations.

19. The method of claim **12**, further comprising:

acquiring the input data in real time with at least one of a video camera, a microphone, or a cell recording electrode operably coupled to the CPU.

20. The method of claim **12**, further comprising:

storing parameters common to all of the computations in the sequence of computations in a first memory bank in the accelerator memory; and

storing data specific to at least one computation in the sequence of computations in a second memory bank in the accelerator memory.

* * * * *

PTO/AIA/53 (09-12)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION: CONSENT OF ASSIGNEE; STATEMENT OF NON-ASSIGNMENT	Docket Number (Optional) NRLA-001US04

This is part of the application for a reissue patent based on the original patent identified below.

Name of Patentee(s)
Neurala, Inc.

Patent Number	Date Patent Issued
9,189,828	11/17/2015

Title of Invention
GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

1. ☑ Filed herein is a statement under 37 CFR 3.73(c). (Form PTO/AIA/96)

2. ☐ Ownership of the patent is in the inventor(s), and no assignment of the patent is in effect.

One of boxes 1 or 2 above must be checked. If multiple assignees, complete this form for each assignee. If box 2 is checked, skip the next entry and go directly to "Name of Assignee."

The written consent of all assignees and inventors owning an undivided interest in the original patent is included in this application for reissue.

The assignee(s) owning an undivided interest in said original patent is/are Neurala, Inc., and the assignee(s) consents to the accompanying application for reissue.

Name of assignee/inventor (if not assigned)
Neurala, Inc.

Signature	Date
/Christopher Max Colice/	12/29/2020

Typed or printed name and title of person signing for assignee (if assigned)

Christopher Max Colice, Reg. No. 65634

This collection of information is required by 37 CFR 1.172. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Inventor:	Anatoli Gorchetchnikov	Confirmation No.:	To Be Assigned
Application No.:	To Be Assigned	Group Art Unit:	To Be Assigned
Filed:	December 29, 2020	Examiner:	To Be Assigned

For: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the above-captioned application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected on the listing of the claims which begins on page 3 of this paper.

Remarks and Statement under 37 C.F.R. 1.173(c) begin on page 15 of this paper.

IN THE SPECIFICATION:

Please replace the paragraph immediately following the heading "Related Applications" with the following paragraph. The amendments to this paragraph are indicated by underlining and brackets.

The present application is a reissue continuation application of U.S. Application No. 15/808,201, which was filed on Nov. 9, 2017 as a broadening reissue application of U.S. Pat. No. 9,189,828, filed Jan. 3, 2014, which claims a priority benefit, under 35 U.S.C. §120, as a continuation of U.S. application Ser. No. 11/860,254, now U.S. Pat. No. 8,648,867 B2, filed Sep. 24, 2007, entitled "Graphic Processor Based Accelerator System and Method," which in turn claims the priority benefit, under 35 U.S.C. §119(e), of U.S. Application No. 60/826,892, filed Sep. 25, 2006. Each of the above-identified applications is incorporated herein by reference in its entirety. More than one reissue application has been filed for the reissue of U.S. Pat. No. 9,189,828, including this application and U.S. Application No. 15/808,201.

IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Changes to any amended claims are indicated by [[double brackets]], ~~strikethrough~~ and/or <u>underlining</u>. This listing also reflects any cancellation and/or addition of claims.

1. A computer system, comprising:

a central processing unit to receive input data;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the [first] main memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one graphics processing unit to perform a sequence of computations on the at least a portion of the input data so as to generate output data, the sequence of computations representing an artificial neural network, intermediate computations in the sequence of computations representing respective layers of the artificial neural network and yielding intermediate results; and

accelerator memory, operably coupled to the [graphic] at least one graphics processing unit, to store the results of the [plurality of sequential] sequence of computations; and

a controller, operably coupled to the at least one graphics processing unit and the accelerator memory, to initialize textures and shaders in the accelerator memory for performing the sequence of computations, to control performance of the sequence of computations by the at least one graphics processing unit, to transfer the at least a portion of the input data into the accelerator memory during performance of the intermediate computations in the sequence of computations by the at least one graphics processing unit, and to transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the intermediate computations in the sequence of computations by the at least one [graphic] graphics processing unit.

2. The computer system of claim 1, wherein the central processing unit is configured to receive the input data in response to a user interaction.

3. The computer system of claim 1, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one graphics processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

4. The computer system of claim 1, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

5. The computer system of claim 1, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

6. The computer system of claim 1, wherein accelerator memory comprises:

a first memory bank to store parameters common to all of the computations in the sequence of computations; and

a second memory bank to store data specific to at least one computation in the sequence of computations.

7. The computer system of claim 1, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

8. The computer system of claim 1, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one graphics processing unit has begun to perform another sequence of computations.

9. The computer system of claim 8, wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one graphics processing unit.

10. The computer system of claim 1, wherein the controller is configured to control execution of the sequence of computations by the at least one graphics processing unit.

11. The computer system of claim 1, further comprising:

at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central [processor] processing unit, to acquire the input data in real time.

12. A method of performing a sequence of computations representing an artificial neural network on a computer system comprising a central processing unit (CPU), a main memory operably coupled to the central processing unit via a bus, an accelerator operably coupled to the CPU and the main memory via the bus, the accelerator comprising a graphics processing unit (GPU) and an accelerator memory, the method comprising:

(A) performing, by the GPU, the sequence of computations on a first portion of [the] input data so as to generate a first portion of [the] output data, the first portion of the output data representing an output of a neuron in a first layer of the artificial neural network, intermediate computations in the sequence of computations yielding intermediate results, wherein performing the sequence of computations on the first portion of the input data comprises (i) assigning an output variable to a first texture and a second texture, the output variable being included in a first computational element of a plurality of computational elements, the plurality of computational elements representing the sequence of computations and (ii) accumulating a first value for the output variable in the first texture during a first time step;

(B) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the input data from the main memory to the accelerator via the bus; [and]

(C) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the output data from the accelerator memory to the main memory via the bus, the second portion of the output data representing an output of a neuron in a second layer in the artificial neural network; and

(D) performing, by the GPU, the sequence of computations on the second portion of the input data, wherein performing the sequence of computations on the second portion of the input data comprises (i) accumulating a second value for the output variable in the second texture during a second time step and (ii) making the first value of the output variable in the first texture accessible to other computational elements in the plurality of computational elements during the second time step.

13. The method of claim 12, further comprising:

storing the input data in the main memory in response to a user interaction.

14. The method of claim 12, further comprising:

receiving the input data at a first rate; and

wherein (A) comprises performing the sequence of computations at a second rate different than the first rate.

15. Cancel claim 15.

16. The method of claim 12, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory without transferring any of the intermediate results of the plurality of sequential computations from the accelerator memory to the main memory so as to reduce data transfer via the bus.

17. The method of claim 12, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory after the GPU has begun to perform another sequence of computations.

18. The method of claim 17, wherein (C) further comprises:

initiating transfer of the second portion of the output data in parallel with performance of at least one computation in the other sequence of computations.

19. The method of claim 12, further comprising:

acquiring the input data in real time with at least one of a video camera, a microphone, or a cell recording electrode operably coupled to the CPU.

20. The method of claim 12, further comprising:

storing parameters common to all of the computations in the sequence of computations in a first memory bank in the accelerator memory; and

storing data specific to at least one computation in the sequence of computations in a second memory bank in the accelerator memory.

21. A method of performing a sequence of computations representing an artificial neural network, the method comprising:

receiving, at a central processing unit (CPU), first input data acquired from an external system in real time;

initializing, by a controller operably coupled to a graphics processing unit (GPU), textures and shaders in a memory operably coupled to the GPU;

transferring the first input data received by the CPU to the memory operably coupled to the GPU;

performing, by the graphics processing unit (GPU), a first computation in the sequence of computations on the first input data based on the textures and shaders to generate first output data, computations in the sequence of computations representing respective layers of neurons in the artificial neural network, an output of the first computation in the sequence of computations representing an output of a first neuron in a first layer in the artificial neural network;

storing, in the memory operably coupled to the GPU, the first input data and the first output data; and

transferring second input data acquired from the external system in real time into the memory operably coupled to the GPU after the GPU starts the first computation and before the GPU starts a second computation of the sequence of computations, an output of the second computation in the sequence of computations representing an output of a second neuron in a second layer in the artificial neural network.

22. The method of claim 21, wherein transferring the second input data comprises transferring the second input data via a bus operably coupled to the CPU.

23. The method of claim 21, further comprising:

transferring the first output data from the memory to another memory during the second computation in the sequence of computations.

24. The method of claim 23, further comprising:

storing intermediate results of the sequence of computations in the memory, and

wherein transferring the first output data from the memory to the other memory occurs without transferring the intermediate results of the sequence of computations.

25. The method of claim 23, wherein transferring the second input data and transferring the first output data occurs in parallel.

26. The method of claim 21, further comprising:

storing, in a first memory partition of the memory, parameters common to all of the computations in the sequence of computations.

27. The method of claim 26, further comprising:

storing, in a second memory partition of the memory, data specific to the first computation in the sequence of computations.

28. The method of claim 27, further comprising:

storing, in the second memory partition, external input data patterns, representations of internal variables, an input of the computation in the sequence of computations, and the output of the computation in the sequence of computations.

29. The method of claim 21, wherein storing the first output data comprises:

accumulating, in the memory, outputs of computational elements executed by the GPU in performing the first computation in the sequence of computations.

30. The method of claim 21, further comprising:

storing, in the memory, an output of a previous computation in the sequence of computations; and

accessing, by the GPU, the output of the previous computation during performance of the computation in the sequence of computations.

31. The method of claim 21, wherein performing the first computation comprises executing a plurality of computational elements representing a layer of neurons in an artificial neural network.

32. The method of claim 31, wherein all neurons in the layer of neurons are described by the same equation.

33. The method of claim 21, further comprising:

acquiring the second input data with at least one of a video camera, a microphone, or a cell recording electrode.

34. The method of claim 21, further comprising:

loading the second input data from disk.

35. A system for performing a sequence of computations, the system comprising:

a camera to generate input data in real time;

a first memory partition;

a second memory partition operably coupled to the first memory partition; and

a processing unit, operably coupled to the camera, the first memory partition, and the second memory partition, to perform the sequence of computations on a first portion of the input data so as to generate a first portion of output data, intermediate computations in the sequence of computations yielding intermediate results, the first portion of the output data representing an output of an artificial neural network,

wherein the first memory partition is configured to transfer a second portion of the input data to the second memory partition in parallel with performance the sequence of computations by the processing unit,

wherein the second memory partition is configured to transfer a second portion of the output data to the first memory partition in parallel with performance the sequence of computations by the processing unit, and

wherein the sequence of computations represents the artificial neural network, each neuron in the artificial neural network has an output variable assigned to a first texture and a second texture in the memory, the first texture holds a first value of the output variable computed during a previous time step of the sequence of computations and accessible to other neurons in the neural network during a current time step of the sequence of computations and the second texture accumulates a second value of the output variable computed during the current time step.

36. The system of claim 35, wherein the first memory partition and the second memory partition are logical partitions.

37. The system of claim 35, wherein the processing unit is comprises a graphics processing unit (GPU).

38. The system of claim 35, wherein the processing unit is configured to receive the input data at a first rate and to perform the sequence of computations at a second rate is different than the first rate.

39. The system of claim 35, wherein the second memory partition is configured to transfer the second portion of the output data to the first memory partition without transferring any of the intermediate results to the first memory partition.

40. A system for executing an artificial neural network, the system comprising:

a central processing unit (CPU) to provide first input data;

a memory, operably coupled to the CPU, to store the first input data in a first partition, referenced by a first pointer, before computing a first layer of neurons of the artificial neural network;

a processing unit, operably coupled to the memory, to perform, during computation of the first layer of neurons, at least one calculation on the first input data so as to generate first output data, the first output data representing an output of at least one neuron in the first layer of neurons; and

a controller, operably coupled to the processing unit and the memory, to:

store the first output data in a second partition of the memory, the second partition referenced by a second pointer, and to swap the first pointer with the second pointer at the end of the computation of the first layer of neurons, such that the first output data becomes an input for a second layer of neurons of the artificial neural network,

transfer the first output data to another memory during computation of the second layer of neurons, and

dictate an order of execution of instructions to the processing unit to perform the computation of the first layer of neurons.

41. The system of claim 40, wherein the processing unit comprises a graphics processing unit.

42. The system of claim 40, wherein the controller is configured to send instructions for performing the at least one calculation to the processing unit.

43. The system of claim 40, wherein the memory further comprises:

a third partition to store internal variables; and

a fourth partition to store data used as input at a particular layer of neurons of the artificial neural network.

44. A computer system, comprising:

a central processing unit to receive input data acquired from an external system;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the main memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one processing unit to perform a sequence of computations representing an artificial neural network on the at least a portion of the input data so as to generate output data, intermediate computations in the sequence of computations representing layers of the neural network and yielding intermediate results; and

accelerator memory, operably coupled to the at least one processing unit, to store the results of the sequence of computations; and

a controller, operably coupled to the at least one processing unit and the accelerator memory, to control transfer of the at least a portion of the input data into the accelerator memory during performance of the intermediate computations in the sequence of computations by the at least one processing unit, to control transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the intermediate computations in the sequence of computations by the at least one processing unit, and to control performance of the sequence of computations by the at least one processing unit.

45. The computer system of claim 44, wherein the central processing unit is configured to receive the input data in response to a user interaction.

46. The computer system of claim 44, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

47. The computer system of claim 44, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

48. The computer system of claim 44, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

49. The computer system of claim 44, wherein accelerator memory comprises:

a first memory partition to store parameters common to all of the computations in the sequence of computations; and

a second memory partition to store data specific to at least one computation in the sequence of computations.

50. The computer system of claim 44, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

51. The computer system of claim 44, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one processing unit has begun to perform another sequence of computations.

52. The computer system of claim 51, wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one processing unit.

53. The computer system of claim 44, wherein the controller is configured to control execution of the sequence of computations by the at least one processing unit.

54. The computer system of claim 44, further comprising:

at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central processing unit, to acquire the input data in real time.

55. The computer system of claim 1, wherein the controller is configured to inform the central processing unit that the sequence of computations is finished.

56. The computer system of claim 1, wherein the controller is configured to reduce a processing load on the central processing unit.

57. The computer system of claim 1, wherein the controller is configured to reduce interactions between the central processing unit and the accelerator.

58. (New) A method of executing computations representing an artificial neural network on a computer system comprising at least one central processing unit (CPU), a processing unit, a first memory partition, and a second memory partition, the method comprising:

executing, by the at least one CPU, a user interaction stream, the user interaction stream controlling transfer of inputs to the artificial neural network to the first memory partition and the second memory partition; and

executing, by the processing unit, a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network.

59. (New) The method of claim 58, wherein the user interaction stream controls data exchange between the user interaction stream and the computational stream outside of execution of the computations representing the artificial neural network.

60. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of computational elements of the computations representing the artificial neural network.

61. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of parameters of the computations representing the artificial neural network.

62. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of parameters of the inputs to the artificial neural network.

63. (New) The method of claim 58, wherein executing the user interaction stream comprises:

specifying an output to be saved to disk and/or displayed on a screen.

64. (New) The method of claim 58, wherein executing the user interaction stream comprises:

parsing elements to be used in the computations representing the artificial neural network.

65. (New) The method of claim 64, wherein the processing unit comprises a graphics processing unit (GPU) and executing the user interaction stream further comprises:

converting the elements into GPU programs.

66. (New) The method of claim 65, wherein executing the user interaction stream comprises:

compiling the GPU programs.

67. (New) The method of claim 66, wherein executing the user interaction stream comprises:

transferring the GPU programs to the second memory partition.

68. (New) The method of claim 58, further comprising:

executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk.

Remarks and Statement under 37 C.F.R. 1.173(c)

Entry and consideration of the foregoing amendments is respectfully requested. The "Related Applications" paragraph is being amended to indicate that this is a reissue continuation application of U.S. Application No. 15/808,201 ("the parent reissue application"), which is a broadening reissue of U.S. Patent No. 9,189,828.

Claims 1–20 issued in U.S. Patent No. 9,189,828. Some of these claims were amended and claim 15 was canceled in the parent reissue application. Claims 21–57 were added in the parent reissue application. Claims 58–77 are being added by way of this reissue continuation application.

Support for claims 58–68 appears in FIG. 3 and in the corresponding section of the Detailed Description. Claims 58–68 were previously filed as claims 68–78 in the parent reissue application and correct Applicant's error in failing to claim the "user interaction stream" that appears in the embodiment of FIG. 3 of US 9,189,828. This is the same error identified in the reissue declarations from the parent reissue application. Hence, Applicant is filing the reissue declarations from the parent reissue application.

Per MPEP 1453(II) and guidance from Examiner Mark Rinehart of the Office of Patent Legal Administration, claims 1–68 are listed here, with only the claims being added *by this amendment* (i.e., new claims 58–68) marked with underlining and indicated as new.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 60-1876.

Dated: December 29, 2020

Respectfully submitted,

Smith Baluch LLP
376 Boylston St, Suite 401
Boston MA 02116

Phone: (617) 947-7280

By /Christopher Max Colice/
Christopher Max Colice
Registration No. 65634

PTO/AIA/05 (06-12)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US03

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted November 17, 2015, and for which a reissue patent is sought on the invention titled Graphic Processor Based Accelerator System and Method,

the specification of which

☐ is attached hereto.

☑ was filed on 11/9/2017 as reissue application number 15/808,201.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☑ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because of antecedent basis errors in issued claim 1 of US 9,189,828. Specifically, claim 1 lacks antecedent basis for "the plurality of computations," which is being amended to recite "the sequence of computations" to correct this error. Reissue is also requested because Applicant erred by claiming less than it had a right to claim in US 9,189,828. Claim 21, for example, corrects this error because it does not recite "a central processing unit" as in claim 1. And claim 79, for example, corrects Applicant's error by claiming the "user interaction stream" that appears in the embodiment of FIG. 3 of US 9,189,828 and has not been claimed to date.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional): NRLA-001US03

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Heather Marie Ames

Inventor's Signature		Date (Optional)	
Residence: City Milton	State MA	Country US	
Mailing Address 13 Myers Lane			
City Milton	State MA	Zip 02186	Country US

☐ Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/05 (08-12)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US03

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted November 17, 2015 and for which a reissue patent is sought on the invention titled Graphic Processor Based Accelerator System and Method,

the specification of which

☐ is attached hereto.

☑ was filed on 11/9/2017 as reissue application number 15/808,201.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☑ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because of antecedent basis errors in issued claim 1 of US 9,189,828. Specifically, claim 1 lacks antecedent basis for "the plurality of computations," which is being amended to recite "the sequence of computations" to correct this error. Reissue is also requested because Applicant erred by claiming less than it had a right to claim in US 9,189,828. Claim 21, for example, corrects this error because it does not recite "a central processing unit" as in claim 1. And claim 79, for example, corrects Applicant's error by claiming the "user interaction stream" that appears in the embodiment of FIG. 3 of US 9,189,828 and has not been claimed to date.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
NRLA-001US03

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Anatoli Gorchetchnikov

Inventor's Signature		Date (Optional)	
Residence: City Newton	State MA	Country US	
Mailing Address 15 Jefferson St.			
City Newton	State MA	Zip 02458	Country US

☐ Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/05 (06-12)
Approved for use through 06/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US03

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted November 17, 2015 and for which a reissue patent is sought on the invention titled Graphic Processor Based Accelerator System and Method,

the specification of which

☐ is attached hereto.

☑ was filed on 11/9/2017 as reissue application number 15/808,201.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☑ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because of antecedent basis errors in issued claim 1 of US 9,189,828. Specifically, claim 1 lacks antecedent basis for "the plurality of computations," which is being amended to recite "the sequence of computations" to correct this error. Reissue is also requested because Applicant erred by claiming less than it had a right to claim in US 9,189,828. Claim 21, for example, corrects this error because it does not recite "a central processing unit" as in claim 1. And claim 79, for example, corrects Applicant's error by claiming the "user interaction stream" that appears in the embodiment of FIG. 3 of US 9,189,828 and has not been claimed to date.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional): NRLA-001US03

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Massimiliano Versace

Inventor's Signature		Date (Optional) 2/13/13
Residence: City Milton	State MA	Country US
Mailing Address 13 Myers Lane		
City Milton	State MA	Zip 02186	Country US

☐ Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/05 (06-12)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US03

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted November 17, 2015 and for which a reissue patent is sought on the invention titled Graphic Processor Based Accelerator System and Method,

the specification of which

☐ is attached hereto.

☑ was filed on 11/9/2017 as reissue application number 15/808,201.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☑ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because of antecedent basis errors in issued claim 1 of US 9,189,828. Specifically, claim 1 lacks antecedent basis for "the plurality of computations," which is being amended to recite "the sequence of computations" to correct this error. Reissue is also requested because Applicant erred by claiming less than it had a right to claim in US 9,189,828. Claim 21, for example, corrects this error because it does not recite "a central processing unit" as in claim 1. And claim 79, for example, corrects Applicant's error by claiming the "user interaction stream" that appears in the embodiment of FIG. 3 of US 9,189,828 and has not been claimed to date.

This collection of information is required by 37 CFR 1.175. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional): NRLA-001US03

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Fabrizio Santini

Inventor's Signature		Date (Optional)
Residence: City	State	Country
Mailing Address		
City	State	Zip	Country

☐ Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/136,343	12/29/2020	2611	160	NRLA-001US04	67	7

CONFIRMATION NO. 6235

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

FILING RECEIPT

OC000000122468339

Date Mailed: 01/06/2021

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

Applicant(s)

Neurala, Inc., Residence Not Provided, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Neurala, Inc., Boston, MA
Neurala, Inc., Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 149890

Domestic Priority data as claimed by applicant

This application is a REI of 14/147,015 01/03/2014 PAT 9189828
and is a CON of 15/808,201 11/09/2017
which is a REI of 14/147,015 01/03/2014 PAT 9189828
which is a CON of 11/860,254 09/24/2007 PAT 8648867
which claims benefit of 60/826,892 09/25/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/05/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/136,343**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
17/136,343

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	160		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	1160		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	67 minus 20 =	* 47	x 50 =	2350	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4	x 240 =	960			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	4980		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04

CONFIRMATION NO. 6235

FORMALITIES LETTER

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

OC000000122468360

Date Mailed: 01/06/2021

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given **TWO MONTHS** from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- An abstract of the technical disclosure preferably not exceeding 150 words in length and commencing on a separate sheet in compliance with 37 CFR 1.72(b) is required. An abstract was not provided for this application.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Additional claim fees of $ **3310** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. Small entity discount is in effect. If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **80** surcharge.
- $ **350** search fee.
- $ **1160** examination fee.
- $ **960** for **4** independent claims over the original patent.
- $ **2350** for **47** total claims over the higher of 20, or the amount in the original patent.

- $(**0**) previous unapplied payment amount.
- $ **4900** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sejordan/

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	10083523	B2	2018-09-25	Versace et al.	Entire Document
	2	5063603	A	1991-11-05	Burt	
	3	5136687	A	1992-08-04	Edelman et al.	
	4	5142665	A	1992-08-25	Bigus	Entire Document
	5	5172253	A	1992-12-15	Lynne	Entire Document
	6	5388206	A	1995-02-07	Poulton et al.	
	7	6018696	A	2000-01-25	Matsuoka et al.	
	8	6647508	B2	2003-11-11	Zalewski et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	9	6336051	B1	2002-01-01	Pangels et al.	Entire Document
	10	7119810	B2	2006-10-10	Sumanaweera et al.	Entire Document
	11	7219085	B2	2007-05-15	Buck et al.	Entire Document
	12	7525547	B1	2009-04-28	Diard	Entire Document
	13	7765029	B2	2010-07-27	Fleischer et al.	
	14	7861060	B1	2010-12-01	Nickolls et al.	
	15	7477256	B1	2009-01-13	Johnson	Entire Document
	16	7873650	B1	2011-01-18	Chapman et al.	Entire Document
	17	8510244	B2	2013-08-13	Carson et al.	
	18	8583286	B2	2013-11-12	Fleischer et al.	
	19	8648867		2014-02-11	Gorchetchnikov et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	20	8392346	B2	2013-03-05	Ueda et al.	Entire Document
	21	9626566	B2	2017-04-18	Versace et al.	Entire Document
	22	9031692	B2	2015-05-12	Zhu	Entire Document
	23	9177246	B2	2015-11-03	Buibas et al.	Entire Document
	24	9189828	B2	2015-11-17	Gorchetchnikov et al.	
	25	RE48438		2021-02-16	Gorchetchnikov et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20010010034	A1	2001-07-26	Burton	Entire Document
	2	20020046271	A1	2002-04-18	Huang	
	3	20020050518	A1	2002-05-02	Roustaei	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	4	20020064314	A1	2002-05-30	Comaniciu et al.	
	5	20020168100	A1	2002-11-14	Woodall	
	6	20030026588	A1	2003-02-06	Elder et al.	Entire Document
	7	20030078754	A1	2003-04-24	Hamza	
	8	20040015334	A1	2004-01-22	Ditlow et al.	
	9	20050166042	A1	2005-07-28	Evans	
	10	20060129506	A1	2006-06-15	Edelman et al.	Entire Document
	11	20060184273	A1	2006-08-17	Sawada et al.	
	12	20070052713	A1	2007-03-08	Chung et al.	
	13	20070198222	A1	2007-08-23	Schuster et al.	Entire Document
	14	20070279429	A1	2007-12-06	Ganzer	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	15	20080033897	A1	2008-02-07	Lloyd	
	16	20080066065	A1	2008-03-13	Kim et al.	
	17	20080258880	A1	2008-10-23	Smith et al.	Entire Document
	18	20090080695	A1	2009-03-26	Yang	
	19	20090089030	A1	2009-04-02	Sturrock et al.	
	20	20090116688	A1	2009-05-07	Monacos et al.	
	21	20100048242	A1	2010-02-25	Rhoads et al.	Entire Document
	22	20110004341	A1	2011-01-06	Sarvadevabhatla et al.	
	23	20110173015	A1	2011-07-14	Chapman et al.	
	24	20110279682	A1	2011-11-17	Li et al.	
	25	20120072215	A1	2012-03-22	Yu et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	26	20120089552	A1	2012-04-12	Chang et al.	
	27	20120197596	A1	2012-08-02	Comi	
	28	20120316786	A1	2012-12-13	Liu et al.	Entire Document
	29	20130126703	A1	2013-05-23	Caulfield	
	30	20130131985	A1	2013-05-23	Weiland et al.	
	31	20140019392	A1	2014-01-16	Buibas et al.	
	32	20140032461	A1	2014-01-30	Weng	Entire Document
	33	20140052679	A1	2014-02-20	Sinyavskiy et al.	
	34	20140089232	A1	2014-03-27	Buibas et al.	
	35	20150127149	A1	2015-05-07	Sinyavskiy et al.	Entire Document
	36	20150134232	A1	2015-05-14	Robinson	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	37	20150224648	A1	2015-08-13	Lee et al.	
	38	20160075017	A1	2016-03-17	Laurent et al.	Entire Document
	39	20160082597	A1	2016-03-24	Gorshechnikov et al.	
	40	20160096270	A1	2016-04-07	Gabardos et al.	Entire Document
	41	20160198000	A1	2016-07-07	Gorshechnikov et al.	
	42	20170024877	A1	2017-01-26	Versace et al.	
	43	20170076194	A1	2017-03-16	Versace et al.	
	44	20170193298	A1	2017-07-06	Versace et al.	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	1224622	EP	B1	2004-11-10	Deering et al.		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	2	190208	WO		2014-11-27	Neurala, Inc.		
	3	2014204615	WO	A2	2014-12-24	Gorshechnikov et al.		
	4	2015143173	WO	A2	2015-09-24	Neurala, Inc.		
	5	2016014137	WO	A2	2016-01-28	Gorchetchnikov et al.		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Adelson, E. H., Anderson, C. H., Bergen, J. R., Burt, P. J., & Ogden, J. M. (1984). Pyramid methods in image processing. RCA engineer, 29(6), 33-41.	
	2	Aggarwal, Charu C, Hinneburg, Alexander, and Keim, Daniel A. On the surprising behavior of distance metrics in high dimensional space. Springer, 2001. 15 pages.	
	3	AL-KAYSI, A. M. et al., A Multichannel Deep Belief Network for the Classification of EEG Data, from Ontology-based Information Extraction for Residential Land Use Suitability: A Case Study of the City of Regina, Canada, DOI 10.1007/978-3-319-26561-2_5, 8 pages (November 2015).	
	4	Ames, H, Versace, M., Gorchetchnikov, A., Chandler, B., Livitz, G., Léveillé, J., Mingolla, E., Carter, D., Abdalla, H., and Snider, G. (2012) Persuading computers to act more like brains. In Advances in Neuromorphic Memristor Science and Applications, Kozma, R.Pino,R., and Pazienza, G. (eds), Springer Verlag. 25 pages.	
	5	Ames, H. Mingolla, E., Sohail, A., Chandler, B., Gorchetchnikov, A., Léveillé, J., Livitz, G. and Versace, M. (2012) The Animat. IEEE Pulse, February 2012, 3(1), 47-50.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	6	APOLLONI, B. et al., Training a network of mobile neurons, Proceedings of International Joint Conference on Neural Networks, San Jose, CA, doi: 10.1109/IJCNN.2011.6033427, pp. 1683-1691 (July 31-August 5, 2011).	
	7	Artificial Intelligence as a Service. Invited talk, Defrag, Broomfield, CO, Nov. 4-6, 2013. 22 pages.	
	8	Aryananda, L. 2006. Attending to learn and learning to attend for a social robot. Humanoids 06, pp. 618-623.	
	9	Baraldi, A. and Alpaydin, E. (1998). Simplified ART: A new class of ART algorithms. International Computer Science Institute, Berkeley, CA, TR-98-004, 1998. 42 pages.	
	10	Baraldi, A. and Alpaydin, E. (2002). Constructive feedforward ART clustering networks – Part I. IEEE Transactions on Neural Networks 13(3), 645–661.	
	11	Baraldi, A. and Parmiggiani, F. (1997). Fuzzy combination of Kohonen's and ART neural network models to detect statistical regularities in a random sequence of multi-valued input patterns. In International Conference on Neural Networks, IEEE. 6 pages.	
	12	Baraldi, Andrea and Alpaydin, Ethem. Constructive feedforward ART clustering networks—part II. IEEE Transactions on Neural Networks, 13(3):662–677, May 2002. ISSN 1045-9227. doi: 10. 1109/tnn.2002.1000131. URL http://dx.doi.org/10.1109/tnn.2002.1000131.	
	13	Bengio, Y., Courville, A., & Vincent, P. Representation learning: A review and new perspectives, IEEE Transactions on Pattern Analysis and Machine Intelligence, Volume 35 Issue 8, August 2013. Pages 1798-1828 .	
	14	Berenson, D. et al., A robot path planning framework that learns from experience, 2012 International Conference on Robotics and Automation, 2012, 9 pages [retrieved from the internet] URL:http://users.wpi.edu/-dberenson/lightning.pdf.	
	15	BERNHARD, F., and KERIVEN, R. 2005. Spiking Neurons on GPUs. Tech. Rep. 05-15, Ecole Nationale des Ponts et Chauss´es, 8 pages.	
	16	Besl, P. J., & Jain, R. C. (1985). Three-dimensional object recognition. ACM Computing Surveys (CSUR), 17(1), 75-145.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	17	BODDAPATI, V., Classifying Environmental Sounds with Image Networks, Thesis, Faculty of Computing Blekinge Institute of Technology, 37 pages (February 2017).	
	18	Bohn, C.-A. Kohonen. 1998. Feature Mapping Through Graphics Hardware. In Proceedings of 3rd Int. Conference on Computational Intelligence and Neurosciences, 4 pages.	
	19	Bradski, G., & Grossberg, S. (1995). Fast-learning VIEWNET architectures for recognizing three-dimensional objects from multiple two-dimensional views. Neural Networks, 8 (7-8), 1053-1080.	
	20	Canny, J.A. (1986). Computational Approach To Edge Detection, IEEE Trans. Pattern Analysis and Machine Intelligence, 8(6):679–698.	
	21	Carpenter, G.A. and Grossberg, S. (1987). A massively parallel architecture for a self-organizing neural pattern recognition machine. Computer Vision, Graphics, and Image Processing 37, 54–115.	
	22	Carpenter, G.A., and Grossberg, S. (1995). Adaptive resonance theory (ART). In M. Arbib (Ed.), The handbook of brain theory and neural networks. (pp. 79–82). Cambridge, M.A.: MIT press.	
	23	Carpenter, G.A., Grossberg, S. and Rosen, D.B. (1991). Fuzzy ART: Fast stable learning and categorization of analog patterns by an adaptive resonance system. Neural Networks 4, 759–771.	
	24	Carpenter, Gail A and Grossberg, Stephen. The art of adaptive pattern recognition by a self-organizing neural network. Computer, 21(3):77–88, 1988.	
	25	Coifman, R.R. and Maggioni, M. Diffusion wavelets. Applied and Computational Harmonic Analysis, 21(1):53–94, 2006.	
	26	Coifman, R.R., Lafon, S., Lee, A.B., Maggioni, M., Nadler, B., Warner, F., and Zucker, S.W. Geometric diffusions as a tool for harmonic analysis and structure definition of data: Diffusion maps. Proceedings of the National Academy of Sciences of the United States of America, 102(21):7426, 2005. 21 pages.	
	27	CORNWALL et al., Automatically translating a general purpose C++ image processing library for GPUs. Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006, 8 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	28	DAVIS, C. E. 2005. Graphic Processing Unit Computation of Neural Networks. Master's thesis, University of New Mexico, Albuquerque, NM, 121 pages.	
	29	Dosher, B.A., and Lu, Z.L. (2010). Mechanisms of perceptual attention in precuing of location. Vision Res., 40(10–12). 1269–1292.	
	30	ELLIAS, S. A., and GROSSBERG, S. 1975. Pattern formation, contrast control and oscillations in the short term memory of shunting on-center off-surround networks. Biol Cybern 20, pp. 69–98.	
	31	Extended European Search Report and Written Opinion mailed June 1, 2017 from European Application No. 14813864.7, 10 pages (Atty. Docket No. NRLA-002/01EP)	
	32	Extended European Search Report and Written Opinion mailed October 12, 2017 from European Application No. 14800348.6, 12 pages (Atty. Docket No. NRLA-003/01EP)	
	33	Extended European Search Report and Written Opinion October 23, 2017 from European Application No. 15765396.5, 8 pages (Atty. Docket No. NRLA-004/01EP)	
	34	Fazl, A., Grossberg, S., and Mingolla, E. (2009). View-invariant object category learning, recognition, and search: How spatial and object attention are coordinated using surface-based attentional shrouds. Cognitive Psychology 58, 1–48.	
	35	Földiák, P. (1990). Forming sparse representations by local anti-Hebbian learning, Biological Cybernetics, vol. 64, pp. 165-170.	
	36	Friston K., Adams R., Perrinet L., & Breakspear M. (2012). Perceptions as hypotheses: saccades as experiments. Frontiers in Psychology, 3 (151), 1-20.	
	37	Galbraith, B.V, Guenther, F.H., and Versace, M. (2015) A neural network-based exploratory learning and motor planning system for co-robots. Frontiers in Neuroscience, in press. 10 pages.	
	38	George, D. and Hawkins, J. (2009). Towards a mathematical theory of cortical micro-circuits. PLoS Computational Biology 5(10), 1–26.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	39	GEORGII, J., and WESTERMANN, R. 2005. Mass-spring systems on the GPU. Simulation Modelling Practice and Theory 13, pp. 693–702.	
	40	Gorchetchnikov A., Hasselmo M. E. (2005). A biophysical implementation of a bidirectional graph search algorithm to solve multiple goal navigation tasks. Connection Science, 17(1-2), pp. 145-166.	
	41	Gorchetchnikov A., Hasselmo M. E. (2005). A simple rule for spike-timing-dependent plasticity: local influence of AHP current. Neurocomputing, 65-66, pp. 885-890.	
	42	Gorchetchnikov A., Versace M., Hasselmo M. E. (2005). A Model of STDP Based on Spatially and Temporally Local Information: Derivation and Combination with Gated Decay. Neural Networks, 18, pp. 458-466.	
	43	GORCHETCHNIKOV A., VERSACE M., HASSELMO M. E. (2005). Spatially and temporally local spike-timing-dependent plasticity rule. In: Proceedings of the International Joint Conference on Neural Networks, number 1568 in IEEE CD-ROM Catalog Number: 05CH37662C, pp. 390-396.	
	44	GORCHETCHNIKOV, A. 2017. An Approach to a Biologically Realistic Simulation of Natural Memory. Master's thesis, Middle Tennessee State University, Murfreesboro, TN, 70 pages.	
	45	Grossberg, S. (1973). Contour enhancement, short-term memory, and constancies in reverberating neural networks. Studies in Applied Mathematics 52, 213–257.	
	46	Grossberg, S., and Huang, T.R. (2009). ARTSCENE: A neural system for natural scene classification. Journal of Vision, 9 (4), 6.1–19. doi:10.1167/9.4.6	
	47	Grossberg, S., and Versace, M. (2008) Spikes, synchrony, and attentive learning by laminar thalamocortical circuits. Brain Research, 1218C, 278-312 [Authors listed alphabetically].	
	48	HAGEN, T. R., HJELMERVIK, J., LIE, K.-A., NATVIG, J., AND OFSTAD HENRIKSEN, M. 2005. Visual simulation of shallow-water waves. Simulation Modelling Practice and Theory 13, pp. 716–726.	
	49	Hasselt, Hado Van. Double q-learning. In Advances in Neural Information Processing Systems, pp. 2613–2621,2010.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	50	Hinton, G. E., Osindero, S., and Teh, Y. (2006). A fast learning algorithm for deep belief nets. Neural Computation, 18, 1527–1554.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	1	HODGKIN, A. L., and HUXLEY, A. F. 1952. Quantitative description of membrane current and its application to conduction and excitation in nerve. J Physiol 117, pp. 500–544.	
	2	HOPFIELD, J. 1982. Neural networks and physical systems with emergent collective computational abilities. In Proc Natl Acad Sci USA, vol. 79, pp. 2554–2558.	
	3	Ilie, A. 2002. Optical character recognition on graphics hardware. Tech. Rep. integrative paper, UNCCH, Department of Computer Science, 9 pages.	
	4	International Preliminary Report on Patentability in related PCT Application No. PCT/US2014/039162 filed 22 May 2014, mailed 24 November 2015, 7 pages.	
	5	International Preliminary Report on Patentability in related PCT Application No. PCT/US2014/039239 filed 22 May 2014, mailed 24 November 2015, 8 pages.	
	6	International Preliminary Report on Patentability mailed November 8, 2016 from International Application No. PCT/US2015/029438, 7 pages (Atty. Docket No. NRLA-006/01WO)	
	7	International Search Report and Written Opinion mailed February 18, 2015 from International Application No. PCT/US2014/039162, 12 pages (Atty. Docket No. NRLA-002/01WO)	
	8	International Search Report and Written Opinion mailed February 23, 2016 from International Application No. PCT/US2015/029438, 11 pages (Atty. Docket No. NRLA-006/01WO)	
	9	International Search Report and Written Opinion mailed July 6, 2017 from International Application No. PCT/US2017/029866, 12 pages (Atty. Docket No. NRLA-009/01WO).	
	10	International Search Report and Written Opinion mailed November 26, 2014 from International Application No. PCT/US2014/039239, 14 pages (Atty. Docket No. NRLA-003/01WO)	
	11	International Search Report and Written Opinion mailed September 15, 2015 from International Application No. PCT/US2015/021492, 9 pages (Atty. Docket No. NRLA-004/01WO)	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	12	Itti, L., and Koch, C. (2001). Computational modelling of visual attention. Nature Reviews Neuroscience, 2 (3), 194-203.	
	13	Itti, L., Koch, C., and Niebur, E. (1998). A Model of Saliency-Based Visual Attention for Rapid Scene Analysis, 1–6.	
	14	Jarrett, K., Kavukcuoglu, K., Ranzato, M. A., & LeCun, Y. (2009, September). What is the best multi-stage architecture for object recognition?. In Computer Vision, 2009 IEEE 12th International Conference on (pp. 2146-2153). IEEE.	
	15	KHALIGH-RAZAVI, S. -M. et al., Deep Supervised, but Not Unsupervised, Models May Explain IT Cortical Representation, PLoS Computational Biology, Vol. 10, Issue 11, 29 pages (November 2014).	
	16	Kim, S., Novel approaches to clustering, biclustering and algorithms based on adaptive resonance theory and intelligent control, Doctoral Dissertations, Missouri University of Science and Technology, 125 pages (2016).	
	17	KIPFER, P., SEGAL, M., and WESTERMANN, R. 2004. UberFlow: A GPU-Based Particle Engine. In Proceedings of the SIGGRAPH/Eurographics Workshop on Graphics Hardware 2004, pp. 115–122.	
	18	KOLB, A., L. LATTA, and C. REZK-SALAMA. 2004. "Hardware-Based Simulation and Collision Detection for Large Particle Systems." In Proceedings of the SIGGRAPH/Eurographics Workshop on Graphics Hardware 2004, pp. 123–131.	
	19	Kompella, Varun Raj, Luciw, Matthew, and Schmidhuber, J¨urgen. Incremental slow feature analysis: Adaptive low-complexity slow feature updating from high-dimensional input streams. Neural Computation, 24(11):2994–3024, 2012.	
	20	Kowler, E. (2011). Eye movements: The past 25years. Vision Research, 51(13), 1457–1483. doi:10.1016/j.visres.2010.12.014	
	21	Larochelle H., & Hinton G. (2012). Learning to combine foveal glimpses with a third-order Boltzmann machine. NIPS 2010,1243-1251.	
	22	LeCun, Y., Kavukcuoglu, K., & Farabet, C. (2010, May). Convolutional networks and applications in vision. In Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on (pp. 253-256). IEEE.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	23	Lee, D. D. and Seung, H. S. (1999). Learning the parts of objects by non-negative matrix factorization. Nature, 401 (6755):788-791.	
	24	Lee, D. D., and Seung, H. S. (1997). "Unsupervised learning by convex and conic coding." Advances in Neural Information Processing Systems, 9.	
	25	Legenstein, R., Wilbert, N., and Wiskott, L. Reinforcement learning on slow features of high-dimensional input streams. PLoS Computational Biology, 6(8), 2010. ISSN 1553-734X. 13 pages.	
	26	Léveillé, J., Ames, H., Chandler, B., Gorchetchnikov, A., Mingolla, E., Patrick, S., and Versace, M. (2010) Learning in a distributed software architecture for large-scale neural modeling. BIONETICS10, Boston, MA, USA. 8 pages.	
	27	Livitz G., Versace M., Gorchetchnikov A., Vasilkoski Z., Ames H., Chandler B., Leveille J. and Mingolla E. (2011) Adaptive, brain-like systems give robots complex behaviors, The Neuromorphic Engineer, : 10.2417/1201101.003500 February 2011. 3 pages.	
	28	Livitz, G., Versace, M., Gorchetchnikov, A., Vasilkoski, Z., Ames, H., Chandler, B., Léveillé, J., Mingolla, E., Snider, G., Amerson, R., Carter, D., Abdalla, H., and Qureshi, S. (2011) Visually-Guided Adaptive Robot (ViGuAR). Proceedings of the International Joint Conference on Neural Networks (IJCNN) 2011, San Jose, CA, USA. 9 pages.	
	29	Lowe, D.G.(2004). Distinctive Image Features from Scale-Invariant Keypoints. Journal International Journal of Computer Vision archive Volume 60, 2, 91 – 110.	
	30	Lu, Z.L., Liu, J., and Dosher, B.A. (2010) Modeling mechanisms of perceptual learning with augmented Hebbian re-weighting. Vision Research, 50(4). 375–390.	
	31	LUO et al., "Artificial neural network computation on graphic process unit." Neural Networks, 2005. IJCNN'05. Proceedings. 2005 IEEE International Joint Conference on. Vol. 1. IEEE, 2005. Pages 622-626.	
	32	Mahadevan, S. Proto-value functions: Developmental reinforcement learning. In Proceedings of the 22nd international conference on Machine learning, pp. 553–560. ACM, 2005.	
	33	MEUTH, J.R. and WUNSCH, D.C. (2007) A SURVEY OF NEURAL COMPUTATION ON GRAPHICS PROCESSING HARDWARE. 22nd IEEE International Symposium on Intelligent Control, Part of IEEE Multi-conference on Systems and Control, Singapore, 1-3 October 2007, 5 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	34	Mishkin M, Ungerleider LG. (1982). "Contribution of striate inputs to the visuospatial functions of parieto-preoccipital cortex in monkeys," Behav Brain Res, 6 (1): 57–77.	
	35	Mnih, Volodymyr, Kavukcuoglu, Koray, Silver, David, Rusu, Andrei A, Veness, Joel, Bellemare, Marc G, Graves, Alex, Riedmiller, Martin, Fidjeland, Andreas K, Ostrovski, Georg, et al. Human-level control through deep reinforcement learning. Nature, 518(7540):529–533, 25 February 2015.	
	36	MONTRYM et al., The GeForce 6800, in IEEE Micro, vol. 25, no. 2, pp. 41-51, March-April 2005.	
	37	Moore, Andrew W and Atkeson, Christopher G. Prioritized sweeping: Reinforcement learning with less data and less time. Machine Learning, 13(1):103–130, 1993.	
	38	Najemnik, J., and Geisler, W. (2009). Simple summation rule for optimal fixation selection in visual search. Vision Research. 49, 1286–1294.	
	39	Non-Final Office Action mailed 01/04/2018 from U.S. Application Serial No. 15/262,637, 23 pages (Atty. Docket No. NRLA-004/01US)	
	40	Non-Final Office Action mailed 05/31/18 from U.S. Application Serial No. 14/947,516, 16 pages (Atty. Docket No. NRLA-003US01)	
	41	Notice of Alllowance mailed May 22, 2018 from U.S. Application Serial No. 15/262,637, 6 pages (Atty. Docket No. NRLA-004/01US).	
	42	Notice of Allowance mailed 07/27/2016 from U.S. Application Serial No. 14/662,657 (Atty. Docket No. NRLA-005/01US)	
	43	Notice of Allowance mailed 12/16/2016 from U.S. Application Serial No. 14/662,657 (Atty. Docket No. NRLA-005/01US)	
	44	OH, K.-S., and JUNG, K. 2004. GPU implementation of neural networks. Pattern Recognition 37, pp. 1311–1314.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	45	Oja, E. (1982). Simplified neuron model as a principal component analyzer. Journal of Mathematical Biology 15(3), 267–273.	
	46	Partial Supplementary European Search Report dated July 4, 2017 from European Application No. 14800348.6, 13 pages (Atty. Docket No. NRLA-003/01EP).	
	47	PERUMALLA, "Discrete-event execution alternatives on general purpose graphical processing units (GPGPUs)." Proceedings of the 20th Workshop on Principles of Advanced and Distributed Simulation. IEEE Computer Society, 2006.8 pages.	
	48	Raijmakers, M.E.J., and Molenaar, P. (1997). Exact ART: A complete implementation of an ART network Neural networks 10 (4), 649-669.	
	49	Ranzato, M. A., Huang, F. J., Boureau, Y. L., & Lecun, Y. (2007, June). Unsupervised learning of invariant feature hierarchies with applications to object recognition. In Computer Vision and Pattern Recognition, 2007. CVPR'07. IEEE Conference on (pp. 1-8). IEEE.	
	50	Raudies, F., Eldridge, S., Joshi, A., and Versace, M. (20 August 2014). Learning to navigate in a virtual world using optic flow and stereo disparity signals. Artificial Life and Robotics, DOI 10.1007/s10015-014-0153-1. 15 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	1	REN, Y. et al., Ensemble Classification and Regression - Recent Developments, Applications and Future Directions, in IEEE Computational Intelligence Magazine, 10.1109/MCI.2015.2471235, 14 pages (2016).	
	2	Riesenhuber, M., & Poggio, T. (1999). Hierarchical models of object recognition in cortex. Nature Neuroscience, 2 (11), 1019-1025.	
	3	Riesenhuber, M., & Poggio, T. (2000). Models of object recognition. Nature neuroscience, 3, 1199-1204.	
	4	ROLFES, T. 2004. Artificial Neural Networks on Programmable Graphics Hardware. In Game Programming Gems 4, A. Kirmse, Ed. Charles River Media, Hingham, MA, pp. 373–378.	
	5	Rublee, E., Rabaud, V., Konolige, K., & Bradski, G. (2011). ORB: An efficient alternative to SIFT or SURF. In IEEE International Conference on Computer Vision (ICCV) 2011, 2564–2571.	
	6	Ruesch, J. et al. 2008. Multimodal Saliency-Based Bottom-Up Attention a Framework for the Humanoid Robot iCub. 2008 IEEE International Conference on Robotics and Automation, pp. 962-965.	
	7	Rumelhart D., Hinton G., and Williams, R. (1986). Learning internal representations by error propagation. In Parallel distributed processing: explorations in the microstructure of cognition, vol. 1, MIT Press. 45 pages.	
	8	RUMPF, M. and STRZODKA, R. Graphics processor units: New prospects for parallel computing. In Are Magnus Bruaset and Aslak Tveito, editors, Numerical Solution of Partial Differential Equations on Parallel Computers, volume 51 of Lecture Notes in Computational Science and Engineering, pp. 89–134. Springer, 2005.	
	9	Salakhutdinov, R., & Hinton, G. E. (2009). Deep boltzmann machines. In International Conference on Artificial Intelligence and Statistics (pp. 448-455).	
	10	Schaul, Tom, Quan, John, Antonoglou, Ioannis, and Silver, David. Prioritized experience replay. arXiv preprint arXiv: 1511.05952, 18 November 2015. 21 pages.	
	11	Schmidhuber, J. (2010). Formal theory of creativity, fun, and intrinsic motivation (1990–2010). Autonomous Mental Development, IEEE Transactions on, 2(3), 230-247.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	12	Schmidhuber, Jürgen. Curious model-building control systems. In Neural Networks, 1991. 1991 IEEE International Joint Conference on, pp. 1458–1463. IEEE, 1991.	
	13	Seibert, M., & Waxman, A.M. (1992). Adaptive 3-D Object Recognition from Multiple Views. IEEE Transactions on Pattern Analysis and Machine Intelligence, 14 (2), 107-124.	
	14	SETOAIN et al., "Parallel hyperspectral image processing on commodity graphics hardware." Parallel Processing Workshops, 2006. ICPP 2006 Workshops. 2006 International Conference on. IEEE, 2006. 8 pages.	
	15	Sherbakov, L. and Versace, M. (2014) Computational principles for an autonomous active vision system. Ph.D., Boston University, http://search.proquest.com/docview/1558856407. 194 pages.	
	16	SHERBAKOV, L. et al. 2012. CogEye: from active vision to context identification, youtube, retrieved from the Internet on 10-10-2017: URL://www.youtube.com/watch?v=i5PQk962B1k, 1 page.	
	17	SHERBAKOV, L. et al. 2013. CogEye: system diagram module brain area function algorithm approx # neurons, retrieved from the Internet on 10-12-2017: URL://http://www-labsticc.univ-ubs.fr/~coussy/neucomp2013/index_fichiers/material/posters/NeuComp2013_final56x36.pdf, 1 page.	
	18	Sherbakov, L., Livitz, G., Sohail, A., Gorchetchnikov, A., Mingolla, E., Ames, H., and Versace, M (2013b) A computational model of the role of eye-movements in object disambiguation. Cosyne, Feb. 28-Mar. 3, 2013. Salt Lake City, UT, USA. 2 pages.	
	19	Sherbakov, L., Livitz, G., Sohail, A., Gorchetchnikov, A., Mingolla, E., Ames, H., and Versace, M. (2013a) CogEye: An online active vision system that disambiguates and recognizes objects. NeuComp 2013. 2 pages.	
	20	Smolensky, Paul. Information processing in dynamical systems: Foundations of harmony theory. No. CU-CS-321-86. COLORADO UNIV AT BOULDER DEPT OF COMPUTER SCIENCE, 1986. 88 pages.	
	21	Snider, Greg, et al. "From synapses to circuitry: Using memristive memory to explore the electronic brain." IEEE Computer, Volume 44(2). (2011): 21-28.	
	22	Spratling, M. W. (2008). Predictive coding as a model of biased competition in visual attention. Vision Research, 48 (12):1391-1408.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	23	Spratling, M. W. (2012). Unsupervised learning of generative and discriminative weights encoding elementary image components in a predictive coding model of cortical function. Neural Computation, 24(1):60-103.	
	24	Spratling, M. W., De Meyer, K., and Kompass, R. (2009). Unsupervised learning of overlapping image components using divisive input modulation. Computational intelligence and neuroscience. 20 pages.	
	25	Sprekeler, H. On the relation of slow feature analysis and laplacian eigenmaps. Neural Computation, pp. 1–16, 2011.	
	26	SUN, Z. et al., Recognition of SAR target based on multilayer auto-encoder and SNN, International Journal of Innovative Computing, Information and Control, Vol. 9, No. 11, pp. 4331-4341, November 2013.	
	27	Sutton, R. S., and Barto, A. G. (1998). Reinforcement learning: An introduction(vol. 1, No. 1). Cambridge: MIT press. 10 pages.	
	28	Tong, F., Ze-Nian Li, (1995). Reciprocal-wedge transform for space-variant sensing," Pattern Analysis and Machine Intelligence, IEEE Transactions on , vol.17, no.5, pp.500 - 51. doi: 10.1109/34.391393	
	29	Torralba, A., Oliva, A., Castelhano, M.S., Henderson, J.M. (2006). Contextual guidance of eye movements and attention in real-world scenes: the role of global features in object search. Psychological Review, 113(4).766–786.	
	30	Van Hasselt, Hado, Guez, Arthur, and Silver, David. Deep reinforcement learning with double q-learning. arXiv preprint arXiv: 1509.06461, 22 September 2015. 7 pages.	
	31	Versace, Brain-inspired computing. Invited keynote address, Bionetics 2010, Boston, MA, USA. 1 page.	
	32	Versace, M. (2006) From spikes to interareal synchrony: how attentive matching and resonance control learning and information processing by laminar thalamocortical circuits. NSF Science of Learning Centers PI Meeting, Washington, DC, USA. 1 page.	
	33	Versace, M., (2010) Open-source software for computational neuroscience: Bridging the gap between models and behavior. In Horizons in Computer Science Research, Volume 3. 43 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

	34	Versace, M., Ames, H., Léveillé, J., Fortenberry, B., and Gorchetchnikov, A. (2008) KInNeSS: A modular framework for computational neuroscience. Neuroinformatics, 2008 Winter; 6(4):291-309. Epub 2008 Aug 10.	
	35	Versace, M., and Chandler, B. (2010) MoNETA: A Mind Made from Memristors. IEEE Spectrum, December 2010. 8 pages.	
	36	VERSACE, TEDx Fulbright, Invited talk, Washington DC, 4/5/2014. 30 pages.	
	37	Webster, Bachevalier, Ungerleider (1994). Connections of IT areas TEO and TE with parietal and frontal cortex in macaque monkeys. Cerebal Cortex, 4(5), 470-483.	
	38	Wiskott, Laurenz and Sejnowski, Terrence. Slow feature analysis: Unsupervised learning of invariances. Neural Computation, 14(4):715–770, 2002.	
	39	Wu, Yan & J. Cai, H. (2010). A Simulation Study of Deep Belief Network Combined with the Self-Organizing Mechanism of Adaptive Resonance Theory. 10.1109/CISE.2010.5677265, 4 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No.: NRLA-001US04 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Anatoli Gorchetchnikov

Confirmation No.: 6235

Application No.: 17/136,343

Group Art Unit:

Filed: 2020-12-29

Examiner:

FOR: **GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD**

VIA EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.56, 1.97, AND 1.98

In accordance with the duty of disclosure set forth in 37 C.F.R. §1.56, Applicant hereby submits the following information in conformance with 37 C.F.R. §§1.97 and 1.98. It is respectfully requested that the information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☐ Pursuant to 37 C.F.R. §1.98, a copy of each non-US patent document cited in the attached Form PTO/SB/08 is enclosed.

☒ No copies of any U.S. Office Actions cited on the accompanying Form PTO/SB/08 are being provided because they are available on PAIR. Copies will be provided to the Examiner upon request.

☒ No copies of the publications listed on the attached Form used in lieu of PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98(d) because the publications were previously cited by or submitted to the Office in prior Application Serial No(s). 15/808,201, 14/147,015, and/or 11/860,254 to which the above-identified application claims priority.

☒ No copies of any U.S. patents or U.S. patent application publications listed on the attached Form PTO/SB/08 are being provided pursuant to 37 C.F.R. §1.98.

☐ Publications ____ listed on the attached Form PTO/SB/08 were cited in a foreign search or examination report corresponding to application serial no. ____ and mailed on ____.

☐ Enclosed is a copy of a non-English publication(s) _____ Pursuant to §609 of the M.P.E.P., Applicant submits the attached foreign search or examination report, which cites such non-English language publication(s).

☐ Enclosed is a copy of a non-English publication(s) _____ English language publication _____ (copy enclosed) claims priority from this non-English publication.

☐ Enclosed is an explanation of non-English publication(s) ____ for which an English translation is not available.

☐ Enclosed is an English translation of non-English publication(s) _____ cited in the attached Form used in lieu of PTO/SB/08.

☐ Enclosed is a copy of pending patent Application Serial No. _____.

☐ Applicants wish to make the Examiner aware of the following co-pending U.S. patents/publications/applications:

Application No.:	**Filing Date**	**Inventor**	**Atty. Docket No.**

In accordance with **37 C.F.R. §1.97(b)**, no additional fee for submission of this Information Disclosure Statement is required, as it is filed within any one of the following time periods:

☐ within three months from the filing date of this national application other than a CPA under 37 C.F.R. § 1.53(d);

☐ within three months from the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in this international application;

☒ before the mailing date of a first office action on the merits; or

☐ before the mailing of a first office action after the filing of a request for continued examination under 37 C.F.R. § 1.114.

In accordance with 37 C.F.R. § 1.97(g), this Information Disclosure Statement shall not be construed as to mean that a search has been made.

In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be material to patentability as defined by 37 C.F.R § 1.56(b).

Remarks

It is respectfully requested that the Examiner consider the above-noted information and return an initialed copy of the attached Form used in lieu of PTO/SB/08 to the undersigned.

The Director is hereby requested and authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 60-1876 which the undersigned is authorized to draw.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Dated: March 29, 2021

Respectfully submitted,
SMITH BALUCH LLP

SMITH BALUCH LLP
376 Boylston St., Suite 401
Boston, MA 02116

Tel: 6179477280

By: /Christopher Max Colice/
Christopher Max Colice
Reg. No.: 65634

Electronic Acknowledgement Receipt

EFS ID:	42305859
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Holly Johnson
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	29-MAR-2021
Filing Date:	29-DEC-2020
Time Stamp:	13:29:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	NRLA001US04_SB08_03-29-2021_1_OF_3.pdf	1060010 d41a58454bad90a127e039aed5c8314e2404091e	no	15

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	NRLA001US04_SB08_03-29-2021_2_OF_3.pdf	1057728 38be6d0503f0e366452ffb0dbfc1d5bec156a25b	no	8
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
3	Information Disclosure Statement (IDS) Form (SB08)	NRLA001US04_SB08_03-29-2021_3_OF_3.pdf	1057222 6173f76bb258112882f017387924bc80f2cd34ef	no	7
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	Transmittal Letter	NRLA-001US04_IDSTransmittal_20210329.pdf	132311 c6ada475d78b5725e201f3d7cd78846ac3e2ab54	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	3307271	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CORRECTED ADS FORM

Application Number	17136343
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number		
Name		
Residence Information		
Residency		
City		
State		
Country of Residence		
Mailing Address of Inventor		
Address 1		
Address 2		
City,State/Province, Postal Code		
Country		

Application Information

	Data of Record	Updated Data
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	
Attorney Docket Number	NRLA-001US04	
Entity Type	Small	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	17136343	
	Continuity Type	REI	
	Prior Application Number	14147015	
	Filing Date (YYYY-MM-DD)	2014-01-03	
	Patent Number	9189828	
	Issue Date (YYYY-MM-DD)	2015-11-17	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	17136343	14147015
	Continuity Type	CON	
	Prior Application Number	~~15808201~~	11860254
	Filing Date (YYYY-MM-DD)	~~2017-11-09~~	2007-09-24
	Patent Number	~~RE48438~~	8648867
	Issue Date (YYYY-MM-DD)	~~2021-02-16~~	2014-02-11

		Data of Record	Updated Data
	Prior Application Status	patented	expired
	Application Number	~~15808201~~	11860254
	Continuity Type	REI	PRO
	Prior Application Number	14147015	60826892
	Filing Date (YYYY-MM-DD)	2014-01-03	2006-09-25
	Patent Number	9189828	
	Issue Date (YYYY-MM-DD)	2015-11-17	

		Data of Record	Updated Data
	Prior Application Status	patented	
	Application Number	~~14147015~~	17136343
	Continuity Type	CON	
	Prior Application Number	~~11860254~~	15808201
	Filing Date (YYYY-MM-DD)	~~2007-09-24~~	2017-11-09
	Patent Number	~~8648867~~	RE48438
	Issue Date (YYYY-MM-DD)	~~2014-02-11~~	2021-02-16

		Data of Record	Updated Data
	Prior Application Status	~~pending~~	patented
	Application Number	~~11860254~~	15808201
	Continuity Type	~~PRO~~	REI
	Prior Application Number	~~60826892~~	14147015
	Filing Date (YYYY-MM-DD)	~~2006-09-25~~	2014-01-03
	Patent Number		9189828
	Issue Date (YYYY-MM-DD)	~~0001-01-01~~	2015-11-17

		Data of Record	Updated Data
	Prior Application Status		patented
	Application Number		14147015
	Continuity Type		CON
	Prior Application Number		11860254
	Filing Date (YYYY-MM-DD)		2007-09-24
	Patent Number		8648867
	Issue Date (YYYY-MM-DD)		2014-02-11

		Data of Record	Updated Data
	Prior Application Status		pending
	Application Number		11860254
	Continuity Type		PRO
	Prior Application Number		60826892
	Filing Date (YYYY-MM-DD)		2006-09-25
	Patent Number		
	Issue Date (YYYY-MM-DD)		0001-01-01

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type	ASG	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization	Yes	
Name		
Organization Name	Neurala, Inc.	
Address 1		P.O. Box 52678

Address 2		
City,State/Province,Postal Code		Boston MA 02205-2678
Country		US
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		
Organization Name		
Mailing Address		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		

Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Christopher Max Colice/	Registration Number	65634
First Name	Christopher	Last Name	Colice

Electronic Acknowledgement Receipt

EFS ID:	42380940
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	
Customer Number:	149890
Filer:	Christopher M. Colice/Holly Johnson
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	06-APR-2021
Filing Date:	29-DEC-2020
Time Stamp:	18:53:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	102994 9d1e25b048562a93621a55574a96f275e14be8cb	no	7

Warnings:

Information:	
Total Files Size (in bytes):	102994

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Inventor:	Anatoli Gorchetchnikov	Confirmation No.:	6235
Application No.:	17/136,343	Group Art Unit:	2611
Filed:	December 29, 2020	Examiner:	To Be Assigned

For: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SECOND PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the above-captioned application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Abstract of the Disclosure begin on page 3 of this paper.

Remarks begin on page 4 of this paper.

IN THE SPECIFICATION:

Please replace the paragraph immediately following the heading "Related Applications" with the following paragraph. The amendments to this paragraph are indicated by underlining and brackets.

The present application is a reissue continuation application of U.S. Application No. 15/808,201, which was filed on Nov. 9, 2017 as a broadening reissue application of U.S. Pat. No. 9,189,828, filed Jan. 3, 2014, which claims a priority benefit, under 35 U.S.C. §120, as a continuation of U.S. application Ser. No. 11/860,254, now U.S. Pat. No. 8,648,867 B2, filed Sep. 24, 2007, entitled "Graphic Processor Based Accelerator System and Method," which in turn claims the priority benefit, under 35 U.S.C. §119(e), of U.S. Application No. 60/826,892, filed Sep. 25, 2006. <u>The present application is also a broadening reissue application of U.S. Pat. No. 9,189,828, filed Jan. 3, 2014, which is a continuation of U.S. application Ser. No. 11/860,254, now U.S. Pat. No. 8,648,867 B2, filed Sep. 24, 2007, which in turn claims the priority benefit, under 35 U.S.C. §119(e), of U.S. Application No. 60/826,892, filed Sep. 25, 2006.</u> Each of the above-identified applications is incorporated herein by reference in its entirety. More than one reissue application has been filed for the reissue of U.S. Pat. No. 9,189,828, including this application and U.S. Application No. 15/808,201.

IN THE ABSTRACT OF THE DISCLOSURE:

Please insert the Abstract of the Disclosure that is attached to this Amendment on a separate sheet.

Remarks

Applicant is updating the specific reference to the parent applications to match the changes in the accompanying Corrected Application Data Sheet (ADS). In addition, the Abstract is being included on a separate sheet of paper. This Abstract was filed with the application itself but was not on a separate sheet of paper. It is identical to the Abstract in the parent application.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 60-1876.

Dated: April 6, 2021

Respectfully submitted,

Smith Baluch LLP
376 Boylston St, Suite 401
Boston MA 02116

Phone: (617) 947-7280

By /Christopher Max Colice/
Christopher Max Colice
Registration No. 65634

Electronic Patent Application Fee Transmittal

Application Number:	17136343
Filing Date:	29-Dec-2020
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Christopher M. Colice/Marie Spakowski
Attorney Docket Number:	NRLA-001US04

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
REISSUE OR REISSUE DESIGN CPA SEARCH FEE	2114	1	350	350
REISSUE OR REISSUE DESIGN CPA EXAM. FEE	2314	1	1160	1160
Pages:				
Claims:				
REISSUE CLAIMS IN EXCESS OF 20 FOR SMALL	2205	47	50	2350
REISSUE- INDEPENDENT CLAIMS	2204	4	240	960
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	2051	1	80	80

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	2251	1	110	110
Miscellaneous:				
		Total in USD ($)		**5010**

Electronic Acknowledgement Receipt

EFS ID:	42383777
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	06-APR-2021
Filing Date:	29-DEC-2020
Time Stamp:	19:23:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$5010
RAM confirmation Number	E202146J23184484
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Abstract	NRLA-001US04_Abstract.pdf	80481 44e3710b3398a5d0fe09fe3f18158b2e7df11780	no	1
Warnings:					
Information:					
2		NRLA-001US04_Second_Preliminary_Amendment.pdf	188585 34cd21fe2206e9d4993652dee60b02c7b17041c7	yes	4

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Specification	2	2
Abstract	3	3
Applicant Arguments/Remarks Made in an Amendment	4	4

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	40255 a9cbfa73f8cd204a7369d3d8c9a94a7d911c0712	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	309321		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Abstract

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

US009189828B2

(12) **United States Patent**
Gorchetchnikov et al.

(10) **Patent No.: US 9,189,828 B2**
(45) **Date of Patent: *Nov. 17, 2015**

(54) **GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD**

(71) Applicant: **Neurala Inc.**, Boston, MA (US)

(72) Inventors: **Anatoli Gorchetchnikov**, Boston, MA (US); **Heather Marie Ames**, South Boston, MA (US); **Massimiliano Versace**, South Boston, MA (US); **Fabrizio Santini**, Jamaica Plain, MA (US)

(73) Assignee: **Neurala, Inc.**, Boston, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/147,015**

(22) Filed: **Jan. 3, 2014**

(65) **Prior Publication Data**

US 2014/0192073 A1 Jul. 10, 2014

Related U.S. Application Data

(63) Continuation of application No. 11/860,254, filed on Sep. 24, 2007, now Pat. No. 8,648,867.

(60) Provisional application No. 60/826,892, filed on Sep. 25, 2006.

(51) **Int. Cl.**

G06T 1/60	(2006.01)
G06F 9/50	(2006.01)
G06T 1/20	(2006.01)

(52) **U.S. Cl.**

CPC ***G06T 1/60*** (2013.01); ***G06F 9/5027*** (2013.01); ***G06T 1/20*** (2013.01); *G06F 2209/509* (2013.01)

(58) **Field of Classification Search**

CPC G06T 1/60

USPC 345/501, 503, 530, 531, 535; 348/739; 712/225

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,388,206	A	2/1995	Poulton et al.	
7,861,060	B1 *	12/2010	Nickolls et al.	712/22
8,648,867	B2 *	2/2014	Gorchetchnikov et al.	345/501
2005/0166042	A1	7/2005	Evans	
2007/0052713	A1	3/2007	Chung et al.	
2007/0279429	A1	12/2007	Ganzer	

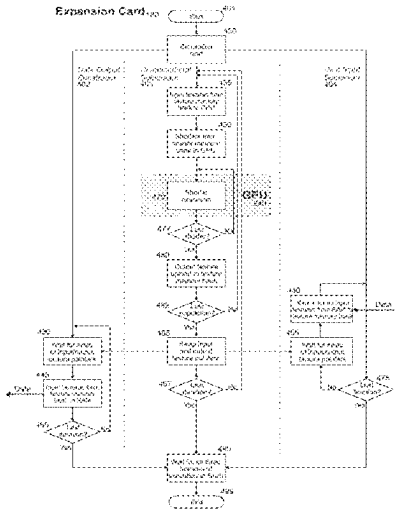
* cited by examiner

Primary Examiner — Maurice L McDowell, Jr.
(74) *Attorney, Agent, or Firm* — Cooley LLP

(57) **ABSTRACT**

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

20 Claims, 5 Drawing Sheets



Electronic Acknowledgement Receipt

EFS ID:	42874007
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	02-JUN-2021
Filing Date:	29-DEC-2020
Time Stamp:	11:16:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Abstract	NRLA-001US04_Abstract.pdf	70728 528edea2186cc814edf5be6bde332446d456a0dd	no	1

Warnings:

Information:	
Total Files Size (in bytes):	70728

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/136,343	12/29/2020	2611	5060	NRLA-001US04	67	7

CONFIRMATION NO. 6235

UPDATED FILING RECEIPT

OC000000126054795

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

Date Mailed: 06/03/2021

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

Applicant(s)

Neurala, Inc., Boston, MA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Neurala, Inc., Boston, MA
Neurala, Inc., Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 149890

Domestic Priority data as claimed by applicant

This application is a REI of 14/147,015 01/03/2014 PAT 9189828
which is a CON of 11/860,254 09/24/2007 PAT 8648867
which claims benefit of 60/826,892 09/25/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/05/2021
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/136,343**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative,

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
17/136,343

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	160		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	1160		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	67 minus 20 =	* 47	x 50 =	2350	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4	x 240 =	960			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	4980		TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/136,343	12/29/2020	2611	5060	NRLA-001US04	67	7

CONFIRMATION NO. 6235

UPDATED FILING RECEIPT

OC000000128054795

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

Date Mailed: 06/03/2021

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

Applicant(s)

Neurala, Inc., Boston, MA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Neurala, Inc., Boston, MA
Neurala, Inc., Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 149890

Domestic Priority data as claimed by applicant This application is a CON of 15/808,201 11/09/2017
and ~~This application~~ is a REI of 14/147,015 01/03/2014 PAT 9189828
~~which is a CON of 11/860,254 09/24/2007 PAT 8648867~~ and said 15/808,201 is a REI of 14/147,015 01/03/2014 9189828
~~which claims benefit of 60/826,892 09/25/2006~~ which is a CON of 11/860,254 09/24/2007 8648867
which claims benefit of 60/826,892 09/25/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/05/2021
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/136,343**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative,

this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

Attorney Docket No. NRLA-001US04 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Inventor:	Anatoli Gorchetchnikov	Confirmation No.:	6235
Application No.:	17/136,343	Group Art Unit:	
Filed:	2020-12-29	Examiner:	

For: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

VIA EFS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTION OF FILING RECEIPT

Applicant requests a Corrected Filing Receipt in the above identified patent application. The Filing Receipt contains the following error:

Domestic Priority data as claimed by applicant

This application is a CON of 15/808,201 11/09/2017
and ~~This application~~ is a REI of 14/147,015 01/03/2014 9189828
and said 15/808,201 is a REI of 14/147,015 01/03/2014 9189828
which is a CON of 11/860,254 09/24/2007 8648867
which claims benefit of 60/826,892 09/25/2006

This priority claim is indicated on the Application Data Sheet and preliminary amendment filed April 6, 2021, within four months of this application's filing date.

Filed herewith is a copy of the Filing Receipt with the correction indicated. Please issue an Updated Filing Receipt for this patent application to reflect the changes made in the Corrected Application Data Sheet submitted on April 6, 2021.

Dated:

Respectfully submitted,
SMITH BALUCH LLP

Smith Baluch LLP
ATTN: Patent Group
376 Boylston St., Suite 401
Boston, MA 02116

Tel: (617) 947-7280

By: /Christopher Max Colice/
Christopher Max Colice
Reg. No.65634

Electronic Acknowledgement Receipt

EFS ID:	42979859
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	14-JUN-2021
Filing Date:	29-DEC-2020
Time Stamp:	15:50:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	NRLA-001US04_Marked-Up_Filing_Receipt.pdf	806772 67bc829c4cdd16537540f7ee16947b46a8cbfb61	no	3

Warnings:

Information:					
2	Request for Corrected Filing Receipt	NRLA-001US04_RequestForCorrectedFilingReceipt.pdf	144752 6713138951ab26f21341ef05d50a18243eb0622d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	951524	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/136,343	Filing Date 12/29/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

AMENDMENT	06/24/2021	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 69	Minus	** 67	= 2		x $50 =	100
	Independent (37 CFR 1.16(h))	* 8	Minus	*** 7	= 1		x $240 =	240
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	340

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LDRC
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EVA V GILLIS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Inventor:	Anatoli Gorchetchnikov	Confirmation No.:	6235
Application No.:	17/136,343	Group Art Unit:	
Filed:	2020-12-29	Examiner:	

For: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Prior to examination of the above-identified application, please amend the above-captioned application as follows:

Amendments to the Claims are reflected on the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 15 of this paper.

IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Changes to any amended claims are indicated by [[double brackets]], ~~strikethrough~~ and/or <u>underlining</u>. This listing also reflects any cancellation and/or addition of claims.

1. A computer system, comprising:

a central processing unit to receive input data;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the [first] main memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one graphics processing unit to perform a sequence of computations on the at least a portion of the input data so as to generate output data, the sequence of computations representing an artificial neural network, intermediate computations in the sequence of computations representing respective layers of the artificial neural network and yielding intermediate results; and

accelerator memory, operably coupled to the [graphic] at least one graphics processing unit, to store the results of the [plurality of sequential] sequence of computations; and

a controller, operably coupled to the at least one graphics processing unit and the accelerator memory, to initialize textures and shaders in the accelerator memory for performing the sequence of computations, to control performance of the sequence of computations by the at least one graphics processing unit, to transfer the at least a portion of the input data into the accelerator memory during performance of the intermediate computations in the sequence of computations by the at least one graphics processing unit, and to transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the intermediate computations in the sequence of computations by the at least one [graphic] graphics processing unit.

2. The computer system of claim 1, wherein the central processing unit is configured to receive the input data in response to a user interaction.

3. The computer system of claim 1, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one graphics processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

4. The computer system of claim 1, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

5. The computer system of claim 1, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

6. The computer system of claim 1, wherein accelerator memory comprises:

a first memory bank to store parameters common to all of the computations in the sequence of computations; and

a second memory bank to store data specific to at least one computation in the sequence of computations.

7. The computer system of claim 1, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

8. The computer system of claim 1, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one graphics processing unit has begun to perform another sequence of computations.

9. The computer system of claim 8, wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one graphics processing unit.

10. The computer system of claim 1, wherein the controller is configured to control execution of the sequence of computations by the at least one graphics processing unit.

11. The computer system of claim 1, further comprising:

at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central [processor] processing unit, to acquire the input data in real time.

12. A method of performing a sequence of computations representing an artificial neural network on a computer system comprising a central processing unit (CPU), a main memory operably coupled to the central processing unit via a bus, an accelerator operably coupled to the CPU and the main memory via the bus, the accelerator comprising a graphics processing unit (GPU) and an accelerator memory, the method comprising:

(A) performing, by the GPU, the sequence of computations on a first portion of [the] input data so as to generate a first portion of [the] output data, the first portion of the output data representing an output of a neuron in a first layer of the artificial neural network, intermediate computations in the sequence of computations yielding intermediate results, wherein performing the sequence of computations on the first portion of the input data comprises (i) assigning an output variable to a first texture and a second texture, the output variable being included in a first computational element of a plurality of computational elements, the plurality of computational elements representing the sequence of computations and (ii) accumulating a first value for the output variable in the first texture during a first time step;

(B) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the input data from the main memory to the accelerator via the bus; [and]

(C) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the output data from the accelerator memory to the main memory via the bus, the second portion of the output data representing an output of a neuron in a second layer in the artificial neural network; and

(D) performing, by the GPU, the sequence of computations on the second portion of the input data, wherein performing the sequence of computations on the second portion of the input data comprises (i) accumulating a second value for the output variable in the second texture during a second time step and (ii) making the first value of the output variable in the first texture accessible to other computational elements in the plurality of computational elements during the second time step.

13. The method of claim 12, further comprising:

storing the input data in the main memory in response to a user interaction.

14. The method of claim 12, further comprising:

receiving the input data at a first rate; and

wherein (A) comprises performing the sequence of computations at a second rate different than the first rate.

15. Cancel claim 15.

16. The method of claim 12, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory without transferring any of the intermediate results of the plurality of sequential computations from the accelerator memory to the main memory so as to reduce data transfer via the bus.

17. The method of claim 12, wherein (C) comprises:

transferring the second portion of the output data from the accelerator memory to the main memory after the GPU has begun to perform another sequence of computations.

18. The method of claim 17, wherein (C) further comprises:

initiating transfer of the second portion of the output data in parallel with performance of at least one computation in the other sequence of computations.

19. The method of claim 12, further comprising:

acquiring the input data in real time with at least one of a video camera, a microphone, or a cell recording electrode operably coupled to the CPU.

20. The method of claim 12, further comprising:

storing parameters common to all of the computations in the sequence of computations in a first memory bank in the accelerator memory; and

storing data specific to at least one computation in the sequence of computations in a second memory bank in the accelerator memory.

21. A method of performing a sequence of computations representing an artificial neural network, the method comprising:

receiving, at a central processing unit (CPU), first input data acquired from an external system in real time;

initializing, by a controller operably coupled to a graphics processing unit (GPU), textures and shaders in a memory operably coupled to the GPU;

transferring the first input data received by the CPU to the memory operably coupled to the GPU;

performing, by the graphics processing unit (GPU), a first computation in the sequence of computations on the first input data based on the textures and shaders to generate first output data, computations in the sequence of computations representing respective layers of neurons in the artificial neural network, an output of the first computation in the sequence of computations representing an output of a first neuron in a first layer in the artificial neural network;

storing, in the memory operably coupled to the GPU, the first input data and the first output data; and

transferring second input data acquired from the external system in real time into the memory operably coupled to the GPU after the GPU starts the first computation and before the GPU starts a second computation of the sequence of computations, an output of the second computation in the sequence of computations representing an output of a second neuron in a second layer in the artificial neural network.

22. The method of claim 21, wherein transferring the second input data comprises transferring the second input data via a bus operably coupled to the CPU.

23. The method of claim 21, further comprising:

transferring the first output data from the memory to another memory during the second computation in the sequence of computations.

24. The method of claim 23, further comprising:

storing intermediate results of the sequence of computations in the memory, and

wherein transferring the first output data from the memory to the other memory occurs without transferring the intermediate results of the sequence of computations.

25. The method of claim 23, wherein transferring the second input data and transferring the first output data occurs in parallel.

26. The method of claim 21, further comprising:

storing, in a first memory partition of the memory, parameters common to all of the computations in the sequence of computations.

27. The method of claim 26, further comprising:

storing, in a second memory partition of the memory, data specific to the first computation in the sequence of computations.

28. The method of claim 27, further comprising:

storing, in the second memory partition, external input data patterns, representations of internal variables, an input of the computation in the sequence of computations, and the output of the computation in the sequence of computations.

29. The method of claim 21, wherein storing the first output data comprises:

accumulating, in the memory, outputs of computational elements executed by the GPU in performing the first computation in the sequence of computations.

30. The method of claim 21, further comprising:

storing, in the memory, an output of a previous computation in the sequence of computations; and

accessing, by the GPU, the output of the previous computation during performance of the computation in the sequence of computations.

31. The method of claim 21, wherein performing the first computation comprises executing a plurality of computational elements representing a layer of neurons in an artificial neural network.

32. The method of claim 31, wherein all neurons in the layer of neurons are described by the same equation.

33. The method of claim 21, further comprising:

acquiring the second input data with at least one of a video camera, a microphone, or a cell recording electrode.

34. The method of claim 21, further comprising:

loading the second input data from disk.

35. A system for performing a sequence of computations, the system comprising:

a camera to generate input data in real time;

a first memory partition;

a second memory partition operably coupled to the first memory partition; and

a processing unit, operably coupled to the camera, the first memory partition, and the second memory partition, to perform the sequence of computations on a first portion of the input data so as to generate a first portion of output data, intermediate computations in the sequence of computations yielding intermediate results, the first portion of the output data representing an output of an artificial neural network,

wherein the first memory partition is configured to transfer a second portion of the input data to the second memory partition in parallel with performance the sequence of computations by the processing unit,

wherein the second memory partition is configured to transfer a second portion of the output data to the first memory partition in parallel with performance the sequence of computations by the processing unit, and

wherein the sequence of computations represents the artificial neural network, each neuron in the artificial neural network has an output variable assigned to a first texture and a second texture in the memory, the first texture holds a first value of the output variable computed during a previous time step of the sequence of computations and accessible to other neurons in the neural network during a current time step of the sequence of computations and the second texture accumulates a second value of the output variable computed during the current time step.

36. The system of claim 35, wherein the first memory partition and the second memory partition are logical partitions.

37. The system of claim 35, wherein the processing unit is comprises a graphics processing unit (GPU).

38. The system of claim 35, wherein the processing unit is configured to receive the input data at a first rate and to perform the sequence of computations at a second rate is different than the first rate.

39. The system of claim 35, wherein the second memory partition is configured to transfer the second portion of the output data to the first memory partition without transferring any of the intermediate results to the first memory partition.

40. A system for executing an artificial neural network, the system comprising:

a central processing unit (CPU) to provide first input data;

a memory, operably coupled to the CPU, to store the first input data in a first partition, referenced by a first pointer, before computing a first layer of neurons of the artificial neural network;

a processing unit, operably coupled to the memory, to perform, during computation of the first layer of neurons, at least one calculation on the first input data so as to generate first output data, the first output data representing an output of at least one neuron in the first layer of neurons; and

a controller, operably coupled to the processing unit and the memory, to:

store the first output data in a second partition of the memory, the second partition referenced by a second pointer, and to swap the first pointer with the second pointer at the end of the computation of the first layer of neurons, such that the first output data becomes an input for a second layer of neurons of the artificial neural network,

transfer the first output data to another memory during computation of the second layer of neurons, and

dictate an order of execution of instructions to the processing unit to perform the computation of the first layer of neurons.

41. The system of claim 40, wherein the processing unit comprises a graphics processing unit.

42. The system of claim 40, wherein the controller is configured to send instructions for performing the at least one calculation to the processing unit.

43. The system of claim 40, wherein the memory further comprises:

a third partition to store internal variables; and

a fourth partition to store data used as input at a particular layer of neurons of the artificial neural network.

44. A computer system, comprising:

a central processing unit to receive input data acquired from an external system;

main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit;

an accelerator, operably coupled to the central processing unit and the main memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising:

at least one processing unit to perform a sequence of computations representing an artificial neural network on the at least a portion of the input data so as to generate output data, intermediate computations in the sequence of computations representing layers of the neural network and yielding intermediate results; and

accelerator memory, operably coupled to the at least one processing unit, to store the results of the sequence of computations; and

a controller, operably coupled to the at least one processing unit and the accelerator memory, to control transfer of the at least a portion of the input data into the accelerator memory during performance of the intermediate computations in the sequence of computations by the at least one processing unit, to control transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the intermediate computations in the sequence of computations by the at least one processing unit, and to control performance of the sequence of computations by the at least one processing unit.

45. The computer system of claim 44, wherein the central processing unit is configured to receive the input data in response to a user interaction.

46. The computer system of claim 44, wherein:

the central processing unit is configured to receive the input data at a first rate; and

the at least one processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

47. The computer system of claim 44, wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

48. The computer system of claim 44, wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

49. The computer system of claim 44, wherein accelerator memory comprises:

a first memory partition to store parameters common to all of the computations in the sequence of computations; and

a second memory partition to store data specific to at least one computation in the sequence of computations.

50. The computer system of claim 44, wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

51. The computer system of claim 44, wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one processing unit has begun to perform another sequence of computations.

52. The computer system of claim 51, wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one processing unit.

53. The computer system of claim 44, wherein the controller is configured to control execution of the sequence of computations by the at least one processing unit.

54. The computer system of claim 44, further comprising:

at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central processing unit, to acquire the input data in real time.

55. The computer system of claim 1, wherein the controller is configured to inform the central processing unit that the sequence of computations is finished.

56. The computer system of claim 1, wherein the controller is configured to reduce a processing load on the central processing unit.

57. The computer system of claim 1, wherein the controller is configured to reduce interactions between the central processing unit and the accelerator.

58. (New, Amended) A method of executing computations representing an artificial neural network on a computer system comprising at least one central processing unit (CPU), a processing unit, a first memory partition, and a second memory partition, the method comprising:

executing, by the at least one CPU, a user interaction stream, the user interaction stream controlling transfer of inputs to the artificial neural network to the first memory partition and the second memory partition;

executing, by the processing unit, a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network;

shifting priority from the user interaction stream to the computational stream in response to starting execution of the computations representing the artificial neural network; and

shifting priority from the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network.

59. (New) The method of claim 58, wherein the user interaction stream controls data exchange between the user interaction stream and the computational stream outside of execution of the computations representing the artificial neural network.

60. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of computational elements of the computations representing the artificial neural network.

61. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of parameters of the computations representing the artificial neural network.

62. (New) The method of claim 58, wherein executing the user interaction stream comprises:

controlling setting and editing of parameters of the inputs to the artificial neural network.

63. (New) The method of claim 58, wherein executing the user interaction stream comprises:

specifying an output to be saved to disk and/or displayed on a screen.

64. (New) The method of claim 58, wherein executing the user interaction stream comprises:

parsing elements to be used in the computations representing the artificial neural network.

65. (New) The method of claim 64, wherein the processing unit comprises a graphics processing unit (GPU) and executing the user interaction stream further comprises:

converting the elements into GPU programs.

66. (New) The method of claim 65, wherein executing the user interaction stream comprises:

compiling the GPU programs.

67. (New) The method of claim 66, wherein executing the user interaction stream comprises:

transferring the GPU programs to the second memory partition.

68. (New) The method of claim 58, further comprising:

executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk.

69. (New) The method of claim 58, further comprising:

generating the inputs with a video camera during execution of the computations.

70. (New) A system for executing computations representing an artificial neural network, the system comprising:

a camera to acquire input data for the artificial neural network;

a first memory partition;

a second memory partition;

at least one central processing unit (CPU), operably coupled to the camera, the first memory partition, and the second memory partition, to execute a user interaction stream, the user interaction stream controlling transfer of the input data acquired by the camera to the first memory partition and the second memory partition; and

a processing unit, operably coupled to the at least one memory and the CPU, to execute a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations

representing the artificial neural network, the execution of the computations representing the artificial neural network occurring while the camera is acquiring the input data.

REMARKS

Entry and consideration of the foregoing amendments is respectfully requested. New claims 58–68 were filed with the application and are supported at least by col. 7, lines 1–53; column 7, line 66 through column 8, line; column 8, lines 12–17; and FIG. 3 of U.S. Patent No. 9,189,828 ("the '828 patent").

Claim 58 is being amended to recite shifting priorities between the user interaction and computational streams. Support for this amendment appears at least in column 7, lines 45–53 of the '828 patent.

Claims 69 and 70 are being added. Support for these claims appears at least in col. 7, lines 1–53; column 7, line 66 through column 8, line; column 8, lines 12–17; and FIG. 3 of the '828 patent.

Recapture does not apply to claims 58–70 with respect to the parent patents because these new claims are directed to a "separate species or embodiment" than the claims of the priority patents, U.S. Patent No. RE48,438 ("the '438 patent"), the '828 patent, and U.S. Patent No. 8,468,867 ("the '867 patent").[1] More specifically, claims 58–70 are directed to the embodiment of FIG. 3, which shows top-level control of the GPU accelerator system. They each recite "a user interaction stream" and "a computational stream," neither of which appear in the claims of the '438 patent, the '828 patent, or the '867 patent. These streams make the subject matter of claims 58–70 patentably distinct from the claims issued in the '438 patent, the '828 patent, and the '867 patent.[2]

Assuming *arguendo* recapture did apply to claims 58–70, it would apply with respect to ***claim 9*** of the'867 patent because claims 58–70 are more similar to claim 9 of the '867 patent than to any other issued claim in the '438 patent, the '828 patent, or the '867 patent. Claim 9 of the '867 patent recites:

> 9. An accelerator system for a computer system performing a numerical simulation, the accelerator system comprising:
>
> at least one graphics processing unit to generate output data by performing at least one computation during a first computational cycle of the numerical simulation;
>
> an accelerator memory, operably coupled to the at least one graphics processing unit, to store data used to perform the at least one computation; and

[1] *See* MPEP § 1412.01(II) ("Claims to separate inventions/embodiments/species that were disclosed but never covered by the claims in the original application prosecution are claims to overlooked aspects. In other words, the reissue claims are drawn to a separate invention or separate species or embodiment that was not covered by a claim (e.g., a generic claim) at any point during the prosecution of the original application…. Recapture analysis would not need to be continued for claims drawn to overlooked aspects.").

[2] MPEP § 802.01 ("[R]elated inventions are distinct if the inventions as claimed are not connected in at least one of design, operation, or effect (e.g., can be made by, or used in, a materially different process) and wherein at least one invention is PATENTABLE (novel and nonobvious) OVER THE OTHER (though they may each be unpatentable over the prior art).").

> an accelerator controller, operably coupled to the accelerator memory and the at least one graphics processing unit, to execute:
>
> (i) a computational stream controlling performance of the at least one computation by the at least one graphics processing unit;
>
> (ii) an output stream controlling transfer of the output data from the at least one graphics processing unit to the accelerator memory during the first computational cycle; and
>
> (iii) an input stream controlling transfer of input data to the accelerator memory for use by the at least one graphics processing unit during a second computational cycle of the numerical simulation.

Nevertheless, applying the three-step recapture test shows that recapture doesn't apply to claims 58–70 with respect to claim 9 either:

First, independent claims 58 and 70 are broader than claim 9 because they don't include all the elements of claim 9 (for instance, neither claim 58 nor 70 recite "an output stream" or "an input stream" as in claim 9).

Second, the broader aspects of claims 58 and 70 do relate to subject matter surrendered during prosecution of claim 9, namely, the accelerator controller and the computational, output, and input streams.[3]

But third, recapture does not apply at step 3 because claims 58 and 70 are materially narrower than claim 9 in at least three respects: they each recite (1) "computations representing an artificial neural network"; (2) "a user interaction stream" that controls "transfer of inputs to the artificial neural network to the first memory partition and the second memory partition"; and (3) "a computational stream" that controls "data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network." An artificial neural network is more specific than the computational cycles that contributed to the patentability of claim 9 over the art. Likewise, the first and second memory partitions in claims 58 and 70 are more specific than the accelerator memory in added portions of claim 9. And the functions of the user interaction and computational streams in claims 58 and 70 are more specific than the functions of the computational, input, and output streams of claim 9. All of these more specific features make claims 58 and 70 materially narrower than claim 9 of the '867 patent.

Independent claims 58 and 70 are also narrower than independent claims 68 and 79 from U.S. Application No. 15/808,201 ("the '201 application"), which issued as the '438 patent. Claim 58 recites "shifting priority," which doesn't appear in claims 68 or 79 of the '201 application. And

[3] Amendment filed on July 31, 2013 in U.S. Application No. 11/860,254 at page 14 ("Applicants respectfully submit that Chung and Evans, alone or in combination, fail to disclose or suggest all of the elements recited in claim 10 [issued claim 9 in the '867 patent]. More specifically, nowhere does Chung or Evans disclose or suggest an accelerator controller that executes a computational stream to control performance of a first computation, an output stream to transfer data at the end of the first computational cycle, and an input stream to control the transfer of input data into the accelerator memory. Therefore, no combination of Chung and Evans yields an accelerator system that includes the accelerator controller of claim 10 as amended.").

claim 70 recites the limitations "a camera to acquire input data for the artificial neural network" and that "the execution of the computations representing the artificial neural network occur[s] while the camera is acquiring the input data," which likewise don't appear in claims 68 and 79of the '201 application. Because claims 58 and 70 are narrower than claims 68 and 79 of the '201 application, recapture doesn't apply with respect to claims 68 and 79 of the '201 application.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 60-1876.

Dated: June 24, 2021

Respectfully submitted,

Smith Baluch LLP
376 Boylston St, Suite 401
Boston MA 02116

Phone: (617) 947-7280

By /Christopher Max Colice/
Christopher Max Colice
Registration No. 65634

Electronic Patent Application Fee Transmittal

Application Number:	17136343
Filing Date:	29-Dec-2020
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	2	50	100
INDEPENDENT CLAIMS IN EXCESS OF 3	2201	1	240	240
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**340**

Electronic Acknowledgement Receipt

EFS ID:	43080197
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	24-JUN-2021
Filing Date:	29-DEC-2020
Time Stamp:	15:30:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$340
RAM confirmation Number	E20216NF30544457
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NRLA-001US04_Preliminary_Amendment_Claims.pdf	318356 90e2ce6cfba37bb091f392ad99b4ffc792f90035	yes	17

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	14
Applicant Arguments/Remarks Made in an Amendment	15	17

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31873 e1dab91ca061c7ad9ae8fb9d4b3665e56f974ba1	no	2

Warnings:

Information:

Total Files Size (in bytes):	350229

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/136,343	12/29/2020	3992	5400	NRLA-001US04	67	7

CONFIRMATION NO. 6235

CORRECTED FILING RECEIPT

OC000000126885734

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

Date Mailed: 07/09/2021

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

Applicant(s)

Neurala, Inc., Boston, MA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Neurala, Inc., Boston, MA
Neurala, Inc., Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 149890

Domestic Priority data as claimed by applicant

This application is a REI of 14/147,015 01/03/2014 PAT 9189828
which is a CON of 11/860,254 09/24/2007 PAT 8648867
which claims benefit of 60/826,892 09/25/2006
This application 17/136,343
is a CON of 15/808,201 11/09/2017 PAT RE48438
which is a REI of 14/147,015 01/03/2014 PAT 9189828
which is a CON of 11/860,254 09/24/2007 PAT 8648867
which claims benefit of 60/826,892 09/25/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/05/2021
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/136,343**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Litigation Search Report CRU 3999

Reissue Serial No. 17/136,343

To: William Wood	**From: Renee Preston**
Location: CRU	**Location: CRU 3999 / REM 4C75**
Art Unit: 3992	**Phone: (571) 272-1607**
Date: 02/18/2022	**E-mail: renee.preston@uspto.gov**

Search Notes

U.S. Patent Number: 9,189,828

1. Performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.
2. Performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.
3. Performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.
4. Performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.
5. Performed a search in Lexis in the news databases for any articles about the patent or any articles about litigation on this patent.

Litigation: No cases found

Paper No. 02/18/2022

Citing References (14)

Treatment	Title	Date	Type	Depth	Headnote(s)
—	**1.** COMPUTER SYSTEM E.G. STANDARD PERSONAL COMPUTER, HAS ACCELERATOR CONTROLLER MOVING INPUT DATA INTO ACCELERATOR MEMORY, MOVING OUTPUT DATA FROM MEMORY AND SUPERVISING DATA EXCHANGE BETWEEN MEMORY AND GRAPHIC PROCESSING UNIT Out Of Plan DWPI 2008-G81326	Sep. 25, 2006	DWPI	—	—
—	**2.** COMPUTER SYSTEM E.G. STANDARD PERSONAL COMPUTER (PC) HAS ACCELERATOR CONTROLLER IN EXPANSION CARD, FOR MOVING INPUT DATA AND OUTPUT DATA AND FOR SUPERVISING DATA EXCHANGE BETWEEN ACCELERATOR MEMORY AND GRAPHIC PROCESSING UNIT Out Of Plan DWPI 2014-M93893	Sep. 25, 2006	DWPI	—	—
—	**3.** RF 032166/0594 Out Of Plan	Feb. 06, 2014	Assignments	—	—
—	**4.** RF 032138/0737 Out Of Plan	Feb. 04, 2014	Assignments	—	—
—	**6.** PatStat 9189828	Feb. 16, 2021	Patent Status Files	—	—
—	**7.** PatStat 9189828	Jan. 16, 2018	Patent Status Files	—	—
—	**8.** METHODS AND APPARATUS FOR ITERATIVE NONSPECIFIC DISTRIBUTED RUNTIME ARCHITECTURE AND ITS APPLICATION TO CLOUD INTELLIGENCE Out Of Plan US PAT 11070623 , U.S. PTO Utility	July 20, 2021	Patents	—	—
—	**9.** METHODS AND APPARATUS FOR EARLY SENSORY INTEGRATION AND ROBUST ACQUISITION OF REAL WORLD KNOWLEDGE Out Of Plan US PAT 10974389 , U.S. PTO Utility	Apr. 13, 2021	Patents	—	—
—	**10.** GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD Out Of Plan US PAT RE48438+ , U.S. PTO Reissue	Feb. 16, 2021	Patents	—	—
—	**11.** METHODS AND APPARATUS FOR AUTONOMOUS ROBOTIC CONTROL Out Of Plan US PAT 10503976 , U.S. PTO Utility	Dec. 10, 2019	Patents	—	—
—	**12.** METHODS AND APPARATUS FOR ITERATIVE NONSPECIFIC DISTRIBUTED RUNTIME ARCHITECTURE AND ITS APPLICATION TO CLOUD INTELLIGENCE Out Of Plan US PAT 10469588 , U.S. PTO Utility	Nov. 05, 2019	Patents	—	—

WESTLAW © 2022 Thomson Reuters. No claim to original U.S. Government Works.

Treatment	Title	Date	Type	Depth	Headnote(s)
—	**13.** METHODS AND APPARATUS FOR EARLY SENSORY INTEGRATION AND ROBUST ACQUISITION OF REAL WORLD KNOWLEDGE Out Of Plan US PAT 10300603 , U.S. PTO Utility	May 28, 2019	Patents	—	—
—	**14.** METHODS AND APPARATUS FOR AUTONOMOUS ROBOTIC CONTROL Out Of Plan US PAT 10083523 , U.S. PTO Utility	Sep. 25, 2018	Patents	—	—
—	**15.** METHODS AND APPARATUS FOR AUTONOMOUS ROBOTIC CONTROL Out Of Plan US PAT 9626566 , U.S. PTO Utility	Apr. 18, 2017	Patents	—	—

WESTLAW © 2022 Thomson Reuters. No claim to original U.S. Government Works.

US9189828B2 - Graphic processor based accelerator system and method

Original

Bibliographic information & Images

Publication number and date
US9189828B2
2015-11-17

Granted

Application number and date
US14147015 (/api/control?query=AN:("US14147015")&autosearch=true)
2014-01-03

Priority number and date
US14147015 (/api/control?query=PRN:("US14147015")&autosearch=true)
2014-01-03

Ultimate owner
NEURALA INC (/api/control?query=uo:("NEURALA%20INC")&autosearch=true)

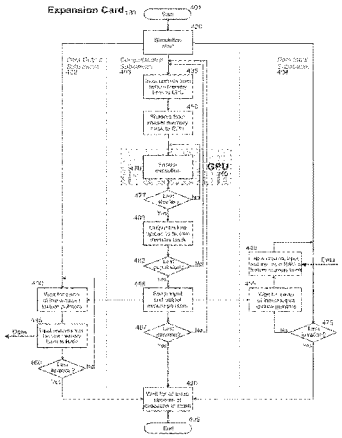
Original assignee
Neurala Inc. (/api/control?query=pa:("Neurala%20Inc.")&autosearch=true)

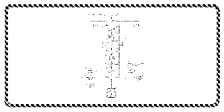
Current assignee
NEURALA LLC, MASSACHUSETTS (/api/control?query=pacu:("NEURALA%20LLC%2C%20MASSACHUSETTS")&autosearch=true)

Inventor
Massimiliano Versace (/api/control?query=in:("Massimiliano%20Versace")&autosearch=true)

Legal representative
Cooley LLP (/api/control?query=ag:("Cooley%20LLP")&autosearch=true)

1/6 Clipped image





Abstract

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

Original

Claims

1. A computer system, comprising: a central processing unit to receive input data; main memory, operably coupled to the central processing unit via a bus, to store the input data received by the central processing unit; an accelerator, operably coupled to the central processing unit and the first memory via the bus, to receive at least a portion of the input data from the main memory, the accelerator comprising: at least one graphics processing unit to perform a sequence of computations on the at least a portion of the input data so as to generate output data, intermediate computations in the sequence of computations yielding intermediate results; and accelerator memory, operably coupled to the graphic processing unit, to store the results of the plurality of sequential computations; and a controller, operably coupled to the at least one graphics processing unit and the accelerator memory, to transfer the at least a portion of the input data into the accelerator memory, and to transfer at least a portion of the output data from the accelerator memory to the main memory during performance of the sequence of computations by the at least one graphic processing unit.

2. The computer system of claim 1 , wherein the central processing unit is configured to receive the input data in response to a user interaction.

3. The computer system of claim 1 , wherein: the central processing unit is configured to receive the input data at a first rate; and the at least one graphics processing unit is configured to perform the sequence of computations at a second rate different than the first rate.

4. The computer system of claim 1 , wherein the main memory is configured to store a copy of the output data stored in the accelerator memory.

5. The computer system of claim 1 , wherein an output of at least one computation in the sequence of computations represents an output of at least one neuron in an artificial neural network.

6. The computer system of claim 1 , wherein accelerator memory comprises: a first memory bank to store parameters common to all of the computations in the sequence of computations; and a second memory bank to store data specific to at least one computation in the sequence of computations.

7. The computer system of claim 1 , wherein the controller is configured to transfer the output data from the accelerator memory to the main memory without transferring any of the intermediate results from the accelerator memory to the main memory so as to reduce data transfer via the bus.

8. The computer system of claim 1 , wherein the controller is configured to transfer at least a portion of the output data from the accelerator memory to the main memory after the at least one graphics processing unit has begun to perform another sequence of computations.

9. The computer system of claim 8 , wherein the controller is configured to initiate transfer of the at least a portion of the input data and to transfer the at least a portion of the output data in parallel with performance of at least one computation in the other sequence of computations by the at least one graphics processing unit.

10. The computer system of claim 1 , wherein the controller is configured to control execution of the sequence of computations by the at least one graphics processing unit.

11. The computer system of claim 1 , further comprising: at least one of a video camera, a microphone, or a cell recording electrode, operably coupled to the central processor unit, to acquire the input data in real time.

12. A method of performing a sequence of computations on a computer system comprising a central processing unit (CPU), a main memory operably coupled to the central processing unit via a bus, an accelerator operably coupled to the CPU and the main memory via the bus, the accelerator comprising a graphics processing unit (GPU) and an accelerator memory, the method comprising: (A) performing, by the GPU, the sequence of computations on a first portion of the input data so as to generate a first portion of the output data, intermediate computations in the sequence of computations yielding intermediate results; (B) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the input data from the main memory to the accelerator via the bus; and (C) in parallel with performing the sequence of computations by the GPU in (A), transferring a second portion of the output data from the accelerator memory to the main memory via the bus.

13. The method of claim 12 , further comprising: storing the input data in the main memory in response to a user interaction.

14. The method of claim 12 , further comprising: receiving the input data at a first rate; and wherein (A) comprises performing the sequence of computations at a second rate different than the first rate.

15. The method of claim 12 , wherein (A) comprises: generating an output representative of an output of at least one neuron in an artificial neural network.

16. The method of claim 12 , wherein (C) comprises: transferring the second portion of the output data from the accelerator memory to the main memory without transferring any of the intermediate results of the plurality of sequential computations from the accelerator memory to the main memory so as to reduce data transfer via the bus.

17. The method of claim 12 , wherein (C) comprises: transferring the second portion of the output data from the accelerator memory to the main memory after the GPU has begun to perform another sequence of computations.

18. The method of claim 17 , wherein (C) further comprises: initiating transfer of the second portion of the output data in parallel with performance of at least one computation in the other sequence of computations.

19. The method of claim 12 , further comprising: acquiring the input data in real time with at least one of a video camera, a microphone, or a cell recording electrode operably coupled to the CPU.

20. The method of claim 12 , further comprising: storing parameters common to all of the computations in the sequence of computations in a first memory bank in the accelerator memory; and storing data specific to at least one computation in the sequence of computations in a second memory bank in the accelerator memory.

Original

Families

Display in a list (/api/control?familiesSearch=_) INPADOC

This section contains all family relations of this particular document. For more information about the different families, refer to the User Manual (Glossary/Families).

Extended (5) Priority date/claims	Complete (2) Priority date/claims	Main (2) Priority date/claims	Domestic (2) Priority date/claims	Publication number	Application number	Title	Status
2007-09-24 US11860254 US14147015 US15808201 US60826892	2017-11-09 US11860254 US14147015 US15808201 US60826892	2017-11-09 US11860254 US14147015 US15808201 US60826892	2017-11-09	USRE048438E	US15808201	Graphic processor based accelerator system and method	Granted
	2014-01-03 US11860254 US14147015 US60826892	2014-01-03 US11860254 US14147015 US60826892	2014-01-03	US9189828B2	US14147015	Graphic processor based accelerator system and method	Granted
				US20140192073A1	US14147015	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	Granted
	2007-09-24 US11860254 US60826892	2007-09-24 US11860254 US60826892	2007-09-24	US8648867B2	US11860254	Graphic processor based accelerator system and method	Granted
				US20080117220A1	US11860254	Graphic Processor Based Accelerator System and Method	Granted

Description

RELATED APPLICATIONS

[0001] The present application claims a priority benefit, under 35 U.S.C. §120, as a continuation of U.S. application Ser. No. 11/860,254, now U.S. Pat. No. 8,648,867 B2, filed Sep. 24, 2007, entitled "Graphic Processor Based Accelerator System and Method," which claims the priority benefit, under 35 U.S.C. §119(e), of U.S. Application No. 60/826,892, filed Sep. 25, 2006. Each of the above-identified applications is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Graphics Processing Units (GPUs) are found in video adapters (graphic cards) of most personal computers (PCs), video game consoles, workstations, etc. and are considered highly parallel processors dedicated to fast computation of graphical content. With the advances of the computer and console gaming industries, the need for efficient manipulation and display of 3D graphics has accelerated the development of GPUs.

[0003] In addition, manufacturers of GPUs have included general purpose programmability into the GPU architecture leading to the increased popularity of using GPUs for highly parallelizable and computationally expensive algorithms outside of the computer graphics domain. When implemented on conventional video card architectures, these general purpose GPU (GPGPU) applications are not able to achieve optimal performance, however. There is overhead for graphics-related features and algorithms that are not necessary for these non-video applications.

SUMMARY

[0004] Numerical simulations, e.g., finite element analysis, of large systems of similar elements (e.g. neural networks, genetic algorithms, particle systems, mechanical systems) are one example of an application that can benefit from GPGPU computation. During numerical simulations, disk and user input/output can be performed independently of computation because these two processes require interactions with peripheral hardware (disk, screen, keyboard, mouse, etc) and put relatively low load on the central processing unit/system (CPU). Complete independence is not desirable, however; user input might affect how the computation is performed and even interrupt it if necessary. Furthermore, the user output and the disk output are dependent on the results of the computation. A reasonable solution would be to separate input/output into threads, so that it is interacting with hardware occurs in parallel with the computation. In this case whatever CPU processing is required for input/output should be designed so that it provides the synchronization with computation.

[0005] In the case of GPGPU, the computation itself is performed outside of the CPU, so the complete system comprises three "peripheral" components: user interactive hardware, disk hardware, and computational hardware. The central processing unit (CPU) establishes communication and synchronization between peripherals. Each of the peripherals is preferably controlled by a dedicated thread that is executed in parallel with minimal interactions and dependencies on the other threads.

[0006] A GPU on a conventional video card is usually controlled through OpenGL, DirectX, or similar graphic application programming interfaces (APIs). Such APIs establish the context of graphic operations, within which all calls to the GPU are made. This context only works when initialized within the same thread of execution that uses it. As a result, in a preferred embodiment, the context is initialized within a computational thread. This creates complications, however, in the interaction between the user interface thread that changes parameters of simulations and the computational thread that uses these parameters.

[0007] A solution as proposed here is an implementation of the computational stream of execution in hardware, so that thread and context initialization are replaced by hardware initialization. This hardware implementation includes an expansion card comprising a printed circuit board having (a) one or more graphics processing units, (b) two or more associated memory banks that are logically or physically partitioned, (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the CPU is freed from this function and is dedicated to other tasks. In this case a few controls (simulation start

and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

[0008] In general, according to one aspect, the invention features a computer system. This system comprises a central processing unit, main memory accessed by the central processing unit, and a video system for driving a video monitor in response to the central processing unit as is common. The computer system further comprises an accelerator that uses input data from and provides output data to the central processing unit. This accelerator comprises at least one graphics processing unit, accelerator memory for the graphic processing unit, and an accelerator controller that moves the input data into the at least one graphics processing unit and the accelerator memory to generate the output data.

[0009] In the preferred, the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit. Preferably, the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit. The use of the separate controller enables data transfer during execution such that the accelerator controller transfers output data from the accelerator memory to main memory of the central processing unit.

[0010] In the preferred embodiment, the accelerator controller comprises an interface controller that enables the accelerator to communicate over a bus of the computer system with the central processing unit.

[0011] In general according to another aspect, the invention also features an accelerator system for a computer system, which comprises at least one graphics processing unit, accelerator memory for the graphic processing unit and an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory.

[0012] In general according to another aspect, the invention also features a method for performing numerical simulations in a computer system. This method comprises a central processing unit loading input data into an accelerator system from main memory of the central processing unit and an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data. The accelerator controller then transfers output data generated by the graphic processing unit to the central processing unit as output data.

[0013] The above and other features of the invention including various novel details of construction and combinations of parts, and other advantages, will now be more particularly described with reference to the accompanying drawings and pointed out in the claims. It will be understood that the particular method and device embodying the invention are shown by way of illustration and not as a limitation of the invention. The principles and features of this invention may be employed in various and numerous embodiments without departing from the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] In the accompanying drawings, reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale; emphasis has instead been placed upon illustrating the principles of the invention. Of the drawings:

[0015] FIG. 1 is a schematic diagram illustrating a computer system including the GPU accelerator according to an embodiment of the present invention;

[0016] FIG. 2 is block diagram illustrating the architecture for the GPU accelerator according to an embodiment of the present invention;

[0017] FIG. 3 is a block/flow diagram illustrating an exemplary implementation of the top level control of the GPU accelerator system;

[0018] FIG. 4 is a flow diagram illustrating an exemplary implementation of the bottom level control of the GPU accelerator system that is used to execute the target computation; and

[0019] FIG. 5 is an example population of nine computational elements arranged in a 3×3 square and a potential packing scheme for texture pixels, according to an implementation of the present invention.

DETAILED DESCRIPTION

[0020] FIG. 1 shows a computer system **100** that has been constructed according to the principles of the present invention.

[0021] In more detail, the computer system **100** in one example is a standard personal computer (PC). However, this only serves as an example environment as computing environment **100** does not necessarily depend on or require any combination of the components that are illustrated and described herein. In fact, there are many other suitable computing environments for this invention, including, but not limited to, workstations, server computers, supercomputers, notebook computers, hand-held electronic devices such as cell phones, mp3 players, or personal digital assistants (PDAs), multiprocessor systems, programmable consumer electronics, networks of any of the above-mentioned computing devices, and distributed computing environments that including any of the above-mentioned computing devices.

[0022] In one implementation the GPU accelerator is implemented as an expansion card **180** includes connections with the motherboard **110**, on which the one or more CPU's **120** are installed along with main, or system memory **130** and mass/non volatile data storage **140**, such as hard drive or redundant array of independent drives (RAID) array, for the computer system **100**. In the current example, the expansion card **180** communicates to the motherboard **110** via a local bus **190**. This local bus **190** could be PCI, PCI Express, PCI-X, or any other functionally similar technology (depending upon the availability on the motherboard **110**). An external version GPU accelerator is also a possible implementation. In this example, the external GPU accelerator is connected to the motherboard **110** through USB-2.0, IEEE 1394 (Firewire), or similar external/peripheral device interface.

[0023] The CPU **120** and the system memory **130** on the motherboard **110** and the mass data storage system **140** are preferably independent of the expansion card **180** and only communicate with each other and the expansion card **180** through the system bus **200** located in the motherboard **110**. A system bus **200** in current generations of computers have bandwidths from 3.2 GB/s (Pentium 4 with AGTL+, Athlon XP with EV6) to around 15 GB/s (Xeon Woodcrest with AGTL+, Athlon 64/Opteron with Hypertransport), while the local bus has maximal peak data transfer rates of 4 GB/s (PCI Express 16) or 2 GB/s (PCI-X 2.0). Thus the local bus **190** becomes a bottleneck in the information exchange between the system bus **200** and the expansion card **180**. The design of the expansion card and methods proposed herein minimizes the data transfer through the local bus **190** to reduce the effect of this bottleneck.

[0024] The system memory **130** is referred to as the main random-access memory (RAM) in the description herein. However, this is not intended to limit the system memory **130** to only RAM technology. Other possible computer storage media include, but are not limited to ROM, EEPROM, flash memory, or any other memory technology.

[0025] In the illustrated example, the GPU accelerator system is implemented on an expansion card **180** on which the one or more GPU's **240** are mounted. It should be noted that the GPU accelerator system GPU **240** is separate from and independent of any GPU on the standard video card **150** or other video driving hardware such as integrated graphics systems. Thus the computations performed on the expansion card **180** do not interfere

with graphics display (including but not limited to manipulation and rendering of images).

[0026] Various brand of GPU are relevant. Under current technology, GPU's based on the GeForce series from NVIDIA Corporation or the Catalyst series from ATI/Advanced Micro Devices, Inc.

[0027] The output to a video monitor **170** is preferably through the video card **150** and not the GPU accelerator system **180**. The video card **150** is dedicated to the transfer of graphical information and connects to the motherboard **110** through a local bus **160** that is sometimes physically separate from the local bus **190** that connects the expansion card **180** to the motherboard **110**.

[0028] FIG. 2 is a block diagram illustrating the general architecture of the GPU accelerator system and specifically the expansion card **180** in which at least one GPU **240** and associated memories **210** and **250** are mounted. Electrical (signal) and mechanical coupling with a local bus **190** provides signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI, PCI-X, PCI Express, or functionally similar technology).

[0029] The GPU accelerator further preferably comprises one specifically designed accelerator controller **220**. Depending upon the implementation, the accelerator controller **220** is field programmable gate array (FPGA) logic, or custom built application-specific (ASIC) chip mounted in the expansion card **180**, and in mechanical and signal coupling with the GPU **240** and the associated memories **210** and **250**. During initial design, a controller can be partially or even fully implemented in software, in one example.

[0030] The controller **220** commands the storage and retrieval of arrays of data (on a conventional video card the arrays of data are represented as textures, hence the term 'texture' in this document refers to a data array unless specified otherwise and each element of the texture is a pixel of color information), execution of GPU programs (on a conventional video card these programs are called shaders, hence the term 'shader' in this document refers to a GPU program unless specified otherwise), and data transfer between the system bus **200** and the expansion card **180** through the local bus **190** which allows communication between the main CPU **120**, RAM **130**, and disk **140**.

[0031] Two memory banks **210** and **250** are mounted on the expansion card **180**. In some example, these memory banks separated in the hardware, as shown, or alternatively implemented as a single, logically partitioned memory component.

[0032] The reason to separate the memory into two partitions **210250** stems from the nature of the computations to which the GPU accelerator system is applied. The elements of computation (computational elements) are characterized by a single output variable. Such computational elements often include one or more equations. Computational elements are same or similar within a large population and are computed in parallel. An example of such a population is a layer of neurons in an artificial neural network (ANN), where all neurons are described by the same equation. As a result, some data and most of the algorithms are common to all computational elements within population, while most of the data and some algorithms are specific for each equation. Thus, one memory, the shader memory bank **210**, is used to store the shaders needed for the execution of the required computations and the parameters that are common for all computational elements and is coupled with the controller **220** only. The second memory, the texture memory bank **250**, is used to store all the necessary data that are specific for every computational element (including, but not limited to, input data, output data, intermediate results, and parameters) and is coupled with both the controller **220** and the GPU **240**.

[0033] The texture memory bank **250** is preferably further partitioned into four sections. The first partition **250** a is designed to hold the external input data patterns. The second partition **250***b* is designed to hold the data textures representing internal variables. The third partition **250***c* is designed to hold the data textures used as input at a particular computation step on the GPU **240**. The fourth partition **250***d* holds the data textures used to accommodate the output of a particular computational step on the GPU **240**. This partitioning scheme can be done logically, does not require hardware implementation. Also the partitioning scheme is also altered based on new designs or needs of the algorithms being employed. The reason for this partitioning is further explained in the Data Organization section, below.

[0034] A local bus interface **230** on the controller **220** serves as a driver that allows the controller **220** to communicate through the local bus **190** with the system bus **200** and thus the CPU **120** and RAM **130**. This local bus interface **230** is not intended to be limited to PCI related technology. Other drivers can be used to interface with comparable technology as a local bus **190**.

[0035] Data Organization

[0036] Each computational element discussed above has output variables that affect the rest of the system. For example in the case of a neural network it is the output of a neuron. A computational element also usually has several internal variables that are used to compute output variables, but are not exposed to the rest of the system, not even to other elements of the same population, typically. Each of these variables is represented as a texture. The important difference between output variables and internal variables is their access.

[0037] Output variables are usually accessed by any element in the system during every time step. The value of the output variable that is accessed by other elements of the system corresponds to the value computed on the previous, not the current, time step. This is realized by dedicating two textures to output variables—one holds the value computed during the previous time step and is accessible to all computational elements during the current time step, another is not accessible to other elements and is used to accumulate new values for the variable computed during the current time step. In-between time steps these two textures are switched, so that newly accumulated values serve as accessible input during the next time step, while the old input is replaced with new values of the variable. This switch is implemented by swapping the address pointers to respective textures as described in the System and Framework section.

[0038] Internal variables are computed and used within the same computational element. There is no chance of a race condition in which the value is used before it is computed or after it has already changed on the next time step because within an element the processing is sequential. Therefore, it is possible to render the new value of internal variable into the same texture where the old was read from in the texture memory bank. Rendering to more than one texture from a single shader is not implemented in current GPU architectures, so computational elements that track internal variables would have to have one shader per variable. These shaders can be executed in order with internal variables computed first, followed by output variables.

[0039] Further savings of texture memory is achieved through using multiple color components per pixel (texture element) to hold data. Textures can have up to four color components that are all processed in parallel on a GPU. Thus, to maximize the use of GPU architecture it is desirable to pack the data in such a way that all four components are used by the algorithm. Even though each computational element can have multiple variables, designating one texture pixel per element is ineffective because internal variables require one texture and output variables require two textures. Furthermore, different element types have different numbers of variables and unless this number is precisely a multiple of four, texture memory can be wasted.

[0040] A more reasonable packing scheme would be to pack four computational elements into a pixel and have separate textures for every variable associated with each computational element. In this case the packing scheme is identical for all textures, and therefore can be accessed using the same algorithm. Several ways to approach this packing scheme are outlined here. An example population of nine computational elements arranged in a 3×3 square (FIG. 5*a*) can be packed by element (FIG. 5*b*), by row (FIG. 5*c*), or by square (FIG. 5*d*).

[0041] Packing by element (FIG. 5*b*) means that elements **1**,**2**,**3**,**4** go into first pixel; **5**,**6**,**7**,**8** go into second pixel; **9** goes into third pixel. This is the most compact scheme, but not convenient because the geometrical relationship is not preserved during packing and its extraction depends on the size of the population.

[0042] Packing by row (column; FIG. 5*c*) means that elements **1**,**2**,**3** go into pixel (**1**,**1**); **3**,**4**,**5** go into pixel (**2**,**1**), **7**,**8**,**9** go into pixel (**3**,**1**). With this scheme the element's y coordinate in the population is the pixel's y coordinate, while the element's x coordinate in the population is the pixel's x coordinate times four plus the index of color component. Five by five populations in this case will use 2×5 texture, or 10 pixels. Five of these pixels will only use one out of four components, so it wastes 37.5% of this texture. 25×1 population will use 6×1 texture (six pixels) and will waste 12.5% of it.

[0043] Packing by square (FIG. 5*d*) means that elements **1**,**2**,**4**,**5** go into pixel (**1**,**1**); **3**,**6** go into pixel (**1**,**2**); **7**,**8** go into pixel (**2**,**1**), and **9** goes into pixel (**2**,**2**). Both the row and the column of the element are determined from the row (column) of the pixel times two plus the second (first) bit of the color component index. Five by five populations in this case will use 3×3 texture, or 9 pixels. Four of these pixels will only use two out of four components, and one will only use one component, so it wastes 34.4% of this texture. This is more advantageous than packing by row, since the texture is smaller and the waste is also lower. 25×1 population on the other hand will use 13×1 texture (thirteen pixels) and waste >50% of it, which is much worse than packing by row.

[0044] In order to eliminate waste altogether the population should have even dimensions in the square packing, and it should have a number of columns divisible by four in row packing. Theoretically, the chances are approximately equivalent for both of these cases to occur, so the particular task and data sizes should determine which packing scheme is preferable in each individual case.

[0045] The System and Framework

[0046] FIG. 3 shows an exemplary implementation of the top level system and method that is used to control the computation. It is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented in the invention described herein and so the implementation is not intended to be limited to the following description and accompanying figure.

[0047] The method presented herein includes two execution streams that run on the CPU **120**—User Interaction Stream **302** and Data Output Stream **301**. These two streams preferably do not interact directly, but depend on the same data accumulated during simulations. They can be implemented as separate threads with shared memory access and executed on different CPUs in the case of multi-CPU computing environment. The third execution stream—Computational Stream **303**—runs on the GPU accelerator of the expansion card **180** and interacts with the User Interaction Stream **302** through initialization routines and data exchange in between simulations. The Computational Stream **303** interacts with the User Interaction Stream and the Data Output Stream through synchronization procedures during simulations.

[0048] The crucial feature of the interaction between the User Interaction Stream **302** and the Computational Stream **303** is the shift of priorities. Outside of the simulation, the system **100** is driven by the user input, thus the User Interaction Stream **302** has the priority and controls the data exchange **304** between streams. After the user starts the simulation, the Computational Stream **303** takes the priority and controls the data exchange between streams until the simulation is finished or interrupted **350**.

[0049] The user starts **300** the framework through the means of an operating system and interacts with the software through the user interaction section **305** of the graphic user interface **306** executed on the CPU **120**. The start **300** of the implementation begins with a user action that causes a GUI initialization **307**, Disk input/output initialization **308** on the CPU **120**, and controller initialization **320** of the GPU accelerator on the expansion card **180**. GUI initialization includes opening of the main application window and setting the interface tools that allow the user to control the framework. Disk I/O initialization can be performed at the start of the framework, or at the start of each individual simulation.

[0050] The user interaction **305** controls the setting and editing of the computational elements, parameters, and sources of external inputs. It specifies which equations should have their output saved to disk and/or displayed on the screen. It allows the user to start and stop the simulation. And it performs standard interface functions such as file loading and saving, interactive help, general preferences and others.

[0051] The user interaction **305** directs the CPU **120** to acquire the new external input textures needed (this includes but is not limited to loading from disk **140** or receiving them in real time from a recording device), parses them if necessary **309**, and initializes their transfer to the expansion card **180**, where they are stored **325** in the texture memory bank **250** by the controller **220**. The user interaction **305** also directs the CPU **120** to parse populations of elements that will be used in the simulation, convert them to GPU programs (shaders), compile them **310**, and initializes their transfer to the expansion card **180**, where they are stored **326** in the shader memory bank **210** by the controller **220**. This operation is accompanied by the upload **309** of the initial data into the input partition of the texture memory bank **250**, and stores the shader order of execution in the controller **220**. The user can perform operations **309** and **310** as many times as necessary prior to starting the simulation or between simulations.

[0052] The editing of the system between simulations is difficult to accomplish without the hardware implementation of the computational thread suggested herein. The system of equations (computational elements) is represented by textures that track variables plus shaders that define processing algorithms. As mentioned above, textures, shaders and other graphics related constructs can only be initialized within the rendering context, which is thread specific. Therefore textures and shaders can only be initialized in the computational thread.

[0053] Network editing is a user-interactive process, which according to the scheme suggested above happens in the User Interaction Stream **302**. The simulation software thus has to take the new parameters from the User Interaction Stream **302**, communicate them to the Computational Stream **303** and regenerate the necessary shaders and textures. This is hard to accomplish without a hardware implementation of the Computational Stream **303**. The Computational Stream **303** is forked from the User Interaction Stream and it can access the memory of the parent thread, but the reverse communication is harder to achieve. The controller **220** allows operations **309** and **310** to be performed as many times as necessary by providing the necessary communication to the User Interaction Stream **302**.

[0054] After execution of the input parser texture generation **309** and population parser shader generator and compiler **310** are performed at least once, the user has the option to initialize the simulation **311**. During this initialization the main control of the framework is transferred to the GPU accelerator system's accelerator controller **220** and computation **330** is started (see FIG. 4; **420**). The user retains the ability to interrupt the simulation, change the input, or to change the display properties of the framework, but these interactions are queued to be performed at times determined by the controller-driven data exchange **314** and **316** to avoid the corruption of the data.

[0055] The progress monitor **312** is not necessary for performance, but adds convenience. It displays the percentage of completed time steps of the simulation and allows the user to plan the schedule using the estimates of the simulation wall clock times. Controller-driven data exchange **314** updates the display of the results **313**. Online screen output for the user selected population allows the user to monitor the activity and evaluate the qualitative behavior of the network. Simulations with unsatisfactory behavior can be terminated early to change parameters and restart. Controller-driven data exchange **314** also drives the output of the results to disk **317**. Data output to disk for convenience can be done on an element per file basis. A suggested file format includes a leftmost column that displays a simulated time for each of the simulation steps and subsequent columns that display variable values during this time step in all elements with identical equations (e.g. all neurons in a layer of a neural network).

[0056] Controller-driven data exchange or input parser texture generator **316** allows the user to change input that is generated on the fly during the simulation. This allows the framework monitoring of the input that is coming from a recording device (video camera, microphone, cell recording electrode, etc) in real time. Similar to the initial input parser **309**, it preprocesses the input into a universal format of the data array suitable for texture generation and generates textures. Unlike the initial parser **309**, here the textures are transferred to hardware not whenever ready but upon the request of the controller **220**.

[0057] The controller **220** also drives the conditional testing **315** and **318** informs the CPU-bound streams whether the simulation is finished. If so, the control returns to the User Interaction Stream. The user then can change parameters or inputs (**309** and **310**), restart the simulation (**311**) or quit the framework (**390**).

[0058] SANNDRA (Synchronous Artificial Neuronal Network Distributed Runtime Algorithm; http://www.kinness.net/Docs/SANNDRA/html) was developed to accelerate and optimize processing of numerical integration of large non-homogenous systems of differential equations. This library is fully reworked in its version 2.x.x to support multiple computational backends including those based on multicore CPUs, GPUs and other processing systems. GPU based backend for SANNDRA-2.x.x can serve as an example practical software implementation of the method and architecture described above and pictorially represented in FIG. 3.

[0059] To use SANNDRA, the application should create a TSimulator object either directly or through inheritance. This object will handle global simulation properties and control the User Interaction Stream, Data Output Stream, and Computational Stream. Through TSimulator::timestep( ), TSimulator::outfileInterval( ), and TSimulator::outmode( ), the application can set the time step of the simulation, the time step of disk output, and the mode of the disk output. The external input pattern should be packed into a TPattern object and bound to the simulation object through TSimulator::resetInputs( ) method. TSimulator::simLength( ) sets the length of the simulation.

[0060] The second step is to create at least one population of equations (Tpopulation object). Population holds one equation object TEquation. This object contains only a formula and does not hold element-specific data, so all elements of the population can share single TEquation.

[0061] The TEquation object is converted to a GPU program before execution. GPU programs have to be executed within a graphical context, which is stream specific. TSimulator creates this context within a Computational Stream, therefore all programs and data arrays that are necessary for computation have to be initialized within Computational Stream. Constructor of TPopulation is called from User Interaction Stream, so no GPU-related objects can be initialized in this constructor.

[0062] TPopulation::fillElements( ) is a virtual method designed to overcome this difficulty. It is called from within the Computational Stream after TSimulator::networkCreate( ) is called in the User Interaction Stream. A user has to override TPopulation::fillElements( ) to create TEquation and other computation related objects both element independent and element-specific. Element independent objects include subcomponents of TEquation and objects that describe how to handle interdependencies between variables implemented through derivatives of TGate class.

[0063] Element-specific data is held in TElement objects. These objects hold references to TEquation and a set of TGate objects. There is one TElement per population, but the size of data arrays within this object corresponds to population size. All TElement objects have to be added to the TSimulator list of elements by calling TSimulator::addUnit( ) method from TPopulation::fillElements( ).

[0064] Finally, TPopulation::fillElements( ) should contain a set of TElement::add*Dependency( ) calls for each element. Each of these calls sets a corresponding dependency for every TGate object. Here TGate object holds element independent part of dependency and TElement::add*Dependency( ) sets element-specific details.

[0065] System provided TPopulation handles the output of computational elements, both when they need to exchange the data and when they need to output it to disk. User implementation of TPopulation derivative can add screen output.

[0066] Listing 1 is an example code of the user program that uses a recurrent competitive field (RCF) equation:

[0067]

Listing 1

```
uint16_t w = 3, h = 3;
static float m_compet = 0.5;
static float m_persist = 1.0;
class TCablePopRCF : public TPopulation
{
TEq_RCF* m_equation;
TGate* m_gatel;
TGate* m_gate2;
void createGatingStructure( )
{
m_gatel = new TGate(0);
m_gate2 = new TGate(1);
};
void createUnitStructure(TBasicUnit* u)
{
u->addO2OPInputDependency(m_gatel, 0., 0., 0.004, 0., 0, 0);
u->addFullDependency(m_gate2, population( ));
}
public: TCablePopRCF( ) : TPopulation("compCPU RCF", w, h, true) { };
~TCablePopRCF( ) {if(m_equation) delete m_equation;
   if(m_gatel) delete m_gatel;
   if(m_gate2) delete m_gate2;};
bool fillElements(TSimulator* sim);
};
bool TCablePopRCF::fillElements(TSimulatior* sim)
```

```
{
m_equation = new TEq_RCF(this, m_compet, m_persist);
createGatingStructure( );
for(size_t i = 0; i < xSize( ); ++i)
for(size_t j = 0; j < ySize( ); ++j)
{
TElement* u = new TCPUElement(this, m_equation, i, j);
sim->addUnit(u);
createUnitStructure(u);
}
Return true;
}
int
main( )
{
// Input pattern generation (309 in FIG.3)
uint32_t* pat = new uint32_t[w*h];
TRandom<float> randGen (0);
for(uint32_t I = 0; I < w*h; ++i)
pat[i] = randGen.random( );
Tpattern* p = new Tpattern(pat, w, h);
// Setting up the simulation
TSimulator* cableSim = new TSimulator("data"); //(308 and 320 in
FIG. 3)
cableSim->timestep(0.05); //(320 in FIG. 3)
cableSim->resetInputs(p); //(325 in FIG. 3)
cableSim->outfileInterval(0.1); //(308 in FIG. 3)
cableSim->outmode(SANNDRA::timefunc); //(308 in FIG. 3)
cableSim->simLength(60.0); //(320 in FIG. 3)
// Preparing the population
TPopulation* cablePop = new TCablePopRCF( ); //(310 in FIG. 3)
cableSim->networkCreate( ); //(326 in FIG. 3)
uint16_t user= 1;
while(user)
{
if(! cableSim->simulationStart(true, 1)) //(311 in FIG. 3)
exit(1);
std::cout<<"Repeat?\\n"; //(305 in FIG. 3)
std::cin>>user; //(305 in FIG. 3)
if(user == 1)
cableSim->networkReset( ); //(305 in FIG. 3)
{
If(cableSim)
Delete cableSim; //Also deletes cablePop and its internals
exit(0);
};
```

[0068] FIG. 4 is a detailed flow diagram illustrating a part of an exemplary implementation of the bottom level system and method performed during the computation on the GPU accelerator of the expansion card **180** and is a more detailed view of the computational box **330** in FIG. 3. FIG. 4 is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented.

[0069] With systems of equations that have complex interdependencies it is likely that the variable in some equation from a previous time step has to be used by some other equation after the new values of this variable are already computed for new time step. To avoid data confusion, the new values of variables should be rendered in a separate texture. After the time step is completed for all equations, these new values should be copied over old values so that they are used as input during the next time step. Copying textures is an expensive operation, computationally, but since the textures are referred to by texture IDs (pointers), swapping these pointers for input and output textures after each time step achieves the same result at a much lesser cost.

[0070] In the hardware solution suggested herein, ID swapping is equivalent to swapping the base memory address for two partitions of the texture memory bank **250**. They are swapped **485** during synchronization (**485**, **430**, and **455**) so that data transfer **445** and the computation **435**-**487** proceeds immediately and in parallel with data transfer as shown in FIG. 4. A hardware solution allows this parallelism through access of the controller **220** to the onboard texture memory bank **250**.

[0071] The main computation and data exchange are executed by the controller **220**. It runs three parallel substreams of execution: Computational Substream **403**, Data Output Substream **402**, and Data Input Substream **404**. These streams are synchronized with each other during the swap of pointers **485** to the input and output texture memory partitions of the texture memory bank **250** and the check for the last iteration **487**. Algorithmically, these two operations are a single atomic operation, but the block diagram shows them as two separate blocks for clarity.

[0072] The Computational Substream **403** performs a computational cycle including a sequential execution of all shaders that were stored in the shader memory bank **210** using the appropriate input and output textures. To begin the simulation the controller **220** initializes three execution substreams **403**, **402**, and **404**. On every simulation step, the Computational Substream **403** determines which textures the GPU **240** will need to perform the computations and initiates the upload **435** of them onto the GPU **240**. The GPU **240** can communicate directly with the texture memory bank **250** to upload the appropriate texture to perform the computations. The controller **220** also pulls the first shader (known by the stored order) from the shader memory bank **210** and uploads **450** it onto the GPU **240**.

[0073] The GPU **240** executes the following operations in this order: performs the computation (execution of the shader) **470**; tells the controller **220** that it is done with the computations for the current shader; and after all shaders for this particular equation are executed sends **480** the output textures to the output portion of the texture memory bank **250**. This cycle continues through all of the equations based on the branching step **482**.

[0074] An example shader that performs fourth order Runge-Kutta numerical integration is shown in Listing 2 using GLSL notation;

[0075]

Listing 2

```
uniform sampler2DRect Variable;
uniform float integration_step;
float halfstep = integration_step*0.5;
float fl_6step = integration_step/6.0;
vec4 output = texture2DRect(Variable, gl_TexCoord[0].st);
// define equation( ) here
vec4 rungekutta4(vec4 x)
{
const vec4 kl = equation(x);
const vec4 k2 = equation(x + halfstep*kl);
const vec4 k3 = equation(x + halfstep*k2);
const vec4 k4 = equation(x + integration step*k3);
return fl_6step*(k1 + 2.0*(k2 + k3) + k4);
}
Void main(void)
{
output += rungekutta4(output);
gl_FragColor = output;
}
```

[0076] The shader in Listing 2 can be executed on conventional video card. Using the controller **220** this code can be further optimized, however. Since the integration step does not change during the simulation, the step itself as well as the halfstep and ⅙ of the step can be computed once per simulation, and updated in all shaders by a shader update procedures **310**, **326** discussed above.

[0077] After all of the equations in the computational cycle are computed the main execution substream **403** on the controller **220** can switch **485** the reference pointers of the input and output portions of the texture memory bank **250**.

[0078] The two other substreams of execution on the controller **220** are waiting (blocks **430** and **455**, respectively) for this switch to begin their execution. The Data Input Substream **404** is controlling **440** the input of additional data from the CPU **120**. This is necessary in cases where the simulation is monitoring the changing input, for example input from a video camera or other recording device in the real time. This substream uploads new external input from the CPU **120** to the texture memory bank **250** so it can be used by the main computational substream **403** on the next computational step and waits for the next iteration **475**. The Data Output Substream **445** controls the output of simulation results to the CPU **120** if requested by the user. This substream uploads the results of the previous step to the main RAM **130** so that the CPU **120** can save them on disk **140** or show them on the results display **313** and waits for the next iteration **460**.

[0079] Since the Computational Substream **403** determines the timing of input **440** and output **445** data transfers, these data transfers are driven by the controller **220**. To further reduce the data transfer overhead (and disk **140** overhead also) the controller **220** initiates transfer only after selected computational steps. For example, if the experimental data that is simulated was recorded every 10 milliseconds (msec) and the simulation for better precision was computed every 1 msec, then only every tenth result has to be transferred to match the experimental frequency.

[0080] This solution stores two copies of output data, one in the expansion card texture memory bank **250** and another in the system RAM **130**. The copy in the system RAM **130** is accessed twice: for disk I/O and screen visualization **313**. An alternative solution would be to provide CPU **120** with a direct read access to the onboard texture memory bank **250** by mapping the memory of the hardware onto a global memory space. The alternative solution will double the communication through the local bus **190**. Since the goal discussed herein is reducing the information transfer through the local bus **190**, the former solution is favored.

[0081] The main substream **403** determines if this is the last iteration **487**. If it is the last iteration, the controller **220** waits for the all of the execution substreams to finish **490** and then returns the control to the CPU **120**, otherwise it begins the next computational cycle.

[0082] This repeats through all of the computational cycles of the simulation.

CONCLUSION

[0083] This GPU accelerator system offers the following potential advantages:

[0084] 1. Limited computations on the CPU **120**. The CPU **120** is only used for user input, sending information to the controller **220**, receiving output after each computational cycle (or less frequently as defined by the user), writing this output to disk **140**, and displaying this output on the monitor **170**. This frees the CPU **120** to execute other applications and allows the expansion card to run at its full capacity without being slowed down by extensive interactions with the CPU **120**.

[0085] 2. Minimizing data transfer between the expansion card **180** and the system bus **200**. All of the information needed to perform the simulations will be stored on the expansion card **180** and all simulations will take place on it. Furthermore, whatever data transfer remains necessary will take place in parallel with the computation, thus reducing the impact of this transfer on the performance.

[0086] 3. New way to execute GPU programs (shaders). Previously, the CPU **120** had full control over the order of shader's execution and was required to produce specific commands on every cycle to tell the GPU **240** which shader to use. With the invention disclosed herein, shaders will initially be stored on the shader memory bank **210** on the expansion card **180** and will be sent to the GPU **240** for execution by the general purpose controller **220** located on the expansion card.

[0087] 4. Multiple parallelisms. The GPU **240** is inherently parallel and is well suited to perform parallel computations. In parallel with the GPU **240** performing the next calculation, the controller **220** is uploading the data from the previous calculation into main memory **130**. Furthermore, the CPU **120** at the same time uses uploaded previous results to save them onto disk **140** and to display them on the screen through the system bus **200**.

[0088] 5. Reuse of existing and affordable technology. All hardware used in the invention and mentioned here-in are based on currently available and reliable components. Further advance of these components will provide straightforward improvements of the invention.

[0089] While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

Original

Classifications

IPC	CPC
G06T1/60	G06F9/5027
G06F9/50	G06F2209/509
G06T1/20	G06N3/063
	G06T1/20
	G06T1/60
	G06N20/00

Persons

Ultimate Owner

Original
NEURALA INC (/api/control?query=uo:("NEURALA%20INC")&autosearch=true)

Original Assignees

Original		Standardized		Normalized
Neurala Inc. Boston, Massachusetts, United States of America, US	(/api/control?query=pa:("Neurala%20Inc.")&autosearch=true)	NEURALA	(/api/control?query=pas:("NEURALA")&autosearch=true)	

Current Assignees

Original		Standardized		Normalized
NEURALA LLC, MASSACHUSETTS	(/api/control?query=pacu:("NEURALA%20LLC%2C%20MASSACHUSETTS")&autosearch=true)	NEURALA LLC, MASSACHUSETTS	(/api/control?query=pacus:("NEURALA%20LLC%2C%20MASSACHUSETTS")&autosearch=true)	
NEURALA, INC., MASSACHUSETTS	(/api/control?query=pacu:("NEURALA%2C%20INC.%2C%20MASSACHUSETTS")&autosearch=true)	NEURALA, INC., MASSACHUSETTS	(/api/control?query=pacus:("NEURALA%2C%20INC.%2C%20MASSACHUSETTS")&autosearch=true)	

Inventor(s)

Original
Massimiliano Versace (/api/control?query=in:("Massimiliano%20Versace")&autosearch=true) South Boston, Massachusetts, United States of America, US
Anatoli Gorchetchnikov (/api/control?query=in:("Anatoli%20Gorchetchnikov")&autosearch=true) Boston, Massachusetts, United States of America, US
Heather Marie Ames (/api/control?query=in:("Heather%20Marie%20Ames")&autosearch=true) South Boston, Massachusetts, United States of America, US
Fabrizio Santini (/api/control?query=in:("Fabrizio%20Santini")&autosearch=true) Jamaica Plain, Massachusetts, United States of America, US

Legal representative(s)

Original	Standardized	Normalized
Cooley LLP	(/api/control?query=ag:("Cooley%20 LLP")&autosearch=true)	

Legal information

Standardized Post issuance INPADOC

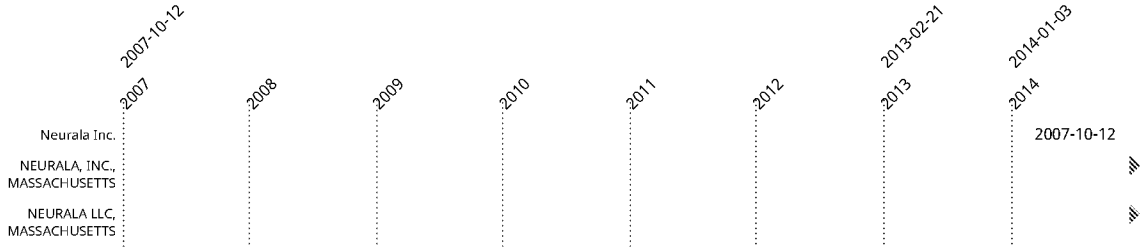
Legal status

Event	Date	Description
Granted	2015-11-17	GRANTED
Filed	2014-01-03	FILED

Designated states

Date	Event code	Description

Ownership



Payment status

Date	Status	Event code	Description
2019-05-17	Fee paid	M2551	PAYMENT OF MAINTENANCE FEE, 4TH YR, SMALL ENTITY.

Litigation/Opposition

Docket number	Docket description	Court	Date Filed

No CourtLink®

Pharmaceuticals

Product	Type	Active Ingredient	Applicant	Application No.	Application Type	Approval Date	Patent Expiry Date	Patent usage code	Exclusivity Code	Exclusivity Date	Dosage	Strength	Product Number	Route	RLD	P R
No pharmaceuticals data																

Citations

Display in a list (/api/control?citationsSearch=)

backwa...	US5388206A	By applicant	1995-02-07	Architecture and apparatus for image generation	UNIVERSITY OF NORTH CAROLINA	
backwa...	US20070279429A1	By applicant	2007-12-06	System and method for rendering graphics	GANZER LEONHARD	
backwa...	US20050166042A1	By applicant	2005-07-28	Secure video card methods and systems		
backwa...	US7861060B1	Cited by the examiner	2010-12-28	Parallel data processing systems and methods using cooperative thread arrays and thread identifier values to determine processing behavior		
backwa...	US20070052713A1	By applicant	2007-03-08	Systems and methods for storing and fetching texture data using bank interleaving		
backwa...	US8648867B2	Cited by the examiner	2014-02-11	Graphic processor based accelerator system and method		
forward	US10503976B2		2019-12-10	Methods and apparatus for autonomous robotic control	NEURALA	
forward	RU199766U1		2020-09-21	Circuit board PCIe expansion for continuous design (inferensa) neural networks	OBSHCHESTVO S OGRANICHENNOJ OTVETSTVENNOSTYU EVEREST	
forward	US10846873B2		2020-11-24	Methods and apparatus for autonomous robotic control	NEURALA	
forward	US9626566B2		2017-04-18	Methods and apparatus for autonomous robotic control	NEURALA BOSTON UNIVERSITY	
forward	US10974389B2		2021-04-13	Methods and apparatus for early sensory integration and robust acquisition of real world knowledge	NEURALA	
forward	US11070623B2		2021-07-20	Methods and apparatus for iterative nonspecific distributed runtime architecture and its application to cloud intelligence	NEURALA	
forward	US10083523B2		2018-09-25	Methods and apparatus for autonomous robotic control	NEURALA	
forward	US10300603B2		2019-05-28	Methods and apparatus for early sensory integration and robust acquisition of real world knowledge	NEURALA	

forward	US10469588B2	2019-11-05	Methods and apparatus for iterative nonspecific distributed runtime architecture and its application to cloud intelligence	NEURALA	

Similar documents

Display in a list (/api/control?similarSearch=_)

The similarity check is done by matching this document to all documents in the database. Only the title and abstract text are matched, resulting in a score. The 10 highest-scoring documents are displayed here.

All

Graphic processor based accelerator system and method

Publication number USRE048438E
Publication date 2021-02-16
Application date 2017-11-09

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

Graphic Processor Based Accelerator System and Method

Publication number US20080117220A1
Publication date 2008-05-22
Application date 2007-09-24

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPU), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the computer's central processing unit (CPU) is freed from this function and is dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

Graphic processor based accelerator system and method

Publication number US8648867B2
Publication date 2014-02-11
Application date 2007-09-24

An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPU), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the computer's central processing unit (CPU) is freed from this function and is dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

SYSTEM AND METHOD FOR MENU-DRIVEN VOICE CONTROL OF CHARACTERS IN A GAME ENVIRONMENT

Publication number KR1020020088058A
Publication date 2002-11-25
Application date 2002-05-14

PURPOSE: A menu type voice control system and a method for characters in a game environment are provided to implement menu-driven voice control of characters in a game environment. CONSTITUTION: A system(100) includes a main memory(110), a central processing unit(CPU, 112), vector processing units(VU0 and VU1), a graphics processing unit(GPU, 114), an input/output processor(IOP, 116), an IOP memory(118), a controller interface(120), a memory card(122), a Universal Serial Bus(USB) interface(124), and an IEEE 1394 interface(126). The system(100) also includes an operating system read-only memory(OS ROM, 128), a sound processing unit(SPU,

132), an optical disc control unit(134), and a hard disc drive(HDD, 136), which are connected via a bus(146) to IOP(116). The system(100) is preferably an electronic gaming console, however, the system(100) is also be implemented as a general-purpose computer, a set-top box, or a hand-held gaming device. The CPU(112) communicates with main memory(110) via a dedicated bus(142. VU1 113 and GPU 114) is also communicate via a dedicated bus(140). The CPU(112) executes programs stored in OS ROM(128) and main memory(110). The main memory(110) is contain prestored programs and is also contain programs transferred via IOP(116) from a CD-ROM, DVD-ROM, or other optical disc using optical disc control unit(134). IOP(116) controls data exchanges between CPU(112), VU0(111), VU1(113), GPU(114) and other devices of the system(100), such as controller interface(120). © KIPO 2003

NEURAL PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Publication number US20170024644A1
Publication date 2017-01-26
Application date 2016-07-24

A configurable spiking neural network based accelerator system is provided. The accelerator system may be executed on an expansion card which may be a printed circuit board. The system includes one or more application specific integrated circuits comprising at least one spiking neural processing unit and a programmable logic device mounted on the printed circuit board. The spiking neural processing unit includes digital neuron circuits and digital, dynamic synaptic circuits. The programmable logic device is compatible with a local system bus. The spiking neural processing units contain digital circuits comprises a Spiking Neural Network that handles all of the neural processing. The Spiking Neural Network requires no software programming, but can be configured to perform a specific task via the Signal Coupling device and software executing on the host computer. Configuration parameters include the connections between synapses and neurons, neuron types, neurotransmitter types, and neuromodulation sensitivities of specific neurons.

Neural processor based accelerator system and method

Publication number US11157800B2
Publication date 2021-10-26
Application date 2016-07-24

A configurable spiking neural network based accelerator system is provided. The accelerator system may be executed on an expansion card which may be a printed circuit board. The system includes one or more application specific integrated circuits comprising at least one spiking neural processing unit and a programmable logic device mounted on the printed circuit board. The spiking neural processing unit includes digital neuron circuits and digital, dynamic synaptic circuits. The programmable logic device is compatible with a local system bus. The spiking neural processing units contain digital circuits comprises a Spiking Neural Network that handles all of the neural processing. The Spiking Neural Network requires no software programming, but can be configured to perform a specific task via the Signal Coupling device and software executing on the host computer. Configuration parameters include the connections between synapses and neurons, neuron types, neurotransmitter types, and neuromodulation sensitivities of specific neurons.

METHOD AND SYSTEM FOR SEARCHING FOR PATTERNS IN DATA

Publication number WO2008090336A2
Publication date 2008-07-31
Application date 2008-01-23

Methods and systems for searching by computer for patterns in data are disclosed. These have particular, but not exclusive application to searching for target nucleotide sequences within a gene database. In the method can be performed by a computer that computer includes a central processing unit (CPU) that has one or more processing core, main memory accessible for read and write operations by the CPU, one or more graphics processing unit (GPU), and graphics memory accessible for read and write operations by the GPU. The method includes a step in which data to be processed as part of the pattern matching algorithm are transferred to the graphics memory, the GPU is operated to perform one or more processing step on the data. Following completion of the processing step, processed data are transferred from the graphics memory to the main memory. Algorithms that can be implemented using the invention include deterministic algorithms (e.g., Smith-Waterman) and non-deterministic algorithms (e.g., BLAST).

METHOD AND SYSTEM FOR SEARCHING FOR PATTERNS IN DATA

Publication number WO2008090336A3
Publication date 2008-11-27
Application date 2008-01-23

Methods and systems for searching by computer for patterns in data are disclosed. These have particular, but not exclusive application to searching for target nucleotide sequences within a gene database. In the method can be performed by a computer that computer includes a central processing unit (CPU) that has one or more processing core, main memory accessible for read and write operations by the CPU, one or more graphics processing unit (GPU), and graphics memory accessible for read and write operations by the GPU. The method includes a step in which data to be processed as part of the pattern matching algorithm are transferred to the graphics memory, the GPU is operated to perform one or more processing step on the data. Following completion of the processing step, processed data are transferred from the graphics memory to the main memory. Algorithms that can be implemented using the invention include deterministic algorithms (e.g., Smith-Waterman) and non-deterministic algorithms (e.g., BLAST).

METHOD AND SYSTEM FOR SEARCHING FOR PATTERNS IN DATA

Publication number	US20100138376A1
Publication date	2010-06-03
Application date	2008-01-23

Methods and systems for searching by computer for patterns in data are disclosed. These have particular, but not exclusive application to searching for target nucleotide sequences within a gene database. In the method can be performed by a computer that computer includes a central processing unit (CPU) that has one or more processing core, main memory accessible for read and write operations by the CPU, one or more graphics processing unit (GPU), and graphics memory accessible for read and write operations by the GPU. The method includes a step in which data to be processed as part of the pattern matching algorithm are transferred to the graphics memory, the GPU is operated to perform one or more processing step on the data. Following completion of the processing step, processed data are transferred from the graphics memory to the main memory. Algorithms that can be implemented using the invention include deterministic algorithms (e.g., Smith-Waterman) and non-deterministic algorithms (e.g., BLAST).

Method and system for searching for patterns in data

Publication number	GB914480D0
Publication date	2009-09-30
Application date	2008-01-23

Methods and systems for searching by computer for patterns in data are disclosed. These have particular, but not exclusive application to searching for target nucleotide sequences within a gene database. In the method can be performed by a computer that computer includes a central processing unit (CPU) that has one or more processing core, main memory accessible for read and write operations by the CPU, one or more graphics processing unit (GPU), and graphics memory accessible for read and write operations by the GPU. The method includes a step in which data to be processed as part of the pattern matching algorithm are transferred to the graphics memory, the GPU is operated to perform one or more processing step on the data. Following completion of the processing step, processed data are transferred from the graphics memory to the main memory. Algorithms that can be implemented using the invention include deterministic algorithms (e.g., Smith-Waterman) and non-deterministic algorithms (e.g., BLAST).

1
1

or: 9189828 or 9,189,828

Cases 0

Filters

Cases Clear

No documents found in Cases filtered by Cases.

Search Tree:

9189828 0 9,189,828 0

or 0

Try the following:

- Remove one or more filters: Cases
- Review your results in the other categories.
- Modify your search (edit or remove some search terms or add synonyms).
- Check for spelling errors.
- Use the options available from the Actions menu above to modify your search.

Copyright © 2022 LexisNexis.

LexisNexis

User Name: Renee Preston
Date and Time: Friday, February 18, 2022 10:21:00 AM EST
Job Number: 164650217

Documents (5)

1. *U.S. Patents Awarded to Inventors in Massachusetts (Nov. 20)*
   Client/Matter: -None-
   Search Terms: 9189828 or 9,189,828
   Search Type: Terms and Connectors
   Narrowed by:

Content Type	Narrowed by
News	-None-

2. *Neurala Assigned Patent*
   Client/Matter: -None-
   Search Terms: 9189828 or 9,189,828
   Search Type: Terms and Connectors
   Narrowed by:

Content Type	Narrowed by
News	-None-

3. *Head Line: US Patent granted to Neurala, Inc (Massachusetts) on November 17, 2015 titled as "Graphic processor based accelerator system and method"*
   Client/Matter: -None-
   Search Terms: 9189828 or 9,189,828
   Search Type: Terms and Connectors
   Narrowed by:

Content Type	Narrowed by
News	-None-

4. *United States Patent for Graphic Processor Based Accelerator System and Method Issued to Neurala Inc*
   Client/Matter: -None-
   Search Terms: 9189828 or 9,189,828
   Search Type: Terms and Connectors
   Narrowed by:

Content Type	Narrowed by
News	-None-

5. *United States Patent for Graphic Processor Based Accelerator System and Method Issued to Neurala Inc*
   Client/Matter: -None-
   Search Terms: 9189828 or 9,189,828

Search Type: Terms and Connectors

Narrowed by:

Content Type	Narrowed by
News	-None-

LexisNexis | About LexisNexis | Privacy Policy | Terms & Conditions | Copyright © 2022 LexisNexis

U.S. Patents Awarded to Inventors in Massachusetts (Nov. 20)

Targeted News Service

November 20, 2015 Friday 2:03 PM EST

Copyright 2015 Targeted News Service LLC All Rights Reserved

Length: 3014 words

Byline: Targeted News Service Targeted News Service

Dateline: Alexandria, VA.

Body

ALEXANDRIA, Va., Nov. 20 -- The following federal patents were awarded to inventors in Massachusetts.

***

Allegro MicroSystems Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Allegro MicroSystems, Worcester, Massachusetts, has been assigned a patent (9,190,606) developed by seven co-inventors for "packaging for an electronic device." The co-inventors are Shixi Louis Liu, Worcester, Massachusetts, Harianto Wong, Southborough, Massachusetts, Paul David, Bow, New Hampshire, John B. Sauber, Millbury, Massachusetts, Shaun D. Milano, Dunbarton, New Hampshire, Raguvir Kanda, North Attleboro, Massachusetts, and Bruce Hemenway, Milford, Massachusetts.

The patent application was filed on March 15, 2013 (13/834,617). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,190,606.PN.&OS=PN/9,190,606&RS=PN/9,190,606

Written by Kusum Sangma; edited by Jaya Anand.

***

General Hospital, Brigham & Women's Hospital Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- General Hospital, Boston, and Brigham & Women's Hospital, Boston, have been assigned a patent (9,187,421) developed by six co-inventors for "etomidate analogues that do not inhibit adrenocortical steroid synthesis." The co-inventors are Douglas E. Raines, Wayland, Massachusetts, Joseph F. Cotton, Grafton, Massachusetts, Stuart A. Forman, Arlington, Massachusetts, Keith W. Miller, Lincoln, Massachusetts, Syed S. Husain, Newton, Massachusetts, and Gregory D. Cuny, Houston.

Renee Preston

The patent application was filed on May 19, 2014 (14/281,149). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,421.PN.&OS=PN/9,187,421&RS=PN/9,187,421

Written by Amal Ahmed; edited by Jaya Anand.

***

General Hospital Assigned Patent for Apparatus for Applying Plurality of Electro-magnetic Radiations to Sample

ALEXANDRIA, Va., Nov. 20 -- General Hospital, Boston, has been assigned a patent (9,186,067) developed by four co-inventors for an "apparatus for applying a plurality of electro-magnetic radiations to a sample." The co-inventors are Guillermo J. Tearney, Cambridge, Massachusetts, Milen Shishkov, Watertown, Massachusetts, Brett Eugene Bouma, Quincy, Massachusetts, and Benjamin J. Vakoc, Cambridge, Massachusetts.

The patent application was filed on May 24, 2013 (13/901,921). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,067.PN.&OS=PN/9,186,067&RS=PN/9,186,067

Written by Amal Ahmed; edited by Jaya Anand.

***

Owens Corning Intellectual Capital Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Owens Corning Intellectual Capital, Toledo, Ohio, has been assigned a patent (9,187,608) developed by seven co-inventors for a "polystyrene foam containing a modifier-free nanoclay and having improved fire protection performance." The co-inventors are Roland R. Loh, Stow, Ohio, Mark E. Polasky, Mogadore, Ohio, Yadollah Delaviz, Lewis Center, Ohio, L. James Lee, Columbus, Ohio, Xia Cao, Arlington, Massachusetts, Jiong Shen, Columbus, Ohio, and Bharat Patel, Dublin, Ohio.

The patent application was filed on Sept. 8, 2005 (11/221,522). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,608.PN.&OS=PN/9,187,608&RS=PN/9,187,608

Written by Sudarshan Harpal; edited by Jaya Anand.

***

University of Massachusetts Assigned Patent

U.S. Patents Awarded to Inventors in Massachusetts (Nov. 20)

ALEXANDRIA, Va., Nov. 20 -- The University of Massachusetts, Boston, has been assigned a patent (9,189,202) developed by two co-inventors for "generate random numbers using metastability resolution time." The co-inventors are Wayne P. Burleson, Shutesbury, Massachusetts, and Vikram Belur Suresh, Amherst, Massachusetts.

The patent application was filed on Dec. 23, 2013 (14/139,020). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,189,202.PN.&OS=PN/9,189,202&RS=PN/9,189,202

Written by Kusum Sangma; edited by Jaya Anand.

***

Bullhorn Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Bullhorn, Boston, has been assigned a patent (9,189,770) developed by four co-inventors for the "automatic tracking of contact interactions." The co-inventors are Geoffrey D. Greene, Dover, Massachusetts, Arthur L.P. Papas, Weston, Massachusetts, Richard L. Leeds, III, Natick, Massachusetts, and Christian M. Baxter, Norwell, Massachusetts.

The patent application was filed on Sept. 16, 2010 (12/883,229). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,189,770.PN.&OS=PN/9,189,770&RS=PN/9,189,770

Written by Kusum Sangma; edited by Jaya Anand.

***

Children's Medical Center Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Children's Medical Center, Boston, has been assigned a patent (9,186,393) developed by two co-inventors for "methods and compositions for reducing blood glucose." The co-inventors are Umut Ozcan, Jamaica Plain, Massachusetts, and Jaemin Lee, Brookline, Massachusetts.

The patent application was filed on Aug. 30, 2012 (14/342,432). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,393.PN.&OS=PN/9,186,393&RS=PN/9,186,393

Written by Amal Ahmed; edited by Jaya Anand.

***

U.S. Patents Awarded to Inventors in Massachusetts (Nov. 20)

T.Q. Delta Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- T.Q. Delta, Austin, Texas, has been assigned a patent (9,191,039) developed by two co-inventors for "randomization using an XOR scrambler in multicarrier communications." The co-inventors are Marcos C. Tzannes, Alamo, California, and Amon Friedmann, Marlborough, Massachusetts.

The patent application was filed on June 19, 2014 (14/308,934). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=91,91,039.PN.&OS=PN/91,91,039&RS=PN/91,91,039

Written by Deviprasad Jena; edited by Jaya Anand.

***

Amazon Technologies Assigned Patent for Named Entity Recognition with Personalized Models

ALEXANDRIA, Va., Nov. 20 -- Amazon Technologies, Seattle, has been assigned a patent (9,190,055) developed by three co-inventors for "named entity recognition with personalized models." The co-inventors are Imre Attila Kiss, Arlington, Massachusetts, Lambert Mathias, Arlington, Massachusetts, and Jeffrey Penrod Adams, Tyngsborough, Massachusetts.

The patent application was filed on March 14, 2013 (13/828,759). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,190,055.PN.&OS=PN/9,190,055&RS=PN/9,190,055

Written by Amal Ahmed; edited by Jaya Anand.

***

Amazon Technologies Assigned Patent for Speech Model Retrieval in Distributed Speech Recognition Systems

ALEXANDRIA, Va., Nov. 20 -- Amazon Technologies, Seattle, has been assigned a patent (9,190,057) developed by three co-inventors for "speech model retrieval in distributed speech recognition systems." The co-inventors are Bjorn Hoffmeister, Seattle, Hugh Evan Secker-Walker, Newburyport, Massachusetts, and Jeffrey Cornelius O'Neill, Somerville, Massachusetts.

The patent application was filed on Dec. 12, 2012 (13/712,891). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,190,057.PN.&OS=PN/9,190,057&RS=PN/9,190,057

Written by Amal Ahmed; edited by Jaya Anand.

Renee Preston

***

General Hospital Assigned Patent for Methods of Treating Vascular Lesions

ALEXANDRIA, Va., Nov. 20 -- General Hospital, Boston, has been assigned a patent (9,186,336) developed by Steven M. Zeitels, Newton, Massachusetts, for "methods of treating vascular lesions."

The patent application was filed on Feb. 5, 2010 (13/147,844). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,336.PN.&OS=PN/9,186,336&RS=PN/9,186,336

Written by Amal Ahmed; edited by Jaya Anand.

***

Cooper Technologies Assigned Patent for Bridgeless Boost Power Factor Correction Circuit for Constant Current Input

ALEXANDRIA, Va., Nov. 20 -- Cooper Technologies, Houston, has been assigned a patent (9,190,901) developed by Traver Gumaer, Easthampton, Massachusetts, for a "bridgeless boost power factor correction circuit for constant current input."

The patent application was filed on May 3, 2013 (13/887,205). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=91,90,901.PN.&OS=PN/91,90,901&RS=PN/91,90,901

Written by Deviprasad Jena; edited by Jaya Anand.

***

General Hospital Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- General Hospital, Boston, has been assigned a patent (9,186,066) developed by four co-inventors for an "apparatus for applying a plurality of electro-magnetic radiations to a sample." The co-inventors are Guillermo J. Tearney, Cambridge, Massachusetts, Milen Shishkov, Watertown, Massachusetts, Brett Eugene Bouma, Quincy, Massachusetts, and Benjamin J. Vakoc, Cambridge, Massachusetts.

The patent application was filed on Feb. 1, 2007 (11/670,027). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,066.PN.&OS=PN/9,186,066&RS=PN/9,186,066

U.S. Patents Awarded to Inventors in Massachusetts (Nov. 20)

Written by Amal Ahmed; edited by Jaya Anand.

***

Brigham & Women's Hospital Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Brigham & Women's Hospital, Boston, has been assigned a patent (9,187,517) developed by Richard Lee, Weston, Massachusetts, for "methods of promoting cardiac repair using growth factors fused to heparin binding sequences."

The patent application was filed on Nov. 7, 2007 (11/979,708). The full-text of the patent can be found at *http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,517.PN.&OS=PN/9,187,517&RS=PN/9,187,517*

Written by Amal Ahmed; edited by Jaya Anand.

***

Neurala Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Neurala, Boston, has been assigned a patent (*9,189,828*) developed by four co-inventors for "graphic processor based accelerator system and method." The co-inventors are Anatoli Gorchetchnikov, Boston, Heather Marie Ames, South Boston, Massachusetts, Massimiliano Versace, South Boston, Massachusetts, and Fabrizio Santini, Jamaica Plain, Massachusetts.

The patent application was filed on Jan. 3, 2014 (14/147,015). The full-text of the patent can be found at *http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,189,828.PN.&OS=PN/9,189,828&RS=PN/9,189,828*

Written by Kusum Sangma; edited by Jaya Anand.

***

Johns Hopkins University Assigned Patent for Compositions Having Antiangiogenic Activity and Uses

ALEXANDRIA, Va., Nov. 20 -- Johns Hopkins University, Baltimore, has been assigned a patent (9,187,539) developed by two co-inventors for "compositions having antiangiogenic activity and uses thereof." The co-inventors are Aleksander S. Popel, Lutherville, Maryland, and Emmanouil D. Karagiannis, Cambridge, Massachusetts.

The patent application was filed on Aug. 23, 2013 (13/975,168). The full-text of the patent can be found at *http://patft.uspto.gov/netacgi/nph-*

Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,539.PN.&OS=PN/9,187,539&RS=PN/9,187,539

Written by Amal Ahmed; edited by Jaya Anand.

***

Saint-Gobain Abrasives Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Saint-Gobain Abrasives, Worcester, Massachusetts, and Saint-Gobain Abrasifs, Conflans-Sainte-Honorine, France, have been assigned a patent (9,186,816) developed by four co-inventors for an "abrasive article and method of forming." The co-inventors are Yinggang Tian, Shrewsbury, Massachusetts, Arup K. Khaund, Northborough, Massachusetts, Krishnamoorthy Subramanian, Lexington, Massachusetts, and John Pearlman, Berlin, Massachusetts.

The patent application was filed on March 7, 2012 (13/414,561). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,816.PN.&OS=PN/9,186,816&RS=PN/9,186,816

Written by Amal Ahmed; edited by Jaya Anand.

***

Northeastern University Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Northeastern University, Boston, has been assigned a patent (9,187,329) developed by two co-inventors for a microparticle organization. The co-inventors are Jeffrey W. Ruberti, Lexington, Massachusetts, and Nima Saeidi, Allston, Massachusetts.

The patent application was filed on April 21, 2010 (13/265,729). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,329.PN.&OS=PN/9,187,329&RS=PN/9,187,329

Written by Amal Ahmed; edited by Jaya Anand.

***

Dana-Farber Cancer Institute, Colorado State University Research Foundation, University of Notre Dame du Lac Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Dana-Farber Cancer Institute, Boston, Colorado State University Research Foundation, Fort Collins, Colorado, and the University of Notre Dame du Lac, Notre Dame, Indiana, have been

assigned a patent (9,186,402) developed by five co-inventors for a "method for preparing largazole analogs and uses thereof." The co-inventors are Robert M. Williams, Fort Collins, Colorado, James E. Bradner, Cambridge, Massachusetts, Albert Bowers, Boston, Tenaya Newkirk, Fort Collins, Colorado, and Olaf G. Wiest, Notre Dame, Indiana.

The patent application was filed on July 17, 2013 (13/944,446). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,402.PN.&OS=PN/9,186,402&RS=PN/9,186,402

Written by Amal Ahmed; edited by Jaya Anand.

***

Ethicon Endo-Surgery Assigned Patent for Tissue Stapler Anvil Feature to Prevent Premature Jaw Opening

ALEXANDRIA, Va., Nov. 20 -- Ethicon Endo-Surgery, Cincinnati, has been assigned a patent (9,186,148) developed by 20 co-inventors for "tissue stapler anvil feature to prevent premature jaw opening." The co-inventors are Kevin D. Felder, Cincinnati, John F. Cummings, Madeira, Ohio, Joseph P. Schowalter, South Lebanon, Ohio, Patrick J. Swindon, Cincinnati, Johnny H. Alexander III, West Chester, Ohio, Patrick A. Weizman, Liberty Township, Ohio, Cory G. Kimball, Cincinnati, Edward G. Chekan, Cincinnati, Joseph E. Young, Loveland, Ohio, Christopher C. Miller, Loveland, Ohio, Barry T. Jamison, Fairfield, Ohio, John V. Hunt, Cincinnati, Kent P. Baker, Liberty Township, Ohio, Cortney E. Henderson, Loveland, Ohio, Chester O. Baxter III, Loveland, Ohio, Jerome R. Morgan, Cincinnati, Adam R. Dunki-Jacobs, Cincinnati, Venkataramanan Mandakolathur Vasudevan, Cincinnati, Carl J. Shurtleff, Mason, Ohio, and Julia F. Serber, Brookline, Massachusetts.

The patent application was filed on Jan. 5, 2012 (13/344,061). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,148.PN.&OS=PN/9,186,148&RS=PN/9,186,148

Written by Sudarshan Harpal; edited by Jaya Anand.

***

Northeastern University Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Northeastern University, Boston, has been assigned a patent (9,186,653) developed by three co-inventors for a "highly stable platinum alloy catalyst for methanol electrooxidation." The co-inventors are Sanjeev Mukerjee, Mansfield, Massachusetts, Qinggang He, Berkeley, California, and Nagappan Ramaswamy, Boston.

The patent application was filed on June 17, 2011 (13/704,765). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,186,653.PN.&OS=PN/9,186,653&RS=PN/9,186,653

Written by Amal Ahmed; edited by Jaya Anand.

***

Johns Hopkins University Assigned Patent for Peptide Modulators of Angiogenesis and Use

ALEXANDRIA, Va., Nov. 20 -- Johns Hopkins University, Baltimore, has been assigned a patent (9,187,544) developed by two co-inventors for "peptide modulators of angiogenesis and use thereof." The co-inventors are Aleksander S. Popel, Lutherville, Maryland, and Emmanouil D. Karagiannis, Cambridge, Massachusetts.

The patent application was filed on Aug. 8, 2013 (13/962,383). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,187,544.PN.&OS=PN/9,187,544&RS=PN/9,187,544

Written by Amal Ahmed; edited by Jaya Anand.

***

Smith & Wesson Corp. Assigned Patent

ALEXANDRIA, Va., Nov. 20 -- Smith & Wesson Corp., Springfield, Massachusetts, has been assigned a patent (9,188,399) developed by two co-inventors for receiver catch. The co-inventors are David S. Findlay, Athol, Massachusetts, and David Jonathan Findlay, Athol, Massachusetts.

The patent application was filed on Oct. 31, 2014 (14/529,554). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,188,399.PN.&OS=PN/9,188,399&RS=PN/9,188,399

Written by Kusum Sangma; edited by Jaya Anand.

Myron Struck, editor, Targeted News Service, Springfield, Va., 703/304-1897; editor@targetednews.com; http://www.targetednews.com

-1235894

Load-Date: November 20, 2015

End of Document

Neurala Assigned Patent

Targeted News Service

November 20, 2015 Friday 2:06 AM EST

Copyright 2015 Targeted News Service LLC All Rights Reserved

Length: 151 words

Byline: Targeted News Service

Dateline: Alexandria, Va.

Body

ALEXANDRIA, Va., Nov. 20 -- Neurala, Boston, has been assigned a patent (9,189,828) developed by four co-inventors for "graphic processor based accelerator system and method." The co-inventors are Anatoli Gorchetchnikov, Boston, Heather Marie Ames, South Boston, Massachusetts, Massimiliano Versace, South Boston, Massachusetts, and Fabrizio Santini, Jamaica Plain, Massachusetts.

The patent application was filed on Jan. 3, 2014 (14/147,015). The full-text of the patent can be found at http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO1&Sect2=HITOFF&d=PALL&p=1&u=%2Fnetahtml%2FPTO%2Fsrchnum.htm&r=1&f=G&l=50&s1=9,189,828.PN.&OS=PN/9,189,828&RS=PN/9,189,828

Written by Kusum Sangma; edited by Jaya Anand.

For more information about Targeted News Service federal patent awards please contact: Myron Struck, Editor, Direct: 703/866-4708, Cell: 703/304-1897, Myron@targetednews.com

KS1120JA1120-1141667 93JAnand

Load-Date: November 20, 2015

End of Document

Head Line: US Patent granted to Neurala, Inc (Massachusetts) on November 17, 2015 titled as "Graphic processor based accelerator system and method"

Plus Patent News

November 17, 2015 Tuesday

Copyright 2015 Plus Media Solutions Private Limited All Rights Reserved

Plus Media Solutions

Length: 252 words

Dateline: Lahore

Body

ALEXANDRIA, Va: United States Patent and Trademark Office has granted patent no. *9,189,828* on November 17, 2015, to Neurala, Inc (Massachusetts) titled as "Graphic processor based accelerator system and method"

Inventors: Gorchetchnikov; Anatoli (Boston, MA), Ames; Heather Marie (South Boston, MA), Versace; Massimiliano (South Boston, MA), Santini; Fabrizio (Jamaica Plain, MA)

Assignee: Neurala, Inc. (Boston, MA) (Massachusetts)

According to the abstract released by the U.S. Patent & Trademark Office: "An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation."

The patent was filed on January 3, 2014 Application No. 14/147,015

Renee Preston

Head Line: US Patent granted to Neurala, Inc (Massachusetts) on November 17, 2015 titled as "Graphic processor based accelerator system and method"

Load-Date: November 18, 2015

End of Document

United States Patent for Graphic Processor Based Accelerator System and Method Issued to Neurala Inc

Global IP News. Information Technology Patent News

November 17, 2015 Tuesday

Copyright 2015 ProQuest Information and Learning
All Rights Reserved
Copyright 2015 Globalipnews.com

Length: 316 words

Dateline: New Delhi

Body

FULL TEXT

Publication Name: Information Technology Patent News**Patent Application Number:** 14/147,015**Patent Publication Number:** 9,189,828**International Patent Classification Codes:** G06T 1/60 (20130101), G06F 9/5027 (20130101), G06T 1/20 (20130101), G06F 2209/509 (20130101)**Patent Status:** Granted

Alexandria, Nov. 17 -- United States Patent for graphic processor based accelerator system and method has been issued to Neurala Inc. This invention was developed by Gorchetchnikov Anatoli, Ames Heather Marie, Versace Massimiliano and Santini Fabrizio. The patent application number is 14/147,015. The International Patent Classification codes are G06T 1/60 (20060101), G06F 9/50 (20060101) and G06T 1/20 (20060101). Cooperative Patent Classification codes are G06T 1/60 (20130101), G06F 9/5027 (20130101), G06T 1/20 (20130101) and G06F 2209/509 (20130101).

The abstract released by U.S. Patent and Trademark Office states, "An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation."

Copyright© 2015, Globalipnews.com

Renee Preston

Load-Date: August 25, 2016

End of Document

United States Patent for Graphic Processor Based Accelerator System and Method Issued to Neurala Inc

Global IP News. Information Technology Patent News

November 17, 2015 Tuesday

Copyright 2015 ProQuest Information and Learning
All Rights Reserved
Copyright 2015 Copyright©, Globalipnews.com

Length: 314 words

Body

Publication Name: Information Technology Patent News Patent Application Number: 14/147,015 Patent Publication Number: *9,189,828* International Patent Classification Codes: G06T 1/60 (20130101), G06F 9/5027 (20130101), G06T 1/20 (20130101), G06F 2209/509 (20130101) Patent Status: Granted

Alexandria, Nov. 17 -- United States Patent for graphic processor based accelerator system and method has been issued to Neurala Inc. This invention was developed by Gorchetchnikov Anatoli, Ames Heather Marie, Versace Massimiliano and Santini Fabrizio. The patent application number is 14/147,015. The International Patent Classification codes are G06T 1/60 (20060101), G06F 9/50 (20060101) and G06T 1/20 (20060101). Cooperative Patent Classification codes are G06T 1/60 (20130101), G06F 9/5027 (20130101), G06T 1/20 (20130101) and G06F 2209/509 (20130101).

The abstract released by U.S. Patent and Trademark Office states, "An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPUs), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards. The controller handles most of the primitive operations to set up and control GPU computation. Thus, the computer's central processing unit (CPU) can be dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation."

Copyright© 2015, Globalipnews.com

Load-Date: November 18, 2015

End of Document

Results for: 9189828 or 9,189,828 | Actions Edit Search Search in same court

Dockets	0
Briefs, Pleadings and Motions	0

Narrow By

Patent

Clear

Filter Results

Dockets (0)

No documents found in **Dockets** filtered by **Patent.**

Try the following:

- Remove one or more filters: **Patent**
- Modify your search (edit or remove some search terms or add synonyms).
- Check for spelling errors.
- Use the options available from the **Actions** menu above to modify your search.
- Note: Some content may not be visible based on the restrictions of your subscription.

Copyright © 2022 LexisNexis.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

149890 7590 03/07/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
03/07/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@smithbaluch.com
eofficeaction@appcoll.com
smith@smithbaluch.com

Office Action Summary	Application No. 17/136,343	Applicant(s) Gorchetchnikov et al.	
	Examiner WILLIAM H WOOD	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12/29/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-70 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-70 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 12/29/2020 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 03/29/2021; 03/29/2021; 03/29/2021.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

For reissue applications filed before September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are "pre-AIA" provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the current provisions.

Claims 1-70 are currently pending in the application. Claims 1-57 are patented claims from patent US RE48,438 E and claims 58-70 are newly added claims.

Reissue

Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. US 9,189,828 B2 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Applicant is notified that any subsequent amendment to the specification and/or claims must comply with 37 CFR 1.173(b).

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 03/29/2021, 03/29/2021, and 03/29/2021 are considered by the examiner in accordance with 37 CFR 1.97, 37 CFR 1.98, MPEP 609, and MPEP 1406, to the fullest extent of the items presented including any concise explanation. Documents not meeting a particular criteria are lined through and not considered.

Objections

The reissue oath/declaration filed with this application is defective and objected to because it fails: [1)] to identify, when not supplied in an Application Data Sheet (ADS), the mailing address where the inventor customarily receives mail (37 CFR 1.76; 37 CFR 1.63(b)), in this case the mailing address of inventor Santini Fabrizio is not identified or supplied by either the declaration or the ADS.

Claim Interpretation

The following is a quotation of 35 U.S.C. 112(f):

> (f) Element in Claim for a Combination. – An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

The following is a quotation of pre-AIA 35 U.S.C. 112, sixth paragraph:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

The claims in this application are given their broadest reasonable interpretation using the plain meaning of the claim language in light of the specification as it would be understood by one of ordinary skill in the art. The broadest reasonable interpretation of a claim element (also commonly referred to as

a claim limitation) is limited by the description in the specification when 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph, is invoked.

As explained in MPEP § 2181, subsection I, claim limitations that meet the following three-prong test will be interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph:

(A) the claim limitation uses the term "means" or "step" or a term used as a substitute for "means" that is a generic placeholder (also called a nonce term or a non-structural term having no specific structural meaning) for performing the claimed function;

(B) the term "means" or "step" or the generic placeholder is modified by functional language, typically, but not always linked by the transition word "for" (e.g., "means for") or another linking word or phrase, such as "configured to" or "so that"; and

(C) the term "means" or "step" or the generic placeholder is not modified by sufficient structure, material, or acts for performing the claimed function.

Use of the word "means" (or "step") in a claim with functional language creates a rebuttable presumption that the claim limitation is to be treated in accordance with 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph. The presumption that the claim limitation is interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph, is rebutted when the claim limitation recites sufficient structure, material, or acts to entirely perform the recited function.

Absence of the word "means" (or "step") in a claim creates a rebuttable presumption that the claim limitation is not to be treated in accordance with 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph. The presumption that the claim limitation is not interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph, is rebutted when the claim limitation recites function without reciting sufficient structure, material or acts to entirely perform the recited function.

Claim limitations in this application that use the word "means" (or "step") are being interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph, except as otherwise indicated in an

Office action. Conversely, claim limitations in this application that do not use the word "means" (or "step") are not being interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph, except as otherwise indicated in an Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-57 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. Claims 1-57 are indefinite because the invention of the claims is not particularly pointed out and distinctly claimed. Claims 1-57 present one coverage in reissue application 15/808,201 and another in the present continuation reissue application. This is inconsistent. See MPEP 1451 (discussion under section I. for Divisional Applications is applicable to Continuation Applications of section II.; also note the example, "The physical cancellation of claim 1 in the second divisional reissue application will not prejudice applicant's rights in the amended version of claim 1 because those rights are retained via the first reissue application. Claim 1 continues to exist in the first reissue application, and both the first and second reissue applications taken together make up the totality of the correction of the original patent").

Claims 58-69 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. Independent claim 58 recites, "shifting priority from the user interaction stream to the computational stream …", and then "shifting the priority from the computational stream to the user interaction stream …", which are unclear. It is not clear to what or perhaps who 'priority' refers. From the specification *('828: column 7, lines 45-53)* it seems likely that 'priority' somehow refers to priority of the system/method over what processing entity controls data exchange. However, this concept is not fully or clearly developed by the claim language. The claim language is indefinite. Further, the claim language of 'shifting' is unclear as to who or what is shifting. Also, the term 'priority' is broad, and considering the CPU and GPU (processor) continue to execute respective tasks independently including communicating data to one another, it is difficult to determine the metes and bounds of 'priority' as it allows the non-priority entity to still control some data exchange.

Additionally, as currently written, the two "shifting priority" limitations merely describe the CPU taking priority for CPU tasks and the GPU (processor) taking priority for GPU tasks.

Rejections – 35 USC § 251

Claims 1-20 and the Declaration of 12/29/2020 are rejected under 35 U.S.C. 251 as the reissue application is not correcting an error in the original patent, because original claims 1-20 would be superseded by the reissuance of claims 1-20 in the other reissue application (15/808,201).

As currently presented, claims 58-70 are directed toward "overlooked aspects" (in particular the current claims relate to the interaction of a "user interaction stream" executed on a CPU and a "computational stream" executed on a processor) and are therefore not subject to further recapture analysis under 35 USC 251. Claims to overlooked aspects are not subject to recapture because the claims

are, by definition, unrelated to subject matter that was surrendered during the prosecution of the original application. In the decision of In re Youman, 679 F.3d 1335, 102 USPQ2d 1862 (Fed. Cir. 2012). See also MPEP 1412.01 II.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-57 is/are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-57 of prior U.S. Patent No. RE48,438. This is a statutory double patenting rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 58-62 and 64-67 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US 7,219,085 B2 *(herein **Buck**)* in view of US 7,477,256 B1 *(herein **Johnson**)* in further view of US 7,525,547 B1 *(herein **Diard**)*.

Claim 58	***Buck**, **Johnson**, and **Diard***
A method of executing computations representing an artificial neural network on a computer system comprising at least one central processing unit (CPU), a processing unit, a first memory partition, and a second memory partition, the method comprising:	*(Buck: column 21, lines 54-64)* *(Buck: figure 2, element 120, element 220)* *(Buck: figure 2, element 230; column 21, lines 46-49; column 15, lines 46-60, figure 9)*
executing, by the at least one CPU, a user interaction stream, the user interaction stream controlling transfer of inputs to the artificial neural network to the first memory partition and the second memory partition;	*(Buck: column 9, lines 35-36)* *(Buck: figures 2 and 5; column 10, lines 41-43; column 23, lines 13-20)*
executing, by the processing unit, a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network;	*(Buck: column 2, lines 24-28; column 8, lines 39-44)* *(Buck: figure 5, elements 220 and 545)* ***Johnson*** demonstrates, to the extent ***Buck*** does not explicitly state, that it was known at the time of invention to provide a controller operably coupled to a GPU so that "the computational stream controlling data exchange between the user interaction stream and the computational stream" *(Johnson: figure 4A, elements 410 and 442; and column 7, lines 33-55)*. It would have

	been obvious to one of ordinary skill in the art at the time of invention to implement accelerator and GPU of *Buck* with a controller for transferring data, and thus the computational stream of the processing unit controlling data exchange between the user interaction stream and the computation stream as suggested by *Johnson*'s teachings. This implementation would have been obvious because one of ordinary skill in the art would have found: the implementation of is a substitution and application of one known element and technique for another yielding a predictable result using an acceptable piece of prior art; and both are directed to graphics processing systems. To the extent *Buck* does not explicitly state exchanging data between the computational stream and the user interaction stream during execution of the computations, ***Diard*** demonstrates that it was known at the time of invention to transfer data between an accelerator memory and the main memory while the GPU is performing other operations/computations *(Diard: figure 1, transfer arrows; column 5, lines 1-3; column 6, lines 10-26; column 13, lines 4-25)*. Further, *Buck* demonstrates repeatedly performing the sequence of computations and periodically transferring data during those sequences of computations *(Buck: column 11, line 12 to column 12, line 26; and column 10, lines 33-35, GPU and*

	CPU compute at the same time). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the CPU and GPU system of *Buck* and controller of *Johnson* with data exchanged between the user interaction stream and the computational stream during execution of the computations as suggested by *Diard*'s teachings. This implementation would have been obvious because one of ordinary skill in the art would have found: the implementation of is a substitution and application of one known element and technique for another yielding a predictable result using an acceptable piece of prior art; and both *Buck* and *Diard* are directed to CPU and GPU processing.
shifting priority from the user interaction stream to the computational stream in response to starting execution of the computations representing the artificial neural network; and	This limitation reads upon a CPU executing a user interaction stream as described above.
shifting priority from the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network.	This limitation reads upon a processor (GPU/accelerator card/controller) executing a computational stream as described above.
Claim 59	***Buck**, **Johnson**, and **Diard***
The method of claim 58, wherein the user interaction stream controls data exchange between the user interaction stream and the	*(Buck: figure 2, element 130 separated by element 120)*

computational stream outside of execution of the computations representing the artificial neural network.	
Claim 60	***Buck, Johnson**, and **Diard***
The method of claim 58, wherein executing the user interaction stream comprises: controlling setting and editing of computational elements of the computations representing the artificial neural network.	*(Buck: figure 5, see at least 'P')*
Claim 61	***Buck, Johnson**, and **Diard***
The method of claim 58, wherein executing the user interaction stream comprises: controlling setting and editing of parameters of the computations representing the artificial neural network.	*(Buck: figure 5, see at least 'W', 'L', 'ERRORS')*
Claim 62	***Buck, Johnson**, and **Diard***
The method of claim 58, wherein executing the user interaction stream comprises: controlling setting and editing of parameters of the inputs to the artificial neural network.	*(Buck: figure 5, see at least 'X' and 'T')*
Claim 64	***Buck, Johnson**, and **Diard***
The method of claim 58, wherein executing the user interaction stream comprises: parsing elements to be used in the computations representing the artificial neural network.	*(Buck: column 2, lines 10-14; column 6, lines 10-16; column 10, lines 36-38; column 14, line 19 to column 15, line 18; programming and languages include parsing)*
Claim 65	***Buck, Johnson**, and **Diard***

The method of claim 64, wherein the processing unit comprises a graphics processing unit (GPU) and executing the user interaction stream further comprises: converting the elements into GPU programs.	*(Buck: column 2, lines 10-14; column 6, lines 10-16; column 10, lines 36-38; column 14, line 19 to column 15, line 18; programming and languages include converting)*
Claim 66	***Buck**, **Johnson**, and **Diard***
The method of claim 65, wherein executing the user interaction stream comprises: compiling the GPU programs.	*(Buck: column 2, lines 10-14; column 6, lines 10-16; column 10, lines 36-38; column 14, line 19 to column 15, line 18; DirectX including compilation)*
Claim 67	***Buck**, **Johnson**, and **Diard***
The method of claim 66, wherein executing the user interaction stream comprises: transferring the GPU programs to the second memory partition.	*(Buck: figure 5; and column 10, lines 36-41)*

Claims 63 and 68-70 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over US 7,219,085 B2 *(herein **Buck**)* in view of US 7,477,256 B1 *(herein **Johnson**)* in view of US 7,525,547 B1 *(herein **Diard**)* in further view of US 2006/0129506 A1 *(herein **Edelman**)*.

Claim 63	***Buck**, **Johnson**, **Diard**, and **Edelman***
The method of claim 58, wherein executing the user interaction stream comprises: specifying an output to be saved to disk and/or displayed on a screen.	*(Edelman: paragraphs 0056, and 0079)* *(Buck: figures 1-2; column 3, lines 46-51; column 9, lines 15-37)*

	To the extent, *Buck* does not explicitly state wherein executing the user interaction stream comprises: specifying an output to be saved to disk and/or displayed on a screen. *Edelman* demonstrates that it was known at the time of invention to save computations of an output stream to a disk *(Edelman: paragraphs 0056, and 0079)* and for the output stream to be related to an artificial or simulated neural system *(Edelman: paragraphs 0056, and 0079)*. Further, *Buck* demonstrates CPU controlled outputs and disk memory disk *(Buck: figures 1 and 2; column 3, lines 46-51; column 9, lines 15-37)*. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the artificial neural network of *Buck* with saving output to disk as suggested by *Edelman*'s teachings. This implementation would have been obvious because one of ordinary skill in the art would have found: the implementation of is a substitution and application of one known element and technique for another yielding a predictable result using an acceptable piece of prior art.
Claim 68	***Buck*, *Johnson*, *Diard*, *and* *Edelman***
The method of claim 58, further comprising: executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk.	*(Edelman: paragraphs 0056, and 0079)* *(Buck: figures 1-2; column 3, lines 46-51; column 9, lines 15-37)*

	To the extent *Buck* does not state executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk. *Edelman* demonstrates that it was known at the time of invention to save computations of an output stream to a disk *(Edelman: paragraphs 0056, and 0079)* and for the output stream to be related to an artificial or simulated neural system *(Edelman: paragraphs 0056, and 0079)*. Further, *Buck* demonstrates CPU controlled outputs and disk memory disk *(Buck: figures 1 and 2; column 3, lines 46-51; column 9, lines 15-37)*. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the artificial neural network of *Buck* with saving output to disk as suggested by *Edelman*'s teachings. This implementation would have been obvious because one of ordinary skill in the art would have found: the implementation of is a substitution and application of one known element and technique for another yielding a predictable result using an acceptable piece of prior art.
Claim 69	***Buck*, *Johnson*, *Diard*, *and* *Edelman***
The method of claim 58, further comprising: generating the inputs with a video camera during execution of the computations.	*(Buck: column 7, line 51 to column 8, line 2; column 9, lines 33-36; column 23, lines 26-30; generating/acquiring inputs during execution of the computations, real-time)*

	(Edelman: paragraphs 0006 and 0049) *Buck* does not explicitly state generating the inputs with a video camera. *Edelman* demonstrates that it was known at the time of invention to make use of video camera input sensors *(Edelman: paragraph 0049)* in an environment related to artificial neural networks *(Edelman: paragraph 0006)*. It would have been obvious to one of ordinary skill in the art at the time of invention to implement an input sensor of *Buck* with or as a video camera as suggested by *Edelman*'s teachings. This implementation would have been obvious because one of ordinary skill in the art would have found: the implementation of is a substitution and application of one known element and technique for another yielding a predictable result using an acceptable piece of prior art; and both references are directed to artificial neural networks.
Claim 70	***Buck, Johnson, Diard,*** *and* ***Edelman***
The limitations of claim 70 correspond to the limitations of claims 58-69.	The limitations of claim 70 are rejected in a corresponding manner to claims 58-69.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)272-3736 and fax number is (571)273-3736. The examiner can normally be reached on Monday-Friday 7:30am-4:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Kosowski can be reached on (571)272-3744. The Central Reexamination Unit's (CRU) fax number is (571)273-9900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see https://ppair-my.uspto.gov/pair/PrivatePair. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William H. Wood/
Primary Examiner, CRU 3992

Conferees:

/RSD/

/ALEXANDER J KOSOWSKI/
Supervisory Patent Examiner, Art Unit 3992

Notice of References Cited	Application/Control No. 17/136,343	Applicant(s)/Patent Under Reexamination Gorchetchnikov et al.	
	Examiner WILLIAM H WOOD	Art Unit 3992	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20060129506-A1	06-2006	Edelman; Gerald M.	G05D1/0088	706/12
*	B	US-7219085-B2	05-2007	Buck; Ian Andrew	G06V10/955	706/12
*	C	US-7477256-B1	01-2009	Johnson; Philip B.	G06F3/14	345/506
*	D	US-7525547-B1	04-2009	Diard; Franck R.	G06T1/20	345/522
*	E	US-RE48438-E	02-2021	Gorchetchnikov; Anatoli	G06F9/5027	1/1
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/01/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								
	24	✓								
	25	✓								
	26	✓								
	27	✓								
	28	✓								
	29	✓								
	30	✓								
	31	✓								
	32	✓								
	33	✓								
	34	✓								
	35	✓								
	36	✓								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CLAIM		DATE								
Final	Original	03/01/2022								
	43	✓								
	44	✓								
	45	✓								
	46	✓								
	47	✓								
	48	✓								
	49	✓								
	50	✓								
	51	✓								
	52	✓								
	53	✓								
	54	✓								
	55	✓								
	56	✓								
	57	✓								
	58	✓								
	59	✓								
	60	✓								
	61	✓								
	62	✓								
	63	✓								
	64	✓								
	65	✓								
	66	✓								
	67	✓								
	68	✓								
	69	✓								
	70	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 9/5027; 2209/509	03/01/2022	/WHW/
G06T 1/20; 1/60	03/01/2022	/WHW/
G06N 3/00; 3/02; 3/04; 3/06; 3/063; 3/08; 3/10; 5/00; 7/00; 7/02; 7/04 ; 7/046; 7/06; 20/00	03/01/2022	/WHW/

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Prosecution History Review	03/01/2022	/WHW/
NPL Review	03/01/2022	/WHW/
IDS Review	03/01/2022	/WHW/
Litigation Search	03/01/2022	/WHW/
PE2E Search	03/01/2022	/WHW/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	3	("9189828").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/10 09:44 AM
L2	1	("RE48438").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/10 09:49 AM
L3	4	L1 OR L2	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/10 09:50 AM
L4	6	("8648867" OR "9189828" OR "RE48438").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/02/11 01:34 PM

NVIDIA Ex1002
Page 229 of 392

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L5	28251	((graphic ADJ processing ADJ unit) OR GPU) WITH (neuron OR neural)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/14 02:50 PM
L6	63	((graphic ADJ processing ADJ unit) OR GPU) WITH (neuron OR neural) WITH offload$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/14 03:58 PM
L7	0	L6 AND (user ADJ interaction ADJ stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2022/02/16 09:30 AM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L8	0	L6 AND (computational ADJ stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:30 AM
L9	34	L6 AND stream	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:30 AM
L10	1	L5 AND (user ADJ interaction ADJ stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:33 AM
L11	2	L5 AND (computational ADJ stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2022/02/16 09:34 AM

NVIDIA Ex1002
Page 231 of 392

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L12	8452	L5 AND stream	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:35 AM
L13	946	(neuron OR neural) SAME (user near3 stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:37 AM
L14	2	(neuron OR neural) SAME ((user near3 stream) AND (computation near3 stream))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	OR	ON	ON	2022/02/16 09:38 AM

			JPO; DERWENT; IBM_TDB)				
L15	0	(neuron OR neural) SAME ((user near3 thread) AND (computation near3 thread))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:39 AM
L16	39	(neuron OR neural) AND ((user near3 thread) AND (computation near3 thread))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:39 AM
L17	280923	((neuron OR neural) near3 network) WITH (stream OR thread OR process OR job OR task)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:44 AM
L18	7156	(((neuron OR neural) near3 network) WITH (stream OR thread OR process OR job OR task)) SAME ((graphic$4 ADJ	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/02/16 09:45 AM

NVIDIA Ex1002
Page 233 of 392

		process$4 ADJ unit) OR GPU)	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L19	559	L18 AND ((user near3 (interface OR interact$4)) WITH (stream OR thread OR process OR job OR task))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 09:48 AM
L20	12169	(((neuron OR neural) near3 network) WITH (stream OR thread OR process OR job OR task)) SAME (process$4 ADJ unit)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 10:38 AM
L21	2584	L20 AND ((separat$4 OR divid$4 OR split$4 OR distribut$4 OR balanc$4) near3 (thread OR job OR process OR stream OR task))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2022/02/16 10:55 AM

			IBM_TDB)				
L22	98	L21 AND (((neuron OR neural) near3 network) near3 (dedicat$4 OR offload$4 OR partition$4 OR devot$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 10:59 AM
L23	24274	(neural near2 network near2 processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:20 PM
L24	556	(neural near2 network near2 (dedicat$4 OR specific$4 OR devot$4) near2 processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:21 PM
L25	541	L24 AND (stream OR thread OR task OR job OR process)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/02/16 02:22 PM

NVIDIA Ex1002
Page 235 of 392

			IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L26	78	L24 AND ((user OR interface OR interact$4) near3 (stream OR thread OR task OR job OR process))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:23 PM
L27	27097	G06T1/60.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:54 PM
L28	30987	G06F9/5027.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:55 PM

L29	44134	G06T1/20.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:55 PM
L30	166437	G06N20/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:56 PM
L31	32308	G06N3/063.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:56 PM
L32	6052	G06F2209/509.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2022/02/16 02:56 PM

			MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L33	9	gorchetchnikov.in. near2 anatoli.in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:58 PM
L34	42	ames.in. near2 heather.in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:59 PM
L35	71	versace.in. near2 massimiliano.in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 02:59 PM
L36	40	santini.in. near2	(US-PGPUB; USPAT;	OR	ON	ON	2022/02/16

NVIDIA Ex1002
Page 238 of 392

		fabrizio.in.	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:00 PM
L37	4259	G06N7/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:05 PM
L38	2380	G06N7/02.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:06 PM
L39	1334	G06N7/04.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2022/02/16 03:06 PM

			NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L40	261	G06N7/046.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:06 PM
L41	460	G06N7/06.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:06 PM
L42	3074	G06N5/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:06 PM
L43	1745	G06N3/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2022/02/16 03:07 PM

NVIDIA Ex1002
Page 240 of 392

			AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L44	21248	G06N3/02.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:08 PM
L45	46069	G06N3/04.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:09 PM
L46	1961	G06N3/06.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2022/02/16 03:09 PM

NVIDIA Ex1002
Page 241 of 392

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L47	168450	G06N3/08.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:09 PM
L48	3371	G06N3/10.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:10 PM
L49	1934	(L27 OR L28 OR L29 OR L30 OR L31 OR L32) AND ((neuron OR neural) near3 network near3 (comput$6 OR execut$4) near3 (thread OR process OR job OR task OR stream))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:13 PM
L50	1	(L33 OR L34 OR L35 OR L36) AND ((neuron OR neural) near3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2022/02/16 03:14 PM

NVIDIA Ex1002
Page 242 of 392

		network near3 (comput$6 OR execut$4) near3 (thread OR process OR job OR task OR stream))	CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L51	2688	(L37 OR L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR L44 OR L45 OR L46 OR L47 OR L48) AND ((neuron OR neural) near3 network near3 (comput$6 OR execut$4) near3 (thread OR process OR job OR task OR stream))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/16 03:15 PM
L52	9	L49 AND ((shift$4 OR chang$4 OR alter$4 OR mov$4 OR adjust$4) near3 priorit$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 09:56 AM
L53	1	L50 AND ((shift$4 OR chang$4 OR alter$4 OR mov$4 OR adjust$4) near3 priorit$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK,	OR	ON	ON	2022/02/17 09:57 AM

			TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L54	9	L51 AND ((shift$4 OR chang$4 OR alter$4 OR mov$4 OR adjust$4) near3 priorit$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 09:57 AM
L55	1	L50 AND (camera near3 input)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:07 AM
L56	1	L50 AND (memory ADJ partition)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:08 AM
L57	13	(L33 OR L34 OR L35 OR L36) AND ((neuron OR neural) near3 network near3 (thread	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/02/17 10:27 AM

NVIDIA Ex1002
Page 244 of 392

		OR process OR job OR task OR stream))	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L58	5	(L33 OR L34 OR L35 OR L36) AND ((neuron OR neural) near3 network) AND (memory ADJ partition)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:29 AM
L59	455014	(L27 OR L28 OR L29 OR L30 OR L31 OR L32) OR (L37 OR L38 OR L39 OR L40 OR L41 OR L42 OR L43 OR L44 OR L45 OR L46 OR L47 OR L48)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:33 AM
L60	14	L59 AND (((neuron OR neural) near2 network) WITH (memory near3 swap$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2022/02/17 10:37 AM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L61	269	L59 AND ((neuron OR neural) near2 network) AND (memory near3 swap$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:39 AM
L62	413	L59 AND ((neuron OR neural) near2 network) AND (memory SAME swap$4 SAME (address OR pointer))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:40 AM
L63	339	L62 AND ((neuron OR neural) SAME processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:41 AM
L64	311	L62 AND ((neuron OR neural) WITH processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2022/02/17 10:42 AM

NVIDIA Ex1002
Page 246 of 392

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L65	186	L62 AND ((neuron OR neural) near3 processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 10:42 AM
L66	66	L59 AND (((neuron OR neural) near3 network) SAME opengl)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 01:52 PM
L67	12	L59 AND (((neuron OR neural) near3 network) SAME directx)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	OR	ON	ON	2022/02/17 01:56 PM

			JPO; DERWENT; IBM_TDB)				
L68	99	((neuron OR neural) near3 network) WITH (directx OR opengl)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 01:57 PM
L69	1265	((neuron OR neural) near3 network) WITH (stream near2 process$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 02:02 PM
L70	0	L69 AND (memory WITH swap$4 WITH (address OR pointer))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 02:04 PM
L71	7	L69 AND ((focus$4 OR shift$4 OR chang$4 OR mov$4 OR alter$4 OR adjust$4) near3 priorit$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2022/02/17 02:05 PM

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L72	3	("7219085").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/17 02:30 PM
L73	69	("10083523" OR "20010010034" OR "20020046271" OR "20020050518" OR "20020064314" OR "20020168100" OR "20030026588" OR "20030078754" OR "20040015334" OR "20050166042" OR "20060129506" OR "20060184273" OR "20070052713" OR "20070198222" OR "20070279429" OR "20080033897" OR "20080066065" OR "20080258880" OR "20090080695" OR "20090089030" OR "20090116688" OR "20100048242" OR "20110004341" OR "20110173015" OR "20110279682" OR "20120072215" OR "20120089552" OR "20120197596" OR "20120316786" OR "20130126703" OR "20130131985" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/02/23 09:10 AM

		"20140019392" OR "20140032461" OR "20140052679" OR "20140089232" OR "20150127149" OR "20150134232" OR "20150224648" OR "20160075017" OR "20160082597" OR "20160096270" OR "20160198000" OR "20170024877" OR "20170076194" OR "20170193298" OR "5063603" OR "5136687" OR "5142665" OR "5172253" OR "5388206" OR "6018696" OR "6336051" OR "6647508" OR "7119810" OR "7219085" OR "7477256" OR "7525547" OR "7765029" OR "7861060" OR "7873650" OR "8392346" OR "8510244" OR "8583286" OR "8648867" OR "9031692" OR "9177246" OR "9189828" OR "9626566" OR "RE48438").pn.					
L74	2157	(stream ADJ comput$4) WITH control$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 03:37 PM
L75	510	L74 AND (stream near3 (user OR interfac$4 OR interaction))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2022/02/24 03:38 PM

NVIDIA Ex1002
Page 250 of 392

			CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L76	32	L75 AND (stream near3 (priorit$4 OR priviledg$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 03:39 PM
L77	257879	(stream near3 (switch$4 OR chang$4 OR priviledg$4 OR priorit$4 OR focus$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 03:46 PM
L78	7050	L77 AND ((neuron OR neural) near3 network)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK,	OR	ON	ON	2022/02/24 03:47 PM

NVIDIA Ex1002
Page 251 of 392

			TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L79	483	L77 AND (((neuron OR neural) near3 network) near3 processor)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 03:47 PM
L80	982846	((instruction OR execut$4 OR comput$4 OR computation$4 OR calculat$4 OR process$4) near3 stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 04:05 PM
L81	288800	((user OR interaction OR interfac$4) near3 stream)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 06:13 PM
L82	109370	L80 AND L81	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/02/24 06:13 PM

NVIDIA Ex1002
Page 252 of 392

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L83	36893	L82 AND (stream near3 (control$4 OR manag$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/24 06:14 PM
L84	9	("7477256" OR "7525547" OR "20060129506").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/02/28 06:21 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

NVIDIA Ex1002
Page 253 of 392

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	1	HODGKIN, A. L., and HUXLEY, A. F. 1952. Quantitative description of membrane current and its application to conduction and excitation in nerve. J Physiol 117, pp. 500–544.	
/WHW/	2	HOPFIELD, J. 1982. Neural networks and physical systems with emergent collective computational abilities. In Proc Natl Acad Sci USA, vol. 79, pp. 2554–2558.	
/WHW/	3	Ilie, A. 2002. Optical character recognition on graphics hardware. Tech. Rep. integrative paper, UNCCH, Department of Computer Science, 9 pages.	
/WHW/	4	International Preliminary Report on Patentability in related PCT Application No. PCT/US2014/039162 filed 22 May 2014, mailed 24 November 2015, 7 pages.	
/WHW/	5	International Preliminary Report on Patentability in related PCT Application No. PCT/US2014/039239 filed 22 May 2014, mailed 24 November 2015, 8 pages.	
/WHW/	6	International Preliminary Report on Patentability mailed November 8, 2016 from International Application No. PCT/US2015/029438, 7 pages (Atty. Docket No. NRLA-006/01WO)	
/WHW/	7	International Search Report and Written Opinion mailed February 18, 2015 from International Application No. PCT/US2014/039162, 12 pages (Atty. Docket No. NRLA-002/01WO)	
/WHW/	8	International Search Report and Written Opinion mailed February 23, 2016 from International Application No. PCT/US2015/029438, 11 pages (Atty. Docket No. NRLA-006/01WO)	
/WHW/	9	International Search Report and Written Opinion mailed July 6, 2017 from International Application No. PCT/US2017/029866, 12 pages (Atty. Docket No. NRLA-009/01WO).	
/WHW/	10	International Search Report and Written Opinion mailed November 26, 2014 from International Application No. PCT/US2014/039239, 14 pages (Atty. Docket No. NRLA-003/01WO)	
/WHW/	11	International Search Report and Written Opinion mailed September 15, 2015 from International Application No. PCT/US2015/021492, 9 pages (Atty. Docket No. NRLA-004/01WO)	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	12	Itti, L., and Koch, C. (2001). Computational modelling of visual attention. Nature Reviews Neuroscience, 2 (3), 194-203.	
/WHW/	13	Itti, L., Koch, C., and Niebur, E. (1998). A Model of Saliency-Based Visual Attention for Rapid Scene Analysis, 1–6.	
/WHW/	14	Jarrett, K., Kavukcuoglu, K., Ranzato, M. A., & LeCun, Y. (2009, September). What is the best multi-stage architecture for object recognition?. In Computer Vision, 2009 IEEE 12th International Conference on (pp. 2146-2153). IEEE.	
/WHW/	15	KHALIGH-RAZAVI, S. -M. et al., Deep Supervised, but Not Unsupervised, Models May Explain IT Cortical Representation, PLoS Computational Biology, Vol. 10, Issue 11, 29 pages (November 2014).	
/WHW/	16	Kim, S., Novel approaches to clustering, biclustering and algorithms based on adaptive resonance theory and intelligent control, Doctoral Dissertations, Missouri University of Science and Technology, 125 pages (2016).	
/WHW/	17	KIPFER, P., SEGAL, M., and WESTERMANN, R. 2004. UberFlow: A GPU-Based Particle Engine. In Proceedings of the SIGGRAPH/Eurographics Workshop on Graphics Hardware 2004, pp. 115–122.	
/WHW/	18	KOLB, A., L. LATTA, and C. REZK-SALAMA. 2004. "Hardware-Based Simulation and Collision Detection for Large Particle Systems." In Proceedings of the SIGGRAPH/Eurographics Workshop on Graphics Hardware 2004, pp. 123–131.	
/WHW/	19	Kompella, Varun Raj, Luciw, Matthew, and Schmidhuber, J¨urgen. Incremental slow feature analysis: Adaptive low-complexity slow feature updating from high-dimensional input streams. Neural Computation, 24(11):2994–3024, 2012.	
/WHW/	20	Kowler, E. (2011). Eye movements: The past 25years. Vision Research, 51(13), 1457–1483. doi:10.1016/j.visres.2010.12.014	
/WHW/	21	Larochelle H., & Hinton G. (2012). Learning to combine foveal glimpses with a third-order Boltzmann machine. NIPS 2010,1243-1251.	
/WHW/	22	LeCun, Y., Kavukcuoglu, K., & Farabet, C. (2010, May). Convolutional networks and applications in vision. In Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on (pp. 253-256). IEEE.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	23	Lee, D. D. and Seung, H. S. (1999). Learning the parts of objects by non-negative matrix factorization. Nature, 401 (6755):788-791.	
/WHW/	24	Lee, D. D., and Seung, H. S. (1997). "Unsupervised learning by convex and conic coding." Advances in Neural Information Processing Systems, 9.	
/WHW/	25	Legenstein, R., Wilbert, N., and Wiskott, L. Reinforcement learning on slow features of high-dimensional input streams. PLoS Computational Biology, 6(8), 2010. ISSN 1553-734X. 13 pages.	
/WHW/	26	Léveillé, J., Ames, H., Chandler, B., Gorchetchnikov, A., Mingolla, E., Patrick, S., and Versace, M. (2010) Learning in a distributed software architecture for large-scale neural modeling. BIONETICS10, Boston, MA, USA. 8 pages.	
/WHW/	27	Livitz G., Versace M., Gorchetchnikov A., Vasilkoski Z., Ames H., Chandler B., Leveille J. and Mingolla E. (2011) Adaptive, brain-like systems give robots complex behaviors, The Neuromorphic Engineer, : 10.2417/1201101.003500 February 2011. 3 pages.	
/WHW/	28	Livitz, G., Versace, M., Gorchetchnikov, A., Vasilkoski, Z., Ames, H., Chandler, B., Léveillé, J., Mingolla, E., Snider, G., Amerson, R., Carter, D., Abdalla, H., and Qureshi, S. (2011) Visually-Guided Adaptive Robot (ViGuAR). Proceedings of the International Joint Conference on Neural Networks (IJCNN) 2011, San Jose, CA, USA. 9 pages.	
/WHW/	29	Lowe, D.G.(2004). Distinctive Image Features from Scale-Invariant Keypoints. Journal International Journal of Computer Vision archive Volume 60, 2, 91 – 110.	
/WHW/	30	Lu, Z.L., Liu, J., and Dosher, B.A. (2010) Modeling mechanisms of perceptual learning with augmented Hebbian re-weighting. Vision Research, 50(4). 375–390.	
/WHW/	31	LUO et al., "Artificial neural network computation on graphic process unit." Neural Networks, 2005. IJCNN'05. Proceedings. 2005 IEEE International Joint Conference on. Vol. 1. IEEE, 2005. Pages 622-626.	
/WHW/	32	Mahadevan, S. Proto-value functions: Developmental reinforcement learning. In Proceedings of the 22nd international conference on Machine learning, pp. 553–560. ACM, 2005.	
/WHW/	33	MEUTH, J.R. and WUNSCH, D.C. (2007) A SURVEY OF NEURAL COMPUTATION ON GRAPHICS PROCESSING HARDWARE. 22nd IEEE International Symposium on Intelligent Control, Part of IEEE Multi-conference on Systems and Control, Singapore, 1-3 October 2007, 5 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	34	Mishkin M, Ungerleider LG. (1982). "Contribution of striate inputs to the visuospatial functions of parieto-preoccipital cortex in monkeys," Behav Brain Res, 6 (1): 57–77.	
/WHW/	35	Mnih, Volodymyr, Kavukcuoglu, Koray, Silver, David, Rusu, Andrei A, Veness, Joel, Bellemare, Marc G, Graves, Alex, Riedmiller, Martin, Fidjeland, Andreas K, Ostrovski, Georg, et al. Human-level control through deep reinforcement learning. Nature, 518(7540):529–533, 25 February 2015.	
/WHW/	36	MONTRYM et al., The GeForce 6800, in IEEE Micro, vol. 25, no. 2, pp. 41-51, March-April 2005.	
/WHW/	37	Moore, Andrew W and Atkeson, Christopher G. Prioritized sweeping: Reinforcement learning with less data and less time. Machine Learning, 13(1):103–130, 1993.	
/WHW/	38	Najemnik, J., and Geisler, W. (2009). Simple summation rule for optimal fixation selection in visual search. Vision Research. 49, 1286–1294.	
/WHW/	39	Non-Final Office Action mailed 01/04/2018 from U.S. Application Serial No. 15/262,637, 23 pages (Atty. Docket No. NRLA-004/01US)	
/WHW/	40	Non-Final Office Action mailed 05/31/18 from U.S. Application Serial No. 14/947,516, 16 pages (Atty. Docket No. NRLA-003US01)	
/WHW/	41	Notice of Alllowance mailed May 22, 2018 from U.S. Application Serial No. 15/262,637, 6 pages (Atty. Docket No. NRLA-004/01US).	
/WHW/	42	Notice of Allowance mailed 07/27/2016 from U.S. Application Serial No. 14/662,657 (Atty. Docket No. NRLA-005/01US)	
/WHW/	43	Notice of Allowance mailed 12/16/2016 from U.S. Application Serial No. 14/662,657 (Atty. Docket No. NRLA-005/01US)	
/WHW/	44	OH, K.-S., and JUNG, K. 2004. GPU implementation of neural networks. Pattern Recognition 37, pp. 1311–1314.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	45	Oja, E. (1982). Simplified neuron model as a principal component analyzer. Journal of Mathematical Biology 15(3), 267–273.	
/WHW/	46	Partial Supplementary European Search Report dated July 4, 2017 from European Application No. 14800348.6, 13 pages (Atty. Docket No. NRLA-003/01EP).	
/WHW/	47	PERUMALLA, "Discrete-event execution alternatives on general purpose graphical processing units (GPGPUs)." Proceedings of the 20th Workshop on Principles of Advanced and Distributed Simulation. IEEE Computer Society, 2006.8 pages.	
/WHW/	48	Raijmakers, M.E.J., and Molenaar, P. (1997). Exact ART: A complete implementation of an ART network Neural networks 10 (4), 649-669.	
/WHW/	49	Ranzato, M. A., Huang, F. J., Boureau, Y. L., & Lecun, Y. (2007, June). Unsupervised learning of invariant feature hierarchies with applications to object recognition. In Computer Vision and Pattern Recognition, 2007. CVPR'07. IEEE Conference on (pp. 1-8). IEEE.	
/WHW/	50	Raudies, F., Eldridge, S., Joshi, A., and Versace, M. (20 August 2014). Learning to navigate in a virtual world using optic flow and stereo disparity signals. Artificial Life and Robotics, DOI 10.1007/s10015-014-0153-1. 15 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/William H. Wood/	Date Considered	02/24/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/WHW/	1	10083523	B2	2018-09-25	Versace et al.	Entire Document
/WHW/	2	5063603	A	1991-11-05	Burt	
/WHW/	3	5136687	A	1992-08-04	Edelman et al.	
/WHW/	4	5142665	A	1992-08-25	Bigus	Entire Document
/WHW/	5	5172253	A	1992-12-15	Lynne	Entire Document
/WHW/	6	5388206	A	1995-02-07	Poulton et al.	
/WHW/	7	6018696	A	2000-01-25	Matsuoka et al.	
/WHW/	8	6647508	B2	2003-11-11	Zalewski et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	9	6336051	B1	2002-01-01	Pangels et al.	Entire Document
/WHW/	10	7119810	B2	2006-10-10	Sumanaweera et al.	Entire Document
/WHW/	11	7219085	B2	2007-05-15	Buck et al.	Entire Document
/WHW/	12	7525547	B1	2009-04-28	Diard	Entire Document
/WHW/	13	7765029	B2	2010-07-27	Fleischer et al.	
/WHW/	14	7861060	B1	2010-12-28 2010-12-01	Nickolls et al.	
/WHW/	15	7477256	B1	2009-01-13	Johnson	Entire Document
/WHW/	16	7873650	B1	2011-01-18	Chapman et al.	Entire Document
/WHW/	17	8510244	B2	2013-08-13	Carson et al.	
/WHW/	18	8583286	B2	2013-11-12	Fleischer et al.	
/WHW/	19	8648867		2014-02-11	Gorchetchnikov et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	20	8392346	B2	2013-03-05	Ueda et al.	Entire Document
/WHW/	21	9626566	B2	2017-04-18	Versace et al.	Entire Document
/WHW/	22	9031692	B2	2015-05-12	Zhu	Entire Document
/WHW/	23	9177246	B2	2015-11-03	Buibas et al.	Entire Document
/WHW/	24	9189828	B2	2015-11-17	Gorchetchnikov et al.	
/WHW/	25	RE48438		2021-02-16	Gorchetchnikov et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/WHW/	1	20010010034	A1	2001-07-26	Burton	Entire Document
/WHW/	2	20020046271	A1	2002-04-18	Huang	
/WHW/	3	20020050518	A1	2002-05-02	Roustaei	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	4	20020064314	A1	2002-05-30	Comaniciu et al.	
/WHW/	5	20020168100	A1	2002-11-14	Woodall	
/WHW/	6	20030026588	A1	2003-02-06	Elder et al.	Entire Document
/WHW/	7	20030078754	A1	2003-04-24	Hamza	
/WHW/	8	20040015334	A1	2004-01-22	Ditlow et al.	
/WHW/	9	20050166042	A1	2005-07-28	Evans	
/WHW/	10	20060129506	A1	2006-06-15	Edelman et al.	Entire Document
/WHW/	11	20060184273	A1	2006-08-17	Sawada et al.	
/WHW/	12	20070052713	A1	2007-03-08	Chung et al.	
/WHW/	13	20070198222	A1	2007-08-23	Schuster et al.	Entire Document
/WHW/	14	20070279429	A1	2007-12-06	Ganzer	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	15	20080033897	A1	2008-02-07	Lloyd	
/WHW/	16	20080066065	A1	2008-03-13	Kim et al.	
/WHW/	17	20080258880	A1	2008-10-23	Smith et al.	Entire Document
/WHW/	18	20090080695	A1	2009-03-26	Yang	
/WHW/	19	20090089030	A1	2009-04-02	Sturrock et al.	
/WHW/	20	20090116688	A1	2009-05-07	Monacos et al.	
/WHW/	21	20100048242	A1	2010-02-25	Rhoads et al.	Entire Document
/WHW/	22	20110004341	A1	2011-01-06	Sarvadevabhatla et al.	
/WHW/	23	20110173015	A1	2011-07-14	Chapman et al.	
/WHW/	24	20110279682	A1	2011-11-17	Li et al.	
/WHW/	25	20120072215	A1	2012-03-22	Yu et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	26	20120089552	A1	2012-04-12	Chang et al.	
/WHW/	27	20120197596	A1	2012-08-02	Comi	
/WHW/	28	20120316786	A1	2012-12-13	Liu et al.	Entire Document
/WHW/	29	20130126703	A1	2013-05-23	Caulfield	
/WHW/	30	20130131985	A1	2013-05-23	Weiland et al.	
/WHW/	31	20140019392	A1	2014-01-16	Buibas et al.	
/WHW/	32	20140032461	A1	2014-01-30	Weng	Entire Document
/WHW/	33	20140052679	A1	2014-02-20	Sinyavskiy et al.	
/WHW/	34	20140089232	A1	2014-03-27	Buibas et al.	
/WHW/	35	20150127149	A1	2015-05-07	Sinyavskiy et al.	Entire Document
/WHW/	36	20150134232	A1	2015-05-14	Robinson	Entire Document

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	37	20150224648	A1	2015-08-13	Lee et al.	
/WHW/	38	20160075017	A1	2016-03-17	Laurent et al.	Entire Document
/WHW/	39	20160082597	A1	2016-03-24	Gorshechnikov et al.	
/WHW/	40	20160096270	A1	2016-04-07	Gabardos et al.	Entire Document
/WHW/	41	20160198000	A1	2016-07-07	Gorshechnikov et al.	
/WHW/	42	20170024877	A1	2017-01-26	Versace et al.	
/WHW/	43	20170076194	A1	2017-03-16	Versace et al.	
/WHW/	44	20170193298	A1	2017-07-06	Versace et al.	Entire Document

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
/WHW/	1	1224622	EP	B1	2004-11-10	Deering et al.		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	2	190208	WO		2014-11-27	Neurala, Inc.		
/WHW/	3	2014204615	WO	A2	2014-12-24	Gorshechnikov et al.		
/WHW/	4	2015143173	WO	A2	2015-09-24	Neurala, Inc.		
/WHW/	5	2016014137	WO	A2	2016-01-28	Gorchetchnikov et al.		

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
/WHW/	1	Adelson, E. H., Anderson, C. H., Bergen, J. R., Burt, P. J., & Ogden, J. M. (1984). Pyramid methods in image processing. RCA engineer, 29(6), 33-41.	
/WHW/	2	Aggarwal, Charu C, Hinneburg, Alexander, and Keim, Daniel A. On the surprising behavior of distance metrics in high dimensional space. Springer, 2001. 15 pages.	
/WHW/	3	AL-KAYSI, A. M. et al., A Multichannel Deep Belief Network for the Classification of EEG Data, from Ontology-based Information Extraction for Residential Land Use Suitability: A Case Study of the City of Regina, Canada, DOI 10.1007/978-3-319-26561-2_5, 8 pages (November 2015).	
/WHW/	4	Ames, H, Versace, M., Gorchetchnikov, A., Chandler, B., Livitz, G., Léveillé, J., Mingolla, E., Carter, D., Abdalla, H., and Snider, G. (2012) Persuading computers to act more like brains. In Advances in Neuromorphic Memristor Science and Applications, Kozma, R.Pino,R., and Pazienza, G. (eds), Springer Verlag. 25 pages.	
/WHW/	5	Ames, H. Mingolla, E., Sohail, A., Chandler, B., Gorchetchnikov, A., Léveillé, J., Livitz, G. and Versace, M. (2012) The Animat. IEEE Pulse, February 2012, 3(1), 47-50.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	6	APOLLONI, B. et al., Training a network of mobile neurons, Proceedings of International Joint Conference on Neural Networks, San Jose, CA, doi: 10.1109/IJCNN.2011.6033427, pp. 1683-1691 (July 31-August 5, 2011).	
/WHW/	7	Artificial Intelligence as a Service. Invited talk, Defrag, Broomfield, CO, Nov. 4-6, 2013. 22 pages.	
/WHW/	8	Aryananda, L. 2006. Attending to learn and learning to attend for a social robot. Humanoids 06, pp. 618-623.	
/WHW/	9	Baraldi, A. and Alpaydin, E. (1998). Simplified ART: A new class of ART algorithms. International Computer Science Institute, Berkeley, CA, TR-98-004, 1998. 42 pages.	
/WHW/	10	Baraldi, A. and Alpaydin, E. (2002). Constructive feedforward ART clustering networks – Part I. IEEE Transactions on Neural Networks 13(3), 645–661.	
/WHW/	11	Baraldi, A. and Parmiggiani, F. (1997). Fuzzy combination of Kohonen's and ART neural network models to detect statistical regularities in a random sequence of multi-valued input patterns. In International Conference on Neural Networks, IEEE. 6 pages.	
/WHW/	12	Baraldi, Andrea and Alpaydin, Ethem. Constructive feedforward ART clustering networks—part II. IEEE Transactions on Neural Networks, 13(3):662–677, May 2002. ISSN 1045-9227. doi: 10. 1109/tnn.2002.1000131. URL http://dx.doi. org/10.1109/tnn.2002.1000131.	
/WHW/	13	Bengio, Y., Courville, A., & Vincent, P. Representation learning: A review and new perspectives, IEEE Transactions on Pattern Analysis and Machine Intelligence, Volume 35 Issue 8, August 2013. Pages 1798-1828 .	
/WHW/	14	Berenson, D. et al., A robot path planning framework that learns from experience, 2012 International Conference on Robotics and Automation, 2012, 9 pages [retrieved from the internet] URL:http://users.wpi.edu/-dberenson/lightning. pdf.	
/WHW/	15	BERNHARD, F., and KERIVEN, R. 2005. Spiking Neurons on GPUs. Tech. Rep. 05-15, Ecole Nationale des Ponts et Chauss´es, 8 pages.	
/WHW/	16	Besl, P. J., & Jain, R. C. (1985). Three-dimensional object recognition. ACM Computing Surveys (CSUR), 17(1), 75-145.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	17	BODDAPATI, V., Classifying Environmental Sounds with Image Networks, Thesis, Faculty of Computing Blekinge Institute of Technology, 37 pages (February 2017).	
/WHW/	18	Bohn, C.-A. Kohonen. 1998. Feature Mapping Through Graphics Hardware. In Proceedings of 3rd Int. Conference on Computational Intelligence and Neurosciences, 4 pages.	
/WHW/	19	Bradski, G., & Grossberg, S. (1995). Fast-learning VIEWNET architectures for recognizing three-dimensional objects from multiple two-dimensional views. Neural Networks, 8 (7-8), 1053-1080.	
/WHW/	20	Canny, J.A. (1986). Computational Approach To Edge Detection, IEEE Trans. Pattern Analysis and Machine Intelligence, 8(6):679–698.	
/WHW/	21	Carpenter, G.A. and Grossberg, S. (1987). A massively parallel architecture for a self-organizing neural pattern recognition machine. Computer Vision, Graphics, and Image Processing 37, 54–115.	
/WHW/	22	Carpenter, G.A., and Grossberg, S. (1995). Adaptive resonance theory (ART). In M. Arbib (Ed.), The handbook of brain theory and neural networks. (pp. 79–82). Cambridge, M.A.: MIT press.	
/WHW/	23	Carpenter, G.A., Grossberg, S. and Rosen, D.B. (1991). Fuzzy ART: Fast stable learning and categorization of analog patterns by an adaptive resonance system. Neural Networks 4, 759–771.	
/WHW/	24	Carpenter, Gail A and Grossberg, Stephen. The art of adaptive pattern recognition by a self-organizing neural network. Computer, 21(3):77–88, 1988.	
/WHW/	25	Coifman, R.R. and Maggioni, M. Diffusion wavelets. Applied and Computational Harmonic Analysis, 21(1):53–94, 2006.	
/WHW/	26	Coifman, R.R., Lafon, S., Lee, A.B., Maggioni, M., Nadler, B., Warner, F., and Zucker, S.W. Geometric diffusions as a tool for harmonic analysis and structure definition of data: Diffusion maps. Proceedings of the National Academy of Sciences of the United States of America, 102(21):7426, 2005. 21 pages.	
/WHW/	27	CORNWALL et al., Automatically translating a general purpose C++ image processing library for GPUs. Proceedings 20th IEEE International Parallel & Distributed Processing Symposium, 2006, 8 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	28	DAVIS, C. E. 2005. Graphic Processing Unit Computation of Neural Networks. Master's thesis, University of New Mexico, Albuquerque, NM, 121 pages.	
/WHW/	29	Dosher, B.A., and Lu, Z.L. (2010). Mechanisms of perceptual attention in precuing of location. Vision Res., 40(10–12). 1269–1292.	
/WHW/	30	ELLIAS, S. A., and GROSSBERG, S. 1975. Pattern formation, contrast control and oscillations in the short term memory of shunting on-center off-surround networks. Biol Cybern 20, pp. 69–98.	
/WHW/	31	Extended European Search Report and Written Opinion mailed June 1, 2017 from European Application No. 14813864.7, 10 pages (Atty. Docket No. NRLA-002/01EP)	
/WHW/	32	Extended European Search Report and Written Opinion mailed October 12, 2017 from European Application No. 14800348.6, 12 pages (Atty. Docket No. NRLA-003/01EP)	
/WHW/	33	Extended European Search Report and Written Opinion October 23, 2017 from European Application No. 15765396.5, 8 pages (Atty. Docket No. NRLA-004/01EP)	
/WHW/	34	Fazl, A., Grossberg, S., and Mingolla, E. (2009). View-invariant object category learning, recognition, and search: How spatial and object attention are coordinated using surface-based attentional shrouds. Cognitive Psychology 58, 1–48.	
/WHW/	35	Földiák, P. (1990). Forming sparse representations by local anti-Hebbian learning, Biological Cybernetics, vol. 64, pp. 165-170.	
/WHW/	36	Friston K., Adams R., Perrinet L., & Breakspear M. (2012). Perceptions as hypotheses: saccades as experiments. Frontiers in Psychology, 3 (151), 1-20.	
/WHW/	37	Galbraith, B.V, Guenther, F.H., and Versace, M. (2015) A neural network-based exploratory learning and motor planning system for co-robots. Frontiers in Neuroscience, in press. 10 pages.	
/WHW/	38	George, D. and Hawkins, J. (2009). Towards a mathematical theory of cortical micro-circuits. PLoS Computational Biology 5(10), 1–26.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	39	GEORGII, J., and WESTERMANN, R. 2005. Mass-spring systems on the GPU. Simulation Modelling Practice and Theory 13, pp. 693–702.	
/WHW/	40	Gorchetchnikov A., Hasselmo M. E. (2005). A biophysical implementation of a bidirectional graph search algorithm to solve multiple goal navigation tasks. Connection Science, 17(1-2), pp. 145-166.	
/WHW/	41	Gorchetchnikov A., Hasselmo M. E. (2005). A simple rule for spike-timing-dependent plasticity: local influence of AHP current. Neurocomputing, 65-66, pp. 885-890.	
/WHW/	42	Gorchetchnikov A., Versace M., Hasselmo M. E. (2005). A Model of STDP Based on Spatially and Temporally Local Information: Derivation and Combination with Gated Decay. Neural Networks, 18, pp. 458-466.	
/WHW/	43	GORCHETCHNIKOV A., VERSACE M., HASSELMO M. E. (2005). Spatially and temporally local spike-timing-dependent plasticity rule. In: Proceedings of the International Joint Conference on Neural Networks, number 1568 in IEEE CD-ROM Catalog Number: 05CH37662C, pp. 390-396.	
/WHW/	44	GORCHETCHNIKOV, A. 2017. An Approach to a Biologically Realistic Simulation of Natural Memory. Master's thesis, Middle Tennessee State University, Murfreesboro, TN, 70 pages.	
/WHW/	45	Grossberg, S. (1973). Contour enhancement, short-term memory, and constancies in reverberating neural networks. Studies in Applied Mathematics 52, 213–257.	
/WHW/	46	Grossberg, S., and Huang, T.R. (2009). ARTSCENE: A neural system for natural scene classification. Journal of Vision, 9 (4), 6.1–19. doi:10.1167/9.4.6	
/WHW/	47	Grossberg, S., and Versace, M. (2008) Spikes, synchrony, and attentive learning by laminar thalamocortical circuits. Brain Research, 1218C, 278-312 [Authors listed alphabetically].	
/WHW/	48	HAGEN, T. R., HJELMERVIK, J., LIE, K.-A., NATVIG, J., AND OFSTAD HENRIKSEN, M. 2005. Visual simulation of shallow-water waves. Simulation Modelling Practice and Theory 13, pp. 716–726.	
/WHW/	49	Hasselt, Hado Van. Double q-learning. In Advances in Neural Information Processing Systems, pp. 2613–2621,2010.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	50	Hinton, G. E., Osindero, S., and Teh, Y. (2006). A fast learning algorithm for deep belief nets. Neural Computation, 18, 1527–1554.

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/William H. Wood/	Date Considered	02/24/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17136343
Filing Date	2020-12-29
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	
Examiner Name	
Attorney Docket Number	NRLA-001US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	1	REN, Y. et al., Ensemble Classification and Regression - Recent Developments, Applications and Future Directions, in IEEE Computational Intelligence Magazine, 10.1109/MCI.2015.2471235, 14 pages (2016).	
/WHW/	2	Riesenhuber, M., & Poggio, T. (1999). Hierarchical models of object recognition in cortex. Nature Neuroscience, 2 (11), 1019-1025.	
/WHW/	3	Riesenhuber, M., & Poggio, T. (2000). Models of object recognition. Nature neuroscience, 3, 1199-1204.	
/WHW/	4	ROLFES, T. 2004. Artificial Neural Networks on Programmable Graphics Hardware. In Game Programming Gems 4, A. Kirmse, Ed. Charles River Media, Hingham, MA, pp. 373–378.	
/WHW/	5	Rublee, E., Rabaud, V., Konolige, K., & Bradski, G. (2011). ORB: An efficient alternative to SIFT or SURF. In IEEE International Conference on Computer Vision (ICCV) 2011, 2564–2571.	
/WHW/	6	Ruesch, J. et al. 2008. Multimodal Saliency-Based Bottom-Up Attention a Framework for the Humanoid Robot iCub. 2008 IEEE International Conference on Robotics and Automation, pp. 962-965.	
/WHW/	7	Rumelhart D., Hinton G., and Williams, R. (1986). Learning internal representations by error propagation. In Parallel distributed processing: explorations in the microstructure of cognition, vol. 1, MIT Press. 45 pages.	
/WHW/	8	RUMPF, M. and STRZODKA, R. Graphics processor units: New prospects for parallel computing. In Are Magnus Bruaset and Aslak Tveito, editors, Numerical Solution of Partial Differential Equations on Parallel Computers, volume 51 of Lecture Notes in Computational Science and Engineering, pp. 89–134. Springer, 2005.	
/WHW/	9	Salakhutdinov, R., & Hinton, G. E. (2009). Deep boltzmann machines. In International Conference on Artificial Intelligence and Statistics (pp. 448-455).	
/WHW/	10	Schaul, Tom, Quan, John, Antonoglou, Ioannis, and Silver, David. Prioritized experience replay. arXiv preprint arXiv: 1511.05952, 18 November 2015. 21 pages.	
/WHW/	11	Schmidhuber, J. (2010). Formal theory of creativity, fun, and intrinsic motivation (1990–2010). Autonomous Mental Development, IEEE Transactions on, 2(3), 230-247.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	12	Schmidhuber, Jürgen. Curious model-building control systems. In Neural Networks, 1991. 1991 IEEE International Joint Conference on, pp. 1458–1463. IEEE, 1991.	
/WHW/	13	Seibert, M., & Waxman, A.M. (1992). Adaptive 3-D Object Recognition from Multiple Views. IEEE Transactions on Pattern Analysis and Machine Intelligence, 14 (2), 107-124.	
/WHW/	14	SETOAIN et al., "Parallel hyperspectral image processing on commodity graphics hardware." Parallel Processing Workshops, 2006. ICPP 2006 Workshops. 2006 International Conference on. IEEE, 2006. 8 pages.	
/WHW/	15	Sherbakov, L. and Versace, M. (2014) Computational principles for an autonomous active vision system. Ph.D., Boston University, http://search.proquest.com/docview/1558856407. 194 pages.	
/WHW/	16	SHERBAKOV, L. et al. 2012. CogEye: from active vision to context identification, youtube, retrieved from the Internet on 10-10-2017: URL://www.youtube.com/watch?v=i5PQk962B1k, 1 page.	
/WHW/	17	SHERBAKOV, L. et al. 2013. CogEye: system diagram module brain area function algorithm approx # neurons, retrieved from the Internet on 10-12-2017: URL://http://www-labsticc.univ-ubs.fr/~coussy/neucomp2013/index_fichiers/material/posters/NeuComp2013_final56x36.pdf, 1 page.	
/WHW/	18	Sherbakov, L., Livitz, G., Sohail, A., Gorchetchnikov, A., Mingolla, E., Ames, H., and Versace, M (2013b) A computational model of the role of eye-movements in object disambiguation. Cosyne, Feb. 28-Mar. 3, 2013. Salt Lake City, UT, USA. 2 pages.	
/WHW/	19	Sherbakov, L., Livitz, G., Sohail, A., Gorchetchnikov, A., Mingolla, E., Ames, H., and Versace, M. (2013a) CogEye: An online active vision system that disambiguates and recognizes objects. NeuComp 2013. 2 pages.	
/WHW/	20	Smolensky, Paul. Information processing in dynamical systems: Foundations of harmony theory. No. CU-CS-321-86. COLORADO UNIV AT BOULDER DEPT OF COMPUTER SCIENCE, 1986. 88 pages.	
/WHW/	21	Snider, Greg, et al. "From synapses to circuitry: Using memristive memory to explore the electronic brain." IEEE Computer, Volume 44(2). (2011): 21-28.	
/WHW/	22	Spratling, M. W. (2008). Predictive coding as a model of biased competition in visual attention. Vision Research, 48 (12):1391-1408.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	23	Spratling, M. W. (2012). Unsupervised learning of generative and discriminative weights encoding elementary image components in a predictive coding model of cortical function. Neural Computation, 24(1):60-103.	
/WHW/	24	Spratling, M. W., De Meyer, K., and Kompass, R. (2009). Unsupervised learning of overlapping image components using divisive input modulation. Computational intelligence and neuroscience. 20 pages.	
/WHW/	25	Sprekeler, H. On the relation of slow feature analysis and laplacian eigenmaps. Neural Computation, pp. 1–16, 2011.	
/WHW/	26	SUN, Z. et al., Recognition of SAR target based on multilayer auto-encoder and SNN, International Journal of Innovative Computing, Information and Control, Vol. 9, No. 11, pp. 4331-4341, November 2013.	
/WHW/	27	Sutton, R. S., and Barto, A. G. (1998). Reinforcement learning: An introduction(vol. 1, No. 1). Cambridge: MIT press. 10 pages.	
/WHW/	28	Tong, F., Ze-Nian Li, (1995). Reciprocal-wedge transform for space-variant sensing," Pattern Analysis and Machine Intelligence, IEEE Transactions on , vol.17, no.5, pp.500 - 51. doi: 10.1109/34.391393	
/WHW/	29	Torralba, A., Oliva, A., Castelhano, M.S., Henderson, J.M. (2006). Contextual guidance of eye movements and attention in real-world scenes: the role of global features in object search. Psychological Review, 113(4).766–786.	
/WHW/	30	Van Hasselt, Hado, Guez, Arthur, and Silver, David. Deep reinforcement learning with double q-learning. arXiv preprint arXiv: 1509.06461, 22 September 2015. 7 pages.	
/WHW/	31	Versace, Brain-inspired computing. Invited keynote address, Bionetics 2010, Boston, MA, USA. 1 page.	
/WHW/	32	Versace, M. (2006) From spikes to interareal synchrony: how attentive matching and resonance control learning and information processing by laminar thalamocortical circuits. NSF Science of Learning Centers PI Meeting, Washington, DC, USA. 1 page.	
/WHW/	33	Versace, M., (2010) Open-source software for computational neuroscience: Bridging the gap between models and behavior. In Horizons in Computer Science Research, Volume 3. 43 pages.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

/WHW/	34	Versace, M., Ames, H., Léveillé, J., Fortenberry, B., and Gorchetchnikov, A. (2008) KInNeSS: A modular framework for computational neuroscience. Neuroinformatics, 2008 Winter; 6(4):291-309. Epub 2008 Aug 10.	
/WHW/	35	Versace, M., and Chandler, B. (2010) MoNETA: A Mind Made from Memristors. IEEE Spectrum, December 2010. 8 pages.	
/WHW/	36	VERSACE, TEDx Fulbright, Invited talk, Washington DC, 4/5/2014. 30 pages.	
/WHW/	37	Webster, Bachevalier, Ungerleider (1994). Connections of IT areas TEO and TE with parietal and frontal cortex in macaque monkeys. Cerebal Cortex, 4(5), 470-483.	
/WHW/	38	Wiskott, Laurenz and Sejnowski, Terrence. Slow feature analysis: Unsupervised learning of invariances. Neural Computation, 14(4):715–770, 2002.	
/WHW/	39	Wu, Yan & J. Cai, H. (2010). A Simulation Study of Deep Belief Network Combined with the Self-Organizing Mechanism of Adaptive Resonance Theory. 10.1109/CISE.2010.5677265, 4 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/William H. Wood/	Date Considered	02/24/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17136343
	Filing Date	2020-12-29
	First Named Inventor	Anatoli Gorchetchnikov
	Art Unit	
	Examiner Name	
	Attorney Docket Number	NRLA-001US04

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Christopher Max Colice/	Date (YYYY-MM-DD)	2021-03-29
Name/Print	Christopher Max Colice	Registration Number	65634

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

149890 7590 06/01/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
06/01/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@smithbaluch.com
eofficeaction@appcoll.com
smith@smithbaluch.com

Applicant-Initiated Interview Summary	**Application No.** 17/136,343	**Applicant(s)** Gorchetchnikov et al.		
	Examiner WILLIAM H WOOD	**Art Unit** 3992	**AIA (First Inventor to File) Status** No	**Page** 1 of 2

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
WILLIAM H WOOD	Primary Examiner	Telephonic
Max Colice	Attorney of Record	
Anatoli Gorchetchnikov	Inventor	
Alexander Kosowski	SPE	
Rachna Desai	Primary Examiner	

Date of Interview: 24 May 2022

Issues Discussed:

35 U.S.C. 112

Discussed lack of clarity with regard to claim 58 language "shifting priority". No agreement reached.

35 U.S.C. 103

Discussed how broad claim language of claim 58 reads upon the cited prior art. No agreement reached.

Other

Discussed need to correct claim amendment in accordance with status as a continuation reissue application. Also discussed the Declaration's need to refer to the correct application and have a corrected error statement applicable to the current claims. Patent Owner considering.

☑ Attachment

/William H. Wood/ Primary Examiner, Art Unit 3992	/A.J.K/ Supervisory Patent Examiner, Art Unit 3992

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete

and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

From: Max Colice
To: Wood, William
Subject: US 17/136,343 - Attorney-Docket No. NRLA-001US04 - Interview Confirmation & Proposed Agenda
Date: Thursday, May 19, 2022 12:01:51 PM

CAUTION: This email has originated from a source outside of USPTO. **PLEASE CONSIDER THE SOURCE** before responding, clicking on links, or opening attachments.

Examiner Wood,

I am writing to confirm our interview in US 17/136,343 for Tuesday, May 24, at 1 pm ET. Inventor Anatoli Gorchetchnikov will be joining me. Should Anatoli and I call your office line at 1 pm, or would you prefer to talk by video conference instead? I would be happy to provide a link for an MS Teams call.

During the interview, Anatoli and I would like to discuss the obviousness rejections. We would particularly like to ask which portions of Buck are being interpreted as separate user interaction and computational streams. (We see that the background of Buck mentions that "GPUs are essentially stream processors" and that CPUs and GPUs have instruction streams, but we don't see anything about user interaction streams or computational streams.) It is also not clear to us which portions of Buck, Johnson, and Diard disclose or suggest shifting priority between user interaction and computational streams.

I would also like to ask about recapture rejection and the double-patenting rejection over the claims of U.S. Patent No. RE48,438. We were advised by OPLA to file this application as a continuation of U.S. Patent No. RE48,438, which is a re-issue of U.S. Patent No. 9,189,828, ***and*** as a re-issue of U.S. Patent No. 9,189,828 and to include all of the claims of U.S. Patent No. RE48,438. If we should do something different, we would appreciate your guidance.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

Sincerely,
Max Colice
Reg. No. 65,634

Max Colice, Ph.D.
SMITH BALUCH LLP
(617) 947-7280

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/136,343	Filing Date 12/29/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	06/07/2022	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 69	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 8	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TYWANA P LOVELACE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No. NRLA-001US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Gorchetchnikov et al.

Application No. 17/136,343

Filed: 2020-12-29

Confirmation No. 6235

Art Unit: 3992

Examiner: William H. Wood

Title: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

AMENDMENT/RESPONSE TO OFFICE ACTION

In response to the Office Action dated March 7, 2022, Applicant submits the following Amendments and/or Remarks, and respectfully requests reconsideration of the application in view thereof.

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Per 37 C.F.R. § 1.173(d), matter to be omitted is enclosed is brackets and matter to be added is underlined. This listing also reflects any cancellation and/or addition of claims.

1–20. (Canceled)

21. (New, Twice Amended) A method of executing computations representing an artificial neural network on a computer system comprising at least one central processing unit (CPU), a processing unit, a first memory partition, and a second memory partition, the method comprising:

executing, by the at least one CPU, a user interaction stream, the user interaction stream controlling transfer of inputs to the artificial neural network to the first memory partition and the second memory partition;

executing, by the processing unit, a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network;

shifting control of data exchange between the user interaction stream and the computational stream to the computational stream in response to starting execution of the computations representing the artificial neural network;

shifting control of the data exchange between the user interaction stream and the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network;

queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network; and

executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream.

22. (New) The method of claim 21, wherein the user interaction stream controls data exchange between the user interaction stream and the computational stream outside of execution of the computations representing the artificial neural network.

23. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of computational elements of the computations representing the artificial neural network.

24. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of parameters of the computations representing the artificial neural network.

25. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of parameters of the inputs to the artificial neural network.

26. (New) The method of claim 21, wherein executing the user interaction stream comprises:
specifying an output to be saved to disk and/or displayed on a screen.

27. (New) The method of claim 21, wherein executing the user interaction stream comprises:
parsing elements to be used in the computations representing the artificial neural network.

28. (New) The method of claim 27, wherein the processing unit comprises a graphics processing unit (GPU) and executing the user interaction stream further comprises:
converting the elements into GPU programs.

29. (New) The method of claim 28, wherein executing the user interaction stream comprises:
compiling the GPU programs.

30. (New) The method of claim 29, wherein executing the user interaction stream comprises:
transferring the GPU programs to the second memory partition.

31. (New) The method of claim 21, further comprising:
executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk.

32. (New) The method of claim 21, further comprising:
generating the inputs with a video camera during execution of the computations.

33. (New, Amended) A system for executing computations representing an artificial neural network, the system comprising:

a camera to acquire input data for the artificial neural network;

a first memory partition;

a second memory partition;

at least one central processing unit (CPU), operably coupled to the camera, the first memory partition, and the second memory partition, to execute a user interaction stream, the user interaction stream controlling transfer of the input data acquired by the camera to the first memory partition and the second memory partition during execution of the computations representing the artificial neural network;

a processing unit, operably coupled to the first memory partition, the second memory partition, and the at least one CPU, to execute a computational stream, the computational stream controlling transfer of the input data from the first memory partition and the second memory partition during execution of the computations representing the artificial neural network, the execution of the computations representing the artificial neural network occurring while the camera is acquiring the input data; and

a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during the execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption.

34. (New) The system of claim 33, wherein the user interactions cause interruption of the computations representing the artificial neural network.

35. (New) The system of claim 33, wherein the user interactions cause a change in inputs to the artificial neural network.

36. (New) The system of claim 33, wherein the user interactions cause a change in display properties of an output of the computations representing the artificial neural network.

37. (New) The system of claim 33, wherein the controller is configured to request the input data during the execution of the computations representing the artificial neural network, the computational stream controls the data exchange between the user interaction stream and the computational stream by requesting the inputs to the artificial neural network.

38. (New) The method of claim 21, wherein the user command causes interruption of the computations representing the artificial neural network.

39. (New) The method of claim 21, wherein the user command causes a change in the inputs to the artificial neural network.

40. (New) The method of claim 21, wherein the user command causes a change in display properties of an output of the computations representing the artificial neural network.

41. (New) The method of claim 21, wherein, during execution of the computations representing the artificial neural network, the computational stream controls the data exchange between the user interaction stream and the computational stream by requesting the inputs to the artificial neural network.

REMARKS

In response to the Office Action dated March 7, 2022, in the above-identified application, Applicant respectfully requests reconsideration. All of the issues raised in the Office Action have been carefully considered and are addressed in this response. The application as now presented is believed to be in allowable condition.

1. Status of the Claims and Summary of Amendments

Upon entry of this response, claims 21–33 will be pending in this application, of which claims 21 and 33 are independent claims.

In this paper, claims 1–57 are being canceled to address the double patenting rejections.

Claims 58–70 are being renumbered as claims 21–33 per guidance from Examiner Wood and 37 C.F.R. § 1.173(e).

Claim 21 is being amended to recite "shifting control of data exchange between the user interaction stream and the computational stream …" instead of "shifting priority … ." Support for this amendment appears at least in col. 7, lines 45–53 of U.S. Patent No. 9,189,828.

Claim 21 is also being amended to recite "queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network; and executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream." Support for these amendments appears at least in col. 8, lines 34–57, and col. 9, lines 8–18, of U.S. Patent No. 9,189,828.

Claim 33 is being amended to recite "a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption." Support for this amendment appears at least in col. 8, lines 34–57; col. 9, lines 8–18; and FIG. 2 of U.S. Patent No. 9,189,828.

Claims 34–41 are being added. Support for these new claims appears at least in col. 7, lines 15–18; col. 8, lines 34–57; and col. 9, lines 8–18 of U.S. Patent No. 9,189,828.

2. Summary of Telephone Interview with Examiner

Inventor Anatoli Gorchetchnikov and Applicant's representative Christopher Max Colice thank Examiner Wood and his conferees for granting and conducting a telephone interview on

May 24, 2022. During the interview, Examiner Wood indicated that the reissue declarations may need to be corrected and said that he might issue guidance or an objection in the next Office Action. Applicant thanks Examiner Wood for the information and looks forward to receiving any suitable written guidance or objection.

The participants then discussed the double patenting rejections and this application's priority claim. Because this application is a continuation of U.S. Patent No. RE48438, which in turn is a reissue of U.S. Patent No. 9,189,828, Examiner Wood indicated that the double patenting rejections could be overcome by canceling claims 1–57, which issued in U.S. Patent No. RE48438, and renumbering the remaining claims starting at 21 because U.S. Patent No. 9,189,828 includes only 20 claims. Applicant thanks Examiner Wood for this guidance and is adopting it as indicated above.

Finally, the participants discussed the claimed technology and the obviousness rejections. Dr. Gorchetchnikov gave an overview of the claimed technology and the state of the art around the priority date (September 25, 2006). The participants then discussed differences between the claimed technology and the cited references and possible directions for claim amendments. No agreement was reached.

3. Prior and Concurrent Judicial Proceedings

To Applicant's knowledge, there are no prior or concurrent judicial proceedings involving U.S. Patent No. 9,189,828.

4. Objections

The reissue oath/declaration filed with this application was objected because neither it nor the Application Data Sheet (ADS) supplies the mailing address where inventor Fabrizio Santini customarily receives mail. Applicant is supplying a corrected ADS with inventor Fabrizio Santini's mailing address and therefore submits that this objection should be withdrawn.

5. Rejections under 35 U.S.C. § 112

Claims 1–57 have been rejected as indefinite. These claims are being canceled, rendering these rejections moot.

Claims 58–69 (relabeled above as claims 21–32) have also been rejected as indefinite.

Originally filed independent claim 58 (now claim 21) recites, among other things, "shifting priority from the user interaction stream to the computational stream" and "shifting the

priority from the computational stream to the user interaction stream." According to page 6 of the Office Action, this claim is indefinite because it is allegedly unclear what the term "priority" refers to or who or what is shifting.

As indicated above, this claim is being amended to recite "shifting control of data exchange between the user interaction stream and the computational stream" instead of "shifting priority." Applicant respectfully submits that this is clear to a person of skill in the art and thus claim 21 is definite so the rejections of claims 21–32 should be withdrawn.

6. Double Patenting

Claims 1–57 were rejected for statutory double patenting over claims 1–57 of U.S. Patent No. RE48,438. These claims are being canceled, rendering these rejections moot.

7. Rejections Under 35 U.S.C. § 103

Applicant respectfully requests withdrawal of the rejections under 35 U.S.C. § 103 for at least the following reasons.

7.1 Claims 21–25 and 27–30

In pages 8–12 of the Office Action, claims 21–25 and 27–30 (formerly claims 58–62 and 64–67) were rejected as unpatentable over US 7,219,085 B2 to Buck in view of US 7,477,256 B1 to Johnson and US 7,525,547 B1 to Diard. According to the Office Action, Buck discloses executing both a user interaction stream and a computational stream. The Office Action states further that it would have been obvious to modify Buck's computational stream to control data exchange between the user interaction stream and the computational stream as allegedly taught by Johnson. And the Office Action states further The Office's motivation for these modifications is that they would have been simple substitutions of known techniques from "acceptable" pieces of prior art.

Applicant respectfully disagrees with this rejection for several reasons, including Buck's failure to disclose user interaction and computational streams as in claim 21 and the Office's failure to identify the steps of "shifting priority" anywhere in the prior art. Nevertheless, solely to advance prosecution, Applicant is amending claim 21 to recite "queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network; and executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream."

Applicant respectfully submits that the proposed combination of Buck, Johnson, and Diard does not queue a user command or executing the user command during execution of the computations representing the artificial neural network at a time determined by the computational stream as in amended claim 21. Thus, amended claim 21 is patentable over Buck, Johnson, and Diard. Claims 22–24 and 27–30 depend from amended claim 21 and are therefore patentable over Buck, Johnson, and Diard for at least the same reasons.

7.2 Claims 26, 31, and 32

In pages 12–15 of the Office Action, claims 26, 31, and 32 (formerly claims 63, 68, and 69) were rejected as unpatentable over Buck in view of Johnson, Diard, and US 2006/0129506 A1 to Edelman.

7.3 Claim 33

Independent claim 33 (formerly claim 70) recites "[a] system for executing computations representing an artificial neural network." This system includes a camera, first and second memory partitions, at least one central processing unit (CPU) to execute a user interaction stream, and a processing unit to execute a computational stream. The processing unit executes computations while the camera acquires input data.

Claim 33 was rejected as unpatentable over Buck in view of Johnson, Diard, and Edelman. According to page 15 of the Office Action, "[t]he limitations of claim 70 [now claim 33] are rejected in a corresponding manner to claims 58–69 [21–32]." The references are complex and the limitations of claim 33 are different than those of claims 21–32, so this statement does not provide the clear explanation of the pertinence of each reference required by 37 C.F.R. § 1.104(c)(2).

Nevertheless, solely to advance prosecution, Applicant is amending claim 33 to recite "a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during the execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption." Applicant respectfully submits that the proposed combination of Buck, Johnson, Diard, and Edelman does not include a controller that queues user interactions received by a user interaction stream during execution of computations representing the artificial neural network for performance at times selected to avoid data corruption as in amended claim 33. Thus, amended claim 33 is patentable over Buck, Johnson, Diard, and Edelman.

CONCLUSION

It is respectfully believed that all of the rejections set forth in the Office Action have been addressed. However, the absence of a reply to a specific rejection, objection, or comment set forth in the Office Action does not signify agreement with or concession of that rejection, objection, or comment. In addition, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Furthermore, nothing in this paper should be construed as an intent to concede any issue with regard to any claim.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper and to credit any overpayment, to Deposit Account No. 60-1876. If an extension of time is required to make this reply timely, please charge the appropriate extension of time fee under 37 C.F.R. § 1.17 to Deposit Account No. 60-1876 if not already paid via EFS.

Dated: June 7, 2022

Respectfully submitted,

Smith Baluch LLP
376 Boylston St, Suite 401
Boston MA 02116

Phone: (617) 947-7280

By /Christopher Max Colice/
Christopher Max Colice
Registration No. 65634

Electronic Acknowledgement Receipt

EFS ID:	45888747
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	07-JUN-2022
Filing Date:	29-DEC-2020
Time Stamp:	19:58:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NRLA-001US04_Amendment_due_2022-06-07.pdf	259046 601493ac9465ca5d7acbdc04f95076330ce95b9d	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	10

Warnings:

Information:

Total Files Size (in bytes):	259046

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CORRECTED ADS FORM

Application Number	17136343
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Inventor Information

****If no data is shown, no data has been corrected****

	Data of Record	Updated Data
Order Number	1	
Name	Anatoli Gorchetchnikov	
Residence Information		
Residency	us-residency	
City	Newton	
State	MA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1		15 Jefferson St
Address 2		
City,State/Province, Postal Code	~~Newton MA~~	Newton MA 02458
Country	US	

	Data of Record	Updated Data
Order Number	2	
Name	Heather Marie Ames	
Residence Information		
Residency	us-residency	
City	Milton	
State	MA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	13 Myers Lane	
Address 2		
City,State/Province, Postal Code	Milton MA 02186	
Country	US	

	Data of Record	Updated Data
Order Number	3	
Name	Massimiliano Versace	
Residence Information		
Residency	us-residency	
City	Milton	
State	MA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1	13 Myers Lane	
Address 2		
City,State/Province, Postal Code	Milton MA 02186	
Country	US	

	Data of Record	Updated Data
Order Number	4	
Name	Fabrizio Santini	
Residence Information		
Residency	us-residency	
City	Jamaica Plain	
State	MA	
Country of Residence	US	
Mailing Address of Inventor		
Address 1		22 Sigourney St Unit E
Address 2		
City,State/Province, Postal Code	~~Jamaica Plain MA~~	Jamaica Plain MA 02130
Country	US	

Application Information

	Data of Record	Updated Data
Title of Invention	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	
Attorney Docket Number	NRLA-001US04	
Entity Type	Small	

Domestic Benefit/National Stage Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121,365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S. C. 119(e) or 120, and 37 CFR 1.78(a).

		Data of Record	Updated Data
	Prior Application Status		
	Application Number		
	Continuity Type		
	Prior Application Number		
	Filing Date (YYYY-MM-DD)		
	Patent Number		
	Issue Date (YYYY-MM-DD)		

Foreign Priority Information

****If no data is shown, no data has been corrected****

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

		Data of Record	Updated Data
	Application Number		
	Country		
	Filing Date		
	Access Code		

Applicant Information

****If no data is shown, no data has been corrected****
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

	Data of Record	Updated Data
Applicant Type		

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is		
Name of the Deceased or Legally Incapacitated Inventor		
Applicant is an Organization		
Name		
Organization Name		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Assignee Information including Non-Applicant Assignee Information

****If no data is shown, no data has been corrected****
Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office

	Data of Record	Updated Data
Order		
Applicant is an Organization		
Name		

Organization Name		
Mailing Address		
Address 1		
Address 2		
City,State/Province,Postal Code		
Country		
Phone Number		
Fax Number		
Email Address		

Signature

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Christopher Max Colice/	Registration Number	65634
First Name	Christopher	Last Name	Colice

Electronic Acknowledgement Receipt

EFS ID:	45888759
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	07-JUN-2022
Filing Date:	29-DEC-2020
Time Stamp:	20:03:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet to update/ correct info	CorrectedADS.pdf	141550 ab489fec099a5e8f36df5050f52dbcb3924138f0	no	7

Warnings:

Information:	
Total Files Size (in bytes):	141550

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO-2326 (04-2019)
Approved for use through 03/31/2021. OMB 0651-0043
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR REFUND

Reference # *(Patent #, Application #, Trademark Serial #, Registration #, etc.)*	**Title of Invention or Mark Information**	
17/136,343	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD	
Attorney Docket # *(if applicable)*	**Payment Date** *(mm/dd/yyyy)*	**Refund Request Amount**
NRLA-001US04	04/06/2021 and 06/24/2021	$ 2,360.00

Refund Option *(Select one)*

- ○ If approved, issue the refund to the account associated with the original payment.
- ◉ If approved, and the original payment was a check, issue the refund to deposit account # 60-1876.
- ○ If approved, and the original payment was a check, issue the refund as a U.S. Treasury check.

Reason for Refund Request *Refund requests must generally be filed within 2 years of payment date (37 CFR 1.26 and 2.209)*

- ☐ Duplicate Payment
- ☐ No Fee Due
- ☐ Office Error
- ☐ Small Entity Later Established* (*must be filed within 3 months of payment date, 37 CFR 1.28)
- ☑ Other Error in Number of Claims

Rationale *(Supporting documentation may be submitted with this form)*

Applicant filed this application as a reissue continuation with new claims and all 57 claims from US RE48438 per guidance from OPLA. As noted in the Examiner Interview Summary Record dated June 1, 2022, however, Applicant should have filed this application with the new claims and only the 20 claims of US 9,189,828. Applicant requests that the Office calculate the excess claim fees using the claims of original US Patent No. 9,189,828 and pending claims 21-41 of the present application.

Requester's Information

Company or Firm Name *(if applicable)*		
Smith Baluch LLP		
Address Line 1	**City**	**State/Region**
376 Boylston St	Boston	Massachusetts
Address Line 2 *(if applicable)*	**Country**	**Zip/Postal Code**
Suite 401	United States	02116
Email Address *(You will receive an acknowledgment of receipt only if you provide a valid email address)*	**Phone Number**	
colice@smithbaluch.com	(617) 947-7280	
Requester's Name	**Registration Number** *(if applicable)*	
Christopher Max Colice	65634	
Signature	**Date** *(mm/dd/yyyy)*	
/Christopher Max Colice/	06/08/2022	

Submit online: EFS-Web *(registered users only; select "Request for Refund" from the document description menu)*, or
Fax to: 571-273-6500, or
Mail to: Director of the U.S. Patent and Trademark Office, Attn: Refunds, 2051 Jamieson Avenue, Suite 300, Alexandria, VA 22314

Electronic Acknowledgement Receipt

EFS ID:	45909619
Application Number:	17136343
International Application Number:	
Confirmation Number:	6235
Title of Invention:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	149890
Filer:	Christopher M. Colice/Marie Spakowski
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	NRLA-001US04
Receipt Date:	08-JUN-2022
Filing Date:	29-DEC-2020
Time Stamp:	17:25:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Refund Request	NRLA-001US04_USPTO_PTO2326_Refund_Request.pdf	529322 e8959303df03f5850d6ada44a911f37774fd4e03	no	1

Warnings:

Information:	
Total Files Size (in bytes):	529322

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

United States Patent and Trademark Office

Office of the Chief Financial Officer

July 07, 2022

149890
SMITH BALUCH LLP
Attn: CHRISTOPHER COLICE
376 BOYLSTON ST,
SUITE 401
BOSTON, MA 02116

Dear Sir/Madam,

The United States Patent and Trademark Office (USPTO) has reviewed your refund request for Reference Number **17136343** - Refund Request ID **REFND-20220609-34423**. Below is the current status of your refund request assigned to the following processing area: Office of Patent Application Processing

Fee code	Decision	Decision Reason(s)	Refund Amount
2205	Dismissed	Other - see attached page(s)	$0.00

Please refer to the following page to review the detailed dismissal reason(s).

You will receive a separate decision letter for any additional fee codes assigned to other processing areas, if applicable. Decisions may be subject to change if an error is identified.

For questions related to this refund request, contact the Office of Patent Application Processing at (703) 756-1158.

Thank you,
Refund Branch

Enclosure: Refund Dismissal Reason(s)

Refund Dismissal Reason(s) for fee code 2205:

- Other - The Office cannot refund excess claim fees that were properly paid merely because the applicant cancels or amends the excess claims prior to the first Office action. No refund will be made once the fee for claims is properly paid, even though claims are later canceled.

United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Lynnell Johnson

Refund Accounting Date:07/13/2022

Effective Date	Sale Item Reference Number	Refund Total
06/24/2021	17136343	$240.00

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method	Account Number
I20227CA28043719	2201	INDEPENDENT CLAIMS IN EXCESS OF 3	$240.00		**********1006

United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Lynnell Johnson

Sale Adjustment Accounting Date:07/13/2022

Effective Date	Sale Accounting Date	Sale Item Reference Number
06/24/2021	07/13/2022	17136343

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20227CA28043719	2201	INDEPENDENT CLAIMS IN EXCESS OF 3	$240.00	

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

149890 7590 08/03/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
08/03/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@smithbaluch.com
eofficeaction@appcoll.com
smith@smithbaluch.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 17/136,343	Applicant(s) Gorchetchnikov et al.	
	Examiner WILLIAM H WOOD	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 06/07/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 21-41 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 21-41 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

For reissue applications filed before September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are "pre-AIA" provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the current provisions.

Claims 21-41 are currently pending in the application. Cancelled claims 1-20 are original claims to patent US 9,189,828 B2 and claims 21-41 are newly added.

NOTE: The most recent amendment, received 06/07/2022, properly cancels claims 1-20 and adds claims 21-41 with markings showing changes relative to the patent under reissue consistent with 37 CFR 1.173. <u>As such examination is conducted with respect to the claims as presented in the amendment of 06/07/2022.</u> Previous amendments mistakenly included claims 21-57 from a previous reissue proceeding 15/808,201 without showing changes.

Reissue

Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. US 9,189,828 B2 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Applicant is notified that any subsequent amendment to the specification and/or claims must comply with 37 CFR 1.173(b).

Objections

The reissue oath/declaration filed with this application is defective and objected to because it fails: 1) to identify the application to which it is directed (37 CFR 1.63(a)(2)); 2) to identify at least one error under 35 USC 251 (37 CFR 1.175(a)); and 3) to identify the broadened claims (MPEP 1412.03).

Claim Rejections – 35 USC § 251

Claims 21-41 are rejected under 35 U.S.C. 251 as the error statement of the oath/declaration is insufficient and must address: 1) to identify the application to which it is directed (37 CFR 1.63(a)(2)); 2) to identify at least one error under 35 USC 251 (37 CFR 1.175(a)); and 3) to identify the broadened claims (MPEP 1412.03). The Declarations received 12/29/2020 are no longer applicable as a result of the amendments of 06/07/2022. A new declaration is required.

Allowable Subject Matter

Claims 21-41 would be allowable should the other outstanding issues be resolved.

The following is a statement of reasons for the indication of allowable subject matter. The cited prior art does not teach or fairly suggest, in combination with the other claim limitations, at least the following limitations of independent claim 21: “shifting control of data exchange between the user interaction stream and the computational stream to the computational stream in response to starting execution of the computations representing the artificial neural network”; “shifting control of the data

exchange between the user interaction stream and the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network"; "queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network"; and "executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream". The cited prior art does not teach or fairly suggest, in combination with the other claim limitations, at least the following limitations of independent claim 33: "… the user interaction stream controlling transfer of the input data acquired by the camera to the first memory partition and the second memory partition during execution of the computations representing the artificial neural network"; "… the computational stream controlling transfer of the input data from the first memory partition and the second memory partition during execution of the computations representing the artificial neural network, the execution of the computations representing the artificial neural network occurring while the camera is acquiring the input data"; and "a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during the execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption."

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)272-3736 and fax number is (571)273-3736. The examiner can normally be reached on Monday-Friday 7:30am-4:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Kosowski can be reached on (571)272-3744. The Central Reexamination Unit's (CRU) fax number is (571)273-9900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see https://ppair.uspto.gov/epatent/portal/home. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William H. Wood/
Primary Examiner, CRU 3992

Conferees:

/RSD/

/ALEXANDER J KOSOWSKI/
Supervisory Patent Examiner, Art Unit 3992

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 9/5027; 2209/509	03/01/2022	/WHW/
G06T 1/20; 1/60	03/01/2022	/WHW/
G06N 3/00; 3/02; 3/04; 3/06; 3/063; 3/08; 3/10; 5/00; 7/00; 7/02; 7/04 ; 7/046; 7/06; 20/00	03/01/2022	/WHW/

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Prosecution History Review	03/01/2022	/WHW/
NPL Review	03/01/2022	/WHW/
IDS Review	03/01/2022	/WHW/
Litigation Search	03/01/2022	/WHW/
PE2E Search	03/01/2022	/WHW/
Prosecution History Review	07/27/2022	/WHW/
PE2E Search	07/27/2022	/WHW/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06T	1/20; 1/60	07/27/2022	/WHW/
G06N	20/00; 3/063	07/27/2022	/WHW/
G06F	9/5027; 2209/509	07/27/2022	/WHW/

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/01/2022	07/28/2022							
	1	✓	-							
	2	✓	-							
	3	✓	-							
	4	✓	-							
	5	✓	-							
	6	✓	-							
	7	✓	-							
	8	✓	-							
	9	✓	-							
	10	✓	-							
	11	✓	-							
	12	✓	-							
	13	✓	-							
	14	✓	-							
	15	✓	-							
	16	✓	-							
	17	✓	-							
	18	✓	-							
	19	✓	-							
	20	✓	-							
	21	✓	✓							
	22	✓	✓							
	23	✓	✓							
	24	✓	✓							
	25	✓	✓							
	26	✓	✓							
	27	✓	✓							
	28	✓	✓							
	29	✓	✓							
	30	✓	✓							
	31	✓	✓							
	32	✓	✓							
	33	✓	✓							
	34	✓	✓							
	35	✓	✓							
	36	✓	✓							
	37	✓	✓							
	38	✓	✓							
	39	✓	✓							
	40	✓	✓							
	41	✓	✓							
	42	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CLAIM		DATE								
Final	Original	03/01/2022	07/28/2022							
	43	✓								
	44	✓								
	45	✓								
	46	✓								
	47	✓								
	48	✓								
	49	✓								
	50	✓								
	51	✓								
	52	✓								
	53	✓								
	54	✓								
	55	✓								
	56	✓								
	57	✓								
	58	✓								
	59	✓								
	60	✓								
	61	✓								
	62	✓								
	63	✓								
	64	✓								
	65	✓								
	66	✓								
	67	✓								
	68	✓								
	69	✓								
	70	✓								

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L85	1715	(graphic$4 near3 processor) WITH CPU WITH block$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:22 PM
L86	64	L85 AND (artificial ADJ neural ADJ network)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:24 PM
L87	39	L86 AND stream	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:24 PM
L88	173	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/07/27 12:28 PM

NVIDIA Ex1002
Page 327 of 392

		stream) WITH (user ADJ stream)	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L89	10	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH block$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:29 PM
L90	0	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH wait$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:32 PM
L91	5	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH queue$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2022/07/27 12:32 PM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L92	1	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (interfac$4 ADJ stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:33 PM
L93	235	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH ((user OR interfac$4) near3 stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:34 PM
L94	1	L93 AND (artificial ADJ neural ADJ network)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:35 PM
L96	0	L93 AND ((graphic$4 OR GPU) near3 (transfer OR exchange) near3 (control$4 OR priviledg$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2022/07/27 12:39 PM

NVIDIA Ex1002
Page 329 of 392

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L97	47	((US-6952827-B1 OR US-7526634-B1 OR US-7525547-B1 OR US-6367122-B1 OR US-6146277-A OR US-7219085-B2 OR US-7477256-B1 OR US-5977977-A OR US-5099447-A OR US-5987443-A OR US-4994982-A OR US-5142665-A OR US-7068278-B1 OR US-7746350-B1 OR US-9349201-B1 OR US-8194085-B2 OR US-7737984-B2 OR US-7119810-B2 OR US-7522167-B1 OR US-6999603-B1).did. AND USPT.dbnm.) OR ((US-20090027383-A1 OR US-20080181081-A1 OR US-20060233525-A1 OR US-20060114254-A1 OR US-20010052123-A1 OR US-20090027402-A1 OR US-20070165035-A1 OR US-20010010034-A1 OR US-20060129506-A1 OR US-20060026358-A1 OR US-20060250417-A1 OR US-20060282855-A1 OR US-20170102950-A1 OR US-20070124363-A1 OR US-20030152288-A1 OR US-20080238917-A1 OR US-20080001957-A1 OR US-20040207618-A1 OR US-20020190994-A1 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:45 PM

NVIDIA Ex1002
Page 330 of 392

		US-20070052713-A1 OR US-20060106591-A1 OR US-20110035737-A1 OR US-20090222572-A1).did. AND PGPB.dbnm.) OR ((US-20050125369-A1 OR US-20050128206-A1).did. AND DWPI.dbnm.) OR ((WO-9316438-A1 OR WO-0227658-A2).did. AND FPRS.dbnm.)					
L98	28	L97 AND (data near2 (exchang$4 OR transfer$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:50 PM
L99	17	L98 AND (graphic$4 near3 (control$4 OR priviledg$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:51 PM
L100	12	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH ((interaction$4) near3 stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2022/07/27 01:59 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	11387	G06T1/20.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:51 PM
N2	8018	G06F9/5027.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N3	6858	G06T1/60.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N4	60171	G06N20/00.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N5	1875	G06F2209/509.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N6	8175	G06N3/063.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:53 PM
N7	0	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH CPU)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:56 PM
N8	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interaction$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:56 PM
N9	0	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interfac$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:57 PM
N10	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH user$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:57 PM
N11	0	(N1 OR N2 OR N3 OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27

		N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH queue$4)					01:58 PM
N12	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interaction$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 02:00 PM

NVIDIA Ex1002
Page 333 of 392

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/136,343	Filing Date 12/29/2020	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $240 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	10/19/2022	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 69	= 0		x $50 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 8	= 0		x $240 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/PATRICIA F LEWIS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No. NRLA-001US04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Gorchetchnikov *et al.*

Application No. 17/136,343

Filed: 2020-12-29

Confirmation No. 6235

Art Unit: 3992

Examiner: William H. Wood

Title: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

REPLY AFTER FINAL OFFICE ACTION

In response to the Final Office Action dated August 3, 2022, Applicant submits the following Amendments and/or Remarks, and respectfully requests reconsideration of the application in view thereof.

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

IN THE CLAIMS:

Set forth below in ascending order, with status identifiers, is a complete listing of all claims currently under examination. Per 37 C.F.R. § 1.173(d), matter to be omitted is enclosed is brackets and matter to be added is underlined. This listing also reflects any cancellation and/or addition of claims.

1–20. (Canceled)

21. (New, Thrice Amended) A method of executing computations representing an artificial neural network on a computer system comprising at least one central processing unit (CPU), a processing unit, a first memory partition, and a second memory partition, the method comprising:

executing, by the at least one CPU, a user interaction stream, the user interaction stream controlling transfer of inputs to the artificial neural network to the first memory partition and the second memory partition;

executing, by the processing unit, a computational stream, the computational stream controlling data exchange between the user interaction stream and the computational stream during execution of the computations representing the artificial neural network;

shifting control of a data exchange between the user interaction stream and the computational stream to the computational stream in response to starting execution of the computations representing the artificial neural network;

shifting control of the data exchange between the user interaction stream and the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network;

queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network; and

executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream.

22. (New, Amended) The method of claim 21, wherein the user interaction stream controls the data exchange between the user interaction stream and the computational stream outside of execution of the computations representing the artificial neural network.

23. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of computational elements of the computations representing the artificial neural network.

24. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of parameters of the computations representing the artificial neural network.

25. (New) The method of claim 21, wherein executing the user interaction stream comprises:
controlling setting and editing of parameters of the inputs to the artificial neural network.

26. (New) The method of claim 21, wherein executing the user interaction stream comprises:
specifying an output to be saved to disk and/or displayed on a screen.

27. (New) The method of claim 21, wherein executing the user interaction stream comprises:
parsing elements to be used in the computations representing the artificial neural network.

28. (New) The method of claim 27, wherein the processing unit comprises a graphics processing unit (GPU) and executing the user interaction stream further comprises:
converting the elements into GPU programs.

29. (New) The method of claim 28, wherein executing the user interaction stream comprises:
compiling the GPU programs.

30. (New) The method of claim 29, wherein executing the user interaction stream comprises:
transferring the GPU programs to the second memory partition.

31. (New) The method of claim 21, further comprising:
executing, by the at least one CPU, a data output stream, the data output stream controlling transfer of outputs of the computations representing the artificial neural network to disk.

32. (New) The method of claim 21, further comprising:
generating the inputs with a video camera during execution of the computations.

33. (New, Amended) A system for executing computations representing an artificial neural network, the system comprising:

a camera to acquire input data for the artificial neural network;

a first memory partition;

a second memory partition;

at least one central processing unit (CPU), operably coupled to the camera, the first memory partition, and the second memory partition, to execute a user interaction stream, the user interaction stream controlling transfer of the input data acquired by the camera to the first memory partition and the second memory partition during execution of the computations representing the artificial neural network;

a processing unit, operably coupled to the first memory partition, the second memory partition, and the at least one CPU, to execute a computational stream, the computational stream controlling transfer of the input data from the first memory partition and the second memory partition during execution of the computations representing the artificial neural network, the execution of the computations representing the artificial neural network occurring while the camera is acquiring the input data; and

a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during the execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption.

34. (New) The system of claim 33, wherein the user interactions cause interruption of the computations representing the artificial neural network.

35. (New) The system of claim 33, wherein the user interactions cause a change in inputs to the artificial neural network.

36. (New) The system of claim 33, wherein the user interactions cause a change in display properties of an output of the computations representing the artificial neural network.

37. (New, Amended) The system of claim 33, wherein the controller is configured to request the input data during the execution of the computations representing the artificial neural network.

38. (New) The method of claim 21, wherein the user command causes interruption of the computations representing the artificial neural network.

39. (New) The method of claim 21, wherein the user command causes a change in the inputs to the artificial neural network.

40. (New) The method of claim 21, wherein the user command causes a change in display properties of an output of the computations representing the artificial neural network.

41. (New) The method of claim 21, wherein, during execution of the computations representing the artificial neural network, the computational stream controls the data exchange between the user interaction stream and the computational stream by requesting the inputs to the artificial neural network.

REMARKS

In response to the Office Action dated August 3, 2022, in the above-identified application, Applicant respectfully requests reconsideration. All of the issues raised in the Office Action have been carefully considered and are addressed in this response. The application as now presented is believed to be in allowable condition.

1. Status of the Claims and Summary of Amendments

Upon entry of this response, claims 21–41 will be pending in this application, of which claims 21 and 33 are independent claims.

Claims 21, 22, and 37 are being amended for clarity.

2. Summary of Telephone Interview with Examiner

Applicant's representative Christopher Max Colice thanks Examiner Wood for discussing appropriate wording for replacement reissue declarations on October 5, 2022, and for reviewing proposed wording for replacement reissue declarations on October 6, 2022. Applicant thanks Examiner Wood for his helpful suggestions and has incorporated them into the enclosed replacement reissue declarations.

3. Prior and Concurrent Judicial Proceedings

To Applicant's knowledge, there are no prior or concurrent judicial proceedings involving U.S. Patent No. 9,189,828.

4. Objection

The reissue declaration filed with this application was objected to under 35 U.S.C. 251 as the error statement allegedly does not identify the application to which it is directed, an error under 35 U.S.C. 251, or the broadened claims. Applicant respectfully submits that the enclosed declarations identify the correct application, a suitable error being corrected, and a broadened claim.

5. Allowable Subject Matter

Applicant thanks Examiner Wood for indicating that claims 21–41 would be allowable should the objection to the reissue declarations be overcome.

CONCLUSION

It is respectfully believed that all of the rejections set forth in the Office Action have been addressed. However, the absence of a reply to a specific rejection, objection, or comment set forth in the Office Action does not signify agreement with or concession of that rejection, objection, or comment. In addition, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Furthermore, nothing in this paper should be construed as an intent to concede any issue with regard to any claim.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Director is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper and to credit any overpayment, to Deposit Account No. 60-1876. If an extension of time is required to make this reply timely, please charge the appropriate extension of time fee under 37 C.F.R. § 1.17 to Deposit Account No. 60-1876 if not already paid via EFS.

Dated: October 19, 2022

Respectfully submitted,

Smith Baluch LLP
376 Boylston St, Suite 401
Boston MA 02116

Phone: (617) 947-7280

By /Christopher Max Colice/
Christopher Max Colice
Registration No. 65634

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/136,343	**10/19/2022 04:32:35 PM ET**	**NRLA-001US04**

Title of Invention

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Application Information

APPLICATION TYPE	Utility - Reissue	PATENT #	-
CONFIRMATION #	6235	FILED BY	Christopher Colice
PATENT CENTER #	61080711	FILING DATE	12/29/2020
CUSTOMER #	149890	FIRST NAMED INVENTOR	Anatoli Gorchetchnikov
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Christopher Colice

Documents

TOTAL DOCUMENTS: 7

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
NRLA-001US04_Reply_after_Final_due_2022-11-03.pdf		7	-	226 KB
NRLA-001US04_Reply_after_Final_due_2022-11-03-TRREISS.pdf	(1-1)	1	Transmittal Reissue Application	145 KB
NRLA-001US04_Reply_after_Final_due_2022-11-03-CLM.pdf	(2-5)	4	Claims	183 KB
NRLA-001US04_Reply_after_Final	(6-7)	2	Applicant Arguments/Remarks Made in an Amendment	134 KB

_due_2022-11-03-REM.pdf			
NRLA-001US04_Replacement_Reissue_Declaration_-_Versace_-_SIGNED.pdf	3	Reissue Oath or Declaration	358 KB
NRLA-001US04_Replacement_Reissue_Declaration_-_Gorchetchnikov_SIGNED.pdf	2	Reissue Oath or Declaration	940 KB
NRLA-001US04_Replacement_Reissue_Declaration_-_Ames_SIGNED.pdf	2	Reissue Oath or Declaration	961 KB
NRLA-001US04_Replacement_Reissue_Declaration_-_Santini_SIGNED.pdf	3	Reissue Oath or Declaration	2376 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
NRLA-001US04_Reply_after_Final_due_2022-11-03.pdf	E9CA5C2D607E0ABE5DBED95937163D4B959A27483F4B3A6D11685EFC83E38621FC12C9E2F10A563B8E3F5716D89CA32E3755A0FF15B7EE41FEA15683473CF471
NRLA-001US04_Reply_after_Final_due_2022-11-03-TRREISS.pdf	D4D2FFAE8C6FC06ACB8E92A0176C7CE81555B125FD292D56422F089E0899225E944D181A497D8388BC2E7F64EC68D8BA655E136742538126A9A3D8E2D73701D1
NRLA-001US04_Reply_after_Final_due_2022-11-03-CLM.pdf	A84EB4851BD203285D3A18817C240701D582FD4E9E60CAD419143CB5ABAAAE654678AF1D1EE734FA6983E043A01B2494C6186F8C8FABE796911B08B69C6F3215

NRLA-001US04_Reply_after_Final_due_2022-11-03-REM.pdf	E4523F1CCDFCC80D072E58750747D71CC0A5E8A73A74C349A086B9239D10CFFA6DCBE72DBE60E8C5B88388D3D3505553DB0E57F5439D2169246280B35FBE9A81
NRLA-001US04_Replacement_Reissue_Declaration_-_Versace_-_SIGNED.pdf	E24656B670D58536E39BE8AEA3DA789C9138FCF676BDEBD7205D379A971010A03D02AAA77D491CB8BBC7DD2A786DC531299B669A8007DDEBA1112F3447DD6495
NRLA-001US04_Replacement_Reissue_Declaration_-_Gorchetchnikov_SIGNED.pdf	8ABA15BC46AF9BE9B84A59AD907FA1FF7786D53656DB2CF6AD8D970FB1266A76DFC3D9772E0C68AE03972E78771A97FF7BA5D72C33899D5ED0D1517A0DDC6073
NRLA-001US04_Replacement_Reissue_Declaration_-_Ames_SIGNED.pdf	7E95F972E5822C77C73C2D0897D9A8CF18D09C8E150C61058F208A65DD72A4A6BE9A4144368AF72EA2FE6A836DD912CEED08F00FAB5B9993BE5F9C264BEAEB27
NRLA-001US04_Replacement_Reissue_Declaration_-_Santini_SIGNED.pdf	454AF4B6E40E6D78934D2FDCC12C93FDE1E12CF03B0FD54ACAF515E71C8249A15AADE368972F0DC36070023D3385E89B457E579411A0CD40E039D7FAA6545B49

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/05 (06-12)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US04

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted 11/17/2015 and for which a reissue patent is sought on the invention titled GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD,

the specification of which

☐ is attached hereto.

☑ was filed on 12/29/2020 as reissue application number 17/136,343.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because Applicant erred by claiming less than it had a right to claim. Claim 21, for example, corrects this error because it does not recite "an accelerator" as in claim 12.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0033. Public burden for this form is estimated to average 12 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
NRLA-001US04

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Anatoli Gorchetchnikov

Inventor's Signature		Date (Optional) October 11, 2022
Residence: City Newton	State MA	Country US

Mailing Address

15 Jefferson St

City	State	Zip	Country
Newton	MA	02458	US

Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

PTO/AIA/05 (06-12)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US04

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted 11/17/2015 and for which a reissue patent is sought on the invention titled GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD,

the specification of which

☐ is attached hereto.

☑ was filed on 12/29/2020 as reissue application number 17/136,343.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because Applicant erred by claiming less than it had a right to claim. Claim 21, for example, corrects this error because it does not recite "an accelerator" as in claim 12.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0033. Public burden for this form is estimated to average 12 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
NRLA-001US04

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Heather Marie Ames

Inventor's Signature		Date (Optional)	
Residence: City Milton	State MA	Country US	
Mailing Address 13 Myers Lane			
City Milton	State MA	Zip 02186	Country US

[ ] Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

PTO/AIA/05 (06-12)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US04

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted 11/17/2015 and for which a reissue patent is sought on the invention titled GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD,

the specification of which

☐ is attached hereto.

☑ was filed on 12/29/2020 as reissue application number 17/136,343.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because Applicant erred by claiming less than it had a right to claim. Claim 21, for example, corrects this error because it does not recite "an accelerator" as in claim 12.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0033. Public burden for this form is estimated to average 12 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
NRLA-001US04

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Massimiliano Versace

Inventor's Signature		Date (Optional) 10/11/2022
Residence: City Milton	State MA	Country US
Mailing Address 13 Myers Lane		
City Milton	State MA	Zip 02186	Country US

☐ Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013). https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Additional Uses

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

Doc Code: REIS.DECL
Document Description: Reissue Oath or Declaration

PTO/AIA/05 (06-12)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) NRLA-001US04

I hereby declare that:
Each inventor's residence and mailing address are stated below next to their name.
I believe I am the original inventor or an original joint inventor of the subject matter which is described and claimed in patent number 9,189,828, granted 11/17/2015 and for which a reissue patent is sought on the invention titled GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD,

the specification of which

☐ is attached hereto.

☑ was filed on 12/29/2020 as reissue application number 17/136,343.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, a claim that the application seeks to broaden must be identified:

Reissue is requested because Applicant erred by claiming less than it had a right to claim. Claim 21, for example, corrects this error because it does not recite "an accelerator" as in claim 12.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0033. Public burden for this form is estimated to average 12 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email informationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/05 (06-12)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional)
NRLA-001US04

Note: To appoint a power of attorney, use form PTO/AIA/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 149890

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

Legal name of sole or first inventor (*E.g.*, Given Name (first and middle (if any) and Family Name or Surname)

Fabrizio Santini

Inventor's Signature		Date (Optional) 10/12/2022	
Residence: City Jamaica Plain	State MA	Country US	
Mailing Address 22 Sigourney St., Unit E			
City Jamaica Plain	State MA	Zip 02130	Country US

Additional joint inventors are named on the _____ supplemental sheet(s) PTO/AIA/10 attached hereto.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013). https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Additional Uses

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/136,343	12/29/2020	3992	5160	NRLA-001US04	67	7

CONFIRMATION NO. 6235

CORRECTED FILING RECEIPT

OC000000136854741

149890
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

Date Mailed: 10/21/2022

Receipt is acknowledged of this reissue patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

Applicant(s)

Neurala, Inc., Boston, MA, Assignee (with 37 CFR 1.172 Interest);

Assignment For Published Patent Application

Neurala, Inc., Boston, MA
Neurala, Inc., Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 149890

Domestic Priority data as claimed by applicant

This application is a REI of 14/147,015 01/03/2014 PAT 9189828
and is a CON of 15/808,201 11/09/2017 PAT RE48438
which is a REI of 14/147,015 01/03/2014 PAT 9189828
which is a CON of 11/860,254 09/24/2007 PAT 8648867
which claims benefit of 60/826,892 09/25/2006

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/05/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/136,343**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

149890 7590 11/08/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
3992	

DATE MAILED: 11/08/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

TITLE OF INVENTION: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/08/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

149890 7590 11/08/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

TITLE OF INVENTION: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/08/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
WOOD, WILLIAM H	3992	345-531000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04	6235

149890 7590 11/08/2022
SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
3992	

DATE MAILED: 11/08/2022

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/136,343	Applicant(s) Gorchetchnikov et al.	
	Examiner WILLIAM H WOOD	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 10/19/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 21-41 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/William H. Wood/
Primary Examiner, Art Unit 3992

The present application is being examined under the pre-AIA first to invent provisions.

NOTICE OF ALLOWANCE

For reissue applications filed before September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are "pre-AIA" provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the current provisions.

Claims 21-41 are allowed.

Claims 21-41 are currently pending in the application. Cancelled claims 1-20 are original claims to patent US 9,189,828 B2 and claims 21-41 are newly added.

NOTE: The most recent amendment, received 10/19/2022, properly cancels claims 1-20 and adds claims 21-41 with markings showing changes relative to the patent under reissue consistent with 37 CFR 1.173. As such examination is conducted with respect to the claims as presented in the amendment of 10/19/2022. Previous amendments mistakenly included claims 21-57 from a previous reissue proceeding 15/808,201 without showing changes.

Reissue

Applicant is reminded of the continuing obligation under 37 CFR 1.178(b), to timely apprise the Office of any prior or concurrent proceeding in which Patent No. US 9,189,828 B2 is or was involved. These proceedings would include interferences, reissues, reexaminations, and litigation.

Applicant is further reminded of the continuing obligation under 37 CFR 1.56, to timely apprise the Office of any information which is material to patentability of the claims under consideration in this reissue application.

These obligations rest with each individual associated with the filing and prosecution of this application for reissue. See also MPEP §§ 1404, 1442.01 and 1442.04.

Applicant is notified that any subsequent amendment to the specification and/or claims must comply with 37 CFR 1.173(b).

Response to Arguments

Patent Owner's arguments, filed 10/19/2022, have been fully considered and are persuasive. The objection and rejection of the declarations have been withdrawn in view of the declarations submitted 10/19/2022 (in accordance with the discussions between the Patent Owner and the Examiner on October 5-6, 2022).

Allowable Subject Matter

Claims 21-41 are allowed (including minor changes of amendment of 10/19/2022).

The following is an examiner's statement of reasons for allowance. The cited prior art does not teach or fairly suggest, in combination with the other claim limitations, at least the following limitations of independent claim 21: "shifting control of a data exchange between the user interaction stream and the computational stream to the computational stream in response to starting execution of the computations representing the artificial neural network"; "shifting control of the data exchange between the user interaction stream and the computational stream to the user interaction stream in response to completion or interruption of the computations representing the artificial neural network"; "queueing a user command received by the user interaction stream during execution of the computations representing the artificial neural network"; and "executing the user command during execution of the computations representing the artificial neural network at times determined by the computational stream". The cited prior art does not teach or fairly suggest, in combination with the

other claim limitations, at least the following limitations of independent claim 33: "... the user interaction stream controlling transfer of the input data acquired by the camera to the first memory partition and the second memory partition during execution of the computations representing the artificial neural network"; "... the computational stream controlling transfer of the input data from the first memory partition and the second memory partition during execution of the computations representing the artificial neural network, the execution of the computations representing the artificial neural network occurring while the camera is acquiring the input data"; and "a controller, operably coupled to the at least one CPU and the processing unit, to queue user interactions received by the user interaction stream during the execution of the computations representing the artificial neural network for performance at times selected to avoid data corruption."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)272-3736 and fax number is (571)273-3736. The examiner can normally be reached on Monday-Friday 7:30am-4:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Kosowski can be reached on (571)272-3744. The Central Reexamination Unit's (CRU) fax number is (571)273-9900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see https://ppair-my.uspto.gov/pair/PrivatePair. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William H. Wood/
Primary Examiner, CRU 3992

Conferees:

/PENG KE/
Primary Examiner, Art Unit 3992

/ALEXANDER J KOSOWSKI/
Supervisory Patent Examiner, Art Unit 3992

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CPC

Symbol					Type	Version
G06T	/	1	/	20	F	2013-01-01
G06T	/	1	/	60	I	2013-01-01
G06F	/	9	/	5027	I	2013-01-01
G06N	/	3	/	063	A	2013-01-01
G06F	/	2209	/	509	A	2013-01-01
G06N	/	20	/	00	A	2019-01-01

CPC Combination Sets

Symbol					Type	Set	Ranking	Version
	/		/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 21	
/William H. Wood/ Primary Examiner, Art Unit 3992 (Primary Examiner)	27 July 2022 (Date)	O.G. Print Claim(s) 21	O.G. Print Figure 4

U.S. Patent and Trademark Office

Part of Paper No.: 20220727

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06T	/	1	/	60

NON-CLAIMED				
G06F	/	9	/	50
G06T	/	1	/	20

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 21	
/William H. Wood/ Primary Examiner, Art Unit 3992 (Primary Examiner) (Date) 27 July 2022	O.G. Print Claim(s) 21	O.G. Print Figure 4

U.S. Patent and Trademark Office Part of Paper No.: 20220727

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28		37						
	2		11		20		29		38						
	3		12		21		30		39						
	4		13		22		31		40						
	5		14		23		32		41						
	6		15		24		33								
	7		16		25		34								
	8		17		26		35								
	9		18		27		36								

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 21	
/William H. Wood/ Primary Examiner, Art Unit 3992 (Primary Examiner)	27 July 2022 (Date)	O.G. Print Claim(s) 21	O.G. Print Figure 4

U.S. Patent and Trademark Office

Part of Paper No.: 20220727

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/01/2022	07/27/2022							
	1	✓	-							
	2	✓	-							
	3	✓	-							
	4	✓	-							
	5	✓	-							
	6	✓	-							
	7	✓	-							
	8	✓	-							
	9	✓	-							
	10	✓	-							
	11	✓	-							
	12	✓	-							
	13	✓	-							
	14	✓	-							
	15	✓	-							
	16	✓	-							
	17	✓	-							
	18	✓	-							
	19	✓	-							
	20	✓	-							
	21	✓	=							
	22	✓	=							
	23	✓	=							
	24	✓	=							
	25	✓	=							
	26	✓	=							
	27	✓	=							
	28	✓	=							
	29	✓	=							
	30	✓	=							
	31	✓	=							
	32	✓	=							
	33	✓	=							
	34	✓	=							
	35	✓	=							
	36	✓	=							
	37	✓	=							
	38	✓	=							
	39	✓	=							
	40	✓	=							
	41	✓	=							
	42	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CLAIM		DATE								
Final	Original	03/01/2022	07/27/2022							
	43	✓								
	44	✓								
	45	✓								
	46	✓								
	47	✓								
	48	✓								
	49	✓								
	50	✓								
	51	✓								
	52	✓								
	53	✓								
	54	✓								
	55	✓								
	56	✓								
	57	✓								
	58	✓								
	59	✓								
	60	✓								
	61	✓								
	62	✓								
	63	✓								
	64	✓								
	65	✓								
	66	✓								
	67	✓								
	68	✓								
	69	✓								
	70	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 9/5027; 2209/509	03/01/2022	/WHW/
G06T 1/20; 1/60	03/01/2022	/WHW/
G06N 3/00; 3/02; 3/04; 3/06; 3/063; 3/08; 3/10; 5/00; 7/00; 7/02; 7/04 ; 7/046; 7/06; 20/00	03/01/2022	/WHW/

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Prosecution History Review	03/01/2022	/WHW/
NPL Review	03/01/2022	/WHW/
IDS Review	03/01/2022	/WHW/
Litigation Search	03/01/2022	/WHW/
PE2E Search	03/01/2022	/WHW/
Prosecution History Review	07/27/2022	/WHW/
PE2E Search	07/27/2022	/WHW/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/136,343	Gorchetchnikov et al.
	Examiner	**Art Unit**
	WILLIAM H WOOD	3992

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06T	1/20; 1/60	07/27/2022	/WHW/
G06N	20/00; 3/063	07/27/2022	/WHW/
G06F	9/5027; 2209/509	07/27/2022	/WHW/

United States Patent And Trademark Office **Reissue Terminal Disclaimer Review Form**	**Application No.** 17/136,343	**Art Unit** 3992
	Examiner WILLIAM H WOOD	**AIA Status** No

Original Patent Number of Patent to be Reissued is: 9,189,828	**The Maintenance fee status is:** ◉ up to date ○ not up to date (Consult with SPRS)

Is there a terminal disclaimer filed and accepted during the prosecution of (i) the current reissue application, (ii) the underlying patent, and/or (iii) reexamination proceeding(s) of the underlying patent?

○ NO
◉ YES (Complete the rest of the form)

The reissue patent is subject to Terminal Disclaimer(s) that was/were:

☐ filed and accepted (DISQ or DISQ.E.FILE) during the prosecution of the current reissue application. (Enter terminal disclaimer(s) filing date(s) below).

1. _____ 2. _____ 3. _____

The underlying patent of the current reissue application is subject to Terminal DIsclaimer(s) that was/were:

☑ accepted (DISQ or DISQ.E.FILE) and of record in the prosecution of the underlying patent and/or reexamination procceeding(s) of the underlying patent. (Enter application/control no(s) and terminal disclaimer(s) filing date(s) below).

1. 14/147,015 30 June 2015 2. 15/808,201 09 November 2017 3. 15/808,201 17 September 2020

Bibliographic Data

Application No: 17/136,343

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /William H. Wood/ [ ]

Examiner's Signature Initials

Title: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/29/2020	345	3992	NRLA-001US04
RULE			

APPLICANTS

Neurala, Inc., Boston, MA, UNITED STATES

INVENTORS

Anatoli Gorchetchnikov, Newton, MA, UNITED STATES

Heather Marie Ames, Milton, MA, UNITED STATES

Massimiliano Versace, Milton, MA, UNITED STATES

Fabrizio Santini, Jamaica Plain, MA, UNITED STATES

CONTINUING DATA

This application is a CON of 15808201 11/09/2017 PAT RE48438

15808201 is a REI of 14147015 01/03/2014 PAT 9189828

This application is a REI of 14147015 01/03/2014 PAT 9189828

14147015 is a CON of 11860254 09/24/2007 PAT 8648867

11860254 has PRO of 60826892 09/25/2006

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

01/05/2021

**** SMALL ENTITY ****

STATE OR COUNTRY

UNITED STATES

ADDRESS

SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

UNITED STATES

FILING FEE RECEIVED

$160

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L85	1715	(graphic$4 near3 processor) WITH CPU WITH block$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:22 PM
L86	64	L85 AND (artificial ADJ neural ADJ network)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:24 PM
L87	39	L86 AND stream	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:24 PM
L88	173	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2022/07/27 12:28 PM

NVIDIA Ex1002
Page 378 of 392

		stream) WITH (user ADJ stream)	CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L89	10	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH block$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:29 PM
L90	0	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH wait$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:32 PM
L91	5	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (user ADJ stream) WITH queue$4	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2022/07/27 12:32 PM

			VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L92	1	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH (interfac$4 ADJ stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:33 PM
L93	235	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH ((user OR interfac$4) near3 stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:34 PM
L94	1	L93 AND (artificial ADJ neural ADJ network)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:35 PM
L96	0	L93 AND ((graphic$4 OR GPU) near3 (transfer OR exchange) near3 (control$4 OR priviledg$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2022/07/27 12:39 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L97	47	((US-6952827-B1 OR US-7526634-B1 OR US-7525547-B1 OR US-6367122-B1 OR US-6146277-A OR US-7219085-B2 OR US-7477256-B1 OR US-5977977-A OR US-5099447-A OR US-5987443-A OR US-4994982-A OR US-5142665-A OR US-7068278-B1 OR US-7746350-B1 OR US-9349201-B1 OR US-8194085-B2 OR US-7737984-B2 OR US-7119810-B2 OR US-7522167-B1 OR US-6999603-B1).did. AND USPT.dbnm.) OR ((US-20090027383-A1 OR US-20080181081-A1 OR US-20060233525-A1 OR US-20060114254-A1 OR US-20010052123-A1 OR US-20090027402-A1 OR US-20070165035-A1 OR US-20010010034-A1 OR US-20060129506-A1 OR US-20060026358-A1 OR US-20060250417-A1 OR US-20060282855-A1 OR US-20170102950-A1 OR US-20070124363-A1 OR US-20030152288-A1 OR US-20080238917-A1 OR US-20080001957-A1 OR US-20040207618-A1 OR US-20020190994-A1 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:45 PM

NVIDIA Ex1002
Page 381 of 392

		US-20070052713-A1 OR US-20060106591-A1 OR US-20110035737-A1 OR US-20090222572-A1).did. AND PGPB.dbnm.) OR ((US-20050125369-A1 OR US-20050128206-A1).did. AND DWPI.dbnm.) OR ((WO-9316438-A1 OR WO-0227658-A2).did. AND FPRS.dbnm.)					
L98	28	L97 AND (data near2 (exchang$4 OR transfer$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:50 PM
L99	17	L98 AND (graphic$4 near3 (control$4 OR priviledg$4))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/07/27 12:51 PM
L100	12	((comput$4 OR computat$6 OR calculat$4 OR neural OR intellige$6) near3 stream) WITH ((interaction$4) near3 stream) WITH (queue$4 OR wait$4 OR block$4)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2022/07/27 01:59 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	11387	G06T1/20.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:51 PM
N2	8018	G06F9/5027.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N3	6858	G06T1/60.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N4	60171	G06N20/00.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N5	1875	G06F2209/509.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:52 PM
N6	8175	G06N3/063.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:53 PM
N7	0	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH CPU)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:56 PM
N8	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interaction$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:56 PM
N9	0	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interfac$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:57 PM
N10	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH user$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 01:57 PM
N11	0	(N1 OR N2 OR N3 OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27

		N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH queue$4)					01:58 PM
N12	5	(N1 OR N2 OR N3 OR N4 OR N5 OR N6) AND (neural ADJ network) AND (stream WITH (data ADJ (exchang$4 OR transfer$4)) WITH computation$4 WITH interaction$4)	(US-PGPUB; USPAT)	OR	ON	ON	2022/07/27 02:00 PM

NVIDIA Ex1002
Page 384 of 392

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/136,343	**02/08/2023 12:35:52 PM ET**	**NRLA-001US04**

Title of Invention

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Application Information

APPLICATION TYPE	Utility - Reissue	PATENT #	-
CONFIRMATION #	6235	FILED BY	Christopher Colice
PATENT CENTER #	61562924	FILING DATE	12/29/2020
CUSTOMER #	149890	FIRST NAMED INVENTOR	Anatoli Gorchetchnikov
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
web85b.pdf	3	Issue Fee Payment (PTO-85B)	62 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
web85b.pdf	173FF234648E5D8807536E0327EF1FA2FAAFE18BECA2035AF63A907D526FA339A830B6E8E3BB20553D8F59843CEF6E22EB40475A30F2B9F87814AF9931480C6C

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/136,343	02/08/2023 12:35:52 PM ET	NRLA-001US04

Title of Invention

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Application Information

APPLICATION TYPE	Utility - Reissue	PATENT #	-
CONFIRMATION #	6235	FILED BY	Christopher Colice
PATENT CENTER #	61562924	AUTHORIZED BY	-
CUSTOMER #	149890	FILING DATE	12/29/2020
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Anatoli Gorchetchnikov

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1006	E202328C36124528	Christopher Colice

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2511	REISSUE ISSUE FEE	600.00	1	600.00
			TOTAL AMOUNT:	$600.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage

submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ISSUE FEE TRANSMITTAL FORM

APPLICATION #	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET #
17136343	12/29/2020	Anatoli Gorchetchnikov	NRLA-001US04

Title of Invention

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Application Information

APPLICATION TYPE	Reissue	DATE DUE	02/08/2023
CONFIRMATION #	6235	ISSUE FEE DUE	$ 600
EXAMINER	WILLIAM WOOD	PUBLICATION DUE	$ 0
GROUP ART UNIT	3992	TOTAL FEES DUE	$600
CLASS - SUBCLASS	345/531000	PREV. PAID FEE	$ 0
ENTITY STATUS	Small		

1. CHANGE OF CORRESPONDENCE ADDRESS AND/OR INDICATION OF FEE ADDRESS (37 CFR 1.33 & 1.363)

Correspondence Address

CURRENT ADDRESS

Maintenance Fee Address

CURRENT ADDRESS

☐ Change of correspondence address requested,system generated AIA/122-PC form attached

☐ Fee address indication requested, system generatedSB/47-PC form attached

2. ENTITY STATUS

Change in Entity Status

NEW STATUS

3. THE FOLLOWING FEES ARE SUBMITTED

- [x] Issue Fee
- [x] Publication Fee
- [ ] Advance Order - # of copies:

4. FEE AUTHORIZATION

- [ ] I authorize USPTO to apply my previously paid issue fee to the current fees due
- [ ] The Director is herby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number:
- [x] If in addition to the payment of the issue fee amount submitted with this form, there are any discrepencies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number: 601876

5. FIRM AND/OR ATTORNEY NAMES TO BE PRINTED

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

Smith Baluch LLP

6. ASSIGNEE NAME(S) AND RESIDENCE DATA TO BE PRINTED

NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a susbstitute for filing an assignment.

Neurala, Inc.	Boston, MA UNITED STATES	Organization

Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also

certify that this Fee(s) Transmittal form is being transmitted to the USPTO via Patent Center on the date indicated below.

Signature	Name	Registration #	Date
/Christopher Max Colice/	Christopher Colice	65634	02/08/2023

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/136,343	03/14/2023	RE49461	NRLA-001US04	6235

149890 7590 02/22/2023

SMITH BALUCH LLP
376 BOYLSTON ST
STE 401
BOSTON, MA 02116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Extension or Adjustment under 35 U.S.C. 154 (b)

A reissue patent is for "the unexpired part of the term of the original patent." See 35 U.S.C. 251. Accordingly, the above-identified reissue application is not eligible for Patent Term Extension or Adjustment under 35 U.S.C. 154(b).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Anatoli Gorchetchnikov, Newton, MA;
Heather Marie Ames, Milton, MA;
Massimiliano Versace, Milton, MA;
Fabrizio Santini, Jamaica Plain, MA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Neurala, Inc., Boston, MA, Assignee (with 37 CFR 1.172 Interest);

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.