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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 09/17/2015
ZILKA-KOTAB, PC- NVID
1155 N. 1st St.
Suite 105
SAN JOSE, CA 95112

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
09/17/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zk-uspto@zilkakotab.com

Notice of Abandonment	Application No.	Applicant(s)
	13/335,850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R. MYERS	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *04 March 2015*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☒ A proposed reply was received on *5/4/15*, but it does not constitute a proper reply under 37 CFR 1.113 to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) if this is utility or plant application, a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. Note that RCEs are not permitted in design applications.)
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☐ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record or other party authorized under 37 CFR 1.33(b). See 37 CFR 1.138(b).

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

/PAUL R MYERS/
Primary Examiner, Art Unit 2185

Petitions to revive under 37 CFR 1.137, or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

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13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 06/03/2015
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EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
06/03/2015	ELECTRONIC

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zk-uspto@zilkakotab.com

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	13/335,850	PELLETIER, SEAN MICHAEL	
	Examiner	Art Unit	
	PAUL R. MYERS	2185	

All participants (applicant, applicant's representative, PTO personnel):

(1) *PAUL R. MYERS*. (3)_____.

(2) *Stepanie L. Winner*. (4)_____.

Date of Interview: *18 May 2015*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner called to inform applicant he was doing an advisory action as per the after final piolet program 2.0 .

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/PAUL R MYERS/ Primary Examiner, Art Unit 2185	

Advisory Action Before the Filing of an Appeal Brief	**Application No.** *13/335,850*	**Applicant(s)** PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	**Art Unit** 2185	**AIA (First Inventor to File) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 04 May 2015 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☒ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance;

(2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection. The current period for reply expires months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.

Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANT'S FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because

a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);

b) ☐ They raise the issue of new matter (see NOTE below);

c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): (a) ☒ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: Li teaches a security code stored on a USB device..

13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

14. ☒ Other: Note the attached interview summery abd AFCP2.0 decision.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: .

Claim(s) objected to: .

Claim(s) rejected: .

Claim(s) withdrawn from consideration: .

/PAUL R MYERS/
Primary Examiner, Art Unit 2185

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	13/335,850	PELLETIER, SEAN MICHAEL	
	Examiner	Art Unit	
	PAUL R. MYERS	2185	

All participants (applicant, applicant's representative, PTO personnel):

(1) *PAUL R. MYERS*. (3)_____.

(2) *Stepanie L. Winner*. (4)_____.

Date of Interview: *18 May 2015*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: _____.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Examiner called to inform applicant he was doing an advisory action as per the after final piolet program 2.0 .

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/PAUL R MYERS/ Primary Examiner, Art Unit 2185	

AFCP 2.0 Decision	Application No.	Applicant(s)
	13/335,850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R. MYERS	2185

This is in response to the After Final Consideration Pilot request filed 04 May 2012.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other:

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☒ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action. See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other:

   Examiner Note: Please attach an interview summary when necessary as described above.

Neural AI, LLC, Exhibit 2019
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IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC

AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended): A method, comprising:

receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

performing one or more operations on the input data, utilizing the computation module and with assistance of a discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

providing output data from the computation module, utilizing the chassis.

2-3. (Cancelled).

4. (Original): The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5-6. (Cancelled).

7. (Previously Presented): The method of claim 1, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. (Original): The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. (Original): The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. (Original): The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. (Original): The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. (Original): The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. (Previously Presented): The method of claim 1, wherein a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module.

14-17. (Cancelled).

18. (Currently Amended): A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data <u>stored</u> within <u>a data storage element of</u> the computation module is secured by the locking platform<u>, and</u>

the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

performing one or more operations on the input data, utilizing the computation module and with assistance of a discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

code for providing output data from the computation module, utilizing the chassis.

19. (Currently Amended): A system, comprising:

a chassis; and

a computation module removably coupled to an external portion the chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

wherein the computation module receives input data utilizing the chassis, performs one or more operations on the input data with assistance of a discrete graphics processing unit (GPU) of the chassis, and provides output data, utilizing the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module.

20. (Original): The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

21-22. (Cancelled).

23. (Previously Presented): The method of claim 1, wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis.

24. (Previously Presented): The method of claim 1, wherein the discrete GPU of the chassis assists the computation module with performing the one or more operations on the input data by offloading at least one processing duty from the computation module.

25. (Previously Presented): The method of claim 1, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

26. (Previously Presented): The computer program product embodied on a computer readable medium of claim 18, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

27. (Previously Presented): The system of claim 19, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

28. (Previously Presented): The method of claim 1, wherein the chassis is an automotive chassis.

29. (Previously Presented): The method of claim 1, wherein the chassis comprises a display configured to display the output data received from the computation module through the first connection.

30. (Cancelled).

31. (Previously Presented): The computer program product embodied on a computer readable medium of claim 18, wherein the chassis is an automotive chassis.

32. (Previously Presented): The system of claim 19, wherein the chassis is an automotive chassis.

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
NVIDP679/SC-09-0042-US1	13/335,850	December 22, 2011

First Named Inventor:	Title:
Sean Michael Pelletier	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:

- Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
- The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
  - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
  - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
    - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
    - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	/Stephanie L. Winner/	Date	May 4, 2015
Name (Print/Typed)	Stephanie L. Winner	Practitioner Registration No.	52,371

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ * Total of 1 forms are submitted.

Neural AI, LLC, Exhibit 2019
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IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sean Michael Pelletier Application No.: 13/335,850 Filed: 12/22/2011 For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Confirmation No.: 2112 Examiner: Myers, Paul R. Art Unit: 2112 Atty. Docket No.: NVIDP679/SC-09-0042-US1 Date: 05/04/2015

AMENDMENT D

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner:

In response to the Final Office Action dated March, 04, 2015, please enter the following amendments believed to place the claims in condition for allowance.

Applicant would also like to participate in the After Final Consideration Pilot (AFCP) Program 2.0 to expedite prosecution in the instant application. Applicant requests the Examiner to contact the undersigned if the present claim amendments merit an Office Action other than a Notice of Allowance.

AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended): A method, comprising:

receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

performing one or more operations on the input data, utilizing the computation module and with assistance of a discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

providing output data from the computation module, utilizing the chassis.

2-3. (Cancelled).

4. (Original): The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5-6. (Cancelled).

7. (Previously Presented): The method of claim 1, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. (Original): The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. (Original): The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. (Original): The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. (Original): The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. (Original): The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. (Previously Presented): The method of claim 1, wherein a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module.

14-17. (Cancelled).

18. (Currently Amended): A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data <u>stored</u> within <u>a data storage element of</u> the computation module is secured by the locking platform<u>, and</u>

the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

performing one or more operations on the input data, utilizing the computation module and with assistance of a discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

code for providing output data from the computation module, utilizing the chassis.

19. (Currently Amended): A system, comprising:

a chassis; and

a computation module removably coupled to an external portion the chassis, wherein the computation module is coupled the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate;

wherein the computation module receives input data utilizing the chassis, performs one or more operations on the input data with assistance of a discrete graphics processing unit (GPU) of the chassis, and provides output data, utilizing the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module.

20. (Original): The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

21-22. (Cancelled).

23. (Previously Presented): The method of claim 1, wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis.

24. (Previously Presented): The method of claim 1, wherein the discrete GPU of the chassis assists the computation module with performing the one or more operations on the input data by offloading at least one processing duty from the computation module.

25. (Previously Presented): The method of claim 1, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

26. (Previously Presented): The computer program product embodied on a computer readable medium of claim 18, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

27. (Previously Presented): The system of claim 19, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

28. (Previously Presented): The method of claim 1, wherein the chassis is an automotive chassis.

29. (Previously Presented): The method of claim 1, wherein the chassis comprises a display configured to display the output data received from the computation module through the first connection.

30. (Cancelled).

31. (Previously Presented): The computer program product embodied on a computer readable medium of claim 18, wherein the chassis is an automotive chassis.

32. (Previously Presented): The system of claim 19, wherein the chassis is an automotive chassis.

REMARKS

The Examiner has rejected Claims 1, 7-13, 18-20, 23-24, and 29 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* (U.S. Patent No. 5,689,654) in view of *Kong* (U.S. Patent No. 7,325,086) and *Dewa* (U.S. Patent No. 6,425,040). The Examiner has rejected Claim 4 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong* and *Dewa*, and further in view of *Utz* (U.S. Patent No. 8,131,904). The Examiner has rejected Claims 25-27 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong*, and further in view of *Kinoshita* (U.S. Patent No. 6,516,374). The Examiner has rejected Claims 28, 31, and 32 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong* and *Dewa*, and further in view of *McConnell* (U.S. Patent No. 6,608,399). The Examiner has rejected Claim 30 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong* and *Dewa*, and further in view of *Li* (U.S. Patent Application Publication No. 2007/006290). Applicant traverses these rejections.

Applicant respectfully disagrees with the rejections, especially in view of the amendments made hereinabove to each of the independent claims. In response to the Final Office Action mailed on March 4, 2015, Applicant hereby amends the claims as set forth above for consideration as part of the After Final Consideration Pilot (AFCP) Program 2.0. The Applicant submits that these amendments do not introduce any new subject matter and are supported at least by paragraphs [0022] and [0041] and Figure 4 of the originally-filed specification. In light of these amendments, the cited references, either alone or in combination, fail to teach or suggest all of the claim limitations in the amended independent claims.

Rejections under pre-AIA 35 U.S.C. § 103(a)

Specifically, Applicant has amended each of independent claims 1, 18, and 19. Claim 30 is cancelled. No combination of the cited references teaches or suggests the limitations recited in each of the independent claims. Thus, amended claims 1, 18, and 19, and claims dependent thereon are in condition for allowance.

As amended each of the independent claims recites the following limitations:

"*data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate*" (see this or similar, but not necessarily identical, language in the independent claims).

Kikinis discloses a notebook computer framework and μPDA that is coupled to the notebook computer framework. The Examiner equates the notebook computer framework (172, 61, or 1011) taught by *Kikinis* with the claimed chassis and the μPDA (10/1061) taught by *Kikinis* with the claimed computation module. See the *Final Office Action* at page 3. *Kikinis* discloses operation of a security mechanism, specifically teaching that the "EEPROM 31 holds one or more codes installed at the point of manufacturing to provide security for information transfer between a host and a μPDA. The purpose is to control access by a host to the memory contents of a μPDA, so each μPDA may be configured to an individual." Additionally, *Kikinis* teaches that the security mechanism is executed by the μPDA and that a bootstrap program is loaded from the memory 13 into a RAM 68 within the microcontroller 11 to perform the security matching. The microcontroller 11 then waits for a password received from the host computer via the host interface 14. See *Kikinis* at column 12, lines 26-54 and Figure 7. Therefore, execution of the security mechanism is performed by the μPDA and relies on accessing the memory 13 and/or RAM 68 of the μPDA. *Kikinis* is clear that the μPDA operates to perform execution of the security mechanism.

Kikinis fails to disclose that a locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate, as now required by claim 1. *Kikinis* is also clear that the memory 13 is not secured because the memory 13 is accessed by the μPDA during execution of the security mechanism. Therefore, *Kikinis* also fails to disclose data stored within a data storage element of the computation module is secured by the locking platform, as also now required by claim 1.

Li teaches a USB device having a descriptor and a computer that compares the descriptor with a security key to control access of data stored in the computer. See *Li* at paragraphs [0014]-[0015] and [0018]. *Li* is clear that the computer searches all attached USB devices and accesses the descriptor of a chosen USB device to form the security key and prevent access of data stored in the computer by the USB device. However, the teachings of *Li* contradict the operation of the security mechanism taught by *Kikinis*. Therefore, Applicant respectfully submits that the combination of the security mechanism implemented in the μPDA to control access to data stored in the μPDA by the host as discussed in *Kikinis* with the security model implemented by the computer to prevent access of data stored in the computer by the USB device of *Li* is improper.

Kikinis specifically teaches that the "EEPROM 31 holds one or more codes installed at the point of manufacturing to provide security for information transfer between a host and a μPDA. The purpose is to control access by a host to the memory contents of a μPDA, so each μPDA may be configured to an individual." (emphasis added) Additionally, *Kikinis* teaches that the security mechanism is executed by the μPDA and that a bootstrap program is loaded from the memory 13 into a RAM 68 within the microcontroller 11 to perform the security matching. The microcontroller 11 then waits for a password received from the host computer via the host interface 14. See *Kikinis* at column 12, lines 26-54 and Figure 7. Therefore, execution of the security mechanism is performed by the μPDA and the host computer is prevented from accessing the memory of the μPDA until the password is received from the host computer.

Again, Applicant respectfully submits that the combination of the security mechanism implemented in the μPDA to control access to data stored in the μPDA by the host as discussed in *Kikinis* with the security model implemented by the computer to prevent access of data stored in the computer by the USB device of *Li* is improper. Applicant respectfully submits that such a combination would not control access by a host to the memory contents of a μPDA as taught by *Kikinis*. Controlling access to the memory contents of the μPDA is important to *Kikinis* and the removal thereof would frustrate the purpose of the system discussed therein.

MPEP § 2143.01(V) states "[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)" (emphasis added). "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)" (emphasis added).

Modifying the teachings of *Kikinis* so that the notebook computer framework searches all attached μPDA devices and accesses the codes of a chosen μPDA, as taught by *Li*, requires that the notebook computer framework access at least the EEPROM memory of the μPDA. In contrast, the technique disclosed by *Kikinis* contains the security mechanism entirely within the μPDA and unsecured access of the memory contents of the μPDA by the notebook computer framework is prevented. As such, Applicant respectfully submits that a person of ordinary skill in the art would not have a reason to combine these features and that, furthermore, the combination thereof would frustrate the principle of operation of *Kikinis*. For these additional reasons, Applicant respectfully requests that the rejection be withdrawn.

Additionally, the Examiner relies on prior art references *Kong*, *Dewa*, *Utz*, *McConnell*, and *Kinoshita* for teaching limitations not taught or suggested by *Kikinis*. See the *Final Office Action* at pages 3-7. No combination of the cited prior art references teaches or suggests the limitations recited in each of the independent claims. Therefore, *Kong*, *Dewa*, *Utz*, *McConnell*, and *Kinoshita* fail to cure the deficiencies of *Kikinis*.

As the aforementioned illustrates, the cited references, alone or in combination, do not teach or suggest the limitations that data stored within a data storage element of the computation module is secured by the locking platform, and the locking platform requires a software key contained within a universal serial bus (USB) device connected to the second connector for the computation module to operate. Thus, the cited references

cannot render amended claim 1 obvious. Therefore, Applicant submits that claim 1, and all claims dependent thereon, are now in condition for allowance.

Furthermore, independent claims 18 and 19 have been amended to include limitations similar to amended claim 1. Applicant submits that claims 18 and 19, as well as all claims dependent thereon, are also in condition for allowance for at least the same reasons as set forth above in conjunction with the discussion of amended claim 1.

Li is clear that the computer accesses data on the USB device during execution of the security model. In particular, the computer searches all attached USB devices and accesses the descriptor of a chosen USB device to form the security key. This operation contradicts the plain language of claim 1 which requires that data within the computation module is secured by the locking platform. The security model taught by *Li* secures data within the computer instead of securing data within the USB device.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at Stephanie@zilkakotab.com or may leave a message at (408) 971-2573. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP679).

Respectfully submitted,
Zilka-Kotab, PC

/Stephanie L. Winner/

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Electronic Acknowledgement Receipt

EFS ID:	22252369
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Stephanie Winner/Justin Bocchino
Filer Authorized By:	Stephanie Winner
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	04-MAY-2015
Filing Date:	22-DEC-2011
Time Stamp:	21:58:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NVIDP679_SC-09-0042-US1_AFCP_AmendFOA_05-04-2015.pdf	243047 6e73bf405abbd9f279d0128142b76324caf36a5a	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	After Final Consideration Program Request	2	2
	Response After Final Action	3	3
	Claims	4	8
	Applicant Arguments/Remarks Made in an Amendment	9	13

Warnings:

Information:

Total Files Size (in bytes):	243047

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AMENDMENT TRANSMITTAL LETTER

Docket No.
NVIDP679/SC-09-0042-US1

Application No.	Filing Date	Examiner	Art Unit
13/335,850	December 22, 2011	P. R. Myers	2185

Applicant(s): Sean Michael Pelletier

Invention: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	21	- 23 =	0	x	
Independent Claims	3	- 3 =	0	x	
Multiple Dependent Claims (check if applicable) ☐					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

[x] Large Entity ☐ Small Entity

[x] No additional fee is required for this amendment.

☐ Please charge Deposit Account No. _____ in the amount of $ _____ .

☐ A check in the amount of $ _____ to cover the filing fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge and credit Deposit Account No. 50-1351 as described below. A duplicate copy of this sheet is enclosed.

- [x] Credit any overpayment.
- [x] Charge any additional filing or application processing fees required under 37 C.F.R. § 1.16 and 1.17.

/Stephanie L. Winner/ Dated: May 4, 2015

Stephanie L. Winner
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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/335,850	12/22/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

05/04/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 21	Minus	** 23	= 0	x $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/BRENDA HARRISON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 03/04/2015
ZILKA-KOTAB, PC- NVID
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SAN JOSE, CA 95112

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
03/04/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zk-uspto@zilkakotab.com

Office Action Summary	Application No. 13/335,850	Applicant(s) PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/12/15.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1,4,7-13,18-20 and 23-32 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) 1,4, 7-13,18-20,23-32 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

2. Applicant's arguments with respect to claims 1, 4, 7-13, 18-20, 23-32 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

In regards to applicants argument regarding the newly added claim limitations: The locking mechanism of Kikinis et al is totally mechanical. Kikinis et al does not expressly teach a second (electrical) connector. The newly added claim language states "a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data within the computation module is secured by the locking platform;". Kikinis et al teaches a mechanical connector including 2 latch pins dedicated to locking the computational module, and the data is secured by the locking platform. . The examiner however notes it is clear from applicants specification that this second connector includes pins upon which signals travel and not simply a physical lock/latch pin. Therefore several references are cited that teach electrical lock signals that travel across pins from one device to another to cause the devices to lock together. For example PN 6,425,040 to Dewa et al teaches plural connectors (a PCI connector, an I2C connector, and another connection upon which the signals (DOCPWON dock power on and WOLEN Wake on LAN enable) are transmitted that control the lock mechanism. It would have been obvious to have electrical control of the locking mechanism of Kikinis et al because this would have allowed the μPDA to confirm electrical isolation before disconnecting. Dewa et al teaches the first and second connector integrated into a single connector. The

examiner notes that each and every pin is a separate connection and the may be grouped together or in plural groups as a simple matter of choice.

Claim Rejections - 35 USC § 103

3. Claims 1, 7-13, 18-20, 23-24, 29 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 and Dewa et al PN 6,425,040.

In regards to claims 1, 8, 10, 18, 19, 24: Kikinis et al teaches a method, comprising: receiving input data at a computation module (10 or 1061), utilizing a chassis (172, 61 or 1011) removably coupled to the computation module (10/1061), wherein the computation module is coupled to a video display controller of the chassis (1091 or 1301(a)); Kikinis et al teaches a first connector including a predetermined number of PINs (1033) dedicated to a bi-directional communication of display data; Kikinis et al teaches a mechanical locking mechanism that secures data within the computational module; performing one or more operations on the data, utilizing the computation module (10/1061 "in situ" Column 11 lines 36-50) and with assistance of the video display controller of the chassis (the video display controller 1091 displays the data of the Unit 1061); and providing output data from the computation module, utilizing the chassis (1072,61 or 1011). Kikinis et al does not use the words "Graphics processing unit or teach the claimed shared graphics processing. Kong et al teaches GPU's on expansion cards wherein the graphics processing is shared by the discrete GPU on the first card and another GPU on another card based on scalability logic within both the GPU cards. It would have been obvious to have the host include a GPU in its video display controller that shares the graphics processing with the

GPU of the computation module because this would have increased performance. Kikinis does not teach but not a second electrical connector including a predetermined number of pins dedicated to a locking platform of the computational module. Dewa et al teaches a first connector PCI dedicated to bidirectional communication of data via a predetermined number of pins and a second connector (DOCPWON, WOLEN) including a predetermined number of pins dedicated to a locking platform of the computational module, and data within the computational module is secured by the locking platform.

In regards to claim 7: Kikinis teaches the locking being hardware.

In regards to claim 9: Kikinis teaches the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met (Figure 7).

In regards to claims 11-13: Kikinis teaches the computation module supplements one or more elements of the chassis during the performing of the one or more operations (Column 13 lines 15-22).

In regards to claim 20: Kikinis et al teaches memory (RAM).

In regards to claim 23: Kikinis teaches the connection may be either parallel or serial Kikinis et al does not teach packetized data. Official notice is taken that packetized data is a standard in serial, Also becoming common in parallel. It would have been obvious to packetize the data because this is a standard.

In regards to claim 29: Kikinis et al teaches a display displaying the data of the μPDA.

4. Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086, and Dewa et al PN 6,425,040 as applied to claim 1 above, and further in view of Utz et al PN 8,131,904.

In regards to claim 4: Kikinis et al teaches the function unit described above. Kikinis et al does not state that it can be implemented as a SOC. Utz et al teaches a SOC function module connected to a system. It would have been obvious to implement Kikinis et al's function module(s) as SOC's because this would have allowed for smaller units.

5. Claims 25-27 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 and Dewa et al PN 6,425,040 as applied to claim 1 above, and further in view of Kinoshita et al PN 6,516374.

In regards to claims 25-27: Kong et al teaches the connection may be PCI Express which is a hot plug standard. Kikinis et al teaches the μPDA having a battery and contemplates the interface may be a PCI mode that is "being developed by Intel corporation". While both references contemplate a hot plug standard neither expressly teaches using hot plugging/unplugging feature of the standard. Kinoshita et al expressly teaches "hot undocking of the portable computer from the expansion unit can be performed". It would have been obvious to allow hot undocking because this would have removed any requirement to power down the μPDA undocking then powering back up the μPDA when the user wants the μPDA instantly still on.

6. Claims 28,31,32 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 and Dewa et al PN 6,425,040 as applied to claim 1 above, and further in view of McConnell et al PN 6,608,399.

In regards to claims 28, 31, 32: Kikinis teaches the chassis being a laptop or a Kiosk but does not teach the docking station chassis may be automotive. McConnell et al teaches automotive docking stations. All the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

7. Claim 30 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 and Dewa et al PN 6,425,040 as applied to claim 1 above, and further in view of Li PN 2007/0006290.

In regards to claim 30. Kikinis et al teaches security code but does not teach it being stored on a USB device. Li teaches a user security code may be stored on a plugged in USB device. It would have been obvious for a security code to be stored on a USB device because this would have only allowed an authorized person the use the device while not having to remember a long security code.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL R. MYERS whose telephone number is (571)272-3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL R MYERS
Primary Examiner
Art Unit 2111

/PAUL R MYERS/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 13/335,850	Applicant(s)/Patent Under Reexamination PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,394,552 A	02-1995	Shirota, Hironao	713/323
*	B	US-5,555,491 A	09-1996	Tao, Adam M.	361/679.43
*	C	US-5,664,118 A	09-1997	Nishigaki et al.	710/304
*	D	US-5,926,627 A	07-1999	Sugimura, Hideo	710/303
*	E	US-5,991,839 A	11-1999	Ninomiya, Ryoji	710/303
*	F	US-6,119,184 A	09-2000	Takahama, Shinichiro	710/303
*	G	US-6,209,105 B1	03-2001	Hamamoto, Akihiko	713/300
*	H	US-6,425,040 B1	07-2002	Dewa et al.	710/303
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*	J	US-6,608,399 B2	08-2003	McConnell et al.	307/10.1
*	K	US-6,718,425 B1	04-2004	Pajakowski et al.	710/315
*	L	US-7,236,863 B2	06-2007	LaPorte et al.	701/36
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

CPC- SEARCHED

Symbol	Date	Examiner
east searched	1/10/14	PRM
east searched	8/7/14	PRM
east searched	2/26/15	PRM

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner
G06F9/5061 G09G5/363 G06T1/00 G09G2360/06	8/5/14	PRM

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
710	301-304	9/9/13	PRM
710	301-304	8/6/14	PRM

SEARCH NOTES

Search Notes	Date	Examiner

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/09/2013	01/10/2014	08/07/2014	02/26/2015					
	1	✓	✓	✓	✓					
	2	✓	✓	-	-					
	3	✓	-	-	-					
	4	✓	✓	✓	✓					
	5	✓	✓	-	-					
	6	✓	✓	✓	-					
	7	✓	✓	✓	✓					
	8	✓	✓	✓	✓					
	9	✓	✓	✓	✓					
	10	✓	✓	✓	✓					
	11	✓	✓	✓	✓					
	12	✓	✓	✓	✓					
	13	✓	✓	✓	✓					
	14	✓	✓	-	-					
	15	✓	✓	✓	-					
	16	✓	✓	✓	-					
	17	✓	✓	✓	-					
	18	✓	✓	✓	✓					
	19	✓	✓	✓	✓					
	20	✓	✓	✓	✓					
	21		✓	✓	-					
	22		✓	-	-					
	23		✓	✓	✓					
	24		✓	✓	✓					
	25			✓	✓					
	26			✓	✓					
	27			✓	✓					
	28				✓					
	29				✓					
	30				✓					
	31				✓					
	32				✓					

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sean Michael Pelletier Application No.: 13/335,850 Filed: 12/22/2011 For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Confirmation No.: 2112 Examiner: Myers, Paul R. Art Unit: 2111 Atty. Docket No.: NVIDP679/SC-09-0042-US1 Date: 02/12/2015

AMENDMENT C

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner:

In response to the Office Action dated August, 12, 2014, please enter the following amendments believed to place the claims in condition for allowance.

AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended) A method, comprising:

receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled ~~to a discrete graphics processing unit (GPU) of~~ the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data within the computation module is secured by the locking platform;

performing one or more operations on the input data, utilizing the computation module and with assistance of a~~the~~ discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

providing output data from the computation module, utilizing the chassis.

2-3. (Cancelled).

4. (Original) The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5-6. (Cancelled).

7. (Currently Amended) The method of claim [[6]]1, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. (Original) The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. (Original) The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. (Original) The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. (Original) The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. (Original) The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. (Previously Presented) The method of claim 1, wherein a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module.

14-17. (Cancelled).

18. (Currently Amended) A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module removably coupled to an external portion of a chassis, wherein the computation module is coupled ~~to a discrete graphics processing unit (GPU) of~~ the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking

platform of the computation module, and data within the computation module is secured by the locking platform;

performing one or more operations on the input data, utilizing the computation module and with assistance of a~~the~~ discrete graphics processing unit (GPU) of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

code for providing output data from the computation module, utilizing the chassis.

19. (Currently Amended) A system, comprising:

a chassis; and

a computation module removably coupled to an external portion the chassis, wherein the computation module is coupled ~~to a discrete graphics processing unit (GPU) of~~ the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and data within the computation module is secured by the locking platform;

wherein the computation module receives input data utilizing the chassis, performs one or more operations on the input data with assistance of a~~the~~ discrete graphics processing unit (GPU) of the chassis, and provides output data, utilizing the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module.

20. (Original) The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

21-22. (Cancelled).

23. (Previously Presented) The method of claim 1, wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis.

24. (Currently Amended) The method of claim 1, wherein the discrete GPU of the chassis assists the computation module with performing the one or more operations on the input data by offloading at least one processing duty from the computation module.

25. (Previously Presented) The method of claim 1, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

26. (Previously Presented) The computer program product embodied on a computer readable medium of claim 18, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

27[[5]]. (Currently Amended) The system of claim 19, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

28. (New): The method of claim 1, wherein the chassis is an automotive chassis.

29. (New): The method of claim 1, wherein the chassis comprises a display configured to display the output data received from the computation module through the first connection.

30. (New): The method of claim 1, wherein the locking platform requires a key contained within a universal serial bus (USB) device for the computation module to operate.

31. (New): The computer program product embodied on a computer readable medium of claim 18, wherein the chassis is an automotive chassis.

32. (New): The system of claim 19, wherein the chassis is an automotive chassis.

REMARKS

The Examiner has rejected Claims 1-3, 5-14, 16, and 18-24 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* (U.S. Patent No. 5,689,654) in view of *Kong* (U.S. Patent No. 7,325,086). The Examiner has rejected Claim 4 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong*, and further in view of *Utz* (U.S. Patent No. 8,131,904). The Examiner has rejected Claim 15 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong*, and further in view of *Li* (U.S. Patent Application Publication No. 2007/006290). The Examiner has rejected Claims 25, 26, and 27 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over *Kikinis* in view of *Kong*, and further in view of *Kinoshita* (U.S. Patent No. 6,516,374). Applicant traverses these rejections.

Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to each of the independent claims. Specifically, Applicant has amended each of independent claims 1, 18, and 19. Claims 6, 15-17, and 21 are cancelled. New claims 28-31 are added. The amendments are supported by paragraphs [0017], [0019], [0037], [0039], and [0048] and Figure 4 of the application, as originally filed, and therefore, the amendments do not introduce new matter. No combination of the cited references teaches or suggests the limitations recited in each of the independent claims. Thus, amended claims 1, 18, and 19, and claims dependent thereon are in condition for allowance.

As amended each of the independent claims recites the following limitations:

"*the computation module is coupled to the chassis through a* <u>*first connector*</u> *including a predetermined number of pins dedicated to a bi-directional display connection and a* <u>*second connector*</u> *including a predetermined number of pins dedicated to a locking platform of the computation module, and data within the computation module is secured by the locking platform*" (see this or similar, but not necessarily identical, language in the independent claims).

Kikinis teaches a notebook computer framework and μPDA that is coupled to the notebook computer framework. The Examiner equates the notebook computer framework (172, 61, or 1011) taught by *Kikinis* with the claimed chassis and the μPDA (10/1061) taught by *Kikinis* with the claimed computation module. See the *Office Action* at page 4. *Kikinis* discloses a host interface 14 that couples the notebook computer framework to the μPDA. See *Kikinis* at column 12, lines 11-17 and Figures 3, 5, and 6. *Kikinis* specifically discloses "a pin configuration (not shown) in connector 14 dedicated to signalling that a module is docked." See *Kikinis* at column 12, lines 18-22. *Kikinis* fails to teach or suggest that the host interface 14 provides a display connection between the μPDA and the notebook computer framework. *Kikinis* does disclose that the μPDA includes an LCD display 25 that is coupled to a touch-sensitive input 27 and the microcontroller CPU 11. See *Kikinis* at Figures 2 and 4. However, *Kikinis* is silent regarding any pins dedicated to a bi-directional display connection, as now required by amended claim 1.

Kikinis is also silent regarding any pins dedicated to a locking platform, as also now required by amended claim 1. *Kikinis* discloses dedicated communication lines between EEPROM 31 and microcontroller 11 for providing data and program security. See *Kikinis* at column 8, line 59 – column 9, line 6. However, the dedicated communication lines are within the μPDA and are not coupled to the host interface 14.

Kikinis fails to teach or suggest that the computation module is coupled to the chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module, and that data within the computation module is secured by the locking platform, as now required by amended independent claim 1. Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Li teaches a USB device having a descriptor and a computer that compares the descriptor with a security key to control access of data stored in the computer. See *Li* at paragraphs [0014]-[0015] and [0018]. The Examiner equates the USB device with the claimed locking platform. See the *Office Action* at page 6. *Li* is clear that the computer accesses data on the USB device during execution of the security model. In particular, the computer searches all attached USB devices and accesses the descriptor of a chosen USB device to form the security key. This operation contradicts the plain language of claim 1 which requires that data within the computation module is secured by the locking platform. The security model taught by *Li* secures data within the computer instead of securing data within the USB device.

Furthermore, the teachings of *Li* contradict the operation of the security mechanism taught by *Kikinis*. *Kikinis* specifically teaches that the "EEPROM 31 holds one or more codes installed at the point of manufacturing to provide security for information transfer between a host and a μPDA. The purpose is to control access by a host to the memory contents of a μPDA, so each μPDA may be configured to an individual." (emphasis added) Additionally, *Kikinis* teaches that the security mechanism is executed by the μPDA and that a bootstrap program is loaded from the memory 13 into a RAM 68 within the microcontroller 11 to perform the security matching. The microcontroller 11 then waits for a password received from the host computer via the host interface 14. See *Kikinis* at column 12, lines 26-54 and Figure 7. Therefore, execution of the security mechanism is performed by the μPDA and relies on accessing the memory of the μPDA.

Applicant respectfully submits that the combination of the security mechanism implemented in the μPDA to control access to data stored in the μPDA by the host as discussed in *Kikinis* with the security model implemented by the computer to prevent access of data stored in the computer by the USB device of *Li* is improper. Applicant respectfully submits that such a combination would not control access by a host to the memory contents of a μPDA as taught by *Kikinis*. Controlling access to the memory contents of the μPDA is important to *Kikinis* and the removal thereof would frustrate the purpose of the system discussed therein.

MPEP § 2143.01(V) states "[i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)" (emphasis added). "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)" (emphasis added).

Modifying the teachings of *Kikinis* so that the notebook computer framework searches all attached μPDA devices and accesses the codes of a chosen μPDA, as taught by *Li*, requires that the notebook computer framework access at least the EEPROM memory of the μPDA. In contrast, the technique disclosed by *Kikinis* contains the security mechanism entirely within the μPDA and unsecured access of the memory contents of the μPDA by the notebook computer framework is prevented. As such, Applicants respectfully submit that a person of ordinary skill in the art would not have a reason to combine these features and that, furthermore, the combination thereof would frustrate the principle of operation of *Kikinis*. For these additional reasons, Applicant respectfully requests that the rejection be withdrawn.

Additionally, the Examiner relies on prior art references *Kong*, *Utz*, and *Kinoshita* for teaching limitations not taught or suggested by *Kikinis*. See the *Office Action* at pages 4-7. No combination of the cited prior art references teaches or suggests the limitations recited in each of the independent claims. Therefore, *Kong*, *Utz*, and *Kinoshita* fail to cure the deficiencies of *Kikinis*.

As the aforementioned illustrates, the cited references, alone or in combination, do not teach or suggest a computation module that is coupled to a chassis through a first connector including a predetermined number of pins dedicated to a bi-directional display connection and a second connector including a predetermined number of pins dedicated to a locking platform of the computation module and that data within the computation module is secured by the locking platform. Thus, the cited references cannot render

amended claim 1 obvious. Therefore, Applicant submits that claim 1, and all claims dependent thereon, are now in condition for allowance.

Furthermore, independent claims 18 and 19 have been amended to include limitations similar to amended claim 1. Applicant submits that claims 18 and 19, as well as all claims dependent thereon, are also in condition for allowance for at least the same reasons as set forth above in conjunction with the discussion of amended claim 1.

New claims 28, 31, and 32 each recite the limitations that the chassis is an automotive chassis. New claim 29 recites the limitations that the chassis comprises a display configured to display the output data received from the computation module through the first connection. New claim 30 recites the limitations that the locking platform requires a key contained within a universal serial bus (USB) device for the computation module to operate. None of the cited references teaches or suggest these limitations. Therefore, these new claims are allowable independent of their dependence on amended claims 1, 18, and 19, respectively.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at Stephanie@zilkakotab.com or may leave a message at (408) 971-2573. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP679).

Respectfully submitted,
Zilka-Kotab, PC

/Stephanie L. Winner/

Stephanie L. Winner
Registration No. 52,371

Electronic Patent Application Fee Transmittal

Application Number:	13335850
Filing Date:	22-Dec-2011
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Filer:	Stephanie Winner/Justin Bocchino
Attorney Docket Number:	NVIDP679/SC-09-0042-US1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
			Total in USD ($)	**1400**

Electronic Acknowledgement Receipt

EFS ID:	21490577
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Stephanie Winner/Justin Bocchino
Filer Authorized By:	Stephanie Winner
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	12-FEB-2015
Filing Date:	22-DEC-2011
Time Stamp:	19:47:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1400
RAM confirmation Number	5914
Deposit Account	501351
Authorized User	ZILKA, KEVIN J

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NVIDP679_AmendOA_02-12-2015.pdf	125515 328dfdb8ba847ba0bc23353daddf7267575ac5cc	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	1
Amendment/Req. Reconsideration-After Non-Final Reject	2	2
Claims	3	7
Applicant Arguments/Remarks Made in an Amendment	8	12

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31265 f26961f4e7fbf8cc284699dfa8020692fa9b0f4f	no	2

Warnings:

Information:

Total Files Size (in bytes):	156780

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2112
Sean Michael Pelletier	Examiner: Myers, Paul R.
Application No.: 13/335,850	Art Unit: 2111
Filed: 12/22/2011	Atty. Docket No.: NVIDP679/SC-09-0042-US1
For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Date: 02/12/2015

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 2233-1450

Sir:

Transmitted herewith is an amendment in the above-identified application.

☒ Applicant(s) hereby petition for a Three Month extension of time to respond to the outstanding Office Action.

☒ Applicant(s) believe that no additional Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 50-1351.

☒ If the required fees are missing or any additional fees are required to facilitate filing the enclosed response, please charge such fees or credit any overpayment to Deposit Account No. 50-1351.

Respectfully submitted,
Zilka-Kotab, PC

/Stephanie L. Winner/

Stephanie L. Winner
Registration No. 52,371

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Telephone: (408) 971-2573

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/335,850	12/22/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

02/12/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 23	= 0	x $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TAMMY L. ACREE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 08/12/2014
ZILKA-KOTAB, PC- NVID
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
08/12/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zk-uspto@zilkakotab.com

Office Action Summary	Application No. 13/335,850	Applicant(s) PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/13/14.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1,4,6-13,15-21 and 23-27 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) 1,4,6-13,15-21 and 23-27 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 5/13/14 5/15/14.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

2. Applicant's arguments filed 5/13/14 have been fully considered but they are not persuasive.

In regards to applicants argument about the claim language "graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module": Kikinis et al teaches two optional video controllers one on the chassis (1301(a)) and another on the computation module (1301). Kikinis et al however does not expressly teach shared graphics processing between the two video controllers. The examiner cited 4 references that taught video controllers include GPU's. The examiner is now specifically focusing on Kong et al PN 7,325,086. Kong et al teaches multiple (two or more) Graphics processing units each of which may be integrated (iGPU) or in expansion cards (dGPU) or any combination of iGPU's and dGPU's. Kong et al also teaches logic on the GPU's the lane controllers (51, 53, 55 and 49) that are a Scalable link interface SLI that allows shared graphics processing. Kong et al teaches "SLI technology may be used to link two video cards together by splitting the rendering load between the two cards to increase performance". Any logic that allows the two (or more) graphics processing units to share the graphics rendering is by definition scalability logic. Thus Kong et al teaches graphics processing is shared by a discrete GPU and another GPU (discrete or integrated) based on scalability logic within both the discrete GPU the other GPU. The combination therefore teaches graphics processing is shared by the

discrete GPU (dGPU) of the chassis (1301(a)) and another GPU (1301) within the computation module based on scalability logic (SLI) within both the discrete GPU (51,53) of the chassis (1301(a) and the GPU (55,49) within the computation module (1301).

The examiner is citing multiple additional references that teach the extremely common practice of having multiple graphics processing units share the rendering load.

Claim Rejections - 35 USC § 112

3. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 17, 21 and 25 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

In regards to claims 17 and 21. Claims 17 and 21 are dependent upon cancelled claim 5. For further examination purposes the examiner will assume they were meant to be dependent on claim 1.

In regards to claims 25: Applicants have numbered 2 claims 25. For further examination purposes the examiner will assume the second claim 25 should have been numbered claim 27.

Claim Rejections - 35 USC § 103

5. Claims 1-3, 5-14, 16, 18-24 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086.

In regards to claims 1, 8, 10, 18, 19, 24: Kikinis et al teaches a method, comprising: receiving input data at a computation module (10 or 1061), utilizing a chassis (172, 61 or 1011) removably coupled to the computation module (10/1061), wherein the computation module is coupled to a video display controller of the chassis (1091 or 1301(a)); performing one or more operations on the data, utilizing the computation module (10/1061 "in situ" Column 11 lines 36-50) and with assistance of the video display controller od the chassis (the video display controller 1091 displays the data of the Unit 1061); and providing output data from the computation module, utilizing the chassis (1072,61 or 1011). Kikinis et al does not use the words "Graphics processing unit or teach the claimed shared graphics processing. Kong et al teaches GPU's on expansion cards wherein the graphics processing is shared by the discrete GPU on the first card and another GPU on another card based on scalability logic within both the GPU cards. It would have been obvious to have the host include a GPU in its video display controller that shares the graphics processing with the GPU of the computation module because this would have increased performance.

In regards to claim 6: Kikinis et al teaches the computation module includes a locking platform (1031 for "latching"),

In regards to claim 7: Kikinis teaches the locking being hardware.

In regards to claim 9: Kikinis teaches the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met (Figure 7).

In regards to claims 11-13: Kikinis teaches the computation module supplements one or more elements of the chassis during the performing of the one or more operations (Column 13 lines 15-22).

In regards to claim 16: Kikinis et al teaches the computation module is placed within a cavity of the chassis and is coupled to the chassis using an internal connector located within the chassis.

In regards to claim 17: Kikinis et al teaches dedicated pins and using the "appropriate pins". Kikinis also teaches display connection, data connection, and locking/security. Kikinis however does not state that the pins are bi-directional. Official notice is taken that bi-directional pins are well known. It would have been obvious to include bi-directional pins because this would have decreased the number of pins required for the connector.

In regards to claim 20: Kikinis et al teaches memory (RAM).

In regards to claim 21: Kikinis et al teaches locking means in the chassis figures 44-47 that is controlled by a control signal. Kikinis also teaches the module having a button to unlock the module from the chassis thus there must be a pin through which this control signal travels from the module to the chassis.

In regards to claim 23: Kikinis teaches the connection may be either parallel or serial Kikinis et al does not teach packetized data. Official notice is taken that packetized data is a

standard in serial, Also becoming common in parallel. It would have been obvious to packetize the data because this is a standard.

6. Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 as applied to claim 1 above, and further in view of Utz et al PN 8,131,904.

In regards to claim 4: Kikinis et al teaches the function unit described above. Kikinis et al does not state that it can be implemented as a SOC. Utz et al teaches a SOC function module connected to a system. It would have been obvious to implement Kikinis et al's function module(s) as SOC's because this would have allowed for smaller units.

7. Claim 15 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 as applied to claim 1 above, and further in view of Li PN 2007/0006290.

In regards to claim 15. Kikinis et al teaches security code but does not teach it being stored on a USB device. Li teaches a user security code may be stored on a plugged in USB device. It would have been obvious for a security code to be stored on a USB device because this would have only allowed an authorized person the use the device while not having to remember a long security code.

8. Claims 25, 26, 27 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Kong et al PN 7,325,086 as applied to claim 1 above, and further in view of Kinoshita et al PN 6,516374.

In regards to claims 25-27: Kong et al teaches the connection may be PCI Express which is a hot plug standard. Kikinis et al teaches the µPDA having a battery and contemplates the interface may be a PCI mode that is "being developed by Intel corporation". While both references contemplate a hot plug standard neither expressly teaches using hot plugging/unplugging feature of the standard. Kinoshita et al expressly teaches "hot undocking of the portable computer from the expansion unit can be performed". It would have been obvious to allow hot undocking because this would have removed any requirement to power down the µPDA undocking then powering back up the µPDA when the user wants the µPDA instantly still on.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

PN 7,522,167 to Diard et al teaches sharing the processing between two discrete GPU's.

PN 7,768,517 to Diard et al teaches sharing the processing between two discrete GPU's.

PN 7,886,094 to Tamasi teaches sharing the processing between two discrete GPU's.

PN 8,612,652 to Tsuei et al teaches sharing the processing between two discrete GPU's.

PN 8,730,247 to Hiroi et al teaches sharing the processing between two discrete GPU's.

PN 2006/0267988 to Hussain et al teaches sharing the processing between two discrete VPU's interchangeable with GPU's.

PN 2011/0050710 to Sahowski et al teaches sharing the processing between two discrete GPU's.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL R. MYERS whose telephone number is (571)272-3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL R MYERS
Primary Examiner
Art Unit 2111

/PAUL R MYERS/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 13/335,850	Applicant(s)/Patent Under Reexamination PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,516,374 B1	02-2003	Kinoshita et al.	710/304
*	B	US-6,658,508 B1	12-2003	Reiss et al.	710/100
*	C	US-2006/0267988 A1	11-2006	Hussain et al.	345/502
*	D	US-7,146,437 B2	12-2006	Robbin et al.	710/16
*	E	US-2007/0195099 A1	08-2007	Diard et al.	345/501
*	F	US-7,522,167 B1	04-2009	Diard et al.	345/502
*	G	US-7,516,301 B1	04-2009	Moreton et al.	712/28
*	H	US-7,768,517 B2	08-2010	Diard et al.	345/502
*	I	US-7,886,094 B1	02-2011	Tamasi, Anthony Michael	710/104
*	J	US-2011/0050710 A1	03-2011	SADOWSKI et al.	345/502
*	K	US-8,233,000 B1	07-2012	Diard, Franck R.	345/502
*	L	US-8,223,159 B1	07-2012	Diard et al.	345/522
*	M	US-8,542,240 B2	09-2013	Nath, Siddhartha	345/502

FOREIGN PATENT DOCUMENTS

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	N					
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	P					
	Q					
	R					
	S					
	T					

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 13/335,850	Applicant(s)/Patent Under Reexamination PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-8,612,652 B2	12-2013	Tsuei et al.	710/62
*	B	US-8,648,867 B2	02-2014	Gorchetchnikov et al.	345/501
*	C	US-8,687,007 B2	04-2014	Nugent et al.	345/502
*	D	US-8,730,247 B2	05-2014	Hiroi et al.	345/503
	E	US-			
	F	US-			
	G	US-			
	H	US-			
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	J	US-			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2111
Examiner Name	P. R. Myers
Attorney Docket Number	NVIDP679/SC-09-0042-US1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /PRM/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13335850 13335850 - GAU: 2111
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	P. R. Myers
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

	1	Decision on Rejection from Chinese Application No. 201010141965.4, dated January 8, 2014	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

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Examiner Signature	/Paul R. Myers/	Date Considered	08/05/2014

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☐ See attached certification statement.

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Signature	/Stephanie L. Winner/	Date (YYYY-MM-DD)	2014-05-15
Name/Print	Stephanie L. Winner	Registration Number	52371

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/09/2013	01/10/2014	08/07/2014						
	1	✓	✓	✓						
	2	✓	✓	-						
	3	✓	-	-						
	4	✓	✓	✓						
	5	✓	✓	-						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						
	11	✓	✓	✓						
	12	✓	✓	✓						
	13	✓	✓	✓						
	14	✓	✓	-						
	15	✓	✓	✓						
	16	✓	✓	✓						
	17	✓	✓	✓						
	18	✓	✓	✓						
	19	✓	✓	✓						
	20	✓	✓	✓						
	21		✓	✓						
	22		✓	-						
	23		✓	✓						
	24		✓	✓						
	25			✓						
	26			✓						
	27			✓						

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2111
Examiner Name	P. R. Myers
Attorney Docket Number	NVIDP679/SC-09-0042-US1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8699218	B2	2014-04-15	Xu	
	2	6246211	B1	2001-06-12	Dalton et al.	

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100325460	A1	2010-12-23	Chen et al.	
	2	20080250179	A1	2008-10-09	Moon	

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	1							☐

/Paul R. Myers/ 08/05/2014

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Notice of Allowance from U.S. Application No. 13/083,469, dated December 13, 2013	☐
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EXAMINER SIGNATURE

Examiner Signature	/Paul R. Myers/	Date Considered	08/05/2014

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Signature	/Stephanie L. Winner/	Date (YYYY-MM-DD)	2014-05-13
Name/Print	Stephanie L. Winner	Registration Number	52371

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	Examiner	**Art Unit**
	PAUL R MYERS	2111

CPC- SEARCHED

Symbol	Date	Examiner
east searched	1/10/14	PRM
east searched	8/7/14	PRM

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner
G06F9/5061 G09G5/363 G06T1/00 G09G2360/06	8/5/14	PRM

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
710	301-304	9/9/13	PRM
710	301-304	8/6/14	PRM

SEARCH NOTES

Search Notes	Date	Examiner

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Electronic Acknowledgement Receipt

EFS ID:	19037453
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Stephanie Winner/Justin Bocchino
Filer Authorized By:	Stephanie Winner
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	15-MAY-2014
Filing Date:	22-DEC-2011
Time Stamp:	12:45:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	NVIDP679_PRC_IDS_05-15-2014.pdf	612219 06147d6c2e7459c911c514ee63f3c59eaa8edabb	no	4

Warnings:

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2	Non Patent Literature	NVIDP653CN_DecisionOnRejection_01-08-2014.pdf	511748 bf520c1e8ad2e02d1cedeb78f5be3589a20addc5	no	6

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Total Files Size (in bytes):	1123967

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/335,850	Filing Date	2011-12-22	Docket Number (if applicable)	NVIDP679/SC-09-0042-US1	Art Unit	2111
First Named Inventor	Sean Michael Pelletier			Examiner Name	P. R. Myers		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
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- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
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MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

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FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 501351

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature
☐ Applicant Signature

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Signature of Registered U.S. Patent Practitioner			
Signature	/Stephanie L. Winner/	Date (YYYY-MM-DD)	2014-05-13
Name	Stephanie L. Winner	Registration Number	52371

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The information provided by you in this form will be subject to the following routine uses:

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Sean Michael Pelletier Application No.: 13/335,850 Filed: 12/22/2011 For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Confirmation No.: 2112 Examiner: Myers, Paul R. Art Unit: 2111 Atty. Docket No.: NVIDP679/SC-09-0042-US1 Date: 05/13/2014

AMENDMENT B

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner:

In response to the Final Office Action dated 1/15/2014, please enter this request for continuing examination (RCE) submitted with the following amendments believed to place the claims in condition for allowance.

AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended) A method, comprising:

receiving input data at a computation module~~, utilizing a chassis~~ removably coupled to an external portion of a chassis~~the computation module~~, wherein the computation module is coupled to a discrete graphics processing unit (GPU) of the chassis;

performing one or more operations on the data, utilizing the computation module and with assistance of the discrete GPU of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

providing output data from the computation module, utilizing the chassis.

2-3. (Cancelled).

4. (Original) The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5. (Cancelled).

6. (Original) The method of claim 1, wherein the computation module includes a locking platform.

7. (Original) The method of claim 6, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. (Original) The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. (Original) The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. (Original) The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. (Original) The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. (Original) The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. (Previously Presented) The method of claim 1, wherein a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module.

14. (Cancelled).

15. (Original) The method of claim 1, wherein a hardware lock is implemented within the computation module, and such hardware lock requires a key contained within a universal serial bus (USB) device for the computation module to operate.

16. (Original) The method of claim 1, wherein the computation module is placed within a cavity of the chassis and is coupled to the chassis using an internal connector located within the chassis.

17. (Original) The method of claim 5, wherein a predetermined number of pins of the connector are dedicated to a bi-directional display connection, a predetermined number of pins of the connector are dedicated to a bi-directional data connection, and a predetermined number of pins of the connector are dedicated to a locking platform of the computation module.

18. (Currently Amended) A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module~~, utilizing a chassis~~ removably coupled to an external portion of a chassis~~the computation module~~, wherein the computation module is coupled to a discrete graphics processing unit (GPU) of the chassis;

code for performing one or more operations on the data, utilizing the computation module and with assistance of the discrete GPU of the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module; and

code for providing output data from the computation module, utilizing the chassis.

19. (Currently Amended) A system, comprising:

a chassis; and

a computation module removably coupled to an external portion the chassis, wherein the computation module is coupled to a discrete graphics processing unit (GPU) of the chassis;

wherein the computation module receives input data utilizing the chassis, performs one or more operations on the data with assistance of the GPU of the chassis, and provides output data, utilizing the chassis, wherein the one or more operations include the graphics processing, and the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability

logic within both the discrete GPU of the chassis and the GPU within the computation module.

20. (Original) The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

21. (Previously Presented) The method of claim 5, wherein a predetermined number of pins of the connector are dedicated to a locking platform of the computation module.

22. (Cancelled).

23. (Previously Presented) The method of claim 1, wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis.

24. (Currently Amended) The method of claim 1, wherein the discrete GPU of the chassis assists the computation module with performing the one or more operations on the data by offloading at least one processing duty from the computation module.

25. (New) The method of claim 1, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

26. (New) The computer program product embodied on a computer readable medium of claim 18, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

25. (New) The system of claim 19, wherein the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis.

REMARKS

The Examiner has rejected Claims 1-3, 5-14, 16, and 18-24 under 35 U.S.C. 103(a) as being unpatentable over *Kikinis* (U.S. Patent No. 5,689,654) in view of what is well known in the art as evidenced by any of *Buck* (U.S. Patent No. 7,219,085), *Kong* (U.S. Patent No. 7,325,086), *Shimamura* (U.S. Patent No. 7,327,361), and *Miller* (U.S. Patent No. 8,284,205). Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to each of the independent claims. Specifically, Applicant has amended each of independent claims 1, 18, and 19 to recite at least the limitations of cancelled claim 22. The amendments are supported by paragraph [0020] of the application, as originally filed, and therefore, the amendments do not introduce new matter. No combination of the cited references teaches or suggests the limitations recited in each of the independent claims. Thus, amended claims 1, 18, and 19, and claims dependent thereon are in condition for allowance.

As amended each of the independent claims recites the following limitations:

"*graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module*" (see this or similar, but not necessarily identical, language in the independent claims).

In the *Final Office Action*, the Examiner rejected the limitations of claim 22 by stating only that "discrete GPU's are known." See the *Final Office Action* at page 5. Applicant respectfully submits that the Examiner neglected to cite prior art that teaches or suggests the claim limitations of "graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module." In particular, no combination of the cited references teaches or suggests sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module.

Kikinis teaches a notebook computer framework including a video display controller and function module that is coupled to the video display controller of the notebook computer framework. The Examiner equates the video display controller of the notebook computer framework (172, 61, or 1011) taught by *Kikinis* with the claimed GPU of the chassis. The Examiner equates the function module (10/1061) taught by *Kikinis* with the claimed computation module. *Kikinis* teaches a CPU and video display controller that are built into a CPU function module "for upgrading by switching CPU function modules." See *Kikinis* at column 30, lines 41-52. *Kikinis* is clear that the video controller is included in one of the case 1223 **or** the function module 1300. *Kikinis* fails to contemplate including a video controller in both the case 1223 and a function module 1300. Specifically *Kikinis* states the following:

> "The video controller may be integral to a function module, which is shown as video controller 1301 in a CPU function module 1300, or implemented in the case, shown as optional video controller 1301(a). ... In another aspect, the I/O area may comprise an active-matrix display, in which case, dedicated analog driver lines from video controller 1301 connect to the display. ... In an alternative embodiment, video controller 1301 is built into case 1223 (FIG. 35A), and connected directly to bus 1255, similar to the modular notebook computer described above."
>
> See *Kikinis* at column 30, lines 17-22. (emphasis added)

Thus, *Kikinis* fails to teach or suggest a system having a both a discrete GPU of the chassis and a GPU within a computation module. *Kikinis* is completely silent regarding sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module, as required by the plain language of amended independent claim 1. Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

The Examiner relies on prior art references *Buck*, *Kong*, *Shimamura*, and *Miller* for what is well known in the art. See the *Final Office Action* at page 3. No combination of the cited prior art references teaches or suggests the limitations recited in each of the independent claims.

Buck teaches offloading **non-graphics** (machine learning) processing from a CPU to a GPU. See *Buck* at column 8, lines 16-24. *Buck* fails to teach or suggest sharing of graphics processing between two or more GPUs, as required by the plain language of amended independent claim 1. In contrast, *Buck* is silent regarding graphics processing. Therefore, *Buck* fails to teach or suggest sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module, as required by amended independent clam 1. *Buck* does not cure the deficiencies of *Kikinis*, set forth above.

Kong teaches a Northbridge device that is configured to support communication paths to two GPUs within a computer chassis. See *Kong* at Column 3, lines 34-42. Nothing in *Kong* teaches or suggests sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module. Thus, *Kong* does not cure the deficiencies of *Kikinis* and *Buck*, discussed above.

Shimamura teaches graphics processing using a GPU that receives rendering commands from a CPU. See *Shimamura* at column 8, lines 54-59. *Shimamura* is completely silent regarding sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module. Thus, *Shimamura* does not cure the deficiencies of *Kikinis*, *Buck*, and *Kong*, discussed above.

Miller teaches redistributing graphics processing to run on a GPU and also on a CPU and/or DSP. "[A] graphics rendering process, though normally compiled to run on a GPU, is also compiled to run on CPU and on DSP to allow dynamic redistribution of such graphic rendering process to one or both of a CPU and a DSP. Re-distribution of this graphics rendering process to a CPU or DSP can include the porting of GPU-specific compiled codes to the CPU or DSP …" See *Miller* at column 2, lines 45-51. *Miller* is completely silent regarding sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module. Thus, *Miller* does not cure the deficiencies of *Kikinis*, *Buck*, *Kong*, and *Shimamura*, discussed above.

As the aforementioned illustrates, the cited references, alone or in combination, do not teach or suggest sharing of graphics processing based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module. Thus, the cited references cannot render amended claim 1 obvious. Therefore, Applicants submit that claim 1, and all claims dependent thereon, are now in condition for allowance.

Furthermore, independent claims 18 and 19 have been amended to include limitations similar to amended claim 1. Applicants submit that claims 18 and 19, as well as all claims dependent thereon, are also in condition for allowance for at least the same reasons as set forth above in conjunction with the discussion of amended claim 1.

New claims 25-27 each recite the limitations that the computation module remains powered on while the computation module is de-coupled from the discrete GPU of the chassis. New claims 25-27 are supported by at least paragraph [0032] of the application, as originally filed. None of the cited references teaches or suggest these limitations. Therefore, these new claims are allowable independent of their dependence on amended claims 1, 18, and 19, respectively.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at Stephanie@zilkakotab.com or may leave a message at (408) 971-2573. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP679).

Respectfully submitted,
Zilka-Kotab, PC

_/Stephanie Winner/__
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2111
Examiner Name	P. R. Myers
Attorney Docket Number	NVIDP679/SC-09-0042-US1

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	2	6246211	B1	2001-06-12	Dalton et al.	

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	1	20100325460	A1	2010-12-23	Chen et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13335850
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	P. R. Myers
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

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	1	Notice of Allowance from U.S. Application No. 13/083,469, dated December 13, 2013	☐
	2	Decision on Rejection from U.S. Application No. 201010141965.4, dated January 8, 2014	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13335850
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	P. R. Myers
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Stephanie L. Winner/	Date (YYYY-MM-DD)	2014-05-13
Name/Print	Stephanie L. Winner	Registration Number	52371

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13335850
Filing Date:	22-Dec-2011
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Filer:	Stephanie Winner/Justin Bocchino
Attorney Docket Number:	NVIDP679/SC-09-0042-US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	19024720
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Stephanie Winner/Justin Bocchino
Filer Authorized By:	Stephanie Winner
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	13-MAY-2014
Filing Date:	22-DEC-2011
Time Stamp:	21:07:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1200
RAM confirmation Number	5755
Deposit Account	501351
Authorized User	ZILKA, KEVIN J

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	NVIDP679_RCE_05-13-2014.pdf	697977 a50dac50e5e393b34a4d306c45c50debf69b3e21	no	3
Warnings:					
Information:					
2		NVIDP679_SC-09-0042-US1_Amendment_B_05-13-2014.pdf	46752 b202b0d62df2d7077e5914a132868f252ef50b66	yes	10

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	10

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	NVIDP679_PRC_IDS_05-13-2014.pdf	612661 7b9e4026b1bee0a1fe315418454e92085c176f5e	no	4
Warnings:					
Information:					
4	Non Patent Literature	NVIDP653_SZ-09-0345-CN1-US1_NOA_12-13-13.pdf	876574 88adcdeacc5e59f97794a4ec268938ac6f30588c	no	19
Warnings:					
Information:					
5	Non Patent Literature	NVIDP653CN_DecisionOnRejection_01-08-2014.pdf	511748 bf520c1e8ad2e02d1cedeb78f5be3589a20addc5	no	6
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30872 b710554a65cba9d3ea4582a2e957b409bb3adc52	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	2776584

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	13335850
Filing Date:	22-Dec-2011
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Filer:	Stephanie Winner/Justin Bocchino
Attorney Docket Number:	NVIDP679/SC-09-0042-US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	200	200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**200**

Electronic Acknowledgement Receipt

EFS ID:	19024730
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Stephanie Winner/Justin Bocchino
Filer Authorized By:	Stephanie Winner
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	13-MAY-2014
Filing Date:	22-DEC-2011
Time Stamp:	21:10:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$200
RAM confirmation Number	5760
Deposit Account	501351
Authorized User	ZILKA, KEVIN J

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	30953 6db5f36c3a8bf5d9a181ce885d06f2ffde920763	no	2

Warnings:

Information:

Total Files Size (in bytes):	30953

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/335,850	12/22/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

05/13/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 22	Minus	** 23	= 0	x $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/VENESSA JONES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 01/15/2014
ZILKA-KOTAB, PC- NVID
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
01/15/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zk-uspto@zilkakotab.com

Office Action Summary	Application No. 13/335,850	Applicant(s) PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12/12/13.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) 1,2 and 4-24 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) 1-2,4-24 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 12/12/13.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Response to Arguments

2. Applicant's arguments filed 12/12/13 have been fully considered but they are not persuasive.

In regards to applicants argument that Kikinis does not teach "receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, wherein the computation module is coupled to a graphics processing unit of the chassis" and "performing one or more operations on the data utilizing the computation module and with assistance of the GPU or the chassis": applicants have already pointed out that Kikinis teaches in on of his many embodiments that "the docked μPDA can be operated in situ by manipulating the input areas of the μPDA <u>displayed on the host's screen</u>" (emphasis added). In this embodiment the user uses "the host's display and input means" (Column 2 line 64 to Column 3 line5 such as a "pointer-style" input or mouse of the host (that is the hosts input device) to click the displayed inputs of the μPDA on the host screen. Kikinis teaches some embodiments that are "manipulating input areas" of the μPDA using the input device of the host. Kikinis also teaches the embodiment of figure 8 including the host having a touch screen for manipulating the input area of the μPDA.. Kikinis also teaches the input device of the host may be a keyboard (Column 22 lines 44-53). Kikinis teaches this information being displayed on the hosts screen. In several embodiments the Video display controller is part of the chassis for example figure 25 item 1091 (Column 22 lines 44-53). In fact only in the embodiment of figure 40 does Kikinis state that the video display controller is on the μPDA. Figure 39 shows the video display controller "optionally" on the

host. Kikinis also teaches the host unit into which the μPDA is inserted may be an enabled or dedicated notebook or desktop computer. See figures 5, 21, and 41. While Kikinis teaches the host having a video display controller. Kikinis does not use the words "graphics processing unit". Although the examiner does not know of any video display controllers that cannot be interpreted as having a GPU the examiner is citing several references that teach GPU's that work in conjunction with a processor.

Claim Rejections - 35 USC § 103

3. Claims 1-3, 5-14, 16, 18-24 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of what is well known in the art as evidenced by any of Buck et al PN 7,219,085, Kong et al PN 7,325,086, Shimamura et al PN 7,327,361, and Miller et al PN 8,284,205.

In regards to claims 1, 8, 10, 18, 19, 24: Kikinis et al teaches a method, comprising: receiving input data at a computation module (10 or 1061), utilizing a chassis (172, 61 or 1011) removably coupled to the computation module (10/1061), wherein the computation module is coupled to a video display controller of the chassis (1091 or 1301(a)); performing one or more operations on the data, utilizing the computation module (10/1061 "in situ" Column 11 lines 36-50) and with assistance of the video display controller od the chassis (the video display controller 1091 displays the data of the Unit 1061); and providing output data from the computation module, utilizing the chassis (1072,61 or 1011). Kikinis et al does not use the words "Graphics processing unit. Although the examiner does not know of any video display controllers that can not be identified as a GPU. Official notice is taken that GPU's are routine for displaying video

data including working to assist the CPU for this displaying. It would have been obvious to have the host include a GPU in the video display controller because this is a standard display tool that takes the graphics requirements from a CPU.

In regards to claim 2: Kikinis et al teaches the chassis (172) includes a computer system form factor with one or more data processing elements ("Host CPU" 24).

In regards to claim 5: Kikinis teaches the computation module includes a connector (14 or 1033) for coupling the computation module to the chassis..

In regards to claim 6: Kikinis et al teaches the computation module includes a locking platform (1031 for "latching"),

In regards to claim 7: Kikinis teaches the locking being hardware.

In regards to claim 9: Kikinis teaches the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met (Figure 7).

In regards to claims 11-13: Kikinis teaches the computation module supplements one or more elements of the chassis during the performing of the one or more operations (Column 13 lines 15-22).

In regards to claim 14: Kikinis teaches the processing includes one or more of graphics processing, network processing, and sound processing (video, network and audio).

In regards to claim 16: Kikinis et al teaches the computation module is placed within a cavity of the chassis and is coupled to the chassis using an internal connector located within the chassis.

In regards to claim 20: Kikinis et al teaches memory.

In regards to claim 21: Kikinis et al teaches locking means figures 44-47.

In regards to claim 22: Discrete GPU's are known.

In regards to claim 23: Kikinis teaches the connection may be either parallel or serial Kikinis et al does not teach packetized data. Official notice is taken that packetized data is a standard in serial, Also becoming common in parallel. It would have been obvious to packetize the data because this is a standard.

4. Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Utz et al PN 8,131,904.

In regards to claim 4: Kikinis et al teaches the function unit described above. Kikinis et al does not state that it can be implemented as a SOC. Utz et al teaches a SOC function module connected to a system. It would have been obvious to implement Kikinis et al's function module(s) ad SOC's because this would have allowed for smaller units.

5. Claim 15 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Li PN 2007/0006290.

In regards to claim 15. Kikinis et al teaches security code but does not teach it being stored on a USB device. Li teaches a user security code may be stored on a plugged in USB device. It would have been obvious for a security code to be stored on a USB device because this would have only allowed an authorized person the use the device while not having to remember a long security code.

6. Claim 17 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654.

In regards to claim 17: Kikinis et al teaches dedicated pins and using the "appropriate pins". Kikinis also teaches display connection, data connection, and locking/security. Kikinis however does not state that the pins are bi-directional. Official notice is taken that bi-directional pins are well known. It would have been obvious to include bi-directional pins because this would have decreased the number of pins required for the connector.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL R. MYERS whose telephone number is (571)272-3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL R MYERS
Primary Examiner
Art Unit 2111

/PAUL R MYERS/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 13/335,850	Applicant(s)/Patent Under Reexamination PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0162336 A1	07-2005	McClintock et al.	345/001.1
*	B	US-2006/0282855 A1	12-2006	Margulis, Neal D.	725/043
*	C	US-7,219,085 B2	05-2007	Buck et al.	706/12
*	D	US-7,325,086 B2	01-2008	Kong et al.	710/307
*	E	US-7,327,361 B2	02-2008	Shimamura et al.	345/422
*	F	US-2008/0084359 A1	04-2008	Giannuzzi et al.	345/1.1
*	G	US-8,284,205 B2	10-2012	Miller et al.	345/502
*	H	US-8,429,299 B2	04-2013	Chan et al.	709/246
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
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	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/09/2013	01/10/2014							
	1	✓	✓							
	2	✓	✓							
	3	✓	-							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
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	11	✓	✓							
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	14	✓	✓							
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	18	✓	✓							
	19	✓	✓							
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	22		✓							
	23		✓							
	24		✓							

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2111
Examiner Name	MYERS, PAUL R
Attorney Docket Number	NVIDP679/SC-09-0042-US1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8238972	B2	2012-08-07	Wang et al.	
	2	6246211	B1	2001-06-12	Dalton et al.	
	3	6085330	A	2000-07-04	Hewitt et al.	

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	1	20090193243	A1	2009-07-30	Ely	

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	1							☐

/Paul R. Myers/ 01/09/2014

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850 13335850 - GAU: 2111
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	MYERS, PAUL R
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action from Chinese Application No. 201010141965.4, dated March 28, 2013	☐
	2	Office Action from Chinese Application No. 201010141965.4, dated June 27, 2013	☐
	3	Non-Final Office Action from U.S. Application No. 13/083,469, dated April 15, 2013	☐

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EXAMINER SIGNATURE

Examiner Signature	/Paul R. Myers/	Date Considered	01/09/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850 13335850 - GAU: 2111
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	MYERS, PAUL R
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE ROSSI/	Date (YYYY-MM-DD)	2013-12-12
Name/Print	Jamie L. Rossi	Registration Number	56875

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

CPC- SEARCHED

Symbol	Date	Examiner
east searched	1/10/14	PRM

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
710	301-304	9/9/13	PRM

SEARCH NOTES

Search Notes	Date	Examiner

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2112
Sean Michael Pelletier	Examiner: Myers, Paul R.
Application No.: 13/335,850	Art Unit: 2111
Filed: 12/22/2011	Atty. Docket No.: NVIDP679/SC-09-0042-US1
For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Date: 12/12/2013

AMENDMENT A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Examiner:

In response to the Office Action dated 09/13/2013, please enter the following amendments believed to place the claims in condition for allowance.

AMENDMENTS TO THE CLAIMS

Amended claims follow:

1. (Currently Amended) A method, comprising:

receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis;

performing one or more operations on the data, utilizing the computation module and with assistance of the GPU of the chassis; and

providing output data from the computation module, utilizing the chassis.

2. (Original) The method of claim 1, wherein the chassis includes a computer system form factor with one or more data processing elements.

3. (Cancelled)

4. (Original) The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5. (Original) The method of claim 1, wherein the computation module includes a connector for coupling the computation module to the chassis.

6. (Original) The method of claim 1, wherein the computation module includes a locking platform.

7. (Original) The method of claim 6, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. (Original) The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. (Original) The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. (Original) The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. (Original) The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. (Original) The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. (Currently Amended) The method of claim 1, wherein a portion of the ~~processing~~ one or more operations is performed by ~~a processor on~~the GPU of the chassis, and another portion of the ~~processing~~ one or more operations is performed by the computation module.

14. (Currently Amended) The method of claim 1, wherein the ~~processing~~ one or more operations include[[s]] one or more of graphics processing, network processing, and sound processing.

15. (Original) The method of claim 1, wherein a hardware lock is implemented within the computation module, and such hardware lock requires a key contained within a universal serial bus (USB) device for the computation module to operate.

16. (Original) The method of claim 1, wherein the computation module is placed within a cavity of the chassis and is coupled to the chassis using an internal connector located within the chassis.

17. (Original) The method of claim 5, wherein a predetermined number of pins of the connector are dedicated to a bi-directional display connection, a predetermined number of pins of the connector are dedicated to a bi-directional data connection, and a predetermined number of pins of the connector are dedicated to a locking platform of the computation module.

18. (Currently Amended) A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis;

code for performing one or more operations on the data, utilizing the computation module and with assistance of the GPU of the chassis; and

code for providing output data from the computation module, utilizing the chassis.

19. (Currently Amended) A system, comprising:

a chassis; and

a computation module removably coupled to [[a]]the chassis, wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis;[[,]]

wherein the computation module ~~for receiving~~ receives input data utilizing the chassis, ~~performing~~ performs one or more operations on the data with assistance of the GPU of the chassis, and ~~providing~~ provides output data, utilizing the chassis.

20. (Original) The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

21. (New) The method of claim 5, wherein a predetermined number of pins of the connector are dedicated to a locking platform of the computation module.

22. (New) The method of claim 14, wherein the one or more operations include the graphics processing, wherein the GPU of the chassis is a discrete GPU, and wherein the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module.

23. (New) The method of claim 1, wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis.

24. (New) The method of claim 1, wherein the GPU of the chassis assists the computation module with performing the one or more operations on the data by offloading at least one processing duty from the computation module.

REMARKS

The Examiner has rejected Claims 1-3, 5-14, 16, and 18-20 under 35 U.S.C. 102(b) as being anticipated by Kikinis et al. (U.S. Patent No. 5,689,654). Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to each of the independent claims. Specifically, applicant has amended each of the independent claims to further distinguish applicant's claim language from the Kikinis reference, as follows:

> "receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, *wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis*;
>
> performing one or more operations on the data, utilizing the computation module *and with assistance of the GPU of the chassis*" (see this or similar, but not necessarily identical, language in the independent claims – emphasis added).

Applicant respectfully notes the Kikinis reference discloses "[a] personal digital assistant module with a local CPU, memory, and I/O interface" that includes "a connector at a surface of the personal digital assistant for interfacing to a bus connector of a host general-purpose computer, providing direct bus communication between the personal digital assistant and the host general-purpose computer," where "[t]he personal digital assistant… forms a host/satellite combination with a host computer having a docking bay, wherein upon docking a docking protocol controls access by the host to memory of the personal digital assistant based on one or more passwords provided by a user to the host" (Abstract – emphasis added). The Kikinis reference also discloses that "[i]f the computer is an enabled host, an application is started to configure host access to the μPDA's data files through the μPDA microcontroller," and "[a] user interface… is displayed on the host monitor 104" such that "[t]he host interface menu, as well as other application menus, may be formatted in part as a display of the μPDA I/O interface 16," and "the docked μPDA can be operated in situ by manipulating the input areas of the μPDA displayed on the host's screen" (Col. 11, lines 36-50 – emphasis added).

However, disclosing a personal digital assistant (PDA) module with a CPU, memory, and a connector for interfacing with a host computer, where a docking protocol controls access by the host to memory of the PDA module based on a password provided by a user at the host, and disclosing that once docked, the PDA module can be operated in situ by manipulating input areas of the PDA module, as in the Kikinis reference, does not teach applicant's claimed "receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis" and "performing one or more operations on the data, utilizing the computation module and with assistance of the GPU of the chassis" (emphasis added), as claimed by applicant.

More clearly, docking a PDA module with a host computer, and operating the PDA module in situ by manipulating input areas of the PDA module, as in Kikinis, fails to teach "receiving input data at a computation module, utilizing a chassis removably coupled to the computation module, wherein the computation module is coupled to a graphics processing unit (GPU) of the chassis" and "performing one or more operations on the data, utilizing the computation module and with assistance of the GPU of the chassis" (emphasis added), as specifically claimed by applicant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the above reference excerpt(s), as noted above. Thus, a notice of allowance or specific prior art showing of each of the foregoing

claim elements, in combination with the remaining claimed features, is respectfully requested.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to Claims 11 and 13, the Examiner has relied on Column 13, lines 15-22, from the Kikinis reference to make a prior art showing of applicant's claimed technique "wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations" (see Claim 11), and applicant's claimed technique "wherein a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module" (see Claim 13 – as amended).

Applicant respectfully notes the excerpt of the Kikinis reference cited by the Examiner discloses that "[a]nother useful feature in host/μPDA communication is a means for a user to select and compose a mix of executable program flies for downloading to a μPDA, either replacing or supplementing those executable routines already resident," and "[a] user can have several different program lists for downloading as a batch, conveniently configuring the applicability of a μPDA among a wide variety of expected work environments" (Col. 13, lines 15-22 – emphasis added).

However, disclosing that a user can select executable program files for downloading to a PDA, and disclosing the user can use program lists for downloading programs to the PDA as a batch for configuring the PDA for different expected work environments, as in the Kikinis reference, does not teach applicant's claimed technique "wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations" (see Claim 11 – emphasis added), and applicant's claimed technique "wherein a portion of the one or more operations is performed by the GPUof the chassis, and another portion of the one or more operations is performed by the computation module" (see Claim 13 – emphasis added), as claimed by applicant.

In other words, downloading executable programs to a PDA based on a user's selection, as in Kikinis, fails to teach that "the computation module supplements one or more elements of the chassis during the performing of the one or more operations" (see Claim 11 – emphasis added), and that "a portion of the one or more operations is performed by the GPU of the chassis, and another portion of the one or more operations is performed by the computation module" (see Claim 13 – emphasis added), as specifically claimed by applicant.

Additionally, the Examiner has rejected Claim 17 under 35 U.S.C. 103(a) as being unpatentable over Kikinis in view of Examiner's Official Notice. Specifically, the Examiner has argued that "Kikinis et al teaches dedicated pins and using the 'appropriate pins'," that "Kikinis also teaches display connection, data connection, and locking/security," and that although "Kikinis… does not state that the pins are bi-directional… [o]fficial notice is taken that bi-directional pins are well known" and "[i]t would have been obvious to include bi-directional pins because this would have decreased the number of pins required for the connector."

Applicant respectfully notes the Kikinis reference discloses that "there is a pin configuration (not shown) in connector 14 dedicated to signalling that a module is docked" (Col. 12, lines 18-21 – emphasis added), and also disclose that "[a] μPDA may serve as the platform for various peripheral attachments via expansion port 20," such that "[u]pon attachment to a peripheral, a dedicated pin or pins within expansion port 20 signal microcontroller 11, and a peripheral boot-strap application is executed," and "[i]nterfacing control routines, which may reside in the peripheral or in the memory of the μPDA, are then executed" (Col. 18, lines 5-13 – emphasis added).

However, disclosing that a pin configuration in a connector may be dedicated to signaling that a module is docked, and similarly disclosing that a dedicated pin or pins may signal a microcontroller upon attachment to a peripheral, and a peripheral boot-strap application is then executed, as in the Kikinis reference, fails to *even suggest* that "[i]t would have been obvious to include bi-directional pins because this would have

decreased the number of pins required for the connector," as argued by the Examiner, much less teach applicant's claimed technique "wherein a predetermined number of pins of the connector are dedicated to a bi-directional display connection, a predetermined number of pins of the connector are dedicated to a bi-directional data connection, and a predetermined number of pins of the connector are dedicated to a locking platform of the computation module" (see Claim 17 – emphasis added), as claimed by applicant.

Simply disclosing that a pin configuration is dedicated to signaling that a module is docked or attached to a peripheral, as in Kikinis, fails to teach that "a predetermined number of pins of the connector are dedicated to a bi-directional display connection, a predetermined number of pins of the connector are dedicated to a bi-directional data connection, **and** a predetermined number of pins of the connector are dedicated to a locking platform of the computation module" (emphasis added), as specifically claimed by applicant.

Again, since this criterion has simply not been met by the above reference excerpt(s), as noted above, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Still yet, applicant brings to the Examiner's attention the subject matter of new Claims 21-24 below, which are added for full consideration:

> "wherein a predetermined number of pins of the connector are dedicated to a locking platform of the computation module" (see Claim 21);
>
> "wherein the one or more operations include the graphics processing, wherein the GPU of the chassis is a discrete GPU, and wherein the graphics processing is shared by the discrete GPU of the chassis and another GPU within the computation module based on scalability logic within both the discrete GPU of the chassis and the GPU within the computation module" (see Claim 22);

"wherein the output data includes packetized data that is transferred from the computation module to a network connection of the chassis" (see Claim 23); and

"wherein the GPU of the chassis assists the computation module with performing the one or more operations on the data by offloading at least one processing duty from the computation module" (see Claim 24).

Again, a notice of allowance or a proper prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. NVIDP679).

Respectfully submitted,
Zilka-Kotab, PC.

/JAMIE ROSSI/

Jamie L. Rossi
Registration No. 56,875

P.O. Box 721120
San Jose, CA 95172-1120
408-971-2573

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2111
Examiner Name	MYERS, PAUL R
Attorney Docket Number	NVIDP679/SC-09-0042-US1

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8238972	B2	2012-08-07	Wang et al.	
	2	6246211	B1	2001-06-12	Dalton et al.	
	3	6085330	A	2000-07-04	Hewitt et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090193243	A1	2009-07-30	Ely	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	MYERS, PAUL R
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action from Chinese Application No. 201010141965.4, dated March 28, 2013	☐
	2	Office Action from Chinese Application No. 201010141965.4, dated June 27, 2013	☐
	3	Non-Final Office Action from U.S. Application No. 13/083,469, dated April 15, 2013	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2111
	Examiner Name	MYERS, PAUL R
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE ROSSI/	Date (YYYY-MM-DD)	2013-12-12
Name/Print	Jamie L. Rossi	Registration Number	56875

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13335850
Filing Date:	22-Dec-2011
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Filer:	Jamie Lynn Rossi/Justin Bocchino
Attorney Docket Number:	NVIDP679/SC-09-0042-US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in Excess of 20	1202	3	80	240
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**420**

Electronic Acknowledgement Receipt

EFS ID:	17649183
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Jamie Lynn Rossi/Justin Bocchino
Filer Authorized By:	Jamie Lynn Rossi
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	12-DEC-2013
Filing Date:	22-DEC-2011
Time Stamp:	22:24:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$420
RAM confirmation Number	9130
Deposit Account	501351
Authorized User	ZILKA, KEVIN J

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NVIDP679_AmendOA_12-12-2013.pdf	74890 a87d3113ea151fc0a9de5a693172ca027c85e2b0	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal Letter	1	1
Amendment/Req. Reconsideration-After Non-Final Reject	2	2
Claims	3	6
Applicant Arguments/Remarks Made in an Amendment	7	12

Warnings:

Information:

2	Non Patent Literature	NVIDP653_SZ-09-0345-CN1_US1_OA1_04-15-13.pdf	517068 6af7d877d30b20c57407b359de74f963a1c0a33c	no	13

Warnings:

Information:

3	Non Patent Literature	NVIDP653CN_OA_03-28-2013.pdf	372225 6a3c554213fa8ae69a8bcf1eded8e2adeac06fc7	no	9

Warnings:

Information:

4	Non Patent Literature	NVIDP653CN_OA_06-27-2013.pdf	567301 4480f28ae460802223f78fbafc4cef469bf105e8	no	7

Warnings:

Information:

5	Information Disclosure Statement (IDS) Form (SB08)	NVIDP679_PRC_IDS_12-12-2013.pdf	612458 3f01c8a8a12a4521b9cf021231a5db1a7bcd9e6a	no	4

Warnings:

Information:

6	Fee Worksheet (SB06)	fee-info.pdf	32333 ed82097051347a376f2746c85af9316758dacbd3	no	2

Warnings:

Information:

Total Files Size (in bytes):	2176275

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2112
Sean Michael Pelletier	Examiner: Myers, Paul R.
Application No.: 13/335,850	Art Unit: 2111
Filed: 12/22/2011	Atty. Docket No.: NVIDP679/SC-09-0042-US1
For: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	Date: 12/12/2013

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 2233-1450

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims Remaining After Amendment		Highest Previously Paid For		Present Extra	SMALL ENTITY RATE FEE		OR	LARGE ENTITY RATE FEE	
TOTAL CLAIMS	23	-	20	=	3	x40	= $	OR	x80 =	$240.00
INDEP CLAIMS	3	-	3	=	0	x210	= $	OR	x420=	$0.00

☐ Multiple Dependent Claim Present and Fee Not Previously Paid $0 $0

TOTAL $_____ **$240.00**

☒ Applicant(s) believe that no Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 50-1351.

☒ If the required fees are missing or any additional fees are required to facilitate filing the enclosed response, please charge such fees or credit any overpayment to Deposit Account No. 50-1351.

Respectfully submitted,
Zilka-Kotab, PC

/JAMIE ROSSI/

Jamie L. Rossi
Registration No. 56,875

P.O. Box 721120
San Jose, CA 95172-1120
Telephone: (408) 971-2573

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/335,850	12/22/2011	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

12/12/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 23	Minus	** 20	= 3	x $80 =	240
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	x $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**240**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/JAMES ELLIOTT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1	2112

75359 7590 09/13/2013
ZILKA-KOTAB, PC- NVID
P.O. BOX 721120
SAN JOSE, CA 95172-1120

EXAMINER
MYERS, PAUL R

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
09/13/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

zk-uspto@zilkakotab.com

Office Action Summary	Application No. 13/335,850	Applicant(s) PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/22/13*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/19/12*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Neural AI, LLC Exhibit 2019
Page 2019 - 150
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC

1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-3, 5-14, 16, 18-20 are rejected under pre-AIA 35 U.S.C. 102b as being clearly anticipated by Kikinis et al PN 5,689,654.

In regards to claims 1, 8, 10, 18, 19: Kikinis et al teaches a method, comprising: receiving input data at a computation module (10 or 1061), utilizing a chassis (172, 61 or 1011) removably coupled to the computation module (10/1061); performing one or more operations on the data, utilizing the computation module (10/1061 "in situ" Column 11 lines 36-50); and providing output data from the computation module, utilizing the chassis (1072,61 or 1011).

In regards to claim 2: Kikinis et al teaches the chassis (172) includes a computer system form factor with one or more data processing elements ("Host CPU" 24).

In regards to claim 3: Kikinis et al teaches the chassis (1011) includes a computer system form factor without one or more data processing elements (Column 22 lines 7-20 "no on-board CPU").

In regards to claim 5: Kikinis teaches the computation module includes a connector (14 or 1033) for coupling the computation module to the chassis..

In regards to claim 6: Kikinis et al teaches the computation module includes a locking platform (1031 for "latching"),

In regards to claim 7: Kikinis teaches the locking being hardware.

In regards to claim 9: Kikinis teaches the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met (Figure 7).

In regards to claims 11-13: Kikinis teaches the computation module supplements one or more elements of the chassis during the performing of the one or more operations (Column 13 lines 15-22).

In regards to claim 14: Kikinis teaches the processing includes one or more of graphics processing, network processing, and sound processing (video, network and audio).

In regards to claim 16: Kikinis et al teaches the computation module is placed within a cavity of' the chassis and is coupled to the chassis using an internal connector located within the chassis.

In regards to claim 20: Kikinis et al teaches memory.

Claim Rejections - 35 USC § 103

4. Claim 4 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Utz et al PN 8,131,904.

In regards to claim 4: Kikinis et al teaches the function unit described above. Kikinis et al does not state that it can be implemented as a SOC. Utz et al teaches a SOC function module

connected to a system. It would have been obvious to implement Kikinis et al's function module(s) ad SOC's because this would have allowed for smaller units.

5. Claim 15 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654 in view of Li PN 2007/0006290.

In regards to claim 15. Kikinis et al teaches security code but does not teach it being stored on a USB device. Li teaches a user security code may be stored on a plugged in USB device. It would have been obvious for a security code to be stored on a USB device because this would have only allowed an authorized person the use the device while not having to remember a long security code.

6. Claim 17 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Kikinis et al PN 5,689,654.

In regards to claim 17: Kikinis et al teaches dedicated pins and using the "appropriate pins". Kikinis also teaches display connection, data connection, and locking/security. Kikinis however does not state that the pins are bi-directional. Official notice is taken that bi-directional pins are well known. It would have been obvious to include bi-directional pins because this would have decreased the number of pins required for the connector.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL R. MYERS whose telephone number is (571)272-3639. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL R MYERS
Primary Examiner
Art Unit 2111

/PAUL R MYERS/
Primary Examiner, Art Unit 2111

Notice of References Cited	Application/Control No. 13/335,850	Applicant(s)/Patent Under Reexamination PELLETIER, SEAN MICHAEL	
	Examiner PAUL R. MYERS	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,579,489 A	11-1996	Dornier et al.	710/303
*	B	US-5,689,654 A	11-1997	Kikinis et al.	710/303
*	C	US-2003/0172217 A1	09-2003	Scott et al.	710/303
*	D	US-6,769,036 B1	07-2004	Cortopassi et al.	710/15
*	E	US-6,779,066 B2	08-2004	Sakamoto, Kiyomi	710/300
*	F	US-2007/0006290 A1	01-2007	Li, Jui Yu	726/009
*	G	US-2007/0294457 A1	12-2007	Gantman et al.	710/313
*	H	US-8,131,904 B2	03-2012	Utz et al.	710/301
*	I	US-2013/0212402 A1	08-2013	Seevers et al.	713/185
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	K	US-			
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/09/2013								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
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	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2835
Examiner Name	Unassigned
Attorney Docket Number	NVIDP679/SC-09-0042-US1

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1	20100325460	A1	2010-12-23	Chen et al.	
	2	20080250179	A1	2008-10-09	Moon	
	3	20110249391	A1	2011-10-13	Xu	

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/Paul R. Myers/ 09/09/2013

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850 13335850 - GAU: 2111
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2835
	Examiner Name	Unassigned
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action from Chinese Patent Application No. 201010141965.4, dated August 21, 2012	☐

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Examiner Signature	/Paul R. Myers/	Date Considered	09/09/2013

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	13335850 13335850 - GAU: 2111
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2835
	Examiner Name	Unassigned
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE ROSSI/	Date (YYYY-MM-DD)	2012-11-19
Name/Print	Jamie L. Rossi	Registration Number	56,875

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13335850	PELLETIER, SEAN MICHAEL
	Examiner	**Art Unit**
	PAUL R MYERS	2111

CPC- SEARCHED

Symbol	Date	Examiner

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Class	Subclass	Date	Examiner
710	301-304	9/9/13	PRM

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/335,850	12/22/2011	Sean Michael Pelletier	NVIDP679/SC-09-0042-US1

CONFIRMATION NO. 2112

PUBLICATION NOTICE

OC000000062231579

75359
ZILKA-KOTAB, PC- NVID
P.O. BOX 721120
SAN JOSE, CA 95172-1120

Title:SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE

Publication No.US-2013-0163195-A1
Publication Date:06/27/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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(Not for submission under 37 CFR 1.99)

Application Number	13335850
Filing Date	2011-12-22
First Named Inventor	Sean Michael Pelletier
Art Unit	2835
Examiner Name	Unassigned
Attorney Docket Number	NVIDP679/SC-09-0042-US1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13335850
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	First Named Inventor	Sean Michael Pelletier
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	1	Office Action from Chinese Patent Application No. 201010141965.4, dated August 21, 2012	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13335850
	Filing Date	2011-12-22
	First Named Inventor	Sean Michael Pelletier
	Art Unit	2835
	Examiner Name	Unassigned
	Attorney Docket Number	NVIDP679/SC-09-0042-US1

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JAMIE ROSSI/	Date (YYYY-MM-DD)	2012-11-19
Name/Print	Jamie L. Rossi	Registration Number	56,875

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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Electronic Acknowledgement Receipt

EFS ID:	14270664
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Jamie Lynn Rossi/Justin Bocchino
Filer Authorized By:	Jamie Lynn Rossi
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	19-NOV-2012
Filing Date:	22-DEC-2011
Time Stamp:	20:09:31
Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	NVIDP679_PRC_IDS_11-19-2012.pdf	612329 7d6c57d0605f18c7693eaf096f3f21ef8210eff5	no	4

Warnings:

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2	Non Patent Literature	NVIDP653CN_OA_08-21-2012.pdf	387979 0c07cd7b28c1fc36cb5c4a407b3234f1bed4948e	no	5

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
13/335,850

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 60 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/335,850	12/22/2011	2183	1250	NVIDP679/SC-09-0042-US1	20	3

CONFIRMATION NO. 2112

75359
ZILKA-KOTAB, PC- NVID
P.O. BOX 721120
SAN JOSE, CA 95172-1120

FILING RECEIPT

OC000000051880638

Date Mailed: 01/12/2012

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Applicant(s)
Sean Michael Pelletier, Austin, TX;

Assignment For Published Patent Application
NVIDIA CORPORATION, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 75359

Domestic Priority data as claimed by applicant

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/335,850**

Projected Publication Date: 06/27/2013

Non-Publication Request: No

Early Publication Request: No

Title

SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE

Preliminary Class

712

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	NVIDP679/SC-09-0042-US1
First Inventor	Sean Michael Pelletier
Title	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
Express Mail Label No.	N/A

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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3. ☑ **Specification** [*Total Pages* 21]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☑ **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 8]
5. **Oath or Declaration** [*Total Sheets* 2]
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   b. ☐ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
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   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☑ **Application Data Sheet.** See 37 CFR 1.76
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9. ☐ **Assignment Papers** (cover sheet & document(s))
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☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: .....

Prior application information: *Examiner* _____ *Art Unit:* _____

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Name (Print/Type)	Jamie L. Rossi	Registration No. (Attorney/Agent)	56,875

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DOCKET: NVIDP679/SC-09-0042-US1

SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE

FIELD OF THE INVENTION

[0001] The present invention relates to computer system configuration, and more particularly to computer system modularization.

BACKGROUND

[0002] Computer systems have become essential to many aspects of modern day life. For example, individuals use computer systems to conduct business, communicate with their friends, maintain their personal finances, etc. However, current techniques for designing and implementing computer systems have been associated with various limitations.

[0003] For example, current computer systems have a finite life cycle with a limited or nonexistent upgrade path. For instance, if an individual would like to upgrade their existing laptop computer to a laptop computer with a larger screen, they may have to purchase an entirely new laptop computer. Further, if the individual purchases a tablet computer in addition to their laptop computer, their tablet computer may have a hardware system that is completely distinct from their laptop computer.

[0004] There is thus a need for addressing these and/or other issues associated with the prior art.

SUMMARY

[0005] A system, method, and computer program product are provided for performing operations on data utilizing a computation module. In use, input data is received at a computation module, utilizing a chassis removably coupled to the computation module. Additionally, one or more operations are performed on the data, utilizing the computation module. Further, output data is provided from the computation module, utilizing the chassis.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure **1** shows a method for performing operations on data utilizing a computation module, in accordance with one embodiment.

[0007] Figure **2** shows an exemplary computation module system, in accordance with another embodiment.

[0008] Figure **3** shows an exemplary computation module, in accordance with yet another embodiment.

[0009] Figure **4** shows exemplary computation module hardware, in accordance with yet another embodiment.

[0010] Figure **5** shows an exemplary case for computation module hardware, in accordance with yet another embodiment.

[0011] Figure **6** shows an exemplary system that is supplemented by a computation module, in accordance with yet another embodiment.

[0012] Figure **7** shows an exemplary online marketplace for purchasing a computation module and chassis, in accordance with yet another embodiment.

[0013] Figure **8** illustrates an exemplary system in which the various architecture and/or functionality of the various previous embodiments may be implemented.

DETAILED DESCRIPTION

[0014] Figure **1** shows a method **100** for performing operations on data utilizing a computation module, in accordance with one embodiment. As shown in operation **102**, input data is received at a computation module, utilizing a chassis removably coupled to the computation module. In one embodiment, the chassis may include a data entry element. For example, the chassis may include one or more of a keyboard, a mouse, a touch screen, a microphone, a digital camera, a network connection (e.g., a wired network connection, a wireless network connection), a bus connection (e.g., a universal serial bus (USB) connection, etc.), etc. In another embodiment, the chassis may include a data output element. For example, the chassis may include one or more of a screen, speakers, tactile output, etc.

[0015] Additionally, in one embodiment, the chassis may include a traditional computer system form factor (e.g., platform, etc.) with one or more data processing elements (e.g., a central processing unit (CPU), a graphics processing unit (GPU), etc.) and one or more storage elements (e.g., a hard disk drive (HDD), etc.). For example, the chassis may include a notebook computer, a netbook, computer, a desktop computer, an all in one (AIO) computer, etc. In another embodiment, the chassis may include the traditional computer system form factor, without the computing capability provided by the traditional computer system form factor (e.g., without one or more data processing elements, etc.). For example, the chassis may include one or more data entry elements and one or more data output elements, but may not include one or more data processing elements.

[0016] Further, in one embodiment, the computation module may include any module capable of performing one or more computations on data. In another embodiment, the computation module may include one or more processors. For example, the computation module may include a central processing unit (CPU), a graphics processing unit (GPU), etc. In yet another embodiment, the computation module may include one or more integrated circuits. For example, the computation module may include a system on a chip

(SOC) that integrates one or more computing components (e.g., a microcontroller, memory, timing sources, timers, interfaces, regulators, etc.) into a single chip. In yet another embodiment, the computation module may include a data communications element (e.g., a wireless network interface, a wired network interface, a Bluetooth © interface, etc.).

[0017] Further still, in one embodiment, the chassis may be removably coupled to the computation module through one or more connections, interfaces, etc. For example, the computation module may include one or more hardware interfaces, software interfaces, etc. For instance, the computation module may include a connector for coupling the computation module to the chassis. In another embodiment, the connector may include a proprietary connector. In still another embodiment, the connector may include a plurality of pins, where a predetermined number of pins are used for display purposes. For example, a predetermined number of pins of the connector may be dedicated to a bi-directional display connection.

[0018] In another embodiment, a predetermined number of pins of the connector may be used for data transfer purposes. For example, a predetermined number of pins of the connector may be dedicated to a bi-directional data connection. In yet another embodiment, the computation module may be coupled to an external portion of the chassis. For example, the computation module may be coupled to the chassis using a dock or other connector located on the outside of the chassis. In another embodiment, the computation module may be coupled to an internal portion of the chassis. For example, the computation module may be placed within a cavity of the chassis and may be coupled to the chassis using an internal connector located within the chassis.

[0019] Also, in one embodiment, one or more security measures may be included within the computation module. For example, the computation module may include a locking platform. In another embodiment, the locking platform may include a hardware lock, a software lock, etc. For example, a hardware lock may be implemented within the computation module, and such hardware lock may require a hardware key (e.g., a key contained within a universal serial bus (USB) device, etc.) for the computation module to

operate. In yet another embodiment, a predetermined number of pins of a connector may be used for security purposes. For example, a predetermined number of pins of the connector may be dedicated to a locking platform of the computation module.

[0020] Additionally, in one embodiment, one or more data storage elements may be included within the computation module. For example, the computation module may contain a local storage device (e.g., a hard disk drive (HDD), a flash memory drive, random access memory (RAM), etc.). In another embodiment, one or more of the data storage elements may store a software operating system, personal data (e.g., data associated with an owner of the computation module), etc.

[0021] Further, in another embodiment, the input data may be received at the computation module through one or more data entry elements of the chassis. For example, a user may provide the input data, utilizing the one or more data entry elements of the chassis (e.g., by typing on a keyboard or touch screen of the chassis, plugging a device such as a removable flash memory-based hard drive into the chassis, etc.). In another example, the input data may be received at the computation module utilizing one or more data connections. For example, the input data may be received by the computation module through a network connection of the chassis (e.g., a wired network connection, a wireless network connection, etc.), a data storage connection of the chassis (e.g., a connection to a hard disk drive of the chassis, etc.), etc.

[0022] Further still, as shown in operation **104**, one or more operations are performed on the data, utilizing the computation module. In one embodiment, the data may be stored within the computation module. For example, the data may be stored within a data storage element of the computation module. In another embodiment, the data may be processed by an application of the computation module (e.g., an application stored within a data storage element of the computation module and run utilizing one or more processors of the computation module). Of course, however, any type of operation may be performed on the data, utilizing the computation module.

[0023] Also, in one embodiment, the one or more operations may be performed on the data only if criteria associated with one or more security measures included within the computation module are met. For example, the one or more operations may be performed only if a hardware key is connected to the computation module, if an encryption key is verified by software running on the computation module, etc.

[0024] Further, in one embodiment, the computation module may supplement one or more elements of the chassis during the performing of the one or more operations. In another embodiment, the chassis may supplement one or more elements of the computation module during the performing of the one or more operations. For example, the input data may represent a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module. For instance, a portion of the processing may be performed by a processor on the chassis, and another portion of the processing may be performed by the computation module. In yet another embodiment, the graphics processing may be performed exclusively by a dGPU on the chassis or by a combination of shared processing between the dGPU on the chassis and the GPU within the computation module (e.g., utilizing SLI® technology, etc.). For example, one or more of software algorithms and dedicated scalability logic may be used withinin the dGPU on the chassis and the GPU within the computation module to enable shared processing. In another embodiment, the processing may include one or more of graphics processing, network processing, sound processing, general processing, etc.

[0025] In addition, as shown in operation **106**, output data is provided from the computation module, utilizing the chassis. In one embodiment, the output data may be provided as output of an application running within the computation module. In another embodiment, the output data may be data stored within a storage component of the computation module that is retrieved. In yet another embodiment, the output data may be processed by one or more processors of the computation module. For example, the output data may include graphics data that is processed by a graphics processing unit (GPU) of the computation module.

[0026] In one embodiment, the output data may be provided from the computation module through one or more data output elements of the chassis. For example, the output data may include video data and such data may be transferred from the computation module to a display of the chassis (e.g., utilizing a connection between the computation module and the chassis). In another example, the output data may include audio data and such data may be transferred from the computation module to one or more speakers of the chassis. In yet another example, the output data may include packetized data (e.g., data packets, etc.), and such data may be transferred from the computation module to a network connection of the chassis.

[0027] In this way, the computation module may act as a portable computer without a display or tactile interface, and may obtain both a display and tactile interface from the chassis to which it is removably coupled. Additionally, an owner of the computation module may purchase a plurality of chasses and may connect to a different chassis when desired for example, the user may connect the computation module to a desktop computer chassis while working with the computation module at home, and may connect the computation module to a laptop computer chassis while working with the computation module away from home.

[0028] More illustrative information will now be set forth regarding various optional architectures and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

[0029] Figure **2** shows an exemplary computation module system **200**, in accordance with another embodiment. As an option, the system **200** may be carried out in the context of the functionality of Figure **1**. Of course, however, the system **200** may be implemented in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0030] As shown, the system **200** includes a computation module **202**, as well as a first computer chassis **204**, a second computer chassis **206**, and a third computer chassis **218**. In one embodiment, each of the computation module **202**, the first computer chassis **204**, the second computer chassis **206**, and the third computer chassis **218** may have their own unique identifier. Additionally, the computation module **202** includes a central processing unit **208**, a graphics processing unit **210**, and a data connection **212**. Additionally, the first computer chassis **204**, the second computer chassis **206**, and the third computer chassis **218** include a connector **214**, **216**, and **220**, respectively. In one embodiment, each connector **214**, **216**, and **220** may include a proprietary connector (e.g., a connector licensed by a particular manufacturer, company, etc.). In another embodiment, the first computer chassis **204**, the second computer chassis **206**, and the third computer chassis **218** may each include one or more of a liquid crystal display (LCD), a notebook housing, a keyboard, a power supply and power adapter, etc.

[0031] Additionally, in one embodiment, a user may purchase the computation module **202** in conjunction with the first computer chassis **204**. For example, the computation module **202** may be coupled to the first computer chassis **204** using the connector **214**, and both may be sold as a single unit (e.g., as an ultraportable notebook, etc.). Additionally, in one embodiment, after purchasing the computation module **202** in conjunction with the first computer chassis **204**, the user may purchase the second computer chassis **206**. For example, the user may purchase a larger notebook chassis with a larger screen.

[0032] Further, in another embodiment, the user may uncouple the computation module **202** from the connector **214** of the first computer chassis **204**, and may couple the computation module **202** to the connector **216** of the second computer chassis **206**. In yet another embodiment, the user may also purchase the third computer chassis **218**, may uncouple the computation module **202** from the connector **216** of the second computer chassis **206**, and may couple the computation module **202** to the connector **220** of the third computer chassis **218**. In one embodiment, the computation module **202** may be powered off before de-coupling the computation module **202** from one of the connectors **214**, **216**, and **220**. In another embodiment, the computation module **202** may remain

powered on while de-coupling the computation module **202** from one of the connectors **214**, **216**, and **220** (e.g., by utilizing a portable power supply such as a battery inside the computation module **202**, etc.).

[0033] Also, although chassis **204**, **206**, and **218** have been shown, it should be noted that the chassis can include any device capable of connecting with the computation module **202**. Table 1 illustrates examples of possible chasses, in accordance with one embodiment. Of course, it should be noted that the chasses shown in Table 1 are set forth for illustrative purposes only, and thus should not be construed as limiting in any manner.

Table 1

Potential platform implementations for computation module:

- **Consumer PCs**
    - Portable PC
        - Netbook
        - "Ultrabook"
        - Notebook
            - Notebook docking stations
        - Tablet
        - PDA (personal digital assistant)
    - Desktop PC
        - All-in-one
        - Traditional PC "tower" or workstation
        - Small-form-factor
    - Servers (rackmount)
    - NAS (network-attached storage)
    - Table PC (ie: Microsoft Surface©)
    - External Hard Drive
- **Consumer Electronics**
    - Televisions
    - Video game consoles (Xbox©, Playstation©, etc.)
    - Blu-ray players
    - AV Receivers
    - Digital Media Player (ie: AppleTV©, Roku©, etc.)
    - Telephone (video conferencing, IP Phones, etc.)
    - Cellphones
    - Camcorders/Video cameras

  - Digital Cameras
  - Wireless Routers
  - Electronic picture frame
  - Alarm clock
  - Behind-glass system (ie: bathroom mirror)
- **Military applications**
  - UAV or drone control
  - Airplane heads-up display
  - Munitions control and guidance (land, air, sea munitions)
  - Military Vehicles (see below)
- **Vehicles (land, air, sea)**
  - Electronic dashboard/console
  - GPS
  - In-vehicle entertainment

[0034] In this way, the computation module **202** may be used in any of the first computer chassis **204**, the second computer chassis **206**, or the third computer chassis **218** by simply coupling the computation module **202** to the desired chassis. In one embodiment, given the flexibility the computation module **202** allows since it may only require a chassis that features the connector **214**, **216**, and **220**, there may be no limitations to the different platforms that the computation module **202** can be coupled with. For example, computer monitors, high definition televisions (HDTVs), and other devices may include the computation module **202** as a "built-in" computing system simply by integrating a connector and appropriate power supply. Additionally, since the computation module **202** may connect with any chassis that features the appropriate connector, a user of the computation module **202** may have the flexibility to leverage the computation module **202** in a wide variety of different designs to best suit their usage model for a given time.

[0035] Figure **3** shows an exemplary computation module **300**, in accordance with another embodiment. As an option, the present computation module **300** may be carried out in the context of the functionality of Figures **1** and **2**. Of course, however, the computation module **300** may be implemented in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0036] As shown, the computation module **300** includes a system on a chip (SOC) **302**. In one embodiment, the SOC **302** may include a central processing unit (CPU), a graphics processing unit (GPU), an input/output mechanism, etc. Additionally, the computation module **300** includes a local storage element **304**. In one embodiment, the local storage element **304** may include a hard disk drive (HDD), a flash-based disk drive, etc. In another embodiment, the local storage element **304** may store an operating system, personal files, etc.

[0037] Additionally, the computation module **300** includes a security element **306**. In one embodiment, the security element **306** may include a proprietary connector. For example, the security element **306** may include a hardware lock (e.g., a proprietary connector) that locks the computation module **300** to a particular manufacturer, user, etc. In another embodiment, the security element **306** may include a software lock (e.g., password protection software), and may use link IDs for everything within the computation module platform. In this way, data within the computation module **300** may be secured.

[0038] Figure **4** shows exemplary computation module hardware **400**, in accordance with another embodiment. As an option, the present hardware **400** may be carried out in the context of the functionality of Figures **1-3**. Of course, however, the hardware **400** may be implemented in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0039] As shown, the computation module hardware **400** includes a CPU **402** and a GPU **404**. Additionally, the computation module hardware **400** includes a proprietary connector **406**. In one embodiment, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to displaying data of the computation module. For example, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to a bi-directional display connection.

[0040] Additionally, in one embodiment, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to the transfer of data to and from the computation module. For example, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to a bi-directional data connection. In another embodiment, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to the security of the computation module. For example, the proprietary connector **406** may include a predetermined number of pins that may be dedicated to a locking platform of the computation module.

[0041] In another example, the locking platform may be associated with a USB device. For example, a USB device with a software key stored on the USB device may have to be connected to the proprietary connector **406** in order for the computation module to operate. In another embodiment, the proprietary connector **406** may include a licensed connector (e.g., a connector licensed to a particular manufacturer, etc.). Further, Figure **5** shows an exemplary case **500** for the computation module hardware **400**. In one embodiment, the case **500** may be made of metal, plastic, or any other material (e.g., radio frequency-shielding material, etc.).

[0042] Figure **6** shows an exemplary system **600** that is supplemented by a computation module, in accordance with another embodiment. As an option, the present system **600** may be carried out in the context of the functionality of Figures **1-5**. Of course, however, the system **600** may be implemented in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0043] As shown, the system **600** includes an existing GPU **602** and storage device **604**. In one embodiment, the GPU **602** may include a discrete GPU (dGPU), and the system may include a dGPU platform (e.g., an all in one (AIO) system, a small form factor gaming system, a notebook docking station, etc.). In another embodiment, the GPU **602** and storage device **604** may be included within a standalone computing device (e.g., a personal computer, an integrated computing system, etc.). Additionally, the GPU **602** and storage device **604** are supplemented by a computation module **606** coupled to

both the GPU **602** and storage device **604**. In one embodiment, the computation module **606** may be coupled to a standalone computing device (e.g., utilizing a proprietary connector), where the standalone computing device contains the GPU **602** and storage device **604**.

[0044] Additionally, in one embodiment, the GPU **602** may attach to the computation module **606** via a bi-directional port (e.g., a mobile PCI express module (MXM), a Thunderbolt connection, etc.). In this way, the GPU **602** may assist the computation module **606** in processing (e.g., by offloading some processing duties from the computation module **606**). Additionally, the GPU **602** may override the computation module **606**. For example, the GPU **602** may perform all processing duties previously performed by the computation module **606**. In this way, the GPU **602** may supplement the computation module **606**, which may result in increased performance of the system **600**.

[0045] Further, in one embodiment, the computation module **606** may attach to the storage device **604** via a bi-directional data connection. In another embodiment, data may be transferred between the computation module **606** and the storage device **604**. In another embodiment, the computation module **606** may perform all or some storage duties previously performed by the storage device **604**. In this way, the computation module **606** may supplement the storage device **604**, which may improve the storage within the system **600**.

[0046] Figure **7** shows an exemplary online marketplace **700** for purchasing a computation module and chassis, in accordance with another embodiment. As an option, the present marketplace **700** may be carried out in the context of the functionality of Figures **1-6**. Of course, however, the marketplace **700** may be implemented in any desired environment. It should also be noted that the aforementioned definitions may apply during the present description.

[0047] As shown, the marketplace **700** includes a selection of available chasses **702** from which to purchase. Additionally, the marketplace **700** includes a processor

selection icon **704**, an operating system selection icon **706**, and a hard drive selection icon **708**. In one embodiment, a user may configure a processor, operating system, and hard drive for a computation module using the processor selection icon **704**, operating system selection icon **706**, and hard drive selection icon **708**, respectively. Additionally, the user may select one or more chasses from the selection of available chasses **702**, where the configured computation module may be removably coupled to the selected chasses.

[0048] In this way, a socketed personal computer platform may be created which may be leveraged across a wide variety of chassis designs the best suit a given application or usage. Additionally, core personal computer components may be present on a proprietary card design and may be swapped between chassis. Further, a wide variety of different chasses (e.g., notebook, desktop, automotive, etc.) may be provided, and television and other display vendors may offer devices with either the computation module included or available as a separate module to update displays in the future.

[0049] Also, multiple inexpensive empty chassis may be purchased for use with a single computation module, instead of purchasing multiple expensive independent computer systems. Further still, personal information stored within the computation module may be secured within the computation module and may be moved with the computation module from chassis to chassis. In addition, the product life cycle of the computation module is separated from the product life cycle of the chassis - a user may upgrade the computation module (e.g., to a higher performance category, etc.) without having to upgrade chasses, and can upgrade one or more chasses without having to upgrade the computation module.

[0050] Figure **8** illustrates an exemplary system **800** in which the various architecture and/or functionality of the various previous embodiments may be implemented. As shown, a system **800** is provided including at least one host processor **801** which is connected to a communication bus **802**. The system **800** also includes a main memory **804**. Control logic (software) and data are stored in the main memory **804** which may take the form of random access memory (RAM).

[0051] The system **800** also includes a graphics processor **806** and a display **808**, i.e. a computer monitor. In one embodiment, the graphics processor **806** may include a plurality of shader modules, a rasterization module, etc. Each of the foregoing modules may even be situated on a single semiconductor platform to form a graphics processing unit (GPU).

[0052] In the present description, a single semiconductor platform may refer to a sole unitary semiconductor-based integrated circuit or chip. It should be noted that the term single semiconductor platform may also refer to multi-chip modules with increased connectivity which simulate on-chip operation, and make substantial improvements over utilizing a conventional central processing unit (CPU) and bus implementation. Of course, the various modules may also be situated separately or in various combinations of semiconductor platforms per the desires of the user.

[0053] The system **800** may also include a secondary storage **810**. The secondary storage **810** includes, for example, a hard disk drive and/or a removable storage drive, representing a floppy disk drive, a magnetic tape drive, a compact disk drive, etc. The removable storage drive reads from and/or writes to a removable storage unit in a well known manner.

[0054] Computer programs, or computer control logic algorithms, may be stored in the main memory **804** and/or the secondary storage **810**. Such computer programs, when executed, enable the system **800** to perform various functions. Memory **804**, storage **810** and/or any other storage are possible examples of computer-readable media.

[0055] In one embodiment, the architecture and/or functionality of the various previous figures may be implemented in the context of the host processor **801**, graphics processor **806**, an integrated circuit (not shown) that is capable of at least a portion of the capabilities of both the host processor **801** and the graphics processor **806**, a chipset (i.e.

a group of integrated circuits designed to work and sold as a unit for performing related functions, etc.), and/or any other integrated circuit for that matter.

[0056] Still yet, the architecture and/or functionality of the various previous figures may be implemented in the context of a general computer system, a circuit board system, a game console system dedicated for entertainment purposes, an application-specific system, and/or any other desired system. For example, the system **800** may take the form of a desktop computer, laptop computer, and/or any other type of logic. Still yet, the system **800** may take the form of various other devices m including, but not limited to a personal digital assistant (PDA) device, a mobile phone device, a television, etc.

[0057] Further, while not shown, the system **800** may be coupled to a network [e.g. a telecommunications network, local area network (LAN), wireless network, wide area network (WAN) such as the Internet, peer-to-peer network, cable network, etc.) for communication purposes.

[0058] While various embodiments have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of a preferred embodiment should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

CLAIMS

What is claimed is:

1. A method, comprising:

receiving input data at a computation module, utilizing a chassis removably coupled to the computation module;

performing one or more operations on the data, utilizing the computation module; and

providing output data from the computation module, utilizing the chassis.

2. The method of claim 1, wherein the chassis includes a computer system form factor with one or more data processing elements.

3. The method of claim 1, wherein the chassis includes a computer system form factor without one or more data processing elements.

4. The method of claim 1, wherein the computation module includes a system on a chip (SOC).

5. The method of claim 1, wherein the computation module includes a connector for coupling the computation module to the chassis.

6. The method of claim 1, wherein the computation module includes a locking platform.

7. The method of claim 6, wherein the locking platform includes one or more of a hardware lock and a software lock.

8. The method of claim 1, wherein the input data is received at the computation module through one or more data entry elements of the chassis.

9. The method of claim 1, wherein the one or more operations are performed on the data only if criteria associated with one or more security measures included within the computation module are met.

10. The method of claim 1, wherein the output data is provided from the computation module through one or more data output elements of the chassis.

11. The method of claim 1, wherein the computation module supplements one or more elements of the chassis during the performing of the one or more operations.

12. The method of claim 11, wherein the input data represents a portion of a larger set of data input to the chassis, where the input data is offloaded from the chassis to the computation module.

13. The method of claim 1, wherein a portion of the processing is performed by a processor on the chassis, and another portion of the processing is performed by the computation module.

14. The method of claim 1, wherein the processing includes one or more of graphics processing, network processing, and sound processing.

15. The method of claim 1, wherein a hardware lock is implemented within the computation module, and such hardware lock requires a key contained within a universal serial bus (USB) device for the computation module to operate.

16. The method of claim 1, wherein the computation module is placed within a cavity of the chassis and is coupled to the chassis using an internal connector located within the chassis.

17. The method of claim 5, wherein a predetermined number of pins of the connector are dedicated to a bi-directional display connection, a predetermined number of pins of the connector are dedicated to a bi-directional data connection, and a predetermined number of pins of the connector are dedicated to a locking platform of the computation module.

18. A computer program product embodied on a computer readable medium, comprising:

code for receiving input data at a computation module, utilizing a chassis removably coupled to the computation module;

code for performing one or more operations on the data, utilizing the computation module; and

code for providing output data from the computation module, utilizing the chassis.

19. A system, comprising:

a computation module removably coupled to a chassis, the computation module for receiving input data utilizing the chassis, performing one or more operations on the data, and providing output data, utilizing the chassis.

20. The system of claim 19, wherein the computation module includes memory coupled to a processor via a bus.

ABSTRACT

A system, method, and computer program product are provided for performing operations on data utilizing a computation module. In use, input data is received at a computation module, utilizing a chassis removably coupled to the computation module. Additionally, one or more operations are performed on the data, utilizing the computation module. Further, output data is provided from the computation module, utilizing the chassis.

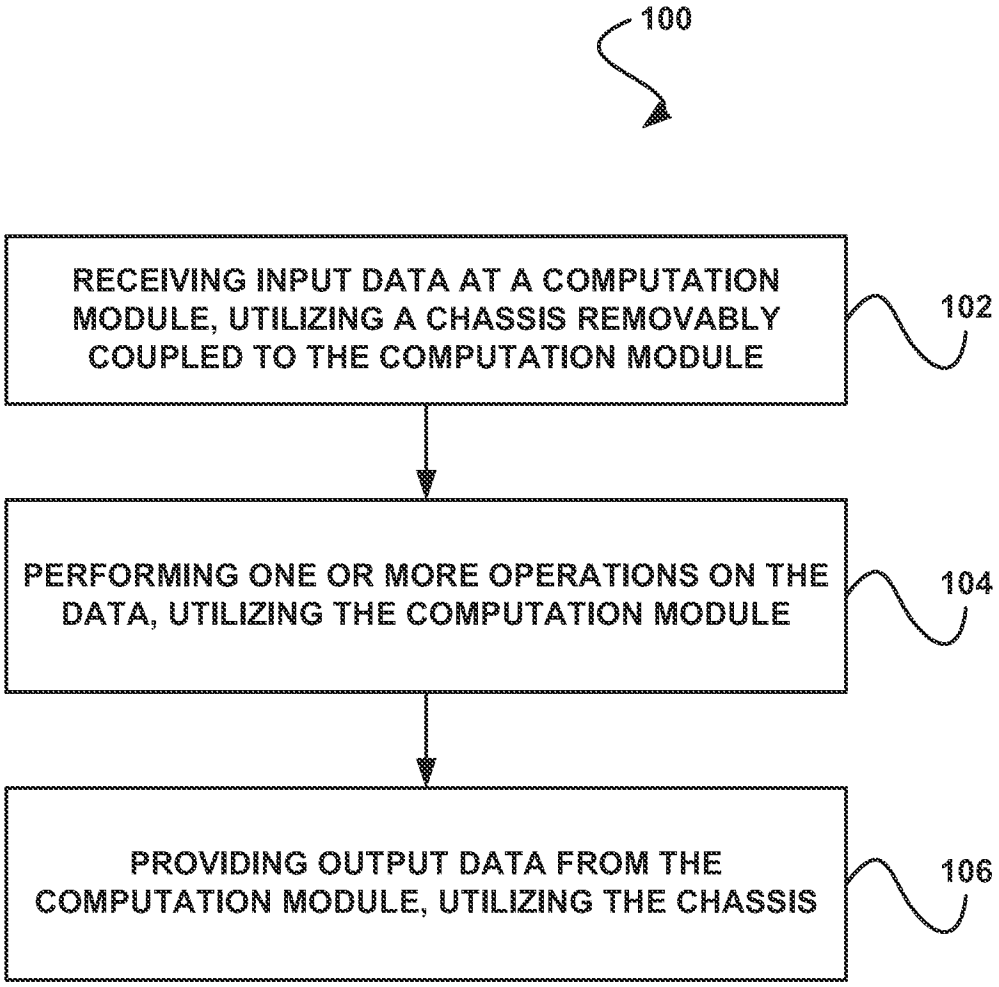
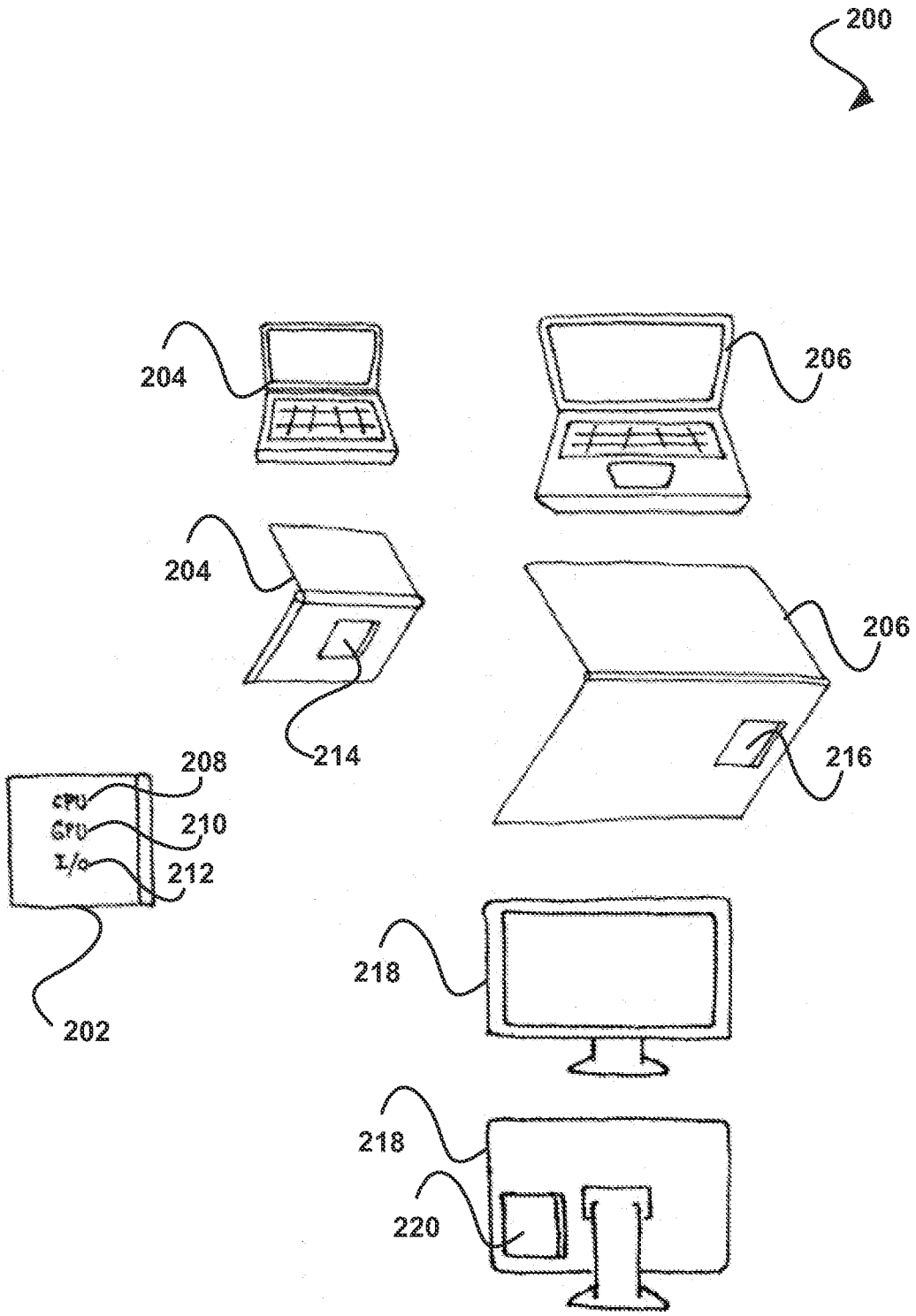

100
RECEIVING INPUT DATA AT A COMPUTATION MODULE, UTILIZING A CHASSIS REMOVABLY COUPLED TO THE COMPUTATION MODULE
102
PERFORMING ONE OR MORE OPERATIONS ON THE DATA, UTILIZING THE COMPUTATION MODULE
104
PROVIDING OUTPUT DATA FROM THE COMPUTATION MODULE, UTILIZING THE CHASSIS
106

FIGURE 1


200
204
206
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206
214
216
208
CPU
210
GPU
212
I/O
202
218
218
220

FIGURE 2

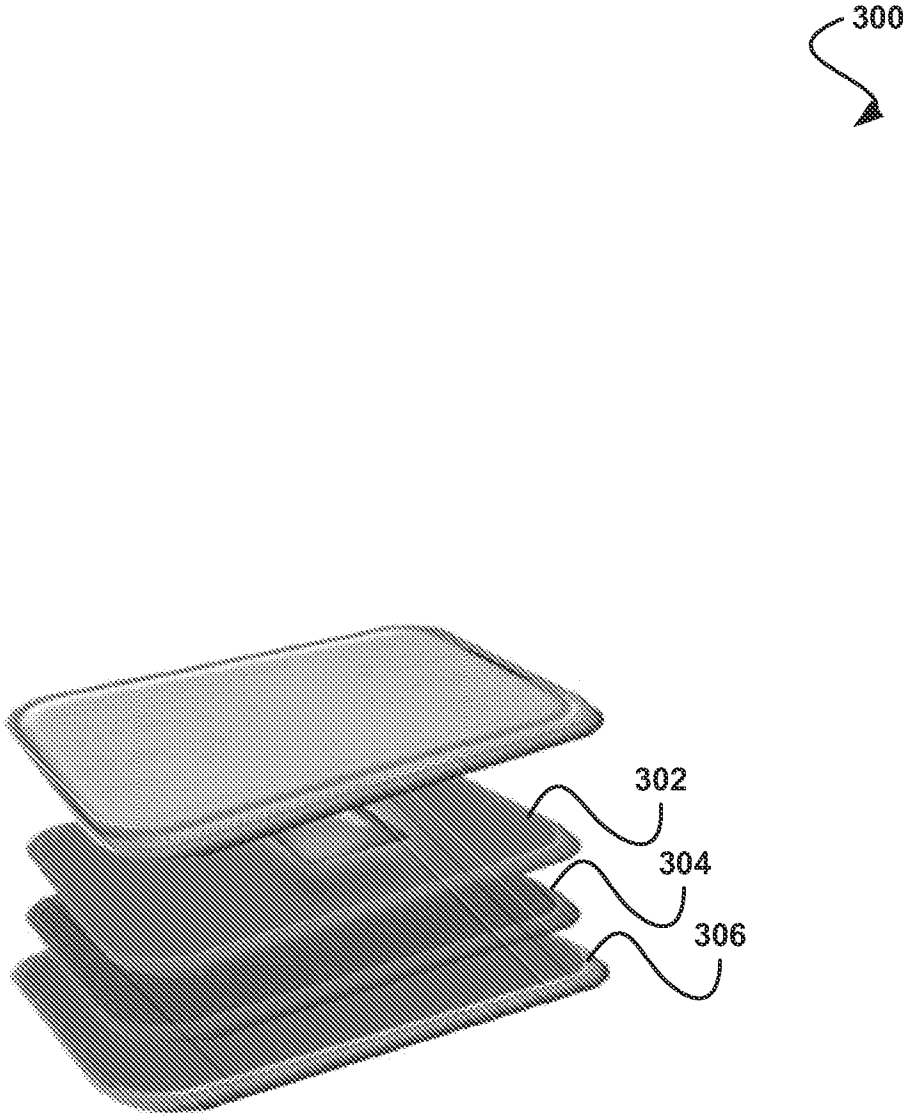


FIGURE 3

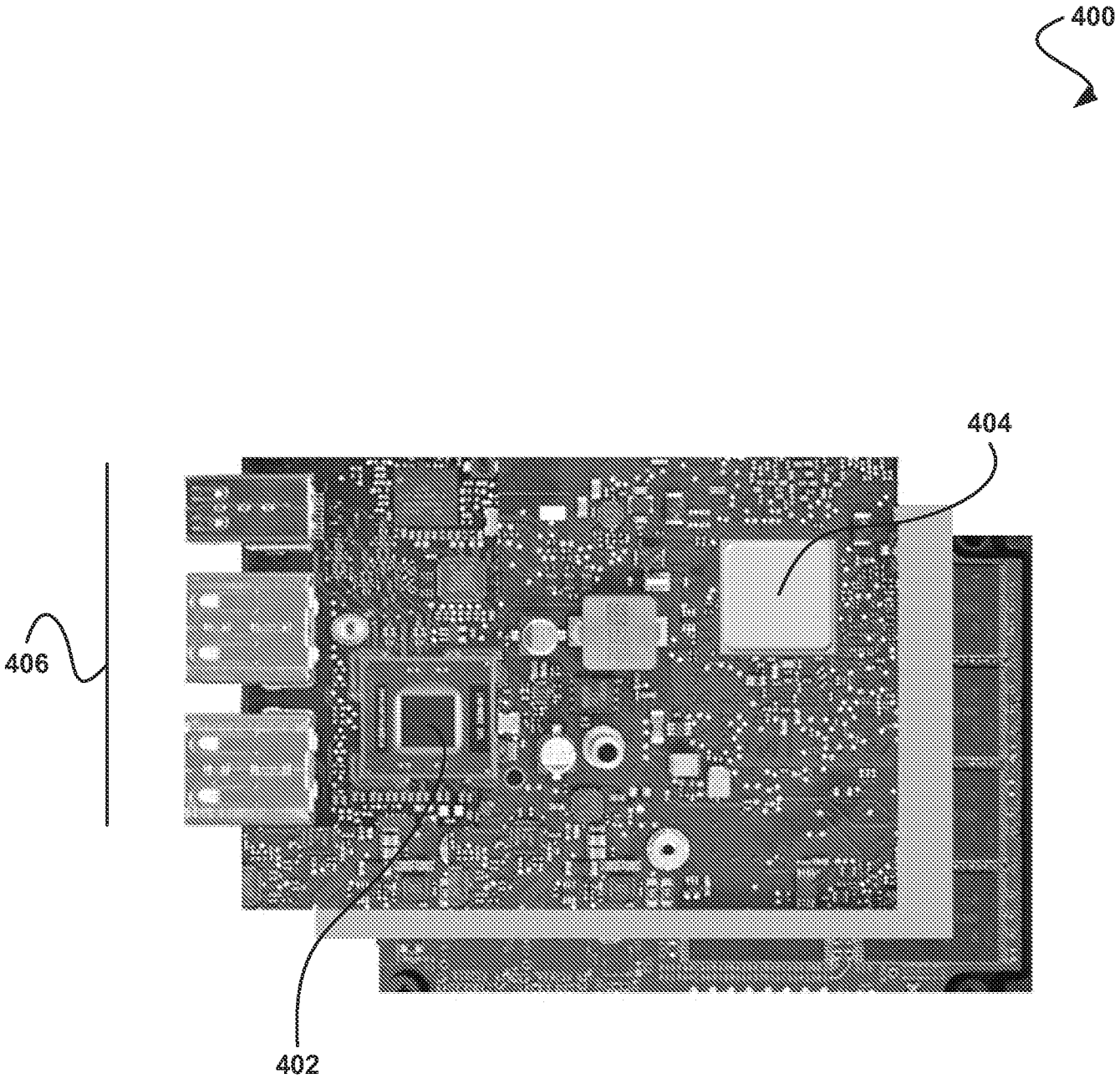


FIGURE 4

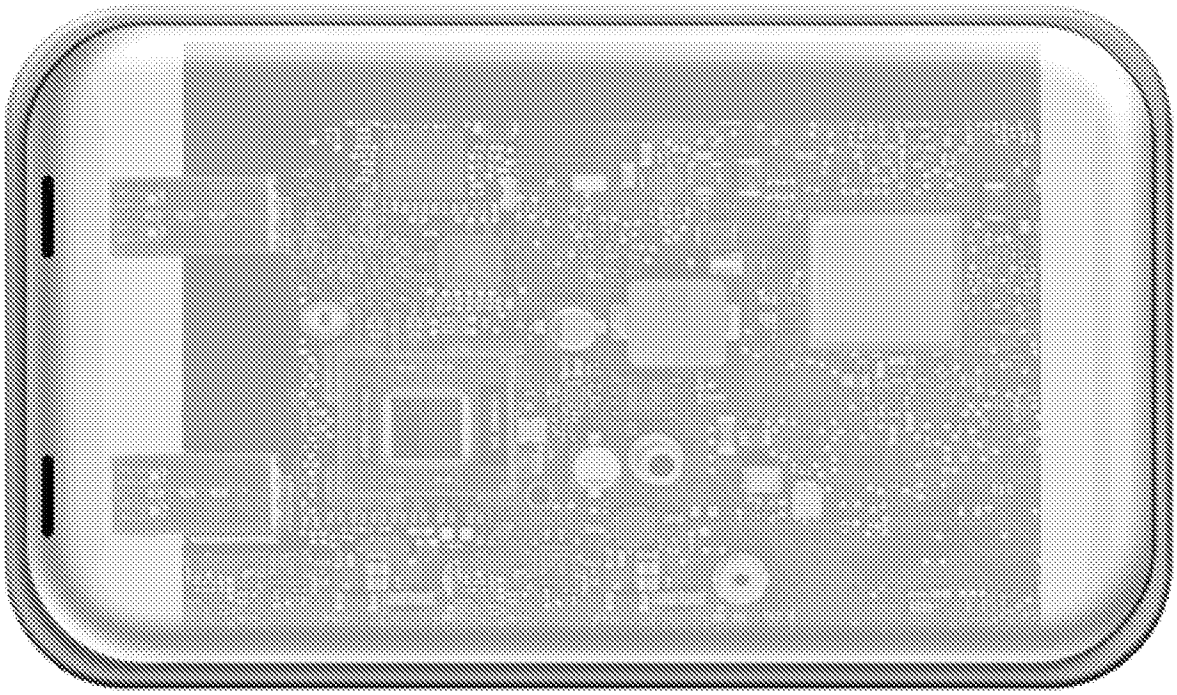


FIGURE 5

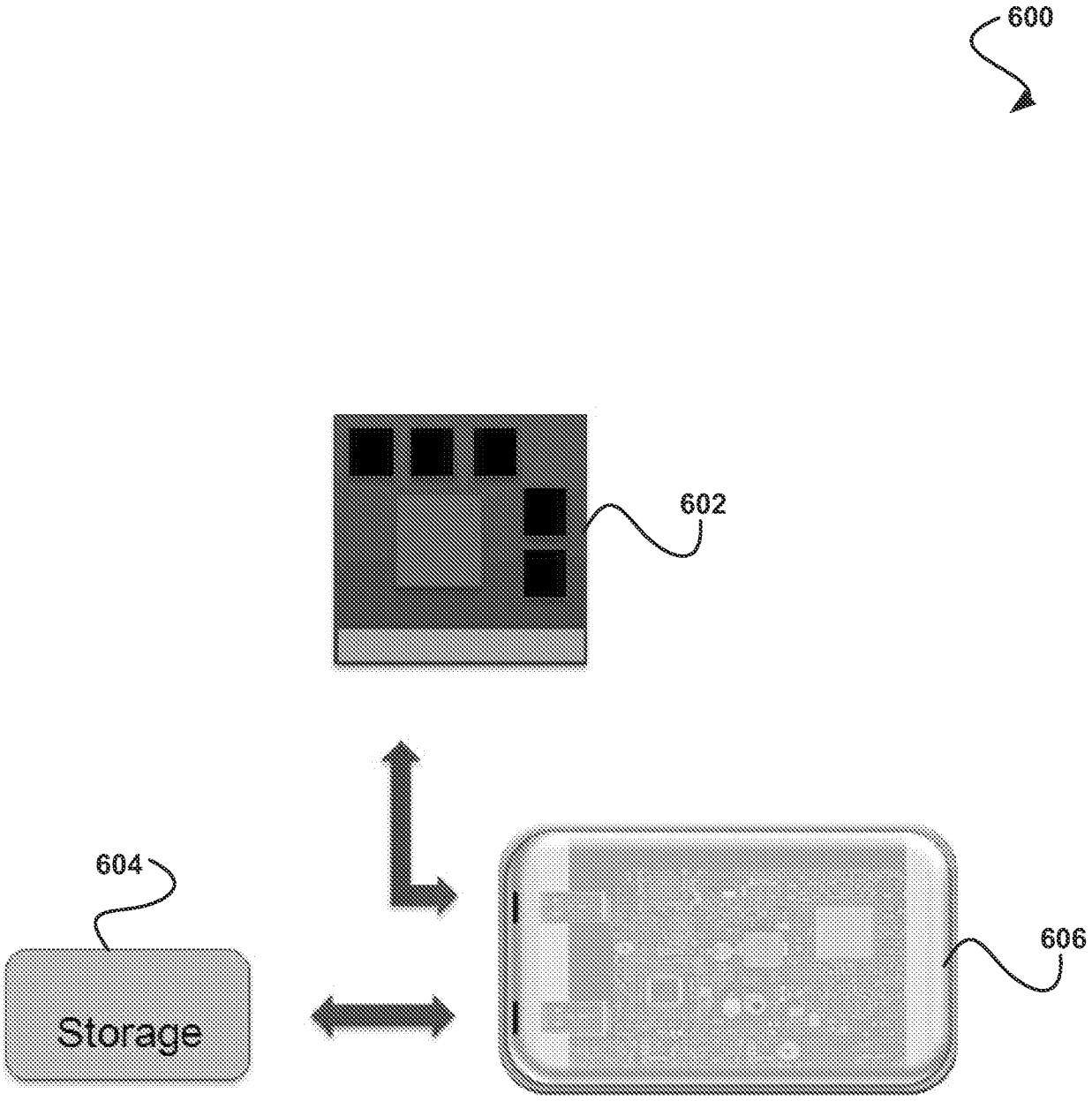
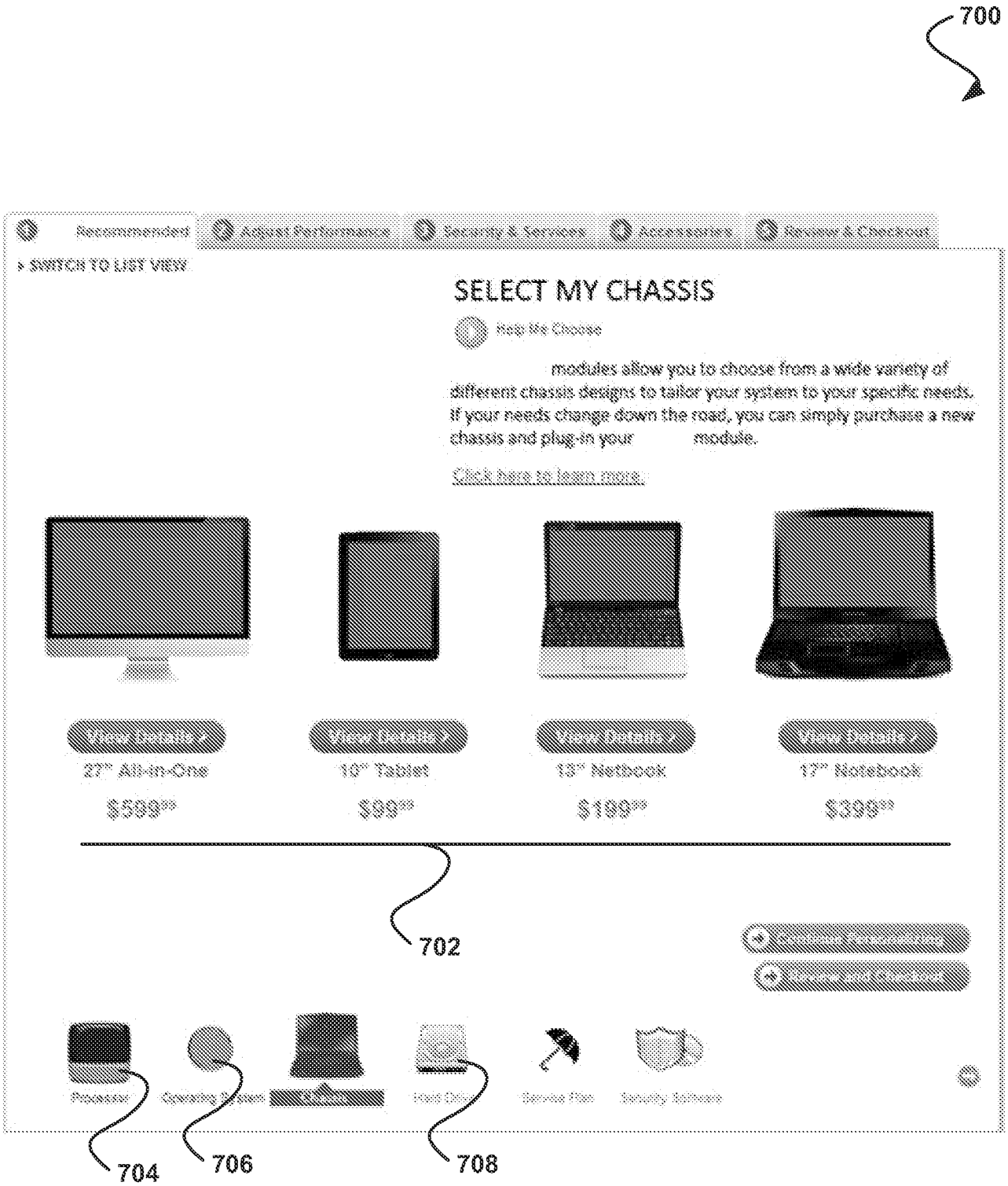


FIGURE 6


700
Recommended
Adjust Performance
Security & Services
Accessories
Review & Checkout
> SWITCH TO LIST VIEW
SELECT MY CHASSIS
Help Me Choose
modules allow you to choose from a wide variety of different chassis designs to tailor your system to your specific needs. If your needs change down the road, you can simply purchase a new chassis and plug-in your module.
Click here to learn more.
View Details >
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$599.99
View Details >
10" Tablet
$99.99
View Details >
13" Netbook
$199.99
View Details >
17" Notebook
$399.99
702
704
706
708

FIGURE 7

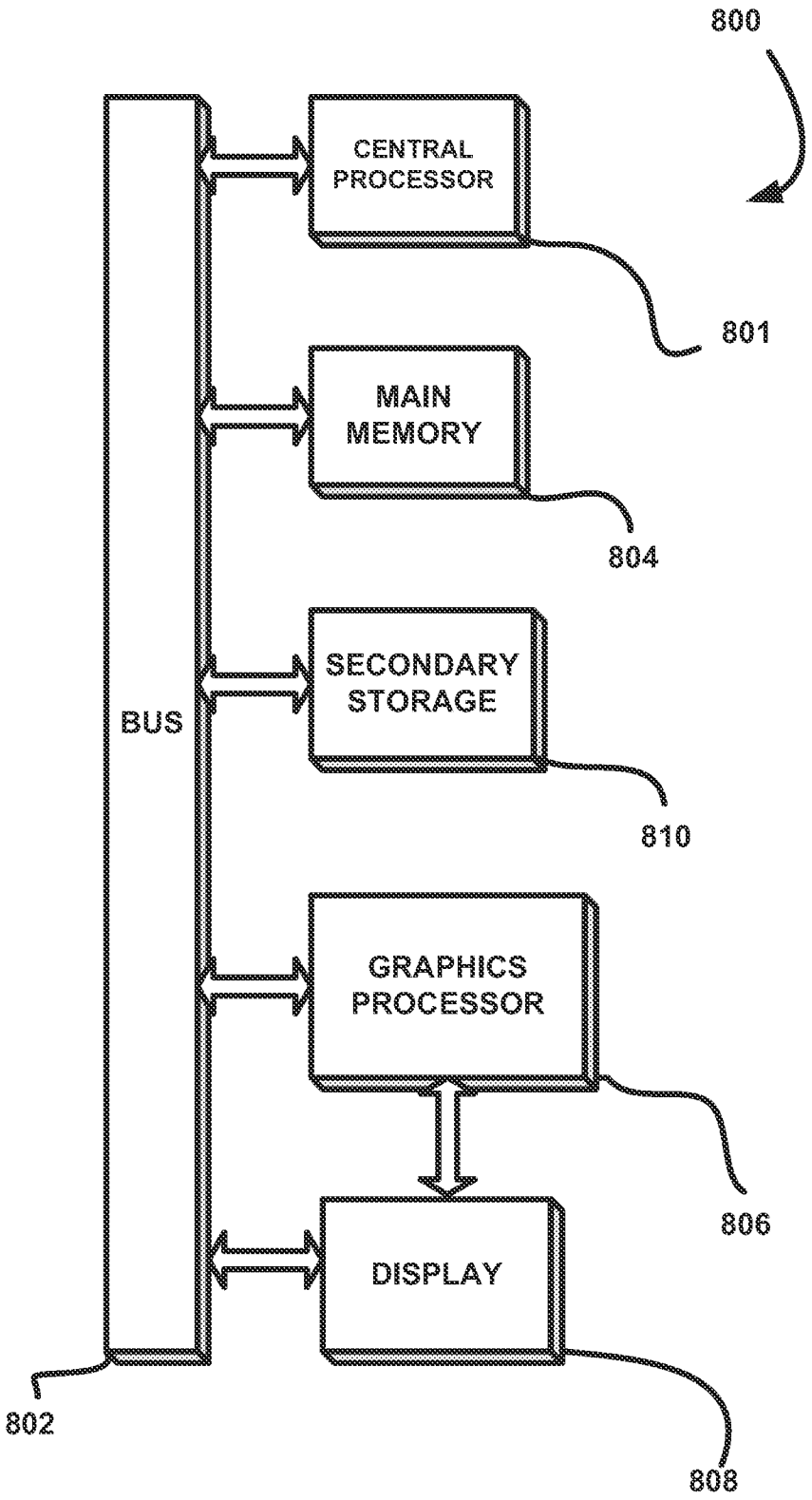
800
CENTRAL PROCESSOR
801
MAIN MEMORY
804
SECONDARY STORAGE
810
BUS
GRAPHICS PROCESSOR
806
DISPLAY
802
808

FIGURE 8

DECLARATION AND POWER OF ATTORNEY FOR ORIGINAL U.S. PATENT APPLICATION

Attorney's Docket No. NVIDP679/SC-09-0042-US1

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE, the specification of which,

(check one)

1. ☒ is attached hereto.

2. ☐ was filed on _____ as
U.S. Application Serial No. _____
and was amended on _____.

3. ☐ was filed on _____ as
International PCT Application Serial No. _____
and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, CFR § 1.56.

I hereby claim foreign priority benefits under Title 35, United States code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Appl. No.)	(Country)	(Filing Date)	Priority Benefits Claimed?
			☐Yes ☐No
			☐Yes ☐No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s)

(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)

And I hereby appoint the following attorney(s) and/or agents associated with PTO Customer Number 75359 as my principal agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Send Correspondence To: **75359**
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San Jose, California 95172-1120

Direct Telephone Calls To: **Jamie L. Rossi at telephone number (408) 971-2573**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Typewritten Full Name of Sole or First Inventor (if any): Sean Michael Pelletier Citizenship: USA

Inventor's signature: _____ **Date of Signature:** 12/22/11

Residence: (City) Austin (State/Country) TX/USA

Post Office Address: 10600 Leafwood Lane, Austin, TX 78750

Attorney Docket No.: NVIDP679/SC-09-0042-US1

Neural AI, LLC, Exhibit 2019
Page 2019 - 204
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NVIDP679/SC-09-0042-US1
	Application Number	
Title of Invention	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Sean	Michael	Pelletier	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Austin	State/Province	TX	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i

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Address 2			
City	Austin	State/Province	TX
Postal Code	78750	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	75359		
Email Address	zk-uspto@zilkakotab.com	Add Email	Remove Email

Application Information:

Title of the Invention	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE		
Attorney Docket Number	NVIDP679/SC-09-0042-US1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NVIDP679/SC-09-0042-US1
	Application Number	
Title of Invention	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	75359		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NVIDP679/SC-09-0042-US1
	Application Number	
Title of Invention	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE	

If the Assignee is an Organization check here. ☒			
Organization Name	NVIDIA Corporation		
Mailing Address Information:			
Address 1	2701 San Tomas Expressway		
Address 2			
City	Santa Clara	**State/Province**	CA
Country i	US	Postal Code	95050
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/JAMIE ROSSI/			Date (YYYY-MM-DD)	2011-12-22
First Name	Jamie	Last Name	Rossi	Registration Number	56875

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Filer:	Jamie Lynn Rossi/Justin Bocchino
Attorney Docket Number:	NVIDP679/SC-09-0042-US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1250**

Electronic Acknowledgement Receipt

EFS ID:	11696877
Application Number:	13335850
International Application Number:	
Confirmation Number:	2112
Title of Invention:	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR PERFORMING OPERATIONS ON DATA UTILIZING A COMPUTATION MODULE
First Named Inventor/Applicant Name:	Sean Michael Pelletier
Customer Number:	75359
Filer:	Jamie Lynn Rossi/Justin Bocchino
Filer Authorized By:	Jamie Lynn Rossi
Attorney Docket Number:	NVIDP679/SC-09-0042-US1
Receipt Date:	22-DEC-2011
Filing Date:	
Time Stamp:	20:39:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1250
RAM confirmation Number	9907
Deposit Account	501351
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NVIDP679_ApplicationAsFiled_12-22-2011.pdf	1581779 c8bf487980a8f13cb117ffec551f0e2f2e857fc6	yes	32

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	1
Specification	2	18
Claims	19	21
Abstract	22	22
Drawings-only black and white line drawings	23	30
Oath or Declaration filed	31	32

Warnings:

Information:

2	Application Data Sheet	NVIDP679_ADS_12-22-2011.pdf	1031728 8fdf515d2b5102eed4eeea7a1a3cc07dff43cc86	no	4

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	33375 bc4c1828f2fc158327f16494fa161cd2efc35f8a	no	2

Warnings:

Information:

Total Files Size (in bytes):	2646882

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 13335850 Document Date: 12/22/2011

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

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- Examiners may access SCORE content via the eDAN interface.
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Form Revision Date: February 8, 2006