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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0167.0001US1
	Application Number	

Title of Invention	Graphic Processor Based Accelerator System and Method

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Title of Invention	Graphic Processor Based Accelerator System and Method	

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☐ **An Address is being provided for the correspondence Information of this application.**

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Application Information:

Title of the Invention	Graphic Processor Based Accelerator System and Method		
Attorney Docket Number	0167.0001US1	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	**Suggested Figure for Publication (if any)**	

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Publication Information:

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☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application has not **and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Prior Application Status			Remove
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	non provisional of	60826892	2006-09-25

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Signature:

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Signature	/grant houston/			Date (YYYY-MM-DD)	2007-09-24
First Name	J. Grant	Last Name	Houston	Registration Number	35900

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TITLE OF THE INVENTION

Graphic Processor Based Accelerator System and Method

RELATED APPLICATIONS

[0001] This application claims the benefit under 35 USC 119(e) of U.S. Provisional Application No. 60/826,892, filed on September 25, 2006, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] Graphics Processing Units (GPUs) are found in video adapters (graphic cards) of most personal computers (PCs), video game consoles, workstations, etc. and are considered highly parallel processors dedicated to fast computation of graphical content. With the advances of the computer and console gaming industries, the need for efficient manipulation and display of 3D graphics has accelerated the development of GPUs.

[0003] In addition, manufacturers of GPUs have included general purpose programmability into the GPU architecture leading to the increased popularity of using GPUs for highly parallelizable and computationally expensive algorithms outside of the computer graphics domain. When implemented on conventional video card architectures, these general purpose GPU (GPGPU) applications are not able to achieve optimal performance, however. There is overhead for graphics-related features and algorithms that are not necessary for these non-video applications.

SUMMARY OF THE INVENTION

[0004] Numerical simulations, *e.g.,* finite element analysis, of large systems of similar elements (e.g. neural networks, genetic algorithms, particle systems, mechanical systems) are one example of an application that can benefit from GPGPU computation. During numerical simulations, disk and user input/output can be performed independently of computation because these two processes require interactions with peripheral hardware (disk, screen, keyboard, mouse, etc) and put relatively low load on the central processing unit/system (CPU).

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Complete independence is not desirable, however; user input might affect how the computation is performed and even interrupt it if necessary. Furthermore, the user output and the disk output are dependent on the results of the computation. A reasonable solution would be to separate input/output into threads, so that it is interacting with hardware occurs in parallel with the computation. In this case whatever CPU processing is required for input/output should be designed so that it provides the synchronization with computation.

[0005] In the case of GPGPU, the computation itself is performed outside of the CPU, so the complete system comprises three "peripheral" components: user interactive hardware, disk hardware, and computational hardware. The central processing unit (CPU) establishes communication and synchronization between peripherals. Each of the peripherals is preferably controlled by a dedicated thread that is executed in parallel with minimal interactions and dependencies on the other threads.

[0006] A GPU on a conventional video card is usually controlled through OpenGL, DirectX, or similar graphic application programming interfaces (APIs). Such APIs establish the context of graphic operations, within which all calls to the GPU are made. This context only works when initialized within the same thread of execution that uses it. As a result, in a preferred embodiment, the context is initialized within a computational thread. This creates complications, however, in the interaction between the user interface thread that changes parameters of simulations and the computational thread that uses these parameters.

[0007] A solution as proposed here is an implementation of the computational stream of execution in hardware, so that thread and context initialization are replaced by hardware initialization. This hardware implementation includes an expansion card comprising a printed circuit board having (a) one or more graphics processing units, (b) two or more associated memory banks that are logically or physically partitioned, (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the CPU is freed from this function and is dedicated to other tasks.

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In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

[0008] In general, according to one aspect, the invention features a computer system. This system comprises a central processing unit, main memory accessed by the central processing unit, and a video system for driving a video monitor in response to the central processing unit as is common. The computer system further comprises an accelerator that uses input data from and provides output data to the central processing unit. This accelerator comprises at least one graphics processing unit, accelerator memory for the graphic processing unit, and an accelerator controller that moves the input data into the at least one graphics processing unit and the accelerator memory to generate the output data.

[0009] In the preferred, the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit. Preferably, the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit. The use of the separate controller enables data transfer during execution such that the accelerator controller transfers output data from the accelerator memory to main memory of the central processing unit.

[0010] In the preferred embodiment, the accelerator controller comprises an interface controller that enables the accelerator to communicate over a bus of the computer system with the central processing unit.

[0011] In general according to another aspect, the invention also features an accelerator system for a computer system, which comprises at least one graphics processing unit, accelerator memory for the graphic processing unit and an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory.

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[0012] In general according to another aspect, the invention also features a method for performing numerical simulations in a computer system. This method comprises a central processing unit loading input data into an accelerator system from main memory of the central processing unit and an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data. The accelerator controller then transfers output data generated by the graphic processing unit to the central processing unit as output data.

[0013] The above and other features of the invention including various novel details of construction and combinations of parts, and other advantages, will now be more particularly described with reference to the accompanying drawings and pointed out in the claims. It will be understood that the particular method and device embodying the invention are shown by way of illustration and not as a limitation of the invention. The principles and features of this invention may be employed in various and numerous embodiments without departing from the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] In the accompanying drawings, reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale; emphasis has instead been placed upon illustrating the principles of the invention. Of the drawings:

[0015] FIG. 1 is a schematic diagram illustrating a computer system including the GPU accelerator according to an embodiment of the present invention;

[0016] FIG. 2 is block diagram illustrating the architecture for the GPU accelerator according to an embodiment of the present invention;

[0017] FIG. 3 is a block/flow diagram illustrating an exemplary implementation of the top level control of the GPU accelerator system;

[0018] FIG. 4 is a flow diagram illustrating an exemplary implementation of the bottom level control of the CPU accelerator system that is used to execute the target computation; and

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[0019] FIG. 5 is an example population of nine computational elements arranged in a 3x3 square and a potential packing scheme for texture pixels, according to an implementation of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] The hardware

[0021] FIG. 1 shows a computer system 100 that has been constructed according to the principles of the present invention.

[0022] In more detail, the computer system 100 in one example is a standard personal computer (PC). However, this only serves as an example environment as computing environment 100 does not necessarily depend on or require any combination of the components that are illustrated and described herein. In fact, there are many other suitable computing environments for this invention, including, but not limited to, workstations, server computers, supercomputers, notebook computers, hand-held electronic devices such as cell phones, mp3 players, or personal digital assistants (PDAs), multiprocessor systems, programmable consumer electronics, networks of any of the above-mentioned computing devices, and distributed computing environments that including any of the above-mentioned computing devices.

[0023] In one implementation the GPU accelerator is implemented as an expansion card 180 includes connections with the motherboard 110, on which the one or more CPU's 120 are installed along with main, or system memory 130 and mass/non volatile data storage 140, such as hard drive or redundant array of independent drives (RAID) array, for the computer system 100. In the current example, the expansion card 180 communicates to the motherboard 110 via a local bus 190. This local bus 190 could be PCI, PCI Express, PCI-X, or any other functionally similar technology (depending upon the availability on the motherboard 110). An external version GPU accelerator is also a possible implementation. In this example, the external GPU accelerator is connected to the motherboard 110 through USB-2.0, IEEE 1394 (Firewire), or similar external/peripheral device interface.

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[0024] The CPU 120 and the system memory 130 on the motherboard 110 and the mass data storage system 140 are preferably independent of the expansion card 180 and only communicate with each other and the expansion card 180 through the system bus 200 located in the motherboard 110. A system bus 200 in current generations of computers have bandwidths from 3.2GB/s (Pentium 4 with AGTL+, Athlon XP with EV6) to around 15GB/s (Xeon Woodcrest with AGTL+, Athlon 64/Opteron with Hypertransport), while the local bus has maximal peak data transfer rates of 4GB/s (PCI Express 16) or 2GB/s (PCI-X 2.0). Thus the local bus 190 becomes a bottleneck in the information exchange between the system bus 200 and the expansion card 180. The design of the expansion card and methods proposed herein minimizes the data transfer through the local bus 190 to reduce the effect of this bottleneck.

[0025] The system memory 130 is referred to as the main random-access memory (RAM) in the description herein. However, this is not intended to limit the system memory 130 to only RAM technology. Other possible computer storage media include, but are not limited to ROM, EEPROM, flash memory, or any other memory technology.

[0026] In the illustrated example, the GPU accelerator system is implemented on an expansion card 180 on which the one or more GPU's 240 are mounted. It should be noted that the GPU accelerator system GPU 240 is separate from and independent of any GPU on the standard video card 150 or other video driving hardware such as integrated graphics systems. Thus the computations performed on the expansion card 180 do not interfere with graphics display (including but not limited to manipulation and rendering of images).

[0027] Various brand of GPU are relevant. Under current technology, GPU's based on the GeForce series from NVIDIA Corporation or the Catalyst series from ATI/Advanced Micro Devices, Inc.

[0028] The output to a video monitor 170 is preferably through the video card 150 and not the GPU accelerator system 180. The video card 150 is dedicated to the transfer of graphical information and connects to the motherboard 110 through a local bus 160 that is sometimes

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physically separate from the local bus 190 that connects the expansion card 180 to the motherboard 110.

[0029] FIG. 2 is a block diagram illustrating the general architecture of the GPU accelerator system and specifically the expansion card 180 in which at least one GPU 240 and associated memories 210 and 250 are mounted. Electrical (signal) and mechanical coupling with a local bus 190 provides signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI, PCI-X, PCI Express, or functionally similar technology).

[0030] The GPU accelerator further preferably comprises one specifically designed accelerator controller 220. Depending upon the implementation, the accelerator controller 220 is field programmable gate array (FPGA) logic, or custom built application-specific (ASIC) chip mounted in the expansion card 180, and in mechanical and signal coupling with the GPU 240 and the associated memories 210 and 250. During initial design, a controller can be partially or even fully implemented in software, in one example.

[0031] The controller 220 commands the storage and retrieval of arrays of data (on a conventional video card the arrays of data are represented as textures, hence the term 'texture' in this document refers to a data array unless specified otherwise and each element of the texture is a pixel of color information), execution of GPU programs (on a conventional video card these programs are called shaders, hence the term 'shader' in this document refers to a GPU program unless specified otherwise), and data transfer between the system bus 200 and the expansion card 180 through the local bus 190 which allows communication between the main CPU 120, RAM 130, and disk 140.

[0032] Two memory banks 210 and 250 are mounted on the expansion card 180. In some example, these memory banks separated in the hardware, as shown, or alternatively implemented as a single, logically partitioned memory component.

[0033] The reason to separate the memory into two partitions 210 250 stems from the nature of the computations to which the GPU accelerator system is applied. The elements of computation (computational elements) are characterized by a single output variable. Such

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computational elements often include one or more equations. Computational elements are same or similar within a large population and are computed in parallel. An example of such a population is a layer of neurons in an artificial neural network (ANN), where all neurons are described by the same equation. As a result, some data and most of the algorithms are common to all computational elements within population, while most of the data and some algorithms are specific for each equation. Thus, one memory, the shader memory bank 210, is used to store the shaders needed for the execution of the required computations and the parameters that are common for all computational elements and is coupled with the controller 220 only. The second memory, the texture memory bank 250, is used to store all the necessary data that are specific for every computational element (including, but not limited to, input data, output data, intermediate results, and parameters) and is coupled with both the controller 220 and the GPU 240.

[0034] The texture memory bank 250 is preferably further partitioned into four sections. The first partition 250a is designed to hold the external input data patterns. The second partition 250b is designed to hold the data textures representing internal variables. The third partition 250c is designed to hold the data textures used as input at a particular computation step on the GPU 240. The fourth partition 250d holds the data textures used to accommodate the output of a particular computational step on the GPU 240. This partitioning scheme can be done logically, does not require hardware implementation. Also the partitioning scheme is also altered based on new designs or needs of the algorithms being employed. The reason for this partitioning is further explained in the Data Organization section, below.

[0035] A local bus interface 230 on the controller 220 serves as a driver that allows the controller 220 to communicate through the local bus 190 with the system bus 200 and thus the CPU 120 and RAM 130. This local bus interface 230 is not intended to be limited to PCI related technology. Other drivers can be used to interface with comparable technology as a local bus 190.

[0036] Data organization

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[0037] Each computational element discussed above has output variables that affect the rest of the system. For example in the case of a neural network it is the output of a neuron. A computational element also usually has several internal variables that are used to compute output variables, but are not exposed to the rest of the system, not even to other elements of the same population, typically. Each of these variables is represented as a texture. The important difference between output variables and internal variables is their access.

[0038] Output variables are usually accessed by any element in the system during every time step. The value of the output variable that is accessed by other elements of the system corresponds to the value computed on the previous, not the current, time step. This is realized by dedicating two textures to output variables – one holds the value computed during the previous time step and is accessible to all computational elements during the current time step, another is not accessible to other elements and is used to accumulate new values for the variable computed during the current time step. In-between time steps these two textures are switched, so that newly accumulated values serve as accessible input during the next time step, while the old input is replaced with new values of the variable. This switch is implemented by swapping the address pointers to respective textures as described in the System and Framework section.

[0039] Internal variables are computed and used within the same computational element. There is no chance of a race condition in which the value is used before it is computed or after it has already changed on the next time step because within an element the processing is sequential. Therefore, it is possible to render the new value of internal variable into the same texture where the old was read from in the texture memory bank. Rendering to more than one texture from a single shader is not implemented in current GPU architectures, so computational elements that track internal variables would have to have one shader per variable. These shaders can be executed in order with internal variables computed first, followed by output variables.

[0040] Further savings of texture memory is achieved through using multiple color components per pixel (texture element) to hold data. Textures can have up to four color

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components that are all processed in parallel on a GPU. Thus, to maximize the use of GPU architecture it is desirable to pack the data in such a way that all four components are used by the algorithm. Even though each computational element can have multiple variables, designating one texture pixel per element is ineffective because internal variables require one texture and output variables require two textures. Furthermore, different element types have different numbers of variables and unless this number is precisely a multiple of four, texture memory can be wasted.

[0041] A more reasonable packing scheme would be to pack four computational elements into a pixel and have separate textures for every variable associated with each computational element. In this case the packing scheme is identical for all textures, and therefore can be accessed using the same algorithm. Several ways to approach this packing scheme are outlined here. An example population of nine computational elements arranged in a 3x3 square (FIG. 5a) can be packed by element (FIG. 5b), by row (FIG. 5c), or by square (FIG. 5d).

[0042] Packing by element (FIG. 5b) means that elements 1,2,3,4 go into first pixel; 5,6,7,8 go into second pixel; 9 goes into third pixel. This is the most compact scheme, but not convenient because the geometrical relationship is not preserved during packing and its extraction depends on the size of the population.

[0043] Packing by row (column; FIG. 5c) means that elements 1,2,3 go into pixel (1,1); 3,4,5 go into pixel (2,1), 7,8,9 go into pixel (3,1). With this scheme the element's y coordinate in the population is the pixel's y coordinate, while the element's x coordinate in the population is the pixel's x coordinate times four plus the index of color component. Five by five populations in this case will use 2x5 texture, or 10 pixels. Five of these pixels will only use one out of four components, so it wastes 37.5% of this texture. 25x1 population will use 6x1 texture (six pixels) and will waste 12.5% of it.

[0044] Packing by square (FIG. 5d) means that elements 1,2,4,5 go into pixel (1,1); 3,6 go into pixel (1,2); 7,8 go into pixel (2,1), and 9 goes into pixel (2,2). Both the row and the column of the element are determined from the row (column) of the pixel times two plus the

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second (first) bit of the color component index. Five by five populations in this case will use 3x3 texture, or 9 pixels. Four of these pixels will only use two out of four components, and one will only use one component, so it wastes 34.4% of this texture. This is more advantageous than packing by row, since the texture is smaller and the waste is also lower. 25x1 population on the other hand will use 13x1 texture (thirteen pixels) and waste >50% of it, which is much worse than packing by row.

[0045] In order to eliminate waste altogether the population should have even dimensions in the square packing, and it should have a number of columns divisible by four in row packing. Theoretically, the chances are approximately equivalent for both of these cases to occur, so the particular task and data sizes should determine which packing scheme is preferable in each individual case.

[0046] The system and framework

[0047] FIG. 3 shows an exemplary implementation of the top level system and method that is used to control the computation. It is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented in the invention described herein and so the implementation is not intended to be limited to the following description and accompanying figure.

[0048] The method presented herein includes two execution streams that run on the CPU 120 – User Interaction Stream 302 and Data Output Stream 301. These two streams preferably do not interact directly, but depend on the same data accumulated during simulations. They can be implemented as separate threads with shared memory access and executed on different CPUs in the case of multi-CPU computing environment. The third execution stream – Computational Stream 303 – runs on the GPU accelerator of the expansion card 180 and interacts with the User Interaction Stream 302 through initialization routines and data exchange in between simulations. The Computational Stream 303 interacts with the User Interaction Stream and the Data Output Stream through synchronization procedures during simulations.

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[0049] The crucial feature of the interaction between the User Interaction Stream 302 and the Computational Stream 303 is the shift of priorities. Outside of the simulation, the system 100 is driven by the user input, thus the User Interaction Stream 302 has the priority and controls the data exchange 304 between streams. After the user starts the simulation, the Computational Stream 303 takes the priority and controls the data exchange between streams until the simulation is finished or interrupted 350.

[0050] The user starts 300 the framework through the means of an operating system and interacts with the software through the user interaction section 305 of the graphic user interface 306 executed on the CPU 120. The start 300 of the implementation begins with a user action that causes a GUI initialization 307, Disk input/output initialization 308 on the CPU 120, and controller initialization 320 of the GPU accelerator on the expansion card 180. GUI initialization includes opening of the main application window and setting the interface tools that allow the user to control the framework. Disk I/O initialization can be performed at the start of the framework, or at the start of each individual simulation.

[0051] The user interaction 305 controls the setting and editing of the computational elements, parameters, and sources of external inputs. It specifies which equations should have their output saved to disk and/or displayed on the screen. It allows the user to start and stop the simulation. And it performs standard interface functions such as file loading and saving, interactive help, general preferences and others.

[0052] The user interaction 305 directs the CPU 120 to acquire the new external input textures needed (this includes but is not limited to loading from disk 140 or receiving them in real time from a recording device), parses them if necessary 309, and initializes their transfer to the expansion card 180, where they are stored 325 in the texture memory bank 250 by the controller 220. The user interaction 305 also directs the CPU 120 to parse populations of elements that will be used in the simulation, convert them to GPU programs (shaders), compile them 310, and initializes their transfer to the expansion card 180, where they are stored 326 in the shader memory bank 210 by the controller 220. This operation is accompanied by the upload 309 of the initial data into the input partition of the texture

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memory bank 250, and stores the shader order of execution in the controller 220. The user can perform operations 309 and 310 as many times as necessary prior to starting the simulation or between simulations.

[0053] The editing of the system between simulations is difficult to accomplish without the hardware implementation of the computational thread suggested herein. The system of equations (computational elements) is represented by textures that track variables plus shaders that define processing algorithms. As mentioned above, textures, shaders and other graphics related constructs can only be initialized within the rendering context, which is thread specific. Therefore textures and shaders can only be initialized in the computational thread.

[0054] Network editing is a user-interactive process, which according to the scheme suggested above happens in the User Interaction Stream 302. The simulation software thus has to take the new parameters from the User Interaction Stream 302, communicate them to the Computational Stream 303 and regenerate the necessary shaders and textures. This is hard to accomplish without a hardware implementation of the Computational Stream 303. The Computational Stream 303 is forked from the User Interaction Stream and it can access the memory of the parent thread, but the reverse communication is harder to achieve. The controller 220 allows operations 309 and 310 to be performed as many times as necessary by providing the necessary communication to the User Interaction Stream 302.

[0055] After execution of the input parser texture generation 309 and population parser shader generator and compiler 310 are performed at least once, the user has the option to initialize the simulation 311. During this initialization the main control of the framework is transferred to the GPU accelerator system's accelerator controller 220 and computation 330 is started (see FIG. 4; 420). The user retains the ability to interrupt the simulation, change the input, or to change the display properties of the framework, but these interactions are queued to be performed at times determined by the controller-driven data exchange 314 and 316 to avoid the corruption of the data.

[0056] The progress monitor 312 is not necessary for performance, but adds convenience. It displays the percentage of completed time steps of the simulation and allows the user to

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plan the schedule using the estimates of the simulation wall clock times. Controller-driven data exchange 314 updates the display of the results 313. Online screen output for the user selected population allows the user to monitor the activity and evaluate the qualitative behavior of the network. Simulations with unsatisfactory behavior can be terminated early to change parameters and restart. Controller-driven data exchange 314 also drives the output of the results to disk 317. Data output to disk for convenience can be done on an element per file basis. A suggested file format includes a leftmost column that displays a simulated time for each of the simulation steps and subsequent columns that display variable values during this time step in all elements with identical equations (e.g. all neurons in a layer of a neural network).

[0057] Controller-driven data exchange or input parser texture generator 316 allows the user to change input that is generated on the fly during the simulation. This allows the framework monitoring of the input that is coming from a recording device (video camera, microphone, cell recording electrode, etc) in real time. Similar to the initial input parser 309, it preprocesses the input into a universal format of the data array suitable for texture generation and generates textures. Unlike the initial parser 309, here the textures are transferred to hardware not whenever ready but upon the request of the controller 220.

[0058] The controller 220 also drives the conditional testing 315 and 318 informs the CPU-bound streams whether the simulation is finished. If so, the control returns to the User Interaction Stream. The user then can change parameters or inputs (309 and 310), restart the simulation (311) or quit the framework (390).

[0059] SANNDRA (Synchronous Artificial Neuronal Network Distributed Runtime Algorithm; http://www.kinness.net/Docs/SANNDRA/html) was developed to accelerate and optimize processing of numerical integration of large non-homogenous systems of differential equations. This library is fully reworked in its version 2.x.x to support multiple computational backends including those based on multicore CPUs, GPUs and other processing systems. GPU based backend for SANNDRA-2.x.x can serve as an example practical software

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implementation of the method and architecture described above and pictorially represented in FIG. 3.

[0060] To use SANNDRA, the application should create a TSimulator object either directly or through inheritance. This object will handle global simulation properties and control the User Interaction Stream, Data Output Stream, and Computational Stream. Through TSimulator::timestep(), TSimulator::outfileInterval(), and TSimulator::outmode(), the application can set the time step of the simulation, the time step of disk output, and the mode of the disk output. The external input pattern should be packed into a TPattern object and bound to the simulation object through TSimulator::resetInputs() method. TSimulator::simLength() sets the length of the simulation.

[0061] The second step is to create at least one population of equations (TPopulation object). Population holds one equation object TEquation. This object contains only a formula and does not hold element-specific data, so all elements of the population can share single TEquation.

[0062] The TEquation object is converted to a GPU program before execution. GPU programs have to be executed within a graphical context, which is stream specific. TSimulator creates this context within a Computational Stream, therefore all programs and data arrays that are necessary for computation have to be initialized within Computational Stream. Constructor of TPopulation is called from User Interaction Stream, so no GPU-related objects can be initialized in this constructor.

[0063] TPopulation::fillElements() is a virtual method designed to overcome this difficulty. It is called from within the Computational Stream after TSimulator::networkCreate() is called in the User Interaction Stream. A user has to override TPopulation::fillElements() to create TEquation and other computation related objects both element independent and element-specific. Element independent objects include subcomponents of TEquation and objects that describe how to handle interdependencies between variables implemented through derivatives of TGate class.

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[0064] Element-specific data is held in TElement objects. These objects hold references to TEquation and a set of TGate objects. There is one TElement per population, but the size of data arrays within this object corresponds to population size. All TElement objects have to be added to the TSimulator list of elements by calling TSimulator::addUnit() method from TPopulation::fillElements().

[0065] Finally, TPopulation::fillElements() should contain a set of TElement::add*Dependency() calls for each element. Each of these calls sets a corresponding dependency for every TGate object. Here TGate object holds element independent part of dependency and TElement::add*Dependency() sets element-specific details.

[0066] System provided TPopulation handles the output of computational elements, both when they need to exchange the data and when they need to output it to disk. User implementation of TPopulation derivative can add screen output.

[0067] Listing 1 is an example code of the user program that uses a recurrent competitive field (RCF) equation:

```
[0068] uint16_t w = 3, h = 3;

[0069] static float m_compet = 0.5;

[0070] static float m_persist = 1.0;

[0071] class TCablePopRCF : public TPopulation

[0072] {

[0073] TEq_RCF* m_equation;

[0074] TGate* m_gate1;

[0075] TGate* m_gate2;

[0076] void createGatingStructure()
```


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```
[0077]  {
[0078]  m_gate1 = new TGate(0);
[0079]  m_gate2 = new TGate(1);
[0080]  };
[0081]  void createUnitStructure(TBasicUnit* u)
[0082]  {
[0083]    u->addO2OInputDependency(m_gate1, 0., 0., 0.004, 0., 0, 0);
[0084]  u->addFullDependency(m_gate2, population());
[0085]  }
[0086]  public: TCablePopRCF() : TPopulation("compCPU_RCF", w, h, true) {};
[0087]  ~TCablePopRCF() {if(m_equation) delete m_equation;
[0088]      if(m_gate1) delete m_gate1;
[0089]      if(m_gate2) delete m_gate2;};
[0090]  bool fillElements(TSimulator* sim);
[0091]  };
[0092]  bool TCablePopRCF::fillElements(TSimulatior* sim)
[0093]  {
[0094]  m_equation = new TEq_RCF(this, m_compet, m_persist);
[0095]  createGatingStructure();
```


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```
[0096]  for(size_t i = 0; i < xSize(); ++i)
[0097]   for(size_t j = 0; j < ySize(); ++j)
[0098]   {
[0099]  TElement* u = new TCPUElement(this, m_equation, i, j);
[00100] sim->addUnit(u);
[00101] createUnitStructure(u);
[00102] }
[00103] return true;
[00104] }
[00105] int
[00106] main()
[00107] {
[00108] // Input pattern generation (309 in FIG. 3)
[00109] uint32_t* pat = new uint32_t[w*h];
[00110] TRandom<float> randGen (0);
[00111] for(uint32_t i = 0; i < w*h; ++i)
[00112] pat[i] = randGen.random();
[00113] TPattern* p = new TPattern(pat, w, h);
[00114] // Setting up the simulation
```


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```
[00115] TSimulator* cableSim = new TSimulator("data"); //(308 and 320 in FIG. 3)
[00116] cableSim->timestep(0.05); //(320 in FIG. 3)
[00117] cableSim->resetInputs(p); //(325 in FIG. 3)
[00118] cableSim->outfileInterval(0.1); //(308 in FIG. 3)
[00119] cableSim->outmode(SANNDRA::timefunc); //(308 in FIG. 3)
[00120] cableSim->simLength(60.0); //(320 in FIG. 3)
[00121] // Preparing the population
[00122] TPopulation* cablePop = new TCablePopRCF(); //(310 in FIG. 3)
[00123] cableSim->networkCreate(); //(326 in FIG. 3)
[00124] uint16_t user = 1;
[00125] while(user)
[00126] {
[00127] if(!cableSim->simulationStart(true, 1)) //(311 in FIG. 3)
[00128] exit(1);
[00129] std::cout<<"Repeat?\n"; //(305 in FIG. 3)
[00130] std::cin>>user; //(305 in FIG. 3)
[00131] if(user == 1)
[00132] cableSim->networkReset(); //(305 in FIG. 3)
[00133] }
```


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[00134] if(cableSim)

[00135] delete cableSim; //Also deletes cablePop and its internals

[00136] exit(0);

[00137] };

[00138] Listing 1.

[00139] FIG. 4 is a detailed flow diagram illustrating a part of an exemplary implementation of the bottom level system and method performed during the computation on the GPU accelerator of the expansion card 180 and is a more detailed view of the computational box 330 in FIG. 3. FIG. 4 is a representation of one of several ways in which a system and method for processing numerical techniques can be implemented.

[00140] With systems of equations that have complex interdependencies it is likely that the variable in some equation from a previous time step has to be used by some other equation after the new values of this variable are already computed for new time step. To avoid data confusion, the new values of variables should be rendered in a separate texture. After the time step is completed for all equations, these new values should be copied over old values so that they are used as input during the next time step. Copying textures is an expensive operation, computationally, but since the textures are referred to by texture IDs (pointers), swapping these pointers for input and output textures after each time step achieves the same result at a much lesser cost.

[00141] In the hardware solution suggested herein, ID swapping is equivalent to swapping the base memory address for two partitions of the texture memory bank 250. They are swapped 485 during synchronization (485, 430, and 455) so that data transfer 445 and the computation 435-487 proceeds immediately and in parallel with data transfer as shown in FIG. 4. A hardware solution allows this parallelism through access of the controller 220 to the onboard texture memory bank 250.

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[00142] The main computation and data exchange are executed by the controller 220. It runs three parallel streams of execution: Computational Stream 303, Data Output Stream 301, and Data Input Stream 302. These streams are synchronized with each other during the swap of pointers 485 to the input and output texture memory partitions of the texture memory bank 250 and the check for the last iteration 487. Algorithmically, these two operations are a single atomic operation, but the block diagram shows them as two separate blocks for clarity.

[00143] The Computational Stream 303 performs a computational cycle including a sequential execution of all shaders that were stored in the shader memory bank 210 using the appropriate input and output textures. To begin the simulation the controller 220 initializes three execution streams 301, 302, 303. On every simulation step, the Computational Stream 303 determines which textures the GPU 240 will need to perform the computations and initiates the upload 435 of them onto the GPU 240. The GPU 240 can communicate directly with the texture memory bank 250 to upload the appropriate texture to perform the computations. The controller 220 also pulls the first shader (known by the stored order) from the shader memory bank 210 and uploads 450 it onto the GPU 240.

[00144] The GPU 240 executes the following operations in this order: performs the computation (execution of the shader) 470; tells the controller 220 that it is done with the computations for the current shader; and after all shaders for this particular equation are executed sends 480 the output textures to the output portion of the texture memory bank 250. This cycle continues through all of the equations based on the branching step 482.

[00145] An example shader that performs fourth order Runge-Kutta numerical integration is shown in Listing 2 using GLSL notation;

[00146] uniform sampler2DRect Variable;

[00147] uniform float integration_step;

[00148] float halfstep = integration_step*0.5;

[00149] float f1_6step = integration_step/6.0;

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```
[00150] vec4 output = texture2DRect(Variable, gl_TexCoord[0].st);
[00151] // define equation() here
[00152] vec4 rungekutta4(vec4 x)
[00153] {
[00154]  const vec4 k1 = equation(x);
[00155]  const vec4 k2 = equation(x + halfstep*k1);
[00156]  const vec4 k3 = equation(x + halfstep*k2);
[00157]  const vec4 k4 = equation(x + integration_step*k3);
[00158]  return f1_6step*(k1 + 2.0*(k2 + k3) + k4);
[00159] }
[00160] void main(void)
[00161] {
[00162]  output += rungekutta4(output);
[00163]  gl_FragColor = output;
[00164] }
```

[00165] Listing 2.

[00166] The shader in Listing 2 can be executed on conventional video card. Using the controller 220 this code can be further optimized, however. Since the integration step does not change during the simulation, the step itself as well as the halfstep and 1/6 of the step can be

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computed once per simulation, and updated in all shaders by a shader update procedures 310, 326 discussed above.

[00167] After all of the equations in the computational cycle are computed the main execution stream on the controller 220 can switch 485 the reference pointers of the input and output portions of the texture memory bank 250.

[00168] The two other streams of execution on the controller 220 are waiting (blocks 430 and 455, respectively) for this switch to begin their execution. The Data Input Stream 302 is controlling 440 the input of additional data from the CPU 120. This is necessary in cases where the simulation is monitoring the changing input, for example input from a video camera or other recording device in the real time. This stream uploads new external input from the CPU 120 to the texture memory bank 250 so it can be used by the main computational stream on the next computational step and waits for the next iteration 475. The Data Output Stream 445 controls the output of simulation results to the CPU 120 if requested by the user. This stream uploads the results of the previous step to the main RAM 130 so that the CPU 120 can save them on disk 140 or show them on the results display 313 and waits for the next iteration 460.

[00169] Since the Computational Stream determines the timing of input 440 and output 445 data transfers, these data transfers are driven by the controller 220. To further reduce the data transfer overhead (and disk 140 overhead also) the controller 220 initiates transfer only after selected computational steps. For example, if the experimental data that is simulated was recorded every 10 milliseconds (msec) and the simulation for better precision was computed every 1 msec, then only every tenth result has to be transferred to match the experimental frequency.

[00170] This solution stores two copies of output data, one in the expansion card texture memory bank 250 and another in the system RAM 130. The copy in the system RAM 130 is accessed twice: for disk I/O and screen visualization 313. An alternative solution would be to provide CPU 120 with a direct read access to the onboard texture memory bank 250 by mapping the memory of the hardware onto a global memory space. The alternative solution

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will double the communication through the local bus 190. Since the goal discussed herein is reducing the information transfer through the local bus 190, the former solution is favored.

[00171] The main stream determines if this is the last iteration 487. If it is the last iteration, the controller 220 waits for the all of the execution streams to finish 490 and then returns the control to the CPU 120, otherwise it begins the next computational cycle.

[00172] This repeats through all of the computational cycles of the simulation.

[00173] Conclusion

[00174] This GPU accelerator system offers the following potential advantages:

[00175] 1. Limited computations on the CPU 120. The CPU 120 is only used for user input, sending information to the controller 220, receiving output after each computational cycle (or less frequently as defined by the user), writing this output to disk 140, and displaying this output on the monitor 170. This frees the CPU 120 to execute other applications and allows the expansion card to run at its full capacity without being slowed down by extensive interactions with the CPU 120.

[00176] 2. Minimizing data transfer between the expansion card 180 and the system bus 200. All of the information needed to perform the simulations will be stored on the expansion card 180 and all simulations will take place on it. Furthermore, whatever data transfer remains necessary will take place in parallel with the computation, thus reducing the impact of this transfer on the performance.

[00177] 3. New way to execute GPU programs (shaders). Previously, the CPU 120 had full control over the order of shader's execution and was required to produce specific commands on every cycle to tell the GPU 240 which shader to use. With the invention disclosed herein, shaders will initially be stored on the shader memory bank 210 on the expansion card 180 and will be sent to the GPU 240 for execution by the general purpose controller 220 located on the expansion card.

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[00178] 4. Multiple parallelisms. The GPU 240 is inherently parallel and is well suited to perform parallel computations. In parallel with the GPU 240 performing the next calculation, the controller 220 is uploading the data from the previous calculation into main memory 130. Furthermore, the CPU 120 at the same time uses uploaded previous results to save them onto disk 140 and to display them on the screen through the system bus 200.

[00179] 5. Reuse of existing and affordable technology. All hardware used in the invention and mentioned here-in are based on currently available and reliable components. Further advance of these components will provide straightforward improvements of the invention.

[00180] While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

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CLAIMS

What is claimed is:

1. A computer system, comprising:

a central processing unit;

main memory accessed by the central processing unit;

a video system for driving a video monitor in response to the central processing unit; and

an accelerator receiving input data from and providing output data to the central processing unit, the accelerator comprising:

at least one graphics processing unit;

accelerator memory for the graphic processing unit; and

an accelerator controller for moving the input data into the accelerator memory, moving output data from the accelerator memory, and supervising data exchange between the accelerator memory and at least one graphic processing unit.

2. A computer system as claimed in claim 1, wherein the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit.

3. A computer system as claimed in claim 1, wherein the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit.

4. A computer system as claimed in claim 1, wherein the accelerator controller sends instructions to the at least one graphics processing unit, which executes the instructions on data, and wherein during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transfers output data from the accelerator memory to main memory of the central processing unit.

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5. A computer system as claimed in claim 1, wherein the accelerator controller comprises an interface controller that enables the accelerator to communicate over a bus of the computer system with the central processing unit.

6. A computer system as claimed in claim 1, wherein the accelerator memory comprises a texture memory bank for storing simulation data and a shader memory bank for storing operations to be performed on the simulation data by the at least one graphic processing unit.

7. A computer system as claimed in claim 6, wherein the texture memory is partitioned into sections in which a first section holds input data patterns, a second section holds data textures representing internal variables, a third section holds data textures used as input at a particular computation step, and a fourth section holds data textures used to store an output of a computational step on the at least one graphic processing unit.

8. A computer system as claimed in claim 1, wherein the accelerator controller inputs data into at least one graphic processing unit and a series of instructions to the at least one graphic processing unit, which then successively executes the instructions on the data.

9. A computer system as claimed in claim 8, wherein the accelerator controller performs successive iterations by feeding output data generated by the at least one graphic processing unit and input data for a next iteration into the at least one graphic processing unit.

10. An accelerator system for a computer system, the accelerator system comprising:
at least one graphics processing unit;
accelerator memory for the graphic processing unit; and
an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory.

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11. A computer system as claimed in claim 10, wherein the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit.

12. A computer system as claimed in claim 10, wherein the accelerator controller sends instructions to the at least one graphics processing unit, which executes the instructions on data, and wherein during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transfers output data from the accelerator system.

13. A computer system as claimed in claim 10, wherein the accelerator memory comprises a texture memory bank for storing simulation data and a shader memory bank for storing operations to be performed on the simulation data by the at least one graphic processing unit.

14. A computer system as claimed in claim 13, wherein the texture memory is partitioned into sections in which a first section holds input data patterns, a second section holds data textures representing internal variables, a third section holds data textures used as input at a particular computation step, and a fourth section holds data textures used to store an output of a computational step on the at least one graphic processing unit.

15. A computer system as claimed in claim 10, wherein the accelerator controller inputs data into at least one graphic processing unit and a series of instructions to the at least one graphic processing unit, which then successively executes the instructions on the data.

16. A computer system as claimed in claim 15, wherein the accelerator controller performs successive iterations by feeding output data generated by the at least one graphic processing unit and input data for a next iteration into the at least one graphic processing unit.

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

17. A method for performing numerical simulations in a computer system, the method comprising:

a central processing unit loading input data into an accelerator system from main memory of the central processing unit;

an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data;

the accelerator controller transferring output data generated by the graphic processing unit to the central processing unit as output data.

18. A method as claimed in claim 17, further comprising:

the accelerator controller sending instructions to the at least one graphics processing unit, which executes the instructions on data; and

during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transferring output data from the accelerator memory to main memory of the central processing unit.

19. A method as claimed in claim 17, further comprising: partitioning accelerator memory of accelerator system a first section holding input data patterns, a second section holding data textures representing internal variables, a third section holding data textures used as input at a particular computation step, and a fourth section holding data textures used to store an output of a computational step on the at least one graphic processing unit.

20. A method as claimed in claim 17, further comprising the accelerator controller performing successive iterations by feeding output data generated by the at least one graphic processing unit and input data for a next iteration into the at least one graphic processing unit.

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
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ABSTRACT OF THE DISCLOSURE

[00181] An accelerator system is implemented on an expansion card comprising a printed circuit board having (a) one or more graphics processing units (GPU), (b) two or more associated memory banks (logically or physically partitioned), (c) a specialized controller, and (d) a local bus providing signal coupling compatible with the PCI industry standards (this includes but is not limited to PCI-Express, PCI-X, USB 2.0, or functionally similar technologies). The controller handles most of the primitive operations needed to set up and control GPU computation. As a result, the computer's central processing unit (CPU) is freed from this function and is dedicated to other tasks. In this case a few controls (simulation start and stop signals from the CPU and the simulation completion signal back to CPU), GPU programs and input/output data are the information exchanged between CPU and the expansion card. Moreover, since on every time step of the simulation the results from the previous time step are used but not changed, the results are preferably transferred back to CPU in parallel with the computation.

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IPR2025-00606

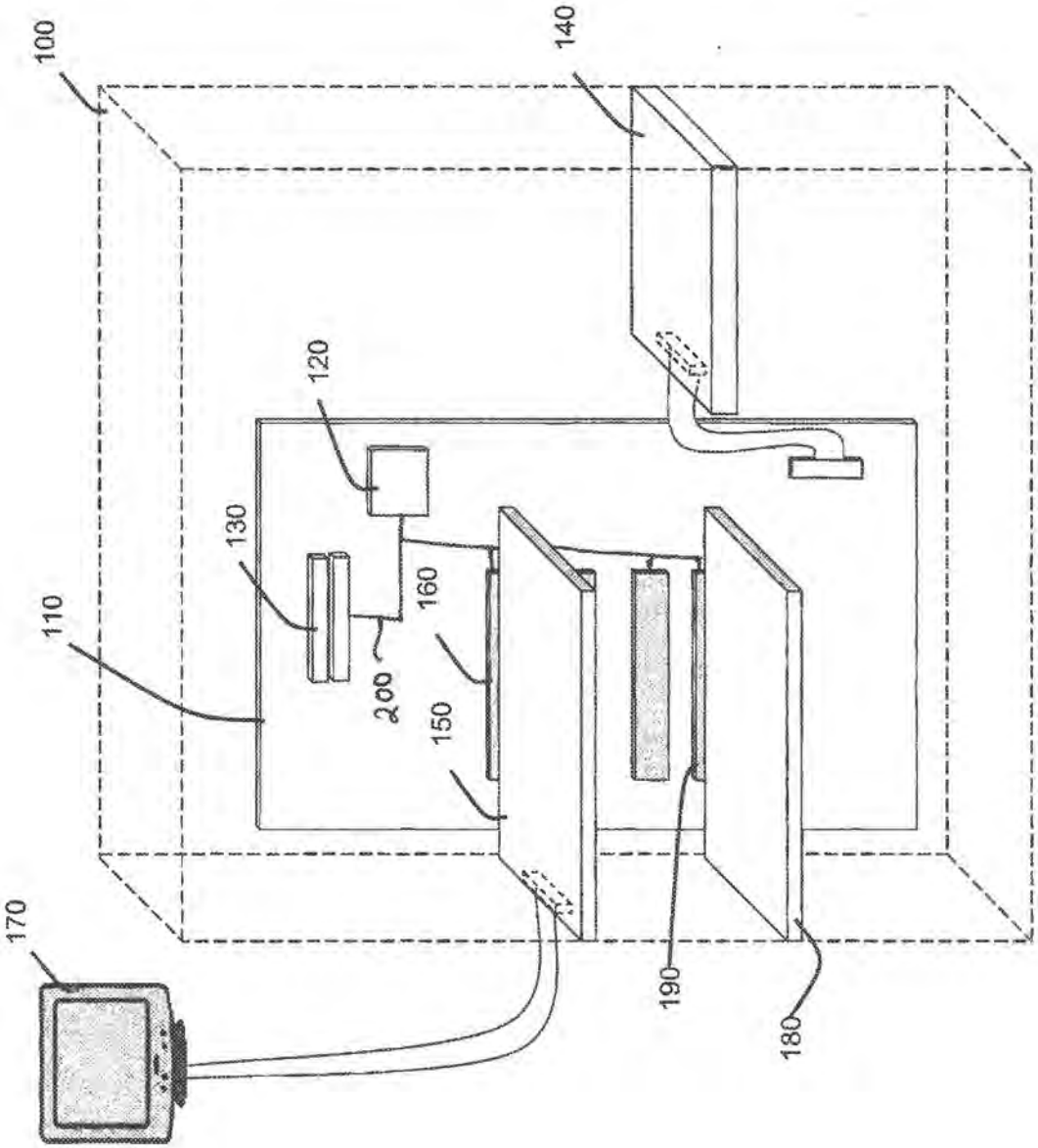


FIG. 1

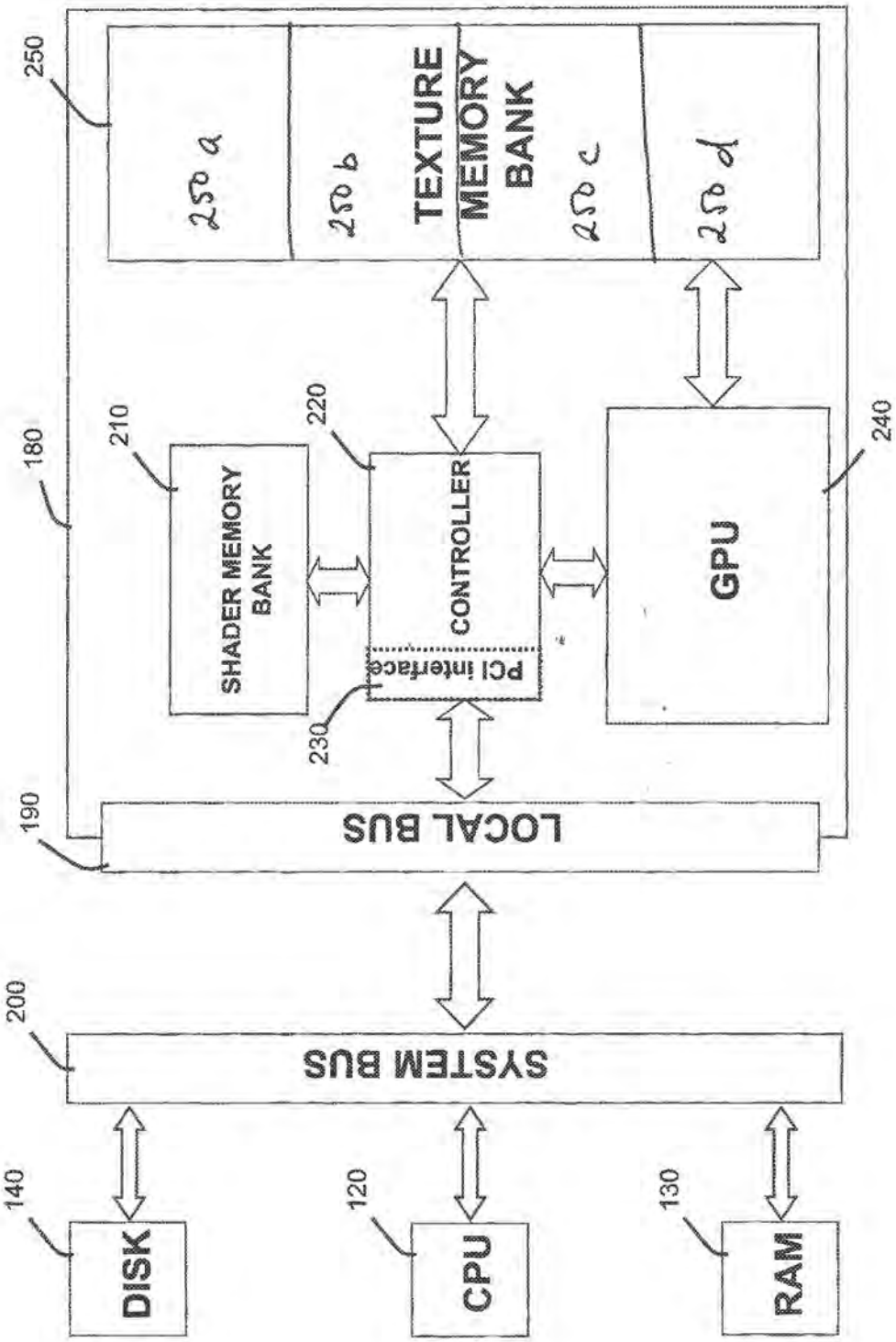

250
250 a
250 b
TEXTURE MEMORY BANK
250 c
250 d
180
210
SHADER MEMORY BANK
220
CONTROLLER
PCI interface
230
GPU
240
190
LOCAL BUS
200
SYSTEM BUS
140
DISK
120
CPU
130
RAM

FIG. 2

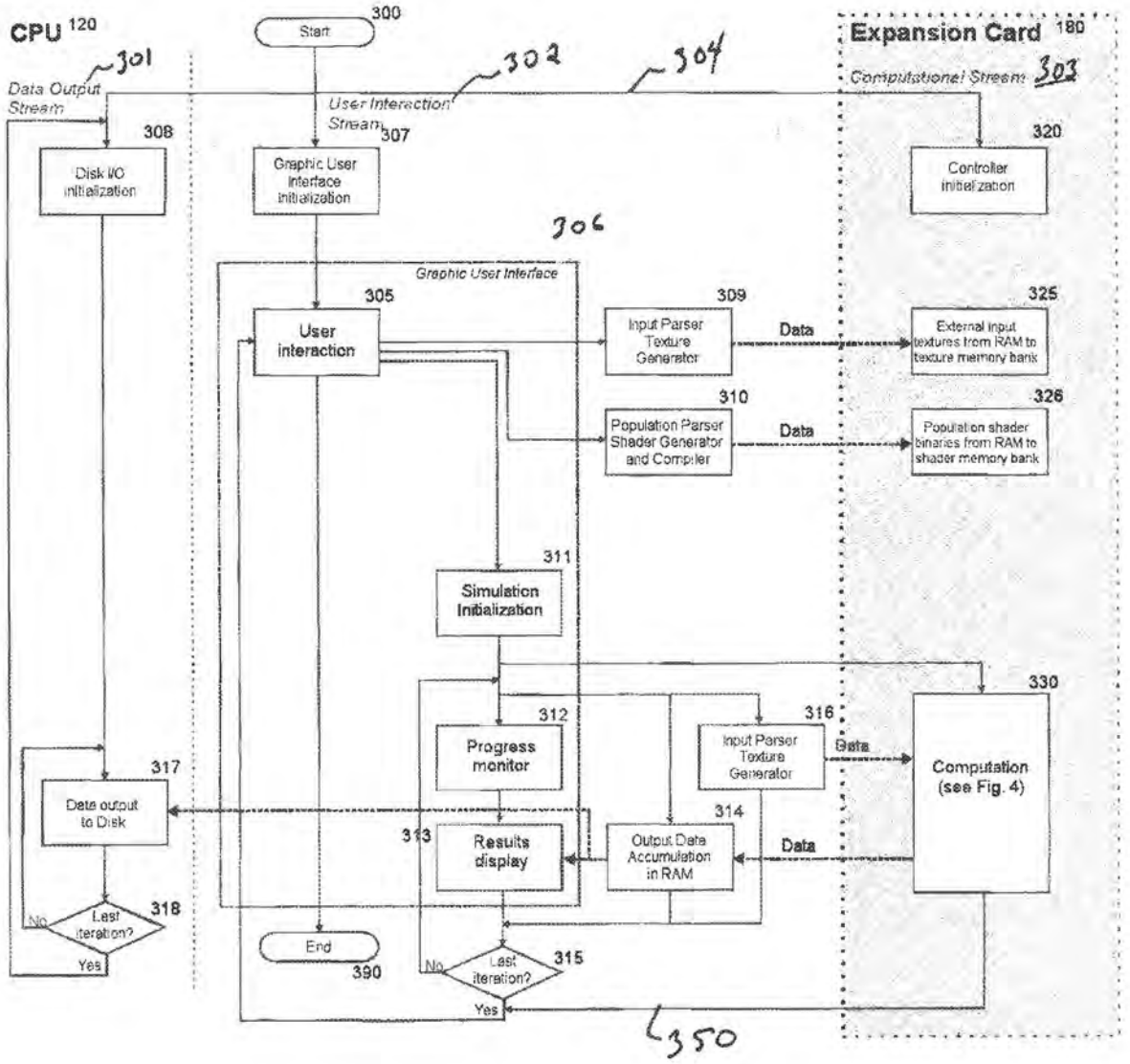

CPU 120
Start
300
Expansion Card 180
301
302
304
Data Output Stream
User Interaction Stream
Computational Stream 303
308
Disk I/O initialization
307
Graphic User Interface initialization
320
Controller initialization
306
Graphic User Interface
305
User interaction
309
Input Parser Texture Generator
Data
325
External input textures from RAM to texture memory bank
310
Population Parser Shader Generator and Compiler
Data
326
Population shader binaries from RAM to shader memory bank
311
Simulation Initialization
330
312
Progress monitor
316
Input Parser Texture Generator
Data
Computation (see Fig. 4)
317
Data output to Disk
313
Results display
314
Output Data Accumulation in RAM
Data
318
No
Last iteration?
Yes
End
390
No
Last iteration?
315
Yes
350

FIG. 3

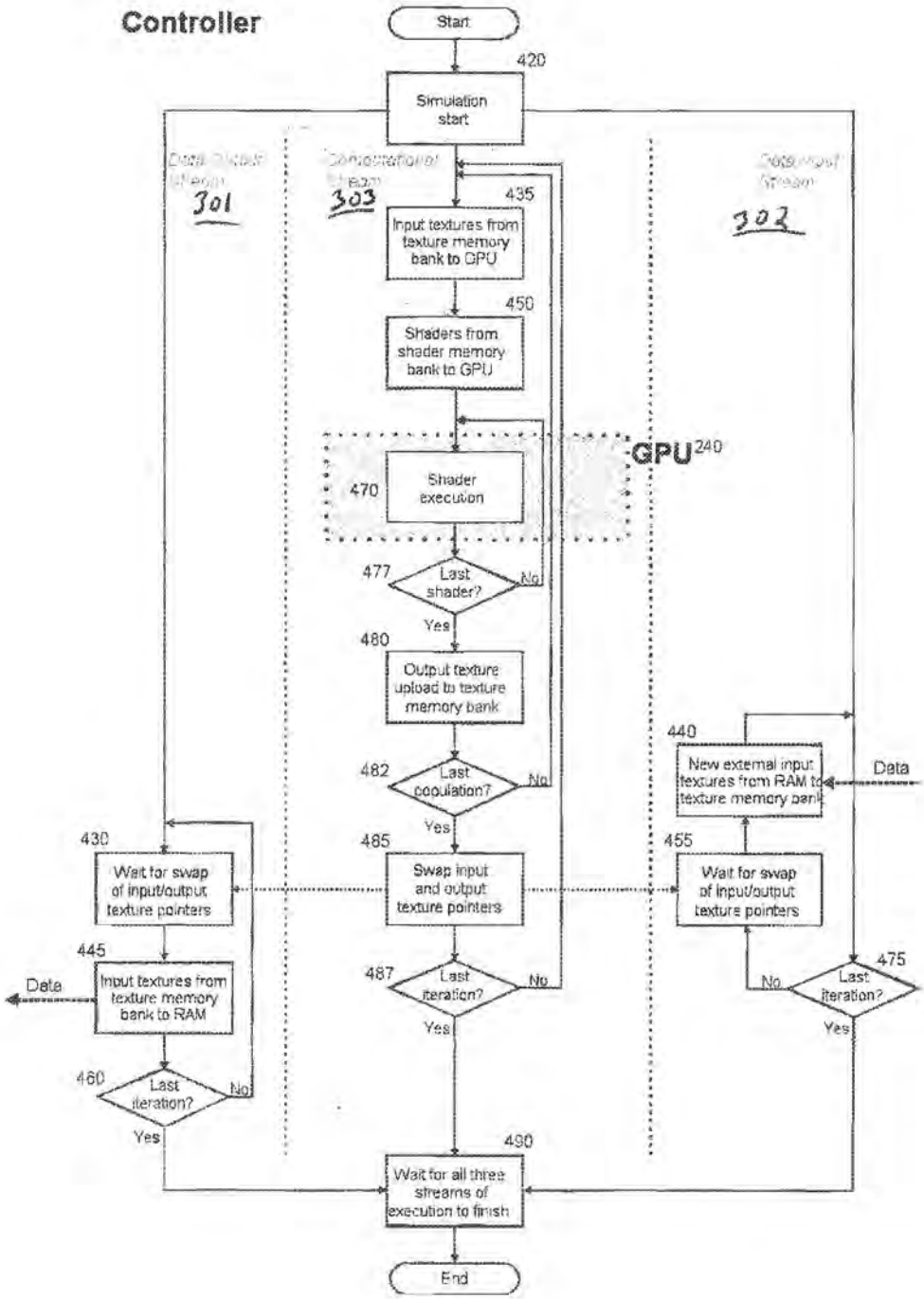
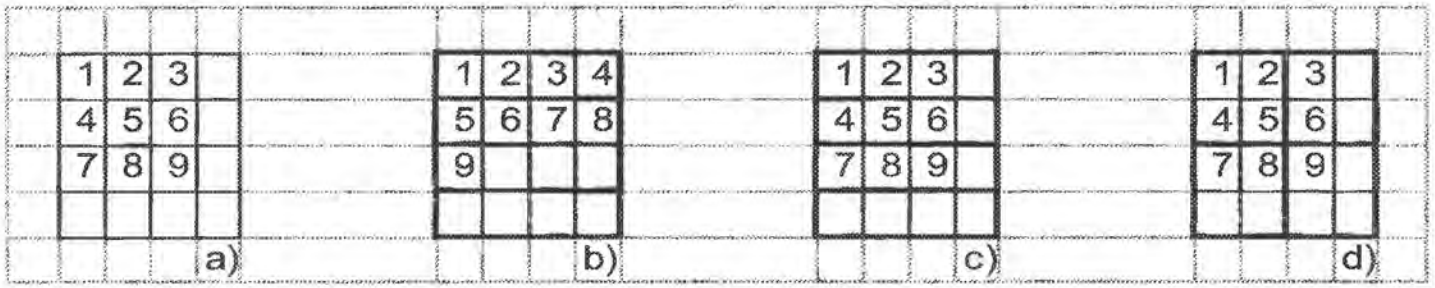

Controller
Start
420
Simulation start
301
303
302
435
Input textures from texture memory bank to GPU
450
Shaders from shader memory bank to GPU
GPU 240
470
Shader execution
477
Last shader?
No
Yes
480
Output texture upload to texture memory bank
482
Last coculation?
No
Yes
440
New external input textures from RAM to texture memory bank
Data
430
Wait for swap of input/output texture pointers
485
Swap input and output texture pointers
455
Wait for swap of input/output texture pointers
445
Input textures from texture memory bank to RAM
Data
487
Last iteration?
No
Yes
475
Last iteration?
No
Yes
460
Last iteration?
No
Yes
490
Wait for all three streams of execution to finish
End

FIG. 4



Bold lines show the packing of data into pixels with four color components.

FIG. 5

Electronic Acknowledgement Receipt

EFS ID:	2232722
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	29127
Filer:	Joseph G. Houston
Filer Authorized By:	
Attorney Docket Number:	0167.0001US1
Receipt Date:	24-SEP-2007
Filing Date:	
Time Stamp:	17:21:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	0167-0001US1_ADS.pdf	1187507 65962aeb044a2ab9dfd2672f5240fac65316e2fe	no	5

Warnings:

Information:					
2		0167-0001US1-SPEC.pdf	186264 56fa9153005d6230865b6d0ccb7932d6 68da554	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	25	
	Claims		26	29	
	Abstract		30	30	
Warnings:					
Information:					
3	Drawings	0167-0001US1_FIGS.pdf	322733 eab196db35e441a03dc4bef9e54bb489 95b8f346	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	1696504		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

9/24/07

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

11/860,254

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)		OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))				75			
SEARCH FEE (37 CFR 1.16(k), (i), or (m))				250			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))				100			
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =		X 25=		OR	X 50=	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =		X 100=			X 200=	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	425		TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	TOT CLAIMS	IND CLAIMS
11/860,254	09/24/2007	3747	0.00	0167.0001US1	20	3

CONFIRMATION NO. 6266

FILING RECEIPT

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA02421

Date Mailed: 10/04/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Anatoli Gorchetchnikov, Boton, MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

Assignment For Published Patent Application

Neurala LLC, Boston, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/826,892 09/25/2006

Foreign Applications

If Required, Foreign Filing License Granted: 10/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/860,254**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

** SMALL ENTITY **

Title

Graphic Processor Based Accelerator System and Method

Preliminary Class

123

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under

37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

FORMALITIES LETTER

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

Date Mailed: 10/04/2007

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  *Applicant must submit $ **75** to complete the basic filing fee for a small entity.*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 2.
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 3-4 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee, or oath or declaration) as set forth in 37 CFR 1.16(f) of $65 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$500** for a small entity

- **$75** Statutory basic filing fee.
- **$65** Surcharge.

- The application search fee has not been paid. Applicant must submit **$255** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$105** to complete the examination fee for a small entity in compliance with 37 CFR 1.27.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199
PART 3 - OFFICE COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re:	Anatoli Gorchetchnikov	Confirmation No:	6266
Application No:	11/860,254	Group:	3747
Filed:	September 24, 2007	Examiner:	Not yet assigned
For:	Graphic Processor Based Accelerator System and Method		
Customer No.:	29127		
Attorney Docket No.	0167.0001US1		

PRELIMINARY AMENDMENT UNDER RULE 115

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the pending Notice to File Missing Parts, please amend the above-captioned patent application as follows:

-amendments to the specification are set forth in the section Amendments to Specification section; and

-amendments to the drawings are set forth in Amendments to Drawings section.

Amendments to Specification

Replace paragraph [0018] beginning at page 4 in the specification as originally filed, with the following rewritten paragraph:

-- FIG. 4 is a flow diagram illustrating an exemplary implementation of the bottom level control of the ~~CPU~~ GPU accelerator system that is used to execute the target computation; and --

Replace paragraph [0142] beginning at page 21 in the specification as originally filed, with the following rewritten paragraph:

-- The main computation and data exchange are executed by the controller 220. It runs three parallel ~~streams~~ substreams of execution: Computational ~~Stream 303~~ Substream 403, Data Output ~~Stream 301~~ Substream 402, and Data Input ~~Stream 302~~ Substream 404. These streams are synchronized with each other during the swap of pointers 485 to the input and output texture memory partitions of the texture memory bank 250 and the check for the last iteration 487. Algorithmically, these two operations are a single atomic operation, but the block diagram shows them as two separate blocks for clarity. --

Replace paragraph [0143] beginning at page 21 in the specification as originally filed, with the following rewritten paragraph:

-- The Computational ~~Stream 303~~ Substream 403 performs a computational cycle including a sequential execution of all shaders that were stored in the shader memory bank 210 using the appropriate input and output textures. To begin the simulation the controller 220 initializes three execution ~~streams 301, 302, 303~~ substreams 403, 402, and 404. On every simulation step, the Computational ~~Stream 303~~ Substream 403 determines which textures the GPU 240 will need to perform the computations and initiates the upload 435 of them onto the GPU 240. The GPU 240 can communicate directly with the texture memory bank 250 to upload the appropriate texture to perform the computations. The controller 220 also pulls the first shader (known by the stored order) from the shader memory bank 210 and uploads 450 it onto the GPU 240. --

Replace paragraph [0167] beginning at page 23 in the specification as originally filed, with the following rewritten paragraph:

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-- After all of the equations in the computational cycle are computed the main execution ~~stream~~ substream 403 on the controller 220 can switch 485 the reference pointers of the input and output portions of the texture memory bank 250. --

Replace paragraph [0168] beginning at page 23 in the specification as originally filed, with the following rewritten paragraph:

-- The two other ~~streams~~ substreams of execution on the controller 220 are waiting (blocks 430 and 455, respectively) for this switch to begin their execution. The Data Input ~~Stream 302~~ Substream 404 is controlling 440 the input of additional data from the CPU 120. This is necessary in cases where the simulation is monitoring the changing input, for example input from a video camera or other recording device in the real time. This ~~stream~~ substream uploads new external input from the CPU 120 to the texture memory bank 250 so it can be used by the main computational ~~stream~~ substream 403 on the next computational step and waits for the next iteration 475. The Data Output ~~Stream~~ Substream 445 controls the output of simulation results to the CPU 120 if requested by the user. This ~~stream~~ substream uploads the results of the previous step to the main RAM 130 so that the CPU 120 can save them on disk 140 or show them on the results display 313 and waits for the next iteration 460. --

Replace paragraph [0169] beginning at page 23 in the specification as originally filed, with the following rewritten paragraph:

-- Since the Computational ~~Stream~~ Substream 403 determines the timing of input 440 and output 445 data transfers, these data transfers are driven by the controller 220. To further reduce the data transfer overhead (and disk 140 overhead also) the controller 220 initiates transfer only after selected computational steps. For example, if the experimental data that is simulated was recorded every 10 milliseconds (msec) and the simulation for better precision was computed every 1 msec, then only every tenth result has to be transferred to match the experimental frequency. --

Replace paragraph [0171] beginning at page 24 in the specification as originally filed, with the following rewritten paragraph:

-- The main ~~stream~~ substream 403 determines if this is the last iteration 487. If it is the last iteration, the controller 220 waits for the all of the execution ~~streams~~

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substreams to finish 490 and then returns the control to the CPU 120, otherwise it begins the next computational cycle. --

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Amendments to Drawings:

The following sheets of drawings include changes to Figs. 1-4. These sheets, which include Figs. 1-4, replace the original sheeting including Figs. 1-4.

Respectfully submitted,

By /grant houston/

J. Grant Houston
Registration No.: 35,900
Tel.: 781 863 9991
Fax: 781 863 9931

Lexington, Massachusetts 02421
Date: November 13, 2007

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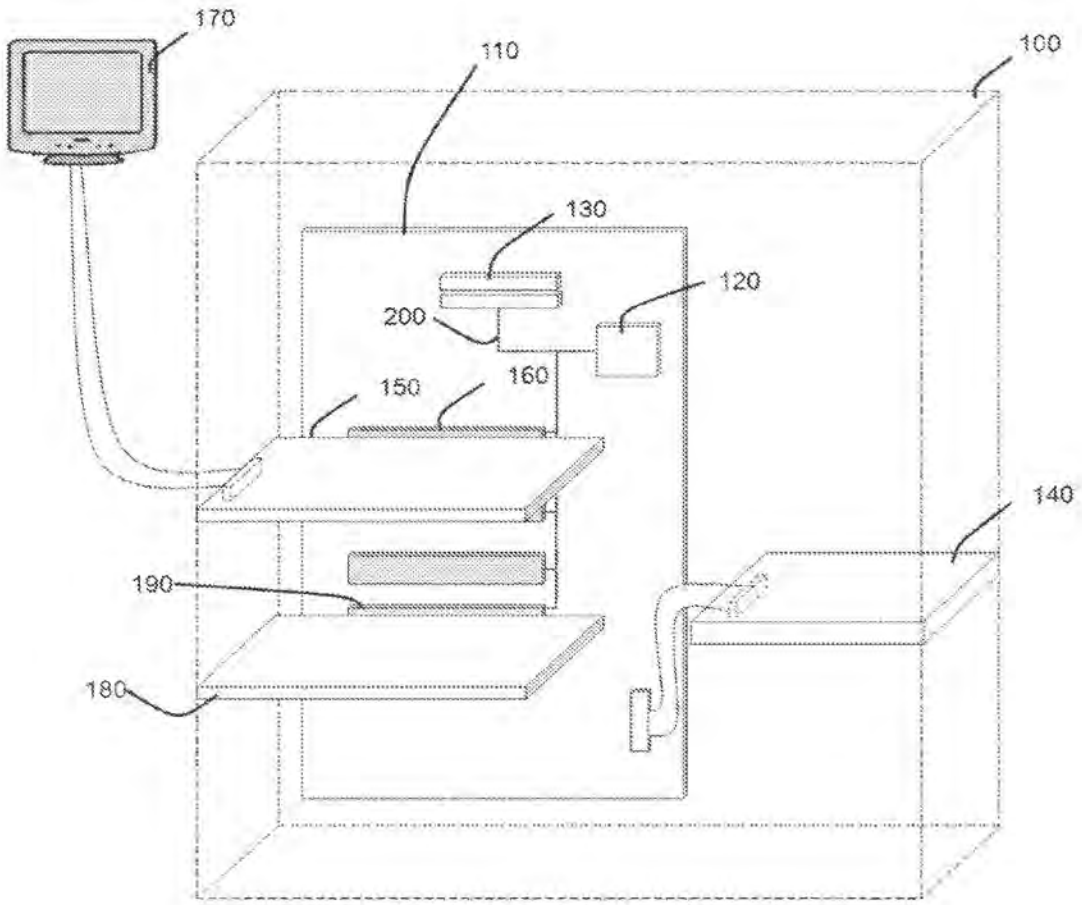

FIG. 1

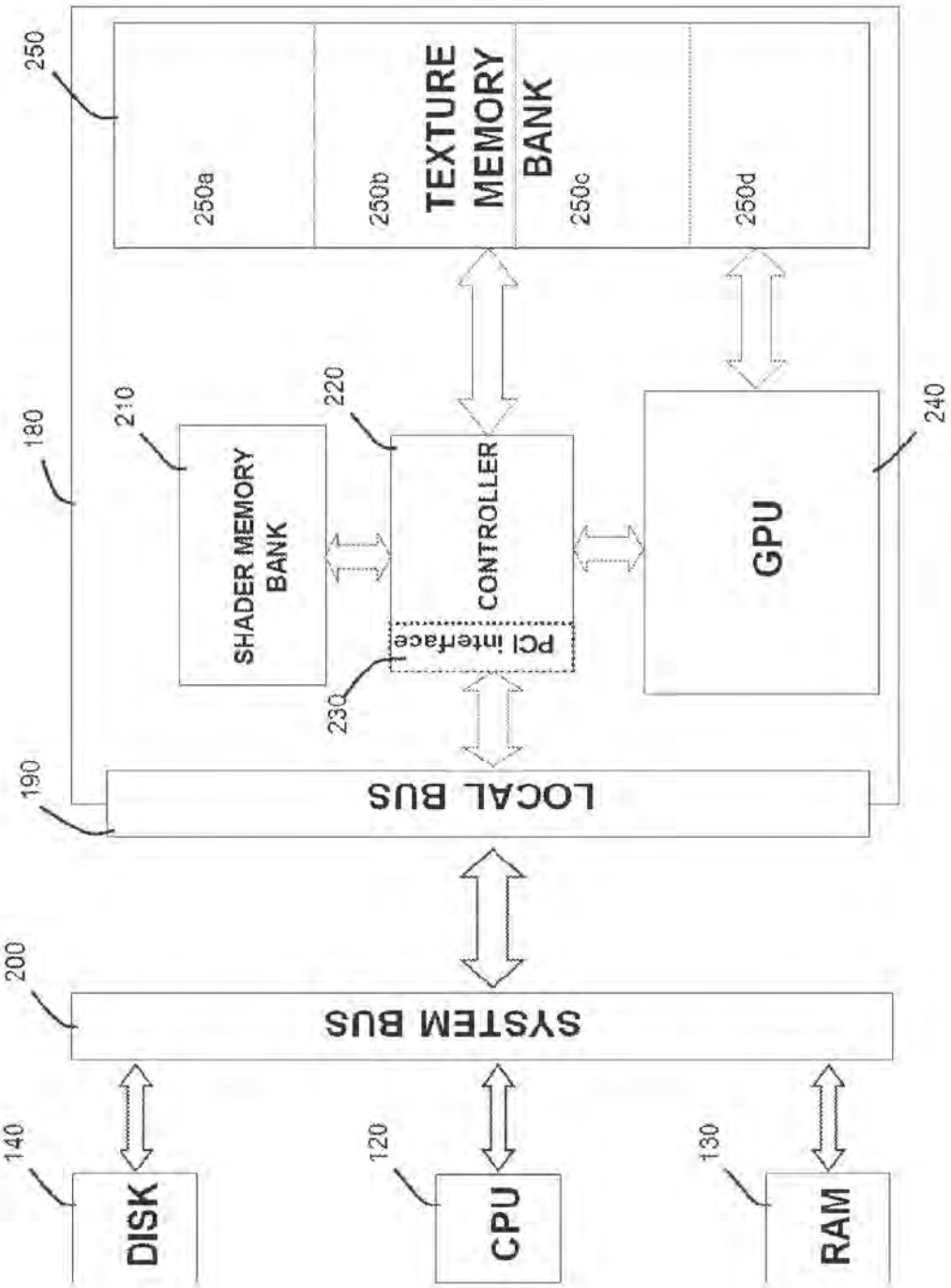
250
250a
250b
TEXTURE MEMORY BANK
250c
250d
180
210
SHADER MEMORY BANK
220
CONTROLLER
PCI interface
230
GPU
240
190
LOCAL BUS
200
SYSTEM BUS
140
DISK
120
CPU
130
RAM

FIG. 2

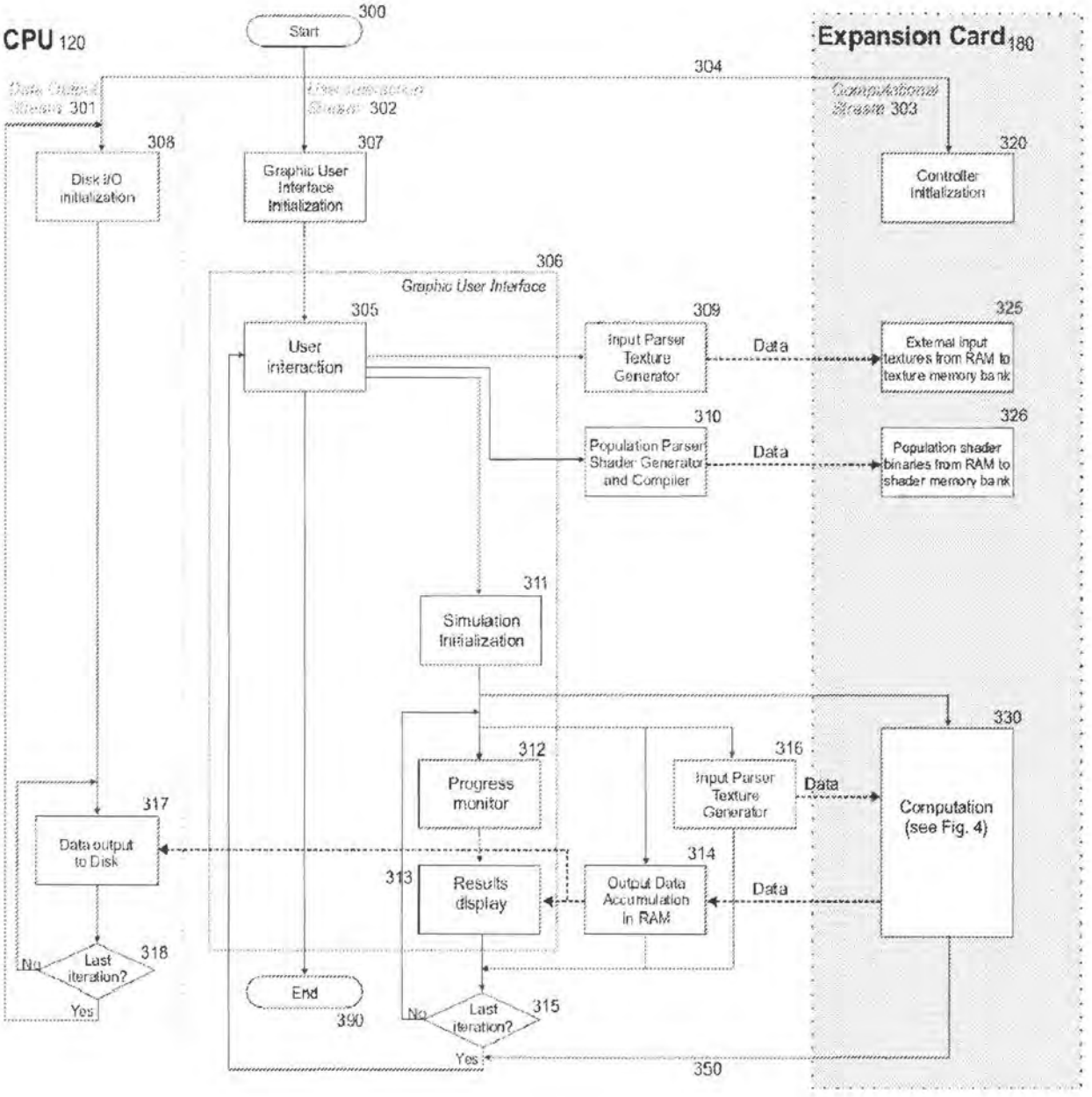
CPU 120
Start
300
Expansion Card 180
304
Data Output Stream 301
User Interface Stream 302
Computational Stream 303
308
Disk I/O Initialization
307
Graphic User Interface Initialization
320
Controller Initialization
306
Graphic User Interface
305
User Interaction
309
Input Parser Texture Generator
Data
325
External input textures from RAM to texture memory bank
310
Population Parser Shader Generator and Compiler
Data
326
Population shader binaries from RAM to shader memory bank
311
Simulation Initialization
330
312
Progress monitor
316
Input Parser Texture Generator
Data
Computation (see Fig. 4)
317
Data output to Disk
313
Results display
314
Output Data Accumulation in RAM
Data
318
Last iteration?
No
Yes
End
390
315
Last iteration?
No
Yes
350

Fig. 3

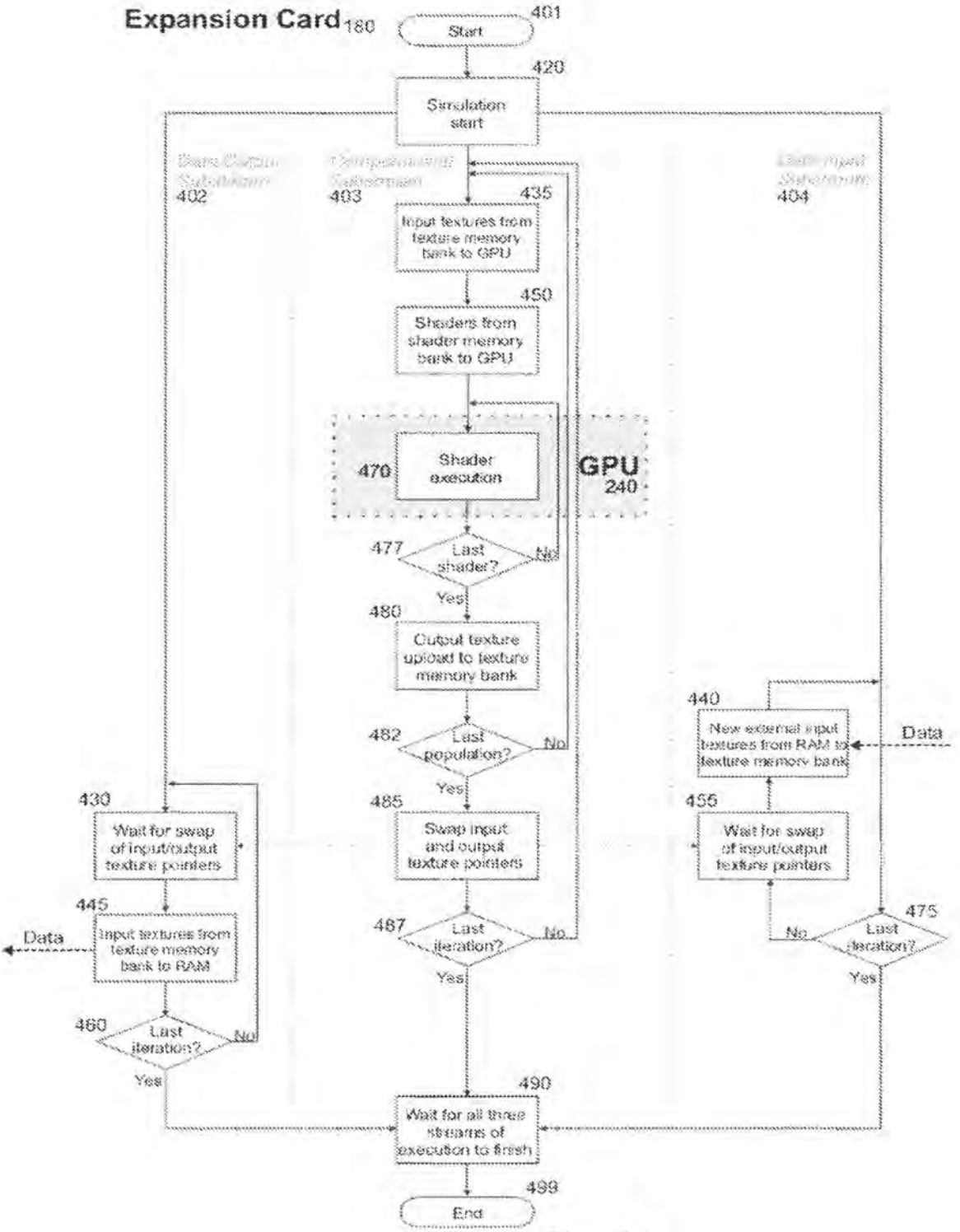
Expansion Card 180
Start
401
Simulation start
420
402
403
404
Input textures from texture memory bank to GPU
435
Shaders from shader memory bank to GPU
450
Shader execution
470
GPU 240
Last shader?
477
No
Yes
Output texture upload to texture memory bank
480
Last population?
482
No
Yes
Swap input and output texture pointers
485
Last iteration?
487
No
Yes
Wait for swap of input/output texture pointers
430
Input textures from texture memory bank to RAM
445
Data
Last iteration?
460
No
Yes
New external input textures from RAM to texture memory bank
440
Data
Wait for swap of input/output texture pointers
456
Last iteration?
475
No
Yes
Wait for all three streams of execution to finish
490
End
499

Fig. 4

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0167.0001US1
	Application Number	

Title of Invention	Graphic Processor Based Accelerator System and Method

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Anatoli		Gorchetchnikov	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service

City	Belmont	State/Province	MA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	RU

Mailing Address of Applicant:

Address 1	43 Alma Avenue		
Address 2			
City	Belmont	State/Province	MA
Postal Code	02478	Country i	US

Applicant 2 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Heather	Marie	Ames	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service

City	South Boston	State/Province	MA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	US

Mailing Address of Applicant:

Address 1	252 East 8th St., Apt #2		
Address 2			
City	South Boston	State/Province	MA
Postal Code	02127	Country i	US

Applicant 3 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Massimiliano		Versace	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service

City	South Boston	State/Province	MA	Country of Residence i	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0167.0001US1
	Application Number	
Title of Invention	Graphic Processor Based Accelerator System and Method	

Citizenship under 37 CFR 1.41(b) i	IT		
Mailing Address of Applicant:			
Address 1	252 East 8th St. Apt. #2		
Address 2			
City	South Boston	**State/Province**	MA
Postal Code	02127	**Country**i	US
Applicant 4			Remove
Applicant Authority	◉ Inventor	◯ Legal Representative under 35 U.S.C. 117	◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Fabrizio		Santini	

Residence Information (Select One)	◉ US Residency	◯ Non US Residency	◯ Active US Military Service		
City	Jamaica Plain	**State/Province**	MA	**Country of Residence** i	US
Citizenship under 37 CFR 1.41(b) i	IT				
Mailing Address of Applicant:					
Address 1	22 Sigourney St. Unit E				
Address 2					
City	Jamaica Plain	**State/Province**	MA		
Postal Code	02130	**Country**i	US		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	29127		
Email Address	grant.houston@ghme.com	Add Email	Remove Email

Application Information:

Title of the Invention	Graphic Processor Based Accelerator System and Method		
Attorney Docket Number	0167.0001US1	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0167.0001US1
	Application Number	
Title of Invention	Graphic Processor Based Accelerator System and Method	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application has not **and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	29127		

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	60826892	2006-09-25

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◉ Yes ○ No

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Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0167.0001US1
	Application Number	
Title of Invention	Graphic Processor Based Accelerator System and Method	

If the Assignee is an Organization check here. ☒			
Organization Name	Neurala LLC		
Mailing Address Information:			
Address 1	252 East 8th Street		
Address 2	Suite 2		
City	Boston	**State/Province**	MA
Country [i]	US	Postal Code	02127
Phone Number	617-416-6817	Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.			Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/grant houston/			Date (YYYY-MM-DD)	2007-10-23
First Name	J. Grant	Last Name	Houston	Registration Number	35900

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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APPL NO.	FILING OR 371(c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO.	TOT CLMS	IND CLMS
11/860,254	09/24/2007	3747	0.00	0167.0001US1	20	3

CONFIRMATION NO. 6266

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

FILING RECEIPT

OC000000026172307

Date Mailed: 10/04/2007

Receipt is acknowledged of this nonprovisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Anatoli Gorchetchnikov, ~~Boton,~~ Belmont MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

Assignment For Published Patent Application

Neurala LLC, Boston, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/826,892 09/25/2006

Foreign Applications

If Required, Foreign Filing License Granted: 10/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is US11/860,254

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

** SMALL ENTITY **

Title

Graphic Processor Based Accelerator System and Method

Preliminary Class

123

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Docket No.: 0167.0001US1

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on September 24, 2007 as United States Application No. or PCT International Application Number 11/860,254

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

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I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/826,892	September 25, 2006
Application Serial No.	Filing Date
Application Serial No.	Filing Date
Application Serial No.	Filing Date

I hereby claim the benefit under 35 U. S. C, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Neural AI, LLC, Exhibit 2045
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IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

HOUSTON ELISEEVA LLP Customer No: 29127

Maria M. Eliseeva, Reg. No. 43,328
J. Grant Houston, Reg. No. 35,900
Anabela Cristina Taylor, Reg. No. 38,999

Send Correspondence to:
J. Grant Houston, Esq.
Houston Eliseeva LLP
4 Militia Drive, Ste. 4
Lexington, MA 02421

Direct Telephone Calls to: *(name and telephone number)*
J. Grant Houston, Esq. 781-863-9991

Full Name of sole or first inventor	Anatoli Gorchetchnikov	
Sole or first inventor's signature		10/12/07 Date
Residence	43 Alma Avenue, Belmont, MA 02478	
Citizenship	Russia	
Post Office Address	Same as above	

Full Name of second inventor, if any	Heather Marie Ames	
Second inventor's signature	Heather Ames	10/12/07 Date
Residence	252 East 8th Street, Apt. #2, South Boston, MA 02127	
Citizenship	US	
Post Office Address	Same as above	

Full Name of third inventor, if any	Massimiliano Versace	
Third inventor's signature		Date 12 OCT 2007
Residence	252 East 8th Street, Apt. #2, South Boston, MA 02127	
Citizenship	Italy	
Post Office Address	Same as above	

Full Name of fourth inventor, if any	Fabrizio Santini	
Fourth inventor's signature		Date 10/12/07
Residence	22 Sigourney Street, Unit E, Jamaica Plain, MA 02130	
Citizenship	Italy	
Post Office Address	Same as above	

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0167.0000

PTO/SB/80 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 29127

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Neurala LLC
252 East 8th Street, Suite 2
Boston, MA 02127

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Heather Ames	Date	10-12-2007
Name	Heather Ames	Telephone	(510)205-8091
Title	COO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/96 (10-07)
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Neurala LLC

Application No./Patent No.: 11/860,254 Filed/Issue Date: September 24, 2007

Entitled: Graphic Processor Based Accelerator System and Method

Neurala LLC, a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [✓] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is_____ %)

in the patent application/patent identified above by virtue of either:

A. [✓] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/grant houston/	October 23, 2007
Signature	Date
J. Grant Houston	781-863-9991
Printed or Typed Name	Telephone Number
Attorney for Assignee	
Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

ASSIGNMENT

Whereas we, the undersigned,

Anatoli Gorchetchnikov, a citizen of Russia, residing at 43 Alma Avenue, Belmont, MA 02478;

Heather Marie Ames, a citizen of the United States, residing at 252 East 8th Street, Apt. #2, South Boston, MA 02127;

Massimiliano Versace, a citizen of Italy, residing at 252 East 8th Street, Apt. #2, South Boston, MA 02127;

Fabrizio Santini, a citizen of Italy, residing at 22 Sigourney Street, Unit E, Jamaica Plain, MA 02130;

hereby have made certain inventions or discoveries (or both) set forth in an application for Letters Patent of the United States of America entitled

GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

identified as Attorney Docket No. **0167.0001US1** which application was filed on **September 24, 2007**, and assigned Application No.**11/860,254**; and

Whereas, **Neurala LLC**, having an office and a place of business at 252 East 8th Street, Suite 2, South Boston, MA 02127, and which, together with its successors and assigns, is hereinafter called "Assignee," is desirous of acquiring the title, rights, benefits and privileges hereinafter recited;

Now, therefore, for valuable consideration furnished by Assignee to us, receipt and sufficiency of which we hereby acknowledge, we hereby, without reservation:

1. Assign, transfer and convey to Assignee the entire right, title and interest in and to said inventions and discoveries, said application for Letters Patent of the United States of America, any and all other applications for Letters Patent on said inventions and discoveries in whatsoever countries, including all divisional, renewal, substitute, continuation, continuation-in-part, reissue and Convention applications based in whole or in part upon said inventions or discoveries, or upon said applications, together with the right of priority of earlier-filed U.S. Provisional Application No. 60/826,892, filed on September 25, 2006, and any and all Letters Patent, reissues, reexaminations, and extensions of Letters Patent granted for said inventions and discoveries or upon said applications, and every priority right that is or may be predicated upon or arise from said inventions, said discoveries, said applications and said Letters Patent;

2. Authorize Assignee to file patent applications in any or all countries on any or all of said inventions and discoveries in our names or in the name of Assignee or otherwise as Assignee may deem advisable, under the International Convention or otherwise;

3. Authorize and request the Commissioner of Patents and Trademarks of the United States of America and the empowered officials of all other governments to issue or transfer all said Letters Patent to Assignee, as assignee of the entire right, title and interest therein or otherwise as Assignee may direct;

4. Warrant that we have not knowingly conveyed to others any right in said inventions, discoveries, applications or patents or any license to use the same or to make, use or sell anything embodying or utilizing any of said inventions or discoveries; and that we have good right to assign the same to Assignee without encumbrance;

5. Bind our heirs, legal representatives and assigns, as well as ourselves, to do, upon Assignee's request and at Assignee's expense, but without additional consideration to us or them, all acts reasonably serving to assure that the said inventions and discoveries, the said patent applications and the said Letters Patent shall be held and enjoyed by Assignee as fully and entirely as the same could have been held and enjoyed by us, our heirs, legal representatives and assigns if this assignment had not been made; and particularly to execute and deliver to Assignee all lawful application documents including petitions, specifications, and oaths, and all assignments, disclaimers, and lawful affidavits in form and substance as may be requested by Assignee; to communicate to Assignee all facts known to us relating to said inventions and discoveries or the history thereof; and to furnish Assignee with any and all documents, photographs, models, samples and other physical exhibits in our control or in the control of our heirs, legal representatives or assigns which may be useful for establishing the facts of our conceptions, disclosures, and reduction to practice of said inventions and discoveries.

In testimony of which we have executed this Assignment on the date indicated next to our name.

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Inventor's Signature: _____

Name: **Anatoli Gorchetchnikov**

Date: 10/12/07

State/Commonwealth of Massachusetts
County of Suffolk

On this 12th day of October, 2007, before me, the undersigned notary public, personally appeared **Anatoli Gorchetchnikov**, proved to me through satisfactory evidence of identification, which were MA driver's licence, to be the person whose name is signed on the preceding or attached document in my presence.

(SEAL)

Notary Public

My Commission expires ____/____/____

DELPHINE BIENVENU
Notary Public
Commonwealth of Massachusetts
My Commission Expires March 15, 2013

Inventor's Signature: _____

Name: **Heather Marie Ames**

Date: 10/12/07

State/Commonwealth of Massachusetts
County of Suffolk

On this 12th day of October, 2007, before me, the undersigned notary public, personally appeared **Heather Marie Ames**, proved to me through satisfactory evidence of identification, which were MA driver's licence, to be the person whose name is signed on the preceding or attached document in my presence.

(SEAL)

Notary Public

My Commission expires ____/____/____

DELPHINE BIENVENU
Notary Public
Commonwealth of Massachusetts
My Commission Expires March 15, 2013

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Inventor's Signature: _____ Name: **Massimiliano Versace**

Date: 12 OCT 2007

State/Commonwealth of Massachusetts
County of Suffolk

On this 12th day of OCTOBER, 2007, before me, the undersigned notary public, personally appeared **Massimiliano Versace**, proved to me through satisfactory evidence of identification, which were MA driver's license, to be the person whose name is signed on the preceding or attached document in my presence.

(SEAL) Notary Public

My Commission expires ___/___/___

DELPHINE BIENVENU
Notary Public
Commonwealth of Massachusetts
My Commission Expires March 15, 2013

Inventor's Signature: _____ Name: **Fabrizio Santini**

Date: 10/12/07

State/Commonwealth of Massachusetts
County of Suffolk

On this 12 day of October, 2007, before me, the undersigned notary public, personally appeared **Fabrizio Santini**, proved to me through satisfactory evidence of identification, which were MA driver's licence, to be the person whose name is signed on the preceding or attached document in my presence.

(SEAL) Notary Public

My Commission expires ___/___/___

DELPHINE BIENVENU
Notary Public
Commonwealth of Massachusetts
My Commission Expires March 15, 2013

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Electronic Patent Application Fee Transmittal

Application Number:	11860254
Filing Date:	24-Sep-2007
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Joseph G. Houston
Attorney Docket Number:	0167.0001US1

Filed as Small Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	75	75
Utility Search Fee	2111	1	255	255
Utility Examination Fee	2311	1	105	105
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	2051	1	65	65
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**500**

Electronic Acknowledgement Receipt

EFS ID:	2458324
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	29127
Filer:	Joseph G. Houston
Filer Authorized By:	
Attorney Docket Number:	0167.0001US1
Receipt Date:	15-NOV-2007
Filing Date:	24-SEP-2007
Time Stamp:	15:40:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$500
RAM confirmation Number	1049
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1		0167-0001US1_Reply_NTFMP.pdf	2121667 63f905bbe51c423a368840f7f35f89330 3aa4ae	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Preliminary Amendment		1	5	
	Drawings-only black and white line drawings		6	9	
Warnings:					
Information:					
2	Application Data Sheet	0167-0001US1_ADS_supplemental.pdf	1187974 e7d7ca7415694a6b84cdd97668bf7242 52c2c4f9	no	5
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	0167-0001US1_Filing_Rct_corrected.pdf	63838 218cbbbe16a323295521c638658a93d dab5858ca	no	3
Warnings:					
Information:					
4	Oath or Declaration filed	0167-0001US1_signed_decl.pdf	257044 40018ec2657be670b7238d6168dda35 52743e381	no	4
Warnings:					
Information:					
5	Power of Attorney	0167-0000_POA_Neurala.pdf	98599 01a817801fb939a8e31db585a4catec0f 0306005	no	1
Warnings:					
Information:					
6	Assignee showing of ownership per 37 CFR 3.73(b).	0167-0001US1_373b_signed_assign.pdf	412820 fa0a7de9404df307db0c7373e14dc164 0ab6bce7	no	5
Warnings:					
Information:					
7	Fee Worksheet (PTO-06)	fee-info.pdf	8522 5bce4e3317c9e4499d4173db2efbad50 21cba76a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4150464		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
11/860,254	09/24/2007	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☒ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x $ =		OR	x $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x $ =			x $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/15/2007

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	=	x $ =		OR	x $ =	
Independent (37 CFR 1.16(h))	* 3	Minus	***3	=	x $ =		OR	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =		OR	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =		OR	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/GLORIA ANTHONY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	TOT CLAIMS	IND CLAIMS
11/860,254	09/24/2007	3747	500	0167.0001US1	20	3

CONFIRMATION NO. 6266

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

FILING RECEIPT

OC000000026838973

Date Mailed: 12/05/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Anatoli Gorchetchnikov, Belmont, MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

Assignment For Published Patent Application

Neurala LLC, Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 29127

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/826,892 09/25/2006

Foreign Applications

If Required, Foreign Filing License Granted: 10/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/860,254**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **

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IPR2025-00606

Title

Graphic Processor Based Accelerator System and Method

Preliminary Class

123

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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IPR2025-00606

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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NVIDIA Ex1002
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IPR2025-00606

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

FORMALITIES LETTER

OC000000026838974

Date Mailed: 12/05/2007

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings have a line quality that is too light to be reproduced (weight of all lines and letters must be heavy enough to permit adequate reproduction) or text that is illegible (reference characters, sheet numbers, and view numbers must be plain and legible) see 37 CFR 1.84(l) and (p)(1)); See Figure(s) 2.
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 3 and 4 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/jsdill/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199

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IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
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11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

WITHDRAWAL NOTICE

OC000000026838971

Date Mailed: 12/05/2007

WITHDRAWAL OF PREVIOUSLY SENT NOTICE

The Notice mailed on 10/04/2007 was sent in error and is hereby withdrawn. A corrected Notice is enclosed. The time period for reply runs from the mail date of the corrected Notice. The Office regrets any inconvenience the error may have caused.

A copy of this notice MUST be returned with the reply.

/jsdill/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re:	Anatoli Gorchetchnikov *et al.*	Confirmation No:	6266
Application No:	11/860,254	Group:	3747
Filed:	September 24, 2007	Examiner:	Not yet assigned
For:	Graphic Processor Based Accelerator System and Method		
Customer No.:	29127		
Attorney Docket No.	0167.0001US1		

REPLACEMENT DRAWING(S) FOR
NOTICE TO FILE CORRECTED APPLICATION PAPERS

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the pending Notice to File Corrected Application Papers, please replace original sheets 2/5, 3/5 and 4/5 including Figs. 2, 3 and 4, with the attached new sheets 2/5, 3/5 and 4/5 including Figs. 2, 3 and 4.

Respectfully submitted,

By /grant houston/
J. Grant Houston
Registration No.: 35,900
Tel.: 781 863 9991
Fax: 781 863 9931

Lexington, Massachusetts 02421
Date: February 4, 2008

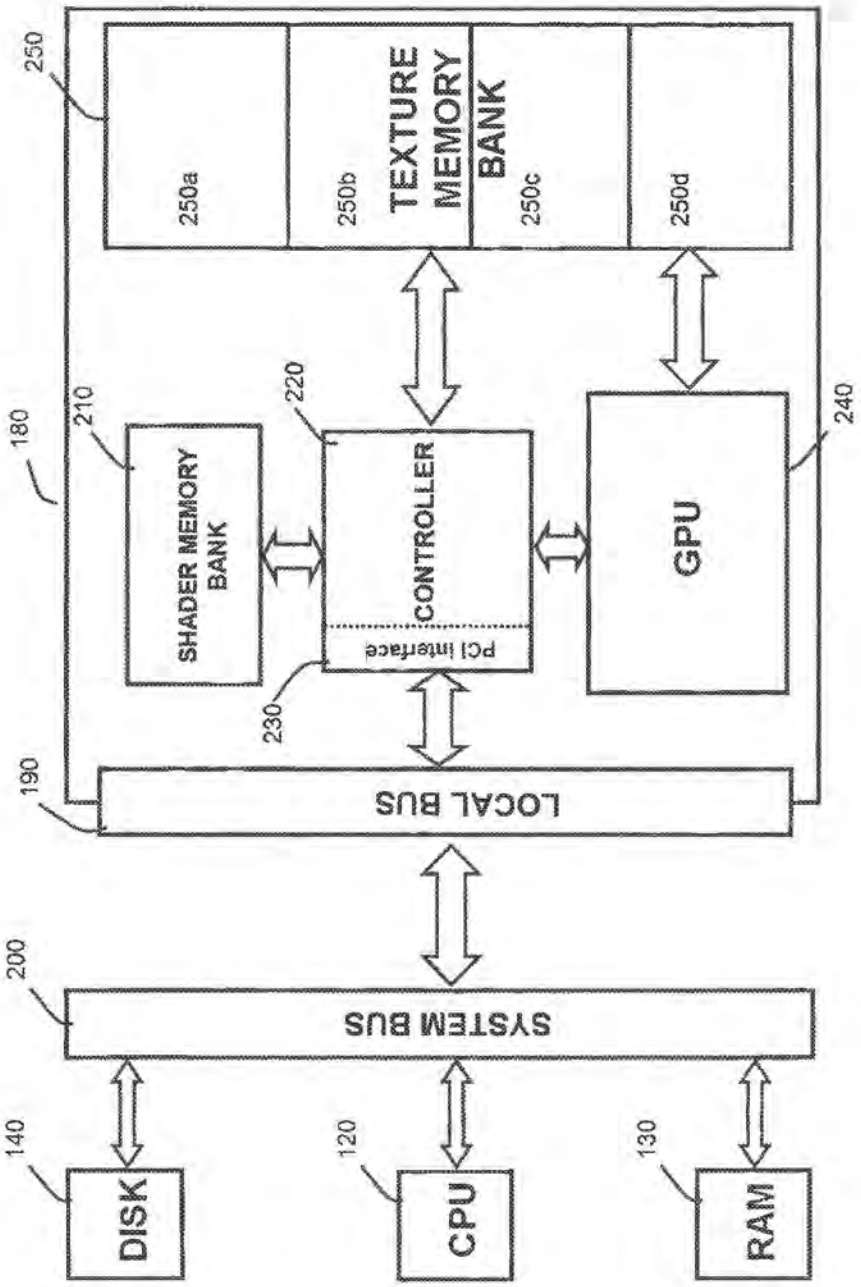
250
250a
250b
TEXTURE MEMORY BANK
250c
250d
180
210
SHADER MEMORY BANK
220
CONTROLLER
PCI interface
230
GPU
240
190
LOCAL BUS
200
SYSTEM BUS
140
DISK
120
CPU
130
RAM

FIG. 2

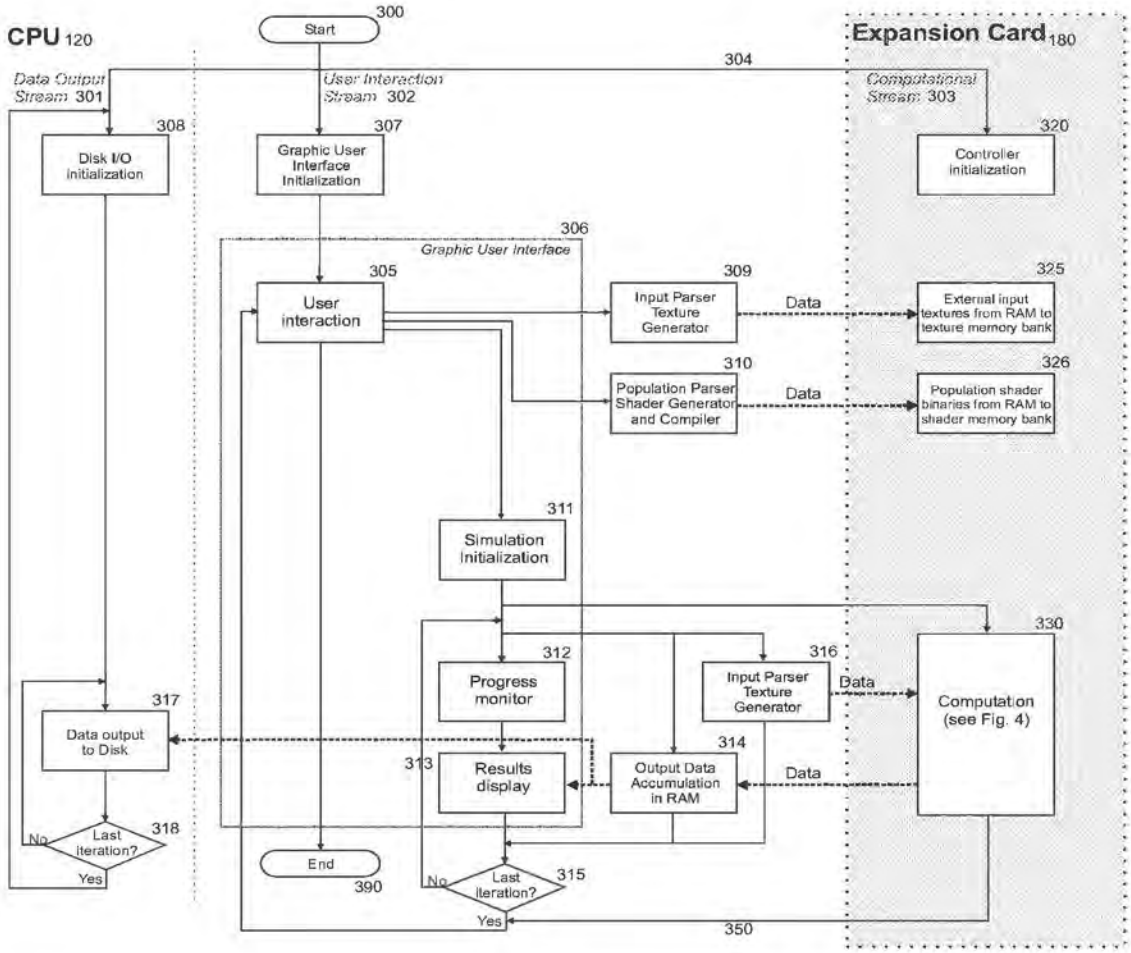
CPU 120
Start
300
Expansion Card 180
304
Data Output Stream 301
User Interaction Stream 302
Computational Stream 303
308
Disk I/O initialization
307
Graphic User Interface Initialization
320
Controller initialization
306
Graphic User Interface
305
User interaction
309
Input Parser Texture Generator
Data
325
External input textures from RAM to texture memory bank
310
Population Parser Shader Generator and Compiler
Data
326
Population shader binaries from RAM to shader memory bank
311
Simulation Initialization
330
312
Progress monitor
316
Input Parser Texture Generator
Data
Computation (see Fig. 4)
317
Data output to Disk
313
Results display
314
Output Data Accumulation in RAM
Data
No
Last iteration?
318
Yes
End
390
No
Last iteration?
315
Yes
350

FIG 3

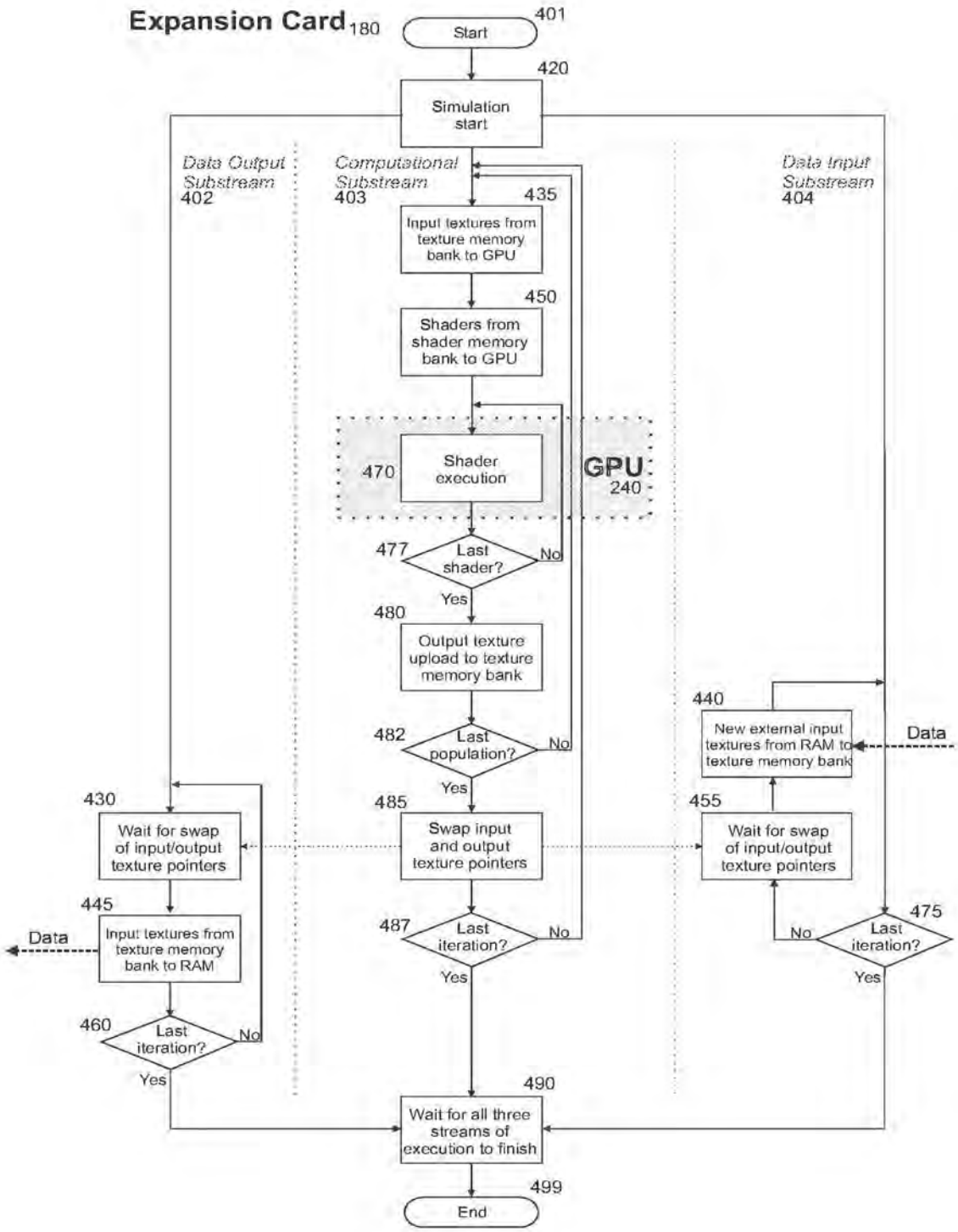
Expansion Card 180
401
Start
420
Simulation start
Data Output Substream 402
Computational Substream 403
Data Input Substream 404
435
Input textures from texture memory bank to GPU
450
Shaders from shader memory bank to GPU
470
Shader execution
GPU 240
477
Last shader?
No
Yes
480
Output texture upload to texture memory bank
482
Last population?
No
Yes
485
Swap input and output texture pointers
487
Last iteration?
No
Yes
440
New external input textures from RAM to texture memory bank
Data
455
Wait for swap of input/output texture pointers
475
Last iteration?
No
Yes
430
Wait for swap of input/output texture pointers
445
Input textures from texture memory bank to RAM
Data
460
Last iteration?
No
Yes
490
Wait for all three streams of execution to finish
499
End

FIG 4

Electronic Acknowledgement Receipt

EFS ID:	2808040
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	29127
Filer:	Joseph G. Houston
Filer Authorized By:	
Attorney Docket Number:	0167.0001US1
Receipt Date:	04-FEB-2008
Filing Date:	24-SEP-2007
Time Stamp:	17:29:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	0167-0001US1_Trans_Replace_Figs.pdf	92312 6b7e1a9e908e9fba6f9c1039a4f706878957b6d6	no	1

Warnings:

Information:

2	Applicant Response to Pre-Exam Formalities Notice	0167-0001US1_Replacemnt_Figs.pdf	468152 eb441cd449479e9009660aa008ddc4bff a383442c	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	560464		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	TOT CLAIMS	IND CLAIMS
11/860,254	09/24/2007	3747	500	0167.0001US1	20	3

CONFIRMATION NO. 6266

UPDATED FILING RECEIPT

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA 02421

OC000000028199844

Date Mailed: 02/13/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Anatoli Gorchetchnikov, Belmont, MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

Assignment For Published Patent Application

Neurala LLC, Boston, MA

Power of Attorney: The patent practitioners associated with Customer Number 29127

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/826,892 09/25/2006

Foreign Applications

If Required, Foreign Filing License Granted: 10/04/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/860,254**

Projected Publication Date: 05/22/2008

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Title

Graphic Processor Based Accelerator System and Method

Preliminary Class

123

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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PTO/SB/83 (01-06)
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REQUEST FOR WITHDRAWAL AS ATTORNEY OR AGENT AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	11/860,254
Filing Date	September 24, 2007
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	3747
Examiner Name	Not yet assigned
Attorney Docket Number	0167.0001US1

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Please withdraw me as attorney or agent for the above identified patent application, and

- [ ] all the attorneys/agents of record.
- [ ] the attorneys/agents (with registration numbers) listed on the attached paper(s), or
- [x] the attorneys/agents associated with Customer Number 29127

NOTE: This box can only be checked when the power of attorney of record in the application is to all the practitioners associated with a customer number.

The reasons for this request are:

CORRESPONDENCE ADDRESS

1. [ ] The correspondence address is NOT affected by this withdrawal.
2. [x] Change the correspondence address and direct all future correspondence to:

[ ] The address associated with Customer Number:

OR

[x] Firm *or* Individual Name	Heather Ames				
Address	252 East 8th St. Apt. 2				
City	Boston	State	MA	Zip	02127
Country	US				
Telephone	510-205-8091	Email	ames@neurala.com		

Signature	/grant houston/		
Name	J. Grant Houston	Registration No.	35,900
Date	May 12, 2008	Telephone No.	781-863-9991

NOTE: Withdrawal is effective when approved rather than when received. Unless there are at least 30 days between approval of withdrawal and the expiration date of a time period for response or possible extension period, the request to withdraw is normally disapproved.

This collection of information is required by 37 CFR 1.36. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	3289053
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	29127
Filer:	Joseph G. Houston
Filer Authorized By:	
Attorney Docket Number:	0167.0001US1
Receipt Date:	12-MAY-2008
Filing Date:	24-SEP-2007
Time Stamp:	18:02:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	0167-0001US1_Request_Withdrawal.pdf	410235 6e52f109e3b56d716642d176e76dd2069c139f8d	no	1

Warnings:

Information:

Total Files Size (in bytes):	410235

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

29127
HOUSTON ELISEEVA
4 MILITIA DRIVE, SUITE 4
LEXINGTON, MA02421

Title: Graphic Processor Based Accelerator System and Method

Publication No. US-2008-0117220-A1
Publication Date: 05/22/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

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LEXINGTON MA 02421

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AUG 18 2008

In re Application of

GORCHETCHNIKOV, Anatoli et al.
Application No. 11/860,254
Filed: September 24, 2007
Attorney Docket No. **0167.0001US1**

DECISION ON PETITION
TO WITHDRAW
FROM RECORD

This is a decision on the Request to Withdraw as attorney or agent of record under 37 C.F.R. § 1.36(b), filed May 12, 2008.

The request is **NOT APPROVED**.

A grantable request to withdraw as attorney/agent of record must be signed by every attorney/agent seeking to withdraw or contain a clear indication that one attorney is signing on behalf of another/others. The Office requires the practitioner(s) requesting withdrawal to certify that he, she, or they have: (1) given reasonable notice to the client, prior to the expiration of the response period, that the practitioner(s) intends to withdraw from employment; (2) delivered to the client or a duly authorized representative of the client all papers and property (including funds) to which the client is entitled; and (3) notified the client of any responses that may be due and the time frame within which the client must respond, pursuant 37 CFR 10.40(c).

The request cannot be approved because there is no indication that the acts noted in the above-identified certifications have been performed.

The request cannot be approved because no reasons for withdrawal have been provided. The Office cannot, at this time, determine whether practitioner's request is one of the mandatory or permissive reasons enumerated in 37 CFR 10.40. Any subsequent requests must include reasons for withdrawal. Please note that there is a space provided for on PTO/SB/83 (Request to Withdraw as Attorney or Agent) to supply practitioner's reasons.

All future communications from the Office will continue to be directed to the above-listed address until otherwise notified by applicant.

Telephone inquiries concerning this decision should be directed to Tredelle Jackson at 571-272- 2783.

Tredelle D. Jackson
Paralegal Specialist
Office of Petitions

cc: **HEATHER AMES**
252 EAST 8TH ST.
APT. 2
BOSTON MA 02127

PTO/SB/122 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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CHANGE OF CORRESPONDENCE ADDRESS
Application

Address to:
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Application Number	11/860,254
Filing Date	September 24, 2007
First Named Inventor	Anatoli Gorchetchnikov
Art Unit	3747
Examiner Name	Not yet assigned
Attorney Docket Number	0167.0001US1

Please change the Correspondence Address for the above-identified patent application to:

☐ The address associated with Customer Number:

OR

☑ Firm or Individual Name Heather Ames

Address 252 East 8th St., Apt 2

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Country U.S.

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I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☑ Attorney or agent of record. Registration Number 35,900

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number_____.

Signature /grant houston/

Typed or Printed Name J. Grant Houston

Date August 25, 2008 | Telephone 781-863-9991

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	3834084
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Customer Number:	29127
Filer:	Joseph G. Houston
Filer Authorized By:	
Attorney Docket Number:	0167.0001US1
Receipt Date:	26-AUG-2008
Filing Date:	24-SEP-2007
Time Stamp:	15:21:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	0167-0001US1_Change_Corresp_Add.pdf	223544 16d035e8544d3f9e6fc54969b1fcf22b8f07d9	no	1

Warnings:

Information:

Total Files Size (in bytes):	223544

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

7590 09/16/2010

Heather Ames
Apt 2
252 East 8th St.
Boston, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
09/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)	
	11/860,254	GORCHETCHNIKOV ET AL.	
	Examiner	Art Unit	
	MAURICE MCDOWELL, JR	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 24 September 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date: _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4-5, 10, 12, 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. Pub. No.: US 2007/0052713 A1 in view of Evans Pub. No.: US 2005/0166042 A1.

3. Regarding claim 1, Chung teaches: A computer system, comprising: a central processing unit (fig. 4, 320); main memory accessed by the central processing unit (fig. 4, 370); a video system for driving a video monitor in response to the central processing unit (fig. 1, 110 see also [0051]); and an accelerator receiving input data from and providing output data to the central processing unit (fig. 4, 350 see also [0062]), the accelerator comprising: at least one graphics processing unit (fig. 4, 351 see also [0062]); accelerator memory for the graphic processing unit (fig. 4, 355 see also [0063]).

4. Chung doesn't teach: an accelerator controller for moving the input data into the accelerator memory, moving output data from the accelerator memory, and supervising data exchange between the accelerator memory and at least one graphic processing unit.

5. The analogous prior art Evans teaches: an accelerator controller for moving the input data into the accelerator memory (fig. 4, 404-408 see also [0064]) (An accelerator controller is suggested or implicitly taught because the input data is moved into the accelerator memory), moving output data from the accelerator memory (fig. 3, 300-306 see also [0061]), and supervising data exchange between the accelerator memory and at least one graphic processing unit (fig. 4, 408 see also [0064]) for the benefit of providing a method that ensures that data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted [0098].

6. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine an accelerator controller for moving the input data into the accelerator memory, moving output data from the accelerator memory, and supervising data exchange between the accelerator memory and at least one graphic processing unit as shown in Evans with Chung for the benefit of providing a method that ensures that data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted.

7. Regarding claim 4, Evans further teaches: A computer system, wherein the accelerator controller sends instructions to the at least one graphics processing unit, which executes the instructions on data (fig. 4, 408 see also [0064]), and wherein during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transfers output data from the accelerator memory to main memory of the central processing unit (fig. 3, 302 and 304 see also [0061]).

8. Regarding claim 5, Evans further teaches: A computer system, wherein the accelerator controller comprises an interface controller that enables the accelerator to communicate over a bus of the computer system with the central processing unit (fig. 3, 304 see also [0061]).

9. Regarding claim 10, Chung teaches: An accelerator system for a computer system, the accelerator system comprising: at least one graphics processing unit (fig. 4, 351 see also [0062]); accelerator memory for the graphic processing unit (fig. 4, 355 see also [0063]).

10. Chung doesn't teach: an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory.

11. The analogous prior art Evans teaches: an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory (fig. 4, 408 see also [0064]) for the benefit of providing a method that ensures that data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted.

12. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine an accelerator controller for moving data between the at least one graphics processing unit and the accelerator memory as shown in Evans with Chung for the benefit of providing a method that ensures that data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted.

13. Regarding claim 12, Evans further teaches: A computer system, wherein the accelerator controller sends instructions to the at least one graphics processing unit, which executes the instructions on data (fig. 4, 408 see also [0064]), and wherein during the execution of the

instructions by the at least one graphics processing unit, the accelerator controller transfers output data from the accelerator system (fig. 3, 302 and 304 see also [0061]).

14. Regarding claim 17, Chung teaches: A method for performing numerical simulations in a computer system, the method comprising: a central processing unit loading input data into an accelerator system from main memory of the central processing unit (fig. 4, 320).

15. Chung doesn't teach: an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data; the accelerator controller transferring output data generated by the graphic processing unit to the central processing unit as output data.

16. The analogous prior art Evans teaches: an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data (fig. 4, 404-408 see also [0064]); the accelerator controller transferring output data generated by the graphic processing unit to the central processing unit as output data (fig. 3, 300-306 see also [0061]) (The output data is provided to the cpu because it is put in the system memory) for the benefit of providing a method that ensures that data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted.

17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine an accelerator controller transferring the input data to a graphics processing unit with instructions to be performed on the input data; the accelerator controller transferring output data generated by the graphic processing unit to the central processing unit as output data as shown in Evans with Chung for the benefit of providing a method that ensures that

data that is intended for used by a video card can be encrypted such that anytime the data is provided onto a bus between the video card and the computer system, the data is encrypted.

18. Regarding claim 18, Evans further teaches: A method, further comprising: the accelerator controller sending instructions to the at least one graphics processing unit, which executes the instructions on data (fig. 4, 408 see also [0064]); and during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transferring output data from the accelerator memory to main memory of the central processing unit (fig. 3, 302 and 304 see also [0061]).

19. Claims 3, 6-9, 11, 13-16, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. Pub. No.: US 2007/0052713 A1 in view of Evans Pub. No.: US 2005/0166042 A1 further in view of Poulton et al. Patent No.: 5,388,206.

20. Regarding claim 3, the previous combination of Chung and Evans remains as above but doesn't teach: A computer system, wherein the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit.

21. The analogous prior art Poulton teaches: A computer system, wherein the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit (fig. 12, 640 and 650 see also col. 14 lines 4-7) (The sequencers control the order of the gpu because each can branch conditionally) for the benefit of to provide an image generation system which is scalable over a wide variety of performance levels and to arbitrarily high levels by combining an arbitrary number of renderers (col. 1 lines 62-67).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine a computer system, wherein the accelerator controller dictates an order of

execution of instructions to the at least one graphics processing unit as shown in Poulton with the previous combination for the benefit of to provide an image generation system which is scalable over a wide variety of performance levels and to arbitrarily high levels by combining an arbitrary number of renderers.

23. Regarding claim 6, Poulton further teaches: A computer system, wherein the accelerator memory comprises a texture memory bank for storing simulation data and a shader memory bank for storing operations to be performed on the simulation data by the at least one graphic processing unit (col. 15 lines 55-68).

24. Regarding claim 7, Poulton further teaches: A computer system, wherein the texture memory is partitioned into sections in which a first section holds input data patterns, a second section holds data textures representing internal variables, a third section holds data textures used as input at a particular computation step, and a fourth section holds data textures used to store an output of a computational step on the at least one graphic processing unit (col. 15 lines 55-68) (The 8 banks of memory are partitioned because the banks are controlled globally but the addresses may vary).

25. Regarding claim 8, Poulton further teaches: A computer system, wherein the accelerator controller inputs data into at least one graphic processing unit and a series of instructions to the at least one graphic processing unit, which then successively executes the instructions on the data (fig. 11, 110 see also col. 14 lines 37-45).

26. Regarding claim 9, Poulton further teaches: A computer system, wherein the accelerator controller performs successive iterations by feeding output data generated by the at least one

graphic processing unit and input data for a next iteration into the at least one graphic processing unit (col. 2 lines 20-26) (The computed pixel values are the same as the output data).

27. Regarding claim 11, Poulton further teaches: A computer system, wherein the accelerator controller dictates an order of execution of instructions to the at least one graphics processing unit (fig. 12, 640 and 650 see also col. 14 lines 4-7).

28. Regarding claim 13, Poulton further teaches: A computer system, wherein the accelerator memory comprises a texture memory bank for storing simulation data and a shader memory bank for storing operations to be performed on the simulation data by the at least one graphic processing unit (col. 15 lines 55-68).

29. Regarding claim 14, Poulton further teaches: A computer system, wherein the texture memory is partitioned into sections in which a first section holds input data patterns, a second section holds data textures representing internal variables, a third section holds data textures used as input at a particular computation step, and a fourth section holds data textures used to store an output of a computational step on the at least one graphic processing unit (col. 15 lines 55-68).

30. Regarding claim 15, Poulton further teaches: A computer system, wherein the accelerator controller inputs data into at least one graphic processing unit and a series of instructions to the at least one graphic processing unit, which then successively executes the instructions on the data (fig. 11, 110 see also col. 14 lines 37-45).

31. Regarding claim 16, Poulton further teaches: A computer system, wherein the accelerator controller performs successive iterations by feeding output data generated by the at least one graphic processing unit and input data for a next iteration into the at least one graphic processing unit (col. 2 lines 20-26).

32. Regarding claim 19, Poulton further teaches: A method, further comprising: partitioning accelerator memory of accelerator system a first section holding input data patterns, a second section holding data textures representing internal variables, a third section holding data textures used as input at a particular computation step, and a fourth section holding data textures used to store an output of a computational step on the at least one graphic processing unit (col. 15 lines 55-68).

33. Regarding claim 20, Poulton further teaches: A method, further comprising the accelerator controller performing successive iterations by feeding output data generated by the at least one graphic processing unit and input data for a next iteration into the at least one graphic processing unit (col. 2 lines 20-26).

34. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. Pub. No.: US 2007/0052713 A1 in view of Evans Pub. No.: US 2005/0166042 A1 further in view of Ganzer Pub. No.: US 2007/0279429 A1.

35. Regarding claim 2, the previous combination of Chung and Evans remains as above but doesn't teach: A computer system, wherein the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit.

36. The analogous prior art Ganzer teaches: A computer system, wherein the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit [0022] for the benefit of providing substantially real-time interactive modeling such as might be used in simulation of hydrocarbon reservoirs or the like [0014].

37. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine a computer system, wherein the central processing unit transfers the input data for a simulation to the accelerator, after which the accelerator executes simulation computations to generate the output data, which is transferred to the central processing unit as shown in Ganzer with the previous combination for the benefit of providing substantially real-time interactive modeling such as might be used in simulation of hydrocarbon reservoirs or the like.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAURICE MCDOWELL, JR whose telephone number is (571)270-3707. The examiner can normally be reached on Mon-Friday 7:30am - 5:00pm Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on 571--272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MM

/XIAO M. WU/

Supervisory Patent Examiner, Art Unit 2628

Notice of References Cited	Application/Control No. 11/860,254	Applicant(s)/Patent Under Reexamination GORCHETCHNIKOV ET AL.	
	Examiner MAURICE MCDOWELL, JR	Art Unit 2628	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,388,206 A	02-1995	Poulton et al.	345/505
*	B	US-2005/0166042 A1	07-2005	Evans, Glenn F.	713/150
*	C	US-2007/0052713 A1	03-2007	Chung et al.	345/501
*	D	US-2007/0279429 A1	12-2007	Ganzer, Leonhard	345/582
	E	US-			
	F	US-			
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	H	US-			
	I	US-			
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	Art Unit
	MAURICE MCDOWELL, JR	2628

SEARCHED

Class	Subclass	Date	Examiner

SEARCH NOTES

Search Notes	Date	Examiner
East text search	9/9/10	MM
Inventor name search	9/9/10	MM
Foreign database search	9/9/10	MM
NPL search on ACM and IEEE databases	9/9/10	MM
Class/subclass combined with text search	9/9/10	MM

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	Art Unit
	MAURICE MCDOWELL, JR	2628

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/09/2010								
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BIB DATA SHEET

CONFIRMATION NO. 6266

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/860,254	09/24/2007 RULE	123	2628	0167.0001US1

APPLICANTS

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Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

**** CONTINUING DATA ***************************

This appln claims benefit of 60/826,892 09/25/2006

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
10/04/2007

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MAURICE L MCDOWELL, JR/ Examiner's Signature	☐ Met after Allowance MM Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	5	20	3

ADDRESS

Heather Ames
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TITLE

Graphic Processor Based Accelerator System and Method

FILING FEE RECEIVED		
500	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07)

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14	US-6246418-$.DID. OR US-20060235667-$.DID. OR US-20060277012-$.DID. OR US-20060282243-$.DID. OR US-20070091090-$.DID. OR US-20070219766-$.DID. OR US-20080278482-$.DID.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:02
L2	31795	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (command instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:50
L3	855	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (command instruction) with (loop$3 iterat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:50

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L4	168	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (command instruction) with (loop$3 iterat$3) and simulation	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:51
L5	99	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (command instruction) with (loop$3 iterat$3) and simulation and texture	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:51
L6	16589	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (gpu vpu (visual graphics media multi$1media video 3d) adj2 (unit engine process $3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:58

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L7	13738	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (gpu vpu (visual graphics media multi$1media video 3d) adj2 (unit engine process $3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 12:58
L8	28	texture with (logical partition$3 section$3) near5 (storage memory register buffer ram vram sdram) same (accelerat$3 graphics$1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:01
L9	14	texture with (two three four multiple plurality) near5 (logical partition$3 section$3) near5 (storage memory register buffer ram vram sdram) same (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:08

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		$1accelerat$3 expansion $1accelerat$3)				
L10	16	texture with (four multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) same (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:10
L11	2	l10 not l9	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:10
L12	18	texture with (four fourth third three five fifth multiple plurality) near5 (logical partition$3 section $3 bank) near5 (storage memory register buffer ram vram sdram) same (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:13
L13	2	l12 not l10	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:13

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L14	117	texture with (four multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:14
L15	61	texture with (four multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) and (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:15
L16	61	texture with (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) and (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:15

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L17	34	texture with (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) and (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (control$3 adj2 (chip module unit device apparatus) control$4 (data $1path data adj path) near2 controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:16
L18	0	texture with (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) with (internal local) adj2 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:49
L19	1	texture with (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (storage memory register buffer ram vram sdram) same (internal local) adj2 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:49
L20	1	texture with (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (bank cache storage memory register buffer ram vram sdram) same (internal local) adj2 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:50

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L21	1	texture same (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) near5 (bank cache storage memory register buffer ram vram sdram) same (internal local) adj2 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:50
L22	1	texture same (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) same (bank cache storage memory register buffer ram vram sdram) same (internal local) adj2 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:50
L23	1	texture same (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) same (bank cache storage memory register buffer ram vram sdram) same (internal local) near3 (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:50
L24	1	texture same (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) same (bank cache storage memory register buffer ram vram sdram) same (internal local) with (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:51
L25	2	texture same (four fourth fifth five multiple plurality) near5 (logical partition$3 section$3 bank) same (bank cache storage memory register buffer ram vram sdram) same (internal local) same (variable identifier)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 13:51
L26	3	"20070052713"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 14:28
L27	3	"20050166042"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 14:28
L28	42	"5388206"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 14:28

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L29	4	(("20070052713") or ("20050166042") or ("5388206") or ("20070279429")).PN.	US-PGPUB; USPAT	OR	OFF	2010/09/08 14:29
S1	74887	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:12
S2	1365	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4 with (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:12
S3	63	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4 with (cpu central adj2 process$3) and vertex	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:13
S4	16	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4 with (cpu central adj2 process$3) and vertex and simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:13
S5	1127236	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter accelerat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:18
S6	85392	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter accelerat$3)) near3 (control$3 asic fpga software program application manager)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:20
S7	3285	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter accelerat$3)) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:21
S8	11	graphics$1accelerat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:28

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S9	1142522	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:37
S10	36287	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:37
S11	4081	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:38

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S12	705	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:39
S13	16	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4) same (gpu vpu (visual graphic media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:39
S14	3	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:47

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		(control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4) same ((general$1purpose general adj2 purpose) adj2 (graphic$2) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU)				
S15	10	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4 transfer$4) same ((general$1purpose general adj2 purpose) adj2 (graphic$2) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:48
S16	31028	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj2 (control$3 asic fpga software program application manager)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:54

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S17	192	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj2 (control$3 asic fpga software program application manager) with (gpu vpu (visual graphics media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:54
S18	189	S17 not S13	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:55
S19	189	S18 not S3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 19:55
S20	63	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4 with (cpu central adj2 process$3) and vertex	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:56
S22	16	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4) same (gpu vpu (visual graphic media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:57

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S23	193	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj2 (control$3 asic fpga software program application manager) with (gpu vpu (visual graphics media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:57
S24	190	S23 not S22	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:57
S25	190	S24 not S20	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:57
S26	17	S25 and (data$1path data adj path)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 10:57
S27	204	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (cpu central adj2 process$3) same (data$1path data adj path)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44
S28	63	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 (card adapter)) near3 control$4 with (cpu central adj2 process$3) and vertex	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44

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S29	16	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 asic fpga software program application manager) same (cpu central adj2 process$3) same (input$4 and output$4) same (gpu vpu (visual graphic media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44
S30	193	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4) adj2 (card board adapter accelerat$3) video$1board graphics$1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj2 (control$3 asic fpga software program application manager) with (gpu vpu (visual graphics media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44
S31	190	S30 not S29	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44
S32	190	S31 not S28	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44
S33	197	S27 not S32	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:44

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S34	27	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (cpu central adj2 process$3) same (data$1path data adj path) same (gpu vpu (visual graphics media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:46
S35	37	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (cpu central adj2 process$3) same (arbiter data$1path data adj path) same (gpu vpu (visual graphics media multi$1media) adj2 (unit engine process$3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:51
S36	10	S35 not S34	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:51

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S37	94737	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 adj2 (chip module unit device apparatus) control$4 (data $1path data adj path) near2 controller asic fpga software program application manager micro $1controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:56
S38	3167	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 adj2 (chip module unit device apparatus) control$4 (data $1path data adj path) near2 controller asic fpga software program application manager micro $1controller) same ((main system) adj2 (ram volatile memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:57

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S39	43	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 adj2 (chip module unit device apparatus) control$4 (data $1path data adj path) near2 controller asic fpga software program application manager micro $1controller) with (local adj2 (memory storage bank cache register)) same ((main system) adj2 (ram volatile memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 11:59
S40	89	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near3 (control$3 adj2 (chip module unit device apparatus) control$4 (data $1path data adj path) near2 controller asic fpga software program application manager micro $1controller) with (local adj2 (memory storage bank cache register))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:23
S41	46	S40 not S39	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:23

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S42	24	S41 not protocol	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:25
S43	3610	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj (memory storage cache bank vram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:29
S44	120	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj (memory storage cache bank vram) with (gpu vpu (visual graphics media multi$1media video 3d) adj2 (unit engine process $3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:29
S45	31	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 12:30

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		(memory storage cache bank vram) with (gpu vpu (visual graphics media multi$1media video 3d) adj2 (unit engine process $3) gpgpu) same (cpu central adj2 process$3)				
S46	45	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (texture shader vertex shading) adj2 (memory storage cache bank vram) same (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:23
S47	31	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) adj (memory storage cache bank vram) with (gpu vpu (visual graphics media multi$1media video 3d) adj2 (unit engine process $3) gpgpu) same (cpu central adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:23
S48	44	S46 not S47	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:23

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S49	1	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near5 (shading shader vertex) adj2 bank$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:53
S50	1	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near5 (texture shading shader vertex) adj2 bank$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:54
S51	4	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) near5 (texture shading shader vertex) near5 bank$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:54

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S52	4	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (texture shading shader vertex) near5 bank$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:57
S53	7	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (texture shading shader vertex) near5 bank$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 14:57
S54	4177	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) same (texture mip$1map mip adj map)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:02

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S55	2097	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (texture mip$1map mip adj map)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:03
S56	1	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (texture mip$1map mip adj map) adj2 bank	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:03
S57	4	(accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3) with (texture mip$1map mip adj map) near5 bank	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:03
S58	1	(texture and shader) adj2 bank	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:13

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S59	4	(texture and shader) near3 bank	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:13
S60	4	(texture and shader) near3 (cache adj (address $3 set portion)bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:15
S61	4	(texture and shader) near3 (cache adj2 (address $3 set portion)bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:16
S62	7	(texture and shader) with (cache adj2 (address$3 set portion)bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:16
S63	3	S62 not S61	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:16
S64	27	(texture and (vertex shader)) with (cache adj2 (address$3 set portion) bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:16
S65	20	S64 not S62	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:17
S66	3	(texture and (vertex shader)) with (cache adj2 (address$3 set portion) bank) same (accelerat$3 graphics$1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:18
S67	0	(texture and (vertex shader)) with (cache adj2 (address$3 set portion) bank) with simd	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:19
S68	0	(texture and (vertex shader)) with (cache adj2 (address$3 set portion) bank) same simd	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:19
S69	0	(texture and (vertex shader)) with (cache near3 (address$3 set portion)bank) same simd	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:21

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S70	3	(texture and (vertex shader)) with (cache near3 (address$3 set portion)bank) same gpu	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:22
S71	3	(texture and (vertex shader)) with (cache near3 (partition$3 address $3 set portion)bank) same gpu	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:22
S72	36	(texture and (vertex shader)) with (cache near3 (partition$3 address $3 set portion)bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:22
S73	9	S72 not S64	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/07 15:23
S74	4962	(data adj2 (array vector) texture and (vertex shader)) with (logical partition$3 address$3 set portion bank) near5 (storage memory register buffer ram vram sdram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 06:33
S75	16	(data adj2 (array vector) texture and (vertex shader)) with (logical partition$3 address$3 set portion bank) near5 (storage memory register buffer ram vram sdram) with (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 06:34

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S76	36	(data adj2 (array vector) texture and (vertex shader)) with (logical partition$3 address$3 set portion bank) near5 (storage memory register buffer ram vram sdram) same (accelerat$3 graphics $1accelerat$3 graphics adj2 accelerat$3 (video graphics expan$4 accelerator) adj2 (card board adapter accelerat $3) video$1board graphics $1board expansion $1board graphics$1card video$1card expansion $1card video$1adapter graphics$1adapter expansion$1adapter video $1accelerat$3 expansion $1accelerat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 06:40
S77	20	S76 not S75	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/08 06:41

EAST Search History (Interference)

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9/8/2010 2:31:18 PM
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EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	Gorchetchnikov-anatoli$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:11
S2	1	ames-heather$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:12
S3	1	versace-massimiliano$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:12
S4	1	santini-fabrizio$.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:12
S5	1	(S1 or S2 or S3 or S4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:12
S6	183556	(pc computer comput$3) adj2 system	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:14
S7	5936	S6 same ((main system) adj2 (ram volatile memory))	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:16
S8	30	S6 same ((main system) adj2 (ram volatile memory)) and ((video moving adj image) adj2 system)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:16
S9	0	S6 same ((main system) adj2 (ram volatile memory)) and ((video moving adj image) adj2 system) and accelerat$3	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:17
S10	0	S6 same ((main system) adj2 (ram volatile memory)) and ((video moving adj image) adj2 system) and (accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:23

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S11	0	S6 same ((main system) near3 (ram volatile memory)) and ((video moving adj image) adj2 system) and (accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:24
S12	8	S6 same ((main system) near3 (ram volatile memory)) and ((video moving adj image) near3 system) and (accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:24
S13	25	((main system) near3 (ram volatile memory)) and ((video moving adj image) near3 system) and (accelerat$3 off $1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:26
S14	0	S13 and (gpgpu general adj2 purpose)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:27
S15	19537	(gpgpu general adj2 purpose)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:27
S16	1	(gpgpu general adj2 purpose adj gpu)	EPO; JPO; DERWENT	OR	ON	2010/09/05 17:27
S17	11452	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 (storage bank cache memory non $1volatile)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:48
S18	526	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 ((storage bank cache memory non $1volatile) and (controller))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:48

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S19	166	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 ((storage bank cache memory non $1volatile) and (controller)) and (gpu vpu (visual graphic) adj2 process$3 gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:51
S20	151	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 ((storage bank cache memory non $1volatile) and (controller)) and (gpu vpu (visual graphic) adj2 process$3 gpgpu) and (cpu central adj2 process $3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:52
S21	1	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 ((storage bank cache memory non $1volatile) and (controller)) and (gpu vpu (visual graphic) adj2 process$3 gpgpu) and (cpu central adj2 process $3) and ((shader shading vertex) adj2 (bank cache memory ram vram))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:55
S22	1	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) near2 ((storage bank cache memory non $1volatile) and (controller)) and (gpu vpu (visual graphic) adj2 process$3 gpgpu) and ((shader shading vertex) adj2 (bank cache memory ram vram))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:55

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S23	45	(accelerat$3 off$1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) same ((storage bank cache memory non $1volatile) and (controller)) and (gpu vpu (visual graphic) adj2 process$3 gpgpu) and ((shader shading vertex) adj2 (bank cache memory ram vram))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 17:55
S24	1	S23 and (general adj2 purpose adj2 gpu gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:00
S25	136	(general adj2 purpose adj2 gpu gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:00
S26	64	S25 and (accelerat$3 off $1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:01
S27	8	S25 and (accelerat$3 off $1load$3 graphics adj2 accelerat$3 dedicated adj2 graphic adj card) and ((shader shading vertex) adj2 (bank cache memory ram vram))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:01
S28	1122	345/501.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:08
S29	40	S28 and accelerator near5 (storage ram main adj2 memory memory bank cache)and (controller)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:10
S30	18	S28 and accelerator near5 ((storage ram main adj2 memory memory bank cache)and (controller))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/05 18:21
S31	46666	(gpgpu general adj2 purpose adj2 process$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:44
S32	314	(gpgpu general adj2 purpose adj2 process$3) same accelerat$3 with (asic fpga software)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:45

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S33	0	(gpgpu general adj2 purpose adj2 process$3) same accelerat$3 near5 controll$3 with (asic fpga software)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:46
S34	21	(gpgpu general adj2 purpose adj2 process$3) same accelerat$3 with controll$3 with (asic fpga software)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:46
S35	21	(gpgpu general adj2 purpose adj2 process$3) same (accelerat$3 off $1load$3 graphics adj2 accelerat$3 graphic adj card) with controll$3 with (asic fpga software)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:49
S36	61	(gpgpu general adj2 purpose adj2 process$3) same (accelerat$3 off $1load$3 graphics adj2 accelerat$3 graphic adj card) same controll$3 same (asic fpga software)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:49
S37	40	S36 not S35	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 15:49
S38	158981	((general$1purpose general adj2 purpose) adj2 comput$5 gpu gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:10
S39	137	((general$1purpose general adj2 purpose) adj2 gpu gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:12
S40	2	((general$1purpose general adj2 purpose) adj2 gpu gpgpu) and simulat$3 adj2 (data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:13
S41	13	((general$1purpose general adj2 purpose) adj2 gpu gpgpu) and simulat$3 near5 (data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:13
S42	5	((general$1purpose general adj2 purpose) adj2 gpu gpgpu) and simulat$3 near5 (software programdata bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:15

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S43	16	((general$1purpose general adj2 purpose) adj2 gpu gpgpu) and simulat$3 near5 (software program data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:16
S44	3	S43 not S41	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:16
S45	9260	((general$1purpose general adj2 purpose) adj2 (graphic$2 comput $5) gpu gpgpu simulat$3 near3 graphic special adj purpose adj2 unit SPU) and simulat$3 near5 (software program data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:19
S46	66004	((general$1purpose general adj2 purpose) adj2 (graphic$2 comput $5) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU) near5 (software program data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:20
S47	916	((general$1purpose general adj2 purpose) adj2 (graphic$2 comput $5) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU) same simulat$3 near5 (software program data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:21
S48	103	((general$1purpose general adj2 purpose) adj2 (graphic$2) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU) same simulat $3 near5 (software program data bit byte info information)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 16:21
S49	2	("20030184551").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2010/09/06 18:05

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S50	6383	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 card) with (asic fpga software application program) near5 (control $4 manag$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 18:14
S51	99	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 card) with (asic fpga software application program) near5 (control $4 manag$3) same (gpu vpu (visual graphic media multi$1media) adj2 (unit engine process $3) gpgpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 18:15
S52	27	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 card) with (asic fpga software application program) near5 (control $4 manag$3) same (gpu vpu (visual graphic media multi$1media) adj2 (unit engine process $3) gpgpu) same (central adj2 process$3 cpu vpu spu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 18:16
S53	66	(accelerat$3 graphics adj2 accelerat$3 (video graphic expan$4) adj2 card) with (asic fpga software application program) near5 (control $4 manag$3) same ((general$1purpose general adj2 purpose) adj2 (graphic$2) gpu gpgpu simulat$3 near3 graphic adj2 process$3 special adj purpose adj2 unit SPU) same (central adj2 process$3 cpu vpu spu)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2010/09/06 18:23

EAST Search History (Interference)

< This search history is empty>

9/9/2010 7:23:23 AM
C:\ Documents and Settings\ mmcdowell1\ My Documents\ EAST\ Workspaces\ 11860254.wsp

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

7590 04/12/2011

Heather Ames
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Boston, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
04/12/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Notice of Abandonment	Application No.	Applicant(s)
	11/860,254	GORCHETCHNIKOV ET AL.
	Examiner	Art Unit
	MAURICE MCDOWELL, JR	2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *16 September 2010*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

Doc Code: PET.OP
Document Description: Petition for Review by the Office of Petitions

PTO/SB/64 (03-13)
Approved for use through 03/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)

Page 1 of 2

Docket Number (Optional) 104821-0103

First-named inventor: Anatoli Gorchetchnikov

Application No.: 11/860,254 Art Unit: 2628

Filed: 09-24-2007 Examiner: MCDOWELL, JR, MAURICE L

Title: Graphic Processor Based Accelerator System and Method

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300

NOTE: If information or assistance is needed in completing this form, please contact the Office of Petitions at (571) 272-3282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the Office notice or action plus any extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION.

NOTE: A grantable petition requires the following items:

(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee – required for all utility and plant applications filed before June 8, 1995, and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. **Petition fee**

☑ Small entity fee $ 950.00 (37 CFR 1.17(m)). Applicant asserts small entity status. See 37 CFR 1.27.

☐ Micro entity fee $ _____ (37 CFR 1.17(m)). Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ Undiscounted fee $ _____ (37 CFR 1.17(m)).

2. **Reply and/or fee**

A The reply and/or fee to the above-noted Office notice or action in the form of

Amendment and Reply under 37 C.F.R. 1.111 (identify the type of reply):

☐ has been filed previously on _____

☑ is enclosed herewith.

B The issue fee and publication fee (if applicable) of $ _____

☐ has been paid previously on _____

☐ is enclosed herewith.

This collection of information is required by 37 CFR 1.137(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 1 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/64 (03-13)
Approved for use through 03/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)

3. **Terminal disclaimer with disclaimer fee**

- [x] Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.
- [ ] A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of $ _____) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. **STATEMENT:** The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

/Christopher Max Colice/	July 31, 2013
Signature	Date
Christopher Max Colice	65,634
Typed or Printed Name	Registration Number, if applicable
FOLEY & LARDNER LLP	(617) 502-3287
Address	Telephone Number
Customer Number: 48329	
Address	

Enclosures:

- [x] Fee Payment
- [x] Reply
- [ ] Terminal Disclaimer Form
- [ ] Additional sheet(s) containing statements establishing unintentional delay
- [ ] Other: _____

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

- [ ] Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.
- [ ] Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (571) 273-8300.

Date _____ Signature _____

Typed or printed name of person signing certificate _____

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	GORCHETCHNIKOV et al.
Title:	GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD
Appl. No.:	11/860254
Filing Date:	9/24/2007
Examiner:	Maurice L. McDowell, Jr.
Art Unit:	2628
Confirmation Number:	6266

AMENDMENT AND REPLY UNDER 37 CFR 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

This communication is responsive to the Non-Final Office Action dated September 16, 2010, concerning the above-referenced patent application.

Applicant has enclosed with this amendment a Petition to Revive under 37 CFR 1.137 to make this response timely.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this document.

Remarks begin on page 9 of this document.

Please amend the application as follows:

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Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A computer system for performing a numerical simulation over a plurality of computational cycles including at least a first computational cycle and a second computational cycle, the computer system comprising:

a central processing unit;

a main memory, operably coupled to the central processing unit, to store input data to be accessed by the central processing unit in performing the numerical simulation;

a video system, operably coupled to the central processing unit, to drive ~~for driving~~ a video monitor to display an indication of the numerical simulation in response to the ~~central processing unit~~ computer system performing the numerical simulation; [[and]]

an accelerator, operably coupled to the central processing unit, to receive at least a portion of the ~~receiving~~ input data from the central processing unit and ~~providing~~ to provide first output data generated during the first computational cycle to the central processing unit after a conclusion of the first computational cycle, the accelerator comprising:

at least one graphics processing unit to generate second output data, during the second computational cycle, by performing at least one calculation on the first output data; and

an accelerator memory, operably coupled to ~~for~~ the at least one graphic processing unit, the accelerator memory comprising:

a first partition, referenced by a first pointer, to store the first output data during the second computational cycle; and

a second partition, referenced by a second pointer, to store the

second output data generated during the second computational cycle; and

an accelerator controller, operably coupled to the accelerator memory and the central processing unit, to transfer the at least the portion of ~~for moving~~ the input data into the accelerator memory before the first computational cycle, ~~moving~~ to transfer the first output data from the accelerator memory to the main memory during the second computational cycle, to direct the second output data into the second partition during the second computational cycle, and to swap the first pointer and the second pointer at the conclusion of the second computational cycle such that the second output data becomes an input for a third computational cycle of the plurality of computational cycles ~~supervising data exchange between the accelerator memory and at least one graphic processing unit~~.

2. (Canceled).

3. (Currently Amended) [[A]] The computer system as claimed in claim 1, wherein the accelerator controller ~~dictates~~ is configured to dictate an order of execution of instructions to the at least one graphics processing unit.

4. (Canceled).

5. (Currently Amended) [[A]] The computer system as claimed in claim 1, wherein the accelerator controller comprises an interface controller ~~that enables the accelerator~~ to communicate with the central processing unit over a bus of the computer system ~~with the central processing unit~~.

6. (Currently Amended) [[A]] The computer system as claimed in claim 1, wherein the accelerator memory comprises a texture memory bank ~~for storing simulation~~ to store the at least the portion of the input data and the first output data and a shader memory bank ~~for storing~~ to store instructions for performing a set of operations to be performed on the ~~simulation~~ at least the portion of the input data by the at least one graphic processing unit.

7. (Currently Amended) [[A]] The computer system as claimed in claim 6, wherein the texture memory is partitioned into ~~sections in which a first section holds input data patterns~~ the first partition, the second partition, a third partition to store ~~second section holds data textures representing~~ internal variables, a fourth partition to store data ~~a third section holds data~~ textures used as input at a particular computation cycle of the plurality of computational cycles ~~step, and a fourth section holds data textures used to store an output of a computational step on the at least one graphic processing unit~~.

8. (Currently Amended) [[A]] The computer system as claimed in claim 1, wherein the accelerator controller inputs the at least the portion of the input data ~~into at least one graphic processing unit~~ and a series of instructions [[to]] into the at least one graphic processing unit, ~~which~~ wherein the at least one graphics processing unit then ~~successively~~ executes the instructions on the at least the portion of the input data.

9. (Canceled).

10. (Currently Amended) An accelerator system for a computer system performing a numerical simulation, the accelerator system comprising:

at least one graphics processing unit to generate output data by performing at least one computation during a first computational cycle of the numerical simulation;

an accelerator memory, operably coupled to the at least one ~~for the graphic~~ graphics processing unit, to store data used to perform the at least one computation; and

an accelerator controller ~~for moving~~, operably coupled to the accelerator memory and the at least one graphics processing unit, to execute:

(i) a computational stream controlling performance of the at least one computation by the at least one graphics processing unit;

(ii) an output stream controlling transfer of the output data ~~between~~ from the at least one graphics processing unit [[and]] to the accelerator memory during the first computational cycle; and

(iii) an input stream controlling transfer of input data to the accelerator memory for use by the at least one graphics processing unit during a second computational cycle of the numerical simulation.

11. (Currently Amended) ~~A computer~~ The accelerator system as claimed in claim 10, wherein the accelerator controller ~~dictates~~ is configured to dictate an order of execution of instructions to the at least one graphics processing unit.

12. (Currently Amended) ~~A computer~~ The accelerator system as claimed in claim 10, wherein the accelerator controller ~~sends~~ is configured to send instructions to the at least one graphics processing unit, ~~which executes~~ wherein the at least one graphics processing unit is configured to execute the instructions on the input data, and wherein the accelerator controller is configured to transfer the output data from the accelerator memory to a main memory during the execution of the instructions by the at least one graphics processing unit~~, the accelerator controller transfers output data from the accelerator system~~.

13. (Currently Amended) ~~A computer~~ The accelerator system as claimed in claim 10, wherein the accelerator memory comprises a texture memory bank ~~for storing simulation~~ to store the input data and the output data and a shader memory bank ~~for storing~~ to store instructions for processing operations to be performed on the ~~simulation~~ input data by the at least one graphic processing unit.

14. (Currently Amended) ~~A computer~~ The accelerator system as claimed in claim 13, wherein the texture memory is partitioned into ~~sections in which~~ a first ~~section holds~~ partition to store the input data ~~patterns~~, a second ~~section holds data textures representing~~ partition to store internal variables, a third ~~section holds data textures used as~~ partition to store data textures used as input at a particular computation cycle of the numerical simulation [[step]], and a fourth ~~section holds data textures used to store an~~ partition to store the output data ~~of a computational step on the at least one graphic processing unit~~.

15. (Canceled).

16. (Currently Amended) ~~A computer~~ The accelerator system as claimed in claim [[15]] 10, wherein the accelerator controller ~~performs~~ is configured to perform successive ~~iterations~~ computational cycles of the numerical simulation by feeding the output data generated by the at least one graphic processing unit from a previous computational cycle and the input data for a next ~~iteration~~ computational cycle into the at least one graphic processing unit.

17. (Currently Amended) A method for performing a numerical ~~simulations~~ simulation on input data in a computer system including a central processing unit and an accelerator, the method comprising:

~~a central processing unit loading input data into an accelerator system from main memory of the central processing unit;~~

receiving, by an accelerator, first input data from the central processing unit;

transferring, by an accelerator controller, the first ~~transferring the~~ input data into a first partition, referenced by first pointer, of an accelerator memory before a first computational cycle of the numerical simulation ~~to a graphics processing unit with instructions to be performed on the input data~~;

performing, by at least one graphics processing unit during the first computational cycle, at least one calculation on the first portion of the input data as to generate first output data;

~~the accelerator controller, transferring output data generated by the graphic processing unit to the central processing unit as output data;~~

storing, by the accelerator controller, the first output data into a second partition, referenced by a second pointer, of the accelerator memory; and

swapping the first pointer with the second pointer at the end of the first computational cycle, such that the first output data becomes an input for a second computational cycle of the numerical simulation.

18. (Currently Amended) [[A]] The method as claimed in claim 17, further comprising:

sending, by the accelerator controller, ~~sending~~ instructions for performing the at least one calculation to the at least one graphics processing unit~~, which executes the instructions on data; and~~

~~during the execution of the instructions by the at least one graphics processing unit, the accelerator controller transferring output data from the accelerator memory to main memory of the central processing unit~~.

19. (Currently Amended) [[A]] The method as claimed in claim 17, further comprising:

partitioning the accelerator memory ~~of accelerator system a~~ into the first ~~section holding~~ partition ~~to store input data patterns~~, the second partition ~~to store output data of a computational step of the at least one graphic processing unit~~, a ~~second section holding data textures representing~~ third partition to store internal variables, and a ~~third section holding~~ fourth partition to store data ~~textures~~ used as input at a particular computation cycle of the numerical simulation ~~step, and a fourth section holding data textures used to store an output of a computational step on the at least one graphic processing unit~~.

20. (Canceled)

21. (New) The method of claim 17, further comprising:

transferring, by the accelerator controller, the first output data to the main memory during the second computational cycle.

22. (New) The computer system as claimed in claim 1, wherein the accelerator controller comprises a set of instructions stored on a memory.

23. (New) The computer system as claimed in claim 1, wherein the at least the portion of the input data represents an initial condition of the numerical simulation.

24. (New) The accelerator system as claimed in claim 10, wherein the accelerator controller comprises a set of instructions stored in a memory.

REMARKS

In response to the Office Action dated September 16, 2010, in the above-identified application, Applicants respectfully request reconsideration. All of the issues raised in the Office Action have been carefully considered and are addressed in this response. The application as now presented is believed to be in allowable condition.

I. Status of the Claims and Summary of Amendments

Upon entry of this response, claims 1, 3, 5–8, 10–19, and 21–24 will be pending in this application, of which claims 1, 10, and 17 are independent claims.

In this paper, claims 1, 3, 5–8, and 10–19 are amended, claims 2, 4, 9, 15, and 20 are canceled, and claims 21–24 are new.

No new matter is added by the amendments or new claims herein; for example, support for the amendments may be found throughout the specification and drawings, including Figure 2 and paragraphs [0030], [0038] and [0138]–[0144] as originally filed.

II. Brief Summary of the Claimed Subject Matter

The following summary of the claimed subject matter is provided to facilitate an understanding of some of the salient innovative and patentable concepts underlying the claims without limiting the claims.

In general, the independent claims are drawn to systems and methods for performing numerical simulations. In one example, the system includes a main memory operably coupled to a central processing unit (CPU). The system also includes a video system to drive a video monitor.

Additionally, the system includes an accelerator that is operably coupled to the CPU. The accelerator receives input data from the CPU at the beginning of a computational cycle, and provides the CPU with the output data from the numerical simulation at the end of the computational cycle. The accelerator includes at least one graphics processing unit (GPU), which performs the numerical simulation. In particular, the GPU uses output data from a particular

computational cycle as input for the next computational cycle, which results in the generation of more output data.

The accelerator further includes an accelerator memory that is operably coupled to the GPU. The accelerator memory includes a first partition for storing the output data used as the input to particular computational cycle and a second partition for storing the output data generated during that computational cycle. Each partition is referenced by a respective pointer.

The system also includes an accelerator controller that is operably coupled to the accelerator memory and the CPU. The accelerator controller transfers the input data received from the CPU into the accelerator memory before the first computational cycle. The accelerator controller also transfers output data from the nth computational cycle from the accelerator memory to the main memory during the $n+1^{th}$ computational cycle, and stores the output data into the second partition at the end of the $n+1^{th}$ computational cycle. Also, the accelerator controller swaps the first pointer and the second pointer at the conclusion of the $n+1^{th}$ computational cycle such that the output data from the $n+1^{th}$ computational cycle becomes an input for the $n+2^{th}$ computational cycle.

It should be appreciated that the foregoing summary is provided solely for the convenience of the Examiner, and is not intended to characterize the scope of any claim in any way. Accordingly, the Examiner is requested to rely upon the language specifically used in the claims to determine whether each of the claims distinguishes over the prior art of record.

III. Rejections Under 35 U.S.C. § 103

In the Office Action, claims 1, 4, 5, 10, 12, 17, and 18 (including independent claims 1, 10, and 17) were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Publication No. 2007/0052713 (hereafter "Chung") in view of U.S. Patent Publication No. 2005/0166042 (hereafter "Evans"). More specifically, pages 2 and 3 of the Office Action state that it would have been obvious to combine the computer system of Chung with the accelerator of Evans to arrive at the computer system of claim 1. Applicants respectfully traverse these rejections to the extent they are maintained over the claims as amended herein.

A. Independent Claims 1 and 17

Independent claim 1 as amended recites:

1. A computer system for performing a numerical simulation over a plurality of computational cycles including at least a first computational cycle and a second computational cycle, the computer system comprising:

a central processing unit;

a main memory, operably coupled to the central processing unit, to store input data to be accessed by the central processing unit in performing the numerical simulation;

a video system, operably coupled to the central processing unit, to drive a video monitor to display an indication of the numerical simulation in response to the computer system performing the numerical simulation;

an accelerator, operably coupled to the central processing unit, to receive at least a portion of the input data from the central processing unit and to provide first output data to the central processing unit at a conclusion of the first computational cycle, the accelerator comprising:

at least one graphics processing unit to generate second output data, during the second computational cycle, by performing at least one calculation on the first output data; and

an accelerator memory, operably coupled to for the at least one graphic processing unit, the accelerator memory comprising:

a first partition, referenced by a first pointer, to store the at least the portion of the input data and the first output data; and

a second partition, referenced by a second pointer, to store the second output data; and

an accelerator controller, operably coupled to the accelerator memory and the central processing unit, to transfer the at least the portion of the input data into the accelerator memory before the first computational cycle, to transfer the first output data from the accelerator memory to the main memory during the second computational cycle, to direct the second output data into the second partition at the end of the second computational cycle, and to swap the first pointer and the second pointer at the conclusion of the second computational cycle such that the second output data becomes an input for a third computational cycle of the plurality of computational cycles.

Claim 17 recites a method with similar limitations to those recited in claim 1. Applicants respectfully submit that Chung and Evans, alone or in combination, fail to teach or suggest all of the elements recited in claims 1 and 17. More particularly, the cited references fail to teach or suggest at least the "accelerator controller" recited in both of these independent claims.

On page 2, the Office Action concedes that Chung does not teach an accelerator controller. The Office Action then relies on Evans to purportedly provide the accelerator controller that is missing from Chung.

More specifically, on page 3, the Office Action refers to Figures 3, 4, and the paragraphs describing Figures 3 and 4 (paragraphs [0061] and [0064], respectively) of Evans as providing purportedly relevant disclosure in connection with the accelerator controller. The cited paragraphs of Evans read:

> [0061] Step 300 provides unencrypted data on the video card. This data is the data that is typically processed by the video card's GPU and is provided in the video card's memory. Step 302 encrypts the unencrypted data on the video card. This step can be implemented in response to a request to transfer the data to the system's memory. For example, the CPU may send an instruction to move the data from the video card to the system's memory. Alternately, the GPU may determine that it does not need the data any longer and therefore initiates a transfer to the system's memory. The data can be encrypted on the video card using any suitable encryption techniques. Step 304 then sends the encrypted data over a bus between the video card and the system. Exemplary buses can be the PCI bus and the AGP bus. Step 306 provides the encrypted data into system memory.
>
> [0064] Step 400 provides data in the system memory. Such data is typically data that is utilized by the video card for processing. The data can be provided in the system memory as either encrypted or unencrypted data. Step 402 can encrypt the data (if it is unencrypted in the system memory) and can send the data to a bus between the system memory and the video card. This step can be implemented in response to a desire to process the data on the video card. Step 404 receives the encrypted data on the video card. Step 406 then decrypts the encrypted data on the video card and step 408 provides the decrypted data into video memory for processing by the GPU.

The above passage of Evans, like the rest of Evans' disclosure, is completely silent with respect to the salient limitations of Applicants' independent claim 1. More specifically, nowhere in the reference does Evans disclose or suggest an accelerator controller, operably coupled to the accelerator memory and the central processing unit, to transfer the at least the portion of the input data into the accelerator memory before the first computational cycle, to transfer the first output

data from the accelerator memory to the main memory during the second computational cycle, to direct the second output data into the second partition at the end of the second computational cycle, and to swap the first pointer and the second pointer at the conclusion of the second computational cycle such that the second output data becomes an input for a third computational cycle of the plurality of computational cycles as recited in independent clam 1. Similarly,

Instead, at best the disclosure of Evans suggests an element that simply moves data into and out of a video card. There is no disclosure whatsoever in Evans of an accelerator controller that swaps respective pointers referencing a portion of the input data and the output data at the end of a first computational cycle as recited in claim 1. Therefore, no combination of Chung and Evans yields an accelerator controller as recited in claim 1 as amended.

Like claim 1 as amended, independent claim 17 as amended recites an accelerator controller that transfers "the first input data into a first partition, referenced by first pointer, of an accelerator memory before a first computational cycle of the numerical simulation" and that loads first output data generated during the first computational cycle "into a second partition, referenced by a second pointer, of the accelerator memory." And Claim 17 as amended also recites "swapping the first pointer with the second pointer at the end of the first computational cycle, such that the first output data becomes an input for a second computational cycle of the numerical simulation." Thus, like the subject matter of claim 1 as amended, the subject matter of claim 17 as amended is patentably distinct from Chung and Evans.

Given these distinctions, claims 1 and 17 as now presented are patentable over Chung and Evans. Claims 4 and 5 depend from claim 1 and claim 18 depends from claim 17, and thus are patentable for at least the same reasons. Accordingly, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a) of these claims.

B. <u>Claim 10</u>

Independent claim 10 as amended recites:

> 10. (Currently Amended) An accelerator system for a computer system performing a numerical simulation, the accelerator system comprising:

at least one graphics processing unit to generate output data by performing at least one computation during a first computation cycle of the numerical simulation;

an accelerator memory, operably coupled to the at least one graphics processing unit, to store data used to perform the at least one computation; and

an accelerator controller, operably coupled to the accelerator memory and the at least one graphics processing unit, to execute:

(i) a computational stream controlling performance of the first computation by the at least one graphics processing unit;

(ii) an output stream controlling transfer of the output data from the at least one graphics processing unit to the accelerator memory at the end of the first computation cycle; and

(iii) an input stream controlling transfer of input data to the accelerator memory for use by the at least one graphics processing unit during a second computation cycle of the numerical simulation.

Applicants respectfully submit that Chung and Evans, alone or in combination, fail to disclose or suggest all of the elements recited in claim 10. More specifically, nowhere does Chung or Evans disclose or suggest an accelerator controller that executes a computational stream to control performance of a first computation, an output stream to transfer data at the end of the first computational cycle, and an input stream to control the transfer of input data into the accelerator memory. Therefore, no combination of Chung and Evans yields an accelerator system that includes the accelerator controller of claim 10 as amended.

Accordingly, claim 10 is patentable over Chung and Evans for at least the reasons set forth above. Claim 12 depends on Claim 10 and thus is patentable for at least the same reasons. Accordingly, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a) of these claims.

C. Claims 3, 6–9, 11, 13–16, 19, and 20

In the Office Action, dependent claims 3, 6–9, 11, 13–16, 19, and 20 were rejected under 35 U.S.C. § 103(a) as allegedly obvious over Chung in view of Evans in further view of U.S. Patent No. 5,388,206 (hereafter "Poulton"). Applicants respectfully traverse these rejections. In any event, as each of the above-identified claims depends from independent claims 1, 10 or 17,

each of which are in patentable condition, the rejections of these dependent claims respectfully are believed to be moot.

IV. General Comments on Dependent Claims

Since each of the dependent claims depends from a base claim that is believed to be in condition for allowance, Applicants believe that it is unnecessary at this time to argue the allowability of each of the dependent claims individually. However, Applicants do not necessarily concur with the interpretation of the dependent claims as set forth in the Office Action, nor do the Applicants concur that the basis for the rejection of any of the dependent claims is proper. Therefore, Applicants reserve the right to specifically address the patentability of the dependent claims in the future.

CONCLUSION

It is respectfully believed that all of the rejections set forth in the Office Action have been addressed. However, the absence of a reply to a specific rejection, objection, or comment set forth in the Office Action does not signify agreement with or concession of that rejection, objection, or comment. In addition, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Furthermore, nothing in this paper should be construed as an intent to concede any issue with regard to any claim.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16–1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to

Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. § 1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date July 31, 2013

By /Christopher Max Colice/

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Attorney for Applicant
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4841-4508-3668.4

Electronic Patent Application Fee Transmittal

Application Number:	11860254
Filing Date:	24-Sep-2007
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Christopher M. Colice/Jennifer Robins
Attorney Docket Number:	0167.0001US1

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Petition-Revive Unintent. Abandoned Appl	2453	1	950	950
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**950**

Electronic Acknowledgement Receipt	
EFS ID:	16465474
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Correspondence Address:	Heather Ames - Apt 2 252 East 8th St. Boston MA 02127 US 5102058091 ames@neurala.com
Filer:	Christopher M. Colice/Jennifer Robins
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	0167.0001US1
Receipt Date:	31-JUL-2013
Filing Date:	24-SEP-2007
Time Stamp:	14:37:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$950

RAM confirmation Number	1076
Deposit Account	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions.	104821-0103petitionRevive.pdf	153257 e61a085b31d83f921c1b42b0c547c0fd6b50ecb4	no	3
Warnings:					
Information:					
2		104821-0103amendment.pdf	199038 e5ed469de81f0895b162c1904fe2c2e183acd47a	yes	16

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	8
Applicant Arguments/Remarks Made in an Amendment	9	16

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30098 1e0ea4213f5bc0039e40c2ead7adba60036c5abd	no	2
Warnings:					
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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
11/860,254	09/24/2007	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 07/31/2013

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or independent) is the highest number found in the appropriate box in column 1.

SLIE
/SHARONE MOORE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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MAILED
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OFFICE OF PETITIONS

In re Application of
GORCHETCHNIKOV et al.
Application No. 11/860,254
Filed: September 24, 2007
Attorney Docket No. 0167.0001US1

DECISION ON PETITION

This is a decision on the petition under the unintentional provisions of 37 CFR 1.137(b), filed July 31, 2013, to revive the above-identified application.

The petition is **GRANTED**.

This above-identified application became abandoned for failure to timely file a reply to the non-final Office Action of September 16, 2010. The non-final Office Action set a three (3) month shortened statutory period for reply. No extension of time was obtained under the provisions of 37 CFR §1.136(a). Accordingly, this application became abandoned on December 17, 2010. A Notice of Abandonment was mailed on April 12, 2011.

The petition satisfies the requirements of 37 CFR 1.137(b) in that petitioner has supplied (1) the reply in the form of an amendment (2) the petition fee of $950.00, and (3) a statement of unintentional delay.

It is not apparent whether the person signing the statement of unintentional delay was in a position to have firsthand or direct knowledge of the facts and circumstances of the delay at issue. Nevertheless, such statement is being treated as having been made as the result of a reasonable inquiry into the facts and circumstances of such delay. See 37 CFR §10.18(b). In the event that such an inquiry has not been made, Petitioner must make such an inquiry. If such inquiry results in the discovery that it is not correct that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition pursuant to 37 CFR §1.137(b) was unintentional, petitioner must notify the Office.

The address given on the petition differs from the address of record. If appropriate, a change of address should be filed in accordance with MPEP 601.03. A courtesy copy of this decision is being mailed to the address given on the petition; however, the Office will mail all future correspondence solely to the address of record.

There is no indication that the petition is signed by a registered patent attorney or patent agent of record. However, in accordance with 37 CFR 1.34, the signature of Mr. Colice appearing on the

correspondence shall constitute a representation to the United States Patent and Trademark Office that he is authorized to represent the particular party in whose behalf he acts.

This application is being referred to Technology Center AU 2628 for appropriate action by the Examiner in the normal course of business on the reply received.

Telephone inquiries concerning this decision should be directed to the undersigned at (571) 272-3215.

/Charlema Grant/
Charlema Grant
Attorney Advisor
Office of Petitions

Cc: FOLEY & LARDNER LLP
3000 K STREET N.W.
SUITE 600
WASHINGTON, DC 20007-5109

Neural AI, LLC, Exhibit 2045
Page 2045 - 181
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

PLUS Search Results for S/N 11860254, Searched Thu Sep 26 12:07:16 EDT 2013

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 10/07/2013

HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/07/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

TITLE OF INVENTION: Graphic Processor Based Accelerator System and Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$890	$300	$0	$1190	01/07/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 10/07/2013
HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

TITLE OF INVENTION: Graphic Processor Based Accelerator System and Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$890	$300	$0	$1190	01/07/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCDOWELL, JR, MAURICE L	2612	345-501000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

7590 10/07/2013

HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/07/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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IPR2025-00606

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 11/860,254	Applicant(s) GORCHETCHNIKOV ET AL.	
	Examiner MAURICE L. MCDOWELL, JR	Art Unit 2612	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/31/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,3,5-8,10-14,16-19 and 21-24*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MAURICE L. MCDOWELL, JR/
Primary Examiner, Art Unit 2612

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IPR2025-00606

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 1, 3, 5-8, 10-14, 16-19, 21-24 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner agrees with the applicant that the prior art doesn't teach: "*an accelerator controller, operably coupled to the accelerator memory and the central processing unit, to transfer the at least the portion of the input data into the accelerator memory before the first computational cycle, to transfer the first output data from the accelerator memory to the main memory during the second computational cycle, to direct the second output data into the second partition during the second computational cycle, and to swap the first pointer and the second pointer at the conclusion of the second computational cycle such that the second output data becomes an input for a third computational cycle of the plurality of computational cycles*" as argued on pgs. 12-13 of remarks filed on 7/31/13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAURICE L. MCDOWELL, JR whose telephone number is

(571)270-3707. The examiner can normally be reached on Mon-Friday 7:30am - 5:00pm Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ke Xiao can be reached on 571--272-7776. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MAURICE L. MCDOWELL, JR/
Primary Examiner, Art Unit 2612

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1823	345/501.OCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 07:21
L2	559	345/503.OCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 07:21
L3	2297	(L1 L2)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 07:21
L4	30777	ACCELERATOR AND (SCHEDUL$3 CONTROL$3)	EPO; JPO; DERWENT	OR	ON	2013/10/02 08:11
L5	1	ACCELERATOR AND (SCHEDUL$3 CONTROL$3) AND NUMERICAL ADJ2 SIMULATION	EPO; JPO; DERWENT	OR	ON	2013/10/02 08:11
L6	1	ACCELERATOR AND NUMERICAL ADJ2 SIMULATION	EPO; JPO; DERWENT	OR	ON	2013/10/02 08:12
L7	14	ACCELERAT$3 AND NUMERICAL ADJ2 SIMULATION	EPO; JPO; DERWENT	OR	ON	2013/10/02 08:12
L8	489	L3 AND GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:19
L9	1	L3 AND GPU AND NUMERICAL ADJ SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:19
L10	3	L3 AND NUMERICAL ADJ SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:20
L11	4	L3 AND NUMERICAL ADJ2 SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:20
L12	4	L3 AND NUMERICAL NEAR2 SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:22

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L22	1138	(COMPUTER ADJ SYSTEM ACCELERATOR ADJ SYSTEM METHOD ADJ2 PERFORMING ADJ2 NUMERICAL ADJ SIMULATION) AND ACCELERAT$3 WITH GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:31
L23	0	(COMPUTER ADJ SYSTEM ACCELERATOR ADJ SYSTEM METHOD ADJ2 PERFORMING ADJ2 NUMERICAL ADJ SIMULATION) AND ACCELERAT$3 WITH GPU SAME NUMERICAL NEAR3 SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:31
L24	7	(COMPUTER ADJ SYSTEM ACCELERATOR ADJ SYSTEM METHOD ADJ2 PERFORMING ADJ2 NUMERICAL ADJ SIMULATION) AND ACCELERAT$3 WITH GPU AND NUMERICAL NEAR3 SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 08:31
S1	50	(US-20070011439-$ or US-20070296613-$ or US-20070297501-$ or US-20080117220-$ or US-20090055596-$ or US-20090064095-$ or US-20090070553-$ or US-20090160863-$ or US-20090177843-$ or US-20100088490-$ or US-20100115233-$ or US-20100115237-$ or US-20100225656-$ or US-20100231600-$ or US-20110022817-$ or US-20110173155-$ or US-20110238957-$ or US-20110307647-$ or US-20120092353-$ or US-20120317556-$ or US-20130021350-$ or US-20130117750-$ or US-20130160016-$ or US-20100037024-$ or US-20100135383-$ or US-20110102443-$).did. or (US-20110161619-$ or US-20110161620-$ or US-20120079177-$ or US-20120079298-$ or US-20130132684-$ or US-20130156101-$ or US-20130187933-$ or US-20130232495-$).did. or (US-7623049-$ or US-7626518-$ or US-7626521-$ or US-7656326-$ or US-8122229-$ or US-8156307-$ or US-8180998-$ or US-8205066-$ or US-8225074-$ or US-8327175-$ or US-8375392-$ or US-8533698-$ or US-8095735-$ or US-8320448-$ or US-8345052-$ or US-8443147-$).did.	US-PGPUB; USPAT	OR	ON	2013/09/26 13:55
S2	48	S1 AND ACCELERATOR WITH GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 13:59
S3	12	S1 AND ACCELERATOR WITH GPU WITH CPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:00
S4	12	S1 AND ACCELERATOR WITH GPU WITH CPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:00

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S5	1	GORCHETCHNIKOV-ANATOLI$.IN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:05
S6	1	AMES-HEATHER$.IN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:06
S7	1	VERSACE-MASSIMILIANO$.IN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:06
S8	2	SANTINI-FABRIZIO$.IN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:06
S9	2	(S5 S6 S7 S8)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:06
S10	0	S9 AND (computer system performing numerical simulation plurality computational cycles first computational cycle second computational cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:09
S11	0	S9 AND (video system operably coupled central processing unit drive video monitor display indication numerical simulation responsecomputer system numerical simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:10
S12	0	S9 AND (video system operably coupled central processing unit drive video monitor display indication numerical simulation response system numerical simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:11
S13	0	S9 AND (accelerator operably coupled central processing unit receive least portion receiving input data central processing unit first output data generated first computational cycle central processing unit conclusion first computational cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:12
S14	0	S9 AND (one graphics processing unit generate second output data second computational cycle performing least one calculation first output data)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:13
S15	0	S9 AND (first partition referenced first pointer store first output data second computational cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:19
S16	0	S9 AND (second partition referenced second pointer store second output data generated during second computational	US-PGPUB; USPAT;	WITH	ON	2013/09/26 14:20

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		cycle)	EPO; JPO; DERWENT			
S17	0	S9 AND (accelerator controller operably coupled accelerator memory central processing unit transfer least portion input data accelerator memory first computational cycle moving transfer first output data accelerator memory main memory)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:32
S18	0	S9 AND (during second computational cycle direct second output data second partition during second computational cycle swap first pointer second pointer conclusion second computational cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:34
S19	0	S9 AND (second output data input third computational cycle plurality computational cycles supervising data exchange accelerator memory least one graphic processing unit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:35
S20	1	S9 AND (accelerator controller dictate order execution instructions least one graphics processing unit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:37
S21	1	S9 AND (accelerator controller interface controller communicate central processing unit bus computer system)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:38
S22	0	S9 AND (accelerator memory texture memory bank simulation store portion input data first output data shader memory bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:40
S23	0	S9 AND (accelerator memory texture memory bank simulation portion input data first output data shader memory bank)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:40
S24	0	S9 AND (textures input particular computation cycle plurality computational cycles step fourth section holds data textures store)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:41
S25	0	S9 AND (accelerator memory texture memory bank store input data output data shader memory bank store instructions processing operations performed simulation input data least one graphic processing unit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:44
S26	0	S9 AND (swapping first pointer second pointer end first computational cycle first output data input second computational cycle numerical simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT	WITH	ON	2013/09/26 14:45
S27	1	(S20 S21)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 14:46

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S28	278	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) WITH ACCELERATOR	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:26
S29	7	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) WITH ACCELERATOR WITH (RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:26
S30	70	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) WITH (GRAPHICS GPU) WITH (RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:36
S31	13	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) WITH (GRAPHICS GPU) WITH (RAM MEMORY VRAM) AND ACCELERAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:37
S32	13	S31 NOT S29	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:37
S33	81	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME (GRAPHICS GPU) SAME (RAM MEMORY VRAM) AND ACCELERAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:43
S34	10	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME (GRAPHICS GPU) SAME (RAM MEMORY VRAM) AND ACCELERAT$3 NEAR2 (CONTROLLER INSTRUCTION APPLICATION SOFTWARE)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:44
S35	10	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME (GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM) AND ACCELERAT$3 NEAR2 (CONTROLLER INSTRUCTION APPLICATION SOFTWARE)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:49

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S36	28	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME (GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM) AND ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:49
S37	18	S36 NOT S35	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/26 15:49
S38	269	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) AND (GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/27 07:39
S39	9	(NUMERICAL ADJ2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR APPLICATION NEURAL ADJ NETWORKS GENETIC ADJ ALGORITHMS PARTICLE ADJ SYSTEMS MECHANICAL ADJ SYSTEMS) SAME ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) SAME (BANK CACHE MEMORY STORAGE) AND (GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/27 07:40
S40	889	(NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) SAME (BANK CACHE MEMORY STORAGE) AND (GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/27 07:43
S41	693	(NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) SAME (BANK CACHE MEMORY STORAGE) SAME(GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/27 07:43
S42	3	(NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2013/09/27 07:44

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		NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) SAME (BANK CACHE MEMORY STORAGE) SAME(GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM) SAME (STREAM THREAD)	DERWENT			
S43	3	(FINITE ADJ ELEMENT ADJ ANALYSIS NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND ACCELERAT$3 WITH (CONTROLLER INSTRUCTION APPLICATION SOFTWARE) SAME (BANK CACHE MEMORY STORAGE) SAME(GRAPHICS GPU) SAME (STORAGE RAM MEMORY VRAM) SAME (STREAM THREAD)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 11:53
S44	1410	(COMPUTATION$2 EXECUTION) ADJ STREAM	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:27
S45	2	(COMPUTATION$2 EXECUTION) ADJ STREAM AND ACCELERAT$3 NEAR2 CONTROL$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:27
S46	26	(COMPUTATION$2 EXECUTION) ADJ2 STREAM AND ACCELERAT$3 NEAR2 CONTROL$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:28
S47	0	(COMPUTATION$2 EXECUTION) ADJ2 STREAM SAME ACCELERAT$3 SAME EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:39
S48	20	(COMPUTATION$2 EXECUTION) ADJ2 STREAM AND ACCELERAT$3 SAME EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:39
S49	19	S48 NOT S46	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:39
S50	277	(COMPUTATION$2 EXECUTION) ADJ2 STREAM AND ACCELERAT$3 AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:40
S51	1	(COMPUTATION$2 EXECUTION) ADJ2 STREAM AND ACCELERAT$3 SAME (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:41

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		GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER				
S52	53	(COMPUTATION$2 EXECUTION) ADJ2 STREAM AND ACCELERAT$3 AND (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:42
S53	52	S52 NOT S46	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 12:42
S54	73	(COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) AND ACCELERAT$3 AND (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:23
S55	0	(INPUT AND OUTPUT) NEAR5 (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) AND ACCELERAT$3 AND (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:24
S56	1	(INPUT AND OUTPUT) WITH (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) AND ACCELERAT$3 AND (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:24
S57	2	(INPUT AND OUTPUT) SAME (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) AND ACCELERAT$3 AND (NUMERICAL NEAR2 SIMULAT$3 (NON-GRAPHICS NON-VIDEO) NEAR2 APPLICATION NEURAL NEAR2 NETWORKS GENETIC NEAR2 ALGORITHMS PARTICLE NEAR2 SYSTEMS MECHANICAL NEAR2 SYSTEMS) AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:24
S58	10	(INPUT AND OUTPUT) WITH (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) AND ACCELERAT$3 SAME GPU AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:26

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S59	0	(INPUT AND OUTPUT) WITH (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) WITH PERFORMANCE AND ACCELERAT$3 SAME GPU AND EXECUTION NEAR2 ORDER	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:33
S60	0	(INPUT AND OUTPUT) WITH (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) WITH PERFORMANCE AND ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:33
S61	0	TRANSFER NEAR3 CONTROL$4 AND (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) WITH PERFORMANCE AND ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:34
S62	0	TRANSFER NEAR3 CONTROL$4 AND (COMPUTATION$2 EXECUTION) ADJ2 (thread STREAM) SAME PERFORMANCE AND ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:34
S63	1	TRANSFER NEAR3 CONTROL$4 AND (COMPUTATION$2 EXECUTION) NEAR3 (thread STREAM) SAME PERFORMANCE AND ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:34
S64	4	TRANSFER NEAR3 CONTROL$4 AND (COMPUTATION$2 EXECUTION) NEAR3 (thread STREAM) SAME ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:35
S65	6	TRANSFER NEAR3 (SCHEDUL$3 CONTROL$4) AND (COMPUTATION$2 EXECUTION) NEAR3 (thread STREAM) SAME ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:35
S66	2	S65 NOT S64	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:35
S67	10	TRANSFER NEAR3 (SCHEDUL$3 CONTROL$4 MANAG$3) AND (COMPUTATION$2 EXECUTION) NEAR3 (thread STREAM) SAME ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:36
S68	4	S67 NOT S65	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:36
S69	11	TRANSFER NEAR3 (SCHEDUL$3 CONTROL$4 MANAG$3) AND (COMPUTATION$2 EXECUTION) WITH (thread STREAM) SAME ACCELERAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:37
S70	1	S69 NOT S67	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:37

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S71	7886	NUMERICAL NEAR SIMULAT$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:42
S72	2	NUMERICAL NEAR SIMULAT$3 WITH GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:42
S73	6	NUMERICAL NEAR SIMULAT$3 SAME GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:42
S74	20	NUMERICAL NEAR SIMULAT$3 SAME2 GPU	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:46
S75	14	S74 NOT S73	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:47
S76	212	(FIRST AND SECOND) ADJ2 (COMPUTATION$2 EXECUT$3) ADJ2 CYCLE	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:49
S77	0	(FIRST AND SECOND) ADJ2 (COMPUTATION$2 EXECUT$3) ADJ2 CYCLE AND ACCELERAT$2 NEAR2 (RAM VRAM MEMORY CACHE)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/01 13:50
S78	5	(FIRST AND SECOND) NEAR5 (COMPUTATION$2 EXECUT$3) ADJ2 CYCLE AND ACCELERAT$2 NEAR2 (RAM VRAM MEMORY CACHE)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 06:26
S79	1823	345/501.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 06:30
S80	559	345/503.CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/10/02 06:30

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L13	0	345/501.CCLS. AND (computer system performing numerical simulation plurality computational cycles first computational cycle second computational cycle).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:23

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L14	0	345/501.CCLS. AND (video system operably coupled central processing unit drive video monitor display indication numerical simulation responsecomputer system numerical simulation).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:23
L15	0	345/501.CCLS. AND (video system operably coupled central processing unit drive video monitor display indication numerical simulation response system numerical simulation).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:24
L16	0	345/501.CCLS. AND (accelerator controller dictate order execution instructions least one graphics processing unit).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:24
L17	1	(accelerator controller dictate order execution instructions least one graphics processing unit).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:24
L18	1	(accelerator controller interface controller communicate central processing unit bus computer system).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:27
L19	0	(accelerator memory texture memory bank simulation store portion input data first output data shader memory bank).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:27
L20	0	(swapping first pointer second pointer end first computational cycle first output data input second computational cycle numerical simulation).CLM.	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:27
L21	1	(L17 OR L18)	US-PGPUB; USPAT; UPAD	WITH	ON	2013/10/02 08:28

10/2/2013 8:47:29 AM
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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/860,254	09/24/2007 RULE	345	2677	0167.0001US1

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Fabrizio Santini, Jamaica Plain, MA;

**** CONTINUING DATA ****************************

This appln claims benefit of 60/826,892 09/25/2006

**** FOREIGN APPLICATIONS ****************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
10/04/2007

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MAURICE L MCDOWELL, JR/ Examiner's Signature	☐ Met after Allowance MM Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	5	20	3

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TITLE

Graphic Processor Based Accelerator System and Method

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500	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	**Art Unit**
	MAURICE L MCDOWELL, JR	2612

CPC

Symbol	Type	Version

CPC Combination Sets

Symbol	Type	Set	Ranking	Version

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/MAURICE L MCDOWELL, JR/ Primary Examiner.Art Unit 2612 (Primary Examiner)	10/02/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

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Part of Paper No.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	**Art Unit**
	MAURICE L MCDOWELL, JR	2612

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
345	501	G 0 6 F 15 / 00 (2006.01 01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
345	503				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/MAURICE L MCDOWELL, JR/ Primary Examiner.Art Unit 2612	10/02/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U S. Patent and Trademark Office

Part of Paper No.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	**Art Unit**
	MAURICE L MCDOWELL, JR	2612

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
	2	17	18												
2	3	18	19												
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10	11														
11	12														
12	13														
13	14														
	15														
14	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/MAURICE L MCDOWELL, JR/ Primary Examiner.Art Unit 2612 (Primary Examiner)	10/02/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

U.S. Patent and Trademark Office Part of Paper No.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11860254	GORCHETCHNIKOV ET AL.
	Examiner	**Art Unit**
	MAURICE MCDOWELL, JR	2612

CPC- SEARCHED		
Symbol	**Date**	**Examiner**

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
345	501, 503	10/2/13	MM

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
East text search	9/9/10	MM
Inventor name search	9/9/10	MM
Foreign database search	9/9/10	MM
NPL search on ACM and IEEE databases	9/9/10	MM
Class/subclass combined with text search	9/9/10	MM
East text search	10/2/13	MM
Inventor name search	10/2/13	MM
Class/subclass combined with text search	10/2/13	MM
PLUS text search	10/2/13	MM
NPL search on ACM and IEEE and Google Scholar	10/2/13	MM
Foreign database search	10/2/13	MM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
345	501	10/2/13	MM

	/MAURICE L MCDOWELL, JR/ Primary Examiner.Art Unit 2612

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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

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OPAP AKIMA-19 OCT 25 2013 PATENT & TRADEMARK OFFICE

MAILED AUG 26 2013 OFFICE OF PETITIONS

Heather Ames
Apt 2
252 East 8th St.
Boston MA 02127

In re Application of :
GORCHETCHNIKOV et al. :
Application No. 11/860,254 : DECISION ON PETITION
Filed: September 24, 2007 :
Attorney Docket No. 0167.0001US1 :

This is a decision on the petition under the unintentional provisions of 37 CFR 1.137(b), filed July 31, 2013, to revive the above-identified application.

The petition is **GRANTED**.

This above-identified application became abandoned for failure to timely file a reply to the non-final Office Action of September 16, 2010. The non-final Office Action set a three (3) month shortened statutory period for reply. No extension of time was obtained under the provisions of 37 CFR §1.136(a). Accordingly, this application became abandoned on December 17, 2010. A Notice of Abandonment was mailed on April 12, 2011.

The petition satisfies the requirements of 37 CFR 1.137(b) in that petitioner has supplied (1) the reply in the form of an amendment (2) the petition fee of $950.00, and (3) a statement of unintentional delay.

It is not apparent whether the person signing the statement of unintentional delay was in a position to have firsthand or direct knowledge of the facts and circumstances of the delay at issue. Nevertheless, such statement is being treated as having been made as the result of a reasonable inquiry into the facts and circumstances of such delay. See 37 CFR §10.18(b). In the event that such an inquiry has not been made, Petitioner must make such an inquiry. If such inquiry results in the discovery that it is not correct that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition pursuant to 37 CFR §1.137(b) was unintentional, petitioner must notify the Office.

The address given on the petition differs from the address of record. If appropriate, a change of address should be filed in accordance with MPEP 601.03. A courtesy copy of this decision is being mailed to the address given on the petition; however, the Office will mail all future correspondence solely to the address of record.

There is no indication that the petition is signed by a registered patent attorney or patent agent of record. However, in accordance with 37 CFR 1.34, the signature of Mr. Colice appearing on the

correspondence shall constitute a representation to the United States Patent and Trademark Office that he is authorized to represent the particular party in whose behalf he acts.

This application is being referred to Technology Center AU 2628 for appropriate action by the Examiner in the normal course of business on the reply received.

Telephone inquiries concerning this decision should be directed to the undersigned at (571) 272-3215.

/Charlema Grant/
Charlema Grant
Attorney Advisor
Office of Petitions

Cc: FOLEY & LARDNER LLP
3000 K STREET N.W.
SUITE 600
WASHINGTON, DC 20007-5109

Organization TC 2600 Bldg./Room KNOX
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NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

7590 10/07/2013
HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/07/2013

OPAP AKIMA-18
NOV 1 2 2013
PATENT & TRADEMARK OFFICE

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Neural AI, LLC, Exhibit 2045
Page 2045 - 212
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 10/07/2013
HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

EXAMINER
MCDOWELL, JR, MAURICE L

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/07/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

TITLE OF INVENTION: Graphic Processor Based Accelerator System and Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$890	$300	$0	$1190	01/07/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Neural AI, LLC, Exhibit 2045
Page 2045 - 213
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

TITLE OF INVENTION: Graphic Processor Based Accelerator System and Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$890	$300	$0	$1190	01/07/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCDOWELL, JR, MAURICE L	2612	345-501000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Neural AI, LLC, Exhibit 2045
Page 2045 - 215
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notices of Allowance and Fee(s) Due mailed between October 1, 2013 and December 31, 2013

(Addendum to PTOL-85)

If the "Notice of Allowance and Fee(s) Due" has a mailing date on or after October 1, 2013 and before January 1, 2014, the following information is applicable to this application.

If the issue fee is being timely paid on or after January 1, 2014, the amount due is the issue fee and publication fee in effect January 1, 2014. On January 1, 2014, the issue fees set forth in 37 CFR 1.18 decrease significantly and the publication fee set forth in 37 CFR 1.18(d)(1) decreases to $0.

If an issue fee or publication fee has been previously paid in this application, applicant is not entitled to a refund of the difference between the amount paid and the amount in effect on January 1, 2014.

Notice of Allowability	Application No. 11/860,254	Applicant(s) GORCHETCHNIKOV ET AL.	
	Examiner MAURICE L. MCDOWELL, JR	Art Unit 2612	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/31/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1,3,5-8,10-14,16-19 and 21-24*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____.
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/MAURICE L. MCDOWELL, JR/
Primary Examiner, Art Unit 2612

Neural AI, LLC, Exhibit 2045
Page 2045 - 218
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 1, 3, 5-8, 10-14, 16-19, 21-24 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner agrees with the applicant that the prior art doesn't teach: "*an accelerator controller, operably coupled to the accelerator memory and the central processing unit, to transfer the at least the portion of the input data into the accelerator memory before the first computational cycle, to transfer the first output data from the accelerator memory to the main memory during the second computational cycle, to direct the second output data into the second partition during the second computational cycle, and to swap the first pointer and the second pointer at the conclusion of the second computational cycle such that the second output data becomes an input for a third computational cycle of the plurality of computational cycles*" as argued on pgs. 12-13 of remarks filed on 7/31/13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAURICE L. MCDOWELL, JR whose telephone number is

(571)270-3707. The examiner can normally be reached on Mon-Friday 7:30am - 5:00pm Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ke Xiao can be reached on 571--272-7776. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MAURICE L. MCDOWELL, JR/
Primary Examiner, Art Unit 2612

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Track One Prioritized Examination

trackone

Final disposition objective is within 12 months

- Faster time to first action, which is currently less than 5 months
- Request must be filed via EFS web and fee required at the time of filing
- No additional examination-related support documents
- Application limited to no more than 30 total claims (4 independent claims maximum)
- Prioritization fee: $4000 ($2000 small, $1000 micro)

http://www.uspto.gov/patents/init_events/Track_One.jsp

Accelerated Examination

ACCELERATED EXAMINATION

12

Final disposition objective is within 12 months

- Faster time to first action, which is currently less than 5 months
- Petition, petition fee, preexamination search, and an "Examination Support Document" required at the time of filing
- Promotes personal interviews prior to issuance of first Office action
- Application limited to 20 claims (3 independent claims maximum)

http://www.uspto.gov/patents/process/file/accelerated/index.jsp

Patent Prosecution Highway

PPH

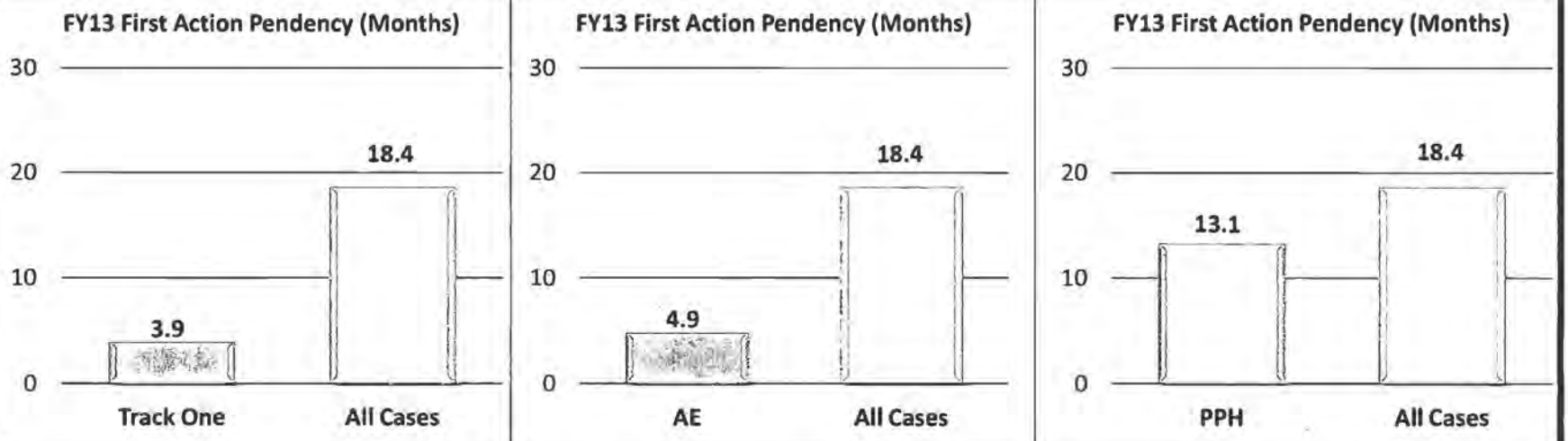
Provides accelerated prosecution following favorable results from a participating foreign office

- Entry based upon at least one allowable claim in counterpart foreign application
- First Office action within 2-3 months of petition grant
- Request must be submitted prior to a first action
- No limit on the number of claims

http://www.uspto.gov/patents/init_events/pph/index.jsp

NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

Track One Prioritized Examination	Accelerated Examination	Patent Prosecution Highway
$4000 fee $2000 small entity fee, $1000 micro entity fee	$140 petition fee $70 small entity fee, $35 micro entity fee	No additional fee
Limited to four independent claims and no more than 30 total claims	Limited to three independent claims and no more than 20 total claims (no multiple dependent claims)	No claim limit (Normal excess claim fees apply)
No examination support documents required	Requires preexamination search documents and an examination support document	Entry based upon at least one allowable claim in counterpart foreign application
Follows normal interview practice	Examiner interview required before issuing an Office Action	Follows normal interview practice
Continuations and RCEs are eligible for the program	Continuations are eligible for the program	Continuations are eligible for the program (before first action is issued)
Number of applications admitted to the program limited to 10,000 per fiscal year	No limit on number of applications admitted to the program per year	No limit on number of applications admitted to the program per year



For full program details and definition, see websites listed on the reverse side. Pendency data as of: September 2013

NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 10/07/2013
HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1	6266

TITLE OF INVENTION: Graphic Processor Based Accelerator System and Method

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	~~$890~~ $480	~~$300~~ $0	$0	$1190	01/07/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
MCDOWELL, JR, MAURICE L	2612	345-501000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 ____
2 ____
3 ____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Neurala LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Boston MA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies ____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 501283 (enclose an extra copy of this form).

PTOL-85 (Rev. 02/11)

Neural AI, LLC, Exhibit 2045
Page 2045 - 223
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Christopher Max Colice/ Date January 3, 2014

Typed or printed name Christopher Max Colice Registration No 65,634

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	11860254
Filing Date:	24-Sep-2007
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Filer:	Christopher M. Colice/Sylvana Householder
Attorney Docket Number:	0167.0001US1

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt	
EFS ID:	17811158
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Correspondence Address:	HEATHER AMES - APT 2 252 EAST 8TH ST. BOSTON MA 02127 US 5102058091 ames@neurala.com
Filer:	Christopher M. Colice/Sylvana Householder
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	0167.0001US1
Receipt Date:	03-JAN-2014
Filing Date:	24-SEP-2007
Time Stamp:	13:13:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$480

RAM confirmation Number	12443
Deposit Account	501283
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

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1	Issue Fee Payment (PTO-85B)	NRLA-001_Issue_Fee_Transmittal.pdf	1993876 e5232bcee03bd6f9091ee6223e4610484edb0d3f	no	2
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2	Fee Worksheet (SB06)	fee-info.pdf	29756 6f4f0fec1750ce1c6c8d185a11313f40e634315bd	no	2
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	02/11/2014	8648867	0167.0001US1	6266

7590 01/22/2014

HEATHER AMES
APT 2
252 EAST 8TH ST.
BOSTON, MA 02127

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1030 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Anatoli Gorchetchnikov, Belmont, MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

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IR103 (Rev. 10/09)

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/860,254	02/11/2014	8648867	0167.0001US1	6266

7590 01/22/2014

HEATHER AMES
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252 EAST 8TH ST.
BOSTON, MA 02127

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APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Anatoli Gorchetchnikov, Belmont, MA;
Heather Marie Ames, South Boston, MA;
Massimiliano Versace, South Boston, MA;
Fabrizio Santini, Jamaica Plain, MA;

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

[X] Practitioners associated with the Customer Number 58249

OR

[ ] Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used)

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

[X] The address associated with Customer Number: 58249

OR

[ ] Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address
Neurala, Inc.
846 East 3rd Street
South Boston MA 02127

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	2/7/14
Name	Dr. Heather Ames	Telephone	
Title	Vice President, Neurala, Inc.		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Gorchetchnikov et al./Neurala Inc.

Application No./Patent No.: 11/860,254 / 8,648,867 Filed/Issue Date: 09/24/2007

Entitled: GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD

Neurala Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title and interest in
(The extent (by percentage) of its ownership interest is _____%); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

in the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Gorchetchnikov et al. To: Neurala LLC
The document was recorded in the United States Patent and Trademark Office at
Reel 020021, Frame 0986, or for which a copy thereof is attached.

2. From: Neurala LLC To: Neurala Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 032166, Frame 0599, or for which a copy thereof is attached.

3. From: _____ To: _____
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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy *(i.e.,* a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Christopher Max Colice/	February 25, 2014
Signature	Date
Christopher Max Colice	Reg. No. 65,634
Printed or Typed Name	Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

American LegalNet, Inc. www.FormsWorkflow.com

Electronic Acknowledgement Receipt	
EFS ID:	18290770
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Correspondence Address:	HEATHER AMES - APT 2 252 EAST 8TH ST. BOSTON MA 02127 US 5102058091 ames@neurala.com
Filer:	Christopher M. Colice/Tanya Koller
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	0167.0001US1
Receipt Date:	25-FEB-2014
Filing Date:	24-SEP-2007
Time Stamp:	14:57:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	NRLA_001_01US__POA.pdf	1629193 d29626315bcd7b098a959b2b779521c899368c97	no	1
Warnings:					
Information:					
2	Assignee showing of ownership per 37 CFR 3.73.	NRLA_001_01US__STATEMENT_373b.pdf	123831 185401b32c0faff8f1aedcb5ed7cdedfeceaa89e	no	1
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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

The United States of America

The Director of the United States Patent and Trademark Office

Has received an application for a patent for a new, original, and ornamental design for an article of manufacture. The title and description of the design are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the design shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the design throughout the United States of America or importing the design into the United States of America for the term of fourteen years from the date of grant of this patent, subject to any disclaimer under 35 U.S.C. 253.

Margaret A. Focarino

Commissioner for Patents of the United States Patent and Trademark Office

Neural AI, LLC, Exhibit 2045
Page 2045 - 236
IPR2025-00609, NVIDIA Corporation v. Neural AI, LLC
NVIDIA Ex1002
NVIDIA Corp. v. Neural AI, LLC
IPR2025-00606

ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C ...). The first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

11860254ZA

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Doc Code: Artifact Artifact Type Code X

1 Other, description: **PATENT GRANT**
Doc Code: Artifact Artifact Type Code: Z

March 8, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	GORCHETCHNIKO V, Anatoli, et al.	Confirmation No.:	6266
Application No.:	11/860,254	Group Art Unit:	2612
Filed:	September 24, 2007	Examiner:	

FOR: **GRAPHIC PROCESSOR BASED ACCELERATOR SYSTEM AND METHOD**

VIA EFS or
Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

COMMUNICATION REGARDING PATENT TERM ADJUSTMENT

In accordance with Applicants' duty of candor and good faith before the U.S. Patent and Trademark Office, Applicants note that the 1030 days of patent term adjustment indicated on the Patent Application Information Retrieval (PAIR) website for the above-captioned application disagrees with the Applicants' own calculation of Patent Term Adjustment. Applicants hereby request that the Patent Office verify the calculation of the Patent Term Adjustment for the present application.

Dated: February 27, 2014

Respectfully submitted,
COOLEY LLP

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By: /Christopher Max Colice/
Christopher Max Colice
Reg. No. 65634

190811 v1/BN

Electronic Acknowledgement Receipt	
EFS ID:	18321509
Application Number:	11860254
International Application Number:	
Confirmation Number:	6266
Title of Invention:	Graphic Processor Based Accelerator System and Method
First Named Inventor/Applicant Name:	Anatoli Gorchetchnikov
Correspondence Address:	HEATHER AMES - APT 2 252 EAST 8TH ST. BOSTON MA 02127 US 5102058091 ames@neurala.com
Filer:	Christopher M. Colice/Tanya Koller
Filer Authorized By:	Christopher M. Colice
Attorney Docket Number:	0167.0001US1
Receipt Date:	27-FEB-2014
Filing Date:	24-SEP-2007
Time Stamp:	14:41:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	NRLA_001_01US__DUTY_OF_CANDOR.pdf	75256 9a467ef1b1457427f22491122596a338c30e40c	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	75256		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

POWER OF ATTORNEY NOTICE

HEATHER AMES
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BOSTON, MA 02127

OC000000066925232

Date Mailed: 03/05/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/27/2014.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/860,254	09/24/2007	Anatoli Gorchetchnikov	0167.0001US1

CONFIRMATION NO. 6266

POA ACCEPTANCE LETTER

58249
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OC000000066925285

Date Mailed: 03/05/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/27/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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