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PROVISIONAL APPLICATION FOR PATENT COVER SHEET – Page 1 of 2

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120106

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Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max):

METHODS AND APPARATUSES FOR PROVIDING DIGITAL BASEBAND PREDISTORTION

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ENCLOSED APPLICATION PARTS (check all that apply)

☐ Application Data Sheet. See 37 CFR 1.76 ☐ CD(s), Number of CDs _____

☒ Specification *Number of Pages* 16 ☒ Other (specify) Appendix A to Specification; Credit

☒ Drawing(s) *Number of Sheets* 5

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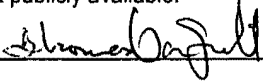


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SIGNATURE



Date December 1, 2006

TYPED or PRINTED NAME Thomas Van Zandt

REGISTRATION NO. 43,219
(if appropriate)

TELEPHONE (408) 292-5800

Docket Number: 038231-008

PROVISIONAL UNITED STATES PATENT APPLICATION

For

**METHODS AND APPARATUSES FOR PROVIDING DIGITAL BASEBAND
PREDISTORTION**

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METHODS AND APPARATUSES FOR PROVIDING DIGITAL BASEBAND PREDISTORTION**FIELD**

[0001] Embodiments of the invention relate generally to the field of predistortion techniques and more specifically to methods and apparatuses for providing digital baseband predistortion.

BACKGROUND

[0002] Modern wireless communication systems employ spectrally efficient, digitally modulated signals with wide bandwidths and time-varying envelopes. Such systems impose strict requirements on RF transmitters due to the utilization of the high spectrum efficient modulation schemes intended to preserve limited frequency resources. Variations in the envelope magnitude of digital modulations generate distortion components at the output of the transmitter that are caused by the inherent nonlinearity of RF amplification circuits.

[0003] Amplifier distortion produces a dilation of the spectrum of the input signal which causes adjacent channel interference. In addition to such spectral regrowth, amplifier nonlinearities produce in-band distortion which deteriorates the integrity of the transmitted signal.

[0004] Though it is desirable to effect a high degree of linearity while maintaining high power efficiency, conventional linearization techniques typically sacrifice power efficiency to enhance linearity.

[0005] A variety of linearization techniques are known in the art. One technique which increases the level of OBO to reduce output distortion by extending the linear

range of operation of the amplifier also produces a severe loss in efficiency due to reductions in RF output power resulting from higher OBO levels. High efficiency amplifiers typically may be linearized by simply increasing OBO and require more sophisticated linearization techniques such as feedback linearization. Feedback linearization is effective for narrow signal bandwidths but has very limited distortion correction capabilities when wide bandwidth operation is required. Such techniques, therefore would not be sufficient to linearize wide bandwidth, highly efficient transmitters. Other techniques such as feed forward linearization do not suffer from the bandwidth limitations of feedback linearizers but typically have low efficiency.

[0006] A technique suitable for high linearity and high efficiency amplification is predistortion linearization. The digital baseband predistortion technique, for example, can improve the linearity of the PA while maintaining high efficiency. However, for the wideband communication systems the strong memory effects exhibited by the transmitter/PA substantially limit the nonlinearity correction capability of the traditional memoryless predistortion techniques.

SUMMARY

[0007] For one embodiment of the invention, a digital baseband predistorter is disclosed that cascades two non-linear blocks. For one such embodiment, a dynamic weak nonlinear block and a static strong nonlinear block are cascaded.

[0008] Other features and advantages of embodiments of the present invention will be apparent from the accompanying drawings, and from the detailed description, that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The invention may be best understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

Figure 1A illustrates a block diagram of a forward LBG model predistorter system in accordance with one embodiment of the invention;

Figure 1B illustrates a block diagram of a reverse LBG model predistorter system in accordance with one embodiment of the invention;

Figure 2 illustrates a DWNL block in accordance with one embodiment of the invention;

Figure 3A illustrates a block diagram of a forward LBG model predistorter system in accordance with one embodiment of the invention;

Figure 3B illustrates a block diagram of a reverse LBG model predistorter system in accordance with one embodiment of the invention;

Figure 4 illustrates a predistorter implemented by cascading two nonlinear blocks to effect an augmented Weiner predistorter in accordance with one embodiment of the invention; and

Figure 5 illustrates a functional block diagram of a digital processing system in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

[0010] Method and apparatuses for providing digital baseband predistortion are disclosed. For one embodiment a digital baseband predistorter is disclosed that cascades two non-linear blocks. For one such embodiment, a dynamic weak nonlinear (DWNL) block and a static strong nonlinear (SSNL) block are cascaded.

[0011] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0012] Reference throughout the specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases “in one embodiment” or “in an embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0013] Moreover, inventive aspects lie in less than all features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention.

[0014] Embodiments of the invention are applicable in a variety of settings in which predistortion is effected. Alternative embodiments of the invention may be applied to analog as well as digital predistortion.

[0015] **Figure 1A** illustrates a block diagram of a forward LBG model predistorter system in accordance with one embodiment of the invention. As shown in Figure 1A, predistorter system 100A includes a DWNL block 105 followed by a SSNL block 110.

[0016] **Figure 1B** illustrates a block diagram of a reverse LBG model predistorter system in accordance with one embodiment of the invention. As shown in Figure 1B, predistorter system 100B includes a SSNL block 110 followed by a DWNL block 105.

[0017] For one embodiment of the invention, the SSNL block is implemented with two memoryless look-up tables (LUTs), which are only dependent on the magnitude of the current input complex signal of the SSNL block. The DWNL block may be implemented as a finite impulse response (FIR) filter based multi-branch non-linear structure.

[0018] **Figure 2** illustrates a DWNL block in accordance with one embodiment of the invention. DWNL block 200, shown in Figure 2, includes a number of FIR filters shown for example as FIR filters $205_1 - 205_p$. Each of the FIR filters $205_1 - 205_p$ has a related input as indicated in Figure 2. In accordance with some embodiments of the invention a limited number of branches are enough to obtain an accurate memory effect model because only weak nonlinear is involved.

[0019] As indicated above, an implementation of an LBG model predistorter in accordance with one embodiment of the invention implements the memoryless LUT and the multi-branch nonlinear structure. **Figure 3A** illustrates a block diagram of a forward LBG model predistorter system in accordance with one embodiment of the invention. Predistorter system 300A, shown in Figure 3A includes a DWNL block 305 implemented

as a FIR filter based multi-branch structure cascaded with an SSNL block 310 implemented as multiple memoryless LUTs.

[0020] The relationship between the input and output signals of the DWNL block 305 and the SSNL block 310, as shown in Figure 3 is described by equations 1 and 2 of Appendix A.

[0021] **Figure 3B** illustrates a block diagram of a reverse LBG model predistorter system in accordance with one embodiment of the invention. Predistorter system 300B, shown in Figure 3B includes an SSNL block 310 implemented as multiple memoryless LUTs cascaded with a DWNL block 305 implemented as a FIR filter based multi-branch structure.

[0022] The relationship between the input and output signals of the SSNL block 310 and the DWNL block 305, as shown in Figure 3B is described by equations 3 and 4 of Appendix A.

[0023] As indicated by equation 1 – 4 of Appendix A, knowledge of the static strong nonlinear part of the nonlinear model can substantially reduce the required number of branches of the DWNL block required for accurately modeling the dynamic nonlinearity of the nonlinear system. For one embodiment of the invention, the forward LBG model and the reverse LBG model can be used to provide pre-compensation for the transmitter output spectrum regrowth caused by the dynamic nonlinearity of the transmitter.

[0024] In accordance with various embodiments of the invention, the forward LBG model and the reverse LBG model can be used to effect a predistortion scheme in which different types of power amplifiers (PAs) are implemented. Such PAs may include for example, a push-pull FET PA, an LDMOS class AB PA, and a Doherty PA. The

effectiveness of the forward and reverse LBG models in accordance with various embodiments of the invention has been experimentally validated for a push-pull FET PA, an LDMOS class AB PA, and two Doherty PAs, having 1 – 4 carrier WCDMA test signals, respectively.

Augmented Wiener Predistorter

[0025] A predistorter in accordance with one embodiment of the invention may be implemented by cascading two nonlinear blocks. An augmented Wiener model in accordance with one embodiment of the invention is a first-order LBG model. Various embodiments of the invention may be of higher order. In the context of wideband transmitters, the electrical memory effects are the dominant sources of dispersion since the thermal time constant is large compared to the inverse of the signal bandwidth. The electrical memory effects may be attributable to such sources as trapping effects, impact ionization, the frequency response of the PA near the carrier frequency, impedance matching conditions at harmonic frequencies and the envelope frequency. A simple linear filter may compensate for device frequency variations, but not for the nonlinearities caused by the other sources.

[0026] For one embodiment of the invention, a conventional Wiener predistorter is augmented by replacing the FIR-based linear filter of the conventional Wiener predistorter with a nonlinear FIR-based filter implemented as multiple parallel FIR branches fed with high-order terms of the input. The nonlinear FIR-based filter acts as a nonlinear equalizer.

[0027] **Figure 4** illustrates a predistorter implemented by cascading two nonlinear blocks to effect an augmented Weiner predistorter in accordance with one embodiment of the invention.

[0028] Predistorter system 400, shown in **Figure 4** includes a first nonlinear block 405 which may be implemented as FIR filter-based memory effect predistorter. The first nonlinear block 405 is cascaded with a second nonlinear block 410 which may be implemented as a LUT-based memoryless nonlinear predistorter.

[0029] The relationship between the input and output signals of the first nonlinear block 405 and the second nonlinear block 410, as shown in **Figure 4** is described by equations 1 and 2 of Appendix A.

[0030] Some embodiments of the invention may employ a digital processing system (DPS) or devices having digital processing capabilities. For some such embodiments, a DPS employed may contain some or all of the components of a conventional DPS.

Figure 5 illustrates a functional block diagram of a digital processing system in accordance with one embodiment of the invention. The components of processing system 500, shown in **Figure 5** are exemplary in which one or more components may be omitted or added. For example, one or more memory devices may be utilized for processing system 500.

[0031] Referring to **Figure 5**, processing system 500 includes a central processing unit 502 and a signal processor 503 coupled to a main memory 504, static memory 506, and mass storage device 507 via bus 501. In accordance with an embodiment of the invention, main memory 504 may store a selective communication application, while mass storage device 507 may store various digital content as discussed above. Processing

system 500 may also be coupled to input/output (I/O) devices 525 via bus 501. Bus 501 is a standard system bus for communicating information and signals. CPU 502 and signal processor 503 are processing units for processing system 500. CPU 502 or signal processor 503 or both may be used to process information and/or signals for processing system 500. CPU 502 includes a control unit 531, an arithmetic logic unit (ALU) 532, and several registers 533, which are used to process information and signals. Signal processor 503 may also include similar components as CPU 502.

[0032] Main memory 504 may be, e.g., a random access memory (RAM) or some other dynamic storage device, for storing information or instructions (program code), which are used by CPU 502 or signal processor 503. Main memory 504 may store temporary variables or other intermediate information during execution of instructions by CPU 502 or signal processor 503. Static memory 506, may be, e.g., a read only memory (ROM) and/or other static storage devices, for storing information or instructions, which may also be used by CPU 502 or signal processor 503. Mass storage device 507 may be, e.g., a hard or floppy disk drive or optical disk drive, for storing information or instructions for processing system 500.

General Matters

[0033] Embodiments of the invention provide predistorters that cascade two or more nonlinear blocks. For one embodiment of the invention, a predistorter cascades a dynamic weak nonlinear block and a static strong nonlinear block.

[0034] Although various embodiments are described as implementing a finite impulse response (FIR) linear filter, alternative embodiments may implement other types

of linear filters (e.g., an infinite impulse response (IIR) filter or an auto-regressive moving average (ARMA) filter). Moreover, although described in the context of digital predistortion, the predistortion techniques described are equally applicable to analog predistortion.

[0035] Embodiments of the invention have been described as including various operations. Many of the processes are described in their most basic form, but operations can be added to or deleted from any of the processes without departing from the scope of the invention.

[0036] The operations of the invention may be performed by hardware components or may be embodied in machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the operations. Alternatively, the steps may be performed by a combination of hardware and software. The invention may be provided as a computer program product that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer (or other electronic devices) to perform a process according to the invention. The machine-readable medium may include, but is not limited to, floppy diskettes, optical disks, CD-ROMs, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, magnet or optical cards, flash memory, or other type of media / machine-readable medium suitable for storing electronic instructions. Moreover, the invention may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer by way of data signals embodied in a carrier wave or other propagation medium via a communication cell (e.g., a modem or network connection).

All operations may be performed at the same central cite or, alternatively, one or more operations may be performed elsewhere.

[0037] While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a dynamic nonlinear predistorter module; and

a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the dynamic nonlinear predistorter module is input to the static nonlinear predistorter module.
2. The apparatus of claim 1 wherein the dynamic nonlinear predistorter is a finite impulse response-based memory effect predistorter and the static nonlinear predistorter is a look-up table-based memoryless predistorter.
3. The apparatus of claim 1 wherein the dynamic nonlinear predistorter is a dynamic weak nonlinear predistorter and the static nonlinear predistorter is a static strong nonlinear predistorter.
4. The apparatus of claim 3 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table dependent on the magnitude of a current input signal.

5. An apparatus comprising:
 - a dynamic nonlinear predistorter module; and
 - a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the static nonlinear predistorter module is input to the dynamic nonlinear predistorter module.
6. The apparatus of claim 5 wherein the dynamic nonlinear predistorter module is a finite impulse response-based memory effect predistorter module and the static nonlinear predistorter is a look-up table-based memoryless predistorter module.
7. The apparatus of claim 5 wherein the dynamic nonlinear predistorter module is a dynamic weak nonlinear predistorter module and the static nonlinear predistorter is a static strong nonlinear predistorter module.
8. The apparatus of claim 7 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table dependent on the magnitude of a current input signal.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for effecting predistortion is disclosed. For one embodiment of the invention an apparatus comprises a first nonlinear predistorter and a second nonlinear predistorter coupled to the first such that an output of the first nonlinear predistorter is input to the second nonlinear predistorter. For one such embodiment of the invention the first nonlinear predistorter is a dynamic weak nonlinear predistorter and the second nonlinear predistorter is a static strong nonlinear predistorter. In an alternative embodiment, the first nonlinear predistorter is a static strong nonlinear predistorter and the second nonlinear predistorter is a dynamic weak nonlinear predistorter.

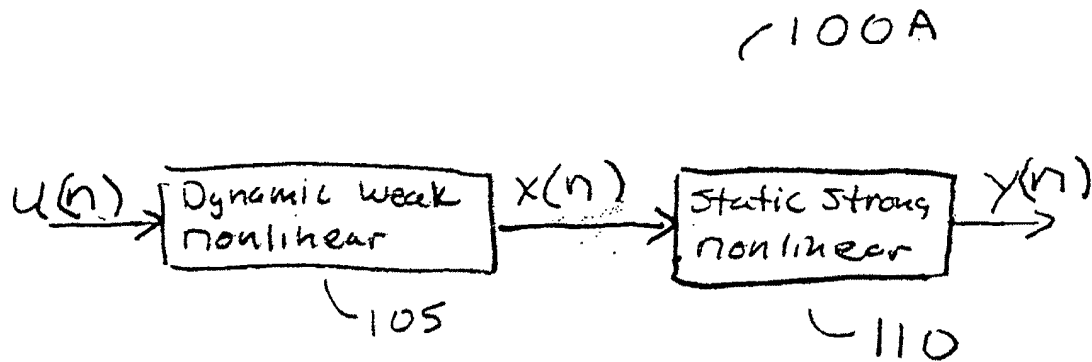


Fig. 1A

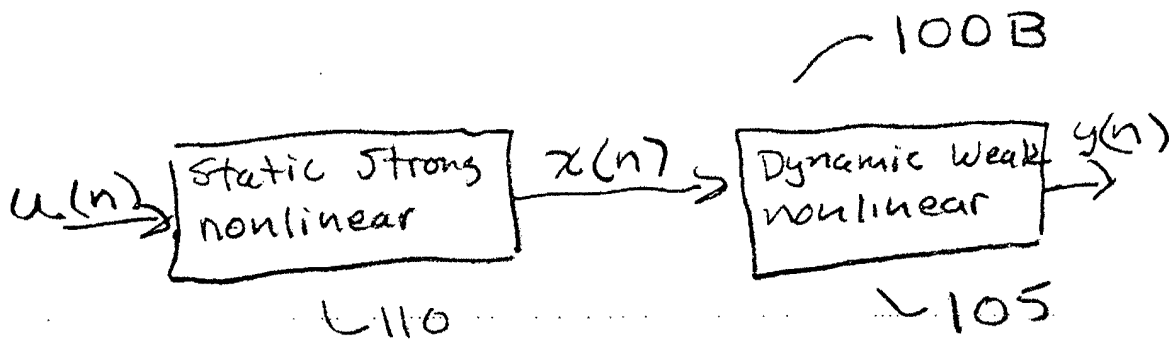


Fig. 1B

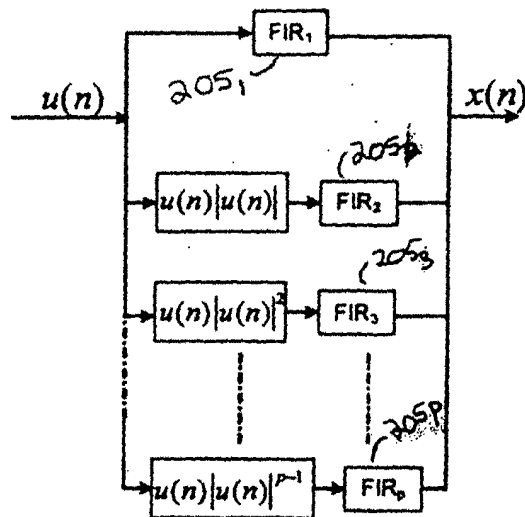


Fig. 2. Low-order memory polynomial based dynamic weak nonlinear sub-model.

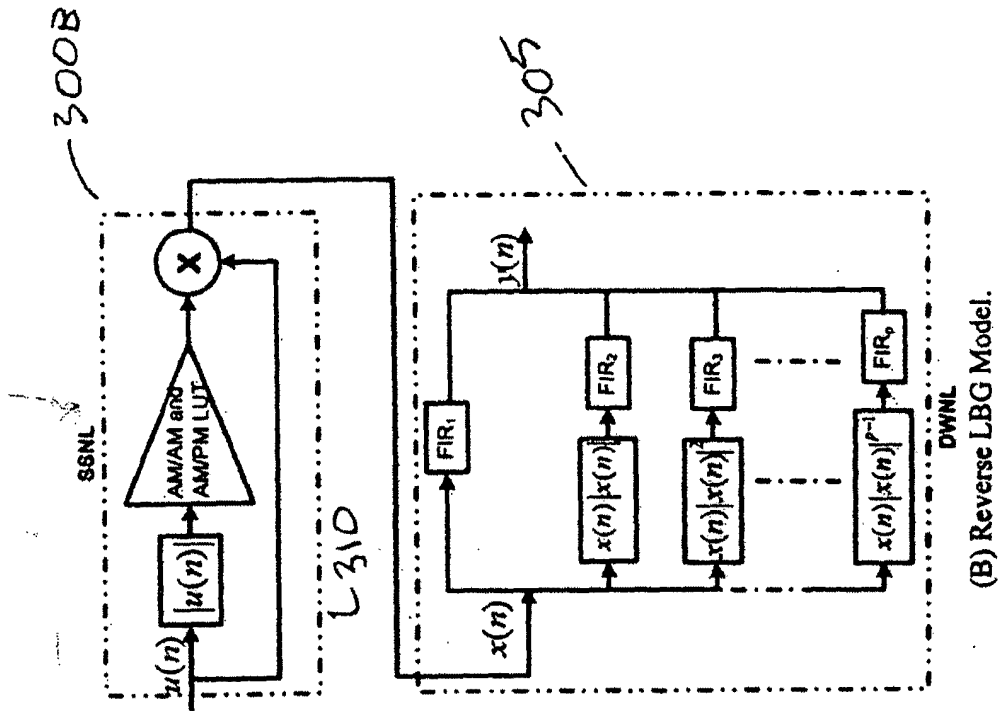


Fig. 3B

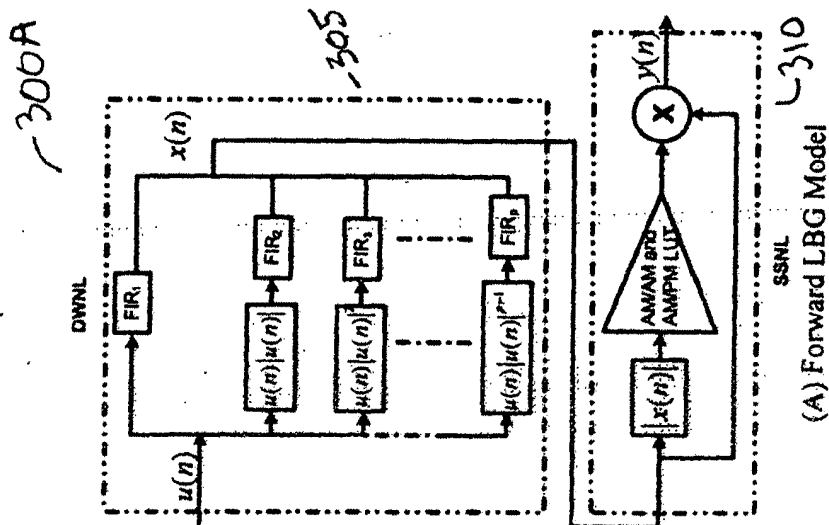


Fig. 3A

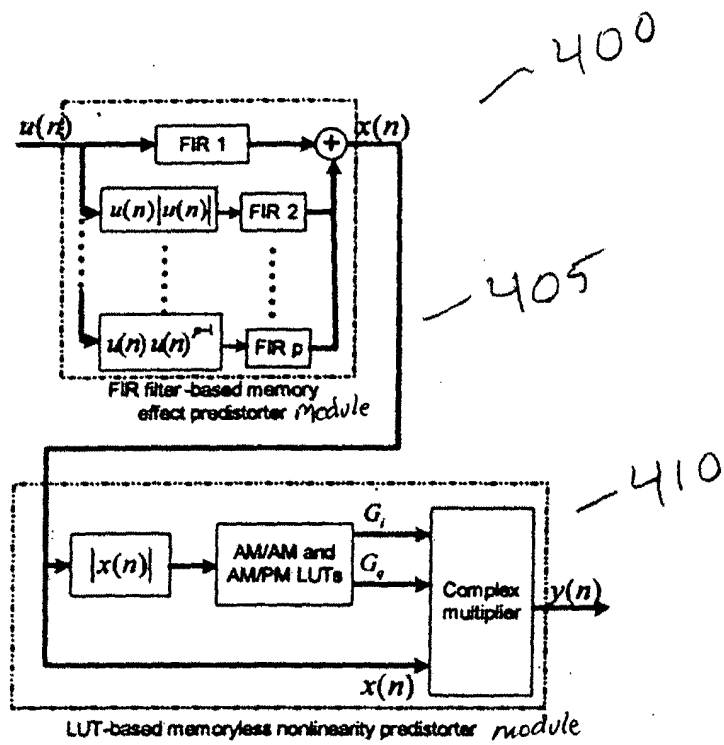


Fig. 4

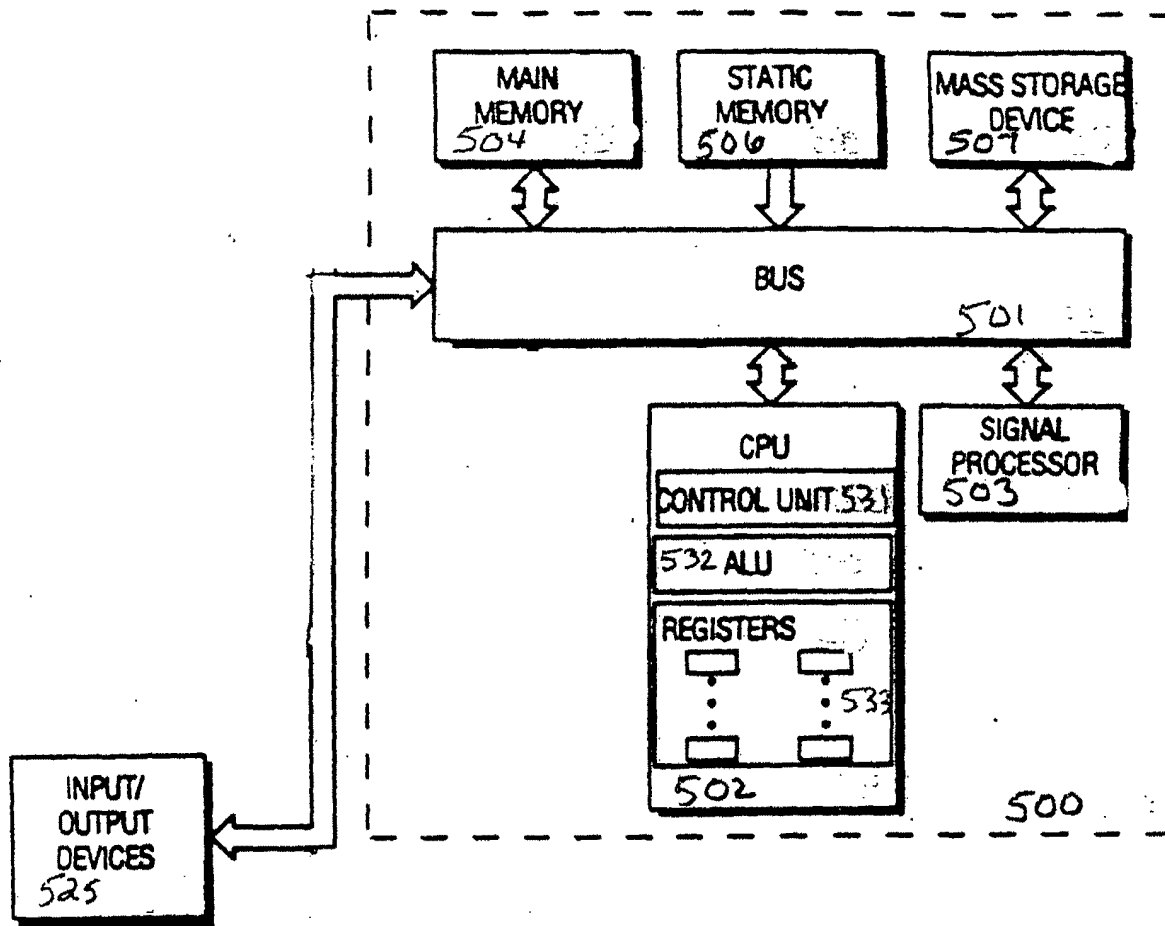


Fig. 5

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APPENDIX A

$$\begin{aligned}
 x(n) = & \sum_{i=0}^{M_1-1} a_{i0} u(n-i) + \sum_{i=0}^{M_2-1} a_{i1} |u(n-i)| u(n-i) \\
 & + \cdots + \sum_{i=0}^{M_p-1} a_{i,p-1} |u(n-i)|^{p-1} u(n-i)
 \end{aligned} \tag{1}$$

$$\begin{aligned}
 y(n) = & [G_{lul,i}(|x(n)|) + jG_{lul,q}(|x(n)|)] x(n) \\
 = & G_{lul}(|x(n)|) x(n)
 \end{aligned} \tag{2}$$

Where $G_{lu}(|x(n)|) = G_{lul,i}(|x(n)|) + jG_{lul,q}(|x(n)|)$ denotes the memoryless complex gain of the transmitter that depends only on the instantaneous magnitude of $x(n)$; $r = |x(n)|$ represents the magnitude of the output signal $x(n)$ of the weak dynamic nonlinear filter. m_j stands for the taps of the j^{th} FIR filter FIR_j , $j = 1, 2, \dots, p$; p represents the number of the branches of the memory model, and a_{ij} is the coefficients of the FIR filters.

Similarly, for the reverse LBG model shown in Fig. 3(B), the input, $u(n)$, and the output, $y(n)$, can be associated as follows:

$$x(n) = [G_{lul,i}(r) + jG_{lul,q}(r)] u(n) = G_{lul}(r) u(n) \tag{3}$$

$$\begin{aligned}
 y(n) = & \sum_{i=0}^{M_1-1} a_{i0} x(n-i) + \sum_{i=0}^{M_2-1} a_{i1} |x(n-i)| x(n-i) \\
 & + \cdots + \sum_{i=0}^{M_p-1} a_{i,p-1} |x(n-i)|^{p-1} x(n-i)
 \end{aligned} \tag{4}$$

where $G_{lu}(r) = G_{lul,i}(r) + jG_{lul,q}(r)$ denotes the memoryless complex gain of the transmitter that depends only on the instantaneous magnitude of $u(n)$. $r = |u(n)|$ represents the magnitude of the input signal $u(n)$. m_j , p and a_{ij} have the same meaning as in (1) and (2).

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
60/872,132	12/01/2006		200	038231-008	5		

CONFIRMATION NO. 9087

46188
THELEN REID & PRIEST, LLP
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SAN JOSE, CA 95164-0640

FILING RECEIPT

Date Mailed: 01/04/2007

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Applicant(s)

Taijun Liu, Calgary, CANADA;
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Power of Attorney:

Thomas Van Zandt--43219

If Required, Foreign Filing License Granted: 01/03/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US60/872,132

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Methods and apparatuses for providing digital baseband predistortion

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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