

EXHIBIT B-4

Invalidity of U.S. Patent No. 8,078,561 by “Digital Predistortion of Power Amplifiers for Wireless Applications” to Lei Ding (“Ding”)

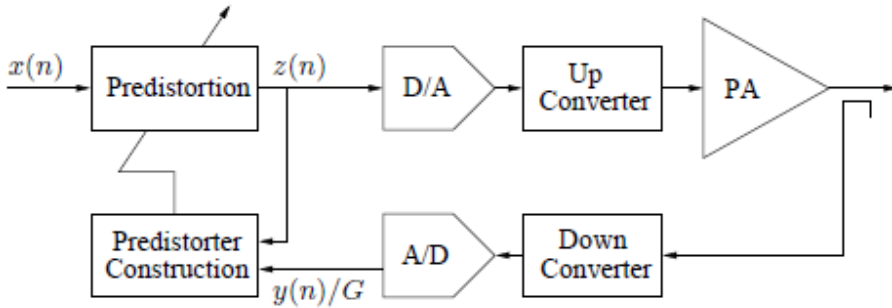
The Asserted Claims of U.S. Pat. No. 8,078,561 (“the ’561 Patent”) are anticipated and/or rendered obvious in view of a dissertation entitled “Digital Predistortion of Power Amplifiers for Wireless Applications” to Lei Ding (“Ding”) alone or in combination with other prior art. Ding was published on March 3, 2005 by the Georgia Institute of Technology School of Electrical and Computer Engineering. Ding, thus, is prior art to the ’561 Patent at least under §§ 102(a), 102(b), and/or 102(e).

As described in detail below, Ding anticipates Asserted Claims 1–22 of the ’561 Patent. In addition, to the extent that Smart RF asserts that Ding or citations below are insufficient, every limitation set forth in the claim was predictable and obvious in view of the knowledge and progression of the art. As such, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention, based on the explicit and implicit teaching of this reference and the prior art, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved to take the purportedly missing element from the art and combine it with the other elements in prior art identified in the cover pleading or herein.

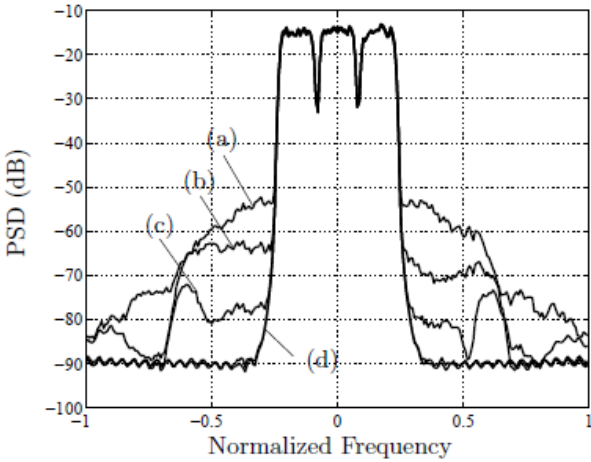
This claim chart is based on Defendants’ present understanding of the asserted claims, Smart RF’s vague and overbroad infringement contentions (and corresponding, implicit claim constructions), and Defendants’ investigations to date. Defendants are not adopting Smart RF’s apparent constructions, nor are Defendants admitting to the accuracy of any particular construction. Defendants reserve all rights to amend this invalidity claim chart in light of any claim-construction developments or any amendment to Smart RF’s infringement contentions. Further, as discovery is ongoing and Defendants continue to seek discovery from third parties regarding the references identified in Defendants’ invalidity contentions as well as other potential prior art, Defendants reserve the right to amend or supplement this claim chart identified in connection with Defendants’ continuing investigation. At minimum, Defendants intend to revise their invalidity contentions as appropriate to include discovery from third parties as discovery progresses. The claim chart below identifies where each limitation of the asserted claims of the ’561 Patent can be found in Ding. The citations provided below are exemplary, rather than exhaustive, and Defendants reserve the right to rely upon any other portion of the cited references.

Claim No.	’561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
1[pre]	A behavioral model of a nonlinear dynamic system, the model comprising:	To the extent the preamble is limiting, Ding discloses and/or renders obvious a behavioral model of a nonlinear dynamic system. <i>See, e.g.:</i> In this dissertation, we propose novel predistorters and their parameter extraction algorithms. We investigate a Hammerstein predistorter, a memory polynomial predistorter, and a new

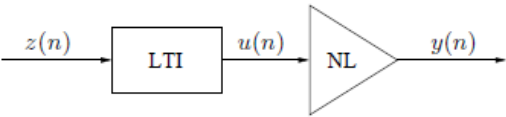
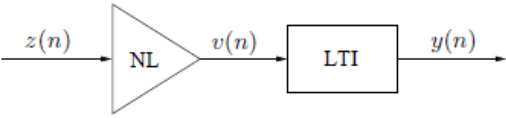
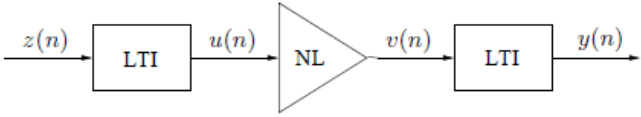
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		combined model based predistorter. The Hammerstein predistorter is designed specifically for power amplifiers that can be modeled as a Wiener system. The memory polynomial predistorter can correct both the nonlinear distortions and the linear frequency response that may exist in the power amplifier. It is a robust predistorter, which has demonstrated good performance on several nonlinear system models. (Ding, at Summary, xiii.) Among all linearization techniques, digital predistortion is one of the most cost effective (see Fig. 1). It adds a digital predistorter in the baseband to create an expanding nonlinearity that is complementary to the compressing characteristic of the power amplifier. Ideally, the cascade of the predistorter and the power amplifier becomes linear and the original input is amplified by a constant gain. With the predistorter, the power amplifier can be utilized up to its saturation point while still maintaining a good linearity, thereby significantly increasing its efficiency. In reality, the power amplifier characteristics may change []over time because of temperature drift, component aging, etc. Therefore, the predistorter should also have the ability to adapt to these changes. (Ding, at 1–2.)

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		 Figure 1: Digital Predistortion System Diagram (Ding, at Fig. 1.) Digital predistortion implementations in the current literature mostly focus on the power amplifier that has a memoryless nonlinearity; i.e., the current output depends only on the current input through a nonlinear mechanism. This instantaneous nonlinearity is usually characterized by the AM/AM and AM/PM responses of the power amplifier, where the output signal amplitude and phase deviation of the power amplifier output are given as functions of the amplitude of its current input. (Ding, at 2.) The causes of the memory effects can be attributed to thermal constants of the active devices or components in the biasing network that have frequency dependent behaviors [47]. As a result, the current output of the power amplifier depends not only on the current input, but also on past input values. In other words, the power amplifier becomes a nonlinear system with memory. For such a power amplifier, memoryless predistortion can achieve only very limited linearization performance [29], [17]. Therefore, digital predistorters also need to have

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		memory structures. This dissertation investigates robust predistorter models that are capable of linearizing power amplifiers with memory effects. It also investigates system implementation issues related to these wideband digital predistortion systems. (Ding, at 2.) A memoryless power amplifier can be characterized by its AM/AM and AM/PM responses. To linearize such a power amplifier, a memoryless predistorter is sufficient. For a power amplifier with memory effects, various models are available to capture the behavior of the power amplifier, which include the Volterra series, the Wiener model, the Hammerstein model, and the Wiener-Hammerstein model. The indirect learning architecture is then presented to construct the predistorter for a power amplifier with memory effects. (Ding, at 3–4.) For power amplifiers with memory effects, memoryless predistortion can achieve only very limited linearization performance [29], [17]. Thus, digital predistorters also need to have memory structures. (Ding, at 14.) In the current literature, digital predistorters with memory structures are mostly considered for data predistortion of the cascade of a pulse shaping filter and a memoryless power amplifier, as reviewed in Section 2.2.1. The models that have been considered for these predistorters include the Volterra series [20], [21], the Hammerstein model [25], and the memory polynomial model [10]. One exception is [32], in which Ma et al. applied a Murray Hill model based predistorter to a power amplifier with memory effects and achieved good linearization performance. (Ding, at 15.)

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		 Figure 12: Comparison of the PSDs for FIR Wiener power amplifier and 15-tap FIR Hammerstein predistorter. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with Hammerstein predistortion (NG); (d) Output with Hammerstein predistortion (LS/SVD). (Ding, at Fig. 12.)
1[a]	a first module characterizing dynamic nonlinear characteristics of the system, wherein the first module includes an input and an output; and	Ding discloses and/or renders obvious a first module characterizing dynamic nonlinear characteristics of the system, wherein the first module includes an input and an output. <i>See, e.g.:</i>

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		Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). The two subsystems are given by $u(n) = \sum_{l=0}^{L-1} a_l z(n-l),$ $y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k u(n) u(n) ^{k-1},$ where a_l are the impulse response values of the LTI block and b_k are the coefficients of the odd-order polynomial describing the memoryless nonlinearity. Substituting (13) into (14) gives

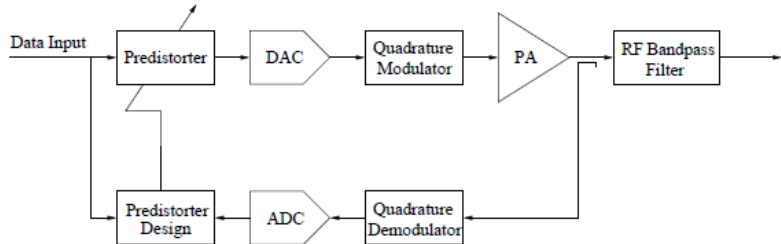
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		$y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k \left[\sum_{l=0}^{L-1} a_l z(n-l) \right] \left \sum_{l=0}^{L-1} a_l z(n-l) \right ^{k-1}.$ The Wiener model was used by Clark et al. [11] to model the power amplifier with memory effects, where improvements in modeling accuracy were observed when the Wiener model replaces the memoryless polynomial model. (Ding, at 11.)  Figure 6: The Wiener Model.  Figure 7: The Hammerstein Model.  Figure 8: The Wiener-Hammerstein model.

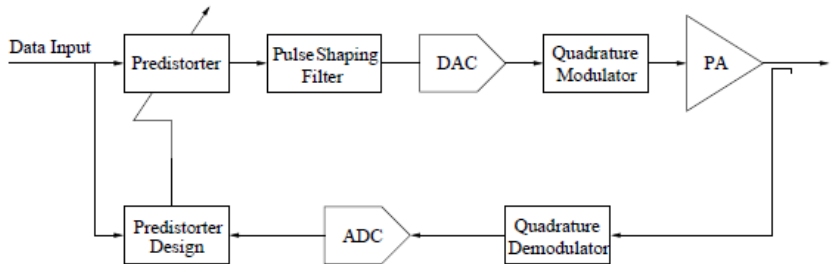
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		(Ding, at Figs. 7–9.) The Wiener-Hammerstein (W-H) model (see Fig. 8) is an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [2]. (Ding, at 13.) Example 3.2 The LTI portion of the Wiener power amplifier is $H(z) = 1 + 0.3z^{-2}$ (FIR), and the LTI portion of the Hammerstein predistorter is assumed to be FIR as well. The objective here is to see whether the algorithms can correctly identify an FIR filter that approximates the inverse of the FIR system in the power amplifier. When the FIR system in the predistorter has 15 taps, the performance of the predistorter is shown in Fig. 12. In this case, the NG algorithm performs worse than the LS/SVD algorithm. When examining the concatenated response of the two LTI blocks (one from the Wiener power amplifier and the other from the Hammerstein predistorter), it is observed that the predistorter's LTI system identified by the NG algorithm can only compensate for the power amplifier's LTI system within the signal bandwidth. However, the LS/SVD algorithm is able to find a good FIR system for the predistorter, both within and outside of the signal bandwidth. (Ding, at 23.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different

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		nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 27.) <pre> graph LR x_n["x(n)"] --> H_z["H(z)"] H_z --> v_n["v(n)"] v_n --> F_v["F(v)"] F_v --> w_n["w(n)"] w_n --> G_z["G(z)"] G_z --> y_n["y(n)"] </pre> Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2]. The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block.

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		(Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.) Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2$, $K = 5$) (d) Original input. (c) and (d) almost coincide.

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		(Ding, at Fig. 16.) In all of the above cases, memoryless predistortion is not very effective in suppressing spectral regrowth, which underscores the notion that power amplifier memory effects must be taken into account when designing the predistorter. [] The objective of power amplifier linearization is two-fold: suppression of spectral regrowth to reduce adjacent channel interference and minimization of in-band distortion to improve BER. Although only PSD plots are shown here, this does not mean that in-band distortion is left un-checked. Recall that in the indirect learning architecture, our convergence criterion requires the mean squared error between $y(n)$ and $Gx(n)$ to be minimized. Therefore, at convergence, the power amplifier is linearized, which automatically ensures the suppression of both in-band and out-of-band distortions. (Ding, at 31.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
1[b]	a second module characterizing static nonlinear characteristics of the nonlinear system, wherein the second module includes an input and an output;	Ding discloses and/or renders obvious a second module characterizing static nonlinear characteristics of the nonlinear system, wherein the second module includes an input and an output. <i>See</i> claim element 1[a], <i>supra</i>, which is incorporated by reference herein.

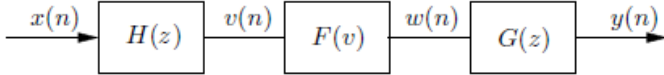
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		<i>See also, e.g.:</i> [P]ower amplifiers that are strictly memoryless or quasi-memoryless can be characterized by their AM/AM and AM/PM conversions. As an example, the AM/AM and AM/PM responses of a memoryless Class AB power amplifier are shown in Fig. 2.  Figure 3: Block diagram of a data predistortion system with the pulse shaping filter implemented after the power amplifier. (Ding, at 6–7.) Depending on the location of the pulse shaping filter in the transmitter, there are two types of data predistorters. The first type, exemplified by [24], [41], implements the pulse shaping filter using a radio frequency (RF) bandpass filter after the power amplifier. . . . The predistorter can be easily implemented as look-up tables (LUTs) that map the original input constellation points to the desired locations. Because of the small size of the input levels, this type of predistorters converges fast and requires very little memory. (Ding, at 7.) The second type, exemplified by [26], [27], [20], considers the case where the pulse shaping filter is placed in the baseband, immediately after the data predistorter (see Fig. 4). . . . The approach taken by [26] uses a specific pulse shaping filter to generate discrete values at two or three equally spaced data points per symbol interval. Each data point is then predistorted

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		by a memoryless predistorter and combined with adjacent data points to reduce the nonlinear distortion at the power amplifier output. (Ding, at 8.)  Figure 4: Block diagram of a data predistortion system with the pulse shaping filter placed in the baseband after the predistorter. (Ding, at Fig. 4.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 27.)

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		Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2].

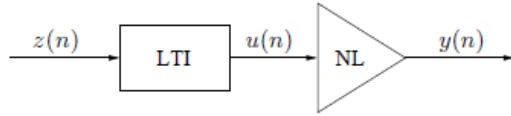
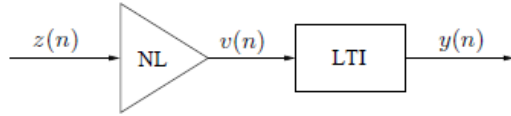
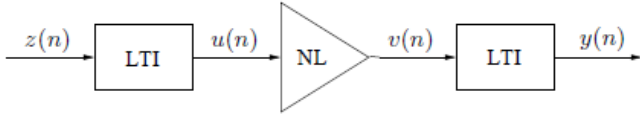
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		The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block. (Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.)

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		Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity

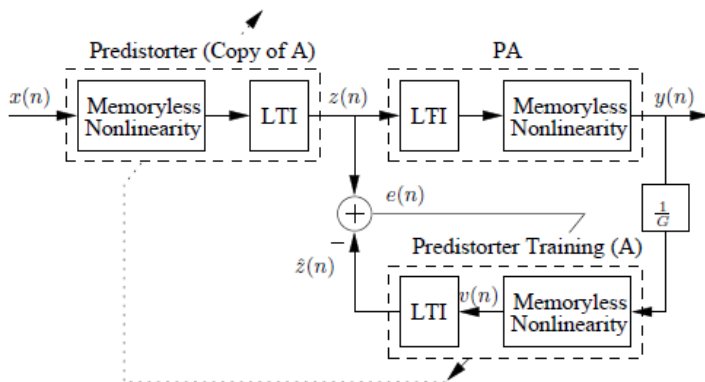
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		Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
1[c]	wherein the first module is coupled to the second module.	Ding discloses and/or renders obvious “wherein the first module is coupled to the second module.” <i>See, e.g.:</i> A Hammerstein predistorter is ideal for linearization of a Wiener system. The Wiener system can be either a power amplifier with memory effects [11] or the cascade of a pulse shaping filter and a memoryless power amplifier [25]. To construct a Hammerstein predistorter, the approach taken be [25] uses a gradient method to first identify the Wiener system and then to find the Hammerstein predistorter as its inverse. An alternative approach is pursued here and [14], which generates the Hammerstein predistorter without first identifying the Wiener power amplifiers by using the indirect learning architecture. (Ding, at 17.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 27.)  Figure 15: Wiener-Hammerstein model diagram.

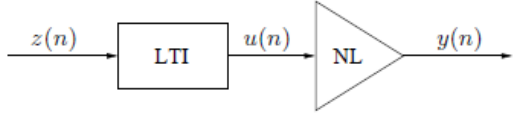
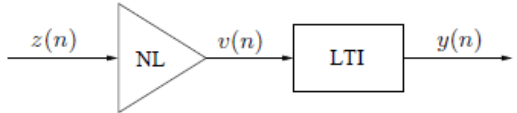
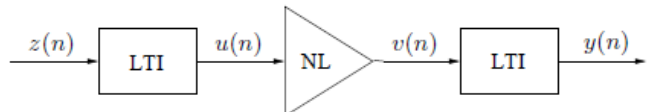
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		(Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2]. The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block. (Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.)

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		Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity

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		Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
2	The model of claim 1, wherein the first module is coupled to the second module such that an output of the first module is input to the second module.	Ding discloses and/or renders obvious the model of claim 1, wherein the first module is coupled to the second module such that an output of the first module is input to the second module. <i>See claim 1, supra, which is incorporated by reference herein.</i> <i>See also, e.g.:</i>  Figure 6: The Wiener Model.  Figure 7: The Hammerstein Model.  Figure 8: The Wiener-Hammerstein model.

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		(Ding, at Figs. 7–9.) The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). . . . The Wiener model was used by Clark et al. [11] to model the power amplifier with memory effects, where improvements in modeling accuracy were observed when the Wiener model replaces the memoryless polynomial model. . . . The Hammerstein model is a memoryless nonlinearity followed by an LTI system (see Fig. 7). . . . The Wiener-Hammerstein (W-H) model (see Fig. 8) is an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [2]. (Ding, at 11–13.) A Hammerstein predistorter is ideal for linearization of a Wiener system. The Wiener system can be either a power amplifier with memory effects [11] or the cascade of a pulse shaping filter and a memoryless power amplifier [25]. To construct a Hammerstein predistorter, the approach taken by [25] uses a gradient method to first identify the Wiener system and then find the Hammerstein predistorter as its inverse. An alternative approach is pursued here and [14], which generates the Hammerstein predistorter without first identifying the Wiener power amplifier by using the indirect learning architecture. (Ding, at 17.)

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		 Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
3	The method of claim 1, wherein the second module is coupled to the first module such that an output of	Ding discloses and/or renders obvious “[t]he method of claim 1, wherein the second module is coupled to the first module such that an output of the second module is input to the first module.”

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	the second module is input to the first module.	See claims 1 and 2, <i>supra</i>, which are incorporated by reference herein. See also, e.g.:  Figure 6: The Wiener Model.  Figure 7: The Hammerstein Model.  Figure 8: The Wiener-Hammerstein model. (Ding, at Figs. 7–9.) The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). . . . The Wiener model was used by Clark et al. [11] to model the power amplifier with memory effects, where improvements in modeling accuracy were

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		observed when the Wiener model replaces the memoryless polynomial model. . . . The Hammerstein model is a memoryless nonlinearity followed by an LTI system (see Fig. 7). . . . The Wiener-Hammerstein (W-H) model (see Fig. 8) is an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [2]. (Ding, at 11–13.) A Hammerstein predistorter is ideal for linearization of a Wiener system. The Wiener system can be either a power amplifier with memory effects [11] or the cascade of a pulse shaping filter and a memoryless power amplifier [25]. To construct a Hammerstein predistorter, the approach taken by [25] uses a gradient method to first identify the Wiener system and then find the Hammerstein predistorter as its inverse. An alternative approach is pursued here and [14], which generates the Hammerstein predistorter without first identifying the Wiener power amplifier by using the indirect learning architecture. (Ding, at 17.)

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
4	The model of claim 1 wherein the first module comprises a nonlinear finite impulse response-based	Ding discloses and/or renders obvious “[t]he model of claim 1 wherein the first module comprises a nonlinear finite impulse response-based memory effect system and the second module comprises a look-up table-based nonlinear memoryless system.”

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
	memory effect system and the second module comprises a look-up table-based nonlinear memoryless system.	See claim 1, <i>supra</i>, which is incorporated by reference herein. See also, e.g.: Considering that the AM/AM and AM/PM responses of the memoryless power amplifier depend only on the input amplitude, the two-dimensional LUT in the mapping predistorter can actually be replaced by two one-dimensional LUTs. Indexed by the input amplitude $r_x(t)$, the one-dimensional LUTs specify the desired output amplitude, $A[r_x(t)]$, and the phase shift, $\phi_A[r_x(t)]$; i.e., the predistorted output is given by $z(t) = A[r_x(t)] e^{j\{\phi_x(t) + \phi_A[r_x(t)]\}}, \quad (6)$ where $\phi_x(t)$ is the p[h]ase of the input signal $x(t)$. Since the predistortion LUTs are in polar form, this predistorter, proposed by [] Faulkner et al. [22], is often referred to as the polar structure predistorter. In practical implementations, phase calculation in the polar conversion for each input complex point is quite computationally intensive. Faulkner <i>et al.</i> [22] also provided an efficient implementation to avoid the polar conversion during predistortion, which is a rearrangement of (6); i.e., $z(t) = x(t) \frac{A[r_x(t)]}{r_x(t)} e^{j\phi_A[r_x(t)]}, \quad (7)$. . . An approach similar to the polar predistorter was proposed by Cavers [6]. It employs a complex gain table instead of the gain and phase tables in the polar predistorter; i.e., $F[r_x(t)] = \frac{A[r_x(t)]}{r_x(t)} e^{j\phi_A[r_x(t)]}. \quad (8)$ The predistorted output is then given by $z(t) = x(t) F[r_x(t)]. \quad (9)$ This structure avoids the conversions between polar and Cartesian forms. Therefore, it is

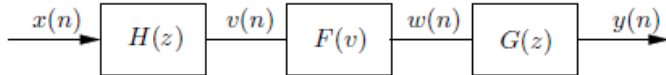
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		more computationally efficient. Furthermore, only one complex multiplication is needed in (9) as opposed to two real and one complex multiplications in (7). (Ding, at 9–10.) Example 3.2 The LTI portion of the Wiener power amplifier is $H(z) = 1 + 0.3z^{-2}$ (FIR), and the LTI portion of the Hammerstein predistorter is assumed to be FIR as well. The objective here is to see whether the algorithms can correctly identify an FIR filter that approximates the inverse of the FIR system in the power amplifier. When the FIR system in the predistorter has 15 taps, the performance of the predistorter is shown in Fig. 12. In this case, the NG algorithm performs worse than the LS/SVD algorithm. When examining the concatenated response of the two LTI blocks (one from the Wiener power amplifier and the other from the Hammerstein predistorter), it is observed that the predistorter's LTI system identified by the NG algorithm can only compensate for the power amplifier's LTI system within the signal bandwidth. However, the LS/SVD algorithm is able to find a good FIR system for the predistorter, both within and outside of the signal bandwidth. (Ding, at 23.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
5	The model of claim 1 wherein the first module is a dynamic weak nonlinear model and the second module is a static strong nonlinear model.	Ding discloses and/or renders obvious “[t]he model of claim 1 wherein the first module is a dynamic weak nonlinear model and the second module is a static strong nonlinear model.” See claim 1, <i>supra</i>, which is incorporated by reference herein. See also, e.g.: Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). The two subsystems are given by

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		$u(n) = \sum_{l=0}^{L-1} a_l z(n-l),$ $y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k u(n) u(n) ^{k-1},$ where a_l are the impulse response values of the LTI block and b_k are the coefficients of the odd-order polynomial describing the memoryless nonlinearity. Substituting (13) into (14) gives $y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k \left[\sum_{l=0}^{L-1} a_l z(n-l) \right] \left \sum_{l=0}^{L-1} a_l z(n-l) \right ^{k-1}.$ The Wiener model was used by Clark et al. [11] to model the power amplifier with memory effects, where improvements in modeling accuracy were observed when the Wiener model replaces the memoryless polynomial model. (Ding, at 11.)

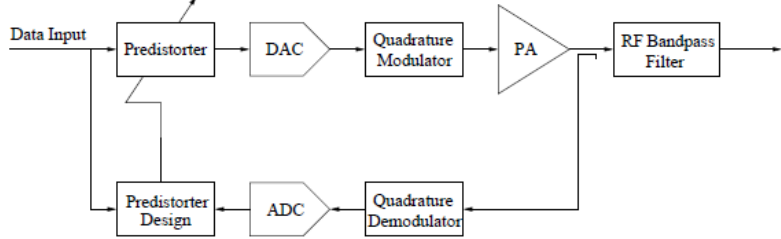
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Figure 6: The Wiener Model. Figure 7: The Hammerstein Model. Figure 8: The Wiener-Hammerstein model. (Ding, at Figs. 7–9.) The Wiener-Hammerstein (W-H) model (see Fig. 8) is an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [2]. (Ding, at 13.)

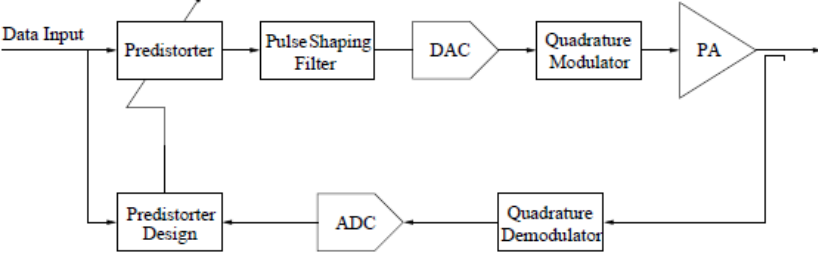
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		The Murray Hill model, proposed by Ma <i>et al.</i> [32], introduces a set of nonlinear terms into the conventional memoryless polynomial model based on the underlying physical phenomena. For each input, these terms generate a complex gain that depends on the combination of the current and past input signal envelopes in a nonlinear fashion. The output of the model is given by $y(n) = \sum_{p=1}^P a_p z(n) z(n) ^{p-1} + \sum_{q=2}^Q b_q z(n) \left[\sum_{l=0}^{L-1} c_l z(n-l) \right]^{q-1}, \quad (24)$ (Ding, at 14.) In the current literature, digital predistorters with memory structures are mostly considered for data predistortion of the cascade of a pulse shaping filter and a memoryless power amplifier, as reviewed in Section 2.2.1. The models that have been considered for these predistorters include the Volterra series [20], [21], the Hammerstein model [25], and the memory polynomial model [10]. One exception is [32], in which Ma <i>et al.</i> applied a Murray Hill model based predistorter to a power amplifier with memory effects and achieved good linearization performance. To construct digital predistorters with memory structures, there are two types of approaches. One type of approach is to first identify the power amplifier and then find the inverse of the power amplifier, which was used in [25]. . . . Another type of approach is to use the indirect learning architecture to design the predistorter directly, as adopted in [20], [10]. (Ding, at 15.) Example 3.2 The LTI portion of the Wiener power amplifier is $H(z) = 1 + 0.3z^{-2}$ (FIR), and the LTI portion of the Hammerstein predistorter is assumed to be FIR as well. The objective here is to see whether the algorithms can correctly identify an FIR filter that

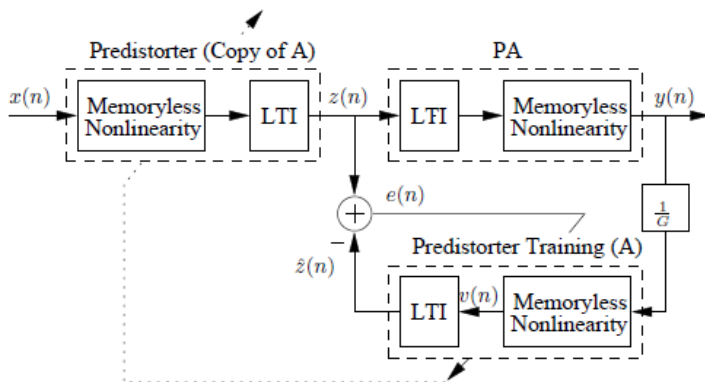
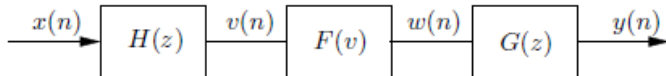
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		approximates the inverse of the FIR system in the power amplifier. When the FIR system in the predistorter has 15 taps, the performance of the predistorter is shown in Fig. 12. In this case, the NG algorithm performs worse than the LS/SVD algorithm. When examining the concatenated response of the two LTI blocks (one from the Wiener power amplifier and the other from the Hammerstein predistorter), it is observed that the predistorter's LTI system identified by the NG algorithm can only compensate for the power amplifier's LTI system within the signal bandwidth. However, the LS/SVD algorithm is able to find a good FIR system for the predistorter, both within and outside of the signal bandwidth. (Ding, at 23.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 26–27.)  Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2]. The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block. (Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.)

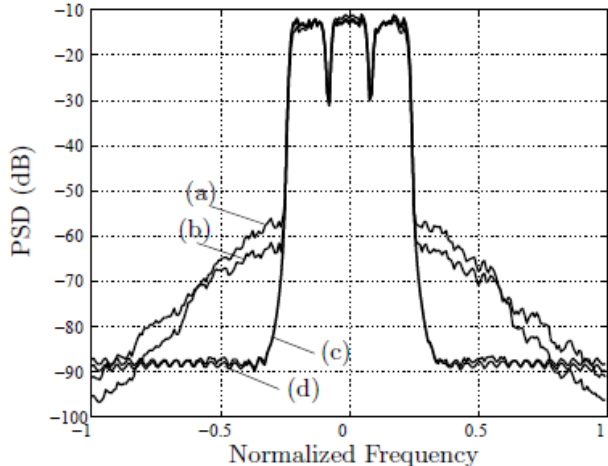
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) In all of the above cases, memoryless predistortion is not very effective in suppressing spectral regrowth, which underscores the notion that power amplifier memory effects must be taken into account when designing the predistorter. [] The objective of power amplifier linearization is two-fold: suppression of spectral regrowth to reduce adjacent channel interference and minimization of in-band distortion to improve BER. Although only PSD plots are shown here, this does not mean that in-band distortion is left un-checked. Recall that in the indirect learning architecture, our convergence criterion requires the mean squared error between $y(n)$ and $Gx(n)$ to be minimized. Therefore, at convergence, the power amplifier

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		is linearized, which automatically ensures the suppression of both in-band and out-of-band distortions. (Ding, at 31.) [P]ower amplifiers that are strictly memoryless or quasi-memoryless can be characterized by their AM/AM and AM/PM conversions. As an example, the AM/AM and AM/PM responses of a memoryless Class AB power amplifier are shown in Fig. 2.  Figure 3: Block diagram of a data predistortion system with the pulse shaping filter implemented after the power amplifier. (Ding, at 6–7.) Depending on the location of the pulse shaping filter in the transmitter, there are two types of data predistorters. The first type, exemplified by [24], [41], implements the pulse shaping filter using a radio frequency (RF) bandpass filter after the power amplifier. . . . The predistorter can be easily implemented as look-up tables (LUTs) that map the original input constellation points to the desired locations. Because of the small size of the input levels, this type of predistorters converges fast and requires very little memory. (Ding, at 7.)

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		The second type, exemplified by [26], [27], [20], considers the case where the pulse shaping filter is placed in the baseband, immediately after the data predistorter (see Fig. 4). . . . The approach taken by [26] uses a specific pulse shaping filter to generate discrete values at two or three equally spaced data points per symbol interval. Each data point is then predistorted by a memoryless predistorter and combined with adjacent data points to reduce the nonlinear distortion at the power amplifier output. (Ding, at 8.)  Figure 4: Block diagram of a data predistortion system with the pulse shaping filter placed in the baseband after the predistorter. (Ding, at Fig. 4.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 27.)

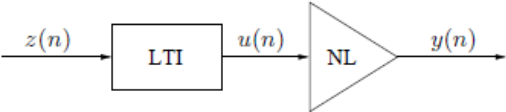
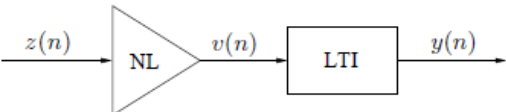
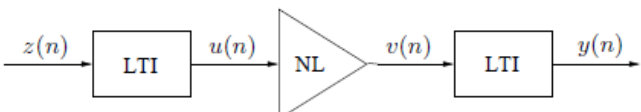
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		 Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.)  Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2].

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block. (Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.)

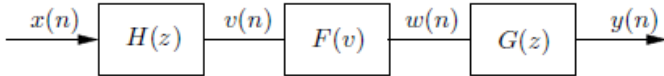
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		 Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity

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		Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
6	The model of claim 1 wherein the first module comprises a finite impulse response filter-based multi-branch nonlinear system and the second module comprises two look-up tables, each look-up table dependent on the magnitude of the input signal.	Ding discloses and/or renders obvious “[t]he model of claim 1 wherein the first module comprises a finite impulse response filter-based multi-branch nonlinear system and the second module comprises two look-up tables, each look-up table dependent on the magnitude of the input signal.” See claim 1, <i>supra</i>, which is incorporated by reference herein. See also, e.g.: Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). The two subsystems are given by

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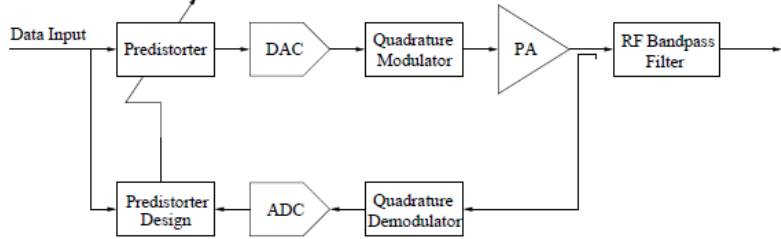
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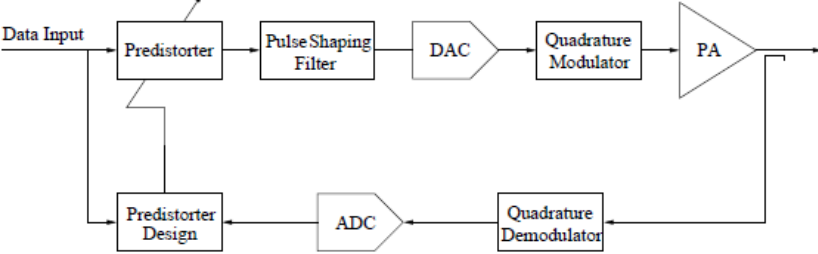
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		The Murray Hill model, proposed by Ma <i>et al.</i> [32], introduces a set of nonlinear terms into the conventional memoryless polynomial model based on the underlying physical phenomena. For each input, these terms generate a complex gain that depends on the combination of the current and past input signal envelopes in a nonlinear fashion. The output of the model is given by $y(n) = \sum_{p=1}^P a_p z(n) z(n) ^{p-1} + \sum_{q=2}^Q b_q z(n) \left[\sum_{l=0}^{L-1} c_l z(n-l) \right]^{q-1}, \quad (24)$ (Ding, at 14.) In the current literature, digital predistorters with memory structures are mostly considered for data predistortion of the cascade of a pulse shaping filter and a memoryless power amplifier, as reviewed in Section 2.2.1. The models that have been considered for these predistorters include the Volterra series [20], [21], the Hammerstein model [25], and the memory polynomial model [10]. One exception is [32], in which Ma <i>et al.</i> applied a Murray Hill model based predistorter to a power amplifier with memory effects and achieved good linearization performance. To construct digital predistorters with memory structures, there are two types of approaches. One type of approach is to first identify the power amplifier and then find the inverse of the power amplifier, which was used in [25]. . . . Another type of approach is to use the indirect learning architecture to design the predistorter directly, as adopted in [20], [10]. (Ding, at 15.) Example 3.2 The LTI portion of the Wiener power amplifier is $H(z) = 1 + 0.3z^{-2}$ (FIR), and the LTI portion of the Hammerstein predistorter is assumed to be FIR as well. The objective here is to see whether the algorithms can correctly identify an FIR filter that

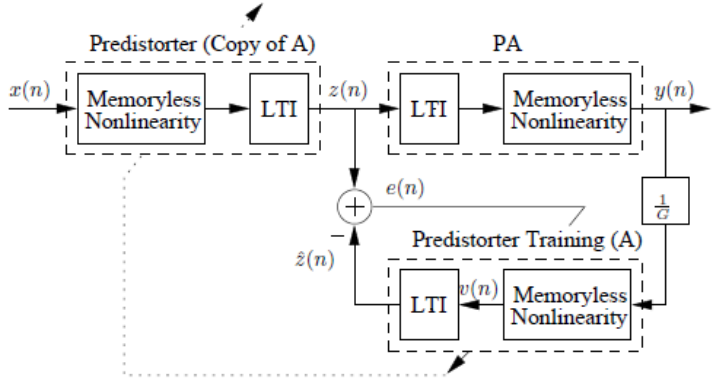
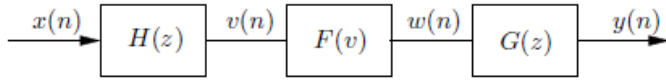
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		approximates the inverse of the FIR system in the power amplifier. When the FIR system in the predistorter has 15 taps, the performance of the predistorter is shown in Fig. 12. In this case, the NG algorithm performs worse than the LS/SVD algorithm. When examining the concatenated response of the two LTI blocks (one from the Wiener power amplifier and the other from the Hammerstein predistorter), it is observed that the predistorter's LTI system identified by the NG algorithm can only compensate for the power amplifier's LTI system within the signal bandwidth. However, the LS/SVD algorithm is able to find a good FIR system for the predistorter, both within and outside of the signal bandwidth. (Ding, at 23.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 26–27.)  Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is

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Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) In all of the above cases, memoryless predistortion is not very effective in suppressing spectral regrowth, which underscores the notion that power amplifier memory effects must be taken into account when designing the predistorter. [] The objective of power amplifier linearization is two-fold: suppression of spectral regrowth to reduce adjacent channel interference and minimization of in-band distortion to improve BER. Although only PSD plots are shown here, this does not mean that in-band distortion is left un-checked. Recall that in the indirect learning architecture, our convergence criterion requires the mean squared error between $y(n)$ and $Gx(n)$ to be minimized. Therefore, at convergence, the power amplifier

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		is linearized, which automatically ensures the suppression of both in-band and out-of-band distortions. (Ding, at 31.) [P]ower amplifiers that are strictly memoryless or quasi-memoryless can be characterized by their AM/AM and AM/PM conversions. As an example, the AM/AM and AM/PM responses of a memoryless Class AB power amplifier are shown in Fig. 2.  Figure 3: Block diagram of a data predistortion system with the pulse shaping filter implemented after the power amplifier. (Ding, at 6–7.) Depending on the location of the pulse shaping filter in the transmitter, there are two types of data predistorters. The first type, exemplified by [24], [41], implements the pulse shaping filter using a radio frequency (RF) bandpass filter after the power amplifier. . . . The predistorter can be easily implemented as look-up tables (LUTs) that map the original input constellation points to the desired locations. Because of the small size of the input levels, this type of predistorters converges fast and requires very little memory. (Ding, at 7.)

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		The second type, exemplified by [26], [27], [20], considers the case where the pulse shaping filter is placed in the baseband, immediately after the data predistorter (see Fig. 4). . . . The approach taken by [26] uses a specific pulse shaping filter to generate discrete values at two or three equally spaced data points per symbol interval. Each data point is then predistorted by a memoryless predistorter and combined with adjacent data points to reduce the nonlinear distortion at the power amplifier output. (Ding, at 8.)  Figure 4: Block diagram of a data predistortion system with the pulse shaping filter placed in the baseband after the predistorter. (Ding, at Fig. 4.) The performance of the memory polynomial predistorter constructed using the indirect learning architecture is demonstrated through the following examples. These examples show that the same memory polynomial structure can effectively linearize several different nonlinear models with memory, thereby demonstrating the robustness of memory polynomial predistortion. (Ding, at 27.)

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		 Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.)  Figure 15: Wiener-Hammerstein model diagram. (Ding, at Fig. 15.) Example 3.4 Here, the nonlinearity to be compensated for is assumed to obey a Wiener-Hammerstein (W-H) model (see Fig. 15); i.e., an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency [2].

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		The LTI blocks before and after the memoryless nonlinearity, which are denoted by $H(z)$ and $G(z)$, respectively, are assumed to be $H(z) = \frac{1 + 0.5z^{-2}}{1 - 0.2z^{-1}},$ $G(z) = \frac{1 - 0.1z^{-2}}{1 - 0.4z^{-1}}.$ For the memoryless nonlinear portion of the W-H model, $w(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k v(n) v(n) ^{k-1},$ where $v(n)$ and $w(n)$ are, respectively, input and output of the memoryless nonlinear block. (Ding, at 27.) Fig. 20 shows the performance of our memory polynomial predistorter in linearizing such a power amplifier. With the memory polynomial predistorter ($Q = 2$, $K = 5$), there is a significant decrease in spectral regrowth, and the result is further improved when Q is increased to 5. (Ding, at 31.)

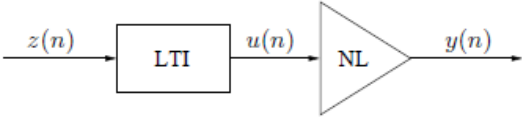
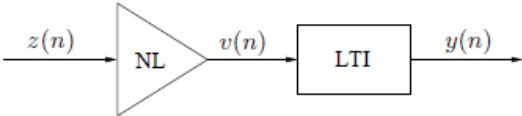
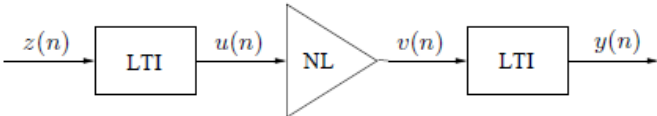
Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Figure 16: Effectiveness of predistortion in suppressing spectral regrowth when the power amplifier is modeled by a Wiener-Hammerstein system. (a) Output without predistortion; (b) Output with memoryless predistortion; (c) Output with memory polynomial predistortion ($Q = 2, K = 5$) (d) Original input. (c) and (d) almost coincide. (Ding, at Fig. 16.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
7[pre]	A predistorter for nonlinear wireless system, the predistorter comprising:	To the extent the preamble is limiting, Ding discloses and/or renders obvious a predistorter for a nonlinear wireless system. <i>See claim 1, supra, which is incorporated by reference herein.</i>
7[a]	a dynamic nonlinear predistorter module; and	Ding discloses and/or renders obvious a dynamic nonlinear predistorter module. <i>See claims 1–5 and claim elements 1[a] and 1[b], supra, which are incorporated by reference herein.</i>
7[b]	a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the dynamic nonlinear predistorter module is input to the static nonlinear predistorter module.	Ding discloses and/or renders obvious a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the dynamic nonlinear predistorter module is input to the static nonlinear predistorter module. <i>See claims 1–5 and claim elements 1[a] and 1[b], supra, which are incorporated by reference herein.</i>
8	The predistorter of claim 7 wherein the dynamic nonlinear predistorter is a finite impulse response-based memory effect predistorter and the static nonlinear predistorter is a look-up table-based memoryless predistorter.	Ding discloses and/or renders obvious the predistorter of claim 7 wherein the dynamic nonlinear predistorter is a finite impulse response-based memory effect predistorter and the static nonlinear predistorter is a look-up table-based memoryless predistorter. <i>See claims 1, 4 and 7, supra, which are incorporated by reference herein.</i>

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9	The predistorter of claim 7 wherein the dynamic nonlinear predistorter is a dynamic weak nonlinear predistorter and the static nonlinear predistorter is a static strong nonlinear predistorter.	Ding discloses and/or renders obvious the predistorter of claim 7 wherein the dynamic nonlinear predistorter is a dynamic weak nonlinear predistorter and the static nonlinear predistorter is a static strong nonlinear predistorter. <i>See</i> claims 1, 5 and 7, <i>supra</i> , which are incorporated by reference herein.
10	The predistorter of claim 9 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure embedded within a polynomial like series and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal.	Ding discloses and/or renders obvious the predistorter of claim 9 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure embedded within a polynomial like series and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal. <i>See</i> claims 1, 5–7 and 9, <i>supra</i> , which are incorporated by reference herein.
11[pre]	A predistorter for nonlinear wireless system, the predistorter comprising:	To the extent the preamble is limiting, Ding discloses and/or renders obvious a predistorter for nonlinear wireless system. <i>See</i> claim 1 and claim elements 1[pre] and 7[pre], <i>supra</i> , which are incorporated by reference herein.
11[a]	a static nonlinear predistorter module; and	Ding discloses and/or renders obvious a static nonlinear predistorter module.

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		See claims 1–5 and claim elements [1.a] and [1.b], <i>supra</i> , which are incorporated by reference herein.
11[b]	dynamic nonlinear predistorter module coupled to the static nonlinear predistorter module such that an output of the static nonlinear predistorter module is input to the dynamic nonlinear predistorter module.	Ding discloses and/or renders obvious a dynamic nonlinear predistorter module coupled to the static nonlinear predistorter module such that an output of the static nonlinear predistorter module is input to the dynamic nonlinear predistorter module. See claims 1–5 and claim elements [1.a] and [1.b], <i>supra</i> , which are incorporated by reference herein.
12	The predistorter of claim 11 wherein the dynamic nonlinear predistorter module is a finite impulse response-based memory effect predistorter module and the static nonlinear predistorter is a look-up table-based memoryless predistorter module.	Ding discloses and/or renders obvious the predistorter of claim 11 wherein the dynamic nonlinear predistorter module is a finite impulse response-based memory effect predistorter module and the static nonlinear predistorter is a look-up table-based memoryless predistorter module See claims 1, 4, and 11, <i>supra</i> , which are incorporated by reference herein.
13	The predistorter of claim 11 wherein the dynamic nonlinear predistorter module is a dynamic weak nonlinear predistorter module and the static nonlinear predistorter is a static strong nonlinear predistorter module.	Ding discloses and/or renders obvious the predistorter of claim 11 wherein the dynamic nonlinear predistorter module is a dynamic weak nonlinear predistorter module and the static nonlinear predistorter is a static strong nonlinear predistorter module. See claims 1, 5, 9, and 11, <i>supra</i> , which are incorporated by reference herein.

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14	The predistorter of claim 12 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal.	Ding discloses and/or renders obvious the predistorter of claim 12 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal. <i>See</i> claims 1, 6, 10 and 12, <i>supra</i>, which are incorporated by reference herein.
15[pre]	An augmented Wiener predistorter, the predistorter comprising:	To the extent the preamble is limiting, Ding discloses and/or renders obvious an augmented Wiener predistorter. <i>See</i> claims 1, 7, and 11, <i>supra</i>, which are incorporated by reference herein. <i>See also, e.g.:</i> The Wiener model is a linear time-invariant (LTI) system followed by a memoryless nonlinearity (NL) (see Fig. 6). The two subsystems are given by $u(n) = \sum_{l=0}^{L-1} a_l z(n-l),$ $y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k u(n) u(n) ^{k-1},$ where a_l are the impulse response values of the LTI block and b_k are the coefficients of the odd-order polynomial describing the memoryless nonlinearity. Substituting (13) into (14) gives

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		$y(n) = \sum_{\substack{k=1 \\ k \text{ odd}}}^K b_k \left[\sum_{l=0}^{L-1} a_l z(n-l) \right] \left \sum_{l=0}^{L-1} a_l z(n-l) \right ^{k-1}.$ The Wiener model was used by Clark et al. [11] to model the power amplifier with memory effects, where improvements in modeling accuracy were observed when the Wiener model replaces the memoryless polynomial model. (Ding, at 11.)  Figure 6: The Wiener Model.  Figure 7: The Hammerstein Model.  Figure 8: The Wiener-Hammerstein model.

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		(Ding, at Figs. 7–9.) The Wiener-Hammerstein (W-H) model (see Fig. 8) is an LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system. Such a configuration is commonly used for satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [2]. (Ding, at 13.) A Hammerstein predistorter is ideal for linearization of a Wiener system. The Wiener system can be either a power amplifier with memory effects [11] or the cascade of a pulse shaping filter and a memoryless power amplifier [25]. To construct a Hammerstein predistorter, the approach taken by [25] uses a gradient method to first identify the Wiener system and then find the Hammerstein predistorter as its inverse. An alternative approach is pursued here and [14], which generates the Hammerstein predistorter without first identifying the Wiener power amplifier by using the indirect learning architecture. (Ding, at 17.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
15[a]	a dynamic nonlinear first order predistorter module; and	Ding discloses and/or renders obvious a dynamic nonlinear first order predistorter module. <i>See</i> claims 1, 7, and 11 and claim elements 1[a], 7[a], and 11[b], <i>supra</i> , which are incorporated by reference herein.
15[b]	a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the dynamic nonlinear predistorter module is input to the static nonlinear predistorter module.	Ding discloses and/or renders obvious a static nonlinear predistorter module coupled to the dynamic nonlinear predistorter module such that an output of the dynamic nonlinear predistorter module is input to the static nonlinear predistorter module. <i>See</i> claims 1–3 and claim elements 1[b], 1[c], 7[b], and 11[a], <i>supra</i> , which are incorporated by reference herein.
16	The predistorter of claim 15 wherein the dynamic nonlinear predistorter is a finite impulse response-based memory effect predistorter and the static nonlinear predistorter is a look-up table-based memoryless predistorter.	Ding discloses and/or renders obvious the predistorter of claim 15 wherein the dynamic nonlinear predistorter is a finite impulse response-based memory effect predistorter and the static nonlinear predistorter is a look-up table-based memoryless predistorter. <i>See</i> claims 1, 4, 8, and 15, <i>supra</i> , which are incorporated by reference herein.
17	The predistorter of claim 15 wherein the dynamic nonlinear predistorter is a dynamic weak nonlinear predistorter and the static nonlinear predistorter is a static strong nonlinear predistorter.	Ding discloses and/or renders obvious the predistorter of claim 15 wherein the dynamic nonlinear predistorter is a dynamic weak nonlinear predistorter and the static nonlinear predistorter is a static strong nonlinear predistorter. <i>See</i> claims 1, 5, 9, 13, and 15, <i>supra</i> , which are incorporated by reference herein.

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
18	The predistorter of claim 17 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal.	Ding discloses and/or renders obvious the predistorter of claim 17 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal. <i>See</i> claims 1, 5, 6, 9, 10, 14 and 17, <i>supra</i>, which are incorporated by reference herein.
19[pre]	An augmented Hammerstein predistorter, the predistorter comprising:	To the extent the preamble is limiting, Ding discloses and/or renders obvious an augmented Hammerstein predistorter. <i>See</i> claims 1, 7, 11, and 15, <i>supra</i>, which are incorporated by reference herein. <i>See also, e.g.:</i> A Hammerstein predistorter is ideal for linearization of a Wiener system. The Wiener system can be either a power amplifier with memory effects [11] or the cascade of a pulse shaping filter and a memoryless power amplifier [25]. To construct a Hammerstein predistorter, the approach taken by [25] uses a gradient method to first identify the Wiener system and then find the Hammerstein predistorter as its inverse. An alternative approach is pursued here and [14], which generates the Hammerstein predistorter without first identifying the Wiener power amplifier by using the indirect learning architecture. (Ding, at 17.) In the training branch (see Fig. 10), the Hammerstein predistorter is given by:

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		$v(n) = \sum_{\substack{k=0 \\ k \text{ odd}}}^K c_k y(n) y(n) ^{k-1}$ $z(n) = \sum_{p=1}^P a_p z(n-p) + \sum_{q=0}^Q b_q v(n-q),$ [. . .] where $y(n)$ and $z(n)$ are, respectively, the input and output of the predistorter in the training branch, c_k in (25) are the coefficients of the nonlinear block of the predistorter, and a_p and b_q in (26) are the coefficients of the LTI portion of the predistorter. (Ding, at 17–18.) Figure 10: The indirect learning architecture for the Hammerstein predistorter. (Ding, at Fig. 10.) One of ordinary skill would find this limitation disclosed either expressly or inherently in the teachings of this reference and its incorporated disclosures taken as a whole, or in combination with

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
		the state of the art at the time of the alleged invention. To the extent this reference is not found to teach this element explicitly, implicitly, or inherently, the element would have been obvious to one of ordinary skill in the art based on this reference, common sense, ordinary creativity of one of ordinary skill in the art, and the state of the art. Additionally, it would have been obvious to combine this reference with one or more other prior art references identified in Defendants' Invalidity Contentions Cover Pleading, particularly, § II.B.2. Rather than repeat those disclosures here, they are incorporated by reference into this chart.
19[a]	a static nonlinear predistorter module; and	Ding discloses and/or renders obvious a static nonlinear predistorter module. <i>See</i> claims 1–3, and 15 and claim elements 1[b], 7[b], and 11[a], <i>supra</i> , which are incorporated by reference herein.
19[b]	a dynamic nonlinear first order predistorter module coupled to the static nonlinear predistorter module such that an output of the static nonlinear predistorter module is input to the dynamic nonlinear predistorter module.	Ding discloses and/or renders obvious a dynamic nonlinear first order predistorter module coupled to the static nonlinear predistorter module such that an output of the static nonlinear predistorter module is input to the dynamic nonlinear predistorter module. <i>See</i> claims 1–3, and 15 and claim elements 1[a], 1[c], 7[a], and 11[b], <i>supra</i> , which are incorporated by reference herein.
20	The predistorter of claim 19 wherein the dynamic nonlinear predistorter module is a finite impulse response-based memory effect predistorter module and the static nonlinear predistorter is a look-up table-based memoryless predistorter module.	Ding discloses and/or renders obvious the predistorter of claim 19 wherein the dynamic nonlinear predistorter module is a finite impulse response-based memory effect predistorter module and the static nonlinear predistorter is a look-up table-based memoryless predistorter module. <i>See</i> claim 1, 4, 8, 16, and 19, <i>supra</i> , which are incorporated by reference herein.

Claim No.	'561 Patent	Exemplary Evidence of Anticipation and/or Obviousness
21	The predistorter of claim 19 wherein the dynamic nonlinear predistorter module is a dynamic weak nonlinear predistorter module and the static nonlinear predistorter is a static strong nonlinear predistorter module.	Ding discloses and/or renders obvious the predistorter of claim 19 wherein the dynamic nonlinear predistorter module is a dynamic weak nonlinear predistorter module and the static nonlinear predistorter is a static strong nonlinear predistorter module. <i>See claim 1, 5, 9, 13, 17, and 19, supra, which are incorporated by reference herein.</i>
22	The predistorter of claim 21 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal.	Ding discloses and/or renders obvious the predistorter of claim 21 wherein the dynamic weak nonlinear predistorter is implemented as a finite impulse response filter-based multi-branch nonlinear structure and the static strong nonlinear predistorter includes two look-up tables, each look-up table depends on the magnitude of a current input signal. <i>See claim 1, 6, 10, 14, 18, and 21, supra, which are incorporated by reference herein.</i>