UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

Vervain, LLC, Plaintiff, v. Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corporation, Defendants.	Civil Action No. 1:24-cv-254 JURY TRIAL DEMANDED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Vervain, LLC ("Vervain") asserts the following claims for patent infringement against Defendants Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corporation (collectively "Defendants" or "Kingston"), and alleges as follows.

NATURE OF THE ACTION

1. This is a civil action for infringement under the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*

2. Vervain is the owner of all rights, title, and interest in U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; 10,950,300; 11,830,546; 11,854,612; 11,967,369; and 11,967,370 (collectively, the "Asserted Patents").

3. Defendants have infringed and continue to infringe one or more claims of Vervain's Asserted Patents by making, using, offering to sell, and selling within the United States, and importing into the United States, including in this District, certain flash memory products. Vervain seeks injunctive relief and monetary damages.

THE PARTIES

4. Plaintiff Vervain is a Texas limited liability company with its principal place of business located at 7424 Mason Dells Drive, Dallas, Texas 75230.

5. On information and belief, Defendant Kingston Technology Company, Inc. is a corporation organized under the laws of Delaware, with its principal place of business at 17600 Newhope Street, Fountain Valley, California 92708. Defendant Kingston Technology Company, Inc. can be served at the address for its agent for service, Tracy Chang, 17600 Newhope Street, Fountain Valley, California 92708.

6. On information and belief, Defendant Kingston Digital, Inc. is a corporation organized under the laws of Delaware, with its principal place of business at 17600 Newhope Street, Fountain Valley, California 92708. Defendant Kingston Digital, Inc. can be served at the address for its agent for service, Tracy Chang, 17600 Newhope Street, Fountain Valley, California 92708.

7. On information and belief, Defendant Kingston Technology Corporation is a corporation organized under the laws of California, with its principal place of business at 17600 Newhope Street, Fountain Valley, California 92708. Defendant Kingston Technology Corporation can be served at the address for its agent for service, Tracy Chang, 17600 Newhope Street, Fountain Valley, California 92708.

8. Kingston is "a world leader in memory products and technology solutions," and in the flash memory industry, it is the number-one third-party supplier of branded SSD modules.[1] It has been ranked as the 23rd largest private company in the U.S.[2]

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[1] Ex. G, https://www.businesswire.com/news/home/20231115145037/en/Kingston-Digital-Leads-Channel-SSD-Shipments-in-2022

[2] Ex. H, https://www.kingston.com/en/company/press/article/68066

9. Kingston sells a variety of flash memory products, including solid state drives (SSDs),[3] USB flash drives,[4] memory cards such as SD and microSD,[5] and embedded flash products like eMMC and UFS.[6] Kingston touts: "From SATA to NVMe, laptop to server, Kingston SSDs provide the speed and reliability you want."[7] To provide this speed and reliability, Kingston uses a variety of flash memory controllers from companies like Phison and Silicon Motion. These flash memory controllers manage the storage of data on Kingston's devices in a reliable, efficient way.[8]

10. Kingston and Phison work jointly on controller design, including in this district. Phison and Kingston have a "partnership" to make SSD controllers for Kingston products, and this partnership even "extends beyond SSDs." In November 2010, Phison and Kingston formed a joint venture to provide flash memory solutions in the mobile, Internet of Things, and embedded markets.[9]

11. Kingston and Phison, which act together in product design, marketing, manufacturing, and sales, have operated as agents of and for one another and have otherwise acted vicariously for each other as elements of the same business group and/or enterprise. They work together in concern and in orchestrated fashion, subject to agreements closer than arms' length, in order to implement a distribution channel of infringing products in the United States.

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[3] Ex. I, https://www.kingston.com/en/ssd
[4] Ex. J, https://www.kingston.com/en/usb-flash-drives
[5] Ex. K, https://www.kingston.com/en/memory-cards
[6] Ex. L, https://www.kingston.com/en/solutions/embedded-and-industrial
[7] Ex. I, https://www.kingston.com/en/ssd
[8] Ex. M, https://www.kingston.com/en/ssd/gaming/kingston-fury-renegade-nvme-m2-ssd ("By leveraging the latest Gen 4x4 NVMe controller and 3D TLC NAND, Kingston FURY Renegade SSD offers blazing speeds up to 7,300/7,000MB/s read/write and up to 1,000,000 IOPS for amazing consistency and exceptional gaming experience.")
[9] Ex. N, https://www.phison.com/en/company/newsroom/press-releases/general/530-phison-and-kingston-collaborate-on-nvme-ssd-controller-to-accelerate-into-the-next-ssd-era-2

12. One of the key ways that Kingston's flash memory controllers manage the storage of data is through the use of SLC and MLC flash. For example, Phison makes many of the controllers that Kingston uses. As Imran Hirani, Phison's Director of Product Architecture, explained, the use of QLC (quad-level-cell) flash memory, a type of multi-level-cell ("MLC") flash memory, in combination with SLC (single-level-cell) memory is a key part of providing high capacity, high speed, and high endurance. "QLC NAND addresses the increased capacity requirement but comes with tradeoffs of slower throughput and lower endurance. One way to address slower throughput and lower endurance of QLC is to add a small SLC cache on the drive. Data from the host is written to the SLC cache first, and then data is moved to QLC."[10]

13. On information and belief, Mr. Hirani, who resides in Cedar Park, Texas, designs many of the controllers Kingston uses.[11]

14. Kingston has over $16 billion in annual sales, and over 2,900 employees worldwide.[12]

15. Kingston sells its storage products not only to end users and customers throughout the U.S., but also to major computer and electronics manufacturers to provide the storage that manufacturers need for their products. Kingston states: "From big data, to laptops and PCs, to IoT-based devices like smart and wearable technology, to design-in and contract manufacturing, Kingston helps deliver the solutions used to live, work and play. The world's largest PC makers

[10] Ex. O, (https://phisonblog.com/qlc-nand-for-consumer-ssds-2/)
[11] Ex. P, (Imran Hirani LinkedIn profile, https://www.linkedin.com/in/imran-hirani-721aa23/).
[12] Ex. Q, https://media.kingston.com/kingston/company/pdf/Kingston-Technology-2022-GRI.pdf at 11.

and cloud-hosting companies depend on Kingston for their manufacturing needs, and our passion fuels the technology the world uses every day."[13]

16. Kingston operates and owns the kingston.com website, and markets, offers, distributes, and provides technical support for its flash memory products throughout the United States including in this District.

17. Kingston develops, designs, manufactures, distributes, markets, offers to sell, or sells infringing products or services within the United States, including in this District, and otherwise purposefully directs infringing activities to this District in connection with its Austin, Texas sales staff; its kingston.com website; and its other places of business in Texas and the rest of the United States.

18. Kingston has employees in the state of Texas and this District–for example, Chuck Lantz, an Enterprise Field Account Manager based in Austin, Texas. Mr. Lantz's "[p]rimary responsibility is to identify the prpoblems customers are facing and, most importantly, to recommend viable solutions."[14] On information and belief, Kingston directs Mr. Lantz to work in the Western District of Texas in order to serve Kingston's local customers in the Austin area, and to distribute products and product samples to Kingston's local customers.

19. Kingston has maintained an office at One Old Town Square, Round Rock, TX, in the Western District of Texas, and filed tax returns for its property in Texas.[15] In prior litigation, Kingston has declined to dispute that venue was proper in the Western District of Texas.[16]

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[13] Ex. Q, https://media.kingston.com/kingston/company/pdf/Kingston-Technology-2022-GRI.pdf at 10.
[14] Ex. R, (https://www.linkedin.com/in/chuck-lantz-a581b811/).
[15] Ex. S, (Sonrai WDTX Docket Nos. 37-24, 37-25, 37-26).
[16] Ex. T, (Sonrai WDTX Docket No. 38 at 1, n.1).

20. Defendants have been and are acting in concert, and are otherwise liable jointly, severally, or otherwise for relief related to or arising out of the same transaction, occurrence, or series of transactions or occurrences related to the making, using, selling, offering for sale, or otherwise distributing the flash memory products in this District.

21. In addition, this action involves questions of law and fact that are common to all Defendants. For example, Defendants are making, using, offering for sale, selling, or otherwise distributing at least some of the same flash memory products in this District.

JURISDICTION AND VENUE

22. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction over the matters asserted in this Complaint under 28 U.S.C. §§ 1331 and 1338(a) and 35 U.S.C. §§ 271 *et seq*.

23. This Court has personal jurisdiction over Kingston in accordance with the Due Process Clause of the United States Constitution and the Texas Long Arm Statute (*see* Tex. Civ. Prac. & Rem. Code §§17.041 *et seq*.) because, among other things, (i) Kingston has done and continues to do business in Texas, (ii) Kingston "recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state," Tex. Civ. Prac. & Rem. Code § 17.042(3), and (iii) Kingston has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State and this District. Such acts of infringement include making, using, offering to sell, selling, and/or importing Accused Products in this State and this District. Kingston places its Accused Products into the stream of commerce through established distribution channels with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in

standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

24. Kingston, directly and through agents, regularly conducts, solicits, and transacts business in this District and elsewhere in Texas, including through its kingston.com website. For example, Defendants employ sales and marketing employees that regularly offer to sell, sell, or otherwise distribute flash memory products in this District and elsewhere in Texas.

25. In particular, Kingston has committed and continues to commit acts of infringement in violation of 35 U.S.C. § 271, and has made, used, marketed, distributed, offered for sale, and sold infringing products in Texas, including in this District, and engaged in infringing conduct within and directed at or from this District. The infringing flash memory products have been and continue to be distributed to and used in this District. Kingston's acts cause injury to Vervain, including injury suffered within this District.

26. Venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendants have committed acts of infringement in this District and have a regular and established place of business in this District.

27. In particular, Defendants each have regular and established places of business in this District located at the workplace of Chuck Lantz, and at their offices at located at One Old Town Square, Round Rock, TX. Furthermore, Defendants are registered to do business in Texas. Upon information and belief, Defendants instruct Mr. Lantz to work in the Western District of Texas so that he can easily meet with customers in the field, and Defendants distribute products and samples through Mr. Lantz.

28. Upon information and belief, Kingston Digital, Inc., and Kingston Technology Corporation are wholly-owned subsidiaries of Kingston Technology Company, Inc.

VERVAIN'S ASSERTED PATENTS

29. U.S. Patent No. 8,891,298 (the "'298 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 18, 2014. A true and correct copy of the '298 patent is attached as Exhibit A to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '298 patent, with the full and exclusive right to bring suit to enforce the '298 patent, including the right to recover for past infringement. The '298 patent is valid and enforceable under United States patent laws.

30. U.S. Patent No. 9,196,385 (the "'385 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 24, 2015. A true and correct copy of the '385 patent is attached as Exhibit B to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '385 patent, with the full and exclusive right to bring suit to enforce the '385 patent, including the right to recover for past infringement. The '385 patent is valid and enforceable under United States patent laws.

31. U.S. Patent No. 9,997,240 (the "'240 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on June 12, 2018. A true and correct copy of the '240 patent is attached as Exhibit C to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '240 patent, with the full and exclusive right to bring suit to enforce the '240 patent, including the right to recover for past infringement. The '240 patent is valid and enforceable under United States patent laws.

32. U.S. Patent No. 10,950,300 (the "'300 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on March 16, 2021. A true and correct copy of the '300 patent is attached as Exhibit D to this Complaint. Vervain is the owner of all rights, title,

and interest in and to the ’300 patent, with the full and exclusive right to bring suit to enforce the ’300 patent, including the right to recover for past infringement. The ’300 patent is valid and enforceable under United States patent laws.

33. U.S. Patent No. 11,830,546 (the “’546 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on November 28, 2023. A true and correct copy of the ’546 patent is attached as Exhibit E to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’546 patent, with the full and exclusive right to bring suit to enforce the ’546 patent, including the right to recover for past infringement. The ’546 patent is valid and enforceable under United States patent laws.

34. U.S. Patent No. 11,854,612 (the “’612 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on December 26, 2023. A true and correct copy of the ’612 patent is attached as Exhibit F to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’612 patent, with the full and exclusive right to bring suit to enforce the ’612 patent, including the right to recover for past infringement. The ’612 patent is valid and enforceable under United States patent laws.

35. U.S. Patent No. 11,967,369 (the “’369 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on April 23, 2024. A true and correct copy of the ’369 patent is attached as Exhibit ZZ to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’369 patent, with the full and exclusive right to bring suit to enforce the ’369 patent, including the right to recover for past infringement. The ’369 patent is valid and enforceable under United States patent laws.

36. U.S. Patent No. 11,967,370 (the “’370 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on April 23, 2024. A true and correct copy of the ’370

patent is attached as Exhibit AAA to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’370 patent, with the full and exclusive right to bring suit to enforce the ’370 patent, including the right to recover for past infringement. The ’370 patent is valid and enforceable under United States patent laws.

37. In addition, Vervain has pending continuations to the patents-in-suit. . Vervain is the owner of all rights, title, and interest in and to these patent applications.

38. G.R. Mohan Rao is the sole inventor of the Asserted Patents.

39. Dr. Rao is the inventor of approximately 113 U.S. patents and the author of at least 15 technical publications spanning several decades.

40. Dr. Rao has been an innovator in the semiconductor industry since the 1960s. After receiving his Ph.D. in physics with a specialization in electronics in September 1968 from Andhra University in Waltair, India, near the village where he grew up, Dr. Rao traveled to the United States to attend a graduate program in physics at the University of Cincinnati, fulfilling his lifelong dream to study in the United States.

41. Shortly after beginning his studies at the University of Cincinnati, Dr. Rao found a bulletin indicating that Prof. William Carr of Southern Methodist University (SMU) was looking for a graduate assistant for his work on MOS transistors. Dr. Rao called Prof. Carr about the opportunity, and by December 1968, after completing the fall semester at the University of Cincinnati, Dr. Rao had received the assistantship with Prof. Carr, moved to Dallas, Texas, and enrolled in a Ph.D. program at SMU in electrical engineering.

42. At the laboratory at SMU, Dr. Rao was able to build MOS devices from scratch. In the 1969-1970 timespan, while attending SMU, Dr. Rao also worked in the SMU laboratory with Jack Kilby of Texas Instruments, a pioneering electrical engineer who would later receive a

Nobel Prize for his work. In early 1972, Mr. Kilby set up an interview for Dr. Rao at Texas Instruments' Houston facility, then the home of Texas Instruments' MOS-related work.

43. Dr. Rao began working for Texas Instruments in June 1972. He would go on to work for the company for 22 years, until 1994. Dr. Rao rose through the ranks at Texas Instruments, starting in an Engineer position and ascending to the position of Senior Fellow—one of 12 out of approximately 20,000 engineers at the company at the time. He then moved into a management position, starting as a Vice President in 1983 and becoming a Senior Vice President in 1985.

44. Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. From the late 1970s through the mid-1980s, he worked on and/or managed Texas Instruments': (1) 64Kb RAM, in a project management capacity as a Senior Member of Technical Staff; (2) 256Kb RAM, in a project management capacity as a Fellow; (3) 1Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects; and (4) 4Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects. At Texas Instruments, Dr. Rao also worked on projects involving EEPROM, SRAM, and microcontrollers. In total, Dr. Rao received approximately 35 U.S. patents during his time at Texas Instruments.

45. Some of Dr. Rao's work for Texas Instruments is featured in the Smithsonian Institution, in the Texas Instruments Collection.[17] For example, the Smithsonian Institution has a display of Texas Instruments' experimental 1-megabit CMOS DRAM with one-micron feature size, produced in April 1985 under Dr. Rao's leadership.

[17] http://smithsonianchips.si.edu/texas/t_360.htm; http://smithsonianchips.si.edu/texas/wafer.htm.

46. After his time at Texas Instruments, Dr. Rao joined Cirrus Logic in 1994. Although Cirrus Logic was a California company, Dr. Rao coordinated a team in the Dallas area. His work focused on a major project involving integration of a graphics controller and memory. During his time at Cirrus Logic, Dr. Rao received approximately 22 U.S. patents relating to his work on integrated graphics controllers and memory. Dr. Rao left Cirrus Logic in the summer of 1996.

47. Later in 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip.

48. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years. For example, Dr. Rao worked to improve non-volatile memories that are used for long term storage of data after the power is turned off, and how to reduce the power consumption of those devices.

49. In non-volatile memories, there are two types of storage cells: single-level cells (SLCs) that store one bit of information, and multi-level cells (MLCs) that store multiple bits of information. SLCs are faster, more reliable, and have a longer life. MLCs are less expensive and can store more data in less space with less power consumption. While working to improve these non-volatile memories, Dr. Rao developed inventions that combine the long life and high-performance of SLCs with the more cost-effective MLCs. The result is the best of both types of cells – longer life and better performance at less cost. By using the MLCs as the default storage, the cheaper, more reliable MLCs are used for the bulk of the data storage. Meanwhile, the SLCs are used for the data that needs it the most.

50. The claims of the Asserted Patents are directed to patent-eligible, non-abstract ideas. They address, among other things, specific improvements for controlling non-volatile memory modules. The claims are particularly useful for flash memory products or other memory devices that use a combination of SLCs and multi-level cells MLCs. If, for example, a range of addresses in a MLC memory module fails a data integrity test, the range of addresses may be mapped to a new range of addresses in a SLC memory module. Also, if a block in the MLC module is used frequently, the block may be transferred to the SLC module. By doing so, the reliability and life of the flash memory is increased.

51. Vervain's Asserted Patents claim, among other things, a specific implementation of a solution to a problem in the design and fabrication of flash memories. For example, the patents identify numerous specific advantages that Vervain's claimed techniques provide compared to traditional forms of flash memories. *See, e.g.*, Ex. A, '298 patent at 1:25-32; Ex. B, '385 patent at 1:28-35; Ex. C, '240 patent at 1:40-47; Ex. D, '300 patent at 1:44-51. Further, the claimed technologies cannot be performed as mental steps by a human, nor do they represent the application of a generic computer to any well-known method of organizing human behavior.

52. The Asserted Patents claim inventive concepts that are significantly more than any patent-ineligible, abstract idea. In particular, the claimed technologies, including individual limitations as well as ordered combinations of limitations, were not well-understood, routine, or conventional, and cover multiple advantages, and combinations of advantages, that were not well-understood, routine, or conventional. *See, e.g.*, Ex. A, '298 patent at 5:24-40, 6:24-35; Ex. B, '385 patent at 5:28-44, 6:28-39; Ex. C, '240 patent at 5:43-59, 6:46-58; Ex. D, '300 patent at 5:51-67, 6:53-65.

KINGSTON'S INFRINGING PRODUCTS AND ACTIVITIES

53. Kingston is a global manufacturer and supplier of memory products, including non-volatile memory products. Kingston's flash memory products, such as solid state drives (SSDs),[18] USB flash drives,[19] memory cards such as SD and microSD,[20] and embedded flash products like eMMC and UFS,[21] are managed by a controller chip. Many of Kingston's controller chips are made by companies like Phison and Silicon Motion. For example, the exemplary products listed below have the controllers listed below:

Drive	**Controller[22]**
XS2000 External Solid State Drive (SSD)	Silicon Motion SM2320[23]
DC1500M U.2 Enterprise SSD	Silicon Motion SM2270[24]
DC1000B M.2 NVMe SSD	Phison PS5012-E12[25]
NV2	Phison E21T or Silicon Motion SM2267XT
NV1	Phison 13T or Silicon Motion SM2263XT
HyperX Savage	Phison S10

[18] Ex. I, https://www.kingston.com/en/ssd
[19] Ex. J, https://www.kingston.com/en/usb-flash-drives
[20] Ex. K, https://www.kingston.com/en/memory-cards
[21] Ex. L, https://www.kingston.com/en/solutions/embedded-and-industrial
[22] Based on Ex. U, https://www.techpowerup.com/ssd-specs/#kingston, or Ex. V, https://www.johnnylucky.org/data-storage/ssd-database.html, pages 10, 21, unless otherwise indicated.
[23] Ex. W, https://www.thessdreview.com/hardware/portable-ssds/kingston-xs2000-1tb-portable-ssd-review/
[24] Ex. X, https://www.kitguru.net/components/ssd-drives/simon-crisp/kingston-dc1500m-3-84tb-ssd-review/all/1/
[25] Ex. Y, https://www.kitguru.net/components/ssd-drives/simon-crisp/kingston-dc1000b-480gb-ssd-review/all/1/

A400	Phison S11
A1000	Phison E8
A2000	Silicon Motion SM2263EN
DC500M	Phison E12
DC500R	Phison S12
FURY Renegade	Phison E18
KC400	Phison S10
KC600	Silicon Motion SM2259H
KC3000	Phison E18
KC2500	Silicon Motion SM2262EN
A2000	Silicon Motion SM2263
KC2000	Silicon Motion SM2262EN
KC1000	Phison PS5007-E7

54. Kingston designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes, and provides support for, flash memory products, including the exemplary products listed above, as well as other SSDs, flash drives, memory cards, embedded flash products, or other flash products that have the same or similar structures, features, or functionalities as the aforementioned products ("Accused Products").

55. The Accused Products are integrated into devices made, used, offered for sale, sold, imported, supplied, or otherwise distributed in the United States by among others, Kingston, Kingston's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), foundry suppliers, distributors, retailers, and other third parties.

Kingston's Accused Products are essential, non-trivial components of the products into which they are integrated.

56. Kingston also conducts research, development, and testing of Accused Products in the United States.

57. Kingston maintains a website that advertised and continues to advertise the Accused Products, including identifying the applications for which they can be used and specifications for the Accused Products.

58. Kingston's development, sales, marketing, and manufacturing activities in the United States, including within this District, directly contributed to Kingston's net revenue in the United States.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,891,298

59. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

60. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '298 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

61. The Accused Products meet all the limitations of at least claim 1 of the '298 patent. Specifically, claim 1 of the '298 patent recites:

A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:

a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

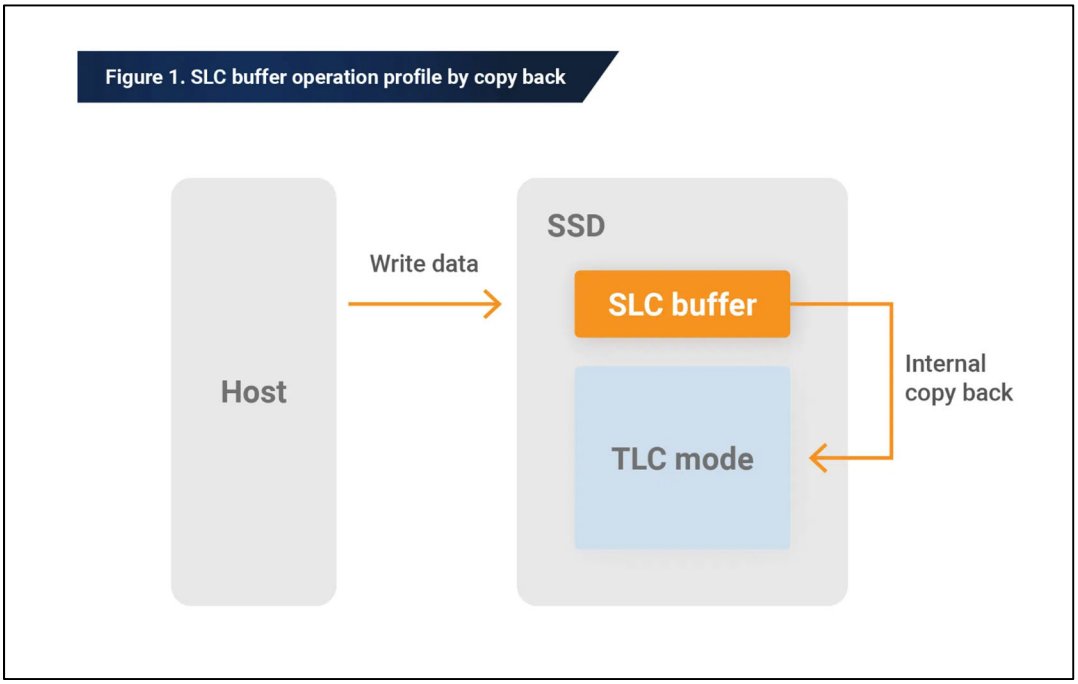
c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

62. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, Kingston's SSDs and other flash storage products are all systems for storing data.

Ex. I, https://www.kingston.com/en/ssd

63. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, Kingston's Phison-based products use MLC (e.g. "TLC mode") memory as part of an SLC buffering system, and Kingston's Silicon Motion-based products use "Direct-to-TLC" and "SLC Caching" systems that include MLC memory.



Ex. Z, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

> Leveraging Silicon Motion's proprietary NANDXtend™ error-correcting code (ECC) technology, the SM2259 and SM2259XT enhance the endurance and retention of 3D NAND. Besides, SM2259 and SM2259XT include such enterprise features such as end-to-end data path protection and SRAM ECC capabilities to ensure the data integrity and reliability. SM2259 and SM2259XT also features advanced Direct-to-TLC and SLC Caching algorithms for optimal sustained performance with TLC and QLC NAND.

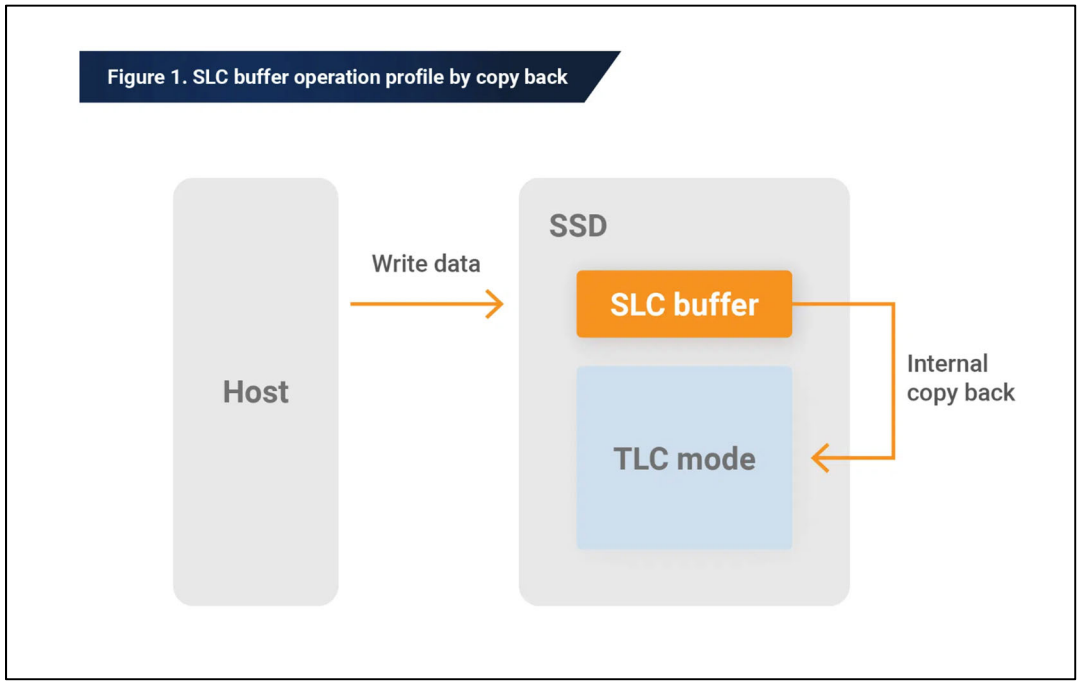
Ex. AA, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf

64. The flash memory uses individually erasable blocks. For example, Phison explains that individual blocks are erased, and that this is an "intrinsic characteristic of NAND device physics":

> A flash memory cell is composed of pages, and pages form a block. Due to the intrinsic characteristic of NAND device physics, the flash cell allows data to be programmed on a page level but only erased on a block level. This inconsistency between program and erase tasks is the major impact on SSD endurance.

Ex. BB, (https://phisonblog.com/ssd-garbage-collection/)

65. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. The SLC caching systems, for example, used by the Accused Products use individually erasable SLC blocks.



Ex. Z, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

> Leveraging Silicon Motion's proprietary NANDXtend™ error-correcting code (ECC) technology, the SM2259 and SM2259XT enhance the endurance and retention of 3D NAND. Besides, SM2259 and SM2259XT include such enterprise features such as end-to-end data path protection and SRAM ECC capabilities to ensure the data integrity and reliability. SM2259 and SM2259XT also features advanced Direct-to-TLC and SLC Caching algorithms for optimal sustained performance with TLC and QLC NAND.

Ex. AA, https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf

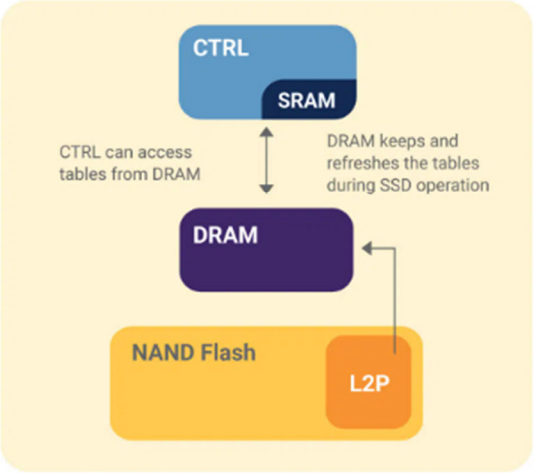
66. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. For example, the exemplary products listed in the table in Paragraph 51 above include the listed controllers.

67. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, Phison and Silicon Motion controllers in the Accused Products uses a mapping table such as an L2P (logical-to-physical) table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

68. Phison controllers use an L2P table:

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

Figure 2. Cache operating mechanism of SSD with DRAM



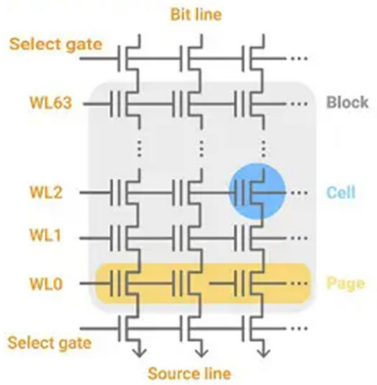
Ex. CC, https://phisonblog.com/host-memory-buffer-2/

69. In Phison controllers, a minimum quanta of addresses—such as a page—is used:

NAND Flash is a non-volatile memory composed of millions of floating-gate transistors that capture electrons within the gate. These floating-gate transistors can be thought of as memory cells. When millions of memory cells are connected, they form an array. Each array consists of blocks and each block contains numbers of pages.

Fig.1 gives a brief illustration of a NAND array f schematic.

Figure 1. NAND composition in transistor level



Ex. DD, https://phisonblog.com/ensuring-data-correctness-with-phisons-guaranteedflush-2/

70. Silicon Motion controllers provide logical-to-physical translation:

DRAM cache with data redundancy:
no data loss during data transfers
Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

Ex. EE, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf

71. Silicon Motion's address map may take the form of a table:

Block translation in Markers table

In the last step of each case, it's necessary to arrange logical blocks in the Markers table, and in the case of these controllers, this step is quite simple and looks similar for every model of these controllers.

Structures of Service area

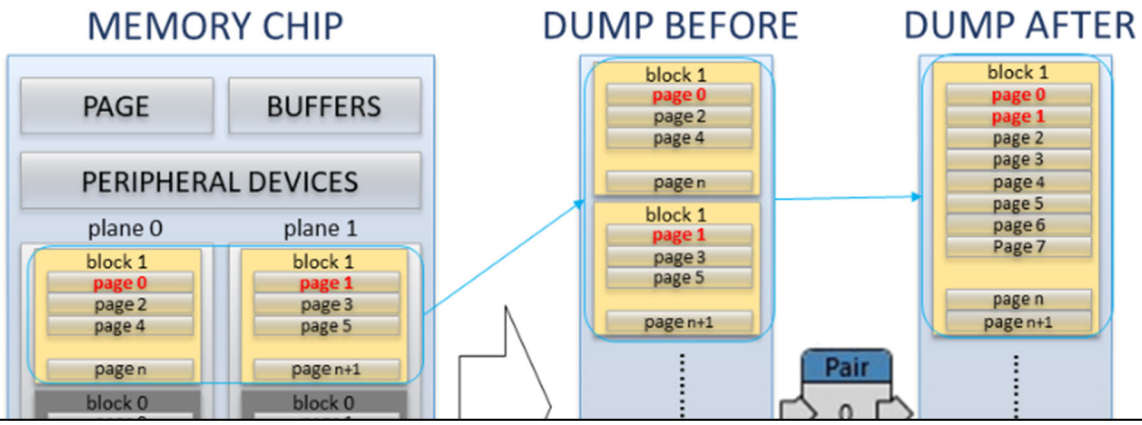
SiliconMotion controllers have exactly the same structure of the Service area.

Ex. FF, https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery

72. In Silicon Motion's address map, a minimum quanta of addresses—such as a page—is mapped to physical locations:

Multi-Plane Page allocation

Parallel allocation of physical pages is the most popular mode used by the controllers to speed up I/O operations. While using this mode controller is allocating physical pages parallelly to the planes of NAND memory. This mode is used by the majority of NAND controllers.



Ex. FF, https://support.rusolut.com/portal/en/kb/articles/silicon-motion-data-recovery

73. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, Kingston's products include Phison and Silicon Motion controllers that incorporate defect and error management technology, and use a variety of tests to determine that there is a data integrity problem.

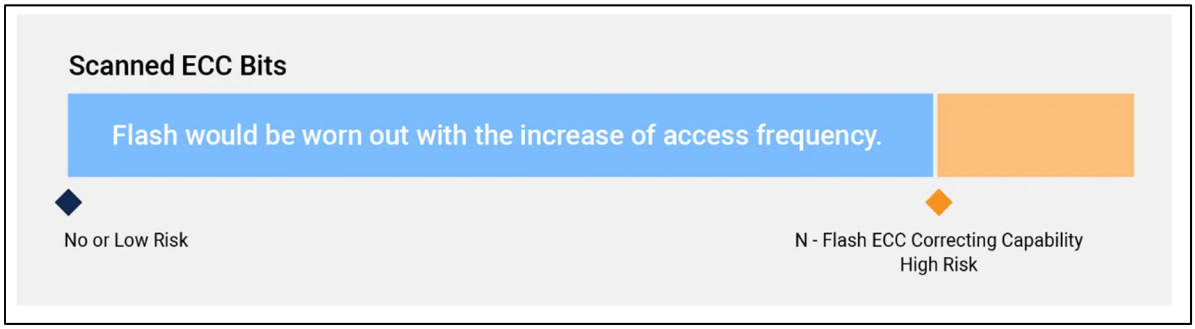
74. Phison controllers use a variety of data integrity tests to determine when there is a data integrity problem:

Phison's SmartRefresh™ technology

To protect the data stored in an SSD, Phison developed a proprietary technology called SmartRefresh™ that uses two primary methodologies:

1. Dynamic Error Bit Monitoring (DEBM)
2. Read Retry

"Phison's embedded firmware runs in the background to check the error bit of each block. Once there is a block fail within the criteria set by our firmware (i.e., the number of error bits is over the threshold decided in advance), the firmware performs specific actions on this failed block to guarantee the integrity of user data."



Ex. GG, (https://phisonblog.com/phisons-smartrefresh-2/)

Advanced Features:

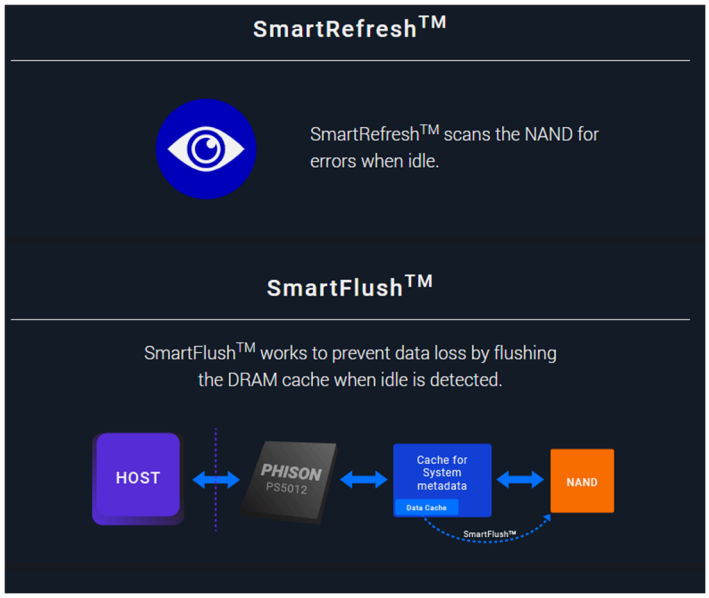
- End-to-end data path protection
- SmartECC RAID data protection
- P-fail protection with SmartFlush and GuaranteedFlush technology
- Advanced read disturb management with SmartRefresh technology
- Advanced global wear-leveling

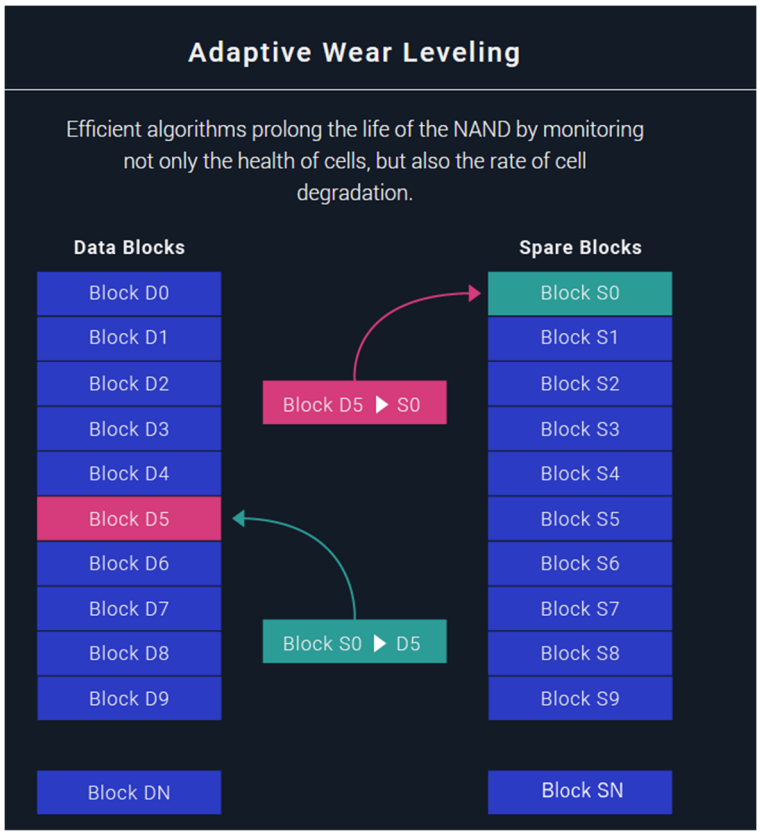
Ex. HH, (https://www.techpowerup.com/203889/phison-announces-quad-core-ps3110-sata-iii-ssd-controller)

75. Upon a data integrity failure, Phison controllers remap degraded data to the next available location:

"the firmware performs specific actions on this failed block to guarantee the integrity of user data."

Ex. GG, (https://phisonblog.com/phisons-smartrefresh-2/)





Ex. II, (https://www.phison.com/en/technologies/ftl)

76. In particular, Phison controllers move data from MLC to SLC as part of the relocation above as part of Phison's SLC caching technology, where writes are made to SLC before being moved to MLC:

> Consumer workloads also write over a limited LBA range. W riting the data to SLC first ensures that only the final valid copy of the data is written to the QLC. This limits the writes to QLC, enabling QLC NAND to be used for consumer drive, despite its lower endurance.
>
> SLC cache is used in the consumer TLC drive today. It takes advantage of customer workloads to address the similar limitation of lower speed and limited endurance on TLC NAND. QLC based drives provide 33% higher capacity as compared to TLC NAND. This lowers the cost of the drive.

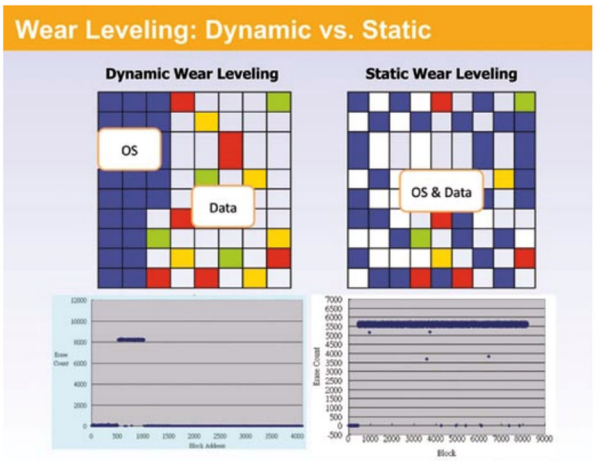
Ex. O, (https://phisonblog.com/qlc-nand-for-consumer-ssds-2/)

77. For example, Phison's articles describing its storage devices discuss "replacing MLC to SLC":

With process advances, NAND Flash can support the development of more cost-competitive solutions but the reliability of NAND Flash is getting worse. In terms of market response, customers won't just accept inferior quality products because of the price drop. On the contrary, they demand products at the same level but with the same or better reliability and performance. Therefore, the focus of attention has turned to the Flash controller to address this problem.

Basically, significant problems of reliability are caused by things like replacing MLC to SLC, increasing 2 bits/cell to 3 bits/cell, reducing the Erase Cycle number from 100K down to 10K, and cutting Data Retention times through the advances of NAND Flash. These issues can be solved within a re-designed and robust controller.

For example, the error rates of NAND Flash are increasing



Ex. JJ, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

78. Silicon Motion controllers use a variety of data integrity tests to determine when there is a data integrity problem:

Full end-to-end data path protection: no bit errors sent to host

Conventional SSDs may employ error detection and correction circuitry at the far ends of the data path: at the front-end host interface and at the back-end

NAND interface. This omits an important gap at the internal SRAM and/or DRAM transfer buffers, and other circuit paths. Data errors that occur between the NAND interface and the host, such as soft error bits, are often extremely difficult to identify and duplicate.

While conventional SSDs may have some internal error detection circuitry, the new PCIe FerriSSD storage solutions incorporate full data recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path.

The PCIe FerriSSD data recovery algorithm can effectively detect any error in the SSD data path, including hardware errors, firmware errors and memory errors arising in SRAM, DRAM or NAND. The PCIe FerriSSD implements an additional redundant back-up in NAND – the SMI Ferri Group Page Raid – which reinforces the protection against the risk of uncorrectable error in the NAND storage medium.

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf)

IntelligentScan & DataRefresh: proactive data loss prevention measures

The features described above protect against the risk of data loss or error in data-transfer operations. The PCIe FerriSSD also incorporates sophisticated functions which ensure the integrity of data in storage.

The IntelligentScan & DataRefresh function achieves this by identifying at-risk memory cells and refreshing the data stored in them. The risk of loss of stored data increases as:

- **the aggregate number of Program / Erase (P/E) cycles increases**
- **the ambient temperature rises**

In either condition, the operation of the IntelligentScan & DataRefresh function becomes increasingly important.

Read disturbance

Performing an excessive number of read cycles from a cell, can cause unintended over-charging of adjacent cells, leading to unrecoverable bit errors, a phenomenon known as Read disturbance. FerriSSD products avoid potential Read disturbance errors by performing periodic IntelligentScan & DataRefresh operations on NAND blocks that undergo repetitive Read cycles. The PCIe FerriSSD firmware – an advanced 4th generation algorithm (IntelligentScan) – automatically manages DataRefresh cycles and processing time to minimize data loss due to the impact of intensive Read operations on the NAND Flash storage medium.

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf)

The IntelligentScan function is responsible for checking whether the stored charge has declined below its threshold value. If it has, it reads out the data bit and rewrites it via the ECC engine, and DataRefresh recharges the cell to restore the NAND cell's voltage to the correct level.

Ex. KK, (https://www.siliconmotion.com/download/3g1/a/FerriSSD_Gaming_WP_EN.pdf)

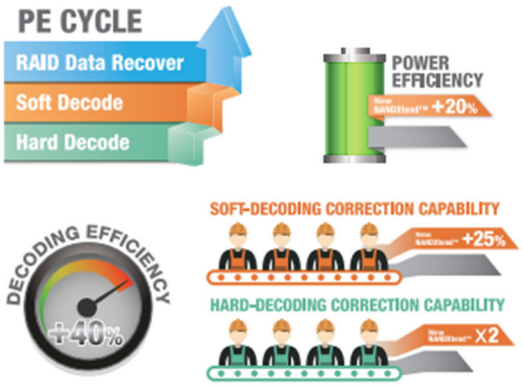
With Intelligent Scan, FerriSSD's firmware will respond to changing usage conditions to intelligently determine where, when and how frequently to scan the SSD. The scan will be triggered during idle time, based on preset thresholds and self-adopting algorithms, to determine which cells should be scanned according to severity priority (such as temperature readings, read counts, and other factors).

When IntelligentScan identifies overstressed cells, SMI's proprietary DataRefresh function will be activated automatically to recharge, repair or retire the cell block accordingly. As a result of the combination of Intelligent Scan and Data Refresh, FerriSSD can prolong its usage life much beyond typical NAND specifications.

Ex. LL, (https://www.siliconmotion.com/download/3TY/a/FerriSSD_BGASSD_WP_EN.pdf)

NANDXtend™ Technology

The SM2259 and SM2259XT employs the company's proprietary NANDXtend™ ECC technology consisting of LDPC hard and soft decoding as well as RAID protection that together enhance the P/E cycles of 3D NAND - extending the SSD lifespan and ensuring data integrity. The new generation NANDXtend™ includes 2KB LDPC engine with advanced firmware algorithm delivers higher power efficiency, decoding efficiency and correction capability to maintain consistent data throughout and provide a better user experience, even as error bits increase throughout the product lifecycle of NAND Flash.



Ex. AA, (https://www.siliconmotion.com/download/q/a/SM2259_XT_PB_EN_201910.pdf)

Silicon Motion's SM689 and SM681 FerriSSDs supports enhanced reliability and data integrity features for use in demanding automotive, commercial, enterprise and industrial applications. Its set of features includes:

- End-to-end data path protection, which applies error correction code (ECC) to the SSD's SRAM and DRAM buffers as well as to the primary NAND Flash memory array
- DRAM data cache to ensure data programming and enable data redundancy, without delaying host processor operations
- Hybrid Zone which enables a single disk to be partitioned into single-level cell (SLC) and multi-level cell/three-level cell (MLC/TLC) zones, enabling faster access speeds and data retention
- Intelligent Scan/DataRefresh protects against the higher data loss from operating at high temperatures
- NANDXtend™ technology incorporating Silicon Motion's proprietary 4th generation high-performance LDPC ECC engine with RAID, ensuring better data integrity even in extreme physical environments

Ex. MM, (https://www.prnewswire.com/news-releases/silicon-motion-announces-worlds-first-pcie-nvme-single-chip-ssds-with-enterprise-grade-data-protection-features-300604092.html)

End to End Data Path Protection

Silicon Motion's SSD controller solutions incorporate full data error detection with recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path. The data recovery algorithm can effectively detect any error in the SSD data path, including hardware (i.e. ASIC) errors, firmware errors, and memory errors arising in SRAM, DRAM, or NAND.

Ex. NN, (https://www.siliconmotion.com/products/client/detail)

79. Upon a data integrity failure, Silicon Motion controllers remap (or "refresh") the data to the next available location:

The IntelligentScan & DataRefresh function achieves this by identifying at-risk memory cells and refreshing the data stored in them. The risk of loss of stored data increases as:

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf).

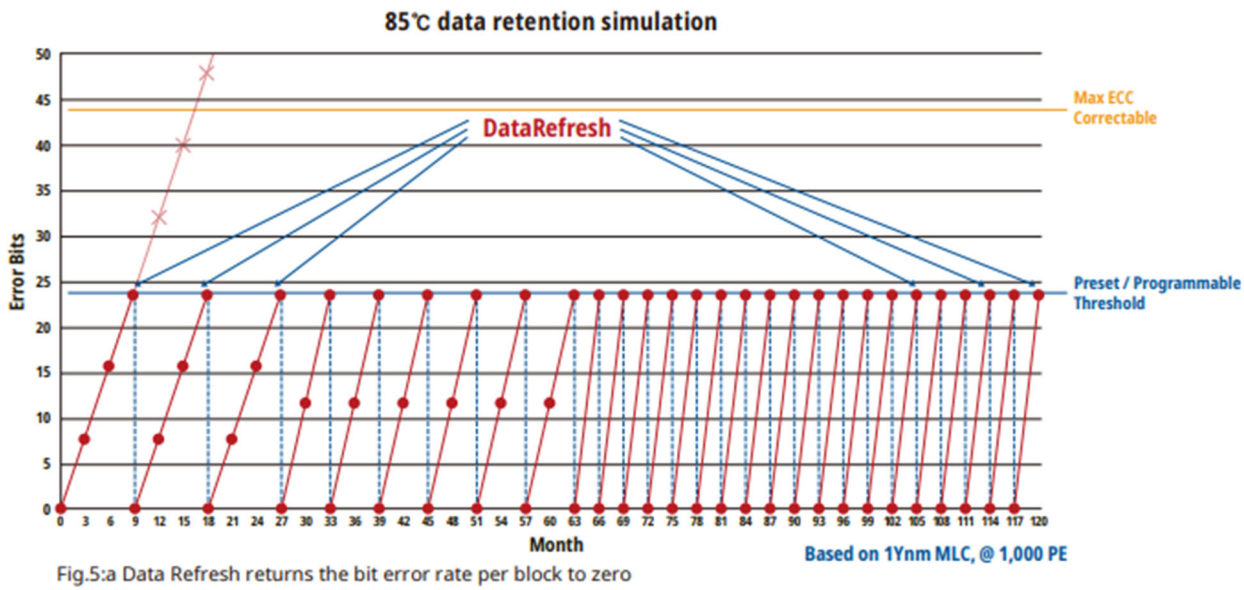


Fig.5:a Data Refresh returns the bit error rate per block to zero

Ex. OO, (https://www.siliconmotion.com/download/3TZ/a/Ferri_Family_Optimizes_Embedded_WP_EN.pdf) (showing that when data integrity test shows error bits exceed a threshold, the data is rewritten to new blocks and that the error rate returns to zero).

80. In particular, Silicon Motion controllers may move data from MLC to SLC as part of the relocation above as part of Silicon Motion's SLC caching technology. Further, Silicon Motion's system also moves data to SLC for emergency shutdown operations, which may be considered a response to a failure of a data integrity test (such as power loss that jeopardizes data):

> Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast Write

> SLC memory, which is ideal for emergency power shutdown operations. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of

Ex. EE, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf

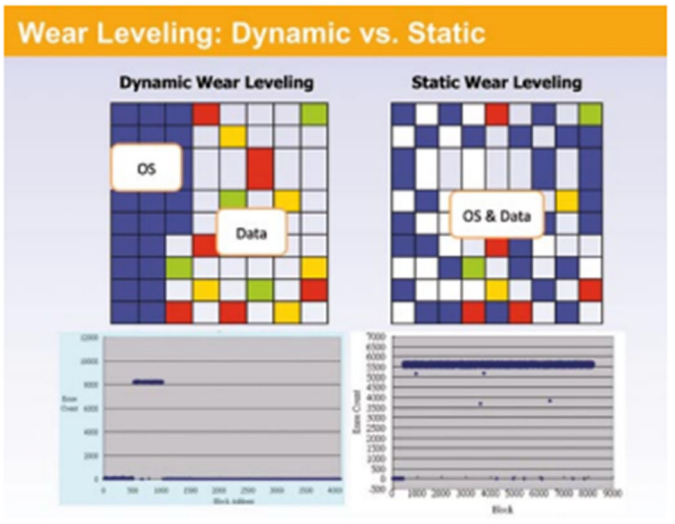
81. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, Kingston's products use controllers, such as Phison or Silicon Motion controllers, that employ various types of block counting.

82. For example, Phison controllers use count data, such as program/erase counts and valid page counts, to maintain a count of the number of times each one of the blocks is accessed:

> **Dynamic SLC buffer (D3)**
>
> A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Ex. Z, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

In addition, decreasing the Erase Count has brought about a shorter life expectancy of NAND Flash. The wear leveling mechanism of the controller can resolve this problem. NAND Flash consists of many blocks and each block has its certain life span. The number of erasable cycles represented the block life-expectancy and was called the Erase Count. In order to extend the lifetime of NAND Flash, we have to balance the Erase Count of all blocks. With a wear leveling mechanism implemented, the controller can achieve this goal to average the Erase Count of each block.



Ex. JJ, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

"A memory management method, and a memory control circuit unit and a memory storage apparatus using the same are provided. The method includes associating physical erasing units with a data area or a spare area, configuring a plurality of logical addresses for mapping to the physical erasing units, and obtaining a garbage collection threshold based on a plurality of valid logical addresses among the logical addresses, and the physical erasing units mapping to the valid logical addresses are associated with the data area. The method further includes performing a garbage collection operation on the data area if the number of the physical erasing units associated with the data area is no less than the garbage collection threshold."

Ex. PP, U.S. Pat. App. Pub. No. 2019/0073298, Abstract.

83. For example, Silicon Motion controllers use count data, such as program/erase (P/E) counts and valid page counts, to maintain a count of the number of times each one of the blocks is accessed:

> **Effect of temperature on data retention**
> One of the most significant inhibitors to data retention is elevated NAND temperature – the higher the ambient working temperature, the shorter the retention capability of the NAND itself. The PCIe FerriSSD incorporates a Silicon Motion patent-pending monitoring algorithm which logs cumulative junction temperature readings, the number of P/E cycles, SSD power on-time, and other essential reference points to dynamically select and prioritize which NAND cells to DataRefresh, and when.

Ex. EE, https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf

> Armed with Silicon Motion's proprietary IntelligentScan & DataRefresh, FerriSSD will intelligently activate a self-scanning feature to prevent potential data lost before it occurs; the self-scan frequency will be intelligently adjusted by ambient temperature, erase count, read count, and associated factors. FerriSSD's

Ex. LL, https://www.siliconmotion.com/download/3TY/a/FerriSSD_BGASSD_WP_EN.pdf

"In the control method, by establishing a valid page count table, a detailed valid page count table and/or a zone valid page count table according to deallocate command from the host device, the flash memory controller can efficiently and quickly determine if any one of the zones does not have any valid data, so that the flash memory controller can recommend the host device to send a reset command to reset the zone. In addition, after receiving the reset command from the host device, the flash memory controller can use a garbage collection operation or directly put the blocks corresponding to the erased zone into a spare block pool, for the further use."

Ex. QQ, U.S. Patent 11,809,328, Abstract; see also Ex. RR, U.S. Patent App. Pub. No. 2023/0350799, Abstract (describing valid page count table).

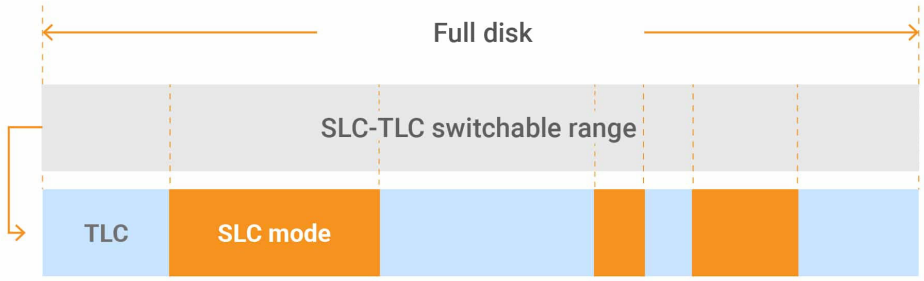
84. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the controller (for example, a Phison or Silicon Motion controller) transfers the contents of those blocks that receive the most frequent writes to SLC memory.

85. Phison controllers move frequently accessed data to SLC NAND. A "count balance scheme" is used to transfer frequently written blocks to SLC, and blocks are switchable between SLC and TLC:

Dynamic SLC buffer (D3)

A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Figure 3. Dynamic SLC buffer profile



Ex. Z, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

86. In addition, garbage collection can relocate frequently accessed data based on a page count:

For random writes, the main issue is invalid pages. Whenever garbage collection engages, the controller needs to write valid pages to other unused blocks. With the background read/write and Host read/write requests, the overall drive performance degrades.

Ex. SS, https://phisonblog.com/using-overprovisioning-with-ssds-2/

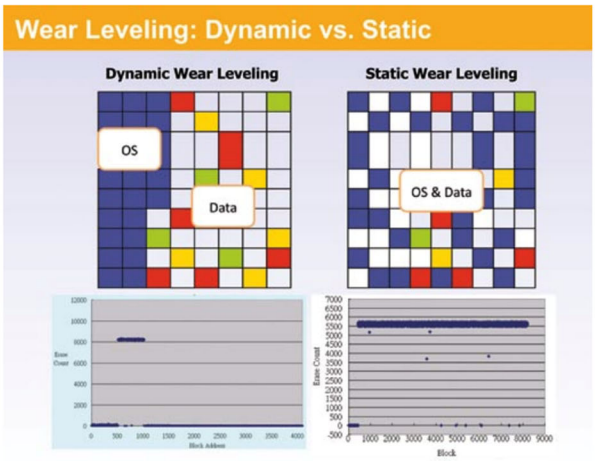
87. Phison also uses a "double rotation" scheme to move data to SLC blocks:

> Therefore, controllers are using many sophisticated functions to protect stored data. We can observe these results during our daily work, many steps have to be applied before data will be recovered and almost every operation, we reverse, is applied to protect user data as well as possible.
>
> In this article, we would like to bring closer SLC blocks topic and present to you the solution for Phison controllers which are using double rotation mode.
>
> How to recognize that controller uses double rotation?
>
> How to reverse this type of rotation?
>
> How to pull out data from the SLC block?
>
> All this information you will find in this article.
>
> In the example below we have a dump from a micro SD card equipped with a Phison controller. We've used static rotation, but despite, that the rotation element is attached, we could not access the file system.
>
> Visual Nand Reconstructor - phison double rotation

Ex. TT, https://support.rusolut.com/portal/en/kb/articles/no-pic-no

88. Phison's articles discuss "replacing MLC to SLC":

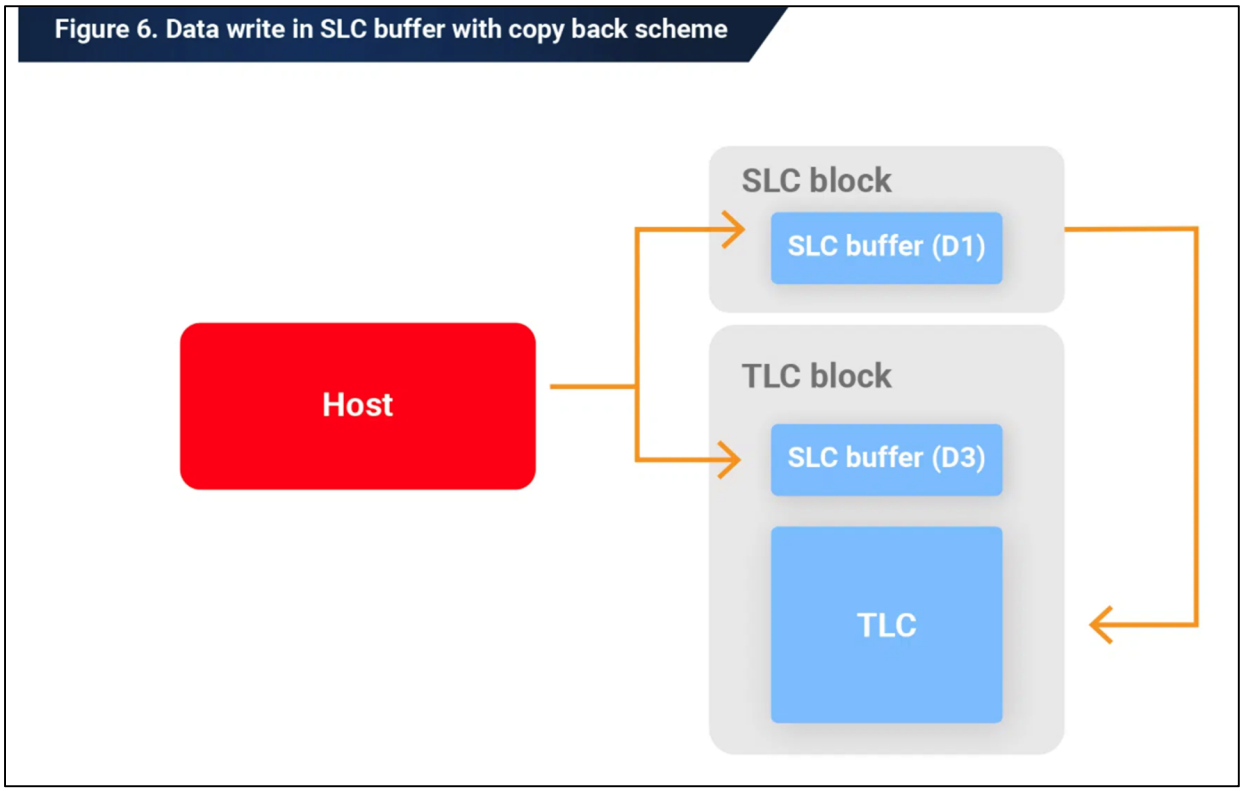
> With process advances, NAND Flash can support the development of more cost-competitive solutions but the reliability of NAND Flash is getting worse. In terms of market response, customers won't just accept inferior quality products because of the price drop. On the contrary, they demand products at the same level but with the same or better reliability and performance. Therefore, the focus of attention has turned to the Flash controller to address this problem.
>
> Basically, significant problems of reliability are caused by things like replacing MLC to SLC, increasing 2 bits/cell to 3 bits/cell, reducing the Erase Cycle number from 100K down to 10K, and cutting Data Retention times through the advances of NAND Flash. These issues can be solved within a re-designed and robust controller.
>
> For example, the error rates of NAND Flash are increasing



Ex. JJ, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

89. Phison's controllers have a copyback scheme where data is moved between SLC and TLC blocks; with this scheme, data being rewritten as part of garbage collection may be

moved from TLC to SLC. For example, Phison's blog explains that "When an SSD uses copy back, host data moves into zone D1," where D1 represents SLC.



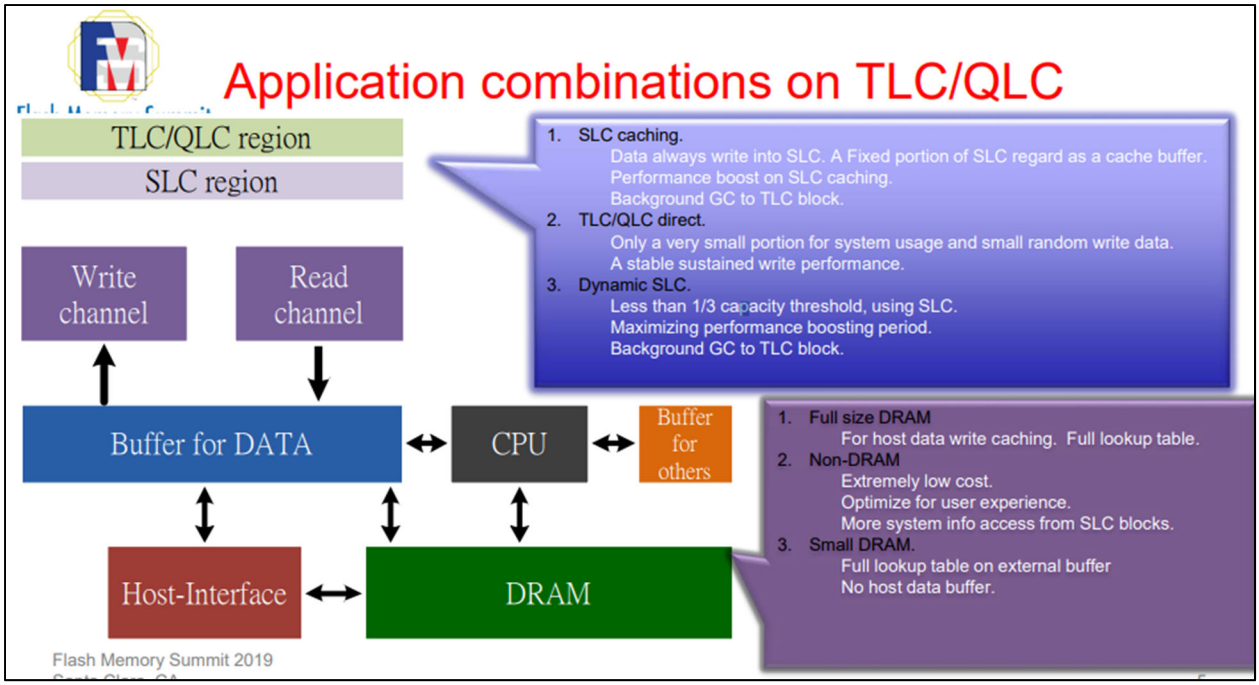
Ex. Z, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

90. Silicon Motion controllers move frequently accessed data to SLC NAND.

> Hybrid Zone, a unique feature of the PCIe FerriSSD, offers a way to take advantage both of the low latency of SLC cells and the high memory density of TLC cells.
>
> The Hybrid Zone feature partitions a single NAND die into separate SLC and MLC/TLC zones. Partitioning a single drive is particularly useful in low- to medium- density SSDs.
>
> Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast Write

> SLC memory, which is ideal for emergency power shutdown operations. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of SLC memory is also ideal for high reliability and fast access— assigning SLC to boot code for instance – while also preserving a portion of the NAND medium for higher density MLC/TLC uses.

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf



Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf)

91. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

92. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

93. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '298 patent by Defendants.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,196,385

94. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

95. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '385 patent by making, using, offer for sale,

selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

96. The Accused Products meet all the limitations of at least claim 1 of the ’385 patent. Specifically, claim 1 of the ’385 patent recites:

> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a flash translation layer (FTL); wherein the FTL is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and
>
> d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

97. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

98. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

99. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

100. The Accused Products include a flash translation layer (FTL). For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table. This is known as a flash translation layer:

Ex. II, (https://www.phison.com/en/technologies/ftl)

101. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer

system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

102. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

103. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, as explained in Count I above, a variety of block counting mechanisms are present in the Accused Products.

104. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For

example, as explained in Count I above, frequently written blocks are allocated and their contents transferred to SLC.

105. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

106. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

107. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '385 patent by Defendants.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 9,997,240

108. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

109. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '240 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

110. The Accused Products meet all the limitations of at least claim 6 of the '240 patent. Specifically, claim 6 of the '240 patent recites:

6. A system for storing data comprising:

at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;

at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and

a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;

wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and

wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

111. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

112. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

113. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

114. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

115. In the Accused Products, the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks. For example, as explained in Count I above, frequently written blocks are allocated and their contents transferred to SLC, and infrequently written data is moved to MLC through copyback/garbage collection and other procedures.

116. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a

failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

117. In the Accused Products, the controller is adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller. For example, as explained in Count I above, the Accused Products employ various types of block counting, and transfer the contents of frequently written blocks to the next available locations in SLC based on the count value.

118. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

119. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

120. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '240 patent by Defendants.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,950,300

121. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

122. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the ’300 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

123. The Accused Products meet all the limitations of at least claim 1 of the ’300 patent. Specifically, claim 1 of the ’300 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
>
> at least one controller to operate memory elements and associated memory space;
>
> at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
>
> at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;
>
> at least one random access volatile memory;
>
> an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;
>
> the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;
>
> the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

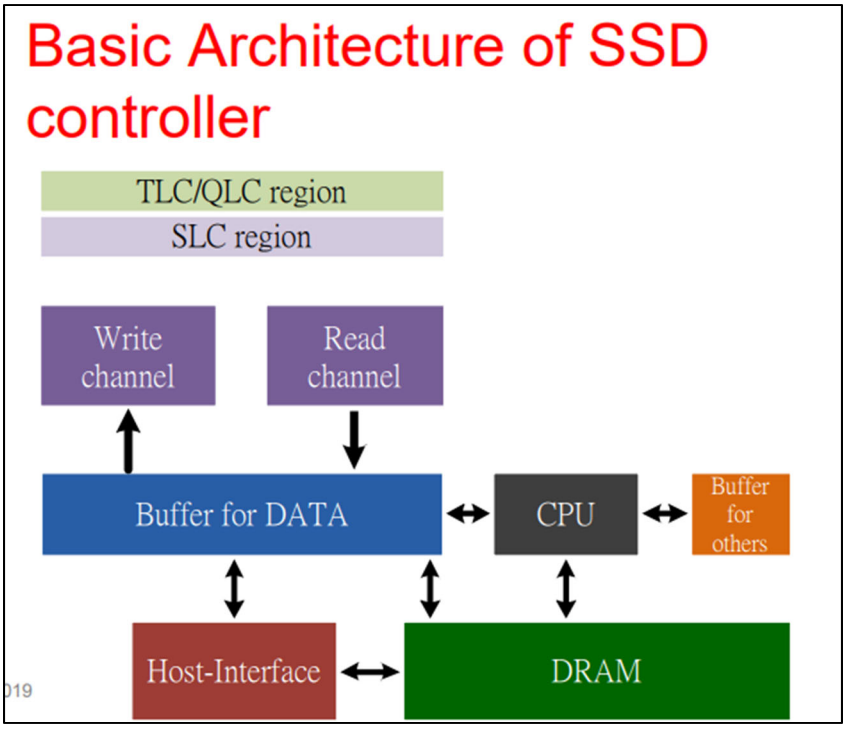
wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

124. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

125. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, as explained in Count I above, the Accused Products include MLC and SLC memory. These locations are mapped to memory space:

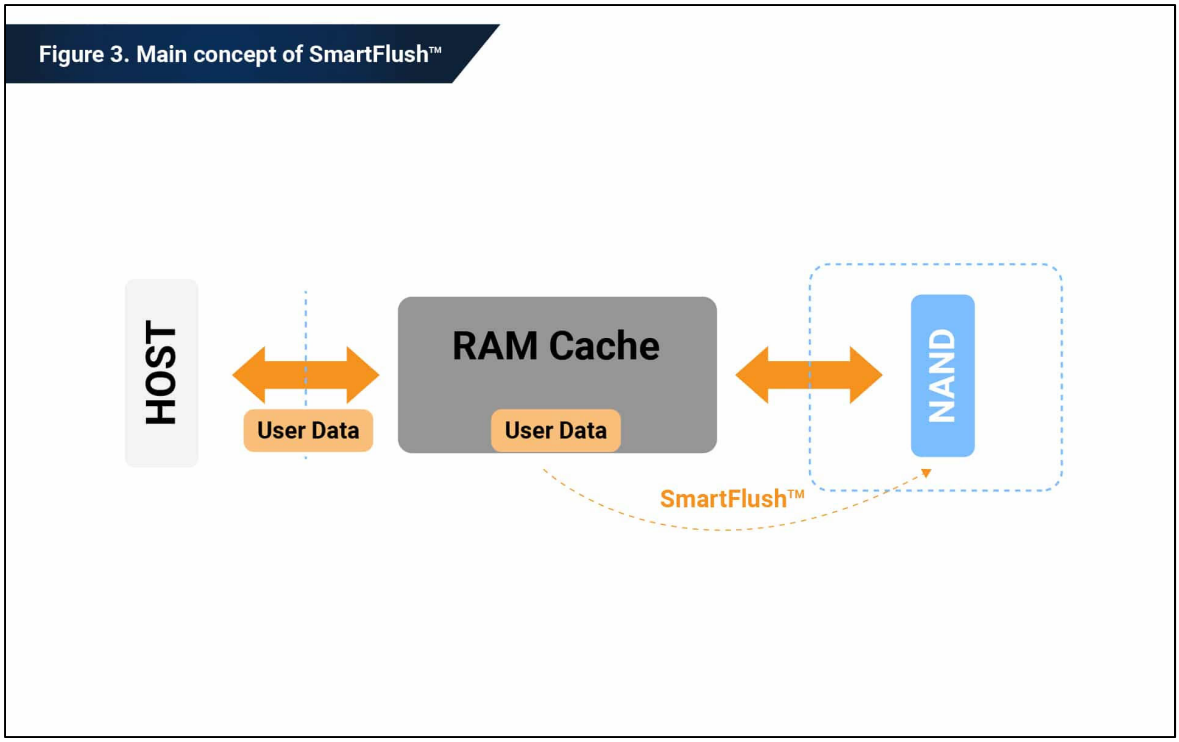
> **How GC processes data**
>
> Since SSDs cannot overwrite existing data in NAND memory cells, they must first erase old data before programming new data to the same location. GC is the process of relocating existing data to new locations within free memory space and allowing the surrounding invalid data to be erased thoroughly.

Ex. BB, (https://phisonblog.com/ssd-garbage-collection/)



Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf) at 3.

In addition, both Phison and Silicon Motion controllers use RAM caching to store user data and metadata in RAM (volatile) memory:



Ex. VV, (https://phisonblog.com/smartflush/)

DRAM cache with data redundancy: no data loss during data transfers

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. EE,

(https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf) at 2.

126. The Accused Products include at least one controller to operate memory elements and associated memory space. The Accused Products include controllers, for example the controllers identified in paragraph 51 above.

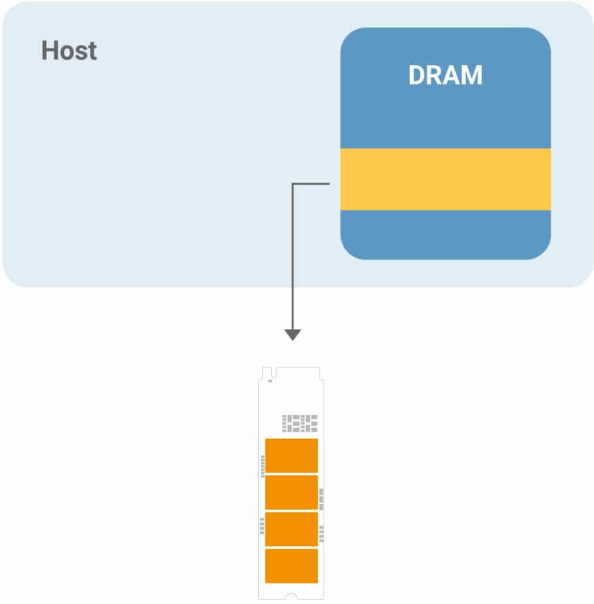
127. The Accused Products include at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. For example, the MLC memory in the Accused Products is mapped into a memory space.

128. The Accused Products include at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. For example, the SLC memory in the Accused Products is mapped into a memory space.

129. The Accused Products include at least one random access volatile memory. For example, the Accused Products include RAM. Certain of the Accused Products, including at least the HyperX Savage, A1000, A2000, DC500M, DC500R, FURY Renegade, KC400, KC600, KC1000, KC2000, KC2500, KC3000, include a type of RAM called DRAM.[26] The Accused Products' controllers also include other types of random access volatile memory, such as static RAM ("SRAM"). Finally, Kingston instructs users to combine many of the Accused Products with a host system that has available random access memory to form a "Host Memory Buffer" for the flash storage product's use. For example, the NV1 and NV2 include an "HMB" or "Host Memory Buffer."

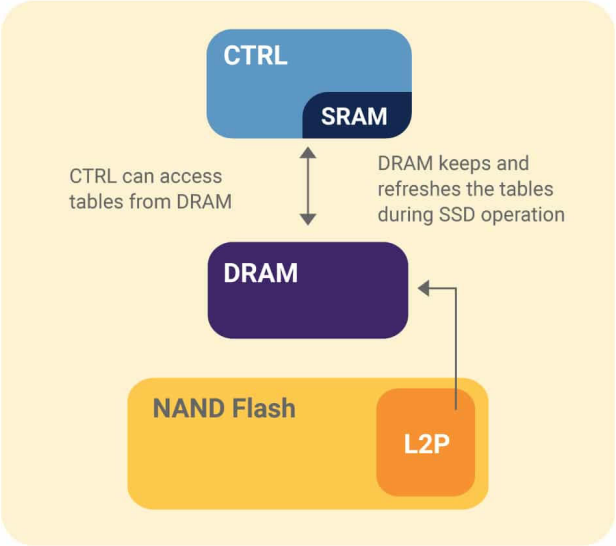
[26] Ex. U, https://www.techpowerup.com/ssd-specs/#kingston

Figure 1. Host memory allocated for SSD utilization



Ex. CC, (https://phisonblog.com/host-memory-buffer-2/)

Figure 2. Cache operating mechanism of SSD with DRAM



Ex. CC, (https://phisonblog.com/host-memory-buffer-2/)

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When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. EE,

(https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf) at 2.

File	Product	Host Standards	Flash Interface	ECC Support	Flash VCCQ Support	DRAM	TCG/AES	Package
	SM2268XT	PCIe Gen4 x4 NVMe 2.0	4-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	FCCSP247 (7mm x 11mm)
	SM2269XT	PCIe Gen4 x4 NVMe 1.4	4-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	FCCSP247 (7mm x 11mm)
	SM2261XT	PCIe Gen3 x2 NVMe 1.3	2-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	FCCSP221L (9 mm x 6.7mm)
	SM2264	PCIe Gen4 x4 NVMe 1.4	8-CH	Configurable LDPC ECC	1.8V/1.2V	Yes	Yes	FCBGA841 (15 x 15mm)
	SM2267	PCIe Gen4 x4 NVMe 1.4	4-CH	Configurable LDPC ECC	1.8V/1.2V	Yes	Yes	FCBGA484 (12 x 12mm)
	SM2267XT	PCIe Gen4 x4 NVMe 1.4	4-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	FCCSP247 (11 x 7.7mm)
	SM2262EN	PCIe Gen3 x4 NVMe 1.3	8-CH	Configurable LDPC ECC	1.8V/1.2V	Yes	Yes	TFBGA472 (18 x 16mm)
	SM2263EN	PCIe Gen3 x4 NVMe 1.3	4-CH	Configurable LDPC ECC	1.8V/1.2V	Yes	Yes	TFBGA288 (12 x 12mm)
	SM2263XT	PCIe Gen3 x4 NVMe 1.3	4-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	TFBGA288 (12 x 12mm)
	SM2259XT2	SATA 6Gb/s (Revision 3.1)	2-CH	Configurable LDPC ECC	1.8V/1.2V	--	Yes	TFBGA (8x8 mm)
	SM2246EN	SATA 6Gb/s (Revision 3.1)	4-CH	Configurable BCH ECC	3.3V/1.8V	Yes	Yes	TFBGA288 (12 x 12mm)
	SM2246XT	SATA 6Gb/s (Revision 3.1)	4-CH	Configurable BCH ECC	3.3V/1.8V	--	--	TFBGA144 (9 x 9mm)

Ex. NN, (https://www.siliconmotion.com/products/client/detail) (showing controllers with DRAM).

"Its innovative hardware features HMB (Host Memory Buffer) technology without compromising performance."

Ex. NN, (https://www.siliconmotion.com/products/client/detail) (describing use of HMB in DRAM-less controllers)

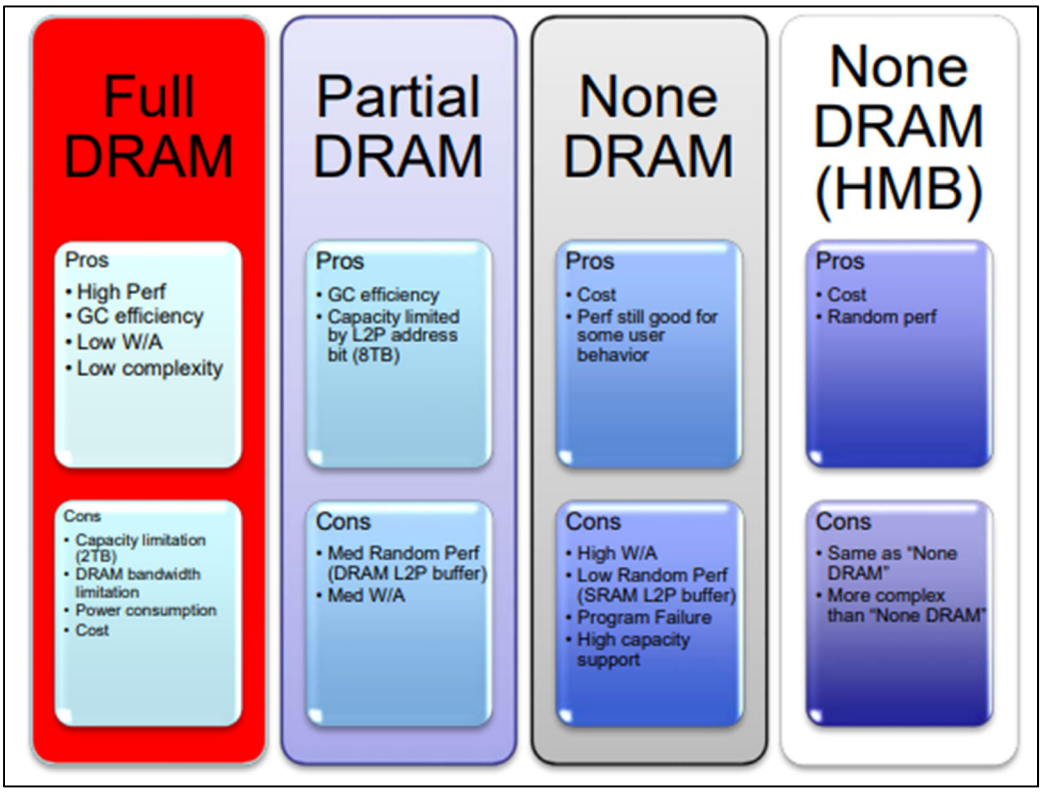
130. The Accused Products include an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. As explained with respect to Counts I and II above, the Accused Products include an FTL flash translation layer with an L2P table. Phison explains that the L2P table is stored in flash memory and in DRAM:

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

On the other hand, during powered-on scenarios, the L2P table is uploaded to DRAM so that it can be constantly updated by the controller. The larger the DRAM size, the more free space available for the controller to play with. This generally means more flexible data placement and thus better reaction time upon receiving commands. In terms of typical data workloads, operations that call for so-called "random read" sequences benefit the most from ample DRAM space.

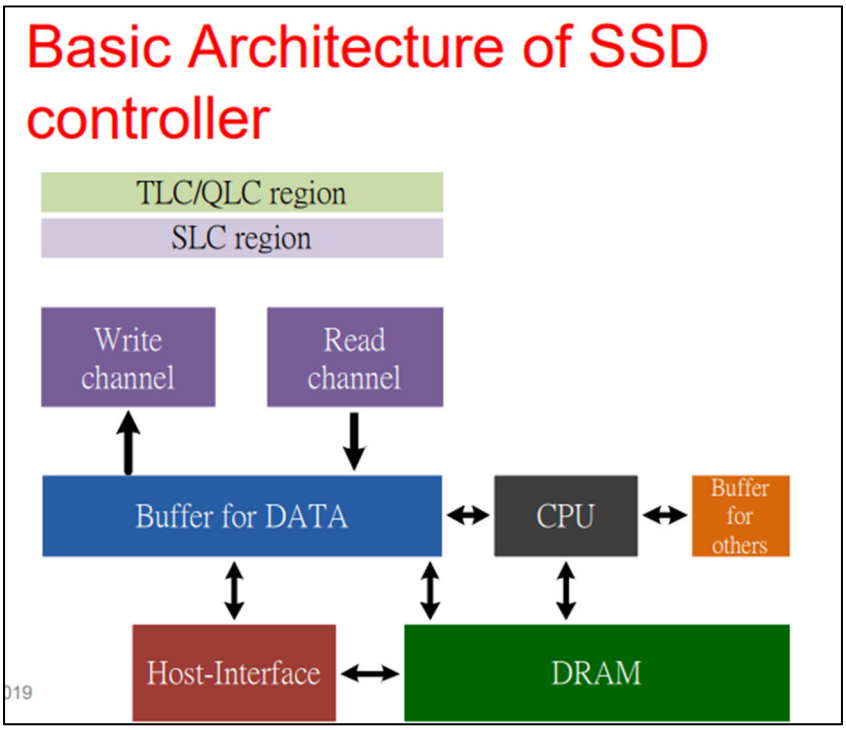
Ex. CC, (https://phisonblog.com/host-memory-buffer-2/)

Similarly, for Silicon Motion products, the L2P table stored in Flash may be cached in DRAM or SRAM:

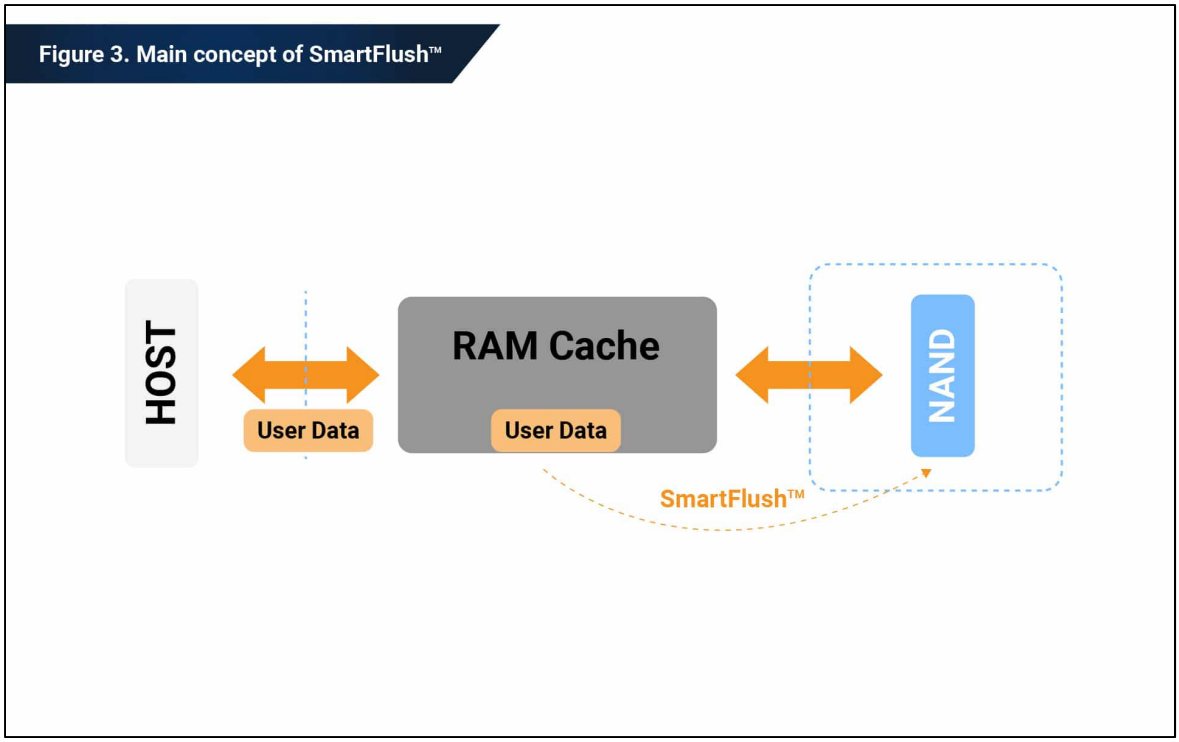


Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf) at 8.

131. The Accused Products include a controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. For example, the controller in the Accused Products controls access to the MLC and SLC memory and the DRAM, storing data in the flash memory and retaining data in the DRAM:



Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf) (Silicon Motion) at 3.



Ex. VV, (https://phisonblog.com/smartflush/)

DRAM cache with data redundancy: no data loss during data transfers

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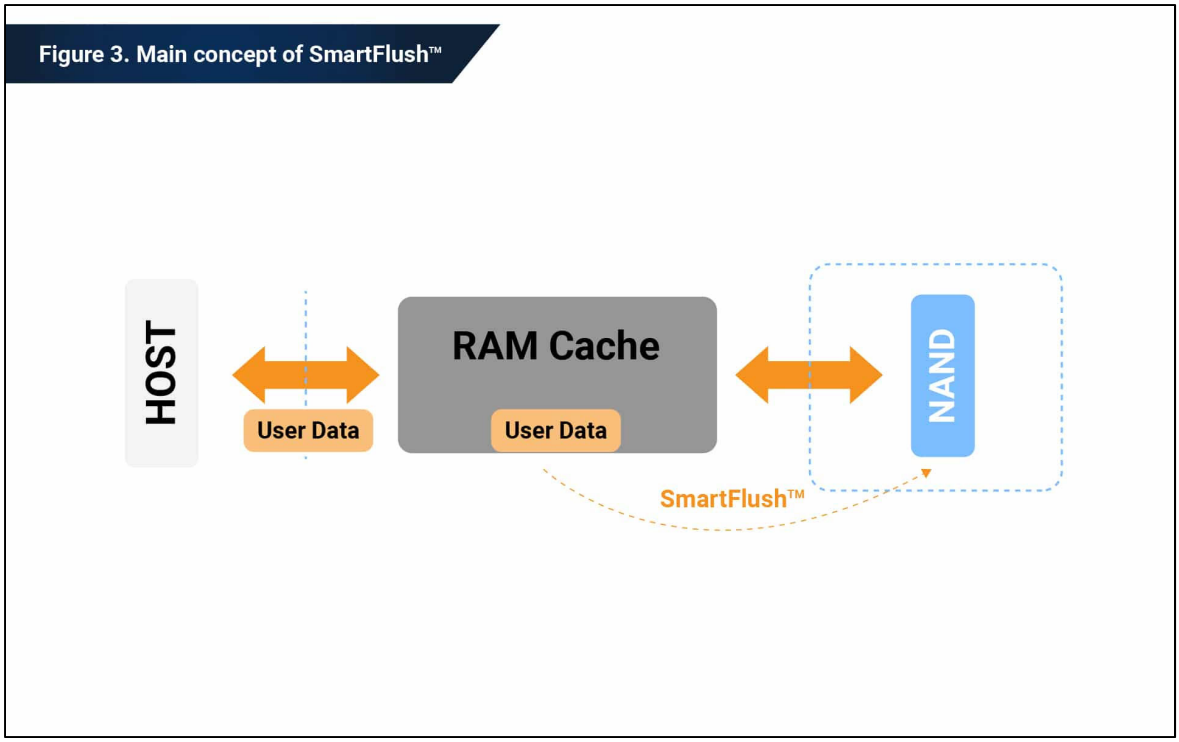
When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. EE,

(https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf) at 2.



Ex. VV, (https://phisonblog.com/smartflush/)

132. In the Accused Products, the controller performs a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory. For example, the controller in the Accused Products performs a data integrity test by comparing data stored in the flash memory with data retained in RAM. For instance, the controller compares data—either user data or data from the logical-to-physical (L2P) table—in RAM with that stored in the NAND flash memory and uses the data to eliminate the risk of data loss in case of any error.

DRAM cache with data redundancy: no data loss during data transfers

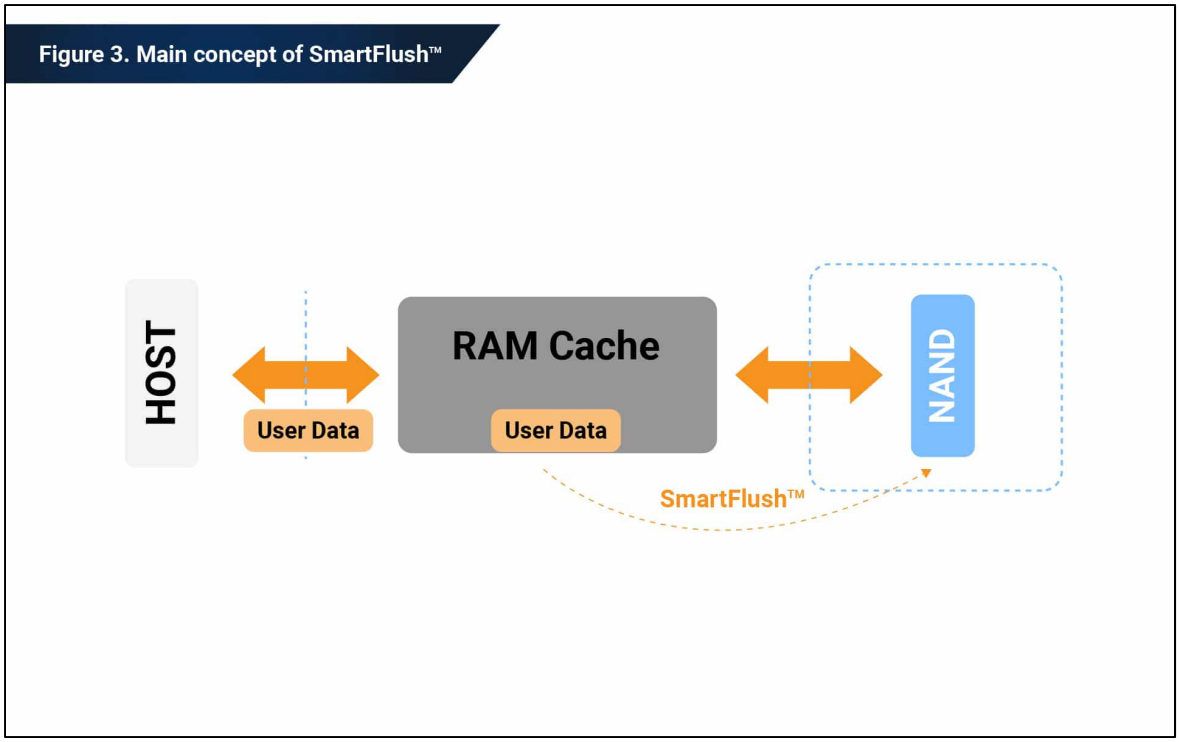
Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

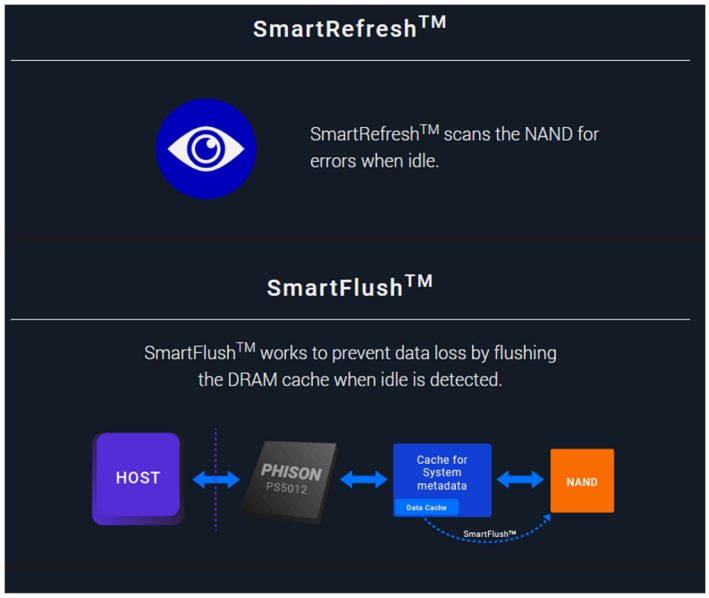
Ex. EE,

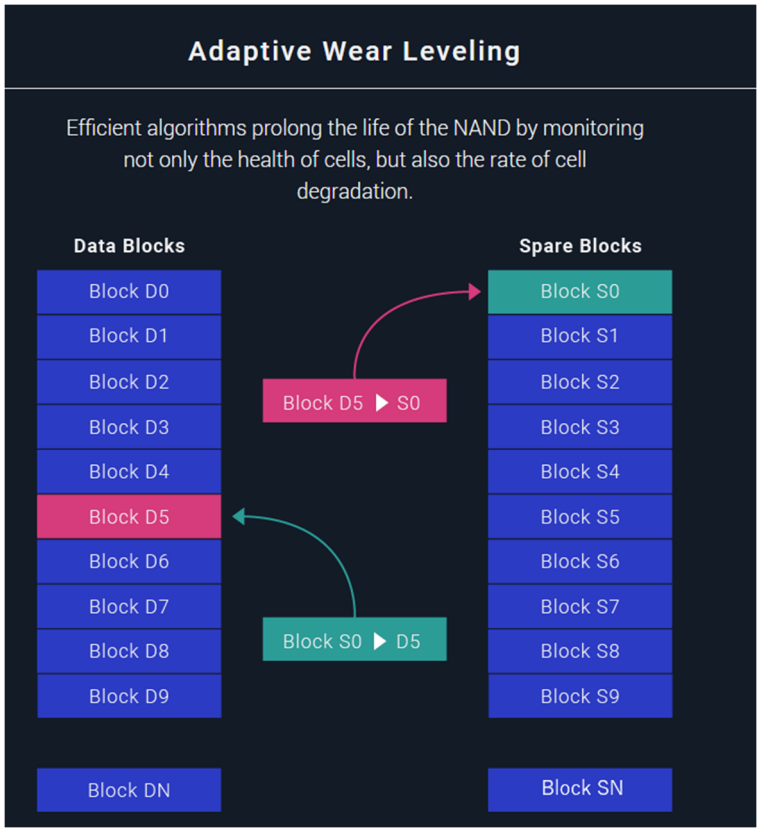
(https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf) at 2.



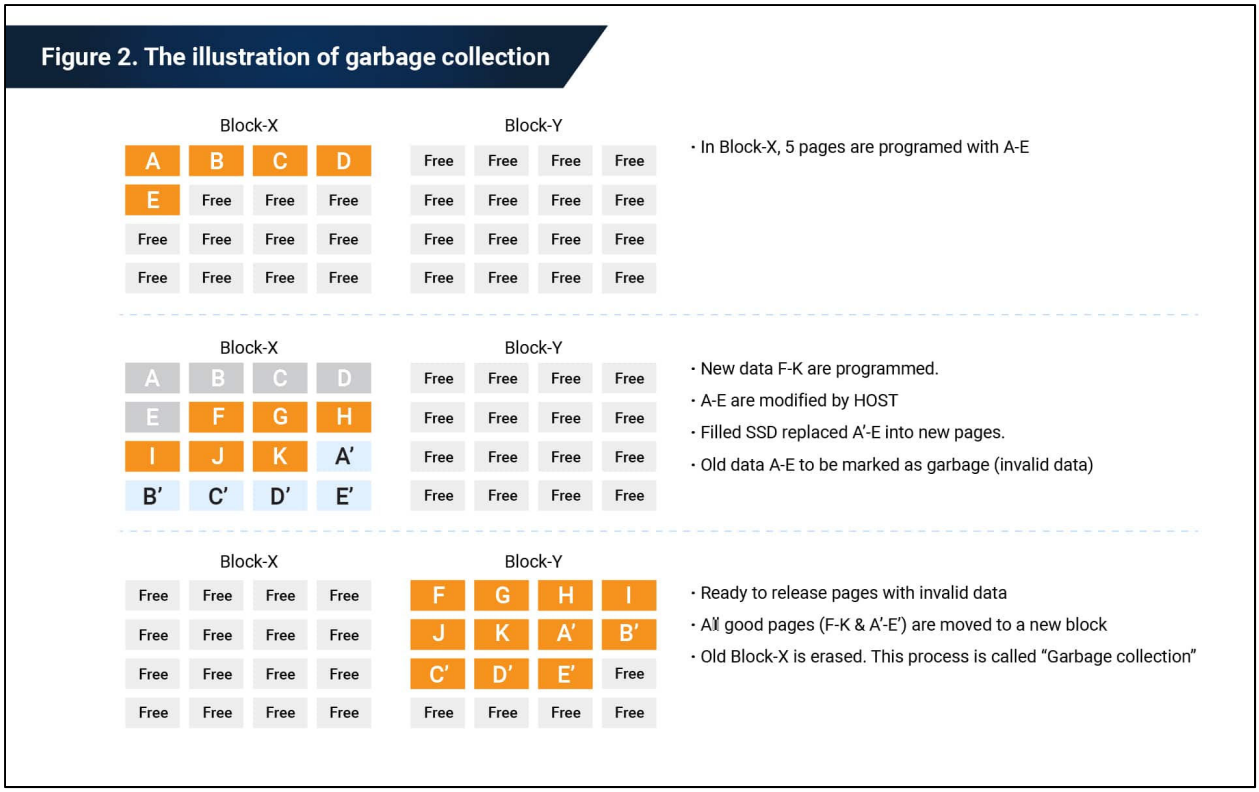
Ex. VV, (https://phisonblog.com/smartflush/)

133. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, the Accused Products' controllers employ wear leveling and garbage collection techniques that transfer blocks within the flash memory in a way that maximizes lifetime.



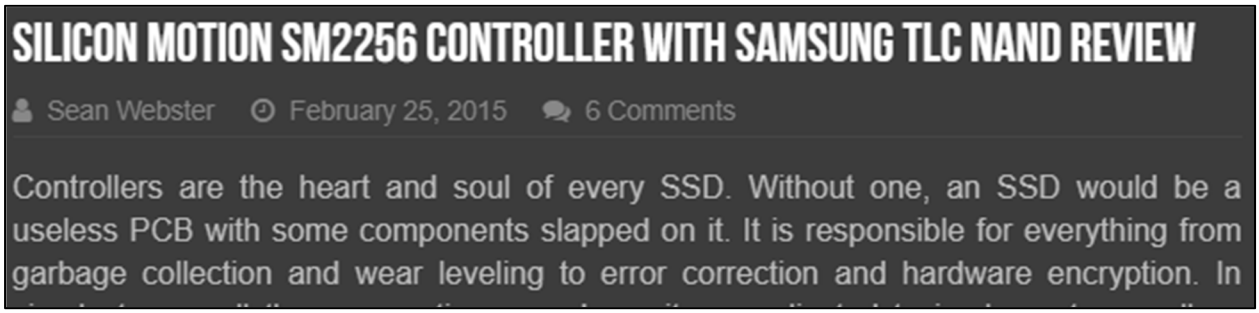


Ex. II, (https://www.phison.com/en/technologies/ftl)



Ex. BB, (https://phisonblog.com/ssd-garbage-collection/)

Ex. NN, (https://www.siliconmotion.com/products/client/detail).

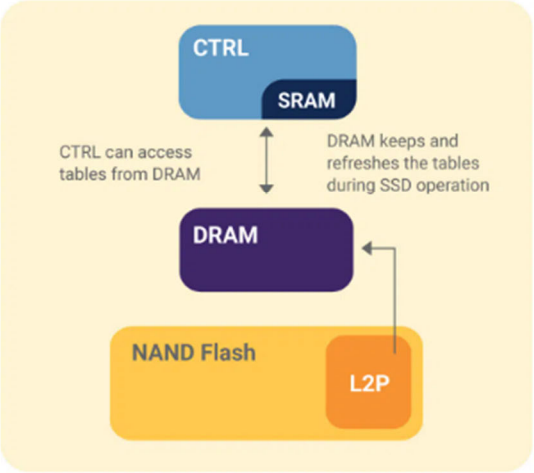


Ex. WW, (https://www.thessdreview.com/our-reviews/silicon-motion-sm2256-controller-with-samsung-tlc-nand-review/).

The controller uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

Figure 2. Cache operating mechanism of SSD with DRAM



Ex. CC, https://phisonblog.com/host-memory-buffer-2/

DRAM cache with data redundancy: no data loss during data transfers

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf).

The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit.

> A flash memory cell is composed of pages, and pages form a block. Due to the intrinsic characteristic of NAND device physics, the flash cell allows data to be programmed on a page level but only erased on a block level. This inconsistency between program and erase tasks is the major impact on SSD endurance.

Ex. BB, (https://phisonblog.com/ssd-garbage-collection/)

134. In the Accused Products, a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance. For example, the Accused Products remap data to new physical addresses after failing a data integrity test which compared data stored in the flash memory with data retained in the DRAM in order to achieve enhanced endurance. When defects in memory are found, valid data in the cells is rewritten. Because a block cannot be rewritten until it is erased, the valid data is remapped to a different physical range of addresses when writing,

> Before claiming the space taken up by invalid data, all the valid data in pages from the initial block must be copied and written into empty pages of a new block. The invalid data in the original block can then be erased, ready for new valid data to be written.

Ex. BB, (https://phisonblog.com/ssd-garbage-collection/)

> Phison's embedded firmware runs in the background to check the error bit of each block. Once there is a block fail within the criteria set by our firmware (i.e., the number of error bits is over the threshold decided in advance), the firmware performs specific actions on this failed block to guarantee the integrity of user data.

Ex. GG, (https://phisonblog.com/phisons-smartrefresh-2/)

DRAM cache with data redundancy: no data loss during data transfers

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

Ex. EE, (https://www.siliconmotion.com/download/3Ta/a/PCIe_FerriSSD_Industrial_Embedded_Applications_WP_EN.pdf) at 2.

The IntelligentScan function is responsible for checking whether the stored charge has declined below its threshold value. If it has, it reads out the data bit and rewrites it via the ECC engine, and DataRefresh recharges the cell to restore the NAND cell's voltage to the correct level.

Ex. KK, (https://www.siliconmotion.com/download/3g1/a/FerriSSD_Gaming_WP_EN.pdf)

135. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

136. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

137. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '300 patent by Defendants.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 11,830,546

138. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

139. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '546 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

140. The Accused Products meet all the limitations of at least claim 1 of the '546 patent. Specifically, claim 1 of the '546 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;
>
> at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;
>
> a bank of nonvolatile memory, including:
>
> a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and

at least one SLC memory module including at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

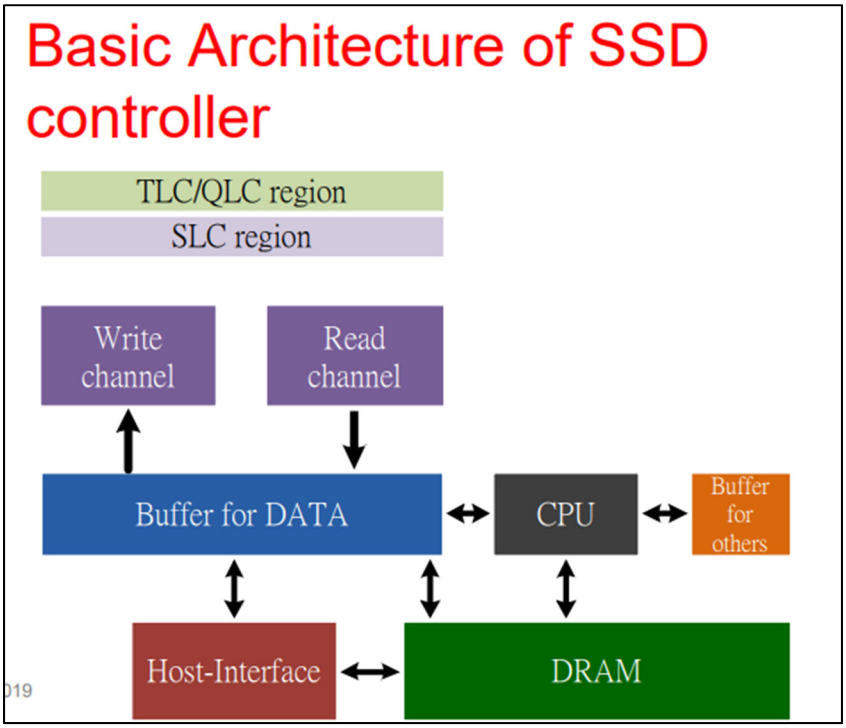
wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

141. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

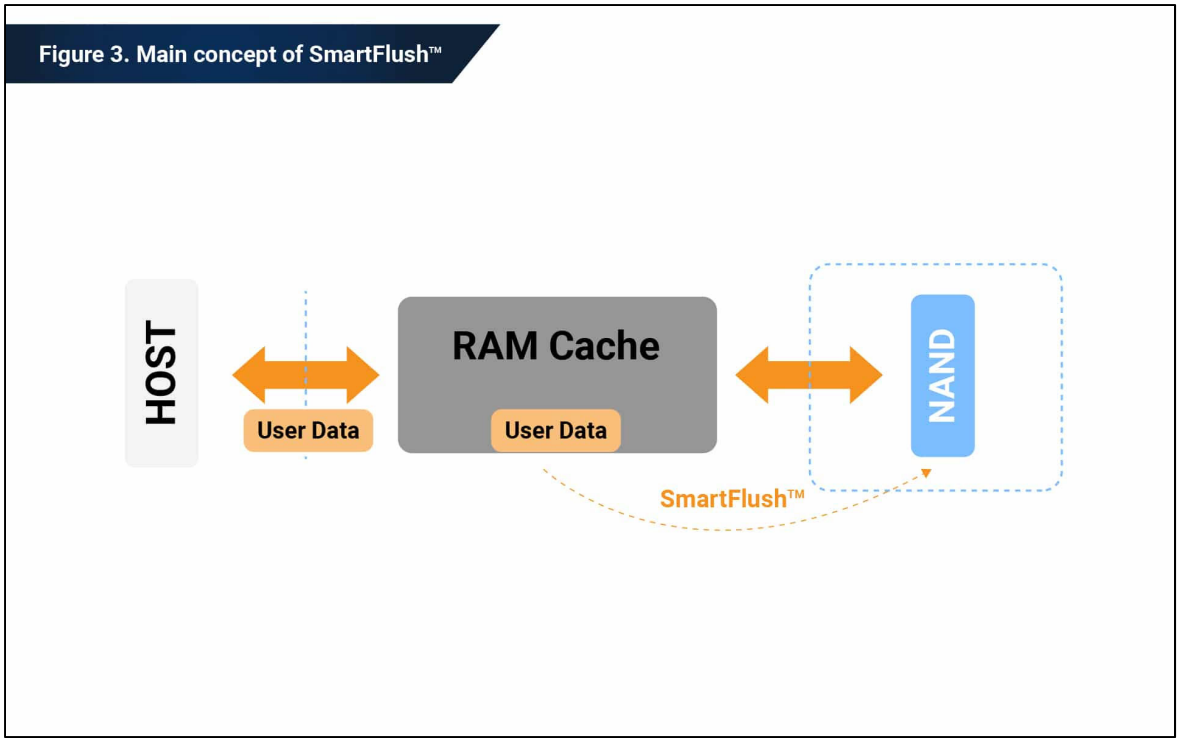
142. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level

cell (MLC) space and single level cell (SLC) space. For example, as explained in Count IV above, Kingston's products use both MLC and SLC memory space, as well as volatile memory space (e.g. for RAM).

143. The Accused Products include at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements. For example, the controllers in the Accused Products handle read and write operations to flash memory.



Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf) (Silicon Motion) at 3.



Ex. VV, (https://phisonblog.com/smartflush/)

144. The Accused Products include a bank of nonvolatile memory, including a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and at least one SLC memory module including at least one SLC nonvolatile memory element. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory.

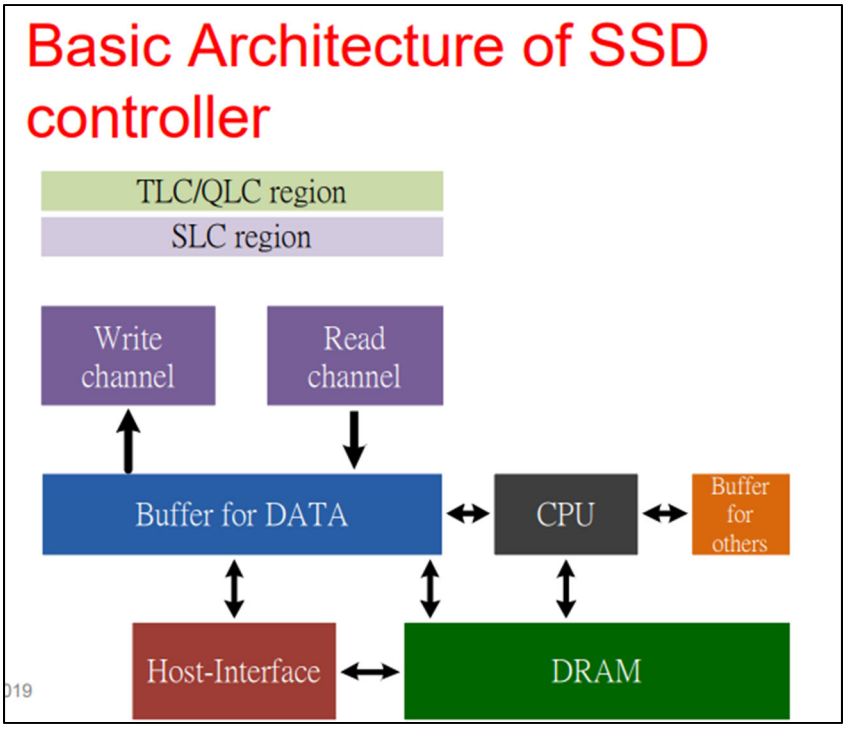
145. The Accused Products include at least one random access volatile memory element. For example, as explained in Count IV above, the Accused Products contain some form of RAM such as DRAM or SRAM. In addition, Kingston instructs users to combine many of the Accused Products with a host system that has available random access memory to form a "Host Memory Buffer" for the flash storage product's use.

146. The Accused Products include a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of

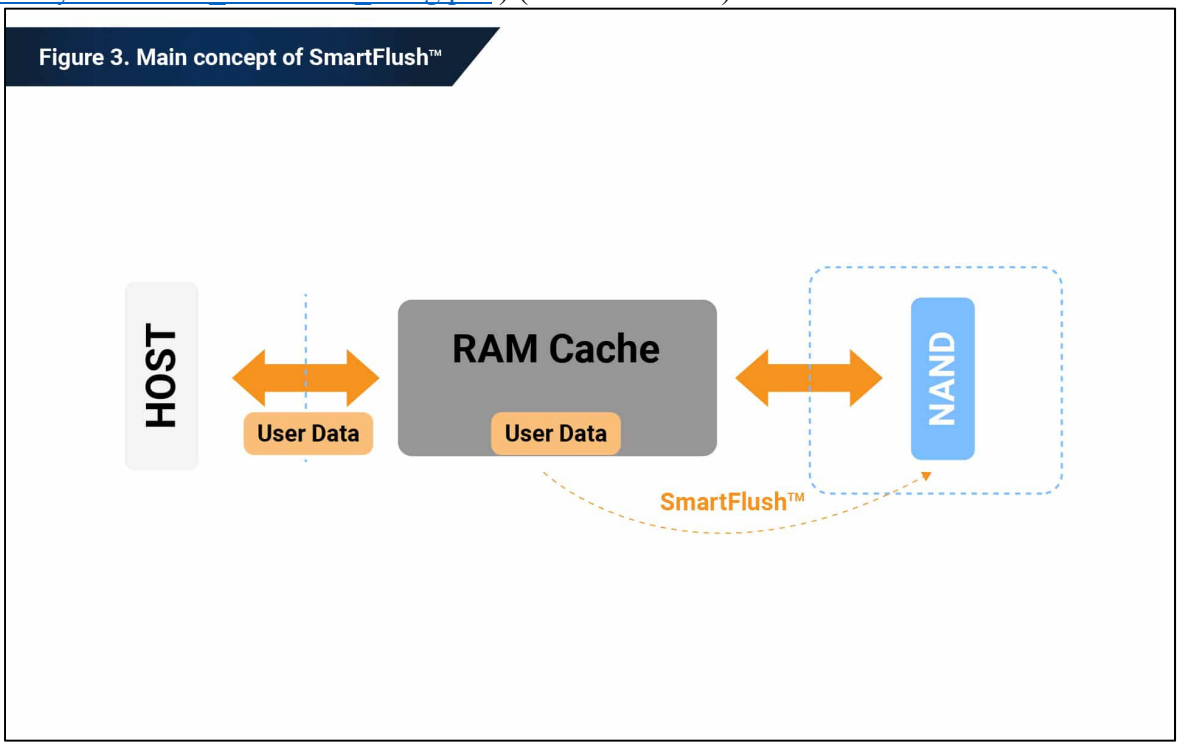
the memory elements. For example, as shown with respect to Count IV above, the Accused Products maintain an address table in flash memory.

147. The controller in the Accused Products has associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data. For example, as shown with respect to Count IV above, the Accused Products cache written data in RAM.

148. The controller in the Accused Products performs a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test by comparing stored data and retained data. In addition, the controller provides controller memory such as buffers or caches to store retained data:



Ex. UU, (https://www.flashmemorysummit.com/Proceedings2019/08-05-Monday/20190805_PreConfG_Yang.pdf) (Silicon Motion) at 3.



Ex. VV, (https://phisonblog.com/smartflush/)

149. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, as shown with respect to Count IV above, the Accused Products use wear leveling and garbage collection, in conjunction with an L2P table, to map logical and physical addresses as necessitated by the system to maximize lifetime.

150. In the Accused Products, a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

151. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

152. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

153. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '546 patent by Defendants.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 11,854,612

154. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

155. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the ’612 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

156. The Accused Products meet all the limitations of at least claim 1 of the ’612 patent. Specifically, claim 1 of the ’612 patent recites:

> A method for storing data comprising:
>
> maintaining an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element;
>
> mapping logical and physical addresses adaptable to the system by the address table, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps data in at least one of volatile or nonvolatile memories;
>
> controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller;
>
> storing received data within a controller memory associated with the at least one controller;
>
> controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data;
>
> transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data;

retaining the received data in the random access volatile memory as retained data associated with the stored data;

performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon, the performing of the data integrity test further comprising:

reading the stored data to the controller memory;

comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

remapping, responsive to a failure of the data integrity test performed on the stored data by the controller, the address space to a different physical range of addresses; and

transferring data corresponding to the retained data to those remapped physical address from those physical addresses determined to have failed the data integrity test.

157. To the extent the preamble is a limitation, when used by Kingston or its customers, the Accused Products perform a method for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

158. When used by Kingston or its customers, the Accused Products maintain an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory, and use an address table such as an L2P table to map logical and physical addresses.

159. When used by Kingston or its customers, the Accused Products map logical and physical addresses adaptable to the system by the address table, wherein the mapping is

performed as necessitated by the system to maximize lifetime, and wherein the mapping maps data in at least one of volatile or nonvolatile memories. For example, as explained in Count IV above, the Accused Products use an address table such as an L2P table to map logical and physical addresses, and use techniques such as wear leveling and garbage collection to map the addresses as necessitated by the system to maximize lifetime.

160. When used by Kingston or its customers, the Accused Products control during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory, and use an address table such as an L2P table to map logical and physical addresses.

161. When used by Kingston or its customers, the Accused Products store received data within a controller memory associated with the at least one controller. For example, as explained in Count V above, the Accused Products include a controller that handles reads and writes and stores data in controller memory, which may be used as a cache, as part of that process.

162. When used by Kingston or its customers, the Accused Products control access of the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data. For example, as explained in Count V above, the Accused Products include a controller that handles and controls reads and writes to and from both flash and volatile memory.

163. When used by Kingston or its customers, the Accused Products transfer the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data. For example, as explained in Count V above, the Accused Products include a controller memory, such as buffers or caches.

164. When used by Kingston or its customers, the Accused Products retain the received data in the random access volatile memory as retained data associated with the stored data. For example, as explained in Count V above, the Accused Products include random access memory that retains stored data.

165. When used by Kingston or its customers, the Accused Products perform a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data.

166. When used by Kingston or its customers, the Accused Products' data integrity test includes reading the stored data to the controller memory. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data. The stored data would enter a controller memory, such as a buffer or cache, for the purposes of the comparison.

167. When used by Kingston or its customers, the Accused Products' data integrity test includes comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the

random access volatile memory by the controller during the Write access operation. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data. The stored data would enter a controller memory, such as a buffer or cache, for the purposes of the comparison.

168. When used by Kingston or its customers, the Accused Products remap, responsive to a failure of the data integrity test performed on the stored data by the controller, the address space to a different physical range of addresses. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

169. When used by Kingston or its customers, the Accused Products transfer data corresponding to the retained data to those remapped physical address from those physical addresses determined to have failed the data integrity test. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

170. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

171. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

172. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '612 patent by Defendants.

COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 11,967,369

173. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

174. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the ’369 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

175. The Accused Products meet all the limitations of at least claim 1 of the ’369 patent. Specifically, claim 1 of the ’369 patent recites:

> A memory system for storing data comprising:
>
> memory space containing logical and physical volatile memory space and nonvolatile memory space, wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;
>
> a bank of physical nonvolatile memory, including:
>
> a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and
>
> at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space;
>
> at least one random access volatile physical memory element that exists in the logical volatile memory space;
>
> at least one controller to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, the controller having a controller memory associated therewith for storing received data therein;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements;

the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile physical memory element as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation;

wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and

wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of logical address space to a different physical range of addresses in the physical address space and transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test.

176. To the extent the preamble is a limitation, the Accused Products include a memory system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

177. The Accused Products include memory space containing logical and physical volatile memory space and nonvolatile memory space. For example, as explained in Count IV above, the Accused Products include MLC and SLC memory (nonvolatile memory), as well as

RAM (volatile memory). This memory is addressed in logical and physical space. For example, as explained in Count IV above, logical block numbers and other memory mappings are used by the controller, and physical memory space is used to map specific physical locations in memory. For example, as explained in Count IV above, host memory buffers are used to address volatile memory.

178. In the Accused Products, the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space. For example, as explained in Count IV above, the Accused Products include SLC and MLC memory space.

179. The Accused Products include a bank of physical nonvolatile memory. For example, as explained in Count I above, the Accused Products include SLC and MLC physical NAND flash memory. This may include memory configured to operate in SLC mode.

180. The Accused Products include a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space. For example, as explained in Count I above, the Accused Products include MLC NAND flash memory, with physical addresses that are mapped to logical addresses using a flash translation layer/L2P table.

181. The Accused Products include at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space. For example, as explained in Count IV above, the Accused Products map physical

nonvolatile memory space, addressed using physical addresses, into SLC logical nonvolatile memory space for addressing memory logically.

182. The Accused Products include at least one random access volatile physical memory element that exists in the logical volatile memory space. For example, as explained in Count IV above, the Accused Products include RAM. As explained in Count IV above, memory mappings and host memory buffer functionality provide a logical volatile memory space in which the RAM exists.

183. The Accused Products include at least one controller to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements. For example, as explained in Count I above, the Accused Products include a controller that manages reads and writes to the physical memory elements.

184. In the Accused Products, the controller has a controller memory associated therewith for storing received data therein. For example, as explained in Count IV above, the Accused Products include RAM that is used by the controller for storing data.

185. The Accused Products include a flash translation layer (FTL). For example, as explained in Count II above, the Accused Products include a flash translation layer, implemented by hardware and software in the controller, that maps logical to physical addresses.

186. In the Accused Products, the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements. For example, as explained in Counts I and II above, the controller and/or FTL in the Accused Products use an L2P table or similar data structure to map logical addresses to physical addresses. This table

may be stored in RAM for easy access, and is also stored in nonvolatile flash memory so that the mapping is maintained even when the device is powered down.

187. In the Accused Products, the controller controls access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data. For example, as explained in Count IV above, the Accused Products have controllers which control the storage of data in both MLC and SLC memory, and use RAM to store data as well (for example as part of caching).

188. In the Accused Products, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, stores the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retains such received data in the random access volatile physical memory element as retained data associated with stored data. For example, as explained in Count IV above, the Accused Products retain data in RAM when data is stored in flash memory, including MLC flash memory. They may retain data in a cache in RAM, and may also retain certain relevant data as part of the L2P tables stored in RAM.

189. In the Accused Products, the controller performs a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation. For example, as explained

in Count IV above, the Accused Products perform a variety of data integrity tests to ensure that data is stored correctly. These data integrity tests take advantage of the retained data to perform comparisons with data stored in MLC flash memory and detect errors after data is written.

190. In the Accused Products, the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime. For example, as explained in Count IV above, the Accused Products' controllers employ wear leveling and garbage collection techniques that transfer blocks within the flash memory in a way that maximizes lifetime.

191. In the Accused Products, a failure of the data integrity test performed on the stored data by the controller results in a remapping of logical address space to a different physical range of addresses in the physical address space and transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test. For example, as explained in Count IV above, the Accused Products remap data to new physical addresses after a data integrity test failure in the physical addresses where the data was originally stored. This data corresponds to the retained data.

192. For example, as explained in Counts I and IV above, the Accused Products include MLC NAND flash, and this flash is addressed in an MLC non-volatile memory space.

193. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

194. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

195. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '369 patent by Defendants.

COUNT VIII: INFRINGEMENT OF U.S. PATENT NO. 11,967,370

196. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

197. Kingston has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '370 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

198. The Accused Products meet all the limitations of at least claim 1 of the '370 patent. Specifically, claim 1 of the '370 patent recites:

> A system for storing data comprising:
>
> an MLC non-volatile memory space including at least one MLC non-volatile memory element;
>
> an SLC non-volatile memory module space including at least one SLC non-volatile memory element; and
>
> a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to:
>
> a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses,

wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;

b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data, and, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element.

199. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

200. The Accused Products include an MLC non-volatile memory space including at least one MLC non-volatile memory element. For example, as explained in Counts I and IV above, the Accused Products include MLC NAND flash, and this flash is addressed in an MLC non-volatile memory space.

201. The Accused Products include an SLC non-volatile memory module space including at least one SLC non- volatile memory element. For example, as explained in Counts I and IV above, the Accused Products include SLC NAND flash, including flash memory configured to operate in SLC mode, and this flash is addressed in an SLC non-volatile memory space.

202. The Accused Products include a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element. For example, as explained in Count I above, the Accused Products have a controller that manages reads and writes to and from the physical memory elements.

203. In the Accused Products, the controller is adapted to maintain an address map of the MLC and SLC non-volatile memory spaces. For example, as explained in Count I above, the controller in the Accused Products maintains an address map, for example in an L2P table or similar structure, that maps logical address ranges to physical addresses in the MLC and SLC memory.

204. In the Accused Products, the address map comprises a list of logical address ranges accessible by a computer system. For example, as explained in Count I above, the L2P or similar table in the Accused Products includes a list of logical address ranges such as blocks and pages.

205. In the Accused Products, the list of logical address ranges has a minimum quanta of addresses. For example, as explained in Count I above, the Accused Products employ a minimum quanta of addresses such as a block or page in the L2P table, and memory is mapped on a block or page granularity.

206. In the Accused Products, each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element. For example, as explained in Count I above, the table entries in the L2P or similar tables in the Accused Products map ranges of logical addresses to similar ranges of physical addresses in MLC or SLC NAND flash memory.

207. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in

the at least one MLC non-volatile memory element as stored data. For example, as explained in Count I above, the Accused Products include controllers that incorporate defect and error management technology, that use a variety of data integrity tests to determine when there is a data integrity problem, including for data stored in MLC flash memory. As explained in Count IV above, these data integrity tests use received data retained at the controller.

208. In the Accused Products, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element. For example, as explained in Count I above, the Accused Products, upon a data integrity failure, remap degraded data to the next available location. As explained in Count I above, the Accused Products move data from MLC to SLC in such situations.

209. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

210. Defendants' infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

211. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '370 patent by Defendants.

REQUEST FOR A JURY TRIAL

212. Vervain requests a jury trial of all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, Vervain respectfully requests:

A. That Judgment be entered that Defendants have infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents;

B. That, in accordance with 35 U.S.C. § 283, Defendants and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Asserted Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the Accused Products;

C. An award of damages sufficient to compensate Vervain for Defendants' infringement under 35 U.S.C. § 284;

D. That the case be found exceptional under 35 U.S.C. § 285 and that Vervain be awarded its reasonable attorneys' fees;

E. Costs and expenses in this action;

F. An award of prejudgment and post-judgment interest; and

G. Such other and further relief as the Court may deem just and proper.

Dated: May 10, 2024.

Respectfully submitted,

/s/ Alan L. Whitehurst

Alan L. Whitehurst
D.C. Bar No. 484873
awhitehurst@McKoolSmith.com
Nicholas T. Matich
D.C. Bar No. 1024907
nmatich@McKoolSmith.com
Christopher P. McNett
D.C. Bar No. 1500360
cmcnett@McKoolSmith.com
MCKOOL SMITH, P.C.
1999 K Street, NW, Suite 600
Washington, DC 20006
Telephone: (202) 221-6267
Facsimile: (212) 402-9444

John Campbell
Texas Bar No. 24036314
James E. Quigley
Texas Bar No. 24075810
jquigley@McKoolSmith.com
MCKOOL SMITH, P.C.
303 Colorado Street, Suite 2100
Austin, TX 78701
Telephone: (512) 692-8700
Facsimile: (512) 692-8744

Jennifer L. Truelove
Texas Bar No. 24012906
jtruelove@mckoolsmith.com
MCKOOL SMITH, P.C.
104 East Houston, Suite 300
Marshall, Texas 75670
Telephone: (903) 923-9000
Facsimile: (903) 923-9099

Attorneys for Plaintiff Vervain, LLC

CERTIFICATE OF SERVICE

The undersigned certifies that on May 10, 2024, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system.

/s/ Alan L. Whitehurst
Alan L. Whitehurst