UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,
Petitioner,

v.

VERVAIN, LLC,
Patent Owner.

IPR2025-00215
U.S. Patent No. 10,950,300

DECLARATION OF SUNIL P. KHATRI IN SUPPORT OF PATENT OWNER'S PRELIMINARY RESPONSE ON THE MERITS AND OTHER NON-DISCRETIONARY CONSIDERATIONS

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EXHIBIT LIST

Exhibit No.	Description
2001	Declaration of Dr. Sunil Khatri
2002	Chen et al., *Ultra MLC Technology Introduction*, Advantech Technical White Paper (Oct. 5, 2012) ("Chen")
2003	Excerpts from Micheloni et al., *Inside NAND Flash Memories* (1st ed. 2010) ("Micheloni")
2004	[RESERVED]
2005	[RESERVED]
2006	*Vervain v. Western Digital Corp. et al.*, No. 6:21-cv-488-ADA, Dkt. 41 (W.D. Tex. Jan. 24, 2022) (Claim Construction Order)
2007	[RESERVED]
2008	[RESERVED]
2009	[RESERVED]
2010	[RESERVED]
2011	[RESERVED]
2012	[RESERVED]
2013	[RESERVED]
2014	[RESERVED]
2015	[RESERVED]
2016	[RESERVED]
2017	[RESERVED]

Exhibit No.	Description
2018	[RESERVED]
2019	[RESERVED]
2020	[RESERVED]
2021	[RESERVED]
2022	[RESERVED]
2023	[RESERVED]
2024	[RESERVED]
2025	[RESERVED]
2026	[RESERVED]
2027	[RESERVED]
2028	[RESERVED]
2029	[RESERVED]
2030	[RESERVED]
2031	Preliminary Claim Constructions for *Vervain, LLC v. Phison Electronics Corporation*, No.1:24-cv-259-ADA and *Vervain, LLC v. Kingston Technology Company., et al*., No. 1:24-cv-254-ADA – email from Mr. Brown received on February 5, 2025.
2032	Markman Hearing Transcript dated February 6, 2025, for *Vervain, LLC v. Phison Electronics Corporation,* No. 1:24-cv-259-ADA and *Vervain, LLC v. Kingston Technology Company., et al.* No. 1:24-cv-254-ADA.
2033	[RESERVED]
2034	[RESERVED]

Exhibit No.	Description
2035	[RESERVED]
2036	[RESERVED]
2037	[RESERVED]
2038	[RESERVED]
2039	*Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00047, Paper 9 (P.T.A.B. Mar. 17, 2025) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,830,546)
2040	[RESERVED]
2041	*Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00048, Paper 9 (P.T.A.B. April 28, 2025) (Decision Denying Institution of Post-Grant Review of U.S. Patent No. 11,854,612)

DECLARATION OF SUNIL P. KHATRI, PH. D

I, Sunil P. Khatri, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained on behalf of Vervain, LLC ("Vervain"), and its counsel, McKool Smith, P.C., as an expert in this proceeding. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I understand that Vervain will submit this Declaration in connection with the Patent Owner's Preliminary Response in IPR2025-00215, which I have been informed is a *inter partes* review (IPR) proceeding challenging the patentability of the claims of U.S. Patent No. 10,950,300 ("the 300 Patent").

3. I receive compensation at an hourly rate of $800 per hour for my time working on this matter, plus expenses. I have no financial interest in Vervain or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The conclusions I present are due to my own judgment.

II. BACKGROUND AND QUALIFICATIONS

4. I have over thirty-eight years of experience with electronics, electrical engineering, and computer engineering. A copy of my latest curriculum vitae (CV) is attached hereto as Appendix A and provides further details regarding my

background and qualifications. During my career, I have acquired extensive knowledge and experience with VLSI circuits, computer architecture, testing, computer-aided design (CAD) algorithms and algorithm acceleration, logic synthesis, semiconductor memory, redundancy, synchronous and asynchronous circuits, and related software and hardware topics. Most relevant to the Asserted Patents, my technical expertise includes extensive work with semiconductor memory devices such as DRAM, SRAM and flash. My work with semiconductor memory devices has included work on 3D integration and novel ring-based memory architectures, power and speed tradeoffs using selective body bias, architectures and circuit approaches for processing-in-memory, radiation hardening analysis for memories, the use of flash transistors for designing logic circuits (such as ternary Content-addressable Memories (CAMs), Field Programmable Gate Arrays (FPGAs), and traditional binary-valued as well as ternary-valued digital logic, secure logic circuits, analog circuits like Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT) circuits, and in-memory mixed-signal computing architectures like Convolutional Neural Networks (CNNs)), and clocking and source-synchronous design. I recently was awarded a research grant by the Air Force Research Laboratory (AFRL) in Rome, NY, to conduct research in secure digital circuits using flash-based digital design approaches. Another recent research grant

from the National Science Foundation (NSF) funds research on the use of flash transistors for general purpose mixed-signal arithmetic. Additionally, I have lead-authored a book chapter on the use of flash transistors in novel Very Large Scale Integrated (VLSI) design applications. My MS thesis involved designing a memory interface for a multi-threaded Reduced Instruction Set Computing (RISC) microprocessor.

5. The following describes some of my relevant experience. I earned my Bachelor of Science in Electrical Engineering in 1987 from the Indian Institute of Technology, Kanpur, India. After graduating with my B.S. degree, I was a candidate for a Master of Science degree in Electrical and Computer Engineering at the University of Texas from 1987–89. At the University of Texas, I held the Microelectronics and Computer Development (MCD) Fellowship from 1987–89. I also conducted my M.S. research and wrote my thesis on the design of the METRIC memory interface and memory system. METRIC was one of the first super-scalar processors that was developed in the world. I earned an M.S. degree in 1989 from the University of Texas, Austin.

6. After leaving the University of Texas, I worked at Motorola Inc. from 1989–93 as a design engineer for the MC88110 reduced instruction set computing (RISC) microprocessor team. My duties included the design of digital and analog

circuitry, test logic and circuits, JTAG boundary scan design, input/output driver design, and clock phase-locked loop (PLL) logic. During my time at Motorola, I was independently responsible for the design of the factory test controller of the MC88110 microprocessor. I performed all attendant tasks in a "vertical" VLSI design methodology, which included high-level modeling, circuit and layout design and verification, as well as global and detailed routing. I also helped in the design of the Translation Lookaside Buffer (TLB) unit, which included a static random-access memory (SRAM) block.

7. In 1999, I earned a Doctor of Philosophy degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley. While at Berkeley, I held the California Microelectronics (MICRO) Fellowship in 1993.

8. I joined the faculty at the University of Colorado, Boulder, in 2000 as an Assistant Professor of Electrical and Computer Engineering. At the University of Colorado my research focused on VLSI logic design automation, VLSI layout design automation, and VLSI design methodologies to address Deep Submicron (DSM) issues such as crosstalk and power.

9. I joined the faculty at Texas A&M University in 2004 as an Assistant Professor in Electrical and Computer Engineering. In 2010 I was promoted to

Associate Professor in Electrical and Computer Engineering. In 2015, I was promoted to full Professor in Electrical and Computer Engineering. My research focuses on three primary areas: the first is computer systems, including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is logic and its applications, while the third area consists of interdisciplinary extensions of the first two. Some specific recent research topics include circuit design using floating gate (flash) devices, wireless power delivery and battery-less electronic systems, machine learning architectures, secure computing approached from both a hardware and software perspective, a formal framework for designing and verifying cryptographic hash functions, and extreme high-speed serial interfaces for Artificial Intelligence / Machine Learning (AI/ML) systems such as those used in Large Language Models (LLMs) like ChatGPT. One of my new focus areas is intelligent and secure computing viewed from the hardware (circuit) as well as the software levels. I have conducted research on tamper-proof memory techniques, as well as multi-row read architectures for SRAM, DRAM and flash memory arrays.

10. At Texas A&M I teach classes that cover memories extensively, featuring a thorough discussion of sense amplifiers, row and column decoders, and different types of memory circuits. For example, in Electrical and Computer

Engineering (ECEN) 752 "Advances in VLSI Circuit Design," a graduate level course, I cover all aspects of VLSI design, including memory design for various types of memories. In this course, (and also in ECEN 449/749 "Microprocessor System Design,"), I cover memories, including flash memories, the design of flash memory cells, the organization of memories into multiple banks, and the division of data across multiple banks of memory, as well as other design techniques that can be used to optimize and manage memories. The ECEN 449/749 course is attended by both undergraduate (ECEN 449) and graduate (ECEN 749) students. In ECEN 454 "Digital Circuit Design," a senior undergraduate course, I cover circuit design techniques for memory in detail. The Ph.D. thesis dissertation topic for 3 of my current Ph.D. students covers the use of flash memory transistors for analog and digital applications. The Ph.D. thesis of one of my recent doctoral students dealt with the use of flash transistors to design logic circuits. The research of a recent M.S. student entailed a new ring-based source synchronous architecture for 3D DRAM technologies, which has been published at a conference and in a journal and is being submitted for dissemination as a research monograph. In the past, I have conducted research into new topologies for efficient memory redundancy as part of a course project for my graduate course.

11. Since 2000, I have earned 24 research contracts from funders including Intel, the National Science Foundation, the National Security Agency, Altera Corporation, the National Center for Atmospheric Research, National Semiconductor Corporation, and several private sources. The total amount for these research grants is $17.53 million, of which my portion is $2.85 million.

12. I have a total of over 289 peer-reviewed publications. Among these papers, five received a best paper award, while seven others received best paper nominations (including one journal best paper nomination). An additional six journal papers and three conference paper are currently undergoing peer review. I have co-authored nine research monographs, one edited research monograph, and four book chapters. Additionally, I have seven awarded U.S. Patents (two of which were filed during my tenure at Texas A&M), two filed provisional U.S. Patents, and another U.S. Patent which is currently under review and was also submitted during my tenure at Texas A&M. I have co-authored one invited journal paper and 13 invited conference or workshop papers (including one from Design Automation Conference (DAC) and one from Allerton). Moreover, I was invited to serve as a panelist at a conference seven times and have presented four conference tutorials. I received the "Outstanding Professor Award" in the ECE Department at Texas A&M University in 2007 and also in 2020. In 2009 and in 2019, I received a university-level and a

college-level teaching award respectively, at Texas A&M. My H-index is 36 (per Google Scholar).

13. Since 2003, I have published numerous research monographs, journal papers, and conference papers on flash transistors and memory systems, as detailed in my CV attached in Appendix A. A few papers on relevant subject areas authored or co-authored by me include:

- *"A Novel Mixed-Signal Flash-based Finite Impulse Response (FFIR)"*, Lee, Khatri, Ghrayeb. Proc. of the 30th ACM Asia and South Pacific Design Automation Conference (ASPDAC) 2025. Tokyo, Japan, January 20-23, 2025. pp 1216-1222.
- *"Flash - A "Forgotten" Technology in VLSI Design*". Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed. ISBN: 978-3-031-16344-9;
- *"Flash – An Overlooked Technology in VLSI Design",* Khatri, Vrudhula. Monday Tutorial to be presented at the ACM/CEDA Design Automation Conference (DAC), San Francisco, CA, June 2024;
- "*A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors*", Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038, March 2024;

- "*An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency*", Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Jan 2024;
- "*A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors*", Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023;
- *"A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells",* Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022);
- *"CIDAN-XE: Computing in DRAM with Artificial Neurons"*, Singh, Wagle, Khatri, Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3, Feb 2022;
- *"An Extremely Low-Voltage Floating Gate Artificial Neuron",* Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023. Monterey, CA;
- *"A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator",* Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic Design (ISQED), April 5-7 2023. San Francisco, CA;
- *"A Flash-based Digital to Analog Converter for Low Power Applications",* Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), October 2022. Lake Tahoe, CA. pp 1-8;

- *"A Flash-based Current-mode IC to Realize Quantized Neural Networks",* Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe Conference, Mar 2022, Antwerp, Belgium. pp 1029-1034;
- *"CIDAN: Computing in DRAM with Artificial Neurons",* Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 349-356, Oct 2021, virtual conference;
- *"A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron"*, Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA. pp 141-148;
- *"Threshold Logic in a Flash"*, Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp 550-558. Nov 17-20, 2019;
- *"Fast, Ring-based Design of 3D Stacked DRAM"*, IEEE Transactions on Very Large Scale Integrated Circuits (TVLSI), IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.;
- *"Fast, Ring-Based Design of 3D Stacked DRAM"*, IEEE International Conference on Computer Design 2017: pp 665-672;
- *"Selective Forward Body Bias for High Speed and Low Power SRAMs"*, Journal of Low Power Electronics, Vol. 5, No. 2, Aug. 2009, pp. 185-95;

- *"Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias"*, IEEE/ACM Great Lakes Symposium on VLSI, May 10-12, 2009, Boston, MA, pp. 441-44;
- *"Modeling Dynamic Stability of SRAMs in the Presence of Single Event Upsets (SEUs)"*, IEEE International Symposium on Circuits and Systems, May 18-21, 2008, Seattle, WA, pp. 1788-91;
- *"Design of a Flash-based Circuit for Multi-valued Logic"*, Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada.
- *"SAT-Based Optimization for Flash-Based Digital Designs"*, IEEE/ACM Design Automation Conference (DAC), Jun 18-22 2017, Austin, TX.
- *"A Flash-based Digital Circuit Design Flow",* IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.
- *"Implementing low power digital circuits using flash devices"*, 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.
- *"Exploring Flash Devices to Implement Digital Circuits"*, IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.
- *"FTCAM: An Area-efficient Flash-based Ternary CAM Design"*, IEEE Transactions on Computers, Vol. 65, No. 8, Aug. 2016, pp. 2652-58;
- "*An Area-efficient Ternary CAM Design Using Floating Gate Transistors"*, IEEE International Conference on Computer Design, Oct. 19-22, 2014, Seoul, S. Kor., pp. 55-60; and

- *"A Fast Ternary CAM Design for IP Networking Applications, International Conference on Computer Communications and Networks"*, October 22, 2003, Dallas, TX, pp. 434-39 (awarded best paper).
- *U.S. Patent 12057831*: "Threshold logic gates using flash transistors", Vrudhula, Khatri. Issued August 2024

14. In addition to my work on the papers listed above, I have also served as an editor for IEEE Transactions on Computers, ACM Transactions on Design Automation of Electronic Systems, and MDPI Journal of Electronics.

15. I have served as EDA Track Co-Chair for ICECS 2014, Panel Chair for TexasWISE 2014, Track Co-Chair (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, Poster Session Chair for TexasWISE 2013, Advisory Committee for HotPI 2013, Panel Session Chair for SLiP 2013, Track Chair (Logic track) for ICCAD 2009-10, 2015-17, Track Chair (logic track) for DAC 2016-17, General Chair for IWLS 2009, Technical Program Chair for IWLS 2008, Track Co-Chair, Computer Aided Network DEsign (CANDE) Track, for ISCAS 2008-10, Track Co-Chair, Test and Methodologies Track, for ICCD 2007, Panel Chair for ITSW 2009, Publicity Co-Chair for GLS-VLSI 2009, and as a member of the TPC for several conferences.

16. I am generally familiar with the analysis of patents. I am a named inventor on the following U.S. Patents:

- Data Processing System Having Serial Self Address Decoding and Method of Operation, United States Patent No. 5,347,523, issued September 13, 1994;
- Circuit Identifier for Use with Focused Ion Beam Equipment, United States Patent No. 5,408,131, issued April 18, 1995 ("the '131 patent");
- Driver Circuit with Self-Adjusting Impedance Matching, United States Patent No. 5,448,182, issued September 5, 1995 ("the '182 patent");
- Circuit Identifier for Use with Focused Ion Beam Equipment, United States Patent No. 6,156,579, issued December 5, 2000 ("the '579 patent);
- Datapath Design Methodology and Routing Apparatus, United States Patent No. 6,598,215, issued July 22, 2003;
- Low Power Reconfigurable Circuits with Delay Compensation, United States Patent No. 7,880,505, issued February 1, 2011.
- U.S. Patent 12057831: *"Threshold logic gates using flash transistors"*, Vrudhula, Khatri. Issued August 2024.

17. The '831 patent discloses a method to design logic gates which implement a class of logic functions called threshold functions, using flash transistors.

18. The '131 and '579 patents are directed to an identification means for redundant circuits that distinguishes said circuits by respective function. This allows

for identification by focused ion beam equipment, which can then repair, replace, or supplement circuits as necessary. These patents disclose a scheme for replacing defective cells or circuits within a larger circuit.

19. The ’182 patent relates to a driver circuit capable of switching from one driving impedance to a second in response to the output signal of a first driver portion reaching a predetermined voltage. It discloses a driver circuit capable of adjusting circuit configurations depending upon the current output state.

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

20. I have been retained by Vervain (“Patent Owner”) to provide an explanation to the Board regarding the invention described and claimed in the 300 Patent. I understand Petitioner Phison Electronics Corporation (“Phison” or “Petitioner”), has filed a petition for inter partes review, No. IPR2025-00215, against the 300 Patent. I have been retained to provide my opinions regarding various technical issues relating to the validity of the challenged patent, including with regard to the validity of the challenged patent over the prior art references identified by Phison’s petition.

21. In preparing this Declaration, I am relying on my own knowledge and expertise as well as the following documents:

- U.S. Patent No. 10,950,300 (Ex. 1001) to G.R. Mohan Rao (“300 Patent”);

- Phison's petition for inter partes review (IPR2025-00215, Paper No. 2), as well as the declaration of Dr. Carl Sechen (Ex. 1002) submitted in support thereof;
- The exhibits cited in Phison's petition for inter partes review (IPR2025-00215, Paper No. 2);
- The alleged prior art references relied upon in Phison's petition;
- Any other documents discussed within this Declaration.

IV. PERSON OF ORDINARY SKILL IN THE ART

22. When interpreting a patent, I understand that it is important to view the disclosure and claims of that patent from the level of ordinary skill in the relevant art at the time of the invention, which I have been asked to initially consider as the 2011 time frame, including and up to July 19, 2011, which is the filing date of Provisional Application No. 61/509,257, which I am informed is a provisional application to which the 300 Patent claims priority. I am informed that the 300 Patent was filed June 12, 2018, and my opinions and analysis are still applicable if the June 12, 2018 date is considered as the time of the invention. My opinion of the level of ordinary skill in the art with regard to the challenged patent is based on my personal experience working and teaching in the fields of electrical engineering and computer science, including work with memory technologies, my knowledge of the background and education of colleagues and others working in that general field as

of and for several years prior to the 2011-2012 time frame, my study of the challenged patent, and its file history, and my knowledge of:

- The level of education and experience of persons actively working in the field at the time the subject matter at issue was developed;
- The types of problems encountered in the art at the time the subject matter was developed;
- The prior art patents and publications;
- The activities of others working in that same technical field;
- Prior art solutions to the problems addressed by the relevant art; and
- The sophistication of the technology at issue in this case.

23. In determining the level of ordinary skill in the art, I also considered the following factors: (1) the sophistication of the relevant technology; (2) the rapidity with which innovations are made in that field; and (3) the educational level of active workers in that field. It is my further understanding that these factors are not exhaustive and are merely a useful guide to determining the level of ordinary skill in the art.

24. Taking the above factors into account, in my opinion a person of ordinary skill in the art (POSA) in the technology field of the 300 Patent would be a person with at least a Bachelor of Science degree in electrical engineering, computer engineering, or a closely related field, with at least 3-5 years of experience in the design of non-volatile memory devices. An individual with an advanced degree in

a relevant field would require less experience in the design of non-volatile memory devices.

25. I understand that Phison's expert, Dr. Carl Sechen, provided a different definition for the POSA. I understand that Dr. Sechen's definition is as follows:

> In view of this instruction, my experience with the issues, and the '300 specification, in my opinion, a person of ordinary skill in the art at the time of the claimed inventions would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well.

Ex. 1002, ¶64.

26. For the limited purpose of this declaration, I rely on the definition of the POSA provided by Dr. Sechen. My opinions in this declaration would remain unchanged if I had adopted my definition of the POSA. At the time of the invention, I qualified as a POSA under either definition.

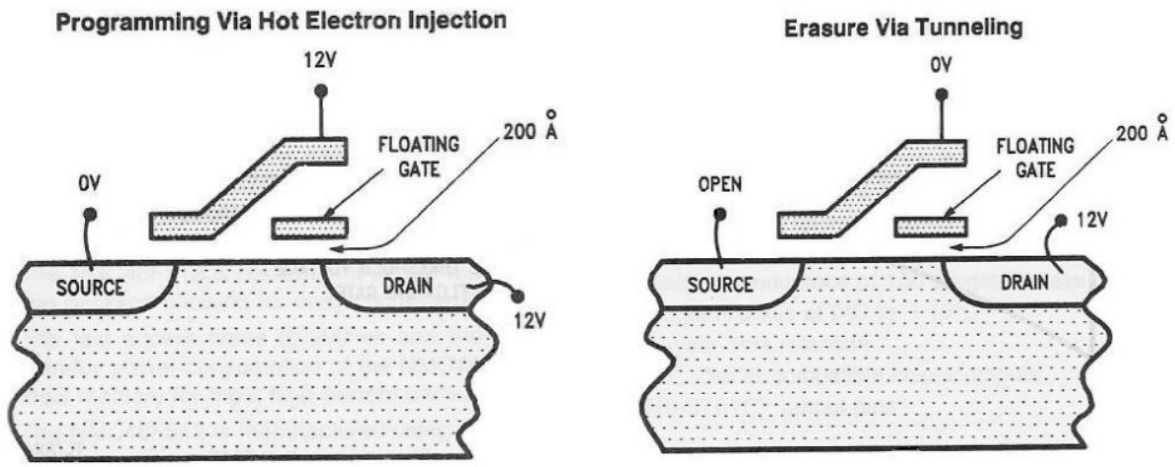
V. GENERAL BACKGROUND OF THE RELEVANT TECHNOLOGY

27. Volatile memory technologies, such as static random access memory ("SRAM") and dynamic random access memory ("DRAM"), lose their contents when power is turned off. However, persistent (non-volatile) memory is needed for many applications, such as storage for photos in a digital camera, bootable code or

settings in desktops, laptops or cellular phones, and a wide range of other applications. Non-volatile memories (e.g., thumb drives, hard drives, and compact discs) can store information even after the system is powered off. Traditionally, media such as hard disks, floppy disks, compact discs, or magnetic tapes was used for non-volatile storage in computing systems, but these media are large, bulky, and slow, and use a large amount of power. Flash memory is a specific type of non-volatile memory, where data is stored in "blocks" of "pages." Flash memory chips have come to be used for persistent data storage in a wide range of applications. Data stored in flash memory persists across power on/off cycles and has a small size, high performance, and low power consumption.

28. Flash memory uses a special type of transistor called a floating gate transistor. Such a transistor, in addition to a "control gate", also has a "floating gate". In a floating gate transistor, charge is stored on the floating gate, which is an isolated conductor. The floating gate cannot discharge, since it is in a high-impedance state. The charge on the floating gate controls the current flowing between the source and drain of the floating gate transistor, by altering the threshold voltage of the floating gate transistor. This current allows the user to determine the value stored in the cell. The charge stored in the floating gate is a proxy for the logical value stored in the flash memory cell that is implemented using the floating gate transistor.

29. To erase the cell, a reverse voltage is applied between the drain and the control gate. Charge is then dissipated through Fowler-Nordheim tunneling.



30. Floating gate transistors individually have limited endurance. Depending on the type of transistor and how it is configured, an individual transistor may not work reliably after it has been programmed and erased too many times. For example, the endurance for some flash transistors is on the order of 10,000 to 100,000 program-erase cycles.

31. Because of the limited endurance of floating gate transistors, and because some locations in a memory may be frequently rewritten, some floating gate transistors in the memory may wear out earlier than others. Therefore, flash memory typically includes a controller that uses a flash translation layer to map logical addresses presented to the host to physical addresses used to address the physical flash memory. This flash translation layer allows for wear to be leveled across all

the transistors on a device, and for bad blocks to be managed and avoided. This is done by changing the logical-to-physical address mapping.

A. SLC and MLC Flash

32. Early flash memory stored only a "0" or a "1" in each transistor. This is today known as "SLC," or "single level cell," flash. Later, to increase the density of storage in flash memory, a technique known as "MLC", or "multiple level cell," was introduced, where multiple threshold voltage levels were used in each transistor, to store multiple bits of data. For example, the following diagram shows how in SLC flash, there are large threshold voltage intervals between the "1" and "0" values, whereas in MLC flash, there are smaller voltage intervals between the multiple-bit logic values such as "11," "10," "01," and "00." The MLC flash design below stores 2 memory bits.

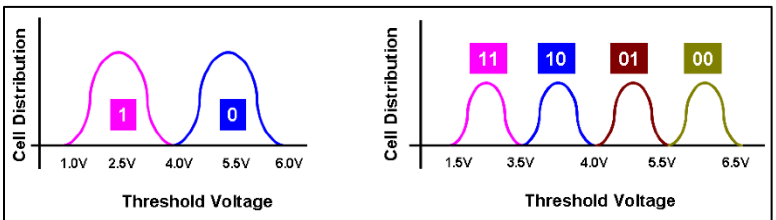


Figure 3: Cell Distribution vs. Threshold Voltage for SLC Flash (Left) and MLC Flash (Right), Respectively

Ex. 2002 (Chen et al., *Ultra MLC Technology Introduction*, Advantech Technical White Paper (Oct. 5, 2012)), 3.

33. The primary difference between SLC and MLC is what data each threshold voltage represents. With SLC flash, the transistor stores only a 1 or 0, so

a wide range of threshold voltages can be allotted to a single bit. This allows for faster and more reliable memory access. On the other hand, MLC flash must be slowly and carefully programmed to a narrower, more precise range of threshold voltages, with each threshold voltage range representing a specific pair of bits (see the figure above, which shows four pairs of bits—11, 10, 01, and 00—corresponding to different ranges of threshold voltages). As a result, the above MLC cell requires two successive read operations to determine which pair of bits were stored in it.

34. Flash memories sometimes use dual-mode flash, where the cells can be configured as SLC or MLC. When the cell is in SLC mode, it uses only two threshold voltages to store a single bit. Ex. 2003 (Micheloni), 511 (where a single NAND memory "has two sub sections, the first of them to be used as SLC, the other one as MLC", in which "[t]he partition is dynamic" and "the "SLC partition" has "a single distribution in the positive side of the threshold voltage values").

B. Address Table

35. To provide wear leveling, garbage collection, and bad block management, a translation layer is used to map logical addresses to actual physical locations. As part of this translation layer, "tables are widely used in order to map sectors and pages from logical to physical (Flash Translation Layer or FTL)." Ex. 2003 (Micheloni), 40. These tables map logical blocks to physical blocks. *Id*., 40-

42. Using a "block" or similar granularity is important, since flash memory is arranged so that when erasing and rewriting data, all the memory in a block is "erased together." *Id*., 22. Therefore, Dr. Rao explained that "[t]he address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum." Ex. 1001 (300 Patent), 5:54-58, Figs. 3A-B. Dr. Rao further explained that memory is written and mapped on the granularity of a "quantum," such as a block or page. *Id.*, 5:54-58.

C. Data Integrity Tests

36. When data is stored in MLC memory, it is more prone to errors, and some data is more prone to errors than other data. One reason for this is that the threshold voltage intervals for MLC memory are smaller than the corresponding intervals for SLC memory. Errors can occur when writing or reading the data. Errors can also be caused by the data stored in neighboring cells. A data integrity test is a test that checks the integrity of the data (*i.e*., whether errors have occurred). This test can be run immediately after data is written, or at a later time. If the test reveals a problem such as corrupt data, the data can be remapped to SLC (which is less error-prone) or less-used MLC, and the address table is modified accordingly. Ex. 1001, 3:13-3:35, 4:30-36.

VI. THE 300 PATENT

37. U.S. Patent No. 10,950,300 (the "'300 patent"), entitled "Lifetime Mixed Level Non-Volatile Memory System," issued on March 16, 2021 and relates to systems for storing data using SLC and MLC flash memory (*see supra* Section V.A for my discussion regarding SLC and MLC flash memory). I understand the challenged claims from the '300 patent are claims 1-12.

38. G.R. Mohan Rao is the sole named inventor of the 300 patent.

39. The Challenged Patent includes two independent claims, Claim 1 and Claim 12. Both independent claims require a "**random access volatile memory**." Claim 1 of the Challenged Patent requires:

Claim 1	
[1Pre]	A system for storing data comprising:
[1a]	memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
[1b]	at least one controller to operate memory elements and associated memory space;
[1c]	at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

[1d]	at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;
[1e]	at least one **random access volatile memory**;
[1f]	an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and **random access volatile memory**;
[1g]	the controller controlling access of the MLC and SLC nonvolatile memory elements and the **random access volatile memory** for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the **random access volatile memory**;
[1h]	the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the **random access volatile memory**;
[1i]	wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
[1j]	wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range

	of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

40. Claim 12 of the Challenged Patent requires:

Claim 12	
[12Pre] (same as [1Pre])	A system for storing data comprising:
[12a] (similar to [1a])	memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;
[12b] (similar to [1b])	at least one controller to operate memory elements and associated memory space, and to maintain an address table in one or more of the memory elements;
[12c] (similar to [1c])	at least one MLC nonvolatile memory element that can be mapped into the nonvolatile memory space;
[12d] (similar to [1d])	at least one SLC nonvolatile memory element that can be mapped into the nonvolatile memory space;
[12e] (same as [1e])	at least one **random access volatile memory**;

[12f] (same as [1g])	the controller controlling access of the MLC and SLC nonvolatile memory elements and the **random access volatile memory** for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the **random access volatile memory**;
[12g] (same as [1h])	the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the **random access volatile memory**;
[12h] (same as [1i])	wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and
[12i] (same as [1j])	wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

VII. CLAIM CONSTRUCTION

41. I understand that claim terms are typically given their ordinary and customary meanings, as would have been understood by a person of ordinary skill in the art (POSA) at the time of the invention. In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

42. Petitioner proposes construction of eight terms: "MLC non-volatile memory," "SLC non-volatile memory," "elements" or "memory element," "memory space," "controller/FTL," "mapping…to maximize lifetime," "remapping…and transfer…to achieved enhanced endurance," and "data integrity test." Petition, 22-25.

43. I understand that Petitioner proposes that "MLC non-volatile memory" means "non-volatile memory cells arranged with circuitry capable of storing multiple logical pages in a single physical page of cells." Petition, 23.

44. I understand that Petitioner proposes that "SLC non-volatile memory" means "non-volatile memory cells arranged with circuitry incapable of storing multiple logical pages in a single physical page of cells." Petition, 23.

45. I understand that Petitioner proposes that "elements" and "memory element" mean "physical locations mapped to their respective 'memory spaces' as

'logical address spaces'" and "physical flash memory block," respectively. Petition, 23.

46. I understand that Petitioner proposes that "memory space" means a "logical address space, subdivided by mapping to physical MLC and SLC memory." Petition, 24.

47. I understand that Petitioner proposes that "controller/FTL" is indefinite, but should nonetheless be "construed as customary for the POSITA." Petition, 24.

48. I understand that Petitioner proposes that "mapping…to maximize lifetime" is indefinite, but nonetheless "maximize lifetime" "means acting to avoid premature failure of a NAND flash component." Petition, 24.

49. I understand that Petitioner proposes that "remapping…and transfer…to achieved enhanced endurance" is indefinite, but nonetheless "enhancing endurance" "means acting to avoid premature failure of a NAND flash component." Petition, 24.

50. I understand that Petitioner proposes that "data integrity test" means "a test that compares stored data to retained data." Petition, 24.

51. While I disagree with all of Petitioner's proposed constructions, I am not presenting opinions about these terms in this declaration. I have been informed that claim construction is only performed in IPR proceedings to the extent that it

affects the outcome of the IPR proceeding. Here, I do not believe that any of Petitioner's proposed constructions that are identified above affect whether this IPR should be instituted because, as I explain below, Petitioner is wrong about numerous points unrelated to these proposed constructions.

VIII. PETITIONER'S INVALIDITY ARGUMENTS

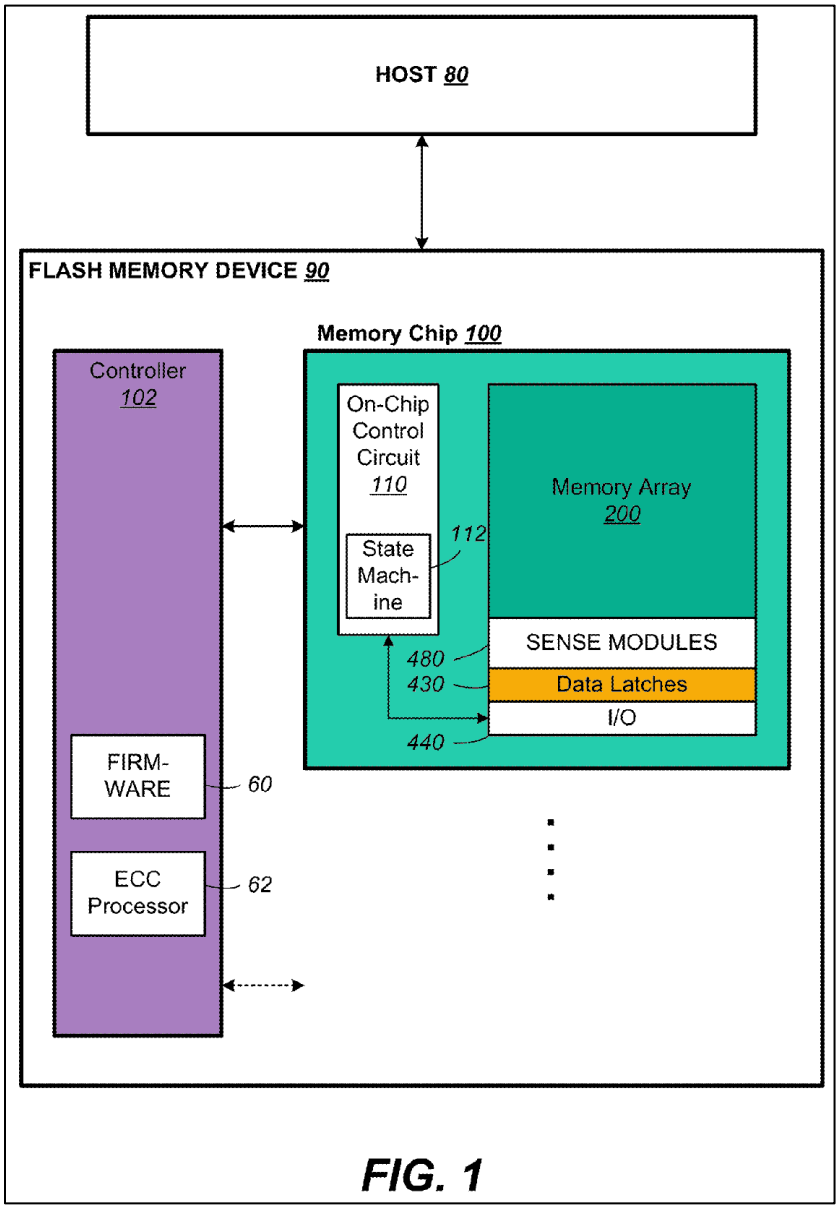
A. OVERVIEW OF THE PRIOR ART

52. I understand that Petitioner asserts that the challenged claims are obvious based on a single ground relying on a single reference: Petitioner alleges that Claims 1-12 are obvious over Gavens (U.S. Patent No. 8,634,240) (Ex. 1045) in view of the knowledge of a POSA. *See* Petition, 25-56. In its single ground, Petitioner also references some references that Petitioner contends Gavens "incorporates by reference," including: U.S. Patent Appl. Pub. No. 2011/0153912 ("Gorobets 912") (Ex. 1049), U.S. Patent Appl. Pub. No. 2010/0172180 ("Paley") (Ex. 1051), U.S. Patent No. 5,936,971 ("Harari") (Ex. 1057), and PCT Pub. No. WO 03/027828 ("Gorobets PCT") (Ex. 1058). I do not present opinions related to whether these references are "incorporated by reference" by Gavens in this Declaration; instead, as provided below, my opinions address whether these references describe distinct teachings/embodiments from Gavens, and whether a POSA would have combined teachings from these references with Gavens.

1. Gavens (Ex. 1045)

53. Gavens discusses a problem that occurs with flash memory (a type of non-volatile memory)—as it ages, its error rate increases. Ex. 1045, 3:56-4:5. To ensure data integrity in such situations, the memory traditionally uses a resource-intensive error correction code (ECC) provisioned to correct errors "at the end of life of the memory device." *Id*. Gavens explains that this poses a problem because, "for most of the life time of the device [(before the device ages and the error rate increases)], the ECC is only marginally utilized, resulting in its large over-heads being wasted[.]" *Id.*, 3:67-4:2.

54. To perform ECC, Gavens describes a flash memory device including **controller 102** (highlighted purple) and **memory chip 100** (highlighted teal).



Ex. 1045, Fig. 1, 8:13-39. The memory chip includes an ***on-chip*** control circuit 110 with state machine 112. The memory chip also includes input/output (I/O) circuits, **data latches 430**, sense modules, and a non-volatile flash **memory array 200**. *Id.*, 4:13-16, 8:13-39. In contrast to the 300 Patent, there is no mention of RAM in the memory chip 100, controller chip 102, or anywhere else in the flash memory device

90. In fact, the only time that Gavens mentions RAM is in the "Background of the Invention," when Gavens is *distinguishing* its purported invention from RAM. *Id*., 1:26-29 ("Unlike RAM…that is also solid-state memory, flash memory is non-volatile"). As a result, a POSA would understand that the flash memory device 90 of Gavens does not include RAM.

55. Before writing a page of data to the memory array, "ECC is computed for the data page" by the ECC Processor 62. *Id.*, 12:51-63. The page of write-data then consists of two portions: the "user data" and the computed ECC. *Id.*

56. When a page is read from the memory array, it is "shifted out" (or "toggled") to **controller 102**. There, "the data page's existing ECC is compared to a second version of the ECC computed on the read data [(the "user data")]". The ECC first runs an error detection code (EDC) which "indicates the existence of any errors in the read data page[,]" and if there are errors, "the ECC is invoked to correct erroneous bits in the read data page." *Id.*, 12:64-13:8.[1]

[1] This EDC/ECC relies entirely on data that is read from the non-volatile memory array. Thus, unlike Dr. Rao's invention, this EDC/ECC does not involve a comparison of data read from the non-volatile memory with data *retained* in volatile memory (such as RAM). Since Gavens does not use RAM, it simply could not perform the comparison in the manner that the 300 Patent teaches.

57. Gavens teaches that using ECC in this way—where the ECC must be programmed to correct the "worst-case" number of bits—is burdensome in terms of processing time as well as chip area on the controller:

> Using ECC to correct a worst-case number of error bits will consume a great amount of processing time. The more bits it has to correct, the more computational time is required. The memory performance will be degraded. Additional dedicated hardware may be implemented to perform the ECC in a reasonable amount of time. ***Such dedicated hardware can take up a considerable amount of space on the controller ASIC chip.*** Moreover, for most of the life time of the device, ***the ECC is only marginally utilized***, resulting in its large over-heads being wasted and realizing no real benefits.

Ex. 1045, 3:60-4:2; *see also id.*, 5:15-30, 13:9-16.

58. To address this problem, Gavens discloses the embodiments of Figures 14A-14B and 16A-16C, which describe the **memory array 200** of Figure 1 in greater detail. *See id.*, 8:13-15 ("Fig. 1 illustrates…a memory device in which the features of the present invention are embodied.").

59. These embodiments rely on a memory with a first SLC portion (which is less error prone) and a second MLC portion (which is more error prone). Gavens explains that optimizing where data is stored (in the SLC or MLC portion) based on the expected number of error bits "allows a smaller and more efficient…ECC…to

be designed for correcting a smaller number of error bits, thereby improving the performance and reducing the cost of the memory." *Id.*, 4:28-31, 12:6-10, 12:39-46, 16:22-24.

a) First Embodiment (Fig. 14A-14B)

60. Gavens describes a first embodiment with respect to Figures 14A-14B. *See id.*, 17:24-26 (referring to "the embodiment described in Fig. 14A and Fig. 14B"). *See also id.,* 16:14-16. For this embodiment, as shown in Figure 14B below, Gavens describes a memory array that relies on a "**lower density**" first portion 410 (*i.e.*, SLC) and a "**higher density**" second portion 420 (*i.e.*, MLC). *Id.*, 4:13-19, 16:14-28, 12:6-10, 12:39-46. The MLC portion is more error prone than the SLC portion but can be used "for efficient storage." *Id.*, 4:16-19, 16:41-45. Gavens explains that data can first be written to the MLC portion, then "read back in a post-write read operation to check for excessive error bits." *Id.*, 4:19-21; *see also id.*, Fig. 14A, 16:41-56. This is performed within the memory chip 200, as described later in this declaration.

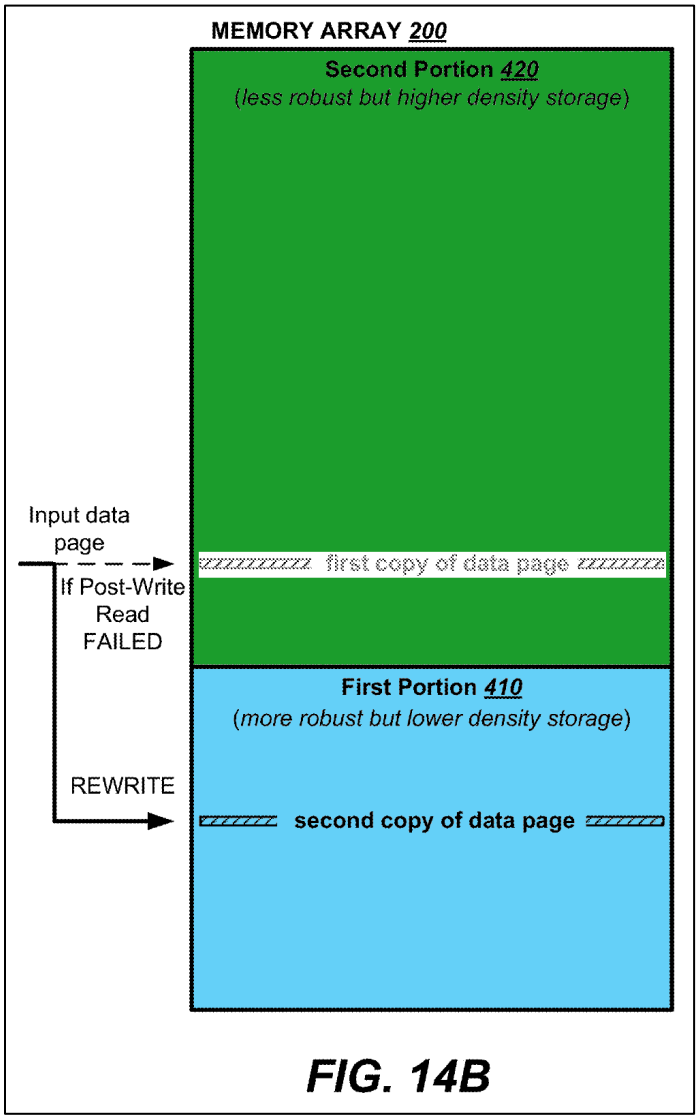


FIG. 14B

61. Gavens explains that the post-write error detection process can check for errors in one of two ways: "either by comparison with the original copy which may be cached or by checking the EDC portion of the ECC." *Id.*, 16:46-49. While Gavens at 16:46-49 does not specify how the "original copy" is cached, Gavens later explains that "[i]n the preferred embodiment" (where the antecedent basis of "the" refers to the immediately preceding "preferred embodiment" of Figures 14A-14B)

the "data is cached in [a] first section of the first portion" of non-volatile memory (*i.e.*, a section of the non-volatile SLC memory). *Id.*, 18:1-8 ("In the preferred embodiment, the first portion is further provided with ***a first section*** and a second section. The incoming data is cached in ***the first section*** of the first portion and a first copy of the data is written to the second portion."); *see also id.*, 16:14-16. Gavens does not describe caching the "original copy" in volatile memory.[2] A POSA would see this as a practical choice, since SLC memory is faster and more reliable than MLC, and would therefore serve as a good candidate as a cache for the MLC data.

62. Once the number of error bits is determined, the device determines whether to keep the data in MLC or instead move it to SLC. If the stored data has an acceptable number of error bits, then the stored copy remains in the MLC and becomes the "valid" copy. *Id.*, 16:41-56. "If the error bits exceeded a predetermined amount, the data is" instead stored in "the less error-prone" SLC portion. *Id.*, 4:21-22; *see also id.*, Fig., 14B, 17:7-20, 18:1-8. To rewrite the data, Gavens teaches that the memory may rely on the "cached" copy of the original data or obtain the data by

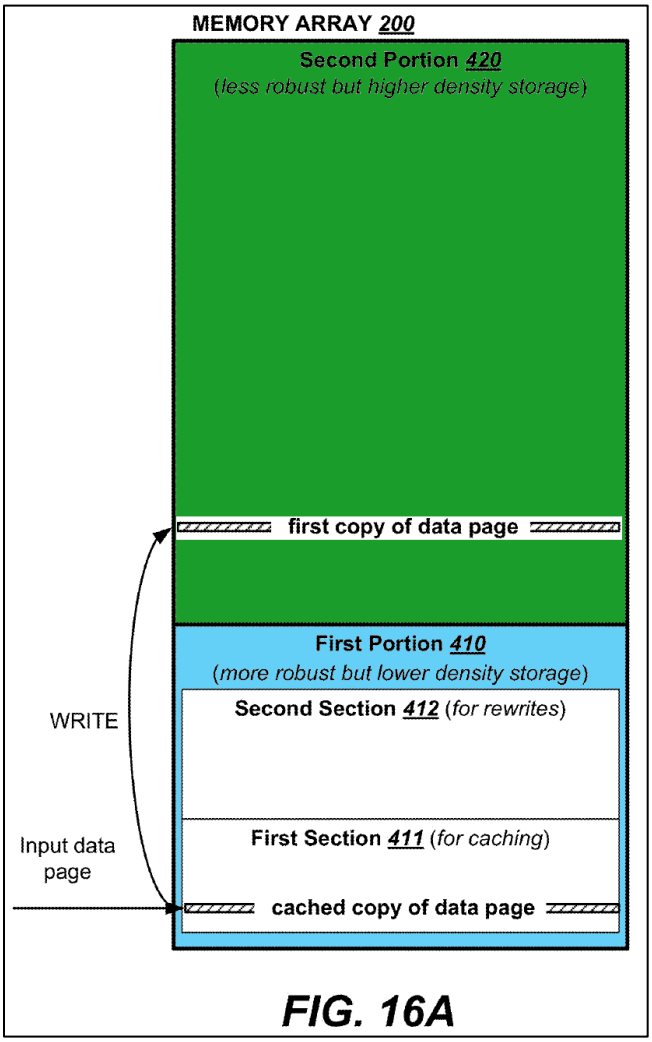
[2] In fact, Gavens does not refer to volatile memory in the disclosure, other than to distinguish the disclosure from RAM (a type of volatile memory). Ex. 1045, 1:26-29.

"correcting the errors bits [from the copy stored in the MLC] with the ECC." *Id.*, 17:12-14; *see also id.*, 18:1-8.

b) Second Embodiment (Fig. 16A-16C)

63. Figures 16A-16C depict a second embodiment. *See id.*, 7:26-28 (referring to "the embodiment described in Fig. 16A to Fig. 16C"). For this embodiment, Gavens, as is explained further below, teaches splitting the first portion (i.e. the SLC portion) into a first cache section and a second section for rewriting data. *Id.*, 18:9-23. Gavens emphasizes that this approach avoids making the comparison at the controller 102, which is a separate chip in the flash memory device 90. *Id.,* Fig 1, 18:36-39.

64. As shown in Figure 16A below, Gavens explains that the lower density First Portion 410 (*i.e.*, SLC) includes two sections—a "first section" 411 for caching write data, and a "second section" 412 for rewriting data from the higher density Second Portion 420 (*i.e.*, MLC). *Id.*, 18:9-23.



65. Incoming data is written both to the MLC and as a "cached copy" to the first section of the SLC. *Id.*, 18:21-29. Detecting the number of error bits is then "accomplished by comparison [of the data written to MLC] with the cached copy." *Id.*, 18:40-44.

66. Gavens specifies that this comparison may be performed at the **data latches 430** (highlighted orange in Figure 1 above) on the **flash memory chip 100**. *Id.*, 18:30-39. Gavens strongly recommends using **data latches 430** because it

eliminates the need to "toggle" the data out to the **controller chip 102**, as would be required if one were to use ECC Processor 62 for EDC-based error detection. *Id*., 18:36-39. Toggling or transferring the data to the controller chip 102 (a separate chip than the memory chip 100 on the flash memory device 90) would require a large delay, power and energy consumption. Gavens explains that "much time can be saved" by eliminating the need to toggle data to the controller chip, thus increasing the performance of the device. *Id*.

67. If there is an acceptable number of error bits, the MLC portion becomes the "valid" copy and the cached copy in the first section of the first portion is obsoleted. *Id.*, 18:45-52, Figure 16B. If there is an unacceptable number of error bits, the "cached copy" in the "first section" of the SLC is rewritten to the "second section" of the SLC which is designated "for rewrites". *Id.*, 18:53-67, Figure 16C.

68. By caching the data in the non-volatile memory array and using the latches to compare the data, Gavens lowers overhead and reduces the reliance on the controller chip. *Id.*, 18:40-67.

2. Other References Which Gavens Purportedly "Incorporates By Reference," Related To Random Access Volatile Memory

a) Gorobets 912 (Ex. 1049)

69. Like Gavens, Gorobets 912 includes a non-volatile memory with SLC and MLC portions. Gorobets 912 describes using the non-volatile SLC as a cache to aggregate data before it is written to MLC.

70. As shown in Figure 11 below, Gorobets 912 describes a Flash Memory Device with an **SLC portion** and an **MLC portion**. Ex. 1049, ¶¶104, 105, 109. The "second portion 204 has the memory cells operating as a cache in a binary mode", indicating that it is an SLC cache. *Id.,* ¶109. The **SLC portion** acts as "a cache for data to be written to the **[MLC] memory**." *Id.*, ¶104; *see also id.*, ¶108 (explaining the utility of the non-volatile SLC cache).

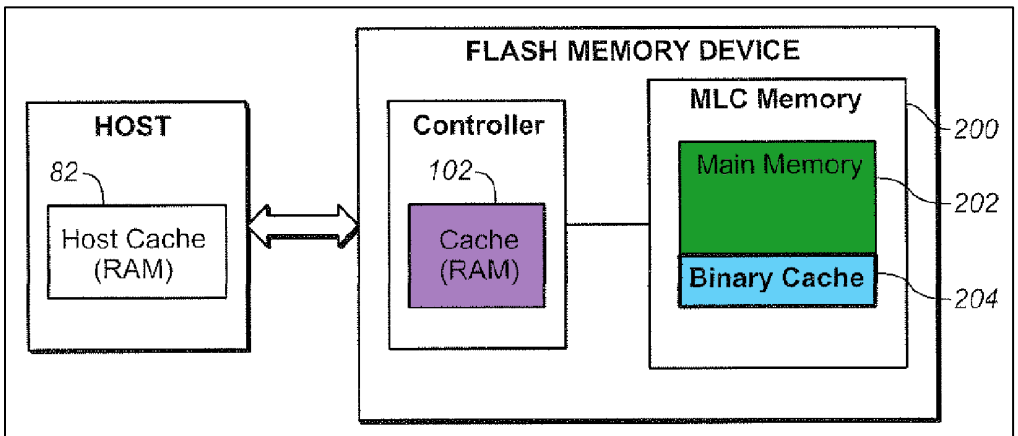


FIG. 11

71. The Flash Memory Device also relies on a controller, including a generic volatile **RAM-based cache** 102. Gorobets 912 explains that this **cache** is "high-speed storage for ***temporarily*** storing data being passed between a high-speed and slower-speed component of the system." *Id.*, ¶109 (emphasis added); *see also*, *id.*, ¶130.

b) Paley (Ex. 1051)

72. Paley is a reference that is related to Gorobets. These references share multiple named inventors. *Compare* Ex. 1051, Cover (listing inventors, including "Sergey…Gorobets") *with* Ex. 1049, Cover (listing inventors, including "Sergey…Gorobets"). Additionally, much of these references' disclosure is substantially the same. *Compare* Ex. 1051, Figure 15 *with* Ex. 1049, Figure 11 (other than differences in numbering, these figures are the same).

73. As shown in Figure 15 below, Paley describes a non-volatile memory with **SLC** and **MLC** portions, where the **SLC portion** is used as a cache to aggregate data before it is written to **MLC**. Ex. 1049, ¶192 ("A second portion forms a cache for data to be written to the main memory."), ¶193 ("In the preferred embodiment, individual cells in the cache portion are each configured to store one bit of data while the cells in the main memory portion each stores more than one bit of data.").

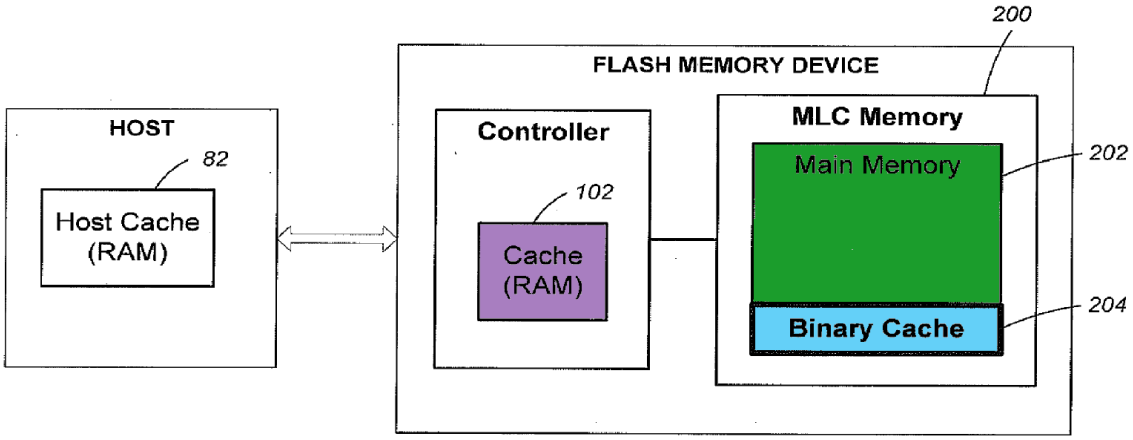


FIG. 15

Ex. 1051, Fig. 15 (annotated); *see also* Ex.1049, Fig. 11 (Gorobets 912's Figure 11 is substantially the same as Paley's Figure 15).

74. Paley additionally describes where the controller includes a generic volatile **RAM-based cache**. Like Gorobets 912, Paley explains that this **cache** is "high-speed storage for ***temporarily*** storing data being passed between a high-speed and slower-speed component of the system." Ex. 1051, ¶197 (emphasis added); Ex. 1049, ¶109 (same).

75. Therefore, unlike the Challenged Claims, Gorobets 912 and Paley both describe a memory system including a **RAM-based cache** that only temporarily stores data being passed between components.

c) Harari (Ex. 1057)

76. Harari describes a RAM "cache buffer" "for temporarily holding write data files." Ex. 1057, Fig. 8 (including "cache buffer 705"), 13:29-30. It acts as a "buffer" because it holds data before it is written to a non-volatile memory. *See id.*, 14:1-38. When "the cache memory 705…start[s] to fill up[,]" it preferentially writes ("archive[s]") infrequently written files to the flash non-volatile memory. *Id,* 14:26-30. "In this way, only infrequently used data files are written into the Flash memory while frequently used data files are trapped in the cache memory." *Id.*, 14:22-25. Harari's "cache buffer" therefore "reduce[s] the number of writes to the Flash…memory[.]" *Id.*, Abstract.

d) Gorobets PCT (Ex. 1058)

77. Like Gorobets 912, Paley, and Harari, Gorobets PCT also describes a volatile RAM-based buffer used to ***temporarily*** store data. Ex. 1058, 11:10-13 (describing "SRAM block 30 [that] stores all ***temporary*** information within the controller") (emphasis added). Data "being transferred" from system components to a flash memory "is ***buffered*** in the SRAM 30." *Id.*, 11:21-23 (emphasis added). Accordingly, unlike the Challenged Claims, Gorobets 912, Paley, Harari, and Gorobets PCT all disclose RAM-based caches that ***temporarily*** store (or buffer) data before it is written to flash.

B. GROUND 1: GAVENS DOES NOT DISCLOSE OR SUGGEST ALL OF THE FEATURES OF CLAIMS 1 AND 12

78. In my opinion, the Petition's analysis of why Gavens in view of the knowledge of a POSA discloses or suggests claims 1 and 12 is deficient. I address some of those deficiencies in Petitioner's analysis below.

1. [1d] and [12d]: "at least one *SLC nonvolatile memory element* that can be mapped into the SLC memory space"

79. Limitation [1d] recites: "at least one SLC nonvolatile memory element that can be mapped into the SLC memory space." In my opinion, Petitioner fails to show that Gavens discloses this limitation as claimed.

80. For this limitation, I understand that Petitioner relies only on its own construction for "SLC non-volatile memory": "non-volatile memory cells arranged with circuitry incapable of storing multiple logical pages in a single physical page of cells." Petition, 23. Applying this construction, Petitioner suggests that limitation [1d] requires a "'***native***' SLC flash chip." Petition, 31. While I disagree with construction, even if it is applied (I note that Petitioner presents its ground based solely on its own construction), in my opinion Petitioner's ground fails.

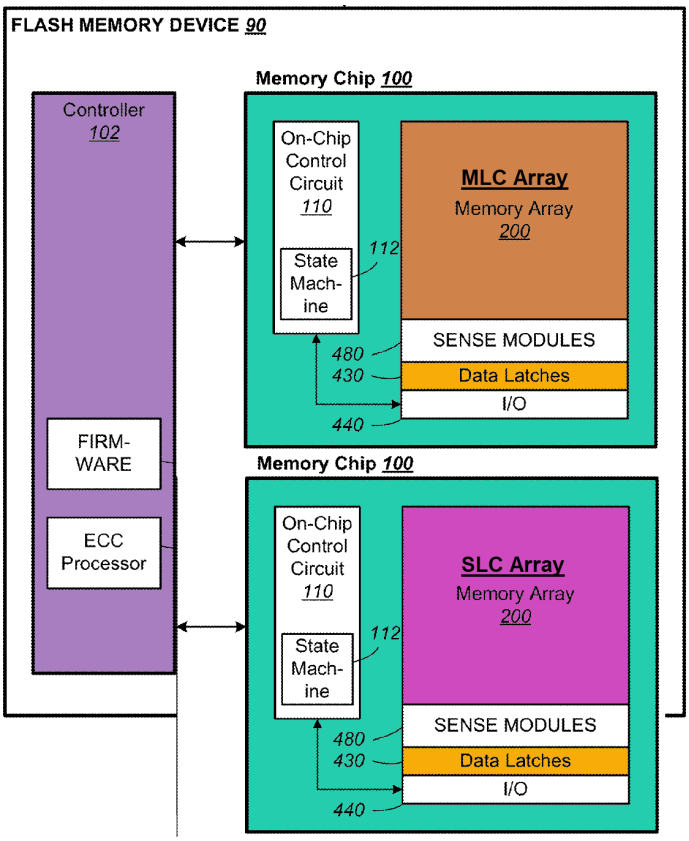
81. In my opinion, Petitioner does not sufficiently explain why it would have been obvious to a POSA to substitute one of Gavens's SLC memory *portions* (operating in SLC mode, or "pseudo-SLC") with a "'native' SLC flash chip."

Petition, 31-32. Instead, Petitioner provides a conclusory statement that cites paragraph 91 of Dr. Sechen's expert report; Petitioner states: that "***[a]s explained in [Sechen ¶ 91]***, it would be obvious to a POSITA to substitute a 'native' SLC flash memory module for the Gavens first portion, with a similar, if not wider margin of error than binary mode operation of MLC (see [Sechen ¶ 49]) and achieve similar, if not better results with the same NAND flash controller…with assurance of success." Petition, 31 (emphasis added).

82. As an initial matter, Sechen ¶91 does not say anything about a POSA substituting a "native" SLC flash memory module for the Gavens first portion. Further, considering Petitioner's analysis, in my opinion, Petitioner fails to explain why a POSA would have been motivated to make the suggested modification. Petitioner alleges that this "substitut[ion]" would yield "similar" results but does not explain why a POSA would have had this opinion, or even considered it to begin with.

83. In my opinion, instead, a POSA would not have been motivated to substitute one of Gavens's SLC portions—which, along with the MLC portion, makes up the memory array of one of Gavens's memory chips—with an entirely separate "**native SLC flash chip**." This is illustrated in the annotated version of Gavens's Figure 1 below. As shown below, in my opinion, Petitioner's proposed

modification would result in **one memory chip consisting entirely of MLC**, and **another memory chip consisting entirely of (native) SLC**.



Ex. 1045, Figure 1 (annotated to include a second memory chip comprising the "SLC array").

84. In my opinion, Gavens teachings do not support this modification/substitution. Gavens explains that each of its memory chips are already capable of operating with one portion as MLC, and another portion as SLC (albeit, not "native" SLC). *See* Ex. 1045, Abstract, 4:13-31, 6:17-25, 15:62-16:12, 16:17-25, Fig. 14, Fig. 16. In my opinion, that is a core of Gavens's invention—***in a single***

memory chip, taking advantage of the efficiencies of MLC storage, by relying on a "less error-prone" SLC ***portion*** when an MLC portion has too any errors. *See id.*, 4:13-31, 4:18-22 ("Data is written to the second portion for efficient storage. Afterwards, the data is readback in a post-write read operation to check for excessive error bits. If the error bits exceeded a predetermined amount, the data is rewritten or kept at the less error-prone first portion."), 15:66-16:13, 16:41-45.

85. Furthermore, Gavens explains that the SLC portion is also used to cache data, as described in its first and second embodiments (*see* above Section VIII.A.1), to avoid needing to "toggle[]" data out to **controller 102** when checking data written to the MLC portion for errors. *See* Ex. 1045, 18:21-39, 18:36-39. Gavens explains that this is because "**data latches**" ***within the memory chip*** (which includes ***both the MLC and SLC portions***) enable data comparison without relying on data being transferred to ***external*** **controller 102** to perform ECC. *See id.*, 18:30-39, Fig. 1 (showing "Data Latches" 430 as part of the Memory Chip, on a separate chip as compared to the Controller 102). Gavens explains: "By not making the comparison at the controller, the data does not have to be toggled out to the controller, [and] much time can be saved. Fig. 1 shows the data latches 430, ***which is on-chip***, for the data comparison to take place." Ex. 1045, 18:36-39 (emphasis added).

86. In my opinion, a POSA would know that replacing the SLC portion of the ***same*** memory chip with a ***separate*** SLC chip connected to the controller 102 would negate this benefit, as data cached in a **separate SLC chip** would need to be toggled out to the **controller** for comparison with data stored in the **MLC chip**. Even if the data cached in the **separate SLC chip** was transferred to the **MLC chip** for comparison, such an operation would require toggling data between the SLC and MLC chips. Thus, in my opinion, Gavens teaches away from Petitioner's proposed modification, and a POSA would not have been motivated to substitute an SLC portion of a memory chip with a separate "'native' SLC flash chip," as this modification would undermine Gavens's intended advantage—efficiently utilizing higher-density MLC memory.

87. Additionally, I understand that limitations [12d] and [1d] are similar, and Petitioner relies on the same ground for both limitations. *See* Petition, 54. Therefore, the Petition's analysis of limitation [12d] is inadequate for the same reasons as those given above for limitation [1d].

2. [1e] and [12e]: "at least one *random access volatile memory*"

88. Limitation [1e] recites: "at least one random access volatile memory."

89. In my opinion, for this limitation, Petitioner does not demonstrate how Gavens and its allegedly incorporated references—Gorobets 912, Paley, Harari, and

Gorobets PCT—disclose wherein the system for storing data includes "at least one random access volatile memory element." Petition, 32-34. In my opinion, Petitioner's ground does not clearly identify which aspect of the prior art is being mapped to this limitation, and instead Petitioner's ground ambiguously references disclosures from Gorobets 912, Paley, Harari, and Gorobets PCT that are unrelated, and different embodiments than the cited disclosure of Gavens. Thus, in my opinion, Petitioner does not demonstrate how the allegedly incorporated references' disclosure of RAM-based buffers applies to or can be combined with Gavens.

90. ***First***, I understand that Petitioner in its ground does not allege that Gavens itself discloses the "at least one random access volatile memory element." Petition, 32-34. In my opinion, Gavens does not disclose or suggest that its system includes RAM. In fact, Gavens explicitly distinguishes its teachings from systems that use RAM, explaining how "nonvolatile storage" is "***unlike*** RAM." Ex. 1045, 1:26-29 ("Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retaining its stored data even after power is turned off."). This is consistent with Gavens's description of its system in Figure 1, as shown below, which includes only the ***non-volatile*** "Memory array 200." *See* Ex. 1045, 1:17-20 ("This application relates to the operation of re-programmable ***non-volatile memory systems*** such as semiconductor flash memory, and, more

specifically, to handling and efficient managing of errors in memory operations.") (emphasis added), 4:13-16 ("According to a general aspect of the invention,…a ***flash*** memory having an array of memory cells is configured with a first portion and a second portion.") (emphasis added).

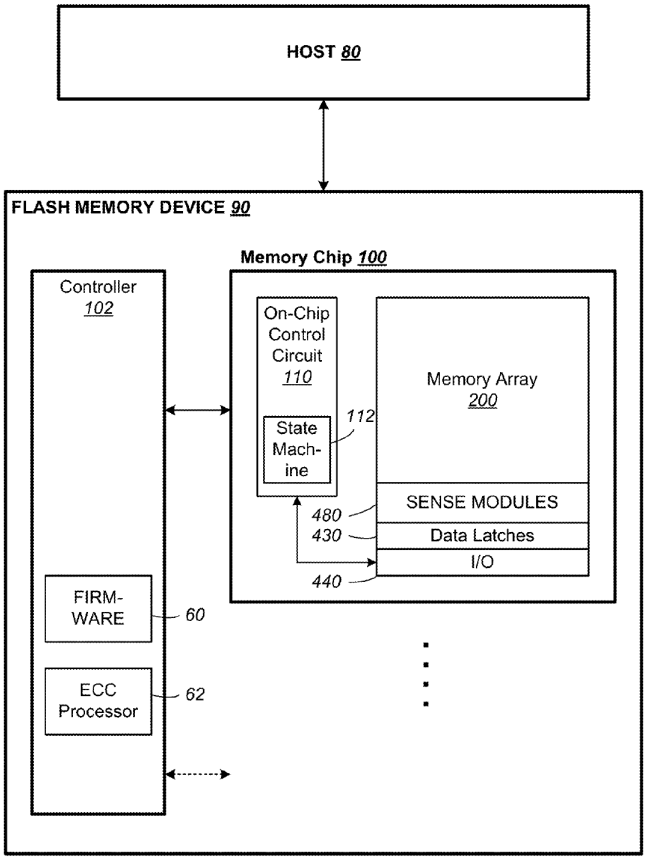


FIG. 1

Ex. 1045, Fig. 1.

91. ***Second***, Petitioner's ground instead points to disclosure from four different references—Gorobets 912, Paley, Harari, and Gorobets PCT. Petition, 32-34. Petitioner suggests that the distinct teachings of these references support its

assertion that it was "well-known" "to use…RAM…in a NAND flash controller as a staging or cache location for data to be written to flash memory." *Id.*, 32. With this assertion, however, in my opinion, Petitioner ignores that the cited embodiments from these references—each allegedly disclosing a RAM-based cache—are distinct from the embodiments of Gavens. For example, as explained above, Gavens never discloses the use of random access volatile memory. Yet, in my opinion, Petitioner provides no explanation how the distinct disclosure of the allegedly incorporated references applies to or can be combined with the previously cited disclosure of Gavens, which explicitly distinguishes its teachings from systems that use RAM, as I have stated supra.

92. Finally, I understand that Petitioner's ground for this limitation does not clearly present an obviousness-based theory for its argument. For example, in my opinion, Petitioner does not explain what aspect of the claim limitation is missing in Gavens or what features of Gavens must be modified to arrive at the claim language. Petitioner merely cites the disclosures of the allegedly incorporated references without clearly stating whether any of those references' RAM is being used to modify Gavens's system, and why a POSA would have been motivated made any modification. *See* Petition, 32-34.

93. Additionally, I understand that limitations [12e] and [1e] are the same, and Petitioner relies on the same ground for both limitations. *See* Petition, 55. Therefore, the Petition's analysis of limitation [12e] is inadequate for the same reasons as those given above for limitation [1e].

3. [1g] and [12f]: "the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and *retain such stored data in the random access volatile memory*"

94. Limitation [1g] recites: "the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory."

95. In my opinion, Petitioner's obviousness analysis is also inadequate for limitation [1g], at least because does not demonstrate how Gavens and its allegedly incorporated references—Gorobets 912, Paley, Harari, and Gorobets PCT—disclose or suggest random access volatile memory" that "***retain[s]*** such stored data." Petition, 38-39.

96. ***First***, similar to its deficient analysis for limitation [1e], in my opinion, here again Petitioner does not demonstrate or adequately explain how Gavens and its allegedly incorporated references disclose or suggest a RAM element. As explained above with respect to limitation [1e], Gavens itself does not disclose a RAM element, and Petitioner does not explain why a POSA would have been motivated to combine the teachings of the allegedly incorporated references with Gavens' distinct disclosure. For limitation [1g], I understand that Petitioner merely cites back to its analysis of limitation [1e], and conclusorily asserts that "Gavens discloses a controller" whose "operation obviously involves control of the RAM data cache … disclosed by Gavens, … *e.g.*, incorporated Paley '180 ¶ [0197][.]" Petition, 38. In my opinion, this conclusory assertion does not provide a meaningful explanation of how or why the distinct teachings of Paley—or any other allegedly incorporated reference—would have been combined with Gavens.

97. ***Second***, I understand that limitation [1g] further requires that "in at least a Write access operation to the MLC nonvolatile memory element, [the controller is] operable to ***store data in the MLC*** nonvolatile memory element ***and retain such stored data in the random access volatile memory***." In my opinion, in other words, limitation [1g] requires that, during a "write access operation," the

controller is operable to store data in MLC memory while ***retaining*** that data in RAM.

98. I understand that Petitioner asserts that a POSA would understand this operation to be "satisfied by Gavens by 'storing' data in the NVM that was and is cached (temporarily stored or 'retained') in the disclosed RAVM." Petition, 38-39. However, in my opinion, Petitioner's assertion is ambiguous, and Petitioner fails to explain how a POSA would have reached this conclusion, including on what basis a POSA would have understood Gavens to suggest that data cached in RAM is "***retained***" within the meaning of Claim 1 including limitation [1g]. In my opinion, Petitioner in its ground appears to assert that RAM that caches or "temporarily store[s]" data in any way necessarily "retains" that data as required by the claim. Petition, 39. But in my opinion, that is incorrect. In my opinion, limitation [1g] requires that the "stored data" be "retain[ed]" in the RAM in the sense that it is *also* operable to be stored in the MLC memory. Petitioner fails to show how Gavens, even with its allegedly incorporated references—Gorobets 912, Paley, Harari, and Gorobets PCT—retain data in this manner, as disclosed by the Limitation [1g].

99. Petitioner also refers to its analysis for the subsequent limitation [1h] (Petition, 38), but that ground also does not provide adequate support for its argument for limitation [1g]. In my opinion, Petitioner's ground for limitation [1h]

also does not provide a sufficient obviousness rationale to cure this deficiency. Petitioner's ground for limitation [1h] instead focuses on the claimed "data integrity test" and Gavens's teaching of data "comparison." Petition, 39-40.

100. In my opinion, notwithstanding the fact that Petitioner did not provide the required obviousness analysis for its ground, a POSA would not have found it obvious that Gavens in combination with any of the allegedly incorporated references, such as Paley, renders obvious a controller operable to ***retain*** data in RAM when it is written to MLC. Instead, in my opinion, the teachings of the allegedly incorporated references cited by Petitioner store data ***temporarily***, where that data is buffered ***until*** it is written to MLC. For example, Petitioner cites ¶197 of Paley but, in this paragraph, Paley explicitly states: "A cache is high-speed storage for ***temporarily storing data*** being ***passed between*** a high-speed and a slower-speed component of the system." Ex. 1051, ¶197; Petition, 38 (citing ¶197 of Paley). Paley further suggests that a "high-speed volatile RAM" in a controller can be used as a cache to temporarily store data being passed to non-volatile memory, including SLC or MLC. *See* Ex. 1051, ¶197. Further, I understand that Gorobets 912 includes the same disclosure. *See* Ex. 1049, ¶109 ("A Cache is high-speed storage for temporarily storing data being passed between a high-speed and a slower-speed component of the system."). Gorobets 912 goes on to explain that this RAM, by

design, is of "relatively limited capacity," so once data is "transferred out" of RAM to the non-volatile memory, the contents of the RAM are cleared to "receive more data" being transferred—in other words, this RAM is not operable to *retain* data that is also written to non-volatile memory, since its contents are cleared once they are "transferred out" to the non-volatile memory. *See* Ex. 1049, ¶144 ("As data has been transferred out of RAM at 721, this has opened up the RAM, which is relatively limited capacity, to receive more data from the host….").

101. Therefore, in my opinion, Paley and Gorobets 912 make clear that—contrary to the assertions in Petitioner's ground—the RAM-based cache only "temporarily" stores data when it is being "passed" to the non-volatile memory. Harari and Gorobets PCT suffer from the same flaw, and similarly disclose RAM-based caches/buffers for *temporarily* storing data. *See* Ex. 1057, Fig. 8, 13:29-30; Ex. 1058, 11:10-13. I further discussed the teachings of the RAM-based caches described in Paley, Gorobets 912, Harari and Gorobets PCT in Sections VIII.A.2.a) through VIII.A.2.d) above.

102. Therefore, in my opinion, even if one of the RAM-based caches taught by Paley, Gorobets 912, Harari and Gorobets PCT were incorporated into Gavens's system, a POSA would not have understood the controller to be operable to also

retain data in that RAM when the data is stored in MLC, as is required by limitation [1g].

103. Additionally, I understand that limitations [12f] and [1g] are the same, and Petitioner relies on the same ground for both limitations. *See* Petition, 55. Therefore, the Petition's analysis of limitation [12f] is inadequate for the same reasons as those given above for limitation [1g].

4. [1h] and [12g]: "the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by ***comparing the stored data to the retained data in the random access volatile memory***"

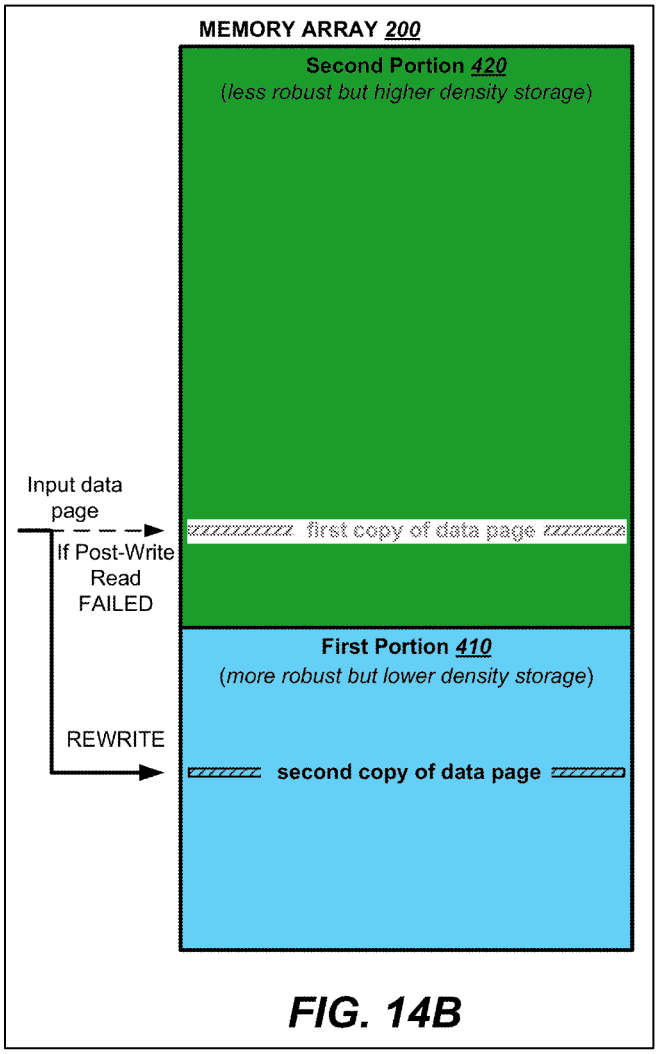
104. Limitation [1h] recites: "the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory."

105. I understand that, for Petitioner's ground for limitation [1h], Petitioner argues that Gavens's disclosure of a "'post write read'…check for errors 'by comparison with the original copy which may be cached'" would have been understood to refer to a RAM-based cache, as required by limitation [1h]. Petition, 39-40 (quoting Ex. 1045, 16:46-49). In my opinion, however, a POSA would not have shared Petitioner's understanding—in fact, Gavens's "cache[]" that retains the

"original copy" (Ex. 1045, 16:46-49) refers to a ***non-volatile cache***, not a RAM-based cache.

106. ***First***, in my opinion, Gavens itself does not disclose a RAM-based cache used in the "post-write read" error check. *See* Ex. 1045, 16:46-49 (describing a post-write read error detection process that can check for errors "by comparison with the original copy which may be cached"). Gavens instead explains that the "original copy" is cached in SLC non-volatile memory. *See supra* Section VIII.A.1.

107. I understand that, for its ground, Petitioner cites teachings from the "first embodiment" of Gavens, including Figure 14; I provided an overview of this embodiment in Section VIII.A.1.a) above. *See* Petition, 39 (citing Gavens's Figures 14 and 15, and its disclosure at 16:13-17:42). With Figure 14B, as illustrated below, Gavens describes a memory including an **SLC portion** which is less error prone, and **MLC portion** which is more error prone but may be used "for [more] efficient storage." Ex. 1045, 4:16-19, 16:41-45; *see also id.*, 4:13-19, 16:14-28. Gavens explains that data written to the MLC portion can be "read back in a post-write read operation to check for excessive error bits." *Id.*, 4:19-21. In my opinion, Gavens at 16:46-49, as cited by Petitioner, refers to this post-write error check of data written to the MLC portion.



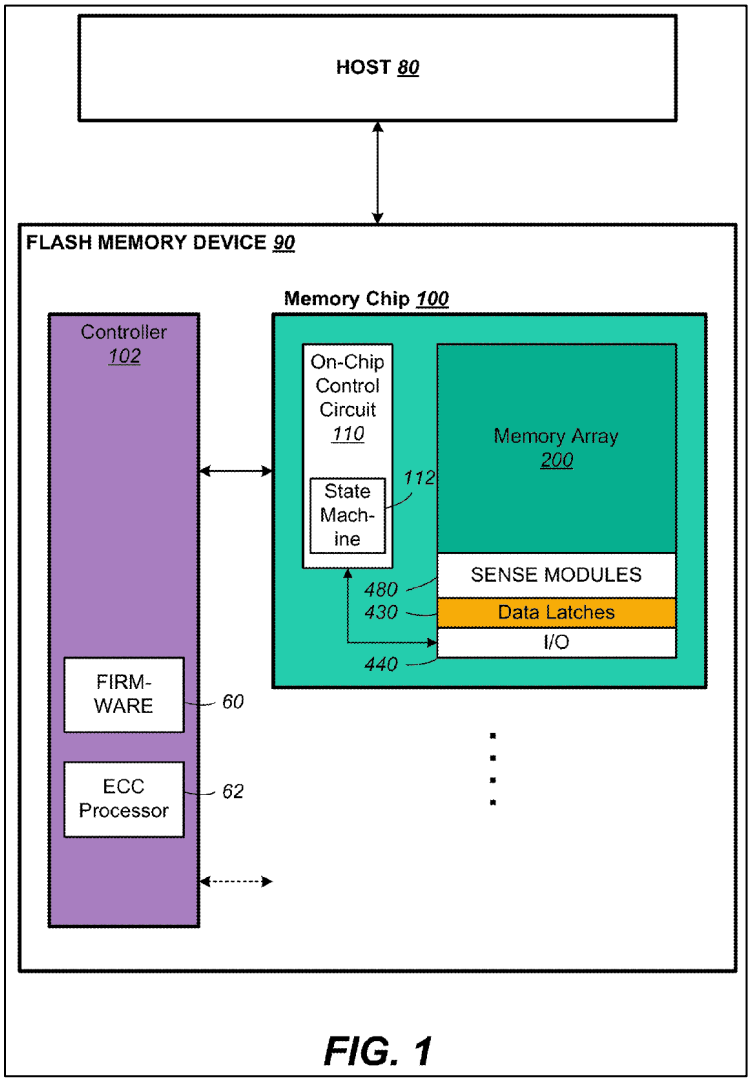
Ex. 1045, Fig. 14B (annotated).

108. Gavens at 16:46-49 specifies that the post-write error check may be performed "by [a] comparison with the original copy which may be cached[.]" Ex. 1045, 16:46-49. In my opinion, at 16:46-49, Gavens does not specify how the "original copy" is cached, but Gavens later explains that "[i]n the preferred embodiment" (where the antecedent basis of "the" refers to the immediately preceding "preferred embodiment" of Figures 14A-14B) the "data is cached in [a]

first section of the first portion" of non-volatile memory (*i.e.*, a section of the non-volatile SLC memory). *Id.*, 18:1-8; *see also id.*, 16:14-16. Thus, in my opinion, Gavens describes that the cached "original copy" resides in non-volatile memory—not volatile memory, such as RAM, as Petitioner argues.

109. Furthermore, in my opinion, Gavens also explains with the embodiment of Figure 16 why caching the original data in non-volatile memory improves the system. I provide an overview of this embodiment in Section VIII.A.1.b) above. Like in the embodiment of Figure 14 discussed above, in the embodiment of Figure 16, Gavens describes caching data in ***non-volatile*** memory ("first section 411") where it is retained for use in error detection. *See* Ex. 1045, 18:21-44. Gavens's non-volatile cache retains data even after the data is written to a "high[er] density second portion" (MLC) of the non-volatile memory. *See id.*, 18:24-29. The retained data in the non-volatile cache can then be compared to the data written to the "higher density second memory" to check if the data was written correctly. *See id.*, 18:30-44. Additionally, Gavens explains that data used for error detection should be cached in the non-volatile memory (*i.e.*, the "First section 411" of Figure 16) to avoid needing to toggle data to the controller for error detection. Ex. 1045, 18:36-39 ("By not making the comparison at the controller, the data does not have to be toggled out to the controller, much time can be saved."). Specifically, as illustrated

in Gavens's Figure 1 below, when data is cached in the SLC portion of the **non-volatile memory array 200** at the time it is written to the MLC portion of that same **array**, the ***on-chip*** **data latches 430** (part of **memory chip 100**) can be used for the post-write read error check—thus avoiding the need to toggle the written data out to the **controller 102**, which is not on the same chip as **memory chip 100**. Gavens explains that caching data in the non-volatile memory improves performance by reducing reliance on the controller chip. *See id.*, 18:36-67.



Ex. 1045, Fig. 1 (annotated).

110. For these reasons, in my opinion, a POSA would not have understood Gavens to teach caching data in RAM for the "comparison" cited by Petitioner. Gavens instead teaches that, for the cited "comparison," data is cached in the non-volatile SLC memory.

111. ***Second***, in my opinion, the teachings of the allegedly incorporated references, including Gorobets 912 and Paley (as cited by Petitioner), do not justify Petitioner's incorrect interpretation of Gavens. I understand that Petitioner cites the distinct teachings of Gorobets 912 and Paley to argue how they believe a POSA would have "understood" Gavens. But, as was also addressed in my opinions related to Petitioner's ground for limitation [1e] above, Petitioner provides no explanation how the unrelated disclosure from these references applies to or can be combined with the previously cited disclosure of Gavens. In my opinion, the RAM-based caches taught by Gorobets 912 and Paley, along with the other allegedly incorporated references, are not part of Petitioner's cited embodiment of Gavens.

112. Notwithstanding, in my opinion, a POSA would have understood that Gavens's non-volatile cache should not be replaced with the RAM-based caches taught by Gorobets 912 and Paley, and in fact, Gavens teaches away from such a replacement. As explained above, the non-volatile, SLC cache of Gavens cited by Petitioner is used to ***retain data*** so it can be used in the subsequent post-write read error-check. *See, e.g.*, Ex. 1045, 16:46-49. In contrast, as explained above in my opinions addressing Petitioner's ground for limitation [1g], the RAM-based caches of Gorobets 912 and Paley cited by Petitioner do not retain data, and instead only "temporarily" store when it is being transferred to non-volatile memory. *See* Ex.

1049, ¶¶109, 144; Ex. 1051, ¶197. Thus, unlike the non-volatile cache of Gavens, Gorobets 912's and Paley's RAM-based based caches ***do not retain data*** and, instead, act only as temporary write buffers. *See, e.g.*, Ex. 1049, ¶144 (explaining that the RAM-based cache is of "relatively limited capacity," so as soon as data is "transferred out of [the] RAM" to the non-volatile memory, the RAM "open[s] up" the space). Accordingly, in my opinion, a POSA would not have been motivated to replace Gavens's non-volatile cache with the RAM-based caches taught by Gorobets 912 or Paley, as these caches perform entirely different functions—***retaining*** data (as in Gavens, and as required by the claims) versus ***temporarily*** storing or buffering data (as in Gorobets 912 and Paley).

113. Furthermore, Gorobets 912 and Paley describe RAM-based caches potentially located in the controller. *See* Ex. 1049, ¶109 ("Typically high-speed volatile RAM are employed as cache as in a host cache 82 and/or in controller cache 102 of the memory controller"); Ex. 1051, ¶197 (same); *see also* Ex. 1049, ¶130. For example, Figure 11 of Gorobets 912, and the substantively identical Figure 15 of Paley, show the "Cache (RAM) 102" in the memory controller. In contrast, in my opinion, Gavens teaches ***against*** using the controller for its error detection process. As described above, Gavens explains that data used for error detection should be cached in the non-volatile memory ***to avoid having to toggle data to the***

controller. Ex. 1045, 18:36-39 ("By not making the comparison at the controller, the data does not have to be toggled out to the controller, much time can be saved."). Gavens explains that caching data in the non-volatile memory increases performance by reducing reliance on the controller chip. *See id.*, 18:36-67. In my opinion, relying on a cache in the controller (as may be required if the RAM-based cache of Gorobets 912 or Paley was used) rather than a cache in the non-volatile memory would contradict the purpose of Gavens's invention. Thus Gavens teaches away from using the RAM-based caches that Petitioner proposes.

114. Additionally, I understand that limitations [12g] and [1h] are the same, and Petitioner relies on the same ground for both limitations. *See* Petition, 55. Therefore, the Petition's analysis of limitation [12g] is inadequate for the same reasons as those given above for limitation [1h].

C. Dependent Claims 2-11

115. For dependent claims 2-11, which all are independent claims of Claim 1 addressed above, the Petition's Grounds also state that these claims are disclosed or suggested by Gavens. Therefore, I understand that the Petition's analysis of claims 2-11 is flawed at least due to the above-discussed deficiencies of the Petition's analysis of independent Claim 1.

IX. CONCLUSION

116. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Respectfully submitted,

Date: May 9, 2025 By: _____
Sunil P. Khatri, Ph.D.

Appendix A

Sunil P Khatri

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Background and Summary

My research areas are:

- **Computer Systems:** My work on Computer Systems is divided in two subcategories: 1) ***circuits and computer architecture*** (including the design of machine learning engines, hardware security paradigms, efficient Networks-on-Chip (NoCs), special function units for comparison, hashing, Boolean Satisfiability and sorting, low energy, low power circuit and high-speed design, system prototyping, as well as circuit/architectural approaches for radiation tolerance/detection, resilience, crosstalk avoidance, clocking, leakage/power reduction and testability); and 2) ***algorithm acceleration*** (using GPUs, FPGAs, map-reduce clusters and custom ICs) for algorithms in the VLSI CAD domain.
- **Logic Synthesis and algorithms for VLSI Design:** In this area, my work initially started in the space of logic synthesis for VLSI CAD. In the last few years, I have directed this work toward genomics, noise based logics, and Boolean Satisfiability solvers (using GPUs, FPGAs, map-reduce clusters and custom IC based accelerators).
- **Interdisciplinary extensions:** The above two areas form a springboard from which I engage in research in other domains. I explore extensions of the above two areas to other areas such as IP routing, Digital Signal Processing (for FFT and radar signal processing), optical networking, wireless communication and coding, cryptography, satellite tracking, drone routing, graph network analytics and gene sequencing. Recent work in this space includes secure computing and distributed consensus (blockchain) techniques and their application.

I have a total of 291 peer-reviewed publications (48 journal papers, 201 conference papers, 42 workshop papers). Among these papers, 5 received a best paper award, while 7 others received best paper nominations (including 1 journal best paper nomination). An additional 3 journal papers and 1 conference papers are currently undergoing peer review. I have co-authored 9 research monographs (contracts for 5 others are being pursued) and 1 edited research monograph, 4 book chapters and 7 awarded US Patents (two of which were filed at Texas A&M). I have co-authored 1 invited journal paper, 13 invited conference or workshop papers (including 1 from DAC and 1 from Allerton) and 3 invited book chapters. Moreover, I was invited to serve as a panelist at a conference 8 times, and have presented 4 conference tutorials. I received the *"Outstanding Professor Award"* in the ECE Department at Texas A&M University in 2007, and again in 2020. My H-index is 36 (per Google Scholar).

I have graduated 13 Ph.D. students (3 co-advised, 5 US citizens or residents, and two women), 20 M.S. students (6 US citizens, 3 women, 3 of my MS students joined my Ph.D. program) and 12 B.S. Honors students and 6 B.S. Senior Design students, whose thesis I have advised. Currently, I advise 5 Ph.D. students (1 co-advised), 1 M.S. student, and 1 B.S. Senior Design students. I have advised 40 undergraduates (18 under the NSF REU, URA or USRG programs), of which 4 students received an award for their research. Eight papers in international conferences (1 invited) resulted from my work with undergraduates. The Ph.D. thesis of one of my students was nominated for the ACM Best Dissertation Award, 2014.

Last update: March 18, 2025

I have taught 5 distinct graduate courses and 3 distinct undergraduate courses at Texas A&M, have substantially redesigned the laboratories for one undergraduate course, and have assisted in the overhaul (lectures and laboratories) of another undergraduate course. My average undergraduate (graduate) teaching ratings are 4.42/5 (4.46/5). The departmental averages for similar courses are 4.15 (undergraduate) and 4.45 (graduate). For undergraduate courses, my average numerical grade is 2.81, while the departmental average for equivalent level courses is 3.18. For graduate courses, these numbers are 3.73 and 3.65 respectively. In Fall 2009, I was awarded the "*Association of Former Students' Distinguished Achievement Award in Teaching*", and the "*Association of Former Students Distinguished Achievement Award in Teaching - College-Level*" in 2019. In 2024, I received the "Engineering Teaching Excellence Award" from the College of Engineering, Texas A&M University.

I have 1 current research grant (total grant amount $1431K, of which my portion is about $674K). The total amount of the grants in which I was involved to date is $18.96M, of which my portion is $3.524M. Some of these grants are with colleagues in ECE as well as other academic departments at TAMU. My research has been funded through government (NSF, LLNL, NSA, DNDO, DTRA, DoE) as well as industrial (Intel, Nascentric, NSC, SRC, Accelicon, Iris Technologies) sources.

I currently serve, or have served, as the *Associate Editor* (ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on Computers, MDPI Journal of Electronics), *EDA Track Co-Chair* for ICECS 2014, *Panel Chair* for TexasWISE 2014, *Track Co-Chair* (VLSI Systems, Applications and Computer Aided Design track) for ICECS 2013, *Poster Session Chair* for TexasWISE 2013, *Advisory Committee* for HotPI 2013, Panel Session Chair *for SLiP 2013, Track Chair* (Logic track) for ICCAD 2009-10, 2015-17, *Track Chair* (logic track) for DAC 2016-17, *General Chair* for IWLS 2009, *Technical Program Chair* for IWLS 2008, *Track Co-Chair*, Computer Aided Network DEsign (CANDE) Track for ISCAS 2008-10 and DSP Track for ISCAS 2022, *Track Co-Chair*, Test and Methodologies Track, for ICCD 2007, *Panel Chair* for ITSW 2009, *Publicity Co-Chair* for GLS-VLSI 2009, and as a *member of the TPC* for several conferences. I have conducted *reviews* of a large number of IEEE and ACM journal and conference papers. I have also served as a *session chair* at several conferences. In addition, I have been involved in Department and group level service activities.

Education

Ph.D. **University of California, Berkeley.** Department of Electrical Engineering and Computer Sciences. (1993 - 99). Awarded the California MICRO Fellowship, 1993-94. Maintained a GPA of 3.963.

M. S. **University of Texas, Austin.** Department of Electrical and Computer Engineering (1987 - 89). Awarded the Microelectronics and Computer Development (MCD) Fellowship, 1987-89). Maintained a GPA of 3.909.

B. S. **Indian Institute of Technology, Kanpur, India.** Department of Electrical Engineering (1983 - 87). Obtained a GPA of 3.72, ranked fourth in a class of sixty students.

Dissertation/Thesis

Ph. D. ***"Cross-talk Noise Immune VLSI Design using Regular Layout Fabrics".*** Committee: Professor R. K. Brayton (Co-chair), A. Sangiovanni-Vincentelli (Co-chair) and Professor Dorit Hochbaum, University of California, Berkeley.

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M. S. ***"The Design of the METRIC Memory Interface and Memory System".*** This involved the design of the memory interface of METRIC, a multi-threaded RISC Microprocessor. Committee: Professor M. Ray Mercer (chair) and Professor Donald Fussell, University of Texas at Austin.

B. S. Senior project involved implementing graphics algorithms on a MC68000-based terminal. Advisor: Professor A Joshi, Indian Institute of Technology, Kanpur, India.

Research and Professional Experience

Faculty Development Leave at National Center for Atmospheric Research (NCAR) and the Air Force Research Laboratory (AFRL), 8/2025 – 8/2026. I plan to spend my sabbatical at NCAR, working with Dr. Jothiram Vivekanandan on several topics related to phased-array radar signal processing, including design and testing (including field test) of the signal processing elements. My work at AFRL will focus on secure hardware.

Faculty Development Leave at Arizona State University (ASU) and the Air Force Research Laboratory (AFRL), 8/2019 – 8/2020. I spent my sabbatical at ASU, working with Prof. Sarma Vrudhula on several topics related to flash-based realization of ASICs, neural networks, and secure hardware. My work at AFRL comprised research on secure hardware. Three papers and three NSF grant proposals and one patent resulted from this effort, and additional collaboration is being pursued.

Texas A&M University, College Station, TX. Professor in Electrical and Computer Engineering, 9/2015 – present. Associate Professor in Electrical and Computer Engineering, 9/2010 – 9/2015. Assistant Professor in Electrical and Computer Engineering, 6/2004 – 9/2010. Conducting research on 3 areas. The first is **Computer Systems,** including computer architecture from the circuits up, and algorithm acceleration using GPUs, FPGAs and custom ICs. The second is **Logic and its applications**, while the third area consists of **Interdisciplinary extension**s of the first two.

Faculty Development Leave at U.T. Austin, 9/2011 – 8/2012. I spent my sabbatical at UT Austin, working with Prof. Jacob Abraham on several topics such as genomics, sinusoidal signal based data transfer, and medical electronics. One paper resulted from this effort, and additional collaboration is being pursued.

University of Colorado, Boulder. Assistant Professor, Electrical and Computer Engineering. 1/2000 – 5/2004. Performed research on VLSI logic design automation, VLSI layout design automation, VLSI design methodologies to address Deep Submicron (DSM) issues such as cross-talk and power along with interdisciplinary extensions.

University of California, Berkeley. Research Assistant with the CAD group, under Professors Robert Brayton and A. Sangiovanni-Vincentelli (8/1993 – 12/1999). Research topics included CAD for DSM design, Sets of Pairs of Functions to be Distinguished (SPFDs), Binary Decision Diagrams, Engineering Change, Hierarchical Synthesis and Verification, Model Matching and Combinational Verification, Timing Analysis in the Presence of Cross-talk and Multi-valued Logic Synthesis.

Design Engineer with Motorola's MC88110 RISC and PowerPC 603 microprocessor groups in Austin, Texas (8/1989 – 7/1993). Was involved in various design areas from Design for Testability to Digital and Analog Circuit Design, along with high-level design.

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Independently responsible for the design of the factory test controller for the MC88110. Familiar with various ad-hoc and structured test methodologies. Designed digital as well as analog circuitry. Designed the MC88110's input / output buffers and clock PLL logic. Performed all attendant tasks in a "vertical" VLSI design methodology, including high-level modeling, layout design and verification, as well as global and detailed routing.

During my years at Motorola, I had definite plans to pursue an academic career. As a result, I intentionally attempted to get an understanding of as many tasks as possible in an entire VLSI design flow, to make for a more rich research base in my future as an academic researcher.

University of Texas, Austin. Researcher with Professor M. Ray Mercer's group (8/1988 - 7/1993). Research topics included IC testing and Boolean function representation using Canonical XOR-based circuit decompositions.

University of Texas, Austin. Researcher with Professor Donald Fussell's group (8/1987 – 7/1989). Research areas included Computer Architecture and Memory Interface design, applied in the context of the METRIC multi-threaded RISC microprocessor, which Professor Fussell was developing.

Research Interests

My research interests are broadly divided into 3 areas listed below. Each area has representative topics listed alongside the heading.

- **Computer Systems:** My work in Computer Systems is divided into 2 categories: 1) ***VLSI circuits and computer architecture*** (including the design of machine learning systems, hardware security paradigms, efficient NoCs using a resonant clocking as well as a superposition-of-sinusoids paradigm, special function units for comparison, hashing, Boolean Satisfiability and sorting, low energy and low power design using sub-threshold circuits, high-speed circuit design, system prototyping, specialized architectures for radiation tolerance/detection, as well as circuit and architectural approaches for resilience, crosstalk avoidance, clocking, leakage reduction and testability). My group also develops system prototypes to validate our ideas – for example, in extreme low power/energy computation, architectures for cryptography and FPGA based architectures for Boolean Satisfiability, and 2) ***Algorithm acceleration*** (using GPUs, FPGAs, map-reduce clusters and custom ICs), for algorithms in the VLSI CAD (for fault simulation, logic simulation, circuit simulation, fault table generation, SAT) domain.
- **Logic Synthesis and Algorithms for VLSI Design:** In this area, my work initially started in the space of logic synthesis for VLSI CAD. In the last few years, I have directed this work toward genomics (predictor inference, Gene Regulatory Network (GRN) construction, determining optimal drug regime for a genetic disease, gene sequencing and alignment), noise based logics and their realization, and fast Boolean Satisfiability solvers (using GPUs, FPGAs, map-reduce clusters and custom IC based accelerators).
- **Interdisciplinary extensions:** The above two areas form a spring-board from which I engage in research in other domains. I explore extensions of the above two areas to other areas such as IP routing (routing table compression, architecture and circuit design of Ternary CAMs), Digital Signal Processing (architectures and designs for FFT, FPGA and GPU based radar signal processors), optical networking (SAT based Routing and Wavelength Assignment for DWDM optical networks), wireless communication (MIMO decoders, WiMAX decoders) and coding (LDPC decoders, fix-free code generators), satellite tracking, drone routing, graph network analytics and cryptography. Recent work spanning this area involves secure computing, and distributed consensus (blockchain) and its applications

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Some of my current research projects (which are yet unpublished) include an interdisciplinary project (with Dr. Suman Chakravorty (Aerospace, TAMU)) in which we are accelerating a receding horizon control method to track satellites, a method to help IC debug by sampling the power supply grid on the fly, a combined hardware and software programming language, a fast map-reduce based implementation of a Boolean Satisfiability (SAT) solver, an asynchronous, low leakage power Network-on-Chip router, several methods to accelerate gene sequencing and alignment, a method to detect coincident events in radiation detection when multiple detectors are deployed (this will be fabricated in a near-threshold IC in the next year), a fast superposition-of-sinusoids approach to deliver very high speed data across ICs on a circuit board, and a new highly efficient circuit design approach that uses flash transistors (which have historically been used only for memory).

Publications

Conventions used:

- For all publications, the names of past or present, graduate or undergraduate student co-authors (who were advised by me or had no advisor at the time of publication) are underlined. The students with no advisor at the time of publication were students who took my graduate course, and we decided to publish their class project.
- The names of past or present co-authors who were graduate students at the time of publication (and were not advised by me) are indicated in *underlined italics*. Such students are the students of colleagues with whom I collaborated after becoming a faculty member, or peer students with whom I collaborated while I was a graduate student.
- All publications listed (other than invited papers) are peer reviewed.
- I have first listed books/book chapters, followed by conference tutorials presented, invited papers or panels, journal papers, conference papers, workshop papers and patents. Accepted items and items which are under review are listed under separate headings.
- Items under review are not included in the paper count totals.
- Invited papers are listed under "Conference Papers" and "Workshop Papers", and also under a separate heading for distinguishability.
- In a handful of cases, page numbers are not available.

Books or Book Chapters Published:

"Flash - A "Forgotten" Technology in VLSI Design". Khatri, Vrudhula, Abusultan, Bharathi, Chu, Lee, Scott, Singh, Wagle. Appears "Frontiers of Quality Electronic Design (QED)". Springer publishers, Sept 2022. Pages 67-136. Ali Iranmanesh, Ed. ISBN: 978-3-031-16344-9.

"A Sum-Of-Product Based Multiplication Approach For FIR Filters And DFT", Kumar, Khatri. Monograph published by LAP LAMBERT Academic Publishing. 1st edition, January 2014. 64p. ISBN 978-3-8484-8636-6.

"Source-Synchronous Networks-On-Chip: Circuit and Architectural Interconnect Modeling", Mandal, Khatri, Mahapatra. Monograph published by Springer Publishers. 1st edition November 2013. 160p. ISBN 978-1-4614-9404-1.

"Logic Synthesis for Genetic Diseases: Modeling Disease Behavior Using Boolean Networks", Lin, Khatri. Monograph published by Springer Publishers. 1st edition, November 2013. 140p. ISBN 978-1-4614-9428-7.

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"Practical & Real Time IP Routing Table Compression - Extending algorithms from digital logic synthesis". Bollapalli, Khatri. Published by LAP Lambert Academic Publishing, January 2012. 68p. ISBN 978-3847321521.

"*Advanced Techniques in Logic Synthesis, Optimizations and Applications*", Khatri, Gulati, editors. Springer Publishers, 1st ed, 2011. 240p. ISBN 978-1-4419-7517-1.

"*Robust Window-Based Multi-node Minimization Technique Using Boolean Relations*", Cobb, Gulati, Khatri. pp 309-333, In "*Advanced Techniques in Logic Synthesis Optimizations and Applications*", Khatri, Gulati, ed. Springer Publishers.

"*Digital Logic Using Non-DC Signals*" Bollapalli, Khatri, Kish. pp 383-400. In "*Advanced Techniques in Logic Synthesis Optimizations and Applications*", Khatri, Gulati, ed. Springer Publishers 2011. ISBN 978-1-4419-7517-1.

"On and Off-chip Cross-talk Avoidance in VLSI Designs", Duan, LaMeres, Khatri. Monograph published by Springer Publishers. 1st edition, 2010. 240p. ISBN 978-1-4419-0946-6.

"EDA Algorithm Acceleration with FPGAs, GPUs, and Custom ICs", Gulati, Khatri. Monograph published by Springer Publishers. 1st edition, 2010. 194p. ISBN 978-1-4419-0943-5.

"Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations", Garg, Khatri. Monograph published by Springer Publishers. 1st edition, 2010. 212p. ISBN 978-1-4419-0930-5.

"Minimizing and Exploiting Leakage in VLSI Design", Jayakumar, Paul, Garg, Khatri. Monograph published by Springer Publishers. 1st edition, 2010. 214p. ISBN 978-1-4419-0949-7.

Invited chapter "*Logic Synthesis*" in the CRC EDA handbook "EDA for IC Implementation, Circuit Design and Process Technology". Editors L. Lavagno, L. Scheffer, G. Martin. ISBN 0849379245, 9780849379246, 571pp, published 2006. Chapter co-authored by Narendra Shenoy of Synopsys Inc. The Wikipedia entry on "Logic Synthesis" is based on the material in this chapter.

"Cross-talk Noise Immune VLSI Design using Regular Layout Fabrics", Khatri, Brayton, Sangiovanni-Vincentelli. Research Monograph published by Kluwer Academic Publishers. ISBN # 0-7923-7407-X.

Book Contracts or Chapter Invitations:

"*A Flash-based Digital to Analog Converter Design",* Scott, Khatri. Contract for this research manuscript being pursued through Springer publishers, 2025-26

"*GPU based acceleration of Reinforcement Learning Approaches",* Zhou, Khatri, Hu, Liu. Contract for this research manuscript being pursued through Springer publishers, 2025-26

"*Synchronous, Scalable Ring-based Design of 3D Stacked DRAM",* Douglass, Khatri, Linderman. Contract for this research manuscript being pursued through Springer publishers, 2025-26

"Metastability Reduction on Asynchronous Circuits", Sharma. Khatri. Contract for this research manuscript being pursued through LAP LAMBERT publishers, 2025-26

"Digital Circuit Design using Flash Transistors", Abusultan, Khatri. Contract for this research monograph being pursued through Springer Publishers, 2025-26

Conference Tutorials Presented:

"Flash – An Overlooked Technology in VLSI Design", Khatri, Vrudhula. Monday Tutorial presented at the 62nd ACM/CEDA Design Automation Conference (DAC), San Francisco, CA, June 22-25, 2024.

"Distributed Consensus and the Smart Grid". Khatri. 3rd IEEE International Conference on Smart Grid and Renewable Energy, Mar 20-22, 2022. Doha, Qatar.

"*Introduction to GPU Programming for EDA*", Croix, Khatri. This tutorial was presented at the International Conference on Computer-Aided Design (ICCAD), San Jose, CA. November 2-5, 2009.

"Structured ASIC Design Approaches and Trends", Technical Forum, DesignCon East, Worcester, MA. September 19-21, 2005.

Conference Panel Invitations:

"Overview of Smart Grids and Their Cyber-physical Security". Invited to serve as a panelist at the 50th annual conference of the IEEE Industrial Electronics Society (IECON), Chicago, IL. Nov 3-6, 2024.

"Challenges and Opportunities of Stochastic Computing in the Dusk of Moore's Law and the Dawn of Big Data", Invited to serve on a panel at the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Nov 7-10, 2016, Austin, TX. Declined due to health reasons.

"*Looking Beyond Moore's Law*", Invited to serve on a panel at the IEEE Texas Workshop on Integrated System Integration (TexasWISE) 2016, Houston, TX.

"Models and High-Speed Simulation". Invited to Chair a Panel Session to discuss this topic, at the 15th ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop 2013, Austin, TX. June 2, 2013.

"Multi-core and GPU based Parallelism". Invited to serve as a panelist to discuss this topic, along with leading academic and industry practitioners in this area. The panel was part of the IEEE CTS CAS/SSC/CEDA Workshop on Data Parallelism for Multi-core Chips and GPUs", Austin, TX. October 5, 2012. My talk was titled *"Algorithm Acceleration for GPU Architectures".*

"Manycore, Heterogenous, or Neither: Which One is the Way to Go for EDA?". Invited to serve as a panelist to discuss this topic, along with other leading researchers in the field of GPU based implementation of EDA algorithms. The panel was part of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, CA. November 7-10, 2011.

"*The Top of Testing's Most Wanted List – What is the most critical Testing challenge? (or have all the bad guys been caught already?)*", invited panelist (along with Jason Doege, T.M. Mak, Rob Dassch, Tom Williams and Luis Basto, some leading researchers in VLSI testing). This panel was part of the International Test Synthesis Workshop (ITSW) 2007, San Antonio, TX. March 5-7, 2007.

"*Are we Fighting a Losing Battle, Dealing with Numerous and Complex Defects?*", invited to serve as a panelist along with 3 leaders in the field. Peer panelists were Dr. Tom Williams (Synopsys), Prof. Melvin Bruer (USC), and Al Crouch (Inovys Corporation). The panel was part of the International Test Synthesis Workshop (ITSW) 2006, Santa Barbara, CA. April 9-12, 2006.

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Invited Papers, Book Chapters and Talks:
***Note:* These papers are re-listed along with regular papers in a later section. They are separately listed here for ease of perusal.**

Invited chapter *"A GPU-based Implementation of a Receding Horizon Sensor Tracking Methodology",* Abusultan, Chakravorty, Khatri. Invited to publish as a chapter in the Elsevier book "Advances in GPU Research and Practice", H. Sarbazi-Azad (Editor).

Invited chapter *"GPU-based Algorithms in Electronic Design Automation",* Gulati, Khatri, Croix. Invited to publish as a chapter in the Elsevier book "Advances in GPU Research and Practice", H. Sarbazi-Azad (Editor).

Invited paper, *"Information, noise and energy dissipation: Laws, limits and applications*", Kish, Granqvist, Khatri, Sundqvist, Peper Plenary talk at International Workshop on Molecular Architectonics, Shiretoko, Hokkaido, Japan, August 3-6, 2015.

Invited paper *""Demonic" challenge: Landauer's erasure-dissipation"* Kish, Granqvist, Khatri. 44th Winter Colloquium on the Physics of Quantum Electronics (PQE) 2014, Snowbird, UT. January 5-9, 2014.

Invited paper *"Demons: Maxwell demon; Szilard engine; and Landauer's erasure-dissipation"*, Kish, Granqvist, Khatri, Wen. Hot Topic of Physical Informatics (HoTPI) 2013, November 10-13, Changsha, China. November 10-13, 2013.

Invited paper, "*Using GPUs to Accelerate CAD Algorithms*", Croix, Gulati, Khatri. IEEE Design & Test, Vol. 30, Issue 1. February 2013, pp 8-16.

Invited paper, "*Algorithm Acceleration for GPU Architectures*", IEEE CTS CAS/SSC/CEDA Workshop on Data Parallelism for Multi-Core Chips and GPUs, Austin, TX. October 5, 2012.

Invited paper, "*Application of logic synthesis to the understanding and cure of genetic diseases*", Lin, Khatri. IEEE/ACM Design Automation Conference (DAC) 2012, San Francisco, CA. June 3-7, 2012, pp 734-740.

Invited paper, "*Noise-based Information Processing*", Kish, Khatri, Bezrukov, Peper, Gingl, Horváth. 21st International Conference on Noise and Fluctuations. June 12-16 2011, Toronto, Canada. June 12-16, 2011, pp 28-33.

Invited paper *"DFM-Aware Structured ASIC Design"*, Gopalani, Garg, Khatri. International Symposium on Integrated Circuits (ISIC) 2009, Singapore. December 14-16, 2009, pp 29-32.

Invited paper *"A PTL based Highly Testable Structured ASIC Design Approach"*, Gulati, Jayakumar, Khatri. International Symposium on Integrated Circuits (ISIC) 2009, Singapore. December 14-16, 2009, pp 33-36.

Invited paper "*Highly Parallel Decoding of Space-Time Codes on Graphics Processing Units",* Bollapalli, *Wu*, Gulati, Khatri, Calderbank. Annual Allerton Conference on Communication, Control and Computing, 2009, Urbana, IL. September 30 – October 2, 2009, pp 1262-1269.

Invited paper "*Noise-based logic",* Kish, Khatri, Bezrukov, Gingl, *Sethuraman*. International Workshop on Natural Computing (IWNC) 2009, Himeji, Japan. September 23-25, 2009. Published by Springer, Eds. F. Peper et al., IWNC 2009, PICT 2, pp 13–22, 2010.

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Invited paper "*Extreme Low Power Computing using Sub-threshold Circuits",* Segundo Magno Congreso Interancional del CIC 2007, Mexico City, Mexico. November 6-8, 2007.

Invited chapter "*Logic Synthesis*" in the CRC EDA handbook "EDA for IC Implementation, Circuit Design and Process Technology". Editors L. Lavagno, L. Scheffer, G. Martin. ISBN 0849379245, 9780849379246, 571pp, published 2006. Chapter co-authored by Narendra Shenoy of Synopsys Inc. The Wikipedia entry on "Logic Synthesis" is based on the material in this chapter.

Invited paper *"A Routing Technique for Structured Designs which Exploits Regularity*". Khatri, Das. VLSI Design and Test Workshop (VDAT-2001), August 2001.

Invited paper *"Multi-valued Logic Synthesis"*- Brayton, Khatri. 12th International Conference on VLSI Design (VLSI-99), Goa, India. 1999, pp 196-205.

Peer-reviewed Journal Publications:

"Attention-Enhanced AGRU Framework for Induction Motor Incipient Fault Diagnosis in Electric Vehicles". Saleh, Ghrayeb, Refaat, Abu-Rub, Khatri, Kammermann. IEEE Transactions on Instrumentation and Measurement, Vol. 74, November 2024, pp 1-17. Appeared in January 2025.

"*A Mixed-Signal Quantized Neural Network Accelerator Using Flash Transistors*", Scott, Lee, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 71, no. 3, pp. 1025-1038, March 2024.

"*An ASIC Accelerator for QNN With Variable Precision and Tunable Energy-Efficiency*", Wagle, Singh, Khatri Vrudhula. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 43, no. 7, pp 2057-2070, Jan 2024.

"*A Digital Low Dropout (LDO) Voltage Regulator Using Pseudoflash Transistors*", Lee, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1960-1969, Dec. 2023.

"A Novel ASIC Design Flow using Weight-tunable Binary Neurons as Standard Cells", Wagle, Singh, Khatri, Vrudhula. IEEE Transactions on Circuits and Systems I (Regular Papers), 69(7): 2968-2981 (Sept 2022).

"CIDAN-XE: Computing in DRAM with Artificial Neurons", Singh, Wagle, Khatri, Vrudhula. Frontiers in Electronics, section Integrated Circuits and VLSI. vol. 3, Feb 2022

"Hardware Acceleration of Hash Operations in Modern Microprocessors", Fairouz, Abusultan, Fedorov, Khatri. IEEE Transactions on Computers 70(9): 1412-1426 (Sept 2021).

"Computational evaluation of a novel Beta radiation probe design using integrated circuits", King, Shah, Marianno, Khatri, Chirayath. SN Applied Sciences 3(3), 386, Mar 2021. Springer Nature.

"Fast, Ring-based Design of 3D Stacked DRAM", Douglass, Khatri. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. Vol 27 number 8, Aug 2019. pp 1731-1741.

"*Comparing Leakage Reduction Techniques for an Asynchronous NoC Router*" Fairouz, Abusultan, Elshennawy, Khatri. Journal of Low Power Electronics (JOLPE). Vol. 14, No. 3, pp 414-427. 2018.

"*A GPU-CPU heterogeneous algorithm for NGS read alignment*", Al Kawam, Khatri, Datta. International Journal of Computational Biology and Drug Design, Vol 11, No 1-2, pp 52-66, 2018.

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"A Neutron Detector Using Integrated Circuits", Shah, Marianno, Khatri, Fisher. Journal of Modern and Applied Physics, 1(1):3-7, December 2017.

"*A Survey of Software and Hardware Approaches to Performing Read Alignment in Next Generation Sequencing*", Al-Kawam, Khatri, Datta. IEEE/ACM Transactions on Computational Biology and Bioinformatics, vol 14(6), pp 1202-1213, Nov-Dec 2017.

"*FTCAM: An Area-Efficient Flash-Based Ternary CAM Design*", *Fedorov*, Abusultan, Khatri. IEEE Transactions on Computers. Vol 65, issue 8, pp 2652-2658, Aug 2016.

"*Response to "Comment on 'Zero and negative energy dissipation at information-theoretic erasure'"*, Kish, Granqvist, Khatri, Peper. Accepted for publication in Journal of Computational Electronics. Vol 15, Issue 1, pp 343-346. Mar 2016.

"*Zero and negative energy dissipation at information theoretic erasure*", Kish, Granqvist, Khatri, Peper. Journal of Computational Electronics, 15(1), pp 335-339, Mar 2016.

"*Demons: Maxwell's Demon, Szilard's Engine and Landauer's Erasure-dissipation*", Kish, Granqvist, Khatri, Wen. International Journal of Modern Physics: Conference Series 33 (2014) 1460364-1 to 1460364-5.

"Simulation Analysis of Scintillation in a NaI Detector", Shah, Marianno, Khatri, Boyle. Journal of the Institute of Nuclear Materials Management (JNMM), Vol. 43, No. 1, Bonus content, 2014.

"List Mode with the ORTEC digiBASE-E", *Hearn*, Marianno, Khatri, *Gypp.* In Health Physics: The Radiation Safety Journal, Vol. 106, Issue 2, February 2014, pp S12-S15**.**

Invited paper, "*Using GPUs to Accelerate CAD Algorithms*", Croix, Gulati, Khatri. IEEE Design & Test, Vol. 30, Issue 1. February 2013, pp 8-16.

"On Optimal and Achievable Fix-Free Codes", Savari, *Yazdi*, *Abedini*, Khatri. IEEE Transactions on Information Theory 58(8): 5112-5129, 2012.

"Application of Max-SAT-based ATPG to optimal cancer therapy design", Lin, Khatri. BMC Genomics 2012, 13 (Suppl 6):S5, 26 October, 2012.

"A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Applications", *Turker*, Khatri, Sanchez-Sinencio. IEEE Transactions On Circuits and Systems – I, Vol. 58, No. 6, June 2011, pp 1225-1238.

"*Computation using Noise-based Logic: Efficient String Verification over a Slow Communication Channel*", Kish, Khatri, Horvath. European Journal of Physics B 79, January 2011, pp 85-90.

"*Noise-based deterministic logic and computing: a brief survey*", Kish, Khatri, Bezrukov, Peper, Gingl, Horvath. International Journal of Unconventional Computing 7, February 2011, pp 101-113.

"*A Simultaneous Input Vector Control and Circuit Modification Technique to Reduce Leakage with Zero Delay Penalty*", Jayakumar, Khatri. ACM Transactions on Design Automation of Electronic Systems, 2010.

"*Towards brain-inspired computing*", Gingl, Khatri, Kish. Fluctuation and Noise Letters 9, December 2010, pp 403–412.

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"*Instantaneous noise-based logic*", Kish, Khatri, Peper. Fluctuation and Noise Letters 9, December 2010, pp 323–330.

"Fault Table Computation on GPUs", Gulati, Khatri. Journal of Electronic Testing: Theory and Applications (JETTA). Vol. 26, No. 2, April 2010, pp 195-209.

"*Selective Forward Body Bias for High Speed and Low Power SRAMs*", Bollapalli, Garg, Gulati, Khatri. Accepted for publication at the Journal of Low Power Electronics (JOLPE), Vol. 5, No. 2, August 2009.

"*Encoding Serial Graphical Data for Energy-Delay Product/Energy Minimization*", Ekambavanan, Garg, Khatri, Narayanan. Accepted for publication at the Journal of Low Power Electronics (JOLPE), Vol. 5, No. 2, August 2009, pp 157-172.

"Noise-based Logic Hyperspace with the Superposition of 2^N States in a Single Wire". Kish, Khatri, *Sethuraman*. Physics Letters A. Vol. 373, No. 22, May 2009, pp 1928-1934.

"Circuit-level Design Approaches for Radiation-hard Digital Electronics", Garg, Jayakumar, Khatri, Choi. IEEE Transactions on Very Large Scale Integration Systems, Vol. 17, No. 6, June 2009, pp 781-792.

"Efficient On-Chip Crosstalk Avoidance CODEC Design", Duan, Cordero, Khatri. IEEE Transactions on Very Large Scale Integration Systems, Vol. 17, No. 4, April 2009, pp 551-560.

"FPGA-Based Hardware Acceleration for Boolean Satisfiability", Gulati, Paul, Khatri, Patil, Jas. ACM Transactions on Design Automation of Electronic Systems (TODAES). Vol. 14, No. 2, March 2009. **Among the top 10 downloaded papers for the journal in 2010. Nominated for best paper for the journal, 2010.**

"A Fast Hardware Approach for Approximate, Efficient Logarithm and Antilogarithm Computations", Paul, Jayakumar, Khatri. IEEE Transactions on Very Large Scale Integration Systems, Vol. 17, No. 2, February 2009, pp 269-277.

"A *Dynamically De-skewable Clock Distribution Methodology*", Jayakumar, Kapoor, Khatri. IEEE Transactions on Very Large Scale Integration (TVLSI), Vol. 16, No. 9, September 2008, pp 1220-1229.

"*Resource Sharing among Mutually Exclusive Sum-of-Product Blocks for Area Reduction*", Das, Khatri. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 13, No. 3, July 2008, pp 51:1-51:7.

"*Efficient, Scalable Hardware Engine for Boolean Satisfiability and Unsatisfiable Core Extraction*", Gulati, *Waghmode*, Khatri, Shi. IET Computers and Digital Techniques, Vol. 2, No. 3, May 2008, pp 214-229.

"*A Probabilistic Method to Determine the Minimum Leakage Vector for Combinational Designs in the Presence of Random PVT Variations*", Gulati, Jayakumar, Khatri, Walker. Integration, the VLSI Journal, Vol. 41, No. 3, May 2008, pp 399-412.

"*SAT-based ATPG using Multi-level Compatible Don't-Cares*", Gulati, Saluja, Khatri. ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 13, No. 2, April 2008, pp 24:1-24:18.

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"*A Novel Hybrid Parallel-Prefix Adder Architecture with Efficient Timing-Area Characteristic*", Das, Khatri. IEEE Transactions on Very Large Scale Integration, Vol. 16, No. 3, March 2008, pp 326-331.

"*A Timing-Driven Approach to Synthesize Fast Barrel Shifters*", Das, Khatri. IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 55, No. 1, January 2008, pp 31-35.

"*Polymer Sensors to Monitor Roach Locomotion*", *Lee*, *Cooper*, *Mika*, *Clayton*, Garg, Gonzalez, Vinson, Khatri, Liang. IEEE Sensors Journal, Vol. 7, No. 12, December 2007, pp 1698-1702.

"*High-throughput VLSI Implementations of Iterative Decoders and Related Code Construction Problems*". *Nagarajan*, *Laendner*, Jayakumar, Milenkovic, Khatri. Springer Journal of VLSI Signal Processing, Vol. 49, No. 1, October 2007, pp 185-206.

"*A Predictably Low Leakage ASIC Design Style*", Jayakumar, Khatri. IEEE Transactions on Very Large Scale Integration, Vol. 15, No. 3, March 2007, pp 276-285.

"*SPFD-based Wire Removal in Standard-cell and Network-of-PLA Circuits*"- Khatri, *Sinha*, Brayton, Sangiovanni-Vincentelli. IEEE Transactions on Computer-Aided Design of Circuits and Systems, Vol. 23, No. 7, June 2004, pp 1020-1030.

"*An Efficient and Regular Routing Methodology for Datapath Designs Using Net Regularity Extraction*". Das, Khatri. Short paper, IEEE Transactions on CAD, Vol. 21, Number 1. Special issue on Physical Design, January 2002, pp 93-101.

Peer-reviewed Journal Submissions Under Review:

"*A Self-Adaptive Physics-Informed Gated Recurrent Unit Neural Networks Model for Estimating the Lifetime of Li-ion Batteries* ", Saleh, Alquennah, Ghrayeb, Refaat, Abu-Rub, Khatri. Submitted to IEEE Transactions on Transportation Electrification (Under Review).

"A Review on the Aging Mechanisms and Lifetime Estimation Methods of XLPE Power Cables ", Saleh, Alquennah, Ghrayeb, Refaat, Abu-Rub, Khatri. Submitted to IEEE Open Journal of Industrial Applications (Under Review)

"*CapsPDNet: Optimized Capsule Network for Predicting Insulator Discharges Using UHF Signals"*, Saleh, Darwish, Ghrayeb, Refaat, Abu-Rub, Khatri, El-Haj. Submitted to IEEE Transactions on Instrumentation and Measurement (Under Review)

Conference Publications (All listed papers are peer-reviewed, except for invited papers):

"A Novel Mixed-Signal Flash-based Finite Impulse Response (FFIR)", Lee, Khatri, Ghrayeb. Proc. of the 30th ACM Asia and South Pacific Design Automation Conference (ASPDAC) 2025. Tokyo, Japan, January 20-23, 2025. pp 1216-1222.

"Self-Adaptive Physics Informed Neural Network for Paper Insulation Degree of Polymerization Prediction", Alquennah, Saleh, Ghrayeb, Abu-Rub, Refaat, Khatri. 50th Annual Conference of the IEEE Industrial Electronics Society (IECON) 2024. Chicago, IL, November 2024, pp 1-6.

"A PINN-based Lifetime Predictor for Oil-Impregnated Paper Insulation Degradation in Power Transformers using Degree of Polymerization". Saleh, Alquennah, Ghrayeb, Refaat, Abu-Rub, Al-Hajri, Khatri, Olesz, Guzinski. 2024 IEEE 18th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Gdynia, Poland. June 2024. pp 1-6.

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"*Power Delivery and Communication with an Infrared Laser (PaCIR)*", Vargass-Calderon, Eedara, Khatri. IEEE Conference on Technologies for Sustainability (SusTech) 2024. Portland, OR. Apr 2024.

"*Double Deep Q Networks Reinforcement Learning based Controller for Grid-Connected 7-Level PUC Inverter*", Alquennah, Chida, Zamzam, Trabelsi, Ghrayeb, Khatri. 2024 4th International Conference on Smart Grid and Renewable Energy (SGRE), Doha, Qatar, 2024, pp. 1-6.

"*A Review on the Applications of Blockchain-Based Smart Contracts in the Smart Grid*", Saleh, Khatri, Ghrayeb Refaat. 2024 4th International Conference on Smart Grid and Renewable Energy (SGRE), Doha, Qatar, 2024, pp. 1-6.

"*A Hardware Validation Framework for a Networked Dynamic Multi-factor Security Protocol*", Lee, Scott, Khatri Ghrayeb. 2023 6th International Conference on Advanced Communication Technologies and Networking (CommNet), Rabat, Morocco, 2023, pp. 1-7.

"*Scaled Population Division for Approximate Computing*", Bharathi, Khatri, Hu. IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) 2023, Vienna, Austria, August 7-8, 2023. pp. 1-6.

"An Extremely Low-Voltage Floating Gate Artificial Neuron", Scott, Khatri. 2023 IEEE International Conference on Circuits and Systems (ISCAS), May 21-25, 2023. Monterey, CA.

"A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator", Lee, Khatri, Vrudhula. 2023 International Symposium on Quality Electronic Design (ISQED), April 5-7 2023. San Francisco, CA.

"A Flash-based Digital to Analog Converter for Low Power Applications", Scott, Khatri. IEEE 40th International Conference on Computer Design (ICCD), October 2022. Lake Tahoe, CA. pp 1-8.

"TD3lite: FPGA Acceleration of Reinforcement Learning with Structural and Representation Optimizations", Hu, Hu, Khatri. IEEE 32nd International Conference on Field-Programmable Logic and Applications (FPL), Aug-Sept 2022. Belfast, UK, pp 79-85.

"A Flash-based Current-mode IC to Realize Quantized Neural Networks", Scott, Lee, Khatri, Vrudhula. IEEE Design Automation and Test in Europe (DATE) Conference, Mar 2022, Antwerp, Belgium. pp 1029-1034.

"Detection and Classification of Defects in XLPE Power Cable Insulation via Machine Learning Algorithms", Saleh, Refaat, Khatri, Ghrayeb, Abu-Rub. IEEE 3rd International Conference on Smart Grid and Renewable Energy, Mar 20-22, 2022. Doha, Qatar. pp 1-6.

"Formal Verification of a Dynamic Multi-factor Secure Communication Protocol", Scott, Khatri, Ghrayeb. IEEE 3rd International Conference on Smart Grid and Renewable Energy, Mar 20-22, 2022. Doha, Qatar. pp 1-6.

"CIDAN: Computing in DRAM with Artificial Neurons", Singh, Wagle, Vrudhula, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 349-356, Oct 2021, virtual conference.

"NIST-Lite: Randomness Testing of RNGs on an Energy-Constrained Platform", Lee, Bharathi, Lansford, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 41-48, October 2021, virtual conference. **Nominated for best paper award (one of 5 papers)**

"Scaled Population Subtraction for Approximate Computing", Bharathi, Hu, Khatri. 38th IEEE International Conference on Computer Design (ICCD) 2020, Oct 24-27, Virtual Conference. pp 348-355.

"*A Configurable BNN ASIC using a Network of Programmable Threshold Logic Standard Cells"*, Wagle, Khatri, Vrudhula. 38th IEEE International Conference on Computer Design (ICCD) 2020, Oct 24-27, Virtual Conference. pp 433-440.

"A Statistical Methodology for Post-Fabrication Weight Tuning in a Binary Perceptron", Azari, Wagle, Khatri, Vrudhula. IEEE 21st International Symposium on Quality Electronic Design (ISQED) 2020. Mar 25-26, 2020, Santa Clara, CA. pp 141-148.

"A Mathematical Framework for Exploring Protein Folding Dynamics using Probabilistic Model Checking", Biswas, Pal, Khatri. 3rd IEEE International Conference on Information and Computer Technologies (ICICT) 2020. Mar 9-12, 2020, San Jose, CA. pp 114-123.

"Scaled Population Arithmetic for Efficient Stochastic Computing". Zhou, Khatri, Hu, Liu. 25th Asia and South Pacific Design Automation Conference (ASPDAC) 2020. Jan 13-16, 2020. Beijing, China. pp. 611-616.

"Threshold Logic in a Flash", Wagle, Singh, Yang, Khatri, Vrudhula. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, pp 550-558. Nov 17-20, 2019.

"PAU: A Programmable Arithmetic Unit for use in Modern Microprocessors" Fairouz, Douglass, Bharathi, Khatri. 37th IEEE International Conference on Computer Design (ICCD), 2019. Abu Dhabi, UAE, Nov 17-20, 2019.

"A Memory-Efficient Markov Decision Process Computation Framework Using BDD-based Sampling Representation". Zhou, Khatri, Hu, Liu. Proceedings of the Design Automation Conference, 2019. Las Vegas, NV, June 2-6, 2019.

"Synchronization of Ring-Based Resonant Standing Wave Oscillators for 3D Clocking Applications", Douglass, Khatri. IEEE International Conference on Computer Design, Orlando, FL, Oct 2018. pp 318-325.

"A Plain-Text Incremental Compression (PIC) Technique with Fast Lookup Ability", Bharathi, Kumar, Fairouz, Al Kawam, Khatri. IEEE International Conference on Computer Design, Orlando, FL, Oct 2018. pp 389-396.

"*A Homomorphic Encryption Scheme Based on Affine Transforms*", Loyka, Zhou, Khatri. Proceedings of the 2018 ACM Great Lakes Symposium on VLSI (GLSVLSI), May 23-25, 2018, Chicago, IL. pp 51-56.

"*An FPGA-based Coprocessor for Hash Unit Acceleration*" Fairouz, Khatri. The 35th IEEE International Conference on Computer Design (ICCD). Nov 5-8, 2017, Boston, MA, pp 301 – 304.

"*Fast, Ring-Based Design of 3D Stacked DRAM*", Douglass, Khatri. The 35th IEEE International Conference on Computer Design (ICCD) 2017, Nov 5-8, 2017, Boston, MA, pp 665-672.

"Fast and Highly Scalable Bayesian MDP on a GPU Platform", Zhou, Khatri, Hu, Liu, Sze. 8th ACM Conference on Bioinformatics, Computational Biology, and Health Informatics, 2017. Boston, MA, Aug 20-23 2017. Pp 158-167.

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"SAT-Based Optimization for Flash-Based Digital Designs", Abusultan, Khatri. IEEE/ACM Design Automation Conferenec (DAC), Jun 18-22 2017, Austin, TX.

"Architectural Simulations of a Fast, Source-synchronous Ring-based Network-on-chip Design", Khatri, Mandal. 2017 AFCEA Autonomous Networking Technology Symposium (ANTS), June 13-14, Utica, NY.

"Design of a Flash-based Circuit for Multi-valued Logic", Abusultan, Khatri. Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 41-46, May 10-12, 2017. Banff, Canada. 24.4% acceptance rate.

"Circuit Level Design of a Hardware Hash Unit for use in Modern Microprocessors", Fairouz, Abusultan, Khatri. Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 101-106, May 10-12, 2017. Banff, Canada. 24.4% acceptance rate.

"A Robust C-element Design with Enhanced Metastability Performance", Sharma, Khatri. Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 95-100, May 10-12, 2017. Banff, Canada. 24.4% acceptance rate**. Best Paper Candidate.**

"*A Flash-based Digital Circuit Design Flow*", Abusultan, Khatri. IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2016, Austin, TX, Nov 2016.

"A GPU-CPU Heterogeneous Algorithm for NGS Read Alignment", Al Kawam, Khatri Datta. International Conference on Intelligent Biology and Medicine (ICIBM), Houston, TX, November 2016.

"*A Practical Methodology to Validate the Statistical Behavior of Bloom Filters*", Kottapalli, Khatri. International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) 2016, Pittsburgh, PA, Oct 2016.

"Implementing low power digital circuits using flash devices", Abusultan, Khatri. 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 109-116, Oct 3-5, 2016, Phoenix, AZ.

"A novel hardware hash unit design for modern microprocessors", Fairouz, Abusultan, Khatri. 2016 IEEE 34th International Conference on Computer Design (ICCD). pp 412-415, Oct 3-5, 2016, Phoenix, AZ.

"Exploring static and dynamic flash-based FPGA design topologies", Abusultan, Khatri. 2016 IEEE 34th International Conference on Computer Design (ICCD), pp 416-419, Oct 3-5, 2016, Phoenix, AZ.

"*A Ternary-valued, Floating Gate Transistor-based Circuit Design Approach"*, Abusultan, Khatri. IEEE International Symposium on VLSI (ISVLSI) 2016, Pittsburgh, PA. July 11-13, 2016, pp 719-724.

"*A GPU-based Implementation of a Sensor Tasking Methodology*", Chakravorty, Abusultan, Khatri. International Conference on Information Fusion (FUSION 2016), Heidelberg, Germany, July 5-8, 2016, pp 1398-1405.

"*Exploring Flash Devices to Implement Digital Circuits*", Abusultan, Khatri. IEEE/ACM Design Automation Conference (DAC), June 2016, Austin, TX.

"*The Neutron Detector Using Radiation Integrated Circuits*," Shah, Marianno, Khatri; 2016 IEEE Symposium on Radiation Measurements and Applications, Berkeley, CA, May 22-26, 2016.

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"*GPU acceleration for Bayesian control of Markovian genetic regulatory networks*", Zhou, Hu, Khatri, Liu, Sze, Yousefi. Workshop on Bioinformatics for Precision Medicine (held in conjunction with the International Conference on Health Informatics (BHI)) 2016), Las Vegas, NV, February 2016. pp 304-307.

"Exploring the viability of stochastic computing", de Aguilar, Khatri. International Conference on Computer Design (ICCD), New York City, NY, Oct 19-21, 2015. pp 391-394.

"*Critical Remarks on Landauer's theorem of erasure dissipation and the related issues of the molecular engines: Maxwell-demon and Szilard-engine*", Kish, Granqvist, Khatri, Smulko, 23rd International Conference on Noise and Fluctuations (ICNF 2015), Xian, China, June 2-5, 2015.

"An Efficient Approach to Sample On-Chip Power Supplies", Murray, Khatri. ACM Great Lakes Symposium on VLSI, Pittsburgh, PA, May 20-22, 2015, pp 241-244.

"Delay, Power and Energy Tradeoffs in Deep Voltage-scaled FPGAs", Abusultan, Khatri. ACM Great Lakes Symposium on VLSI, Pittsburgh, PA, May 20-22, 2015, pp 111-114.

"*An Asynchronous Network-on-Chip Router with Low Standby Power*", Elshennawy, Khatri. Accepted at the 32nd IEEE International Conference on Computer Design (ICCD), Seoul, Korea. October 19-22, 2014. Acceptance rate 31.1%. To appear.

"*An Area-efficient Ternary CAM Design using Floating Gate Transistors*", *Fedorov*, Abusultan, Khatri. Accepted at the 32nd IEEE International Conference on Computer Design (ICCD), Seoul, Korea. October 19-22, 2014, pp55-60. Acceptance rate 31.1%.

"Simulation Analysis of Scintillation in a NaI Detector", *Shah*, Marianno, Khatri, Boyle. Accepted at 55th Annual Meeting of the Institute of Nuclear Materials Management (INMM), Atlanta, GA. July 20-24, 2014. **Best paper award, Nonproliferation and Arms Control division.**

"*Look-up Table Design for Deep Sub-threshold through Full-supply Operation*", Abusultan, Khatri. Accepted at the 22nd IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), Boston, MA. May 11-13, 2014, pp 259-266. Acceptance rate 16.4%.

"A Comparison of FinFET based FPGA LUT Designs", Abusultan, Khatri. ACM/IEEE Great Lakes Symposium on VLSI Systems (GLSVLSI) 2014, Houston, TX. May 21-23, 2014. pp 353-358.

"Integrated Circuits Replacing PMTs" Shah, Marianno, Khatri. South Texas Chapter of the Health Physics Society's Student Presentations and Annual Business Meeting. March 2014.

"FPGA LUT Design for Wide-band Dynamic Voltage and Frequency Scaled Operation", Abusultan, Khatri, 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA) 2014, Monterey, CA. February 25-28, 2014.

Invited paper *""Demonic" challenge: Landauer's erasure-dissipation*" Kish, Granqvist, Khatri. 44th Winter Colloquium on the Physics of Quantum Electronics (PQE) 2014, Snowbird, UT. January 5-9, 2014.

"Techniques to Improve the Efficiency of SAT Based Path Delay Test Generation", *Bian*, Walker, Khatri. 27th International Conference on VLSI Design (2014), Mumbai, India. January 5-9, 2014, pp 50-55.

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Invited paper *"Demons: Maxwell demon; Szilard engine; and Landauer's erasure-dissipation*", Kish, Granqvist, Khatri, Wen. Hot Topic of Physical Informatics (HoTPI) 2013, Changsha, China. November 10-13, 2013.

"Noise-based algorithms for functional equivalence and tautology checking", Lin, Khatri. 31st IEEE International Conference on Computer Design (ICCD) 2013, Asheville, NC. October 6-9, pp 235-240.

"A low-jitter phase-locked resonant clock generation and distribution scheme", Mandal, Bollapalli, Jayakumar, Khatri, Mahapatra. 31st IEEE International Conference on Computer Design (ICCD) 2013, Asheville, NC. October 6-9, 2013, pp 487-490.

"Mixed structural-functional path delay test generation and compaction", Bian, Walker, Khatri, *Lahiri*. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2013, New York City, NY. October 2-4, 2013, pp 7-12.

"*Solving the SAT Problem Using Noise-Based Logic on FPGAs*", Belsare, Elshennawy, Khatri. IEEE/ACM Design Automation Conference (DAC) 2013, Austin, TX. June 2-6, 2013.

"*FPGA LUT Design for Wide-Band Dynamic Voltage and Frequency Scaled Operation*", Abusultan, Khatri. IEEE/ACM Design Automation Conference (DAC) 2013, Austin, TX. June 2-6, 2013.

"*GPU Implementation of a Scalabale, Non-Linear Congruential Generator for Cryptography Applications*", Belsare, Liu, Khatri. ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2013, Paris, France. May 2-3, 2013, pp 89-94.

"*A Source-synchronous Htree-based Network-on-Chip*", Mandal, Khatri, Mahapatra. ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2013, Paris, France. May 2-3, 2013, pp 161-166.

"*Architecture and 3D Device Simulation of a PIN Diode-based Gamma Radiation Detector*", Elshennawy, Marianno, Khatri. ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2013, Paris, France. May 2-3, 2013, pp 329-330.

"*Exploring topologies for source-synchronous ring-based Network-on-Chip*", Mandal, Khatri, Mahapatra. Design Automation and Test in Europe (DATE) Conference 2013, Grenoble, France. March 18-22, 2013, pp 1026-1031.

"*Crosstalk avoidance codes for 3D VLSI*", Kumar, Khatri. Design Automation and Test in Europe (DATE) Conference 2013, Grenoble, France. March 18-22, 2013, pp 1673-1678.

"*Timing aware partitioning for multi-FPGA based logic simulation using top-down selective hierarchy flattening*", Swaminathan, Lin, Khatri. IEEE International Conference on Computer Design (ICCD) 2012, Montreal, Canada. September 30 - October 3, 2012, pp 153-158.

"*An efficient arithmetic Sum-of-Product (SOP) based multiplication approach for FIR filters and DFT*", Kumar, Mandal, Khatri. IEEE International Conference on Computer Design (ICCD) 2012, Montreal, Canada. September 30 – October 3, 2012, pp 195-200.

"*Architectural simulations of a fast, source-synchronous ring-based Network-on-Chip design*", Mandal, Khatri, Mahapatra. IEEE International Conference on Computer Design (ICCD) 2012, Montreal, Canada. September 30 – October 3, 2012, pp 482-483.

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Invited Paper, "*Application of logic synthesis to the understanding and cure of genetic diseases*", Lin, Khatri. IEEE/ACM Design Automation Conference (DAC) 2012, San Francisco, CA. June 3-7, 2012, pp 734-740.

"*Boolean Satisfiability using noise based logic*", Lin, Mandal, Khatri. IEEE/ACM Design Automation Conference (DAC) 2012, San Francisco, CA. June 3-7, 2012, pp 1260-1261.

"*Alleviating NBTI-induced failure in off-chip output drivers*", Bhadviya, Mandal, Khatri. ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2012, Salt Lake City, UT. May 3-4, 2012, pp 295-298.

"*A fast, source-synchronous ring-based network-on-chip design*", Mandal, Khatri, Mahapatra. Design Automation and Test in Europe (DATE) Conference 2012, Dresden, Germany. March 12-16, 2012, pp 1489-1494.

"A Novel Cryptographic Key Exchange Scheme using Resistors", Lin, Ivanov, Johnson, Khatri. IEEE International Conference on Computer Design (ICCD) 2011, Amherst, MA. October 2011, pp 451-452.

Invited Paper, "*Noise-based Information Processing*", Kish, Khatri, Bezrukov, Peper, Gingl, Horváth. 21st International Conference on Noise and Fluctuations. Toronto, Canada. June 12-16, 2011, pp 28-33.

"*An Automated Approach for Minimum Jitter Buffered H-tree Construction*", Mandal, Jayakumar, Bollapalli, Khatri, Mahapatra. 24th International Conference on VLSI Design, Chennai, India. January 2-7, 2011, pp 76-81.

"*Interconnected Tile Standing Wave Resonant Oscillator based Clock Distribution Circuits*", Mandal, Karkala, Khatri, Mahapatra. 24th International Conference on VLSI Design, Chennai, India. January 2-7, 2011, pp 82-87.

"*Efficient Arithmetic Sum-of-Product (SOP) Based Multiple Constant Multiplication (MCM) for FFT*", Karkala, Wanstrath, Lacour, Khatri. International Conference on Computer-Aided Design (ICCAD) 2010, San Jose, CA. November 7-11, pp 735~738.

"*Exploring a Circuit Design Approach Based on One-Hot Multi-Valued Domino Logic*", Gope, Lin, Khatri. 2010 IEEE International Midwest Symposium on Circuits & Systems (MWSCAS), Seattle, WA. August 1-4, 2010, pp 69-72.

"*Minimum Leakage Vector Computation Using Weighted Partial MaxSAT*", Singh, Gulati, Khatri. 2010 IEEE International Midwest Symposium on Circuits & Systems (MWSCAS), Seattle, WA. August 1-4, 2010, pp 201-204.

"*Unique Radiation Detection Method Using Si based Integrated Circuits*", Marianno, Khatri. 2010 Annual Meeting of the Health Physics Society, Salt Lake City, UT. June 27 - July1, 2010.

"An Efficient Pulse Flip-Flop Based Launch-on-Shift Scan Cell", Kumar, Bollapalli, Khatri. IEEE International Symposium on Circuits and Systems (ISCAS) 2010, Paris, France. May 30 - June 2, 2010, pp 4105-4108.

"VLSI Implementation of a Non-Linear Feedback Shift Register for High-Speed Cryptography Applications", Lin, Khatri. Great Lakes Symposium on VLSI (GLS-VLSI) 2010. Providence, RI. May 16-18, 2010, pp 381-384.

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"Boolean Satisfiability on a Graphics Processor", Gulati, Khatri. Great Lakes Symposium on VLSI (GLS-VLSI) 2010. Providence, RI. May 16-18, 2010, pp 123-126.

"A SAT-based Scheme to Determine Optimal Fix-free Codes", Abedini, Khatri, Savari. Data Compression Conference (DCC), Snowbird, UT. March 24-26, 2010, pp 169-178. **Best student paper award.**

"Implementing Digital Logic with Sinusoidal Supplies", Bollapalli, Khatri, Kish. Design Automation and Test in Europe (DATE) conference, 2010, Dresden, Germany. March 8-12, 2010, pp 315-318.

Invited Paper *"DFM-Aware Structured ASIC Design"*, Gopalani, Garg, Khatri. International Symposium on Integrated Circuits (ISIC) 2009, Singapore, December 14-16, 2009, pp 29-32.

Invited Paper *"A PTL based Highly Testable Structured ASIC Design Approach"*, Gulati, Jayakumar, Khatri. International Symposium on Integrated Circuits (ISIC) 2009, Singapore. December 14-16, 2009, pp 33-36.

"A Variation Tolerant Circuit Design Approach using Parallel Gates", Garg, Khatri. Austin Conference on Integrated Systems and Circuits (ACISC) 2009, Austin, TX. October 26-27, 2009.

"Implementing Digital Logic with Sinusoidal Supplies", Bollapalli, Khatri, Kish. Austin Conference on Integrated Systems and Circuits (ACISC) 2009, Austin, TX. October 26-27, 2009, pp 315-318.

"A Weighted Partial MaxSAT Based Method to Determine the MLV for Combinational Designs", Singh, Gulati, Khatri. Austin Conference on Integrated Systems and Circuits (ACISC) 2009, Austin, TX. October 26-27, 2009.

"*On-chip Bidirectional Wiring for Heavily Pipelined Systems using Network Coding*", Bollapalli, Garg, Gulati, Khatri. IEEE International Conference on Computer Design (ICCD) 2009, Lake Tahoe, CA. October 4-7, 2009.

"*A PLL Design based on a Standing Wave Resonant Oscillator*", Karkala, Bollapalli, Garg, Khatri. IEEE International Conference on Computer Design (ICCD) 2009, Lake Tahoe, CA. October 4-7, 2009.

"*A Robust Pulsed Flip-Flop and its use in Enhanced Scan Design*", Kumar, Bollapalli, Garg, Soni, Khatri. IEEE International Conference on Computer Design (ICCD) 2009, Lake Tahoe, CA. October 4-7, 2009, pp 97-102.

"*A Radiation Tolerant Phase Locked Loop Design for Digital Electronics*", Kumar, Karkala, Garg, *Jindal*, Khatri. IEEE International Conference on Computer Design (ICCD) 2009, Lake Tahoe, CA. October 4-7, 2009, pp 505-510.

"*3D Simulation and Analysis of the Radiation Tolerance of Voltage Scaled Digital Circuits*", Garg, Khatri. IEEE International Conference on Computer Design (ICCD) 2009, Lake Tahoe, CA. October 4-7, 2009, pp 498-504.

Invited Paper "*Highly Parallel Decoding of Space-Time Codes on Graphics Processing Units",* Bollapalli, *Wu*, Gulati, Khatri, Calderbank. Annual Allerton Conference on Communication, Control and Computing, 2009, Urbana, IL. September 30 – October 2, 2009, pp 1262-1269.

"*RF Receiver and Transmitter for Insect Mounted Sensor Platform*", Duperre, Burgett, Garg, Khatri. IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2009, Cancun, Mexico. August 2-5, 2009, pp 264-267.

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"*An Automated Approach for SIMD Kernel Generation for GPU based Software Acceleration*", Gulati, Khatri. Symposium on Application Accelerators in High Performance Computing (SAAHPC) 2009, Urbana, IL. July 28-30, 2009.

"Sorting Binary Numbers in Hardware - a Novel Algorithm and its Implementation", Alaparthi, Gulati, Khatri. International Symposium on Circuits and Systems (ISCAS) 2009, Taipei, Taiwan. May 24-27, 2009.

"Low Power and High Performance SRAM Design using Bank-based Selective Forward Body Bias", Bollapalli, Garg, Gulati, Khatri. IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) 2009, Boston, MA. May 10-12, 2009, pp 441-444.

"Robust Window-based Multi-node Technology-Independent Logic Minimization", Cobb, Gulati, Khatri. IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI) 2009, Boston, MA. May 10-12, 2009, pp 357-362.

"SEU Hardened Clock Regeneration Circuits", Dash, Garg, Khatri, Choi. International Symposium on Quality Electronic Design (ISQED) San Jose, CA. March 16-18, 2009, pp 806-813.

"Design and Implementation of a Sub-threshold BFSK Transmitter", Paul, Garg, Khatri, Vaidya. International Symposium on Quality Electronic Design (ISQED) San Jose, CA. March 16-18, 2009, pp 664-672.

"Closed-Loop Modeling of Power and Temperature Profiles of FPGAs", Gulati, Khatri, Li. ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA). Monterey, CA. February 22-24, 2009, pp 287.

"Accelerating Statistical Static Timing Analysis Using Graphics Processing Units", Gulati, Khatri. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2009, Yokohama, Japan. January 19-22, 2009, pp 260-265.

"Efficient Analytical Determination of the SEU-induced Pulse Shape", Garg, Khatri. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2009, Yokohama, Japan. January 19-22, 2009, pp 461-467. **Selected among the finalists for the best paper award at the conference.**

"Fast Circuit Simulation on Graphics Processing Units", Gulati, Croix, Khatri, Shastry. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2009, Yokohama, Japan. January 19-22, 2009, pp 403-408.

"A Novel, Highly SEU Tolerant Digital Circuit Design Approach", Garg, Khatri. IEEE International Conference on Computer Design (ICCD) 2008, Lake Tahoe, CA. October 12-15, 2008, pp 14-20.

"A Timing-Driven Synthesis Approach of a Fast Four-Stage Hybrid Adder in Sum-of-Products", Das, Khatri. IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2008, Knoxville, TN. August 10-13, 2008, pp 507-510.

"Forbidden Transition Free Crosstalk Avoidance CODEC Design", Duan, Khatri. ACM/EDAC/IEEE Design Automation Conference (DAC) 2008, Anaheim, CA. June 8-13, 2008, pp 986-991.

"Towards Acceleration of Fault Simulation using Graphics Processing Units", Gulati, Khatri. ACM/ EDAC/IEEE Design Automation Conference (DAC) 2008, Anaheim, CA. June 8-13, 2008

pp 822-827.

"A Fast, Analytical Estimator for the SEU-induced Pulse Width in Combinational Designs", Garg, Nagpal, Khatri. ACM/ EDAC/IEEE Design Automation Conference (DAC) 2008, Anaheim, CA. June 8-13, 2008, pp 918-923.

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U.S. Patent 7880505:*"Low Power Reconfigurable Circuits with Delay Compensation"*, Khatri, Vaidya, Griffin, Jayakumar. Issued February 2011.

U.S. Patent 06598215: *"Datapath Design Methodology and Routing Apparatus".* Das, Khatri. Issued July 2003.

U.S. Patent 06156579: "*Circuit Identifier for use with Focused Ion Beam Equipment*." Khatri, Eisele. Issued December 2000.

U.S. Patent 05448182: "*Driver Circuit with Self-adjusting Impedance Matching.*" Countryman, Khatri. Issued September 1995.

U.S. Patent 05408131: "*Circuit Identifier for use with Focused Ion Beam Equipment*." Khatri, Eisele. Issued April 1995.

U.S. Patent 05347523: "*Data processing system having serial self address decoding and method of operation*." Khatri, Bruce, Moyer. Issued September 1994.

Teaching Experience

A summary of my teaching at Texas A&M is shown in the table below. For each course taught, the average (over all 8 categories) student evaluation ratings (out of 5) are listed, along with the course enrolment in parentheses. My graduate courses are offered through the distance education program as well.

	EE248	EE454	EE449	EE749	EE689 (logic) EE699	EE689 (circuits) EE752	EE689 (Scalable Distrib. Consensus)	EE689 (Quantum & Logic Synthesis)
F04	4.36 (29)							
S05					4.50 (9)			
F05						4.65 (18)		
S06		4.62 (47)						
F06	4.23 (47)				4.33 (22)			
S07						4.44 (12)		
F07			4.68 (34)		4.32 (20)			
S08			4.05 (39)					
F08			4.67 (14)			4.27 (16)		
S09			4.38 (16)					
F09	4.37 (46)				4.52 (6)			
S10			4.54 (24)					
S11			4.66 (29)					

	EE248	EE454	EE449	EE749	EE689 (logic) EE699	EE689 (circuits) EE752	EE689 (Scalable Distrib. Consensus)	EE689 (Quantum & Logic Synthesis)
F12			4.55 (19)			4.65 (12)		
S13			4.45 (46)		4.19 (12)			
F13			4.73 (55)					
S14			4.45 (59)					
F14			4.42 (70)					
S15			4.53 (61)					
F15			4.42 (53)	4.64 (14)				
S16			4.66 (35)					
S16				4.74 (40)	4.74 (14)			
F17			4.29 (20)	4.30 (25)				
S18			4.09 (58)	4.30 (13)	4.20 (17)			
F18			3.78 (60)	4.78 (20)				
S19			4.07 (72)	4.27 (36)				
F20			4.40 (57)	4.42 (9)				
S21			4.68 (122)	4.64 (12)				
F21			4.08** (51)	4.28** (30)				
S22			TBD (48)	TBD (21)			TBD (9)	
F22								TBD (28)
S23			TBD (59)	TBD (24)			TBD (5)	
F23			TBD (55)	TBD (29)				
S24			TBD (66)	TBD (22)				TBD (7)
F24			TBD (54)	TBD (34)		TBD (25)		

**** This data has missing entries in AEFIS (the PDF export and Excel export data do not agree and answers to several questions are missing). I have used information that is available, but do not use this data to compute averages due to the unreliability of the data.**

Texas A&M University, College Station (Fall 2025 - Spring 2026). I plan to develop a new graduate course on chiplet based design. This course will be first offered in Fall 2026.

Texas A&M University, College Station (Fall 2024). I modified my graduate course (ECEN 752) to include a substantial coverage of flash transistors, and flash-based accelerators of various special functions. The modified version of this course was first offered in Fall 2024.

Texas A&M University, College Station (Summer 2023). I revised all labs and lab manuals for ECEN 449 and ECEN 248, to be compatible with a newer version of the Xilinx FPGA software.

Texas A&M University, College Station (Fall 2022). I developed a new graduate elective course (ECEN 689) titled "Quantum and Logic Synthesis". This course covers quantum logic synthesis, and its connection with traditional logic synthesis. It was first offered in Fall 2022.

Texas A&M University, College Station (Spring 2022). I developed a new graduate elective course (ECEN 689) titled "Scalable Distributed Consensus". This course covers the mathematics of scalable cryptocurrency, and was first offered in Spring 2022.

Texas A&M University, College Station (Summer 2020). I redesigned all the labs for ECEN 248 (Digital Systems Design) and ECEN 449/749 (Microprocessor Systems Design) to be completely conducted without the need of a laboratory, in response to the pandemic. These modified labs can be used to create a distance ECE degree program, if need be.

Texas A&M University, College Station (Summer 2019). I redesigned all the labs for ENGR 217/PHYS 217 (Experimental Physics and Engineering Lab III – Electricity and Magnetism) redoing all lab manuals in the process.

Texas A&M University, College Station (Summer 2018). I am converting all the labs for ECEN 449 (Microprocessor Systems Design) and ECEN 248 (Digital Systems Design) to the Digilent Zybo Z7 FPGA board and redoing all lab manuals in the process.

Texas A&M University, College Station (Fall 2016 / Spring 2017). I converted all the labs for ECEN 449 (Microprocessor Systems Design) and ECEN 248 (Digital Systems Design) from the Xilinx ISE software to the Xilinx Vivado software, and from the Virtex hardware to the Kintex hardware, redoing all lab manuals in the process

Texas A&M University, College Station (Fall 2014). I am working on converting the laboratory exercises of two courses, ECEN 248 (Digital Systems Design) and ECEN 449 (Microprocessor Systems Design) to a mobile laboratory station environment, using mobile test equipment from National Instruments and Xilinx Inc.

Texas A&M University, College Station (Spring 2014). I have been working on developing a new undergraduate 2-semester course. In this course, students will design, synthesize, simulate, place, route, and tape out a digital Integrated Circuit (IC) in the first semester. This IC will be fabricated and the second semester of the course will involve testing and debugging the fabricated IC. The course will be a senior-level elective course. The knowledge and skills that the students will learn through this course will make them very attractive hires for the IC industry in Texas and the United States.

Texas A&M University, College Station (Spring 2014). I have obtained permission from the Department Head of the ECE Department to initiate a course (a pass/fail, 1 credit course for sophomores or seniors) in which I will discuss career issues. The course will cover life lessons that are important for a healthy career, including life-long learning, networking, people skills, career choices and self-improvement. The lectures will be augmented by visits from industry leaders who will be able to share their career lessons with the students. This course is under development, and will be submitted for approval in Fall 2014.

Texas A&M University, College Station (Summer 2013). I have begun converting all the lectures of ECEN 248 (Digital Systems Design) and ECEN 449 (Microprocessor Systems Design) into video lectures, to be posted online for students to use as a reference resource.

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Texas A&M University, College Station (Summer 2011). Along with Dr. Choi, I helped migrate the ECEN 248 Laboratories exercises to a Linux platform instead of a Windows platform, and update the laboratory manuals accordingly.

Texas A&M University, College Station (Fall 2009). In Fall 2009, I was awarded the "*Association of Former Students' Distinguished Achievement Award in Teaching*".

Texas A&M University, College Station (Summer 2008). Along with Dr. Choi, I redesigned the laboratory portion of ECEN 248 (Digital Systems Design). The laboratories of ECEN 248 were aging, hence the decision to redo them. The new exercises are designed to be more relevant to current-day design styles. New laboratory manuals were written as well.

Texas A&M University, College Station (Fall 2007, Spring 2008, Fall 2008, Spring 2009, Spring 2010, Spring 2011, Fall 2012, Spring 2013, Fall 2013, Spring 2014, Fall 2014, Spring 2015, Fall 2015, Spring 2016). In Fall 2007, I co-taught a course (ELEN 449 – Microprocessor System Design), which is a laboratory oriented course that covers digital VLSI design using reconfigurable hardware and software. Along with Dr. Reddy, in Summer 2007, I overhauled the lectures and the laboratories in Summer 2007, and developed the new course, which uses an FPGA board based on a hardware/software co-design toolkit. This made the ECEN 449 course in step with the design technologies and approaches used in industry today. From Spring 2008 onwards, I taught this course alone. I visited TAMU-Q in January 2008 to demonstrate the new labs to the faculty and laboratory coordinators.

Texas A&M University, College Station (Fall 2015, Spring 2016). I taught a course (ECEN 749 – Microprocessor System Design), which is a laboratory oriented course that covers digital VLSI design using reconfigurable hardware and software. This is a graduate version of ECEN 449, with additional tasks required for graduate credit.

Texas A&M University, College Station (Spring 2006). I taught a course (ELEN 454 – Digital Circuit Design), which covers digital VLSI design including MOSFETs, static and dynamic characteristics of CMOS circuits, interconnect modeling, memory design, etc.

Texas A&M University, College Station (Fall 2004, Fall 2006, Fall 2009). Taught a course (ELEN 248 - Introduction to Digital Systems Design) which is a sophomore-level course in switching theory and finite state machine design.

Texas A&M University, College Station (Fall 2005, Spring 2007, Fall 2008, Fall 2012). I taught a course (ELEN 689 – VLSI Circuit Design), which is similar in content to the ECEN 6003 course taught by me at the University of Colorado, Boulder.

Texas A&M University, College Station (Spring 2005, Fall 2006, Fall 2007, Fall 2009, Spring 2013, Spring 2016). I taught a course (ELEN 689 - VLSI Logic Synthesis), which covered two-level and multi-level logic synthesis and sequential logic synthesis. The course was renamed ECEN 699 before I taught it in Spring 2013.

University of Colorado, Boulder (Spring 2004). Taught a newly developed course (ECEN 6009 - Research Problems in VLSI) which consists of research readings in nano-electronics, embedded and real-time systems, and quantum computing. The course had a strong research focus. This course did not exist in the ECE curriculum prior to this semester. The enrolment for this course was 16.

University of Colorado, Boulder (Fall 2002/2003). Developed a new graduate class (ECEN 6013 - Computer-Aided Design Techniques for VLSI). This class covered circuit-level, switch-level, and logic-level simulation techniques, in addition to physical design topics like circuit partitioning, wave pipelining, and detailed routing for random logic as well as datapath circuits. The topics covered in

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this class did not exist in the ECE curriculum earlier. The focus of the class was research-centric, and the class had a research project in lieu of a final exam, to encourage students to perform research. This 3-unit course had an enrolment of 23 students (2002) and 16 students (2003).

University of Colorado, Boulder (Fall 2000/2001, Summer 2001/2002/2003). Developed a new graduate class (ECEN 6003 – Digital Circuit Design). The class covered design techniques applicable in a custom Deep Sub-micron VLSI design setting. The topics covered in this class did not exist in the ECE graduate curriculum earlier. The class had a research project in lieu of a final. This 3 unit course had an enrolment of 33 (10 via CATECS) in 2000, and 28 (11 via CATECS) in 2001. I also offered it via the CATECS tape library in Summer 2001 (1 student) and Summer 2002 (4 students) and Summer 2003 (10 students).

University of Colorado, Boulder (Spring 2000/2001/2003). Taught a graduate course (ECEN 6139 – VLSI Logic Synthesis). The course was significantly re-designed with respect to an existing course by the same name, with increased emphasis on VLSI design techniques that drive corresponding logic synthesis algorithms. Heavy emphasis on theory as well as practical applications of the topics being taught. The course had a research project in lieu of a final exam. This 3-unit course had an enrolment of 8 in 2000, 11 in 2001, and 22 in 2003.

University of Colorado, Boulder (Spring 2001/2002/2003). Taught a senior course (ECEN 4703 – Switching and Finite Automata Theory) on fundamentals of switching theory, two-level and multi-level logic optimization, and finite automata theory. This 3 unit course had an enrolment of 55 in 2001, 48 in 2002 and 41 in 2003. ***Course ratings (FCQs) for this course in Spring 2003 were the highest in a decade.***

Independent Study courses supervised for several TAMU and CU students: Individual students and dates not listed. The total would be approximately 100 students.

Informally advised a large number of ECE graduate (>35) and undergraduate (>120) students). I enjoy helping students with discussions on career choices, senior project selection, and by providing general guidance.

Xilinx Corporation, Santa Clara, CA (Summer 2000/2001/2002). Class on the VHDL (Verilog in 2001) hardware design language to employees of Xilinx Corporation in Colorado and California. This 11-week class emphasized practical HDL development and debugging. Each of these classes was attended by about 20 designers.

University of California, Berkeley (Spring 1998). Graduate Student Instructor for Professor Brayton's Logic Synthesis class, EECS 219B. The class is an advanced graduate-level class dealing with two-level and multi-level logic synthesis and optimization techniques.

University of California, Berkeley (1993-99). Held numerous seminars and presentations as part of weekly verification and logic synthesis seminar series, as well as class project presentations.

Motorola, Inc., Austin, TX (1989-93). Delivered numerous presentations as part of my role as Design for Testability (DFT) coordinator for the MC88110 design team. In addition, I performed several one-on-one DFT education sessions for interested design engineers.

Indian Institute of Technology, Kanpur, India. (1986-87). Conducted tutorial classes in basic electronics and electrical engineering subjects, intended to help sophomores. These were attended by approximately 75 students.

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Supervision of Students.

Current Ph.D. / M.S. / B.S. Students (Ph.D. listed first, then M.S., then B.S.)

Kyler Scott, Ph.D. student. Kyler is working with me on his PhD in the area of flash-based circuits for efficient implementation of neural networks. Kyler obtained his BS and MS degrees from Texas A&M University. Kyler's MS thesis was supervised by me.

Cheng-yen Lee, Ph.D. student. Cheng-yen is working with me on his PhD in the area of flash-based analog circuits as well as a fast hardware-assisted nonlinear optimization engine. Cheng-yen has his BS and MS degree from National Chiao Tung University (NCTU) in Hzinchu, Taiwan.

Pranay Kumar Eedara, Ph.D. student. Pranay is working with me on his PhD in the area of applying VLSI CAD algorithms to the problem of drone routing. Pranay has his MS from Texas A&M University, and his BS from IIT Bhubaneshwar, India. Pranay is a ECE fellowship recipient.

Shao-Wei Chu, Ph.D. student. Shao-Wei will be joining my group in Fall 2022. Shao-Wei will be working on logic synthesis techniques for VLSI security, and also blockchain. Shao-Wei is an ECE fellowship recipient and has received his MS degree from National Taiwan University, Taipei.

Alamera Nouran Nader Alquennah, PhD. Student. Alamera is working with me (and Ali Ghrayeb at TAMUQ), on her PhD in machine learning techniques to predict degradation of power grid equipment. Alamera received her BS and MS degrees in Electrical Engineering from Kywait University.

Gautham Nemani, M.S. Student. Gautham is working with me on his MS in the area of arithmetics. Gautham received his BS degree from the Indian Institute of Technology, Tirupathi, in 2022.

Graduated Ph.D. / M.S. Students (Ph.D. listed first):

Mohammad AlShaikh Saleh, Ph.D. student. Mohammad worked with me (and Ali Ghrayeb at TAMUQ), on computational and machine learning techniques to enhance power grid reliability and stability. Mohammad has a Masters degree from TU Munich (Germany) and a BS degree from The University of Applied Sciences Upper Austria. Mohammad successfully defended his Ph.D. in Spring 2025.

He Zhou, Ph.D. candidate. He is working on her Ph.D. degree in ECE, in the area of accelerating computations in genomics and classification using FPGA and GPU platforms. He is being co-advised by Dr. Jiang Hu (ECE, TAMU) as well as me. He obtained her BS degree from X'ian Jiaotong University in China in 2013, and has been pursuing her graduate work at Texas A&M since 2013. He defended her thesis in Summer 2019.

Abbas Fairouz, Ph.D. candidate. Abbas obtained his Ph.D. degree in the areas of VLSI design and design automation. Abbas received his B.S. and M.S. in Computer Engineering from Kuwait University, and his Ph.D. research is supported by the Kuwait Government. Abbas completed his PhD in Summer 2019.

Monther Abusultan, Ph.D. candidate. Monther completed his Ph.D. degree in Fall 2016. His research included techniques to use floating-gate transistors for digital circuit designs. Monther has his B.S. and M.S. degrees from Montana State University, Bozeman, MT. Monther is currently with Intel Corporation in Hillsboro, OR.

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Kun Bian, Ph.D. Student. Kun obtained his Ph.D. in Fall 2013, in the area of using Boolean Satisfiability techniques to speed up delay testing. Kun was a CSE student, primarily advised by Dr. Hank Walker. I served as his co-advisor. Kun has a B.S. from Tsinghua University (China), and an M.S. from Stanford University and Rensslaer Polytechnic Institute. Kun is currently with Broadcom, Inc.

Kent Lin, Ph.D. Student. Kent defended his Ph.D. in Spring 2013, and worked on his Ph.D. with my group since Spring 2009 in the areas of GPU based extraction of the Gene Regulatory Network for cancer, and on cryptographic key generator circuits. Kent received his B.S. degree from UC Berkeley, and his M.S. degree from Yale University. Kent is currently with Synopsys, Inc.

Ayan Mandal, Ph.D. Student. Ayan obtained his Ph.D. in Spring 2013, and has been working in my group since Spring 2010, in the areas of Network-on-Chip (NoC) architectures based on a resonant clock based source-synchronous paradigm, and on low-jitter clock distribution networks. Ayan received his B.S. degree from IIT Kharagpur, India. Ayan was co-advised by Prof. Rabi Mahapatra (CSE, TAMU), although I was Ayan's primary Ph.D. thesis advisor. Ayan is currently with Intel Corporation, in Bangalore, India.

Kanupriya Gulati, Ph.D. Student. Kanupriya's Ph.D. research was in the area of VLSI-CAD algorithm acceleration using FPGAs and GPUs. Kanupriya graduated in Fall 2009. Kanupriya has a B.S. from the Delhi College of Engineering in India, and her M.S. from Texas A&M University (from my group). She received the *NVIDIA fellowship* ($25,000) for the 2008-9 academic years. Kanupriya worked at Intel Corporation's Strategic CAD Laboratory (SCL) in Hillsboro, OR, after graduation, and is currently pursuing her MBA degree from Harvard University.

Rajesh Garg, Ph.D. student. Rajesh's Ph.D. research was in the area resilient circuit design (including radiation tolerant circuit design and variation tolerant circuit design/analysis). In addition, Rajesh has publications in the areas of Pass Transistor Logic based VLSI circuit design, statistical sensitizable timing analysis in VLSI, extreme low power transceiver design, fabric based circuit design and flip-flop design. Rajesh successfully defended his Ph.D. in Spring 2009. Rajesh has a B.S. from IIT Delhi, and a M.S. from Texas A&M University (from my group). Rajesh began full-time employment at Intel Corporation in Hillsboro, OR starting April 2009.

Chunjie Duan, Ph.D. student. Chunjie worked with me on encoding techniques to avoid cross-talk in on-chip VLSI buses and VDD-scaling approaches for Embedded Real-time Systems. Chunjie passed his Ph.D. preliminary examination in Spring 2002, and his Ph.D. comprehensive exam in Fall 2007. He defended his Ph.D. thesis in Spring 2008. Chunjie is employed at the Mitsubishi Electric Research Laboratory (MERL) in Cambridge, MA.

Sabyasachi Das, Ph.D. student. Sabyasachi's dissertation was in the area of datapath design automation techniques. Sabyasachi passed his Ph.D. preliminary examination in Spring 2001, his comprehensive exam in Spring 2007 and his dissertation in Fall 2007. Sabyasachi is currently with Xilinx, Inc. in Silicon Valley.

Nikhil Jayakumar, Ph.D. student. Nikhil worked with me on leakage current reduction in VLSI design, extreme low power circuit design approaches, and VLSI implementation of LDPC codes. Nikhil passed his Ph.D. preliminary examination in Spring 2003 and defended his Ph.D. in Fall 2007. Nikhil is currently with a stealth-mode startup in San Jose, CA.

Brock LaMeres, Ph.D. student. Brock's research involved efficient board-level I/O design methodologies, including inductive cross-talk reduction using hardware and software approaches. Brock passed his Ph.D. preliminary examination in Spring 2004, and defended his Ph.D. thesis in October 2005. Brock is currently an Associate Professor at Montana State University.

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Kushagra Gupta, M.S. Student. Kushagra obtained his M.S. with me in the area of a light-weight cloud based computing architecture. Kushagra has a BS degree from Motilal Nehru National Institute of Technology, Allahabad, India.

Kyler Scott, M.S. student. Kyler obtained his MS degree in Spring 2022, in the area of flash-based Digital to Analog Converters (DACs). Kyler obtained his BS from Texas A&M University.

Joellen Lansford, M.S. Student. Joellen worked with me in the area of a embedded system implementation of a secure 2-party (and a 3-party) communication protocol. Joellen joined Texas A&M on a scholarship from Los Alamos National Laboratories. Joellen graduated in Spring 2021.

Andrew Douglass, MS candidate. Andrew completed his BS Honors thesis with me in Spring 2017. His research topic was a fast resonant ring-based data delivery fabric for next-generation 3D stacked memory designs. He graduated with his MS degree in Spring 2019.

Harsh Kumar, M.S. candidate. Harsh has been working with me on his M.S. degree since Spring 2015, and defended in Fall 2016, in the area of searchable compression of textual data. Harsh obtained his BS in Electronics in 2011, and then worked as a software developer until July 2014. Harsh is currently with Intel Corporation.

Kinshuk Sharma, M.S. student. Kinshuk has been working on his M.S. degree with me since Spring 2015, and defended in Summer 2016, in the area of on-chip synchronizers to communicate signals between different clock domains. Kinshuk obtained his BS degree in Electrical Engineering from the Indian Institute of Technology, Rourkee in 2013.

Amr Elshennawy, M.S. student. Amr started on his M.S. degree in Fall 2011, and defended in Fall 2014. His research interests include GPU based implementations of algorithms (Boolean Satisfiability, radiation transport), and radiation detection circuits. Amr obtained his B.S. from Cairo University in Egypt in 2009, and worked as a software engineer (at IBM, Mentor Graphics and Cerner Corp.) between 2009 and 2011. Amr is currently with Intel Corporation in Hillsboro OR.

Luke Murray, M.S. candidate. Luke started with me on his M.S. degree since Fall 2013, and finished in Fall 2014. Luke has a B.S. from the ECE Department at Texas A&M University, and his research topic covers circuit approaches to sample the on-chip power grid for efficient chip diagnostics. Luke is currently with IBM Corporation in Austin, TX

Rajeev Kumar, M.S. Student. Rajeev obtained his M.S. degree in Spring 2013. His research was on fast FFT and DFT computations using Sum-of-Product (SOP) based architectures. Rajeev has his undergraduate degree from IIT Guwahati in India, in 2007. Rajeev worked at ARM from 2007 to 2010. Rajeev is currently with Broadcom, Inc.

Subramanian Poothamkurissi, M.S. Student. Subramanian obtained his M.S. degree in Fall 2012. His research consisted of partitioning RTL netlists for FPGA based emulation. Subramanian has his B.S. degree from NIT Trichy in India. Subramanian is currently with Apple, Inc.

Rajesh Kumar, M.S. Student. Rajesh obtained his M.S. degree in Summer 2010. His thesis was on radiation tolerant VLSI IC design. Rajesh obtained his B.S. from IIT Roorkee, and has 2 years experience with ST Microelectronics. Rajesh is currently working at Qualcomm, Inc.

Vinay Karkala, M.S. Student. Vinay obtained his M.S. degree in Summer 2010. His thesis was on resonant clocks in VLSI designs. Vinay obtained his B.S. from IIT Madras, India, and has 1 year experience with Cypress Semiconductor. Vinay is currently with Qualcomm, Inc.

Kalyana Bollapalli, M.S. Student. Kalyana's M.S. thesis was in the area of IP routing table compression using Logic Synthesis techniques. Kalyana also worked in the area of hardware acceleration of the logic tautology problem, MIMO decoding on a GPU platform, noise based logic realization, network coding for unicast wiring in VLSI, and low leakage memory design. Kalyana has a B.Tech degree from IIT Bombay in India. Kalyana is currently with NVIDIA Corporation in San Jose, CA.

Charu Nagpal, M.S. Student. Charu's work was in the area of radiation tolerant circuit design, as well as approaches to design circuits in the presence of noisy components. Charu graduated in May 2008 and works in the Atom group of Intel Corporation, in Austin, TX.

Jeff Cobb, M.S. student. Jeff's research was in the area of Logic Synthesis for VLSI, including novel Boolean multi-node minimization techniques. Jeff is currently with Apple, Inc.

Suganth Paul, M.S. Student. Suganth's research was in the area of subthreshold IC design, efficient arithmetic circuit implementation, and hardware approaches to accelerate VLSI algorithms. Suganth graduated in December 2007, and is now with the Atom group in Intel Corporation in Austin, TX.

Ekambavanan Sasidharan, M.S. Student. Sasidharan's research was in the area of energy-delay product minimization in serial data transmission, as well as energy minimization in parallel buses. Sasidharan graduated in May 2007, and is currently with LinkaMedia in Silicon Valley.

Rajesh Garg, M.S. student. Rajesh defended his M.S. under my supervision in Spring 2006, and worked with me on his Ph.D. since. He completed his Ph.D. requirements in Spring 2009.

Kanupriya Gulati, M.S. student. Kanupriya defended her M.S. under my supervision in Spring 2006, and subsequently worked with me on her Ph.D. thesis.

Karandeep Singh, M.S. student. Karandeep's research was in the area of Don't Care enhanced technology mapping for VLSI, exploitation of battery recovery effects in scheduling computation for mobile applications, and timing optimization of VLSI circuits. Karandeep graduated in May 2007, and is currently with Texas Instruments in Houston, TX.

Undergraduate Students (B.S. Honors Thesis and Senior Project students listed first):

Zach Assad, BS Senior Design student. Zach is working with me on his senior design project on flash-based key-value stores. He will graduate in 2025.

Brayden Vargas-Calderon, BS Senior Design student. Brayden is working with me on his senior design project on wireless power delivery (combined with communication). He will graduate in 2024.

Thomas Dexter, BS Senior Design student. Thomas is working with me on his senior design project on the design and validation of a new cryptographic hash function. He will graduate in Spring 2023.

Conner Wallis, BS Senior Design student. Conner worked with me on his senior design project on the testing of a alpha particle detecting IC which we had developed in my lab a few years ago. He graduated in Fall 2021.

Daniel Schwartz, BS Honors student. Under my supervision, Daniel completen his BS Honors thesis in the area of a disk-less cloud-based computing system in Spring 2020.

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Hung Bui, BS Honors student. Under my supervision, Hung completed his BS Honors thesis in the area of a disk-less cloud-based computing system in Spring 2020.

Kyler Scott, BS Senior Project student. Kyler is working with me on his BS senior project in the area of multi-port readable memories, using a single physical port. Kyler is expected to graduate in Fall 2019

Matthew Skolaut, BS candidate. Matthew is working with me on his capstone project in the area of wireless (infrared) data and power delivery for portable and hand-held electronics. Matthew is expected to graduate in Fall 2019

Jacob Sacco, BS Honors thesis candidate. Jacob is working with me on his BS Honors thesis in the area of FPGA based implementation of efficient machine learning engines. Jacob is expected to graduate in Spring 2019.

Joseph Harris, BS Honors thesis candidate. Joseph is working with me on his BS Honors thesis in the area of wireless (infrared) data and power delivery for portable and hand-held electronics. Joseph is expected to graduate in Spring 2019.

Ryan Bailey, BS Honors thesis candidate. Ryan is working with me on his BS Honors thesis in the area of fast ring-based data transfer fabrics to implement a reservation station in a modern microprocessor. Ryan graduated in Fall 2018.

Andrew Douglass, B.S. Honors Thesis. Andrew completed his BS Honors thesis with me in Spring 2017. His research topic was a fast resonant ring-based data delivery fabric for next-generation 3D stacked memory designs.

Kyle Loyka, B.S. Honors Thesis. Kyle has been working with me on research in sleep apnea since Summer 2016, under the auspices of the NSF REU program. Kyle completed his BS Honors thesis with me in Spring 2017. His research topic was an efficient homomorphic encryption technique based on affine transforms.

Michael Bass, Honors B.S. Thesis. Mike obtained his Honors thesis in Spring 2015, on the area of a combined language for synthesis of hardware as well as software. He is also working on a radiation detection multi-channel analyzer (MCA) with me. Mike obtained his BS degree from the ECE department at Texas A&M in Spring 2015.

John Leslie, Honors B.S. Thesis. John obtained his Honors thesis in Spring 2015, in the area of hardware engines for enhanced credit card security using physically unclonable functions. John obtained his BS degree from the ECE department at Texas A&M in Spring 2015.

Shayok Dutta, Honors B.S. Thesis. Shayok obtained n his Honors thesis in Spring 2015, in the area of hardware engines for enhanced credit card security using physically unclonable functions. Shayok obtained his BS degree from the ECE department at Texas A&M in Spring 2015.

Amnay Amimeur, Honors B.S. Thesis. Amnay obtained his Honors thesis in Spring 2015, in the area of hardware engines for enhanced credit card security using physically unclonable functions. Amnay obtained his BS degree from the ECE department at Texas A&M in Spring 2015.

Salman Gopalani, Honors B.S. Thesis. Salman successfully graduated in May 2007, while working on an undergraduate Honors thesis with me. His thesis was on the topic of NAND2 gate based structured ASIC design approaches. This thesis was obtained under the auspices of the Honors Thesis program at TAMU. Salman is currently with National Instruments in Austin, TX.

Advised an undergraduate student (**John Pickering**) in Spring 2016. John worked on circuit modeling of ambipolar devices using HSPICE.

Jordan Taylor, B.S. candidate. Jordan has been working with me on research in infrared light based communication since Fall 2014. Jordan joined Texas A&M in Fall 2014, and is expected to complete his B.S. degree in Fall 2018.

Dakota Plesa, B.S. candidate. Dakota has been working with me on research in the area of secure erasure of flash-based memory (SSDs, memory sticks) using beta radiation since Spring 2015. Dakota joined Texas A&M in Fall 2014, and is expected to graduate with his B.S. degree in Fall 2018.

Michael Bartling, B.S. candidate. Michael worked with me on a project to solve the Boolean Satisfiability (SAT) problem using a map-reduce algorithm running on Texas A&M's Supercomputing cluster. By partitioning the SAT problem, we attempted to obtain a significant speedup for this very important problem.

Matthew Romero. I advised Matthew during Summer 2013. Matthew worked on a semester-long study of different kinds of memory technologies that are on the horizon, comparing and contrasting them with existing memory technologies in terms of speed, power consumption, reliability, and volatility.

Ahmed Elsherif, Kirk Lundblade. Advised these two USRG students in the Summer of 2011.

Nick Barnes, Alex Ivanov and Bradley Johnson. I advised these students in Summer 2010, under the NSF REU and USRG programs. The work conducted by Alex and Bradley involved designing an FPGA based shared cryptographic key generator using resistors, and was accepted at the IEEE International Conference on Computer Design (ICCD) 2011.

Joseph Wanstrath and Travis LaCour. I advised these students during Summer 2009, under the NSF Research Experience for Undergraduates (REU) program. Joseph and Travis' work involved building a Sum-of-Products based Multiple Constant Multiplication (MCM) algorithm for Fast Fourier Transform (FFT) applications. Their work was accepted at ICCAD 2010, and an extended version of this work has been submitted to the ACM Transactions on Design Automation of Electronic Systems (TODAES).

Gordon Burgett, Joseph Duperre and Jacob Bachmeyer. I advised these students during Summer 2008, under the NSF Research Experience for Undergraduates (REU) program. Gordon and Joseph won the first and second prizes for their REU work at TAMU, which involved the design of a RF transmitter (to be carried on the back of a roach) and receiver. A paper based on this effort was accepted at the IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2009.

Prince Varghese and Brandon Buscher. I advised these students during Summer 2007, under the NSF Research Experience for Undergraduates (REU) program.

Mario Sanchez, Anshul Gupta. Advised these students in 2005. The work conducted with these students resulted in a conference publication, and the proposed circuit design approach improved circuit area as well as speed appreciably, compared to the traditional standard-cell based design approach.

Eric Menendez and Dumezie Maduike. I advised these students during Summer 2005, under the NSF Research Experience for Undergraduates (REU) program. They received the first prize for their REU work at TAMU, which involved the design of a fast comparator. The work they performed

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was subsequently published at the International Conference on Computer Design (ICCD) 2006. Both students are currently pursuing graduate studies.

Advised TAMU EE undergraduates Rob Hammond and Anshul Gupta, under the URA program (2004-05).

Invited Talks

Note: ***Invited panel, invited tutorials, or invited paper talks are listed under separate heading.***

Indian Institute of Technology, Kanpur, India. (January 2014). Invited to present a talk on our work in applying Logic Synthesis to the understanding and cure of genetic diseases.

Advanced Micro Devices (AMD), Austin, TX. (December 2012). Invited to present a talk on our work on GPU based EDA algorithm acceleration.

University of Texas MD Anderson Research Center. (May 2010). Invited to present a talk on our work in logic techniques to infer the predictors for gene regulation.

University of California, Los Angeles (April 2009). Invited to present a talk on our work on specialized hardware architectures for solving Boolean Satisfiability.

University of Michigan, Ann Arbor (March 2009). Invited to present a talk on our work on our variation tolerant sub-threshold design flow.

University of Texas, Austin (February 2009). Invited to present a talk on our work on sub-threshold design of a BFSK transmitter.

Intel Corporation, Strategic CAD Labs, Hillsboro, OR (May 2008). Invited to present talks on GPU based acceleration of VLSI CAD algorithms, as well as extreme low power sub-threshold design.

Nascentric, Inc., Austin, TX (February 2007). Invited to present a talk on FPGA and GPU architectures for high speed circuit simulation.

Samsung Microelectronics, Seoul, Korea (August 2003). Invited to present two lectures on cross-talk immune VLSI design, and cross-talk avoidance in on-chip VLSI buses.

Indian Institute of Technology, Kanpur, India (August 2001). Presented a guest lecture on Bus Encoding to Alleviate Cross-talk in VLSI Design.

Indian Institute of Technology, Bombay, India (August 2001). Presented a guest seminar on Bus Encoding to Alleviate Cross-talk in VLSI Design.

Indian Institute of Technology, Delhi, India (August 2001). Presented a talk on Detailed Routing of Datapath Designs using Net Regularity Extraction.

Indian Institute of Technology, Madras, India (August 2001). Presented a guest lecture on Detailed Routing of Datapath Designs using Net Regularity Extraction.

Seagull Semiconductor, Austin, TX (August 2000). Invited to give a presentation on Network Flows and Graph Theoretic techniques to model an InfiniBand switch fabric I/O system.

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Applications discussed included a performance simulator, and a tool to estimate reliability of connections in a switched fabric I/O system.

Hewlett-Packard Company, Fort Collins, CO (August 2000). Invited to give a talk on "Accurate Static CMOS Standard Cell Library Characterization".

Cirrus Logic, Broomfield, CO (July-August 2000). Two separate invited talks. One was on "Cross-talk Immune VLSI Design using Regular Layout Fabrics", and the other on "Mixed-signal Testing using Multi-valued Satisfiability".

Cadence Design Systems, San Jose, CA (March 2000). Invited presentation, "Network of PLA based VLSI design using Regular Layout Fabrics".

Sun Laboratories, Menlo Park, CA (March 2000). Invited to present my work on ASIC Design Flows for Deep-Submicron VLSI Design.

National Semiconductor Corporation, Santa Clara, CA (1999). Invited lecture on Sets of Pairs of Functions to be Distinguished (SPFDs) and their use in multi-level logic synthesis, with an emphasis on wire removal.

Honors and Impact

Received the "Engineering Teaching Excellence Award" from the College of Engineering, Texas A&M University, in Spring 2024.

Affiliate Scientist, National Center for Atmospheric Research (2022-2025). I was invited to serve as an Affiliate Scientist by NCAR (Boulder, CO), a leading weather research laboratory. I will be helping NCAR in the design of the radar down-conversion hardware for an airborne phased-array radar system that they are designing. An application to extend this position for 3 additional years is in progress.

"NIST-Lite: Randomness Testing of RNGs on an Energy-Constrained Platform", Lee, Bharathi, Lansford, Khatri. 39th IEEE International Conference on Computer Design (ICCD) 2021, pp 41-48, October 2021, virtual conference. **Nominated for best paper award (one of 5 papers)**

Received the "Outstanding Professor Award" in the of ECE, Texas A&M University, 2020. This award is in "recognition of teaching, research and service excellence".

Awarded the Air Force Research Laboratory (AFRL) *"Entrepreneural Research Fellowship – Flash-based Hardware Security",* in 2020. The total amount of this award is $100K.

I was awarded the "*Association of Former Students' Distinguished Achievement Award in Teaching (College Level)*", in Fall 2019.

Our paper *"A Robust C-element Design with Enhanced Metastability Performance"* co-authored by Sharma, Khatri, was deemed **Best Paper Award Candidate.** It appeared in the proceedings of the Great Lakes Symposium on VLSI (GLSVLSI) 2017, pp 95-100, May 10-12, 2017. Banff, Canada (24.4% acceptance rate)**.**

My student **John Leslie (an US Army Veteran) recommended me to the Texas A&M University Veteran Resource and Support Center** as the faculty who has made the greatest impact to their career. I received a medallion coin, and a letter from the Director of the Veteran Resource and Support Center, acknowledging my support of John's career.

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My student **Michael Bass** graduated with his B.S. degree in Spring 2015, and received the **"Brown Family – Earl Rudder Outstanding Student Award"** among all the graduating students in Spring 2015. Michael is continuing with me on his Ph.D. degree starting Fall 2015.

"Simulation Analysis of Scintillation in a NaI Detector", Shah, Marianno, Khatri, Boyle. Accepted at 55th Annual Meeting of the Institute of Nuclear Materials Management (INMM), Atlanta, GA. July 20-24, 2014. **Best paper award, Nonproliferation and Arms Control division.**

The Ph.D. thesis of Ayan Mandal, of my students, was nominated for the ACM Best Dissertation Award, 2014 (outcome awaited).

Our work on GPU-based acceleration of EDA algorithms was featured in Deep Chip, (www.deepchip.com), a EDA and VLSI newsletter in February 2013. The article stated that "Five years ago, two researchers from Texas A&M (Gulati & Khatri), gave at DAC 08, the first paper on GPU acceleration for EDA SW".
http://deepchip.com/items/0518-03.html?goback=%2Egde_772377_member_215279073

My work (with Dr. Laszlo Kish) on noise-based logic is featured in its own Wikipedia page. http://en.wikipedia.org/wiki/Noise-based_logic

My work (with Dr. Laszlo Kish) on noise based logic was featured in New Scientist Tech. Issue 2780, 7 October 2010, in an article by Justin Mullins titled "Breaking the Noise Barrier -- Enter the Phonon Computer".

My group was the first to exploit GPUs to accelerate VLSI design algorithms. One of the first algorithms we accelerated on the GPU was *circuit simulation*. Our work in this area was funded by Nascentric Inc., an Austin, Texas startup. Nascentric's fast circuit simulator was sped up by a further 2.5X as a result of our research, and incorporated into their product offering.

The Wikipedia entry on "Logic Synthesis" is based on the material I wrote for an invited chapter titled "*Logic Synthesis*" in the CRC EDA handbook "EDA for IC Implementation, Circuit Design and Process Technology". Chapter co-authored by Narendra Shenoy of Synopsys Inc.

"*A SAT-based Scheme to Determine Optimal Fix-free Codes*", Best Student Paper Award at the Data Compression Conference (DCC), Snowbird, UT. March 24-26, 2010. My co-authors on this paper were Navid Abedini and Prof. Serap Savari (ECE, TAMU).

*"***FPGA-Based Hardware Acceleration for Boolean Satisfiability***"*, Gulati, Paul, Khatri, Patil, Jas. ACM Transactions on Design Automation of Electronic Systems (TODAES). Vol. 14, No. 2, March 2009. **Among the top 10 downloaded papers for the journal in 2010. Nominated for best paper for the journal (2010).**

I was awarded the "*Association of Former Students' Distinguished Achievement Award in Teaching*", in Fall 2009.

"*Fault Table Generation Using Graphics Processing Units*", Gulati, Khatri. IEEE International Test Synthesis Workshop 2009, Austin, TX. March. 23-25, 2009. **Received best student paper award.**

My Ph.D. candidate Kanupriya Gulati received the NVIDIA Fellowship for the 2008-2009 terms. This fellowship award included funds to the tune of $25,000, to be spent towards her Ph.D. research.

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"Efficient Analytical Determination of the SEU-induced Pulse Shape". IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) 2009, Yokohama, Japan. January 19-22, 2009, pp 461-467. **Selected among the finalists for the best paper award at the conference.** My co-author on this paper was my student Rajesh Garg.

Our 2008 paper titled "*A Single-Supply True Voltage Level Shifter*" has been **incorporated in the IC designs of LSI Logic Corporation.**

Undergraduates Joseph Duperre and Gordon Burgett, two NSF Research Experience for Undergraduates (REU) students who I supervised in Summer 2008, won the first and second prize for their summer REU work at TAMU.

Received the "Outstanding Professor Award" in the of ECE, Texas A&M University, 2007. This award is in "recognition of teaching, research and service excellence".

Our work on the use of coding techniques to mitigate the impact of inductive cross-talk allows a VLSI IC manufacturer to utilize less expensive wire-bond packages for high-speed applications, which was earlier infeasible. **I am told that Agilent Technologies Inc. is using this technique in their ICs.**

"Broadband Impedance Matching for Inductive Interconnect in VLSI Packages". International Conference on Computer Design (ICCD) 2005, October 2-5, San Jose, CA. **Best Paper Award, ICCD 2005.** My co-author on this paper was my student Brock LaMeres.

Undergraduates Eric Menendez and Dumezie Maduike, two NSF Research Experience for Undergraduates (REU) students who I supervised in Summer 2005, won the first prize for their summer REU work at TAMU.

"Performance Model for Inter-chip Busses Considering Bandwidth and Cost", received best paper award at the DesignCon East (2005) conference, Worcester, MA. September 19-21, 2005. My co-authors on this paper were student Brock LaMeres.

"Non-Manhattan Routing using a Manhattan Router", **selected among the top 4 papers, and nominated for best paper award at the VLSI Design conference in January 2005.** My co-authors for this paper were CU ECE student Edward Hursey and my Ph.D. student Nikhil Jayakumar.

"A Fast Ternary CAM Design for IP Networking Applications", candidate for Best Paper Award at the International Conference on Computer Communications and Networks (ICCCN-03), Dallas. October 2003. My co-authors on this paper were CU ECE students Bruce Gamache and Zachary Pfeffer.

California Microelectronics (MICRO) Fellowship, University of California, Berkeley (1993 - 94).

Microelectronics and Computer Development Fellowship, University of Texas, Austin (1987 - 89).

Honor Society Membership: Eta Kappa Nu, Tau Beta Pi, and Mensa.

Graduate Student Researcher funded by SRC and MARCO projects (1994 - 99).

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Scholarship for Excellent Academic Performance, IIT Kanpur (III and V semesters, 1984 and 1986).

Valedictorian and School President, The Scholar High School, Bombay, India (1980).

Grants

Present:

"Edge Reinforcement Learning with Algorithm, Architecture and Circuit Co-Design". Hu, Khatri, Kalathil. This FuSe2 NSF proposal extends from 10/24 through 9/27. The total amount is $1.431M, and my portion of this is $674K.

Past:

"Multi-layer Cybersecurity and Situational Awareness to Enhance Resiliency in Qatar's Power Grid", Abu-Rub et al. This is a Qatar National Research Fund grant. This proposal extends from Jan 2021 to Jan 2025. The total amount is $3,865K, and my part is about $250K.

"RTML:Small:Real-Time Model-Based Bayesian Reinforcement Learning". Hu, Khatri. This proposal extends from Dec 2019 through Dec 2023. The total amount is $500K, my portion is $250K.

"Internet-of-Clothing: Wearable Wireless Energy and Smart Sensors", Ganta, Khatri. TEES Annual Research Conference (TARC) seed grant. The total amount of this grant is $5K, and my part is $2.5K. The duration of this project is from 5/21 to 8/22.

"Entrepreneural Research Fellowship – Flash-based Hardware Security". Khatri. This Air Force Research Laboratory (AFRL) proposal extends from Jan 2020 until October 2020. The total amount is $100K, my portion is $100K.

"Intel-Altera HARP Board Research Donation", Khatri. Selected among competitive proposals to receive a donation of an Intel Heterogenous Architecture Research Platform (HARP) in Summer 2015. Estimated value of this donation is $20k, support duration 3 years.

"Memory Architectures using a Ring-based Topology (MART)", PI Khatri. $10,000 proposal submitted to the Air Force Research Laboratory (AFRL), Rome, NY in August 2017. Period of performance 8/31/17 through 12/31/17. My portion of this is $10,000. Awarded.

"Memory Architectures using a Ring-based Topology (MART)", PI Khatri. $25,800 proposal submitted to the Air Force Research Laboratory (AFRL), Rome, NY in March 2017. Period of performance 6/5/17 through 8/18/17. My portion of this is $25,800. Awarded.

"*PFI-AIR-TT: Wearable Sleepwear for Quantitative Prognostication and Non-invasive Therapy of Obstructive Sleep Apnea",* Bukkapatnam, Khatri, Hanks, Le. Proposal submitted to the NSF, in April 2015. Total amount $200K, over 2 years. Awarded.

"Autonomous System to Measure, Assess and Report Rail Neutral Temperature", Fry, Khatri. Phase II Proposal awarded by Texas A&M Transportation Institute (TTI), September 5, 2014. Period of Performance is 2 years. Total amount $80K, my share of this is $80K. Internal proposal.

"Xilinx Gift Donation for Support of the teaching of Professor Sunil P Khatri", Khatri (PI). A gift of $8,000 was awarded in August 2014, by Xilinx Inc., a Silicon Valley company, for developing

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new teaching techniques using Field Programmable Gate Arrays. Period of performance 8/2014 to 7/2016.

"University Research Supporting Deputy Assistant Secretary of Defense for Nuclear Matters (DASD (NM)). Subtask: Investigating New Types of Radiation Detectors Comprised of Integrated Circuits for Post-Detonation Forensics", Gamache, Khatri, Boyle, Castillo, Yates, Nelson, Gariazzo (PIs). Grant amount $1.81M, my portion is $170K (pending year 3 and 4 approvals). Sponsor is Science Applications International Corporation. Period of performance 5/2012 – 10/2016.

"*Revolutionary Low Power Component Design for Man Portable Radiation Detectors*", Marianno (PI), Khatri, Guise, Braithwaite. Defense Threat Reduction Agency (DTRA) grant awarded in June 2013. Total grant amount is $1,135,700K over 3 years. Awarded. My portion of this grant is about $260K.

"Noise-based Boolean Satisfiability on a GPU Platform", Khatri (PI). Research gift of $25,000 from Multicoreware, Inc. a Silicon Valley startup, for developing GPU based solutions for fast Boolean Satisfiability. Period of performance 1/2012 to 12/2014.

"*Low Power Field Programmable Gate Array with Specialized Serial Input/Output (I/O)*", Khatri (PI). This Maryland Procurement Office grant was submitted in April 2011. Total grant amount is $140K, over a period of 1 year starting May 2011. Awarded.

"*Extreme Low-power Sub-threshold FPGA*", Khatri (PI). Intelligence community postdoc (IC postdoc) proposal submitted in March 2011. The total amount of this proposal is $360K, over a period of 3 years. Awarded.

"GPU based Acceleration of BSIM4 Model Evaluation", Khatri (PI). Research gift of $15,000.00 from Accelicon Technologies, Inc., a Silicon Valley startup for developing GPU based techniques to speed up BSIM4 model evaluations in VLSI circuit simulation. The gift will be offered in two parts, of which the first part ($10,000) has already been sent by the donor. Period of performance 1/2009 to 12/2010.

"A Framework for Developing Novel Detection Systems Focused on Interdicting Shielded HEU", NSF proposal awarded in Fall 2007, award amount is $7.5M. My portion of this is about $300,000. The duration of this grant is September 2007 through August 2012.

"Low Power Field Programmable Gate Array (FPGA)", Single-PI NSA proposal awarded in Fall 2008, award amount is $10,000. The duration of this grant was until Fall 2010.

"High-End Virtex 5 FPGAs for Research Studies", received a high-end Virtex 5 LX110 FPGA board, along with software, from Xilinx Inc. Estimated value of this grant is $5,000. Equipment grant, Fall 2008.

"Research Applications on High-End FPGAs", received a high-end DE3 FPGA board along with software, from Altera Corporation. Estimated value of the grant is $3,000. Equipment grant, Fall 2008.

"*Research and Instructional FPGA Application*". Requested six FPGA hardware boards along with relevant software from Xilinx, Inc. Proposal awarded. PI Khatri. Total amount approximately $2,000. These boards will be used in our research as well as for course projects. The boards are currently being used for two research projects, and have been used by undergraduate students for their capstone projects. Equipment grant, Fall 2007.

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"*ARM Armulator Software Grant*". Requested ARMulator software from ARM, Inc. Proposal awarded. PI Khatri. Total amount approximately $5000. This software is used in our research. Equipment grant, Spring 2006.

"*Hardware Architectures for ATPG using Boolean Satisfiability*", Khatri. Proposal accepted by Intel Corporation, gift amount is $35,000 for a period of 3 years beginning December 2005.

"Functional Sensors", Liang, Khatri, Vinson. Proposal accepted in February 2005, award amount is $700,000 over three years. My portion of this grant is about $225,000. This project ended in Spring 2009.

"Fast Look-up Algorithms on FPGAs and GPUs", Khatri. Proposal accepted in Spring 2007, award amount is $15,000, by Nascentric, a start-up company based in Silicon Valley. The duration of this grant was March 2007 through February 2008.

"NSF REU Proposal", This was submitted by PIs Kundur (ECE) and Butler-Purry (ECE). I had participated as a co-PI. This proposal covered 2 months of my summer salary in two separate years. Total amount of my portion is estimated at $23K.

"*Validation of an Extreme Low Power Design Approach*", Khatri. Proposal funded by Lawrence Livermore National Laboratories, award amount is $70,000 for a period of 2 year beginning April 2006.

"FPGA based Radar Signal Processor for Weather Radar Applications". I received this award (which covered my summer 2006 salary, as well as that of one of my graduate students) to spend 3 months at the National Center for Atmospheric Research (NCAR) in Boulder, CO. In these 3 months, we developed a general purpose, frequency-agile radar signal processing platform for NCAR. I anticipate that this collaboration will yield further research grants from NCAR. Total amount approximately $62K.

"Two-vector based Timing Analysis of Digital Circuits". National Semiconductor Corporation, Santa Clara, CA. August 2000 – May 2001. Research funded through the University of Colorado Foundation, and structured as an unrestricted gift. $50,000 total grant amount.

"Vector-pair based Timing Analysis of Digital Circuits". Semiconductor Research Corporation, Raleigh, NC. August 2001 – December 2001. Total grant amount was $50,000.

"Intelligent Adaptive Signal Processing for Wireless Communication". National Security Agency, February 2003 - February 2004. My portion of this $702,724 award from the NSA was approximately $233,747. This was a joint project with the PI Prof. Roop Mahajan (ME) and Prof. Gregory Grudic (Computer Science).

Service

External Service:

Invited to serve on the Technical Program Committee (TPC) for the International Symposium on Very Large Scale Integration (ISVLSI), 2025. I was invited to serve on the ISVLSI TPC in Spring 2025.

Invited to serve on the Technical Program Committee (TPC) for the International Conference on Computer-Aided Design (ICCAD), 2024. I was invited to serve on the ICCAD TPC in Spring 2024.

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Invited to serve as Affiliate Scientist, National Center for Atmospheric Research (2022-2025). I was invited to serve as an Affiliate Scientist by NCAR (Boulder, CO), a leading weather research laboratory, in September 2022. I will be helping NCAR in the design of the radar down-conversion hardware for an airborne phased-array radar system that they are designing. An application to extend this position for 3 additional years is in progress.

Invited to serve on the Technical Program Committee (TPC) for the International Conference on Computer-Aided Design (ICCAD), 2023. I was invited to serve on the ICCAD TPC in Spring 2023.

Invited to serve on the Technical Program Committee (TPC) for the International Conference on Computer-Aided Design (ICCAD), 2022. I was invited to serve on Track 2.2 (Testing, Validation, Simulation and Verification), in Spring 2022.

Invited to serve as a track co-chair, International Conference on Circuits and Systems (ISCAS) 2022. I was invited to serve on the Digital Signal Processing track (Track 10), in Fall 2021.

Invited to serve as an external referee for a PhD thesis, Anna University. I was requested to serve as a referee in Fall 2021.

Invited to serve as an external referee for a Czech Science Foundation grant. I was requested to serve as a referee in June 2018.

Invited to serve as an external referee for the tenure case of a faculty member at the University of Missouri, Kansas City. I was requested to serve as an external referee in Spring 2018.

Invited to serve as Track Chair for the Logic Track for the International Conference on Computer-Aided Design (ICCAD) 2018. I was invited to serve as Track Chair in Spring 2018. Declined due to health reasons.

Invited to serve as Track Chair for the Logic Track for the International Conference on Computer-Aided Design (ICCAD) 2017. I was invited to serve as Track Chair in Spring 2017. Declined due to health reasons.

Invited to serve as Track Chair for the Logic Track for the Design Automation Conference (DAC) 2017. I was invited to serve in late 2016.

Invited to serve as a panelist for ICCAD 2016, for the panel titled *"Challenges and Opportunities of Stochastic Computing in the Dusk of Moore's Law and the Dawn of Big Data",* Declined due to health reasons.

Invited to serve as Track Chair for the Logic Track for the International Conference on Computer-Aided Design (ICCAD) 2016. I was invited to serve as Track Chair in Spring 2016

Invited to serve on the Technical Program Committee (TPC) for the Design Automation Conference (DAC) 2016. I was invited to serve on the EDA5 track (RTL/Logic Level and FPGA Synthesis, Design and Testing)

Invited to serve as Track Chair for the Logic Track for the International Conference on Computer-Aided Design (ICCAD) 2015. I was invited to serve as Track Chair in Spring 2015

Invited to serve on the Technical Program Committee (TPC) for the Design Automation Conference (DAC) 2015. I was invited to serve on the Logic Synthesis track.

Invited to serve on the Technical Program Committee (TPC) of the 28th International Conference on VLSI Design, Bangalore, India in 2015. I was invited to join the TPC in August 2014.

Invited to serve as Technical Program Committee (TPC) co-Chair, EDA Track, for the 21st IEEE International Conference on Electronic Circuits and Systems (ICECS), 2014. I was invited to serve as co-Chair in July 2014.

Invited to serve on the Technical Program Committee (TPC), Design Automation Conference (DAC) 2014. I served on the EDA6 track "High-level and Logic Synthesis and FPGA".

Invited to serve as Special Sessions Co-Chair for the 57th IEEE Midwest Symposium on Circuits and Systems (MWSCAS) 2014. Also serving on the organizing committee for this conference.

Invited to serve as a Review Committee Member (RCM) for the IEEE International Symposium on Circuits and Systems (ISCAS) 2014.

Invited to serve as Panel Chair for the 2nd IEEE Texas Workshop on Integrated Systems Exploration (TexasWISE), 2014. Also serving on the organizing committee for this workshop.

Invited to serve on the Advisory Committee, for the Hot Topics in Physical Informatics (HotPI) Workshop, 2013.

Invited to serve as Co-Chair for the IEEE International Conference on Electronics, Circuits, and Systems (ICECS) 2013. I served as co-chair for the "VLSI Systems, Applications and Computer Aided Design" track.

Invited to serve as a Panel Chair for the "Models and High-Speed Simulation" session, 15th ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop 2013, Austin, TX. June 2, 2013.

Invited to join the Technical Program Committee (TPC), The 1st Workshop on Modeling of Biological Systems (MoBS) 2013, Austin, TX. June 2013.

Invited to serve on the ACM Transactions on Design Automation of Electronic Systems (TODAES) best paper committee, March 2013.

Invited to serve as Poster Chair for the 1st IEEE Texas Workshop on Integrated System Exploration (TexasWISE) 2013, Winedale, TX. March 2013. Also served on the organizing committee for this workshop.

Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES). Invited to serve in this capacity in February 2012. I will cover papers in the area of Logic, RTL and behavioral synthesis for a 3-year term.

Lead Guest Editor, VLSI Design. Invited in 2012 to serve as a lead Guest Editor for a Special Issue of VLSI Design.

Invited to join the Editorial Board, MDPI Journal of Electronics, May 2011.

Associate Editor, IEEE Transactions on Computers. I served in this position from 2010 to 2011.

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Chair, ACM/SIGDA Logic/RTL Synthesis Technical Committee. I was invited to serve on this committee, from June 2009-2010.

Area Editor (Electronics Design) for the book "GPU Computing Gems". I was invited to serve as Area Editor in 2009.

Member, Technical Program Committee, IEEE International Workshop on Logic Synthesis (IWLS) 2005-07, 2010. Invited to join this committee in 2004.

Member, Technical Program Committee, Design Automation and Test in Europe (DATE) conference, 2010. I was invited to join the DATE TPC for Track D13 (Logic and Technology Dependent Synthesis for Deep-Submicron Circuits).

Member, selection committee for "ACM Best Ph.D. Dissertation Award in EDA for 2009", starting February 2010.

Track Chair for Logic Synthesis track, IEEE International Conference on Computer-Aided Design (ICCAD) 2009-10. I was invited to chair the Logic Synthesis track in Spring 2009.

General Chair, IEEE International Workshop on Logic Synthesis (IWLS-09).

Member, Technical Program Committee, International Symposium on Quality Electronic Devices (ISQED) 2009, 2010.

Publicity Co-chair, ACM/IEEE Great Lakes Symposium on VLSI (GLS-VLSI), 2009. Invited to serve as Publicity Co-chair in 2008.

Panel Chair, International Test Synthesis Workshop (ITSW), 2009. Invited to serve on the ITSW committee in 2008.

Technical Program Committee Chair, IEEE International Workshop on Logic Synthesis (IWLS-08). I was invited to join this committee in 2007.

Track Co-chair, IEEE International Symposium on Circuits and Systems (ISCAS) 2008-10. I was invited to co-chair the "Computer Aided Network DEsign" (CANDE) track of ISCAS in 2007.

Member, Technical Program Committee, IEEE International Conference on Computer-Aided Design (ICCAD) 2007, 2008, 2009. I was invited to join this committee in 2007.

Member, Technical Program Committee, DesignCon, 2007-2009.

Member, Technical Program Committee, IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2008-10. I was invited to join this committee in late 2007.

Review Committee Member (RCM), IEEE International Symposium on Circuits and Systems (ISCAS) 2007. I was invited to serve as an RCM for the "Computer Aided Network DEsign" (CANDE) track.

Track Co-chair, IEEE International Conference on Computer Design (ICCD-07). I was invited to co-chair the "Test and Methodologies" Track of ICCD in 2007.

Technical Program Committee Member, IEEE International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2004-06. Invited to join this committee in

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2003.

Member, Technical Program Committee, IEEE International Conference on Computer Communications and Networks (ICCCN-04). Invited to join this committee in 2003.

Invited to serve as Session Chair for several conferences including the International Conference on Computer Aided Design (ICCAD 2008), Great Lakes Symposium on VLSI (GLSVLSI) 2008, International Test Synthesis Workshop (ITSW) 2007, the International Symposium on Circuits and Systems (ISCAS 2006, 2007), the Asia-South Pacific Design Automation Conference (ASP-DAC 2006), the Design Automation Conference (DAC) 2005, the International Conference on Networking (ICON-03), and the Design Automation Conference (2005).

Reviewed a large number of technical papers for numerous technical journals and conferences (1993-2004). Reviews include IEE Transactions (Computers and Digital Techniques), IEEE Transactions on VLSI, IEEE Transactions on CAD of ICs and Systems, Electronic Letters, IEEE Journal of Solid-State Circuits, International Conference on VLSI Design, Design Automation Conference (DAC), International Symposium on Low-Power Electronic Design (ISLPED), Great-Lakes Symposium on VLSI (GLS-VLSI), International Conference on Computer-Aided Design (ICCAD), International Conference on Computer Design (ICCD), International Symposium on Circuits and Systems (ISCAS), European Design Automation Conference (Euro-DAC-96), and International Test Conference (ITC).

University and ECE Departmental Service:

Serving on the ECE Hiring Committee, Department of ECE, TAMU. My term on this committee is expected to be from 2024-25.

Serving on the CPEN ETAM Committee, Department of ECE, TAMU. My term on this committee is expected to be from 2024-25.

Serving on the ECE Former Students and External Relations Committee, Department of ECE, TAMU. My term on this committee is expected to be from 2024-25.

Serving on the Faculty Advisory Committee (FAC), Department of ECE, TAMU. My term on this committee is expected to be from 2022-24.

Serving on the Awards Committee, Department of ECE, TAMU. My term on this committee is expected to be from 2022-24.

Serving on the Internal Transfer Committee, Department of ECE, TAMU-Qatar. My term on this committee began in 2023.

Serving on the Computer Engineering Hiring Committee, Department of ECE, TAMU-Qatar. My term on this committee began in 2023.

Serving on the Graduate Students Committee (GSC), Department of ECE, TAMU. My term on this committee is expected to be from 2021-22.

Invited to join the University-level "Identity, Data, and Access Committee (IDAC)", in 2021

Invited to join the University-level "Online PhD" committee, 2021.

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Served on the Peer Mentoring Committee, Department of ECE, TAMU. I served on this committee from late 2020 through summer 2021, and helped offload peer mentoring tasks to the Academic Success Center at TAMU.

Invited to join the College of Engineering Tenure and Promotion Advisory Council (CETPAC), 2020-21

Invited to take charge of the ECE Department Peer Tutor Program, Fall 2020.

Texas A&M University, College Station (Summer 2020). I redesigned all the labs for ECEN 248 (Digital Systems Design) and ECEN 449/749 (Microprocessor Systems Design) to be completely conducted without the need of a laboratory, in response to the pandemic. These modified labs can be used to create a distance ECE degree program, if need be.

Nominated to serve as Chair of the ECE Department Tenure and Promotion Commiteee, 2020.

Serving on the Tenure and Promotion committee, ECE department, TAMU (2019-20)

Served on the Graduate Studies Appeals committee, ECE department, TAMU (2019)

Serving on hiring committee for Faculty search, ECE department, TAMU-Qatar. I served on the search committee for the Assistant Professor level faculty search in our sister department, 2019.

Served on hiring committee for Faculty search, ECE department, TAMU-Qatar. I served on the search committee for instructional faculty in our sister department, 2018.

Serving on the ECE Hiring Committee (Jan 2018 – Dec 2018). I have been participating by reviewing faculty applications, meeting faculty candidates, and helping decide on hiring decisions for tenure-track as well as professional faculty

Serving on the Computer Engineering Curriculum Committee (CECC), Fall 2017 – Fall 2018.

Invited to serve on the College-level "High Performance Computing" (HPC) search committee. I was invited to serve on this committee by Dr. Georghiades in Spring 2015

Helped the ECE undergraduate recruiting efforts by presenting a talk on the benefits of an ECE degree, to about 100 freshman students who were considering ECE during their entry to major.

Helping undergraduate recruiting by helping conduct a laboratory session in the revamped "ECE Summer Enrichment Workshops" week in July, 2014. In this laboratory, students will learn about ECE by developing a solar car.

On the request of the ECE Department Head, I am initiating a "ECE Pizza Friday" in Spring 2014, in which students will attend a monthly evening meeting hosted by the ECE Department, to showcase the career opportunities that an ECE graduate enjoys. This will be continued in Fall 2014, when all incoming undergraduates will join TAMU with no declared major.

Serving on the TAMU College of Engineering "Emerging Technologies Advisory Council", (ELTAC), since 2014.

Presentation at Aggieland Saturday (2014). I attended a faculty panel session in which prospective students and their parents asked questions about the TAMU ECE Department.

New Course Development (Spring 2014). I have been working on developing a new undergraduate course. In this course, students will design, synthesize, simulate, place, route, and tape out a digital Integrated Circuit (IC). The course will be a senior elective course.

Course Laboratory Redesign (Spring-Summer 2014). I am working on converting the laboratory exercises of two courses, ECEN 248 (Digital Systems Design) and ECEN 449 (Microprocessor Systems Design) to a mobile laboratory station environment, using mobile test equipment from National Instruments.

New Course Development (Spring 2014). I have obtained permission from the Department Head of the ECE Department to initiate a course (a pass/fail, 1 credit course for sophomores or seniors) in which I will discuss career issues. The course will cover life lessons that are important for a healthy career, including life-long learning, networking, people skills, career choices and self-improvement. The lectures will be augmented by visits from industry leaders who will be able to share their career lessons with the students. This course is under development, and will be submitted for approval in Spring 2014.

Represented the ECE Department in the College of Engineering initiative to foster closer research ties with the ECE Department at the Indian Institute of Technology, Kanpur, India. Visited IIT Kanpur in 2013 to help identify possible areas of research synergy.

Serving on the ECE Distinguished Speaker Committee, as a representative of the CE group, starting Spring 2013.

Serving on the Computer Engineering Curriculum Committee as the representative of the CE group, starting 2013.

Helped migrate the ECEN 248 laboratory from a Windows platform to a Linux platform (Summer 2011).

Served as the College of Engineering representative for the Friends of India Network (FIN) (2010 - 11).

Served as the representative for ECE in the college level IT committee, to help reduce costs by shared services (2010 - present).

TAMU ECE Scholarship Committee Member, starting February 2010.

Serving as a Faculty Mentor under TAMU's Network Mentoring Program (NMP) (2009 – present).

Serving on the ECE Undergraduate Studies Committee as the representative of the CE group, starting 2009.

ECE Unix Committee (2008-2014). Along with two other faculty, I am helping provide recommendations for the upgrade and maintenance of the ECE Unix computing infrastructure. I am serving as the chair of this committee since 2009.

Presentation at Discover ECE day (2008-09). Presented a talk to prospective TAMU Engineering students and their parents. The talk titled "What does a Computer Engineer do?" covers courses, research and job prospects in the Computer Engineering area after a B.S. degree in CE from TAMU.

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Texas A&M University, assisting in ABET Certification (Spring 2008, Spring 2009, Spring 2013, Spring 2014). Provided data and analysis results for the ECEN 449 course, for ABET certification purposes. Will be providing similar data for Spring 2009.

Redesigned Laboratories for ECEN 248 (Summer 2008). Along with Dr. Choi, I helped to substantially redesign the laboratories for ECEN 248 (Introduction to Digital Systems Design), and make them more current and technically relevant.

Texas A&M University, Qatar. Visited our ECE Department at TAMU-Q during January 2008, to demonstrate the laboratory exercises that we had developed for ECEN 449, to the faculty and laboratory coordinators at TAMU-Q.

Texas A&M University, designed and developed the website for the Computer Engineering group, 2007. Along with my colleague Dr. Alex Sprintson, we developed a new website for the CE group (http://cegroup.ece.tamu.edu).

Course Redesign, ECEN 449 (Summer 2007). Along with Dr. Reddy, I helped to redesign the laboratories and lectures for ECEN 449 (Microprocessor Systems Design).

Presentation at Aggieland Saturday (2007-09). Presented a 15-minute talk to prospective TAMU Engineering students and their parents. The talk covered courses, research and job prospects in the Computer Engineering area after a B.S. degree in CE from TAMU.

Graduate Admissions, Computer Engineering group (2006-2009). Along with a colleague, I help screen graduate applicants for the Computer Engineering group, and make admissions decisions.

Member, ECE Distinguished Visitor Committee (Fall 2005). I served on this committee from Fall 2005 through Fall 2006.

Texas A&M University, ECE faculty interviews, 2004-12. I have made special efforts to attend all ECE faculty hiring candidate seminars, and spend time with ECE faculty candidates. I have provided my feedback to the ECE Department Head, to help ensure that we hire the best faculty.

Texas A&M University, participated in ABET Certification for the Computer Engineering program, 2004-05. The certification process went through flawlessly. My course was used by the ABET personnel to interview the students.

Was invited to be a panelist on a panel discussion on "How to Search for an Academic Job", Texas A&M University, Fall 2004.

Informal advising of undergraduates. Some of my undergraduate and graduate students frequently solicit my input on their courses, career choices and technology trends.

Encouraging undergraduates in ELEN 248, ELEN 449 and ELEN 454 to consider pursuing graduate school. Most of them enjoy this discussion very much, since they were not familiar with the option of continuing studies in graduate school.

Advised TAMU EE undergraduates Rob Hammond and Anshul Gupta, under the URA program (2004-05).

Member, Dissertation and Thesis Committee for several Texas A&M students. The students include Hari Sankar (EE, Ph.D.), Ekpe Orafur (EE, Ph.D.), Taekwon Jee (ME, M.S.), Seraj Ahmad (CS, M.S.), Nitin Nangre (ECE, Ph.D.), Kiran Gunnam (ECE, Ph.D.), Ganesh Venkataraman (EE, Ph.D.), Rohit Singhal (EE, Ph.D.), Rupak Samanta (CS, Ph.D.), Maja Knezev (EE, Ph.D.), Zarko

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Djekic (EE, Ph.D.), Tae Kim (CS, Ph.D.), Meng Shi (EE, M.S.), Jing Sun (EE, M.S.) and John Kocurek (EE, M.S.).

University of Colorado, ECE VLSI Group Ph.D. Preliminary Exam Committee. Since I joined CU, I had been on the VLSI Group Ph.D. Preliminary Exam Committee. I had been involved in conducting about 15 preliminary exams to date. I chaired this committee in 2003, and in 2004 as well.

Member, Graduate Admissions Committee, Department of ECE, CU Boulder (2000 – 2002). Reviewed files and recommended graduate students for admissions. Proposed methods to improve the quality of admitted ECE graduate students. Visited top international schools to encourage high-quality graduate students to apply to the ECE department. Pointed out that we were emphasizing undergraduate GPA too heavily in our graduate admissions process, which is error-prone since the undergraduate GPA is estimated in many cases. Recommended and helped implement methods to advertise ECE more aggressively, to ensure that we get quality applicants.

Book review of "Cross-talk Avoidance Techniques in VLSI", Kluwer Academic Publishers, 2002.

University of Colorado, ECE faculty hiring (2000 – 2002). Provided detailed feedback on all faculty candidates to the Hiring Committee to support the effort of hiring quality faculty. I have met with and attended the seminars of most of the ECE faculty candidates since my arrival at CU.

University of Colorado, ECE Technical Reports (2000 – 2001) When I joined the ECE department, there was no mechanism for faculty to create Technical Reports for their research work. I recommended this to our Chair, and worked with the ECE staff to bootstrap this effort.

University of Colorado, participated in ABET Certification for the ECE Department by providing statistical information about exams and homework from the ECEN 4703 course.

Book review of "Introduction to VLSI Circuits and Systems" by John Uyemura (John Wiley and Sons Publishers), 2001.

Contributed to the release of VIS, a formal verification tool that is developed and distributed by the VLSI group under the direction of Prof Fabio Somenzi. VIS-1.4 was released in Summer 2001 and VIS-2.0 was released in Fall 2002. I have worked on code review, bug fixes and several low-level tasks related to the release.

Member, Dissertation and Thesis Committee for the following CU students: Chao Wang (ECE, Ph.D.), HoonSang Jin (ECE, Ph.D.), Bing Li (ECE, Ph.D.), Adrian Michalicek (ME Ph.D.), Sandeep Dhar (ECE Ph.D.), Yin Yan (ECE Ph.D.), Se-Ho You (ECE Ph.D.), Garrett Holthaus (ECE, M.S.), In-Ho Moon (ECE Ph.D.), Benjamin Patella (ECE M.S.), Balakrishna Kumthekar (ECE Ph.D.), Stephen Gallant (ECE M.S.), Nwanua Elumeze (ECE M.S.), Subramoni Parameswaran (ECE M.S.), Jay Plucienkowski (ECE M.S.), Matthew Lovell (ECE M.S.).

Computing infrastructure of the CU VLSI CAD group: Along with Prof. Fabio Somenzi, I had worked on upgrading the hardware and software infrastructure of the VLSI research laboratory. I had been instrumental in obtaining educational licenses for Rational Software products, which are critically important for us to be able to develop quality software releases from the VLSI group.

Technical Advisor, Accelicon, Inc. (2009-10). Invited to join the Technical Advisory Board of Accelicon, a Silicon Valley company specializing in SPICE model card extraction for circuit simulation. My role was to advise the company in areas relating to the use of GPUs to accelerate their products.

Technical Advisor, Nascentric, Inc. (2008-09). Invited to join the Technical Advisory Board of Nascentric, a company specializing in fast circuit simulation. My role was to advise the company in areas relating to the use of GPUs to accelerate their products.

Technical Advisor, InMage Systems, Inc., Milpitas, CA (2002-06). Invited to join the Technical Advisory Board of SV Systems, a Storage-area Networking (SAN) start-up company specializing in data recovery. My role was to advise the company in areas relating to VLSI design and implementation of relevant ICs.

Faculty Advisor, ITU Ventures, Beverly Hills, CA (2002-04). My role was to advise the ITU personnel about the viability of business proposals in the areas of VLSI Design and CAD.

Technical Advisor, Jasmine Networks, Inc., Santa Clara, CA (2000-01). Invited to join the Technical Advisory Board of Jasmine Networks, an optical networking startup company. My involvement included advice on VLSI issues, including system-level high-speed I/O issues, cross-talk immune bus design, and advice on VLSI design and fabrication.

Recommended to the ECE Department Chair at the University of Colorado, to conduct an **"Industrial Visitor Day", w**here we would showcase our ECE research and network with the members of the local industry to share our results, and also possibly develop research collaborations with industry. This was implemented in April 2000.

Responsible for responding to user queries about SIS (1993-99). SIS (Sequential Interactive System) is a logic synthesis and optimization system developed at the CAD group at the University of California, Berkeley.

Conducted the Computer-Aided Design Seminar at UC Berkeley (1997-98). Tasks involved inviting and hosting international guests at the seminars, and coordinating the seminars.

Reviewed grant proposals for California MICRO grants (1997).

Involved in industrial consulting with Silicon Valley companies (1994-95). Consultant for SUN microsystems' CAD group as well as their UltraSPARC group in the area of CAD algorithms and issues. Conducted a week-long series of lectures on state-of-the-art CAD algorithms. The focus was SIS, a logic synthesis and optimization tool developed at UC Berkeley. The audience was a group of practicing engineers from the corporate CAD group and the UltraSPARC microprocessor design groups.

Additional

Professional Society Membership: Institution of Electrical and Electronic Engineers (IEEE), Association of Computing Machinery (ACM), American Association for the Advancement of Science (AAAS).

Volunteer, Boulder Shelter for the Homeless. Once each month, a small group of us sponsor dinner for the homeless who visit the shelter.

Student Counselor for the Counseling Service, I.I.T., Kanpur, India (1984-1987).

Naturalized Citizen of the United States of America.

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References

Available upon request.