UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

Vervain, LLC, Plaintiff, v. Phison Electronics Corporation, Defendant.	Civil Action No. 1:24-cv-259-ADA JURY TRIAL DEMANDED

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Vervain, LLC ("Vervain") asserts the following claims for patent infringement against Defendant Phison Electronics Corporation ("Phison" or "Defendant"), and alleges as follows.

NATURE OF THE ACTION

1. This is a civil action for infringement under the patent laws of the United States of America, 35 U.S.C. § 1 *et seq.*

2. Vervain is the owner of all rights, title, and interest in U.S. Patent Nos. 8,891,298; 9,196,385; 9,997,240; 10,950,300; 11,830,546; 11,854,612; 11,967,369; and 11,967,370 (collectively, the "Asserted Patents").

3. Defendant has infringed and continue to infringe one or more claims of Vervain's Asserted Patents by making, using, offering to sell, and selling within the United States, and importing into the United States, including in this District, certain flash memory products. Vervain seeks injunctive relief and monetary damages.

THE PARTIES

4. Plaintiff Vervain is a Texas limited liability company with its principal place of business located at 7424 Mason Dells Drive, Dallas, Texas 75230.

5. On information and belief, Defendant Phison Electronics Corporation. ("Phison") is a corporation organized and existing under the laws of Taiwan with its principal place of business located at No. 1, Qun Yi Rd., Jhunan, Miaoli, 350 Taiwan. Phison is a market leader in NAND flash storage products and controllers sold and distributed in the United States and the world, generally. Phison conducts business in Texas and, particularly, the Western District of Texas, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, or others).

6. According to Phison's website, "Phison Electronics Corporation was established in November 2000 in Hsinchu, Taiwan. Starting with the world's first single-chip USB flash drive IC, Phison is now a market leader in NAND Flash controllers and applications including USB, SD, eMMC, PATA, SATA, PCIe and UFS. The company has shipped over 600 million controllers worldwide yearly and topped over US 2.2 billion dollars in sales revenue (2021). As a NAND flash total solution provider, Phison also offers system and OEM/ODM services for major brand names."[1]

7. Phison now has over 2600 employees.[2] This includes employees at Phison's R&D center in the United States.

8. 70-80% of Phison's business "comes from private-label NAND flash products through partnerships with OEMs like Kingston."[3] Phison makes numerous flash shortage

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[1] Ex. G, (https://www.phison.com/en/company/about-us)
[2] *Id*.
[3] Ex. H, (https://gestaltit.com/exclusive/zach/phison-electronics-is-everywhere-in-nand-flash-storage-and-more/).

products—including controllers, complete SSDs, embedded flash, and other products, that are sold in the United States. Phison's controllers are used in all kinds of flash memory products sold by other companies, including in the United States.

9. As Phison's Director of Product Architecture Imran Hirani has explained, the use of QLC (quad-level-cell) flash memory, a type of multi-level-cell ("MLC") flash memory, in combination with SLC (single-level-cell) memory is a key part of providing high capacity, high speed, and high endurance. "QLC NAND addresses the increased capacity requirement but comes with tradeoffs of slower throughput and lower endurance. One way to address slower throughput and lower endurance of QLC is to add a small SLC cache on the drive. Data from the host is written to the SLC cache first, and then data is moved to QLC."[4]

10. Phison has employees in the Western District of Texas. For example, Mr. Hirani, Phison's Director of Product Architecture who wrote about Phison's use of QLC and SLC flash, resides in Cedar Park, Texas.[5]

11. Kingston and Phison work jointly on controller design, including in this district. Phison and Kingston have a "partnership" to make SSD controllers for Kingston products, and this partnership even "extends beyond SSDs." In November 2010, Phison and Kingston formed a joint venture to provide flash memory solutions in the mobile, Internet of Things, and embedded markets.[6]

12. Kingston and Phison, which act together in product design, marketing, manufacturing, and sales, have operated as agents of and for one another and have otherwise

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[4] Ex. I, (https://phisonblog.com/qlc-nand-for-consumer-ssds-2/)
[5] Ex. J, (Imran Hirani LinkedIn profile, https://www.linkedin.com/in/imran-hirani-721aa23/).
[6] Ex. K, https://www.phison.com/en/company/newsroom/press-releases/general/530-phison-and-kingston-collaborate-on-nvme-ssd-controller-to-accelerate-into-the-next-ssd-era-2

acted vicariously for each other as elements of the same business group and/or enterprise. They work together in concern and in orchestrated fashion, subject to agreements closer than arms' length, in order to implement a distribution channel of infringing products in the United States.

JURISDICTION AND VENUE

13. This is a civil action for patent infringement arising under the patent laws of the United States, 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction over the matters asserted in this Complaint under 28 U.S.C. §§ 1331 and 1338(a) and 35 U.S.C. §§ 271 *et seq*.

14. This Court has personal jurisdiction over Phison in accordance with the Due Process Clause of the United States Constitution and the Texas Long Arm Statute (*see* Tex. Civ. Prac. & Rem. Code §§17.041 *et seq*.) because, among other things, (i) Phison has done and continues to do business in Texas, (ii) Phison "recruits Texas residents, directly or through an intermediary located in this state, for employment inside or outside this state," Tex. Civ. Prac. & Rem. Code § 17.042(3), and (iii) Phison has committed and continues to commit, directly or through intermediaries (including subsidiaries, distributors, affiliates, retailers, suppliers, integrators, customers, and others), acts of patent infringement in this State and this District. Such acts of infringement include making, using, offering to sell, selling, and/or importing Accused Products in this State and this District, as well as acts of induced and contributory infringement. Phison places its Accused Products into the stream of commerce through established distribution channels with the expectation and intent that such products will be sold to and purchased by consumers in the United States, this State, and this District; and with the knowledge and expectation that such products (whether in standalone form or as integrated in downstream products) will be imported into the United States, this State, and this District.

15. Phison is engaged in making, using, selling, offering for sale, and/or importing products, such as SSD controllers, SSDs, and embedded flash, used in PCs and other electronic

devices, to and throughout the United States, including this District. Phison induces its subsidiaries, distributors, affiliates, retailers, suppliers, integrators, and customers in the making, using, selling, offering for sale, and/or importing such products to and throughout the United States, including this District. Phison and its subsidiaries act together and have operated as agents of and for one another and have otherwise acted vicariously for Phison as elements of the same business group and/or enterprise. They work in concert, under agreements far nearer than arm's length, in order to implement a distribution channel of infringing products within this District and the United States.

16. Phison maintains a corporate presence in the United States via at least its U.S.-based affiliate Phison Technology, Inc. (USA) ("Phison – USA").[7]

17. On information and belief, Phison – USA is a corporation organized under the laws of the State of California, with a place of business at 2526 Qume Drive, Unit 28, San Jose, CA 95131, and is a wholly-owned subsidiary of Phison.

18. Phison – USA is registered to conduct business in the State of Texas, including this District, with a registered agent address of 815 Brazos St., Suite 500, Austin, TX 78701-2509.[8]

19. Alone and through at least the activities of its U.S.-based affiliates (e.g., Phison – USA), Phison conducts business in the United States and this District, including importing, distributing, and selling flash memory products and controllers that are incorporated into third-party flash memory products that infringe the Asserted Patents. Through this conduct, Phison conducts extensive business in the United States, this State, and this District.

[7] Ex. G, (https://www.phison.com/en/company/about-us.)
[8] Ex. L, (Phison Texas Secretary of State Registration).

20. On information and belief, Phison provides Accused Products to be used as part of end products sold, used, and imported in the United States and this District. On information and belief, Phison encourages and instructs users in this district of Phison's Accused Products to configure and operate them in an infringing matter.

21. Phison has therefore purposefully availed itself of the privileges of conducting business in the United States and this District and subjected itself to this Court's personal jurisdiction. Phison has sufficient contacts with this forum through its transaction of substantial business in this State and through its commission of acts of patent infringement as alleged in this Complaint that are purposefully directed toward this State and District.

22. In the alternative, the Court has personal jurisdiction over Phison under Federal Rule of Civil Procedure 4(k)(2).

23. Venue is proper in this District pursuant to 28 U.S.C. § 1391 because Phison is not a resident of the United States, and thus may be sued in any judicial district in the United States under 28 U.S.C. § 1391(c)(3). Alternatively, venue is proper in this District under 28 U.S.C. §§ 1391 and 1400(b) because a substantial part of the events or omissions giving rise to the claims occurred in this District, and because Defendant has committed acts of infringement in this District and have a regular and established place of business in this District.

VERVAIN'S ASSERTED PATENTS

24. U.S. Patent No. 8,891,298 (the "'298 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 18, 2014. A true and correct copy of the '298 patent is attached as Exhibit A to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '298 patent, with the full and exclusive right to bring suit to enforce the '298 patent, including the right to recover for past infringement. The '298 patent is valid and enforceable under United States patent laws.

25. U.S. Patent No. 9,196,385 (the "'385 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 24, 2015. A true and correct copy of the '385 patent is attached as Exhibit B to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '385 patent, with the full and exclusive right to bring suit to enforce the '385 patent, including the right to recover for past infringement. The '385 patent is valid and enforceable under United States patent laws.

26. U.S. Patent No. 9,997,240 (the "'240 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on June 12, 2018. A true and correct copy of the '240 patent is attached as Exhibit C to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '240 patent, with the full and exclusive right to bring suit to enforce the '240 patent, including the right to recover for past infringement. The '240 patent is valid and enforceable under United States patent laws.

27. U.S. Patent No. 10,950,300 (the "'300 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on March 16, 2021. A true and correct copy of the '300 patent is attached as Exhibit D to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '300 patent, with the full and exclusive right to bring suit to enforce the '300 patent, including the right to recover for past infringement. The '300 patent is valid and enforceable under United States patent laws.

28. U.S. Patent No. 11,830,546 (the "'546 patent") is entitled "Lifetime Mixed Level Non-Volatile Memory System" and issued on November 28, 2023. A true and correct copy of the '546 patent is attached as Exhibit E to this Complaint. Vervain is the owner of all rights, title, and interest in and to the '546 patent, with the full and exclusive right to bring suit to

enforce the ’546 patent, including the right to recover for past infringement. The ’546 patent is valid and enforceable under United States patent laws.

29. U.S. Patent No. 11,854,612 (the “’612 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on December 26, 2023. A true and correct copy of the ’612 patent is attached as Exhibit F to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’612 patent, with the full and exclusive right to bring suit to enforce the ’612 patent, including the right to recover for past infringement. The ’612 patent is valid and enforceable under United States patent laws.

30. U.S. Patent No. 11,967,369 (the “’369 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on April 23, 2024. A true and correct copy of the ’369 patent is attached as Exhibit KK to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’369 patent, with the full and exclusive right to bring suit to enforce the ’369 patent, including the right to recover for past infringement. The ’369 patent is valid and enforceable under United States patent laws.

31. U.S. Patent No. 11,967,370 (the “’370 patent”) is entitled “Lifetime Mixed Level Non-Volatile Memory System” and issued on April 23, 2024. A true and correct copy of the ’370 patent is attached as Exhibit LL to this Complaint. Vervain is the owner of all rights, title, and interest in and to the ’370 patent, with the full and exclusive right to bring suit to enforce the ’370 patent, including the right to recover for past infringement. The ’370 patent is valid and enforceable under United States patent laws.

32. In addition, Vervain has pending continuations to the patents-in-suit. Vervain is the owner of all rights, title, and interest in and to these patent applications.

33. G.R. Mohan Rao is the sole inventor of the Asserted Patents.

34. Dr. Rao is the inventor of approximately 113 U.S. patents and the author of at least 15 technical publications spanning several decades.

35. Dr. Rao has been an innovator in the semiconductor industry since the 1960s. After receiving his Ph.D. in physics with a specialization in electronics in September 1968 from Andhra University in Waltair, India, near the village where he grew up, Dr. Rao traveled to the United States to attend a graduate program in physics at the University of Cincinnati, fulfilling his lifelong dream to study in the United States.

36. Shortly after beginning his studies at the University of Cincinnati, Dr. Rao found a bulletin indicating that Prof. William Carr of Southern Methodist University (SMU) was looking for a graduate assistant for his work on MOS transistors. Dr. Rao called Prof. Carr about the opportunity, and by December 1968, after completing the fall semester at the University of Cincinnati, Dr. Rao had received the assistantship with Prof. Carr, moved to Dallas, Texas, and enrolled in a Ph.D. program at SMU in electrical engineering.

37. At the laboratory at SMU, Dr. Rao was able to build MOS devices from scratch. In the 1969-1970 timespan, while attending SMU, Dr. Rao also worked in the SMU laboratory with Jack Kilby of Texas Instruments, a pioneering electrical engineer who would later receive a Nobel Prize for his work. In early 1972, Mr. Kilby set up an interview for Dr. Rao at Texas Instruments' Houston facility, then the home of Texas Instruments' MOS-related work.

38. Dr. Rao began working for Texas Instruments in June 1972. He would go on to work for the company for 22 years, until 1994. Dr. Rao rose through the ranks at Texas Instruments, starting in an Engineer position and ascending to the position of Senior Fellow—one of 12 out of approximately 20,000 engineers at the company at the time. He then moved into

a management position, starting as a Vice President in 1983 and becoming a Senior Vice President in 1985.

39. Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. From the late 1970s through the mid-1980s, he worked on and/or managed Texas Instruments': (1) 64Kb RAM, in a project management capacity as a Senior Member of Technical Staff; (2) 256Kb RAM, in a project management capacity as a Fellow; (3) 1Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects; and (4) 4Mb RAM, in a management capacity as a Senior Fellow, overseeing several projects. At Texas Instruments, Dr. Rao also worked on projects involving EEPROM, SRAM, and microcontrollers. In total, Dr. Rao received approximately 35 U.S. patents during his time at Texas Instruments.

40. Some of Dr. Rao's work for Texas Instruments is featured in the Smithsonian Institution, in the Texas Instruments Collection.[9] For example, the Smithsonian Institution has a display of Texas Instruments' experimental 1-megabit CMOS DRAM with one-micron feature size, produced in April 1985 under Dr. Rao's leadership.

41. After his time at Texas Instruments, Dr. Rao joined Cirrus Logic in 1994. Although Cirrus Logic was a California company, Dr. Rao coordinated a team in the Dallas area. His work focused on a major project involving integration of a graphics controller and memory. During his time at Cirrus Logic, Dr. Rao received approximately 22 U.S. patents relating to his work on integrated graphics controllers and memory. Dr. Rao left Cirrus Logic in the summer of 1996.

[9] http://smithsonianchips.si.edu/texas/t_360.htm (last visited Apr. 12, 2021); http://smithsonianchips.si.edu/texas/wafer.htm (last visited Apr. 12, 2021).

42. Later in 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip.

43. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years. For example, Dr. Rao worked to improve non-volatile memories that are used for long term storage of data after the power is turned off, and how to reduce the power consumption of those devices.

44. In non-volatile memories, there are two types of storage cells: single-level cells (SLCs) that store one bit of information, and multi-level cells (MLCs) that store multiple bits of information. SLCs are faster, more reliable, and have a longer life. MLCs are less expensive and can store more data in less space with less power consumption. While working to improve these non-volatile memories, Dr. Rao developed inventions that combine the long life and high-performance of SLCs with the more cost-effective MLCs. The result is the best of both types of cells – longer life and better performance at less cost. By using the MLCs as the default storage, the cheaper, more reliable MLCs are used for the bulk of the data storage. Meanwhile, the SLCs are used for the data that needs it the most.

45. The claims of the Asserted Patents are directed to patent-eligible, non-abstract ideas. They address, among other things, specific improvements for controlling non-volatile memory modules. The claims are particularly useful for flash memory products or other memory devices that use a combination of SLCs and multi-level cells MLCs. If, for example, a range of addresses in a MLC memory module fails a data integrity test, the range of addresses may be mapped to a new range of addresses in a SLC memory module. Also, if a block in the

MLC module is used frequently, the block may be transferred to the SLC module. By doing so, the reliability and life of the flash memory is increased.

46. Vervain's Asserted Patents claim, among other things, a specific implementation of a solution to a problem in the design and fabrication of flash memories. For example, the patents identify numerous specific advantages that Vervain's claimed techniques provide compared to traditional forms of flash memories. *See, e.g.*, Ex. A, '298 patent at 1:25-32; Ex. B, '385 patent at 1:28-35; Ex. C, '240 patent at 1:40-47; Ex. D, '300 patent at 1:44-51; Ex. E, '546 patent at 1:35-42, Ex. F, '612 patent at 1:41-48. Further, the claimed technologies cannot be performed as mental steps by a human, nor do they represent the application of a generic computer to any well-known method of organizing human behavior.

47. The Asserted Patents claim inventive concepts that are significantly more than any patent-ineligible, abstract idea. In particular, the claimed technologies, including individual limitations as well as ordered combinations of limitations, were not well-understood, routine, or conventional, and cover multiple advantages, and combinations of advantages, that were not well-understood, routine, or conventional. *See, e.g.*, Ex. A, '298 patent at 5:24-40, 6:24-35; Ex. B, '385 patent at 5:28-44, 6:28-39; Ex. C, '240 patent at 5:43-59, 6:46-58; Ex. D, '300 patent at 5:51-67, 6:53-65; Ex. E, '546 patent at 5:41-57, 6:44-56, Ex. F, '612 patent at 5:54-6:3, 6:58-7:3.

48. On July 18, 2022, Phison was served with subpoenas from Vervain in the *Vervain, LLC v. Micron Tech., Inc.* case, No. 6:21-cv-487-ADA (W.D. Tex.), and the *Vervain, LLC v. Western Digital Corp.* case, No. 6:21-cv-48-ADA (W.D. Tex.). Exs. O-R. The *Micron* case asserted Vervain's patents against a variety of Micron flash storage products, including flash storage products using Phison controllers. With the service of that subpoena, Phison was aware of Vervain's patent portfolio and of its infringement of Vervain's patents.

PHISON'S INFRINGING PRODUCTS AND ACTIVITIES

49. Phison is a is a global manufacturer and supplier of memory products, including flash memory controllers and other flash memory products such as SSDs based on those controllers. [10]

50. Phison's product lines include "different NAND Flash controllers for different application markets." Phison's SSD controllers "lead the industry" and are used in a variety of applications from the "mainstream market," to "high-end application/enterprise-level SSD" applications, to "the world's highest-capacity enterprise-level QLC SSD storage solution." Phison's eMMC and UFS products "push mobile storage devices into a new generation of higher speed and more energy saving" because the technology it uses "not only provides low power consumption, but also demonstrates excellent error correction capabilities and provides SSD-like performance." Phison's SD memory card-related products include controllers of "the industry's highest specification." Phison's USB products include controllers "specialized in high-capacity mobile storage applications."[11]

51. Getting the best speed, reliability, and storage capacity is critical in the flash storage market, and "manufacturers without advanced technology will lose their competitiveness."[12]

52. Phison designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes complete flash memory products (such as private-label SSDs) as well as the controllers that form the core of third parties' flash memory products and enable those products

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[10] Ex. S, Phison's Annual Report, available at https://www.phison.com/phocadownload/Annual_Reports/2023/Phison_Electronic_Corporation_2022_Annual_Report.pdf, at 4.
[11] *Id*. at 155.
[12] *Id*. at 154.

to have high speed, good reliability, and large capacity. This includes controllers, SSDs, USB memory cards, and embedded flash. It includes third-party products, including Kingston products such as DC1000B,[13] NV2, NV1, HyperX Savage, A400, A1000, DC500M, DC500R, FURY Renegade, KC400, KC3000, and KC1000,[14] and Phison-based products of a variety of other third-party flash memory vendors such as ADATA, Addlink, Apacer, Asura, Corsair, Digma, Galax, Gigabyte, Goodram, Inland, Integral Memory, Kingston, Kingmax, Klevv, Lite-On, MSI, Mushkin, MyDigitalSSD, Neo Forza, Patriot, PNY, Sabrent, Seagate, Silicon Power, Smartbuy, Team Force, Zadak, and Zotac.[15]

53. Phison designs, makes, uses, offers to sell, sells, imports, supplies, or otherwise distributes, and provides support for, flash memory products, including SSDs and flash memory controllers, for example the PS5026-E26 (consumer SSD), SA50 (enterprise SSD), PS8131 (SD), PS2251-11 (USB), and PS8229 (embedded flash), and other memory products that have the same or similar structures, features, or functionalities, as the aforementioned products, including finished products as well as controllers used to provide infringing functionality in Phison-based third-party flash products ("Accused Products").

54. The Accused Products are integrated into devices made, used, offered for sale, sold, imported, supplied, or otherwise distributed in the United States by among others, Phison, Phison's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), foundry suppliers, distributors, and other third parties. Phison's Accused Products are essential, non-trivial components of the products into which they are integrated.

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[13] Ex. T, https://www.kitguru.net/components/ssd-drives/simon-crisp/kingston-dc1000b-480gb-ssd-review/all/1/
[14] Ex. U, https://www.techpowerup.com/ssd-specs/#phison
[15] Ex. V, https://www.johnnylucky.org/data-storage/ssd-database.html.

55. Phison instructs its customers—such as OEMs of storage products—to combine its controllers with other components, such as MLC and SLC flash memory and volatile RAM, to create storage systems such as SSDs, memory cards, USB drives, embedded flash, and other devices. The Accused Products include these products for which Phison induces and contributes to infringement. Phison's controller products are especially adapted to operate in an infringing manner when combined as intended, and Phison knowingly instructs its customers to design and operate third-party products based on Phison controllers in an infringing manner.

56. Phison instructs its customers to connect the Accused Products to other systems, such as host computers and to NAND flash memory, and to operate the Accused Products in a particular manner.

57. Phison also conducts research, development, and testing of Accused Products in the United States. "Phison's R&D center located in Colorado, USA, . . . not only effectively cooperates with partners to develop and verify products, but also serves Tier-1 enterprise server manufacturer customers nearby." [16]

58. Phison maintains a website that advertised and continues to advertise the Accused Products, including identifying the applications for which they can be used and specifications for the Accused Products.

59. Phison's development, sales, and marketing activities in the United States, including within this District, directly contributed to Phison net revenue in the United States.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,891,298

60. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

[16] Ex. S at 1.

61. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the ’298 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

62. Phison has also knowingly and intentionally induces infringement of one or more claims of the ’298 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the ’298 Patent and the infringing nature of the Accused Products. Despite this knowledge of the ’298 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’298 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’298 Patent, thereby specifically intending for and inducing its customers to infringe the ’298 Patent through the customers’ normal and customary use of the Accused Products.

63. Phison has also infringed, and continues to infringe, one or more claims of the ’298 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’298 Patent, are especially made or adapted to infringe the ’298 Patent, and are not staple

articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’298 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

64. On information and belief, despite having knowledge of the ’298 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

65. The Accused Products meet all the limitations of at least claim 1 of the ’298 patent. Specifically, claim 1 of the ’298 patent recites:

> A system for storing data comprising:
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> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
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> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
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> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by

maintaining a count of the number of times each one of the blocks is accessed; and

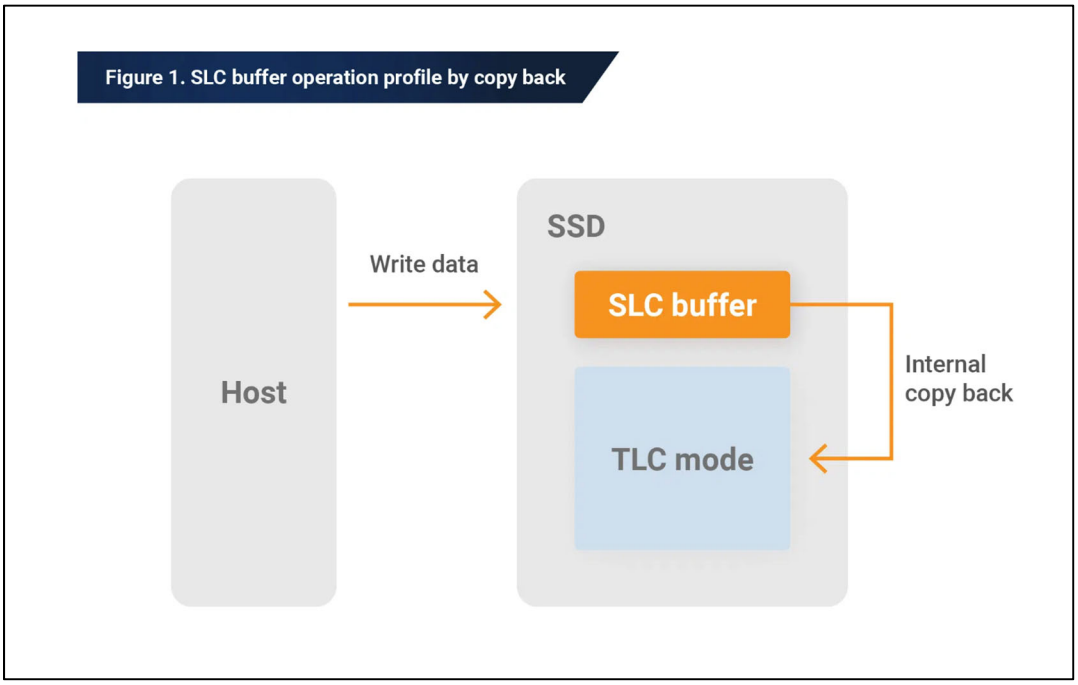
d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

66. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, Phison's SSDs, controllers, and other flash storage products are all systems for storing data.

Ex. W, (https://www.phison.com/en/solutions/enterprise).

67. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. For example, Phison products use MLC

(e.g. "TLC mode") memory as part of an SLC buffering system, and



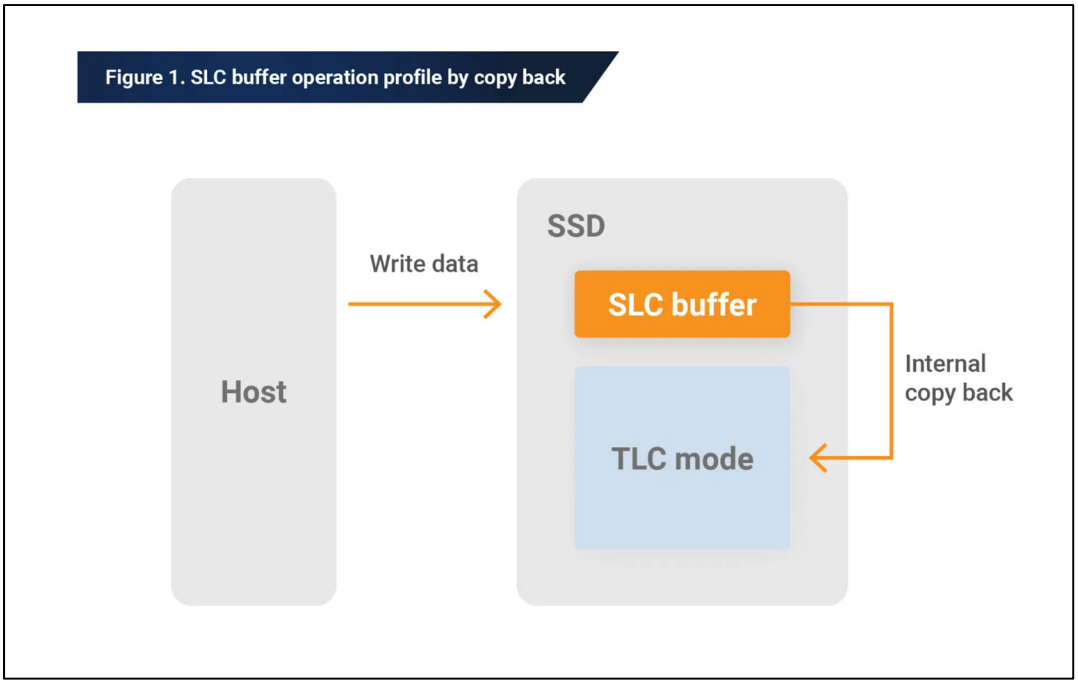
Ex. X, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

68. The flash memory uses individually erasable blocks. For example, Phison explains that individual blocks are erased, and that this is an "intrinsic characteristic of NAND device physics":

> A flash memory cell is composed of pages, and pages form a block. Due to the intrinsic characteristic of NAND device physics, the flash cell allows data to be programmed on a page level but only erased on a block level. This inconsistency between program and erase tasks is the major impact on SSD endurance.

Ex. Y, (https://phisonblog.com/ssd-garbage-collection/)

69. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. The SLC caching systems, for example, used by the Accused Products use individually erasable SLC blocks.



Ex. X, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

70. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module. For example, Phison's controller products are themselves controllers, and Phison's SSDs include Phison controllers.

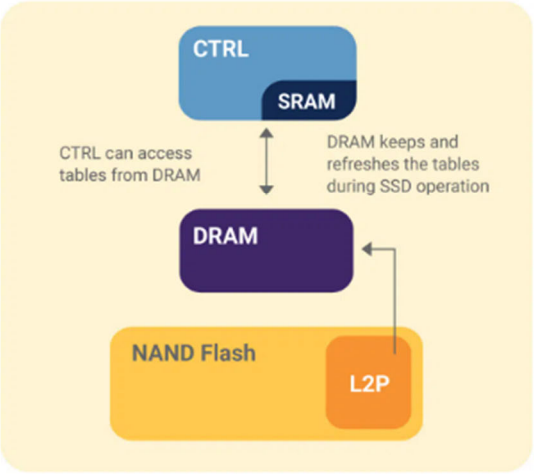
71. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, Phison controllers in the Accused

Products uses a mapping table such as an L2P (logical-to-physical) table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

72. Phison controllers use an L2P table:

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

Figure 2. Cache operating mechanism of SSD with DRAM



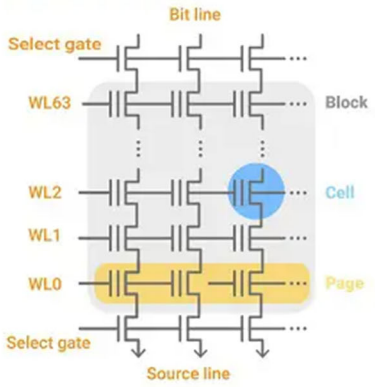
Ex. Z, https://phisonblog.com/host-memory-buffer-2/

73. In Phison controllers, a minimum quanta of addresses—such as a page—is used:

NAND Flash is a non-volatile memory composed of millions of floating-gate transistors that capture electrons within the gate. These floating-gate transistors can be thought of as memory cells. When millions of memory cells are connected, they form an array. Each array consists of blocks and each block contains numbers of pages.

Fig.1 gives a brief illustration of a NAND array f schematic.

Figure 1. NAND composition in transistor level



Ex. AA, https://phisonblog.com/ensuring-data-correctness-with-phisons-guaranteedflush-2/

74. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, Phison's products include controllers that incorporate defect and error management technology, and use a variety of tests to determine that there is a data integrity problem.

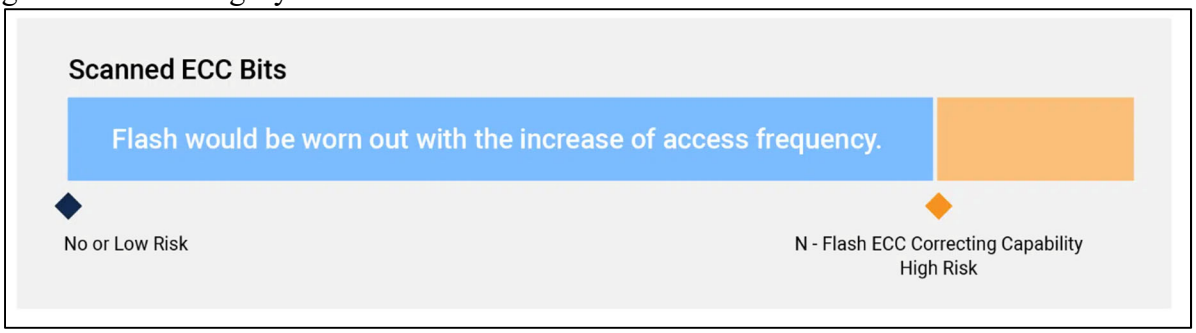
75. Phison controllers use a variety of data integrity tests to determine when there is a data integrity problem:

Phison's SmartRefresh™ technology

To protect the data stored in an SSD, Phison developed a proprietary technology called SmartRefresh™ that uses two primary methodologies:

1. Dynamic Error Bit Monitoring (DEBM)
2. Read Retry

"Phison's embedded firmware runs in the background to check the error bit of each block. Once there is a block fail within the criteria set by our firmware (i.e., the number of error bits is over the threshold decided in advance), the firmware performs specific actions on this failed block to guarantee the integrity of user data."



Ex. BB, (https://phisonblog.com/phisons-smartrefresh-2/)

Advanced Features:

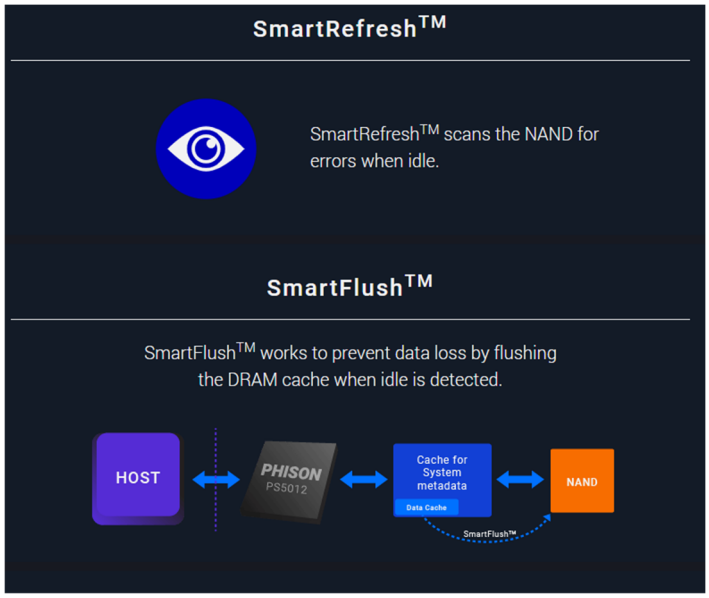
- End-to-end data path protection
- SmartECC RAID data protection
- P-fail protection with SmartFlush and GuaranteedFlush technology
- Advanced read disturb management with SmartRefresh technology
- Advanced global wear-leveling

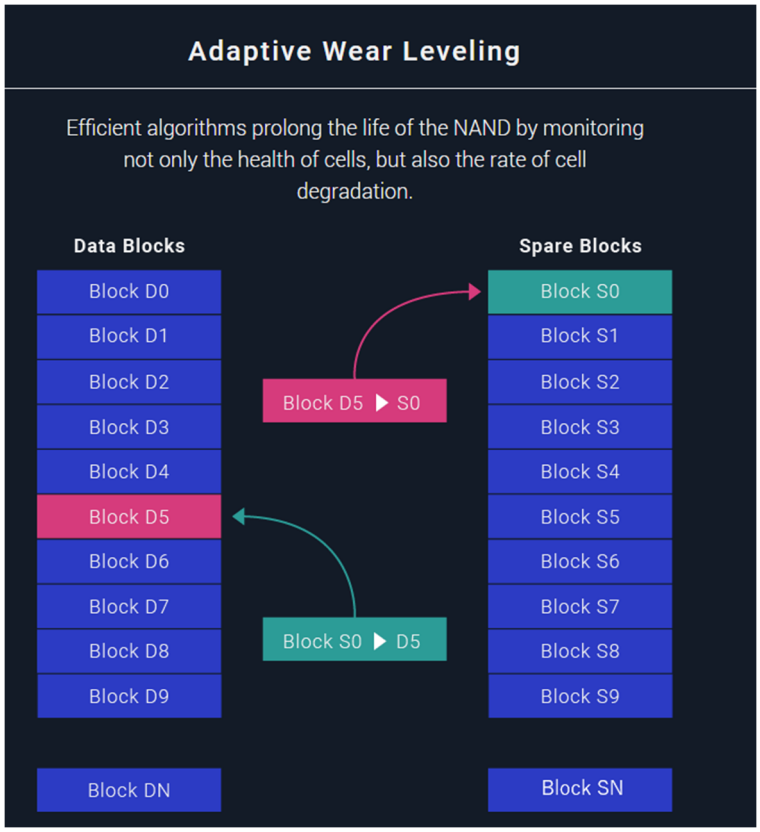
Ex. CC, (https://www.techpowerup.com/203889/phison-announces-quad-core-ps3110-sata-iii-ssd-controller)

76. Upon a data integrity failure, Phison controllers remap degraded data to the next available location:

"the firmware performs specific actions on this failed block to guarantee the integrity of user data."

Ex. BB, (https://phisonblog.com/phisons-smartrefresh-2/)





Ex. DD, (https://www.phison.com/en/technologies/ftl)

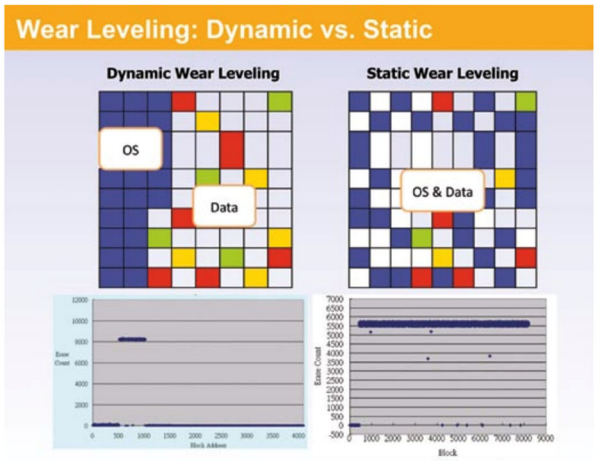
77. In particular, Phison controllers move data from MLC to SLC as part of the relocation above as part of Phison's SLC caching technology, where writes are made to SLC before being moved to MLC:

> Consumer workloads also write over a limited LBA range. W riting the data to SLC first ensures that only the final valid copy of the data is written to the QLC. This limits the writes to QLC, enabling QLC NAND to be used for consumer drive, despite its lower endurance.
>
> SLC cache is used in the consumer TLC drive today. It takes advantage of customer workloads to address the similar limitation of lower speed and limited endurance on TLC NAND. QLC based drives provide 33% higher capacity as compared to TLC NAND. This lowers the cost of the drive.

Ex. I, (https://phisonblog.com/qlc-nand-for-consumer-ssds-2/)

78. For example, Phison's articles describing its storage devices discuss "replacing MLC to SLC":

> With process advances, NAND Flash can support the development of more cost-competitive solutions but the reliability of NAND Flash is getting worse. In terms of market response, customers won't just accept inferior quality products because of the price drop. On the contrary, they demand products at the same level but with the same or better reliability and performance. Therefore, the focus of attention has turned to the Flash controller to address this problem.
>
> Basically, significant problems of reliability are caused by things like replacing MLC to SLC, increasing 2 bits/cell to 3 bits/cell, reducing the Erase Cycle number from 100K down to 10K, and cutting Data Retention times through the advances of NAND Flash. These issues can be solved within a re-designed and robust controller.
>
> For example, the error rates of NAND Flash are increasing



Ex. EE, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

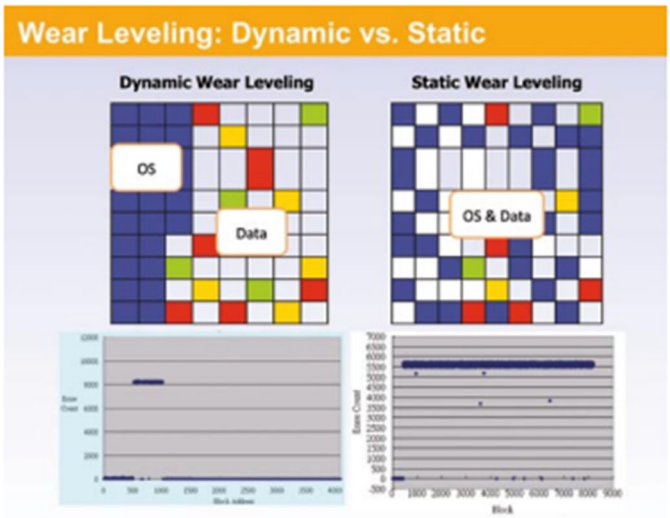
79. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, Phison's products use controllers that employ various types of block counting.

80. For example, Phison controllers use count data, such as program/erase counts and valid page counts, to maintain a count of the number of times each one of the blocks is accessed:

> **Dynamic SLC buffer (D3)**
>
> A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Ex. X, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

In addition, decreasing the Erase Count has brought about a shorter life expectancy of NAND Flash. The wear leveling mechanism of the controller can resolve this problem. NAND Flash consists of many blocks and each block has its certain life span. The number of erasable cycles represented the block life-expectancy and was called the Erase Count. In order to extend the lifetime of NAND Flash, we have to balance the Erase Count of all blocks. With a wear leveling mechanism implemented, the controller can achieve this goal to average the Erase Count of each block.



Ex. EE, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

"A memory management method, and a memory control circuit unit and a memory storage apparatus using the same are provided. The method includes associating physical erasing units with a data area or a spare area, configuring a plurality of logical addresses for mapping to the physical erasing units, and obtaining a garbage collection threshold based on a plurality of valid logical addresses among the logical addresses, and the physical erasing units mapping to the valid logical addresses are associated with the data area. The method further includes performing a garbage collection operation on the data area if the number of the physical erasing units associated with the data area is no less than the garbage collection threshold."

Ex. FF, U.S. Pat. App. Pub. No. 2019/0073298, Abstract.

81. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module wherein the controller is adapted to allocate those blocks that receive the most frequent writes by transferring

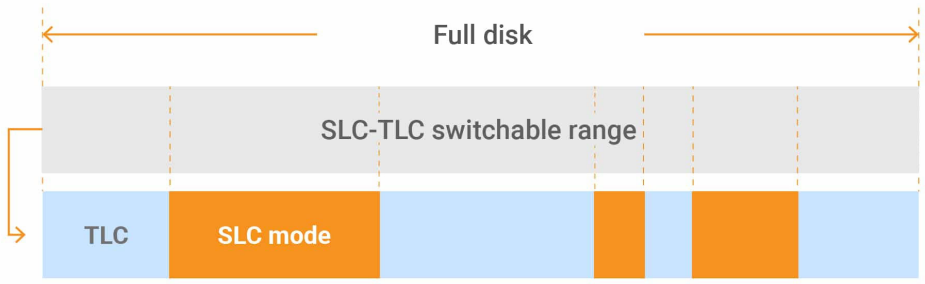
the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, the controller transfers the contents of those blocks that receive the most frequent writes to SLC memory.

82. Phison controllers move frequently accessed data to SLC NAND. A "count balance scheme" is used to transfer frequently written blocks to SLC, and blocks are switchable between SLC and TLC:

Dynamic SLC buffer (D3)

A dynamic SLC buffer used with TLC flash, meaning that the SLC buffer in zone D3 zone can dynamically use the TLC flash by erasing the count balance scheme. The SSD firmware configures to select the block with the lowest erase count every time the dynamic SLC buffer is processed. The dynamic SLC buffer can be automatically disabled using FW calculations based on flash endurance for different flash types.

Figure 3. Dynamic SLC buffer profile



Ex. X, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

83. In addition, garbage collection can relocate frequently accessed data based on a page count:

> For random writes, the main issue is invalid pages. Whenever garbage collection engages, the controller needs to write valid pages to other unused blocks. With the background read/write and Host read/write requests, the overall drive performance degrades.

Ex. GG, https://phisonblog.com/using-overprovisioning-with-ssds-2/

84. Phison also uses a "double rotation" scheme to move data to SLC blocks:

> Therefore, controllers are using many sophisticated functions to protect stored data. We can observe these results during our daily work, many steps have to be applied before data will be recovered and almost every operation, we reverse, is applied to protect user data as well as possible.
>
> In this article, we would like to bring closer SLC blocks topic and present to you the solution for Phison controllers which are using double rotation mode.
>
> How to recognize that controller uses double rotation?
>
> How to reverse this type of rotation?
>
> How to pull out data from the SLC block?
>
> All this information you will find in this article.
>
> In the example below we have a dump from a micro SD card equipped with a Phison controller. We've used static rotation, but despite, that the rotation element is attached, we could not access the file system.
>
> Visual Nand Reconstructor - phison double rotation

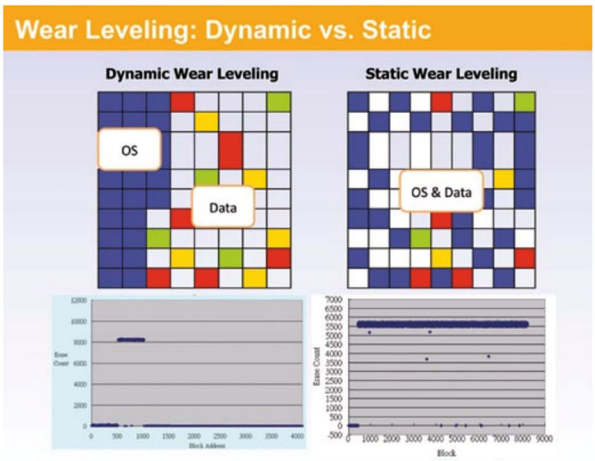
Ex. HH, https://support.rusolut.com/portal/en/kb/articles/no-pic-no

85. Phison's articles discuss "replacing MLC to SLC":

With process advances, NAND Flash can support the development of more cost-competitive solutions but the reliability of NAND Flash is getting worse. In terms of market response, customers won't just accept inferior quality products because of the price drop. On the contrary, they demand products at the same level but with the same or better reliability and performance. Therefore, the focus of attention has turned to the Flash controller to address this problem.

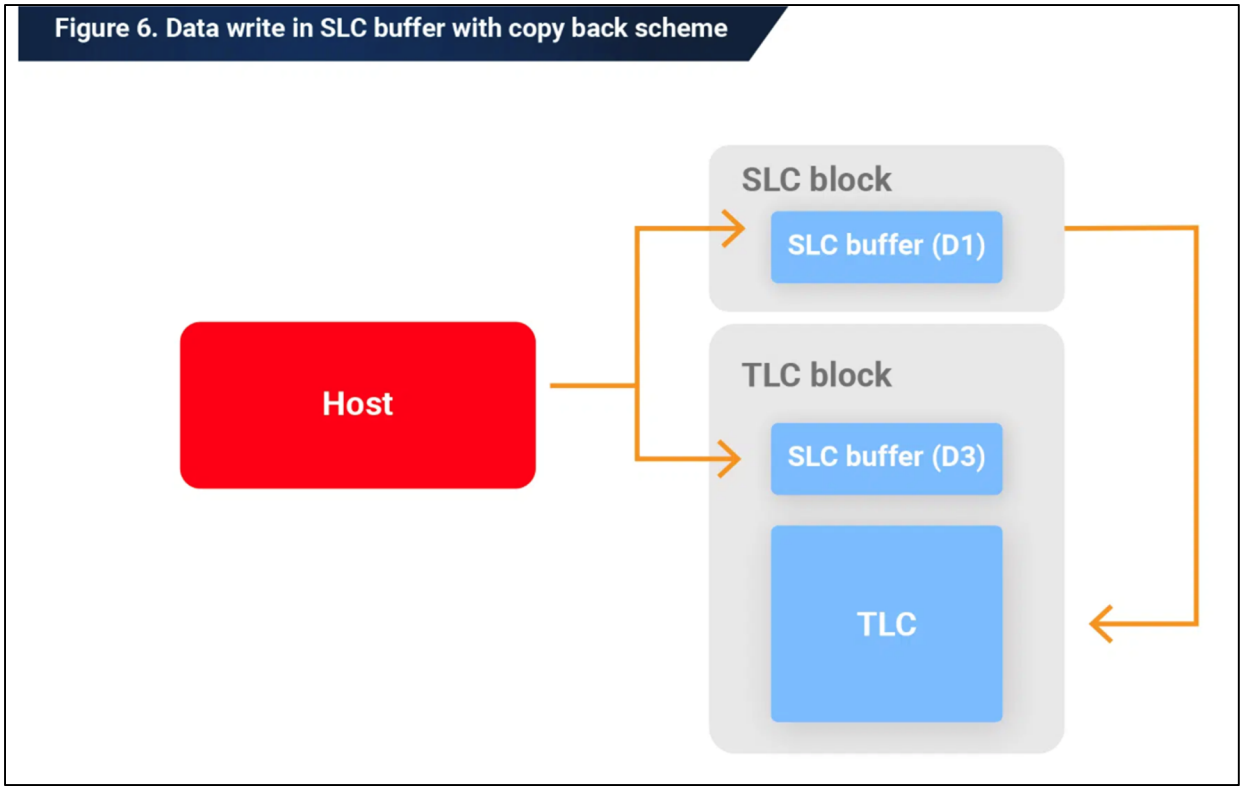
Basically, significant problems of reliability are caused by things like replacing MLC to SLC, increasing 2 bits/cell to 3 bits/cell, reducing the Erase Cycle number from 100K down to 10K, and cutting Data Retention times through the advances of NAND Flash. These issues can be solved within a re-designed and robust controller.

For example, the error rates of NAND Flash are increasing



Ex. EE, (https://www2.advantech.com/embcore/promotions/whitepaper/PHISON%20Electronics-The_Stability_and_Reliability_of_Storage_Devices.pdf)

86. Phison's controllers have a copyback scheme where data is moved between SLC and TLC blocks; with this scheme, data being rewritten as part of garbage collection may be moved from TLC to SLC. For example, Phison's blog explains that "When an SSD uses copy back, host data moves into zone D1," where D1 represents SLC.



Ex. X, https://phisonblog.com/the-benefits-of-using-slc-buffers-with-ssds-2/

87. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

88. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

89. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '298 patent by Defendant.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,196,385

90. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

91. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the ’385 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

92. Phison has also knowingly and intentionally induces infringement of one or more claims of the ’385 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the ’385 Patent and the infringing nature of the Accused Products. Despite this knowledge of the ’385 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’385 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’385 Patent, thereby specifically intending for and inducing its customers to infringe the ’385 Patent through the customers’ normal and customary use of the Accused Products.

93. Phison has also infringed, and continues to infringe, one or more claims of the ’385 Patent by selling, offering for sale, or importing into the United States, the Accused

Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’385 Patent, are especially made or adapted to infringe the ’385 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’385 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

94. On information and belief, despite having knowledge of the ’385 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

95. The Accused Products meet all the limitations of at least claim 1 of the ’385 patent. Specifically, claim 1 of the ’385 patent recites:

> A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a flash translation layer (FTL); wherein the FTL is adapted to:
>
> a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;

c) determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed; and

d) allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module.

96. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

97. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

98. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

99. The Accused Products include a flash translation layer (FTL). For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table. This is known as a flash translation layer:

FLASH TRANSLATION LAYER

Phison develops its own FTL with proprietary improvements from generation to generation. Proprietary technologies include:

Ex. DD, (https://www.phison.com/en/technologies/ftl)

100. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

101. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

102. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed. For example, as explained in Count I above, a variety of block counting mechanisms are present in the Accused Products.

103. The Accused Products include a flash translation layer (FTL), wherein the FTL is adapted to allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module. For example, as explained in Count I above, frequently written blocks are allocated and their contents transferred to SLC.

104. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

105. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

106. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '385 patent by Defendant.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 9,997,240

107. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

108. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '240 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

109. Phison has also knowingly and intentionally induces infringement of one or more claims of the ’240 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the ’240 Patent and the infringing nature of the Accused Products. Despite this knowledge of the ’240 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’240 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’240 Patent, thereby specifically intending for and inducing its customers to infringe the ’240 Patent through the customers’ normal and customary use of the Accused Products.

110. Phison has also infringed, and continues to infringe, one or more claims of the ’240 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’240 Patent, are especially made or adapted to infringe the ’240 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’240 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

111. On information and belief, despite having knowledge of the ’240 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

112. The Accused Products meet all the limitations of at least claim 6 of the ’240 patent. Specifically, claim 6 of the ’240 patent recites:

> 6. A system for storing data comprising:
>
> at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks;
>
> at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks; and
>
> a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module;
>
> wherein the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks; and
>
> wherein the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module;
>
> wherein the controller is further adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller.

113. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

114. The Accused Products include at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in MLC memory with individually erasable blocks, for example as part of an SLC caching or direct-to-TLC system.

115. The Accused Products include at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks. As explained in Count I above, the Accused Products store certain data in SLC memory with individually erasable blocks, for example as part of an SLC caching system.

116. The Accused Products include a controller coupled to the at least one MLC non-volatile memory module and the at least one SLC non-volatile memory module, the controller maintaining an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module. For example, as explained in Count I above, the Accused Products provide mapping between logical and physical addresses using a data structure such as a L2P table, and these mappings have a minimum quanta such as a page.

117. In the Accused Products, the controller allocates those blocks that receive frequent writes into the SLC non-volatile memory module as hot blocks and those blocks that only receive infrequent writes into the MLC non-volatile memory module as cold blocks. For example, as explained in Count I above, frequently written blocks are allocated and their

contents transferred to SLC, and infrequently written data is moved to MLC through copyback/garbage collection and other procedures.

118. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory module, fails a data integrity test, and, in the event of such a failure, the controller remaps the entry to the next available equivalent range of physical addresses within the at least one SLC non-volatile memory module. For example, as explained in Count I above, the controllers in the Accused Products perform a variety of data integrity functions, and remap data to SLC memory upon the failure of a data integrity test.

119. In the Accused Products, the controller is adapted to maintain a count value of those blocks that are accessed most frequently and, on a periodic basis when the count value is a predetermined count value, transfer the contents of those counted blocks into the SLC non-volatile memory module, wherein the counted blocks transferred to after reaching the predetermined count value are determined in accordance with the next equivalent range of physical addresses determined by the controller. For example, as explained in Count I above, the Accused Products employ various types of block counting, and transfer the contents of frequently written blocks to the next available locations in SLC based on the count value.

120. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

121. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

122. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '240 patent by Defendant.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,950,300

123. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

124. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '300 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

125. Phison has also knowingly and intentionally induces infringement of one or more claims of the '300 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the '300 Patent and the infringing nature of the Accused Products. Despite this knowledge of the '300 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the '300 Patent, including but not limited to the use of host memory buffers. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the '300 Patent, thereby specifically intending for and inducing its customers to

infringe the ’300 Patent through the customers’ normal and customary use of the Accused Products.

126. Phison has also infringed, and continues to infringe, one or more claims of the ’300 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’300 Patent, are especially made or adapted to infringe the ’300 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’300 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

127. On information and belief, despite having knowledge of the ’300 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

128. The Accused Products meet all the limitations of at least claim 1 of the ’300 patent. Specifically, claim 1 of the ’300 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;
>
> at least one controller to operate memory elements and associated memory space;
>
> at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;
>
> at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;
>
> at least one random access volatile memory;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

129. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

130. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space. For example, as explained in Count I above, the Accused Products include MLC and SLC memory. These locations are mapped to memory space:

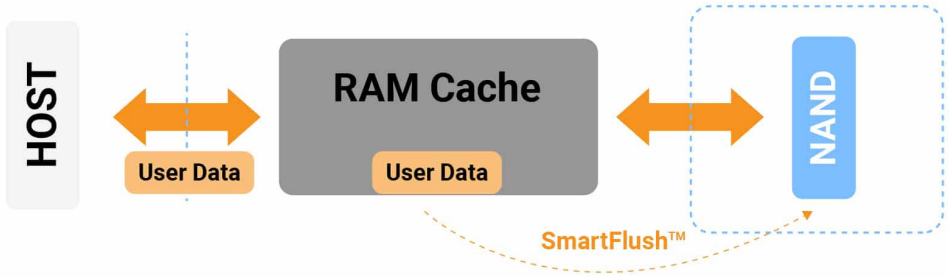
How GC processes data

Since SSDs cannot overwrite existing data in NAND memory cells, they must first erase old data before programming new data to the same location. GC is the process of relocating existing data to new locations within free memory space and allowing the surrounding invalid data to be erased thoroughly.

Ex. Y, (https://phisonblog.com/ssd-garbage-collection/)

In addition, Phison controllers use RAM caching to store user data and metadata in RAM (volatile) memory:

Figure 3. Main concept of SmartFlush™



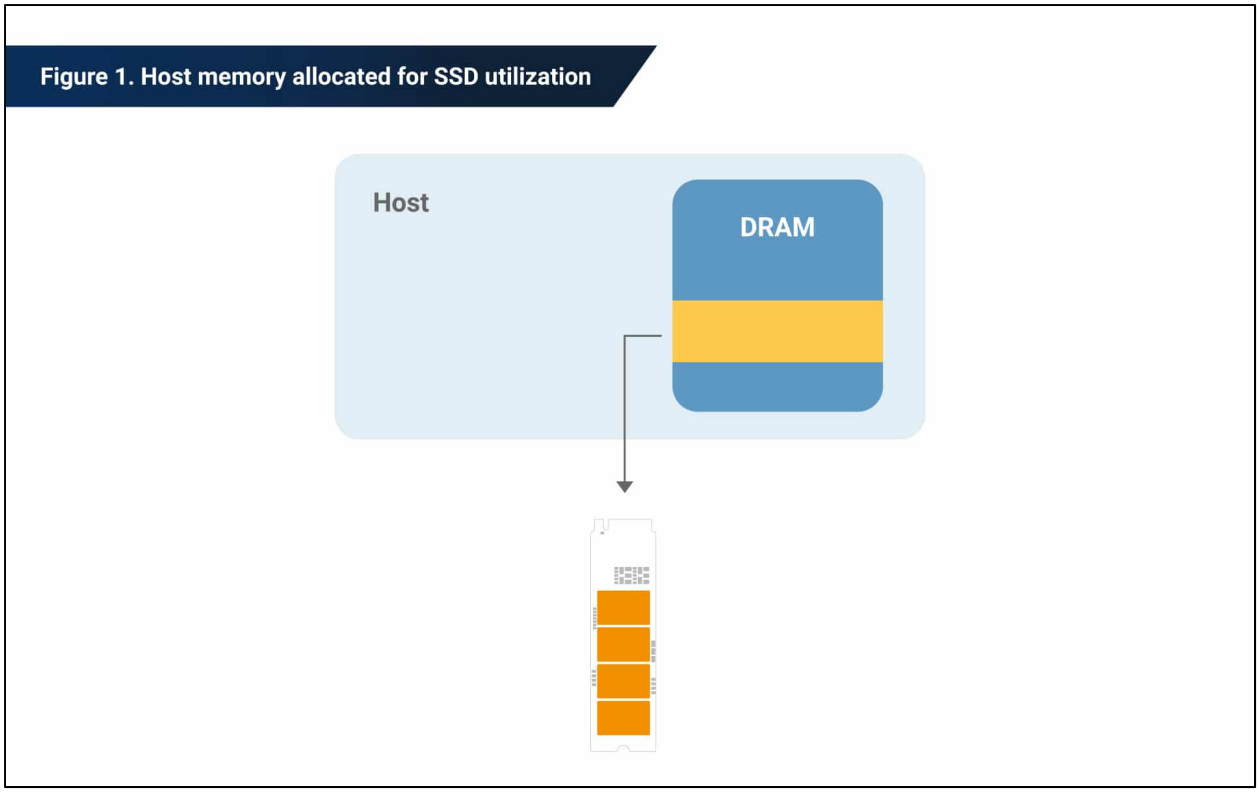
Ex. II, (https://phisonblog.com/smartflush/)

131. The Accused Products include at least one controller to operate memory elements and associated memory space. The Accused Products include controllers, for example the controllers identified in paragraph 50 above.

132. The Accused Products include at least one MLC nonvolatile memory element that can be mapped into the MLC memory space. For example, the MLC memory in the Accused Products is mapped into a memory space.

133. The Accused Products include at least one SLC nonvolatile memory element that can be mapped into the SLC memory space. For example, the SLC memory in the Accused Products is mapped into a memory space.

134. The Accused Products include at least one random access volatile memory. For example, the Accused Products include RAM. Many of the Accused Products are designed to work with, and in some cases include, a type of RAM called DRAM. The Accused Products' controllers also include other types of random access volatile memory, such as static RAM ("SRAM"). Finally, Phison instructs users to combine many of the Accused Products with a host system that has available random access memory to form a "Host Memory Buffer" for the flash storage product's use.

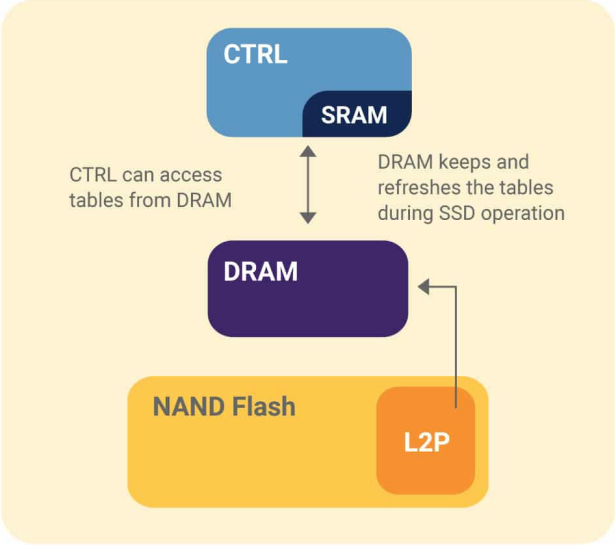


Ex. Z, (https://phisonblog.com/host-memory-buffer-2/)

Phison NVMe SSD Controller Comparison					
	E31T	E27T	E21T	E26	E18
Market Segment	Mainstream Consumer			High-End Consumer	
Manufacturing Process	7nm	12nm	12nm	12nm	12nm
CPU Cores	1x Cortex R5	1x Cortex R5	1x Cortex R5	2x Cortex R5	3x Cortex R5
Error Correction	7th Gen LDPC	5th Gen LDPC	4th Gen LDPC	5th Gen LDPC	4th Gen LDPC
DRAM	No	No	No	DDR4, LPDDR4	DDR4
Host Interface	PCIe 5.0 x4	PCIe 4.0 x4	PCIe 4.0 x4	PCIe 5.0 x4	PCIe 4.0 x4
NVMe Version	NVMe 2.0?	NVMe 2.0?	NVMe 1.4	NVMe 2.0	NVMe 1.4
NAND Channels, Interface Speed	4 ch, 3200 MT/s?	4 ch, 2400 MT/s?	4 ch, 1600 MT/s	8 ch, 2400 MT/s	8 ch, 1600 MT/s
Max Capacity	8 TB	8 TB	4 TB	8 TB	8 TB
Sequential Read	10.8 GB/s	7.4 GB/s	5.0 GB/s	14 GB/s	7.4 GB/s
Sequential Write	10.8 GB/s	6.7 GB/s	4.5 GB/s	11.8 GB/s	7.0 GB/s
4KB Random Read IOPS	1500k	1200k	780k	1500k	1000k
4KB Random Write IOPS	1500k	1200k	800k	2000k	1000k

Ex. JJ, (https://www.anandtech.com/show/18879/phison-unveils-ps5031e31t-ssd-platform-for-lower-power-mainstream-pcie-5-ssds)

Figure 2. Cache operating mechanism of SSD with DRAM



Ex. Z, (https://phisonblog.com/host-memory-buffer-2/)

135. The Accused Products include an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory. As explained with respect to Counts I and II above, the Accused Products include an FTL flash translation layer with an L2P table. Phison explains that the L2P table is stored in flash memory and in DRAM:

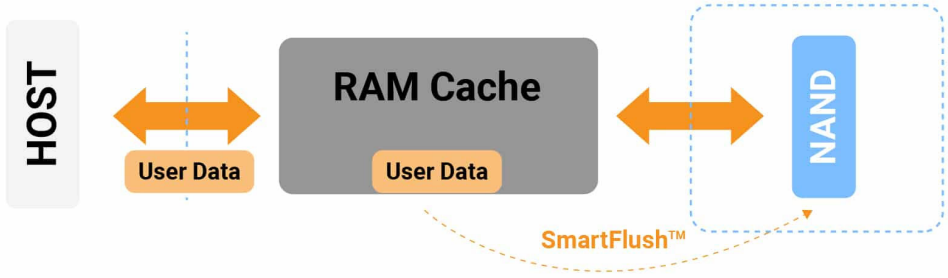
> The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

> On the other hand, during powered-on scenarios, the L2P table is uploaded to DRAM so that it can be constantly updated by the controller. The larger the DRAM size, the more free space available for the controller to play with. This generally means more flexible data placement and thus better reaction time upon receiving commands. In terms of typical data workloads, operations that call for so-called "random read" sequences benefit the most from ample DRAM space.

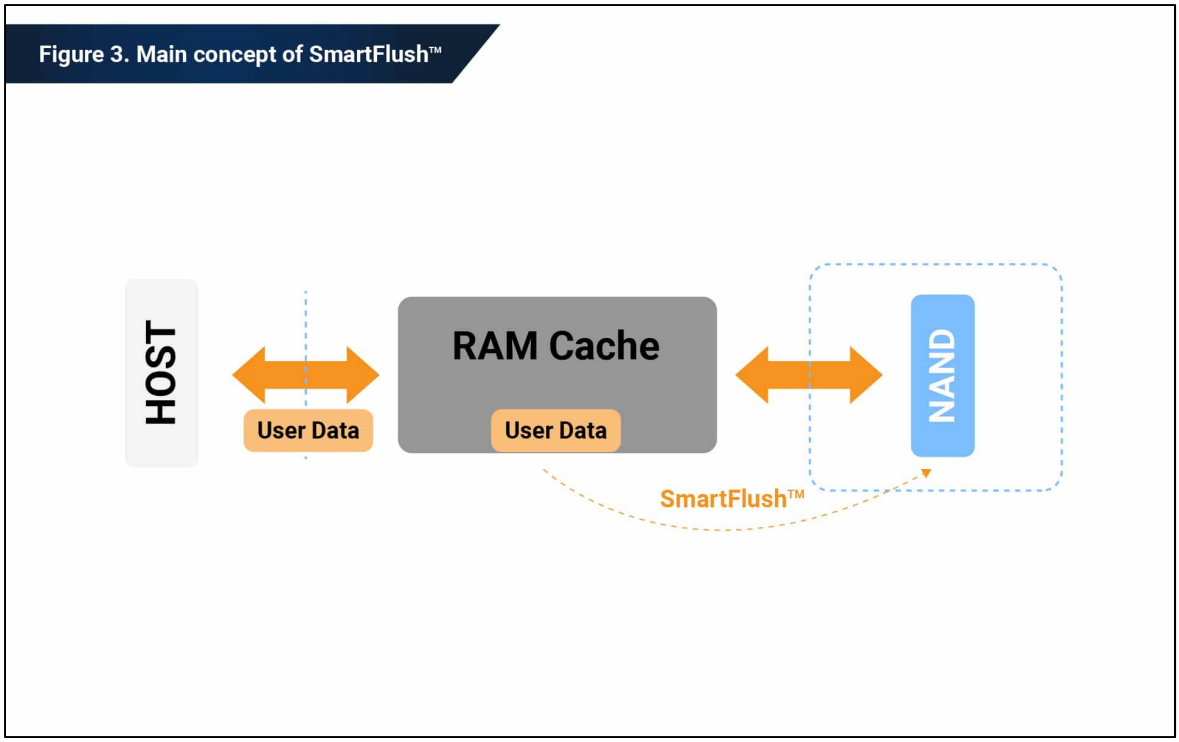
Ex. Z, (https://phisonblog.com/host-memory-buffer-2/)

136. The Accused Products include a controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory. For example, the controller in the Accused Products controls access to the MLC and SLC memory and the DRAM, storing data in the flash memory and retaining data in the DRAM:

Figure 3. Main concept of SmartFlush™

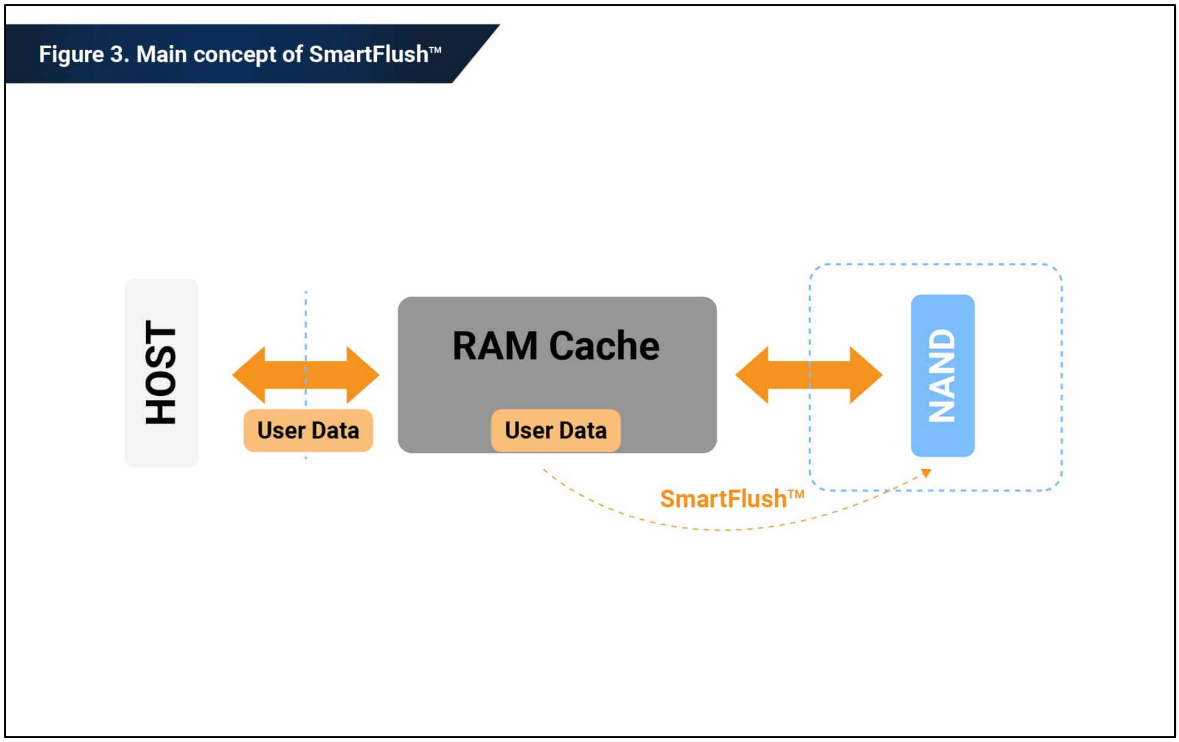


Ex. II, (https://phisonblog.com/smartflush/)



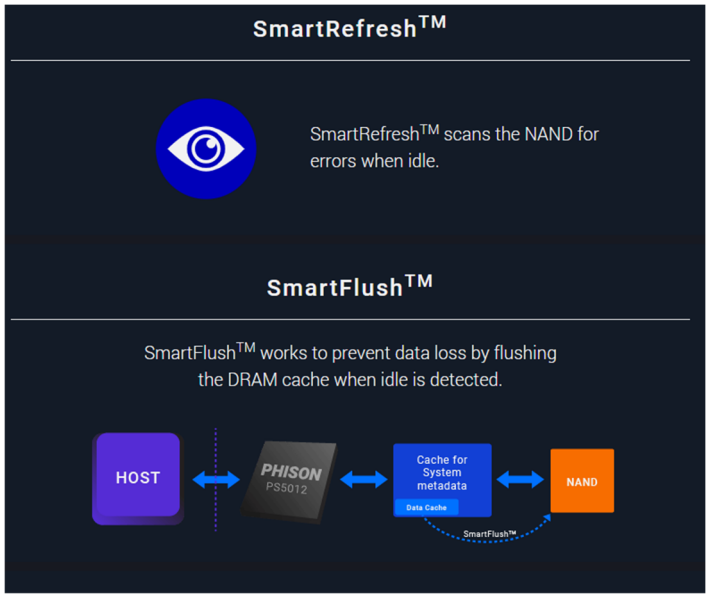
Ex. II, (https://phisonblog.com/smartflush/)

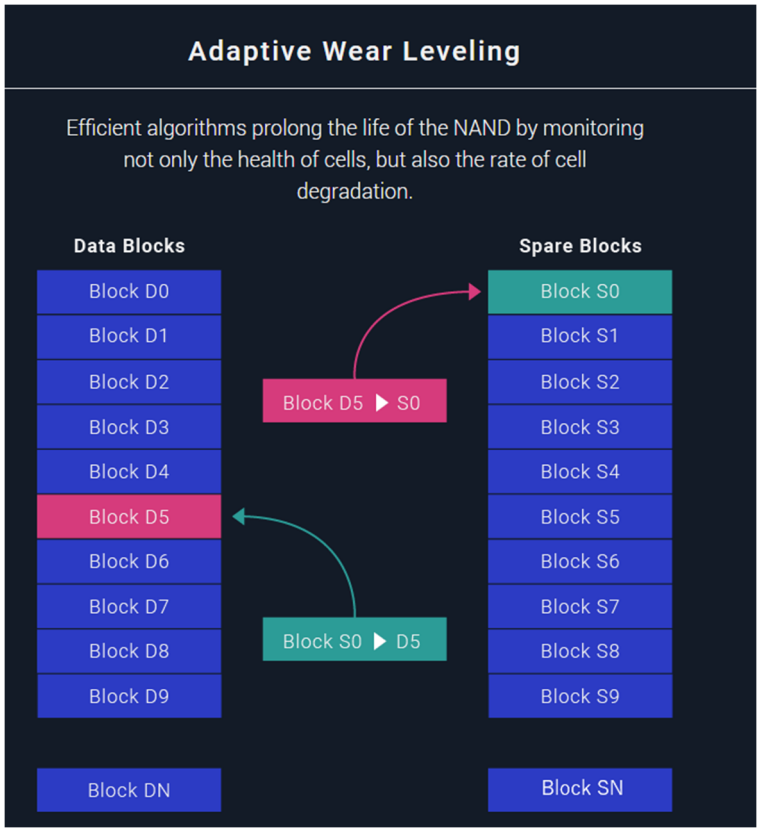
137. In the Accused Products, the controller performs a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation is performed thereon by comparing the stored data to the retained data in the random access volatile memory. For example, the controller in the Accused Products performs a data integrity test by comparing data stored in the flash memory with data retained in RAM. For instance, the controller compares data—either user data or data from the logical-to-physical (L2P) table—in RAM with that stored in the NAND flash memory and uses the data to eliminate the risk of data loss in case of any error.



Ex. II, (https://phisonblog.com/smartflush/)

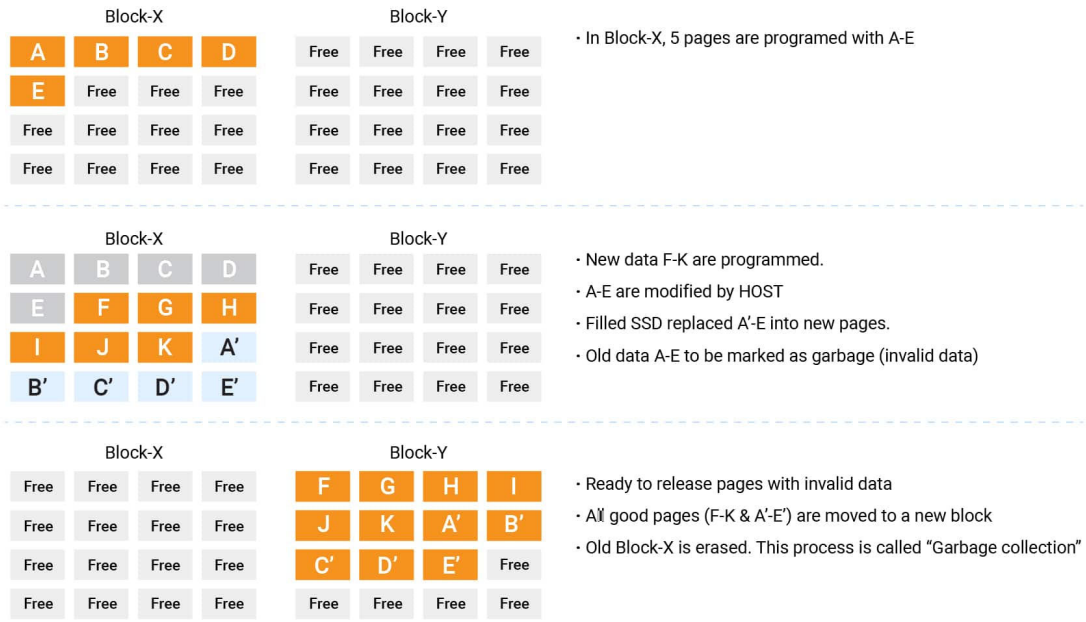
138. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, the Accused Products' controllers employ wear leveling and garbage collection techniques that transfer blocks within the flash memory in a way that maximizes lifetime.





Ex. DD, (https://www.phison.com/en/technologies/ftl)

Figure 2. The illustration of garbage collection

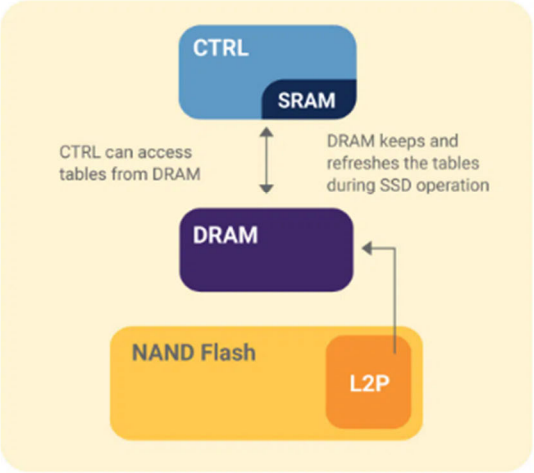


Ex. Y, (https://phisonblog.com/ssd-garbage-collection/)

The controller uses a mapping table to keep track of the relationship between the logical blocks and the physical addresses of the flash memory.

The most important information that gets cached to or retrieved from a DRAM is the mapping information that turns logical addresses into the physical locations of stored data within the NAND flash array. This information is stored in mapping tables called L2P (logical-to-physical) tables and is updated frequently as SSDs move data in and out of flash storage. During shutdowns, the L2P table is stored in flash memory, since DRAM quickly becomes inoperable without a continuous power supply.

Figure 2. Cache operating mechanism of SSD with DRAM



Ex. Z, https://phisonblog.com/host-memory-buffer-2/

The flash memory is organized by page and block, where a page is the smallest program unit and a block is the smallest erase unit.

A flash memory cell is composed of pages, and pages form a block. Due to the intrinsic characteristic of NAND device physics, the flash cell allows data to be programmed on a page level but only erased on a block level. This inconsistency between program and erase tasks is the major impact on SSD endurance.

Ex. Y, (https://phisonblog.com/ssd-garbage-collection/)

139. In the Accused Products, a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance. For example, the Accused Products remap data to new physical addresses after failing a data integrity test which compared data stored in the flash memory with data retained in the DRAM in order to achieve enhanced endurance. When defects in memory are found, valid data in the cells is rewritten. Because a block cannot be rewritten until it is erased, the valid data is remapped to a different physical range of addresses when writing,

> Before claiming the space taken up by invalid data, all the valid data in pages from the initial block must be copied and written into empty pages of a new block. The invalid data in the original block can then be erased, ready for new valid data to be written.

Ex. Y, (https://phisonblog.com/ssd-garbage-collection/)

> Phison's embedded firmware runs in the background to check the error bit of each block. Once there is a block fail within the criteria set by our firmware (i.e., the number of error bits is over the threshold decided in advance), the firmware performs specific actions on this failed block to guarantee the integrity of user data.

Ex. BB, (https://phisonblog.com/phisons-smartrefresh-2/)

140. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

141. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

142. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '300 patent by Defendant.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 11,830,546

143. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

144. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '546 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

145. Phison has also knowingly and intentionally induces infringement of one or more claims of the '546 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the '546 Patent and the infringing nature of the Accused Products. Despite this knowledge of the '546 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the '546 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the '546 Patent, thereby specifically intending for and inducing its customers to infringe the '546 Patent through the customers' normal and customary use of the Accused Products.

146. Phison has also infringed, and continues to infringe, one or more claims of the ’546 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’546 Patent, are especially made or adapted to infringe the ’546 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’546 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

147. On information and belief, despite having knowledge of the ’546 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

148. The Accused Products meet all the limitations of at least claim 1 of the ’546 patent. Specifically, claim 1 of the ’546 patent recites:

> A system for storing data comprising:
>
> memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space;
>
> at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements;
>
> a bank of nonvolatile memory, including:
>
> a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and
>
> at least one SLC memory module including at least one SLC nonvolatile memory element;
>
> at least one random access volatile memory element;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller having associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

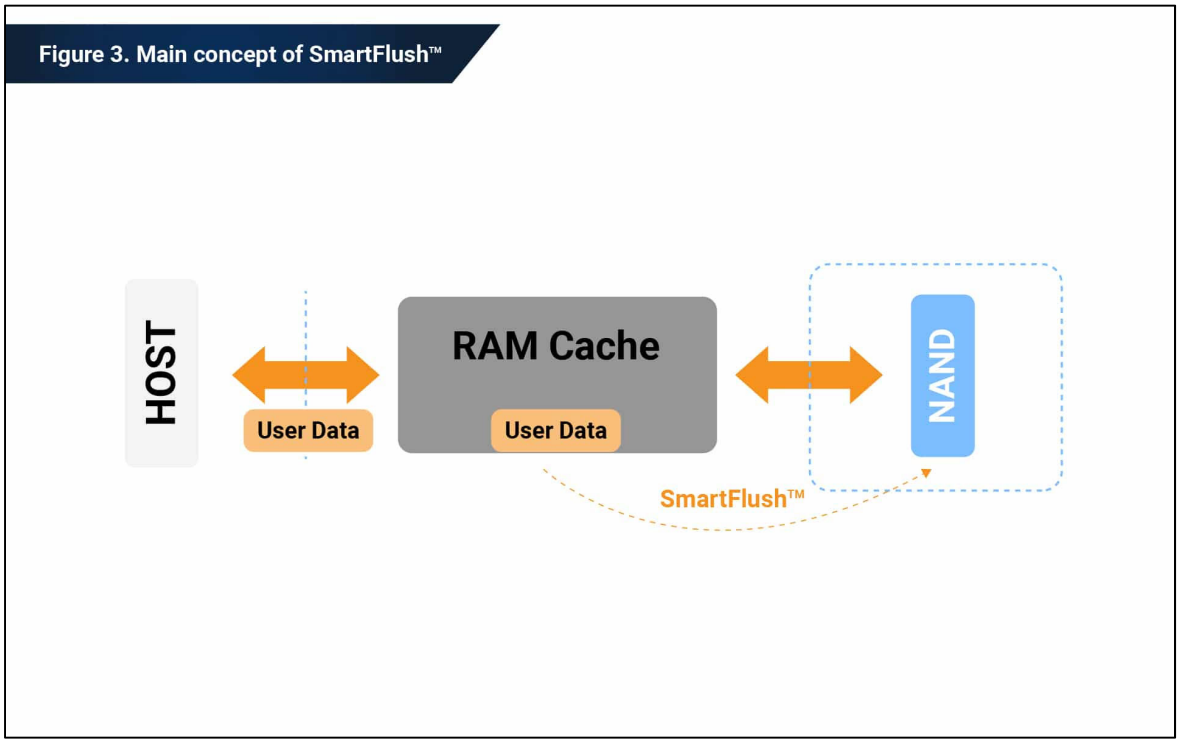
wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test.

149. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

150. The Accused Products include memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space. For example, as explained in Count IV

above, Phison's products use both MLC and SLC memory space, as well as volatile memory space (e.g. for RAM).

151. The Accused Products include at least one controller to operate memory elements and associated memory space for associated Write access operations to the memory elements and Read access operations from the memory elements. For example, the controllers in the Accused Products handle read and write operations to flash memory.



Ex. II, (https://phisonblog.com/smartflush/)

152. The Accused Products include a bank of nonvolatile memory, including a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element, and at least one SLC memory module including at least one SLC nonvolatile memory element. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory.

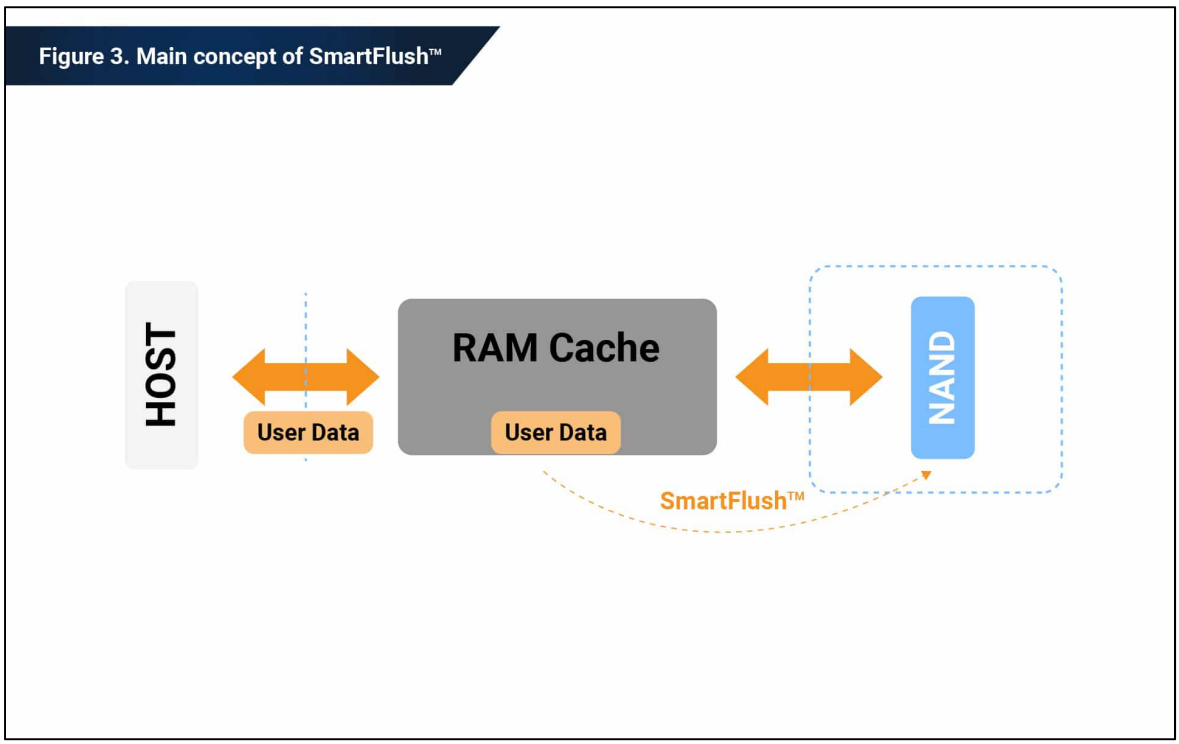
153. The Accused Products include at least one random access volatile memory element. For example, as explained in Count IV above, the Accused Products contain some form of RAM such as DRAM or SRAM. In addition, Phison instructs users to combine many of the Accused Products with a host system that has available random access memory to form a "Host Memory Buffer" for the flash storage product's use.

154. The Accused Products include a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the memory elements. For example, as shown with respect to Count IV above, the Accused Products maintain an address table in flash memory.

155. The controller in the Accused Products has associated controller memory for storing received data therein, the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one of the MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile memory as retained data associated with stored data. For example, as shown with respect to Count IV above, the Accused Products cache written data in RAM.

156. The controller in the Accused Products performs a data integrity test on stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated

with the stored data in the random access volatile memory by the controller during the Write access operation. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test by comparing stored data and retained data. In addition, the controller provides controller memory such as buffers or caches to store retained data:



Ex. II, (https://phisonblog.com/smartflush/)

157. In the Accused Products, the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories. For example, as shown with respect to Count IV above, the Accused Products use wear leveling and garbage collection, in conjunction with an L2P table, to map logical and physical addresses as necessitated by the system to maximize lifetime.

158. In the Accused Products, a failure of the data integrity test performed on the stored data by the controller results in a remapping of address space to a different physical range of addresses and transfer of data corresponding to the retained data to those remapped physical addresses from those physical addresses determined to have failed the data integrity test. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

159. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

160. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

161. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '546 patent by Defendant.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 11,854,612

162. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

163. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '612 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

164. Phison has also knowingly and intentionally induces infringement of one or more claims of the ’612 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the ’612 Patent and the infringing nature of the Accused Products. Despite this knowledge of the ’612 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’612 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’612 Patent, thereby specifically intending for and inducing its customers to infringe the ’612 Patent through the customers’ normal and customary use of the Accused Products.

165. Phison has also infringed, and continues to infringe, one or more claims of the ’612 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’612 Patent, are especially made or adapted to infringe the ’612 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’612 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

166. On information and belief, despite having knowledge of the ’612 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

167. The Accused Products meet all the limitations of at least claim 1 of the ’612 patent. Specifically, claim 1 of the ’612 patent recites:

> A method for storing data comprising:
>
> maintaining an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element;
>
> mapping logical and physical addresses adaptable to the system by the address table, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps data in at least one of volatile or nonvolatile memories;
>
> controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller;
>
> storing received data within a controller memory associated with the at least one controller;
>
> controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data;
>
> transferring the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data;
>
> retaining the received data in the random access volatile memory as retained data associated with the stored data;
>
> performing a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon, the performing of the data integrity test further comprising:
>
> reading the stored data to the controller memory;
>
> comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation;

> remapping, responsive to a failure of the data integrity test performed on the stored data by the controller, the address space to a different physical range of addresses; and
>
> transferring data corresponding to the retained data to those remapped physical address from those physical addresses determined to have failed the data integrity test.

168. To the extent the preamble is a limitation, when used by Phison or its customers, the Accused Products perform a method for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

169. When used by Phison or its customers, the Accused Products maintain an address table for a memory space containing volatile memory and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space and the volatile memory includes a random access volatile memory element. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory, and use an address table such as an L2P table to map logical and physical addresses.

170. When used by Phison or its customers, the Accused Products map logical and physical addresses adaptable to the system by the address table, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps data in at least one of volatile or nonvolatile memories. For example, as explained in Count IV above, the Accused Products use an address table such as an L2P table to map logical and physical addresses, and use techniques such as wear leveling and garbage collection to map the addresses as necessitated by the system to maximize lifetime.

171. When used by Phison or its customers, the Accused Products control during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module

including at least one SLC nonvolatile memory element and associated memory space using at least one controller. For example, as explained in Count IV above, the Accused Products include both SLC and MLC nonvolatile memory, and use an address table such as an L2P table to map logical and physical addresses.

172. When used by Phison or its customers, the Accused Products store received data within a controller memory associated with the at least one controller. For example, as explained in Count V above, the Accused Products include a controller that handles reads and writes and stores data in controller memory, which may be used as a cache, as part of that process.

173. When used by Phison or its customers, the Accused Products control access of the MLC and SLC nonvolatile memory elements and the random access volatile memory element for storage of the received data. For example, as explained in Count V above, the Accused Products include a controller that handles and controls reads and writes to and from both flash and volatile memory.

174. When used by Phison or its customers, the Accused Products transfer the stored received data from the controller memory to a given one of the MLC nonvolatile memory elements in an associated MLC memory module, operable to store the received data in the given one given one of the MLC nonvolatile memory element as stored data. For example, as explained in Count V above, the Accused Products include a controller memory, such as buffers or caches.

175. When used by Phison or its customers, the Accused Products retain the received data in the random access volatile memory as retained data associated with the stored data. For example, as explained in Count V above, the Accused Products include random access memory that retains stored data.

176. When used by Phison or its customers, the Accused Products perform a data integrity test on the stored data in the given one of the MLC nonvolatile memory elements in the associated one of the MLC memory modules after at least a Write access operation performed thereon. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data.

177. When used by Phison or its customers, the Accused Products' data integrity test includes reading the stored data to the controller memory. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data. The stored data would enter a controller memory, such as a buffer or cache, for the purposes of the comparison.

178. When used by Phison or its customers, the Accused Products' data integrity test includes comparing the stored data in the controller memory in the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller during the Write access operation. For example, as shown with respect to Count IV above, the Accused Products perform a data integrity test after data is written by comparing stored data and retained data. The stored data would enter a controller memory, such as a buffer or cache, for the purposes of the comparison.

179. When used by Phison or its customers, the Accused Products remap, responsive to a failure of the data integrity test performed on the stored data by the controller, the address space to a different physical range of addresses. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

180. When used by Phison or its customers, the Accused Products transfer data corresponding to the retained data to those remapped physical address from those physical

addresses determined to have failed the data integrity test. For example, as shown with respect to Count IV above, data is remapped when it fails the data integrity test after a comparison.

181. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

182. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

183. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '612 patent by Defendant.

COUNT VII: INFRINGEMENT OF U.S. PATENT NO. 11,967,369

184. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

185. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '369 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing activities, products, and services, including, for example, on the basis of information obtained during discovery.

186. Phison has also knowingly and intentionally induces infringement of one or more claims of the '369 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the '369 Patent and the infringing nature of the

Accused Products. Despite this knowledge of the ’369 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’369 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’369 Patent, thereby specifically intending for and inducing its customers to infringe the ’369 Patent through the customers’ normal and customary use of the Accused Products.

187. Phison has also infringed, and continues to infringe, one or more claims of the ’369 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’369 Patent, are especially made or adapted to infringe the ’369 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’369 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

188. On information and belief, despite having knowledge of the ’369 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement. Phison’s infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

189. The Accused Products meet all the limitations of at least claim 1 of the ’369 patent. Specifically, claim 1 of the ’369 patent recites:

> A memory system for storing data comprising:
>
> memory space containing logical and physical volatile memory space and nonvolatile memory space, wherein the logical and physical nonvolatile memory

space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;

a bank of physical nonvolatile memory, including:

a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space, and

at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space;

at least one random access volatile physical memory element that exists in the logical volatile memory space;

at least one controller to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements, the controller having a controller memory associated therewith for storing received data therein;

a flash translation layer (FTL), wherein the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements;

the controller controlling access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, operable to store the received data in the given one of the physical MLC nonvolatile memory elements as stored data and retain such received data in the random access volatile physical memory element as retained data associated with stored data;

the controller performing a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation;

> wherein the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime; and
>
> wherein a failure of the data integrity test performed on the stored data by the controller results in a remapping of logical address space to a different physical range of addresses in the physical address space and transfer of data corresponding to the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test.

190. To the extent the preamble is a limitation, the Accused Products include a memory system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

191. The Accused Products include memory space containing logical and physical volatile memory space and nonvolatile memory space. For example, as explained in Count IV above, the Accused Products include MLC and SLC memory (nonvolatile memory), as well as RAM (volatile memory). This memory is addressed in logical and physical space. For example, as explained in Count IV above, logical block numbers and other memory mappings are used by the controller, and physical memory space is used to map specific physical locations in memory. For example, as explained in Count IV above, host memory buffers are used to address volatile memory.

192. In the Accused Products, the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space. For example, as explained in Count IV above, the Accused Products include SLC and MLC memory space.

193. The Accused Products include a bank of physical nonvolatile memory. For example, as explained in Count I above, the Accused Products include SLC and MLC physical NAND flash memory. This may include memory configured to operate in SLC mode.

194. The Accused Products include a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element having a physical address within the physical MLC nonvolatile memory space that can be mapped to a logical address in the MLC logical nonvolatile memory space. For example, as explained in Count I above, the Accused Products include MLC NAND flash memory, with physical addresses that are mapped to logical addresses using a flash translation layer/L2P table.

195. The Accused Products include at least one SLC memory module including at least one physical SLC nonvolatile memory element having a physical address within the physical SLC nonvolatile memory space that can be mapped into the SLC logical nonvolatile memory space. For example, as explained in Count IV above, the Accused Products map physical nonvolatile memory space, addressed using physical addresses, into SLC logical nonvolatile memory space for addressing memory logically.

196. The Accused Products include at least one random access volatile physical memory element that exists in the logical volatile memory space. For example, as explained in Count IV above, the Accused Products include RAM. As explained in Count IV above, memory mappings and host memory buffer functionality provide a logical volatile memory space in which the RAM exists.

197. The Accused Products include at least one controller to operate physical memory elements and associated memory space for associated Write access operations to the physical memory elements and Read access operations from the physical memory elements. For example,

as explained in Count I above, the Accused Products include a controller that manages reads and writes to the physical memory elements.

198. In the Accused Products, the controller has a controller memory associated therewith for storing received data therein. For example, as explained in Count IV above, the Accused Products include RAM that is used by the controller for storing data.

199. The Accused Products include a flash translation layer (FTL). For example, as explained in Count II above, the Accused Products include a flash translation layer, implemented by hardware and software in the controller, that maps logical to physical addresses.

200. In the Accused Products, the at least one controller, or the FTL, or a combination of both maintain an address table in one or more of the physical memory elements. For example, as explained in Counts I and II above, the controller and/or FTL in the Accused Products use an L2P table or similar data structure to map logical addresses to physical addresses. This table may be stored in RAM for easy access, and is also stored in nonvolatile flash memory so that the mapping is maintained even when the device is powered down.

201. In the Accused Products, the controller controls access of the physical MLC and SLC nonvolatile memory elements and the random access volatile physical memory elements for storage of the received data therein as stored data. For example, as explained in Count IV above, the Accused Products have controllers which control the storage of data in both MLC and SLC memory, and use RAM to store data as well (for example as part of caching).

202. In the Accused Products, the controller, in at least a Write access operation transferring the stored received data from the controller memory to a given one of the physical MLC nonvolatile memory elements in an associated physical MLC memory module, stores the received data in the given one of the physical MLC nonvolatile memory elements as stored data

and retains such received data in the random access volatile physical memory element as retained data associated with stored data. For example, as explained in Count IV above, the Accused Products retain data in RAM when data is stored in flash memory, including MLC flash memory. They may retain data in a cache in RAM, and may also retain certain relevant data as part of the L2P tables stored in RAM.

203. In the Accused Products, the controller performs a data integrity test on stored data in the given one of the physical MLC nonvolatile memory elements in the associated one of the physical MLC memory modules after the at least a Write access operation performed thereon by reading the stored data to the controller memory and comparing the stored data in the controller memory in the given one of the physical MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile physical memory element by the controller during the Write access operation. For example, as explained in Count IV above, the Accused Products perform a variety of data integrity tests to ensure that data is stored correctly. These data integrity tests take advantage of the retained data to perform comparisons with data stored in MLC flash memory and detect errors after data is written.

204. In the Accused Products, the address table maps logical addresses to physical addresses of the memory system, wherein the mapping is performed as necessitated by the memory system to maximize lifetime. For example, as explained in Count IV above, the Accused Products' controllers employ wear leveling and garbage collection techniques that transfer blocks within the flash memory in a way that maximizes lifetime.

205. In the Accused Products, a failure of the data integrity test performed on the stored data by the controller results in a remapping of logical address space to a different physical range of addresses in the physical address space and transfer of data corresponding to

the retained data to those remapped physical addresses in the physical address space from those physical addresses in the physical address space determined to have failed the data integrity test. For example, as explained in Count IV above, the Accused Products remap data to new physical addresses after a data integrity test failure in the physical addresses where the data was originally stored. This data corresponds to the retained data.

206. For example, as explained in Counts I and IV above, the Accused Products include MLC NAND flash, and this flash is addressed in an MLC non-volatile memory space.

207. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

208. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

209. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '369 patent by Defendant.

COUNT VIII: INFRINGEMENT OF U.S. PATENT NO. 11,967,370

210. Vervain incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint as if fully set forth herein.

211. Phison has directly infringed and continue to infringe, either literally or under the doctrine of equivalents, at least claim 1 of the '370 patent by making, using, offer for sale, selling, and importing, without authority or license, the Accused Products in violation of 35 U.S.C. § 271(a). The Accused Products are non-limiting examples that were identified based on currently available information, and Vervain reserves the right to identify additional infringing

activities, products, and services, including, for example, on the basis of information obtained during discovery.

212. Phison has also knowingly and intentionally induces infringement of one or more claims of the ’370 Patent in violation of 35 U.S.C. § 271(b). Through at least the filing and service of this Complaint, and through the service of the subpoenas in the Micron and Western Digital cases, Phison has had knowledge of the ’370 Patent and the infringing nature of the Accused Products. Despite this knowledge of the ’370 Patent, Phison continues to actively encourage and instruct its customers and end users (for example, through user manuals and technical documentation) to use the Accused Products in ways that directly infringe the ’370 Patent. Phison does so knowing and intending that its customers and end users will commit these infringing acts. Phison also continues to make, use, offer for sale, sell, and/or import the Accused Products, despite its knowledge of the ’370 Patent, thereby specifically intending for and inducing its customers to infringe the ’370 Patent through the customers’ normal and customary use of the Accused Products.

213. Phison has also infringed, and continues to infringe, one or more claims of the ’370 Patent by selling, offering for sale, or importing into the United States, the Accused Products, knowing that the Accused Products constitute a material part of the inventions claimed in the ’370 Patent, are especially made or adapted to infringe the ’370 Patent, and are not staple articles or commodities of commerce suitable for non-infringing use. Phison has been, and currently is, contributorily infringing the ’370 Patent in violation of 35 U.S.C. §§ 271(c) and (f).

214. On information and belief, despite having knowledge of the ’370 Patent and knowledge that it is directly and/or indirectly infringing one or more of its claims, Phison has continued its infringing conduct and disregarded an objectively high likelihood of infringement.

Phison's infringing activities have been, and continued to be, willful, wanton, and deliberate, such that Vervain is entitled to enhanced damages under 35 U.S.C. ¶ 284.

215. The Accused Products meet all the limitations of at least claim 1 of the '370 patent. Specifically, claim 1 of the '370 patent recites:

> A system for storing data comprising:
>
> an MLC non-volatile memory space including at least one MLC non-volatile memory element;
>
> an SLC non-volatile memory module space including at least one SLC non-volatile memory element; and
>
> a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to:
>
> a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;
>
> b) determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data, and, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element.

216. To the extent the preamble is a limitation, the Accused Products include a system for storing data. For example, as explained in Count I above, the Accused Products are flash memory products for storing data.

217. The Accused Products include an MLC non-volatile memory space including at least one MLC non-volatile memory element. For example, as explained in Counts I and IV

above, the Accused Products include MLC NAND flash, and this flash is addressed in an MLC non-volatile memory space.

218. The Accused Products include an SLC non-volatile memory module space including at least one SLC non- volatile memory element. For example, as explained in Counts I and IV above, the Accused Products include SLC NAND flash, including flash memory configured to operate in SLC mode, and this flash is addressed in an SLC non-volatile memory space.

219. The Accused Products include a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element. For example, as explained in Count I above, the Accused Products have a controller that manages reads and writes to and from the physical memory elements.

220. In the Accused Products, the controller is adapted to maintain an address map of the MLC and SLC non-volatile memory spaces. For example, as explained in Count I above, the controller in the Accused Products maintains an address map, for example in an L2P table or similar structure, that maps logical address ranges to physical addresses in the MLC and SLC memory.

221. In the Accused Products, the address map comprises a list of logical address ranges accessible by a computer system. For example, as explained in Count I above, the L2P or similar table in the Accused Products includes a list of logical address ranges such as blocks and pages.

222. In the Accused Products, the list of logical address ranges has a minimum quanta of addresses. For example, as explained in Count I above, the Accused Products employ a

minimum quanta of addresses such as a block or page in the L2P table, and memory is mapped on a block or page granularity.

223. In the Accused Products, each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element. For example, as explained in Count I above, the table entries in the L2P or similar tables in the Accused Products map ranges of logical addresses to similar ranges of physical addresses in MLC or SLC NAND flash memory.

224. In the Accused Products, the controller is adapted to determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data. For example, as explained in Count I above, the Accused Products include controllers that incorporate defect and error management technology, that use a variety of data integrity tests to determine when there is a data integrity problem, including for data stored in MLC flash memory. As explained in Count IV above, these data integrity tests use received data retained at the controller.

225. In the Accused Products, in an event of such a failure, the controller remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element. For example, as explained in Count I above, the Accused Products, upon a data integrity failure, remap degraded

data to the next available location. As explained in Count I above, the Accused Products move data from MLC to SLC in such situations.

226. The foregoing allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Accused Products. Vervain reserves the right to modify this description, including, for example, on the basis of information about the Accused Products that it obtains during discovery.

227. Defendant's infringement has damaged and continues to damage Vervain in an amount yet to be determined, of at least a reasonable royalty.

228. This is an exceptional case. Vervain is entitled to attorneys' fees and costs under 35 U.S.C. § 285 as a result of the infringement of the '370 patent by Defendant.

229.

REQUEST FOR A JURY TRIAL

230. Vervain requests a jury trial of all issues in this action so triable.

PRAYER FOR RELIEF

WHEREFORE, Vervain respectfully requests:

A. That Judgment be entered that Defendant has infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents;

B. That Defendant has willfully infringed one or more claims of the Asserted Patents, literally and under the doctrine of equivalents;

C. That, in accordance with 35 U.S.C. § 283, Defendant and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Asserted Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the Accused Products;

D. An award of damages sufficient to compensate Vervain for Defendant's infringement under 35 U.S.C. § 284;

E. That the case be found exceptional under 35 U.S.C. § 285 and that Vervain be awarded its reasonable attorneys' fees;

F. Costs and expenses in this action;

G. An award of prejudgment and post-judgment interest; and

H. Such other and further relief as the Court may deem just and proper.

Dated: May 13, 2024.

Respectfully submitted,

/s/ Alan L. Whitehurst

Alan L. Whitehurst
D.C. Bar No. 484873
awhitehurst@McKoolSmith.com
Nicholas T. Matich
D.C. Bar No. 1024907
nmatich@McKoolSmith.com
Christopher P. McNett
D.C. Bar No. 1500360
cmcnett@McKoolSmith.com
MCKOOL SMITH, P.C.
1999 K Street, NW, Suite 600
Washington, DC 20006
Telephone: (202) 221-6267
Facsimile: (212) 402-9444

John Campbell
Texas Bar No. 24036314
James E. Quigley
Texas Bar No. 24075810
jquigley@McKoolSmith.com
MCKOOL SMITH, P.C.
303 Colorado Street, Suite 2100
Austin, TX 78701
Telephone: (512) 692-8700
Facsimile: (512) 692-8744

Jennifer L. Truelove
Texas Bar No. 24012906
jtruelove@mckoolsmith.com
MCKOOL SMITH, P.C.
104 East Houston, Suite 300
Marshall, Texas 75670
(903) 923-9000
Fax: (903) 923-9099

Attorneys for Plaintiff Vervain, LLC

CERTIFICATE OF SERVICE

The undersigned certifies that on May 13, 2024, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system.

/s/ Alan L. Whitehurst
Alan L. Whitehurst