UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	11/25/2014	8898395	TRAN-P602	7036

45590 7590 11/05/2014

Patent Prosecution Dept.
MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 466 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Guillermo J. Rozas, Los Gatos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Murabito, Hao & Barnes LLP
2 N. Market Street
3rd floor
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Katie Smith	(Depositor's name)
/Katie Smith/	(Signature)
10/21/2014	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$960	$0	$0	$960	10/22/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 504160 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Anthony C. Murabito/ Date 10/21/2014

Typed or printed name Anthony C. Murabito Registration No. 35295

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12121531
Filing Date:	15-May-2008
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	Anthony C. Murabito/Katie Smith
Attorney Docket Number:	TRAN-P602

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	20479729
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Anthony C. Murabito/Katie Smith
Filer Authorized By:	Anthony C. Murabito
Attorney Docket Number:	TRAN-P602
Receipt Date:	21-OCT-2014
Filing Date:	15-MAY-2008
Time Stamp:	19:01:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$960
RAM confirmation Number	5236
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	TRAN-P084C1_ISSUE_FEE_10-21-2014.pdf	86843 1276ef4f890087b4638d2307e69c69ac91267b51	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30350 f2e3e799278f5813ba9143d891ffa7e68f89b27f	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	117193	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

45590 7590 07/22/2014

Patent Prosecution Dept.
MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER
OTTO, ALAN

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/22/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

TITLE OF INVENTION: MEMORY MANAGEMENT FOR CACHE CONSISTENCY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/22/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

45590 7590 07/22/2014
Patent Prosecution Dept.
MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

TITLE OF INVENTION: MEMORY MANAGEMENT FOR CACHE CONSISTENCY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	10/22/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
OTTO, ALAN	2182	711-144000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 07/22/2014

Patent Prosecution Dept.
MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
OTTO, ALAN	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/22/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/121,531	Applicant(s) ROZAS, GUILLERMO J.	
	Examiner ALAN OTTO	Art Unit 2182	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment dated 6/30/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *33, 36-41, 44-50 and 52-57, renumbered claims 1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/A. O./
Examiner, Art Unit 2182

Detailed Action

The instant application having Application No. 12/121,531 has a total of 20 claims pending in the application; there are 4 independent claims and 16 dependent claims.

Reasons for Allowance

1. The reasons for allowance can be found below:

The following is an examiner's statement of reasons for allowance:

2. **Claim 33** recites the limitation of "executing a third group of instructions that causes said cache line to be accessed, wherein said third group of instructions is executed by an agent other than said processor, wherein said processing comprises rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, and otherwise granting access." This limitation is taught in the specification, pages 12-13. This limitation in combination with other recited limitations of claim 33 is not taught or suggested by the prior art of record. Claims 41, 49 and 56 contain similar limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

3. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER NO LONGER IN THE APPLICATION

4. Claims 1-32 were cancelled by the amendment dated 5/15/2008. Claims 34-35, 42-43 and 51 were canceled by the amendment dated 6/30/2014.

a(2) SUBJECT MATTER CONSIDERED ALLOWABLE

5. Per the instant office action, claims 33, 36-41, 44-50 and 52-57 are allowed, and renumbered claims 1-20.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN OTTO whose telephone number is (571)270-1626. The examiner can normally be reached on 11:00-7:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. O./
Examiner, Art Unit 2182
/MATTHEW BRADLEY/
Primary Examiner, Art Unit 2182

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BIB DATA SHEET

CONFIRMATION NO. 7036

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/121,531	05/15/2008	711	2182	TRAN-P602

APPLICANTS

INVENTORS

Guillermo J. Rozas, Los Gatos, CA;

**** CONTINUING DATA ********************** YES /A.O./ 7/12/14**

This application is a CON of 11/102,127 04/07/2005 PAT 7376798

**** FOREIGN APPLICATIONS ********************** NO /A.O./ 7/12/14**

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

06/03/2008

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ALAN OTTO/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	25	4

ADDRESS

Patent Prosecution Dept.
MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113
UNITED STATES

TITLE

MEMORY MANAGEMENT FOR CACHE CONSISTENCY

FILING FEE RECEIVED		
1490	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	**Art Unit**
	ALAN OTTO	2182

CPC						
Symbol					**Type**	**Version**
G06F		12	/	0815	F	2013-01-01
G06F		12	/	0806	A	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

/ALAN OTTO/ Examiner.Art Unit 2182	07/12/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MATTHEW BRADLEY/ Primary Examiner.Art Unit 2182	07/17/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	33	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	**Art Unit**
	ALAN OTTO	2182

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
711	144	G 0 6 F 12 / 00 (2006.0)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	141	143	145	130	133
710	22				
714	11	12			

/ALAN OTTO/ Examiner.Art Unit 2182	07/12/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MATTHEW BRADLEY/ Primary Examiner.Art Unit 2182	07/17/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	33	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	**Art Unit**
	ALAN OTTO	2182

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	33	17	54												
2	36	18	55												
3	37	19	56												
4	38	20	57												
5	39														
6	40														
7	41														
8	44														
9	45														
10	46														
11	47														
12	48														
13	49														
14	50														
15	52														
16	53														

/ALAN OTTO/ Examiner.Art Unit 2182	07/12/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/MATTHEW BRADLEY/ Primary Examiner.Art Unit 2182	07/17/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	33	1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	35	rozas-guillermo.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L2	8	US-6938130-$.DID. OR US-6263407-$.DID. OR US-6625694-$.DID. OR US-5428761-$.DID. OR US-5701432-$.DID. OR US-6658536-$.DID. OR US-5974438-$.DID. OR US-6006299-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L3	5	US-6189074-$.DID. OR US-6304944-$.DID. OR US-6738864-$.DID. OR US-6779085-$.DID. OR US-6839813-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L4	1335	(indicat$4 or mark$4) with read with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L5	2312	(indicat$4 or mark$4) with (read or access$3) with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L6	16181	711/130.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls. or 711/146.ccls. or 710/22.ccls. or 711/133-134.ccls. or 711/118.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L7	39269	g06f12/00.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L8	1242	L5 same (bit or tag or indicator)	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L9	38531	L7 or L6	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L10	687	L8 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L11	373	L5 same (bit or tag or indicator) same (application or process or transaction or thread or (group near3 instruction))	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:14
L12	209	L11 and L9	US-PGPUB; USPAT;	OR	ON	2014/07/12 16:14

			USOCR			
L13	1501	((transaction$3 near3 system) or (transaction$3 near3 memory)) same (cache adj line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L14	55	(L11 and L13) not L12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L15	5699	711/143.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L16	15972	valid adj (bit or tag or indicator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L17	5268	mesi or moesi	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L18	187	L15 and L16 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L19	90	shared with (read adj (miss or hit))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L20	3	L18 and L19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L21	700780	(compar$4 or check$4 or detect$4) with (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L22	1757	714/11-12.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT;	OR	ON	2014/07/12 16:14

			IBM_TDB			
L23	596	L21 and L22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L24	1172	711/130.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L25	0	L23 and L24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L26	61091	shared adj (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L27	6175	L26 same L21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L28	48	L27 and L23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L29	2	"7376798".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L30	21456	(dual or multi) adj core adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L31	429	L30 and ("same" adj die)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L32	137	L31 and coherency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT;	OR	ON	2014/07/12 16:14

			IBM_TDB			
L33	7	"10993757"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L34	17921	L6 or L22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L35	1970	g06f12/0815.cpc. or g06f12/0891.cpc. or g06f12/0806.cpc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L36	18831	L34 or L35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:14
L37	4396	(bit or tag or indicat$4 or mark$4) with (access$4 or read) with (cache adj line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:27
L38	215	(roll adj back or rollback) near instructions	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:27
L39	0	l38 same l37	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:27
L41	295	l37 and l35	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/07/12 16:28
L42	26	l11 and l35	US-PGPUB; USPAT; USOCR	OR	ON	2014/07/12 16:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L43	10329	711/130.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls. or 711/146.ccls. or 710/22.ccls. or 711/133-	USPAT; UPAD	OR	ON	2014/07/12 16:30

		134.ccls. or 711/118.ccls. or 714/11-12.ccls.				
L44	424	((bit or tag or indicat$4 or mark$4) with (access$4 or read) with (cache adj line)).clm.	USPAT; UPAD	OR	ON	2014/07/12 17:23
L45	278	((indicat$4 or mark$4) with (read or access$3) with (cache adj line)).clm.	USPAT; UPAD	OR	ON	2014/07/12 17:23
L46	29	((roll adj back or rollback) near instructions).clm.	USPAT; UPAD	OR	ON	2014/07/12 17:23
L47	0	l44 and l46	USPAT; UPAD	OR	ON	2014/07/12 17:23
L48	0	l45 and l46	USPAT; UPAD	OR	ON	2014/07/12 17:23
L49	0	l43 and l46	USPAT; UPAD	OR	ON	2014/07/12 17:24

7/ 12/ 2014 5:24:55 PM
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Your search for *((roll NEAR/4 back OR rollback) NEAR/4 instructions)* **AND** *((bit OR tag OR indicat[*4] OR mark[*4]) NEAR/8 (access[*4] OR read) NEAR/8 (cache NEAR/4 line))* found 0 results.
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s3 and s1

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S4	s3 and s1 **Databases:** Inspec®	Inspec®	**0** *	Actions
S3	(roll near back or rollback) near instructions **Databases:** Inspec®	Inspec®	**24** *	Actions
S2	(indicat$4 or mark$4) near/8 (read or access$3) near/8 (cache near line) **Databases:** Inspec®	Inspec®	**0** *	Actions
S1	(bit or tag or indicat$4 or mark$4) near/8 (access$4 or read) near/8 (cache near line) **Databases:** Inspec®	Inspec®	**21** *	Actions

* Duplicates are removed from your search and from your result count.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Updated East text search	7/12/14	AO
Inventor name search (Palm and East)	7/12/14	AO
711/130, 118, 133-134, 141, 144-146, 710/22, g06f12/00 (text search - see attached search results)	7/12/14	AO
g06f12/0815, g06f12/0891, g06f12/0806 (text search - see attached search results)	7/12/14	AO
Updated NPL search - Dialog	7/12/14	AO
Consulted with Matthew Bradley	7/12/14	AO

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	118, 133-134, 141, 144-146	7/12/14	AO
710	22	7/12/14	AO
714	11-12	7/12/14	AO

/A.O./ Examiner.Art Unit 2182	

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/121,531	ROZAS, GUILLERMO J.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 30 JUN 2014	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
JAB

U.S. Patent and Trademark Office

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	12121531	Filing Date	2008-05-15	Docket Number (if applicable)	TRAN-P084C1	Art Unit	2187
First Named Inventor	Guillermo ROZAS			Examiner Name	Alan OTTO		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____ (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 504160

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

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Signature of Registered U.S. Patent Practitioner			
Signature	/William A. Zarbis/	Date (YYYY-MM-DD)	2014-06-30
Name	William A. Zarbis	Registration Number	46120

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)		
	)		
Rozas	)	Examiner:	OTTO, A.
	)		
Serial No.: 12/121,531	)	Art Unit:	2187
	)		
Filed: May 15, 2008	)	Confirmation No.:	7036
	)		
For: MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)	)		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO DECISION ON APPEAL

Dear Sir:

In response to the Decision on Appeal mailed April 28, 2014, and per the Request for Continued Examination filed herewith, the Applicant respectfully requests further examination and reconsideration of the above captioned patent application in view of the following amendments and remarks. Amendments to the claims are presented beginning on page 2, and remarks begin on page 10.

AMENDMENTS TO THE CLAIMS

1-32. (Canceled).

33. (Currently Amended) A method of managing memory in a computer system, said method comprising:

setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; ~~and~~

setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions;

executing a third group of instructions that causes said cache line to be accessed, wherein said third group of instructions is executed by an agent other than said processor, wherein said processing comprises rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, and otherwise granting said access; and

processing said first group and said second group of instructions according to a value of said indicator.

34-35. (Canceled).

36. (Currently Amended) The method of Claim 33 [[35]] wherein said processing further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set, and then granting said access provided said cache line is in other than said shared state, and otherwise granting said access only when said cache line is in said shared state.

37. (Currently Amended) The method of Claim 33 [[35]] further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. (Original) The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. (Original) The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. (Original) The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. (Currently Amended) A computer system comprising:

a processor;

a cache memory for use by said processor; and

a memory unit coupled to said processor and having stored therein instructions, said instructions comprising:

instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read;

instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; ~~and~~

instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions;

instructions to execute a third group of instructions that causes said cache line to be accessed, wherein said third group of instructions is for execution by an agent other than said processor, wherein said instructions further comprise instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, wherein otherwise said access is granted; and

instructions to process said first group and said second group of instructions according to a value of said indicator.

42-43. (Canceled).

44. (Currently Amended) The computer system of Claim 41 [[43]] wherein said instructions further comprise:

instructions to determine a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set, wherein said access is granted provided said cache line is in other than said shared state, and wherein otherwise said access is granted only when said cache line is in said shared state.

45. (Previously Presented) The computer system of Claim 44 wherein said instructions further comprise instructions to maintain a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. (Previously Presented) The computer system of Claim 45 wherein said instructions further comprise instructions to eliminate one or more instructions from said first group of instructions if said first count exceeds a threshold and to eliminate one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise instructions to clear said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise:

instructions to execute a plurality of groups of instructions in parallel using said processor;

instructions to change an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

instructions to roll back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache

memory provided all cache lines in said cache memory are indicated as having been accessed, wherein otherwise said plurality of groups of instructions continue to be executed.

49. (Currently Amended) A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions with a processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions with said processor; ~~and~~

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions;

executing a third group of instructions that causes said cache line to be accessed; and

rolling back said first group of instructions and said second group of instructions before granting said access.

50. (Previously Presented) The method of Claim 49 wherein said first group of instructions includes multiple memory operations and said second group of instructions includes multiple memory operations.

51. (Canceled).

52. (Currently Amended) The method of Claim 49 [[51]] wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. (Currently Amended) The method of Claim 49 [[51]] further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. (Original) The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. (Original) The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. (Currently Amended) A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of indicator bits per cache line, wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended;

wherein further, in response to an agent other than said processor executing a third group of instructions that causes said cache line to be accessed, said first group of instructions is rolled back provided said first bit is set and said second group of instructions is rolled back provided said second bit is set before allowing an instruction in said third group to access said cache line, wherein otherwise said access is granted.

57. (Previously Presented) The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an entry in said memory unit, wherein an indicator bit of said entry is set in response to said cache line being accessed.

REMARKS

The Office Action mailed August 26, 2010, and the Advisory Action mailed October 29, 2010, were the last Office Actions issued prior to the Decision on Appeal. According to those Office Actions, Claims 33-57 stand rejected on the ground of non-statutory obviousness-type double patenting; Claims 33, 34, 39, 41, 42, 47, 49, 50, 55, 56, and 57 stand rejected under 35 U.S.C. § 103(a), as more fully described below; and Claims 35-38, 40, 43-46, and 51-54 are allowable if written in independent form once the double patenting rejection is overcome.

Applicant thanks the Examiner for indicating the allowability of Claims 35-38, 40, 43-46, and 51-54.

Please cancel Claims 34, 35, 42, 43, and 51 without prejudice. Claims 33, 36-41, 44-50, and 52-57 are pending. Claims 33, 36, 37, 41, 44, 49, 52, 53, and 56 are amended.

Double Patenting

Remaining Claims 33, 36-41, 44-50, and 52-57 stand rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over U.S. Patent No. 7,376,798. A terminal disclaimer is filed along with this response, thereby overcoming the double patenting rejection.

§ 103 Rejections

Claims 33, 39, 41, 47, 56, and 57

Claims 33, 39, 41, 47, 56, and 57 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray et al. ("Gray;" U.S. Patent No. 5,086,429) in view of Hady et al. ("Hady;" U.S. Patent Application Publication No. 2006/0112226).

Claim 33 is amended to incorporate the subject matter of allowable Claim 35 and intervening Claim 34. Claim 33 is therefore in condition for allowance, and Claim 39 is also in condition for allowance because of its dependence on Claim 33. Therefore, a discussion of the rejection of Claims 33 and 39 under 35 U.S.C. § 103(a) is rendered moot at this time.

Claim 41 is amended to incorporate the subject matter of allowable Claim 43 and intervening Claim 42. Claim 41 is therefore in condition for allowance, and Claim 47 is also in condition for allowance because of its dependence on Claim 41. Therefore, a discussion of the rejection of Claims 41 and 47 under 35 U.S.C. § 103(a) is rendered moot at this time.

With regard to Claim 56, Applicant respectfully submits that neither Gray nor Hady nor the combination thereof teaches or suggests the features included in the amendment to that claim, namely "in response to an agent other than said processor executing a third group of instructions that causes said cache line to be accessed, said first group of instructions is rolled back provided said first bit is set and said second group of instructions is rolled back provided said second bit is set before allowing an instruction in said third group to access said cache line,

wherein otherwise said access is granted." Both of those references are silent with regard to the recited features. Thus, Claim 56 overcomes the basis for rejection under 35 U.S.C. § 103(a) and is in condition for allowance, and Claim 57 is in condition for allowance at least because of its dependence on an allowable claim.

Claims 49, 50, and 55

Claims 49, 50, and 55 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray and Hady in view of Examiner's official notice.

Claim 49 is amended to incorporate the subject matter of allowable Claim 51. Claim 49 is therefore in condition for allowance, and Claims 50 and 55 are also in condition for allowance because of their dependence on Claim 49. Therefore, a discussion of the rejection of Claims 49, 50, and 55 under 35 U.S.C. § 103(a) is rendered moot at this time.

Conclusions

In light of the above amendments and remarks, Applicant respectfully requests reconsideration of the rejected claims.

Based on the amendments and arguments presented above, Applicant respectfully asserts that pending Claims 33, 36-41, 44-50, and 52-57 overcome the rejections of record, and therefore Applicant respectfully solicits allowance of those claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Date: June 30, 2014

/William A. Zarbis/

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San Jose, California 95113
Phone: (408) 938-9080 Ext. 113

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Rozas

Application No./Patent No.: 12/121,531 Filed/Issue Date: May 15, 2008

Titled: Memory Management for Cache Consistency

Intellectual Venture Funding LLC , a LLC

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

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The document was recorded in the United States Patent and Trademark Office at
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2. From: Transmeta Corporation To: Transmeta LLC

The document was recorded in the United States Patent and Trademark Office at
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3. From: Transmeta LLC To: Intellectual Venture Funding LLC

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/WILLIAM A. ZARBIS/ June 30, 2014

Signature Date

William A. Zarbis Agent

Printed or Typed Name Title

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) TRAN-P084C1

In re Application of: Rozas

Application No.: 12/121,531

Filed: May 15, 2008

For: Memory Management for Cache Consistency

The owner*, Intellectual Venture Funding LLC, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,376,798 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 46,120

/WILLIAM A. ZARBIS/ — Signature
June 30, 2014 — Date

WILLIAM A. ZARBIS — Typed or printed name

408-938-9060 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Electronic Patent Application Fee Transmittal	
Application Number:	12121531
Filing Date:	15-May-2008
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	William A. Zarbis/Arann Capri
Attorney Docket Number:	TRAN-P602
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1200**

Electronic Acknowledgement Receipt

EFS ID:	19460644
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Arann Capri
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	30-JUN-2014
Filing Date:	15-MAY-2008
Time Stamp:	20:12:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1200
RAM confirmation Number	9658
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Request for Continued Examination (RCE)	TRAN-P084C1_RCE_06-30-2014.pdf	697959 9b81a616636c40ef11ec019210fb0c7a863a9fd8	no	3
Warnings:					
Information:					
2		TRAN-P084C1_RESPONSE_AFTER_APPEAL_DECISION_06-30-2014.pdf	64052 fc6f4039950c9bd208f0f49e4dc37594102ede6a	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	13

Warnings:					
Information:					
3	Assignee showing of ownership per 37 CFR 3.73.	TRAN-P084C1_STATEMENT_UNDER_37-3-B_06-30-2014.pdf	429491 3613d0bdbf574dac252359d315bddd5814d648e4	no	2
Warnings:					
Information:					
4	Terminal Disclaimer Filed	TRAN-P084C1_TERMINAL_DISCLAIMER_06-30-2014.pdf	210121 9f212de4e334b136b676d8cc8f0e4afd734a1fea	no	2
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30307 02c3fa59075549f3bad81ee8841b4c026bb8d16d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1431930		

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Electronic Patent Application Fee Transmittal	
Application Number:	12121531
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First Named Inventor/Applicant Name:	Guillermo J. Rozas
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Attorney Docket Number:	TRAN-P602
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
		Total in USD ($)		**160**

Electronic Acknowledgement Receipt

EFS ID:	19460716
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Arann Capri
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	30-JUN-2014
Filing Date:	15-MAY-2008
Time Stamp:	20:20:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$160
RAM confirmation Number	9738
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Fee Worksheet (SB06)	fee-info.pdf	30321 457188ef6fec3e59eddabf308fe39b43e2555c9a	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	30321	

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New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/121,531	Filing Date 05/15/2008	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **06/30/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 25	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TAMMY d. MCBETH BROWN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 04/28/2014

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EXAMINER	
OTTO, ALAN	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
04/28/2014	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte GUILLERMO J. ROZAS[1]

Appeal 2011-011495
Application 12/121,531
Technology Center 2100

Before CAROLYN D. THOMAS, ELENI MANTIS MERCADER, and JASON V. MORGAN, *Administrative Patent Judges*.

MORGAN, *Administrative Patent Judge*.

DECISION ON APPEAL

Introduction

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 33–57. Claims 1–32 are canceled. App. Br. 1. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

---

[1] Intellectual Venture Funding LLC is the Real Party in Interest. App. Br. 1.

Invention

Appellant invented "[m]ethods and systems for maintaining cache consistency." Abstract.

Exemplary Claim

Claim 33, reproduced below with key limitations emphasized, is representative:

> 33. A method of managing memory in a computer system, said method comprising:
>
> setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to *a processor executing an instruction in a first group of instructions*; and
>
> setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to *said processor executing an instruction in a second group of instructions*.

Rejections

The Examiner rejects claims 33–57 under a non-statutory obviousness-type double patenting rejection as being unpatentable over claims in U.S. Patent 7,376,798 B1.[2] Fin. Rej. 3–4; Ans. 2.

The Examiner rejects claims 33, 34, 39, 41, 42, 47, 56, and 57 under 35 U.S.C. § 103(a) as being unpatentable over Gray (U.S. 5,086,429) and Hady (U.S. App. No. 2006/0112226 A1). Ans. 4–10.

[2] Appellant acknowledges the non-statutory obviousness-type double patenting rejection, but fails to address its merits. App. Br. 1. Accordingly, we *pro forma* affirm this rejection.

The Examiner rejects claims 49, 50, and 55 under 35 U.S.C. § 103(a) as being unpatentable over Gray, Hady, and the Examiner's taking of Official Notice. Ans. 10–13.

ISSUE

Did the Examiner err in finding the combination of Gray and Hady teaches or suggests "a processor executing an instruction in a first group of instructions" and "said processor executing an instruction in a second group of instructions," as recited in claim 33?

ANALYSIS

We only consider those arguments that Appellant actually raises in the Briefs. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2008). Arguments in the Reply Brief that could have been presented in the Appeal Brief to rebut rejections made in the Final Office Action are waived and are not considered. *See Ex parte Borden*, 93 USPQ2d 1473, 1474 (BPAI 2010) (informative decision) ("[T]he reply brief [is not] an opportunity to make arguments that could have been made in the principal brief on appeal to rebut the Examiner's rejections, but were not." (Quotations omitted)).

The Examiner finds Gray teaches most of the recitations of claim 33, including processor execution of a first and second group of instructions. Ans. 4–5. However, the Examiner finds that Gray does not disclose "where the same processor executes both the first and second group of instructions." *Id.* at 5. That is, Gray has a first processor that executes a first group of instructions and a second processor that executes a second group of instruction. Therefore, the Examiner further relies on Hady, which discloses "a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs." *Id.* (citing Hady

¶¶ 0022–23). The Examiner concludes that it would have been obvious to an artisan of ordinary skill to modify Gray to have the same processor execute both a first group of instructions (in a first core of the processor) and a second group of instructions (in a second core of the same processor). Ans. 5 (citing Hady ¶ 0017).

Appellant contends the Examiner erred because "Gray relies on a pair of redundant processors for error detection." App. Br. 12. Appellant argues "[i]f the same processor is used as suggested in the final rejection, then Gray's principle of operation (two processors that simultaneously execute the same instructions) would be changed, and Gray would be rendered unsatisfactory for its intended purpose (error detection)." *Id.* at 13.

Appellant's argument is not persuasive of error because, as the Examiner correctly notes, modifying Gray "would allow the same processor to execute both groups of instructions, but because *a separate core* inside the processor is executing each group, Gary's intended purpose would remain. *Each processor core* would be able to error check effectively while still remaining inside the same processor." Ans. 15 (emphases added). In other words, modifying Gray by using processor cores on a single processor, rather than multiple processors, would still allow for error checking of the processor cores. Thus, the proposed modification would not render Gray's system unsatisfactory for the intended purpose of error checking.

Each processor core in Gray, as modified, would execute its own copy of the instructions. That is, the first core of the processor would execute instructions in a first group of instructions (the first core's copy) while the second core of the processor would execute instructions in a second group of instructions (the second core's copy). Therefore, we agree with the

Examiner the combination of Gray and Hady teaches or suggests "a processor executing an instruction in a first group of instructions" and "said processor executing an instruction in a second group of instructions," as recited in claim 33. Ans. 4–5.

Accordingly, we sustain the Examiner's 35 U.S.C. § 103(a) rejection of claim 33, and of claims 34, 39, 41, 42, 47, 49, 50, and 55–57, which Appellant does not argue separately with sufficient specificity. App. Br. 13–15.

DECISION

We affirm the Examiner's decision to reject claims 33–57.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 41.50(f).

AFFIRMED

ELD

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 07/29/2011

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EXAMINER	
OTTO, ALAN	
ART UNIT	**PAPER NUMBER**
2187	
MAIL DATE	**DELIVERY MODE**
07/29/2011	PAPER

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SAN JOSE, CA 95113

Appeal No: 2011-011495
Application: 12/121,531
Appellant: Guillermo J. Rozas

Board of Patent Appeals and Interferences
Docketing Notice

Application 12/121,531 was received from the Technology Center at the Board on July 25, 2011 and has been assigned Appeal No: 2011-011495.

In all future communications regarding this appeal, please include both the application number and the appeal number.

The mailing address for the Board is:

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The facsimile number of the Board is 571-273-0052. Because of the heightened security in the Washington D.C. area, facsimile communications are recommended. Telephone inquiries can be made by calling 571-272-9797 and referencing the appeal number listed above.

By order of the Board of Patent Appeals and Interferences.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 07/27/2011

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EXAMINER	
OTTO, ALAN	
ART UNIT	PAPER NUMBER
2187	
MAIL DATE	DELIVERY MODE
07/27/2011	PAPER

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12/121,531	15 May, 2008	ROZAS, GUILLERMO J.	TRAN-P602

Patent Prosecution Dept.
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ART UNIT	PAPER
2187	20110721

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Commissioner for Patents

The reply brief filed 6/13/2011 has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

/Kevin L Ellis/ Supervisory Patent Examiner, Art Unit 2187	/A. O./ Examiner, Art Unit 2187

PTO-90C (Rev.04-03)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:			
	Rozas	Examiner:	OTTO, A.
Serial No.:	12/121,531	Art Unit:	2187
Filed:	May 15, 2008	Confirmation No.:	7036
For:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)		

REPLY BRIEF

This Reply Brief is in response to the Examiner's Answer mailed April 11, 2011, which was in response to the Appeal Brief filed January 24, 2011.

REMARKS

In these remarks, the Appellant is responding to certain arguments presented in the Examiner's Answer. Although only certain arguments are addressed in this Reply Brief, this should not be construed that the Appellant agrees with the other arguments presented in the Examiner's Answer (those other arguments have been addressed in the Appeal Brief).

Two references are cited in the final rejection: Gray and Hady. As understood by the Appellant, on a read operation, Gray's syndrome generators 24 and 25 do not generate check bits as stated on page 4 of the Examiner's Answer, but actually generate two eight-bit syndromes (one per syndrome generator) based on a check bit read from memory and a check bit generated by code generator 23, as described in column 8, lines 54-60, of Gray. According to the final rejection and the Examiner's Answer (pages 4-5), "[w]hen both syndromes are generated, it would indicate that both groups of instructions from processor 1A and processor 1B have read the cache line." Thus, it would appear that, as interpreted in the Examiner's Answer, operation of the Gray/Hady processor (consisting of Gray's processors 1A and 1B, if indeed Gray and Hady can be combined) generates a first eight-bit syndrome and a second eight-bit syndrome as a result of a first read operation that perhaps accesses a particular cache line and a second read operation that perhaps accesses the same cache line, and that the generation of both syndromes "would indicate that both groups of instructions from processor 1A and processor 1B have read the cache line."

However, Appellant finds no teaching within Gray and Hady of the specific features recited in the claims. That is, Appellant finds no teaching within Gray and Hady that associates a syndrome with a cache line, no teaching within Gray and Hady that associates the value of a bit in a syndrome with whether an instruction has been

executed that causes the particular cache line to be accessed, and no teaching within Gray and Hady that associates one bit in a syndrome with an instruction in a first group of instructions and associates another bit in the syndrome with an instruction in a second group of instructions. Thus, Appellant submits that Gray and Hady, even if they could be combined, do not teach or suggest, for example, an indicator associated with a cache line, where one bit of such an indicator is set if that cache line has been accessed in response to execution of an instruction in a first group of instructions and another bit of that same indicator is set (while the first bit remains set) if that same cache line has also been accessed in response to execution of an instruction in a second group of instructions.

More specifically, Appellant submits that Gray and Hady, even if they can be combined, do not teach or suggest "setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions" as recited in independent Claim 33 (emphases added). Similarly, Appellant submits that Gray and Hady do not teach or suggest "instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read; instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read; instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions"

as recited in independent Claim 41; or "wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions …, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group" as recited in independent Claim 56.

Also, independent Claim 33, for example, recites a first group of instructions and a second group of instructions. Gray teaches "[e]ach processor in each pair … is made to simultaneously execute the same program of instructions" (column 3, lines 57-60; emphasis added). Therefore, Appellant submits that Gray does not teach or suggest the claimed first and second groups of instructions. Hady teaches "multi-threaded operation" (paragraph [0011]), but appears to be silent with regard to the nature of the threads. Thus, Appellant submits that Hady, if combinable with Gray, does not teach or suggest a modification to Gray that remedies the deficiencies of Gray with regard to the claimed first and second groups of instructions.

In summary, in light of the above remarks as well as the arguments presented in the Appeal Brief, Appellants respectfully request that the rejection of Claims 33, 34, 39, 41, 42, 47, 49, 50, and 55-57 be reversed.

Respectfully submitted,
MURABITO HAO & BARNES LLP

Date: June 13, 2011

/William A. Zarbis/

William A. Zarbis
Registration No.: 46,120

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The time period for reply, if any, is set in the attached communication.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 12/121,531
Filing Date: May 15, 2008
Appellant(s): ROZAS, GUILLERMO J.

William A. Zarbis
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/24/2011 appealing from the Office action mailed 8/26/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-32 are canceled. Claims 33-57 are pending. Claims 33-57 are rejected on the ground on non-statutory obviousness-type double patenting. Claims 33-34, 39, 41-42, 47, 49-50 and 55-57 are rejected under 35 U.S.C. 103(a). Claims 35-38, 40, 43-46 and 51-54 would be allowable if the double patenting rejection is overcome and if rewritten in independent form.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(**5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(**8) Evidence Relied Upon**

5,086,429	Gray	2-1992
2006/0112226	Hady et al.	11-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 33-34, 39, 41-42, 47 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (U.S. Patent No. 5,086,429), herein referred to as Gray et al. in view of Hady et al. (U.S. Patent Application Publication No. 2006/0112226), herein referred to as Hady et al.

5. Referring to claim 33, Gray et al. disclose as claimed, a method of managing memory in a computer system, said method comprising: setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to a said processor executing an instruction in a second group of instructions. (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both**

syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

6. As to claim 34, Gray et al. also disclose the method of Claim 33 further comprising: executing a third group of instructions that causes said cache line to be accessed; and processing said first group and said second group of instructions

according to a value of said indicator (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

7. As to claim 39, Gray et al. also disclose the method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

8. Referring to claim 41, Gray et al. disclose as claimed, a computer system comprising: a processor; a cache memory used by said first processor; and a memory unit coupled to said processor and having stored therein instructions, said instructions comprising: instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read; instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read; instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the**

address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor

system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

9. As to claim 42, Gray et al. also disclose the computer system of Claim 41 wherein said instructions further comprise: Instructions to execute a third group of instructions that causes said cache line to be accessed; and instructions to process said first group and said second group of instructions according to a value of said indicator (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

10. As to claim 47, Gray et al. also disclose the computer system of Claim 41 wherein said instructions further comprise instructions to clear said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

11. Referring to claim 56, Gray et al. disclose as claimed, a computer system comprising: a processor; a cache memory coupled to said processor and having a plurality of cache lines; and a memory unit coupled to said processor, wherein said memory unit has a plurality of indicator bits per cache line, wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions

and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line. Also see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

12. As to claim 57, Gray et al. also disclose the computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an entry in said memory unit wherein an indicator bit of said entry is set in response to said cache line being accessed (**see col. 9, lines 12-18, where checkers 28 and 29 compare the address bits from the processors, and if there is a miscompare, then fail flags are set**).

13. Claims 49-50 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. in view of Hady et al. and in view of the examiner taking official notice.

14. Referring to claim 49, Gray et al. disclose as claimed, a method of managing shared memory in a computer system, said method comprising: executing a first group of instructions on a first processor; associating a second state with said cache line during said executing of said first group of instructions, wherein said second state

indicates that said cache line has been accessed because of said first group of instructions; executing a second group of instructions on said first processor; associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line**).

Gray et al. disclose the claimed invention except for associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and where the same processor executes both the first and second group of instructions.

However, using a cache coherency protocol such as MESI is well known in the art. MESI is used to allow multiprocessor systems to keep track of the states of cache lines in order to have an efficient cache coherent system. It would be obvious to employ such a system with Gray et al. in a multiprocessor system.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise associating a first state with a

cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state, in order to have cache coherency in a multi-processor system, allowing the caches in a multi-processor system to be identical or to be controlled and kept track of.

Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

15. As to claim 50, Gray et al. also disclose the method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations

(**see col. 3, lines 62-68 and col. 4, lines 1-10, where each memory access is checked. There would be multiple memory operations in a group of instructions, thread, or program running on the processors**).

16. As to claim 55, Gray et al. also disclose the method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

(10) Response to Argument

Appellant contends with respect to claim 33 that Gary and Hady do not teach or suggest “setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions.”

Appellant argues that Hady cannot be combined with Gray to teach "where the same processor executes both the first and second group of instructions." Appellant argues that Gray relies on two separate processors to simultaneously execute

instructions for error detection and therefore the same processor is not executing both groups of instructions. Each processor pair is made to execute the same program and compare error checking results in order to detect an error. Appellant argues that if Hady were combined with Gary and the same processor is used to run two error detection routines, then Gary would be rendered unsatisfactory for its intended purpose because it wouldn't be able to check the other processor's work.

However, Hady can be applied to Gary and still be used for its intended purpose. Appellant described the operation of Gary correctly. Gary uses two separate processors to check for errors. Each processor generates read and check bits for groups of instructions. These bits would act as indicators that are set in response to the processor executing that group of instructions. Claim 33 requires that the same processor execute both groups of instructions. Gary uses two separate processors to execute two groups of instructions. However, Hady is being combined with Gary so that the combination will allow a single processor to execute both groups of instructions.

Appellant's arguments appear to be directed toward a single processor with a single core. However, Hady is directed toward a single processor with multiple cores or a multi-core processor. Hady explains in para. 17 that a conventional system, such as Gary, would have multiple processors on separate silicon. A multi-core processor system, such as Hady, utilizes separate processor cores on the same die as the cache, allowing it to share data more efficiently. Para. 17 explains the advantages of a multi-core system. Each core in a multi-core processor can execute separate threads simultaneously, as explained in para. 11. Dual and multi-core processors are well

known in the art. With them, a single processor can execute multiple programs at the same time by using multiple cores to execute programs. It would be obvious to take the system of Gary which uses two separate processors to run two programs at the same time in order to check for errors, and implement it using a multi-core processor, where the two separate cores would be able to run programs simultaneously to check for errors. This would allow the same processor to execute both groups of instructions, but because a separate core inside the processor is executing each group, Gary's intended purpose would remain. Each processor core would be able to error check effectively while still remaining inside the same processor.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ALAN OTTO/

Examiner, Art Unit 2187

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/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187

/Brian R. Peugh/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:			
	Rozas	Examiner:	OTTO, A.
Serial No.:	12/121,531	Art Unit:	2187
Filed:	May 15, 2008	Confirmation No.:	7036
For:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)		

APPEAL BRIEF

Docket No.: TRAN-P084C1 (2279USCN159990)
Serial No.: 12/121,531

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1. Real Party in Interest

The real party in interest is Intellectual Venture Funding LLC.

2. Related Appeals and Interferences

There are no related appeals or interferences known to the Appellant.

3. Status of Claims

Claims 1-32 are canceled. Claims 33-57 are pending. Claims 35-38, 40, 43-46, and 51-54 are allowable. Claims 33-57 are rejected on the ground of non-statutory obviousness-type double patenting, and Claims 33, 34, 39, 41, 42, 47, 49, 50, and 55-57 are rejected under 35 U.S.C. § 103(a).

4. Status of Amendments

Claim 41 was amended in response to the final rejection that was mailed on August 26, 2010. That amendment was entered.

5. Summary of Claimed Subject Matter

Please note that while the discussion below associates portions of the specification with the claim recitations, the discussion does not necessarily equate the claim recitations with those portions. Rather, the discussion below is intended to show where support exists in the specification for embodiments within the scope of the claim recitations.

Independent Claim 33 pertains to a method of managing memory in a computer system (5; Figure 1). A first bit (24; Figure 2) of an indicator associated with a cache line (21; Figure 2) in a cache memory (14; Figures 1 and 2) is set if the

cache line has been accessed in response to a processor (10; Figure 1) executing an instruction in a first group of instructions (A; Figure 2). A second bit (25; Figure 2) of the indicator is set while the first bit remains set if the cache line has also been accessed in response to the processor executing an instruction in a second group of instructions (B; Figure 2). Please refer to page 10, lines 1-19; page 14, line 22, through page 15, line 15; and Figure 3, blocks 31-33.

According to Claim 34 (dependent on Claim 33), a third group of instructions, that causes the cache line to be accessed, is executed. The first group and the second group of instructions are processed according to a value of the indicator. Please refer to page 11, line 25, through page 12, line 16.

According to Claim 35 (dependent on Claim 34), the third group of instructions is executed by an agent (11; Figure 1) other than the processor. The processing comprises rolling back the first group of instructions provided the first bit is set and rolling back the second group of instructions provided the second bit is set before allowing an instruction in the third group to access the cache line; otherwise, the access is granted. Please refer to page 12, lines 6-16; page 16, line 20, through page 17, line 7; and Figure 4, blocks 43 and 44.

According to Claim 36 (dependent on Claim 35), the processing further comprises determining a state of the cache line, where the state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state. Also, the processing comprises rolling back the first group of instructions provided the first bit is set and rolling back the second group of instructions provided the second bit is set, and then granting the access

provided the cache line is in other than the shared state; otherwise, the access is granted only when the cache line is in the shared state. Please refer to page 13, lines 4-11; page 16, lines 14-16 and 20-22; and Figure 4, blocks 42 and 43.

According to Claim 37 (dependent on Claim 35), a first count of how many times the first group of instructions has been rolled back and a second count of how many times the second group of instructions has been rolled back are maintained. Please refer to page 13, lines 24-26; page 17, lines 9 and 10; and Figure 4, block 45.

According to Claim 38 (dependent on Claim 37), one or more instructions are eliminated from the first group of instructions if the first count exceeds a threshold, and one or more instructions are eliminated from the second group of instructions if the second count exceeds the threshold. Please refer to page 14, lines 2-7; page 17, lines 10-15; and Figure 4, block 45.

According to Claim 39 (dependent on Claim 33) the first bit is cleared when the execution of the first group of instructions is ended; the second bit remains set until execution of the second group of instructions is ended. Please refer to page 11, lines 1-7.

According to Claim 40 (dependent on Claim 33), a plurality of groups of instructions are executed in parallel. An indicator, associated with each cache line in the cache that has been accessed because of an instruction in any of the plurality of groups of instructions, is changed. Provided all cache lines in the cache memory are indicated as having been accessed, a group of instructions, that includes an

instruction that when executed attempts to replace information in a cache line of the cache memory, is rolled back. Otherwise, execution of the plurality of groups of instructions is continued. Please refer to page 18, lines 4-21, and Figure 5, blocks 51-54.

Independent Claim 41 pertains to a computer system (5; Figure 1) comprising a processor (10; Figure 1), a cache memory (14; Figures 1 and 2) for use by the processor, and a memory unit (18; Figure 1) having instructions stored therein. The instructions comprise instructions to execute a first group of instructions (A; Figure 2) using the processor, where the first group of instructions includes an instruction that causes a cache line (21; Figure 2) of the cache memory to be read. The instructions also comprise instructions to set a first bit (24; Figure 2) of an indicator associated with the cache line to indicate that the cache line has been read. The instructions also comprise instructions to execute a second group of instructions (B; Figure 2) using the processor, where the second group of instructions includes an instruction that causes the cache line to be read. The instructions also include instructions to set a second bit (25; Figure 2) of the indicator while the first bit remains set to indicate the cache line has been accessed by both the first group of instructions and the second group of instructions. Please refer to page 14, line 22, through page 15, line 15, and Figure 3, blocks 31-33.

According to Claim 42 (dependent on Claim 41), the instructions further comprise instructions to execute a third group of instructions that causes the cache line to be accessed, and instructions to process the first group and the second group of instructions according to a value of the indicator. Please refer to page 11, line 25, through page 12, line 16.

According to Claim 43 (dependent on Claim 42), the third group of instructions is for execution by an agent other than the processor. The instructions further comprise instructions to roll back the first group of instructions provided the first bit is set and to roll back the second group of instructions provided the second bit is set before allowing an instruction in the third group to access the cache line; otherwise, the access is granted. Please refer to page 12, lines 6-16; page 16, line 20, through page 17, line 7; and Figure 4, blocks 43 and 44.

According to Claim 44 (dependent on Claim 43), the instructions further comprise instructions to determine a state of the cache line, wherein the state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state. The instructions also comprise instructions to roll back the first group of instructions provided the first bit is set and to roll back the second group of instructions provided the second bit is set, where the access is granted provided the cache line is in other than the shared state; otherwise, the access is granted only when the cache line is in the shared state. Please refer to page 13, lines 4-11; page 16, lines 14-16 and 20-22; and Figure 4, blocks 42 and 43.

According to Claim 45 (dependent on Claim 44), the instructions further comprise instructions to maintain a first count of how many times the first group of instructions has been rolled back and a second count of how many times the second group of instructions has been rolled back. Please refer to page 13, lines 24-26; page 17, lines 9 and 10; and Figure 4, block 45.

According to Claim 46 (dependent on Claim 45), the instructions further comprise instructions to eliminate one or more instructions from the first group of instructions if the first count exceeds a threshold and to eliminate one or more instructions from the second group of instructions if the second count exceeds the threshold. Please refer to page 14, lines 2-7; page 17, lines 10-15; and Figure 4, block 45.

According to Claim 47 (dependent on Claim 41), the instructions further comprise instructions to clear the first bit when the execution of the first group of instructions is ended, where the second bit remains set until execution of the second group of instructions is ended. Please refer to page 11, lines 1-7.

According to Claim 48 (dependent on Claim 41), the instructions further comprise instructions to execute a plurality of groups of instructions in parallel using the processor. The instructions also comprise instructions to change an indicator associated with each cache line in the cache memory that has been accessed because of an instruction in any of the plurality of groups of instructions. The instructions also comprise instructions to roll back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of the cache memory provided all cache lines in the cache memory are indicated as having been accessed; otherwise, the plurality of groups of instructions continue to be executed. Please refer to page 18, lines 4-21, and Figure 5, blocks 51-54.

Independent Claim 49 pertains to a method of managing shared memory in a computer system (5; Figure 1). A first group of instructions (A; Figure 2) is

executed with a processor (10; Figure 1). A first state (23; Figure 2) is associated with a cache line (21; Figure 2) in a cache (14; Figures 1 and 2) comprising a plurality of cache lines, where the first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state. A second state (24; Figure 2) is associated with the cache line during the executing of the first group of instructions, where the second state indicates that the cache line has been accessed because of the first group of instructions. A second group of instructions (B; Figure 2) is executed with the processor. A third state (25; Figure 2) is associated with the cache line during the executing of the second group of instructions, where the third state indicates that the cache line has been accessed because of the second group of instructions. Please refer to page 10, lines 1-19; page 14, line 22, through page 15, line 15; and Figure 3, blocks 31-33. Please also refer to page 13, lines 4-11; page 16, lines 14-16 and 20-22; and Figure 4, blocks 42 and 43.

According to Claim 50 (dependent on Claim 49), the first group of instructions includes multiple memory operations and the second group of instructions includes multiple memory operations. Please refer to page 8, lines 3 and 4.

According to Claim 51 (dependent on Claim 49), a third group of instructions, that causes the cache line to be accessed, is executed. The first group of instructions and the second group of instructions are rolled back before granting the access. Please refer to page 11, line 25, through page 12, line 16; page 16, line 20, through page 17, line 7; and Figure 4, blocks 43 and 44.

According to Claim 52 (dependent on Claim 51), the rolling back is only performed provided the cache line is in other than the shared state. Please refer to page 16, lines 16-18.

According to Claim 53 (dependent on Claim 51), a first count of how many times the first group of instructions is rolled back and a second count of how many times the second group of instructions is rolled back are maintained. Please refer to page 13, lines 24-26; page 17, lines 9 and 10; and Figure 4, block 45.

According to Claim 54 (dependent on Claim 53), one or more instructions are eliminated from the first group of instructions if the first count exceeds a threshold, and one or more instructions are eliminated from the second group of instructions if the second count exceeds the threshold. Please refer to page 14, lines 2-7; page 17, lines 10-15; and Figure 4, block 45.

According to Claim 55 (dependent on Claim 49), the second state is indicated by setting a first bit associated with the cache line, where the first bit is cleared when the execution of the first group of instructions is ended, and the third state is indicated by setting a second bit associated with the cache line, where the second bit is cleared when the execution of the second group of instructions is ended. Please refer to page 11, lines 1-7.

Independent Claim 56 pertains to a computer system (5; Figure 1) comprising a processor (10; Figure 1), a cache memory (14; Figures 1 and 2) having a plurality of cache lines (21 and 22; Figure 2), and a memory unit (18; Figure 1). The memory unit has a plurality of indicator bits per cache line, where a

first indicator bit (24; Figure 2) associated with a cache line (21; Figure 2) of the cache memory is set to indicate that the cache line has been accessed responsive to the processor executing a first group of instructions (A; Figure 2), and where the first indicator bit is cleared when execution of the first group of instructions is ended. Also, a second indicator bit (25; Figure 2) associated with the cache line is set to indicate that the cache line has been accessed responsive to the processor executing a second group of instructions (B; Figure 2) in parallel with the first group, where the second indicator bit is cleared when execution of the second group of instructions is ended. Please refer to page 10, lines 1-19; page 11, lines 1-7; page 14, line 22, through page 15, line 15; and Figure 3, blocks 31-33.

According to Claim 57 (dependent on Claim 56), a subset of address bits of the cache line is used to identify an entry in the memory unit, where an indicator bit of the entry is set in response to the cache line being accessed. Please refer to page 19, line 21, through page 20, line 4.

6. Grounds of Rejection to be Reviewed on Appeal

This appeal involves Claims 33, 34, 39, 41, 42, 47, 49, 50, and 55-57. Claims 33, 34, 39, 41, 42, 47, 56, and 57 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray et al. ("Gray;" U.S. Patent No. 5,086,429) in view of Hady et al. ("Hady;" U.S. Patent Application Publication No. 2006/0112226), and Claims 49, 50, and 55 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray and Hady in view of Examiner's official notice.

7. Arguments

A. The following arguments are applicable to the 35 U.S.C. § 103(a) rejection of Claims 33, 34, 39, 41, 42, 47, 56, and 57.

For the reasons presented below, Appellant respectfully submits that the features recited in Claims 33, 34, 39, 41, 42, 47, 56, and 57 are not shown or suggested by the cited references (Gray and Hady). More specifically, Appellant respectfully submits that Gray and Hady do not teach or suggest "setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions" as recited in independent Claim 33; "instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read; instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read; instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions" as recited in independent Claim 41; or "wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions …, wherein a second indicator bit associated with said cache line is set

to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group" as recited in independent Claim 56.

The final rejection, on page 6, acknowledges that Gray does not disclose all of the claimed features. Specifically, according to the final rejection, Gray does not disclose "where the same processor executes both the first and second group of instructions." Accordingly, Appellant respectfully submits that Gray also does not teach or suggest the other claim features recited above, because those claim features are predicated on the subject matter admittedly not disclosed by Gray.

Hady is relied upon to overcome the shortcomings of Gray. However, for the reasons presented below, Appellant respectfully submits that Hady cannot be combined with Gray as suggested in the final rejection.

Specifically, according to the final rejection (page 6), "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al." However, Appellant respectfully submits that Gray cannot be modified in this manner, based on the following rationale.

As understood by the Appellant, Gray relies on <u>two different</u> processors that simultaneously execute instructions for error detection. According to Gray (column 3, lines 53-62), there are two pairs of processors, "with one pair being

arbitrarily designated the 'active pair' while the other is designated as a 'hot stand-by pair.' Each processor in each pair … is made to simultaneously execute the same program of instructions" (emphasis added). "During a read by the processors, the appropriate code word is read from the memory and the syndrome generators determine whether an error exists" (column 4, lines 8-10, of Gray; emphasis added). "Checkers 28 and 29 provide two redundant output signals for indicating that an error has been detected. These signals are called FAIL 1 and FAIL 2" (column 9, lines 1-4, of Gray). "Checkers 28 and 29 comprise digital comparators for comparing, bit-for-bit, the address bits and the control bits from the dual processors" (column 9, lines 12-14, of Gray; emphasis added). "If there is a miscompare …, then the error flag signals FAIL 1 and FAIL 2 become true" (column 9, lines 15-19, of Gray). Thus, as understood by the Appellant, Gray relies on a pair of redundant processors for error detection.

It is well-established that "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious" (MPEP § 2143.01; *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Moreover, "[i]f the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed amendment" (MPEP § 2143.01; *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

As presented above, Appellant respectfully submits that Gray cannot be modified by Hady in the manner suggested because to do so would change a principle of operation of Gray and would render Gray unsatisfactory for its

intended purpose. More specifically, Appellant asserts that Gray cannot be modified "to comprise where the same processor executes both the first and second group of instructions, as taught by Hady" as stated in the final rejection. According to Gray, two processors execute the same instructions; if the results are not the same, then an error exists. Essentially, according to Gray, the processors check each other's work. If the same processor is used as suggested in the final rejection, then Gray's principle of operation (two processors that simultaneously execute the same instructions) would be changed, and Gray would be rendered unsatisfactory for its intended purpose (error detection).

Accordingly, Appellant respectfully submits that there is no suggestion or motivation to make the proposed modification and a *prima facie* case of obviousness has not been established.

Consequently, Appellant respectfully submits that the basis for rejecting Claims 33, 34, 39, 41, 42, 47, 56, and 57 under 35 U.S.C. § 103(a) is traversed.

B. The following arguments are applicable to the 35 U.S.C. § 103(a) rejection of Claims 49, 50, and 55.

By rationale similar to that presented above, Appellant respectfully submits that the features recited in Claims 49, 50, and 55 are not shown or suggested by the cited references (Gray and Hady) in view of Examiner's official notice. More specifically, Appellant respectfully submits that Gray and Hady in view of Examiner's official notice do not show or suggest "executing a first group of

instructions with a processor; … associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions; executing a second group of instructions with said processor; and associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions" as recited in independent Claim 49.

The final rejection, on page 12, acknowledges that Gray does not disclose all of the claimed features. Specifically, according to the final rejection, Gray does not disclose "where the same processor executes both the first and second group of instructions." Accordingly, Appellant respectfully submits that Gray also does not teach or suggest the other features of Claim 49 that are recited above, because those claim features are predicated on the subject matter admittedly not disclosed by Gray.

Hady is relied upon to overcome the shortcomings of Gray. However, for the reasons presented previously herein, Appellant respectfully submits that Hady cannot be combined with Gray as suggested in the final rejection and, therefore, a *prima facie* case of obviousness has not been established.

Examiner's official notice is applied to the cache coherency protocol feature of Claim 49 and, therefore, does not assist in establishing a *prima facie* case with regard to the other features of Claim 49 that are recited above.

In summary, Appellant respectfully submits that the basis for rejecting Claims 49, 50, and 55 under 35 U.S.C. § 103(a) is traversed.

8. Conclusions

Appellant believes that Claims 33, 34, 39, 41, 42, 47, 49, 50, and 55-57 traverse the bases for rejection under 35 U.S.C. § 103(a).

Appellant respectfully requests that the 35 U.S.C. § 103(a) rejections of Claims 33, 34, 39, 41, 42, 47, 49, 50, and 55-57 be reversed.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Dated: January 24, 2011

/William A. Zarbis/

William A. Zarbis
Registration No. 46,120

Appendix I – Clean Copy of Claims on Appeal

1-32. (Canceled).

33. (Previously Presented) A method of managing memory in a computer system, said method comprising:

setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and

setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions.

34. (Previously Presented) The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed; and

processing said first group and said second group of instructions according to a value of said indicator.

35. (Previously Presented) The method of Claim 34 wherein said third group of instructions is executed by an agent other than said processor, wherein said processing comprises rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, and otherwise granting said access.

36. (Previously Presented) The method of Claim 35 wherein said processing further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set, and then granting said access provided said cache line is in other than said shared state, and otherwise granting said access only when said cache line is in said shared state.

37. (Original) The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. (Original) The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. (Original) The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. (Original) The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. (Previously Presented) A computer system comprising:

a processor;

a cache memory for use by said processor; and

a memory unit coupled to said processor and having stored therein instructions, said instructions comprising:

instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read;

instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and

instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions.

42. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise:

instructions to execute a third group of instructions that causes said cache line to be accessed; and

instructions to process said first group and said second group of instructions according to a value of said indicator.

43. (Previously Presented) The computer system of Claim 42 wherein said third group of instructions is for execution by an agent other than said processor, wherein said instructions further comprise instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, wherein otherwise said access is granted.

44. (Previously Presented) The computer system of Claim 43 wherein said instructions further comprise:

instructions to determine a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set, wherein said access is granted provided said cache line is in other than said shared state, and wherein otherwise said access is granted only when said cache line is in said shared state.

45. (Previously Presented) The computer system of Claim 44 wherein said instructions further comprise instructions to maintain a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. (Previously Presented) The computer system of Claim 45 wherein said instructions further comprise instructions to eliminate one or more instructions from said first group of instructions if said first count exceeds a threshold and to eliminate one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise instructions to clear said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise:

instructions to execute a plurality of groups of instructions in parallel using said processor;

instructions to change an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

instructions to roll back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory provided all cache lines in said cache memory are indicated as having

been accessed, wherein otherwise said plurality of groups of instructions continue to be executed.

49. (Previously Presented) A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions with a processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions with said processor; and

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. (Previously Presented) The method of Claim 49 wherein said first group of instructions includes multiple memory operations and said second group of instructions includes multiple memory operations.

51. (Previously Presented) The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed; and

rolling back said first group of instructions and said second group of instructions before granting said access.

52. (Original) The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. (Original) The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. (Original) The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. (Original) The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. (Previously Presented) A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of indicator bits per cache line, wherein a first indicator bit associated with a

cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. (Previously Presented) The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an entry in said memory unit, wherein an indicator bit of said entry is set in response to said cache line being accessed.

Appendix II – Evidence

There is no evidence entered and relied upon in this appeal.

Ex.1002 / Page 116 of 370
TESLA, INC.

Appendix III – Related Proceedings

There are no proceedings identified as related appeals and interferences.

Electronic Patent Application Fee Transmittal

Application Number:	12121531
Filing Date:	15-May-2008
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	William A. Zarbis/Tatiana Carvalho
Attorney Docket Number:	TRAN-P602

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Filing a brief in support of an appeal	1402	1	540	540
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**540**

Electronic Acknowledgement Receipt

EFS ID:	9294542
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Tatiana Carvalho
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	24-JAN-2011
Filing Date:	15-MAY-2008
Time Stamp:	17:54:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$540
RAM confirmation Number	4938
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Appeal Brief Filed	TRAN-P084C1_APPEAL_BRIEF_1-24-2011.pdf	93310 12113fb3f7f631387c70800074eccd18d95b5f0f	no	27
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30324 8b68d702bb278318d02b975870929c7c20b386ce	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	123634	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/31 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): TRAN-P084C1

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on 11/24/2010

Signature: /Tatiana Carvalho/

Typed or printed name: Tatiana Carvalho

In re Application of: Guillermo J. Rozas

Application Number	Filed
12/121,531	2008-05-15

For: MEMORY MANAGEMENT FOR CACHE CONSISTENCY

Art Unit	Examiner
2187	OTTO, ALAN

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 540.00

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 504160 .

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record. Registration number 46,120.

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

/William A. Zarbis/
Signature

William A. Zarbis
Typed or printed name

408-938-9060
Telephone number

11/24/2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	12121531
Filing Date:	15-May-2008
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	William A. Zarbis/Tatiana Carvalho
Attorney Docket Number:	TRAN-P602

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of appeal	1401	1	540	540
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**540**

Electronic Acknowledgement Receipt

EFS ID:	8909548
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Tatiana Carvalho
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	24-NOV-2010
Filing Date:	15-MAY-2008
Time Stamp:	13:32:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$540
RAM confirmation Number	1567
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Notice of Appeal Filed	TRAN-P084C1_NOTICE_OF_APPEAL_11-24-2010.pdf	258693 18196d3144cbd7d93f229407f958a235dc4cedc6	no	2
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30371 a44e5ec01a3c8455a4eae7701b5d9c0d4e144e0a	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	289064	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 10/29/2010

IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
OTTO, ALAN	

ART UNIT	PAPER NUMBER
2187	

MAIL DATE	DELIVERY MODE
10/29/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action

Response to Amendment

1. Examiner acknowledges receipt of the amendment dated 10/18/2010. Claims 33-57 are pending in the application.

Response to Arguments

2. Applicant's arguments filed 10/18/2010 have been fully considered but they are not persuasive.

3. Specifically applicant argues that Gray and Hady could not be combined because doing so would change a principle of operation of Gray. Gray uses two processors in an error checking system, by comparing the result of the processors. Applicant argues that the system wouldn't work if only one processor was used. However, Hady is being applied because it teaches multi-core processors. By combining Hady with Gray, Gray would still use the same system, but one core would be compared to another core in error checking. Multi-core processors are well known in the art. It would be obvious to take a multi-processor system such as Gray, and implement that same system in one processor with multiple cores.

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

4. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

5. Per the instant office action, claims 33-57 stand rejected.

b. DIRECTION OF FUTURE CORRESPONDENCES

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN OTTO whose telephone number is 571-270-1626. The examiner can normally be reached on 8:00-5:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on 571-272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. O./

Examiner, Art Unit 2187

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 12/121,531	**Applicant(s)** ROZAS, GUILLERMO J.	
	Examiner ALAN OTTO	**Art Unit** 2187	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 18 October 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 33-57.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☒ Other: see attached.

/A. O./
Examiner, Art Unit 2187

OK TO ENTER: /A.O./ 10/25/2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Rozas	)	Examiner: OTTO, A.
	)	
Serial No.: 12/121,531	)	Art Unit: 2187
	)	
Filed: May 15, 2008	)	Confirmation No.: 7036
	)	
For: MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO AN OFFICE ACTION

Dear Sir:

In response to the Office Action mailed August 26, 2010, the Applicant respectfully requests further examination and reconsideration of the above captioned patent application in view of the following amendments and remarks.

Amendments to the claims are presented beginning on page 2, and remarks begin on page 10.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)		
	)		
Rozas	)	Examiner:	OTTO, A.
	)		
Serial No.: 12/121,531	)	Art Unit:	2187
	)		
Filed: May 15, 2008	)	Confirmation No.:	7036
	)		
For: MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)	)		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO AN OFFICE ACTION

Dear Sir:

In response to the Office Action mailed August 26, 2010, the Applicant respectfully requests further examination and reconsideration of the above captioned patent application in view of the following amendments and remarks.

Amendments to the claims are presented beginning on page 2, and remarks begin on page 10.

AMENDMENTS TO THE CLAIMS

1-32. (Canceled).

33. (Previously Presented) A method of managing memory in a computer system, said method comprising:

setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and

setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions.

34. (Previously Presented) The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed; and

processing said first group and said second group of instructions according to a value of said indicator.

35. (Previously Presented) The method of Claim 34 wherein said third group of instructions is executed by an agent other than said processor, wherein said processing comprises rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, and otherwise granting said access.

36. (Previously Presented) The method of Claim 35 wherein said processing further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set, and then granting said access provided said cache line is in other than said shared state, and otherwise granting said access only when said cache line is in said shared state.

37. (Original) The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. (Original) The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. (Original) The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. (Original) The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. (Currently Amended) A computer system comprising:

a processor;

a cache memory for use ~~used~~ by said processor; and

a memory unit coupled to said processor and having stored therein instructions, said instructions comprising:

instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read;

instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and

instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions.

42. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise:

instructions to execute a third group of instructions that causes said cache line to be accessed; and

instructions to process said first group and said second group of instructions according to a value of said indicator.

43. (Previously Presented) The computer system of Claim 42 wherein said third group of instructions is for execution by an agent other than said processor, wherein said instructions further comprise instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, wherein otherwise said access is granted.

44. (Previously Presented) The computer system of Claim 43 wherein said instructions further comprise:

instructions to determine a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

instructions to roll back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second

bit is set, wherein said access is granted provided said cache line is in other than said shared state, and wherein otherwise said access is granted only when said cache line is in said shared state.

45. (Previously Presented) The computer system of Claim 44 wherein said instructions further comprise instructions to maintain a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. (Previously Presented) The computer system of Claim 45 wherein said instructions further comprise instructions to eliminate one or more instructions from said first group of instructions if said first count exceeds a threshold and to eliminate one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise instructions to clear said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. (Previously Presented) The computer system of Claim 41 wherein said instructions further comprise:

instructions to execute a plurality of groups of instructions in parallel using said processor;

instructions to change an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

instructions to roll back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory provided all cache lines in said cache memory are indicated as having been accessed, wherein otherwise said plurality of groups of instructions continue to be executed.

49. (Previously Presented) A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions with a processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions with said processor; and

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. (Previously Presented) The method of Claim 49 wherein said first group of instructions includes multiple memory operations and said second group of instructions includes multiple memory operations.

51. (Previously Presented) The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed; and

rolling back said first group of instructions and said second group of instructions before granting said access.

52. (Original) The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. (Original) The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. (Original) The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. (Original) The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said

cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. (Previously Presented) A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of indicator bits per cache line, wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. (Previously Presented) The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an entry in said memory unit, wherein an indicator bit of said entry is set in response to said cache line being accessed.

REMARKS

Claims 33-57 are pending. Claim 41 is amended. Claims 35-38, 40, 43-46, and 51-54 are allowable. Applicant thanks the Examiner for indicating the allowability of those claims.

Double Patenting

According to the Office Action, Claims 33-57 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over U.S. Patent No. 7,376,798. A timely filed terminal disclaimer may be filed to overcome a rejection based on non-statutory double patenting. Applicant respectfully submits that a terminal disclaimer will be considered once the application is otherwise considered to be allowable. The Applicant respectfully requests that the double-patenting rejection be held in abeyance until the claims are otherwise allowable.

§ 103 Rejections

Claims 33, 34, 39, 41, 42, 47, 56, and 57

According to the Office Action, Claims 33, 34, 39, 41, 42, 47, 56, and 57 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray et al. ("Gray;" U.S. Patent No. 5,086,429) in view of Hady et al. ("Hady;" U.S. Patent Application Publication No. 2006/0112226). The Applicant has reviewed the cited reference and respectfully submits that the features recited in Claims 33, 34, 39, 41, 42, 47, 56, and 57 are not shown or suggested by Gray and Hady, alone or in combination. (It is not conceded that Hady is in fact prior art with respect to the present application. The option to swear behind Hady is reserved.)

Applicant respectfully agrees with the statement on page 6 of the Office Action to the effect that Gray does not disclose all of the claimed features. Hady is relied upon to overcome the shortcomings of Gray; however, Applicant respectfully submits that Hady cannot be combined with Gray as suggested in the Office Action.

Specifically, according to the Office Action (page 6), "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al." However, Applicant respectfully submits that Gray cannot be modified in this manner, based on the following rationale.

As understood by the Applicant, Gray relies on two different processors that simultaneously execute instructions for error detection. According to Gray (column 3, lines 53-62), there are two pairs of processors, "with one pair being arbitrarily designated the 'active pair' while the other is designated as a 'hot stand-by pair.' Each processor in each pair … is made to simultaneously execute the same program of instructions" (emphasis added). "During a read by the processors, the appropriate code word is read from the memory and the syndrome generators determine whether an error exists" (column 4, lines 8-10, of Gray; emphasis added). "Checkers 28 and 29 provide two redundant output signals for indicating that an error has been detected. These signals are called FAIL 1 and FAIL 2" (column 9, lines 1-4, of Gray). "Checkers 28 and 29 comprise digital comparators for comparing, bit-for-bit, the address bits and the control bits from the dual processors" (column 9, lines 12-14, of Gray; emphasis

added). "If there is a miscompare …, then the error flag signals FAIL 1 and FAIL 2 become true" (column 9, lines 15-19, of Gray). Thus, as understood by the Applicant, Gray relies on a pair of redundant processors for error detection.

It is well-established that "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious" (MPEP § 2143.01; *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Moreover, "[i]f the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed amendment" (MPEP § 2143.01; *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

As presented above, Applicant respectfully submits that Gray cannot be modified by Hady in the manner suggested because to do so would change a principle of operation of Gray and would render Gray unsatisfactory for its intended purpose. More specifically, Applicant asserts that Gray cannot be modified "to comprise where the same processor executes both the first and second group of instructions, as taught by Hady" as stated in the Office Action. According to Gray, two processors execute the same instructions; if the results are not the same, then an error exists. Essentially, according to Gray, the processors check each other's work. If the same processor is used as suggested in the Office Action, then Gray's principle of operation (two processors that simultaneously execute the same instructions) would be changed, and Gray would be rendered unsatisfactory for its intended purpose (error detection).

Accordingly, Applicant respectfully submits that there is no suggestion or motivation to make the proposed modification and a *prima facie* case of obviousness has not been established.

Consequently, Applicant respectfully submits that the basis for rejecting Claims 33, 34, 39, 41, 42, 47, 56, and 57 under 35 U.S.C. § 103(a) is traversed.

Claims 49, 50, and 55

According to the Office Action, Claims 49, 50, and 55 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray and Hady in view of Examiner's official notice. By rationale similar to that presented above, Applicant respectfully submits that a *prima facie* case of obviousness has not been established and the basis for rejecting Claims 49, 50, and 55 under 35 U.S.C. § 103(a) is traversed.

Conclusions

In light of the above remarks, Applicant respectfully requests reconsideration of the rejected claims.

Based on the arguments presented above, Applicant respectfully asserts that Claims 33-57 overcome the rejections of record, and therefore Applicant respectfully solicits allowance of those claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Date: 10/18/2010

/William A. Zarbis/

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Electronic Acknowledgement Receipt

EFS ID:	8647741
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT FOR CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Mina Oliveri
Filer Authorized By:	William A. Zarbis
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Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TRAN-P084C1_AMDT_AFTER_FINAL_10-18-2010.pdf	88848 e03c2a5dfd2caafb7fea8485c8fc871489555 39b	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	14
Warnings:			
Information:			
	Total Files Size (in bytes):	88848	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/121,531	Filing Date 05/15/2008	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	**10/18/2010**	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 25	Minus	** 25	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MYRTLE B. LEIGH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 08/26/2010

IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
OTTO, ALAN	

ART UNIT	PAPER NUMBER
2187	

MAIL DATE	DELIVERY MODE
08/26/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/121,531	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	ALAN OTTO	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

The instant application having Application No. 12/121,531 has a total of 25 claims pending in the application, there are 4 independent claim and 21 dependent claims, all of which are ready for examination by the examiner. Claims 1-32 were cancelled by the amendment dated 5/15/2008.

REJECTIONS NOT BASED ON PRIOR ART

1. The previous 112 rejection is withdrawn due to applicant's amendments.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 33-57 are rejected on the ground of nonstatutory double patenting over claims 1-6, 8-11, 13-24 and 26-28 of U. S. Patent No. 7,376,798 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

Instant Application 12/121,531 – Claim #	**Patent No. 7,376,798 – Claim #**
33	1
34	2
35	3
36	4
37	5
38	6
39	8

40	9
41	10
42	11
43	13
44	14
45	15
46	16
47	17
48	18
49	19
50	20
51	21
52	22
53	23
54	24
55	26
56	27
57	28

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 33-34, 39, 41-42, 47 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. (U.S. Patent No. 5,086,429), herein referred to as Gray et al. in view of Hady et al. (U.S. Patent Application Publication No. 2006/0112226), herein referred to as Hady et al.

5. Referring to claim 33, Gray et al. disclose as claimed, a method of managing memory in a computer system, said method comprising: setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to a said processor executing an instruction in a second group of instructions. (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both**

syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

6. As to claim 34, Gray et al. also disclose the method of Claim 33 further comprising: executing a third group of instructions that causes said cache line to be accessed; and processing said first group and said second group of instructions

according to a value of said indicator (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

7. As to claim 39, Gray et al. also disclose the method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

8. Referring to claim 41, Gray et al. disclose as claimed, a computer system comprising: a processor; a cache memory used by said first processor; and a memory unit coupled to said processor and having stored therein instructions, said instructions comprising: instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read; instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read; instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the**

address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor

system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

9. As to claim 42, Gray et al. also disclose the computer system of Claim 41 wherein said instructions further comprise: Instructions to execute a third group of instructions that causes said cache line to be accessed; and instructions to process said first group and said second group of instructions according to a value of said indicator (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

10. As to claim 47, Gray et al. also disclose the computer system of Claim 41 wherein said instructions further comprise instructions to clear said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

11. Referring to claim 56, Gray et al. disclose as claimed, a computer system comprising: a processor; a cache memory coupled to said processor and having a plurality of cache lines; and a memory unit coupled to said processor, wherein said memory unit has a plurality of indicator bits per cache line, wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions

and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line. Also see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

Gray et al. disclose the claimed invention except where the same processor executes both the first and second group of instructions.

However, Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

12. As to claim 57, Gray et al. also disclose the computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an entry in said memory unit wherein an indicator bit of said entry is set in response to said cache line being accessed (**see col. 9, lines 12-18, where checkers 28 and 29 compare the address bits from the processors, and if there is a miscompare, then fail flags are set**).

13. Claims 49-50 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. in view of Hady et al. and in view of the examiner taking official notice.

14. Referring to claim 49, Gray et al. disclose as claimed, a method of managing shared memory in a computer system, said method comprising: executing a first group of instructions on a first processor; associating a second state with said cache line during said executing of said first group of instructions, wherein said second state

indicates that said cache line has been accessed because of said first group of instructions; executing a second group of instructions on said first processor; associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line**).

Gray et al. disclose the claimed invention except for associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and where the same processor executes both the first and second group of instructions.

However, using a cache coherency protocol such as MESI is well known in the art. MESI is used to allow multiprocessor systems to keep track of the states of cache lines in order to have an efficient cache coherent system. It would be obvious to employ such a system with Gray et al. in a multiprocessor system.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise associating a first state with a

cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state, in order to have cache coherency in a multi-processor system, allowing the caches in a multi-processor system to be identical or to be controlled and kept track of.

Hady et al. disclose a multi-core processor, where a single processor would have multiple cores, each capable of executing different threads or programs (**see para. 22-23, explaining a processor that has a shared cache and has multiple processor cores. Multi-core processors are well known in the art, and it would be obvious to combine such technology with Hady et al.**).

Gray et al. and Hady et al. are analogous art because they are from the same field of endeavor of shared cache and memory (**see Gray et al., col. 3, lines 60-62 and see Hady et al., para. 22, regarding shared memory**).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise where the same processor executes both the first and second group of instructions, as taught by Hady et al., in order to allow the cores to more efficiently share data. The interconnects of a multi-core processor would be faster and shorter than the interconnects on a multiprocessor system with separate processors (**see para. 17, explaining the advantages of multi-core systems).**

15. As to claim 50, Gray et al. also disclose the method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations

(**see col. 3, lines 62-68 and col. 4, lines 1-10, where each memory access is checked. There would be multiple memory operations in a group of instructions, thread, or program running on the processors**).

16. As to claim 55, Gray et al. also disclose the method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

Response to Arguments

17. Applicant's arguments with respect to claims 33, 41 and 56 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

18. Claims 35-38, 40, 43-46 and 51-54 are rejected for double patenting, but would be allowable if the double patenting rejection is overcome and if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Claims 35 and 43 disclose “rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line

has been read, and otherwise granting said access without rolling back said first group and said second group of instructions." This limitation is taught in the specification, page 11, lines 15-21. This limitation in combination with other recited limitations of claims 35 and 43 are not taught or suggested by the prior art of record.

20. Claim 40 discloses "provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions." This limitation is taught in the specification, page 17, lines 26-28 and page 18, lines 1-2. This limitation in combination with other recited limitations of claim 40 is not taught or suggested by the prior art of record.

21. Claim 51 discloses "executing a third group of instructions that causes said cache line to be accessed; using said second state and said second state to indicate said cache line has been accessed; and rolling back said first group and said second group of instructions before granting access." This limitation is taught in the specification, page 11, lines 15-21. This limitation in combination with other recited limitations of claim 51 is not taught or suggested by the prior art of record.

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

22. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

23. Per the instant office action, claims 33-57 have received a second action on the merits and are the subject of a final rejection.

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN OTTO whose telephone number is 571-270-1626. The examiner can normally be reached on 8:00-5:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on 571-272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. O./
Examiner, Art Unit 2187

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2187

Notice of References Cited	Application/Control No. 12/121,531	Applicant(s)/Patent Under Reexamination ROZAS, GUILLERMO J.	
	Examiner ALAN OTTO	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0112226	05-2006	Hady et al.	711/130
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/13/2010	08/24/2010							
	1	-	-							
	2	-	-							
	3	-	-							
	4	-	-							
	5	-	-							
	6	-	-							
	7	-	-							
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	9	-	-							
	10	-	-							
	11	-	-							
	12	-	-							
	13	-	-							
	14	-	-							
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	19	-	-							
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	24	-	-							
	25	-	-							
	26	-	-							
	27	-	-							
	28	-	-							
	29	-	-							
	30	-	-							
	31	-	-							
	32	-	-							
	33	✓	✓							
	34	✓	✓							
	35	✓	✓							
	36	✓	✓							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/13/2010	08/24/2010							
	37	✓	✓							
	38	✓	✓							
	39	✓	✓							
	40	✓	✓							
	41	✓	✓							
	42	✓	✓							
	43	✓	✓							
	44	✓	✓							
	45	✓	✓							
	46	✓	✓							
	47	✓	✓							
	48	✓	✓							
	49	✓	✓							
	50	✓	✓							
	51	✓	✓							
	52	✓	✓							
	53	✓	✓							
	54	✓	✓							
	55	✓	✓							
	56	✓	✓							
	57	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Updated East text search	8/24/10	AO
Inventor name search (Palm and East)	8/24/10	AO
711/130, 118, 133-134, 141, 144-146, 710/22, g06f12/00 (text search - see attached search results)	8/24/10	AO

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/A. O./ Examiner.Art Unit 2187	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	18	rozas-guillermo.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L2	8	US-6938130-$.DID. OR US-6263407-$.DID. OR US-6625694-$.DID. OR US-5428761-$.DID. OR US-5701432-$.DID. OR US-6658536-$.DID. OR US-5974438-$.DID. OR US-6006299-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L3	5	US-6189074-$.DID. OR US-6304944-$.DID. OR US-6738864-$.DID. OR US-6779085-$.DID. OR US-6839813-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L4	946	(indicat$4 or mark $4) with read with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L5	1580	(indicat$4 or mark $4) with (read or access$3) with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L6	10069	711/130.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls. or 711/146.ccls. or 710/22.ccls. or 711/133-134.ccls. or 711/118.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27

L7	22644	g06f12/00.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L8	833	L5 same (bit or tag or indicator)	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L9	23308	L7 or L6	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L10	447	L8 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L11	219	L5 same (bit or tag or indicator) same (application or process or transaction or thread or (group near3 instruction))	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L12	121	L11 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2010/08/23 11:27
L13	1060	((transaction$3 near3 system) or (transaction$3 near3 memory)) same (cache adj line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L14	29	(L11 and L13) not L12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L15	3852	711/143.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L16	12300	valid adj (bit or tag or indicator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L17	4115	mesi or moesi	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27

L18	146	L15 and L16 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L19	81	shared with (read adj (miss or hit))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L20	2	L18 and L19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L21	523286	(compar$4 or check$4 or detect $4) with (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L22	1262	714/11-12.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L23	474	L21 and L22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L24	630	711/130.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L25	0	L23 and L24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L26	38247	shared adj (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27

L27	4063	L26 same L21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L28	40	L27 and L23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L29	2	"7376798".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 11:27
L33	4488	(dual or multi) adj core adj processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 16:36
L35	128	l33 and ("same" adj die)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 16:48
L36	27	l35 and coherency	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/08/23 16:48

EAST Search History (Interference)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Rozas	)	Examiner: OTTO, A.
	)	
Serial No.: 12/121,531	)	Art Unit: 2187
	)	
Filed: May 15, 2008	)	Confirmation No.: 7036
	)	
For: MEMORY MANAGEMENT FOR CACHE CONSISTENCY (As Amended)	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO AN OFFICE ACTION

Dear Sir:

In response to the Office Action mailed March 22, 2010, the Applicant respectfully requests further examination and reconsideration of the above captioned patent application in view of the following amendments and remarks.

Amendments to the specification are presented on page 2, amendments to the claims are presented beginning on page 3, and remarks begin on page 12.

AMENDMENTS TO THE SPECIFICATION

Please amend the title of the application, which appears on pages 1 and 30 of the substitute specification, as follows:

MEMORY MANAGEMENT FOR ~~METHODS AND SYSTEMS THAT SUPPORT~~ CACHE CONSISTENCY

AMENDMENTS TO THE CLAIMS

1-32. (Canceled).

33. (Currently Amended) A method of managing memory in a computer system, said method comprising:

~~executing a first group of instructions that causes a cache line of a cache memory to be read;~~

setting a first bit of an indicator associated with a ~~said~~ cache line in a cache memory if ~~to indicate that~~ said cache line has been accessed in response to a processor executing an instruction in a first group of instructions ~~read~~;

~~executing a second group of instructions that causes said cache line to be read;~~ and

setting a second bit of said indicator while said first bit remains set if ~~to indicate~~ said cache line has also been accessed in response to said processor executing an instruction in a ~~by both said first group and said~~ second group of instructions.

34. (Currently Amended) The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

~~using a value of said indicator to determine whether said cache line has been read and generating a result thereof;~~ and

processing ~~handling~~ said first group and said second group of instructions according to a value of said indicator ~~said result~~.

35. (Currently Amended) The method of Claim 34 wherein said third group of instructions is executed by an agent other than said processor, wherein said processing ~~handling~~ comprises rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line ~~granting said access provided said indicator indicates said cache line has been read~~, and otherwise granting said access ~~without rolling back said first group and said second group of instructions~~.

36. (Currently Amended) The method of Claim 35 wherein said processing ~~handling~~ further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

rolling back said first group of instructions provided said first bit is set and rolling back said second group of instructions provided said second bit is set, and then granting said access provided said cache line is in other than said shared state ~~and said indicator indicates said cache line has been read~~, and otherwise granting said access ~~without rolling back said first group and said second group of instructions~~ only when said cache line is in said shared state.

37. (Original) The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. (Original) The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. (Original) The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. (Original) The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. (Currently Amended) A computer system comprising:

a ~~first~~ processor;

a cache memory used by said ~~first~~ processor; and

a memory unit coupled to said ~~first~~ processor and having stored therein instructions, said instructions ~~said memory unit containing instructions that when executed implement a memory management method, said method~~ comprising:

instructions to execute ~~executing~~ a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read;

instructions to set ~~setting~~ a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

instructions to execute ~~executing~~ a second group of instructions using said ~~first~~ processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and

instructions to set ~~setting~~ a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions.

42. (Currently Amended) The computer system of Claim 41 wherein said instructions ~~method~~ further comprise ~~comprises~~:

instructions to execute ~~executing~~ a third group of instructions that causes said cache line to be accessed;

~~using a value of said indicator to determine whether said cache line has been read and generating a result thereof;~~ and

instructions to process ~~handling~~ said first group and said second group of instructions according to a value of said indicator ~~said result~~.

43. (Currently Amended) The computer system of Claim 42 wherein said third group of instructions is for execution by an agent other than said processor,

wherein said instructions ~~method~~ further comprise instructions to roll ~~comprises rolling~~ back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set before allowing an instruction in said third group to access said cache line, wherein otherwise said access is granted. ~~granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.~~

44. (Currently Amended) The computer system of Claim 43 wherein said instructions ~~method~~ further comprise ~~comprises~~:

instructions to determine ~~determining~~ a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state; and

instructions to roll ~~rolling~~ back said first group of instructions provided said first bit is set and to roll back said second group of instructions provided said second bit is set, wherein ~~and then granting~~ said access is granted provided said cache line is in other than said shared state ~~and said indicator indicates said cache line has been read~~, and wherein otherwise ~~granting~~ said access is granted ~~without rolling back said first group and said second group of instructions~~ only when said cache line is in said shared state.

45. (Currently Amended) The computer system of Claim 44 wherein said instructions ~~method~~ further comprise instructions to maintain ~~comprises maintaining~~ a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. (Currently Amended) The computer system of Claim 45 wherein said instructions ~~method~~ further comprise instructions to eliminate ~~comprises eliminating~~ one or more instructions from said first group of instructions if said first count exceeds a threshold and to eliminate ~~eliminating~~ one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. (Currently Amended) The computer system of Claim 41 wherein said instructions ~~method~~ further comprise instructions to clear ~~comprises clearing~~ said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. (Currently Amended) The computer system of Claim 41 wherein said instructions ~~method~~ further comprise ~~comprises~~:

instructions to execute ~~executing~~ a plurality of groups of instructions in parallel using ~~on~~ said ~~first~~ processor;

instructions to change ~~changing~~ an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

~~provided all cache lines in said cache memory are indicated as having been accessed,~~ instructions to roll ~~rolling~~ back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory provided all cache lines in said cache memory

are indicated as having been accessed, wherein ~~and~~ otherwise ~~continuing said executing of~~ said plurality of groups of instructions continue to be executed.

49. (Currently Amended) A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions with ~~on~~ a ~~first~~ processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state, and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions with ~~on~~ said ~~first~~ processor; and

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. (Currently Amended) The method of Claim 49 wherein said first group of instructions includes multiple memory operations and said second group of instructions ~~each~~ includes multiple memory operations.

51. (Currently Amended) The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

~~using said second state and said second state to indicate said cache line has been accessed;~~ and

rolling back said first group of instructions and said second group of instructions before granting said access.

52. (Original) The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. (Original) The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. (Original) The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. (Original) The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. (Currently Amended) A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a ~~plurality of entries and a~~ plurality of indicator bits per cache line ~~entry~~, wherein a first indicator bit associated with a cache line of said cache memory ~~plurality of indicator bits~~ is set to indicate that said [[a]] cache line ~~of said cache memory~~ has been accessed responsive to said processor executing ~~because of~~ a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit associated with said cache line ~~of said plurality of indicator bits~~ is set to indicate that said cache line has been accessed responsive to said processor executing ~~because of~~ a second group of instructions in parallel with said first group and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. (Currently Amended) The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify an ~~said~~ entry in said memory unit ~~of said plurality of entries~~, wherein ~~in response to said cache line being accessed,~~ an indicator bit of said entry ~~corresponding to said subset of address bits~~ is set in response to said cache line being accessed.

REMARKS

Claims 33-57 are pending. Claims 33-36, 41-51, 56, and 57 are amended herein. No new matter is introduced by the claim amendments.

Claims 35-38, 40, 43-46, and 51-54 are allowable. Applicant thanks the Examiner for indicating the allowability of those claims.

§ 112 Rejections

According to the Office Action, Claims 51-54 are rejected under 35 U.S.C. § 112, second paragraph. Specifically, Claim 51 is rejected, and Claims 52-54 are rejected because of their dependence on Claim 51.

Applicant respectfully submits that, as amended, Claim 51 and its dependent claims traverse the basis for rejection under 35 U.S.C. § 112, second paragraph.

Double Patenting

According to the Office Action, Claims 33-57 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over U.S. Patent No. 7,376,798.

A timely filed terminal disclaimer may be filed to overcome a rejection based on non-statutory double patenting. Applicant respectfully submits that a terminal disclaimer will be considered once the application is otherwise considered to be allowable. The Applicant respectfully requests that the double-patenting rejection be held in abeyance until the claims are otherwise allowable.

§ 102 Rejections

According to the Office Action, Claims 33, 34, 39, 41, 42, 47, 56, and 57 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Gray et al. ("Gray;" U.S. Patent No. 5,086,429). The Applicant has reviewed the cited reference and respectfully submits that the features recited in Claims 33, 34, 39, 41, 42, 47, 56, and 57 are not shown or suggested by Gray.

According to Gray (column 3, lines 53-62), there are two pairs of processors, "with one pair being arbitrarily designated the 'active pair' while the other is designated as a 'hot stand-by pair.' Each processor in each pair … is made to simultaneously execute the same program of instructions …, [and] the two processors in each pair share a common memory." "During a read by the processors, the appropriate code word is read from the memory and the syndrome generators determine whether an error exists" (column 4, lines 8-10, of Gray). "Checkers 28 and 29 provide two redundant output signals for indicating that an error has been detected. These signals are called FAIL 1 and FAIL 2" (column 9, lines 1-4, of Gray). "Checkers 28 and 29 comprise digital comparators for comparing, bit-for-bit, the address bits and the control bits from the dual processors" (column 9, lines 12-14, of Gray). "If there is a miscompare …, then the error flag signals FAIL 1 and FAIL 2 become true" (column 9, lines 15-19, of Gray).

In other words, according to Gray, the error flag signals are set if a pair of redundant processors reads the same information differently.

Therefore, Applicant respectfully submits that Gray does not teach or suggest "setting a first bit of an indicator associated with a cache line in a cache memory if said cache line has been accessed in response to a processor executing an instruction in a first group of instructions; and setting a second bit of said indicator while said first bit remains set if said cache line has also been accessed in response to said processor executing an instruction in a second group of instructions" as recited in independent Claim 33 (emphasis added); "instructions to execute a first group of instructions using said processor, wherein said first group of instructions includes an instruction that causes a cache line of said cache memory to be read; instructions to set a first bit of an indicator associated with said cache line to indicate that said cache line has been read; instructions to execute a second group of instructions using said processor, wherein said second group of instructions includes an instruction that causes said cache line to be read; and instructions to set a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group of instructions and said second group of instructions" as recited in independent Claim 41; or "wherein a first indicator bit associated with a cache line of said cache memory is set to indicate that said cache line has been accessed responsive to said processor executing a first group of instructions …, wherein a second indicator bit associated with said cache line is set to indicate that said cache line has been accessed responsive to said processor executing a second group of instructions in parallel with said first group" as recited in independent Claim 56.

Accordingly, Applicant respectfully submits that Gray does not show or suggest the features of independent Claims 33, 41, and 56, and that those claims are in condition for allowance.

Each of the Claims 34 and 39 includes all of the features of Claim 33 plus additional features. Each of the Claims 42 and 47 includes all of the features of independent Claim 41 plus additional features. Claim 57 includes all of the features of independent Claim 56 plus additional features. Applicant respectfully submits that Gray does not show or suggest the features of Claims 34, 39, 42, 47, and 57 in combination with the features of their respective base claim, and that Claims 34, 39, 42, 47, and 57 are in condition for allowance at least because they depend from an allowable claim.

In conclusion, Applicant respectfully submits that Claims 33, 34, 39, 41, 42, 47, 56, and 57 traverse the basis for rejection under 35 U.S.C. § 102(b).

§ 103 Rejections

According to the Office Action, Claims 49, 50, and 55 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Gray in view of Examiner's official notice (in view of what is known in the art).

By rationale similar to that presented above, Applicant respectfully submits that Gray does not teach or suggest "executing a first group of instructions with a processor; … associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of

instructions; executing a second group of instructions with said processor; and associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions" as recited in independent Claim 49.

Accordingly, Applicant respectfully submits that Claim 49 is in condition for allowance.

Each of the Claims 50 and 55 includes all of the features of Claim 49 plus additional features. Applicant respectfully submits that Gray does not show or suggest the features of Claims 50 and 55 in combination with the features of Claim 49, and that Claims 50 and 55 are in condition for allowance at least because they depend from an allowable claim.

In conclusion, Applicant respectfully submits that Claims 49, 50, and 55 traverse the basis for rejection under 35 U.S.C. § 103(a).

Conclusions

In light of the above remarks, Applicant respectfully requests reconsideration of the rejected claims.

Based on the arguments presented above, Applicant respectfully asserts that Claims 33-57 overcome the rejections of record, and therefore Applicant respectfully solicits allowance of those claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO HAO & BARNES LLP

Date: 6/17/2010

/William A. Zarbis/

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Electronic Acknowledgement Receipt

EFS ID:	7840777
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Tatiana Carvalho
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	17-JUN-2010
Filing Date:	15-MAY-2008
Time Stamp:	20:17:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		TRAN-P084C1_AMDT_06-17-2010.pdf	72536 ca05fa63e542df13e43b3fbade668e89115a798e	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	2
	Claims	3	11
	Applicant Arguments/Remarks Made in an Amendment	12	17
Warnings:			
Information:			
	Total Files Size (in bytes):	72536	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/121,531	Filing Date 05/15/2008	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/17/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 25	Minus	** 25	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MARSHA R. RICHARDS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/121,531	05/15/2008	Guillermo J. Rozas	TRAN-P602	7036

45590 7590 03/22/2010

IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
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SAN JOSE, CA 95113

EXAMINER	
OTTO, ALAN	

ART UNIT	PAPER NUMBER
2187	

MAIL DATE	DELIVERY MODE
03/22/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/121,531	ROZAS, GUILLERMO J.	
	Examiner	Art Unit	
	ALAN OTTO	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/15/2008, 12/19/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

The instant application having Application No. 12/121,531 has a total of 25 claims pending in the application, there are 4 independent claim and 21 dependent claims, all of which are ready for examination by the examiner. Claims 1-32 were cancelled by the amendment dated 5/15/2008.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by **M.P.E.P. 201.14(c)**, acknowledgment is made of applicant's claim for priority based on an application filed 4/7/2005.

INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted 5/15/2008 are acceptable for examination purposes.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by **M.P.E.P. 609 (C)**, the applicant's submission of the Information Disclosure Statements dated 5/15/2008 and 12/19/2009 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 51-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 51 discloses “using said second state and said second state." It is unclear why the second state was listed twice. It is unclear what combination of states was intended, whether the first, second, or third in some combination. Dependent claims 52-54 fail to remedy the deficiency.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 33-57 are rejected on the ground of nonstatutory double patenting over claims 1-6, 8-11, 13-24 and 26-28 of U. S. Patent No. 7,376,798 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

Instant Application 12/121,531 – Claim #	**Patent No. 7,376,798 – Claim #**
33	1
34	2
35	3
36	4
37	5
38	6
39	8
40	9
41	10
42	11
43	13
44	14
45	15
46	16
47	17
48	18
49	19

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56	27
57	28

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 33-34, 39, 41-42, 47 and 56-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Gray et al. (U.S. Patent No. 5,086,429), herein referred to as Gray et al.

12. Referring to claim 33, Gray et al. disclose as claimed, a method of managing memory in a computer system, said method comprising: executing a first group of instructions that causes a cache line of a cache memory to be read; setting a first bit of

an indicator associated with said cache line to indicate that said cache line has been read; executing a second group of instructions that causes said cache line to be read; and setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line**).

13. As to claim 34, Gray et al. also disclose the method of Claim 33 further comprising: executing a third group of instructions that causes said cache line to be accessed; using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and handling said first group and said second group of instructions according to said result (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

14. As to claim 34, Gray et al. also disclose the method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is

ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

15. Referring to claim 41, Gray et al. disclose as claimed, a computer system comprising: a first processor; a cache memory used by said first processor; and a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising: executing a first group of instructions that causes a cache line of said cache memory to be read; setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read; executing a second group of instructions using said first processor that causes said cache line to be read; and setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line**).

16. As to claim 42, Gray et al. also disclose the computer system of Claim 41 wherein said method further comprises: executing a third group of instructions that

causes said cache line to be accessed; using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and handling said first group and said second group of instructions according to said result (**see col. 3, lines 53-57, describing the active pair of processors and a hot stand-by pair. If a problem was discovered with the active pair from the check bits, then the standby pair would need to be used. Therefore the standby pair instructions could be handled based on the value from the indicator in the active pair**).

17. As to claim 47, Gray et al. also disclose the computer system of Claim 41 wherein said method further comprises clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

18. Referring to claim 56, Gray et al. disclose as claimed, a computer system comprising: a processor; a cache memory coupled to said processor and having a plurality of cache lines; and a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and a plurality of indicator bits per entry, wherein a first indicator bit of said plurality of indicator bits is set to indicate that a cache line of said cache memory has been accessed because of a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit of said plurality of indicator bits is set to indicate that said cache line has been accessed because of a second group of

instructions and wherein said second indicator bit is cleared when execution of said second group of instructions is ended (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line. Also see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

19. As to claim 57, Gray et al. also disclose the computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set (**see col. 9, lines 12-18, where checkers 28 and 29 compare the address bits from the processors, and if there is a miscompare, then fail flags are set**).

Claim Rejections - 35 USC 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 49-50 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al. in view of the examiner taking official notice.

21. Referring to claim 49, Gray et al. disclose as claimed, a method of managing shared memory in a computer system, said method comprising: executing a first group of instructions on a first processor; associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions; executing a second group of instructions on said first processor; associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions (**see fig. 2, showing checker 28 and 29 checking the address bits to the memory and checking the values generated by the syndrome generators. See col. 9, lines 12-19 and see col. 6,lines 23-59, where the syndrome generator generates check bits after each read for each processor, and the checker generates flag signals which indicate errors with the read. When both syndromes are generated, it would indicate that both groups of instructions from processor 1a and processor 1b have read the cache line**).

Gray et al. disclose the claimed invention except for associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state;

However, using a cache coherency protocol such as MESI is well known in the art. MESI is used to allow multiprocessor systems to keep track of the states of cache lines in order to have an efficient cache coherent system. It would be obvious to employ such a system with Gray et al. in a multiprocessor system.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gray et al. to comprise associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state, in order to have cache coherency in a multi-processor system, allowing the caches in a multi-processor system to be identical or to be controlled and kept track of.

22. As to claim 50, Gray et al. also disclose the method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations (**see col. 3, lines 62-68 and col. 4, lines 1-10, where each memory access is checked. There would be multiple memory operations in a group of instructions, thread, or program running on the processors**).

23. As to claim 55, Gray et al. also disclose the method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group

of instructions is ended (**see col. 9, lines 12-19, where the instructions are ended once the error or fail bits are set, until the RESET signal is triggered**).

Allowable Subject Matter

24. Claims 35-38, 40, 43-46 and 51-54 are rejected for double patenting, but would be allowable if the double patenting rejection and the 112 rejection as to claim 51 are overcome and if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. Claims 35 and 43 disclose “rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.” This limitation is taught in the specification, page 11, lines 15-21. This limitation in combination with other recited limitations of claims 35 and 43 are not taught or suggested by the prior art of record.

26. Claim 40 discloses "provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.” This limitation is taught in the specification, page 17, lines 26-28 and page 18, lines 1-2. This limitation in combination with other recited limitations of claim 40 is not taught or suggested by the prior art of record.

27. Claim 51 discloses "executing a third group of instructions that causes said cache line to be accessed; using said second state and said second state to indicate said cache line has been accessed; and rolling back said first group and said second group of instructions before granting access." This limitation is taught in the specification, page 11, lines 15-21. This limitation in combination with other recited limitations of claim 51 is not taught or suggested by the prior art of record.

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

28. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

29. Per the instant office action, claims 33-57 have received a first action on the merits and are the subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN OTTO whose telephone number is 571-270-1626. The examiner can normally be reached on 8:00-5:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on 571-272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. O./
Examiner, Art Unit 2187

/Christian P. Chace/
Supervisory Patent Examiner, Art Unit 2187

Notice of References Cited	Application/Control No. 12/121,531	Applicant(s)/Patent Under Reexamination ROZAS, GUILLERMO J.	
	Examiner ALAN OTTO	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,086,429	02-1992	Gray et al.	714/13
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/13/2010								
	1	-								
	2	-								
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	15	-								
	16	-								
	17	-								
	18	-								
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	25	-								
	26	-								
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	33	✓								
	34	✓								
	35	✓								
	36	✓								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/13/2010								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								
	44	✓								
	45	✓								
	46	✓								
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	51	✓								
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	54	✓								
	55	✓								
	56	✓								
	57	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12121531	ROZAS, GUILLERMO J.
	Examiner	Art Unit
	ALAN OTTO	2187

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
East text search	3/15/10	AO
NPL search - Dialog	3/15/10	AO
Inventor name search (Palm and East)	3/15/10	AO
Consulted with examiners Brian Peugh, Jared Rutz, and Kevin Verbrugge	3/15/10	AO
711/130, 118, 133-134, 141, 144-146, 710/22, g06f12/00 (text search - see attached search results)	3/15/10	AO

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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CONFIRMATION NO. 7036

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/121,531	05/15/2008 RULE	712	2187	TRAN-P602

APPLICANTS
Guillermo J. Rozas, Los Gatos, CA;

**** CONTINUING DATA **************************
This application is a CON of 11/102,127 04/07/2005 PAT 7,376,798 YES /A.O./ 3/13/10

**** FOREIGN APPLICATIONS ************************** NO /A.O./ 3/13/10

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
06/03/2008

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /ALAN OTTO/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	25	4

ADDRESS

IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
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SAN JOSE, CA 95113
UNITED STATES

TITLE

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	rozas-guillermo.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L2	8	US-6938130-$.DID. OR US-6263407-$.DID. OR US-6625694-$.DID. OR US-5428761-$.DID. OR US-5701432-$.DID. OR US-6658536-$.DID. OR US-5974438-$.DID. OR US-6006299-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L3	5	US-6189074-$.DID. OR US-6304944-$.DID. OR US-6738864-$.DID. OR US-6779085-$.DID. OR US-6839813-$.DID.	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L4	897	(indicat$4 or mark $4) with read with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L5	1505	(indicat$4 or mark $4) with (read or access$3) with (cache adj line)	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L6	9602	711/130.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls. or 711/146.ccls. or 710/22.ccls. or 711/133-134.ccls. or 711/118.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48

L7	20090	g06f12/00.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L8	795	L5 same (bit or tag or indicator)	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L9	21126	L7 or L6	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L10	425	L8 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L11	204	L5 same (bit or tag or indicator) same (application or process or transaction or thread or (group near3 instruction))	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L12	111	L11 and L9	US-PGPUB; USPAT; USOCR	OR	ON	2010/03/15 11:48
L13	1021	((transaction$3 near3 system) or (transaction$3 near3 memory)) same (cache adj line)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L14	29	(L11 and L13) not L12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L15	3700	711/143.ccls. or 711/141.ccls. or 711/144.ccls. or 711/145.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L16	11893	valid adj (bit or tag or indicator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L17	3981	mesi or moesi	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48

L18	146	L15 and L16 and L17	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L19	81	shared with (read adj (miss or hit))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L20	2	L18 and L19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L21	504169	(compar$4 or check$4 or detect $4) with (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L22	1212	714/11-12.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L23	455	L21 and L22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L24	588	711/130.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L25	0	L23 and L24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L26	36225	shared adj (memory or cache)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48

L27	3873	L26 same L21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L28	38	L27 and L23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 11:48
L29	2	"7376798".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 13:04

EAST Search History (Interference)

< This search history is empty>

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C:\Documents and Settings\aotto\My Documents\EAST\Workspaces\12121531.wsp

Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-08)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	12/121,531
Filing Date	2008-05-15
First Named Inventor	Guillermo J. Rozas
Art Unit	2187
Examiner Name	Otto, Alan
Attorney Docket Number	TRAN-P602

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.O./	1	6938130		2005-08-30	Jacobson et al.	
/A.O./	2	6263407		2001-07-17	Arimilli et al.	
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/A.O./	6	6658536		2003-12-02	Arimilli et al.	
/A.O./	7	5974438		1999-10-26	Neufeld	
/A.O./	8	6006299		1999-12-21	Wang et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12/121,531
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	First Named Inventor	Guillermo J. Rozas
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	Examiner Name	Otto, Alan
	Attorney Docket Number	TRAN-P602

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Application Number	12121531
Filing Date	2008-05-15
First Named Inventor	Guillermo J. Rozas
Art Unit	~~2188~~ 2187
Examiner Name	Otto, Alan
Attorney Docket Number	TRAN-P084C1

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/A.O./	1	6189074		2001-02-13	Pedneau	
/A.O./	2	6304944		2001-10-16	Pedneau	
/A.O./	3	6738864		2004-05-18	Chauvel	
/A.O./	4	6779085		2004-08-17	Chauvel	
/A.O./	5	6839813		2005-01-04	Chauvel	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12121531
	Filing Date	2008-05-15
	First Named Inventor	Guillermo J. Rozas
	Art Unit	~~2483~~ 2187
	Examiner Name	Otto, Alan
	Attorney Docket Number	TRAN-P084C1

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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	1		☐

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Advanced Search:

Inspec - 1898 to date (INZZ)

limit

Search history:

No.	Database	Search term	Info added since	Results	
CP		[Clipboard]		0	-
1	Inspec - 1898 to date	(indicat$4 OR mark$4) WITH read WITH cache ADJ line	unrestricted	0	-
2	Inspec - 1898 to date	(indicat$4 OR mark$4) WITH (read OR access$3) WITH cache ADJ line	unrestricted	0	-
4	Inspec - 1898 to date	(transaction$3 NEAR system OR transaction$3 NEAR memory) SAME cache ADJ line	unrestricted	8	show titles
5	Inspec - 1898 to date	(bit OR tag OR indicator) SAME (application OR process OR transaction OR thread OR group NEAR instruction)	unrestricted	25752	show titles
6	Inspec - 1898 to date	(indicat$4 OR mark$4) WITH cache ADJ line	unrestricted	5	show titles
7	Inspec - 1898 to date	6 SAME 5	unrestricted	0	-
8	Inspec - 1898 to date	valid ADJ (bit OR tag OR indicator)	unrestricted	44	show titles
9	Inspec - 1898 to date	mesi OR moesi	unrestricted	89	show titles
10	Inspec - 1898 to date	8 AND 9	unrestricted	0	-
11	Inspec - 1898 to date	(compar$4 OR check$4 OR detect$4) WITH (memory OR cache)	unrestricted	11928	show titles
12	Inspec - 1898 to date	shared ADJ (memory OR cache)	unrestricted	11034	show titles
13	Inspec - 1898 to date	11 SAME 12	unrestricted	658	show titles
14	Inspec - 1898 to date	multiprocessor OR multiple ADJ processors OR second ADJ processor	unrestricted	30771	show titles
16	Inspec - 1898 to date	14 SAME 13 SAME error$2	unrestricted	14	show titles

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	12121531
Filing Date	2008-05-15
First Named Inventor	Guillermo J. Rozas
Art Unit	2183
Examiner Name	
Attorney Docket Number	TRAN-P084C1

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	2	6304944		2001-10-16	Pedneau	
	3	6738864		2004-05-18	Chauvel	
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	First Named Inventor	Guillermo J. Rozas
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	Examiner Name	
	Attorney Docket Number	TRAN-P084C1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12121531
	Filing Date	2008-05-15
	First Named Inventor	Guillermo J. Rozas
	Art Unit	2183
	Examiner Name	
	Attorney Docket Number	TRAN-P084C1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jose S. Garcia/	Date (YYYY-MM-DD)	2009-12-19
Name/Print	Jose S. Garcia	Registration Number	43628

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EFS ID:	6674939
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	Jose S. Garcia/Missy Isaac
Filer Authorized By:	Jose S. Garcia
Attorney Docket Number:	TRAN-P602
Receipt Date:	19-DEC-2009
Filing Date:	15-MAY-2008
Time Stamp:	20:47:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	TRAN-P084C1_IDS_transmittal_12-19-09.pdf	608520 003e3af7cf316e64a25520398cfcd90a30ea1942	no	4
Warnings:					
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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
12/121,531		2189	

OC000000031804973

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SAN JOSE, CA 95113

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/121,531	05/15/2008	2183	1490	TRAN-P602	25	4

CONFIRMATION NO. 7036

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OC00000030276640

Date Mailed: 06/04/2008

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Applicant(s)

Guillermo J. Rozas, Los Gatos, CA;

Assignment For Published Patent Application

TRANSMETA CORPORATION, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 45590

Domestic Priority data as claimed by applicant

This application is a CON of 11/102,127 04/07/2005 PAT 7,376,798

Foreign Applications

If Required, Foreign Filing License Granted: 06/03/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/121,531**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

Preliminary Class

712

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Rozas)
)
For: MEMORY MANAGEMENT)
METHODS AND SYSTEMS)
THAT SUPPORT CACHE)
CONSISTENCY)
_____)

A Continuation Application of:

In re Application of:)
)
Rozas) Examiner: OTTO, A.
)
Serial No.: 11/102,127) Art Unit: 2187
)
Filed: April 7, 2005) Confirmation No.: 6398
)
For: MEMORY MANAGEMENT)
METHODS AND SYSTEMS)
THAT SUPPORT CACHE)
CONSISTENCY)
_____)

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of this Continuation Application, please enter the following preliminary amendment. Amendments to the specification begin on page 2 of this paper. Amendments to the claims are reflected in the listing of claims, which begins on page 3 of this paper. Remarks begin on page 11 of this

paper. Attachments including a Marked-up Substitute Specification and a Clean Version Substitute Specification are attached to this paper.

AMENDMENTS TO THE SPECIFICATION

Please replace the original specification with the attached Marked-up Substitute Specification and Clean Version Substitute Specification pursuant to 37 C.F.R. Sections 1.121(b)(3) and 1.125. The Marked-up Substitute Specification and Clean Version Substitute Specification include no new matter. The Clean Version Substitute Specification is attached pursuant to 37 C.F.R. Sections 1.121(b)(3) and 1.125(c).

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims

1-32. (Canceled).

33. (New) A method of managing memory in a computer system, said method comprising:

executing a first group of instructions that causes a cache line of a cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

34. (New) The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

35. (New) The method of Claim 34 wherein said handling comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.

36. (New) The method of Claim 35 wherein said handling further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

37. (New) The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. (New) The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. (New) The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. (New) The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. (New) A computer system comprising:

a first processor;

a cache memory used by said first processor; and

a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising:

executing a first group of instructions that causes a cache line of said cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions using said first processor that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

42. (New) The computer system of Claim 41 wherein said method further comprises:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

43. (New) The computer system of Claim 42 wherein said method further comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.

44. (New) The computer system of Claim 43 wherein said method further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

45. (New) The computer system of Claim 44 wherein said method further comprises maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. (New) The computer system of Claim 45 wherein said method further comprises eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. (New) The computer system of Claim 41 wherein said method further comprises clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. (New) The computer system of Claim 41 wherein said method further comprises:

executing a plurality of groups of instructions in parallel on said first processor;

changing an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

49. (New) A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions on a first processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions on said first processor;

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. (New) The method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations.

51. (New) The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using said second state and said second state to indicate said cache line has been accessed; and

rolling back said first group and said second group of instructions before granting said access.

52. (New) The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. (New) The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. (New) The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. (New) The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. (New) A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and a plurality of indicator bits per entry, wherein a first indicator bit of said plurality of indicator bits is set to indicate that a cache line of said cache memory has been accessed because of a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit of said plurality of indicator bits is set to indicate that said cache line has been accessed because of a second group of instructions and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. (New) The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set.

REMARKS

This patent application is a Continuation of Patent Application Serial No. 11/102,127, filed on April 7, 2005. Claims 1-32 are canceled and new Claims 33-57 are added. Accordingly, after this Preliminary Amendment, Claims 33-57 are pending.

The disclosure has been amended. Moreover, the original disclosure has been replaced with the attached Marked-up Substitute Specification and Clean Version Substitute Specification pursuant to 37 C.F.R. Sections 1.121(b)(3) and 1.125. The Marked-up Substitute Specification and Clean Version Substitute Specification include no new matter. The Clean Version Substitute Specification is attached pursuant to 37 C.F.R. Sections 1.121(b)(3) and 1.125(c).

Please charge any associated fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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Attachments: 1. Marked-up Substitute Specification
2. Clean Version Substitute Specification

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

RELATED UNITED STATES PATENT APPLICATION

This application is a Continuation Application of the co-pending, commonly-owned U.S. Patent Application with Attorney Docket No. TRAN-P084, Serial No. 11/102,127, filed April 7, 2005, by G. J. Rozas, and entitled "Memory Management Methods and Systems That Support Cache Consistency."

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

Embodiments of the present invention relate to computer system memory, in particular the management of cache memory.

RELATED ART

With direct memory access (DMA), an input/output (I/O) system can issue read requests and writes directly to main memory without passing through the central processing unit (CPU). However, if the I/O system uses DMA to write to main memory, and changes data cached previously by the CPU, then the CPU will not receive the new data unless the CPU fetches the data from main memory. Also, for DMA reads, the CPU cache may contain more recent data than main memory, and so the I/O system will not receive the new data unless it reads the cache instead of main memory. Multiprocessor systems, particularly systems referred to as shared-memory simultaneous multiprocessor (SMP) architectures, have to deal with similar types of scenarios. The MESI (Modified, Exclusive, Shared, Invalid) protocol is a popular cache consistency (coherency)

protocol that addresses these issues. A modification of the MESI protocol is the MOESI (Modified, Owned, Exclusive, Shared, Invalid) protocol. These protocols are known in the art.

Constraints are also applied to memory operations to prevent processors and DMA systems from reordering memory operations at will. If, for example, each processor could reorder memory operations for optimization, code sequences that work on a single processor would not work on multiprocessor systems. One type of constraint can be referred to as sequential consistency. With sequential consistency, the legal orders of memory operations are those that are indistinguishable from strict interleaving of the operations from each thread of control. For example, for two threads, the operations of one thread can be interleaved with those of the other thread, but the order of operations within each thread is preserved.

There are different classes of high-level processor architectures with regard to operation reordering, optimization and speculation. One such class can be referred to as a lumped in-order architecture, and another such class as a lumped out-of-order architecture. With lumped in-order architectures, instructions are lumped into instruction groups that can be committed and rolled back atomically. Different instruction groups are committed sequentially and in order, but within an instruction group, arbitrary reordering and optimization can occur. Full speculation is possible within an instruction group, but speculation, reordering and optimization across instruction groups is limited. With lumped out-of-order architectures, instructions are lumped into instruction groups that

can be committed and rolled back atomically. Different groups can execute out of order but are committed in order.

SUMMARY OF THE INVENTION

A method or system that can maintain sequential consistency for lumped (in-order or out-of-order) architectures would be advantageous. Prior attempts to achieve a sequentially consistent, lumped architecture are limited with respect to the number of memory operations that can be included in an instruction group. Specifically, such attempts are limited to a single memory operation per instruction group. Embodiments in accordance with the present invention overcome this disadvantage.

According to one embodiment of the present invention, a group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed (e.g., read, write, store, load, etc.). In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended. If an external agent (e.g., another processor or a DMA system) snoops the cache and the cache line (or any other cache line in the cache, for that matter) is indicated as having been accessed, then the instruction group is rolled back and reissued. If an external agent (e.g., another processor or a DMA system) snoops the cache and no cache line is indicated as having been accessed, then the snoop can be processed using a conventional cache coherency protocol (MESI, for example).

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the present invention and, together with the description, serve to explain the principles of the invention. The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

Figure 1 is a block diagram of a portion of a computer system upon which embodiments of the present invention can be implemented.

Figure 2 is a block diagram of a cache and showing cache tags that are used according to one embodiment of the present invention.

Figure 3 is a flowchart of a method for managing memory in accordance with one embodiment of the present invention.

Figure 4 is a flowchart that continues from the flowchart of Figure 3.

Figure 5 is a flowchart of a method for replacing a cache line in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined,

compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, bytes, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "executing," “changing,” “using,” “accessing,” “handling,” “rolling back,” “maintaining,” “eliminating,” “setting,” “clearing,” “incrementing,” “decrementing,” “associating,” “granting,” "determining" or the like, refer to the action and processes (e.g., flowcharts 30, 40 and 50 of Figures 3, 4 and 5, respectively) of a computer system or similar intelligent electronic computing device (generally, a controller), that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Figure 1 is a block diagram of a portion of a computer system 5 upon which embodiments of the present invention can be implemented. Computer system 5 can include elements in addition to those illustrated in Figure 1. Generally speaking, embodiments in accordance with the present invention pertain to a computer system (or similar electronic device) that includes a

processor, a main memory, a cache associated with the processor, and one or more external agents that can access the main memory and the processor's cache.

In the example of Figure 1, computer system 5 includes a first processor 10, an optional second processor 11, and other optional processors 12 that are coupled to main memory 18 via bus 19. In the present embodiment, computer system 5 also includes a peripheral device 13 coupled to main memory 18 via bus 19. For ease of discussion, the processors 10, 11 and 12 and the peripheral device 13 may be collectively referred to herein as agents 10-13. Relative to processor 10, processors 11 and 12 and peripheral device 13 may be referred to as external agents; relative to processor 11, processors 10 and 12 and peripheral device 13 may be referred to as external agents; and so on.

In one embodiment, peripheral device 13 is capable of direct memory access (DMA). In general, DMA refers to a hardware circuit or software agent that can transfer data directly to or from main memory 18.

Associated with the processors 10-12 are first cache 14, optional second cache 15, and other optional caches 16, respectively. In one embodiment, each of the processors 10-12 has their own cache. The caches may be physically incorporated into the processors 10-12, or they may be physically external to the processors 10-12. In the present embodiment, each of the processors 10-12 can access each of the caches 14, 15 and 16 via bus 19.

In general, the agents 10-13 may each be executing a group of instructions according to a lumped in-order architecture or according to a lumped out-of-order architecture. The group of instructions can each include one or more memory operations (e.g., read, load, store, write, lock acquisition, etc.). The group of instructions can be demarcated by commit points (e.g., a commit ending one group of instructions can mark the beginning of the next group of instructions, which in turn ends at another commit). An instruction group is handled atomically (e.g., it is treated as a unit). An instruction (or instructions) in the group of instructions being executed by one of the agents 10-13 may seek access to a cache associated with any of the other agents 10-13.

In one embodiment, computer system 5 implements a cache coherency protocol such as, but not limited to, MESI (Modified, Exclusive, Shared, Invalid). According to the MESI protocol, a cache line is identified as being in one of the modified, exclusive, shared or invalid states. In the modified state, the cache line includes more recent information than main memory 18 (only the information in the cache line is valid because main memory 18 is not up to date), and no other cache holds the information in the cache line. In the exclusive state, the information in the cache line is not in any other cache and the information in the cache line is unmodified, and accordingly main memory 18 is up to date. In the shared state, the information in the cache line may be in one or more other caches, and main memory 18 is up to date. In the invalid state, the cache line does not contain valid information. MESI is consistent with sequential consistency.

Figure 2 is a block diagram of cache 14 according to one embodiment of the present invention. Cache 14 includes a number of cache lines exemplified by cache lines 21 and 22.

In the embodiment of Figure 2, a cache line tag is associated with each of the cache lines in cache 14. In one such embodiment, each cache line tag includes a number of cache coherency protocol bits. For example, cache coherency protocol bits 23 are associated with cache line 21, and cache coherency protocol bits 26 are associated with cache line 22. The cache coherency protocol bits 23 and 26 can be used to indicate the state of the cache lines 21 and 22, respectively, according to a cache coherency protocol such as the MESI protocol.

Furthermore, in the present embodiment, each cache line tag includes a number of additional bits referred to herein as observed bits for ease of discussion. For example, observed bits 24, 25, ..., N1 are associated with cache line 21, and observed bits 27, 28, ..., N2 are associated with cache line 22. The observed bits for cache 14 are associated with groups of instructions executed by the agent (e.g., processor 10) that is associated with cache 14. In one embodiment, each cache line tag is extended by one observed bit for each group of instructions that may be executed by processor 10 (Figure 1) at the same time. If, for example, processor 10 can execute five (5) instruction groups in parallel, then the cache line tags are each extended by 5 observed bits.

In the example of Figure 2, observed bits 24 and 27 (associated with cache line 21) are associated with instruction group A, and observed bits 25 and 28 (associated with cache line 22) are associated with instruction group B.

In one embodiment, an observed bit is set (e.g., set to a value of one) for a cache line in a cache if execution of an instruction in the group of instructions executed by the agent associated with that cache causes that cache line to be accessed (e.g., load, store, read, or write). For example, in one embodiment, observed bit 24 is set if an instruction in instruction group A, when executed by processor 10, causes cache line 21 to be accessed, because cache line 21 is in cache 14 associated with processor 10 (Figure 1). In such an embodiment, observed bit 27 (also associated with instruction group A) is not set unless cache line 22 is also accessed because of instruction group A.

In general, with reference to Figures 1 and 2, a group of instructions executed by processor 10 may result in multiple cache lines in cache 14 being accessed. For each cache line in cache 14 accessed because of a group of instructions executed by processor 10, the observed bit corresponding to that group of instructions is set. However, an observed bit associated with a cache line in cache 14 is not set if an instruction executed on an external agent 11-13 causes access (e.g., a snoop or interrogation, or perhaps a read) to that cache line. For example, in one embodiment, an instruction executed by an agent other than processor 10 that causes cache line 21 to be accessed will not set an observed bit for cache line 21.

In one embodiment, when execution of a group of instructions is ended (e.g., the instruction group is committed, rolled back, or aborted), each observed bit set by that group of instructions is cleared (e.g., unset, or set to a value of zero). For example, if instruction group A is committed (or retired), rolled back or aborted, any of the observed bits 24 and 27 that are set are cleared. From another perspective, the observed bits associated with instruction group A, if set, remain set until the execution of instruction group A is ended.

To summarize, in one embodiment, when an agent (e.g., processor 10) begins to execute a group of instructions, it allocates an observed bit for that group of instructions to each cache line in the cache associated with the agent (e.g., cache 14 associated with processor 10). If a cache line (e.g., cache line 21) has been accessed because of an instruction in an instruction group (e.g., instruction group A) being executed by processor 10, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 24) is set. If another cache line (e.g., cache line 22) has also been accessed because of an instruction in instruction group A, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 27) is set. When execution of an instruction group is ended, the observed bits associated with that instruction group are cleared, and thus the observed bits are available for subsequent instruction groups executed by the agent. For example, if instruction group A is committed, rolled back or aborted, then observed bits 24 and 27 are cleared.

In one embodiment, the observed bits are used in the following manner. Continuing with reference to Figures 1 and 2, if an external agent (e.g., another

processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that causes access to (or a request for access to) cache line 21, for example, and any of the observed bits 24, 25, ..., N1 have been set, then the instruction groups associated with the observed bits that are set are forced to roll back and then reissue. Also, any of the observed bits 24, 25, ..., N1 associated with cache line 21 that have been set are cleared. For example, if observed bits 24 and 25 have been set, then instruction group A (which corresponds to observed bit 24) and instruction group B (which corresponds to observed bit 25) are rolled back, and observed bits 24 and 25 are cleared. The rollback also clears the observed bits associated with other cache lines in cache 14 if those observed bits correspond to the groups of instructions that are rolled back. For example, if the instruction groups A and B are rolled back as mentioned above, then observed bits 27 and 28 are also cleared if those observed bits are set. The cache state transition occurs at this point, before the instruction groups A and B are reissued and are able to again cause cache line 21 (and perhaps cache line 22) to be accessed.

In general, if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, and an observed bit associated with that cache line has been set, then all the observed bits that have been set for that cache line are cleared, all the instruction groups corresponding to the observed bits that are cleared are rolled back, and the observed bits associated with the instruction groups that are rolled back are also cleared for other cache lines in cache 14.

In one embodiment, the rollbacks just described occur only if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, an

observed bit associated with that cache line has been set, and the cache line is not in the shared state. Again consider an example in which an external agent (e.g., another processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that seeks access to cache line 21. In one embodiment, in addition to checking the observed bits 24, 25, ..., N1 associated with cache line 21, the cache coherency protocol bits 23 are also checked to determine the state (e.g., the MESI state) of cache line 21. In a MESI embodiment, for example, if cache line 21 is in the shared state, and if the access from the external agent is for sharing (e.g., it is not exclusive), then access to cache line 21 can be granted without rolling back the instruction groups associated with the observed bits 24, 25, ..., N1 that are set.

In one embodiment, observed bits that are set are not forgotten (e.g., cleared) except in the case of a rollback, commit or abort. In such an embodiment, a cache line that has at least one of its observed bits set is not replaceable, although the cache line and its set observed bit(s) can be moved to another location. This can lead to a situation in which a cache line is needed, but no cache lines are available (that is, all cache lines have at least one of their respective bits set, so none of the cache lines can be replaced or moved). In one embodiment, if such a situation arises, the group of instructions that needs the cache line, as well as following instruction groups, is rolled back and then reissued.

To prevent instruction groups from being repeatedly rolled back, in one embodiment, the number of times each instruction group is rolled back is counted and compared to a threshold. In such an embodiment, if the number of times an

instruction group is rolled back exceeds the threshold, then the instruction group is rolled back for the last time. If it fails to execute to completion in the next attempt, the instruction group is reformed into a new instruction group that is reduced in size (e.g., one or more instructions is removed from the instruction group), and the counter for the new instruction group is set to zero. In the limiting case, the instruction group is eventually reduced to a single instruction that will be able to complete execution.

Figures 3 and 4 are flowcharts 30 and 40 of a method for managing memory in accordance with one embodiment of the present invention (the flowchart of Figure 4 is a continuation of the flowchart of Figure 3). Although specific steps are disclosed in flowcharts 30 and 40, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowcharts 30 and 40. It is appreciated that the steps in flowcharts 30 and 40 may be performed in an order different than presented, and that not all of the steps in flowcharts 30 and 40 may be performed. Some or all of the processes and steps of flowcharts 30 and 40 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory 18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 31 of Figure 3, a first group of instructions (e.g., instruction group A) is executed (e.g., by processor 10 of Figure 1). In one embodiment, the first group of instructions includes multiple memory operations (e.g., reads, writes, loads, stores, lock acquisition, etc.). At least one of the instructions in the first group of instructions, when executed, causes a cache line (e.g., cache line 21 of

Figure 2) in a cache associated with processor 10 (e.g., cache 14) to be accessed (e.g., read, written, etc.).

In step 32 of Figure 3, and continuing with reference to Figure 2, that instruction is executed, causing cache line 21 to be accessed.

In step 33 of Figure 3, with reference also to Figure 2, an indicator associated with the first group of instructions is changed, in order to indicate that cache line 21 has been accessed because of the first group of instructions. In one embodiment, the indicator is also associated with cache line 21. In one embodiment, a bit (e.g., observed bit 24) associated with cache line 21 and the first group of instructions is set. In one embodiment, cache line 21 is indicated as having been accessed (that is, for example, the observed bit remains set) until execution of the first group of instructions is ended (e.g., because of a roll back, commit or abort).

In step 34 of Figure 3, with reference also to Figure 1, a second group of instructions is executed by an agent external to processor 10 (e.g., processor 11 or 12 or a DMA agent such as peripheral device 13). At least one of the instructions in the second group of instructions, when executed, causes (or will cause) the cache line of interest (e.g., cache line 21 of Figure 2) to be accessed.

In step 35 of Figure 3, access to the cache line of interest (e.g., cache line 21 of Figure 2) is sought because of the second group of instructions. As will be seen, the first group of instructions is then handled depending on whether or not cache line 21 has been accessed because of the first group of instructions and is

identified as having been accessed (e.g., by an observed bit). That is, it is possible that cache line 21 is accessed because of the second group of instructions before it is accessed because of the first group of instructions.

In step 41 of Figure 4, with reference also to Figure 2, a determination is made with regard to whether or not the cache line of interest (e.g., cache line 21) has been accessed because of the first group of instructions. In one embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 43, and otherwise flowchart 44 proceeds to step 44. In another embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 42.

In step 42 of Figure 4, and with reference to Figure 2, a determination is made with regard to whether or not cache line 21 is in the shared state (e.g., according to the MESI protocol). If cache line 21 is in the shared state, then flowchart 40 proceeds to step 44, and otherwise flowchart 40 proceeds to step 43.

In step 43 of Figure 4, with reference also to Figure 2, the first group of instructions is atomically rolled back, and the observed bits 24, 25, ..., N1 associated with cache line 21 are cleared. Other observed bits, associated with other cache lines in cache 14 and corresponding to the first group of instructions, are also cleared if they are set. For example, if observed bit 27 (which also corresponds to the first group of instructions) is set, then it is also cleared by the rollback of the first group of instructions. Also, other groups of instructions

associated with any of the observed bits of cache 14 that are cleared are also rolled back. For example, if observed bit 25 is set, then it is cleared and the instruction group associated with observed bit 25 (e.g., instruction group B) is rolled back, which in turn results in observed bit 28 (which also corresponds to instruction group B) of cache line 22 being cleared.

In step 44 of Figure 4, access to cache line 21 (Figure 2) is granted.

In step 45 of Figure 4, in one embodiment, the number of times that the first group of instructions has been rolled back is counted. If the number of times the first group of instructions has been rolled back exceeds a threshold, then one or more instructions are eliminated from the first instruction group. Specifically, in one embodiment, the first group of instructions is reissued, and if the next execution attempt results in another rollback, then the first instruction group is reduced by one or more instructions.

Figure 5 is a flowchart 50 of a method for replacing a cache line in accordance with one embodiment of the present invention. Although specific steps are disclosed in flowchart 50, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowchart 50. It is appreciated that the steps in flowchart 50 may be performed in an order different than presented, and that not all of the steps in flowchart 50 may be performed. Some or all of the processes and steps of flowchart 50 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory

18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 51 of Figure 5, a number of instruction groups are executed in parallel using processor 10 (Figure 1), for example.

In step 52 of Figure 5, with reference also to Figures 1 and 2, each cache line in the cache associated with processor 10 (e.g., cache 14) that is accessed because of the groups of instructions being executed in step 51 is indicated as being accessed. For example, as previously described herein, an observed bit can be set for each cache line accessed because of the groups of instructions of step 51.

In step 53 of Figure 5, one of the instructions in one of the instruction groups attempts to replace a cache line.

In step 54, in one embodiment, if all of the cache lines in the cache of interest (e.g., cache 14) are indicated as having been accessed (e.g., at least one observed bit is set for each of the cache lines in cache 14, then the instruction group that has the instruction that attempted the cache line replacement (the instruction group of step 53) is rolled back.

In summary, methods and systems that can maintain sequential consistency for lumped (in-order or out-of-order) architectures are described. Significantly, embodiments in accordance with the present invention permit

sequentially consistent, lumped architectures in which multiple memory operations can be included in instruction groups.

Embodiments in accordance with the present invention can incorporate variations to the features described above. For systems with large speculation ability (e.g., potentially 20 or more active instruction groups), the cost (e.g., the storage cost) of the associated number of observed bits can be reduced in various ways. For example, a protocol can be established in which any external snoop causes all active instruction groups to roll back and reissue after the cache line state transition. In effect, such a protocol acts as if there is a single observed bit that is always set, except during the period of inactivity after rollback, and so no additional storage is needed for the observed bit. Alternatively, instead of an observed bit per cache line per instruction group, there can be an observed bit per instruction group.

Furthermore, new hardware structures can be added to track which cache lines have been accessed, without the storage of data. These hardware structures can be direct-mapped, set-associative, or fully-associative and of varying capacity.

Also, instead of having an observed bit per cache line per instruction group, a smaller memory structure (e.g., another cache, or a memory structure within main memory) that covers the whole cache address space and that has an observed bit per entry and per instruction group can be used. Each entry covers some portion of the cache address space, in such a way that every cache line address maps uniquely to an entry, but an entry maps to many cache lines. For

example, some subset of the address bits of a cache line can be used to identify an entry. The subset of the address bits are the address summary. When accessing a cache line, the entry corresponding to the address summary for the cache line is used to set the observed bits. Similarly, on a snoop request, the address is "summarized," and the entry corresponding to the summary is examined for the presence of observed bits. The observed bits are cleared when an instruction group is committed, rolled back, or aborted. To illustrate, consider a cache complex where each cache holds 32 bytes, so that, for example, the bottom five bits (bits 4-0) of an address indicate bytes within the same cache line. Furthermore, consider a 32-entry observed bit structure, where bits 9-5 of the cache line address are used to select an entry, and this entry holds the observed bits. Then, any two addresses that have the same bits 9-5 will use the same entry in the summary structure; that is, they collide. This can mean that when a snoop comes, an instruction group that did not really conflict may be rolled back, because there is a conflict/collision in the summary structure even though there would not have been a conflict/collision in the cache. Thus, there is a tradeoff between the size of the summary structure and the overhead incurred by the "spurious" rollbacks due to collisions.

Embodiments in accordance with the present invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

~~1. A method of managing memory in a computer system, said method comprising:~~

~~executing a first group of instructions, wherein said first group of instructions comprises multiple memory operations and a first instruction that when executed causes a cache line of a cache memory to be read; and~~

~~in response to said first instruction causing said cache line to be read, changing an indicator associated with said first group of instructions to indicate that said cache line has been read, wherein said cache line is so indicated as having been read until execution of said first group of instructions is ended.~~

~~2. The method of Claim 1 further comprising:~~

~~executing a second group of instructions, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed, and wherein said first group of instructions is associated with a thread executing on a first processor and said second group of instructions is associated with a thread executing on an agent external to said first processor;~~

~~in response to said second instruction seeking access to said cache line, using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and~~

~~handling said first group of instructions according to said result.~~

~~3. The method of Claim 2 wherein said handling comprises rolling back said first group of instructions before granting said access provided said indicator~~

~~indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.~~

~~4. The method of Claim 3 wherein said handling further comprises:~~

~~determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and~~

~~rolling back said first group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.~~

~~5. The method of Claim 3 further comprising maintaining a count of how many times said first group of instructions has been rolled back.~~

~~6. The method of Claim 5 further comprising eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.~~

~~7. The method of Claim 2 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).~~

~~8. The method of Claim 2 wherein said indicator comprises one bit per instruction group for each group of instructions being executed at a same time by said first processor.~~

9. The method of Claim 2 wherein said indicator comprises one bit per cache line per instruction group for each group of instructions being executed at a same time by said first processor.

10. The method of Claim 1 further comprising:

setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and

clearing said bit when said execution of said first group of instructions is ended.

11. The method of Claim 1 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

~~12. A computer system comprising:~~

~~a first processor;~~

~~a cache memory used by said first processor; and~~

~~a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising:~~

~~executing a first group of instructions using said first processor, wherein said first group of instructions includes multiple memory operations and a first instruction that when executed causes a cache line of said cache memory to be read; and~~

~~in response to said first instruction causing said cache line to be read, changing an indicator associated with said first group of instructions to indicate that said cache line has been read, wherein said cache line is so indicated as having been read until execution of said first group of instructions is ended.~~

~~13. The computer system of Claim 12 wherein said method further comprises:~~

~~executing a second group of instructions using an agent coupled to said cache memory, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed, and wherein said agent is external to said first processor;~~

~~in response to said second instruction seeking access to said cache line, using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and~~

~~handling said first group of instructions according to said result.~~

~~14. The computer system of Claim 13 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).~~

~~15. The computer system of Claim 13 wherein said method further comprises rolling back said first group of instructions before granting said access provided said indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.~~

~~16. The computer system of Claim 15 wherein said method further comprises:~~

~~determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and~~

~~rolling back said first group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.~~

~~17. The computer system of Claim 15 wherein said method further comprises maintaining a count of how many times said first group of instructions is rolled back.~~

~~18. The computer system of Claim 17 wherein said method further comprises eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.~~

~~19. The computer system of Claim 17 wherein said indicator comprises one bit per instruction group for each group of instructions being executed at a same time by said first processor.~~

~~20. The computer system of Claim 17 wherein said indicator comprises one bit per cache line per instruction group for each group of instructions being executed at a same time by said first processor.~~

~~21. The computer system of Claim 12 wherein said method further comprises:~~

~~setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and~~

~~clearing said bit when said execution of said first group of instructions is ended.~~

~~22. The computer system of Claim 12 wherein said method further comprises:~~

~~executing a plurality of groups of instructions in parallel on said first processor;~~

~~changing an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and~~

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

23. A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions;

associating a first state with a cache line, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

associating a second state with said cache line during said executing, wherein said second state indicates that said cache line has been accessed because of a first instruction of said first group of instructions and wherein said second state is cleared when execution of said first group of instructions is ended.

24. The method of Claim 23 wherein said first group of instructions includes multiple memory operations.

25. The method of Claim 23 further comprising:

executing a second group of instructions, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed and wherein said first group of instructions is associated with a thread executing on a first processor and wherein said second group of

instructions is associated with a thread executing on an agent external to said first processor;

in response to said second instruction seeking access to said cache line, using said second state to indicate said cache line has been accessed because of said first instruction; and

rolling back said first group of instructions before granting said access.

26. The method of Claim 25 wherein said rolling back is only performed provided said cache line is in other than said shared state.

27. The method of Claim 25 further comprising maintaining a count of how many times said first group of instructions is rolled back.

28. The method of Claim 27 further comprising eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.

29. The method of Claim 25 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).

30. The method of Claim 23 wherein said second state is indicated by:

setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and

clearing said bit when said execution of said first group of instructions is ended.

~~31. A computer system comprising:~~

~~a processor;~~

~~a cache memory coupled to said processor and having a plurality of cache lines; and~~

~~a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and an indicator bit per entry, wherein said indicator bit is set to indicate that a cache line of said cache memory has been accessed because of an instruction of a group of instructions and wherein said indicator bit is cleared when execution of said group of instructions is ended, and wherein each of said entries covers the address space of said cache memory such that a cache line maps uniquely to an entry but an entry maps to multiple cache lines.~~

~~32. The computer system of Claim 31 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set.~~

33. A method of managing memory in a computer system, said method comprising:

executing a first group of instructions that causes a cache line of a cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

34. The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

35. The method of Claim 34 wherein said handling comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.

36. The method of Claim 35 wherein said handling further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read, and otherwise

granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

37. The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache

memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. A computer system comprising:

a first processor;

a cache memory used by said first processor; and

a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising:

executing a first group of instructions that causes a cache line of said cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions using said first processor that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

42. The computer system of Claim 41 wherein said method further comprises:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

43. The computer system of Claim 42 wherein said method further comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.

44. The computer system of Claim 43 wherein said method further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

45. The computer system of Claim 44 wherein said method further comprises maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. The computer system of Claim 45 wherein said method further comprises eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. The computer system of Claim 41 wherein said method further comprises clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. The computer system of Claim 41 wherein said method further comprises:

executing a plurality of groups of instructions in parallel on said first processor;

changing an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

49. A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions on a first processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions on said first processor;

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. The method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations.

51. The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using said second state and said second state to indicate said cache line has been accessed; and

rolling back said first group and said second group of instructions before granting said access.

52. The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line, wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and a plurality of indicator bits per entry, wherein a first indicator bit of said plurality of indicator bits is set to indicate that a cache line of

said cache memory has been accessed because of a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit of said plurality of indicator bits is set to indicate that said cache line has been accessed because of a second group of instructions and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set.

MEMORY MANAGEMENT METHODS AND SYSTEMS
THAT SUPPORT CACHE CONSISTENCY

ABSTRACT

Methods and systems for maintaining cache consistency are described. A group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed. In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended.

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

RELATED UNITED STATES PATENT APPLICATION

This application is a Continuation Application of the co-pending, commonly-owned U.S. Patent Application with Attorney Docket No. TRAN-P084, Serial No. 11/102,127, filed April 7, 2005, by G. J. Rozas, and entitled "Memory Management Methods and Systems That Support Cache Consistency."

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

Embodiments of the present invention relate to computer system memory, in particular the management of cache memory.

RELATED ART

With direct memory access (DMA), an input/output (I/O) system can issue read requests and writes directly to main memory without passing through the central processing unit (CPU). However, if the I/O system uses DMA to write to main memory, and changes data cached previously by the CPU, then the CPU will not receive the new data unless the CPU fetches the data from main memory. Also, for DMA reads, the CPU cache may contain more recent data than main memory, and so the I/O system will not receive the new data unless it reads the cache instead of main memory. Multiprocessor systems, particularly systems referred to as shared-memory simultaneous multiprocessor (SMP) architectures, have to deal with similar types of scenarios. The MESI (Modified, Exclusive, Shared, Invalid) protocol is a popular cache consistency (coherency)

protocol that addresses these issues. A modification of the MESI protocol is the MOESI (Modified, Owned, Exclusive, Shared, Invalid) protocol. These protocols are known in the art.

Constraints are also applied to memory operations to prevent processors and DMA systems from reordering memory operations at will. If, for example, each processor could reorder memory operations for optimization, code sequences that work on a single processor would not work on multiprocessor systems. One type of constraint can be referred to as sequential consistency. With sequential consistency, the legal orders of memory operations are those that are indistinguishable from strict interleaving of the operations from each thread of control. For example, for two threads, the operations of one thread can be interleaved with those of the other thread, but the order of operations within each thread is preserved.

There are different classes of high-level processor architectures with regard to operation reordering, optimization and speculation. One such class can be referred to as a lumped in-order architecture, and another such class as a lumped out-of-order architecture. With lumped in-order architectures, instructions are lumped into instruction groups that can be committed and rolled back atomically. Different instruction groups are committed sequentially and in order, but within an instruction group, arbitrary reordering and optimization can occur. Full speculation is possible within an instruction group, but speculation, reordering and optimization across instruction groups is limited. With lumped out-of-order architectures, instructions are lumped into instruction groups that

can be committed and rolled back atomically. Different groups can execute out of order but are committed in order.

SUMMARY OF THE INVENTION

A method or system that can maintain sequential consistency for lumped (in-order or out-of-order) architectures would be advantageous. Prior attempts to achieve a sequentially consistent, lumped architecture are limited with respect to the number of memory operations that can be included in an instruction group. Specifically, such attempts are limited to a single memory operation per instruction group. Embodiments in accordance with the present invention overcome this disadvantage.

According to one embodiment of the present invention, a group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed (e.g., read, write, store, load, etc.). In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended. If an external agent (e.g., another processor or a DMA system) snoops the cache and the cache line (or any other cache line in the cache, for that matter) is indicated as having been accessed, then the instruction group is rolled back and reissued. If an external agent (e.g., another processor or a DMA system) snoops the cache and no cache line is indicated as having been accessed, then the snoop can be processed using a conventional cache coherency protocol (MESI, for example).

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the present invention and, together with the description, serve to explain the principles of the invention. The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

Figure 1 is a block diagram of a portion of a computer system upon which embodiments of the present invention can be implemented.

Figure 2 is a block diagram of a cache and showing cache tags that are used according to one embodiment of the present invention.

Figure 3 is a flowchart of a method for managing memory in accordance with one embodiment of the present invention.

Figure 4 is a flowchart that continues from the flowchart of Figure 3.

Figure 5 is a flowchart of a method for replacing a cache line in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined,

compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, bytes, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "executing," “changing,” “using,” “accessing,” “handling,” “rolling back,” “maintaining,” “eliminating,” “setting,” “clearing,” “incrementing,” “decrementing,” “associating,” “granting,” "determining" or the like, refer to the action and processes (e.g., flowcharts 30, 40 and 50 of Figures 3, 4 and 5, respectively) of a computer system or similar intelligent electronic computing device (generally, a controller), that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Figure 1 is a block diagram of a portion of a computer system 5 upon which embodiments of the present invention can be implemented. Computer system 5 can include elements in addition to those illustrated in Figure 1. Generally speaking, embodiments in accordance with the present invention pertain to a computer system (or similar electronic device) that includes a

processor, a main memory, a cache associated with the processor, and one or more external agents that can access the main memory and the processor's cache.

In the example of Figure 1, computer system 5 includes a first processor 10, an optional second processor 11, and other optional processors 12 that are coupled to main memory 18 via bus 19. In the present embodiment, computer system 5 also includes a peripheral device 13 coupled to main memory 18 via bus 19. For ease of discussion, the processors 10, 11 and 12 and the peripheral device 13 may be collectively referred to herein as agents 10-13. Relative to processor 10, processors 11 and 12 and peripheral device 13 may be referred to as external agents; relative to processor 11, processors 10 and 12 and peripheral device 13 may be referred to as external agents; and so on.

In one embodiment, peripheral device 13 is capable of direct memory access (DMA). In general, DMA refers to a hardware circuit or software agent that can transfer data directly to or from main memory 18.

Associated with the processors 10-12 are first cache 14, optional second cache 15, and other optional caches 16, respectively. In one embodiment, each of the processors 10-12 has their own cache. The caches may be physically incorporated into the processors 10-12, or they may be physically external to the processors 10-12. In the present embodiment, each of the processors 10-12 can access each of the caches 14, 15 and 16 via bus 19.

In general, the agents 10-13 may each be executing a group of instructions according to a lumped in-order architecture or according to a lumped out-of-order architecture. The group of instructions can each include one or more memory operations (e.g., read, load, store, write, lock acquisition, etc.). The group of instructions can be demarcated by commit points (e.g., a commit ending one group of instructions can mark the beginning of the next group of instructions, which in turn ends at another commit). An instruction group is handled atomically (e.g., it is treated as a unit). An instruction (or instructions) in the group of instructions being executed by one of the agents 10-13 may seek access to a cache associated with any of the other agents 10-13.

In one embodiment, computer system 5 implements a cache coherency protocol such as, but not limited to, MESI (Modified, Exclusive, Shared, Invalid). According to the MESI protocol, a cache line is identified as being in one of the modified, exclusive, shared or invalid states. In the modified state, the cache line includes more recent information than main memory 18 (only the information in the cache line is valid because main memory 18 is not up to date), and no other cache holds the information in the cache line. In the exclusive state, the information in the cache line is not in any other cache and the information in the cache line is unmodified, and accordingly main memory 18 is up to date. In the shared state, the information in the cache line may be in one or more other caches, and main memory 18 is up to date. In the invalid state, the cache line does not contain valid information. MESI is consistent with sequential consistency.

Figure 2 is a block diagram of cache 14 according to one embodiment of the present invention. Cache 14 includes a number of cache lines exemplified by cache lines 21 and 22.

In the embodiment of Figure 2, a cache line tag is associated with each of the cache lines in cache 14. In one such embodiment, each cache line tag includes a number of cache coherency protocol bits. For example, cache coherency protocol bits 23 are associated with cache line 21, and cache coherency protocol bits 26 are associated with cache line 22. The cache coherency protocol bits 23 and 26 can be used to indicate the state of the cache lines 21 and 22, respectively, according to a cache coherency protocol such as the MESI protocol.

Furthermore, in the present embodiment, each cache line tag includes a number of additional bits referred to herein as observed bits for ease of discussion. For example, observed bits 24, 25, ..., N1 are associated with cache line 21, and observed bits 27, 28, ..., N2 are associated with cache line 22. The observed bits for cache 14 are associated with groups of instructions executed by the agent (e.g., processor 10) that is associated with cache 14. In one embodiment, each cache line tag is extended by one observed bit for each group of instructions that may be executed by processor 10 (Figure 1) at the same time. If, for example, processor 10 can execute five (5) instruction groups in parallel, then the cache line tags are each extended by 5 observed bits.

In the example of Figure 2, observed bits 24 and 27 (associated with cache line 21) are associated with instruction group A, and observed bits 25 and 28 (associated with cache line 22) are associated with instruction group B.

In one embodiment, an observed bit is set (e.g., set to a value of one) for a cache line in a cache if execution of an instruction in the group of instructions executed by the agent associated with that cache causes that cache line to be accessed (e.g., load, store, read, or write). For example, in one embodiment, observed bit 24 is set if an instruction in instruction group A, when executed by processor 10, causes cache line 21 to be accessed, because cache line 21 is in cache 14 associated with processor 10 (Figure 1). In such an embodiment, observed bit 27 (also associated with instruction group A) is not set unless cache line 22 is also accessed because of instruction group A.

In general, with reference to Figures 1 and 2, a group of instructions executed by processor 10 may result in multiple cache lines in cache 14 being accessed. For each cache line in cache 14 accessed because of a group of instructions executed by processor 10, the observed bit corresponding to that group of instructions is set. However, an observed bit associated with a cache line in cache 14 is not set if an instruction executed on an external agent 11-13 causes access (e.g., a snoop or interrogation, or perhaps a read) to that cache line. For example, in one embodiment, an instruction executed by an agent other than processor 10 that causes cache line 21 to be accessed will not set an observed bit for cache line 21.

In one embodiment, when execution of a group of instructions is ended (e.g., the instruction group is committed, rolled back, or aborted), each observed bit set by that group of instructions is cleared (e.g., unset, or set to a value of zero). For example, if instruction group A is committed (or retired), rolled back or aborted, any of the observed bits 24 and 27 that are set are cleared. From another perspective, the observed bits associated with instruction group A, if set, remain set until the execution of instruction group A is ended.

To summarize, in one embodiment, when an agent (e.g., processor 10) begins to execute a group of instructions, it allocates an observed bit for that group of instructions to each cache line in the cache associated with the agent (e.g., cache 14 associated with processor 10). If a cache line (e.g., cache line 21) has been accessed because of an instruction in an instruction group (e.g., instruction group A) being executed by processor 10, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 24) is set. If another cache line (e.g., cache line 22) has also been accessed because of an instruction in instruction group A, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 27) is set. When execution of an instruction group is ended, the observed bits associated with that instruction group are cleared, and thus the observed bits are available for subsequent instruction groups executed by the agent. For example, if instruction group A is committed, rolled back or aborted, then observed bits 24 and 27 are cleared.

In one embodiment, the observed bits are used in the following manner. Continuing with reference to Figures 1 and 2, if an external agent (e.g., another

processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that causes access to (or a request for access to) cache line 21, for example, and any of the observed bits 24, 25, ..., N1 have been set, then the instruction groups associated with the observed bits that are set are forced to roll back and then reissue. Also, any of the observed bits 24, 25, ..., N1 associated with cache line 21 that have been set are cleared. For example, if observed bits 24 and 25 have been set, then instruction group A (which corresponds to observed bit 24) and instruction group B (which corresponds to observed bit 25) are rolled back, and observed bits 24 and 25 are cleared. The rollback also clears the observed bits associated with other cache lines in cache 14 if those observed bits correspond to the groups of instructions that are rolled back. For example, if the instruction groups A and B are rolled back as mentioned above, then observed bits 27 and 28 are also cleared if those observed bits are set. The cache state transition occurs at this point, before the instruction groups A and B are reissued and are able to again cause cache line 21 (and perhaps cache line 22) to be accessed.

In general, if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, and an observed bit associated with that cache line has been set, then all the observed bits that have been set for that cache line are cleared, all the instruction groups corresponding to the observed bits that are cleared are rolled back, and the observed bits associated with the instruction groups that are rolled back are also cleared for other cache lines in cache 14.

In one embodiment, the rollbacks just described occur only if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, an

observed bit associated with that cache line has been set, and the cache line is not in the shared state. Again consider an example in which an external agent (e.g., another processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that seeks access to cache line 21. In one embodiment, in addition to checking the observed bits 24, 25, ..., N1 associated with cache line 21, the cache coherency protocol bits 23 are also checked to determine the state (e.g., the MESI state) of cache line 21. In a MESI embodiment, for example, if cache line 21 is in the shared state, and if the access from the external agent is for sharing (e.g., it is not exclusive), then access to cache line 21 can be granted without rolling back the instruction groups associated with the observed bits 24, 25, ..., N1 that are set.

In one embodiment, observed bits that are set are not forgotten (e.g., cleared) except in the case of a rollback, commit or abort. In such an embodiment, a cache line that has at least one of its observed bits set is not replaceable, although the cache line and its set observed bit(s) can be moved to another location. This can lead to a situation in which a cache line is needed, but no cache lines are available (that is, all cache lines have at least one of their respective bits set, so none of the cache lines can be replaced or moved). In one embodiment, if such a situation arises, the group of instructions that needs the cache line, as well as following instruction groups, is rolled back and then reissued.

To prevent instruction groups from being repeatedly rolled back, in one embodiment, the number of times each instruction group is rolled back is counted and compared to a threshold. In such an embodiment, if the number of times an

instruction group is rolled back exceeds the threshold, then the instruction group is rolled back for the last time. If it fails to execute to completion in the next attempt, the instruction group is reformed into a new instruction group that is reduced in size (e.g., one or more instructions is removed from the instruction group), and the counter for the new instruction group is set to zero. In the limiting case, the instruction group is eventually reduced to a single instruction that will be able to complete execution.

Figures 3 and 4 are flowcharts 30 and 40 of a method for managing memory in accordance with one embodiment of the present invention (the flowchart of Figure 4 is a continuation of the flowchart of Figure 3). Although specific steps are disclosed in flowcharts 30 and 40, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowcharts 30 and 40. It is appreciated that the steps in flowcharts 30 and 40 may be performed in an order different than presented, and that not all of the steps in flowcharts 30 and 40 may be performed. Some or all of the processes and steps of flowcharts 30 and 40 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory 18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 31 of Figure 3, a first group of instructions (e.g., instruction group A) is executed (e.g., by processor 10 of Figure 1). In one embodiment, the first group of instructions includes multiple memory operations (e.g., reads, writes, loads, stores, lock acquisition, etc.). At least one of the instructions in the first group of instructions, when executed, causes a cache line (e.g., cache line 21 of

Figure 2) in a cache associated with processor 10 (e.g., cache 14) to be accessed (e.g., read, written, etc.).

In step 32 of Figure 3, and continuing with reference to Figure 2, that instruction is executed, causing cache line 21 to be accessed.

In step 33 of Figure 3, with reference also to Figure 2, an indicator associated with the first group of instructions is changed, in order to indicate that cache line 21 has been accessed because of the first group of instructions. In one embodiment, the indicator is also associated with cache line 21. In one embodiment, a bit (e.g., observed bit 24) associated with cache line 21 and the first group of instructions is set. In one embodiment, cache line 21 is indicated as having been accessed (that is, for example, the observed bit remains set) until execution of the first group of instructions is ended (e.g., because of a roll back, commit or abort).

In step 34 of Figure 3, with reference also to Figure 1, a second group of instructions is executed by an agent external to processor 10 (e.g., processor 11 or 12 or a DMA agent such as peripheral device 13). At least one of the instructions in the second group of instructions, when executed, causes (or will cause) the cache line of interest (e.g., cache line 21 of Figure 2) to be accessed.

In step 35 of Figure 3, access to the cache line of interest (e.g., cache line 21 of Figure 2) is sought because of the second group of instructions. As will be seen, the first group of instructions is then handled depending on whether or not cache line 21 has been accessed because of the first group of instructions and is

identified as having been accessed (e.g., by an observed bit). That is, it is possible that cache line 21 is accessed because of the second group of instructions before it is accessed because of the first group of instructions.

In step 41 of Figure 4, with reference also to Figure 2, a determination is made with regard to whether or not the cache line of interest (e.g., cache line 21) has been accessed because of the first group of instructions. In one embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 43, and otherwise flowchart 44 proceeds to step 44. In another embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 42.

In step 42 of Figure 4, and with reference to Figure 2, a determination is made with regard to whether or not cache line 21 is in the shared state (e.g., according to the MESI protocol). If cache line 21 is in the shared state, then flowchart 40 proceeds to step 44, and otherwise flowchart 40 proceeds to step 43.

In step 43 of Figure 4, with reference also to Figure 2, the first group of instructions is atomically rolled back, and the observed bits 24, 25, ..., N1 associated with cache line 21 are cleared. Other observed bits, associated with other cache lines in cache 14 and corresponding to the first group of instructions, are also cleared if they are set. For example, if observed bit 27 (which also corresponds to the first group of instructions) is set, then it is also cleared by the rollback of the first group of instructions. Also, other groups of instructions

associated with any of the observed bits of cache 14 that are cleared are also rolled back. For example, if observed bit 25 is set, then it is cleared and the instruction group associated with observed bit 25 (e.g., instruction group B) is rolled back, which in turn results in observed bit 28 (which also corresponds to instruction group B) of cache line 22 being cleared.

In step 44 of Figure 4, access to cache line 21 (Figure 2) is granted.

In step 45 of Figure 4, in one embodiment, the number of times that the first group of instructions has been rolled back is counted. If the number of times the first group of instructions has been rolled back exceeds a threshold, then one or more instructions are eliminated from the first instruction group. Specifically, in one embodiment, the first group of instructions is reissued, and if the next execution attempt results in another rollback, then the first instruction group is reduced by one or more instructions.

Figure 5 is a flowchart 50 of a method for replacing a cache line in accordance with one embodiment of the present invention. Although specific steps are disclosed in flowchart 50, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowchart 50. It is appreciated that the steps in flowchart 50 may be performed in an order different than presented, and that not all of the steps in flowchart 50 may be performed. Some or all of the processes and steps of flowchart 50 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory

18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 51 of Figure 5, a number of instruction groups are executed in parallel using processor 10 (Figure 1), for example.

In step 52 of Figure 5, with reference also to Figures 1 and 2, each cache line in the cache associated with processor 10 (e.g., cache 14) that is accessed because of the groups of instructions being executed in step 51 is indicated as being accessed. For example, as previously described herein, an observed bit can be set for each cache line accessed because of the groups of instructions of step 51.

In step 53 of Figure 5, one of the instructions in one of the instruction groups attempts to replace a cache line.

In step 54, in one embodiment, if all of the cache lines in the cache of interest (e.g., cache 14) are indicated as having been accessed (e.g., at least one observed bit is set for each of the cache lines in cache 14, then the instruction group that has the instruction that attempted the cache line replacement (the instruction group of step 53) is rolled back.

In summary, methods and systems that can maintain sequential consistency for lumped (in-order or out-of-order) architectures are described. Significantly, embodiments in accordance with the present invention permit

sequentially consistent, lumped architectures in which multiple memory operations can be included in instruction groups.

Embodiments in accordance with the present invention can incorporate variations to the features described above. For systems with large speculation ability (e.g., potentially 20 or more active instruction groups), the cost (e.g., the storage cost) of the associated number of observed bits can be reduced in various ways. For example, a protocol can be established in which any external snoop causes all active instruction groups to roll back and reissue after the cache line state transition. In effect, such a protocol acts as if there is a single observed bit that is always set, except during the period of inactivity after rollback, and so no additional storage is needed for the observed bit. Alternatively, instead of an observed bit per cache line per instruction group, there can be an observed bit per instruction group.

Furthermore, new hardware structures can be added to track which cache lines have been accessed, without the storage of data. These hardware structures can be direct-mapped, set-associative, or fully-associative and of varying capacity.

Also, instead of having an observed bit per cache line per instruction group, a smaller memory structure (e.g., another cache, or a memory structure within main memory) that covers the whole cache address space and that has an observed bit per entry and per instruction group can be used. Each entry covers some portion of the cache address space, in such a way that every cache line address maps uniquely to an entry, but an entry maps to many cache lines. For

example, some subset of the address bits of a cache line can be used to identify an entry. The subset of the address bits are the address summary. When accessing a cache line, the entry corresponding to the address summary for the cache line is used to set the observed bits. Similarly, on a snoop request, the address is "summarized," and the entry corresponding to the summary is examined for the presence of observed bits. The observed bits are cleared when an instruction group is committed, rolled back, or aborted. To illustrate, consider a cache complex where each cache holds 32 bytes, so that, for example, the bottom five bits (bits 4-0) of an address indicate bytes within the same cache line. Furthermore, consider a 32-entry observed bit structure, where bits 9-5 of the cache line address are used to select an entry, and this entry holds the observed bits. Then, any two addresses that have the same bits 9-5 will use the same entry in the summary structure; that is, they collide. This can mean that when a snoop comes, an instruction group that did not really conflict may be rolled back, because there is a conflict/collision in the summary structure even though there would not have been a conflict/collision in the cache. Thus, there is a tradeoff between the size of the summary structure and the overhead incurred by the "spurious" rollbacks due to collisions.

Embodiments in accordance with the present invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

33. A method of managing memory in a computer system, said method comprising:

executing a first group of instructions that causes a cache line of a cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

34. The method of Claim 33 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

35. The method of Claim 34 wherein said handling comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise

granting said access without rolling back said first group and said second group of instructions.

36. The method of Claim 35 wherein said handling further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

37. The method of Claim 35 further comprising maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

38. The method of Claim 37 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

39. The method of Claim 33 further comprising clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

40. The method of Claim 33 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

41. A computer system comprising:

a first processor;

a cache memory used by said first processor; and

a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising:

executing a first group of instructions that causes a cache line of said cache memory to be read;

setting a first bit of an indicator associated with said cache line to indicate that said cache line has been read;

executing a second group of instructions using said first processor that causes said cache line to be read; and

setting a second bit of said indicator while said first bit remains set to indicate said cache line has been accessed by both said first group and said second group of instructions.

42. The computer system of Claim 41 wherein said method further comprises:

executing a third group of instructions that causes said cache line to be accessed;

using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group and said second group of instructions according to said result.

43. The computer system of Claim 42 wherein said method further comprises rolling back said first group and said second group of instructions before granting said access provided said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions.

44. The computer system of Claim 43 wherein said method further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group and said second group of instructions and then granting said access provided said cache line is in other than said shared state

and said indicator indicates said cache line has been read, and otherwise granting said access without rolling back said first group and said second group of instructions only when said cache line is in said shared state.

45. The computer system of Claim 44 wherein said method further comprises maintaining a first count of how many times said first group of instructions has been rolled back and a second count of how many times said second group of instructions has been rolled back.

46. The computer system of Claim 45 wherein said method further comprises eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

47. The computer system of Claim 41 wherein said method further comprises clearing said first bit when said execution of said first group of instructions is ended, wherein said second bit remains set until execution of said second group of instructions is ended.

48. The computer system of Claim 41 wherein said method further comprises:

executing a plurality of groups of instructions in parallel on said first processor;

changing an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

49. A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions on a first processor;

associating a first state with a cache line in a cache comprising a plurality of cache lines, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state;

associating a second state with said cache line during said executing of said first group of instructions, wherein said second state indicates that said cache line has been accessed because of said first group of instructions;

executing a second group of instructions on said first processor;

associating a third state with said cache line during said executing of said second group of instructions, wherein said third state indicates that said cache line has been accessed because of said second group of instructions.

50. The method of Claim 49 wherein said first group and said second group of instructions each includes multiple memory operations.

51. The method of Claim 49 further comprising:

executing a third group of instructions that causes said cache line to be accessed;

using said second state and said second state to indicate said cache line has been accessed; and

rolling back said first group and said second group of instructions before granting said access.

52. The method of Claim 51 wherein said rolling back is only performed provided said cache line is in other than said shared state.

53. The method of Claim 51 further comprising maintaining a first count of how many times said first group of instructions is rolled back and a second count of how many times said second group of instructions is rolled back.

54. The method of Claim 53 further comprising eliminating one or more instructions from said first group of instructions if said first count exceeds a threshold and eliminating one or more instructions from said second group of instructions if said second count exceeds said threshold.

55. The method of Claim 49 wherein said second state is indicated by setting a first bit associated with said cache line, wherein said first bit is cleared when said execution of said first group of instructions is ended, and wherein said third state is indicated by setting a second bit associated with said cache line,

wherein said second bit is cleared when said execution of said second group of instructions is ended.

56. A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and a plurality of indicator bits per entry, wherein a first indicator bit of said plurality of indicator bits is set to indicate that a cache line of said cache memory has been accessed because of a first group of instructions and wherein said first indicator bit is cleared when execution of said first group of instructions is ended, wherein a second indicator bit of said plurality of indicator bits is set to indicate that said cache line has been accessed because of a second group of instructions and wherein said second indicator bit is cleared when execution of said second group of instructions is ended.

57. The computer system of Claim 56 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set.

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

ABSTRACT

Methods and systems for maintaining cache consistency are described. A group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed. In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TRAN-P602
	Application Number	
Title of Invention	MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY	

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Prefix	Given Name	Middle Name	Family Name	Suffix
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Attorney Docket Number	TRAN-P602	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

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	Continuation of	11102127	2005-04-07

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TRAN-P602
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	Application Number	
	Filing Date	2008-05-15
	First Named Inventor	Guillermo J. Rozas
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	Attorney Docket Number	TRAN-P602

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6938130		2005-08-30	Jacobson et al.	
	2	6263407		2001-07-17	Arimilli et al.	
	3	6625694		2003-09-23	Masri et al.	
	4	5428761		1995-06-27	Herlihy et al.	
	5	5701432		1997-12-23	Wong et al.	
	6	6658536		2003-12-02	Arimilli et al.	
	7	5974438		1999-10-26	Neufeld	
	8	6006299		1999-12-21	Wang et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2008-05-15
	First Named Inventor	Guillermo J. Rozas
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TRAN-P602

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/William A. Zarbis/	Date (YYYY-MM-DD)	2008-05-15
Name/Print	William A. Zarbis	Registration Number	46120

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Application Number:	
Filing Date:	
Title of Invention:	MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Filer:	William A. Zarbis/Julie Giaramita
Attorney Docket Number:	TRAN-P602

Filed as Large Entity

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	5	50	250
Independent claims in excess of 3	1201	1	210	210
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1490**

Electronic Acknowledgement Receipt

EFS ID:	3307326
Application Number:	12121531
International Application Number:	
Confirmation Number:	7036
Title of Invention:	MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY
First Named Inventor/Applicant Name:	Guillermo J. Rozas
Customer Number:	45590
Filer:	William A. Zarbis/Julie Giaramita
Filer Authorized By:	William A. Zarbis
Attorney Docket Number:	TRAN-P602
Receipt Date:	15-MAY-2008
Filing Date:	
Time Stamp:	17:58:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Electronic Funds Transfer
Payment was successfully received in RAM	$1490
RAM confirmation Number	3373
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1	Oath or Declaration filed	TRAN-P602_DECL_5-15-08.pdf	60810 636d13ea35249305d3e04da15acfe0f1715a836c	no	2
Warnings:					
Information:					
2		TRAN-P602_AppFINAL_5-15-08.pdf	113955 8ca8f9dcc55314eb45c028dc566227158452312b	yes	30

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	20
	Claims	21	29
	Abstract	30	30

Warnings:					
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3	Drawings-only black and white line drawings	tran-p602_figsfinal_5-15-08.pdf	46126 181eb404df0ec6afb71633d65c364ec89fbd4892	no	5
Warnings:					
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4		TRAN-P602_Prelim_Amend_5-15-08.pdf	50579 ee71c1fa6dad7c18effff3e26ecb8bd827e28e27	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Claims	3	11
	Applicant Arguments/Remarks Made in an Amendment	12	12

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5		tran-p602_markedupspec_5-15-08.pdf	118187 f8ce9848b1c67ec1d8af70bdc68b8f6f26151cf9	yes	39

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	Document Description	**Start**	**End**
	Specification	1	21
	Claims	22	38
	Abstract	39	39

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6		TRAN-P602_cleanedversion spec_5-15-08.pdf	96643 0e3f9df8d33b1aa732210a4f3431c6506153db58	yes	30

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	21
	Claims	22	29
	Abstract	30	30

Warnings:					
Information:					
7	Application Data Sheet	TRAN-P602_AppDataSheet _5-15-08.pdf	1300689 b0b8d87b79e421ba939d8c35f015ed20723f07ff	no	4
Warnings:					
Information:					
8	Information Disclosure Statement (IDS) Filed	TRAN-P602_IDS_5-15-08.pdf	1313030 23c9224fe8c8ef3f464277766d65d59bd9a7fdb4	no	4
Warnings:					
Information:					
9	Fee Worksheet (PTO-06)	fee-info.pdf	8592 7eb8d7f9ff85b08a7b5c010c31f24c051c363b06	no	2
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Declaration

As below named inventor, I hereby declare that my residence post office address, and citizenship are as stated below my name. Further, I hereby declare that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

the specification of which:

__X__ is attached hereto, or
_____ was filed on _____ as application serial no. _____ : and
_____ was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; and

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Number	Country	Date Filed	Priority Claimed	
_____	_____	_____	_____ yes	_____ no
_____	_____	_____	_____ yes	_____ no

U.S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 and 119(e) of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Serial Number	Filing Date	Status (patented/pending/abandoned)
_____	_____	_____
_____	_____	_____

Power of Attorney

As a named inventor, I hereby appoint practitioners associated with this Customer Number:

45590

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: Guillermo J. Rozas

Inventor's Signature _____ Date April 6, 2005

Residence Los Gatos, CA Citizenship USA
(City State)

P.O. Address 104 Magneson Terrace, Los Gatos, CA 95032

MEMORY MANAGEMENT METHODS AND SYSTEMS THAT SUPPORT CACHE CONSISTENCY

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

Embodiments of the present invention relate to computer system memory, in particular the management of cache memory.

RELATED ART

With direct memory access (DMA), an input/output (I/O) system can issue read requests and writes directly to main memory without passing through the central processing unit (CPU). However, if the I/O system uses DMA to write to main memory, and changes data cached previously by the CPU, then the CPU will not receive the new data unless the CPU fetches the data from main memory. Also, for DMA reads, the CPU cache may contain more recent data than main memory, and so the I/O system will not receive the new data unless it reads the cache instead of main memory. Multiprocessor systems, particularly systems referred to as shared-memory simultaneous multiprocessor (SMP) architectures, have to deal with similar types of scenarios. The MESI (Modified, Exclusive, Shared, Invalid) protocol is a popular cache consistency (coherency) protocol that addresses these issues. A modification of the MESI protocol is the MOESI (Modified, Owned, Exclusive, Shared, Invalid) protocol. These protocols are known in the art.

Constraints are also applied to memory operations to prevent processors and DMA systems from reordering memory operations at will. If, for example, each processor could reorder memory operations for optimization, code sequences that work on a single processor would not work

on multiprocessor systems. One type of constraint can be referred to as sequential consistency. With sequential consistency, the legal orders of memory operations are those that are indistinguishable from strict interleaving of the operations from each thread of control. For example, for two threads, the operations of one thread can be interleaved with those of the other thread, but the order of operations within each thread is preserved.

There are different classes of high-level processor architectures with regard to operation reordering, optimization and speculation. One such class can be referred to as a lumped in-order architecture, and another such class as a lumped out-of-order architecture. With lumped in-order architectures, instructions are lumped into instruction groups that can be committed and rolled back atomically. Different instruction groups are committed sequentially and in order, but within an instruction group, arbitrary reordering and optimization can occur. Full speculation is possible within an instruction group, but speculation, reordering and optimization across instruction groups is limited. With lumped out-of-order architectures, instructions are lumped into instruction groups that can be committed and rolled back atomically. Different groups can execute out of order but are committed in order.

SUMMARY OF THE INVENTION

A method or system that can maintain sequential consistency for lumped (in-order or out-of-order) architectures would be advantageous. Prior attempts to achieve a sequentially consistent, lumped architecture are limited with respect to the number of memory operations that can be included in an instruction group. Specifically, such attempts are limited to a single memory operation per instruction group. Embodiments in accordance with the present invention overcome this disadvantage.

According to one embodiment of the present invention, a group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed (e.g., read, write, store, load, etc.). In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended. If an external agent (e.g., another processor or a DMA system) snoops the cache and the cache line (or any other cache line in the cache, for that matter) is indicated as having been accessed, then the instruction group is rolled back and reissued. If an external agent (e.g., another processor or a DMA system) snoops the cache and no cache line is indicated as having been accessed, then the snoop can be processed using a conventional cache coherency protocol (MESI, for example).

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the present invention and, together with the description, serve to explain the principles of the invention. The drawings referred to in this description should not be understood as being drawn to scale except if specifically noted.

Figure 1 is a block diagram of a portion of a computer system upon which embodiments of the present invention can be implemented.

Figure 2 is a block diagram of a cache and showing cache tags that are used according to one embodiment of the present invention.

Figure 3 is a flowchart of a method for managing memory in accordance with one embodiment of the present invention.

Figure 4 is a flowchart that continues from the flowchart of Figure 3.

Figure 5 is a flowchart of a method for replacing a cache line in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to the various embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, logic block, process, etc., is here, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system. It has proven convenient at times, principally for reasons of

common usage, to refer to these signals as bits, bytes, values, elements, symbols, characters, terms, numbers, or the like.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "executing," “changing,” “using,” “accessing,” “handling,” “rolling back,” “maintaining,” “eliminating,” “setting,” “clearing,” “incrementing,” “decrementing,” “associating,” “granting,” "determining" or the like, refer to the action and processes (e.g., flowcharts 30, 40 and 50 of Figures 3, 4 and 5, respectively) of a computer system or similar intelligent electronic computing device (generally, a controller), that manipulates and transforms data represented as physical (electronic) quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices.

Figure 1 is a block diagram of a portion of a computer system 5 upon which embodiments of the present invention can be implemented. Computer system 5 can include elements in addition to those illustrated in Figure 1. Generally speaking, embodiments in accordance with the present invention pertain to a computer system (or similar electronic device) that includes a processor, a main memory, a cache associated with the processor, and one or more external agents that can access the main memory and the processor’s cache.

In the example of Figure 1, computer system 5 includes a first processor 10, an optional second processor 11, and other optional processors 12 that are coupled to main memory 18 via bus 19. In the present embodiment, computer system 5 also includes a peripheral device 13 coupled to main memory 18 via bus 19. For ease of discussion, the processors 10, 11 and 12 and the peripheral device 13 may be collectively referred to herein as agents 10-13. Relative to processor 10, processors 11 and 12 and peripheral device 13 may be referred to as external agents; relative to processor 11, processors 10 and 12 and peripheral device 13 may be referred to as external agents; and so on.

In one embodiment, peripheral device 13 is capable of direct memory access (DMA). In general, DMA refers to a hardware circuit or software agent that can transfer data directly to or from main memory 18.

Associated with the processors 10-12 are first cache 14, optional second cache 15, and other optional caches 16, respectively. In one embodiment, each of the processors 10-12 has their own cache. The caches may be physically incorporated into the processors 10-12, or they may be physically external to the processors 10-12. In the present embodiment, each of the processors 10-12 can access each of the caches 14, 15 and 16 via bus 19.

In general, the agents 10-13 may each be executing a group of instructions according to a lumped in-order architecture or according to a lumped out-of-order architecture. The group of instructions can each include one or more memory operations (e.g., read, load, store, write, lock acquisition, etc.). The group of instructions can be demarcated by commit points (e.g., a

commit ending one group of instructions can mark the beginning of the next group of instructions, which in turn ends at another commit). An instruction group is handled atomically (e.g., it is treated as a unit). An instruction (or instructions) in the group of instructions being executed by one of the agents 10-13 may seek access to a cache associated with any of the other agents 10-13.

In one embodiment, computer system 5 implements a cache coherency protocol such as, but not limited to, MESI (Modified, Exclusive, Shared, Invalid). According to the MESI protocol, a cache line is identified as being in one of the modified, exclusive, shared or invalid states. In the modified state, the cache line includes more recent information than main memory 18 (only the information in the cache line is valid because main memory 18 is not up to date), and no other cache holds the information in the cache line. In the exclusive state, the information in the cache line is not in any other cache and the information in the cache line is unmodified, and accordingly main memory 18 is up to date. In the shared state, the information in the cache line may be in one or more other caches, and main memory 18 is up to date. In the invalid state, the cache line does not contain valid information. MESI is consistent with sequential consistency.

Figure 2 is a block diagram of cache 14 according to one embodiment of the present invention. Cache 14 includes a number of cache lines exemplified by cache lines 21 and 22.

In the embodiment of Figure 2, a cache line tag is associated with each of the cache lines in cache 14. In one such embodiment, each cache line tag includes a number of cache coherency protocol bits. For example, cache

coherency protocol bits 23 are associated with cache line 21, and cache coherency protocol bits 26 are associated with cache line 22. The cache coherency protocol bits 23 and 26 can be used to indicate the state of the cache lines 21 and 22, respectively, according to a cache coherency protocol such as the MESI protocol.

Furthermore, in the present embodiment, each cache line tag includes a number of additional bits referred to herein as observed bits for ease of discussion. For example, observed bits 24, 25, ..., N1 are associated with cache line 21, and observed bits 27, 28, ..., N2 are associated with cache line 22. The observed bits for cache 14 are associated with groups of instructions executed by the agent (e.g., processor 10) that is associated with cache 14. In one embodiment, each cache line tag is extended by one observed bit for each group of instructions that may be executed by processor 10 (Figure 1) at the same time. If, for example, processor 10 can execute five (5) instruction groups in parallel, then the cache line tags are each extended by 5 observed bits.

In the example of Figure 2, observed bits 24 and 27 (associated with cache line 21) are associated with instruction group A, and observed bits 25 and 28 (associated with cache line 22) are associated with instruction group B.

In one embodiment, an observed bit is set (e.g., set to a value of one) for a cache line in a cache if execution of an instruction in the group of instructions executed by the agent associated with that cache causes that cache line to be accessed (e.g., load, store, read, or write). For example, in one embodiment, observed bit 24 is set if an instruction in instruction group A,

when executed by processor 10, causes cache line 21 to be accessed, because cache line 21 is in cache 14 associated with processor 10 (Figure 1). In such an embodiment, observed bit 27 (also associated with instruction group A) is not set unless cache line 22 is also accessed because of instruction group A.

In general, with reference to Figures 1 and 2, a group of instructions executed by processor 10 may result in multiple cache lines in cache 14 being accessed. For each cache line in cache 14 accessed because of a group of instructions executed by processor 10, the observed bit corresponding to that group of instructions is set. However, an observed bit associated with a cache line in cache 14 is not set if an instruction executed on an external agent 11-13 causes access (e.g., a snoop or interrogation, or perhaps a read) to that cache line. For example, in one embodiment, an instruction executed by an agent other than processor 10 that causes cache line 21 to be accessed will not set an observed bit for cache line 21.

In one embodiment, when execution of a group of instructions is ended (e.g., the instruction group is committed, rolled back, or aborted), each observed bit set by that group of instructions is cleared (e.g., unset, or set to a value of zero). For example, if instruction group A is committed (or retired), rolled back or aborted, any of the observed bits 24 and 27 that are set are cleared. From another perspective, the observed bits associated with instruction group A, if set, remain set until the execution of instruction group A is ended.

To summarize, in one embodiment, when an agent (e.g., processor 10) begins to execute a group of instructions, it allocates an observed bit for that

group of instructions to each cache line in the cache associated with the agent (e.g., cache 14 associated with processor 10). If a cache line (e.g., cache line 21) has been accessed because of an instruction in an instruction group (e.g., instruction group A) being executed by processor 10, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 24) is set. If another cache line (e.g., cache line 22) has also been accessed because of an instruction in instruction group A, then the observed bit for that cache line and corresponding to instruction group A (e.g., observed bit 27) is set. When execution of an instruction group is ended, the observed bits associated with that instruction group are cleared, and thus the observed bits are available for subsequent instruction groups executed by the agent. For example, if instruction group A is committed, rolled back or aborted, then observed bits 24 and 27 are cleared.

In one embodiment, the observed bits are used in the following manner. Continuing with reference to Figures 1 and 2, if an external agent (e.g., another processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that causes access to (or a request for access to) cache line 21, for example, and any of the observed bits 24, 25, ..., N1 have been set, then the instruction groups associated with the observed bits that are set are forced to roll back and then reissue. Also, any of the observed bits 24, 25, ..., N1 associated with cache line 21 that have been set are cleared. For example, if observed bits 24 and 25 have been set, then instruction group A (which corresponds to observed bit 24) and instruction group B (which corresponds to observed bit 25) are rolled back, and observed bits 24 and 25 are cleared. The rollback also clears the observed bits associated with other cache lines in cache 14 if those observed bits correspond to the groups of instructions that are rolled back. For example, if the instruction groups A and

B are rolled back as mentioned above, then observed bits 27 and 28 are also cleared if those observed bits are set. The cache state transition occurs at this point, before the instruction groups A and B are reissued and are able to again cause cache line 21 (and perhaps cache line 22) to be accessed.

In general, if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, and an observed bit associated with that cache line has been set, then all the observed bits that have been set for that cache line are cleared, all the instruction groups corresponding to the observed bits that are cleared are rolled back, and the observed bits associated with the instruction groups that are rolled back are also cleared for other cache lines in cache 14.

In one embodiment, the rollbacks just described occur only if an external agent 11-13 accesses, or requests access to, a cache line in cache 14, an observed bit associated with that cache line has been set, and the cache line is not in the shared state. Again consider an example in which an external agent (e.g., another processor 11 or 12 or a DMA agent such as peripheral device 13) executes an instruction that seeks access to cache line 21. In one embodiment, in addition to checking the observed bits 24, 25, ..., N1 associated with cache line 21, the cache coherency protocol bits 23 are also checked to determine the state (e.g., the MESI state) of cache line 21. In a MESI embodiment, for example, if cache line 21 is in the shared state, and if the access from the external agent is for sharing (e.g., it is not exclusive), then access to cache line 21 can be granted without rolling back the instruction groups associated with the observed bits 24, 25, ..., N1 that are set.

In one embodiment, observed bits that are set are not forgotten (e.g., cleared) except in the case of a rollback, commit or abort. In such an embodiment, a cache line that has at least one of its observed bits set is not replaceable, although the cache line and its set observed bit(s) can be moved to another location. This can lead to a situation in which a cache line is needed, but no cache lines are available (that is, all cache lines have at least one of their respective bits set, so none of the cache lines can be replaced or moved). In one embodiment, if such a situation arises, the group of instructions that needs the cache line, as well as following instruction groups, is rolled back and then reissued.

To prevent instruction groups from being repeatedly rolled back, in one embodiment, the number of times each instruction group is rolled back is counted and compared to a threshold. In such an embodiment, if the number of times an instruction group is rolled back exceeds the threshold, then the instruction group is rolled back for the last time. If it fails to execute to completion in the next attempt, the instruction group is reformed into a new instruction group that is reduced in size (e.g., one or more instructions is removed from the instruction group), and the counter for the new instruction group is set to zero. In the limiting case, the instruction group is eventually reduced to a single instruction that will be able to complete execution.

Figures 3 and 4 are flowcharts 30 and 40 of a method for managing memory in accordance with one embodiment of the present invention (the flowchart of Figure 4 is a continuation of the flowchart of Figure 3). Although specific steps are disclosed in flowcharts 30 and 40, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowcharts

30 and 40. It is appreciated that the steps in flowcharts 30 and 40 may be performed in an order different than presented, and that not all of the steps in flowcharts 30 and 40 may be performed. Some or all of the processes and steps of flowcharts 30 and 40 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory 18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 31 of Figure 3, a first group of instructions (e.g., instruction group A) is executed (e.g., by processor 10 of Figure 1). In one embodiment, the first group of instructions includes multiple memory operations (e.g., reads, writes, loads, stores, lock acquisition, etc.). At least one of the instructions in the first group of instructions, when executed, causes a cache line (e.g., cache line 21 of Figure 2) in a cache associated with processor 10 (e.g., cache 14) to be accessed (e.g., read, written, etc.).

In step 32 of Figure 3, and continuing with reference to Figure 2, that instruction is executed, causing cache line 21 to be accessed.

In step 33 of Figure 3, with reference also to Figure 2, an indicator associated with the first group of instructions is changed, in order to indicate that cache line 21 has been accessed because of the first group of instructions. In one embodiment, the indicator is also associated with cache line 21. In one embodiment, a bit (e.g., observed bit 24) associated with cache line 21 and the first group of instructions is set. In one embodiment, cache line 21 is indicated as having been accessed (that is, for example, the observed bit remains set) until execution of the first group of instructions is ended (e.g., because of a roll back, commit or abort).

In step 34 of Figure 3, with reference also to Figure 1, a second group of instructions is executed by an agent external to processor 10 (e.g., processor 11 or 12 or a DMA agent such as peripheral device 13). At least one of the instructions in the second group of instructions, when executed, causes (or will cause) the cache line of interest (e.g., cache line 21 of Figure 2) to be accessed.

In step 35 of Figure 3, access to the cache line of interest (e.g., cache line 21 of Figure 2) is sought because of the second group of instructions. As will be seen, the first group of instructions is then handled depending on whether or not cache line 21 has been accessed because of the first group of instructions and is identified as having been accessed (e.g., by an observed bit). That is, it is possible that cache line 21 is accessed because of the second group of instructions before it is accessed because of the first group of instructions.

In step 41 of Figure 4, with reference also to Figure 2, a determination is made with regard to whether or not the cache line of interest (e.g., cache line 21) has been accessed because of the first group of instructions. In one embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 43, and otherwise flowchart 44 proceeds to step 44. In another embodiment, if the observed bit (e.g., observed bit 24) associated with cache line 21 and the first instruction group is set, then flowchart 40 proceeds to step 42.

In step 42 of Figure 4, and with reference to Figure 2, a determination is made with regard to whether or not cache line 21 is in the shared state

(e.g., according to the MESI protocol). If cache line 21 is in the shared state, then flowchart 40 proceeds to step 44, and otherwise flowchart 40 proceeds to step 43.

In step 43 of Figure 4, with reference also to Figure 2, the first group of instructions is atomically rolled back, and the observed bits 24, 25, ..., N1 associated with cache line 21 are cleared. Other observed bits, associated with other cache lines in cache 14 and corresponding to the first group of instructions, are also cleared if they are set. For example, if observed bit 27 (which also corresponds to the first group of instructions) is set, then it is also cleared by the rollback of the first group of instructions. Also, other groups of instructions associated with any of the observed bits of cache 14 that are cleared are also rolled back. For example, if observed bit 25 is set, then it is cleared and the instruction group associated with observed bit 25 (e.g., instruction group B) is rolled back, which in turn results in observed bit 28 (which also corresponds to instruction group B) of cache line 22 being cleared.

In step 44 of Figure 4, access to cache line 21 (Figure 2) is granted.

In step 45 of Figure 4, in one embodiment, the number of times that the first group of instructions has been rolled back is counted. If the number of times the first group of instructions has been rolled back exceeds a threshold, then one or more instructions are eliminated from the first instruction group. Specifically, in one embodiment, the first group of instructions is reissued, and if the next execution attempt results in another rollback, then the first instruction group is reduced by one or more instructions.

Figure 5 is a flowchart 50 of a method for replacing a cache line in accordance with one embodiment of the present invention. Although specific steps are disclosed in flowchart 50, such steps are exemplary. That is, embodiments of the present invention are well-suited to performing various other steps or variations of the steps recited in flowchart 50. It is appreciated that the steps in flowchart 50 may be performed in an order different than presented, and that not all of the steps in flowchart 50 may be performed. Some or all of the processes and steps of flowchart 50 can be realized, in one embodiment, as a series of instructions that reside in hardware or software (e.g., in main memory 18 of Figure 1) and are executed by one or more of the agents 10-13 in a computer system 5 (Figure 1).

In step 51 of Figure 5, a number of instruction groups are executed in parallel using processor 10 (Figure 1), for example.

In step 52 of Figure 5, with reference also to Figures 1 and 2, each cache line in the cache associated with processor 10 (e.g., cache 14) that is accessed because of the groups of instructions being executed in step 51 is indicated as being accessed. For example, as previously described herein, an observed bit can be set for each cache line accessed because of the groups of instructions of step 51.

In step 53 of Figure 5, one of the instructions in one of the instruction groups attempts to replace a cache line.

In step 54, in one embodiment, if all of the cache lines in the cache of interest (e.g., cache 14) are indicated as having been accessed (e.g., at least one observed bit is set for each of the cache lines in cache 14, then the

instruction group that has the instruction that attempted the cache line replacement (the instruction group of step 53) is rolled back.

In summary, methods and systems that can maintain sequential consistency for lumped (in-order or out-of-order) architectures are described. Significantly, embodiments in accordance with the present invention permit sequentially consistent, lumped architectures in which multiple memory operations can be included in instruction groups.

Embodiments in accordance with the present invention can incorporate variations to the features described above. For systems with large speculation ability (e.g., potentially 20 or more active instruction groups), the cost (e.g., the storage cost) of the associated number of observed bits can be reduced in various ways. For example, a protocol can be established in which any external snoop causes all active instruction groups to roll back and reissue after the cache line state transition. In effect, such a protocol acts as if there is a single observed bit that is always set, except during the period of inactivity after rollback, and so no additional storage is needed for the observed bit. Alternatively, instead of an observed bit per cache line per instruction group, there can be an observed bit per instruction group.

Furthermore, new hardware structures can be added to track which cache lines have been accessed, without the storage of data. These hardware structures can be direct-mapped, set-associative, or fully-associative and of varying capacity.

Also, instead of having an observed bit per cache line per instruction group, a smaller memory structure (e.g., another cache, or a memory

structure within main memory) that covers the whole cache address space and that has an observed bit per entry and per instruction group can be used. Each entry covers some portion of the cache address space, in such a way that every cache line address maps uniquely to an entry, but an entry maps to many cache lines. For example, some subset of the address bits of a cache line can be used to identify an entry. The subset of the address bits are the address summary. When accessing a cache line, the entry corresponding to the address summary for the cache line is used to set the observed bits. Similarly, on a snoop request, the address is "summarized," and the entry corresponding to the summary is examined for the presence of observed bits. The observed bits are cleared when an instruction group is committed, rolled back, or aborted. To illustrate, consider a cache complex where each cache holds 32 bytes, so that, for example, the bottom five bits (bits 4-0) of an address indicate bytes within the same cache line. Furthermore, consider a 32-entry observed bit structure, where bits 9-5 of the cache line address are used to select an entry, and this entry holds the observed bits. Then, any two addresses that have the same bits 9-5 will use the same entry in the summary structure; that is, they collide. This can mean that when a snoop comes, an instruction group that did not really conflict may be rolled back, because there is a conflict/collision in the summary structure even though there would not have been a conflict/collision in the cache. Thus, there is a tradeoff between the size of the summary structure and the overhead incurred by the "spurious" rollbacks due to collisions.

Embodiments in accordance with the present invention are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not

be construed as limited by such embodiments, but rather construed according to the below claims.

CLAIMS

What is claimed is:

1. A method of managing memory in a computer system, said method comprising:

executing a first group of instructions, wherein said first group of instructions comprises multiple memory operations and a first instruction that when executed causes a cache line of a cache memory to be read; and

in response to said first instruction causing said cache line to be read, changing an indicator associated with said first group of instructions to indicate that said cache line has been read, wherein said cache line is so indicated as having been read until execution of said first group of instructions is ended.

2. The method of Claim 1 further comprising:

executing a second group of instructions, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed, and wherein said first group of instructions is associated with a thread executing on a first processor and said second group of instructions is associated with a thread executing on an agent external to said first processor;

in response to said second instruction seeking access to said cache line, using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group of instructions according to said result.

3. The method of Claim 2 wherein said handling comprises rolling back said first group of instructions before granting said access provided said

indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.

4. The method of Claim 3 wherein said handling further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.

5. The method of Claim 3 further comprising maintaining a count of how many times said first group of instructions has been rolled back.

6. The method of Claim 5 further comprising eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.

7. The method of Claim 2 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).

8. The method of Claim 2 wherein said indicator comprises one bit per instruction group for each group of instructions being executed at a same time by said first processor.

9. The method of Claim 2 wherein said indicator comprises one bit per cache line per instruction group for each group of instructions being executed at a same time by said first processor.

10. The method of Claim 1 further comprising:

setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and

clearing said bit when said execution of said first group of instructions is ended.

11. The method of Claim 1 further comprising:

executing a plurality of groups of instructions in parallel;

changing an indicator associated with each cache line in said cache that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

12. A computer system comprising:

a first processor;

a cache memory used by said first processor; and

a memory unit coupled to said first processor, said memory unit containing instructions that when executed implement a memory management method, said method comprising:

executing a first group of instructions using said first processor, wherein said first group of instructions includes multiple memory operations and a first instruction that when executed causes a cache line of said cache memory to be read; and

in response to said first instruction causing said cache line to be read, changing an indicator associated with said first group of instructions to indicate that said cache line has been read, wherein said cache line is so indicated as having been read until execution of said first group of instructions is ended.

13. The computer system of Claim 12 wherein said method further comprises:

executing a second group of instructions using an agent coupled to said cache memory, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed, and wherein said agent is external to said first processor;

in response to said second instruction seeking access to said cache line, using a value of said indicator to determine whether said cache line has been read and generating a result thereof; and

handling said first group of instructions according to said result.

14. The computer system of Claim 13 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).

15. The computer system of Claim 13 wherein said method further comprises rolling back said first group of instructions before granting said access provided said indicator indicates said cache line has been read by said

first instruction, and otherwise granting said access without rolling back said first group of instructions.

16. The computer system of Claim 15 wherein said method further comprises:

determining a state of said cache line, wherein said state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

rolling back said first group of instructions and then granting said access provided said cache line is in other than said shared state and said indicator indicates said cache line has been read by said first instruction, and otherwise granting said access without rolling back said first group of instructions.

17. The computer system of Claim 15 wherein said method further comprises maintaining a count of how many times said first group of instructions is rolled back.

18. The computer system of Claim 17 wherein said method further comprises eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.

19. The computer system of Claim 17 wherein said indicator comprises one bit per instruction group for each group of instructions being executed at a same time by said first processor.

20. The computer system of Claim 17 wherein said indicator comprises one bit per cache line per instruction group for each group of instructions being executed at a same time by said first processor.

21. The computer system of Claim 12 wherein said method further comprises:

setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and

clearing said bit when said execution of said first group of instructions is ended.

22. The computer system of Claim 12 wherein said method further comprises:

executing a plurality of groups of instructions in parallel on said first processor;

changing an indicator associated with each cache line in said cache memory that has been accessed because of an instruction in any of said plurality of groups of instructions; and

provided all cache lines in said cache memory are indicated as having been accessed, rolling back a group of instructions that includes an instruction that when executed attempts to replace information in a cache line of said cache memory, and otherwise continuing said executing of said plurality of groups of instructions.

23. A method of managing shared memory in a computer system, said method comprising:

executing a first group of instructions;

associating a first state with a cache line, wherein said first state is specified according to a cache coherency protocol comprising at least a modified state, a shared state and an invalid state; and

associating a second state with said cache line during said executing, wherein said second state indicates that said cache line has been accessed because of a first instruction of said first group of instructions and wherein said second state is cleared when execution of said first group of instructions is ended.

24. The method of Claim 23 wherein said first group of instructions includes multiple memory operations.

25. The method of Claim 23 further comprising:

executing a second group of instructions, wherein said second group of instructions includes a second instruction that when executed causes said cache line to be accessed and wherein said first group of instructions is associated with a thread executing on a first processor and wherein said second group of instructions is associated with a thread executing on an agent external to said first processor;

in response to said second instruction seeking access to said cache line, using said second state to indicate said cache line has been accessed because of said first instruction; and

rolling back said first group of instructions before granting said access.

26. The method of Claim 25 wherein said rolling back is only performed provided said cache line is in other than said shared state.

27. The method of Claim 25 further comprising maintaining a count of how many times said first group of instructions is rolled back.

28. The method of Claim 27 further comprising eliminating one or more instructions from said first group of instructions if said count exceeds a threshold.

29. The method of Claim 25 wherein said agent is a second processor or an input/output agent capable of direct memory access (DMA).

30. The method of Claim 23 wherein said second state is indicated by:

setting a bit associated with said cache line in response to said first instruction causing said cache line to be read; and

clearing said bit when said execution of said first group of instructions is ended.

31. A computer system comprising:

a processor;

a cache memory coupled to said processor and having a plurality of cache lines; and

a memory unit coupled to said processor, wherein said memory unit has a plurality of entries and an indicator bit per entry, wherein said indicator bit is set to indicate that a cache line of said cache memory has been accessed because of an instruction of a group of instructions and wherein said indicator bit is cleared when execution of said group of instructions is ended, and wherein each of said entries covers the address space of said

cache memory such that a cache line maps uniquely to an entry but an entry maps to multiple cache lines.

32. The computer system of Claim 31 wherein a subset of address bits of said cache line is used to identify said entry, wherein in response to said cache line being accessed, an indicator bit of said entry corresponding to said subset of address bits is set.

MEMORY MANAGEMENT METHODS AND SYSTEMS
THAT SUPPORT CACHE CONSISTENCY

ABSTRACT

Methods and systems for maintaining cache consistency are described. A group of instructions is executed. The group of instructions can include multiple memory operations, and also includes an instruction that when executed causes a cache line to be accessed. In response to execution of that instruction, an indicator associated with the group of instructions is updated to indicate that the cache line has been accessed. The cache line is indicated as having been accessed until execution of the group of instructions is ended.

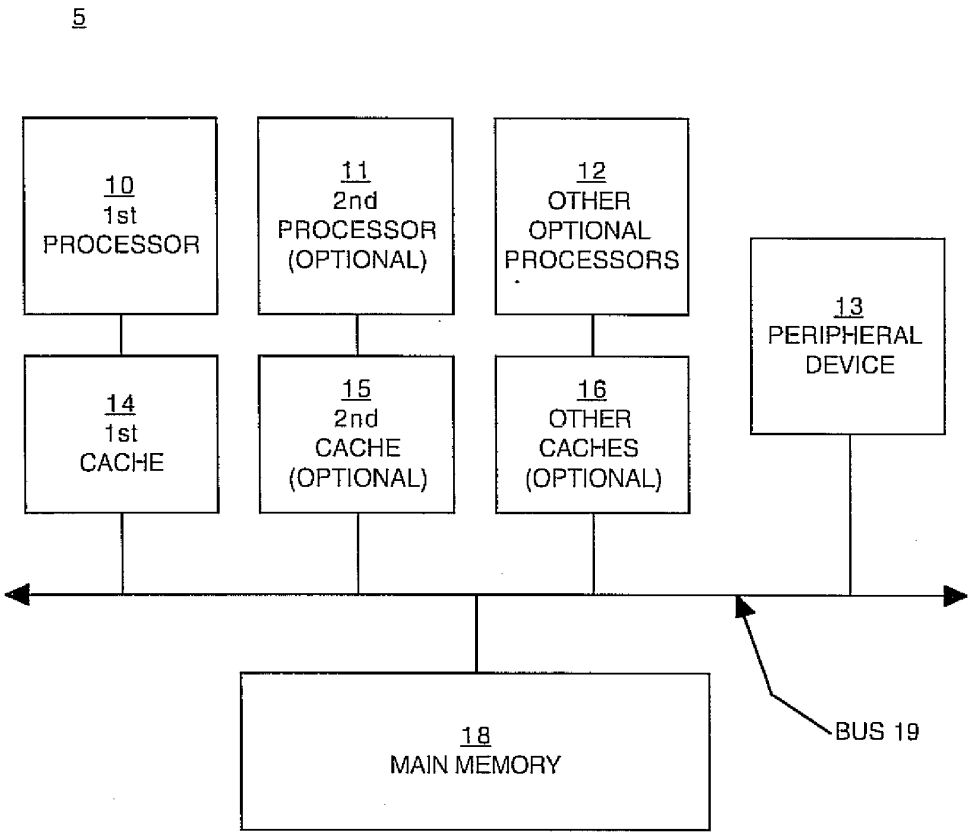

5
10
1st
PROCESSOR
11
2nd
PROCESSOR
(OPTIONAL)
12
OTHER
OPTIONAL
PROCESSORS
13
PERIPHERAL
DEVICE
14
1st
CACHE
15
2nd
CACHE
(OPTIONAL)
16
OTHER
CACHES
(OPTIONAL)
18
MAIN MEMORY
BUS 19

Figure 1

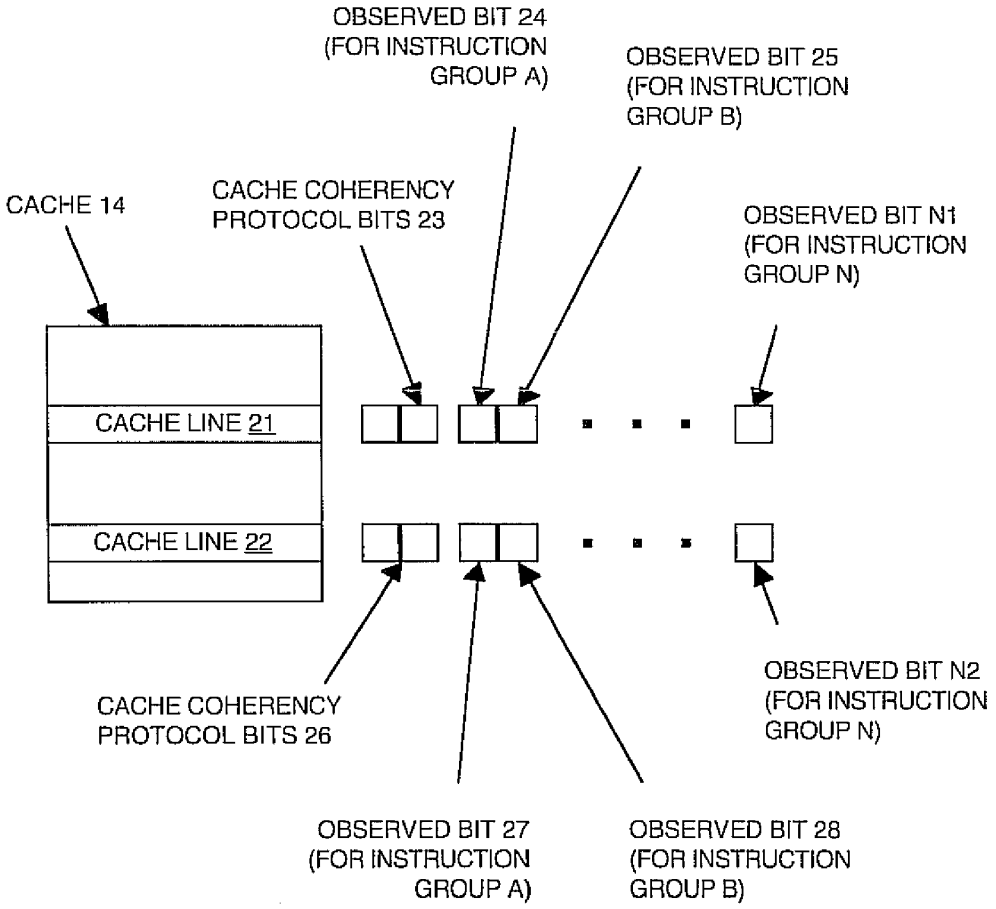

OBSERVED BIT 24
(FOR INSTRUCTION
GROUP A)
OBSERVED BIT 25
(FOR INSTRUCTION
GROUP B)
CACHE 14
CACHE COHERENCY
PROTOCOL BITS 23
OBSERVED BIT N1
(FOR INSTRUCTION
GROUP N)
CACHE LINE 21
CACHE LINE 22
CACHE COHERENCY
PROTOCOL BITS 26
OBSERVED BIT N2
(FOR INSTRUCTION
GROUP N)
OBSERVED BIT 27
(FOR INSTRUCTION
GROUP A)
OBSERVED BIT 28
(FOR INSTRUCTION
GROUP B)

Figure 2

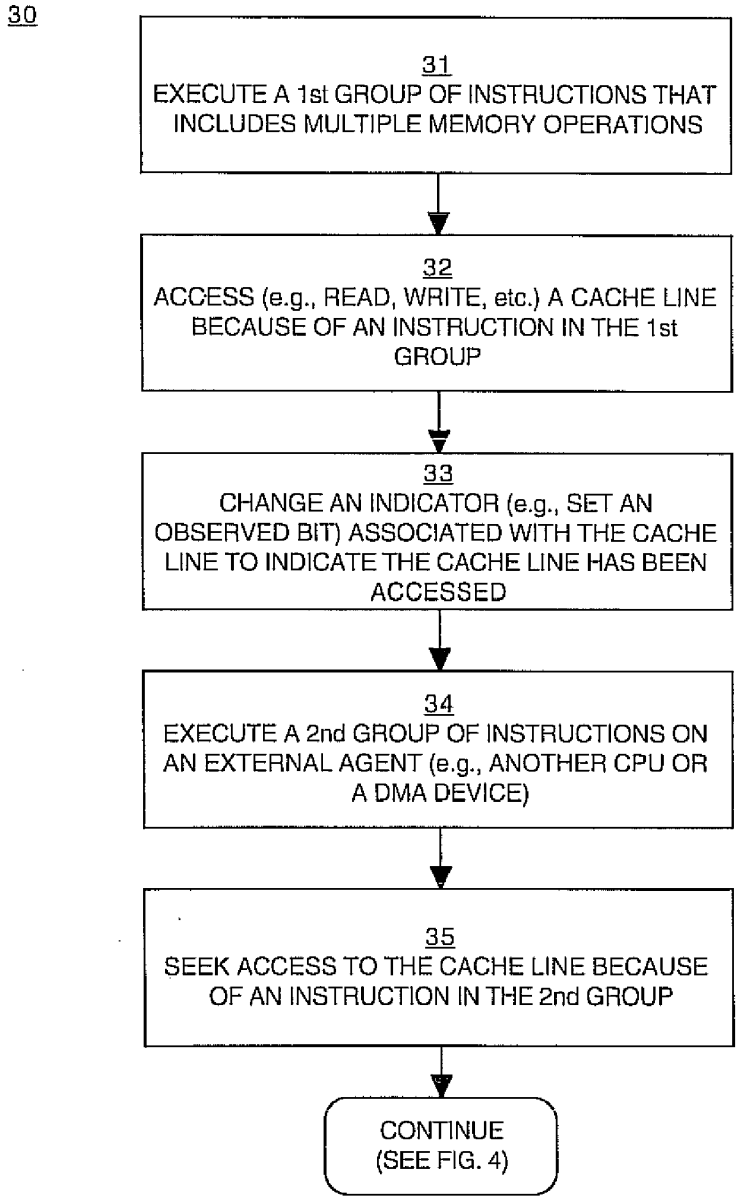

30
31
EXECUTE A 1st GROUP OF INSTRUCTIONS THAT INCLUDES MULTIPLE MEMORY OPERATIONS
32
ACCESS (e.g., READ, WRITE, etc.) A CACHE LINE BECAUSE OF AN INSTRUCTION IN THE 1st GROUP
33
CHANGE AN INDICATOR (e.g., SET AN OBSERVED BIT) ASSOCIATED WITH THE CACHE LINE TO INDICATE THE CACHE LINE HAS BEEN ACCESSED
34
EXECUTE A 2nd GROUP OF INSTRUCTIONS ON AN EXTERNAL AGENT (e.g., ANOTHER CPU OR A DMA DEVICE)
35
SEEK ACCESS TO THE CACHE LINE BECAUSE OF AN INSTRUCTION IN THE 2nd GROUP
CONTINUE
(SEE FIG. 4)

Figure 3

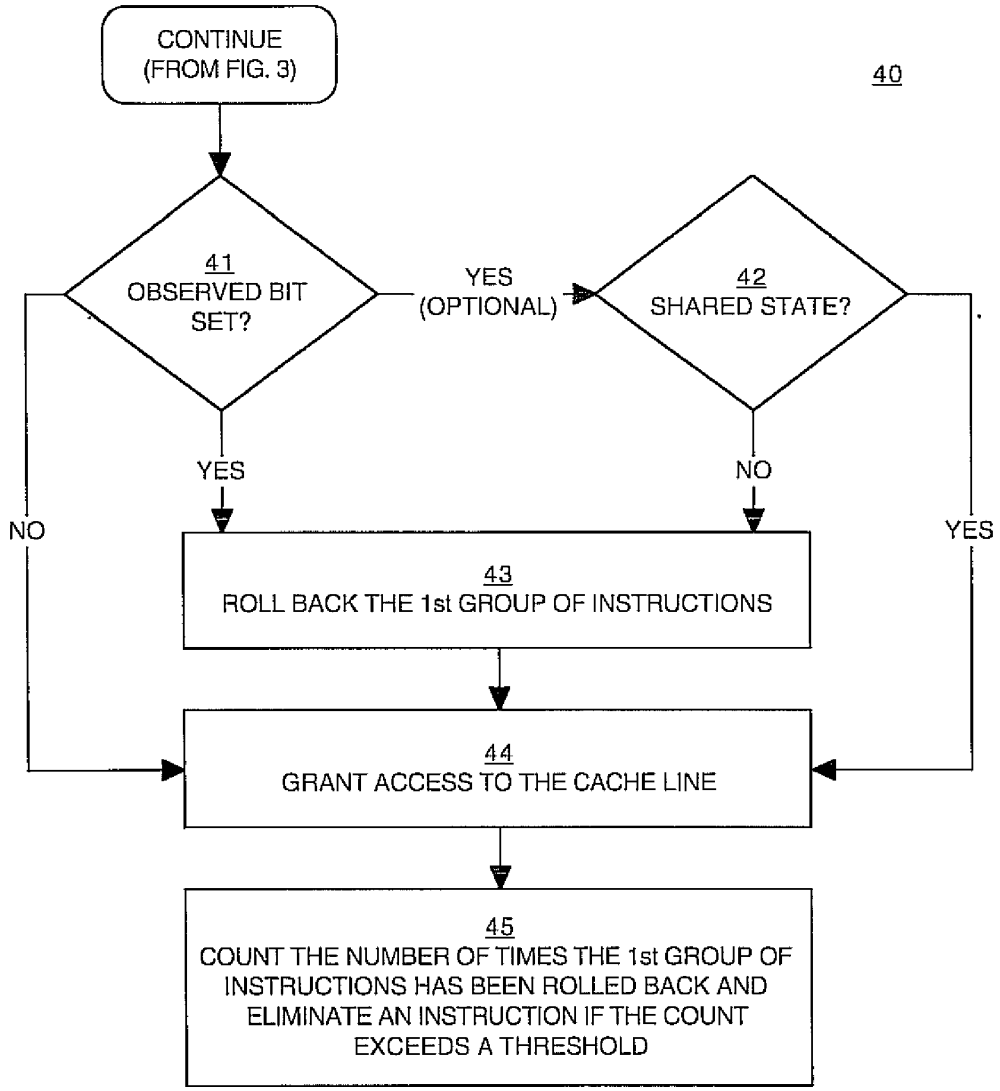

CONTINUE
(FROM FIG. 3)
40
41
OBSERVED BIT
SET?
YES
(OPTIONAL)
42
SHARED STATE?
YES
NO
NO
YES
43
ROLL BACK THE 1st GROUP OF INSTRUCTIONS
44
GRANT ACCESS TO THE CACHE LINE
45
COUNT THE NUMBER OF TIMES THE 1st GROUP OF
INSTRUCTIONS HAS BEEN ROLLED BACK AND
ELIMINATE AN INSTRUCTION IF THE COUNT
EXCEEDS A THRESHOLD

Figure 4

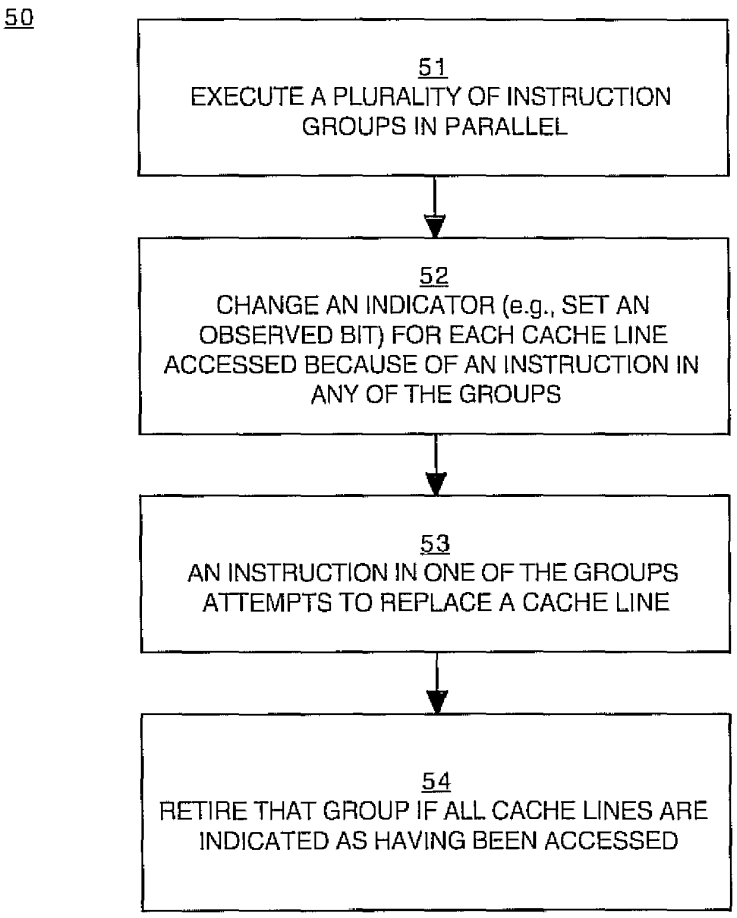

50
51
EXECUTE A PLURALITY OF INSTRUCTION GROUPS IN PARALLEL
52
CHANGE AN INDICATOR (e.g., SET AN OBSERVED BIT) FOR EACH CACHE LINE ACCESSED BECAUSE OF AN INSTRUCTION IN ANY OF THE GROUPS
53
AN INSTRUCTION IN ONE OF THE GROUPS ATTEMPTS TO REPLACE A CACHE LINE
54
RETIRE THAT GROUP IF ALL CACHE LINES ARE INDICATED AS HAVING BEEN ACCESSED

Figure 5

PTO/SB/06 (12-04)

Filing Date: 05/15/08

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/121,531

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	510
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	210
TOTAL CLAIMS (37 CFR 1.16(i))	25	5	X$ 25		OR	X$50	250
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1	X$105			X$210	210
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			185			370	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	0		TOTAL	1490

APPLICATION AS AMENDED – PART II

AMENDMENT A		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.