

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioners,

v.

ICASHE, INC.,
Patent Owner.

Case IPR2025-00642

Patent No. 8,403,219

DECLARATION OF MARC E. LEVITT

I, Marc E. Levitt, Ph.D., of San Jose, California, declare that:

I. ASSIGNMENT

1. I have been retained by Robins Kaplan LLP on behalf of Patent Owner iCashe, Inc. (“iCashe”) as an expert with regard to this matter. I understand that Petitioners are requesting that the Patent Trial and Appeal Board (“Board”) institute inter partes review (IPR) of U.S. Pat. No. 8,403,219 (“’219 patent”) (Ex. 1001).

2. In my capacity as an expert, I have been asked to provide my independent analysis and opinions regarding the ’219 patent, the prosecution history of the ’219 patent and related applications as applicable, the alleged prior art relied upon by Petitioner, the meaning of various claim terms from the ’219 patent from the perspective of a person of ordinary skill in the art (“POSITA”), and the opinions offered by Petitioners’ expert, Mr. Henry N. Dreifus, in his declaration (“Dreifus Declaration”) (Ex. 1003). My opinions and conclusions are fully discussed in later sections of this declaration.

3. I am an independent consultant, and I am not, and have never been, an employee of iCashe or Samsung. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent analyzing the ’219 patent, the prosecution history of the ’219 patent and related applications, the prior art publications relied upon by Petitioners, the Declaration of Henry N.

Dreifus, and other related materials. I will not receive any added compensation based on the outcome of any IPR or other proceedings involving the '219 patent.

II. BACKGROUND AND QUALIFICATIONS

4. I am an independent high technology consultant with over 30 years of experience in the areas of executive leadership, business development, technology, technology development, and intellectual property. I have extensive technical and business experience in computer architecture, networking, mobile, semiconductor design, semiconductor manufacturing, systems-on-a-chip, systems architecture, technical software, embedded software, enterprise software, algorithms, and computational finance.

5. I graduated from Lehigh University in 1986 with a Bachelor of Science degree with High Honors in Computer Engineering, and later obtained my Master's degree and PhD in Electrical Engineering from the University of Illinois in Urbana-Champaign, Illinois. I completed my studies in 1990, and wrote my doctoral thesis on time-based strategies for semiconductor manufacturing and test under the supervision of Dr. Jacob A. Abraham. During my education, I conducted VLSI testing research at Hewlett-Packard and EDA software development at Digital Equipment Corporation.

6. After receiving my PhD, I worked at Sun Microsystems (Sun) rising to the dual position of Senior Hardware Manager and Senior Staff Engineer. While at

Sun I worked on multiprocessor server systems, high performance workstation systems, microprocessors and related chipsets/ASICs. At Sun I was responsible for, among other things, the test and design-for-test strategy for all SPARC microprocessors and related ASICs, JAVA processors, processor modules, and SPARC reference platform designs. I also worked with issues related to power management, clocking, reset, test, design-for-test, and debug issues throughout numerous departments at Sun Microsystems. I was a key member of the VLSI Design Review team, and reviewed and signed off on every circuit design used inside Sun's custom chips. Additionally, I developed or architected CAD tools to aid in the design, test, manufacture, and debug of integrated circuits and computer systems within Sun.

7. I later brought my extensive architecture expertise and expertise in circuit design, development, and manufacturing to positions I held at Sonics Inc. and Transmeta Corp. At Sonics Inc. I was the Director of Silicon Development, in which capacity I was in charge of in-house deep sub-micron design projects in 0.18um CMOS, and was also responsible for developing, planning and executing product ideas, system-on-chip platforms, and OEM silicon based on the Sonics Integration Architecture. At Sonics Inc. I also designed the OC-12 network processor (MIPS based) and assisted in the design and development of two VoIP chipsets.

8. At Transmeta Corp., I was the Director of VLSI. In this position I managed and architected the Northbridge and Southbridge for the Efficeon TM8xxx and the TM6000 1GHz x86 Low Power System on a Chip project, for which I was responsible for the logic, verification, and circuit design teams on this unique project that integrated a 1GHz x86 processor, north bridge, south bridge, video processing, and graphics engine in 130nm/90nm technology. My responsibilities included all hardware product management, scheduling, resource planning, and lab prototype work, including managing interactions with software engineering (CMS, BIOS, and drivers), systems engineering, packaging, foundry, and operations requirements for the project. Additionally, I was a key interface with consumer electronics companies in developing solutions for set-top-boxes for smart video delivery and processing.

9. I later became a Vice President and General Manager at Cadence Design Systems, where I ran Cadence's Design for Manufacturing (DFM) Business Unit, which is responsible for enterprise class technical software used in semiconductor design, analysis, and manufacturing including mixed signal and RF circuit design and analysis. I oversaw a \$130+ million per year business and approximately 240 worldwide employees in R&D, operations, marketing, sales, and application engineering with teams in Japan, Taiwan, Russia, India and the United States.

10. Since my work at Cadence Design Systems, I have principally acted as a professional consultant in the areas of technology development, intellectual property, and business development in the areas of software, networking hardware, and semiconductors. My consulting clients included CNEX LABS where I helped develop the clocking, power management, and PCIe capabilities of their NVMe PCIe SSD controller ASIC.

11. As a result of my extensive industry experience, I have expertise in, among other things, computer architecture, VLSI design, VLSI manufacturing, software, and systems. This expertise and background extends to at least the following areas:

- Computer Architecture: RISC, CISC, DSP, memory hierarchies, memory systems, pipelining, clock design, power management, low power design, microcode, microarchitecture, multicore, 2d & 3d graphics, SPARC, x86, MIPS, ARM, USB, GPU, VGA, LPC, PCI, PCI-X, Hypertransport, PCIe, NVMe, SoCs, AGP, Ethernet, cache, FPU, TLB, DDR, DRAM, and SRAM;
- VLSI Design: All aspects of front to back design process and methodologies for digital, analog, and mixed signal designs, including RTL (Verilog & VHDL), logic, circuit, physical design, layout, verification, PLL, RAM, TLB/CAM, IO, PHY, scan, DFT, BIST, LCDs;

- VLSI Manufacturing: CMOS, mask making, OPC, testing, packaging, yield enhancement, debug, failure analysis, and production ramp;
- Software: Computer aided design (CAD), drivers, BIOS, operating systems (Windows, Linux, Unix, Android, etc.), mobile software, embedded software, JSRs, client-server software, enterprise software, applications, large web based systems (Google, Facebook, AWS etc.), algorithms, and computational finance. I have expertise in the following exemplary languages: Fortran, C, C++, Perl, Python, Pascal, Java, and ASM; and
- Systems: Systems-on-a-Chip, VoIP, networking, multiprocessors, servers, PCs, parallel processing, distributed computing, mobile phone, tablets, settop-boxes, TV, digital camera/camcorders, encryption/security, power management, ACPI, LCD, OLED, GSM, EDGE, WCDMA, 3GPP, CDMA, IEEE 802.x/Ethernet, switching, routing, RFID, Bluetooth.

12. I am also a named inventor on at least 15 issued U.S. patents relating to, among other things, circuit design, logic design, memory design, hardware testing, software, diagnosis, and formal verification. I have published as author or co-author over 30 journal articles, conference publications, and book chapters.

13. I was also the recipient of the Sun Microelectronics Engineering Excellence Award in 1996. I am a member of Tau Beta Pi and Eta Kappa Nu

Engineering Honor Societies and, from January to March of 1997, I was the guest editor of IEEE Design & Test of Computers magazine for a special issue on microprocessors.

14. My curriculum vitae, which is attached to this declaration as Appendix A, sets forth the details of my background and experience in the relevant field.

III. BASIS FOR OPINIONS

15. I believe that I am qualified to render opinions regarding the technology described and claimed in the '219 patent, based on my experience and education. Based on my expertise and qualifications, I believe that I am qualified to provide opinions as to the state of the art and what a POSITA would have understood, known, or concluded as of the conception of the inventions of the '219 patent. I was working in the integrated circuit and system design field in the 2005 timeframe, worked closely with many others in the field, companies designing RF circuits, and participated in various industry organizations.

16. In reaching my opinions and conclusions, I have relied upon my education, my work experience in the relevant field, and my training, and considered and relied upon my review and analysis of the following materials:

- The Petition;
- Ex. 1001, the '219 patent;
- Ex. 1002, the prosecution history of the '219 patent;

- Ex. 1003, Dreifus Declaration;
- Ex. 1009, U.S. Patent No. 5,943,624 (“Fox”);
- Ex. 1014, Plaintiff iCashe’s Infringement Contentions, Including Exhibit E;
- Ex. 1015, Uwe Hansmann et al., Smart Card Application Development Using Java (July 2002);
- Ex. 1016, Software, Microsoft Press Computer Dictionary (2nd ed., 1993);
- Ex. 1019, Katherine M. Shelfer and J. Drew Procaccino, Smart Card Evolution (July 2002);
- Ex. 1020, U.S. Patent App. Pub. No. 2005/0015275 (“Takekawa”);
- Ex. 1021, U.S. Patent No. 6,402,033 (“Ohn”);
- Ex. 1022, U.S. Patent No. 6,138,916 (“Zolkos”);
- Ex. 1023, U.S. Patent App. Pub. 2005/0165784 (“Gomez”);
- Ex. 1024, U.S. Patent App. Pub. 2004/0146066 (“Palmade”);
- Ex. 1025, U.S. Patent App. Pub. 2003/0168515 (“Gray”);
- Ex. 1026, U.S. Patent App. Pub. 2006/0056216 (“Rhelimi”);
- Ex. 1027, L. A Mohammed et al., Smart Card Technology: Past, Present, and Future (2004) (“Mohammed”);
- Ex. 1033, U.S. Patent App. Pub. 2007/0026893 (“Sakamoto”);

- Ex. 1034, Finkenzeller, K., RFID Handbook, First Edition (“Finkenzeller-RFID”);
- Ex. 1038, U.S. Patent App. Pub. 2004/0214560 (“Date”);
- Ex. 1039, U.S. Patent No. 6,012,634 (“Brogan”); and
- Ex. 1040, Serway Jewett, Physics for Scientists and Engineers (6th ed., 2004).

IV. LEVEL OF ORDINARY SKILL IN THE ART

17. For purposes of this declaration, I do not dispute the following opinions of Mr. Dreifus:

- That the patent claims and prior art should be considered “through the eyes of a person of ordinary skill in the art at the time of the alleged invention,” and the various factors that contribute to that consideration as listed in Ex. 1003, ¶ 49;
- That the Challenged Claims are entitled to the benefit of the February 22, 2005 filing date of U.S. Patent Application No. 11/063,291 (“the ’291 Application”) (Ex. 1003, ¶ 50);
- That “person having ordinary skill in the art in this matter would have had at least a Bachelor’s degree in electrical engineering, computer engineering, computer science, or the equivalent thereof and approximately two years of

professional experience...,” where [a]dditional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.” Ex. 1003, ¶ 51.

18. I disagree with Mr. Dreifus that a POSITA in this matter necessarily must have specific experience in “the field of electronic devices used for transactions” rather than electronic devices more generally. *Id.* The technology at issue in this matter and the state of the art at the time of the ’219 patent’s priority date would be understood by a person who has the qualifications I list above, even without specific experiences with “electronic devices used for transactions.”

19. Although I disagree with Mr. Dreifus, many of the electronic devices I have designed or contributed to as a team member were used for transactions including: powering every transaction at EBay during the 1990-2000’s, any transaction performed by Nokia phones 2005-2010, and transactions performed by Broadcomm WiFi chips in the 2000-2010s.

20. Based on my experience, and whether under Mr. Dreifus’s definition or my own, I am qualified to render opinions regarding the technology claimed and described in the ’219 patent. Based on my expertise and qualifications, I am qualified to provide an opinion as to what a POSITA would have understood, known, or concluded as of the 2005 timeframe.

V. RELEVANT LEGAL PRINCIPLES

21. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. I have applied these legal principles in rendering my opinions below.

A. Claim Construction

22. I understand that the ordinary and customary meaning of a claim term is the meaning that the term would have to a POSITA at the time of the invention.

23. In the absence of an express intent on the part of the inventor to give a special meaning to the claim terms, the words are presumed to take on the ordinary and customary meanings attributed to them by a POSITA.

24. I understand that it is the use of the words in the context of the written description, and as customarily used by those skilled in the relevant art, that accurately reflects both the ordinary and the customary meaning of the terms in the claims.

25. I understand that the basis for a term's ordinary and customary meaning may be derived from a variety of sources, including the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art at the time of the invention.

26. I have been instructed that dictionary definitions or definitions from technical references can be used to inform or confirm the ordinary and customary meaning of words found in a claim, but that in construing claim terms, the general meanings gleaned from reference sources, such as dictionaries, must always be compared against the use of the terms in the context of the claim itself.

27. I understand that a patent applicant is entitled to be his or her own lexicographer (in other words, provide his or her own meaning to a word or phrase) and may rebut the presumption that claim terms are to be given their plain and ordinary meaning. To do so, the applicant must clearly set forth a definition of the term that is different from its ordinary and customary meaning. Where the applicant provides an explicit definition for a term, that definition will control interpretation of the term as it is used in the claim in which it appears. I understand that the specification can also be relied on for more than just explicit lexicography to determine the meaning of a claim term. For example, I understand that the meaning of a particular claim term may also be determined by implication, that is, according to the usage of the term in the context of the specification.

B. Anticipation

28. I understand that under U.S. Patent Law, 35 U.S.C. § 102, a claim is invalid as anticipated only if each and every element as set forth in the claim is actually disclosed, either expressly or inherently, in a single prior art reference.

29. I am informed that a reference is anticipatory if it contains the claim elements in the same order as claimed, regardless of whether the prior art and the claimed invention are directed to achieving the same purpose.

30. I am informed that a prior art reference may anticipate a claim without expressly disclosing a feature of the claimed invention if that missing feature is necessarily present, or inherent, in the single anticipating reference.

31. I am informed that inherency requires more than the probability or possibility that a claimed feature is present in the prior art, but rather that the feature or characteristic is a necessary part of the prior art. I also am informed that recognition of the inherency by a POSITA—at the time—is not required.

C. Obviousness

32. I understand that under U.S. Patent Law, 35 U.S.C. § 103, a claim is invalid as obvious if the differences sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

33. I am informed that an obviousness analysis requires an assessment of the scope and content of the prior art, the differences between the art and the claims at issue, and the level of ordinary skill in the art. I am told that it is against this backdrop that obviousness is assessed.

34. I am informed that a POSITA is a hypothetical person who is presumed to be aware of all the pertinent prior art. I am also informed that an obviousness analysis may take account of the inferences and creative steps that a POSITA would employ.

D. Enablement

35. I am informed that under U.S. patent law, a petitioner attempting to invalidate a patent for anticipation or obviousness, must establish enablement. I understand that without a showing of enablement, a petitioner cannot establish a reasonable likelihood of a patent being invalid for anticipation or obviousness.

36. I am informed that the test for enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the prior art, coupled with information known in the art without undue experimentation.

37. I am informed that the more that is known in the prior art about the nature of the invention, how to make, and how to use the invention, and the more predictable the art is, the less information needs to be explicitly stated in the specification.

38. I am informed that what is known in the art at the time of invention can provide evidence as to the question of predictability.

VI. BACKGROUND OF THE '219 PATENT

A. State of the art at the time of invention

39. Devices that communicate using RF communications, such as near field communication (NFC) devices, traditionally operate in either a passive mode or an active mode.

40. A passive RF device is characterized by the fact that it does not generate its own RF field; it relies instead upon an interrogating RF field generated by an active device. To communicate with the active device, the passive device modulates and reflects back the signal received from the active device. Passive devices are typically not powered by a battery or similar power source. Instead, the passive device builds a charge from the active device's signal in order to process, modulate, and return the active device's signal.

41. In contrast to passive devices, active devices are typically connected to a power source, such as a battery, and generate an RF signal. An active device communicates by transmitting its own generated signal to another device, rather than modulating a received signal.

42. Active and passive RF device communicate differently. When a passive device communicates with an active device, the active device continuously generates an RF signal and the passive device modulates and reflects back the same signal. When two active devices communicate, the devices must alternate their

transmissions, such that one device receives while the other device transmits. A device cannot both listen and transmit simultaneously.

B. Overview of the '219 patent

43. At a high level, the '219 patent describes and claims a mobile device with smartcard circuitry powered by that mobile device, for use in transactions.

44. The inventors of the '219 patent developed an innovative technology that advanced the state of the art when filed. In 2005, with the prevalence of mobile phones growing rapidly across the world, inventors Dr. Narendra, Mr. Tadepalli, and Mr. Spitzer envisioned a future in which mobile phones would replace consumers' wallets. They set out to invent a mechanism for consumers to use their phones, instead of cash, checks, or credit cards, to complete point-of-sale transactions.

45. The '219 patent claims are directed to circuitry for high-performance communications between mobile devices and point-of-sale payment terminals to facilitate speedy mobile contactless payments—a technology that is today commonly referred to as “tap to” functionality.

46. The '219 patent inventors also recognized that their solution would need to interface with existing point-of-sale infrastructure in order to maximize adoption.

47. In 2005, point-of-sale terminals relied primarily on magnetic stripe readers through which consumers would physically swipe a credit card with a

magnetic stripe. Ex. 1001, 1:22-25. At that time, while magnetic stripe cards and readers were prevalent, smartcards, i.e., those that were the shape and form of a magnetic stripe card, but were embedded with a small microprocessor that interacted with a different type of coordinating reader, were also becoming more common. *See, e.g.*, Ex. 1001, 3:3-6, 4:17-22, 4:64-67.

48. Further, the inventors sought to implement these inventions with an internal power source—that is, where the mobile phone could power these communications, rather than being powered by an external source. *See* Ex. 1001, 7:12-21.

49. Prior to the '219 patent, financial transactions required an electronic transaction card, like a credit card, to be swiped through a card reader, such that “[w]hen the card is swiped through a magnetic card reader, the information is transferred to the magnetic card reader to perform a transaction.” *Id.* at 1:22-25. Rather than requiring a physical swipe, the '219 patent contemplates implementing the invention by “emulat[ing] the swipe of a credit card.” *E.g., id.* at 3:2-5.

50. Additionally, the '219 patent discloses the use of “smartcard interfaces on electronic transaction cards.” *Id.* at 1:54-58; 11:8-10. These communications, stripe emulation or smart card, are used to effectuate transactions, including financial transactions, among other types. *See id.* at 3:40-47. In this way, “intelligent device

102 may program electronic transaction card 104 to operate as a credit card, a debit card, or the like.” *Id.* at 3:54-56.

51. In the ’219 patent, the intelligent electronic device is a mobile phone. *Id.* at 16:16-22 (claim 1). The electronic transaction card of the ’219 patent need not have a particular form factor, as long as it is compliant with integration within the phone. *Id.* at 4:8-22. The stripe on the card embodiment need not be visible, such as where “circuitry may be included within electronic transaction card 106 to produce the time-varying magnetic field and no visible indication may be present on an external face of electronic transaction card 104.” *Id.* at 3:12-15. Indeed, “in some embodiments of the present invention, transactions may utilize smartcard interfaces on electronic transaction cards in addition to, or in lieu of, stripes that emit time-varying magnetic fields.” *Id.* at 3:48-51.

52. The ’219 patent further describes that the smartcard functionality of the electronic transaction card is powered by the mobile phone. *See* Ex. 1001 (54) (“Apparatus with Smartcard Circuitry Powered by a Mobile Device”), 16:21-22 (“wherein the point-of-sale interface receives power from the mobile phone”); *see also id.* at 11:1-10. The ’219 patent describes various mechanisms for deriving power from the mobile phone itself to power the smartcard functionality:

Electronic transaction card 300 may include one or more power sources (not shown). For example, electronic transaction card 300 may include

a battery or a capacitor such as a supercapacitor. In some embodiments, a rechargeable battery may be included. The rechargeable battery may accept a charge from an add-on slot in an intelligent electronic device. In some embodiments, a capacitor may accept a charge from an intelligent electronic device. The capacitor may provide power to electronic transaction card 300 for enough time to perform a transaction.

Id. at 7:12-21.

53. Claim 1 of the '219 patent recites:

[1.pre] An apparatus with a compatible interface in a mobile phone,

[1.a] the apparatus including smartcard circuitry accessible by the mobile phone,

[1.b] the smartcard circuitry including a point-of-sale interface to communicate with a point-of-sale terminal,

[1.c] wherein the point-of-sale interface receives power from the mobile phone.

Ex. 1001, 16:17-22.

VII. ANALYSIS OF FOX

54. Mr. Dreifus opines that claims 1-6 of the '219 patent are anticipated or rendered obvious by Fox (Ground 1). I disagree with Mr. Dreifus's conclusions regarding Fox, for the reasons discussed below.

A. Overview of Fox

55. The invention of Fox incorporates electronics associated with a smartcard into the housing of a cellular telephone. Ex. 1009, Abstract.

56. Unlike the '219 patent, Fox does not contemplate powering smartcard circuitry via a mobile phone. Rather, Fox contemplates only *passive* smartcard circuitry housed within a phone and operable to communicate with a smartcard reader. *See, e.g.*, Ex. 1009, Abstract, 3:26-4:2.

57. Fox articulates a number of disadvantages associated with traditional plastic smartcards. As articulated in the Fox specification, it is disadvantageous to need to insert a smartcard into an external reader such as a point-of-sale system or an ATM. *Id.* at 1:9-30. Fox describes that smartcard functionality in a “plastic-type credit card presents additional problems.” *Id.* at 1:31-45. For example, the flexibility required to prevent breakage of the card in a wallet may lead to damage to incorporated electronics necessary for the smartcard functionality. *Id.*

58. Further, smartcards in the form of a credit card may be easily lost. A POSITA would therefore understand Fox to explain that its advantage is to “incorporate the electronics associated with a smart card into an alternative housing arrangement so as to overcome problems and disadvantages associated with flexible plastic smartcards,” and that “[a]dditionally, it would be desirable to provide a

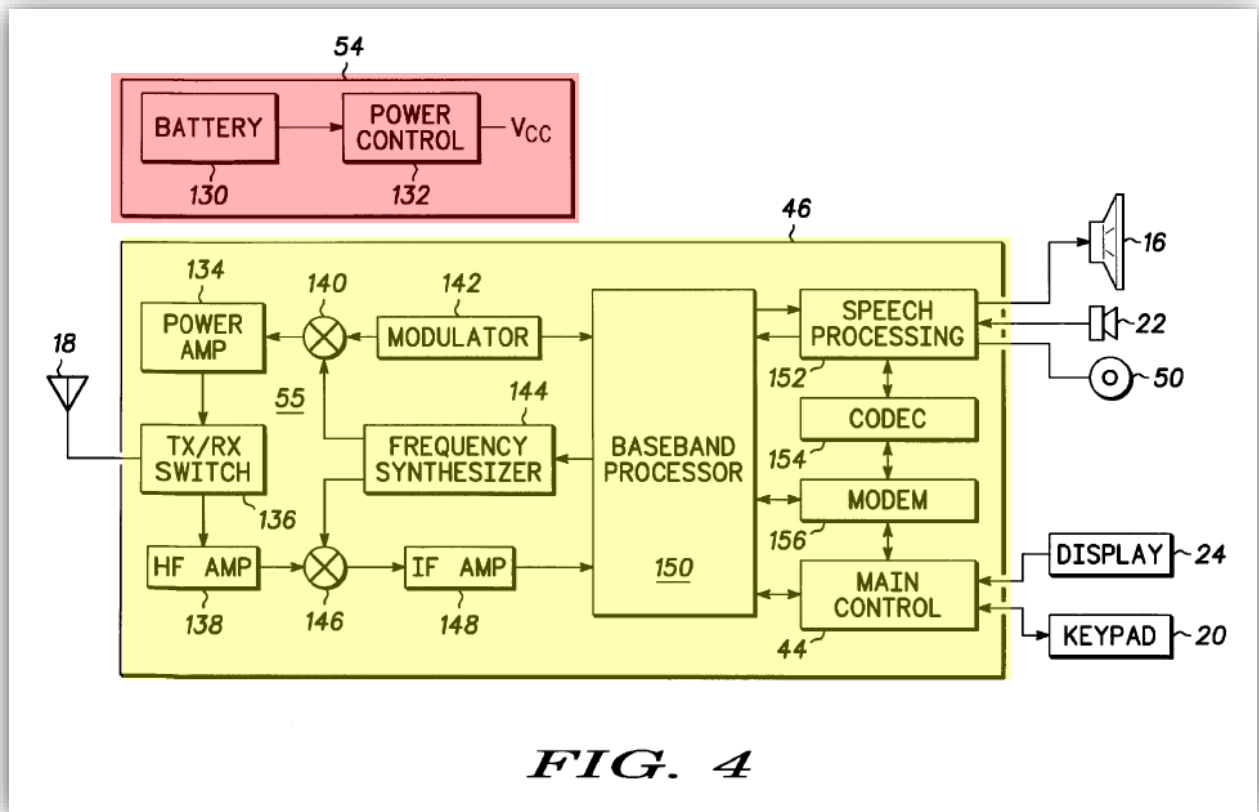
smartcard that does not require contact with an external reader in order to perform a transaction.” *Id.* at 1:46-1:52.

59. Thus, Fox teaches standard, unmodified smartcard functionality incorporated into a cellular phone alongside—and entirely distinct from—cellular phone functionality. *See, e.g.*, Ex. 1009, 2:13-16, 2:44-3:1, 4:42-46, FIG. 3, FIG 4 Fox repeatedly demonstrates that cellular functionality and smartcard functionality are separate systems within the cellular phone. *See id.* at 2:13-16 (“Cellular telephone 10 includes cellular telephone circuitry and smartcard circuitry (shown in block form in FIG. 2 and in detailed block form in FIGS. 3 and 4) for performing both a cellular telephone function and a smartcard function.”); *id.* at 2:30-33 (“Cellular telephone 10 includes casing 12 for housing the electronics for implementing both a smartcard function and a cellular telephone function as will be described and shown in more detail with respect to FIG. 2.”); *see also id.* at 2:44-3:1.

60. Indeed, Fox makes clear that these two functions are performed by separate circuitry within the cellular phone. *See id.* at 3:27-31 (“The present invention provides a cellular telephone that incorporates the electronic circuitry for implementing both a cellular telephone function and a smartcard function functions via smartcard circuitry 42 and cellular telephone circuitry 46, respectively.”) Fox

details the smartcard functionality in Figure 3 and the cellular functionality in Figure 4.

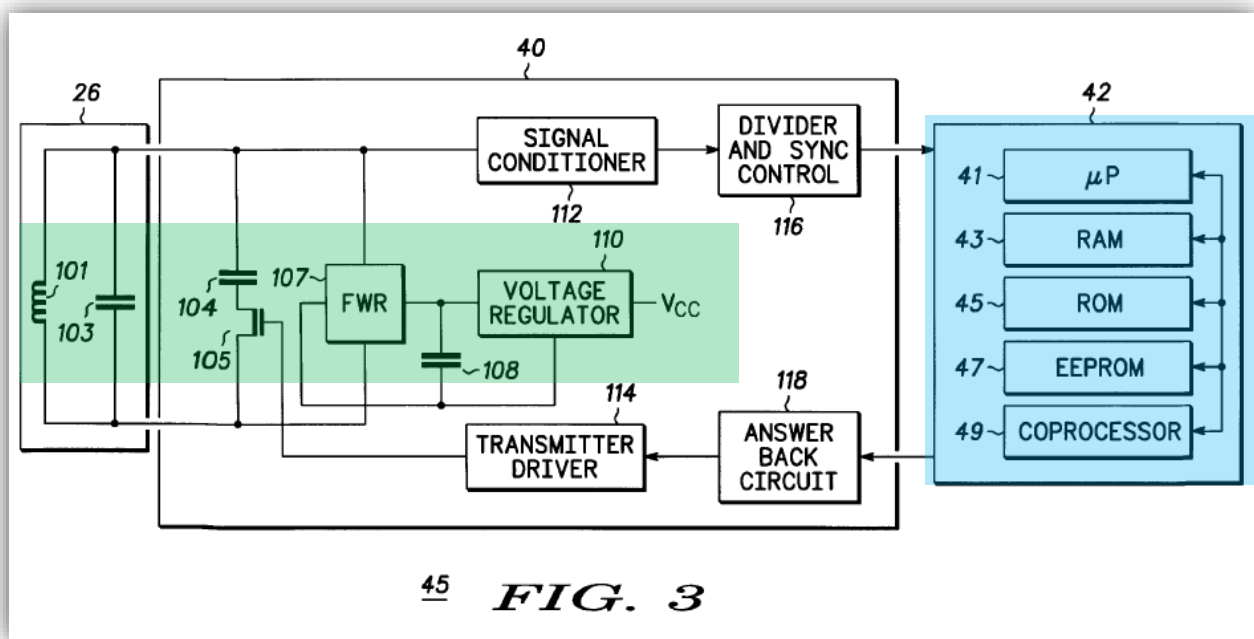
61. The cellular circuitry and the smartcard circuitry are also powered by different systems. According to Fox, the cellular functionality is powered by the battery of the mobile phone. *See id.*, 4:3-8 (“Cellular telephone circuitry 46 is powered via battery and power conditioner 54 which comprises a battery 130 and a power control 132.”); FIG. 4. This is demonstrated with reference to Figure 4, where the battery and power conditioner 54 (highlighted in red below) is illustrated with respect to the cellular telephone circuitry 46 (highlighted in yellow below) that it powers.



Id. at FIG. 4 (coloring added).

62. Separately, Fox’s smartcard functionality receives its power from an interrogating RF signal, and does not receive power from the mobile phone battery, as a POSITA would expect for the unmodified smartcard technology. As Fox describes, “antenna 26 may take the form, for example, of capacitor 103 and a wire such as inductor 101,” which together “form a tuned circuit that is resonant at the desired frequency of information and/or power transmission into the smartcard.” *Id.* 3:49-53 More, a “[p]ower supply voltage Vcc is generated via full-wave rectifier (FWR) 107.” *Id.* at 3:66-4:1. The rectified voltage is then filtered and regulated by

voltage regulator 110. *Id.* at 4:1-2. This is illustrated with reference to Figure 3, where the antenna 26, full-wave rectifier (FWR) 107, voltage regulator 110, and power supply voltage V_{CC} is shown (collectively, highlighted in green, as part of smart card RF interface 40) in connection with the smartcard logic function 42 (highlighted in blue).



Id. at FIG. 3 (coloring added).

63. Fox describes how the smartcard circuitry is powered by an interrogating RF field. “Generally, the smartcard function within cellular telephone 10 is interrogated or updated by a smartcard infrastructure using an RF field that is received by the integral smartcard antenna 26 whereby antenna 26 may be the same or separate from antenna 18 associated with the cellular telephone function.” *Id.* at

5:1-6. As Fox explains, “[w]hen a user desires to initiate a smartcard function with a corresponding RF reader, the user may, for example, cause cellular telephone 10 to come into the RF power range associated with RF interface 40 so that communication between the reader and cellular telephone 10 may be facilitated.” *Id.* at 5:13-18.

B. Fox Does Not Disclose “A Point-of-Sale Interface Powered by the Mobile Phone”

64. All challenged claims include a limitation “a point-of-sale interface powered by the mobile phone.” Ex. 1001, 16:17-22.

65. As described above, a major advance of the ’219 patent—as named in its title and as explicitly claimed—was that the smartcard circuitry within the mobile phone was powered by the mobile phone itself and not by an RF field into which the mobile phone entered. Ex. 1001, (54); 7:12-21; 16:20-22. That is, the ’219 patent claims an active system. Other efforts to incorporate smartcard functionality into mobile phones at the time of invention produced only passive systems requiring the RF field to power the smartcard circuitry.

66. Fox is one of those prior art systems, where smartcard circuitry (and the smartcard functionality it enables) is powered by introducing the mobile phone into an RF field and receiving power from that field. *See* Ex. 1009, 3:49-4:2 (“Smartcard antenna 26 may take the form, for example, of capacitor 103 and a wire such as

inductor 101. These two components form a tuned circuit that is resonant at the desired frequency of information and/or *power transmission into the smartcard.*") (emphasis added); *id.* at 5:1-18 ("Generally, the smartcard function within cellular telephone 10 is interrogated or updated by a smartcard infrastructure using an RF field that is received by the integral smartcard antenna 26 whereby antenna 26 may be the same or separate from antenna 18 associated with the cellular telephone function. ... *When a user desires to initiate a smartcard function with a corresponding RF reader, the user may, for example, cause cellular telephone 10 to come into the RF power range associated with RF interface 40* so that communication between the reader and cellular telephone 10 may be facilitated.") (emphasis added); FIG. 3; FIG. 5.

67. Mr. Dreifus opines that that the smartcard circuitry is powered by the battery and power conditioner 54. Ex. 1003, ¶¶ 80-81 (citing Ex. 1009, 4:3-8). I disagree. Fox *only* describes the battery and power conditioner 54 in connection with the cellular functionality. Ex. 1009, 4:3-8. Fox refers to Figure 4 as "a more detailed block diagram... illustrating the *electronic circuitry of cellular circuitry 46,*" i.e., the separate cellular circuitry and functionality *distinct from* the smartcard circuitry 45 depicted in Figure 3. Ex. 1009, 4:3-5. Fox gives no indication that the battery and power conditioner 54 powers the smartcard circuitry 45. Likewise, Fox describes the smartcard circuitry 45 as *only* receiving power from an interrogating RF field. *Id.* at

5:1-17; *see also id.* at 3:66-4:2. Nothing in Fox discloses powering the smartcard interface, including 40 the RF interface, from the battery—quite the opposite, as in FIG. 3. *See id.* at 3:66-4:2 (description of powering of smartcard functionality). Fox discloses no smart card functionality other than smartcard function 45, smartcard logic function 42, and smartcard RF interface 40 of FIG. 3, all of which are powered by the interrogating RF field.

68. A POSITA would understand Fox to only disclose standard prior art technology—where the smartcard function 45 (composed of smartcard RF interface 40 and smartcard logic 42) of Fox is powered by the RF circuit. In describing the RF interface 40 and smartcard circuitry 42, Fox’s specification only discusses the power supply voltage V_{cc} generated from the full-wave rectifier 107 and regulated by voltage regulator 110, which a POSITA would understand to be a passive system. Ex. 1009, 3:49-4:2.

69. A POSITA would understand Fox to teach that battery and power conditioner 54 powers *only* the cellular telephone circuitry 46. Nor is Mr. Dreifus correct that power control 132, a component within battery and power conditioner 54, powers the smartcard circuitry 40. Ex. 1003, ¶ 80. Instead, as described in Fox’s specification, smartcard circuitry 40 is powered via a different component—including voltage regulator 110, which receives power from the RF field into which cellular telephone 10 is introduced. Ex. 1009, 3:35-4:2; *id.* at 5:1-18; FIG. 3.

70. To the extent Mr. Dreifus bases his opinion on Figure 2 of Fox to demonstrate that the battery and power conditioner 54 powers the smartcard 45, that is not how a POSITA would understand Figure 2. Rather, a POSITA would understand smartcard functionality to be powered by an RF signal regulated by voltage regulator 110 of Figure 3. If anything within the smartcard of Figure 2 is possibly powered by the battery and power conditioner 54 at all, it would be the display and audio capabilities. Ex. 1009, 4:56-67. These functions are not part of the RF interface (40) and are solely subfunctions of the smartcard logic functions within 42, although not shown in Figure 3. It would be well known by a POSITA that this display and audible functionality are not part of a typical smartcard functionality and non-standard functionality could require external power.

71. Nor is Mr. Dreifus correct that power control 132, a component within battery and power conditioner 54, powers the smartcard circuitry 40. Ex. 1003, ¶¶ 80-81. Instead, as described in Fox's specification, smartcard circuitry 40 is powered via a different component—including voltage regulator 110, which receives power passively from the RF field into which cellular telephone 10 is introduced. *See* Ex. 1009, 3:35-4:2; *id.* at 5:1-18; FIG. 3.

72. Altogether, Fox discloses a system with distinct cellular and smartcard circuitries and functionalities. Each of those is depicted in its own figure (Figure 3 and Figure 4) and powered by separate sources, as described in the specification.

The smartcard circuitry 40 is powered by an external RF signal—and does not “receive power from the mobile phone” as claimed in all challenged claims of the ’219 patent. Thus, Fox cannot anticipate or render obvious the claims of the ’219 patent.

VIII. ANALYSIS OF THE COMBINATION OF FOX AND TAKEKAWA

73. Mr. Dreifus opines that claims 1-6 of the ’219 patent are obvious in view of the combination of Fox and Takekawa (Ground 2). I disagree with Mr. Dreifus’s conclusions regarding the combination of Fox and Takekawa, for the reasons discussed below.

A. Overview of Takekawa

74. U.S. Patent App. Pub. No. 2005/0015275 entitled “Information Processing Device and Information Processing Terminal” to Takekawa et al. (Ex. 1020 or “Takekawa”) is directed to “an information processing device such as an IC card that is capable of retaining data in a secure manner” which is inserted into “an information processing terminal such as a portable telephone.” Ex. 1020, [0002].

75. Prior art IC cards required software necessary to carry out the functions related to the data stored on the IC card to be downloaded “via a network” from service providers. *Id.* at [0006]-[0007]. The invention of Takekawa involves that software being present on the portable, removable IC card. *Id.* at [0016]-[0017], [0083]-[0084].

B. A POSITA Would Have Neither a Reason to Combine Doughty and Fox or an Expectation of Success from the Combination.

76. Mr. Dreifus contends, “In my opinion, a person of ordinary skill in the art would have been motivated to apply Takekawa’s teaching of using a removable smartcard to Fox’s smartcard device to advantageously allow a user to switch the smartcard device between devices.” Ex. 1003, ¶ 104; *see also id.* at ¶ 105 (“In my opinion, a person of ordinary skill in the art would have found that using a removable smartcard in Fox’s phone to be straightforward.”). Mr. Dreifus further opines, in my opinion, a person of ordinary skill in the art would have been motivated to apply Takekawa’s teaching of installing software on a phone with a removeable smartcard to Fox’s mobile phone.” *Id.* at ¶¶ 106-107.

77. A POSITA would not look to combine Fox and Takekawa as both address significantly different issues within electronic transactions and propose solutions that are contrary to the other. Further, the two references operate using incompatible technologies and protocols.

78. Fox seeks to address problems caused by “smartcards housed within a plastic card.” Ex. 1009, 1:12. A problem with these portable smartcards is that “small plastic smartcards are easy to misplace, lose, or steal thereby resulting in the user being without their smartcard as well as a third party having unauthorized access to their smartcard.” *Id.* at 1:42-45. “Accordingly,” Fox teaches, “it would be desirable

to incorporate the electronics associated with a smartcard into an alternate housing arrangement so as to overcome problems and disadvantages associated with flexible plastic smartcards.” *Id.* at 1:46-49. Fox repeatedly teaches that “integration of a contactless smartcard into a cellular telephone function provides ... enhanced security from theft or loss.” *Id.* at 2:18-23; *see also id.* at 3:26-34 (“The present invention provides a cellular telephone that ... allows the smartcard electronics to be protected from damage by the housing associated with the cellular telephone and also decreases the likelihood that the smartcard will be lost or stolen.”).

79. A POSITA would therefore understand that an important objective of Fox would be to have non-removable, non-portable smartcard circuitry, in order to prevent that circuitry from being lost, stolen, or damaged.

80. On the other hand, the goal of Takekawa is to create a portable IC card that holds important data and software separate from a mobile phone, which can then be inserted into (and therefore also removed from and stored separately from) a mobile phone. Ex. 1020, [0016]-[0017], [0083]-[0084].

81. A POSITA would not be motivated to combine a system seeking to avoid portable cards that can get lost, stolen, or misused by “integrating” a smartcard into a mobile phone (Fox), with a system that touts a portable IC card loaded with data and software (Takekawa) that itself could be lost or stolen.

82. I therefore disagree with Mr. Dreifus' conclusions that "a person of ordinary skill in the art would have been motivated to apply Takekawa's teaching of using a removable smartcard to Fox's smartcard device." Ex. 1003, ¶¶ 104-107. I see no motivation for this combination, and rather believe that a POSITA would be discouraged from this combination.

C. Even if They Were Combined, The Combination of Fox and Takekawa Does Not Disclose The Limitations of the '219 Patent

83. Even if Fox and Takekawa were combined, the combination does not disclose all limitations of the '219 patent claims.

84. Mr. Dreifus contends only that Takekawa would supply the "apparatus including software to be installed on the mobile phone" claimed in the '219 patent. Ex. 1003, ¶ 101.

85. Mr. Dreifus and Petitioner make no argument that Takekawa discloses the "a point-of-sale interface powered by the mobile phone" limitation of the '219 patent claims. As described above, that limitation is lacking from Doughty. Thus, combining these two references, even where it is possible, does not disclose the claims of the '219 patent.

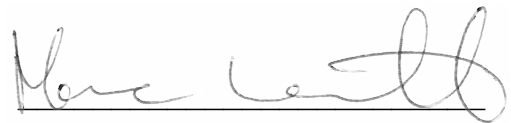
IX. ADDITIONAL REMARKS

86. I reserve any right that I may have to supplement this declaration if further information becomes available or if I am asked to consider additional

information or to submit an additional declaration if inter partes review is instituted. Furthermore, I reserve any right that I may have to consider and comment on any additional expert statements and testimony of Petitioners' experts in this matter.

87. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Dated: July 16, 2025

A handwritten signature in black ink, appearing to read "Marc Levitt", written over a horizontal line.

Marc E. Levitt, Ph.D.

APPENDIX A

MARC E. LEVITT, PH.D.

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**Technology Development ▪ Patent/IP Consulting ▪ Business Development
Startup Ventures, Hardware, Software and Systems**

Independent consultant with 30+ years of experience in the areas of executive leadership, business development, technology, technology development, and intellectual property. Broad technical and business depth in computer architecture, networking, mobile, semiconductor design, semiconductor manufacturing, systems-on-a-chip, systems architecture, technical software, embedded software, enterprise software, algorithms, and computational finance. Experience in negotiating IP/patent related issues as part of technology sharing agreements, licensing, and M&A. Strong track record in turn around management and developing new strategic markets through internal development, start-ups, and M&A.

**AREAS OF
EXPERTISE**

Computer Architecture: RISC, CISC, DSP, GPU, memory hierarchies, pipelining, clock design, power management, low power design, microcode, microarchitecture, multicore, memory controllers, 2d & 3d graphics, interconnects/NoC, PCI, PCIe, USB2, USB3, UFS, SDIO, MIPI DSI.

VLSI Design: All aspects of front to back design process and methodologies for digital, analog, and mixed signal designs. Includes RTL (Verilog & VHDL), logic, circuit, physical design, layout, verification. Tapeouts to: IBM, TSMC, UMC, TI, NEC, LSI Logic, & Mitsubishi.

VLSI Manufacturing: CMOS, mask making, OPC, testing, packaging, yield enhancement, debug, failure analysis, and production ramp.

Software: Computer aided design (CAD), drivers, BIOS, operating systems (Windows, Linux, Unix, Android, etc), mobile software, embedded software, JSRs, client-server software, enterprise software, applications, large web based systems (Google, Facebook, AWS etc), algorithms, video streaming, and computational finance.

Systems: Systems-on-a-Chip, VoIP, networking, multiprocessors, servers, PCs, parallel processing, distributed computing, mobile phone, tablets, set-top-boxes, DTV, digital camera/camcorders, automotive, encryption/security, power management, video streaming, MPEG, H264, H265, IEEE 802.x/Ethernet, switching, routing, Bluetooth.

Video: DASH, HLS, Dash.js, ExoPlayer, PlayReady DRM, Widevine DRM, MPEG, H264, H265, VP9, AV1, ffmpeg, GStreamer, CAMF, CENC, BMFF, encoding pipelines, decoding, packaging, all SoC hardware.

Business Development. Product development teams, software product lines, and semiconductor product development projects. Includes strategy, execution, division P&L, margin improvement, and cost management. New product introduction in both large companies and start-ups. Market and technology roadmap development and execution.

PROFESSIONAL EXPERIENCE**Consultant Levitt Technologies****2007 - Present**

Independent consultant in the areas of: technology development, intellectual property, and business development/strategy.

Clients in business strategy and technology development include start-ups, VCs, Private Equity firms, and public companies in areas of software, networking hardware, and semiconductors. Partial list of former clients: PhysWare/Nimble (sold to Mentor Graphics Q2'14), PwrLite Software (sold to Xilinx Q3'09), Proficient Design, and Credence Test Systems.

Intellectual property consulting clients are IP investors, patent brokers, public & private corporations, law firms and their clients in the semiconductor, communications, software, and systems areas. Experience at District Court, ITC, and PTAB including expert reports and being deposed.

Complete list available upon request.

Girasole Imports LLC**2014 – Present****Managing Member**

Italian wine importer and distributor for California.

Commodity Trading Advisor**1999 – Present**

Registered Commodity Trading Advisor with NFA ID 0311607

LongRun Technologies LLC**2010 – 2022****MEMBER**

LongRun Technologies LLC owns and administers former Transmeta LongRun Technology licensing agreements with five (5) major semiconductor and systems companies.

Video Over Cellular Innovations LLC**2010 – 2011****CHIEF TECHNICAL OFFICER**

Responsible for technical positioning and analysis to support the sale of this Emmy Award winning mobile video technology, IP, and associated patents. Worked with potential purchasers and bankers on due diligence. Helped successfully support sale to Samsung October 2011. Patents were part of Apple-Samsung litigation.

Cadence Design Systems, San Jose, California**2002 – 2007****VICE PRESIDENT & GENERAL MANAGER**

Ran Cadence's Design for Manufacturing (DFM) Business Unit. This unit is responsible for enterprise class technical software used in semiconductor design, analysis, and manufacturing. Profit/loss responsibility for ~\$130M/year business worldwide and ~240 worldwide employees in R&D, operations, marketing, sales, and AE teams. Locations in Taiwan, Japan, Russia, India, along with three primary locations in the United States (CA, NJ, NC).

- Lead business partner in creating the corporate partnerships between Cadence and ASML, Cadence and Applied Materials, Cadence and Hitachi HiTech, and Cadence and IBM. Included all IP rights and patent issues.
- Initiated and negotiated M&A activity in support of business unit and company's strategic objectives. Drove the purchase of two start-ups by Cadence for DFM BU. Experience in evaluating and developing business models, financial models, sources of value calculations, synergies, due diligence.
- Present at IEEE conferences such as DAC and ISQED. Participation ranges from technical papers, panel sessions, to keynote addresses.
- Analyst Day team member. Help represent Cadence to Wall Street by presenting Yield and DFM strategy to analysts and fund managers during the event.
- Turned around business unit and drove margins from negative territory to top quartile companywide. Maintained and improved morale, expanded product line, technically overtook competition in key sectors, and improved customer relationships.

Transmeta Corp, Santa Clara, CA**2000 – 2002****DIRECTOR VLSI**

Product manager and architect in charge of running the TM6000 1GHz x86 Low Power System on a Chip project. Responsible for the logic, verification, and circuit design teams on this unique project that integrated a 1GHz x86 processor, north bridge, south bridge, and graphics engine in 130nm/90nm technology. Duties include all hardware product management responsibilities, scheduling, resource planning, and lab prototype work. Interaction with software engineering (CMS, BIOS, and drivers), systems engineering, packaging, foundry, and operations. Coordinate and drive all teams (hw, sw, system) to deliver on commitments.

Sonics Inc, Mountain View, CA**1998 – 2000****DIRECTOR SILICON DEVELOPMENT**

In charge of in-house deep sub-micron design projects in 0.18um CMOS. Responsible for developing, planning and executing product ideas, SoC platforms, and OEM silicon based on the Sonics' Integration Architecture. Ownership encompassed product definition, project planning, resource development, resource allocation, packaging, and test. Designed OC-12 network processor (MIPS based) and assisted in two VoIP chipsets for clients.

**Independent
CONSULTANT**

1997 – 1998

Clients included Transmeta and Raycer Graphics (now Apple). Worked in the areas of clocks, reset, design-for-test, design-for-debug, and power management. Consulted with management, design teams and product engineering teams on foundry, debug, yield, quality and test issues.

**High Frequency Finance, Sunnyvale, CA
FOUNDER**

1996 – 1998

Company started to develop and deliver a new generation of decision support tools to professional traders and treasury professionals with emphasis on FX. Extensive work in nonlinear statistics, quantitative finance, and real-time software. Realtime streaming software development for Reuters and Bloomberg. Worked with leading money managers and hedge funds.

**Sun Microsystems, Mountain View, CA
SR HW MANAGER & SR STAFF ENGINEER**

1990 – 1997

- Significant operational experience performing design, management, and product ramp related tasks.
- Responsible for the test and design-for-test strategy for all SPARC microprocessors and related ASICs, JAVA processors, processor modules, and SPARC reference platform designs.
- Corporate wide consultant on power management, clocking, reset, test, design-for-test, and debug issues.
- Key member of VLSI Design Review team – reviewed and signed off on every circuit design used inside Sun's custom chips.
- Member of ATE selection committee and key interface to test and product engineering organization both inside and outside of Sun.
- Staff Engineer working on the UltraSPARC-I processor. Developed the power management, clocking, test strategy and methodology used for the project at the chip, module, and system level. This strategy and methodology was adopted as a division wide standard used by UltraSPARC-I+, UltraSPARC-II, UltraSPARC-IIi, and UltraSPARC-III.
- Responsible for the evaluation CAD tools. Worked closely with tool vendors to specify new features and functionality. Responsible for specification and some implementation of in-house CAD tools that were directly tied to our advanced design practices.
- Developed, specified, and patented a methodology for fast synchronous SRAM testing that was adopted as a JEDEC standard.

ADDITIONAL EMPLOYMENT

VLSI Testing Research, Hewlett-Packard, 1989

EDA Software Development, Digital Equipment Corporation 1988

PUBLICATIONS, HONORS, AWARDS

Sixteen patents awarded in the areas of circuit design, logic design, hardware testing, software, diagnosis, and formal verification

Over 30 journal, conference publications, and book chapters

Sun Microelectronics Engineering Excellence Award 1996.

Member of Tau Beta Pi and Eta Kappa Nu Engineering Honor Societies

Guest editor of *IEEE Design & Test of Computers* magazine for a special issue on microprocessors January-March 1997.

EDUCATION

MS and PhD in Electrical Engineering, University of Illinois, Urbana, IL, 1986-1990

BS with High Honors Computer Engineering, Lehigh University, Bethlehem, PA, 1982-1986

PUBLICATIONS LIST

JOURNALS AND CONFERENCES

1. "Moving Manufacturing More Effectively Into Design," *DesignCon* 2007.
2. "The Impact of DFM in the Design Phase below 90 Nanometers," *DesignCon* 2006
3. "Making the (Yield) Difference: DFY/DFM," *Proceedings 24th VLSI Test Symposium*, 2006.
4. "Using yield-focused design methodologies to speed time-to-market," *Proceedings of the SPIE Design and Process Integration for Microelectronic Manufacturing III*, 2005.
5. "What Is Design for Yield, and How Do We Get There?" *DesignCon* 2005.
6. "Collaborating Effectively on the Rocky Road to DFM" *FSA Suppliers Expo & Conference* 2005
7. "Using Yield-Focused Design Methodologies to Speed Time-to-Market," *DesignCon* 2005.
8. "Design for manufacturing? Design for yield!!!," *Proceedings 5th International Symposium on Quality Electronic Design*, 2004.
9. "When IC yield misses the target, who is at fault?," *Proceedings 41st Design Automation Conference*, 2004
10. "SOC Testing - Throwing the Baby out with the Bath Water!" *IEEE BAST Workshop*, 2000.
11. "FXYYI?: A Foreign Exchange Yield Investing Index," *Proceedings of Forecasting Financial Markets and Computational Finance*, 2000.
12. "System-on-Chip Debug and Test," *IEEE BAST Workshop*, 1999
13. "Market Time Data™ Improving Technical Analysis and Technical Trading," *Proceedings of Forecasting Financial Markets*, 1998.
14. "Microprocessors Lead The Way In Complex Design," *IEEE Design & Test of Computers*, vol.14, no.1, Jan-Mar 1997
15. "Designing UltraSparc for testability," *IEEE Design & Test of Computers*, vol.14, no.1, Jan-Mar 1997
16. "A fault diagnosis methodology for the UltraSPARC-I microprocessor," *Proceedings European Design and Test Conference*, 1997.
17. "Formal verification of the UltraSPARC family of Processors via ATPG Methods," *International Test Conference*, 1996.
18. "Market Time and Short-Term Forecasting of Foreign Exchange Rates", *Proceedings of Neural Networks in the Capital Markets*, 1996.
19. "A 64-b microprocessor with multimedia support," *IEEE Journal of Solid-State Circuits*, Nov 1995
20. "Testability, debuggability, and manufacturability features of the UltraSPARC-I microprocessor," *Proceedings International Test Conference*, 1995.
21. "A 64b microprocessor with multimedia support," *Digest of Technical Papers IEEE International Solid-State Circuits Conference*, 1995.
22. "UltraSPARC: The next generation superscalar 64-bit SPARC," *Digest of Papers Compcon '95. Technologies for the Information Superhighway*, 1995
23. "Practicing DFT: The Good, The Bad, and The Ugly" *IEEE BAST Workshop*, 1995
24. "Exploitation of Market Inefficiencies via Nonlinear Prediction," *Proceedings of Neural Networks in the Capital Markets*, 1994.
25. "BiCMOS logic testing," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Jun 1994
26. "Microprocessor Testing: Which technique is best?" *Proceedings 31st Design Automation Conference*, 1994.
27. "SPARCcenter 2000: Multiprocessing for the 90's," *Digest of Papers Compcon Spring '93*, 1993
28. "Economic and productivity considerations in ASIC test and design-for-test," *Digest of Papers Compcon Spring '92*, 1992
29. "ASIC testing upgraded," *IEEE Spectrum*, vol.29, no.5, May 1992
30. "The effect of multiple charge-discharge paths on testing of BiCMOS logic circuits," *Proceedings 3rd European Conference on Design Automation*, 1992.
31. "Test considerations for BiCMOS logic families," *Proceedings of the Custom Integrated Circuits Conference*, 1991
32. "Physical design of testable VLSI: Techniques and experiments," *IEEE Journal of Solid-State Circuits*, Apr 1990
33. "BiCMOS fault models: Is stuck-at adequate?," *Proceedings International Conference on Computer Design: VLSI in Computers and Processors*, 1990.
34. "Just-in-time methods for semiconductor manufacturing," *Proceedings Advanced Semiconductor Manufacturing Conference and Workshop*, 1990.
35. "Physical design of testable VLSI: Techniques and experiments," *Proceedings of the IEEE Custom Integrated Circuits Conference*, 1989.

36. "The economics of scan design," *Proceedings International Test Conference*, 1989.

BOOK CHAPTERS

1. *Market Time and Short-Term Forecasting of Foreign Exchange Rates*, in **Decision Technologies for Financial Engineering**, A. Weigend, Y. Abu-Mostafa, and P. Refenes eds., World Scientific, Singapore, 1997.
2. *Machine Learning for Foreign Exchange Trading*, in **Neural Networks in the Capital Markets**, P. Refenes ed., John Wiley & Sons, Chichester, UK, 1995.
3. *BiCMOS Testing*, in **BiCMOS Technology and Applications 2nd Edition**, A.R. Alvarez ed., Kluwer Academic Publishers, Boston, MA, 1993.

PATENT LIST

1. US5341382 "Method and apparatus for improving fault coverage of system logic of an integrated circuit with embedded memory arrays", 1994
2. US5379303 "Maximizing improvement to fault coverage of system logic of an integrated circuit with embedded memory arrays", 1995
3. US5513186 "Method and apparatus for interconnect testing without speed degradation", 1996
4. US5528165 "Logic signal validity verification apparatus", 1996
5. US5570376 "Method and apparatus for identifying faults within a system", 1996
6. US5774474 "Pipelined scan enable for fast scan testing", 1998
7. US5787012 "Integrated circuit with identification signal writing circuitry distributed on multiple metal layers", 1998
8. US5850150 "Final stage clock buffer in a clock distribution network", 1998.
9. US5864564 "Control circuit for deterministic stopping of an integrated circuit internal clock", 1999
10. US5870408 "Method and apparatus for on die testing", 1999
11. US5872796 "Method for interfacing boundary-scan circuitry with linearized impedance control type output drivers", 1999
12. US5892778 "Boundary-scan circuit for use with linearized impedance control type output drivers", 1999
13. US5898702 "Mutual exclusivity circuit for use in test pattern application scan architecture circuits", 1999
14. US5900757 "Clock stopping schemes for data buffer", 1999
15. US6081913 "Method for ensuring mutual exclusivity of selected signals during application of test patterns", 2000
16. US8549339 "Processor core communication in multi-core processor", 2013.