# SCOTT EMMET THOMPSON

*Prof. Electrical Engineering and Computer Science Department / Univ. of Florida*
*IEEE Fellow for contributions on advancing MOSFETs*
*Former Intel Corporation Fellow and Director of Computer Chip Technology*

## A. Education and Training

### Education

1992 Ph.D. (Electrical Engineering), University of Florida
1988 Master of Science in Electrical Engineering, University of Florida
1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

## B. Professional Experience

- Tenured Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
  - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- Researcher on advanced chip technology at University of Florida totaling $4M worth of research contracts.
  - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- Consultant (non litigation) last last 5 years: Xperi Corporation
- **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

## C. Legal cases

- Bold is the client
  - Godo Kaisha IP Bridge v/ **Xilinx**/**TSMC**
    - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017

- KAIST IP v. **Apple**
    - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
    - Case in Korea : Intellectual Property Trial and Appeal Board ("IPTAB") regarding Korean Patent No. 10-0458288 (hereinafter, "KR '288 patent").
- Godo Kaisha IP Bridge, Inc. v. **NVIDIA**
    - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1
- Chinese Academy of Sciences v. **Intel**
    - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
    - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
    - Beijing Court Testimony IME vs Lenovo 11/21/2021
    - Beijing court Testimony IME vs Intel China 1/12/2022
- IFT v. **TSMC (**ITC case)
    - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
    - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- NXP v. **Impinj**
    - 9,495,631, IPR2020-00543 - filed 2/10/2020
    - 9,633,302, IPR2020-00516 - filed 2/5/2020
    - 6,680,523, IPR2020-01630 - filed 9/17/2020
    - 7,538,444, IPR2021-00003 - filed 10/5/2020
    - Oakland District Court Case No. 4:19-cv-03161-YGR
- Katana Silicon Technology LLC v. **GlobalFoundries** 2022
    - IPR2022-01083
- Ericsson v. **Apple** Brazil Patent BRPI 9811639-8 filed 2022
- Greenthread v. **Intel** Case 6:22-cv-105-ADA filed 12/2022
- ITC Daedalus v. **TSMC** Case 337-TA-1336 filed 10/2022
- Oasis Tooling, Inc v. **GlobalFoundries** C.A. No. 22-312-CJB 3/2023
- BiTMICRO LLC v. **Intel** IPR2023-00781 filed 3/31/2023
- Longitude Licensing LTD, v **Western Digital Technologies, Inc**. IPR2023-01286 filed 8/08/2023

**Honors and Awards**

- 100 granted US patents, 60 publications and 1 book on semiconductors
- Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- Elected to Intel Fellow in 2003
- Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- 2008 SEMI award North American Recipient

- 2014 TiE 50: Top Startup (SuVolta)
- 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- 2011 EuroAsia IC Industry Award for start-up
- 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

**D. Publications/Patents**

[1] T. A. Weingartner, C. -H. Kuo, A. Thomas, S. E. Thompson and M. E. Law, "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, doi: 10.1109/TCPMT.2021.3095670.

[2] C.-H. Kuo, T. A. Weingartner, M. E. Law, S. E. Thompson, and A. Appaswamy, *Effect of Stress on Bipolar Transistor,* SRC TECHCON 2021

[3] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent 10,250,257, 2019.

[4] S. E. Thompson et al., "Advanced Transistors with Punch Through Suppression", US Patent US10325986B2, 2019.

[5] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10,217,668, 2019.

[6] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10224244B2, 2019.

[7] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent US20180248548A1, 2018.

[8] S.E. Thompson et.al., "Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof", US9865596B2, 2018.

[9] S.E. Thompson et al. "Integrated Circuit Devices and Methods", US Patent US9966130B2, 2018

[10] S.E. Thompson et al. "Buried Channel Deeply Depleted Channel Transistor, US Patent US9991300B2, 2018.

[11] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent US10074568B2, 2018

[12] S.E. Thompson et al., Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof" US Patent US9922977B2, 2018.

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[15] S. E. Thompson et. al., “Field Effect Transistor And Method For Producing The Same,” JP2017055140A, 2017.

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[21] S. E. Thompson et. al., “CMOS Gate Stack Structures And Processes,” US 9,508,728 B2, 2016.

[22] S. E. Thompson et. al., “Integrated Circuit Devices and Methods,” US 9,362,291 B1, 2016.

[23] S. E. Thompson et. al., “Method For Fabricating A Transistor With Reduced Junction Leakage Current,” US 9,368,624 B2, 2016.

[24] S. E. Thompson et. al., “Advanced Transistors With Punch Through Suppression,” US 9,263,523 B2, 2016.

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[30] S. E. Thompson et. al., “CMOS Structures and Processes Based On Selective Thinning,” US 9,391,076 B1, 2016.

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[32] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, and Methods Therefor,” US 2016/0020768 A1, 2016.

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[63] S. E. Thompson et. al., “Advanced Transistors With Punch Through Suppression,” US 8,421,162 B2, 2013.

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