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Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS

P. Morin, D. Benoit, F. Perrier[b], C Chaton[a], M. Charleux, J. Regolini, K. Barla, and P. Ferreira

STMicroelectronics, - 850 rue Jean Monnet, F-38928 Crolles, France
a-CEA-LETI, - 850 rue Jean Monnet, F-38928 Crolles, France
b-NXP - 850 rue Jean Monnet, F-38928 Crolles, France
pierre.morin@st.com

Mobility enhancement by process induced strain in the Si channel has been extensively used since 90nm node to improve transistor drive current. Such technique becomes mandatory to compensate scalability limits of several processes like ultra thin gate oxide growth. The Contact Etch Stop nitride Layer (CESL) is the most commonly used method to get stress induced mobility enhancement. However, the re-engineering of this nitride layer for stress enhancement needs to cover all electrical aspects including reliability characteristics, in particular the Negative Bias Temperature Instabilities (NBTI). In this work, we confirm that pMOS NBTI can be significantly impacted by the nitride CESL properties. A Design Of Experiment methodology allows demonstrating that the NBTI is enhanced by the nitride weight density, linked to hydrogen diffusivity within the film. It is finally shown that the nitride density must be set as low as possible to minimize the NBTI.

Introduction

Mobility enhancement by process induced strain in the Si channel is mandatory to reach the transistors performances since the 90 nm node, to compensate scalability limits of several processes like as example the ultra thin gate oxide growth. Among the technical solutions developed to generate some strain in the silicon channel, mechanical stress engineering of the contact etch stop nitride layer (CESL) is the most commonly used method. This low cost method allows getting highly strained transistor channels and therefore stress induced mobility enhancement (1-2). It has been introduced first in 90 nm node (Figure 1) and is still considered as one of the most efficient boosters in advanced process flows such as in 45nm node, since it can be added to other stressor techniques (3-4).

As seen before, electron and hole mobility has to be improved compared to the un-strained silicon case in the same time. Electron mobility enhancement is obtained by increasing the tensile strain in the silicon channel in transistor length L and width W direction (see Figure 2). Similarly, a more compressive channel in vertical z direction will also improve the nMOS performance as summarized in Table I (3, 4). Experiments have shown that a tensile CESL will generate tensile strain in the silicon channel plane and a compressive strain in the out of plane direction. Following similar considerations, it is

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shown that pMOS drive current is improved by compressive CESL which makes difficult to find a compromise for the CMOS technology.

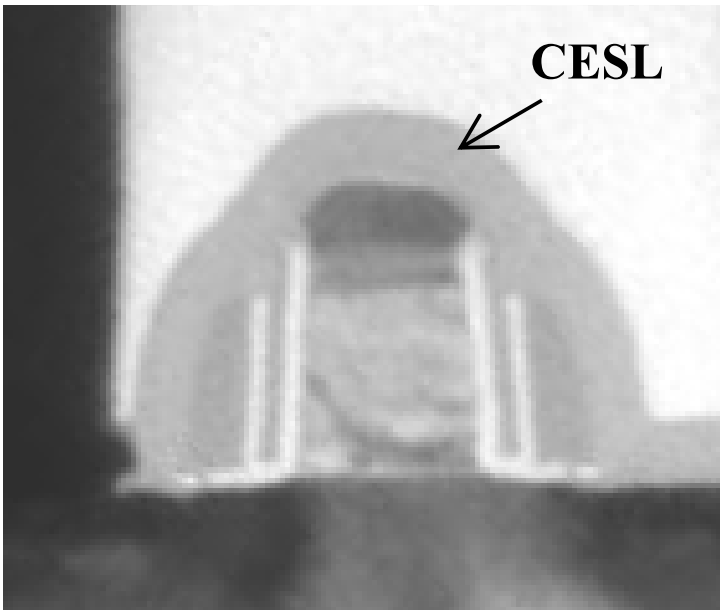

Figure 1. Typical 90 nm node CMOS Low Power transistor. Lg= 65 nm, EOT = 21 Å, V_{DD} = 1.2 V.

However, in low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions like <100> silicon substrate orientation can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.

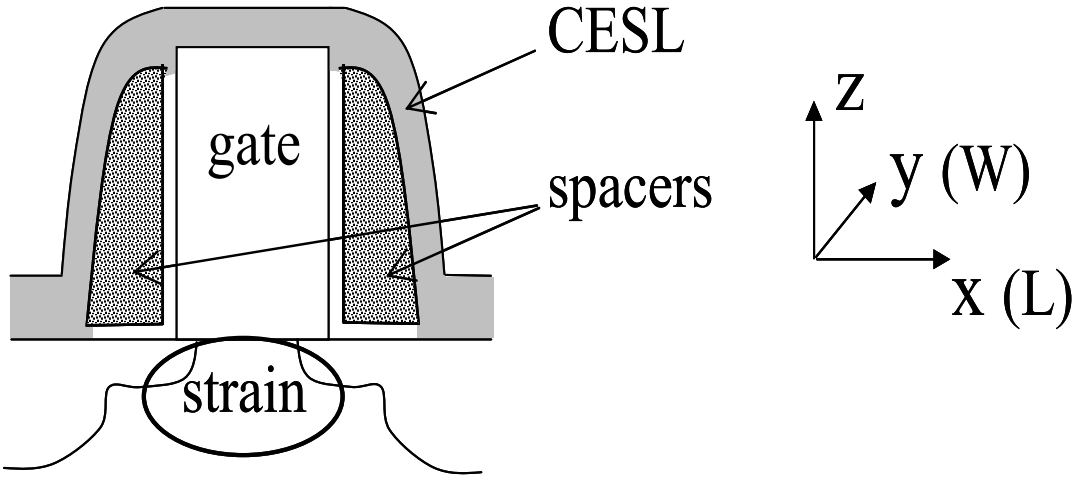

Figure 2. Schematic view of a transistor. The CESL consist of a nitride layer deposited above the transistor for contacts etch integration purpose. This liner may generate lattice strain in ***x*** (length), ***y*** (width) and ***z*** (height or out of plane) direction within the silicon channel. This phenomenon induces some modifications of the electronic band structure and carrier mobility enhancement.

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Table I. Effect of Si channel strain on electron and hole mobility, <110> (100) channel, from (3-4). * The number of (+) indicates the intensity of mobility enhancement for the strain variation mentioned above (tensile or compressive).

	Direction	nMOS	pMOS
x	Longitudinal	More tensile +++ *	More Compressive ++++
y	Transverse	More tensile ++	More tensile +++
z	Out-of-plane	More Compressive ++++	More tensile +

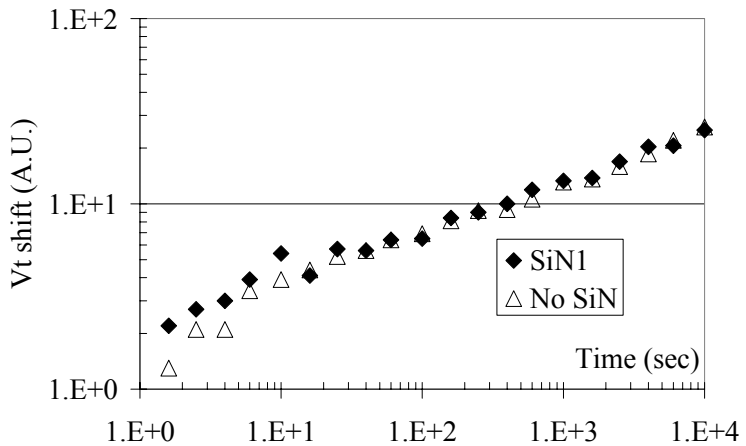

Figure 3. Vt shift as a function of time with reference nitride SiN1 and without any nitride. Essentially no difference: Both cases (no SIN and SiN1) present a 16.5 mV Vt shift (Vg = -3.6 V, T = 125 °C).

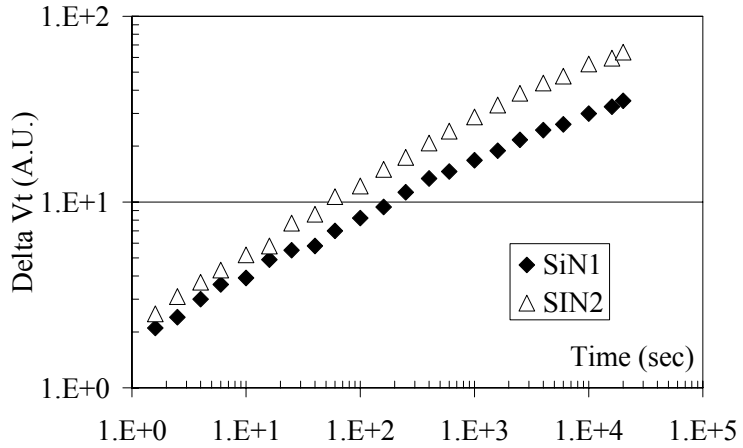

Figure 4. Comparison of Vt shift for reference nitride SiN1 and another nitride (SiN2) not optimized for NBTI (Vg = -3.6 V, T = 125 °C).

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The re-engineering of this nitride layer needs to cover all electrical aspects including reliability characteristics, and in particular the NBTI. As an example, an "optimized" CESL nitride "SiN1" doesn't bring any threshold voltage shift (Figure 3) as compared to a device without nitride CESL. On the opposite, another nitride "SIN2", not optimized, degrades the NBTI (Figure 4). The reasons for the NBTI degradation induced by CESL are still under discussion. Some works consider nitride mechanical stress as a source of NBTI degradation, through a modification of the Si-H dissociation energy, while others conclude that hydrogen content of SiN film is a key factor for interface states depassivation (5-8).

This study aims to bring new arguments to the discussion and to determine the relevant nitride properties that influence the NBTI by means of the Design of Experiment (DOE) methodology as presented in Figure 5. Thus, the experiment aimed first to provide a model that relates the process parameters with the electrical, reliability and material responses. In a second time, an attempt to determine correlations between the material properties (more universal than process parameters) and the electrical and reliability results will be carried out, thanks to a multivariate analysis.

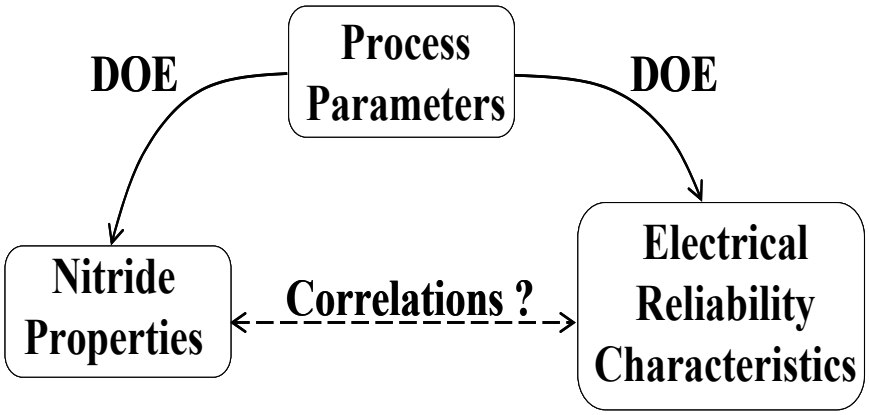

Figure 5. First, nitride properties and electrical responses are modeled as a function of process parameters. Then, Vt shift is correlated to nitride properties.

Experimental

Process description

Experiments were conducted on a conventional stabilized CMOS 90 nm Low Power bulk process (GO1: Lg = 85 nm, EOT = 21 Å, VDD = 1.2 V). A <110> (100) P doped silicon substrate was used for these devices, which allows significant impact of the strain induced in the channel on both electron and hole mobilities. To improve the film morphology and the stressor efficiency (9), nitride films have been deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) using a mix plasma frequency system. Plasma low frequency power (LFP), pressure (P), SiH4 and NH3 flows and layer thickness (Thick.) have been chosen as DOE process parameters (see Table II). Since the films will be used as stressors for the nMOS FET, the experimental plan is centered as to obtain preferentially tensile nitrides.

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Table II. PECVD process parameter used as experiment factors within the response surface DOE using a d-optimal matrix. 3 or 2 level per factors (-1, 0 and 1) have been used which allow a quadratic model for the responses.

	LFP	Pressure	SiH_4	NH_3	Thick.
	(Watt)	(Torr)	(sccm)	(sccm)	(Å)
1	30	5	360	3600	600
0	22.5	3.75	220	2400	-
-1	15	2.5	80	1200	300

Electrical characterization

Standard electrical responses linked to device performance as Ion/Ioff gain have been measured on GO1 transistors (EOT = 22 Å) with 17 points per wafer. For each wafers, saturation current Ion and off state current Ioff were measured for transistors with different L, at W = 1µm. The Ion gain at Ioff =10^{-8} A/µm was estimated by comparison to a stress-less reference. The NBTI characterizations have been carried out on pMOS GO2 devices (EOT = 50 Å), more sensitive to threshold voltage variation and often used for applications highly sensitive to threshold variation. To this purpose, a DC stress voltage of -3.6 V was applied during 3000 sec on transistors heated at 125 °C. During the voltage stress, the threshold voltage shift (Vt shift) was monitored at logarithmic stress time interval with a 60 sec unstressed waiting time following the methodology as schematized on Figure 6 and 7(a). The recovery phase after voltage stress allows addressing specifically the Si-H depassivation and the interface state evolution (10-11) by reducing the effect of hole trapping which is not our concern in this paper. A typical Vt shift evolution along the stress time is plotted in Figure 7(b) and presents linear behavior on a log/log scale. All these films have been compared to the electrical properties obtained on similar devices with reference nitride SiN1.

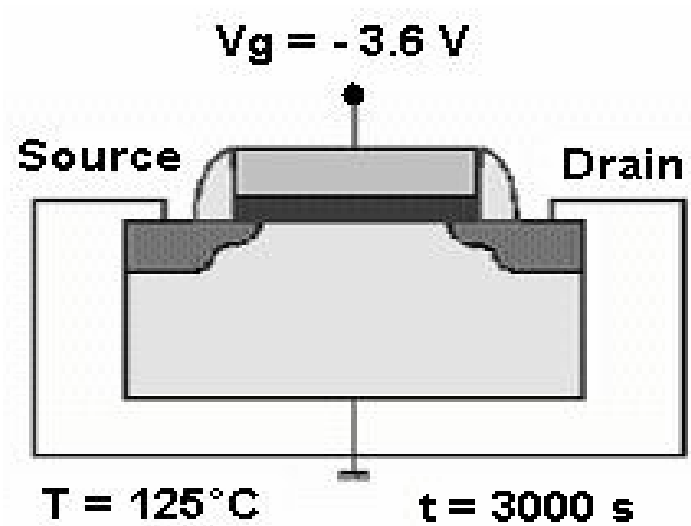

Figure 6. Negative Bias Temperature voltage stress conditions (W/L = 10*0.38 μm^2).

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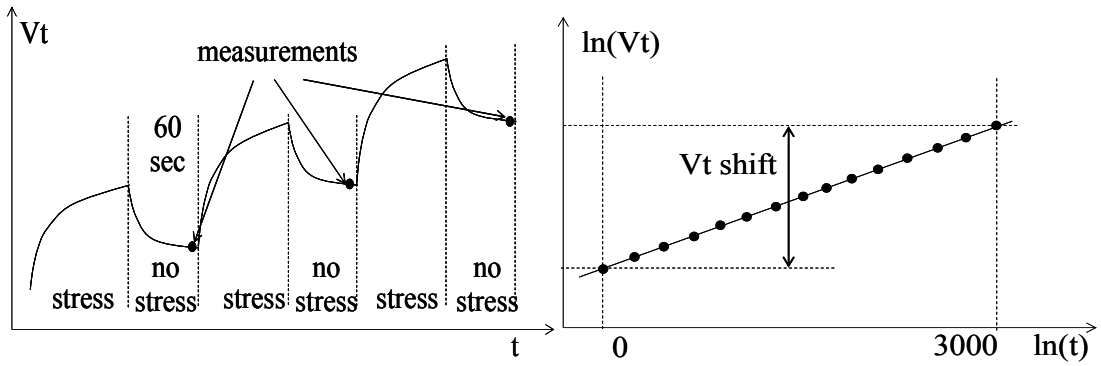

(a) (b)

Figure 7. (a) Vt shift is measured after 60 sec of stress relaxation, after stabilization and partial recovery (8). As a consequence, Vt shift is only due to Si-H depassivation. (b) Definition of the Vt shift measurement (difference between initial Vt voltage and that measured after 3000 sec voltage stress).

Material characterization

In parallel, similar layers have been deposited on blanket wafers for material characterization. Films thicknesses (***Thick***) and Refractive Index ***RI*** were measured by spectroscopic ellipsometry. The mechanical stress (σ) was obtained by the curvature method on thick nitride film samples (around 2000 Å), using the Stoney formula,

$$\sigma = \frac{E_{Si}}{6\left(1-\upsilon_{Si}\right)} \frac{t_{Si}^2}{Thick} \left(\frac{1}{R_2} - \frac{1}{R_1} \right) \qquad [1]$$

where E_{Si}, υ_{Si} and t_{Si} are the Young modulus, the Poisson coefficient and the thickness of the Silicon substrate respectively. R_1 and R_2 are the radii of curvature before and after the layer deposition and ***e*** is the film thickness. Hydrogen content (both Si-H and N-H bond concentration) was determined by Fourier Transform Infra Red spectroscopy using the methodology developed by Landford and Rand (12). In addition, the film densities were evaluated by X Ray Refraction (XRR).

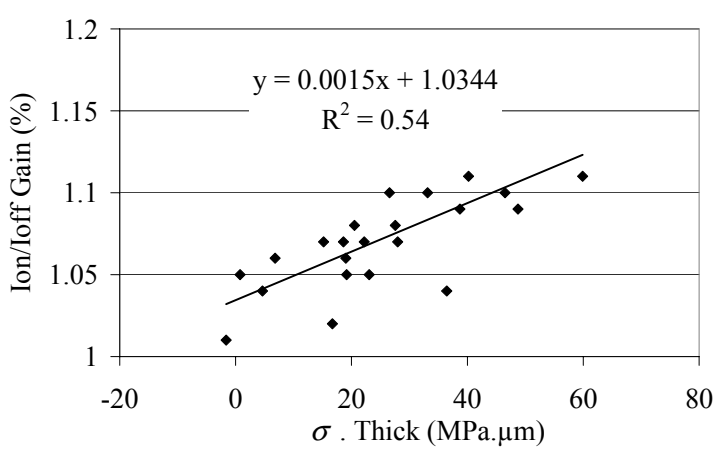

Figure 8. Impact of the nitride mechanical stress σ by the film thickness on nMOS performance gain (GO1). Transistor performance is improved when increase the stress or the thickness.

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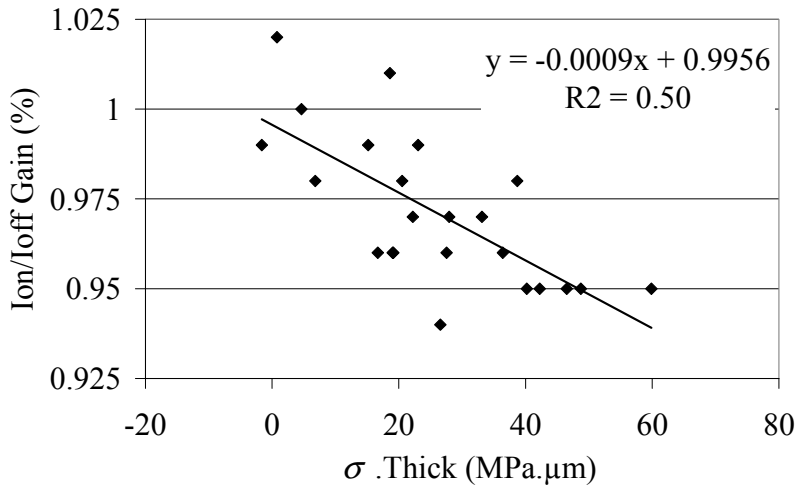

Figure 9. Impact of the nitride mechanical stress σ by the film thickness on pMOS performance gain (GO1). Transistor performance is improved when decreasing the stress or the thickness.

Results

Electrical results

As plotted before, transistor performances are improved (nMOS, Figure 8) or degraded (pMOS, Figure 9) by higher tensile stress and thicker layers, similarly to the literature (1-3). On the contrary, applying a compressive nitride film will enhance the pMOS saturation current while deteriorating the electron mobility.

DOE analyses

A standard statistical analysis has been performed to relate the DOE responses to the process parameters (LFP, P, SiH4, NH3, thick). The experimental plan is a response surface design so the experimental matrix allows modeling each response to the process parameters with a quadratic polynomial model. The distance between the experimental data and the model is expressed by the R^2 while a variance analysis provides the statistical significance of the analysis and the more influent parameters. Results are typically presented in main effect plots which summarize the sign and the magnitude of the dependence of a particular response to the process parameters. Note that since the material properties have been measured on thick films, these responses are of course not dependent of the DOE parameter "Thick", contrary to responses measured on electrical lots.

Following the explained procedure, main effect plots of nitride density, RI, Hydrogen and mechanical stress are plotted in Figure 10. R^2 values are close to 1, showing a performing statistical model of these properties.

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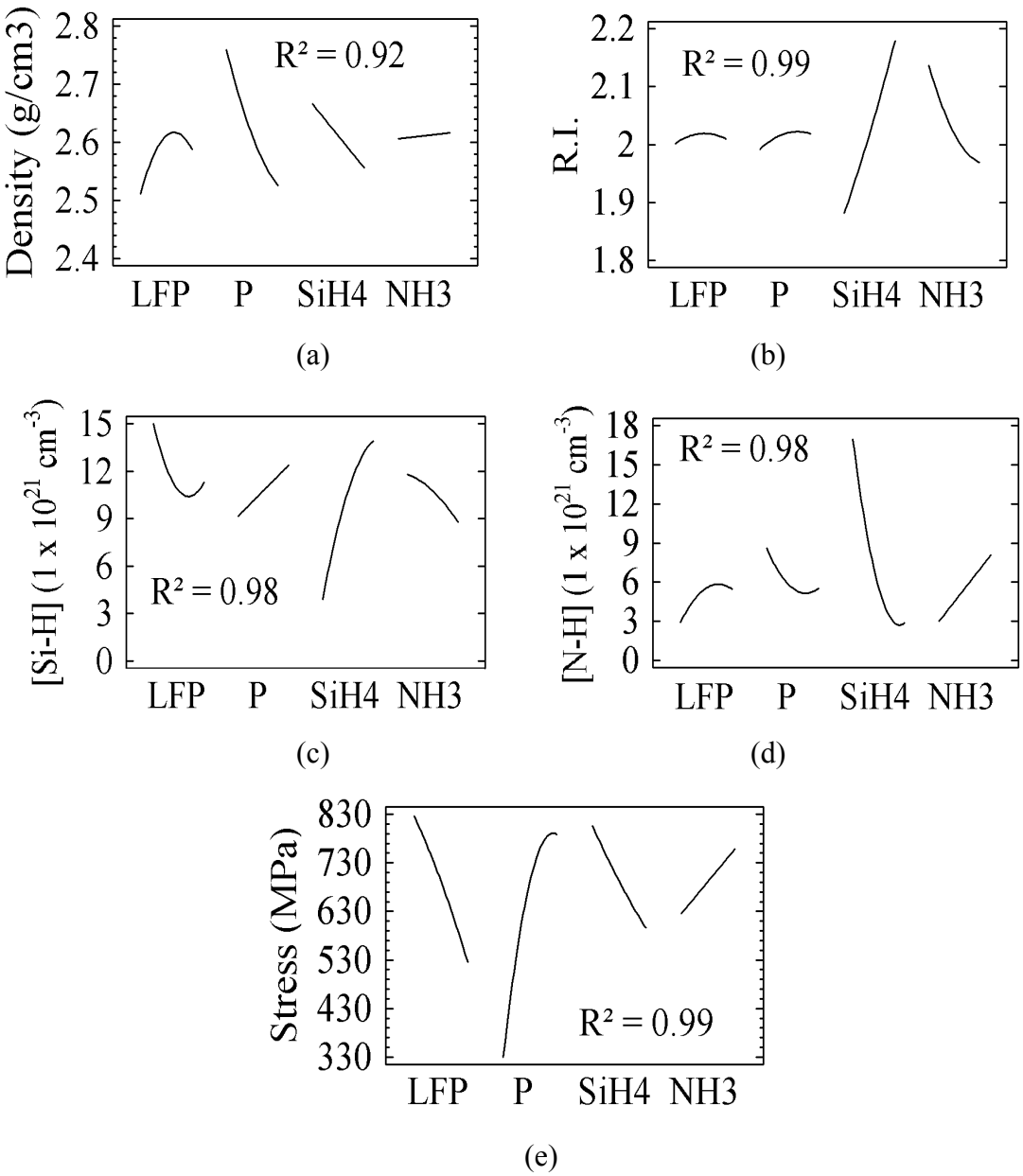

Figure 10. (a) Film density main effect plot. Influent process parameters are LFP and P. (b) Nitride RI main effect plot. Influent process parameters are SiH4 and NH3 flows. (c) (d) Hydrogen content and (e) Nitride mechanical stress main effect plot. Influent process parameters are LFP and P.

One can observe for example that the film density is increasing with a Low Plasma Power (LFP) increase while it decreases when the pressure (P) is increased. Inversely, the mechanical stress becomes more tensile when P is increased and the LFP is decreased. This is in agreement with the common observations since these two material properties are modulated by ion bombardment that occurs during deposition. A higher ion bombardment during deposition (high LFP, low P) will generates a denser and more compressive film.

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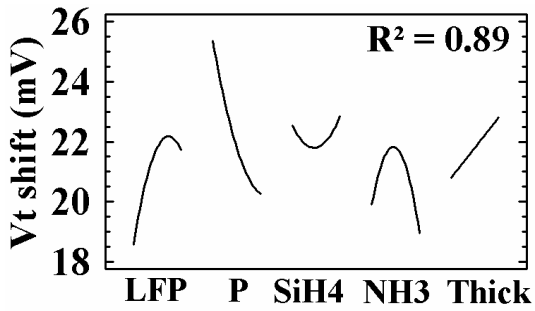

Figure11. Vt shift main effect plot. Influent process parameters are LFP and P, $(NH3)^2$ and film thickness.

The Vt shift effect plot is shown in Figure 11. The lowest values are similar to that obtained with the reference nitride SiN1 (16.5 mV), which means no impact on NBTI. A $R^2 = 0.89$, validates the dependence between NBTI and process parameters, P, LFP and thickness being the significant parameters. Note that a larger thickness tends to increase the NBTI.

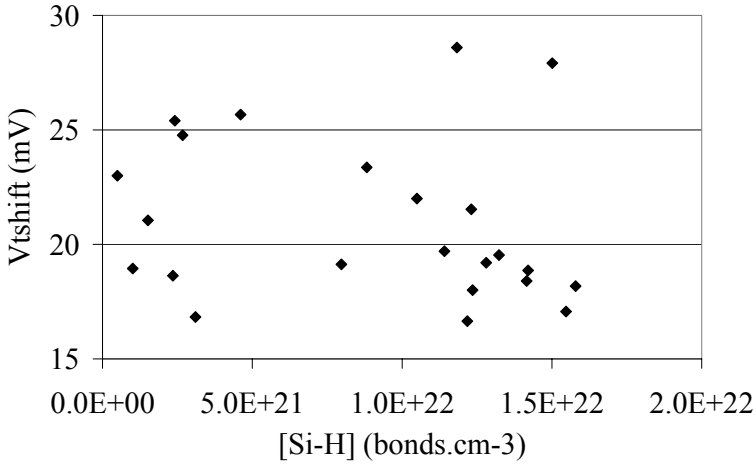

Figure12. Vt shift versus nitride Si-H bond concentration. No correlation.

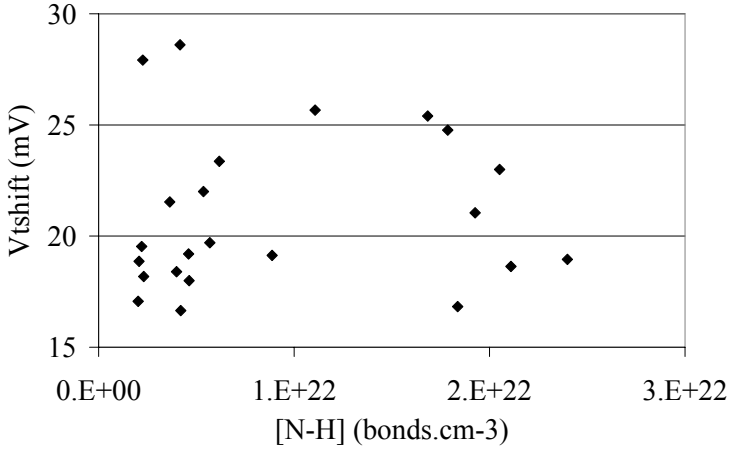

Figure13. Vt shift versus nitride N-H bond concentration. No correlation.

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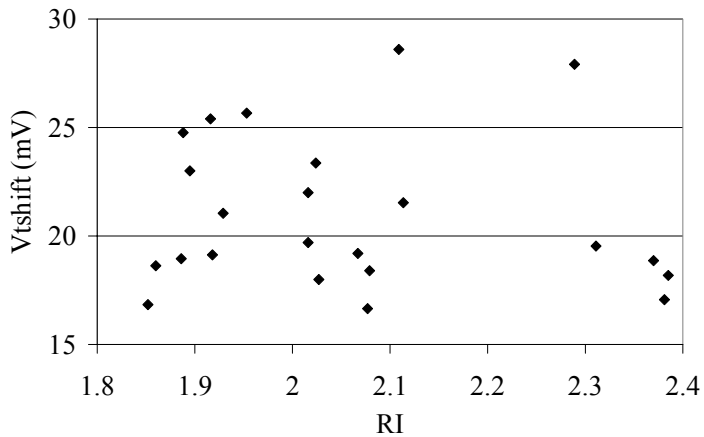

Figure14. Vt shift versus nitride film RI. No correlation.

As proposed in Figure 5, correlation analyses are then carried out to relate the NBTI parameter Vt shift to the different material properties measured on the full sheet monitors. Several correlation studies are presented in Figures 12-14 and prove that there is no correlation between Vt shift and neither RI and nitride Si-H and N-H bonds concentration while these properties span on a large experimental domain.

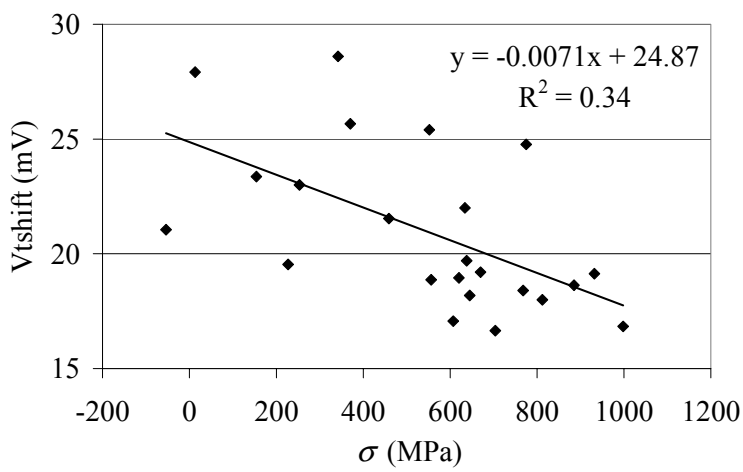

Figure 15. Vt shift versus nitride film mechanical stress.

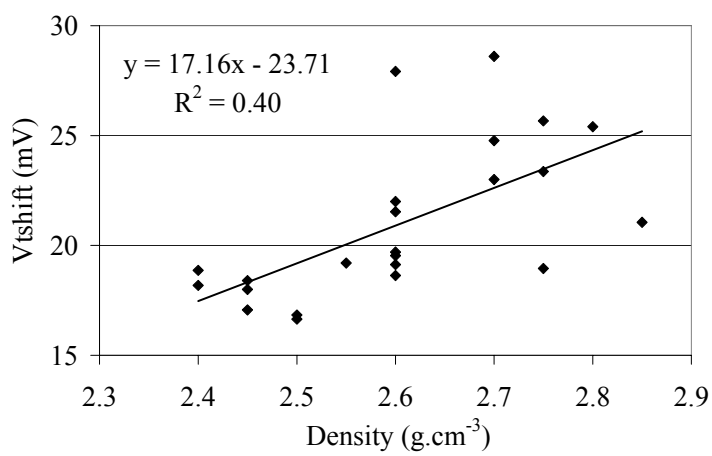

Figure 16. Vt shift versus nitride film density are positively correlated.

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On the contrary, as visible in Figure 15, NBTI decreases when CESL is becoming more tensile. Inversely, transistors with high density nitride liners present higher Vt shift (Figure 16). These two correlations are due to the fact that film density and mechanical stress are inversely modulated by bombardment during growth. In the following section, we will try to discriminate between these 2 properties the relevant one responsible for the Vt shift.

Analyses and discussion

Influence of the thickness and the stress

CESL mechanical stress has been proposed to be responsible for a part of the NBTI increase in (7). In this paper, it is postulated that the higher the nitride stress, the higher the Vt shift, contrary to the trend observed in Figure 15. Data from this Figure are presented again in Figure 17, with a differentiation of the two experimental liner thicknesses, 300 or 600 Å. As seen in this Figure, Vt shift decreases with an increase of the tensile stress.

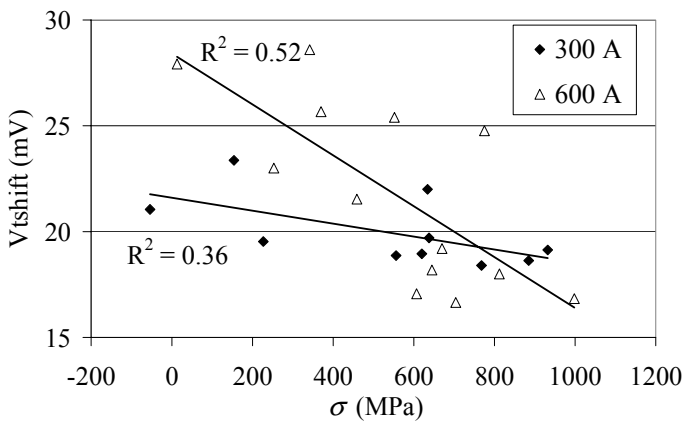

Figure 17. Vt shift versus nitride mechanical stress and film thickness. NBTI is inversely correlated with stress but increases with a larger thickness. This proves that the nitride mechanical stress is not the root cause of the NBTI degradation because a larger thickness should have increased the positive nitride stress effect.

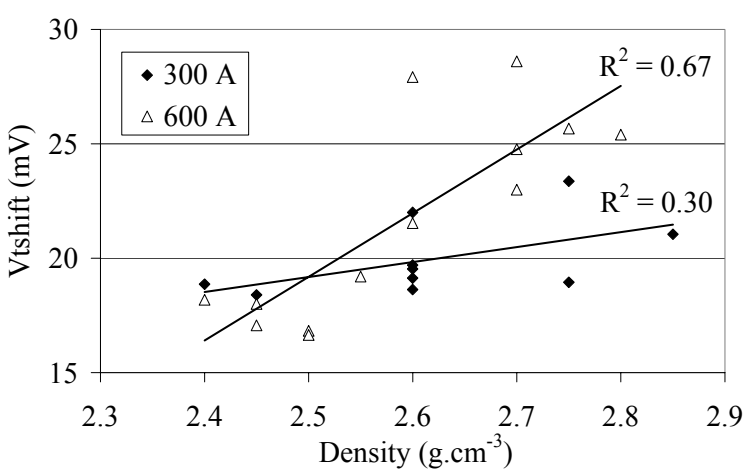

Figure 18. Vt shift versus nitride density and film thickness. Higher shift is observed with denser and thicker nitride layers.

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On the other hand, Vt shift increases with larger thickness. Both observations are in contradiction since the stress at the level of the gate oxide is dependent on both the stress level and the film thickness. This proves that nitride mechanical stress is not the main cause of the NBTI degradation. On the contrary, a larger density is correlated with a deterioration of the NBTI, similarly to a larger thickness (Figure 18).

The influence of the nitride density can be related to the hydrogen concentration at the surface of the gate oxide. Sensitivity of hydrogen diffusivity in nitride films has already been studied by some of the authors in (13). In this paper, samples of different types of silicon nitride deposited on silicon oxide films have been submitted to a final D_2 (hydrogen isotope) annealing at 400 °C followed by SIMS analyses. The deuterium profiles obtained on some of these nitride oxide stacks after D_2 annealing, for different nitride density, are presented in Figure 19. It is visible in this figure that the deuterium (hydrogen isotope) diffusivity within nitride is strongly dependent on CESL material property. The larger the nitride film density, the lower the deuterium diffusivity is.

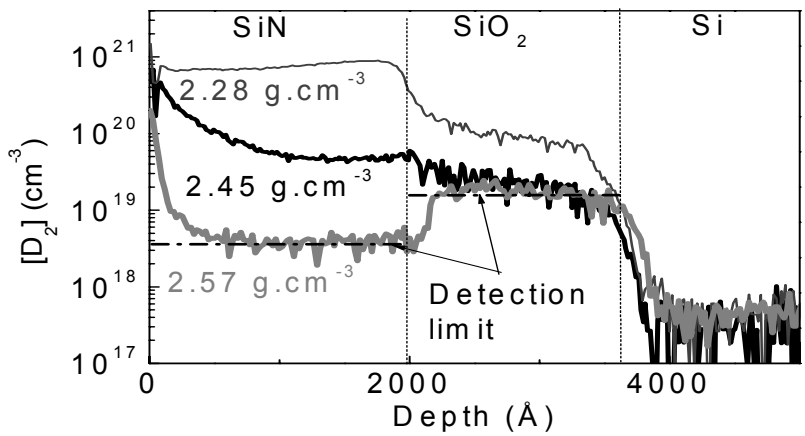

Figure 19. Deuterium concentrations in Si/SiO2/SiN stacks after D_2 anneal 400 °C / 60 min for different SiN film density. In case of a dense nitride, deuterium concentration is minimized within nitride and oxide, revealing a lower diffusivity within the nitride layer.

These observations indicate that the nitride (by it's density and thickness) can acts as a hydrogen barrier, with a detrimental impact on the NBTI by following the mechanisms proposed in Figure 20a and b. Before any further discussion, it is important to recall that the transient recovery of the threshold voltage is not considered in this study, since the measurement is carried out after 60 sec of stress relaxation, after stabilization and partial recovery. As mentioned in (14-15) the depassivation of Si-H bond enhanced by the presence of hydrogen H^+ is the most plausible reaction to generate a silicon dangling bond. In case of a high density nitride, hydrogen out diffusion in the gate region is blocked; which can enhance the Si-H interface depassivation and a significant Vt shift. On the contrary, hydrogen diffusion is not limited in case of a porous (low density) nitride contact etch stop layer which allow for limited hydrogen concentration within the gate and less depassivation. No additional Si-H depassivation induced by CESL during the NBT stress occurs. As explained by Tsetseris & al. (15), when considering quasi static conditions, as in our case, the trap generation is limited by the hydrogen diffusion. These conclusions are in agreement with Morifuji & al. in (16): the CESL nitride must be "transparent" to H diffusion.

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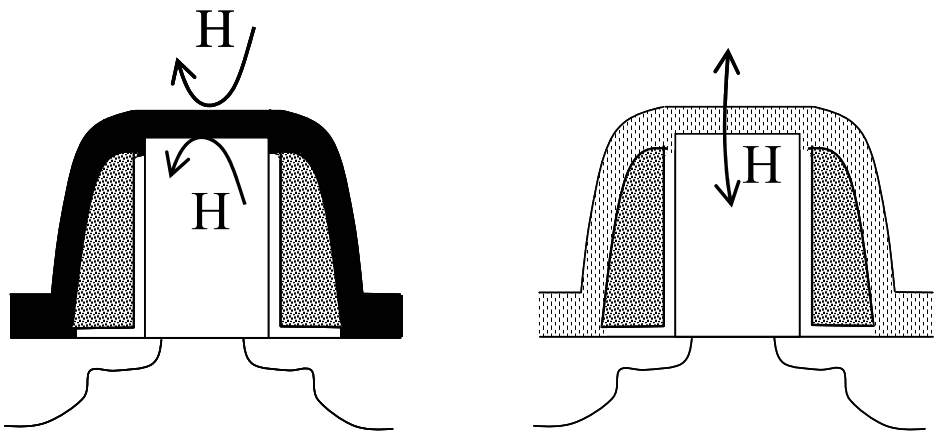

(a) (b)

Figure 20. (a) Hydrogen diffusion is blocked in case of a thick dense nitride contact etch stop layer. Si-H depassivation is enhanced by the CESL capping. (b) Hydrogen diffusion is not blocked in case of a porous nitride contact etch stop layer. No additional Si-H depassivation induced by CESL.

The positive correlation observed between the Vt shift and nitride stress in Figure 17 can be finally explained as follow: densities of tensile stress films are reduced because of less plasma bombardment during deposition, which enhance the hydrogen diffusivity within the film and as a consequence a decrease of NBTI.

Conclusion

The impact of the CESL nitride properties on the threshold voltage measured during negative bias voltage stress has been studied. NBTI measurement procedure is fixed to characterize the gate oxide interface state related to the Si-H bond concentration while excluding the transient oxide charging phenomenon.

This study shows that the NBTI requires an optimization of the nitride CESL properties. Thanks to a Design Of Experiment methodology, it has been statistically and physically demonstrated that nitride density, thus hydrogen diffusion, is the major nitride property responsible for NBTI induced by CESL. On the contrary, it has been proved that neither the nitride stress, nor hydrogen content or refractive index is responsible for the NBTI.

The nitride density in link with hydrogen diffusivity must be considered for further film developments, as in the case of highly tensile nitride used as CESL in 45 nm technologies. While nMOS performances are significantly improved, pMOS NBTI can be drastically deteriorated in case of no specific nitride adaptation. In addition, the lessons of this study can be applied for the development of compressive thick nitrides used in the Dual Stress Liner integration (17). This technique consists in the co-integration of a tensile CESL above the nMOS device and of a compressive liner above the pMOS transistors. In fact, these compressive films presents generally high weight density due to the level of ion bombardment required to achieve ultra compressive stress values. They may act as a blocker for hydrogen diffusion within the transistors.

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Acknowledgments

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