Single Stress Liner for Both NMOS and PMOS Current Enhancement by a Novel Ultimate Spacer Process

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Abstract

For the first time, ***15% and 7%*** drive current improvement is ***simultaneously*** achieved in ***both N/PMOS*** by adopting ***ultimate spacer process (USP)*** with a single stress liner. High out-of-plane stress in the channel accounts for the simultaneously enhanced drive current in N/PMOS. A 15% speed enhancement without compromising yield and product qualification in Field-Programmable Gate Arrays (FPGA) confirms immediate manufacturing feasibility of USP. This process provides a unique approach to significantly enhance device performance for 65nm CMOS technology and beyond. Extreme current increase of 25% in NMOS and 35% in PMOS can be achieved by applying additional strain enhancement methods.

Introduction

Utilizing strain in the channel region to improve electron and hole mobility has been reported for maintaining the device scaling roadmap [1,2]. Local strain techniques such as dual stress liner process have been reported to enhance CMOS performance [3]. Process induced strain methods have also been studied widely in the industry as an alternative approach to enhance device performance [4]. However, complicated process steps are required to simultaneously enhance drive currents of both N/PMOS.

In this paper, drive currents of NMOS and PMOS are simultaneously increased by only inserting USP into the standard CMOS process. The device with USP shows higher drive current enhancement compared to the devices with tensile contact etching stop layer (CESL), due to the extreme channel stress obtained. Additional approaches are also implemented to achieve higher mobility enhancement. Moreover, USP is verified through wafer and product level reliability qualification for its high-volume fabrication feasibility.

Device Preparation

High performance CMOS devices using ultimate spacer process (USP) were fabricated with a 35nm gate length as shown in **Fig. 1**. After gate patterning, the transistors were integrated with shallow extensions and pocket implants, followed by rapid thermal annealing. Details of the CMOS process flow with USP are shown in **Fig. 2**. Only one ultimate spacer process step was inserted into the salicide module for both N/PMOS without any extra lithography steps. In addition, the oriented channel and poly stressor were applied to further enhance the drive current.

Device Performance

Based on the previous work, drive current of NMOS is enhanced by using tensile CESL for inducing higher channel stress. However, this channel stress will be reduced by the nitride spacer. Therefore, channel stress as a function of nitride spacer width is simulated and shown in **Fig.3**. It is found that an extreme channel stress, including longitudinal stress ($Stress_{xx}$, S_{xx}) and out-of-plane stress ($Stress_{yy}$, S_{yy}), is obtained by narrowing the nitride spacer width. As a result, the device with ultimate spacer process is fabricated without the nitride spacer to achieve the highest channel stress. The summary of current gain for devices with USP is listed in **Table I**. The universal curves for NMOS and PMOS are also shown in **Fig.4** and **Fig.5**, respectively. Drive currents of NMOS and PMOS with USP are enhanced by 15 % and 7 % compared to the control device, respectively. A simultaneous drive current gain is obviously obtained in N/PMOS with this USP.

Table I Device performance summary of USP and tensile CESL.

Scheme		USP*	Tensile CESL
Additional Process		Inserted One Step	-
Capping Layer		Stress : +1GPa Thickness : 700 A	
Core ** (current gain)	NMOS	15%	5%
	PMOS	7%	0
IO ** (current gain)	NMOS	7%	0
	PMOS	0	0
* Simultaneous current gain of N/PMOS ** Compared with Control sample			

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The drive current gain of device with tensile CESL is also shown in **Table I** for comparison. Although the same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both USP and tensile-CESL process, the drive current enhancement of USP is still higher by more than 7 %. This higher drive current gain is due to the higher channel stress induced by USP. The simulated S_{xx} and S_{yy} distribution in channel region are shown in **Fig. 6** and **Fig. 7**, respectively. It is found that both S_{xx} and S_{yy} can be effectively increased compared to the control and the devices with tensile CESL. The resulting simultaneous NMOS and PMOS drive current enhancement may be due to its higher out-of-plane compressive stress in the USP. The Id-Vd characteristics of NMOS and PMOS devices with ultimate spacer process compared with control samples are shown in **Fig. 8**. Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow. The Id-Vg characteristics of the NMOS and PMOS with ultimate spacer process are shown in **Fig.9**. Comparable device characteristics in sub-threshold swing (Swing) and drain induced barrier lowering (DIBL) are observed. The excellent short channel performance of this USP device is obtained.

Product Performance

The die photograph of the FPGA fabricated using ultimate spacer process is shown in **Fig. 10**. Comparable product yield was successfully achieved for control wafers and strained USP wafers. At the same leakage current, the speed of product with USP is much faster than that of control wafer. From the speed distribution plots as shown in **Fig. 11**, the USP splits show overall 15% faster product speed. Product qualification was also performed on control and USP wafers. Both of them passed product level reliability qualification specs (HTOL, TC, ESD, and Latch-up) and no difference was observed between USP and control wafers.

Combination of Additional Strained Si Scheme and Wafer Level Reliability

A 35% drive current enhancement of PMOS can be obtained by applying the ultimate spacer process with channel orientation engineering as shown in **Fig. 12**. **Fig. 13** illustrates a 25% drive current enhancement for NMOS with both the ultimate spacer process and poly stress memorized process. The ring-oscillators fabricated with USP and additional strain engineering shows about 20% time delay improvement compared to control samples as shown in **Fig. 14**. The width dependence of linear and saturation drive current enhancement is shown in **Fig. 15**. As the width of the active region scales down below 1um, maximum 60% and 35% current enhancement can be observed at linear and saturation regions, respectively.

When temperature increases from 25ºC to 125ºC, the devices with USP still maintain better performance compared to control samples as shown in **Fig. 16**. The wafer level reliability performances are shown in **Fig. 17** and **Fig. 18**. Obviously, the oxide quality and wafer level reliability for the devices with the ultimate spacer process are better than that of the control wafer. **Table II** summarizes drive current gain benchmark of the strained devices with highly tensile CESL process. Only this work presents simultaneous drive current enhancement for N/PMOS.

Conclusion

The ultimate spacer process with single stress liner has been successfully demonstrated to ***simultaneously*** enhance both N/PMOS drive currents. A 20% speed enhancement of CMOS ring oscillator with comparable wafer level reliability is also observed. The immediate manufacturing feasibility of USP has been proven by 15% speed enhancement without compromising yield and product qualification in FPGA. In addition, 25% and 35% drive current enhancements for NMOS and PMOS are achieved by combining the USP with poly stressor and channel orientation engineering, respectively. We have verified simultaneous performance enhancement in both N/PMOS with USP for 65nm CMOS technology and beyond.

References

1. K. Mistry, et al., *Symp. VLSI Tech. Dig.*, pp. 50-51, 2004.
2. R. Khamankar, et al., *Symp. VLSI Tech. Dig.*, pp. 162-163 , 2004.
3. H. S. Yang, et al, *IEDM Tech. Dig.*, pp.1075-1078, 2004.
4. K. Ota, et al., *IEDM Tech. Dig.*, pp. 27-30, 2002.
5. F. Boeuf, et al., *IEDM Tech. Dig.*, pp. 425-428, 2004.
6. K. Goto, et al., *IEDM Tech. Dig.*, pp. 209-212, 2004.
7. T. Komoda, et al., *IEDM Tech. Dig.*, pp. 217-220, 2004.
8. C.H.Chen, et al., *Symp. VLSI Tech. Dig.*, pp. 56-57, 2004.

Table II Benchmark of strain silicon devices.

		This work	Ref. [1]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]
Process		USP	CESL	CESL	CESL	CESL	CESL
Capping Layer	Stress	1GPa	>1.5 GPa	>1.5 GPa	>1.5 GPa	>1 GPa	>1.5 GPa
	Thickness	700 A	700 A	-	700 A	-	-
Current Gain	NMOS	15%*	10%	10%	12%	10%	10%
	PMOS	7%*	-2%	-10%	0%	0%	-
* Utilizing USP scheme enhances both NMOS and PMOS drive currents							

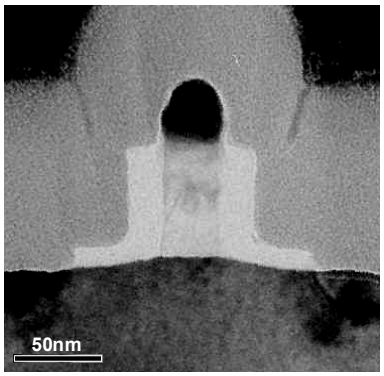

Fig. 1 TEM cross-section image illustrating 35nm NMOS strained device with ultimate spacer process (**USP**).

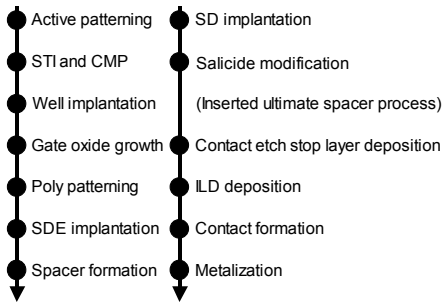

Fig. 2 Detailed strained CMOS process flow with ultimate spacer process (**USP**).

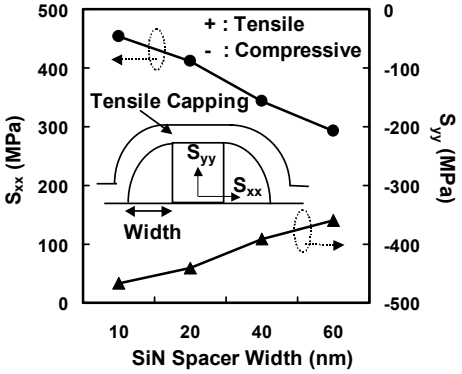

Fig. 3 2D simulation of tensile capping layer induced channel stress as a function of nitride spacer width. An extreme channel stress can be obtained by narrowing the SiN spacer width.

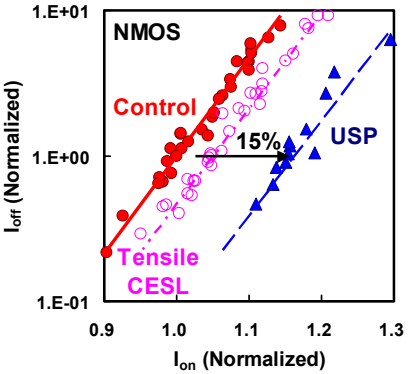

Fig. 4 Ion vs Ioff plots of NMOS. 15% drive current gain is achieved on strained devices with USP. Using this USP, higher current gain is obtained.

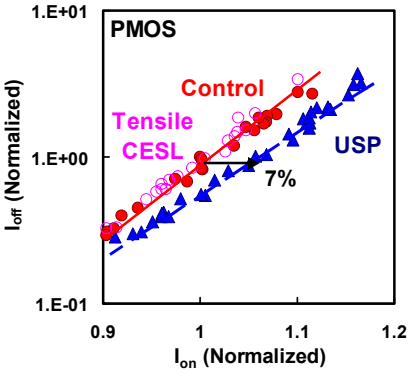

Fig. 5 Ion vs Ioff curves of PMOS. 7% drive current gain is achieved on strained devices with USP. ***Both N/PMOS can be enhanced by this single step USP.***

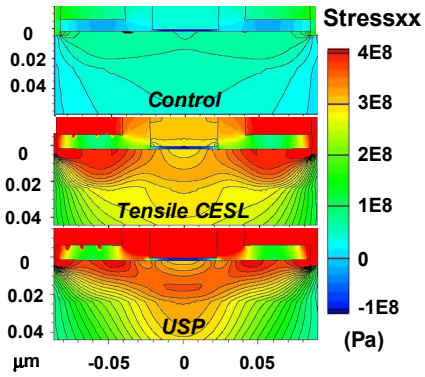

Fig. 6 2D simulated stress distribution in the channel direction for different devices. 11% channel stress increase is obtained in USP compared to tensile CESL process.

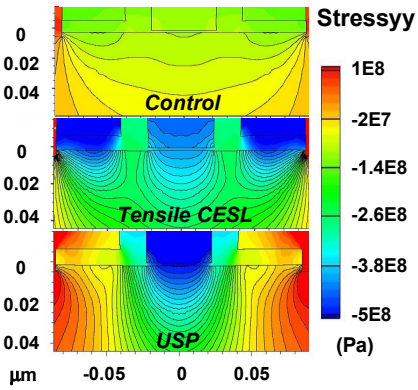

Fig. 7 2D simulated stress distribution in the out-of-plane direction for different devices. 19% channel stress increase is obtained in USP compared to tensile CESL process. The drive current enhancement of PMOS with USP is due to the larger compressive stress.

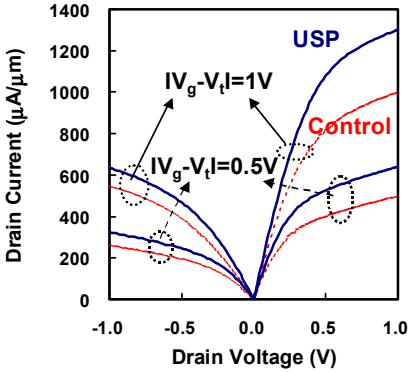

Fig. 8 Id-Vd characteristics of NMOS and PMOS devices. Significant drive current enhancement of both N/PMOS is achieved with inserting this USP in standard CMOS flow.

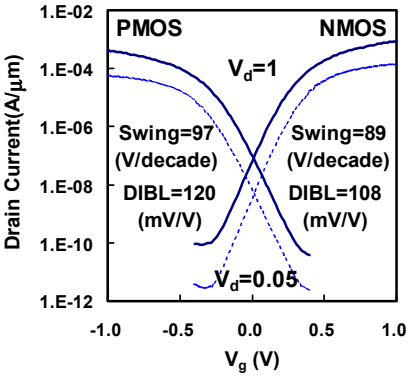

Fig. 9 Id-Vgs characteristics of strained NMOS and PMOS devices. Excellent short channel performance of this USP device is obtained.

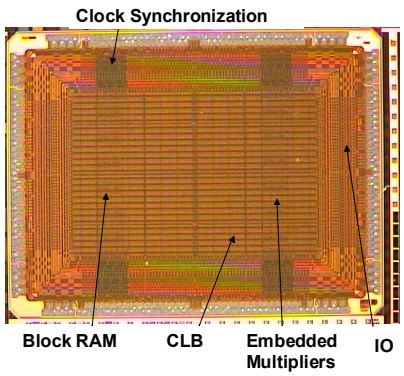

Fig. 10 Die photograph of FPGA fabricated using USP.

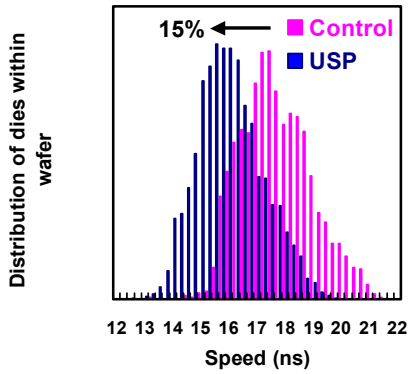

Fig. 11 The Fabricated FPGA speed distribution of control and USP samples. The USP wafer presents uniformly overall 15% faster product speed.

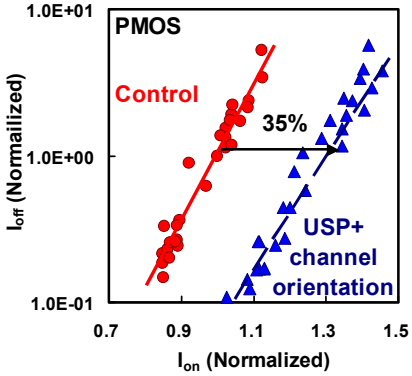

Fig. 12 Ion vs Ioff curves of PMOS. Extreme 35% current gain is obtained by using *USP* with channel orientation engineering.

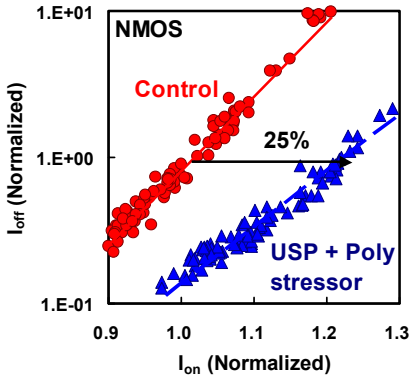

Fig. 13 Ion vs Ioff plots of NMOS. 25% current gain can be achieved on NMOS by using the USP and poly stress memorized process (*poly-stressor*).

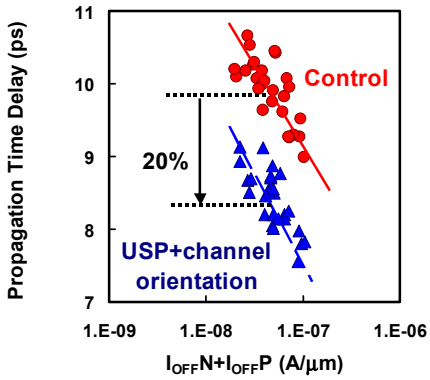

Fig. 14 Ring oscillator performance of the control and strained devices. The strained devices with USP and channel orientation engineering presents about 20% propagation time delay improvement.

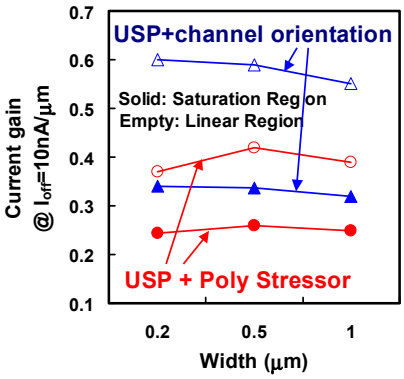

Fig. 15 The linear and saturated drive current enhancement dependence of device widths.

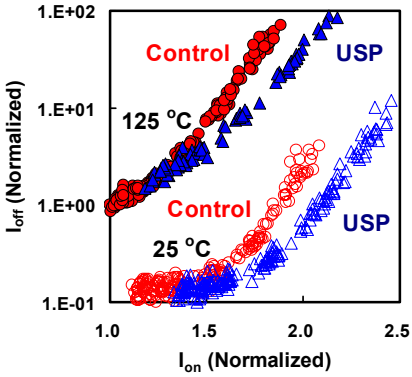

Fig. 16 Temperature effect of control and strained sample. Even at high temperature condition, devices with USP maintain better performance.

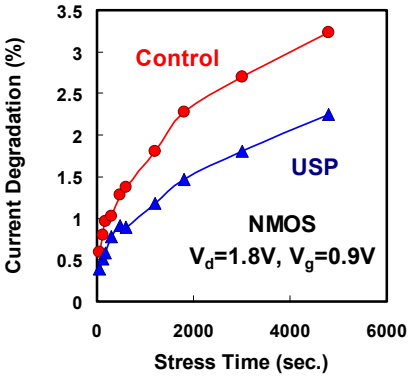

Fig. 17 Current degradation induced by hot carrier injection (HCI) on NMOS of control and strained sample. The ultimate spacer process sample reveals lower drive current degradation.

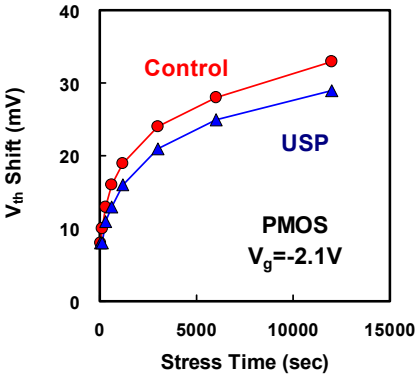

Fig. 18 The V_{th} shift induced by Negative bias temperature instability (NBTI) on PMOS of control and strained sample. The ultimate spacer process wafer presents better performance.