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(54) DUAL METAL SILICIDES FOR LOWERING CONTACT RESISTANCE

(76) Inventors: **Chung-Hu Ke**, Taipei (TW); **Chih-Hsin Ko**, Fongshan City (TW); **Hung-Wei Chen**, Hsinchu (TW); **Wen-Chin Lee**, Hsin-chu (TW)

Correspondence Address:
SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

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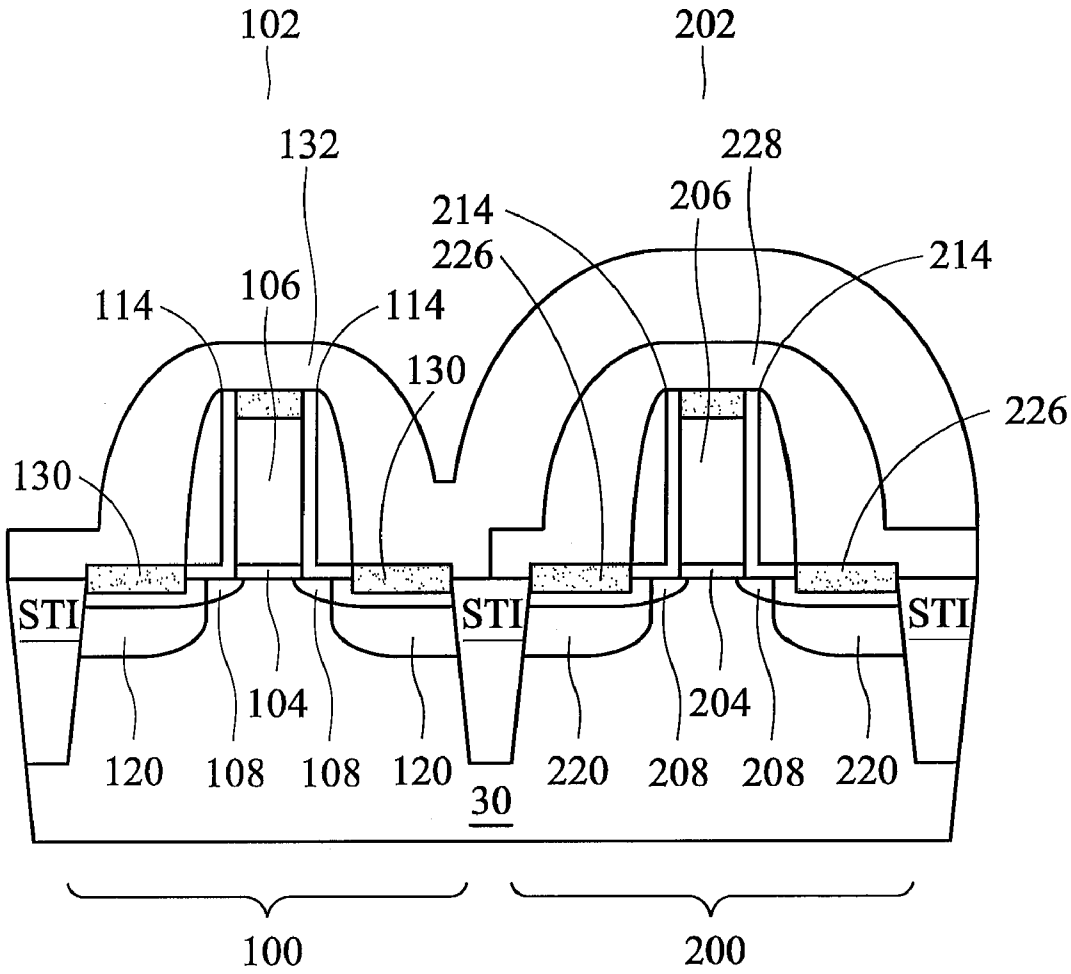
(57) **ABSTRACT**

A method for forming a semiconductor structure includes: providing a semiconductor substrate; forming an NMOS device at a surface of the semiconductor substrate, which comprises forming a first source/drain electrode on a first source/drain region of the NMOS device, wherein the first source/drain electrode has a first barrier height; forming a PMOS device at the surface of the semiconductor substrate comprising forming a second source/drain electrode on a second source/drain region of the PMOS device, wherein the second source/drain electrode has a second barrier height, and wherein the first barrier height is different from the second barrier height; forming a first stressed film having a first intrinsic stress over the NMOS device; and forming a second stressed film having a second intrinsic stress over the PMOS device, wherein the first intrinsic stress is more tensile than the second intrinsic stress.



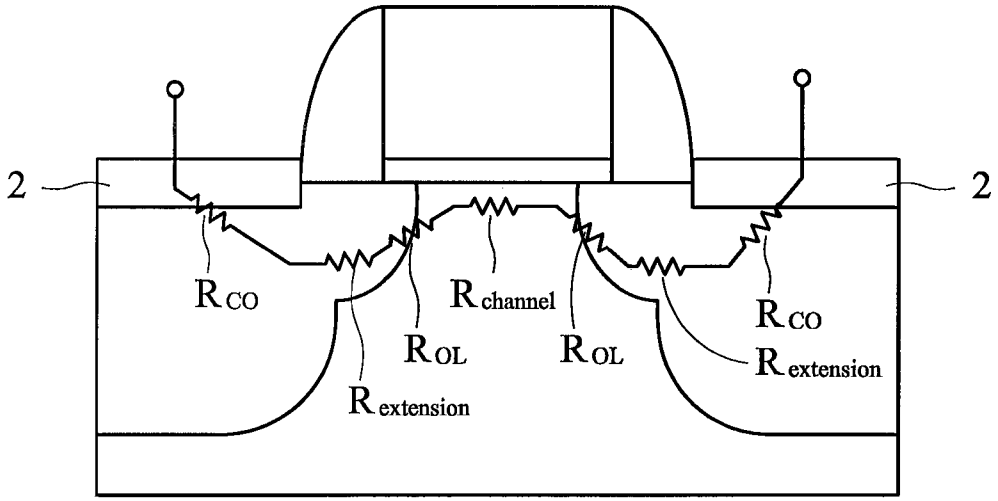

2
2
RCO
RCO
Rchannel
ROL
ROL
Rextension
Rextension

FIG. 1

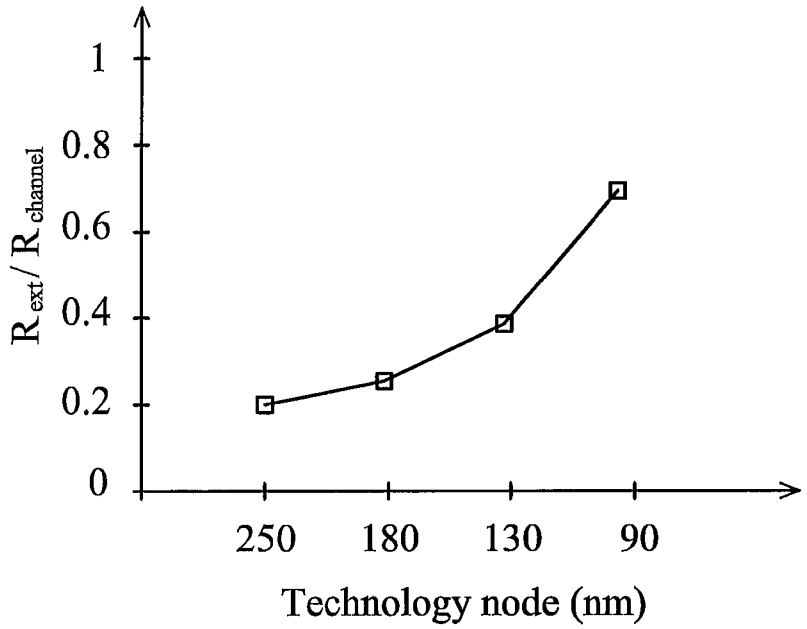

1
0.8
0.6
0.4
0.2
0
Rext / Rchannel
250
180
130
90
Technology node (nm)

FIG. 2

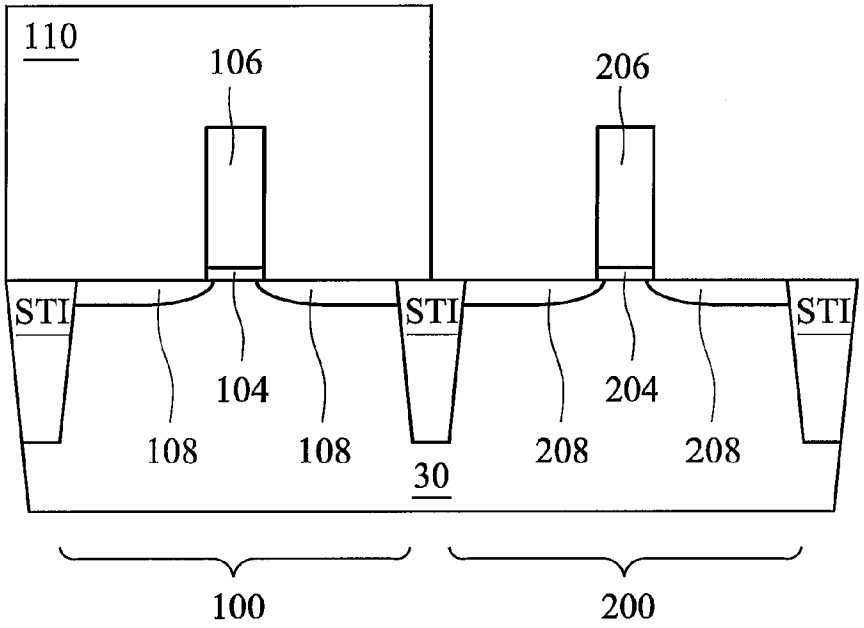

110
106
206
STI
STI
STI
104
204
108
108
208
208
30
100
200

FIG. 3

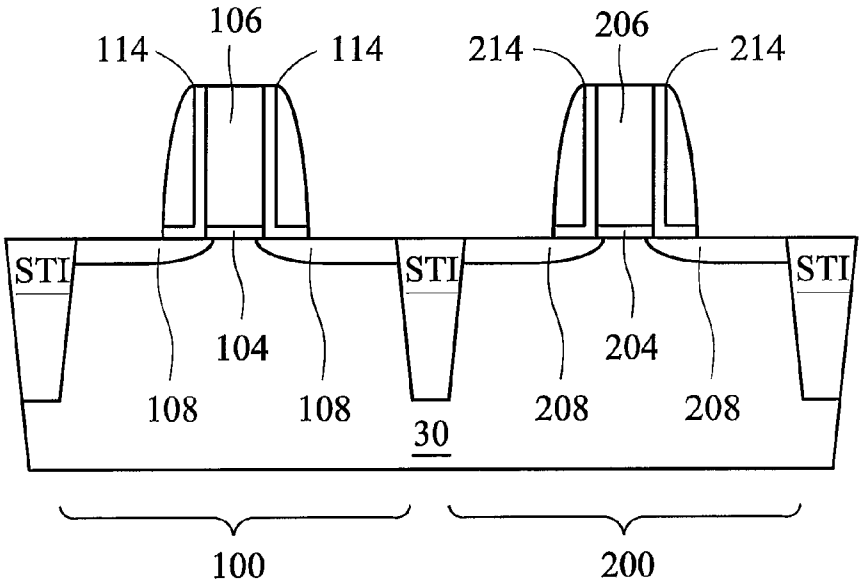
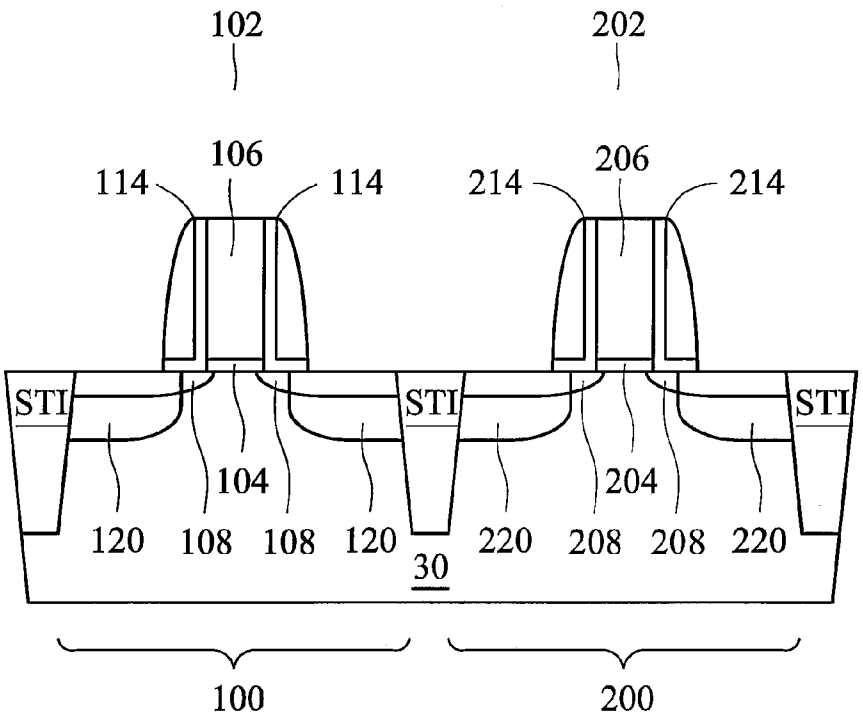

106
114
114
206
214
214
STI
STI
STI
104
204
108
108
208
208
30
100
200

FIG. 4


102
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114
206
214
214
STI
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STI
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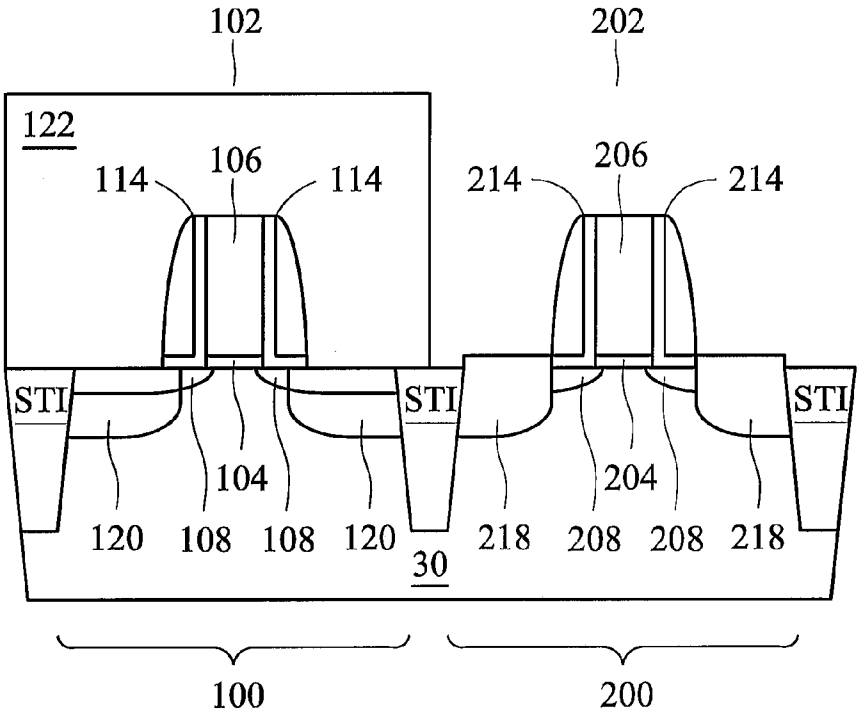
208
220
30
100
200

FIG. 5A


102
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122
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114
206
214
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STI
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218
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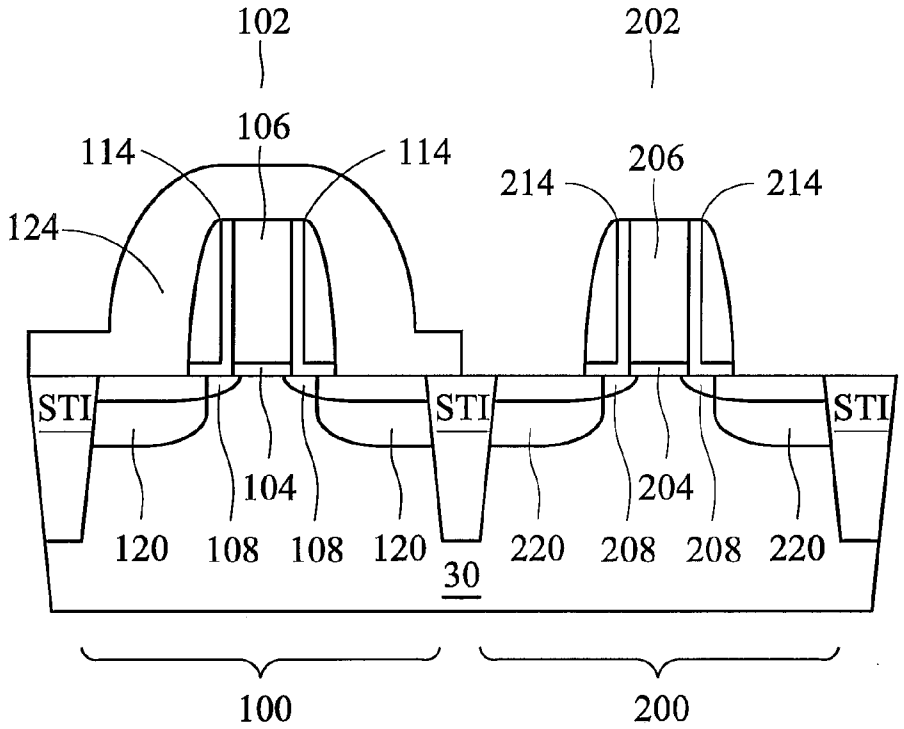
208
218
30
100
200

FIG. 5B


102
202
106
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114
206
214
214
124
STI
STI
STI
104
204
120
108
108
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220
208
208
220
30
100
200

FIG. 6

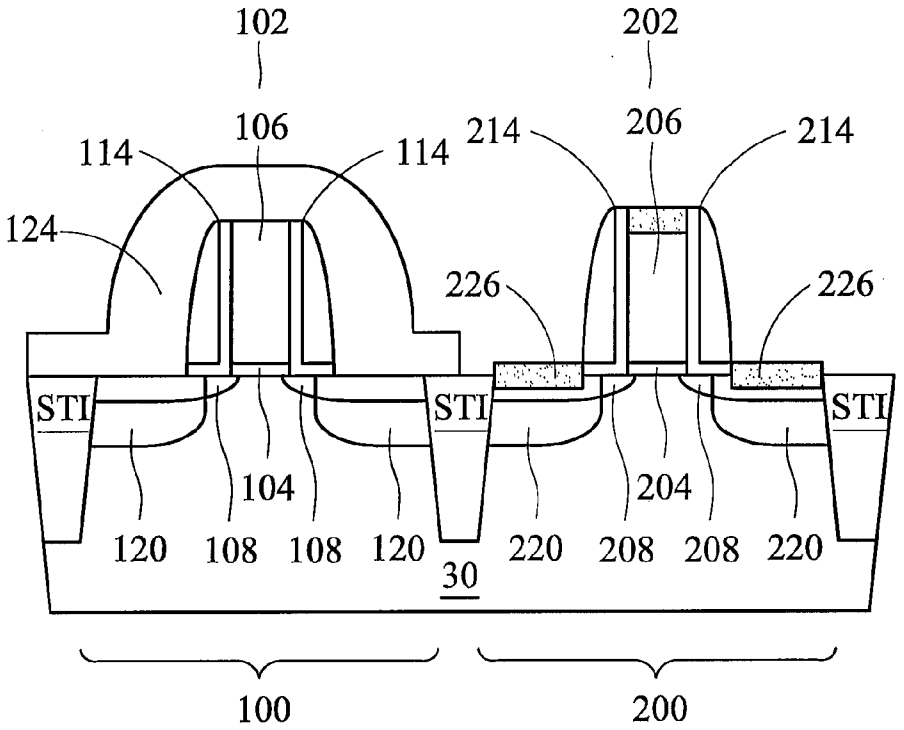
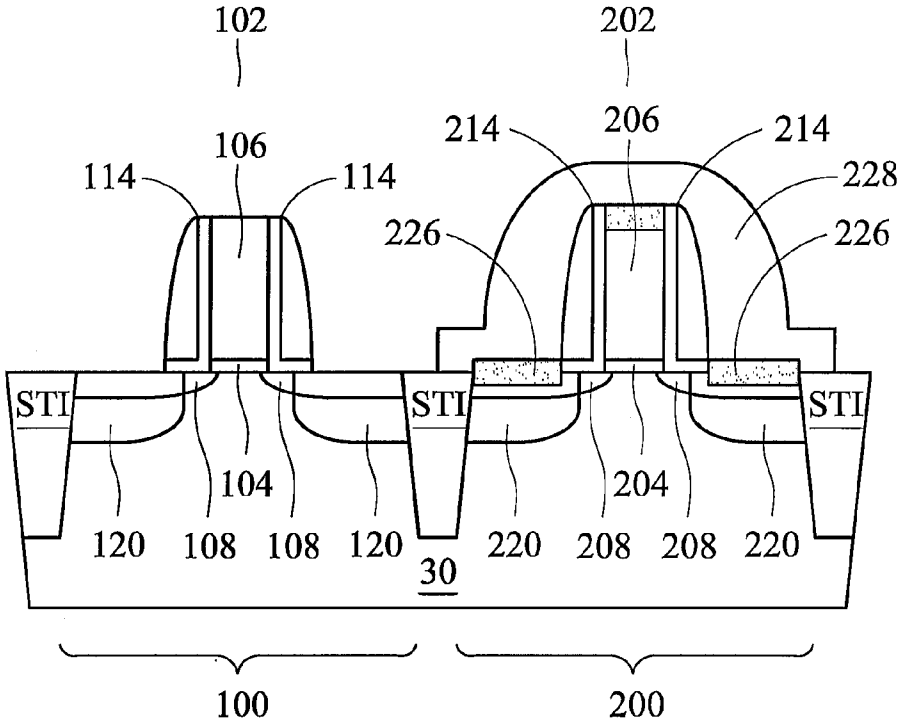

102
202
106
214
206
214
114
114
124
226
226
STI
STI
STI
104
204
120
108
108
120
220
208
208
220
30
100
200

FIG. 7


102
202
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214
214
228
226
226
STI
STI
STI
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220
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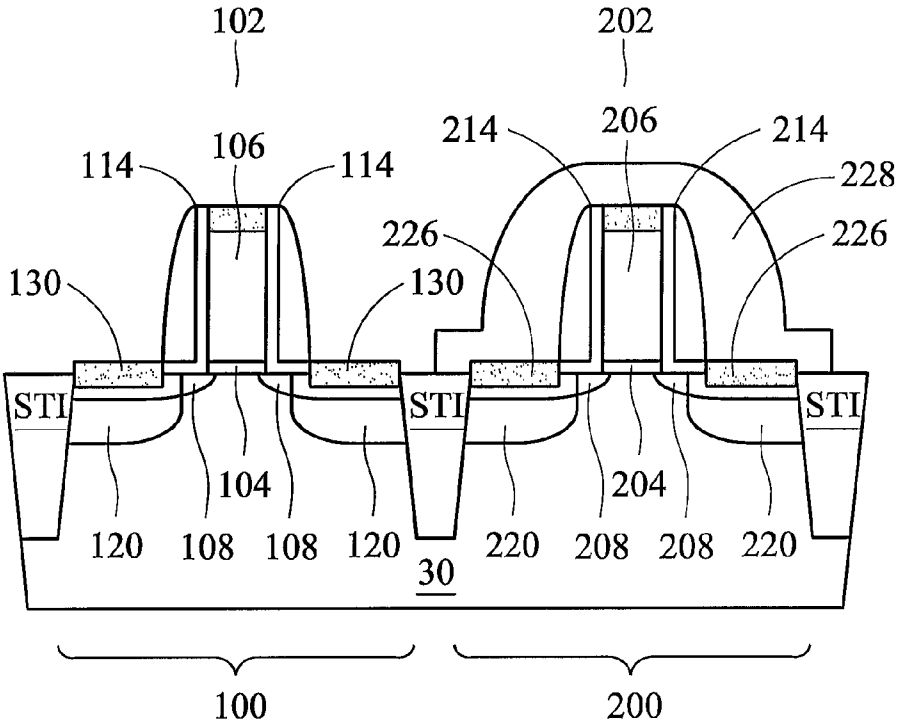
100
200

FIG. 8


102
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226
226
130
130
STI
STI
STI
104
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FIG. 9

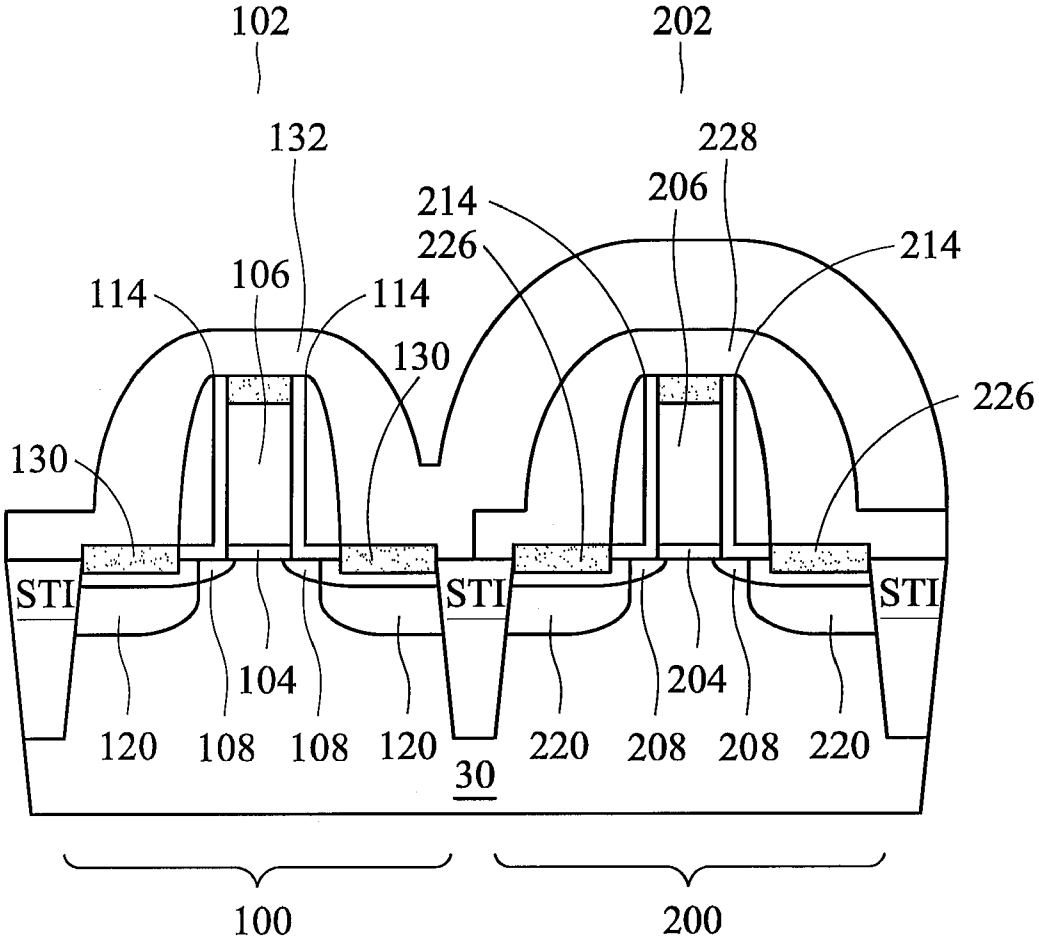
102
202
132
228
214
206
226
214
106
114
114
130
226
130
STI
STI
STI
104
204
120
108
108
120
220
208
208
220
30
100
200

FIG. 10

DUAL METAL SILICIDES FOR LOWERING CONTACT RESISTANCE

TECHNICAL FIELD

[0001] This invention relates generally to semiconductor devices, and more particularly to structures and manufacturing methods of metal-oxide-semiconductor (MOS) devices.

BACKGROUND

[0002] The scaling of VLSI circuits is a constant effort. Smaller integrated circuits allow more devices to be formed in one semiconductor chip. Additionally, power consumption and performance are also improved. With circuits becoming smaller and faster, improvement in the device driving current is becoming more important, which can be increased by improving carrier mobility. Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to the circuit fabrication or design.

[0003] Research has revealed that a bi-axial in-plane tensile stress field can improve NMOS performance, and a compressive stress parallel to the channel length direction can improve PMOS device performance. A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved. Typically, thick CESLs are preferred since thicker CESLs apply greater stresses in the channel regions of MOS devices. Another commonly used method is forming stressors in source/drain regions. The stressors typically have lattice constants different from that of the semiconductor substrate in which the MOS devices are formed.

[0004] The scaling of integrated circuits, however, encounters a problem with such a method. FIG. **1** illustrates a modeling of the resistances in a MOS device. The resistances include four portions, a contact resistance R_{co}, an extension resistance $R_{extension}$, an overlap resistance R_{ol}, and a channel region $R_{channel}$. FIG. **2** illustrates a trend reflecting the weight of an external resistance R_{ext}, which equals (R_{co}+$R_{extension}$+R_{ol}), with respect to the channel resistance $R_{channel}$ as a function of the technology nodes. It is found that for 130 nm technology or greater, external resistance R_{ext} is small compared to the channel resistance $R_{channel}$. With the scaling of integrated circuits, R_{ext} becomes increasingly greater with respect to the channel resistance $R_{channel}$. Since the device drive current is inversely proportional to the total resistance ($2R_{ext}$+$R_{channel}$), the increase in drive current is at least partially offset by the increase in external resistance R_{ext}. When technologies evolve to 65 nm and beyond, the benefit of stressing channels to increase device drive currents is so small that the benefit will no longer be worth the process complexity introduced for generating stresses. It is also expected that in 45 nm technology and below, extension resistance $R_{extension}$ will far exceed channel resistance $R_{channel}$. Beyond 45 nm technology, R_{ext} becomes the bottleneck for further improvement of device performance. Since contact resistance R_{co} plays an important role in R_{ext}, it must be reduced in order to continue improving the device performance, especially when the gain comes from strained silicon. A semiconductor device that may overcome the previously discussed deficiencies of the prior art is thus needed.

SUMMARY OF THE INVENTION

[0005] In accordance with one aspect of the present invention, a semiconductor structure includes a semiconductor substrate, an NMOS device, and a PMOS device on a surface of the semiconductor substrate. The NMOS device includes a first source/drain electrode on a source/drain region of the NMOS device, wherein the first source/drain electrode has a first barrier height, and a first stressed film having a first intrinsic stress over the NMOS device. The PMOS device includes a second source/drain electrode on a source/drain region of the PMOS device, wherein the second source/drain electrode has a second barrier height, and a second stressed film having a second intrinsic stress over the PMOS device. The first intrinsic stress is preferably more tensile than the second intrinsic stress. The first barrier height is preferably different from the second barrier height.

[0006] In accordance with another aspect of the present invention, a semiconductor structure includes: a semiconductor substrate; an NMOS device comprising a first source/drain electrode over a first portion of the semiconductor substrate, wherein the first portion has a first lattice constant, and wherein the first source/drain electrode comprises a first metal; and a PMOS device comprising a second source/drain electrode over a second portion of the semiconductor substrate, wherein the second portion has a second lattice constant greater than the first lattice constant, and wherein the second source/drain electrode comprises a second metal different from the first metal. The semiconductor structure further includes a stressed film over the NMOS device and the PMOS device.

[0007] In accordance with yet another aspect of the present invention, a method for forming a semiconductor structure includes: providing a semiconductor substrate; forming an NMOS device at a surface of the semiconductor substrate, which comprises forming a first source/drain electrode on a first source/drain region of the NMOS device, wherein the first source/drain electrode has a first barrier height; and forming a PMOS device, which comprises forming a second source/drain electrode on a second source/drain region of the PMOS device, wherein the second source/drain electrode has a second barrier height, and wherein the first barrier height is different from the second barrier height. The method further includes forming a first stressed film having a first intrinsic stress over the NMOS device, and forming a second stressed film having a second intrinsic stress over the PMOS device. The first intrinsic stress is more tensile than the second intrinsic stress.

[0008] In accordance with yet another aspect of the present invention, a method for forming a semiconductor structure includes: providing a semiconductor substrate; forming a first source/drain region of a first MOS device, wherein the first source/drain region has at least a portion in the semiconductor substrate; forming a second source/drain region of a second MOS device, wherein the second source/drain region has at least a portion in the semiconductor substrate; and wherein the second MOS device is of an opposite conductivity type than the first MOS device. The method further includes: masking the second MOS device; forming a first source/drain electrode having a first barrier height on the first source/drain region; masking the first MOS device; forming a second

source/drain electrode having a second barrier height on the second source/drain region, wherein the first barrier height is different from the second barrier height; forming a first stressed film having a first intrinsic stress over the first MOS device; and forming a second stressed film having a second intrinsic stress over the second MOS device, wherein the first intrinsic stress is more tensile than the second intrinsic stress.

[0009] The advantageous feature of the present invention includes reduced contact resistance in MOS devices. The improvements in device drive currents resulting from the stressed channel regions are thus significant enough to justify the process complexity introduced by forming stressed channel regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0011] FIG. **1** illustrates a modeling of the resistances in a MOS device;

[0012] FIG. **2** illustrates ratios of an external resistance with respect to a channel resistance as a function of technology nodes; and

[0013] FIGS. **3** through **10** illustrate cross-sectional views of intermediate stages in the manufacture of a preferred MOS embodiment.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0014] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0015] To continue the trend of improving the device drive current with stressed channels, the external resistance R_{ext} needs to be reduced. It has been found that the greatest portion of the external resistance R_{ext} is the contact resistance between the source/drain electrodes and the underlying source/drain regions. As used herein, source/drain represents either source or drain or both. With the scaling of integrated circuits, the contact resistance will become an increasingly greater portion of the external resistance. The contact resistance is exponentially proportional to a barrier height Φ between the source/drain electrodes and the underlying semiconductor substrate. Therefore, reducing barrier height Φ will exponentially reduce the contact resistance. The preferred embodiments of the present invention are thus provided to address such reasoning.

[0016] FIG. **3** illustrates a substrate **30** comprising two regions, a region **100** for forming an NMOS device and a region **200** for forming a PMOS device. Shallow trench isolation (STI) regions are formed in substrate **30** to isolate device regions **100** and **200**. Substrate **30** is preferably a bulk silicon substrate, but other commonly used materials and structures such as SiGe, silicon on insulator (SOI), SiGe on insulator, and strained silicon on insulator can also be used. A gate stack, including a gate dielectric **104** and a gate electrode **106**, is formed in NMOS region **100**. Similarly, a gate stack, including a gate dielectric **204** and a gate electrode **206**, is formed in PMOS region **200**.

[0017] Lightly doped drain/source (LDD) regions **108** and **208** are then formed. Preferably, a photo resist **110** is formed and patterned to mask NMOS region **100**. PMOS region **200** is then implanted with a p-type impurity such as boron, and LDD regions **208** are formed. Photo resist **110** is then removed. Similarly, NMOS region **100** may be implanted with an n-type impurity, forming LDD regions **108**. During the n-type impurity implantation, PMOS region **200** is masked by a photo resist (not shown).

[0018] FIG. **4** illustrates the formation of spacers **114** and **214** in regions **100** and **200**, respectively. As is known in the art, the formation of spacers preferably includes forming one or more dielectric layer(s) and etching the dielectric layer(s). The remaining portion of the dielectric layer(s) becomes spacers. The formation of the dielectric layer(s) includes commonly used techniques, such as plasma enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), sub-atmospheric chemical vapor deposition (SACVD), and the like. Spacers **114** and **214** may comprise a single layer or more than one layer, such as a silicon nitride layer on a silicon oxide layer.

[0019] FIG. **5**A illustrates the formation of the source/drain regions **120** and **220**. As is known in the art, source/drain regions **120** and **220** may be recessed in or elevated above substrate **30** (using, e.g., epitaxially grown regions). In the preferred embodiment, source/drain regions **120** and **220** are formed by implanting impurities into semiconductor substrate **30**. Gate electrodes **106** and **206** are preferably implanted simultaneously with the respective source/drain regions to reduce sheet resistance. When region **100** is implanted with an n-type impurity, region **200** is masked by a photo resist (not shown). Similarly, when region **200** is implanted with a p-type impurity, region **100** is masked by a photo resist (not shown). The resulting NMOS device and PMOS device are denoted as NMOS device **102** and PMOS device **202**, respectively.

[0020] Implantation may also be performed to introduce stress to channel regions. Preferably, atoms of a material with a native lattice constant greater than that of silicon, for example, germanium, are preferably implanted into source/drain regions **220** to introduce compressive stress to the channel region of PMOS device **202**. Atoms of a material with a native lattice constant smaller than that of silicon, for example, carbon, are preferably implanted into source/drain region **120** to introduce tensile stress to the channel region of NMOS device **102**.

[0021] In alternative embodiments, as is shown in FIG. **5**B, SiGe stressors **218** are formed in PMOS regions **200**. Preferably, a photo resist **122** is formed covering NMOS region **100**. Recesses are formed in substrate **30** along the outside edges of the spacers **214**, preferably by etching. SiGe stressors **218** are then formed in the recesses. In the preferred embodiment, SiGe stressors **218** are epitaxially grown. P-type impurities, such as boron, may be doped either during or after the epitaxial growth. The photo resist **122** is then removed. Stressors **218** introduce a compressive stress to the respective channel region of the resulting PMOS device **202**, and the drive current of the respective PMOS device **202** is increased. SiC stressors (not shown) may also be formed in source/drain regions **120** for NMOS device **102** using similar methods.

[0022] FIG. **6** illustrates the formation of a mask layer **124** covering NMOS region **100**. In the preferred embodiment, mask layer **124** is a blanket resist protective oxide (RPO) layer. The portion of the mask layer **124** over PMOS region **200** is removed. Exemplary RPO materials include silicon oxide, silicon nitride, and combinations thereof. The removal process of the mask layer **124** includes wet etching and dry etching. Mask layer **124** preferably has an inherent tensile stress.

[0023] Referring to FIG. **7**, source/drain electrodes **226** are formed on source/drain regions **220**. In a first embodiment for forming source/drain electrodes **226**, a metal layer is blanket deposited. The metal layer preferably includes metals that will have a low barrier height with the underlying semiconductor material, such as platinum, manganese, palladium, cobalt, nickel, tantalum, ruthenium, tungsten, and combinations thereof. As a result, contact resistance is reduced. The device is then annealed to form a silicide between the deposited metal layer and the underlying source/drain regions **220**. Un-reacted metal is then removed. Gate electrode **206** is preferably silicided simultaneously with source/drain regions **220**. It is to be realized that if germanium is present in the source/drain regions, germano-silicide will be formed. Throughout the description, the term "silicide" also includes germano-silicide.

[0024] In a second embodiment, a selective electroless plating is performed. Preferably, source/drain electrodes **226** are deposited from an electroless solution containing at least a metal salt and a reducing agent. The electroless solution may further include additives to improve deposition of the metal. Additives may include surfactants, complexing agents, pH adjusting agents, and combinations thereof. Suitable metal salts include chlorides, sulfates, sulfamates, and combinations thereof. Cobalt chloride is an example of a metal salt. Silicon compounds are also preferably added in the electroless solution, for example, in the form of chemicals comprising Si(OH). The metal salt may be in the electroless solution at a concentration between about 0.5 g/L and about 30 g/L, such as between about 2.5 g/L and about 25 g/L. Suitable reducing agents include sodium hypophosphite, hydrazine, formaldehyde, and combinations thereof. Additives include surfactants, such as RE 610, complexing agents including salts of carboxylic acids, for example, sodium citrate and sodium succinate, pH adjusting agents including sodium hydroxide and potassium hydroxide, and combinations thereof. The additives can be used to control deposition properties of the electroless solution. For example, stabilizers prevent unwanted side reactions while complexing agents may limit available ions in the electroless solution. Additives have a concentration between about 0.01 g/L and about 50 g/L of the electroless solution, such as between about 0.05 g/L and about 4 g/L of the electroless solution.

[0025] Forming the metal layer includes applying the metal electroless solutions described herein to the previously formed structure for between about 30 seconds and about 180 seconds, at a temperature between about 60° C. and about 90° C. The optimum time and temperature may be found through routine experiments.

[0026] In the preferred embodiment, source/drain electrodes **226** comprise metal silicides having a high barrier height with the underlying semiconductor material. The respective metals preferably include platinum, manganese, palladium, cobalt, nickel, tantalum, ruthenium, tungsten, and combinations thereof. As a result, contact resistances between electrodes **226** and the underlying semiconductor material are reduced. Alternatively, source/drain electrodes **226** are substantially pure metal electrodes, and thus the respective contacts to the underlying source/drain regions **220** are Schottky contacts.

[0027] Referring to FIG. **8**, mask layer **124** is removed. A contact etch stop layer (CESL) **228** is formed in region **200**. CESL **228** preferably has a compressive stress, which can be formed by forming a stressed layer directly, or introducing stress into CESL **228** after its formation. Alternatively, CESL **228** may have a tensile stress, however, with a smaller magnitude than the tensile stress applied on NMOS device **102**. Preferably, CESL **228** is blanket deposited, and a portion over NMOS region **100** is etched. The preferred materials of CESL **228** include, but are not limited to, silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, and combinations thereof.

[0028] FIG. **9** illustrates the formation of source/drain electrode regions **130**, which may be formed using essentially the same methods as used for forming source/drain electrodes **226**. Preferably, selective electroless plating is performed. Source/drain electrodes **130** preferably comprise one or more high band-level or mid-gap metals, such as erbium, holmium, titanium, hafnium, zirconium, ytternium, cobalt, nickel, and the like. Source/drain electrodes **130** are preferably silicide regions. Alternatively, they comprise substantially pure metal, and thus the resulting contacts are Schottky contacts. Preferably, if at least one of the source/drain electrodes **130** and **226** are formed using electroless plating, an annealing is performed to form bonds between silicon and metal atoms.

[0029] As a general preference, the selection of the metals in source/drain electrodes **130** and **226** is determined as follows. Assuming an NMOS barrier height Φ_{bp} is defined as the Schottky barrier height between a pure metal source/drain electrode and silicon doped with an n-type impurity, then the metals used in source/drain electrodes **130** are preferably selected so that NMOS barrier height Φ_{bn} is less than about 0.4 eV. Assuming a PMOS barrier height Φ_{bp} is defined as the Schottky barrier height between a pure metal source/drain electrode and silicon doped with an n-type impurity, then the metals used in source/drain electrodes **226** are preferably selected so that PMOS barrier height Φ_{bp} is greater than about 0.7 eV. The difference between barrier heights Φ_{bp} and Φ_{bn} is preferably greater than about 0.15 eV.

[0030] FIG. **10** illustrates the formation of a CESL **132**. Preferably, the materials of CESL **132** include commonly used materials such as silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, and combinations thereof. CESL **132** is preferably tensile-stressed to introduce a tensile stress to the channel region of NMOS device **102**. Alternatively, CESL **132** may have a compressive stress, however, with a smaller magnitude than the compressive stress applied on PMOS device **202**. CESL **132** may include a single layer or a composite layer.

[0031] One skilled in the art will realize that in the preferred embodiment, the sequence for forming source/drain electrodes for NMOS device **102** and PMOS device **202** can be reversed. Also, the orders for forming CESLs **132** and **228** can also be reversed.

[0032] By differentiating barrier heights of source/drain electrodes of NMOS and PMOS devices, the contact resistances between the source/drain electrodes and the underlying source/drain regions are reduced. This results in the improvement of device drive current. The effects of forming

stressed channel regions thus become more significant in small-scale integrated circuits. As a result, MOS devices with gate lengths of less then 65 nm may still have good performance.

[0033] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

1. A method for forming a semiconductor structure, the method comprising:
- providing a semiconductor substrate;
- forming an NMOS device at a surface of the semiconductor substrate comprising forming a first source/drain electrode on a first source/drain region of the NMOS device, wherein the first source/drain electrode has a first barrier height;
- forming a PMOS device at the surface of the semiconductor substrate comprising forming a second source/drain electrode on a second source/drain region of the PMOS device, wherein the second source/drain electrode has a second barrier height, and wherein the first barrier height is different from the second barrier height; and wherein at least one of the steps of forming the first and the second source/drain electrodes is selective electroless plating and is free from a silicidation step;
- forming a first stressed film having a first intrinsic stress over the NMOS device; and
- forming a second stressed film having a second intrinsic stress over the PMOS device, wherein the first intrinsic stress is more tensile than the second intrinsic stress.

2. The method of claim **1**, wherein gate lengths of the PMOS and NMOS devices are less than about 65 nm.

3. The method of claim **1**, wherein the first source/drain electrode comprises a metal selected from the group consisting essentially of platinum, manganese,. palladium, and combinations thereof.

4. The method of claim **1**, wherein the second source/drain electrode comprises a metal selected from the group consisting essentially of erbium, holmium, titanium, hafnium, zirconium, ytterbium, and combinations thereof.

5. (canceled)

6. The method of claim **1**, wherein the steps of forming the first and the second source/drain electrodes comprise:
- electroless plating on one of the first and the second source/drain regions to form a source/drain electrode;
- forming a mask layer over the source/drain electrode; and
- forming a metal layer on a remaining one of the first source/drain region and the second source/drain region.

7. The method of claim **1**, wherein the steps of forming the first and the second source/drain electrodes comprise:
- forming a first mask layer to mask one of the first and the second source/drain regions;
- blanket forming a metal layer;
- performing an annealing to form a silicide region on an unmasked one of the first source/drain region and the second source/drain region;
- removing an un-reacted portion of the metal layer;
- removing the first mask layer;
- forming a second mask layer over the silicide region; and
- electroless plating the one of the first and the second source/drain regions to form one of the first and the second source/drain electrodes.

8. The method of claim **6**, wherein the mask layer is a dielectric hard mask having an intrinsic tensile stress.

9. The method of claim **1**, wherein the first barrier height is less than about 0.4eV.

10. The method of claim **1**, wherein the second barrier height is greater than about 0.7eV.

11. The method of claim **1**, wherein the second barrier height is greater than the first barrier height by greater than about 0.15eV.

12. A method for forming a semiconductor structure, the method comprising:
- providing a semiconductor substrate;
- forming a first source/drain region of an NMOS device, wherein the first source/drain region has at least a portion in the semiconductor substrate;
- forming a second source/drain region of a PMOS device, wherein the second source/drain region has at least a portion in the semiconductor substrate,
- masking the PMOS device;
- forming a first source/drain electrode having a first barrier height less than about 0.4eV on the first source/drain region;
- masking the NMOS device;
- forming a second source/drain electrode having a second barrier height greater than about 0.7eV on the second source/drain region;
- forming a first stressed film having a first intrinsic stress over the NMOS device; and
- forming a second stressed film having a second intrinsic stress over the PMOS device, wherein the first intrinsic stress is more tensile than the second intrinsic stress.

13. The method of claim **12**, wherein gate lengths of the NMOS and PMOS devices are less than about 65 nm.

14-15. (canceled)

16. The method of claim **12**, where at least one of the steps of forming the first and the second source/drain electrodes comprises selective electroless plating.

17. The method of claim **12**, where the steps of forming the first and the second source/drain electrodes both comprise selective electroless plating.

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