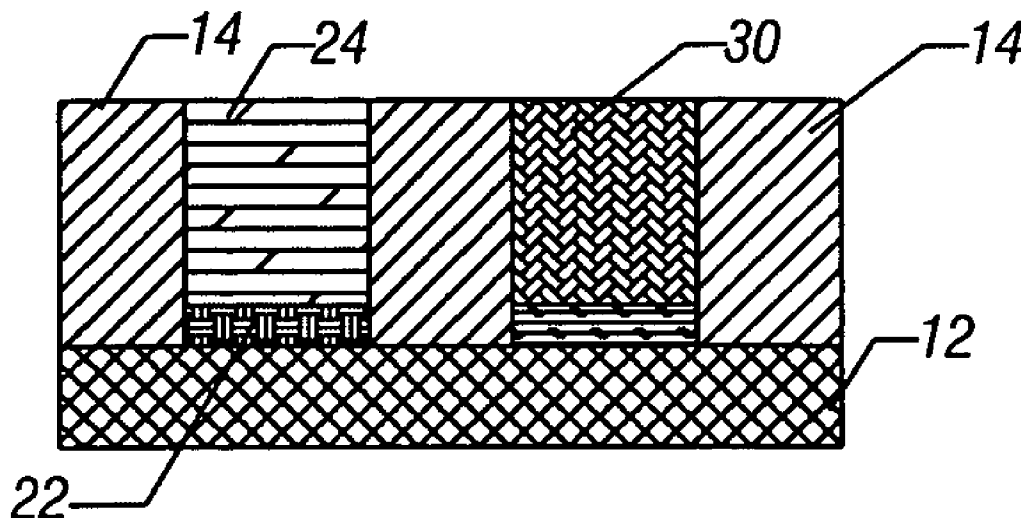




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(19) **United States**(12) **Patent Application Publication**
Metz et al.(10) **Pub. No.: US 2006/0001106 A1**(43) **Pub. Date: Jan. 5, 2006**(54) **USING DIFFERENT GATE DIELECTRICS
WITH NMOS AND PMOS TRANSISTORS OF
A COMPLEMENTARY METAL OXIDE
SEMICONDUCTOR INTEGRATED CIRCUIT**(76) Inventors: **Matthew V. Metz**, Hillsboro, OR (US);
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HOUSTON, TX 77024 (US)(21) Appl. No.: **10/881,055**(22) Filed: **Jun. 30, 2004****Publication Classification**(51) **Int. Cl.****H01L 29/76** (2006.01)**H01L 29/94** (2006.01)(52) **U.S. Cl.** **257/369**(57) **ABSTRACT**

Complementary metal oxide semiconductor integrated circuits may be formed with NMOS and PMOS transistors having different gate dielectrics. The different gate dielectrics may be formed, for example, by a replacement process. The gate dielectrics may differ in material, thickness, or formation techniques, as a few examples.



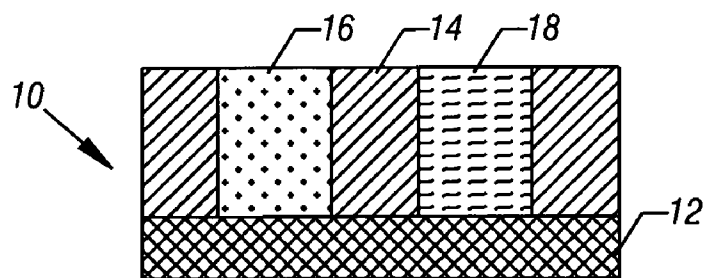


FIG. 1

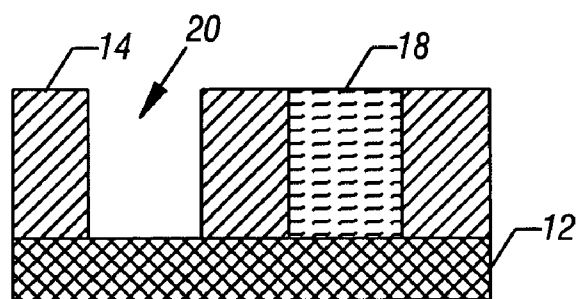


FIG. 2

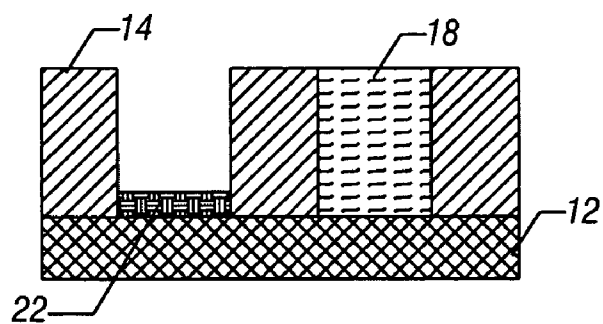


FIG. 3

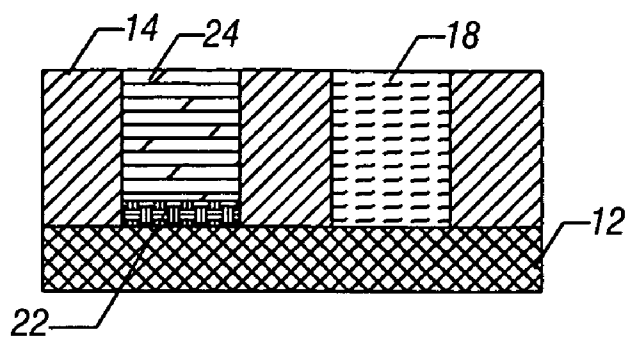


FIG. 4

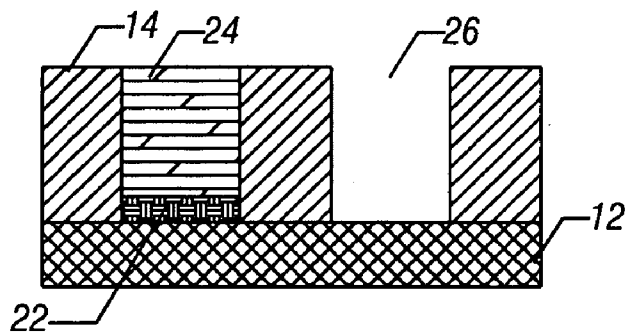


FIG. 5

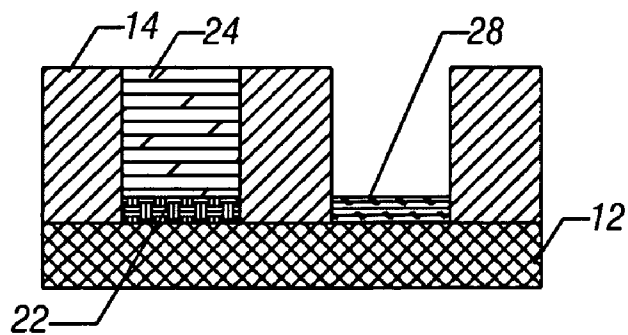


FIG. 6

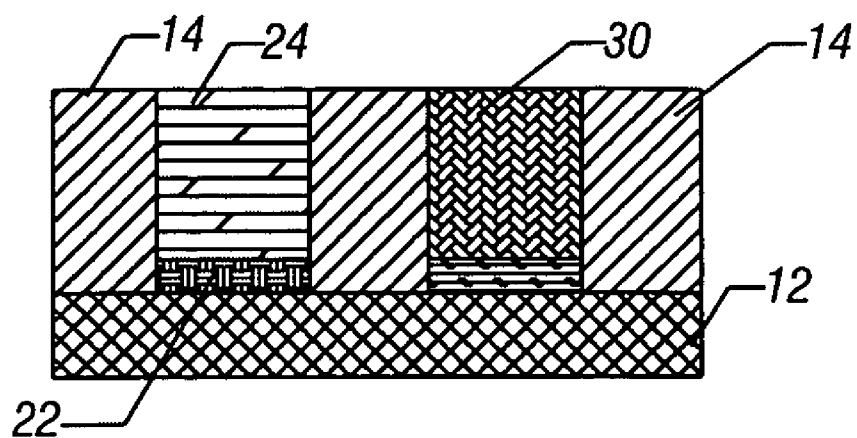


FIG. 7

USING DIFFERENT GATE DIELECTRICS WITH NMOS AND PMOS TRANSISTORS OF A COMPLEMENTARY METAL OXIDE SEMICONDUCTOR INTEGRATED CIRCUIT

BACKGROUND

[0001] This invention relates generally to semiconductor technology, semiconductor processing, and the formation of complementary metal oxide semiconductor integrated circuits.

[0002] Complementary metal oxide semiconductor integrated circuits include NMOS transistors and PMOS transistors. Generally, these transistors may be made by forming a gate dielectric and then forming NMOS and PMOS gate structures on top of that dielectric. The gate electrode structures may be made of polysilicon, silicide, or metal.

[0003] A dummy gate electrode, such as a polysilicon gate electrode, may also be formed over a gate dielectric. Then the dummy gate electrode may be removed and replaced with a metal gate electrode. In such a process, different metal gate electrodes may be utilized for the NMOS and PMOS transistors, but a common dielectric is utilized.

[0004] Thus, there is a need for complementary metal oxide semiconductor fabrication techniques.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 is an enlarged, partial, cross-sectional view of one embodiment of the present invention at an early stage of manufacture;

[0006] FIG. 2 is an enlarged, partial, cross-sectional view of the embodiment shown in FIG. 1 at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

[0007] FIG. 3 is an enlarged, partial, cross-sectional view of the embodiment shown in FIG. 2 at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

[0008] FIG. 4 is a partial, enlarged, cross-sectional view of the embodiment shown in FIG. 3 at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

[0009] FIG. 5 is an enlarged, partial, cross-sectional view of the embodiment shown in FIG. 4 at a subsequent stage of manufacture in accordance with one embodiment of the present invention;

[0010] FIG. 6 is a partial, enlarged, cross-sectional view of the embodiment shown in FIG. 5 at a subsequent stage of manufacture in accordance with one embodiment of the present invention; and

[0011] FIG. 7 is a partial, enlarged, cross-sectional view of the embodiment shown in FIG. 6 at a subsequent stage of manufacture in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0012] Complementary metal oxide semiconductor (CMOS) integrated circuits may be fabricated with NMOS and PMOS transistors having different gate dielectrics. The

dielectrics may be different in terms of the materials used, their thicknesses, or the techniques used to form the gate dielectrics, to mention a few examples. As a result, the gate dielectric can be tailored to the particular type of transistor, be it an NMOS or PMOS transistor, as the case may be.

[0013] Referring to FIG. 1, in accordance with one embodiment of the present invention, an initial semiconductor structure 10 includes a semiconductor substrate 12 having an insulator 14 formed thereon with trenches filled by dummy gate materials 16 and 18. The dummy gate materials 16 and 18, in one embodiment, may be doped polysilicon, for example.

[0014] Referring to FIG. 2, the dummy gate material 16 has been removed. The removal of the dummy gate material 16 may be accomplished by masking, etch-out, or other methods. In an etch-out process, the material 16 may be selectively etched relative to the material 18. Thus, in one embodiment, the materials 16 and 18 may be different materials such that one may be etched selectively relative to the other. If an etchant, such as a wet etchant, is utilized which preferentially attacks the material 16, the material 16 can be selectively etched while the material 18 remains.

[0015] For example, in accordance with one embodiment of the present invention, the material 16 may be an N-doped polysilicon, while the material 18 is a P-doped polysilicon. An etchant such as tetramethylammonium hydroxide (TMAH) or NH_4OH , together with sonication, may be utilized to selectively etch one of the materials 16 or 18, while not significantly etching the other material. Depending on the choice of wet etchant utilized to etch the material 16 or 18, one of the dummy gate materials 16 and 18 can be etched while the other one is substantially unetched. Then the other or remaining gate material 16 or 18 may be removed.

[0016] Referring to FIG. 3, in accordance with one embodiment of the present invention, a dielectric 22 may be formed on the substrate 12 in the opening 20 created by the removal of the gate material 16. In one embodiment, the dielectric 22 can be selected to have characteristics to optimize the performance of either an NMOS or PMOS transistor to be formed in the region 20. For example, the gate dielectric 22 material, thickness or formation technique may be tailored for its particular application.

[0017] For example, the NMOS transistor may use a larger conduction band offset material, such as silicon dioxide, and the PMOS transistor may use a material with a higher dielectric constant, such as hafnium dioxide, which also happens to have good band offset for holes. Higher dielectric constants may be greater than ten in one embodiment. As another example, a thicker material may be utilized for the NMOS than the PMOS transistors in some cases. For example, hafnium dioxide leaks electrons more than holes, so a thicker hafnium dioxide layer may be utilized on the NMOS transistors and a thinner hafnium dioxide layer may be utilized on the PMOS transistors. For example, in one embodiment, the hafnium dioxide gate dielectric may be 30 Angstroms for the NMOS transistors and 15 Angstroms for the gate dielectric for PMOS transistors.

[0018] As still another example, the deposition techniques may be different for the two gate dielectrics. For example, materials for the NMOS transistor, such as silicon dioxide,

may be deposited using diffusion techniques, while atomic layer deposition, sputtering, or metal organic chemical vapor deposition (MOCVD) may be utilized to deposit high dielectric constant materials such as hafnium dioxide.

[0019] One gate dielectric may be a high-k material (having a dielectric constant greater than 10) and the other may be a low-k material (having a dielectric constant less than 10). Alternatively, both dielectrics may be high-k or both may be low-k dielectrics.

[0020] The appropriate gate electrode material **24** may then be deposited over the gate dielectric **22** in the opening **20** created by the removal of the material **16**.

[0021] Referring to **FIG. 4**, a gate electrode material **24** may be deposited over the gate dielectric **22**. The material **24** may be any conductive material, including doped polysilicon or metal. The material may be deposited using any suitable technique.

[0022] Referring to **FIG. 5**, the gate material **18** may be selectively removed. The selective removal may again be accomplished using selective etching, masking, or any other method to remove the material **18**, while leaving the material **24**.

[0023] Then, as shown in **FIG. 6**, a gate dielectric **28** may be formed in the opening **26** created by the removal of the material **18**. Again, the characteristics of the gate dielectric **28** may be optimized for its particular application, be it for a PMOS or an NMOS transistor. For example, its thickness, formation technique, or the material utilized may be selected to optimize the performance of the ultimate transistor.

[0024] In some embodiments of the present invention, it may be desirable to ensure that the material **18** is selectively etchable relative to the material **24**. For example, selective etching may be based on the fact that the materials **18** and **24** are of a different material type.

[0025] Referring to **FIG. 7**, an appropriate gate electrode material **30** may then be formed in the opening **26** over the gate dielectric **28**. In some embodiments, the gate materials **24** and **30** may be doped polysilicon, may include silicide, or may be a metal.

[0026] In some embodiments, a single gate dielectric material may not provide the highest performance for both NMOS and PMOS structures. This may be due, for example, to poor band offset with conduction or valence bands, incompatibility to the gate electrode material, incompatibility with gate electrode processing or thickness requirements. By selecting the better candidate dielectric film for each structure, and depositing the best film with the optimal thickness, higher performance complementary metal oxide semiconductor devices may be created in some embodiments. By using better gate dielectric material of optimal thickness for each electrode stack, higher performance structures may be created that may exhibit higher mobility, higher saturation current, or better threshold voltage in some embodiments.

[0027] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

1. A method comprising:

filling a first trench with a first material and a second trench with a second material;

selectively etching the first material in the first trench to remove said first material;

forming a gate dielectric in said first trench while said second trench remains filled with said second material; and

forming a gate electrode over said dielectric in said first trench.

2. The method of claim 1 including forming transistors having different gate dielectrics.

3. The method of claim 1 including forming transistors having different gate dielectrics.

4. The method of claim 3 wherein forming transistors having different gate dielectrics includes forming transistors having gate dielectrics deposited by different techniques.

5-7. (canceled)

8. The method of claim 1 including forming NMOS and PMOS transistors with metal gates.

9. The method of claim 8 including using an NMOS gate dielectric with a larger conduction band offset.

10. The method of claim 9 including using a PMOS gate dielectric with a higher dielectric constant than the NMOS gate dielectric.

11. The method of claim 10 including using a thicker gate dielectric for said NMOS transistor than for said PMOS transistor.

12. The method of claim 11 including using gate dielectrics with dielectric constants greater than 10 as the gate dielectrics of said NMOS and PMOS transistors.

13. The method of claim 10 including using silicon dioxide for said gate dielectric for said NMOS transistor and using a material having a dielectric constant greater than that of silicon dioxide for said PMOS transistor.

14. The method of claim 13 including depositing said dielectric for said NMOS transistor using diffusion.

15. The method of claim 13 including forming the dielectric for said PMOS transistor using one of atomic layer deposition, metal organic chemical vapor deposition, or sputter deposition.

16. An integrated circuit comprising:

a substrate; and

NMOS and PMOS transistors formed on said substrate, said transistors forming a complementary metal oxide semiconductor structure, said transistors having different gate dielectrics, one of said transistors having a gate dielectric with a dielectric constant greater than 10 and the other of said transistors having a gate dielectric with a dielectric constant of less than 10.

17. The circuit of claim 16 wherein said dielectrics have different dielectric thicknesses.

18. The circuit of claim 16 wherein said dielectrics are formed of different dielectric materials.

19. The circuit of claim 16 wherein said dielectrics are formed by different techniques.

20. The circuit of claim 16 wherein said dielectrics are covered by metal gate electrodes.

21. The circuit of claim 16 wherein said NMOS transistor has a gate dielectric with a larger conduction band offset.

22. The circuit of claim 16 wherein said PMOS transistor has a gate dielectric with a higher dielectric constant.

23. The circuit of claim 16 wherein the gate dielectric of said NMOS transistor is thicker than the gate dielectric of said PMOS transistor.

24-36. (canceled)

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