UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Advanced Integrated Circuit Process LLC,

Patent Owner

Patent No. 8,198,686 B2
Filing Date: December 2, 2009
Issue Date: June 12, 2012

Title: SEMICONDUCTOR DEVICE

Inter Partes Review No. IPR2025-00682

**DECLARATION OF DR. SCOTT E. THOMPSON, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 8,198,686**

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I, Dr. Scott E. Thompson, Ph.D., declare as follows:

I. Introduction

1. My name is Dr. Scott E. Thompson. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited ("TSMC") in connection with a petition for *inter partes* review of U.S. Patent No. 8,198,686 ("'686 Patent"), which I have been told TSMC is submitting to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-35 of the '686 Patent ("Challenged Claims").

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the bases for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the '686 Patent is unpatentable for at least the reasons I discuss below.

II. Background and Qualifications

A. Education and Career

5. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing, and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

6. I received a Ph.D. degree in Electrical Engineering from the University of Florida in 1992. Before that, I received a Master of Science degree in 1988 and a Bachelor of Electrical Engineering with Highest Honors in 1987, both from the University of Florida.

7. I was employed at Intel Corporation ("Intel") from 1992 to 2004. During that time, I worked on evaluating, implementing, and ramping into high-volume production new materials, process architectures, and transistor structures. I was the yield manager and overall program manager for Intel's 90 nanometer (nm) process.

8. Of specific relevance to this case, I played a key role at Intel in the development of a form of strained silicon using silicon germanium ("SiGe") implemented in the source/drain regions of p-type field effect transistors ("pFETs") that I refer to as "SiGe/Strained Silicon" technology in this report. The original SiGe/Strained Silicon technology concept was developed around the year 2000

(about eight years before the earliest claimed priority date for the '686 Patent). SiGe/Strained Silicon quickly became a nearly universal technology that speeds up transistors in all types of integrated circuits. Modern integrated circuits use both nFETs (negative charge flows) and pFETs (positive charge flows). Before the development of SiGe/Strained Silicon, pFETs were about half the speed of nFETs. SiGe/Strained Silicon improved pFET speed to equal that of nFETs, which provides a large benefit to power and performance.

9. Through my work in the industry, I was aware that TSMC adopted strained silicon in 2003.[1] By 2008, TSMC had added many inventions to the field of SiGe/Strained Silicon. Today, TSMC is the undisputed leader in producing integrated circuits, as even Intel's current CEO has acknowledged.[2]

[1] *See* M. LaPedus, "TSMC to Offer Strained-Silicon at 90- and 65-nm Nodes," EE Times (Apr. 22, 2003), https://www.eetimes.com/tsmc-to-offer-strained-silicon-at-90-and-65-nm-nodes/.

[2] *See* K. Tarasov, "How Intel Plans to Catch Samsung and TSMC and Regain Its Dominance in the Chip Market," CNBC (Nov. 6, 2021) ("'We had some missteps,' said Pat Gelsinger, who took over as Intel's CEO in February [2021]. . . . Gelsinger has an ambitious roadmap to catch and surpass . . . TSMC by 2025."), *available at* https://www.cnbc.com/2021/11/06/how-intel-plans-to-catch-up-to-samsung-and-tsmc-with-44-billion-of-new-global-chip-fabs.html; *see also* Vested Finance, "The Empires that TSMC Built" (Mar. 28, 2022), *available at* https://vestedfinance.com/in/blog/the-empires-that-tsmc-built/.

10. Working at Intel, I announced the SiGe/Strained Silicon technology to the industry in 2002.[3] I managed a team of about 100 engineers that developed and implemented the SiGe/Strained Silicon technology in pFETs that went into high-volume manufacturing in 2003 as part of Intel's 90 nm process. My team was responsible for fabricating, ramping into production, and transferring the SiGe/Strained Silicon technology to Intel's design and fabrication sites worldwide. The SiGe/Strained Silicon technology has been used by Intel for its entire microprocessor product line since the 90 nm process, including its latest 7th generation of SiGe/Strained Silicon. Within a few years after 2002, every advanced computer chip manufacturer was using SiGe/Strained Silicon technology.

11. My work on the SiGe/Strained Silicon technology helped me earn an **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers ("IEEE") Fellow rank (awarded in 2006), along with numerous industry awards for our Intel development team. In 2008, I and key members of the Intel SiGe/Strained Silicon development team were awarded the SEMI AWARD NORTH AMERICA for "Process Integration of Strain-

[3] *See* D. Lammers, "Industry Reacts to Intel's Strained Silicon Move," EE Times (Aug. 16, 2002), *available at* https://www.eetimes.com/industry-reacts-to-intels-strained-silicon-move/#.

enhanced Mobility Techniques for CMOS Transistors."[4] This award is the highest honor achievable through SEMI, a 2,000-member trade organization.

12. In 2007, my Intel colleague Mark Bohr described my role and how Intel came to invent the SiGe/Strained Silicon technology.[5] At Intel, I worked on several generations of Intel's transistors, each of which implemented SiGe/Strained Silicon technology after 2002.

13. I have given invited talks and organized and taught international courses on SiGe/Strained Silicon technology. For example, I was asked to give a lecture on strained silicon at the 2006 International Electron Devices Meeting.

14. I have also developed and taught graduate level courses on SiGe/Strained Silicon technology at the University of Florida, including a course entitled "EEE5400: Future of Nano/Micro Electronics."

15. As a professor at the University of Florida, I have been awarded over $4 million in research funding largely directed towards understanding the scalability of SiGe/Strained Silicon transistors. I have received research funding from the

[4] *See* SEMI AWARD NORTH AMERICA RECIPIENTS, https://www.semi.org/en/semi-organization/awards/north-american-semi-award/recipients.

[5] *See* https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.488.9606&rep=rep1&type=pdf. As explained by Mark, "By early 2002 [Scott Thompson] became the 90 nm program manager and was responsible for getting strained silicon transistors along with copper plus low-k interconnects to meet performance, yield and reliability requirements in time for the first product shipments in 2003."

National Science Foundation, Semiconductor Research Corporation, and other agencies. I am currently conducting industry-funded research to investigate strained transistors.

16. As a result of my industry work, I am familiar with various areas of advanced computer chip technology. I have worked extensively on the use of shallow trench isolation ("STI") in manufacturing processors, novel low-resistance source and drain regions, silicides (titanium, cobalt, and nickel silicide), and low-resistance tungsten plugs. Throughout 1991-2004, I was part of the Intel development team that introduced titanium, cobalt, and nickel silicide into the production of high-performance microprocessors.[6] My work experience has also extended to layout design rules, SRAM cell layouts, oxide and nitride spacer formation, gate patterning, gate oxides, gate electrodes, interlayer dielectrics, electrical contacts, silicide, interconnects, process integration (lithography, etch, diffusion, thin film deposition, and chemical mechanical polishing), and yield and reliability.

[6] *See, e.g.*, S. Thompson et al., "A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell," Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002); A. Brand et al., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology," Intel Technology Journal (Q3 1998).

17. As one of the original inventors of SiGe/Strained Silicon technology, I am extremely familiar with MISFETs (**M**etal-**I**nsulator-**S**emiconductor **F**ield **E**ffect **T**ransistors), including related technology and manufacturing techniques. I have authored numerous papers, given many invited talks, and organized and taught international courses on MISFETs, including, for example, courses for the IEEE.

18. Every year since 2004 (except for one year when I took a sabbatical and the course was taught by video), I have taught a course I developed at the University of Florida on future MISFET technologies and designs. I have also taught other undergraduate and graduate courses on MISFETs, transistor layout, and fabrication at the University of Florida, including courses covering the scaling and scaling limits of MISFETs.

19. I have experience analyzing transmission electron microscope ("TEM") images at Intel and other places in industry, including as a consultant of Chipworks, an independent reverse engineering firm that merged with TechInsights, another independent reverse engineering firm. I helped Chipworks staff understand features of transistors in electron micrographs (pictures obtained using electrons to image transistor structures).

20. I also co-founded a low-power transistor technology company called SuVolta in 2009 that developed transistors that could operate at ultra-low power for

internet-of-things applications. SuVolta's intellectual property was sold to Fujitsu and included patents on FETs that could operate at ultra-low power.

21. As the co-founder and Chief Technology Officer of SuVolta, and as an inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

22. I am a named inventor on over 100 granted United States patents and have authored over 60 peer-reviewed academic journal publications. I have co-authored a book on strained silicon transistors titled *Strain Effects in Semiconductors: Theory and Device Applications* (2009). I have patents and publications on SiGe/Strained Silicon technology, high-κ gate dielectric films, metal gate electrodes, and nanoscale transistors, all of which are relevant technologies in this case. Some examples are:

- My work on the SiGe/Strained Silicon technology is described in frequently cited IEEE peer-reviewed papers, including the following:
    - S. Thompson, et al., "A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell," Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002) (cited over 450 times in peer-reviewed literature);

  - S.E. Thompson et al., "A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, vol. 25, no. 4, pp. 191-93 (Apr. 2004) (cited nearly 700 times in peer-reviewed literature); and

  - S. Thompson et al., "In Search of 'Forever,' Continued Transistor Scaling One New Material at a Time," IEEE Transactions on Semiconductor Manufacturing, vol. 18, no. 1, pp. 26-36 (Feb. 2005) (cited over 250 times in peer-reviewed literature).

- The history of the SiGe/Strained Silicon invention is explained in the frequently cited IEEE peer-reviewed paper S.E. Thompson et al., "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," IEEE Transactions on Electron Devices, vol. 53, no. 5, pp. 1010-20 (May 2006) (cited nearly 750 times in peer-reviewed literature).

23. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which I understand is being included as Ex-1004.

24. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae.

25. I am being compensated for services provided in this matter at my standard consulting rate, plus travel expenses. My compensation is in no way conditioned on the outcome of this *inter partes* review or any issue therein, nor is it contingent upon the results of my study or the substance of my testimony. Similarly, my compensation is in no way dependent upon and in no way affects the substance of my statements in this declaration.

III. Materials Reviewed

26. In forming my opinions regarding the ’686 Patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. Legal Standards

27. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the ’686 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

28. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. § 102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

29. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

30. I have been told that under 35 U.S.C. § 103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in § 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

31. When considering the issues of obviousness, I have been told that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

32. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged

invention, which I have been asked to assume is just before the earliest claimed priority date of the '686 Patent (i.e., **March 13, 2008**).

33. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '686 Patent).

34. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

35. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

36. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of

ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

37. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

38. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

39. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

40. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

41. When considering the obviousness of claimed dimensions, I have been told obviousness depends on whether a person of ordinary skill in the art would have appreciated that new and unexpected properties (as compared with known dimensions and trends) resulted from the claimed dimensions. I have been told that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable dimensions by routine experimentation. For example, I have been told that if the prior art teaches the dimensions in a device can

be modified to affect the device properties, it is not inventive to discover the optimum or workable dimensions by routine experimentation. I have also been told the prior art does not need to provide the exact method of optimization, and a claim to a device does not become non-obvious simply because the patent's specification provides a more comprehensive explication of the known relationships between dimensions and device properties.

42. I have been told that the outcome of optimizing a device dimension may only be patentable if the claimed dimensions are "critical" and produce a new and unexpected result that differs in kind, not merely in degree, from the results of the prior art. I have been told that when obtaining the claimed dimension was within the capabilities of a person of ordinary skill in the art and does not produce any unexpectedly beneficial properties, the optimization of a dimension known to affect device properties would have been obvious.

43. In addition, I have been told that any allegedly new and unexpected result must be "commensurate in scope" with the claimed range of dimensions, meaning the new and unexpected result must apply across the entire range of dimensions recited in the claim.

V. Level of Ordinary Skill in the Art

44. I have been informed that a person of ordinary skill in the art ("POSITA") is determined by considering several factors, including the (i) type of

problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

45. I have been instructed to assume a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

46. A person having ordinary skill in the art in reference to the ’686 Patent would have had at least a master’s degree in electrical engineering, physics, materials science, or a related field and at least three years of work experience in semiconductor device design and manufacturing, including replacement metal gates, strained-channel MISFETs, and fabrication of such devices. Additional education could substitute for professional experience, and significant work experience or training could substitute for formal education.

47. I have not analyzed the priority date of the ’686 Patent, but I note that the earliest claim of priority listed on the face of the ’686 Patent is March 13, 2008, the filing date of Japanese Patent Application Serial No. 2008-064435. Because all the prior art discussed in this declaration predates March 13, 2008, I have been asked for simplicity to treat **March 13, 2008**, as the priority date for the ’686 Patent. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

VI. Technological Background

48. I understand that **March 13, 2008**, may be the earliest claimed priority date for the '686 Patent. In my opinion, all the elements in the '686 Patent were well known before this date—in fact, already commonplace in high-volume commercial production. For example, as explained below, SiGe/Strained Silicon technology was in widespread use well before 2008. In fact, each of the three preceding generations of high-volume commercial devices (i.e., 90nm, 65nm, and 45nm devices) used SiGe/Strained Silicon technology. So has every generation of high-volume commercial transistors ever since. And, beginning with the 45nm generation, high-volume commercial transistors have also used high-κ gate dielectrics and replacement metal gates.

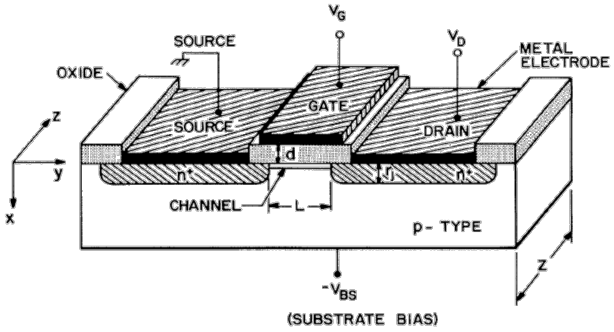
49. A person of ordinary skill in the art in the timeframe relevant to the '686 Patent would have been familiar with the background information described in subsections A through D below.

A. MISFETs

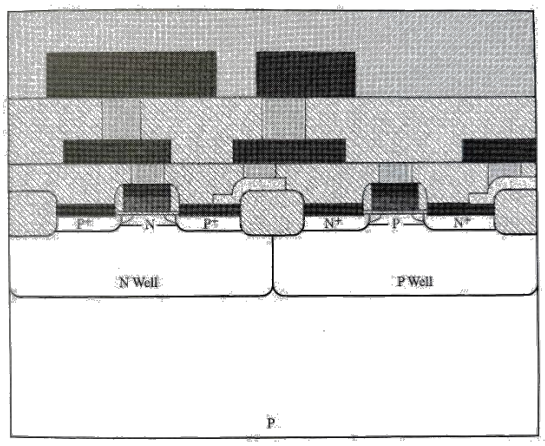
50. A "MISFET" is a "**M**etal-**I**nsulator-**S**emiconductor **F**ield-**E**ffect **T**ransistor."[7] MISFETs have a ***source*** and a ***drain*** for current input and output. Sze,

[7] The term "MOSFET" is also used to describe such devices. MOSFET stands for "Metal-***Oxide***-Semiconductor Field-Effect Transistor," referring specifically to oxide-based insulators. Although other insulator materials also may be used, a POSITA would have understood "MISFET" and "MOSFET" are interchangeable.

433-34, Figs. 3, 6; Plummer, 76-82. MISFETs like the ones at issue here also have a ***gate*** above a ***channel*** region between the source and drain. Sze, 433-34, Fig. 3; Plummer, 71-76. The ***gate*** includes a ***gate electrode*** separated from the channel region by a ***gate dielectric*** (also called a gate "oxide" or gate "insulator"). Sze, 433-34, Fig. 3; Plummer, 71-76. Applying appropriate voltage to the gate electrode controls a conductive channel in the channel region to connect or disconnect the source and drain regions. Sze, 433-34, 438, Figs. 3, 6.



Sze's Fig. 3



Plummer's Fig. 1-11

51. Source/drain regions are generally doped with either a ***p-type*** or ***n-type*** impurity, and the channel region is generally doped with the opposite type. *See* Sze, 433-34; Plummer, 76-82. A MISFET with ***n***-type source/drain regions is called ***NMOS*** (the '686 Patent calls it "nMIS," or it may be called an "nFET" or "NMOSFET" or "NMISFET"), and one with ***p***-type source/drain regions is called ***PMOS*** (the '686 Patent calls it "pMIS," or it may be called a "pFET" or "PMOSFET" or "PMISFET"). Plummer, 12-13, 50-51, Figs. 1-11, 2-2. An

integrated circuit with both NMOS and PMOS devices is called ***CMOS*** ("Complementary MOS"), as on the right above. " Plummer, 12.

B. High-κ Gate Dielectrics

52. The International Technical Roadmap for Semiconductors ("ITRS") was a highly influential report published every two years for nearly two decades by a consortium of the world's leading academic and industry experts. The 2007 edition of the ITRS explains the status at the time:

> In no area is the issue of material-limited device scaling more clear or urgent than in the MOSFET gate stack. Here, a new gate dielectric material having a higher dielectric constant than SiO_2 is needed. This need was identified in the 1999 ITRS where it was linked to MOSFETs having gate lengths smaller than 65 nm, which were at that time expected to emerge in the year 2005. In the interim, the patterning technology for producing 65 nm gates has accelerated and these have been achieved in 2001. Combined with the extension of silicon oxynitride gate dielectric materials and the introduction of strain-enhanced-mobility channels, the need for high-κ had been delayed, but is now upon us. It is expected that leading manufacturers will start production of high-κ gate dielectrics in 2008. Mobility enhancement and channel-length scaling, which requires accelerated scaling of junctions to control short channel effects, will continue to provide enhanced device performance. In addition, the depletion layers that exist in the doped polysilicon gate material become more limiting as planar devices are scaled into the deep submicron region. Therefore, it is also expected that dual metal gates, having appropriate work functions, will be put in production by leading manufacturers in 2008 to replace the dual doped polysilicon gates, currently the mainstay of CMOS technology.

ITRS_FEP, 2. In fact, dual metal gates and high-κ gate dielectrics (also known as "high-k" gate dielectrics) were earlier than predicted, being released that same year in 2007. *See generally* Mistry2007 (announcing details of Intel's 45nm process); Mistry_Presentation (same).

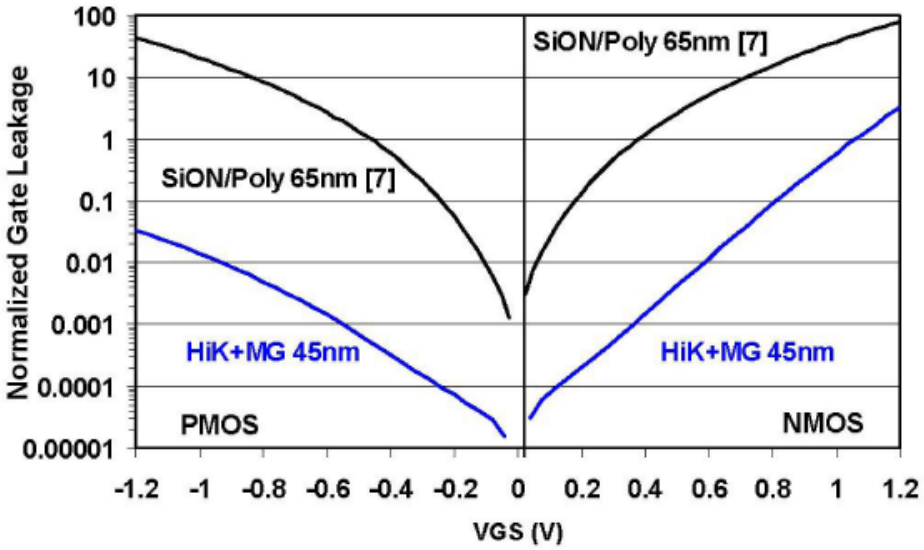
53. To provide a little more context, early MISFETs used silicon dioxide (SiO_2) gate dielectrics. Baklanov, xiii. As MISFETs became smaller due to industry forces and Moore's Law (a concise phrase used to describe the steady rate at which transistors shrank, beginning in the 1960s), gate dielectrics had to become thinner to increase gate capacitance, which allows for improved drive currents and reduced power consumption. Baklanov, xiii; ITRS_FEP, 2, 20; ITRS_PIDS, 1, 6, 8, 27, Fig. PIDS5; Akasaka939 ¶¶[0003]-[0004]. This eventually required gate dielectric layers only a few atoms thick, leading to increased gate leakage current, high power consumption, and reduced reliability. Baklanov, xiii; Akasaka939 ¶[0003]; Kavalieros ¶[0002]. To permit further scaling of MISFETs, the industry knew for many years (since the late 1990s) that alternative gate dielectrics were needed. By 2008, the industry had turned to so-called ***high-κ*** dielectrics. ITRS_FEP, 2, 20; ITRS_PIDS, 1, 6, 8, 27, Fig. PIDS5; Baklanov, xiii; Mistry2007, 247; Mistry_Presentation, 14-19; Akasaka939 ¶[0004].

54. High-k dielectrics have a larger ***dielectric constant κ*** (also called "relative permittivity") than SiO_2, which has a value of κ=3.9. Baklanov, xiii. This

means that, to achieve a given capacitance, high-κ dielectrics are thicker than SiO_2, leading to less gate leakage, lower power consumption, and better reliability than ultra-thin layers of silicon oxide. Baklanov, xiii. Common examples of high-κ dielectrics include Group IV-B metal oxides, most notably Hf-based oxides like hafnium oxide, hafnium silicon oxide, and hafnium silicon oxynitride, all of which may have a κ exceeding 10:

> [C]ertain films which are made of hafnium (Hf)-containing material such as HfO_2, $HfSiO_x$, or $HfAlO_x$, and oxynitrides thereof are relatively excellent in thermal stability. . . . A high dielectric constant film made of the above-noted high-k material has its dielectricity of more than ten (10), which is greater than SiO_2 film's dielectricity of 3.9.

Akasaka939 ¶[0004]; *see also* Kavalieros ¶[0002] (explaining that a "high-k dielectric means having a dielectric constant higher than 10"), ¶[0008] (similar); Baklanov, xiii ("Dielectrics with values approximately between 10 and 30 are under consideration."). Compared to devices with ultra-thin silicon oxide gate dielectrics, those with high-κ dielectrics (as the figure below shows) can exhibit gate leakage currents 25 times smaller in NMOS devices and 1,000 times smaller in PMOS devices. Mistry2007, 248, Fig. 7; Mistry_Presentation, 17.



Mistry2007's Fig. 7

C. Replacement Metal Gate MISFETs

55. In early MISFETs, the gate electrode was typically formed from polycrystalline silicon ("polysilicon"). ITRS_FEP, 2; Saito, 1:24-26. When polysilicon is used, a depletion region (a region where mobile charges have diffused away, leaving behind a region with fixed, ionized impurities that effectively create an insulating barrier that hinders current flow) forms at the interface of the polysilicon and the gate dielectric and, as a result, increases resistance and decreases transistor drive current. Saito, 1:26-31; Hou, 1:25-35; Colombo ¶[0004]. As gate dielectrics became thinner to make MISFETs smaller (due to Moore's Law), this reduction in drive current worsened and eventually became intolerable. Saito, 1:31-34; Hou, 1:36-44; '686 Patent, 1:23-27. Moreover, when a high-κ gate dielectric is used with a polysilicon gate electrode, a large threshold voltage offset develops because polysilicon dopants diffuse into the high-κ layer. Colombo ¶[0005];

Kavalieros ¶[0003]. To address these issues, the industry began adding metals to the gate electrodes. Saito, 1:31-34; Iriyama, 1:28-34, 1:41-42; ITRS_FEP, 2-3, 20; ITRS_PIDS, 1, 3, 27, Fig. PIDS5.

56. In CMOS devices, threshold voltage is minimized by adjusting the ***work functions***[8] of nFET and pFET gate electrodes. Hou, 1:17-22; Colombo ¶[0020]. PMOS devices require a work function to be close to the conduction band edge of silicon (e.g., greater than about 4.8 eV). NMOS devices require adjusting the work function to be close to the valence band edge of silicon (e.g., less than about 4.6 eV). Hou, 1:17-22; Colombo ¶¶[0020]-[0021]; ITRS_FEP, Tbl. FEP4a ($|E_{c,v}-\varphi_m|$ (eV) < 0.2). Polysilicon can be doped n-type or p-type, which allows the work function to be adjusted accordingly. The same is not true of metals.

57. This is why nFET and pFET devices call for different gate metals. Kavalieros ¶[0003]. Suitable metals for nFETs were known, but many metals with appropriate work functions for pFETs exhibited less thermal stability, making them unable to withstand the high temperatures used to activate dopants in the source/drain regions. Hou, 1:45-48; Iriyama, 1:41-48.

58. A solution to this problem was to use ***replacement metal gates ("RMG")***, which is a "gate-last" approach, opposed to what had been the more

[8] The ***work function*** of a material is the minimum energy required to bring an electron from the Fermi level to the vacuum level.

conventional way of making the gate first. As the figures below illustrate, the RMG approach avoids subjecting the metal gates to high temperatures. As shown, source/drain regions (107), a polysilicon ***dummy gate*** (105), a SiN film (106), and ***sidewalls*** (108) are formed for each NMOS and PMOS device. Matsuo ¶¶[0009]-[0010], ¶[0016], FIG. 3A.

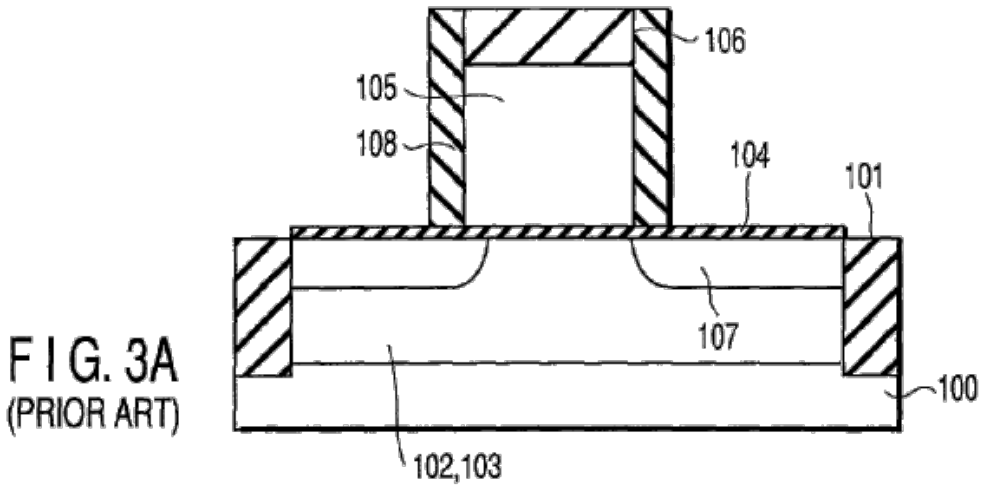


FIG. 3A
(PRIOR ART)

Matsuo's FIG. 3A

59. The source/drain regions are then doped, and high temperatures are applied to activate the source/drain regions. Matsuo ¶[0010], FIGS. 3B, 3C; *see also* Hou, 2:8-11; Iriyama, 1:59-2:6. As the figure below illustrates, the dummy gates are eventually removed near the conclusion of the front-end device processing sequence. Matsuo ¶¶[0011]-[0013], FIG. 3D.

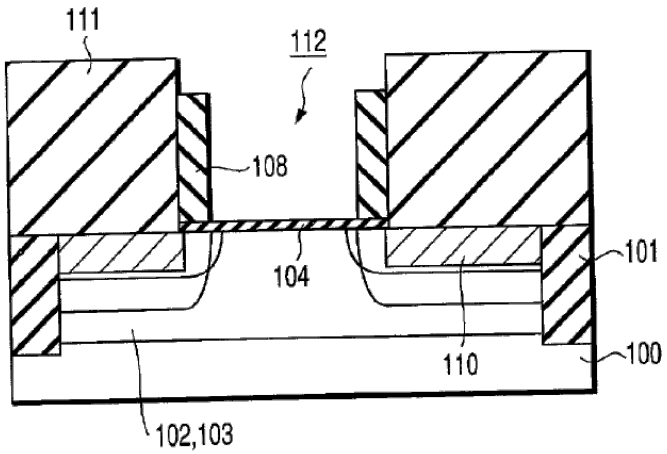


FIG. 3D
(PRIOR ART)

Matsuo's FIG. 3D

60. Subsequently, NMOS and PMOS gate electrodes are formed, as shown below. Matsuo ¶¶[0012]-[0016], FIG. 3J. Gate dielectric (113) is formed, followed by metal layers 114, 116, and 117. Matsuo ¶¶[0012]-[0016]. Because these steps occur after applying the high temperatures necessary to activate the source/drain dopants, metals with less thermal stability can be used without subjecting them to those high temperatures. Iriyama, 2:22-29.

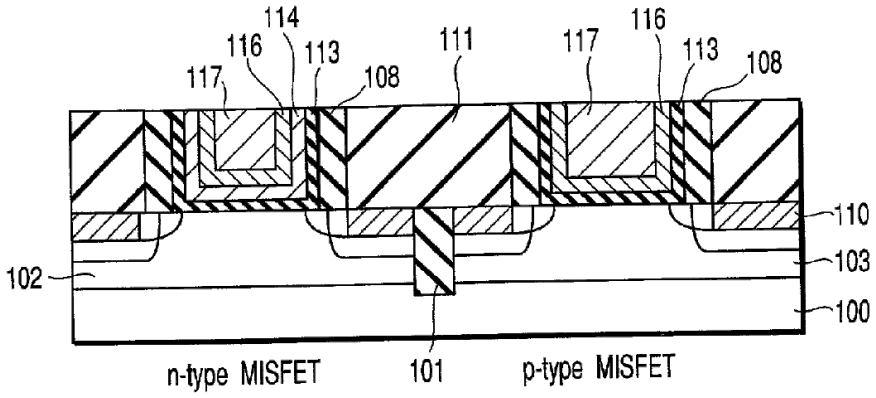


FIG. 3J
(PRIOR ART)

Matsuo's FIG. 3J

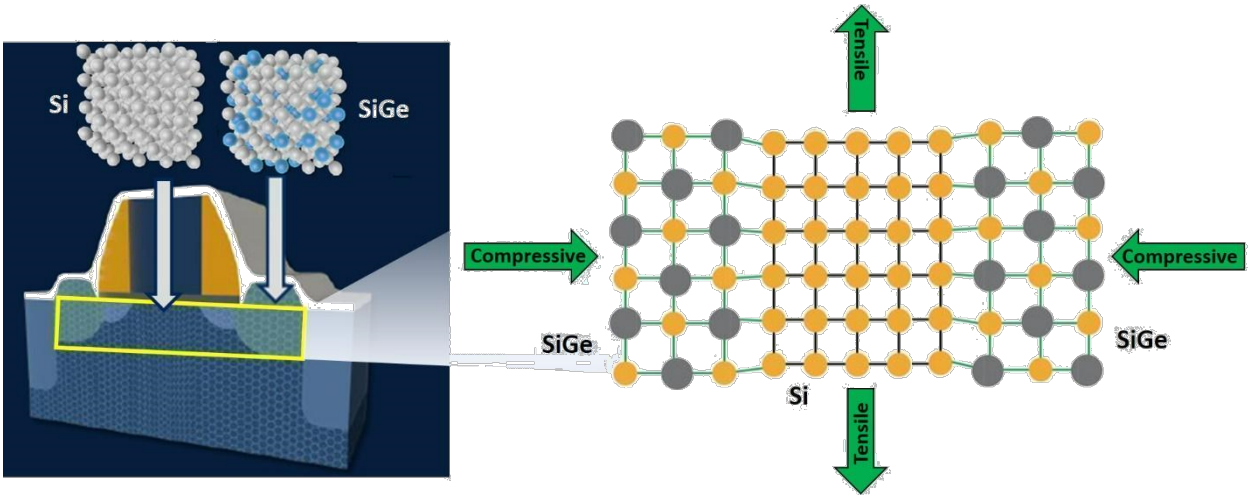
61. As shown above, metal layer 114 covers the gate dielectric 113 in the NMOS gate electrode (left), whereas the PMOS gate electrode (right) does not include metal layer 114. Matsuo ¶[0021]. The NMOS and PMOS gates thus have different metal work functions, one optimized for NMOS and one optimized for PMOS. Matsuo ¶[0021], FIG. 3J; Hou, 2:11-14; Iriyama, 2:10-12; Mistry2007, 247; Mistry_Presentation, 16, 18.

62. So, to briefly summarize, high-κ dielectrics were a necessity, but traditional gate electrodes consisting essentially of doped polysilicon were incompatible with high-κ dielectrics. To control NMOS and PMOS threshold voltages independently, metal gates were required to replace doped polysilicon gates. And because certain metal gates could not tolerate the processing temperatures used to activate source/drain dopants, the metal gates needed to be formed at the end of the process rather than at the beginning, e.g., using an RMG process. The industry knew this transition was coming, and it went into mass production before the application for the ’686 Patent was filed.

D. Strained Silicon Technology

63. PMOS was once much slower than NMOS until SiGe/Strained-Silicon technology changed that. Because Ge atoms are larger than Si atoms, epitaxial silicon-germanium (“SiGe,” i.e., $Si_{1-x}Ge_x$) source/drain regions ***compressively*** strain the Si channel region along the direction of current flow (i.e., left to right in the

illustrations below). In PMOS, such compressive strain improves carrier (hole) mobility and boosts operating speed. Thompson2004, 1790-96; Sun, 2. By 2005, compressively strained epitaxial SiGe source/drain regions had increased PMOS "hole mobility by as much as 50%" (James, 2) and had doubled PMOS operating speeds.



64. Strained-silicon technology has a long history and was well known before March 13, 2008, as the '686 Patent acknowledges. *See* Sun, 1-2; '425 Patent, 1:23-2:62, FIGS. 8A-10C. At least three generations of high-volume commercial devices already used it by 2007. *See* Thompson2004, 1790-91 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry2007, 247-48 (describing Intel's 45nm devices); Mistry_Presentation, 1-19 (same).

65. The same strain engineering principles apply to NMOS, except that improving carrier (electron) mobility in NMOS requires ***tensile*** strain instead of ***compressive*** strain along the current-flow direction. *See* Murthy151 ¶[0005],

¶[0048], ¶[0072]; James, 2. Creating tensile strain with epitaxial source/drain regions requires using an atom smaller than silicon, such as carbon, to grow a material like silicon carbide (SiC) instead of SiGe, which was also known. *See* Murthy151 ¶[0005], ¶[0048], ¶[0072]; James, 2; Bohr683 ¶[0045].

66. As an alternative or supplement to source/drain epitaxy, by 2008, the semiconductor industry was also already depositing compressive or tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain. *See* James, 2, 4; Morin, 355-56, 367; Hsu823 ¶[0003]; Jung, Abstract, ¶[0090] ("In addition to being deposited as part of a structure to control electron mobility, . . . a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer . . . ."). Most commonly, a contact etch stop layer ("CESL") made of silicon nitride was used. If prepared under certain conditions, a silicon nitride CESL may be "used . . . for applying stress to [a] channel region" to improve carrier mobility. Hsu823 ¶[0003]; *see also* Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Jung ¶[0090] ("In addition to being deposited as part of a structure to control electron mobility, . . . a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device

structure."); Morin, 355-56. Depending on how such a silicon nitride CESL is prepared, it may provide tensile stress, compressive stress, or no stress at all. *See, e.g.*, Jung ¶[0017], ¶¶[0099]-[0100], ¶¶[0131]-[0132], Tbls. IV-V, VII, Fig. 15.

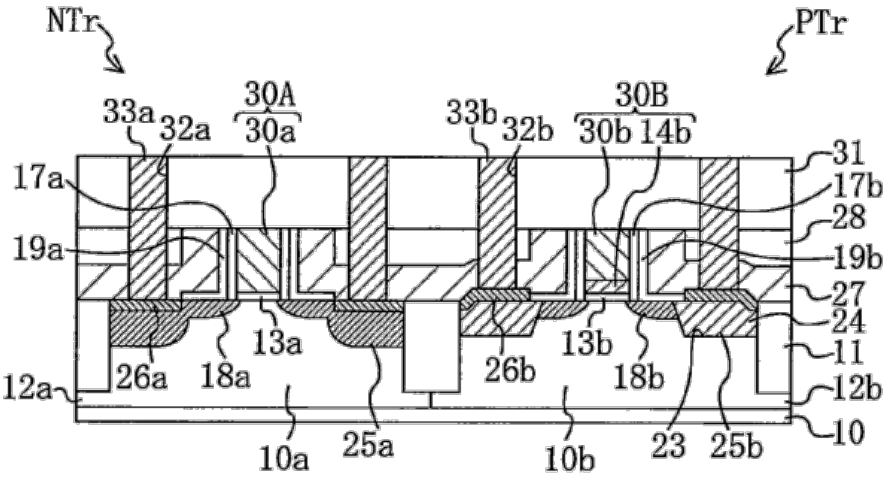
VII. The '686 Patent

A. A Description of the Claimed Embodiments of the '686 Patent

67. The '686 Patent describes "a semiconductor device including n- and p-type MIS transistors having gate electrodes made of different metal materials." '686 Patent, 5:39-45. FIG. 5C below illustrates one embodiment.

68. As shown below, the device includes an nMIS transistor (NTr) and a pMIS transistor (PTr). '686 Patent, 16:55-60. The nMIS transistor includes a gate insulating film (13a) and a first gate electrode (30A) that includes a metal film (30a) formed on the gate insulating film. '686 Patent, 16:16-22. The pMIS transistor includes a gate insulating film (13b) and a second gate electrode (30B) that includes a metal film (14b) and a conductive film (30b). '686 Patent, 16:16-22. Insulative sidewall spacers (17a/19a, 17b/19b) line the outer surfaces of each gate electrode. '686 Patent, 12:50-63. As shown below, sidewalls 19a/19b have an L-shaped cross-section, and an insulating film (27) and inter-layer insulating film (28) fill the space between the gates. '686 Patent, 14:51-15:5, FIG. 4A.

FIG. 5C



'686 Patent's FIG. 5C

NTr:	nMIS transistor	**PTr:**	pMIS transistor
13a:	gate insulating film	**13b:**	gate insulating film
30A:	first gate electrode	**30B:**	second gate electrode
30a:	metal film	**14b:**	metal film
		30b:	conductive film
17a:	insulative sidewall spacer	**17b:**	insulative sidewall spacer
19a:	insulative sidewall spacer	**19b:**	insulative sidewall spacer

nMIS & pMIS Transistors

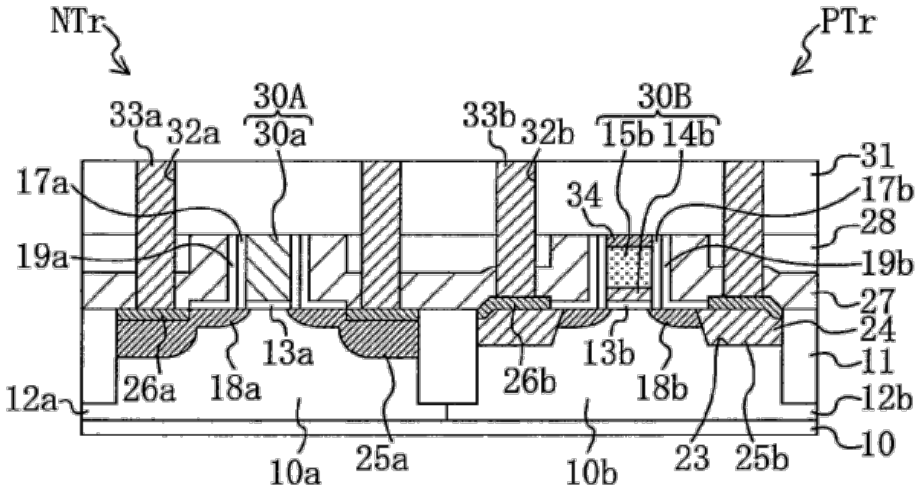
27: insulating film **28:** inter-layer insulating film

69. The gate insulating films (13a/13b) may be formed of the same or of different materials. In some embodiments, the gate insulating films (13a/13b) are a high-κ metal-oxide having a relative dielectric constant *k* of 10 or more. '686 Patent, 11:31-37, 29:16-24. As examples, the '686 Patent identifies "hafnium-based oxides

such as hafnium oxide (HfO_2), hafnium silicate (HfSiO), and hafnium silicon oxynitride (HfSiON) and the like." '686 Patent, 29:16-24. As shown above, the insulating film (27), made of silicon nitride, for example, does not lie on any upper surface of the gate electrodes, because the wafer has been planarized. '686 Patent, 6:42-45, 14:65-15:30.

70. In some embodiments, as FIG. 5C shows above, the conductive film (30b) in the pMIS gate electrode (30B) may be a metal film formed of the same material as the metal film (30a) in the nMIS gate electrode (30A). This is because they are formed by patterning the same layer. '686 Patent, 15:64-16:22, FIGS. 5A-5C. In other embodiments, as FIG. 8C shows below, the conductive film (15b) in the pMIS gate electrode (30B) is silicon. '686 Patent, 21:61-67, FIGS. 7A-8C. In this embodiment, a metal silicide film (34) is formed on the silicon film (15b). '686 Patent, 22:33-41, FIG. 8C.

FIG. 8C



'686 Patent's FIG. 8C

71. Additionally, the ’686 Patent describes causing stress in the first and second active regions (10a/10b). ’686 Patent, 28:63-29:15. In the second active region (10b), for example, a silicon mixed crystal layer (24) (e.g., SiGe) may be formed in the trenches (23) to cause compressive stress in the gate length direction of the channel region. ’686 Patent, 13:60-65, 19:54-61, 23:28-33. In the first active region (10a), the insulating film (27) causes tensile stress in the gate length direction of the channel region. ’686 Patent, 28:16-43.

B. Prosecution History

72. The Prosecution File History of the ’686 Patent (“’686 File History”) includes four rounds of office actions and amendments. *See generally* ’686 File History.

73. In a first office action, the Examiner rejected original claims 1-14 for various reasons, including rejection of claims 1-4 and 7 based on Aoyama’s first embodiment (Figs. 1-2N).[9] ’686 File History, 201-06. In response, the Applicant amended claim 1 to recite: “the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region.” ’686 File History, 213. According to the Applicant, this feature distinguished

[9] The Examiner never cited or relied on Aoyama’s third embodiment relied on in this Petition (FIGS. 5-6Q). *See* Section VIII.A below.

Aoyama from claim 1. '686 File History, 227. The Applicant also added various new claims 21-50. '686 File History, 218-26.

74. In a second office action, the Examiner cited different art—the Hou reference—to reject most of the new and amended claims. '686 File History, 236. In response, the Applicant amended claim 1 to further recite: "the insulating film has a thickness smaller than that of the first gate electrode." '686 File History, 246.

75. In a third office action, the Examiner cited the Hou reference again, this time in combination with another reference, to reject pending claims 31-33 and 38. '686 File History, 268. In response, the Applicant amended the claims considerably, including by reciting additional spacers and specific material requirements for various features. '686 File History, 274-75.

76. In a fourth office action, the Examiner took issue with several informalities but otherwise indicated that the claims would be allowed if the Applicant resolved those issues. '686 File History, 294-95. The Applicant complied ('686 File History, 310), and the claims were allowed ('686 File History, 319). After correcting another informality in the claims, they issued. '686 File History, 329, 354.

C. Challenged Claims

77. Independent claim 19 is the broadest claim. It is best understood with reference to the embodiments described with respect to FIGS. 1A-6B. Claim 19 recites "[a] semiconductor device" that includes "a first MIS transistor" and a

"second MIS transistor," each of which includes a "gate insulating film" that includes a "high-k film made of oxide containing hafnium and silicon"; a metal "gate electrode"; and "sidewall spacers." A "silicon nitride film" extends "over the side surfaces of" the gate electrodes but "is not formed on any of [the] upper surfaces of the" gate electrodes. Claim 19 recites the following:

19. A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

the first metal film is made of titanium nitride.

78. Independent claim 1 is similar to claim 19, except the second MIS transistor has "source/drain regions" that "include a silicon mixed crystal layer which . . . causes first stress" in an "active region" of the second MIS transistor, and the silicon nitride film "has a thickness smaller than that of" the gate electrode of the first MIS transistor. Claim 1 recites the following, with the changes relative to claim 19 highlighted:

1. A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; ~~and~~

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers~~,~~; and

source/drain regions formed in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, ~~and~~

~~the first metal film is made of titanium nitride.~~ the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and

the silicon nitride film has a thickness smaller than that of the first gate electrode.

79. Independent claim 11 is similar to claim 19, except the "gate insulating film[s]" are not required to include a "high-k film made of oxide containing hafnium and silicon," and claim 11 additionally recites that the "conductive film" of the second MIS transistor "is made of a silicon film"; the second MIS transistor includes "a metal silicide film formed on the silicon film"; and the silicon nitride film "has a thickness smaller than that of" the gate electrode of the first MIS transistor. Claim 11 recites the following, with the changes relative to claim 19 highlighted:

11. A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate~~, and including a first high-k film made of oxide containing hafnium and silicon~~;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, ~~and including a second high-k film made of oxide containing hafnium and silicon;~~

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, ~~and~~

the ~~first metal~~ conductive film is made of ~~titanium nitride~~ a silicon film,

the semiconductor device further comprises a metal silicide film formed on the silicon film, and

the silicon film has a thickness smaller than that of the first gate electrode.

80. Independent claim 25 is similar to claim 19, except the "gate insulating film[s]" are not recited to include a "high-k film made of oxide containing hafnium and silicon," and "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region."

25. A semiconductor device comprising:

a first MIS transistor; and

a second MIS transistor, wherein:

the first MIS transistor includes:

a first gate insulating film formed on a first active region in a semiconductor substrate~~, and including a first high-k film made of oxide containing hafnium and silicon~~;

a first gate electrode including a second metal film formed on the first gate insulating film;

first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

the second MIS transistor includes:

a second gate insulating film formed on a second active region in the semiconductor substrate, ~~and including a second high-k film made of oxide containing hafnium and silicon;~~

a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and

the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,

the first and second metal films are made of different metal materials,

the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and

~~the first metal film is made of titanium nitride.~~ the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

81. Dependent claims 2, 12, 20, and 26 recite that "the first metal film has a thickness smaller than that of the second metal film."

82. Dependent claims 3, 13, 21, and 27 recite that "the first and second metal films have different work functions."

83. Dependent claims 4 and 29 recite that "the conductive film is made of the second metal film."

84. Dependent claims 5 and 30 recite that "the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film."

85. Dependent claims 6, 14, and 31 recite that "the first and second gate insulating films are made of the same insulating material."

86. Dependent claims 15 and 32 recite that "the first and second gate insulating films are made of different insulating materials."

87. Dependent claims 7, 16, 23, and 33 recite that "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape."

88. Dependent claim 8 recites that "the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region."

89. Dependent claim 9 recites that "the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress."

90. Dependent claim 10 recites that "the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress."

91. Dependent claims 17, 24, and 34 recite "source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region."

92. Dependent claims 18 and 35 recite that "the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more."

93. Dependent claims 22 and 28 recite that "the silicon nitride film has a thickness smaller than that of the first gate electrode."

D. Claim Construction

94. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent document. In my analysis of the Challenged Claims, I have therefore applied the meanings of the claim terms as understood by a person of ordinary skill in the art in the context of the asserted patent and asserted claims.

95. In forming my opinions, I do not believe that any express constructions are required because the prior art teaches substantially the same teachings as the '686 Patent's disclosures.

96. If Patent Owner offers constructions of any terms, I reserve the right to address those constructions at a future time.

VIII. Descriptions of Asserted Prior Art References

A. Overview of Aoyama

97. Aoyama (U.S. Patent Appl. Pub. No. 2007/0215950) published on September 20, 2007, from an application filed March 19, 2007. I have been told this qualifies Aoyama as prior art.

98. In my opinion, Aoyama is analogous art to the ’686 Patent because Aoyama is in the same field of endeavor as the ’686 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* ’686 Patent, 1:14-20; Aoyama ¶¶[0002]-[0003]. In my opinion, Aoyama is also analogous art to the ’686 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’686 Patent addresses, for example, fabricating semiconductor devices with high-κ/metal-gate structures. *See* ’686 Patent, 1:14-50, 11:31-37; Aoyama ¶¶[0002]-[0003].

99. Aoyama describes three embodiments, each of which uses a replacement metal gate (“RMG”) approach to form the gate electrodes. My declaration focuses on the third embodiment (Aoyama, ¶¶[0097]-[0121], FIGS. 5-6Q), as illustrated below. Aoyama’s FIG. 5 (annotated below) illustrates Aoyama’s NMOS on the left side in NMOSFET (i.e., nFET) region 106 and Aoyama’s PMOS on the right side in PMOSFET (i.e., pFET) region 105. Aoyama ¶¶[0097]-[0121], FIGS. 5-6Q.

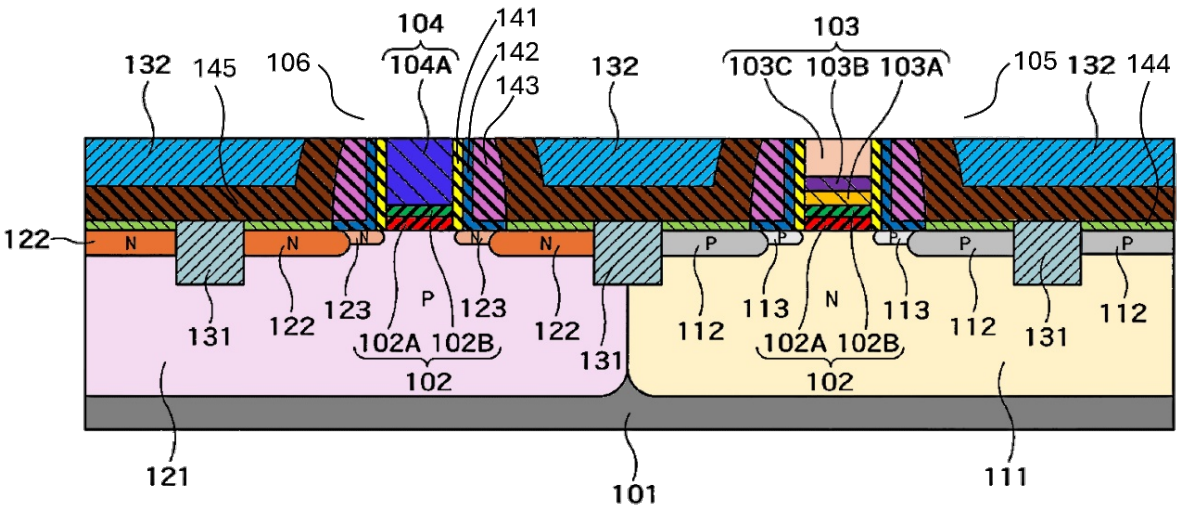


FIG. 5

Aoyama's FIG. 5 (annotated)

100. Both NMOS and PMOS devices include an interfacial silicon oxide dielectric layer 102A, a high-κ gate dielectric layer 102B, and gate sidewall spacers 141, 142, and 143. Aoyama ¶[0098], ¶[0111]. But the NMOS and PMOS gate structures differ above the high-κ gate dielectric. The PMOS gate electrode 103 comprises a first conductive layer 103A (e.g., W), a second conductive layer 103B (e.g., TiN), and a semiconductor layer (silicide layer) 103C (e.g., polysilicon capped with NiSi). Aoyama ¶[0107], ¶[0114], ¶[0121]. The NMOS gate electrode 104, however, comprises only a third conductive layer 104A (e.g., TaCN). Aoyama ¶[0118]. The spaces between Aoyama's NMOS and PMOS gate structures are filled with a silicon nitride etch stopper 145 and a silicon oxide interlayer dielectric 132. Aoyama ¶[0113].

B. Overview of Akasaka

101. Akasaka (U.S. Patent Appl. Pub. No. 2007/0066077) published on March 22, 2007, from an application filed September 20, 2006. I have been told this qualifies Akasaka as prior art.

102. In my opinion, Akasaka is analogous art to the '686 Patent because Akasaka is in the same field of endeavor as the '686 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '686 Patent, 1:14-20; Akasaka ¶¶[0002]-[0003]. In my opinion, Akasaka is also analogous art to the '686 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '686 Patent addresses, for example, fabricating semiconductor devices with high-κ/metal-gate structures. *See* '686 Patent, 1:14-50, 11:31-37; Akasaka ¶¶[0002]-[0007].

103. As illustrated below, Akasaka describes p-type MISFET and n-type MISFET devices formed using an RMG approach to form the gate electrodes. Akasaka, FIG. 26 (annotated below). The left side of FIG. 26 illustrates Akasaka's pFET 301A, and the right side of the image illustrates Akasaka's nFET 301B. Akasaka ¶[0072], FIG. 26.

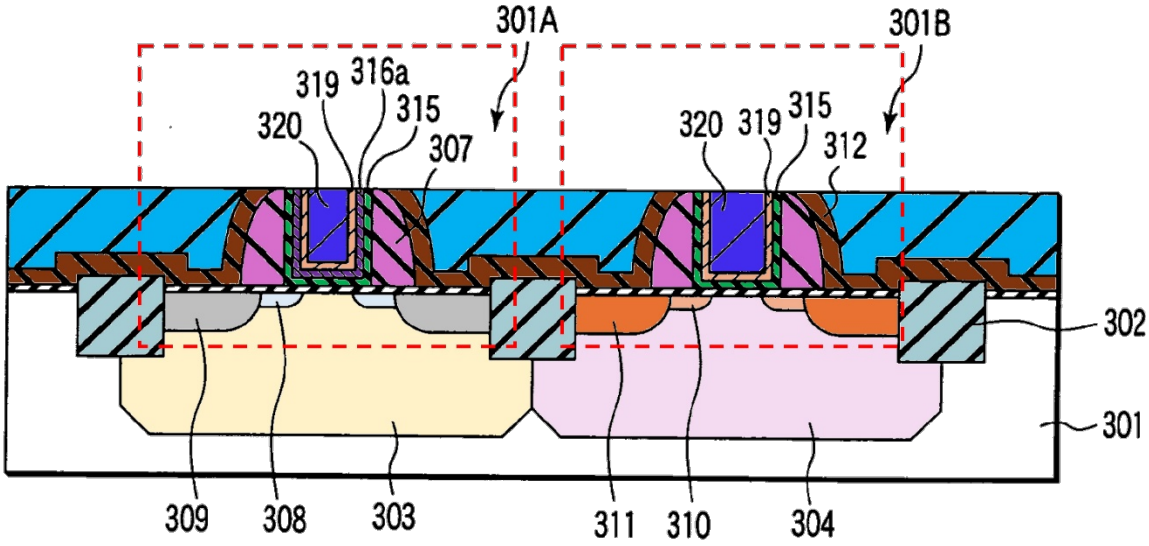


FIG. 26

Akasaka's FIG. 26 (annotated)

104. The pFET and nFET each use a gate dielectric 315 (e.g., hafnium silicon oxide). Akasaka ¶[0075]. Above the gate dielectric, the nFET gate electrode comprises conductive films 319 and 320. Akasaka ¶¶[0084]-[0086]. Conductive film 319 "has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon," and conductive film 320 may be tungsten. Akasaka ¶¶[0085]-[0086] (emphasis added). The pFET gate electrode additionally comprises conductive film 316, which "has a metallic band structure with a work function close to that of p^+-poly-crystalline silicon" (e.g., TiN). Akasaka ¶¶[0076]-[0077] (emphasis added). The spaces between the nFET and pFET gate structures are filled with a silicon nitride film 312 and an inter-level insulating film 313. Akasaka ¶[0073].

C. Overview of Hsu823

105. Hsu823 (U.S. Patent Appl. Pub. No. 2007/0235823) published on October 11, 2007, from an application filed March 30, 2006. I have been told this qualifies Hsu823 as prior art.

106. In my opinion, Hsu823 is analogous art to the ’686 Patent because Hsu823 is in the same field of endeavor as the ’686 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* ’686 Patent, 1:14-20; Hsu823 ¶[0001]. In my opinion, Hsu823 is also analogous art to the ’686 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’686 Patent addresses, for example, fabricating strain-engineered semiconductor devices with SiGe source/drain regions and strain-inducing CESL. *See* ’686 Patent, 1:14-50, 13:33-50, 28:10-56; Hsu823 ¶[0033], ¶[0036].

107. Hsu823 explains that “[w]hen devices become smaller, the distance between devices decreases,” and this leads to a “gap-filling problem” (also known as voiding), as FIG. 1 below illustrates. Hsu823 ¶[0004]. To address this problem, as FIG. 15A below shows, Hsu823 teaches to use an L-shaped spacer liner made of silicon oxide and a spacer made of silicon nitride. Hsu823 ¶[0031], ¶[0035], FIGS. 6, 15A. After using the silicon nitride spacer to define source/drain regions, Hsu823 teaches that the outer spacer may be removed, leaving only the L-shaped spacer liner as in FIG. 15B below. Hsu823 ¶[0035], FIGS. 9, 15B. By adopting this technique,

Hsu823 explains that "gap-filling is improved and the contact etching process can be better controlled." Hsu823 ¶¶[0042]-[0043].

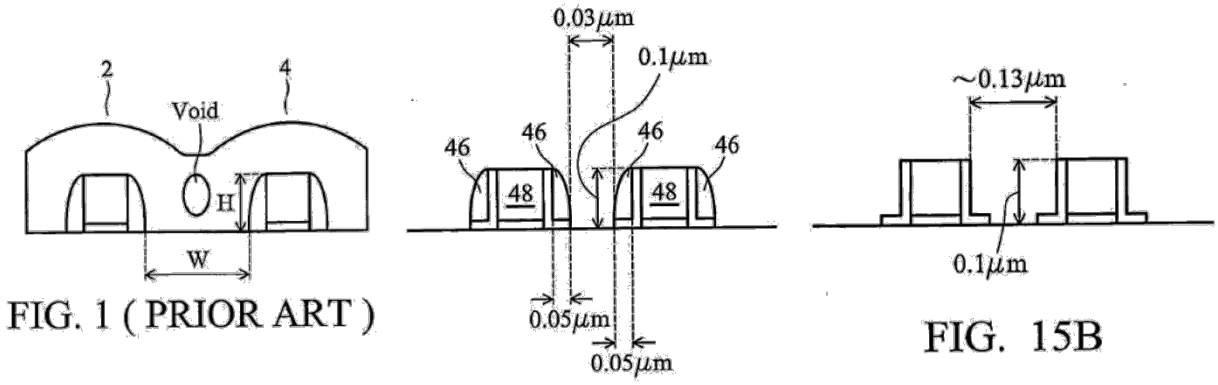


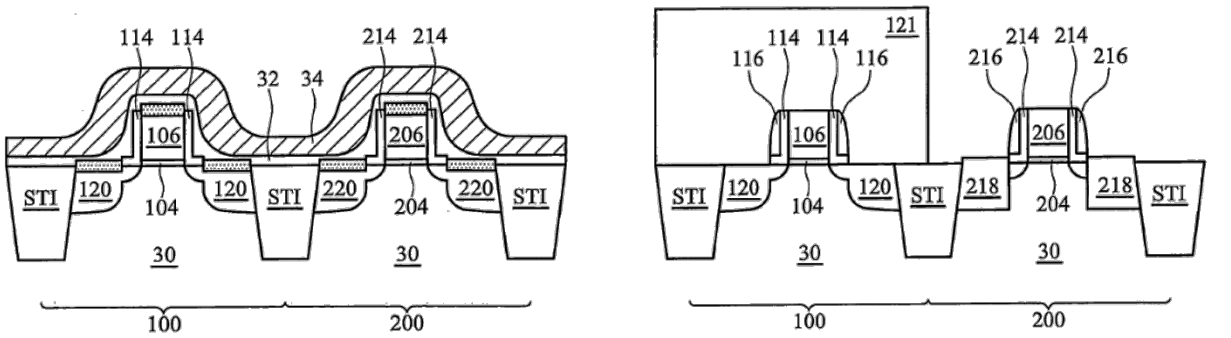
FIG. 1 (PRIOR ART)

FIG. 15A

FIG. 15B

Hsu823's FIGS. 1, 15A, and 15B

108. Using this technique, Hsu823 discloses MISFETs like the exemplary one illustrated below on the left. Hsu823, FIG. 10. According to Hsu823, a "dielectric layer 32 is optionally formed," meaning it may be omitted (*see* Hsu823 ¶[0036])—an option on which I rely when discussing Aoyama's claims 7, 16, 23, and 33. In such an embodiment, a contact etch stop layer (CESL) 34 directly contacts L-shaped spacer liners 114/214 and boosts channel stress. *See* Hsu823 ¶[0015], ¶[0036], FIGS. 9, 14. For example, Hsu823 teaches a CESL 34 that exerts tensile stress on both NMOS and PMOS devices. Hsu823 ¶¶[0036]-[0037].



Hsu823's FIGS. 10 and 7B

109. Additionally, Hsu823 teaches that the PMOS source/drain regions (labeled 220 in FIG. 10 on the left above) may be formed using epitaxial SiGe (labeled 218 in FIG. 7B on the right above). Hsu823 ¶¶[0032]-[0033], FIGS. 7A-7B. In this technique, which was well known by 2008 (*see* Section VI.D above), a recess etch is performed to open cavities in the source/drain regions of the substrate, and those cavities are filled by growing epitaxial SiGe. Hsu823 ¶[0033], FIG. 7B. "This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased." Hsu823 ¶[0033].

D. Overview of Hobbs

110. Hobbs (U.S. Patent No. 6,171,910) issued on January 9, 2001, from an application filed July 21, 1999. I have been told this qualifies Hobbs as prior art.

111. In my opinion, Hobbs is analogous art to the '686 Patent because Hobbs is in the same field of endeavor as the '686 Patent (semiconductor devices and

methods for fabricating semiconductor devices, including MISFETs). *See* '686 Patent, 1:14-20; Hobbs, 1:19-22. In my opinion, Hobbs is also analogous art to the '686 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '686 Patent addresses, for example, fabricating semiconductor devices with metal gate structures and different pFET and nFET gate dielectric films. *See* '686 Patent, 1:14-50, 18:25-33, 27:32-36; Hobbs, 1:19-22, 1:50-67.

112. Hobbs discloses an RMG process in which both polysilicon dummy gates ***and*** dummy gate dielectrics are removed and replaced. As FIG. 5 shows below, dummy structures 201 and 202 are formed, each of which includes a polysilicon layer 164 overlying a dielectric layer 162. Hobbs, 3:19-23, 3:47-51, 8:35-45.

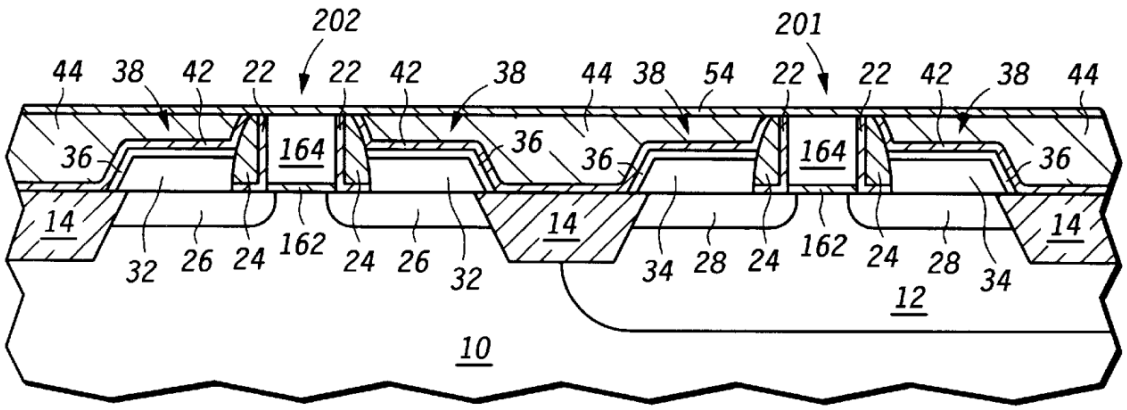


FIG. 5

Hobbs's FIG. 5

113. As FIGS. 6-10 show, Hobbs discloses removing both polysilicon layer 164 and dielectric layer 162 of the dummy structures 201 and 202. Hobbs,

4:42-44, 4:60-62, 5:52-56. Hobbs explains that this process allows for "different gate dielectric materials and thickness[es] as well as different gate materials [to] be selected to form . . . various transistors with different threshold voltages and operating characteristics." Hobbs, 8:40-45.

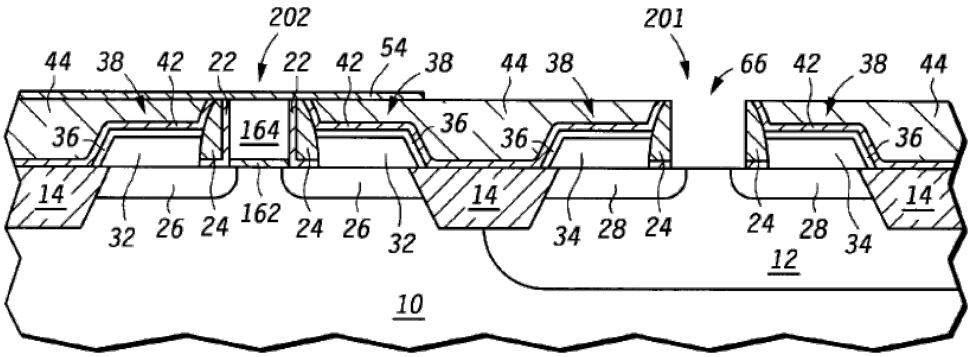


FIG.6

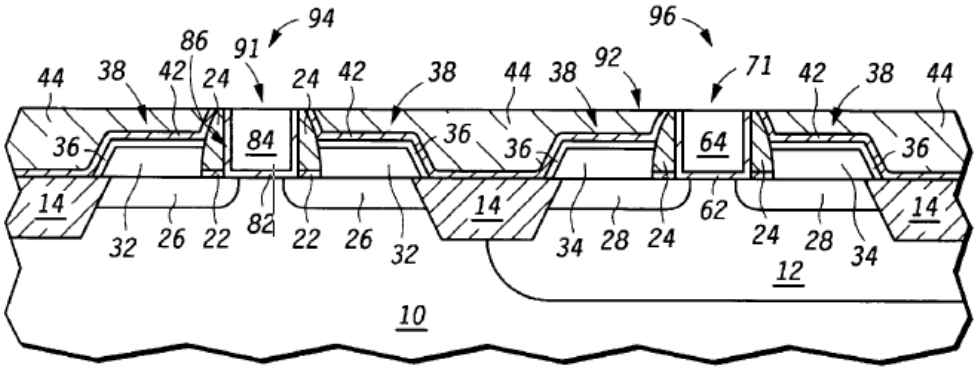


FIG.10

Hobbs's FIGS. 6 and 10

IX. Claims 1-35 of the '686 Patent Are Unpatentable

114. By March 13, 2008, structures like the ones described in the '686 Patent were already known and used extensively throughout the semiconductor industry. *See, e.g.*, *generally* Mistry2007; Mistry_Presentation. Because the relevant

principles and structures were already thoroughly established and widely known, a person of ordinary skill in the art would have found the claimed structures in the '686 Patent obvious. The following sections explain why in greater detail, and the chart below summarizes the grounds I address.

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	19-22	102	Aoyama
1B	11-15, 18-22	103	Aoyama
1C	1-3, 5-10, 16-17, 23-28, 30-35	103	Aoyama, Hsu823
1D	15	103	Aoyama, Hobbs
1E	32	103	Aoyama, Hsu823, Hobbs
2A	19-22	102	Akasaka
2B	19-22	103	Akasaka
2C	1-4, 6-10, 23-29, 31, 33-35	103	Akasaka, Hsu823
2D	32	103	Akasaka, Hsu832, Hobbs

A. Grounds 1A and 1B: Aoyama Anticipates (Ground 1A) or at Least Renders Obvious (Ground 1B) Claims 19-22

1. Independent Claim 19

a. [19Pre]: "A semiconductor device"

115. Aoyama discloses "[a] semiconductor device."

116. Aoyama "relates to a semiconductor device and a manufacturing method thereof, for example, to a semiconductor device which includes a PMOSFET and an NMOSFET which are constituted by high-permittivity gate dielectric films

(high-k gate dielectric films) and metal gate electrodes, and a manufacturing method thereof." Aoyama ¶[0003]. Aoyama's "FIG. 5 is a side sectional view showing a semiconductor device according to a third embodiment," which is the embodiment I discuss for purposes of my analysis of Aoyama in this declaration. Aoyama ¶[0097]; *see also* Aoyama, FIG. 5.

117. For the same reasons I explain above, a POSITA also would have found "[a] semiconductor device" obvious in view of Aoyama.

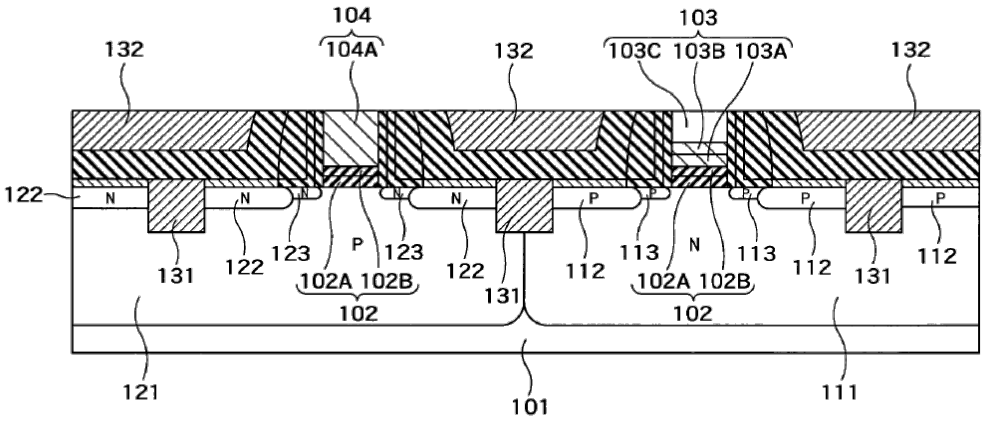


FIG. 5

Aoyama's FIG. 5

b. [19A]: "a first MIS transistor"

118. Aoyama discloses "a first MIS transistor."

119. Aoyama's FIG. 5 device includes "a NMOSFET region 106," which "is a region where the NMOSFET is to be formed." Aoyama ¶[0106]; *see also* Aoyama, FIGS. 5, 6D. Aoyama's NMOSFET (i.e., nFET) includes features [19C]-[19F], as I further explain below.

120. For the same reasons I explain above, a POSITA also would have found "a first MIS transistor" obvious in view of Aoyama.

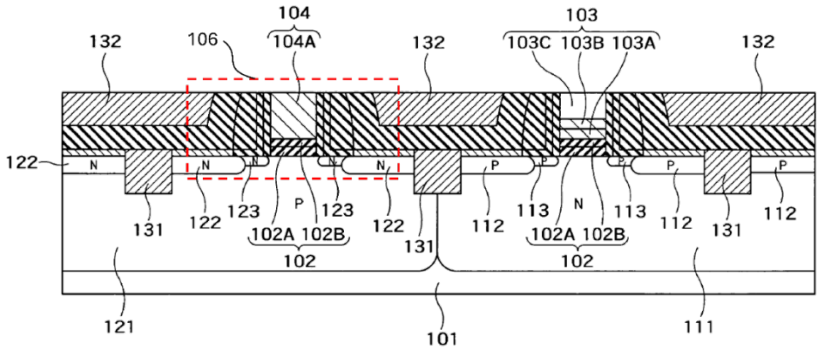


FIG. 5

Aoyama's FIG. 5 (annotated)

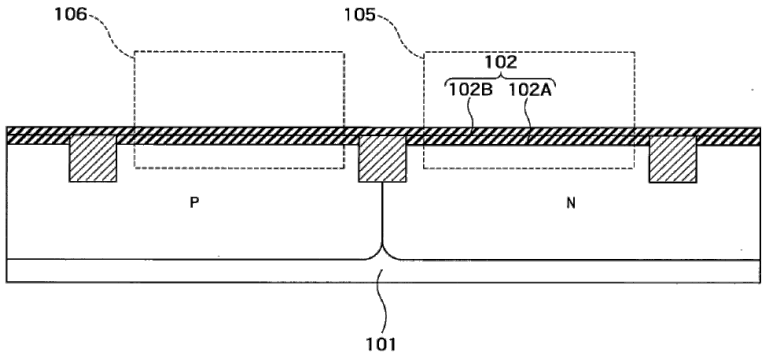


FIG. 6D

Aoyama's FIG. 6D

c. [19B]: "a second MIS transistor"

121. Aoyama discloses "a second MIS transistor."

122. Aoyama's FIG. 5 device includes a "PMOSFET region 105," which "is a region where the PMOSFET is to be formed." Aoyama ¶[0106]; *see also* Aoyama, FIGS. 5, 6D. Aoyama's PMOSFET (i.e., pFET) includes features [19G]-[19J], as I further explain below.

123. For the same reasons I explain above, a POSITA also would have found "a second MIS transistor" obvious in view of Aoyama.

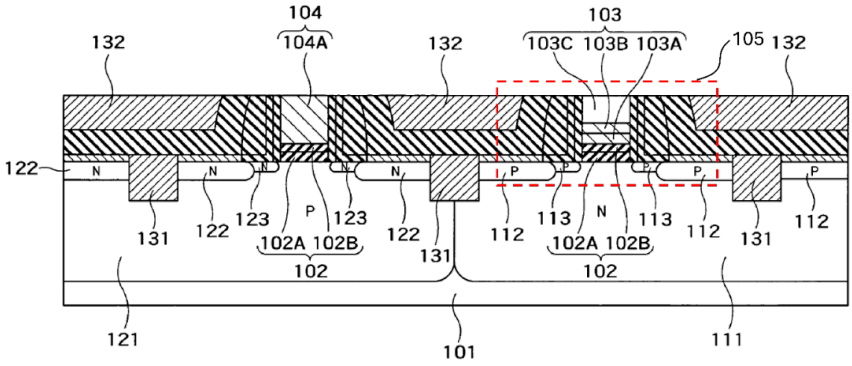


FIG. 5

Aoyama's FIG. 5 (annotated)

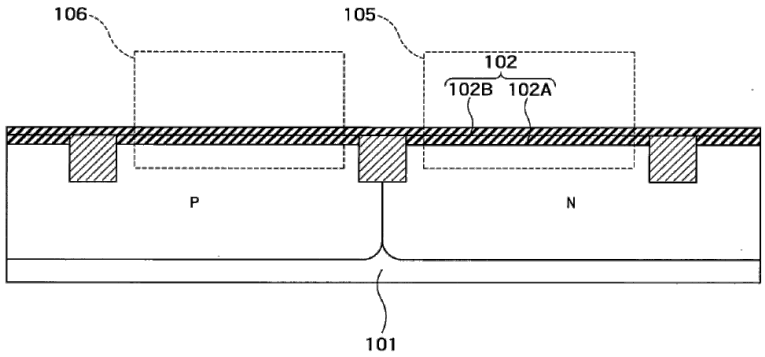


FIG. 6D

Aoyama's FIG. 6D (annotated)

d. [19C]: "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon"

124. Aoyama discloses that "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon."

125. Aoyama's "first MIS transistor" (the nFET in region 106) includes a gate dielectric film 102 that comprises "a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity [i.e., high-κ] dielectric film." Aoyama ¶[0098]. In region 106, gate dielectric film 102 (including gate dielectric film 102A and gate dielectric film 102B) discloses the claimed "first gate insulating film."

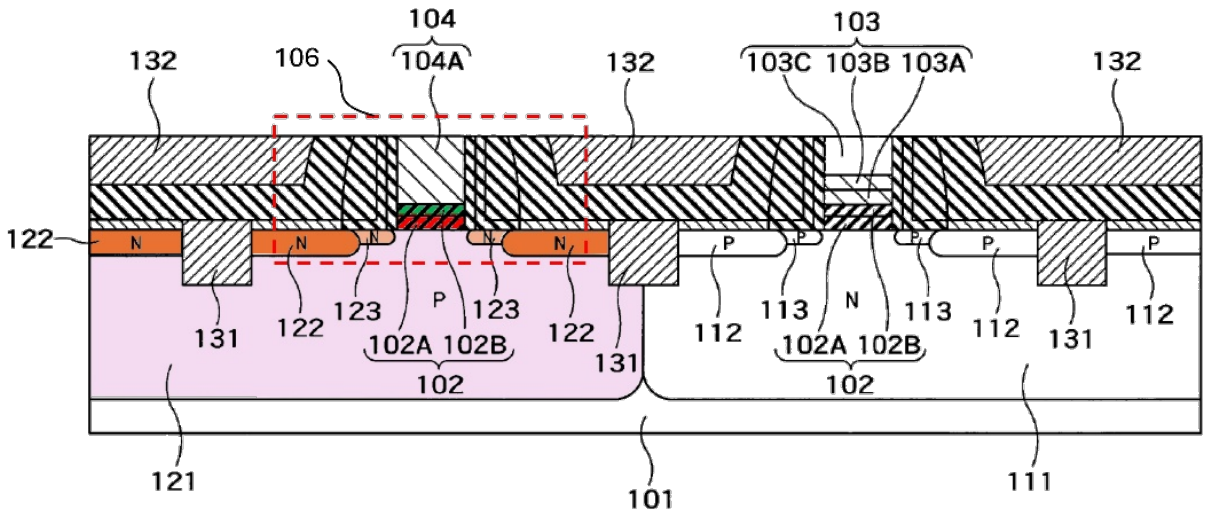


FIG. 5

Aoyama's FIG. 5 (annotated)

126. Gate dielectric film 102 is formed on an "NMOSFET region 106" (first active region) in "substrate 101" "where the NMOSFET is to be formed." Aoyama ¶¶[0105]-[0106]; *see also* Aoyama, FIGS. 5, 6C-6D. From this, a POSITA would have recognized that Aoyama's gate dielectric film 102 is formed on a first active region in semiconductor substrate 101, i.e., the doped areas of the NMOSFET region

106, including p-type well diffusion layer 121, n-type source/drain diffusion layers 122, and n-type extension diffusion layers 123. *See* Aoyama ¶[0100], FIG. 5.

127. Gate dielectric film 102B is a hafnium silicon oxynitride film made by exposing a hafnium silicate film to nitrogen. Aoyama ¶[0106]. A POSITA would have recognized that hafnium silicon oxynitride is "a high-k film" because Aoyama refers to it as "a high-permittivity dielectric film," which is synonymous with "a high-k film" (*k* or *κ* being the symbol for dielectric permittivity). Aoyama ¶[0098]; *see also* Akasaka939 ¶[0004] (explaining that "[a] high dielectric constant film made of the above-noted high-k material [referring to hafnium silicon oxynitride] has its dielectricity of more than ten (10)"). According to the '686 Patent, hafnium silicon oxynitride is an "oxide containing hafnium and silicon." Hafnium silicon oxynitride is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON) . . . ." '686 Patent, 29:16-24.

128. In fact, Aoyama's gate dielectric film 102 is identical to the gate insulating film structure the '686 Patent discloses: a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. The '686 Patent discloses "an underlying film . . . made of a silicon oxide film having a thickness of about 0.8 to 1 nm" and "a gate insulating film formation film 13 made of, for example, a high-k film having a thickness of 2 nm." '686 Patent, 11:25-37.

According to the ’686 Patent, “examples of the gate insulating film formation film 13 . . . include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON).” ’686 Patent, 29:16-24. As FIG. 5 shows above, Aoyama identically discloses “a silicon oxide film . . . 102A with a thickness of 0.5 to 0.8 nm” and “a hafnium silicon oxynitride film 102B” “with a thickness of about 2.0 nm.” Aoyama ¶[0106].

129. If only part of the gate dielectric film structure may qualify as the claimed “gate insulating film,” Aoyama’s gate dielectric film 102B alone in region 106 also discloses a “first gate insulating film” for the reasons stated above. In any event, because Aoyama and the ’686 Patent identically disclose the same gate dielectric stack, Aoyama discloses the claimed “first gate insulating film” no matter how the claim is mapped to the gate dielectric stack.

130. Also, for the same reasons I explain above, a POSITA also would have found it obvious that “the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon,” in view of Aoyama.

e. [19D]: “the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film”

131. Aoyama discloses that “the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film.”

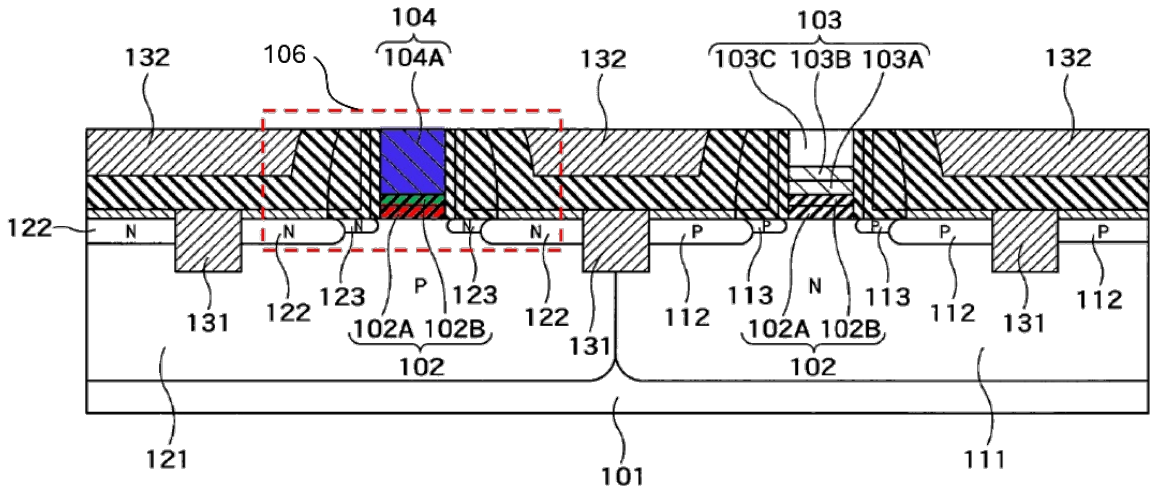


FIG. 5

Aoyama's FIG. 5 (annotated)

132. In the semiconductor device of Aoyama's FIG. 5, the nFET in region 106 has a gate electrode 104 that comprises a conductive layer 104A, which is "made of [a] conductive metal." Aoyama ¶[0098]. Conductive layer 104A discloses the claimed "second metal film." As Aoyama's FIG. 5 shows above, conductive layer 104A is formed on gate dielectric film 102 in region 106 (the claimed "first gate insulating film").

133. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film" in view of Aoyama.

f. [19E]: "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative"

134. Aoyama discloses that "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative."

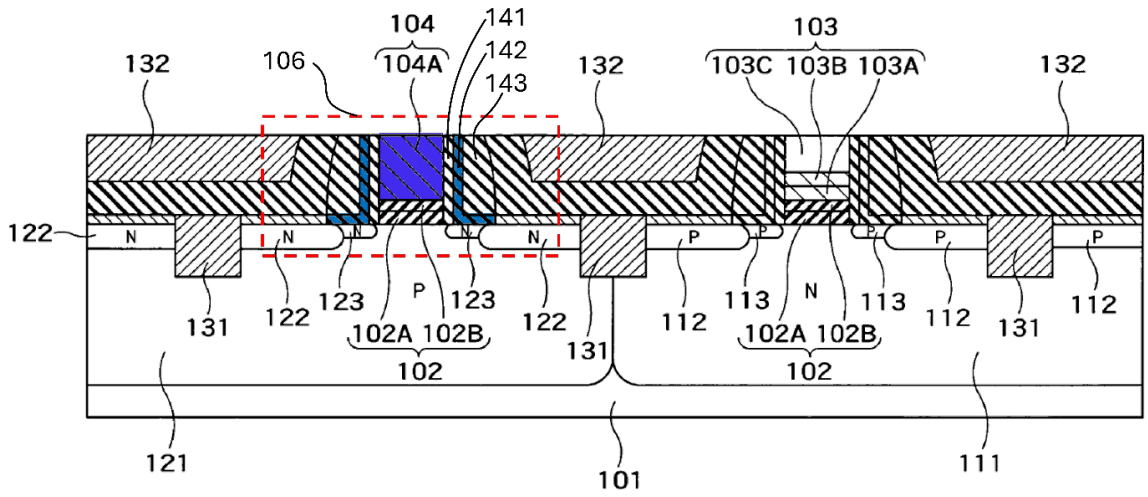


FIG. 5

Aoyama's FIG. 5 (annotated)

135. In Aoyama's third embodiment, as shown in FIG. 5, the nFET in region 106 includes "an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film," both of which "are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE." Aoyama ¶[0111]. In region 106, either Aoyama's sidewall spacers 142 alone

disclose the claimed "first sidewall spacers," or Aoyama's offset spacers 141 and sidewall spacers 142, collectively, disclose the claimed "first sidewall spacers."

136. A POSITA would have recognized that Aoyama's sidewall spacers 142, which are made of silicon oxide, and Aoyama's offset spacers 141, which are made of silicon oxide or silicon nitride, are both insulative. Silicon oxide and silicon nitride are the oldest and most prominent insulating materials used in semiconductor manufacturing.

137. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative," in view of Aoyama.

g. [19F]: "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers"

138. Aoyama discloses that "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers."

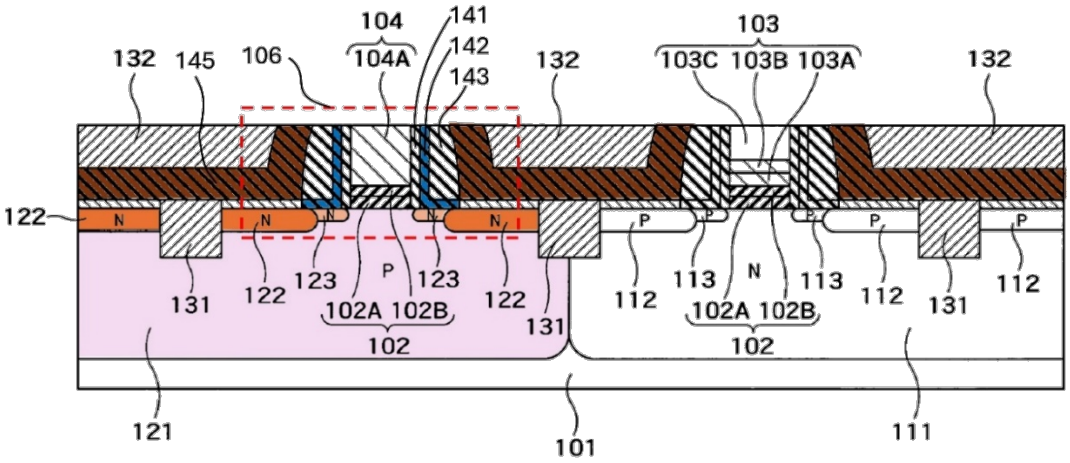


FIG. 5

Aoyama's FIG. 5 (annotated)

139. The semiconductor device of Aoyama's FIG. 5 includes an "etch stopper film 145 made of a silicon nitride film." Aoyama ¶[0113]. Etch stopper film 145 discloses the claimed "silicon nitride film."

140. Aoyama explains that etch stopper film 145 "is formed over the entire surface by CVD," then "planarized by chemical mechanical polishing or etching (dry etching or wet etching)" to expose the area where the nFET and pFET gate electrodes are formed. Aoyama ¶[0113]; *see also* Aoyama ¶¶[0114]-[0119], FIGS. 5, 6K-6Q.

141. As FIG. 5 shows above, Aoyama's silicon nitride etch stopper film 145 (brown) extends over the side surfaces of the nFET gate electrode (gate electrode 104) on which the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)) are formed. *See* Aoyama, FIG. 5.

142. As FIG. 5 also shows above, silicon nitride etch stopper film 145 (brown) extends over upper surfaces of the first active region (NMOSFET region 106) located laterally outside of the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)).

143. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers," in view of Aoyama.

h. [19G]: "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon"

144. Aoyama discloses "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon."

145. Aoyama's "second MIS transistor" (the pFET in region 105) includes a gate dielectric film 102 that comprises "a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity [i.e., high-κ] dielectric film." Aoyama ¶[0098]. In region 105, gate dielectric

film 102 (including gate dielectric film 102A and gate dielectric film 102B) discloses the claimed "second gate insulating film."

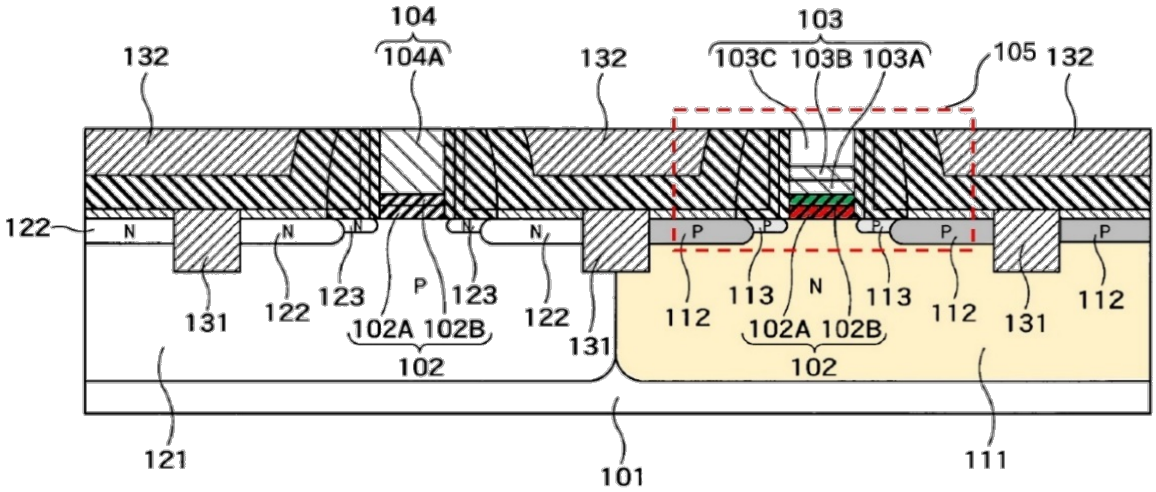


FIG. 5

Aoyama's FIG. 5 (annotated)

146. Gate dielectric film 102 is formed on a "PMOSFET region 105" (second active region) in "substrate 101" "where the PMOSFET is to be formed." Aoyama ¶¶[0104]-[0106]; *see also* Aoyama, FIGS. 5, 6B-6D. From this, a POSITA would have recognized that Aoyama's gate dielectric film 102 is formed on a second active region in semiconductor substrate 101, i.e., the doped areas of PMOSFET region 105, including n-type well diffusion layer 111, p-type source/drain diffusion layers 112, and p-type extension diffusion layers 113. *See* Aoyama ¶[0099], FIG. 5.

147. Gate dielectric film 102B is a hafnium silicon oxynitride film made by exposing a hafnium silicate film to nitrogen. Aoyama ¶[0106]. A POSITA would have recognized that hafnium silicon oxynitride is "a high-k film" because Aoyama

refers to it as "a high-permittivity dielectric film," which is synonymous with "a high-k film" (*k* or *κ* being the symbol for dielectric permittivity). Aoyama ¶[0098]; *see also* Akasaka939 ¶[0004] (explaining that "[a] high dielectric constant film made of the above-noted high-k material [referring to hafnium silicon oxynitride] has its dielectricity of more than ten (10)"). According to the '686 Patent, hafnium silicon oxynitride is an "oxide containing hafnium and silicon." Hafnium silicon oxynitride is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON) . . . ." '686 Patent, 29:16-24.

148. In fact, Aoyama's gate dielectric film 102 is identical to the gate insulating film structure the '686 Patent discloses: a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. The '686 Patent discloses "an underlying film . . . made of a silicon oxide film having a thickness of about 0.8 to 1 nm" and "a gate insulating film formation film 13 made of, for example, a high-k film having a thickness of 2 nm." '686 Patent, 11:25-37. According to the '686 Patent, "examples of the gate insulating film formation film 13 . . . include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON)." '686 Patent, 29:16-24. As FIG. 5 shows above, Aoyama identically discloses "a silicon oxide film . . . 102A with a thickness of 0.5 to 0.8 nm" and

"a hafnium silicon oxynitride film 102B" "with a thickness of about 2.0 nm." Aoyama ¶[0106].

149. If only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," Aoyama's gate dielectric film 102B alone in region 105 also discloses a "second gate insulating film" for the reasons stated above. In any event, because Aoyama and the '686 Patent identically disclose the same gate dielectric stack, Aoyama discloses the claimed "second gate insulating film" no matter how the claim is mapped to the gate dielectric stack.

150. Also, for the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon," in view of Aoyama.

i. [19H]: "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film"

151. Aoyama discloses "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film."

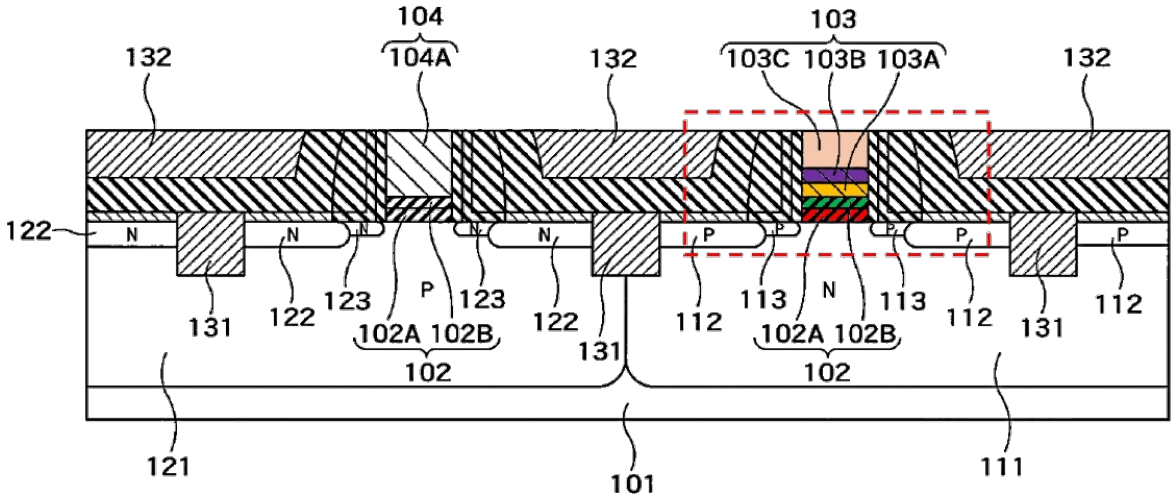


FIG. 5

Aoyama's FIG. 5 (annotated)

152. In the semiconductor device of Aoyama's FIG. 5, the pFET in region 105 has a gate electrode 103 that comprises (1) a "conductive layer 103A which is made of conductive metal," (2) a "conductive layer 103B which is made of conductive metal," and (3) a "semiconductor layer (silicide layer) 103C" comprising a "polysilicon or amorphous silicon" layer and a "Ni monosilicide (NiSi)" layer.[10] Aoyama ¶[0098], ¶[0107], ¶[0114], ¶[0121].

[10] I discuss this further below, in Sections IX.B.1.c-d, where I describe how Aoyama discloses claim features [11M] and [11N]. Aoyama's silicon layer (silicide layer) 103C is just like the uppermost portion of gate electrode 30B in the '686 Patent—a polysilicon or amorphous silicon layer in which a nickel silicide layer is formed. *See* '686 Patent, 11:50-67 (disclosing "a silicon film 15 made of, for example, a polysilicon film" that is patterned into "a second silicon film 15b" in the pFET active region), 29:41-45 ("[A]lthough a polysilicon film is used as the silicon film 15 . . . , a silicon film made of other semiconductor materials, such as an amorphous silicon

153. Aoyama's "conductive layer 103B which is made of conductive metal" discloses the claimed "first metal film." Aoyama ¶[0098]. As Aoyama's FIG. 5 shows above, conductive layer 103B is formed on gate dielectric film 102 in region 105 (the claimed "second gate insulating film").

154. Aoyama's FIG. 5 above further shows that semiconductor layer (silicide layer) 103C is formed on conductive layer 103B (the claimed "first metal film"). Either or both constituent parts of Aoyama's semiconductor layer (silicide layer) 103C—i.e., the semiconductor layer and/or the silicide layer—correspond to the claimed "conductive film." Aoyama explains that gate electrode 103 is conductive (i.e., has low resistance) due to semiconductor layer (silicide layer) 103C: "[G]ate electrode 103 for the PMOSFET includes . . . semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). ***For this reason,*** in the third embodiment, ***the gate resistance of the PMOSFET is relatively low.***" Aoyama ¶[0121] (emphases added). A POSITA would have understood this means semiconductor layer (silicide layer) 103C is conductive.

155. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . a second gate electrode

film, a silicon film and the like, may be used."), 21:25-35 (explaining that "a metal silicide film 34 made of nickel silicide [is formed] in an upper portion of the second silicon film 15b").

including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film" in view of Aoyama.

j. [19I]: "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative"

156. Aoyama discloses "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative."

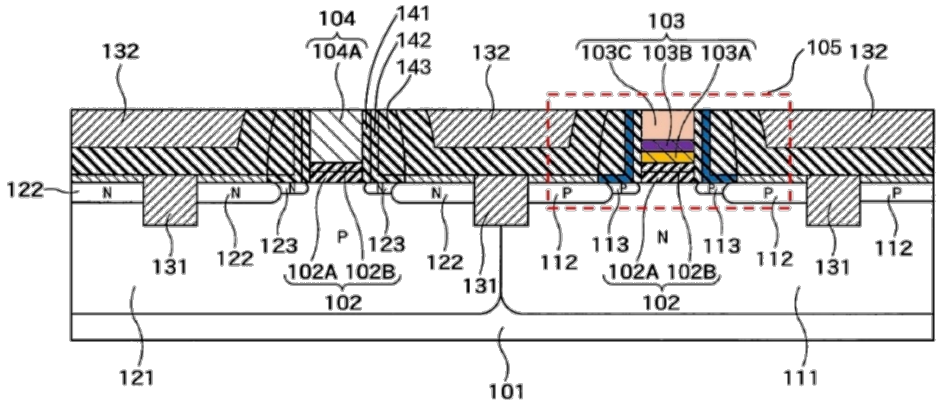


FIG. 5

Aoyama's FIG. 5 (annotated)

157. In the semiconductor device of Aoyama's FIG. 5, the pFET in region 105 includes "an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film," both of which "are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE." Aoyama ¶[0111]. In region 105, either Aoyama's sidewall spacers 142 alone (shaded in blue above) disclose the claimed "second sidewall spacers," or Aoyama's

offset spacers 141 and sidewall spacers 142, collectively, disclose the claimed "second sidewall spacers."

158. A POSITA would have recognized that Aoyama's sidewall spacers 142, which are made of silicon oxide, and Aoyama's offset spacers 141, which are made of silicon oxide or silicon nitride, are both insulative. Silicon oxide and silicon nitride are the oldest and most prominent insulating materials used in semiconductor manufacturing.

159. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative," in view of Aoyama.

k. [19J]: "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers"

160. Aoyama discloses "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers."

161. The semiconductor device of Aoyama's FIG. 5 includes an "etch stopper film 145 made of a silicon nitride film." Aoyama ¶[0113]. Etch stopper film 145 discloses the claimed "silicon nitride film."

162. Aoyama explains that etch stopper film 145 "is formed over the entire surface by CVD," then "planarized by chemical mechanical polishing or etching (dry etching or wet etching)" to expose the area where the nFET and pFET gate electrodes will be formed. Aoyama ¶[0113]; *see also* Aoyama ¶¶[0114]-[0119], FIGS. 5, 6K-6Q.

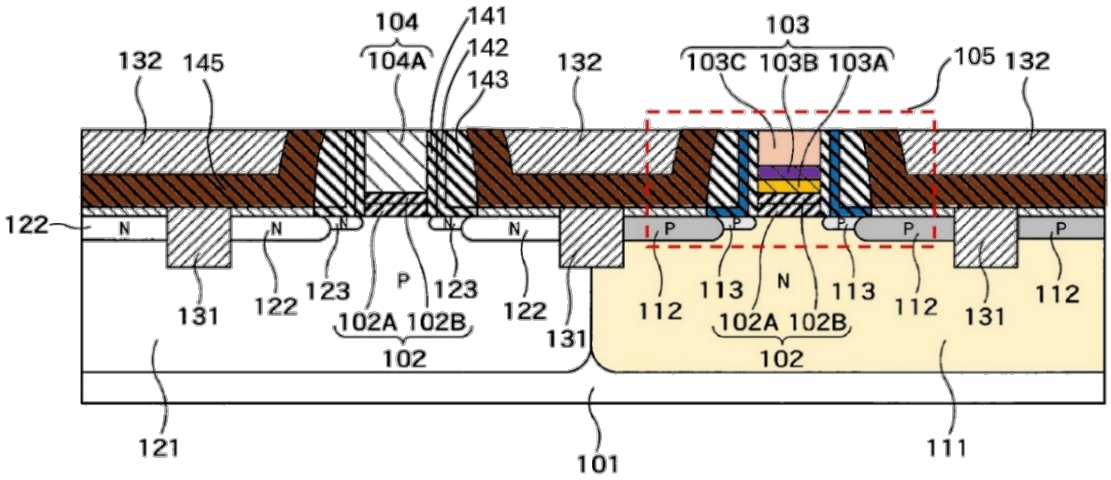


FIG. 5

Aoyama's FIG. 5 (annotated)

163. As FIG. 5 shows above, Aoyama's silicon nitride etch stopper film 145 (brown) extends over the side surfaces of the pFET gate electrode (gate electrode 103) on which the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)) are formed. *See* Aoyama, FIG. 5.

164. As FIG. 5 also shows above, silicon nitride etch stopper film 145 (brown) extends over upper surfaces of the second active region (PMOSFET region 105) located laterally outside of the gate sidewalls (sidewall spacer 142 (blue) alone or together with offset spacer 141 (not colored)).

165. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers," in view of Aoyama.

l. [19K]: "the first and second metal films are made of different metal materials"

166. Aoyama discloses "the first and second metal films are made of different metal materials."

167. As I explain for feature [19D], Aoyama's conductive layer 104A discloses the claimed "second metal film" (in the nFET region). In the embodiment of FIG. 5, the exemplary metal material used to form conductive layer 104A is TaCN. Aoyama ¶[0118].

168. As I explain for feature [19H], Aoyama's conductive layer 103B discloses the claimed "first metal film" (in the pFET region). In the embodiment of

FIG. 5, the exemplary metal material used to form conductive layer 103B is TiN. Aoyama ¶[0107].

169. Thus, the first metal film (conductive layer 103B) is made of a different metal material than the second metal film (conductive layer 104B). *See* Aoyama ¶[0107], ¶[0118]. Titanium nitride and tantalum carbonitride are different metal materials.

170. For the same reasons I explain above, a POSITA also would have found it obvious that "the first and second metal films are made of different metal materials" in view of Aoyama.

m. [19L]: "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes"

171. Aoyama discloses "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes."

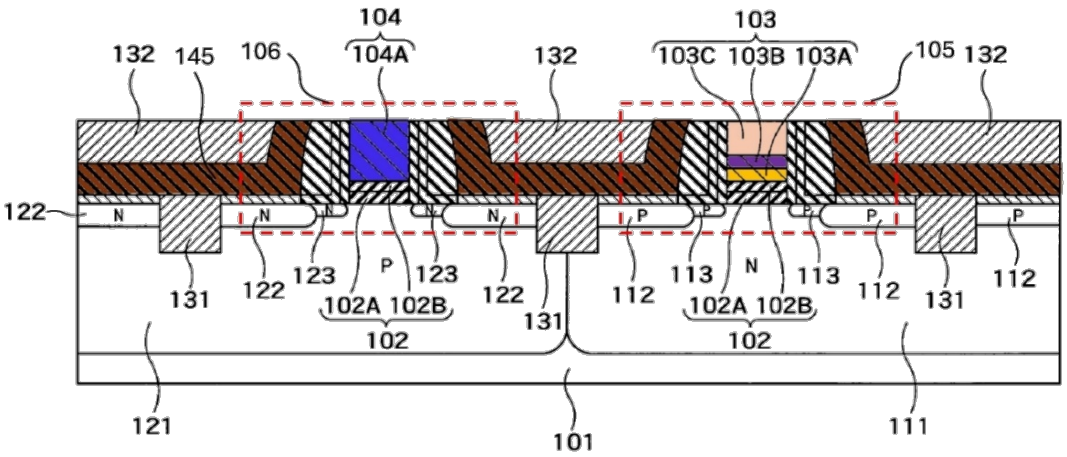


FIG. 5

Aoyama's FIG. 5 (annotated)

172. In the semiconductor device Aoyama's FIG. 5 shows, silicon nitride etch stopper film 145 is not formed on any upper surfaces of the nFET and pFET gate electrodes 104 and 103, respectively. A POSITA would have recognized this from the manufacturing process Aoyama discloses. As Aoyama's FIGS. 6J-6K illustrate, gate electrode 103, which serves as a pFET gate electrode as well as a dummy gate electrode for the nFET, is formed where the nFET and pFET gate electrodes will be located. Aoyama ¶[0109]. As FIG. 6K shows below, silicon nitride etch stopper film 145 and interlayer dielectric film 132 are formed over the pFET gate electrode 103 (right side) and the nFET dummy gate electrode 103 (left side). Aoyama ¶[0113]. As Aoyama explains, etch stopper film 145 is "formed over the entire surface" of the semiconductor device, then "planarized" so that "semiconductor layer[] 103C . . . [is] exposed both in the PMOSFET region 105 and the NMOSFET region 106." Aoyama ¶[0113].

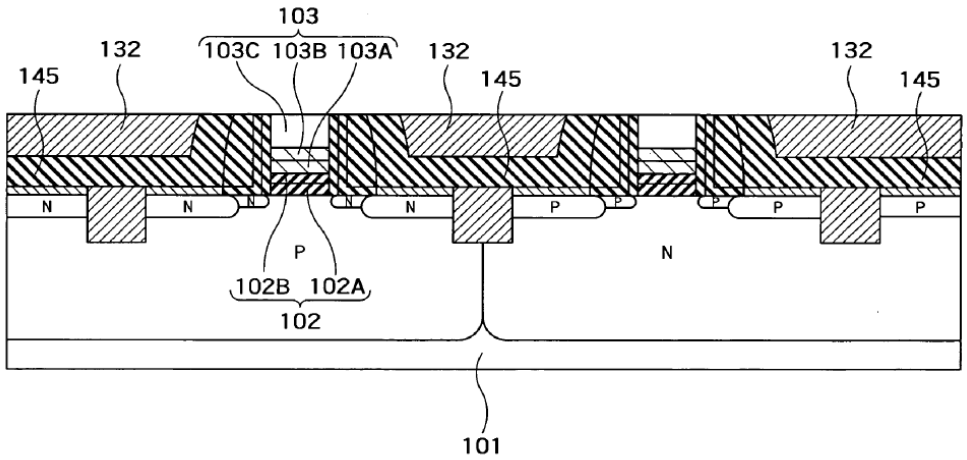


FIG. 6K

Aoyama's FIG. 6K

173. Thereafter, semiconductor layer 103C and conductive layers 103B and 103A are removed from the nFET dummy gate electrode in region 106 and replaced with conductive layer 104A, thereby forming gate electrode 104. Aoyama ¶¶[0114]-[0119], FIGS. 6M-6Q.

174. A POSITA would have understood this process prevents silicon nitride etch stopper film 145 from being located on any upper surface of the first or second gate electrode.

175. For the same reasons I explain above, a POSITA also would have found it obvious that "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes" in view of Aoyama.

n. [19M]: "the first metal film is made of titanium nitride"

176. Aoyama discloses "the first metal film is made of titanium nitride."

177. As I explain for feature [19H], Aoyama's conductive layer 103B discloses the claimed "first metal film." In the embodiment of FIG. 5, the exemplary metal material used to form conductive layer 103B is "TiN (titanium nitride)." Aoyama ¶[0107] (referring to "TiN (titanium nitride) layer 103B"); *see also* Aoyama ¶[0109] (referring to "TiN layer 103B"), ¶¶[0115]-[0116] (same).

178. For the same reasons I explain above, a POSITA also would have found it obvious that "the first metal film is made of titanium nitride" in view of Aoyama.

2. Claim 20

179. Claim 20 depends from claim 19. I understand that means claim 20 requires all the same features as claim 19, plus the additional features recited in claim 20. Aoyama discloses all the features recited in claim 19 for the reasons I provide in Section IX.A.1 above.

180. Aoyama further discloses "wherein the first metal film has a thickness smaller than that of the second metal film."

181. As I explain for feature [19D], Aoyama's conductive layer 104A discloses the claimed "second metal film."

182. As I explain for feature [19H], Aoyama's conductive layer 103B discloses the claimed "first metal film."

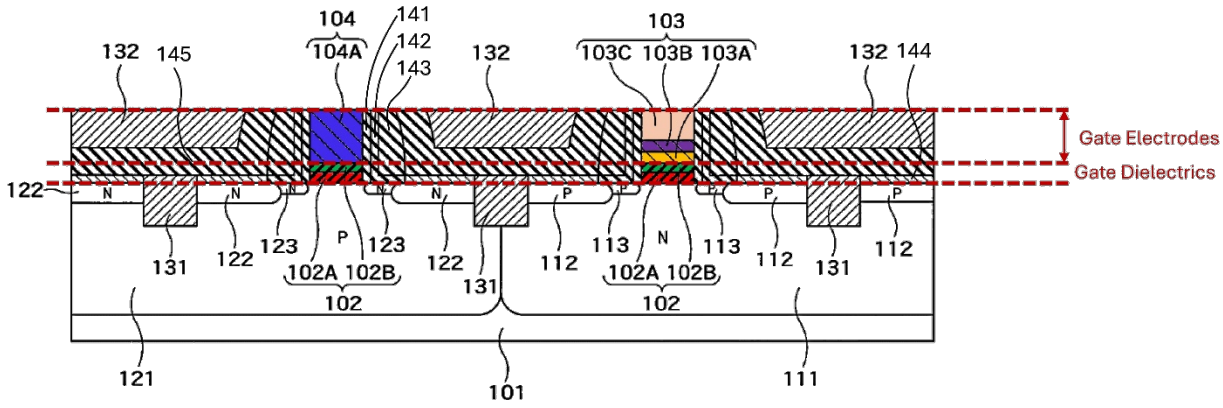


FIG. 5

Aoyama's FIG. 5 (annotated)

183. In the embodiment of FIG. 5, Aoyama discloses planarizing the device structures after forming conductive layer 104A. *See* Aoyama ¶[0119] ("[A]s shown

in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback).”), FIG. 6Q. As the annotations above indicate, Aoyama’s gate electrodes 103 and 104 must have the same thickness because Aoyama’s gate electrodes 103 and 104 are both formed on gate dielectric films 102A and 102B, and the gate structures are both planarized to have the same total height. Thus, pFET layers 103A, 103B, and 103C, collectively, have a thickness equal to nFET layer 104A. It follows that the claimed “first conductive layer” (i.e., conductive layer 103B) is necessarily thinner than the claimed “second conductive layer” (i.e., conductive layer 104A).

184. Again, the process Aoyama describes for forming the semiconductor device of FIG. 5 ensures this is true. As FIG. 6G shows below, before conductive layer 104A is formed, layers 103A, 103B, and 103C are deposited to form pFET gate electrode 103 and a “dummy gate electrode” 103 for the nFET. Aoyama ¶[0109].

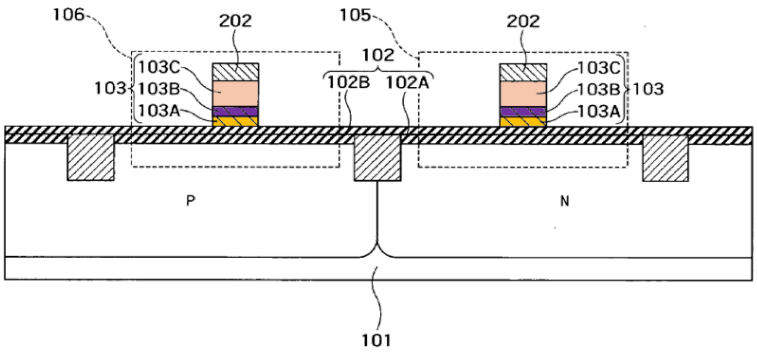


FIG. 6G

Aoyama’s FIG. 6G (annotated)

185. As Aoyama's FIGS. 6L-6O show, layers 103A, 103B, and 103C of the nFET dummy gate electrode 103 are then removed in region 106, creating a trench 151 while leaving intact films 102A and 102B comprising the gate dielectric 102.[11] *See* Aoyama ¶¶[0114]-[0117], FIG. 6O.

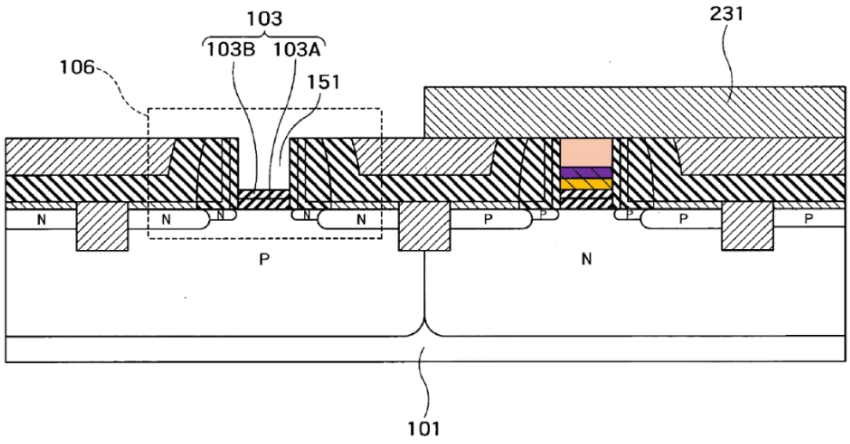


FIG. 6O

Aoyama's FIG. 6O (annotated)

186. Finally, conductive layer 104A is formed in trench 151 left by removing nFET dummy gate electrode 103, thereby forming nFET gate electrode 104, as FIG. 6Q shows below. *See* Aoyama ¶[0119], FIG. 6Q. In this step, the nFET and pFET gate electrodes are planarized to have the same total height. Aoyama explains: "Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback)." Aoyama ¶[0119].

[11] In FIG. 6O, Aoyama's first gate dielectric film 102A, second gate dielectric film 102B, and gate dielectric film 102 are mislabeled 103A, 103B, and 103, respectively. *See* Aoyama ¶¶[0115]-[0117], FIGS. 6L-6O.

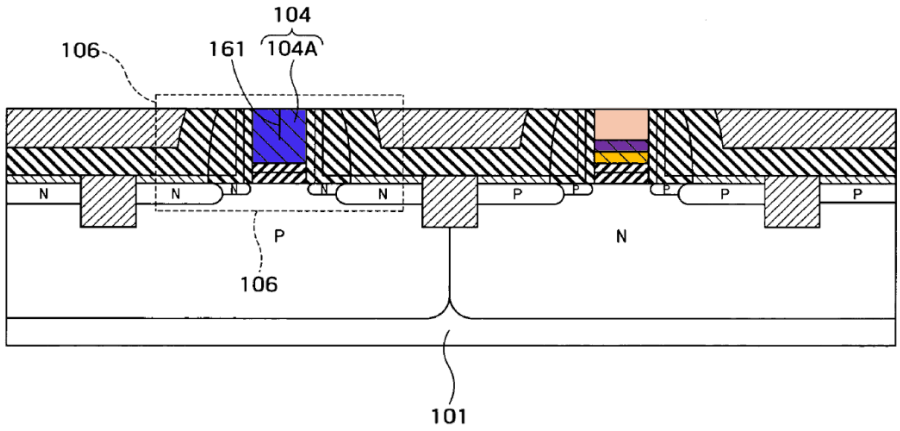


FIG. 6Q

Aoyama's FIG. 6Q (annotated)

187. A POSITA thus would have recognized from the manufacturing process Aoyama discloses for the semiconductor device of FIG. 5 that gate electrode 104, which fills the trench 151 left by removing layers 103A, 103B, and 103C of nFET dummy gate electrode 103, has the same thickness as layers 103A, 103B, and 103C, collectively. Accordingly, it follows that the claimed "first conductive layer" (i.e., conductive layer 103B) is necessarily thinner than the claimed "second conductive layer" (i.e., conductive layer 104A).

188. For the same reasons I explain above, a POSITA also would have found it obvious that "the first metal film has a thickness smaller than that of the second metal film" in view of Aoyama.

3. Claim 21

189. Claim 21 depends from claim 19. I understand that means claim 21 requires all the same features as claim 19, plus the additional features recited in claim

21. Aoyama anticipates and/or renders obvious all the features recited in claim 19 for the reasons I provide in Section IX.A.1 above.

190. Aoyama further discloses "wherein the first and second metal films have different work functions."

191. As I explain for feature [19D], Aoyama's conductive layer 104A discloses the claimed "second metal film." In the embodiment of FIG. 5, the exemplary metal material used to form conductive layer 104A is TaCN. Aoyama ¶[0118].

192. As I explain for feature [19H], Aoyama's conductive layer 103B discloses the claimed "first metal film." In the embodiment of FIG. 5, the exemplary metal material used to form conductive layer 103B is titanium nitride (TiN). Aoyama ¶[0107].

193. Aoyama's "Related Art" section explains that "metals such as . . . TaCN . . . [have] a work function of 4.3 eV or less," which increases "to about 4.5 eV" when annealed to about 1,000 ºC. Aoyama ¶[0010]. By adopting Aoyama's RMG process for the nFET, however, conductive film 104A never experiences such temperatures, and "[i]t is possible to adopt, for example, a . . . TaCN layer . . . as a metal electrode layer to form the gate electrode 104 for the NMOSFET." Aoyama ¶[0069]. That is, Aoyama's TaCN conductive layer 104A has "a work function of 4.3 eV or less." Aoyama ¶[0010].

194. Additionally, TiN has "a work function close to that of p^+-polycrystalline silicon, such as a work function of 4.8 to 5.3 eV." Akasaka ¶[0046]; *see also* Akasaka ¶[0077] (same). Westlinder explains: "The work function of ALD TiN changes from a p-type gate material (5.1 ± 0.1 eV) toward a more midgap material (4.8 ± 0.1 eV) after annealing above ~ 800 ºC. The latter is close to what was reported recently for sputtered PVD TiN. It is interesting to note that the work function remains p-type up to 700 ºC." Westlinder, 551.

195. Accordingly, the work functions of TaCN (e.g., 4.3 eV or less) and TiN (e.g., 5.1 eV) are different. In the device of Aoyama's FIG. 5, a POSITA thus would have understood from Aoyama's disclosures that the claimed "first metal film" (conductive layer 103B made of TiN) and the claimed "second metal film" (conductive layer 104A made of TaCN) have different work functions.

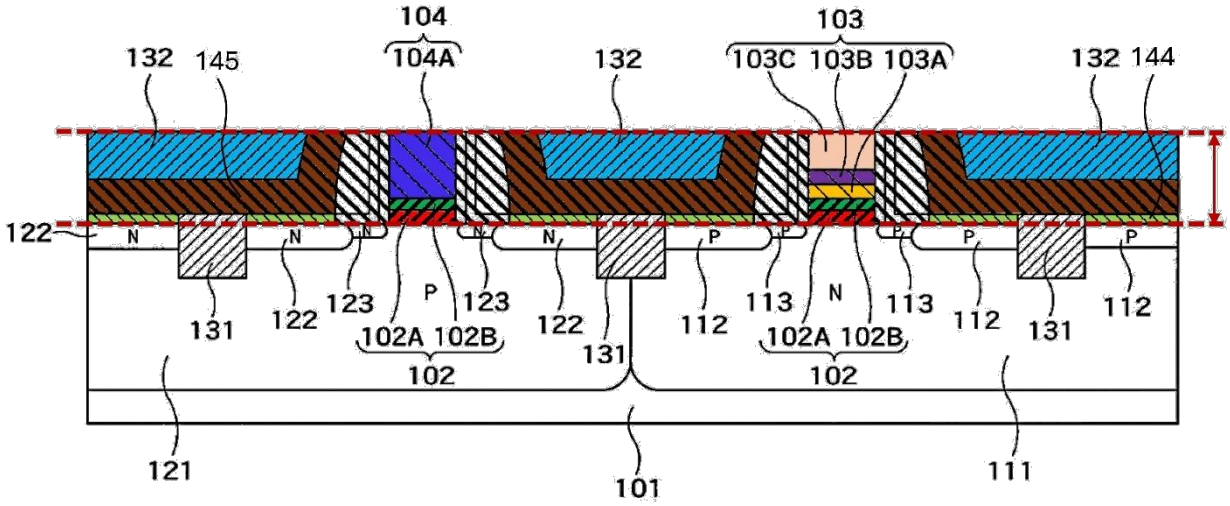
196. For the same reasons I explain above, a POSITA also would have found it obvious that "the first and second metal films have different work functions" in view of Aoyama.

4. Claim 22

197. Claim 22 depends from claim 19. I understand that means claim 22 requires all the same features as claim 19, plus the additional features recited in claim 22. Aoyama discloses all the features recited in claim 19 for the reasons I provide in Section IX.A.1 above.

198. Aoyama further discloses "wherein the silicon nitride film has a thickness smaller than that of the first gate electrode."

199. As I explain regarding features [19D] and [19F], Aoyama's silicon nitride etch stopper film 145 discloses the claimed "silicon nitride film," and Aoyama's gate electrode 104 discloses the claimed "first gate electrode." Aoyama discloses that silicon nitride etch stopper film 145 has a smaller thickness than Aoyama's gate electrode 104 because FIG. 5 (annotated below) shows etch stopper film 145 (brown) is much thinner than gate electrode 104 (purple), consistent with what a person of ordinary skill in the art would have expected.



Aoyama, FIG. 5 (annotated)

200. Accordingly, it is my opinion that Aoyama discloses claim 22.

201. It is also my opinion that Aoyama renders obvious "wherein the silicon nitride film has a thickness smaller than that of the first gate electrode." For at least four additional reasons, a person of ordinary skill in the art would have found it

obvious that Aoyama's silicon nitride etch stopper film 145 has a smaller thickness than Aoyama's gate electrode 104.

202. **The first reason** a POSITA would have found it obvious for Aoyama's etch stopper film 145 (brown) to have a smaller thickness than gate electrode 104 is that a POSITA would have expected it. In fact, a POSITA would have found it highly unusual were it otherwise.

203. In the process Aoyama describes for manufacturing its semiconductor device, Aoyama's gate electrodes 103 and 104 are planarized to have the same total height. As Aoyama explains with reference to FIG. 6Q, "the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback)." Aoyama ¶[0119]. As a result, and as the red arrow above indicates, the total height of etch stopper film 145 and interlayer dielectric 132 cannot exceed the total height of the gate dielectric film 102 and gate electrode 104. Mathematically, the following must be true:

$$\mathbf{T_{145} + T_{132} + T_{144} = T_{102} + T_{104}} \qquad \textbf{(Eq. 1)}$$

where $\mathbf{T_x}$ is the thickness of layer **x** above the substrate.

204. Translating the requirement of claim 22 into these mathematical variables, claim 22 applied to Aoyama requires:

$$\mathbf{T_{145} < T_{104}} \qquad \textbf{(Eq. 2)}$$

205. Substituting Equation 2 into Equation 1, the following inequality obtains for Aoyama:

$$\mathbf{T_{104} + T_{132} + T_{144} > T_{102} + T_{104}} \qquad \textbf{(Eq. 3)}$$

206. Canceling the common variable on both sides of the inequality (T_{104}) gives the following relationship between the thickness of interlayer dielectric 132, the thickness of the silicide film 144 extending above the substrate surface, and the thickness of gate dielectric film 102:

$$\mathbf{T_{132} + T_{144} > T_{102}} \qquad \textbf{(Eq. 4)}$$

207. Thus, even completely (and improperly) ignoring the thickness of the silicide above the substrate surface (T_{144}), which itself would have been expected to exceed the thickness of gate dielectric film 102,[12] Aoyama satisfies claim 22 so long as the thickness of interlayer dielectric 132 is greater than the thickness of gate dielectric film 102.

208. This inequality illustrates in stark terms why Aoyama renders obvious claim 22. A POSITA would have expected Aoyama's interlayer dielectric 132 to be significantly thicker than gate dielectric film 102 and would have found it highly unusual were it otherwise. Factoring in the thickness of silicide film 144 only further

[12] *See, e.g.*, Bohr683 ¶[0037] ("[L]ayers of silicide material 523, 513, 524, and 514 may comprise nickel silicide consuming approximately 20 nanometers of silicon alloy materials 470 and 480 beginning at surfaces 472 and 482 and extending downward, as shown in FIG. 5."), FIG. 5.

emphasizes the point, as silicide film 144 and interlayer dielectric film 132 each would be expected to be thicker than gate dielectric film 102. *See, e.g.*, Nakajima ¶[0326] (providing an exemplary interlayer dielectric film thickness); Bohr683 ¶[0037] (providing an exemplary NiSi film thickness). Summing their thicknesses would certainly exceed the thickness of gate dielectric film 102.

209. A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode. The gate dielectric is famous for being an extremely thin insulating layer, which is necessary to achieve an extraordinarily ***large*** capacitance. *See* Baklanov, xiii (describing "the high drive current and gate capacitance required of scaled MOSFETs"). Interlayer dielectric films, on the other hand, require ***small*** capacitance and are thus much thicker. That is, "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. *See* Baklanov, xiii.

210. According to Aoyama, gate dielectric layer 102A is 0.5-0.8 nm thick, and gate dielectric layer 102B is about 2.0 nm thick, meaning gate dielectric film 102 has a thickness less than 3 nm. *See* Aoyama ¶[0047]. To underscore the point of just how thin these layers are, layer 102A is only about 2-3 atomic layers thick, and layer 102B is only about 6-7 atomic layers thick. Thus, Aoyama's gate dielectric film 102, like all gate dielectric films in this technology, is extremely thin—much thinner than any interlayer dielectric film.

211. Any real-world device, such as the ones below, can be used to illustrate the point visually. *See also* James, Figs. 1-3, 5-6, 8-12; Mistry2007, Fig. 6; Mistry_Presentation, 16, 19; Thompson2004, Fig. 2; Morin, Fig. 1.

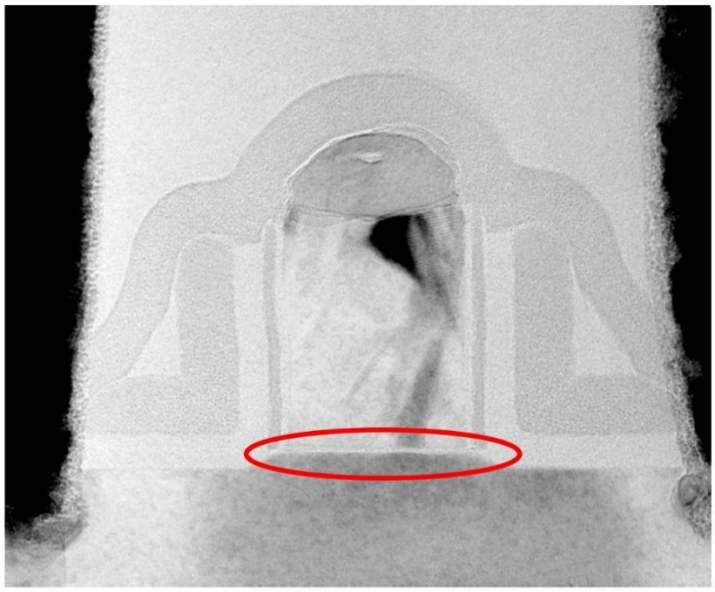


Figure 3. Transistor in TI DSP

James's Fig. 3 (annotated)

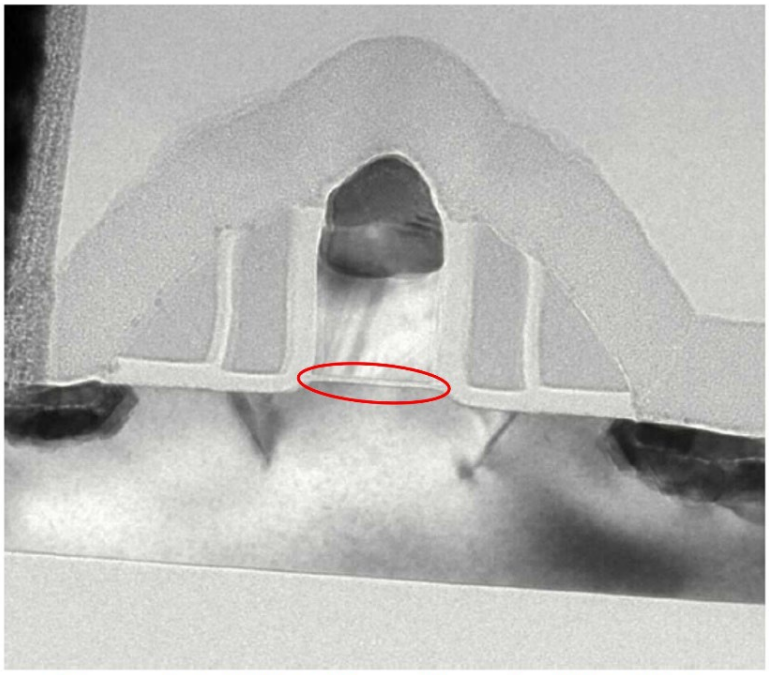
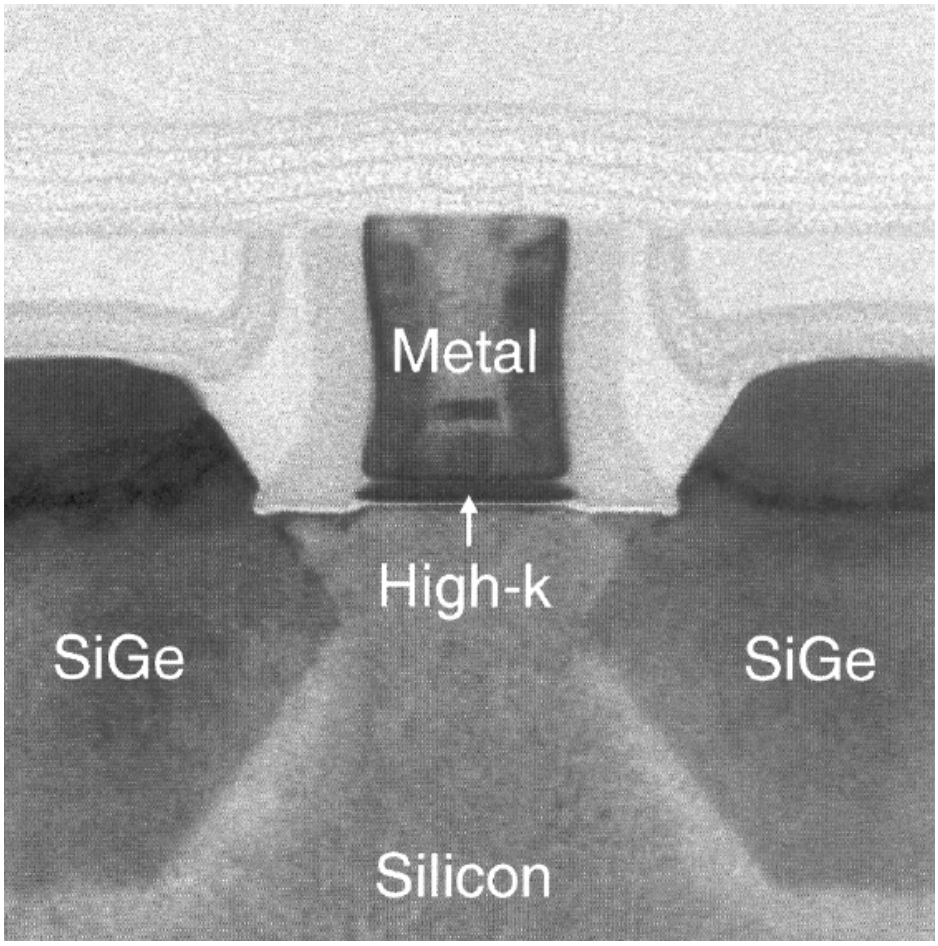


Figure 11. NMOS Transistor in AMD Athlon

James's Fig. 11 (annotated)



Mistry_Presentation, 16 (excerpted)

212. This is why I can say without any doubt that a POSITA would have found it obvious for Aoyama's interlayer dielectric film 132 to be significantly thicker than Aoyama's gate dielectric film 102 and would have found it highly unusual were it otherwise. The prior-art micrograph immediately above illustrates the point well. *See* Mistry_Presentation, 16 (showing Intel's 45nm device); Mistry2007, Fig. 6 (same). The interlayer dielectric is significantly thicker than the gate dielectric in the same type of device Aoyama discloses.

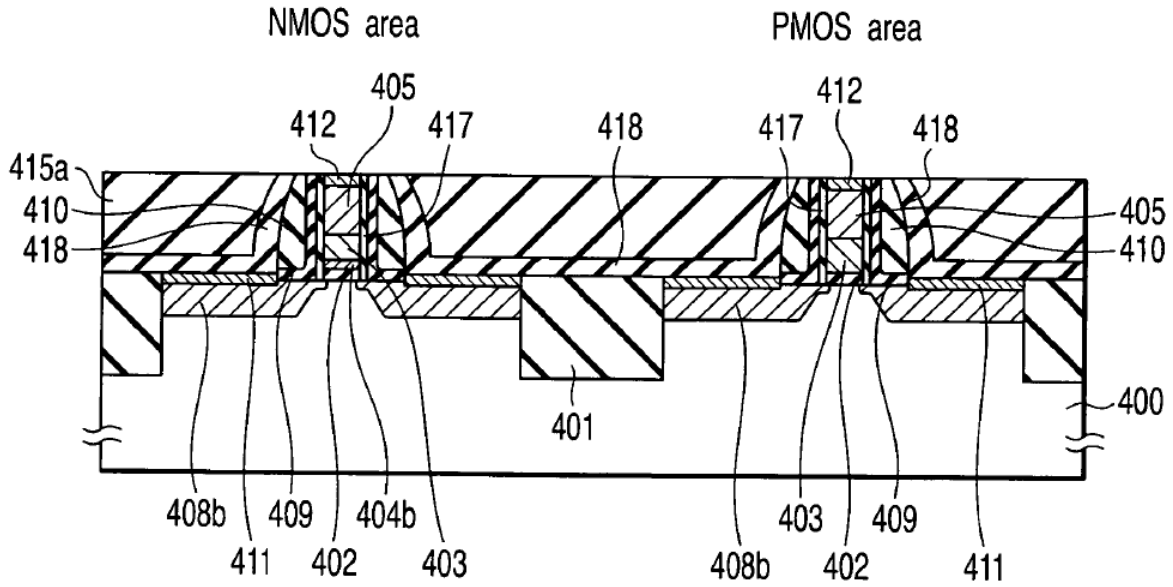


FIG. 52

Nakajima's FIG. 52

213. As another example that is similar to Aoyama, Nakajima (shown above) teaches a metal layer 403 that is 20 nm thick and a metal layer 405 that is 100 nm thick, meaning the gate electrode is at least about 120 nm thick (*see* Nakajima, FIG. 52 below). Nakajima ¶[0317]. The silicon nitride CESL 418 is only about 30 nm thick, and interlayer insulating layer 415a is initially 250 nm thick before being planarized down to what is still more than 90 nm thick (the difference between the thickness of gate electrode layers 403 and 405, minus the thickness of CESL 418). Nakajima ¶[0326], FIGS. 51-52. A thickness of 90 nm is more than an order of magnitude thicker than any conceivable gate dielectric layer, which is indicative of the relative thicknesses a POSITA would have expected.

214. Again, without a doubt, a POSITA would have found it obvious for Aoyama's interlayer dielectric 132 to be significantly thicker than gate dielectric film 102 and would have found it highly unusual were it otherwise. Interlayer dielectric 132 would have been expected to be significantly thicker than gate dielectric film 102.

215. Because Aoyama's silicon nitride etch stopper film 145 is thinner than Aoyama's gate electrode 104 so long as interlayer dielectric 132 is thicker than gate dielectric film 102, a POSITA would have found it obvious for Aoyama's etch stopper film 145 to be thinner than Aoyama's gate electrode 104. Not only would this have been obvious, but a POSITA would have found it very unusual were it otherwise in Aoyama's structure. *See* Aoyama, FIG. 5.

216. **The second reason** a POSITA would have found it obvious for Aoyama's etch stopper film 145 (brown) to have a smaller thickness than gate electrode 104 is that this was one of only two or three possibilities. In fact, it was the most well known of those very limited options.

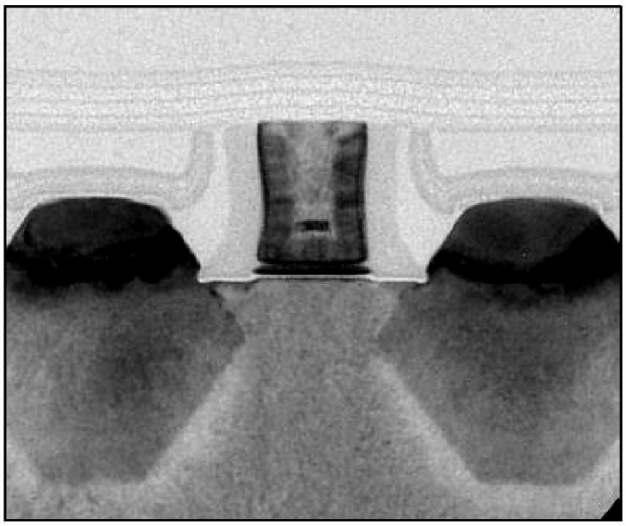
217. I have been told that when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

218. There was a design need to make Aoyama's interlayer dielectric 132 thicker than Aoyama's gate dielectric film 102 because "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. *See* Baklanov, xiii. This would have indicated to a person ordinarily skilled in the art that Aoyama's interlayer dielectric 132 should be thicker than Aoyama's gate dielectric film 102. The result, as I explain above, is that Aoyama's etch stopper film 145 would be thinner than Aoyama's gate electrode 104 as claimed.

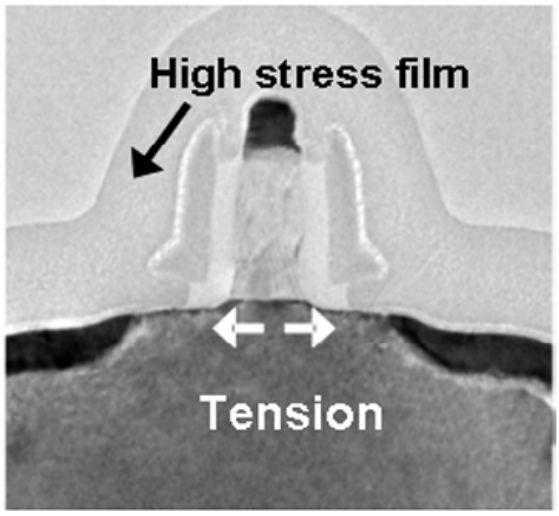
219. Additionally, the design needs of Aoyama's device dictate only two options for the thickness of Aoyama's etch stopper film 145: either it is thinner than Aoyama's gate electrode 104, or it is not. Even being generous, there are only three options available in Aoyama's device structure: Aoyama's etch stopper film 145 is thinner than Aoyama's gate electrode 104; Aoyama's etch stopper film 145 is thicker than Aoyama's gate electrode 104; or Aoyama's etch stopper film 145 has the same thickness as Aoyama's gate electrode 104. Again, Aoyama's planarized structure sets a restriction that the collective thickness of etch stopper film 145 and interlayer dielectric film 132 cannot exceed the height of Aoyama's gate structures.

220. I have been told that two or three options qualify as a finite number of identified, predictable solutions under the law, and I agree in the context at issue here (i.e., the thickness of Aoyama's etch stopper film 145 relative to the thickness of Aoyama's gate electrode 104). Of the limited options available, an etch stopper

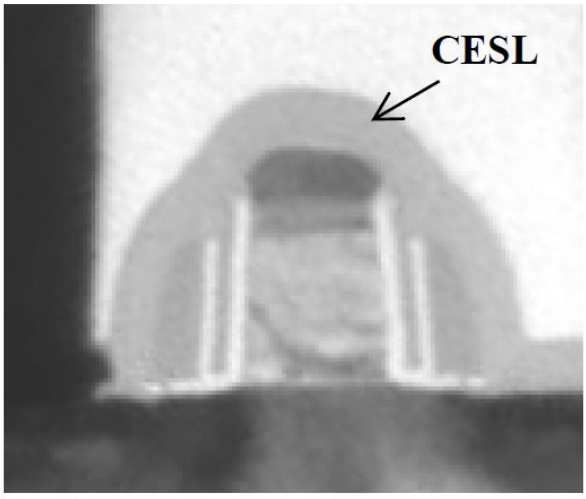
film 145 thinner than the gate electrode 104 was certainly within the technical grasp of a POSITA. Indeed, it would have been expected. A POSITA thus would have found it obvious. Numerous examples below illustrate the point. *See* Mistry2007, Fig. 6; James, Figs. 1-3, 5-6, 8-12; Morin, Fig. 1; Thompson2004, Fig. 2.



Mistry2007's Fig. 6



Thompson2004's Fig. 2 (excerpted)



Morin's Fig. 1

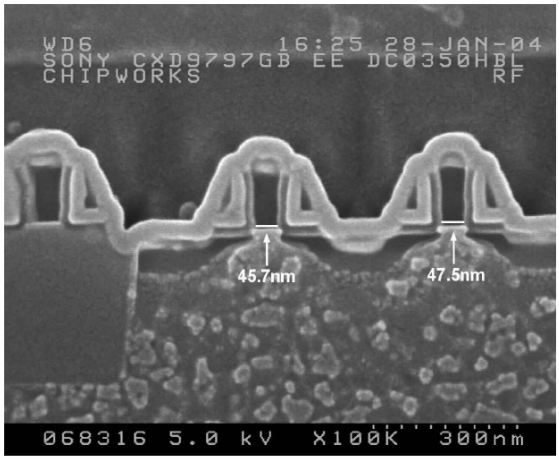


Figure 1. SEM Cross-Section of NMOS Transistors in Sony PSX

James's Fig. 1

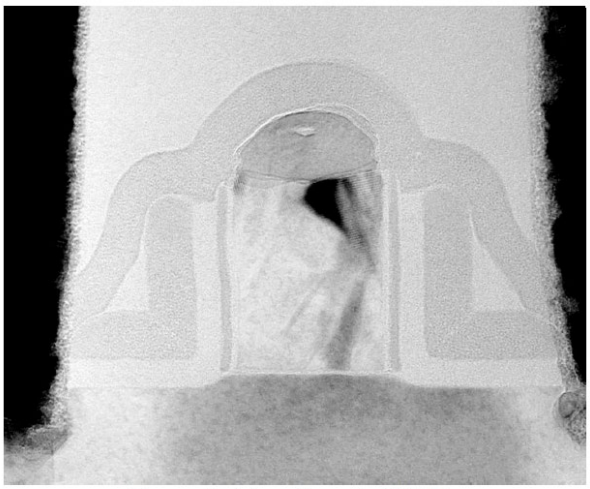


Figure 3. Transistor in TI DSP

James's Fig. 3

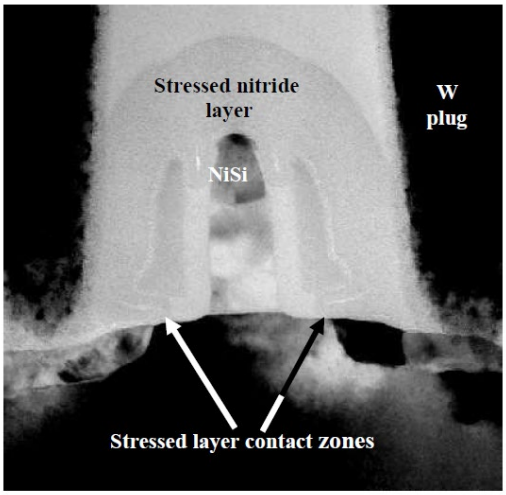


Figure 5. NMOS Transistor in Intel Prescott

James's Fig. 5

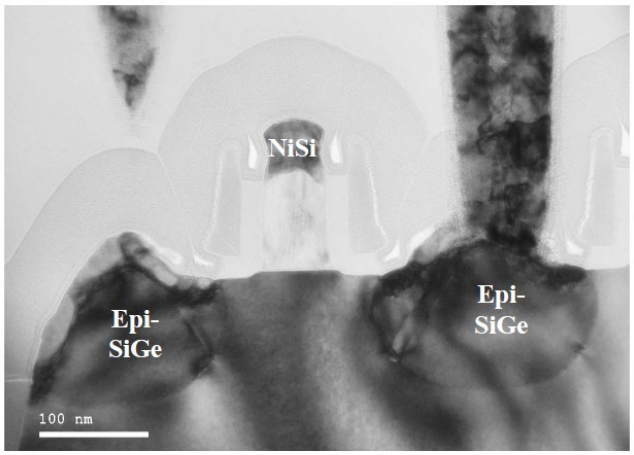


Figure 6. Intel PMOS Transistor

James's Fig. 6

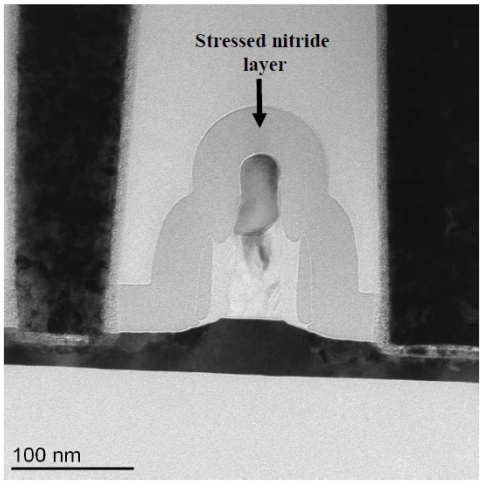


Figure 8. NMOS Transistor in IBM PPC970FX

James's Fig. 8



Figure 9. PMOS Transistor in IBM PPC970FX

James's Fig. 9

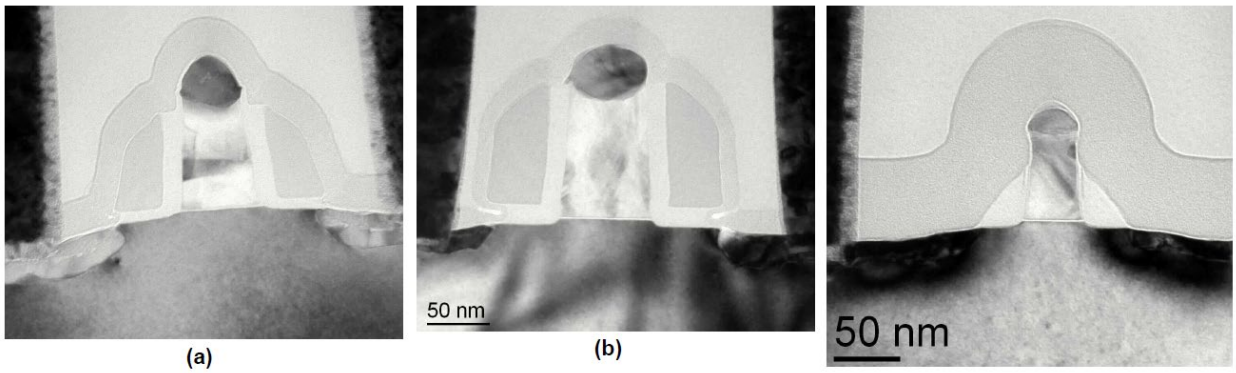


Figure 10. Transistors in (a) Xilinx Spartan-3, (b) Altera Stratix-II, (c) Transmeta Efficeon-2

James's Fig. 10

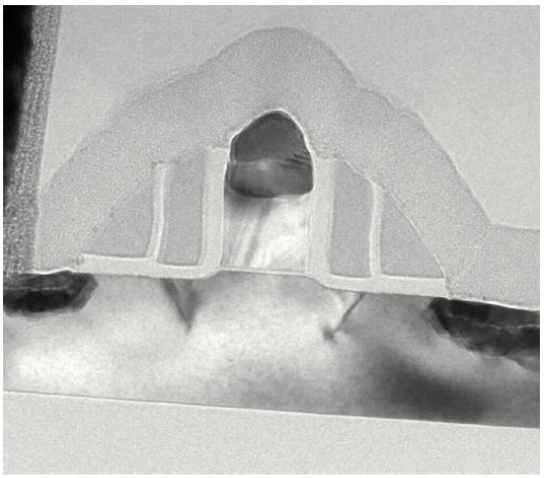


Figure 11. NMOS Transistor in AMD Athlon

James's Fig. 11

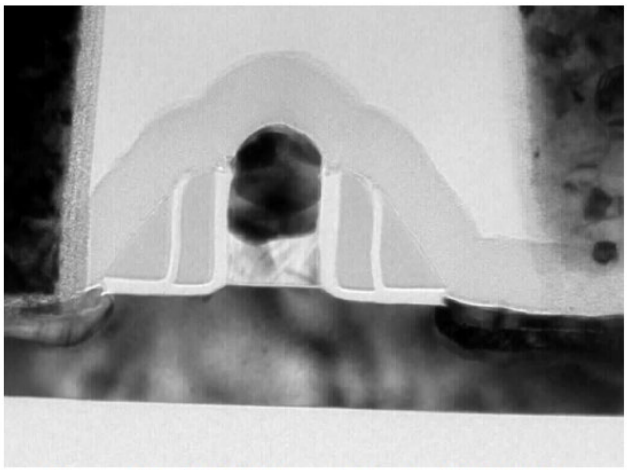


Figure 12. PMOS Transistor in AMD Athlon

James's Fig. 12

221. Thus, because there are only a finite number of identified, predictable solutions to comply with the design requirements of Aoyama's device, and because the most predictable solution would have been to make Aoyama's etch stopper film 145 thinner than Aoyama's gate electrode 104, a POSITA would have found that solution obvious.

222. **The third reason** a POSITA would have found it obvious for Aoyama's etch stopper film 145 (brown) to have a smaller thickness than gate

electrode 104 is that the disclosed thickness of Aoyama's gate electrode 104 significantly exceeds the typical thickness used for silicon nitride etch stopper films like Aoyama's etch stopper film 145.

223. I have been informed that when evidence shows techniques and conditions were routine such that a POSITA would have understood a claimed property to be "typical," it would have been obvious.

224. Aoyama discloses that gate electrode 104 is thicker than 80 nm. This is because, as I explain above, Aoyama's gate electrodes 103 and 104 are planarized to have the same total height. *See* Aoyama ¶[0119], FIG. 6Q. Aoyama discloses that conductive layer 103A is about 20 nm thick, and conductive layer 103B is about 60 nm thick, meaning gate electrode 103 (which further includes semiconductor layer (silicide layer) 103C) is thicker than 80 nm. *See* Aoyama ¶[0107]. Because gate electrode 104 must have the same thickness as gate electrode 103, gate electrode 104 is also thicker than 80 nm.

225. A POSITA would have understood that silicon nitride etch stopper films like Aoyama's etch stopper film 145 "ha[ve] a typical thickness of 20 nm" or so—much less than the 80 nm minimum thickness of Aoyama's gate electrode 104. Eneman, 1446. That is, a "typical" silicon nitride CESL thickness was less than a typical gate electrode thickness in MOSFETs like Aoyama's. *See* Nakajima ¶[0317], ¶[0326], FIG. 52; Mistry2007, Fig. 6; James, Figs. 1-3, 5-6, 8-12; Morin, Fig. 1;

Thompson2004, Fig. 2. A POSITA thus would have found it obvious that Aoyama's etch stopper film 145 is thinner than Aoyama's gate electrode 104.

226. **The fourth reason** a POSITA would have found it obvious for Aoyama's etch stopper film 145 (brown) to have a smaller thickness than gate electrode 104 is that the thickness of etch stopper film 145 affects the amount of stress, and tuning it would have been a matter of routine optimization.

227. I have been told that where claimed dimensions are known to be result-effective variables, it is not inventive to discover the optimum or workable ranges by routine experimentation. I have been told that such a claimed dimension is only patentable if it produces a new and unexpected result that differs in kind, not merely degree, from the prior art.

228. Here, silicon nitride CESL thickness was a variable known to affect stress. *See generally* Eneman. Eneman, for example, details "[t]he effect [of scaling] on CESL-induced stress" due to silicon nitride CESL films. Eneman, 1447. Silicon nitride CESL thickness was thus a known, result-effective variable. *See, e.g.*, Eneman, 1447-48, Figs. 2-3.

229. Implementing Aoyama's etch stopper film 145 to be thinner than Aoyama's gate electrode 104, as claimed, would not have yielded any unexpected results, as the relationship between silicon nitride CESL thickness and the stress it induces was known and predictable. *See generally* Eneman (including Fig. 3).

230. Applying the legal principles explained to me, this provides another reason a POSITA would have found it obvious for Aoyama's etch stopper film 145 to be thinner than Aoyama's gate electrode 104. That is, making etch stopper film 145 thinner than the gate electrode 104 would have involved nothing more than routine experimentation to discover the optimum or workable ranges of CESL thickness.

231. For all four of these additional reasons, in addition to the relative thicknesses disclosed by Aoyama's FIG. 5, it is my opinion that claim 22 would have been obvious in view of Aoyama's disclosures.

B. Ground 1B (Continued): Aoyama Renders Obvious Claims 11-15 and 18

1. Independent Claim 11

a. [11Pre]-[11B], [11D]-[11F], and [11H]-[11L]

232. Feature [11Pre] recites "[a] semiconductor device." Aoyama discloses this feature for the same reasons I provide for feature [19Pre], which also recites "[a] semiconductor device."

233. Feature [11A] recites "a first MIS transistor." Aoyama discloses this feature for the same reasons I provide for feature [19A], which also recites "a first MIS transistor."

234. Feature [11B] recites "a second MIS transistor." Aoyama discloses this feature for the same reasons I provide for feature [19B], which also recites "a second MIS transistor."

235. Feature [11D] recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Aoyama discloses this feature for the same reasons I provide for feature [19D], which also recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film."

236. Feature [11E] recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19E], which also recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative."

237. Feature [11F] recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Aoyama discloses this feature for the same reasons I provide for feature [19F], which also recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the

side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers."

238. Feature [11H] recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Aoyama discloses this feature for the same reasons I provide for feature [19H], which also recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film."

239. Feature [11I] recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19I], which also recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative."

240. Feature [11J] recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Aoyama

discloses this feature for the same reasons I provide for feature [19J], which also recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers."

241. Feature [11K] recites "the first and second metal films are made of different metal materials." Aoyama discloses this feature for the same reasons I provide for feature [19K], which also recites "the first and second metal films are made of different metal materials."

242. Feature [11L] recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Aoyama discloses this feature for the same reasons I provide for feature [19L], which also recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes."

b. [11C]: "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate" and

[11G]: "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate"

243. As I explain for features [19C] and [19G], Aoyama discloses a gate insulating film 102 identical to the gate insulating film the '686 Patent describes in

its specification: a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. *Compare* '686 Patent, 11:25-37, 29:16-24, *with* Aoyama ¶[0106]. Because Aoyama and the '686 Patent identically disclose the same gate dielectric film structure, Aoyama discloses the claimed "first gate insulating film" and "second gate insulating film" no matter how the claim is mapped. More specifically, gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's nFET region 106 discloses a "first gate insulating film" ([11C]), and gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's pFET region 105 discloses a "second gate insulating film" ([11G]).

244. Again, Aoyama's gate dielectric film 102 is identical to the gate insulating film structure the '686 Patent discloses: a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. The '686 Patent discloses "an underlying film . . . made of a silicon oxide film having a thickness of about 0.8 to 1 nm" and "a gate insulating film formation film 13 made of, for example, a high-k film having a thickness of 2 nm." '686 Patent, 11:25-37. According to the '686 Patent, "examples of the gate insulating film formation film 13 . . . include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON)." '686 Patent, 29:16-24. As FIG. 5 shows below, Aoyama identically discloses "a silicon oxide film . . . 102A with a thickness of 0.5 to 0.8 nm" and

"a hafnium silicon oxynitride film 102B" "with a thickness of about 2.0 nm." Aoyama ¶[0106].

245. If only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," either Aoyama's gate dielectric film 102A alone or Aoyama's gate dielectric film 102B alone in Aoyama's nFET region 106 also discloses a "first gate insulating film." Likewise, either Aoyama's gate dielectric film 102A alone or Aoyama's gate dielectric film 102B alone in Aoyama's pFET region 105 also discloses a "second gate insulating film."

c. [11M]: "the conductive film is made of a silicon film"

246. As I explain for feature [19H] above and further explain for feature [11N] in the section below, Aoyama's semiconductor layer (silicide layer) 103C comprises a "polysilicon or amorphous silicon" layer and a "Ni monosilicide (NiSi)" layer. Aoyama ¶[0107], ¶[0114]. Aoyama's silicon layer (silicide layer) 103C is thus just like the uppermost portion of gate electrode 30B in the '686 Patent—a polysilicon or amorphous silicon layer in which a nickel silicide layer is formed. The table below compares Aoyama's disclosures with the relevant written descriptions in the '686 Patent:

Aoyama	'686 Patent
¶[0107]: "[A] semiconductor layer 103C made of polysilicon or amorphous silicon is deposited . . . ." **¶[0109]:** "[S]emiconductor layer 103C . . . [is] processed using a dielectric film 202 as a hard mask" such that "a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105 . . . ."	**11:50-67:** "[A] silicon film 15 made of, for example, a polysilicon film" is patterned into "a second silicon film 15b" in the pFET active region. **29:41-45**: "[A]lthough a polysilicon film is used as the silicon film 15 . . . , a silicon film made of other semiconductor materials, such as an amorphous silicon film, a silicon film and the like, may be used."
¶[0114]: "Ni monosilicide (NiSi) is formed in" the pFET portion of semiconductor layer 103C.	**21:25-35:** "[A] metal silicide film 34 made of nickel silicide [is formed] in an upper portion of the second silicon film 15b."

247. The silicon portion of semiconductor layer (silicide layer) 103C—i.e., the semiconductor layer "made of polysilicon or amorphous silicon" (Aoyama ¶[0107])—constitutes the claimed "conductive film" for purposes of claim 11.

248. Aoyama explains that gate electrode 103 is conductive (i.e., has low resistance) due to semiconductor layer (silicide layer) 103C: "[G]ate electrode 103 for the PMOSFET includes . . . semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). ***For this reason,*** in the third embodiment, ***the gate resistance of the PMOSFET is relatively low.***" Aoyama ¶[0121] (emphases added). To a POSITA, this indicates that semiconductor layer (silicide layer) 103C and its constituent layers—including the semiconductor layer (made of silicon)—are conductive. A POSITA also would have understood more generally that such silicon

films are conductive when used in gate electrodes. *See, e.g.*, Aoyama ¶[0007] ("Polysilicon is widely adopted as a material for forming a gate electrode in a conventional FET.").

d. [11N]: "the semiconductor device further comprises a metal silicide film formed on the silicon film"

249. Aoyama discloses "the semiconductor device further comprises a metal silicide film formed on the silicon film."

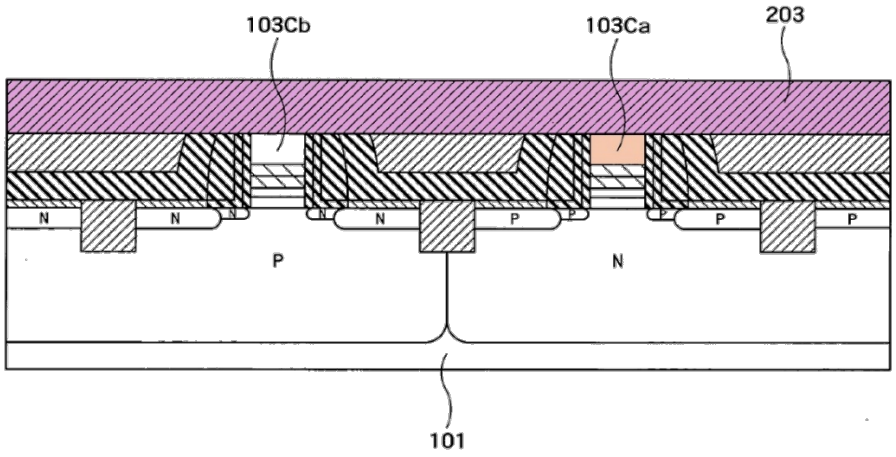


FIG. 6L

Aoyama's FIG. 6L (annotated)

250. As Aoyama's FIG. 6L shows above, sacrificial nickel layer 203 (purple) is formed over the entire surface, including in contact with layer 103Ca (peach, the portion of semiconductor layer 103C in the pFET gate electrode). Aoyama ¶[0108], ¶[0114]. Upon annealing, "Ni monosilicide (NiSi) is formed ***in***" layer 103Ca. Aoyama ¶[0114] (emphasis added).

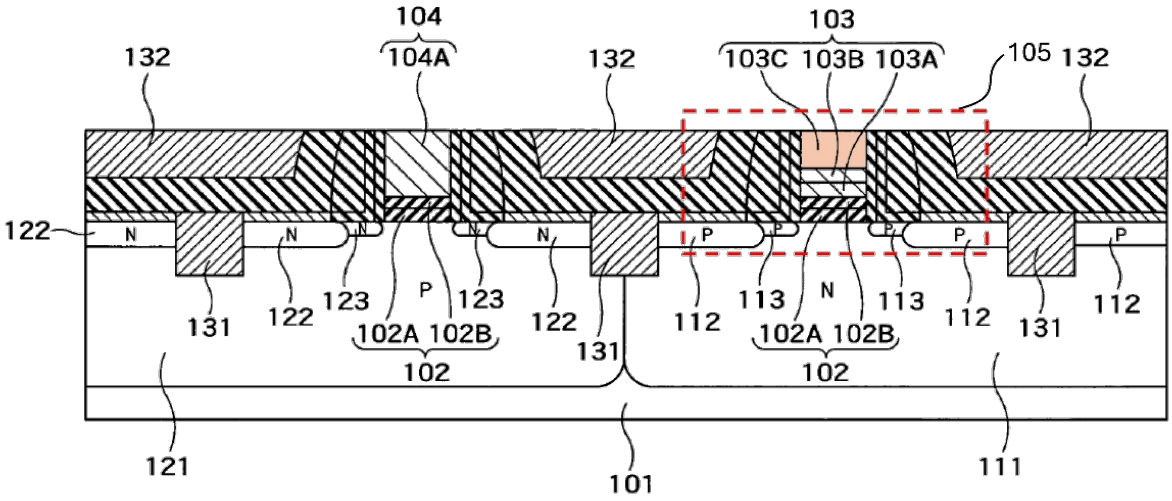


FIG. 5

Aoyama's FIG. 5 (annotated)

251. Thus, in Aoyama's final structure, as FIG. 5 illustrates above, Aoyama's "gate electrode 103 for the PMOSFET includes . . . the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide)." Aoyama ¶[0121].

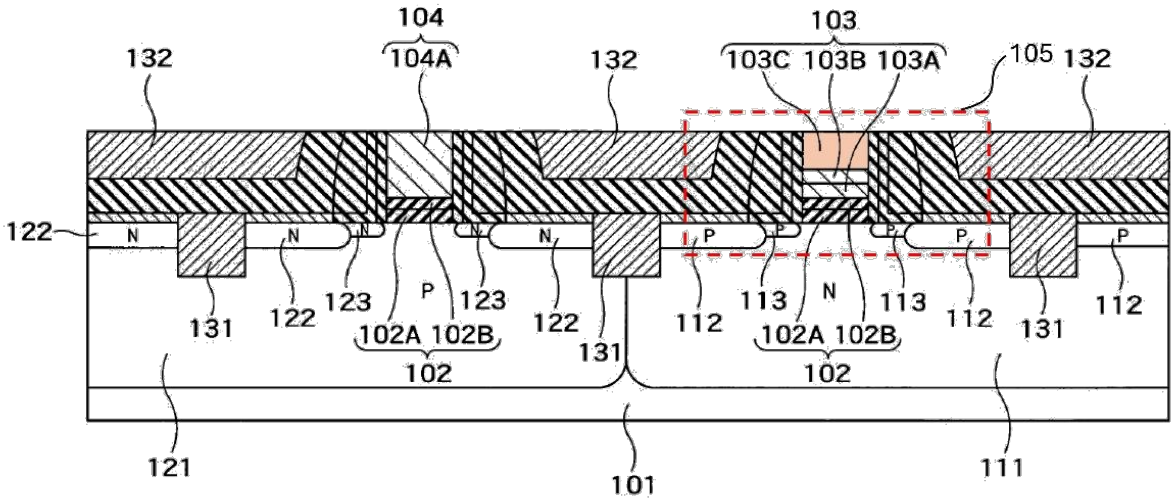


FIG. 5

Aoyama, FIG. 5 (annotated)

105

252. A POSITA would have recognized, or at least found obvious, from Aoyama's descriptions that when the NiSi forms "in" semiconductor layer 103C, semiconductor layer 103C is not entirely consumed. When initially formed, Aoyama describes semiconductor layer 103C as "a semiconductor layer 103C which is made of [a] semiconductor," such as "polysilicon." Aoyama ¶[0098], ¶[0107]. Aoyama then teaches that layer 103C is subjected to a silicidation process, such that "Ni monosilicide (NiSi) is formed ***in***" the portion of semiconductor layer 103C used for the pFET gate electrode. Aoyama ¶[0114] (emphasis added).

253. A POSITA would have been very familiar with the textbook silicidation process Aoyama describes. The resulting silicide is not a semiconductor material but a metal material. As one textbook explains, "[a] *silicide* is a metal compound that is thermally stable and provides for low electrical resistivity at the silicon/refractory metal interface." Quirk, 309.

254. In the final structure, Aoyama refers to ***semiconductor*** layer 103C as "the ***semiconductor*** layer (silicide layer)," thereby emphasizing it is still a semiconductor layer but that a silicide layer has been added. Aoyama ¶[0121] (emphasis added). Because silicide forms "***in***" semiconductor layer 103C and Aoyama refers to ***semiconductor*** layer 103C as a "semiconductor layer (silicide layer) 103C," a POSITA would have immediately understood, or at least found obvious, that a silicided region is formed in the uppermost part of semiconductor

layer 103C. Aoyama ¶[0114], ¶[0121] (emphasis added). That is, although not shown in FIG. 5, a POSITA would have understood semiconductor layer (silicide layer) 103C may be a layer of polysilicon capped by NiSi—the textbook structure that results from the silicidation process Aoyama describes. *See, e.g.*, Quirk, FIG. 12.9.

255. In fact, Aoyama's disclosures are identical to what the '686 Patent discloses in this regard. The '686 Patent discloses "a silicon film 15 made of, for example, a polysilicon film" that is patterned into "a second silicon film 15b" in the pFET active region. '686 Patent, 11:50-67; *see also* '686 Patent, FIGS. 1B-1C. "[A]lthough a polysilicon film is used as the silicon film 15 . . . , a silicon film made of . . . an amorphous silicon film . . . may be used." '686 Patent, 29:41-45. This is just like Aoyama's "semiconductor layer 103C made of polysilicon or amorphous silicon," which is patterned to form "gate electrode 103 for the PMOSFET." Aoyama ¶[0107], ¶[0109]; *see also* Aoyama, FIG. 6G.

256. The '686 Patent then discloses that "a metal film (not shown) made of, for example, nickel having a thickness of 10 nm is deposited on an entire surface of the semiconductor substrate." '686 Patent, 21:25-30. "Thereafter, Si in the second silicon film 15b and Ni in the metal film are caused to react with each other by, for example, a first RTA treatment . . . to form a metal silicide film 34 made of nickel silicide ***in*** an upper portion of the second silicon film 15b." '686 Patent, 21:30-35

(emphasis added). This is the same language Aoyama uses to describe the silicidation of semiconductor layer 103C. Like the '686 Patent, Aoyama discloses that "a Ni (nickel) film (sacrificial film) 203 is formed over the entire surface." Aoyama ¶[0114]. "After that, the substrate 101 is subjected to annealing" such that "Ni monosilicide (NiSi) is formed ***in***" semiconductor layer 103C. Aoyama ¶[0114] (emphasis added). Aoyama refers to this composite structure as a "semiconductor layer (silicide layer) 103C" (Aoyama ¶[0121]), which is analogous to silicon layer 15b of the '686 Patent once silicide layer 34 is formed "in" silicon layer 15b. '686 Patent, 21:25-35.

257. A POSITA would have understood from Aoyama's disclosure that there are only two options for the silicidation process that Aoyama describes: the semiconductor layer 103C is partially silicided, or semiconductor layer 103C is completely silicided. Partial silicidation was not just known but ***textbook***, and therefore would have been obvious. *See* Quirk, FIGS. 12.9-12.10; *see also* Chang, 13:39-49 ("[S]ilicon region 920 is partially silicided . . . . Alternatively, the entire silicon region can be silicided."), FIG. 9. I have been told that when there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. I have also been told that two options constitute a finite number of identified, predictable solutions, and I agree in the context at issue here (i.e., whether or not Aoyama's

semiconductor layer 103C in pFET region 105 is partially or completely silicided—the former being the textbook solution).

258. Aoyama's NiSi layer thus discloses, or at least renders obvious, "a metal silicide film formed on the silicon film" as claimed.

e. [11O]: "the silicon nitride film has a thickness smaller than that of the first gate electrode"

259. Aoyama discloses and renders this feature obvious for the same reasons I explain regarding claim 22. *See* Section IX.A.4 above.

2. Claim 12

260. Claim 12 depends from claim 11. I understand that means claim 12 requires all the same features as claim 11, plus the additional features recited in claim 12. Aoyama renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

261. Aoyama discloses the addition limitations of claim 12 for the same reasons I explain regarding claim 20 in Section IX.A.2 above.

3. Claim 13

262. Claim 13 depends from claim 11. I understand that means claim 13 requires all the same features as claim 11, plus the additional features recited in claim 13. Aoyama renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

263. Aoyama discloses the addition limitations of claim 13 for the same reasons I explain regarding claim 21 in Section IX.A.3 above.

4. Claim 14

264. Claim 14 depends from claim 11. I understand that means claim 14 requires all the same features as claim 11, plus the additional features recited in claim 14. Aoyama renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

265. Aoyama further discloses "wherein the first and second gate insulating films are made of the same insulating material." Aoyama discloses a gate insulating film 102 identical to the gate insulating film the '686 Patent describes in its specification: a 2 nm-thick hafnium silicon oxynitride film formed on a 0.8 nm-thick silicon oxide film. *Compare* '686 Patent, 11:25-37, 29:16-24, *with* Aoyama ¶[0106]. Because Aoyama and the '686 Patent identically disclose the same gate dielectric stack, Aoyama discloses that "the first and second gate insulating films are made of the same insulating material" no matter how the claim is mapped.

266. As I explain for feature [11C], gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's region 106 discloses a "first . . . gate insulating film[]."

267. Likewise, as I explain for feature [11G], gate dielectric film 102 (including both gate dielectric films 102A and 102B) in Aoyama's region 105 discloses a "second gate insulating film."

268. Because the claimed "first gate insulating film" and "second gate insulating film" are both disclosed by Aoyama's gate dielectric film 102 (including both gate dielectric films 102A and 102B), Aoyama's "gate insulating films are made of the same insulating material." The gate dielectric film 102 in PMOSFET region 105 is made from the same silicon oxide film 102A and the same hafnium silicon oxynitride dielectric film 102B as the gate dielectric film 102 in NMOSFET region 106. Aoyama ¶[0106], ¶[0109].

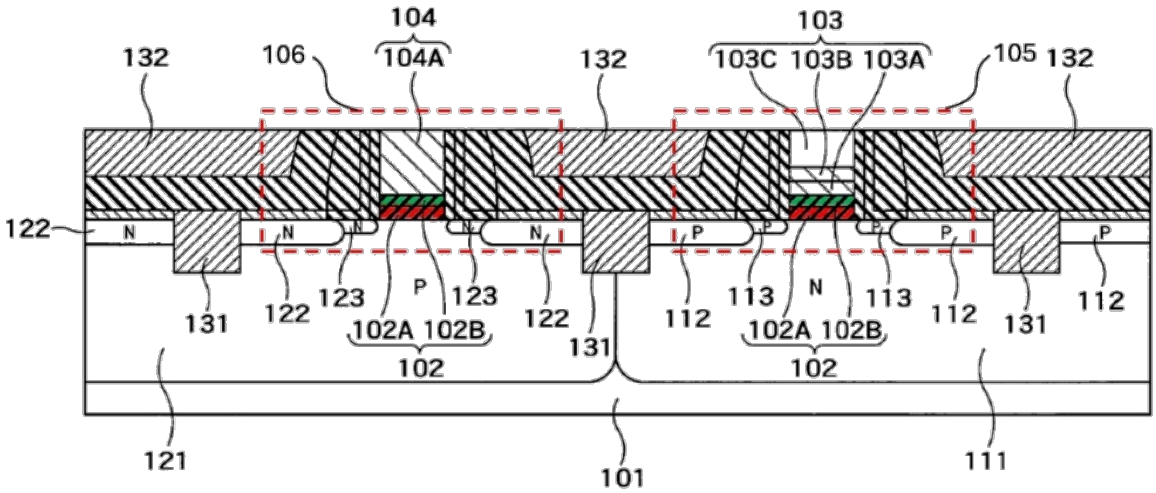


FIG. 5

Aoyama's FIG. 5 (annotated)

5. Claim 15

269. Claim 15 depends from claim 11. I understand that means claim 15 requires all the same features as claim 11, plus the additional features recited in claim 15. Aoyama renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

270. If only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," Aoyama further discloses "wherein the first and second gate insulating films are made of different insulating materials."

271. As I explain for feature [11C], if only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," either Aoyama's gate dielectric film 102A alone or Aoyama's gate dielectric film 102B alone in nFET region 106 discloses a "first gate insulating film."

272. Likewise, as I explain for feature [11G], if only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," either Aoyama's gate dielectric film 102A alone or Aoyama's gate dielectric film 102B alone in region 105 discloses a "second gate insulating film."

273. Under a first mapping for claim 15, Aoyama's gate dielectric film 102A in nFET region 106 discloses the "first . . . gate insulating film[]," and Aoyama's gate dielectric film 102B in pFET region 105 discloses the "second gate insulating film[]."

274. Under a second mapping for claim 15, Aoyama's dielectric film 102B in nFET region 106 discloses the "first gate insulating film," and Aoyama's gate dielectric film 102A in pFET region 105 discloses the "second gate insulating film."

275. Under either of these two mappings, Aoyama's "gate insulating films are made of different insulating materials." One is made of the silicon oxide of gate dielectric film 102A, and the other is made of the hafnium silicon oxynitride of gate dielectric film 102B. Aoyama ¶[0106].

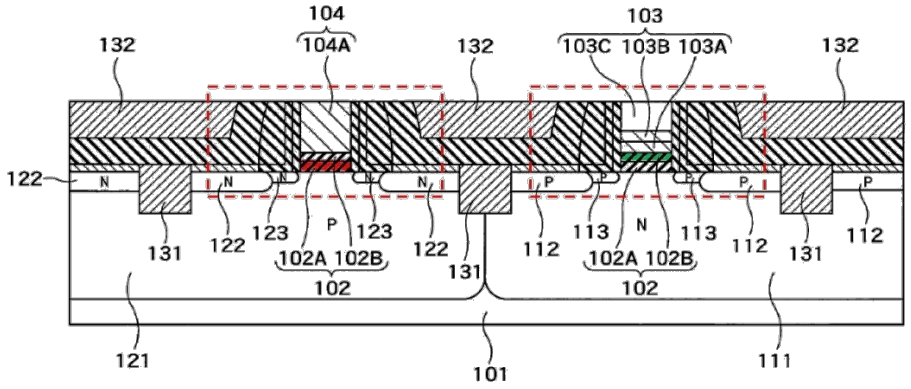


FIG. 5

Aoyama's FIG. 5 (annotated first mapping)

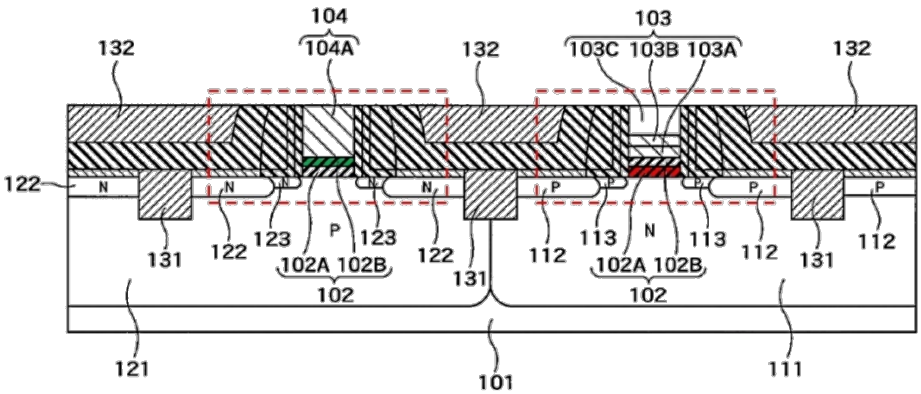


FIG. 5

Aoyama's FIG. 5 (annotated second mapping)

113

6. Claim 18

276. Claim 18 depends from claim 11. I understand that means claim 18 requires all the same features as claim 11, plus the additional features recited in claim 18. Aoyama renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

277. Aoyama further discloses "the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more."

278. As I explain for feature [11C], Aoyama's gate dielectric film 102 (including both gate dielectric films 102A and 102B) in nFET region 106 discloses the claimed "first gate insulating film." *See* Section IX.B.1.b above.

279. Likewise, as I explain for feature [11G], Aoyama's gate dielectric film 102 (including both gate dielectric films 102A and 102B) in pFET region 105 discloses the claimed "second gate insulating film." *See* Section IX.B.1.b above.

280. Aoyama's gate dielectric film 102B is formed of hafnium silicon oxynitride. Aoyama ¶[0106]. A POSITA would have understood that Aoyama's gate dielectric film 102B discloses, or at least renders obvious, the claimed "high-k film made of a metal oxide having a relative dielectric constant of 10 or more."

281. A POSITA would have recognized that hafnium silicon oxynitride is "a high-k film" because Aoyama refers to it as "a high-permittivity dielectric film,"

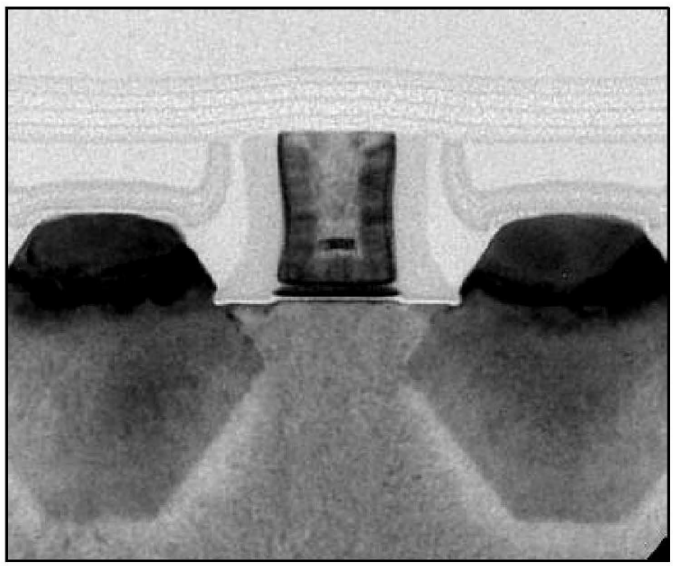
which is synonymous with "a high-k film" (k or κ being the symbol for dielectric permittivity). Aoyama ¶[0098]; *see also* Akasaka939 ¶[0004] (explaining that "[a] high dielectric constant film made of the above-noted high-k material [referring to hafnium silicon oxynitride] has its dielectricity of more than ten (10)").

282. According to the '686 Patent, hafnium silicon oxynitride is a "metal oxide having a relative dielectric constant of 10 or more." In fact, hafnium silicon oxynitride is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicon oxynitride (HfSiON) . . . ." '686 Patent, 29:16-24. Aoyama's hafnium silicon oxynitride is "a high-permittivity dielectric film." Aoyama ¶[0098]. A POSITA would have understood it has a dielectric constant of 10 or more. *See* Akasaka939 ¶[0004] ("[C]ertain films which are made of hafnium (Hf)-containing material such as HfO_2, $HfSiO_x$, or $HfAlO_x$, and oxynitrides thereof are relatively excellent in thermal stability. . . . A high dielectric constant film made of the above-noted high-k material has its dielectricity of more than ten (10) . . . ."); Baklanov, xiii ("Dielectrics with values approximately between 10 and 30 are under consideration."); Kavalieros ¶[0002] (explaining that a "high-k dielectric means having a dielectric constant higher than 10"), ¶[0008] (similar).

C. Ground 1C: The Aoyama-Hsu823 Combination Renders Obvious Claims 1-3, 5-10, 16-17, 23-28, and 30-35

1. A POSITA would have found it obvious to implement SiGe stressors in the source/drain regions of Aoyama's pFET

283. By the time the application for the '686 Patent was filed, SiGe stressors had already been known and used in three generations of high-volume commercial transistors. *See* Thompson2004, 1790-91 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry2007, 247-48 (describing Intel's 45nm devices); Mistry_Presentation (same). The most recent generation prior to the filing date of the '686 Patent, shown publicly in images like the one below before the application for the '686 Patent, not only used SiGe stressors but also high-κ gate dielectrics and metal gates in an RMG process. *See generally* Mistry2007; Mistry_Presentation, 14-19. By the time the application for the '686 Patent was filed, such SiGe stressors were standard industry practice. *See* Section VI.D above.

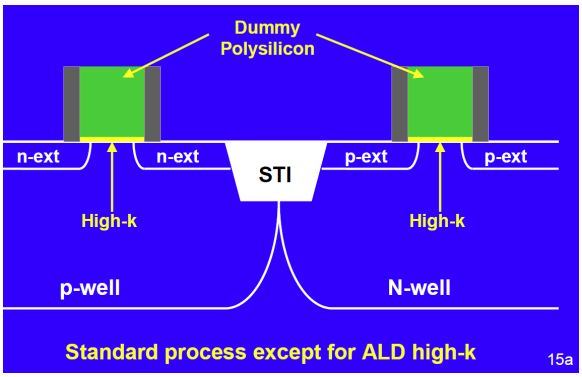


Mistry2007's Fig. 6

284. Although Aoyama may not expressly describe using SiGe stressors, it would have been obvious to use SiGe stressors in Aoyama's FIG. 5 transistor design, as the micrograph above—showing Intel's high-volume 45nm generation of devices that had been in production since 2007—should make abundantly clear. Mistry2007, Fig. 6; *see also* Mistry_Presentation, 16.

285. At the December 2007 International Electron Devices Meeting ("IEDM")[13] in Washington, D.C., which I attended and for which I organized a short course and two speakers on high-κ/metal-gates, Kaizad Mistry of Intel described Intel's 45 nm process flow. Again, it was a high-κ/RMG process. *See generally* Mistry_Presentation, 14-19 (in-person IEDM presentation); Mistry2007 (publication of related IEDM paper).

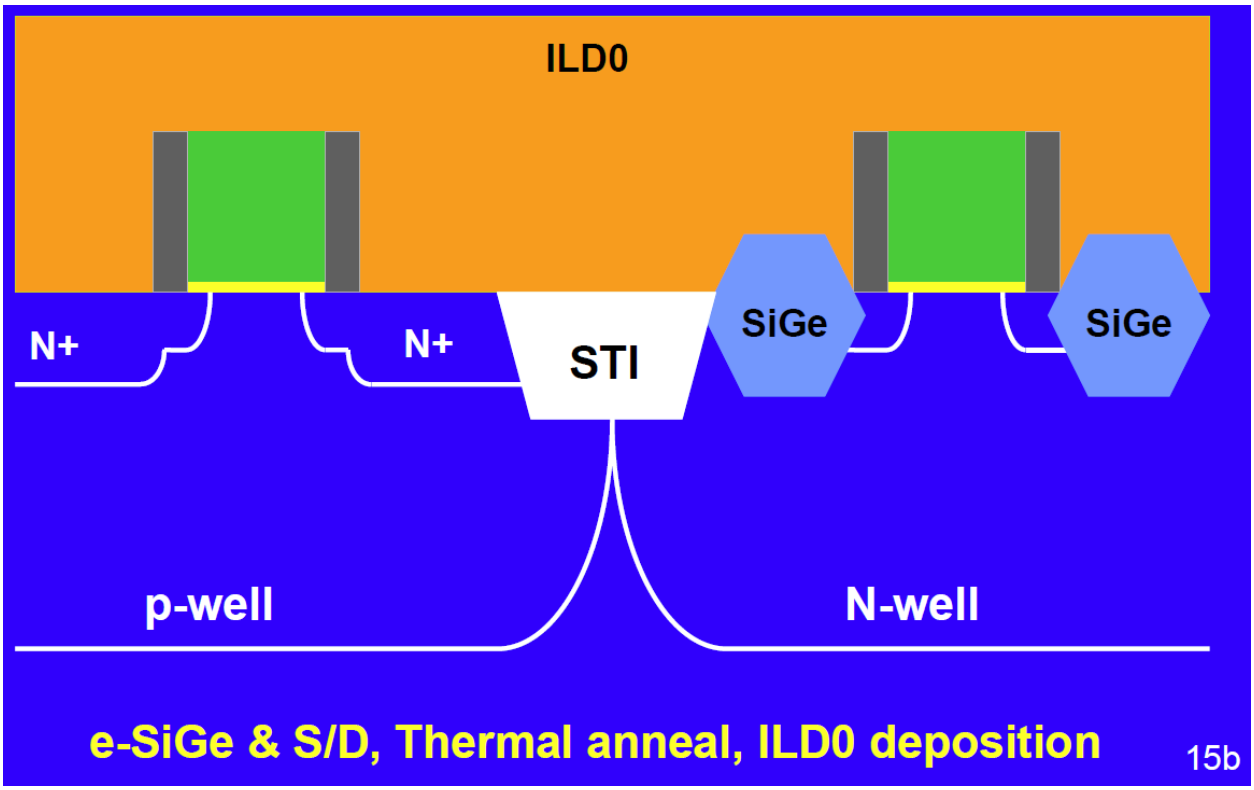
286. To begin, nFET and pFET dummy gate structures are formed. The dummy gates comprise high-κ dielectrics (yellow) and dummy polysilicon gate electrodes (green). Mistry_Presentation, 15a (below).



Mistry_Presentation, 15a

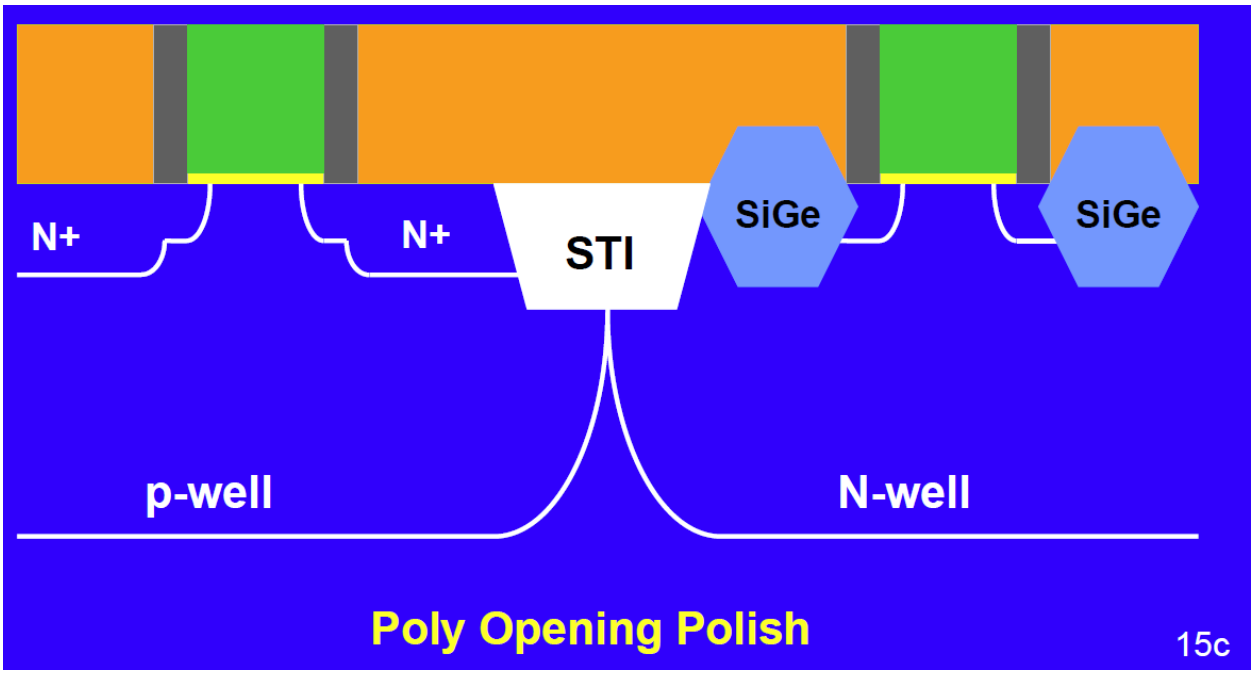
[13] IEDM is a very prominent and well attended conference in the field.

287. Next, the source/drain regions are formed, including the formation of embedded epitaxial SiGe source/drain regions for the pFET (light blue hexagons). *See* Section VI.D above. This is followed by thermal annealing to activate implanted dopants and then by a blanket deposition of interlayer dielectric ILD0 (orange), as shown below. Mistry_Presentation, 15b.



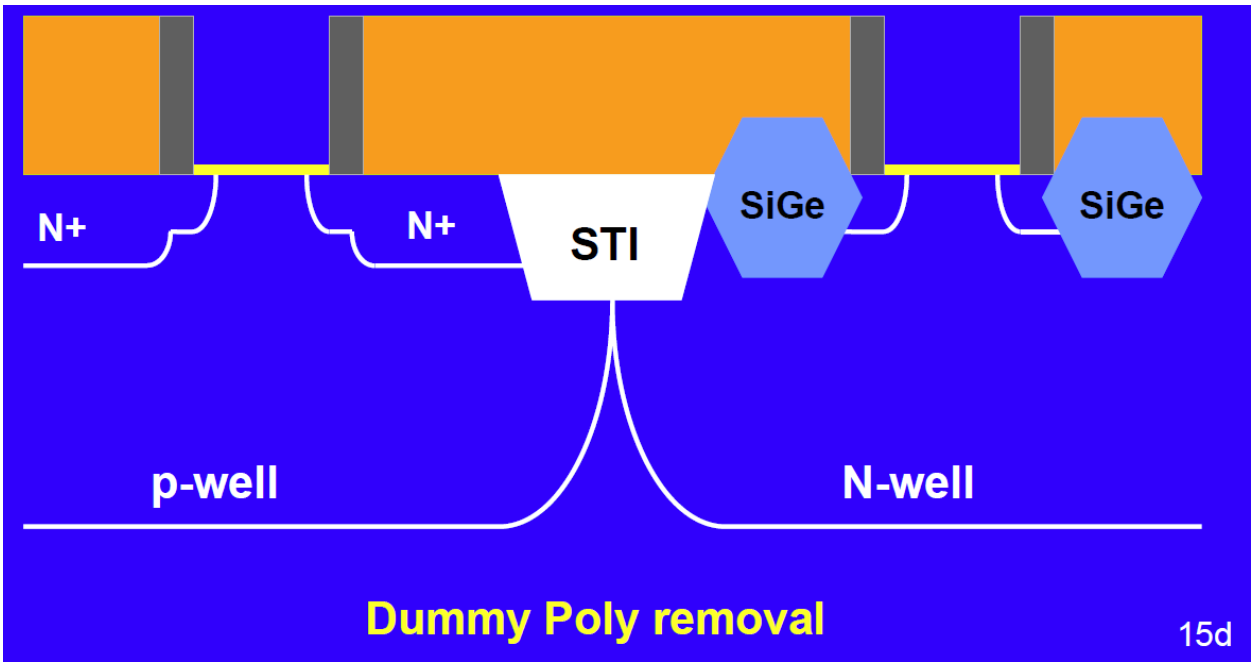
Mistry_Presentation, 15b

288. Following this, a polishing step is performed to planarize interlayer dielectric ILD0 (orange) such that its top surface aligns with the top surfaces of the dummy polysilicon gate electrodes (green). Mistry_Presentation, 15c.



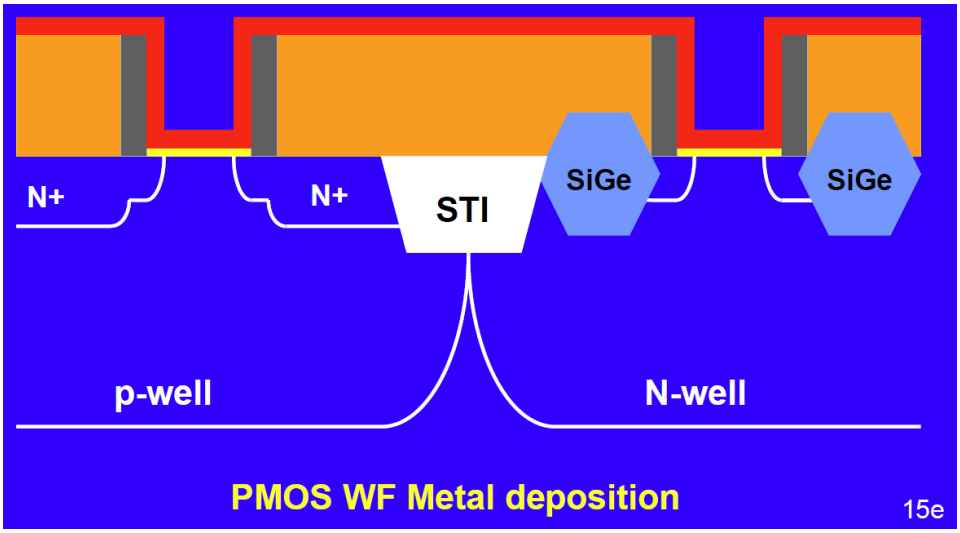
Mistry_Presentation, 15c

289. Next, the dummy polysilicon gate electrodes (green) are removed by etching. Mistry_Presentation, 15d.



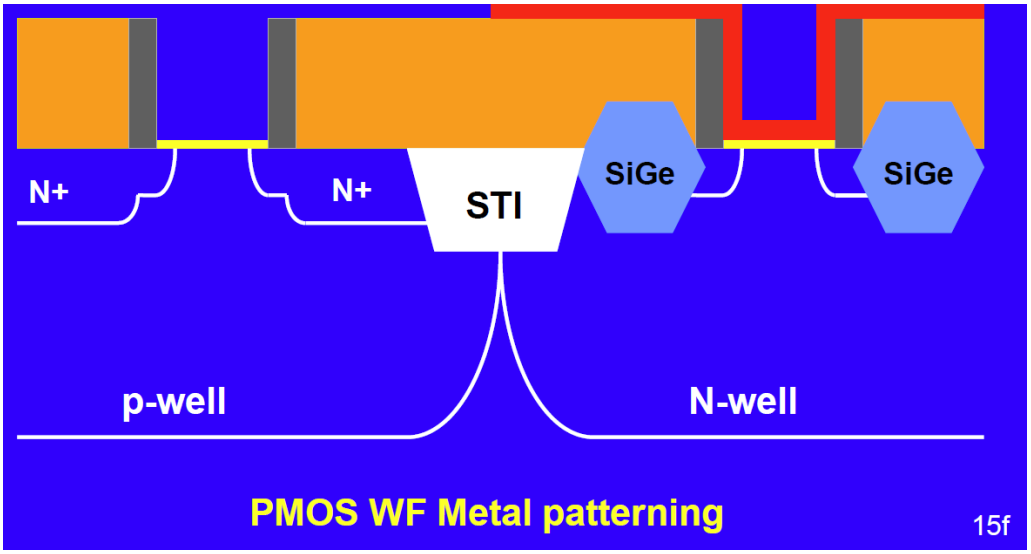
Mistry_Presentation, 15d

290. The pFET work-function metal (red) is then deposited over the wafer, including in the void left by removing the dummy polysilicon gate electrodes. Mistry_Presentation, 15e.



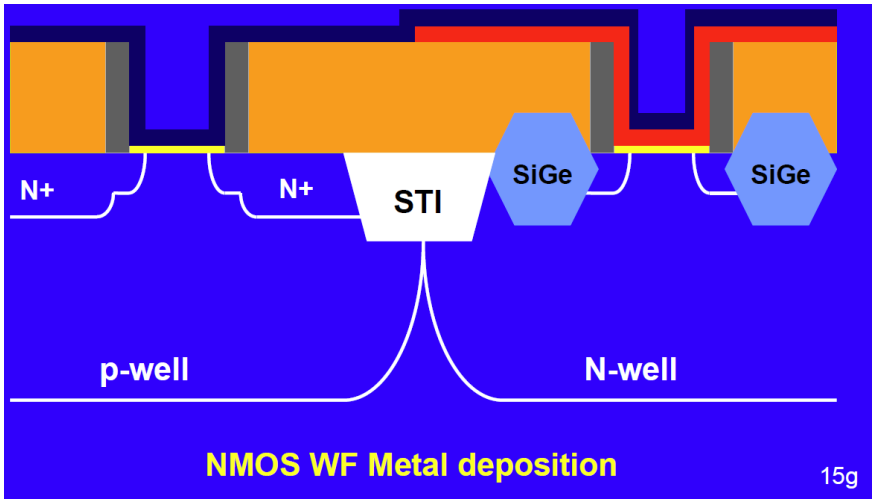
Mistry_Presentation, 15e

291. Because this is the pFET work-function metal, it is removed from the wafer by etching everywhere except in the pFET regions. Mistry_Presentation, 15f.



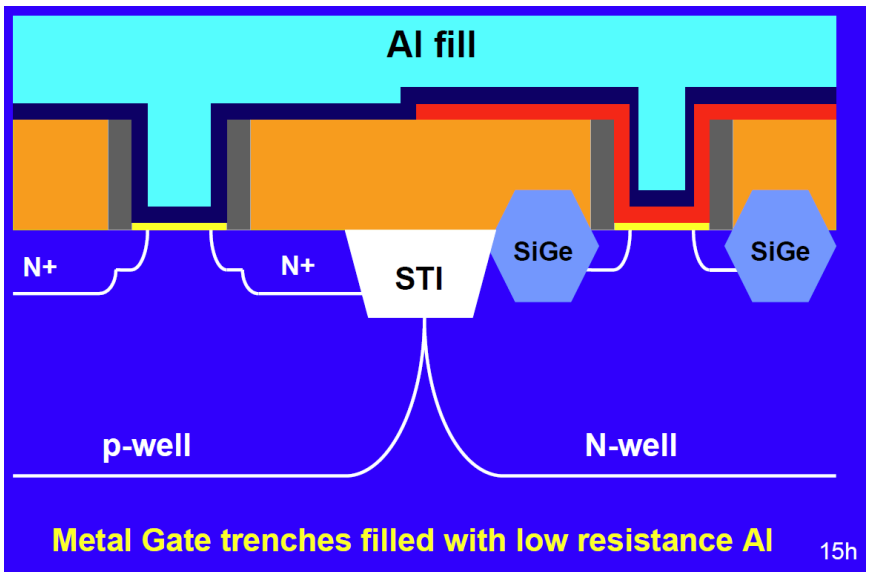
Mistry_Presentation, 15f

292. Next, the nFET work-function metal (dark blue) is deposited over the wafer, including in the voids left by removing the dummy polysilicon gate electrodes. Mistry_Presentation, 15g.



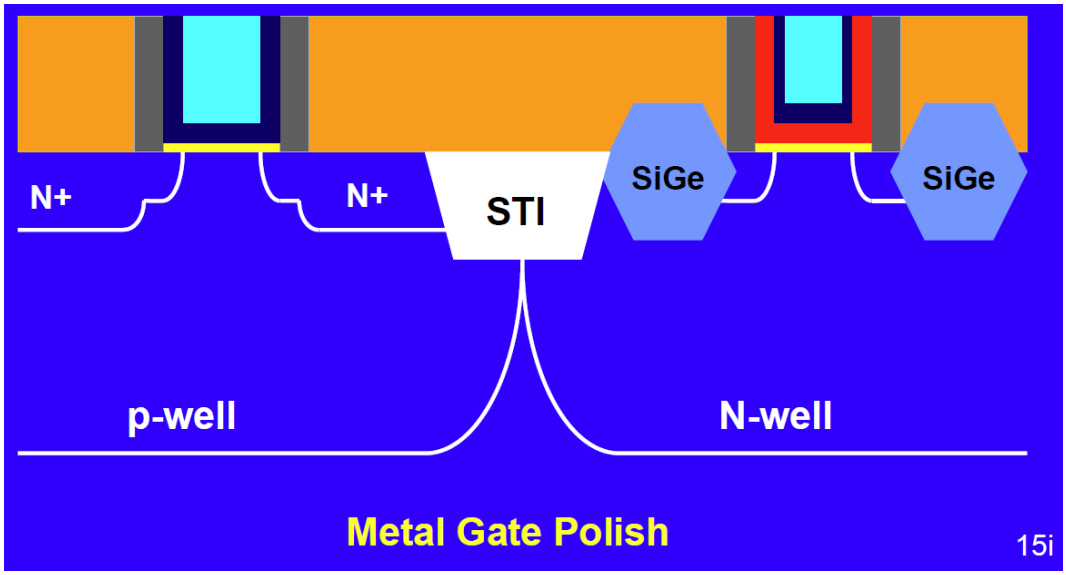
Mistry_Presentation, 15g

293. Then, an aluminum filler (turquoise) is deposited over the entire wafer to fill the remaining voids left in the nFET and pFET gate electrode regions. Mistry_Presentation, 15h.

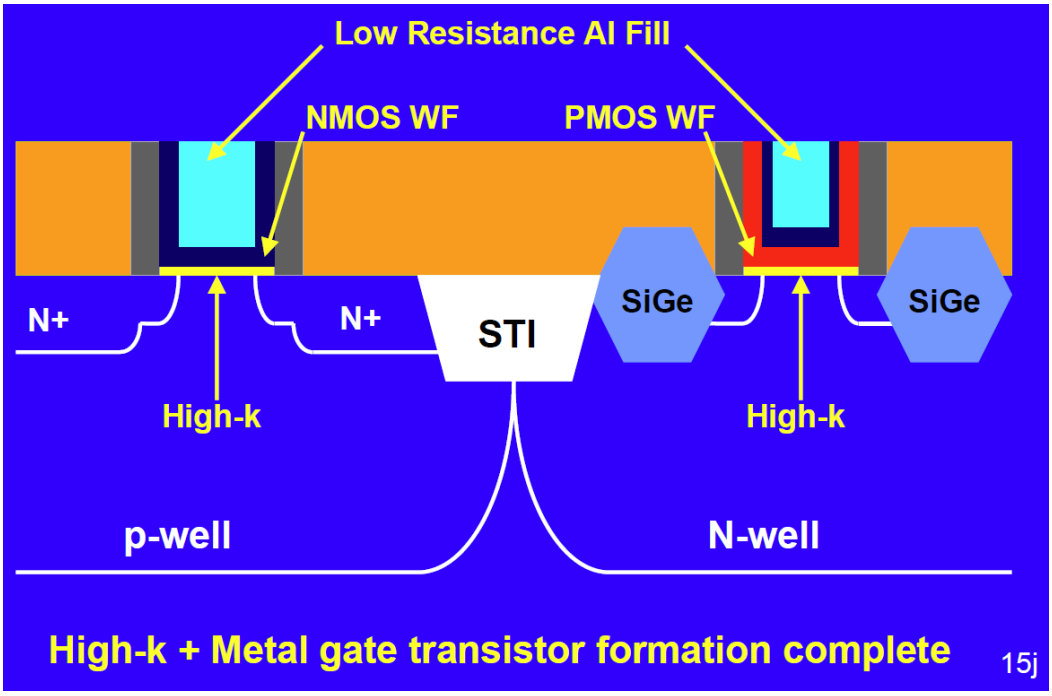


Mistry_Presentation, 15h

294. A second polishing step is done to planarize the metal films such that the top surfaces of the replacement metal gate electrodes are aligned with the top surface of interlayer dielectric film ILD0 (orange). Mistry_Presentation, 15i-15j.

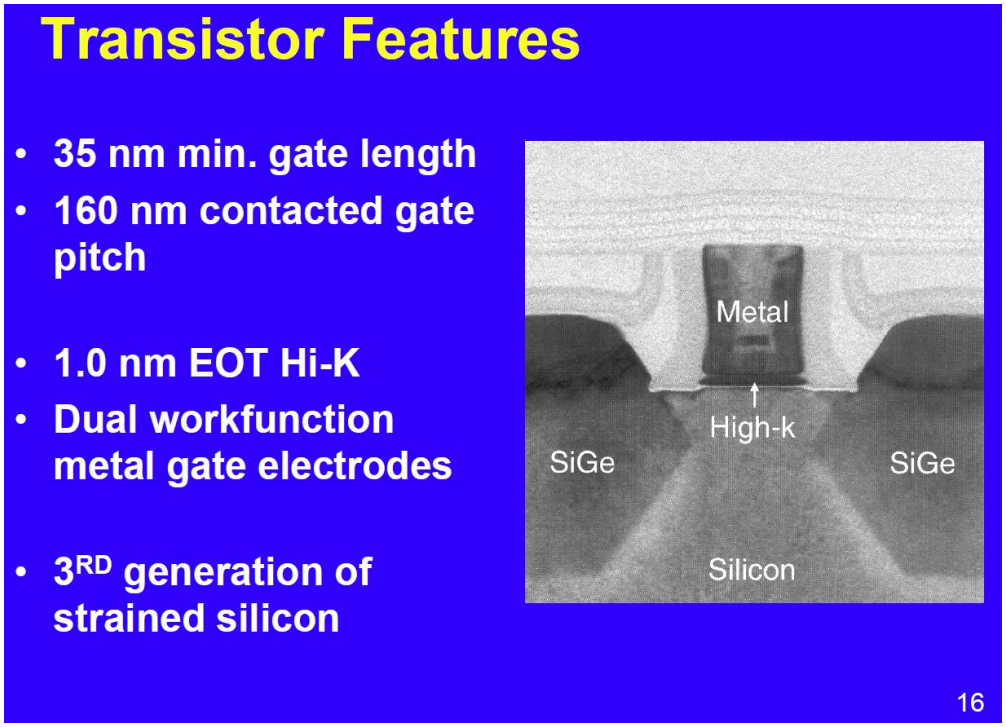


Mistry_Presentation, 15i

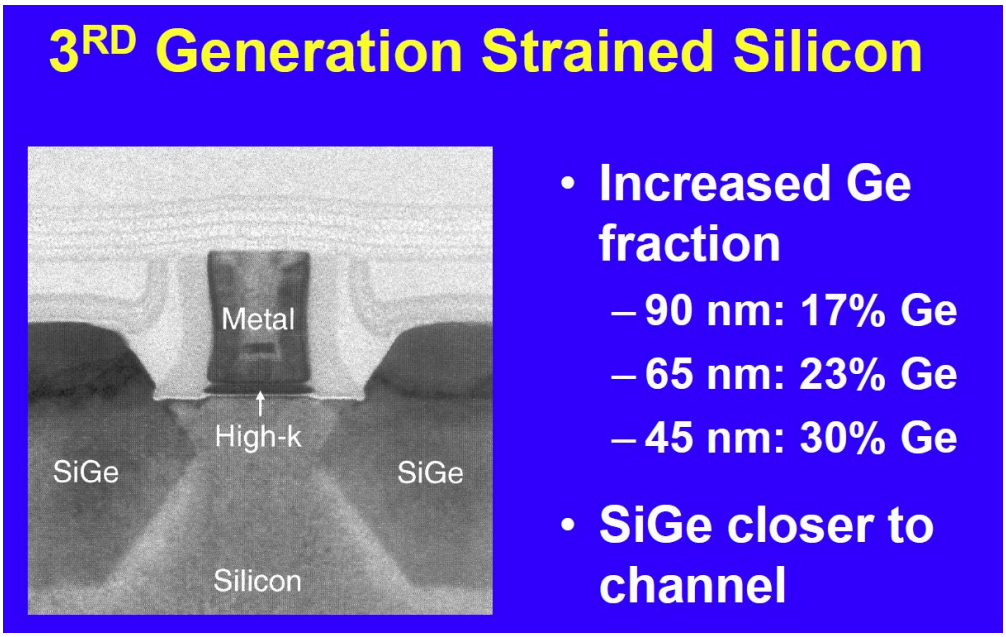


Mistry_Presentation, 15j (same as 15i but with additional labels)

295. The final structure made using Intel's 45 nm high-κ/RMG process appears below. Mistry_Presentation, 16, 19.



Mistry_Presentation, 16 (micrograph showing a pFET)



Mistry_Presentation, 19 (micrograph showing a pFET)

296. As the above presentation demonstrates, epitaxial SiGe had been fully integrated with high-κ/RMG technology in Intel's high-volume commercial 45nm products, and that was common knowledge in the industry well before the application for the '686 Patent was filed. *See generally* Mistry2007; Mistry_Presentation. Given the stark similarity between Intel's 45 nm process above and the process used to make Aoyama's third embodiment (Aoyama ¶¶[0097]-[0121], FIGS. 5-6Q), there is no question a POSITA would have found it obvious to integrate epitaxial SiGe into Aoyama's third embodiment.

297. Although the commercial adoption of SiGe stressors by Intel demonstrates both motivation to use such technology and a reasonable expectation of success, there is no shortage of other literature explaining why that is. For example, as an alternative to forming pFET source/drain regions solely by ion implantation, Hsu823 teaches to form SiGe stressors 218 in trenches of pFET active regions to induce compressive stress in the pFET channel region. Hsu823 explains that, in one embodiment, "source/drain regions 120 and 220 are formed [only] by implanting impurities into semiconductor substrate 30." Hsu823 ¶[0032]. As an alternative, Hsu823 teaches that SiGe stressors may be used:

> In alternative embodiments, as shown in FIG. 7B, SiGe stressors 218 are formed in PMOS region 200. Preferably, a photo resist 121 is formed covering NMOS region 100. Recesses are formed in substrate 30 along the outside edges of the spacers 216, preferably by etching. SiGe stressors 218 are then formed in the recesses. In the

> preferred embodiment, SiGe stressors 218 are epitaxially grown. P-type impurities such as boron are preferably doped during the epitaxial growth. The photo resist 121 is then removed. After being annealed, SiGe stressors 218 will try to restore their lattice spacing, which is greater than the lattice spacing of the substrate 30. This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.

Hsu823 ¶[0033]. Hsu823's FIGS. 7A and 7B show this below.

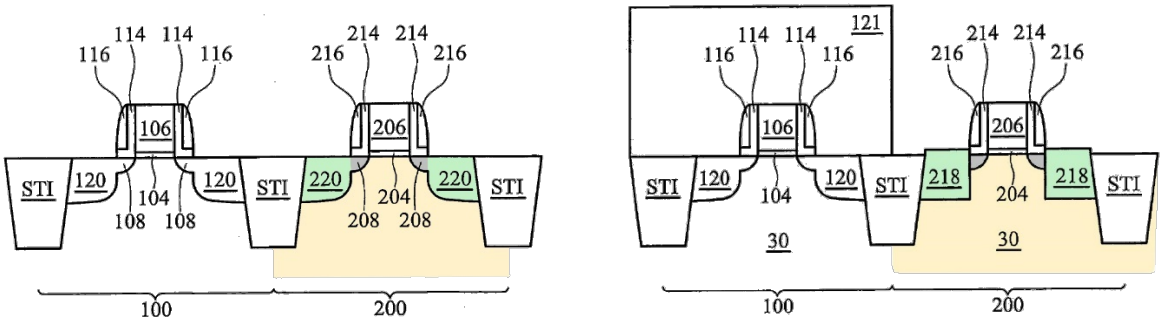


FIG. 7A FIG. 7B

Hsu823's FIGS. 7A and 7B (annotated)

298. A POSITA would have found it obvious to modify the pFET in Aoyama's FIG. 5 by using epitaxial SiGe stressors, as Hsu823 discloses (and as Intel's public disclosures confirm), to form Aoyama's pFET source/drain regions 112.

299. A POSITA would have been motivated to do so because SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. *See* Section VI.D above. As Hsu823 explains, SiGe stressors "introduce[] compressive stress[] in the . . . channel region[]" such that the "device drive current[] of the . . . PMOS device[] [is] increased." Hsu823 ¶[0033]. Again, this was already

standard industry practice when the application for the '686 Patent was filed, as Hsu823 further confirms:

> Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design. Research has revealed that . . . a compressive stress parallel to the channel length direction can improve PMOS device performance.

Hsu823 ¶¶[0002]-[0003].

300. A POSITA would have reasonably expected to succeed in implementing Hsu823's SiGe stressors in Aoyama's FIG. 5 semiconductor device because such SiGe crystal layers were known and widely used to induce compressive stress in pFETs. *See* Section VI.D above. The structure in Aoyama's FIG. 6I is materially the same as the structure in Hsu823's FIG. 7A. *Compare* Aoyama ¶¶[0103]-[0111], FIG. 6I, *with* Hsu823 ¶¶[0028]-[0032], FIG. 7A. As I explain above, Hsu823 teaches (and the Intel disclosures confirm) that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Hsu823 ¶[0033]; *see also* Mistry_Presentation, 14-19. Thus, as Figure A shows below, a POSITA would have known the same process steps Hsu823 describes regarding Figure 7B readily integrate into Aoyama's process at FIG. 6I with the

ordinary and expected result: SiGe stressors to boost pFET performance. Hsu823 ¶[0033]; *see also* Section VI.D above.

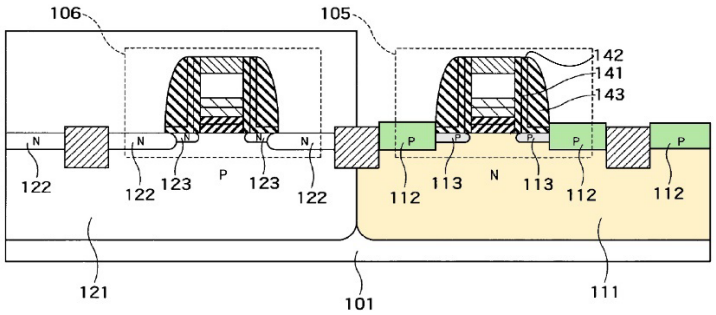


Figure A
(Aoyama's FIG. 6I, modified & annotated)

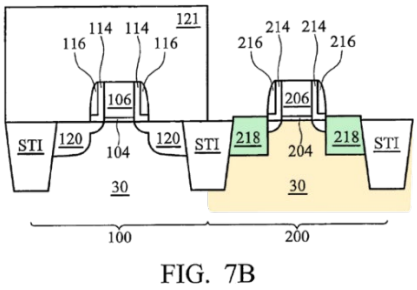


FIG. 7B

Hsu823, FIG. 7B
(annotated)

301. Figure B below illustrates an exemplary modification of Aoyama's semiconductor device that includes SiGe stressors like the ones Hsu823 discloses. Hsu823 ¶[0033], FIG. 7B; Aoyama, FIG. 5; Hsu660, 6:27-31, FIGS. 3-10 (illustrating a similar implementation of SiGe stressors in an RMG device); Mistry2007, Fig. 6 (same).

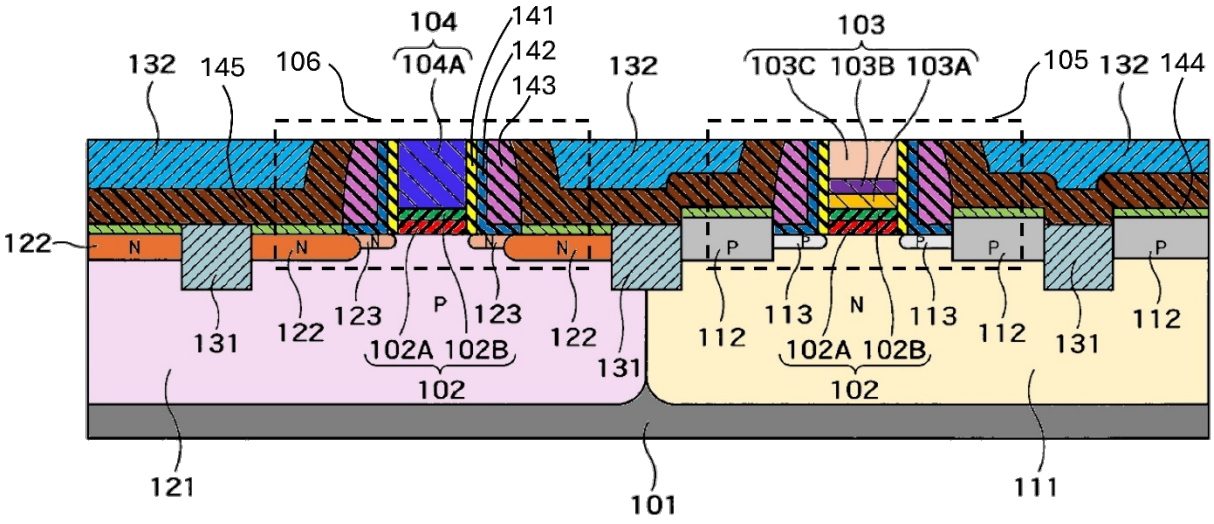


Figure B (Aoyama's FIG. 5, modified and annotated)

2. Independent Claim 1

a. [1Pre]-[1A], [1C]-[1J], and [1L]-[1M]

302. Feature [1Pre] recites "[a] semiconductor device." Aoyama discloses this feature for the same reasons I provide for feature [19Pre], which also recites "[a] semiconductor device." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19Pre] applies to feature [1Pre].

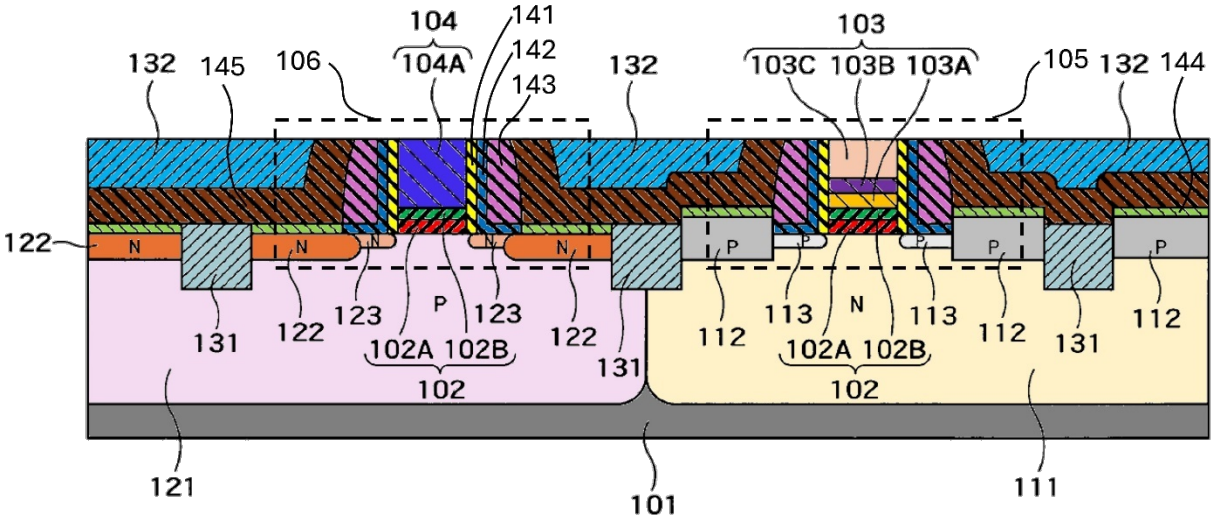


Figure B (Aoyama's FIG. 5, modified and annotated)

303. Feature [1A] recites "a first MIS transistor." Aoyama discloses this feature for the same reasons I provide for feature [19A], which also recites "a first MIS transistor." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19A] applies to feature [1A].

304. Feature [1C] recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." Aoyama

discloses this feature for the same reasons I provide for feature [19C], which also recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19C] applies to feature [1C].

305. Feature [1D] recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Aoyama discloses this feature for the same reasons I provide for feature [19D], which also recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19D] applies to feature [1D].

306. Feature [1E] recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19E], which also recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19E] applies to feature [1E].

307. Feature [1F] recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Aoyama discloses this feature for the same reasons I provide for feature [19F], which also recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19F] applies to feature [1F].

308. Feature [1G] recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon." Aoyama discloses this feature for the same reasons I provide for feature [19G], which also recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19G] applies to feature [1G].

309. Feature [1H] recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Aoyama discloses this feature for the same reasons I provide for feature [19H], which also recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19H] applies to feature [1H].

310. Feature [1I] recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19I], which also recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19I] applies to feature [1I].

311. Feature [1J] recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Aoyama

discloses this feature for the same reasons I provide for feature [19J], which also recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19J] applies to feature [1J].

312. Feature [1L] recites "the first and second metal films are made of different metal materials." Aoyama discloses this feature for the same reasons I provide for feature [19K], which also recites "the first and second metal films are made of different metal materials." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19K] applies to feature [1L].

313. Feature [1M] recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Aoyama discloses this feature for the same reasons I provide for feature [19L], which also recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Combining Hsu823 with Aoyama does not materially affect how my analysis for feature [19L] applies to feature [1M].

b. [1B]: "a second MIS transistor"

314. The Aoyama-Hsu823 combination includes "a second MIS transistor."

315. Aoyama's FIG. 5 device includes a "PMOSFET region 105," which "is a region where the PMOSFET is to be formed." Aoyama ¶[0106]; *see also* Aoyama, FIGS. 5, 6D. For the reasons I explain in Section IX.C.1, a POSITA would have found it obvious to modify Aoyama's pFET (i.e., PMOSFET) in region 105 to include SiGe source/drain stressors, as Hsu823 discloses. *See* Hsu823 ¶[0033], FIG. 7B. Figure B below illustrates such a modification to Aoyama's pFET.

316. Aoyama's pFET, as modified to include SiGe source/drain stressors as in Hsu823, includes features [1G]-[1J] for the reasons I explain regarding [19G], [1H], [19I], and [19J], respectively.

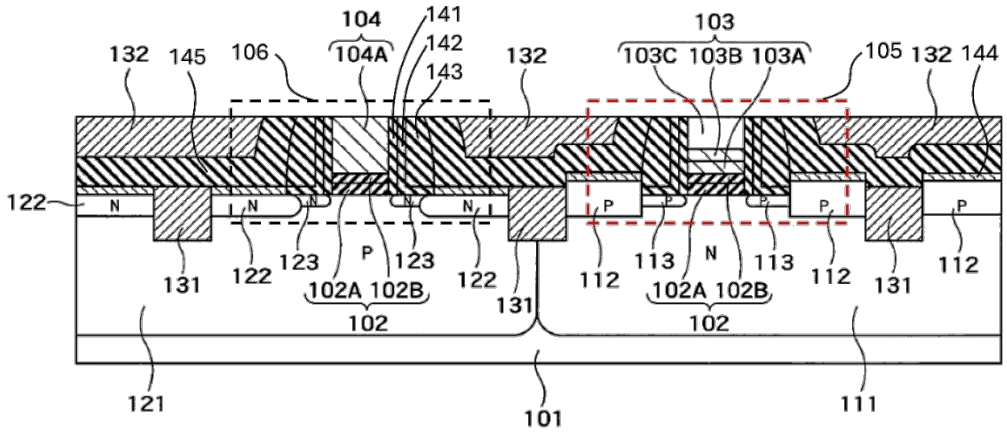


Figure B

c. [1K]: "the second MIS transistor includes . . . source/drain regions formed in the second active region laterally outside the second sidewall spacers"

317. In the Aoyama-Hsu823 combination, "the second MIS transistor includes: . . . source/drain regions formed in the second active region laterally outside the second sidewall spacers."

318. Aoyama's pFET in region 105 includes an n-type well diffusion layer 111, p-type source/drain diffusion layers 112, and p-type extension diffusion layers 113. Aoyama ¶[0099].

319. For the reasons I explain in Section IX.C.1 above, a POSITA would have found it obvious to substitute p-type SiGe stressors for p-type source/drain diffusion layers 112 in Aoyama's pFET. Figure B below provides an exemplary illustration of the resulting combination.

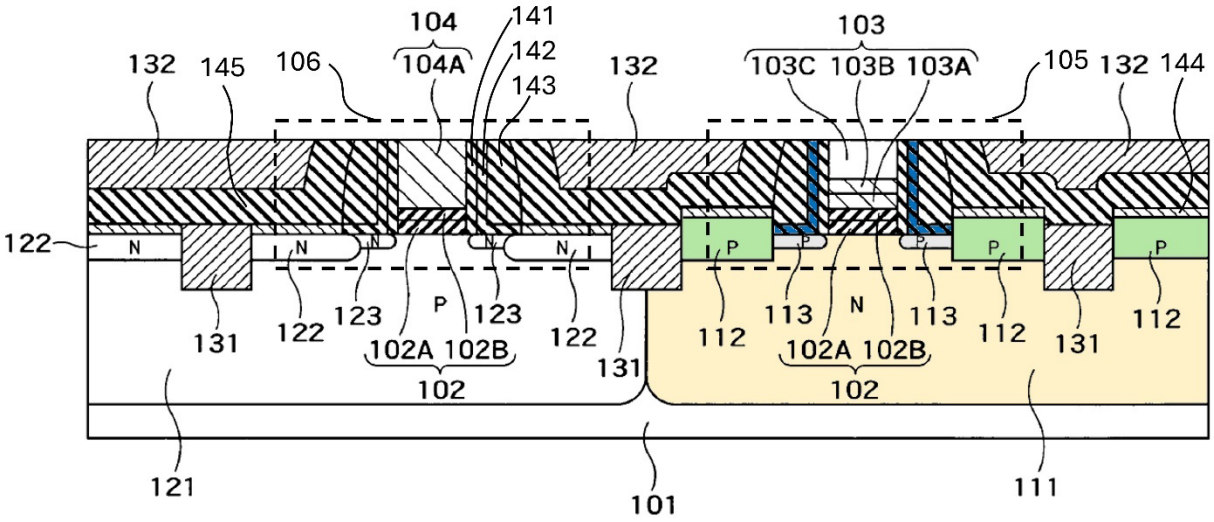


Figure B

320. Hsu823 explains: "Recesses are formed in [the] substrate . . . along the outside edges of the spacers" by etching. Hsu823 ¶[0033]. "SiGe stressors . . . are then formed in the recesses" and "doped [by boron] during the epitaxial growth." Hsu823 ¶[0033]; *see also* Hsu823, FIG. 7B. In this process—which is the same process a POSITA would have applied to Aoyama's pFET (*see* Section IX.C.1

above)—SiGe stressors are formed as source/drain regions in the pFET active region laterally outside the sidewall spacers in pFET region 105.

321. Thus, as Figure B illustrates, the Aoyama-Hsu823 combination includes source/drain regions (SiGe stressors, shown in green above) formed in the active region (pFET active region) laterally outside the claimed "sidewall spacers" (Aoyama's sidewall spacers 142 alone, shown in blue above, or together with Aoyama's offset spacers 141, not colored above).

d. [1N]: "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region"

322. In the Aoyama-Hsu823 combination, "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region."

323. As I explain in Section IX.C.1, a POSITA would have found it obvious to replace Aoyama's ion-implanted pFET source/drain regions 112 with epitaxial SiGe stressors, as Hsu823 teaches. Figure B above shows an example of the resulting Aoyama-Hsu823 combination.

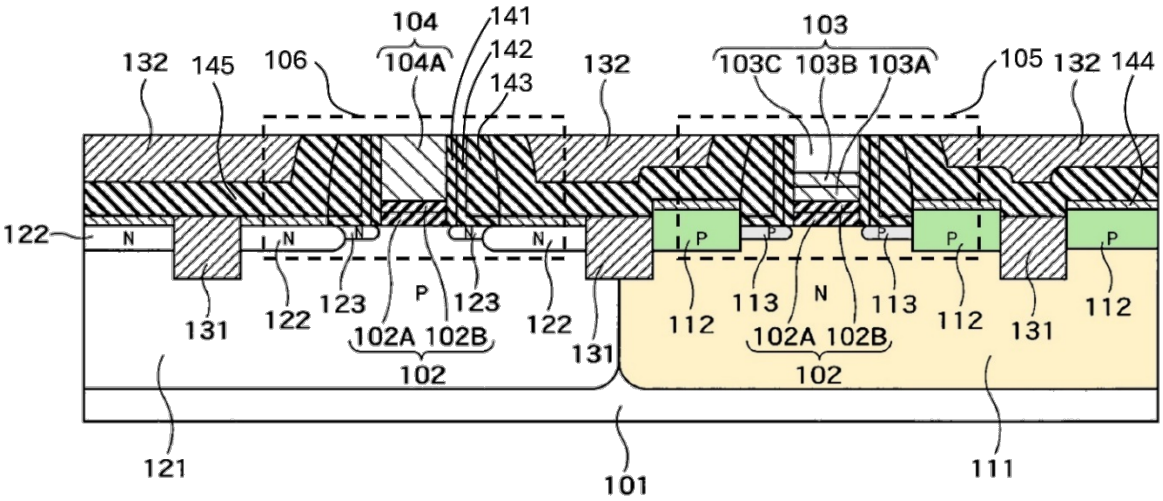


Figure B

324. As Hsu823 explains, a POSITA would have recognized that such SiGe stressors (shown in green above) are "a silicon mixed crystal layer which is formed in trenches provided in" the pFET active region, as claimed, because they comprise silicon and germanium atoms that are "epitaxially grown" (i.e., a mixed crystal of Si and Ge grown) in "[r]ecesses [that] are formed . . . along the outside edges of the spacers" (i.e., in trenches of the pFET region). Hsu823 ¶[0033]; *see also* '686 Patent, 6:60-61 ("The silicon mixed crystal layer is preferably made of a SiGe layer."), 13:33-50 (similar), 19:62-20:20 (similar), claim 10 (similar).

325. As Hsu823 further explains, a POSITA also would have recognized that such SiGe stressors "cause[] . . . stress in a gate length direction of a channel region in the . . . active region" of the pFET because they "introduce[] compressive stress[] in the . . . channel region[] of the resulting PMOS device[]." Hsu823 ¶[0033]. As I explain in Section VI.D, that is the fundamental purpose for which SiGe stressors

were developed and why they were so rapidly adopted in the semiconductor industry.

e. [1O]: "the silicon nitride film has a thickness smaller than that of the first gate electrode"

326. In the Aoyama-Hsu823 combination, it would have been obvious that "the silicon nitride film has a thickness smaller than that of the first gate electrode" for the reasons I provide for claim 22 in Ground 1B (Section IX.A.4). Combining Hsu823 with Aoyama does not materially affect my analysis of Aoyama regarding claim 22 in the context of feature [1O].

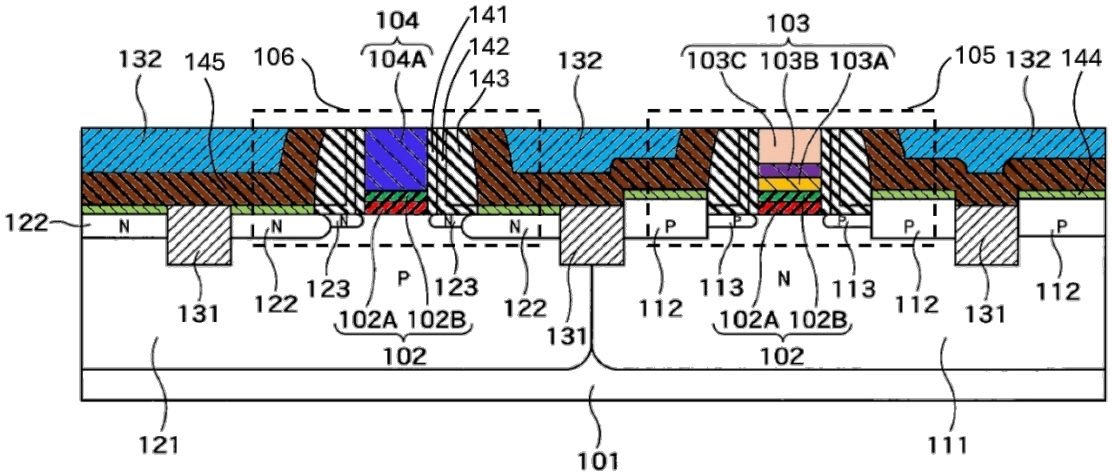


Figure B

3. Independent Claim 25

327. For purposes of claim 25, the Aoyama-Hsu823 combination may optionally include SiGe source/drain stressors, as I describe in Section IX.C.1 above, or it may optionally omit them. Either way, it is my opinion that a POSITA would have found claim 25 obvious in view of the Aoyama-Hsu823 combination.

a. [25Pre]-[25L]

328. Feature [25Pre] recites "[a] semiconductor device." Aoyama discloses this feature for the same reasons I provide for feature [19Pre] (and feature [11Pre]), which also recites "[a] semiconductor device." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1Pre]) above.

329. Feature [25A] recites "a first MIS transistor." Aoyama discloses this feature for the same reasons I provide for feature [19A] (and feature [11A]), which also recites "a first MIS transistor." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1A]) above.

330. Feature [25B] recites "a second MIS transistor." Aoyama discloses this feature for the same reasons I provide for feature [19B] (and feature [11B]), which also recites "a second MIS transistor." If SiGe source/drain stressors are present, the Aoyama-Hsu823 combination also includes this feature for the reasons I provide above for feature [1B], which also recites "a second MIS transistor." *See* Section IX.C.2.b ([1B]) above.

331. Feature [25C] recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate." Aoyama discloses this feature for the same reasons I provide for feature [11C],

which also recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1C]) above.

332. Feature [25D] recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Aoyama discloses this feature for the same reasons I provide for feature [19D] (and feature [11D]), which also recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1D]) above.

333. Feature [25E] recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19E] (and feature [11E]), which also recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1E]) above.

334. Feature [25F] recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Aoyama discloses this feature for the same reasons I provide for feature [19F] (and feature [11F]), which also recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1F]) above.

335. Feature [25G] recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate." Aoyama discloses this feature for the same reasons I provide for feature [11G], which also recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1G]) above.

336. Feature [25H] recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film

and a conductive film formed on the first metal film." Aoyama discloses this feature for the same reasons I provide for feature [1H], which also recites "the second MIS transistor includes . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1H]) above.

337. Feature [25I] recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Aoyama discloses this feature for the same reasons I provide for feature [19I] (and feature [11I]), which also recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1I]) above.

338. Feature [25J] recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Aoyama discloses this feature for the same reasons I provide for feature [19J] (and feature [11J]), which also recites "the second MIS transistor includes: . . . the silicon

nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1J]) above.

339. Feature [25K] recites "the first and second metal films are made of different metal materials." Aoyama discloses this feature for the same reasons I provide for feature [19K] (and feature [11K]), which also recites "the first and second metal films are made of different metal materials." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1L]) above.

340. Feature [25L] recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Aoyama discloses this feature for the same reasons I provide for feature [19L] (and feature [11L]), which also recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." This remains true whether or not SiGe source/drain stressors are present in the Aoyama-Hsu823 combination. *See* Section IX.C.2.a ([1M]) above.

b. [25M]: "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region"

341. In the Aoyama-Hsu823 combination, "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region."

342. As I explain regarding feature [19F], Aoyama's silicon nitride etch stopper film 145 discloses the claimed "silicon nitride film." A POSITA would have found it obvious to implement Aoyama's etch stopper film 145 as a tensile etch stop layer to "cause[] . . . stress in a gate length direction of a channel region in" Aoyama's nFET.

343. Hsu823 discloses a similar CESL 34 made of silicon nitride and formed in a manner that causes tensile stress in a gate length direction of a channel region in the active region of the nFET device. Hsu823 explains why doing so would have been beneficial:

> With circuits becoming smaller and faster, improvement in device driving current is becoming more important, which can be increased by improving carrier mobility. Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design.
>
> Research has revealed that a bi-axial, in-plane tensile stress field can improve NMOS performance, and a compressive stress parallel to the channel length direction can improve PMOS device performance. A commonly

> used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.

Hsu823 ¶¶[0002]-[0003]; *see also* Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.").

344. As one example, a POSITA would have been motivated to implement Aoyama's silicon nitride etch stopper film 145 as a tensile layer covering both pFET and nFET devices, which was well known in the art to improve electron mobility in the nFET channel regions. *See* Section VI.D above. Morin, for instance, explains that "in low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL." Morin, 356; *see also* Murthy151 ¶[0005] ("For n-MOS devices, carrier mobility (i.e. electron mobility) is enhanced by generating a tensile strain in the transistor's channel region."); Hsu823 ¶[0039] (teaching the option of applying a tensile CESL over both pFET and nFET devices because "the performance of PMOS devices can be easily improved . . . , while the performance of NMOS devices is relatively

difficult to improve"); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c).

345. If SiGe source/drain stressors are present, as they optionally are in the asserted combination for claim 25, Bohr683 explains that a net compressive stress still obtains in the pFET channel region when a tensile CESL is formed over both pFET and nFET devices to apply tensile stress to the nFET channel region. Bohr683's FIG. 6 illustrates this below. Bohr683 ¶¶[0038]-[0039], FIG. 6; *see also* Hsu823 ¶[0039] (teaching the option of applying a tensile CESL over both pFET and nFET devices because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 356 ("[I]t is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL."); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current

enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c).

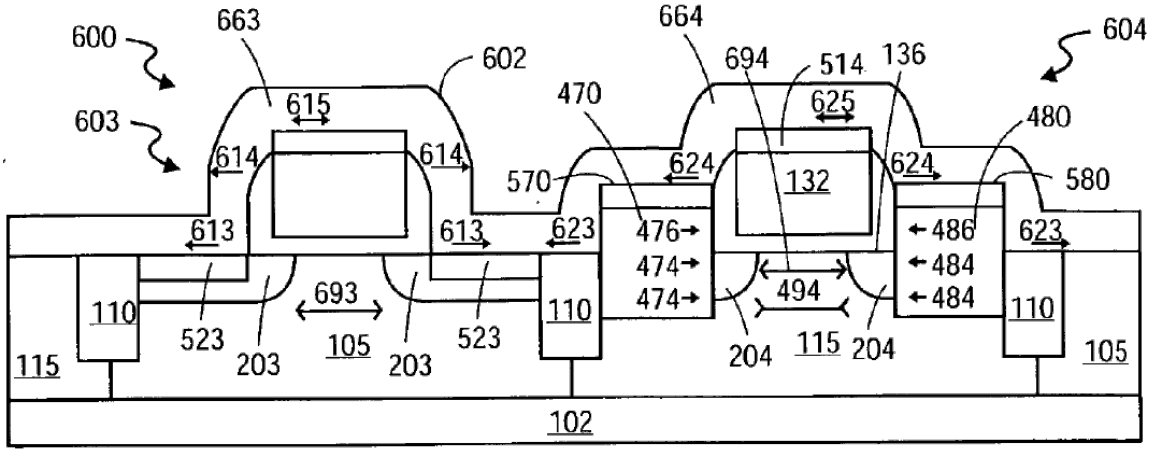


FIG. 6

Bohr683's FIG. 6

346. A POSITA would have reasonably expected to succeed at implementing Aoyama's silicon nitride etch stopper film 145 as a tensile layer because such tensile CESLs were widely used to improve carrier mobility in nFETs. *See* Section VI.D above. Moreover, it would have been well within a POSITA's ability to create a tensile silicon nitride CESL film. For example, Jung explains that "a stress-tuned silicon nitride film can be deposited . . . to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure." Jung ¶[0090]. Jung also describes exemplary recipes for forming a tensile CESL for this purpose. *See* Jung ¶[0099]-[0100] ("Table V shows the deposition conditions for silicon nitride films which were deposited under conditions which

provided tensile stress films."), Tbl. V. Accordingly, a POSITA would have reasonably expected to succeed at implementing Aoyama's silicon nitride etch stopper film 145 as a tensile layer, as such layers were ubiquitous in the industry by the time the application for the '686 Patent was filed. This remains true whether or not SiGe source/drain stressors are present.

4. Claims 2 and 26

347. Claim 2 depends from claim 1. I understand that means claim 2 requires all the same features as claim 1, plus the additional features recited in claim 2. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

348. Claim 26 depends from claim 25. I understand that means claim 26 requires all the same features as claim 25, plus the additional features recited in claim 26. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

349. Aoyama further discloses "wherein the first metal film has a thickness smaller than that of the second metal film" for the same reasons I provide in Section IX.A.2 regarding claim 20. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to claim 20.

5. Claims 3 and 27

350. Claim 3 depends from claim 1. I understand that means claim 3 requires all the same features as claim 1, plus the additional features recited in claim 3. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

351. Claim 27 depends from claim 25. I understand that means claim 27 requires all the same features as claim 25, plus the additional features recited in claim 27. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

352. Aoyama further discloses "wherein the first and second metal films have different work functions" for the same reasons I provide in Section IX.A.3 regarding claim 21. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to claim 21.

6. Claims 5 and 30

353. Claim 5 depends from claim 1. I understand that means claim 5 requires all the same features as claim 1, plus the additional features recited in claim 5. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

354. Claim 30 depends from claim 25. I understand that means claim 30 requires all the same features as claim 25, plus the additional features recited in claim

30. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

355. Aoyama further discloses "the conductive film is made of a silicon film," and "the semiconductor device further comprises a metal silicide film formed on the silicon film" for the same reasons I provide in Sections IX.B.1.c-d for features [11M] and [11N]. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to feature [11M] or [11N].

7. Claims 6 and 31

356. Claim 6 depends from claim 1. I understand that means claim 6 requires all the same features as claim 1, plus the additional features recited in claim 6. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

357. Claim 31 depends from claim 25. I understand that means claim 31 requires all the same features as claim 25, plus the additional features recited in claim 31. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

358. Aoyama further discloses "wherein the first and second gate insulating films are made of the same insulating material" for the same reasons I provide in Section IX.B.4 regarding claim 14. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to claim 14.

8. Claims 7, 16, 23, and 33

359. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2.

360. Claim 16 depends from claim 11. I understand that means claim 16 requires all the same features as claim 11, plus the additional features recited in claim 16. Aoyama discloses and/or renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

361. Claim 23 depends from claim 19. I understand that means claim 23 requires all the same features as claim 19, plus the additional features recited in claim 19. Aoyama discloses all the features recited in claim 19 for the reasons I provide in Section IX.A.1 above.

362. Claim 33 depends from claim 25. I understand that means claim 33 requires all the same features as claim 25, plus the additional features recited in claim 33. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

363. Further, as I explain below, the Aoyama-Hsu823 combination includes the following features: "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers

is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape."

a. A POSITA would have found it obvious to remove Aoyama's second sidewall spacers

364. The Aoyama-Hsu823 combination includes Aoyama's sidewall spacers 142 (blue) and 143 (purple), as Figure B shows below (showing Aoyama's pFET source/drain regions as epitaxial SiGe layers). Aoyama ¶[0111], FIG. 5.

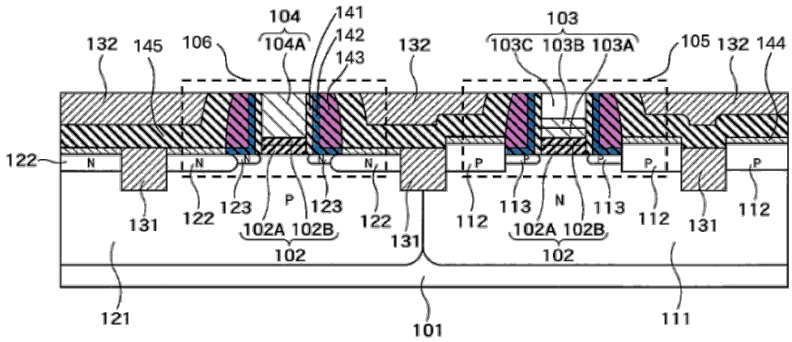


Figure B

365. Hsu823 similarly discloses forming silicon nitride sidewall spacers 116 and 216, as Hsu823's FIG. 7B shows below. Hsu823 ¶[0031], ¶[0035].

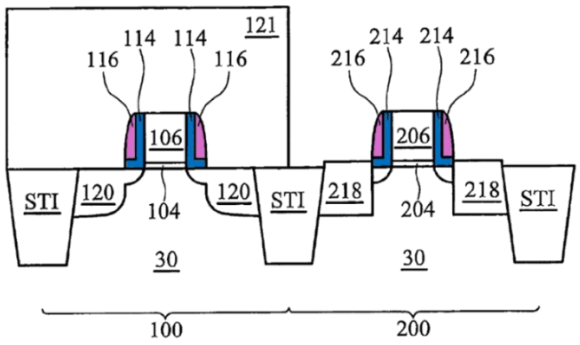


FIG. 7B

Hsu823's FIG. 7B (annotated)

151

366. Hsu823 also discloses L-shaped spacer liners 114 and 214, which are formed before spacers 116 and 216 (*see* Hsu823's FIG. 7B above). Hsu823's spacers and spacer liners, like Aoyama's sidewall spacers 142 and 143, define the location of the deep source/drain regions (whether ion-implanted or grown as epitaxial SiGe). Hsu823 ¶¶[0032]-[0033], FIGS. 6, 7A-7B; Aoyama ¶[0111], FIGS. 6H-6I.

367. As Hsu823's FIGS. 9 and 10 illustrate below, Hsu823 teaches to remove spacers 116 and 216—but not L-shaped spacer liners 114 and 214—before forming CESL 34. Hsu823 ¶¶[0035]-[0036]. Although Hsu823's FIG. 10 illustrates a "dielectric layer 32" formed prior to the contact etch stop layer 34, dielectric layer 32 is "optionally formed" and may be omitted. Hsu823 ¶[0036]. For purposes of this declaration, optional dielectric layer 32 is not present—an option a POSITA would have exercised so that CESL 34 is closer to the nFET channel region to improve stress transfer from the CESL to the channel regions. *See* Hsu823 ¶[0015]; Liu, 1-2, Tbls. I-II, Figs. 1-7.

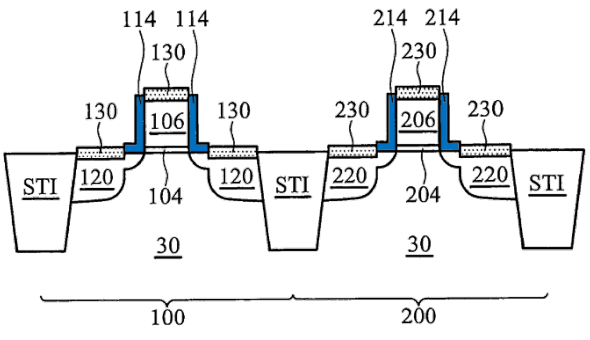


FIG. 9

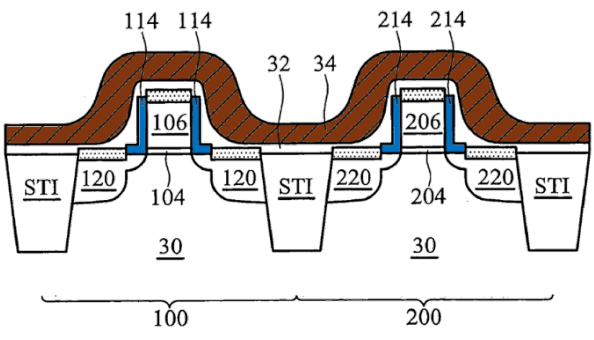


FIG. 10

Hsu823's FIGS. 9 and 10 (annotated)

368. More specifically, Hsu823 teaches to remove spacers 116 and 216 just before forming CESL 34 by applying a selective etchant, such as phosphoric acid (H_3PO_4) (a common etchant used to preferentially remove silicon nitride over silicon oxide):

> Referring to FIG. 9, spacers 116 and 216 are removed. Both wet and dry etchings can be used. The removal is preferably performed using an etchant that attacks the spacers 116 and 216, but not the spacer liners 114 and 214 and silicides 130 and 230. In the preferred embodiment wherein the spacers 116 and 216 are formed of silicon nitride and spacer liners 114 and 214 are formed of silicon oxide, . . . H_3PO_4 can be used to remove spacers 116 and 216. Referring to FIG. 10, a dielectric layer 32 is optionally formed. A contact etch stop layer (CESL) 34 is then formed.

Hsu823 ¶¶[0035]-[0036].

369. Hsu823 recommends using L-shaped spacer liners 114 and 214 and removing spacers 116 and 216 because it reduces the aspect ratio of the gap between neighboring FETs. Hsu823 explains: "With the scaling of integrated circuits, . . . the distance between devices decreases" and "subsequently performed gap-filling and contact etch processes suffer problems accordingly." Hsu823 ¶[0004] (referring to FIG. 1 and discussing "difficulty in subsequent processes," and "problems, such as short circuits," that occur due to voiding). By removing the spacers 116 and 216, Hsu823 teaches that the aspect ratio of the space between FETs becomes smaller, as FIGS. 15A and 15B show below.

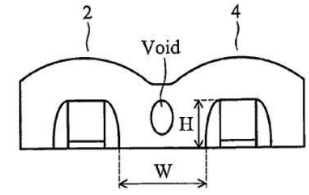


FIG. 1 (PRIOR ART)

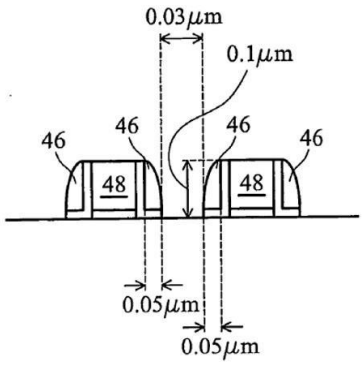


FIG. 15A

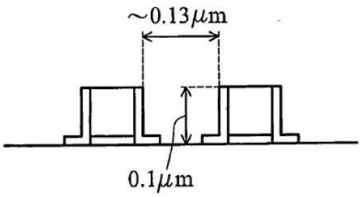


FIG. 15B

Hsu823's FIGS. 1, 15A, 15B

370. More specifically, Hsu823 explains:

> An example is shown in FIGS. 15A and 15B to explain the improvement of the aspect ratio. Referring to FIG. 15A, assuming the spacers have a thickness of 0.05 μm, and the spacing between spacers is 0.03 μm, and further assuming the height of the gates is 0.1 μm, the aspect ratio is 0.1/0.03, which is about 3.3. By removing spacers (refer to FIG. 15B), the spacing is increased to close to 0.13 μm, and the aspect ratio is reduced to 0.8. . . . By reducing the aspect ratio, gap-filling is improved and the contact etching process can be better controlled. Additionally, thicker CESLs can be applied without causing difficulty in subsequent processes, so that the performance of devices is improved.

Hsu823 ¶¶[0042]-[0043]. Hsu823 further explains: "With the spacers removed, the aspect ratio of the gap between neighboring MOS devices is reduced. Thus, the stresses applied by the CESL can be better applied to the channel regions of the respective MOS devices." Hsu823 ¶[0015].

371. Turning back to Aoyama's device structure, a POSITA would have found it obvious to remove Aoyama's sidewall spacers 143, leaving in place

L-shaped sidewall spacers 142. Specifically, a POSITA would have found it obvious to remove Aoyama's sidewall spacers 143 just before forming etch stopper film 145, because Hsu823 teaches the same process to form its analogous sidewall structures. That is, Hsu823 teaches to remove spacers 116/216 (analogous to Aoyama's sidewall spacers 143) just before forming contact etch stop layer 34 (analogous to Aoyama's etch stopper film 145). Hsu823 ¶¶[0035]-[0036], FIGS. 8-10.

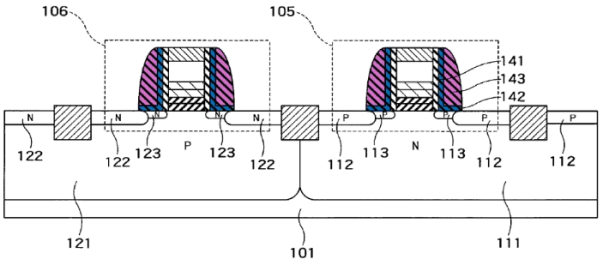


FIG. 6I

Aoyama's FIG. 6I (annotated)

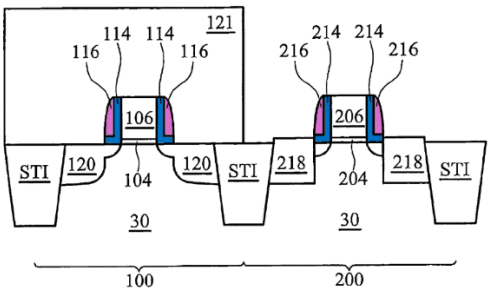


FIG. 7B

Hsu823's FIG. 7B (annotated)

372. Like Hsu823's spacer liners 114/214 and spacers 116/216, Aoyama's sidewall spacers 142 and 143 are, respectively, made of silicon oxide and silicon nitride. *Compare* Aoyama ¶[0111] ("[A] side wall spacer 142 made of a silicon oxide film[is] formed on the lateral surface of each gate electrode . . . . Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE."), FIGS. 6H-6I, *with* Hsu823 ¶[0030] ("[S]ub-layer 110 is a liner oxide layer and sub-layer 112 is a nitride layer."), ¶[0031] ("FIG. 6 illustrates the patterning of sub-layer 110 and sub-layer 112. . . . The remaining portions of the sub-layer 110 and sub-layer 112 form spacer liner 114 and spacer 116 in region 100, and spacer

liner 214 and spacer 216 in region 200, respectively."), FIGS. 5-6. Accordingly, the removal of Aoyama's sidewall spacers 143 would readily fit into the context of Aoyama's FETs. Figure C below illustrates this modification to the Aoyama-Hsu823 combination when SiGe source/drain stressors are present (e.g., for claim 7 and optionally claim 33).

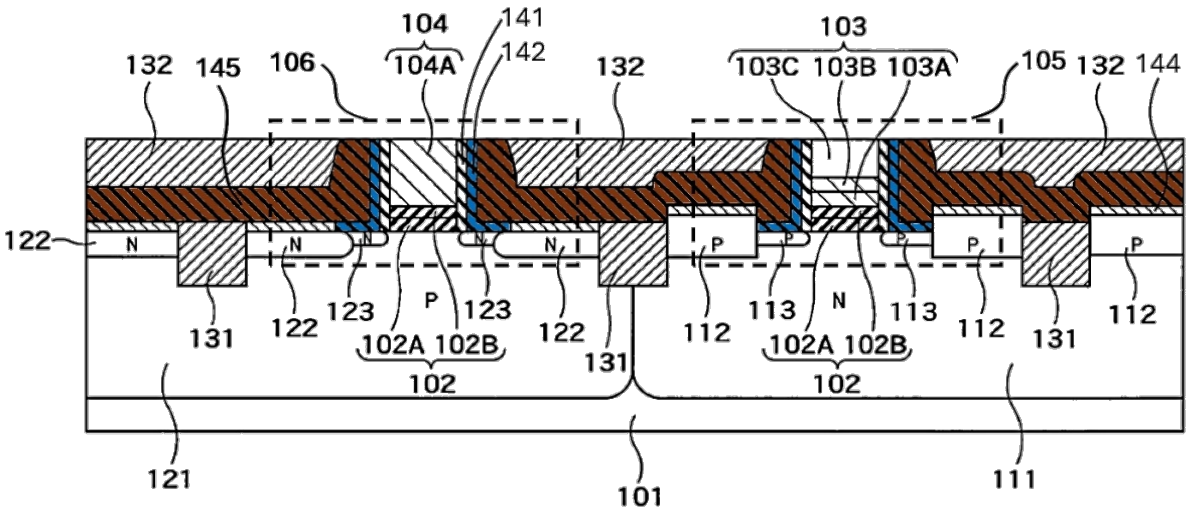


Figure C

373. Before forming Aoyama's etch stopper film 145, a POSITA would have found it obvious to remove Aoyama's sidewall spacers 143 and to leave L-shaped sidewall spacers 142 intact, just as Hsu823 instructs. Hsu823 ¶¶[0035]-[0036], FIGS. 8-10. Hsu823 explains: "The removal is preferably performed using an etchant that attacks the [sidewall spacers 143], but not the [L-shaped sidewall spacers 142]." Hsu823 ¶[0035]. Since Aoyama's sidewall spacers 143 are (like Hsu823's spacers 116 and 216) made of silicon nitride, "H_3PO_4 can be used to remove [sidewall spacers 143]" without removing the L-shaped sidewall spacers 142

underneath, which are made of silicon oxide. Hsu823 ¶[0035]. Figure D below illustrates this intermediate modification to the Aoyama-Hsu823 combination when SiGe source/drain stressors are present (e.g., for claim 7 and optionally claim 33).

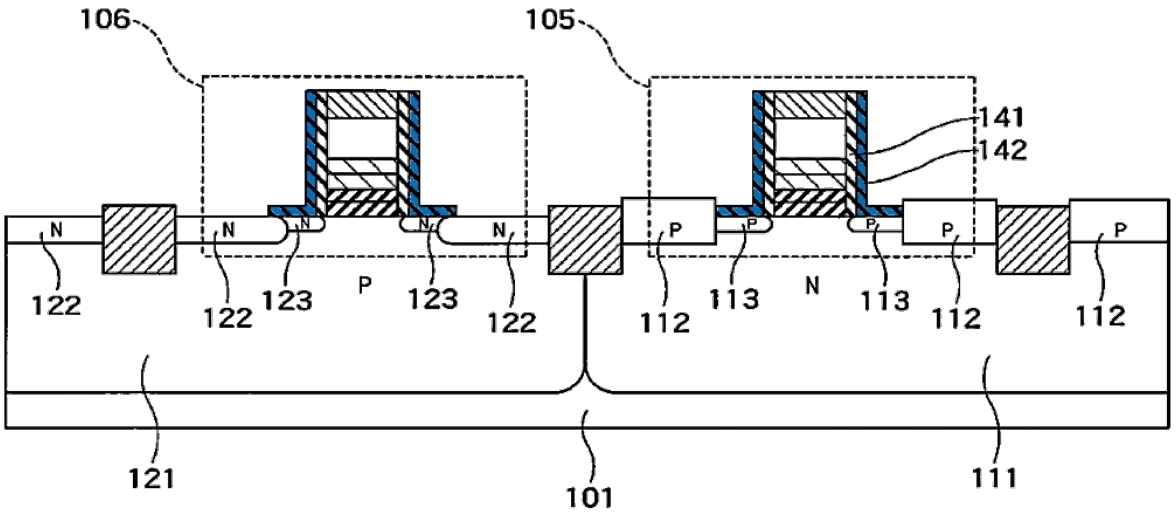


Figure D

374. Finally, a POSITA would have been motivated to continue Aoyama's process by forming etch stopper film 145 over L-shaped sidewall spacers 142, just as Hsu823 teaches to form CESL 34 over L-shaped spacer liners 114 and 214. *Compare* Aoyama ¶[0113] ("[A]n etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD."), *with* Hsu823 ¶[0036] ("A contact etch stop layer (CESL) 34 is then formed. . . . [T]he materials of CESL 34 include commonly used materials such as nitride . . . ."). Figure C below illustrates this modification to the Aoyama-Hsu823 combination when SiGe source/drain stressors are present.

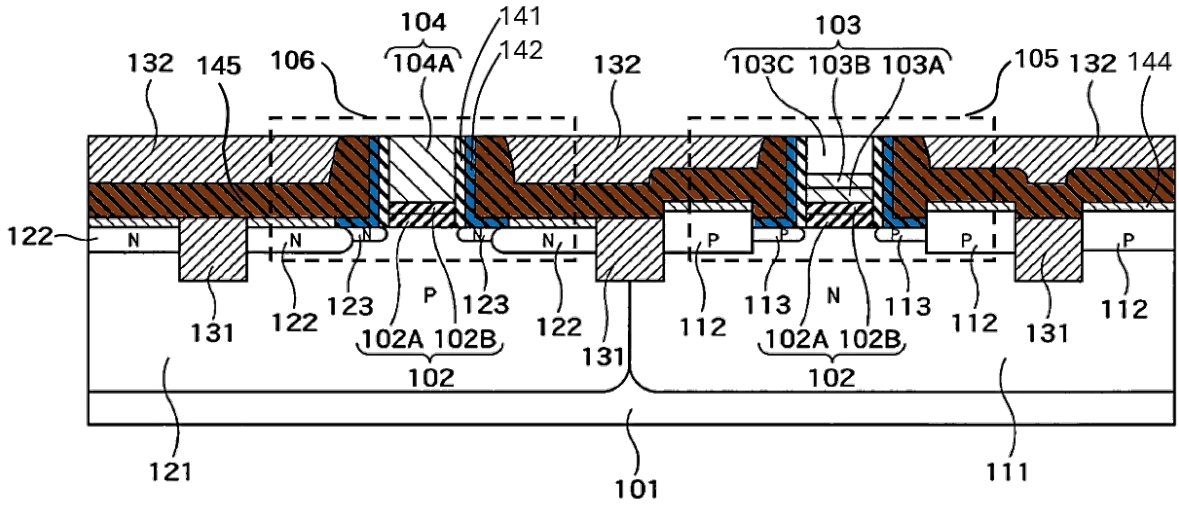


Figure C

375. A POSITA would have been motivated to modify Aoyama in this way to reduce the aspect ratio of the gap between neighboring FETs, thereby minimizing voiding that can cause "difficulty in subsequent processes" and "problems, such as short circuits." Hsu823 ¶[0004]. By the time the application for the '686 Patent was filed, it was well known that removing outer sidewalls but leaving L-shaped sidewalls (as Hsu823 teaches) increases the packing density in an integrated circuit, making it easier to fill gaps and preventing contact-to-gate shorts. Similar to Hsu823, Yeh explains:

> [T]he residual oxide layer 18 is removed by etching. The L-shaped portion of the nitride material layer 14 is not covered and it can be used as a portion of the L-shaped spacer of the gate structure 16. In accordance with the present invention, the design of the L-shaped spacer 14 of the gate structure 16 can benefit from increased packaging density because it causes easier gap filling and prevents contact-to-gate shorts.

Yeh ¶[0018]; *see also* Yeh, Abstract ("The gate structures having L-shaped spacers benefit from increased packaging density in an integrated circuit, and improve gap filling and prevent contact-to-gate shorts."), ¶[0019] ("[T]he L-shaped spacer 14 can benefit from the filling of the interlayer dielectric 20 so as to improve the packaging density of the integrated circuit.").

376. A POSITA also would have been motivated to remove Aoyama's sidewall spacers 143 as described above to improve stress transfer to the channel. For example, Hsu823 explains that, "[w]ith the spacers removed, the aspect ratio of the gap between neighboring MOS devices is reduced. Thus, the stresses applied by the CESL can be better applied to the channel regions of the respective MOS devices." Hsu823 ¶[0015]. Similarly, Liu explains that channel stress may be improved "by narrowing the nitride spacer width" and teaches to fabricate both nFETs and pFETs "without the nitride spacer to achieve the highest channel stress." Liu, 1; *see also* Liu, 2 ("Although the same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es], the drive current enhancement of USP is still higher by more than 7 %."), Tbls. I-II, Figs. 1-7.

377. A POSITA would have reasonably expected to succeed in removing Aoyama's sidewall spacers 143 as described above. Like Hsu823's spacers 116 and 216, Aoyama's sidewall spacers 143 are made of silicon nitride and can be removed

selectively over L-shaped sidewall spacers 142, which are made of silicon oxide, by using an etchant like H_3PO_4 that attacks silicon nitride preferentially over silicon oxide. *See* Hsu823 ¶¶[0035]-[0036], FIGS. 8-10.

b. Claim 7

378. In this version of the Aoyama-Hsu823 combination (which I describe in Section IX.C.8.a immediately above), "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape."

379. As I explain regarding feature [19F], Aoyama's silicon nitride etch stopper film 145 discloses the claimed "silicon nitride film." *See* Aoyama ¶[0113] ("[A]n etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD.").

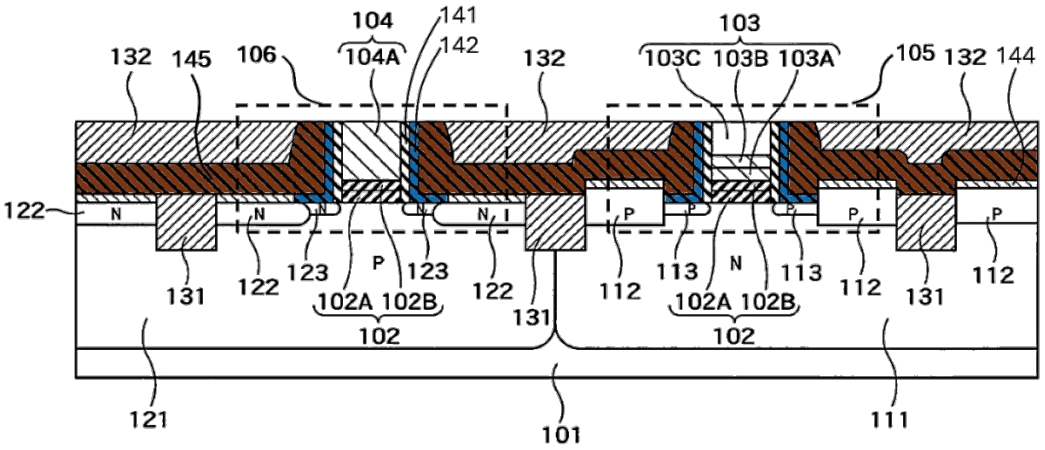


Figure C

160

380. As I explain in Section IX.C.8.a, a POSITA would have found it obvious (as Hsu823 teaches) to remove Aoyama's sidewall spacers 143, thereby increasing packing density, reducing void formation, and preventing contact-to-gate shorts. As Figure C illustrates above, upon doing so, Aoyama's nFET and pFET both include L-shaped sidewall spacers 142 (blue) that—like Hsu823's spacer liners 114 and 214—form an "inner sidewall having an L-shaped cross-section," and Aoyama's silicon nitride etch stopper film 145 would contact surfaces of those sidewall spacers 142 that are bent in an L-shape.

c. Claims 16, 23, and 33

381. The features of claims 16, 23, and 33 would have been obvious based on the Aoyama-Hsu823 combination for the same reasons I explain above regarding claim 7.

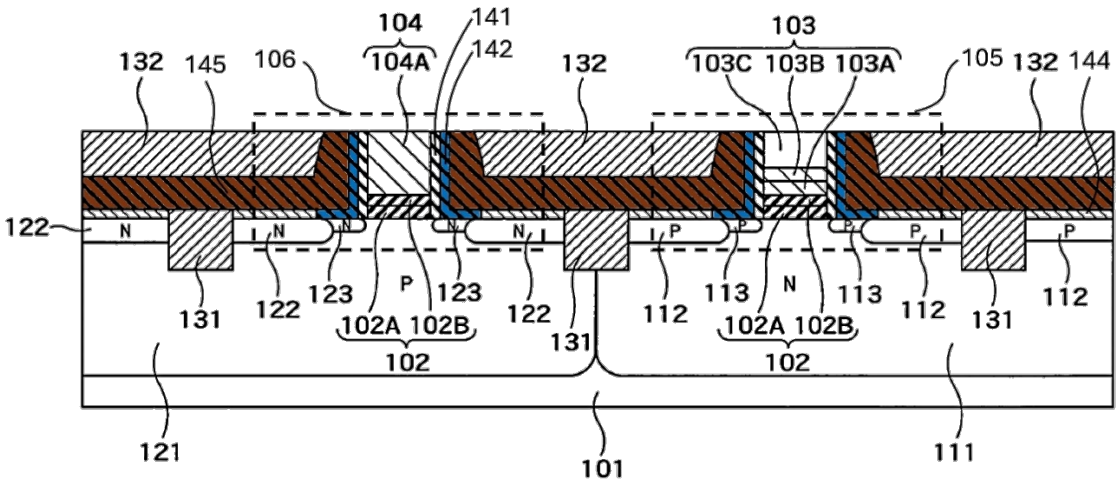


Figure E

382. Although optional in the context of claim 33, Hsu823's SiGe source/drain stressors are not required for claims 16, 23, and 33 as they are for claim 7. Without such SiGe source/drain stressors, the Aoyama-Hsu823 combination for claims 16, 23, and 33 would appear as in Figure E above.

383. As Figure E illustrates above, each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section (Aoyama's gate sidewall spacers 142 in nFET region 106), and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section (Aoyama's gate sidewall spacers 142 in pFET region 105), and the silicon nitride film (Aoyama's silicon nitride etch stopper film 145) is formed in contact with surfaces of the first and second inner sidewalls, which are bent in an L-shape.

9. Claim 8

384. Claim 8 depends from claim 1. I understand that means claim 8 requires all the same features as claim 1, plus the additional features recited in claim 8. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

385. Further, in the Aoyama-Hsu823 combination, "the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region" for the same reasons I provide in Section IX.C.3.b for feature [25M]. That is, a POSITA would have found it obvious to implement Aoyama's etch stopper

film 145 as a tensile etch stop layer to "cause[] . . . stress in a gate length direction of a channel region in" Aoyama's nFET. Because claim 8 depends from claim 1, it requires SiGe stressors, which would have been obvious for the reasons I explain in Section IX.C.1. The explanations I provide regarding feature [25M] also apply in the context of claim 8.

386. Although feature [25M] recites "the silicon nitride film causes ***first*** stress in a gate length direction of a channel region in the first active region," whereas claim 8 recites "the silicon nitride film causes ***second*** stress in a gate length direction of a channel region in the first active region" (emphases added), this difference is linguistic only. Independent claim 1 calls the SiGe stress the "first stress," and dependent claim 8 calls the CESL stress the "second stress." Conversely, feature [25M] calls the CESL stress the "first stress." This is a distinction without a difference.

10. Claim 9

387. Claim 9 depends from claim 8. I understand that means claim 9 requires all the same features as claim 8, plus the additional features recited in claim 9. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 8 for the reasons I provide in Sections IX.C.2 and IX.C.9 above.

388. Further, in the Aoyama-Hsu823 combination, "the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress."

389. As I explain for claim 8 and feature [25M], a POSITA would have found it obvious to implement Aoyama's silicon nitride etch stopper film 145 as a tensile etch stop layer. A POSITA would have recognized that, to improve carrier mobility in Aoyama's nFET (the "first MIS transistor"), the silicon nitride etch stopper film 145 should be implemented with tensile stress. *See* Hsu823 ¶[0003] (explaining "bi-axial, in-plane tensile stress field can improve NMOS performance"), ¶[0037] (explaining "tensile stress is applied to the channel region of the resulting NMOS device, so that the NMOS device is improved"), ¶[0038] (explaining "NMOS device . . . prefers a tensile stress"), ¶[0039] (explaining it is preferable to apply tensile CESL across both nFETs and pFETs because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 356 ("[I]n low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL."); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c).

Accordingly, in the Aoyama-Hsu823 combination, the first MIS transistor (Aoyama's nFET) is n-type, and the second stress (applied by Aoyama's silicon nitride etch stopper film 145) is tensile stress.

11. Claim 10

390. Claim 10 depends from claim 1. I understand that means claim 10 requires all the same features as claim 1, plus the additional features recited in claim 10. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 1 for the reasons I provide in Section IX.C.2 above.

391. Further, in the Aoyama-Hsu823 combination, "the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress."

392. As I explain for feature [1N], a POSITA would have found it obvious to substitute SiGe source/drain stressors (a "silicon mixed crystal layer is made of a SiGe layer") for source/drain diffusion layers 112 in Aoyama's pFET. A POSITA would have understood those SiGe stressors apply compressive stress (the "first stress") to the pFET channel regions. *See* Section IX.C.2.d above. As Hsu823 explains, SiGe stressors "introduce[] compressive stress[] in the respective channel regions of the . . . PMOS device[]," such that the "device drive current[] of the . . . PMOS device[] [is] increased." Hsu823 ¶[0033]; *see also* Hsu823 ¶[0003] (explaining that "a compressive stress parallel to the channel length direction can

improve PMOS device performance"), ¶[0037] (explaining that a "PMOS device . . . prefers a compressive stress").

12. Claims 17, 24, and 34

393. Claim 17 depends from claim 11. I understand that means claim 17 requires all the same features as claim 11, plus the additional features recited in claim 17. Aoyama anticipates and/or renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

394. Claim 24 depends from claim 19. I understand that means claim 24 requires all the same features as claim 19, plus the additional features recited in claim 19. Aoyama anticipates and/or renders obvious all the features recited in claim 19 for the reasons I provide in Section IX.A.1 above.

395. Claim 34 depends from claim 25. I understand that means claim 34 requires all the same features as claim 25, plus the additional features recited in claim 34. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

396. Further, for the same reasons I provide for features [1K] and [1N] and claim 10, a POSITA would have found it obvious for the Aoyama-Hsu823 combination to include "source/drain regions [SiGe stressors] formed in the second active region [pFET active region 105] laterally outside the second sidewall spacers [Aoyama's sidewall spacers 142, alone or together with Aoyama's offset

spacers 141, in pFET region 105], wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region." Figure B below illustrates this combination. *See* Sections IX.C.1, IX.C.2.c-d, and IX.C.11 above.

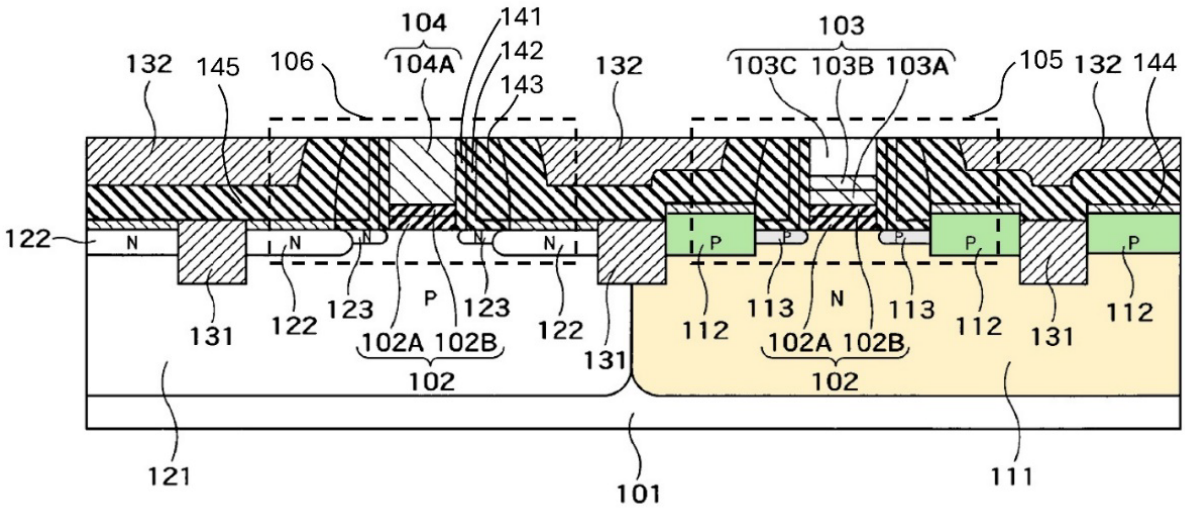


Figure B

13. Claim 28

397. Claim 28 depends from claim 25. I understand that means claim 28 requires all the same features as claim 25, plus the additional features recited in claim 28. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

398. In the Aoyama-Hsu823 combination, "the silicon nitride film has a thickness smaller than that of the first gate electrode" for the reasons I provide for claim 22 in Ground 1B (Section IX.A.4). Combining Hsu823 with Aoyama in claim 25 does not change Aoyama's structure as it relates to claim 22.

14. Claim 32

399. Claim 32 depends from claim 25. I understand that means claim 32 requires all the same features as claim 25, plus the additional features recited in claim 32. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

400. If only part of the gate dielectric film structure may qualify as the claimed "gate insulating film," Aoyama further discloses "wherein the first and second gate insulating films are made of different insulating materials" for the same reasons I provide in Section IX.B.5 regarding claim 15. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to claim 15.

15. Claim 35

401. Claim 35 depends from claim 25. I understand that means claim 35 requires all the same features as claim 25, plus the additional features recited in claim 35. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

402. Aoyama further discloses "wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more" for the same reasons I provide in Section IX.B.6 regarding claim 18. Combining Hsu823 with Aoyama does not change Aoyama's structure as it relates to claim 18.

D. Ground 1D: The Aoyama-Hobbs Combination Renders Obvious Claim 15

403. Claim 15 depends from claim 11. I understand that means claim 15 requires all the same features as claim 11, plus the additional features recited in claim 15. Aoyama discloses and/or renders obvious all the features recited in claim 11 for the reasons I provide in Section IX.B.1 above.

1. A POSITA would have found it obvious to use different gate insulating films for Aoyama's pFETs and nFETs

404. A POSITA would have found it obvious to use different gate dielectric materials for Aoyama's nFETs and pFETs.

405. It is no coincidence that Hobbs was filed in 1999. As I explain in Section VI.B above, the semiconductor industry recognized around 1999 that high-κ gate dielectrics would replace SiO_2-only gate dielectrics. ITRS_FEP, 2. And for reasons I explain in Section VI.C, the industry immediately recognized that metal-based gate electrodes would replace polysilicon-only gate electrodes as part of that transition.[14]

406. Hobbs recognizes this as well. Hobbs notes that "[m]etals are an alternative material currently being investigated to replace polysilicon for use as gate

[14] The reason it took from 1999 to 2007 until commercial devices began implementing high-κ gate dielectrics and metal gates was not because it was unable to do so technologically, but because subsequent advancements prolonged the need to replace SiO_2. *See* ITRS_FEP, 2.

electrodes." Hobbs, 1:50-51. According to Hobbs, because metals cannot be doped, the threshold voltages (VTs) of nFET and pFET devices may differ when using a metal gate. For example, when the same metal serves as the gate electrode for both nFET and pFET devices, the threshold voltages will differ unless the gate metal has a work function that lies close to the middle of the silicon bandgap. Such an approach, however, does not yield very good device performance. Hobbs explains:

> [M]erging metal gate technology into complementary MOS (CMOS) designs introduces new process integration and manufacturing issues. For example, current polysilicon gate CMOS processes can use a combination of doped N^+ and P^+ polysilicon in respective NMOS and PMOS devices to overcome problems associated with adjusting channel threshold voltages (VT). Metals, however, are not readily doped. Therefore, when replacing polysilicon with metal, efforts have focused on selecting those metals having work functions that are close to the mid band-gap of silicon. This allows the VT of the respective n-channel and p-channel devices to be symmetrical. Unfortunately, these mid-gap metal materials can result in transistor VTs that are not optimized for low-voltage, low-power, high-performance devices.

Hobbs, 1:53-67.

407. Aoyama and Hobbs use a better approach: selecting ***different*** gate metals with work functions appropriate to adjust the threshold voltages of nFET and pFET devices, respectively. As Aoyama explains, "since the threshold voltage changes according to the work function of the metal used, an appropriate threshold voltage can be ensured by using a metal with an appropriate work function. . . . A

metal suitable for the metal gate electrode of a PMOSFET is a metal with a work function of 4.8 eV or more, and a metal suitable for the metal gate electrode of an NMOSFET is a metal with a work function of 4.3 eV or less." Aoyama ¶¶[0009]-[0010]; *see also* Hobbs, 8:37-40 ("The work functions of the different materials can be selected such that the threshold voltages can be specifically matched to each of the NMOS and PMOS transistors."). Again, as I explain in Section VI.C above, this approach was not just well known by the time the application for the '686 Patent was filed; it was being used in high-volume commercial devices. *See generally* Mistry2007 (describing Intel's 45nm devices); Mistry_Presentation (same).

408. Both Aoyama and Hobbs implement this solution using what is an RMG process, in which an nFET "dummy" gate electrode is replaced near the end of device fabrication using the desired gate electrode materials. *See* Aoyama ¶[0109], ¶[0117], FIGS. 6H-6Q; Hobbs, FIGS. 4-10.

409. As Hobbs's FIGS. 6 and 7 illustrate below, Hobbs teaches that—in addition to removing and replacing the nFET dummy gate electrode—a dummy nFET gate ***dielectric*** may be removed and replaced as well. Hobbs explains: "[T]he dielectric layer 162 and portions of the liner layer 22 are removed and replaced with a gate dielectric layer 62, as shown in FIG. 7." *See* Hobbs, 4:60-62. "A gate electrode material 64 is then formed within the feature opening 66." Hobbs, 5:12-13.

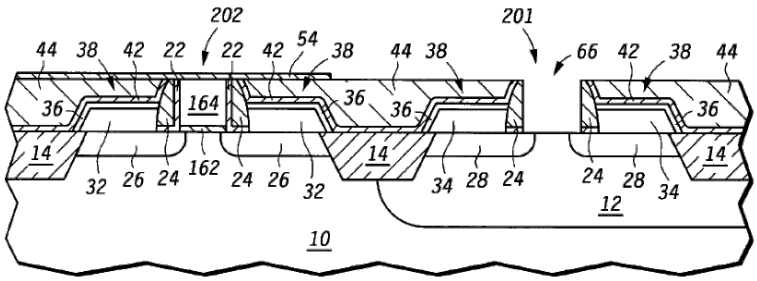


FIG. 6

Hobbs's FIG. 6

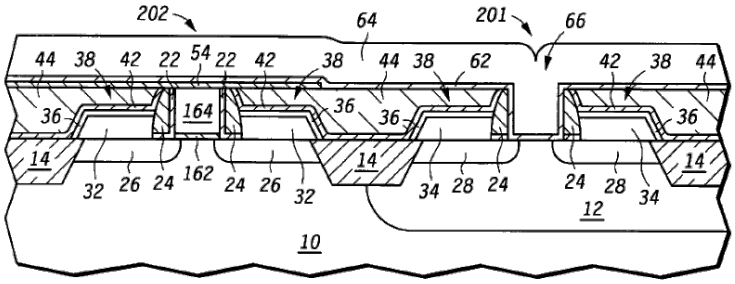


FIG. 7

Hobbs's FIG. 7

410. Hobbs teaches that such a process allows for "different gate dielectric materials and thickness[es] as well as different gate materials [to] be selected to form . . . various transistors with different threshold voltages and operating characteristics." Hobbs, 8:40-45; *see also* Hobbs, 5:66-6:5 ("[T]he combination of materials or thicknesses used to form the gate structure from dielectric layer 82 and gate electrode material 84 is selected such that the VT or some other electrical parameter is different from that of the gate structure formed from the gate dielectric layer 62 and gate electrode material 64."), 7:33-37 ("These processing steps can subsequently be repeated to include different materials and thicknesses of gate dielectrics and gate electrodes in the formation of multiple transistors, thereby

forming a number of transistors having different physical, operational, and performance characteristics."). This serves the same purpose as described in the '686 Patent, thereby confirming that the '686 Patent is employing this same well-known technique. *See* '686 Patent, 27:39-48 ("[T]he third gate insulating film 35a has a thickness optimized for the n-type MIS transistor and is made of an insulating material optimized for the n-type MIS transistor . . . . Also, the second gate insulating film 13b has a thickness optimized for the p-type MIS transistor and is made of an insulating material optimized for the p-type MIS transistor . . . . Therefore, the flexibility of transistor design is increased, whereby a desired transistor characteristic can be achieved.").

411. Consistent with Hobb's teachings (and also like the '686 Patent), Metz demonstrates that a POSITA would have understood "a single gate dielectric material may not provide the highest performance for both NMOS and PMOS structures" because of "poor band offset with conduction or valence bonds, incompatibility to the gate electrode material, incompatibility with gate electrode processing or thickness requirements." Metz ¶[0026]. "By selecting the better candidate dielectric film for each structure, . . . higher performance complementary metal oxide semiconductor devices may be created . . . ." Metz ¶[0026]. In other words, such devices "may exhibit higher mobility, higher saturation current, or better threshold voltage." Metz ¶[0026].

412. For these reasons—i.e., to achieve better band offset, better compatibility with gate electrode materials, and better compatibility with gate electrode processing and thickness requirements, thereby achieving higher performance CMOS devices with higher mobility, higher saturation current, or better threshold voltage—Hobbs teaches that "the thickness and composition of the second gate dielectric and second gate electrode material can be the same or ***different*** from those of the first gate dielectric and first gate electrode material." Hobbs, 7:65-8:2 (emphasis added); *see also* Hobbs, 8:40-45 ("[D]ifferent gate dielectric materials and thickness[es] as well as different gate materials can be selected to form . . . various transistors with different threshold voltages and operating characteristics.").

413. A POSITA would have understood that Hobbs's teachings in that regard apply equally to RMG devices using high-κ gate insulating films. In fact, Hobbs itself expressly discloses using high-k gate dielectric materials. Hobbs, 7:43-47 ("The first gate dielectric layer can include high-k gate dielectric materials . . . ."). Other references confirm this as well. Metz, for instance, explains: "One gate dielectric may be a high-k material (having a dielectric constant greater than 10) and the other may be a low-k material (having a dielectric constant less than 10). Alternatively, both dielectrics may be high-k or both may be low-k dielectrics." Metz ¶[0019]; *see also* Metz ¶¶[0016]-[0017], ¶[0023], FIGS. 1-7. Okazaki similarly explains that suitable "high relative dielectric constant material[s]" in its RMG

process "include zirconium oxide (ZrO_2), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), yttrium oxide (Y_2O_3), and lanthanum oxide (La_2O)," as well as "metal silicates such as HfSiO, ZrSiO, AlSiO, and LaSiO." Okazaki, 6:21-34; *see also* Okazaki, FIGS. 2B-2F. And Hsu660 explains that suitable gate dielectric films for its RMG process "include a metal oxide [or] a silicate of Hf, Al, Zr, combinations thereof, and multi-layers thereof." Hsu660, 5:16-30; *see also* Hsu660, FIG. 10.

414. A POSITA also would have understood that the procedure Hobbs teaches is entirely compatible with Aoyama's RMG process. In fact, Aoyama recommends selecting gate dielectric films to optimize device performance. Aoyama explains: "[G]ate dielectric films with preferable characteristics such as a preferable film quality, and gate electrodes with preferable characteristics such as a preferable work function, can be used as gate dielectric films and gate electrodes constituting a PMOSFET and an NMOSFET." Aoyama ¶[0066].

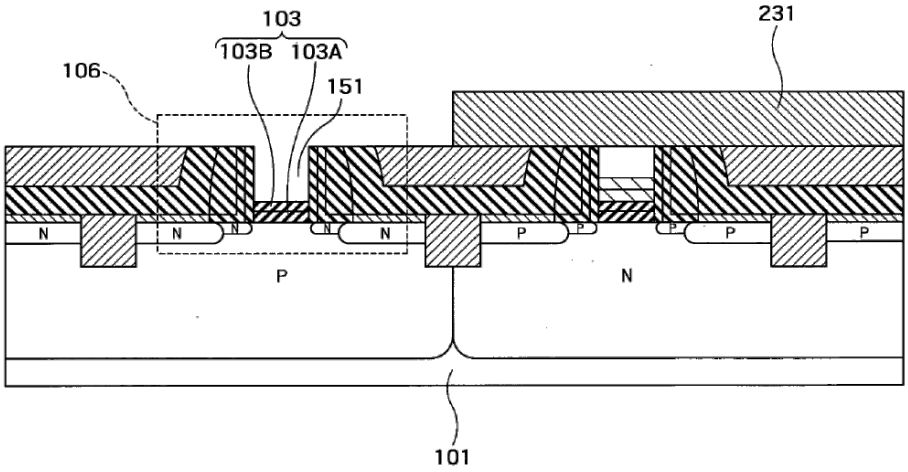


FIG. 6O

Aoyama's FIG. 6O

415. A POSITA would have reasonably expected to succeed when forming different gate dielectric films in Aoyama's nFET and pFET devices according to Hobbs's teachings. For example, at the step of Aoyama's process FIG. 6O shows above, a POSITA would have found it obvious to remove Aoyama's dielectric film 102[15]—from the nFET gate region after removing dummy nFET gate electrode 103, and then to form a different gate dielectric film in the nFET gate structure so that the nFET and pFET gate dielectrics are uniquely tailored to each device.

416. A POSITA would have reasonably expected to succeed in doing so based on the success others previously had in doing the same. *See* Hobbs, FIGS. 4-10; Metz, FIGS. 1-7; Okazaki, FIGS. 2B-2F; Hsu660, FIGS. 10-11. Moreover, a POSITA would have understood this would provide the known and predictable result that Hobbs teaches: forming pFET and nFET gate dielectric films with properties uniquely tailored to each. *See, e.g.*, Hobbs, 5:66-6:5 ("[T]he combination of materials or thicknesses used to form the [nFET] gate structure from dielectric layer 82 and gate electrode material 84 is selected such that the VT or some other electrical parameter is different from that of the [pFET] gate structure formed from the gate dielectric layer 62 and gate electrode material 64."), 8:40-45 ("[D]ifferent gate dielectric materials and thickness[es] as well as different gate materials can be

[15] Mislabeled as 103 in Aoyama's FIG. 6O.

selected to form . . . various transistors with different threshold voltages and operating characteristics.").

2. Claim 15

417. In the Aoyama-Hobbs combination, "the first and second gate insulating films are made of different insulating materials."

418. As I explain immediately above in Section IX.D.1, as an alternative to using the same dielectric film 102 in both Aoyama's nFET and pFET devices, a POSITA would have found it obvious to use different gate dielectric films for Aoyama's nFET and pFET devices to improve device performance. *See* Hobbs, 7:43-47, 7:65-8:2; Metz ¶[0019], ¶[0026]; Okazaki, 6:21-34. In such an embodiment, Aoyama's first and second gate insulating films (i.e., gate dielectric film 102 formed in nFET region 106 and pFET region 105, respectively) would be made of different insulating materials as claimed.

E. Ground 1E: The Aoyama-Hsu823-Hobbs Combination Renders Obvious Claim 32

419. Claim 32 depends from claim 25. I understand that means claim 32 requires all the same features as claim 25, plus the additional features recited in claim 32. The Aoyama-Hsu823 combination renders obvious all the features recited in claim 25 for the reasons I provide in Section IX.C.3 above.

420. Further, in the Aoyama-Hsu823-Hobbs combination, "the first and second gate insulating films are made of different insulating materials" for the same

reasons I provide in Sections IX.D.1-2 regarding claim 15. Combining with Hsu823 with Aoyama and Hobbs does not change the Aoyama-Hobbs structure as it relates to claim 15.

F. Grounds 2A and 2B: Akasaka Anticipates or at Least Renders Obvious Claims 19-22

1. Independent Claim 19

a. [19Pre]: "A semiconductor device"

421. Akasaka discloses "[a] semiconductor device."

422. Akasaka explains: "The present invention relates to a method for manufacturing a semiconductor device, particularly an FET (Field Effect Transistor) of the MIS (Metal Insulator Semiconductor) type . . . ." Akasaka ¶[0003]. Akasaka's FIG. 26 and corresponding descriptions describe a "semiconductor device" that includes a "p-type MISFET . . . formed in . . . area 301A" and an "n-type MISFET . . . formed in . . . area 301B." Akasaka ¶[0073]; *see also* Akasaka ¶[0072] ("FIGS. 15 to 26 are sectional views showing . . . a semiconductor device . . . ."), FIG. 26.

423. For the same reasons I explain above, a POSITA also would have found "[a] semiconductor device" obvious in view of Akasaka.

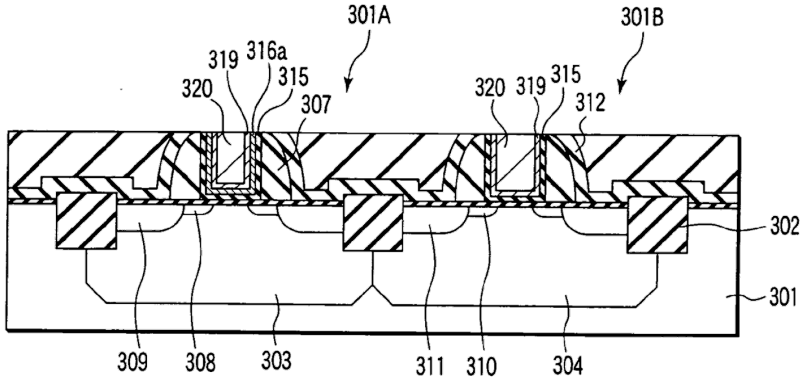


FIG. 26

Akasaka's FIG. 26

b. [19A]: "a first MIS transistor"

424. Akasaka discloses "a first MIS transistor."

425. As FIG. 26 shows below, Akasaka's semiconductor device includes an "n-type MISFET . . . formed in . . . area 301B." Akasaka ¶[0073]; *see also* Akasaka ¶[0072].

426. For the same reasons I explain above, a POSITA also would have found "a first MIS transistor" obvious in view of Akasaka.

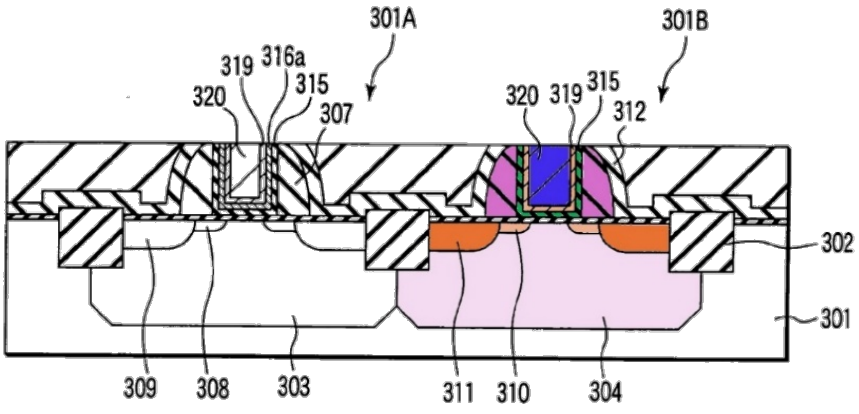


FIG. 26

Akasaka's FIG. 26 (annotated)

c. [19B]: "a second MIS transistor"

427. Akasaka discloses "a second MIS transistor."

428. As FIG. 26 shows below, Akasaka's semiconductor device includes a "p-type MISFET . . . formed in . . . area 301A." Akasaka ¶[0073]; *see also* Akasaka ¶[0072].

429. For the same reasons I explain above, a POSITA also would have found "a second MIS transistor" obvious in view of Akasaka.

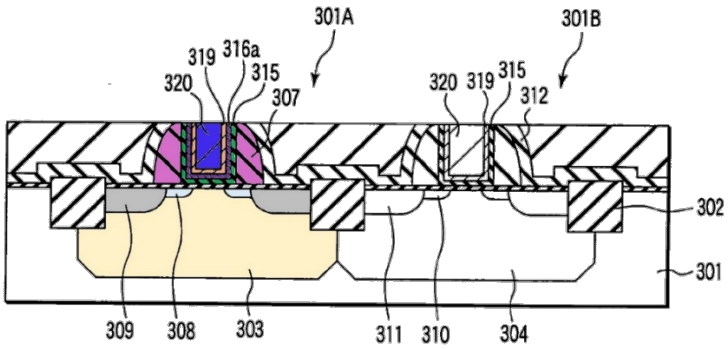


FIG. 26

Akasaka's FIG. 26 (annotated)

d. [19C]: "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon"

430. Akasaka discloses "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon."

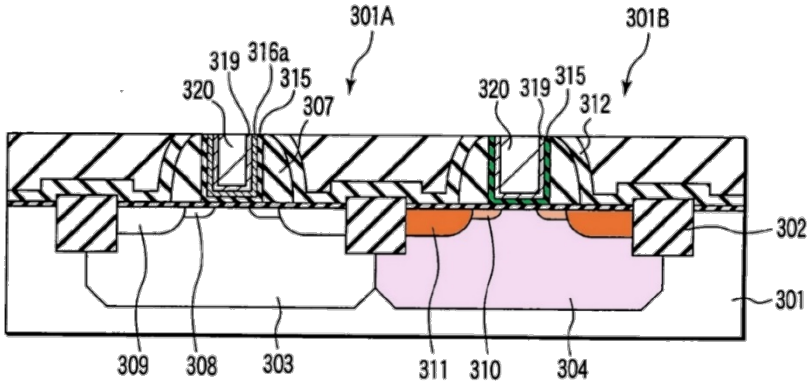


FIG. 26

Akasaka's FIG. 26 (annotated)

431. In the semiconductor device Akasaka's FIG. 26 shows, the nFET in area 301B includes a "gate dielectric (insulating) film 315." Akasaka ¶[0075]. Gate dielectric film 315 is formed of $HfSi_xO_y$, which is an "oxide containing hafnium and silicon." Akasaka ¶[0075]. A POSITA would have recognized that Akasaka's $HfSi_xO_y$ gate dielectric film is "a high-k film." *See* Akasaka939 ¶[0004] (listing "hafnium (Hf)-containing material such as . . . $HfSiO_x$" as a "high-k material [with] dielectricity of more than ten (10)"). In fact, hafnium silicon oxide ($HfSi_xO_y$) is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicate (HfSiO) . . . ." '686 Patent, 29:16-24.

432. Akasaka's "gate dielectric film 315" is "depos[it]ed all over the substrate[301]," including area 301B, "for forming . . . an n-type MISFET," as FIG. 26 shows. Akasaka ¶¶[0072]-[0073], ¶[0075]. From this, a POSITA would

have recognized that "gate dielectric film 315" is formed on a first active region in semiconductor substrate 301, e.g., nFET area 301B.

433. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon," in view of Akasaka.

e. [19D]: "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film"

434. Akasaka discloses "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film."

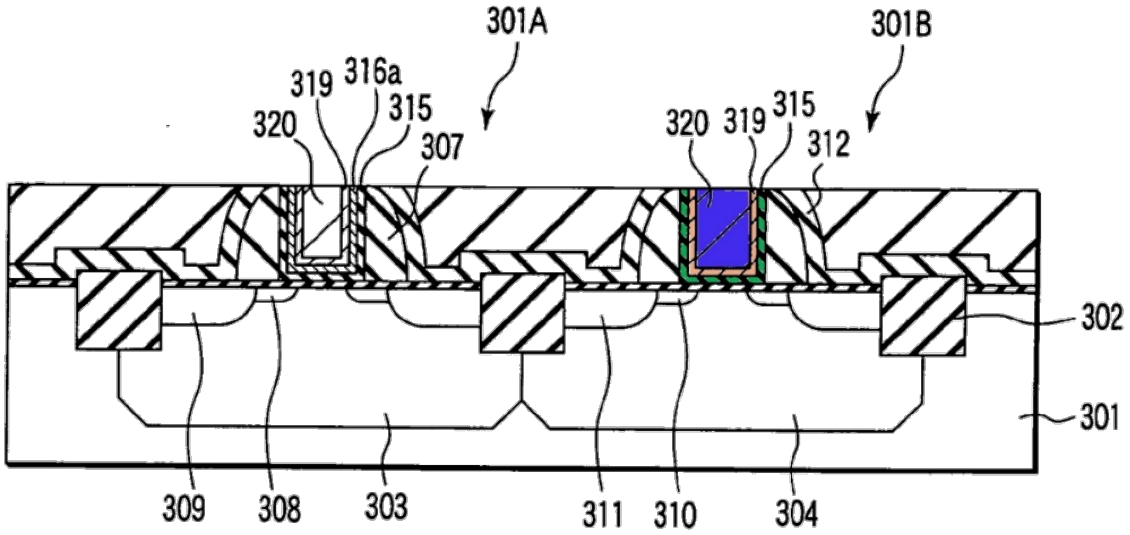


FIG. 26

Akasaka's FIG. 26 (annotated)

435. In the semiconductor device Akasaka's FIG. 26 shows, the nFET in area 301B has a gate electrode that includes conductive film 319 and conductive film 320. Akasaka ¶¶[0084]-[0086]. Either or both conductive films 319/320 disclose the claimed "second metal film."

436. Conductive film 319 may be "a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon," and conductive film 320 may be tungsten, which is also a metal. Akasaka ¶¶[0085]-[0086]. In one embodiment, "conductive film 319 and conductive film 320 are made of one integral film." Akasaka ¶[0086].

437. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film" in view of Akasaka.

f. [19E]: "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative"

438. Akasaka discloses "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative."

439. In the semiconductor device Akasaka's FIG. 26 shows, the nFET in area 301B includes "[a] gate sidewall 307 formed of an insulating film, such as a

silicon nitride film." Akasaka ¶[0073]. As shown below, the gate sidewall 307 (pink) is formed on side surfaces of the gate electrode (conductive films 319/320) of the nFET.

440. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative," in view of Akasaka.

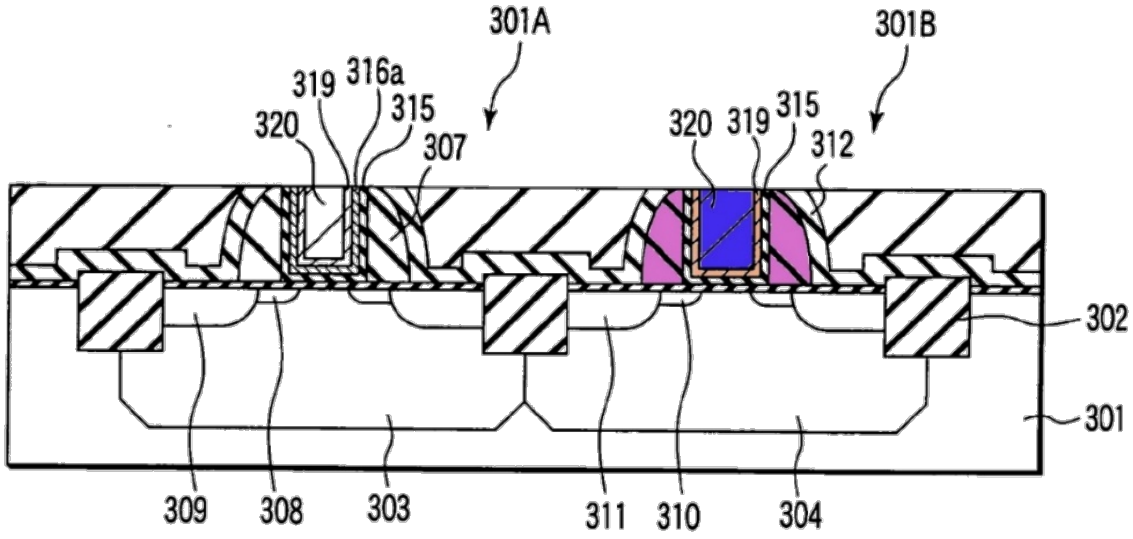


FIG. 26

Akasaka's FIG. 26 (annotated)

g. [19F]: "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers"

441. Akasaka discloses "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers."

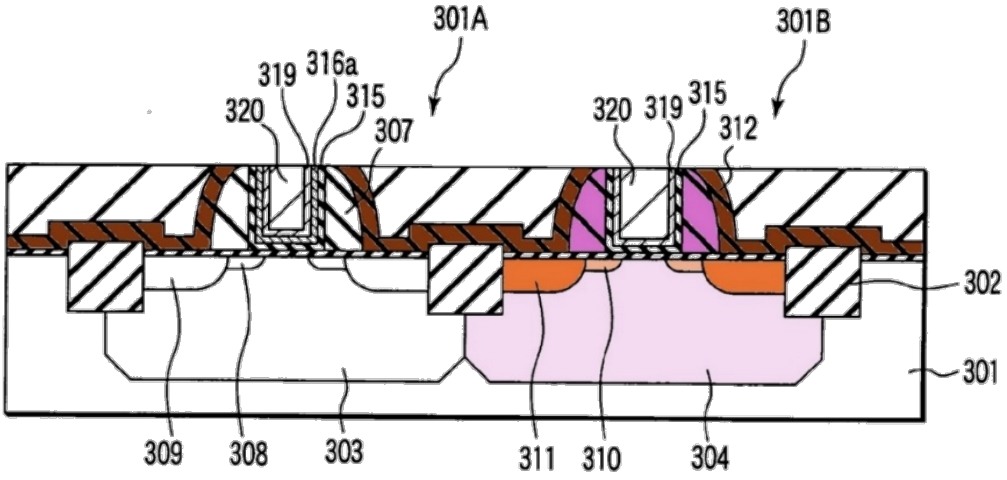


FIG. 26

Akasaka's FIG. 26 (annotated)

442. In the semiconductor device Akasaka's FIG. 26 shows, the nFET in area 301B includes a "silicon nitride film 312 serving as an etching stopper." Akasaka ¶[0073]. This discloses the claimed "silicon nitride film."

443. As shown above, the gate electrode structure and its sidewalls 307 "are covered with a silicon nitride film 312," such that Akasaka's silicon nitride film 312

(brown) extends over the side surfaces of the nFET gate electrode (conductive films 319/320) on which gate sidewalls 307 (purple) are formed. *See* Akasaka ¶[0073] (explaining that "gate sidewall[s] 307 are covered with a silicon nitride film 312"), FIG. 16. Then, a chemical-mechanical polishing ("CMP") process is applied to silicon nitride film 312 to remove it from above the upper surfaces of the gate electrode structures. *See* Akasaka ¶[0074], ¶[0087].

444. As shown above, Akasaka's silicon nitride film 312 (brown) extends over upper surfaces of area 301B (the first active region)—e.g., in p-type well region 304 and n-type source/drain layers 311—located laterally outside of gate sidewalls 307 (purple). A POSITA would have understood that gate sidewalls 307 are used to define the location of source/drain layers 311. *See, e.g.*, Hsu823 ¶[0032] ("The respective spacers . . . are used as masks so that the edges of the source/drain regions . . . are substantially aligned with the respective spacers."), FIG. 7A. As a result, the majority of source/drain layers 311 remain laterally outside of Akasaka's gate sidewalls 307.

445. For the same reasons I explain above, a POSITA also would have found it obvious that "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers," in view of Akasaka.

h. [19G]: "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon"

446. Akasaka discloses "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon."

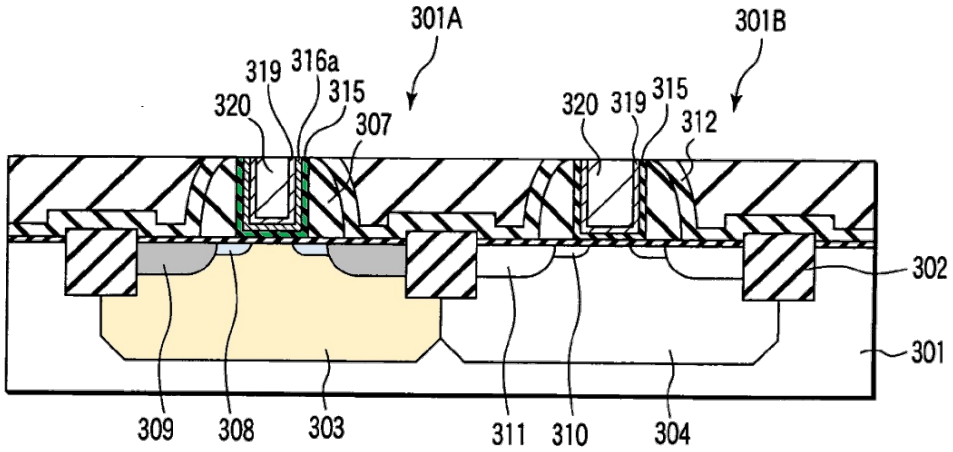


FIG. 26

Akasaka's FIG. 26 (annotated)

447. In the semiconductor device Akasaka's FIG. 26 shows, the pFET in area 301A includes a "gate dielectric (insulating) film 315." Akasaka ¶[0075]. Gate dielectric film 315 is formed of hafnium silicon oxide ($HfSi_xO_y$), which is an "oxide containing hafnium and silicon." Akasaka ¶[0075]. A POSITA would have recognized that Akasaka's $HfSi_xO_y$ gate dielectric (insulating) film 315 is a "high-k film." *See* Akasaka939 ¶[0004] (listing "hafnium (Hf)-containing material such as . . . $HfSiO_x$" as a "high-k material [with] dielectricity of more than ten (10)"). In fact,

hafnium silicon oxide is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicate (HfSiO) . . . ." '686 Patent, 29:16-24.

448. Akasaka's "gate dielectric film 315" is "depos[it]ed all over the substrate[301]," including area 301A, "for forming a p-type MISFET," as FIG. 26 shows. Akasaka ¶¶[0072]-[0073], ¶[0075]. From this, a POSITA would have recognized that "gate dielectric film 315" is formed on a second active region in semiconductor substrate 301, e.g., area pFET area 301A.

449. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon," in view of Akasaka.

i. [19H]: "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film"

450. Akasaka discloses "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film."

451. In the semiconductor device Akasaka's FIG. 26 shows, the pFET in area 301A has a gate electrode that includes conductive films 316a, 319, and 320.

Conductive film 316a discloses the claimed "first metal film," and either or both of conductive films 319 and 320 disclose the claimed "conductive film." Akasaka ¶¶[0076]-[0077], ¶[0082], ¶[0086].

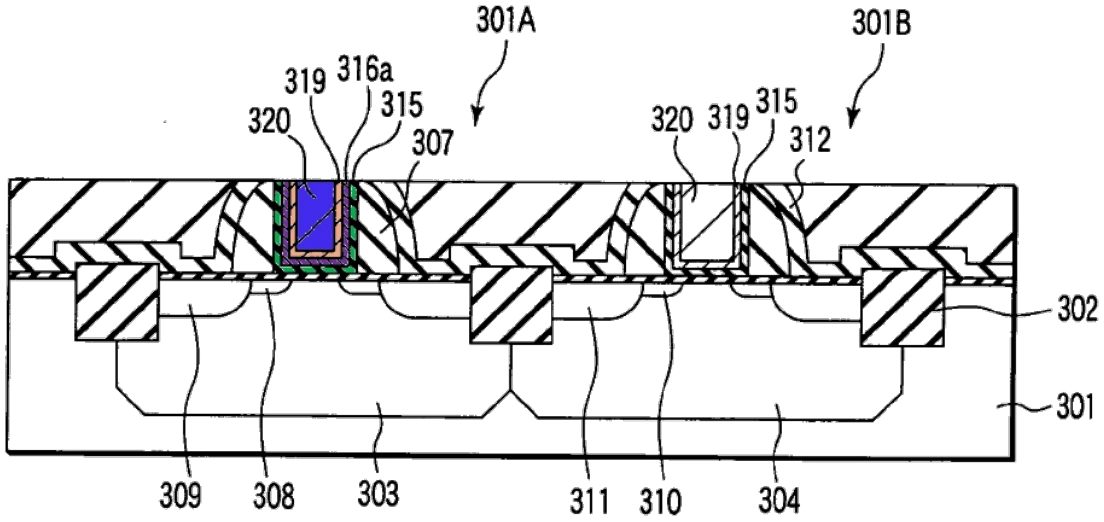


FIG. 26

Akasaka's FIG. 26 (annotated)

452. Conductive film 316a may be "a [Group-VIII] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of p^+-poly-crystalline silicon." Akasaka ¶[0077].

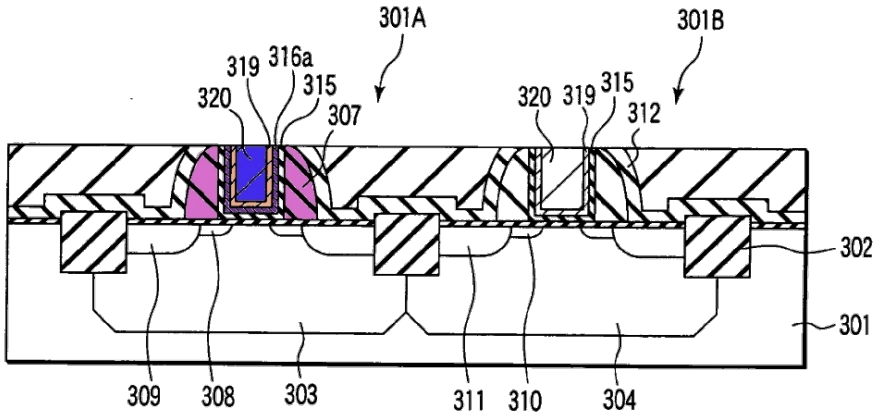
453. Conductive film 319 may be "a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon." Akasaka ¶[0085]. And conductive film 320 may be tungsten. Akasaka ¶[0086]. It "is preferably set to provide a sheet resistance of about 5Ω/□ or

less." Akasaka ¶[0086]. In one embodiment, "conductive film 319 and conductive film 320 are made of one integral film." Akasaka ¶[0086].

454. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film" in view of Akasaka.

j. [19I]: "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative"

455. Akasaka discloses "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative."



Akasaka's FIG. 26 (annotated)

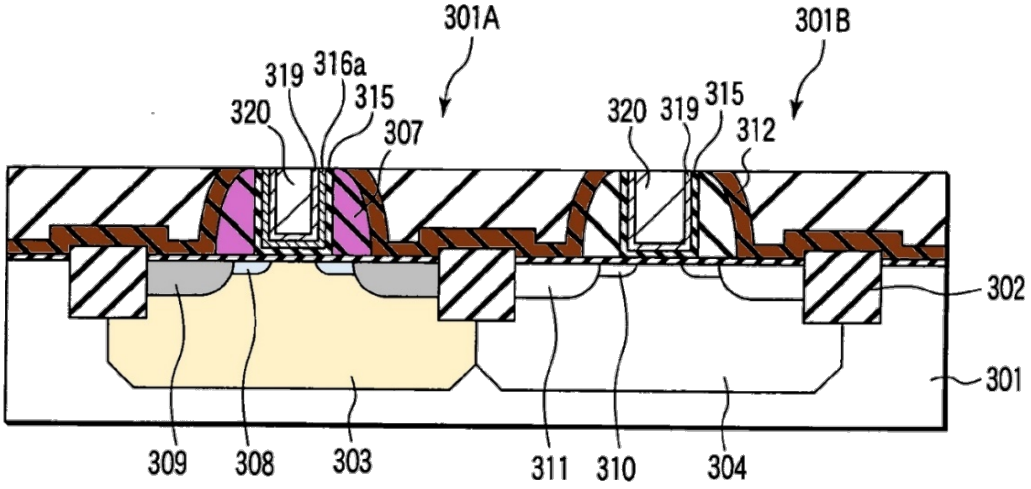
456. In the semiconductor device Akasaka's FIG. 26 shows, the pFET in area 301A includes "[a] gate sidewall 307 formed of an insulating film, such as a silicon nitride film." Akasaka ¶[0073]. As shown above, the gate sidewall 307

(purple) is formed on side surfaces of the gate electrode (conductive films 316a/319/320) of the pFET.

457. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative," in view of Akasaka.

k. [19J]: "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers"

458. Akasaka discloses "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers."



Akasaka's FIG. 26 (annotated)

459. In the semiconductor device Akasaka's FIG. 26 shows, the pFET in area 301A includes a "silicon nitride film 312 serving as an etching stopper." Akasaka ¶[0073]. This discloses the claimed "silicon nitride film."

460. As shown above, the gate electrode structure and its sidewalls 307 "are covered with silicon nitride film 312," such that Akasaka's silicon nitride film 312 (brown) extends over the side surfaces of the pFET gate electrode (conductive films 316a/319/320) on which gate sidewalls 307 (purple) are formed. *See* Akasaka ¶[0073] (explaining that "gate sidewall[s] 307 are covered with a silicon nitride film 312"), FIG. 16. Then, a chemical-mechanical polishing ("CMP") process is applied to silicon nitride film 312 to remove it from above the upper surfaces of the gate electrode structures. *See* Akasaka ¶[0074], ¶[0087].

461. As shown above, Akasaka's silicon nitride film 312 (brown) extends over upper surfaces of area 301A (the second active region)—e.g., in n-type well region 303 and p-type source/drain layers 309—located laterally outside of gate sidewalls 307 (purple).

462. For the same reasons I explain above, a POSITA also would have found it obvious that "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the

second active region laterally outside the second sidewall spacers," in view of Akasaka.

l. [19K]: "the first and second metal films are made of different metal materials"

463. Akasaka discloses "the first and second metal films are made of different metal materials."

464. As I explain for feature [19D], either or both of conductive film 319 and conductive film 320 disclose the claimed "second metal film." Conductive film 319 may be "a [Group-IVa, Group-Va, or Group-VIa] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . , as long as it has a metallic band structure with a work function close to that of n^+-poly-crystalline silicon," and conductive film 320 may be tungsten, which is also a metal. Akasaka ¶¶[0085]-[0086].

465. As I explain for feature [19H], conductive film 316a discloses the claimed "first metal film." Conductive film 316a may be "a [Group-VIII] pure metal, . . . a metal silicide, a metal nitride, or another compound . . . as long as it has a metallic band structure with a work function close to that of p^+-poly-crystalline silicon." Akasaka ¶[0077].

466. Conductive film 316a and conductive films 319/320 are thus made of different metal materials. Akasaka ¶[0077], ¶¶[0085]-[0086]. They are chosen from different elements of the periodic table to have different metallic band structures.

467. For the same reasons I explain above, a POSITA also would have found it obvious that "the first and second metal films are made of different metal materials" in view of Akasaka.

m. [19L]: "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes"

468. Akasaka discloses "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes."

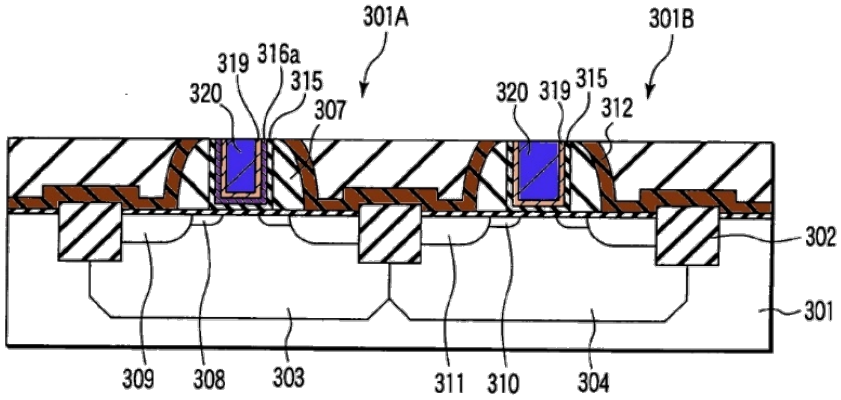


FIG. 26

Akasaka's FIG. 26 (annotated)

469. In the semiconductor device Akasaka's FIG. 26 shows, silicon nitride film 312 is not formed on any upper surfaces of the nFET and pFET gate electrodes. A POSITA would have recognized this from the manufacturing process Akasaka discloses. As Akasaka's FIGS. 16-18 illustrate, dummy gate electrodes 306 are formed where the nFET and pFET gate electrodes will be located. Akasaka ¶[0073]. As FIG. 16 shows below, silicon nitride film 312 and inter-level insulating film 313 are formed over dummy gate electrodes 306. Akasaka ¶[0073].

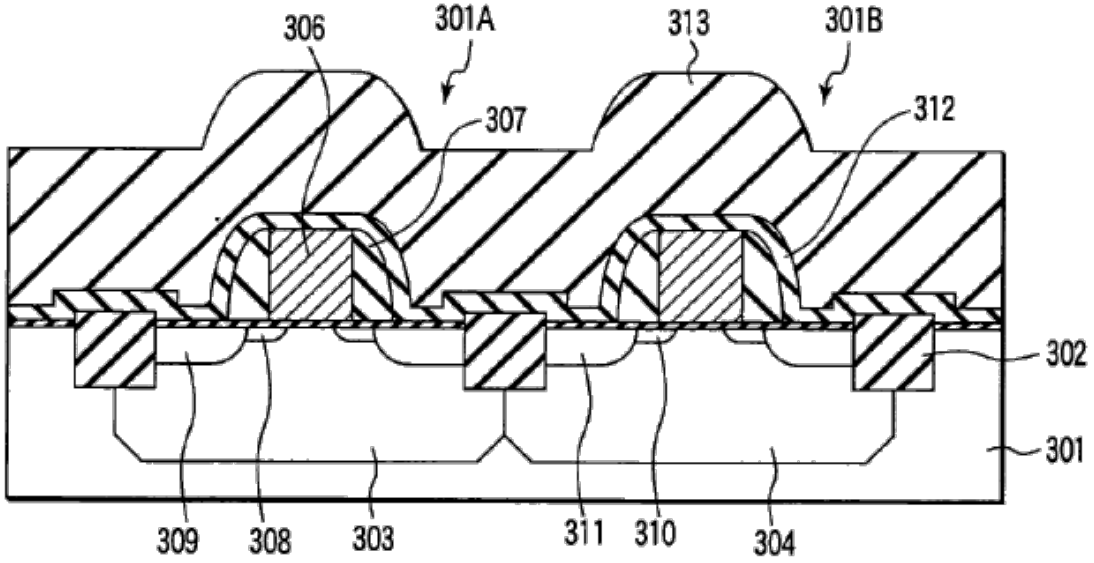


FIG. 16

Akasaka's FIG. 16

470. As FIG. 17 shows below, the inter-level insulating film is "polished from above by a CMP (Chemical Mechanical Polishing) method . . . to expose . . . the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306." Akasaka ¶[0074].

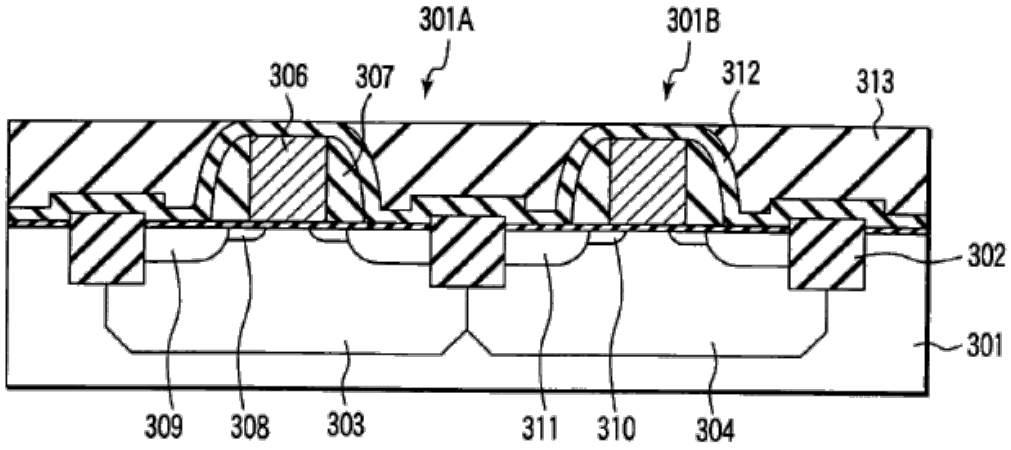


FIG. 17

Akasaka's FIG. 17

471. "Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314." Akasaka ¶[0074]. Thereafter, conductive layers 316a, 319, and 320 are deposited into recesses 314. Akasaka ¶¶[0075]-[0076], ¶¶[0084]-[00086], FIGS. 19, 25. After forming gate electrode layers 316a, 319, and 320 for the nFET and pFET, a second CMP step ensures that nothing—including silicon nitride film 312—remains on any upper surface of the gate electrodes. *See* Akasaka ¶[0087], FIG. 26. A POSITA would have understood this process prevents silicon nitride film 312 from being located on any upper surface of the first or second gate electrode.

472. For the same reasons I explain above, a POSITA also would have found it obvious that "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes" in view of Akasaka.

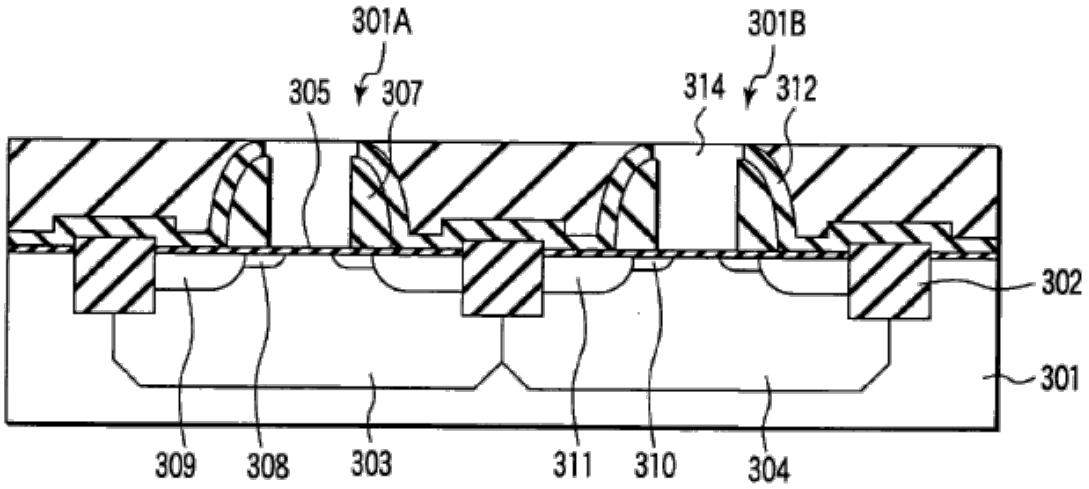


FIG. 18

Akasaka's FIG. 18

n. [19M]: "the first metal film is made of titanium nitride"

473. Akasaka discloses "the first metal film is made of titanium nitride."

474. In the semiconductor device Akasaka's FIG. 26 shows, conductive film 316a (the "first metal film") may be made of "a titanium nitride (TiN) film." Akasaka ¶[0077].

475. For the same reasons I explain above, a POSITA also would have found it obvious that "the first metal film is made of titanium nitride" in view of Akasaka.

2. Claim 20

476. Claim 20 depends from claim 19. I understand that means claim 20 requires all the same features as claim 19, plus the additional features recited in claim 20. Akasaka discloses all the features recited in claim 19 for the reasons I provide in Section IX.F.1 above.

477. Akasaka further discloses "wherein the first metal film has a thickness smaller than that of the second metal film."

478. As I explain for feature [19D], either or both of Akasaka's conductive films 319 and 320 discloses the claimed "second metal film." For purposes of claim 20, either conductive film 320 alone, or both conductive films 319 and 320 collectively, disclose the claimed "second metal film."

479. As I explain for feature [19H], Akasaka's conductive film 316a discloses the claimed "first metal film."

480. Akasaka discloses that conductive film 316a has a thickness "preferably set to be about 5 nm" or "a very small value of about 1 to 2 nm." Akasaka ¶[0077]. Akasaka discloses that conductive film 320 has a thickness of "about 40 to 50 nm." Akasaka ¶[0086]. Thus, conductive film 316a (the claimed "first metal film") has a thickness smaller than that of conductive film 320 alone or together with conductive film 319 (the claimed "second metal film").

481. For the same reasons I explain above, a POSITA also would have found it obvious that "the first metal film has a thickness smaller than that of the second metal film" in view of Akasaka.

3. Claim 21

482. Claim 21 depends from claim 19. I understand that means claim 21 requires all the same features as claim 19, plus the additional features recited in claim 21. Akasaka discloses all the features recited in claim 19 for the reasons I provide in Section IX.F.1 above.

483. Akasaka further discloses "wherein the first and second metal films have different work functions."

484. As I explain for feature [19D], either or both of conductive film 319 and conductive film 320 disclose the claimed "second metal film." For purposes of claim 21, conductive film 319 alone discloses the claimed "second metal film."

485. As I explain for feature [19H], Akasaka's conductive film 316a discloses the claimed "first metal film."

486. Akasaka discloses that conductive film 316a (the claimed "first metal film") "is preferably selected to have a work function close to that of p^+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV." Akasaka ¶[0077]; *see also* Akasaka ¶[0076] ("[T]he type of the material of the conductive film 316 should be determined in consideration of its work function.").

487. Akasaka also discloses that conductive film 319 (the claimed "second metal film") "is preferably selected to have a work function close to that of n^+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV." Akasaka ¶[0085]; *see also* Akasaka ¶[0084] ([T]he type of the material of the conductive film 319 should also be determined in consideration of its work function.").

488. Thus, conductive film 316a (the claimed "first metal film" with a work function of 4.8 to 5.3 eV) and conductive film 319 (the claimed "second metal film" with a work function of 3.9 to 4.2 eV) have different work functions.

489. For the same reasons I explain above, a POSITA also would have found it obvious that "the first and second metal films have different work functions" in view of Akasaka.

4. Claim 22

490. Claim 22 depends from claim 19. I understand that means claim 22 requires all the same features as claim 19, plus the additional features recited in claim 22. Akasaka discloses all the features recited in claim 19 for the reasons I provide in Section IX.F.1 above.

491. Akasaka further discloses "wherein the silicon nitride film has a thickness smaller than that of the first gate electrode."

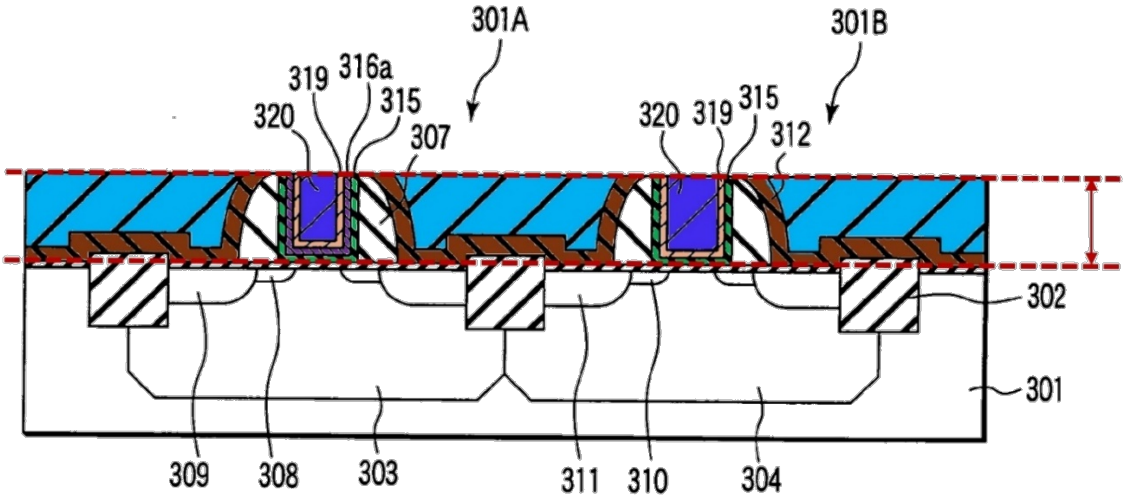


FIG. 26

Akasaka's FIG. 26 (annotated)

492. As I explain regarding feature [19D], Akasaka's silicon nitride film 312 discloses the claimed "silicon nitride film," and Akasaka's conductive films 319 and 320 in nFET area 310B disclose the claimed "first gate electrode." Akasaka discloses that silicon nitride film 312 has a smaller thickness than conductive films 319 and 320 in nFET area 301B because FIG. 26 (annotated above) shows silicon nitride film

312 (brown) is much thinner than conductive films 319 and 320 (yellow and purple, respectively) in nFET area 301B. This is consistent with what a person of ordinary skill in the art would have expected.

493. Accordingly, it is my opinion that Akasaka discloses claim 22.

494. It is also my opinion that Akasaka renders obvious "wherein the silicon nitride film has a thickness smaller than that of the first gate electrode." For essentially the same four reasons I discuss in Section IX.A.4 above, Akasaka's silicon nitride film 312 has a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B. The only differences between Aoyama and Akasaka regarding claim 22 are minor differences in the ranges of their respective gate dielectric and gate electrode thicknesses. As I further demonstrate below, however, these differences do not meaningfully affect the analysis I provide in Section IX.A.4. Thus, in my opinion, a POSITA would have found claim 22 obvious in view of Akasaka for at least the same four reasons, as well as the relative thicknesses depicted in Akasaka's FIG. 26.

495. **The first reason** a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to have a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B is that a POSITA would have expected it. In fact, a POSITA would have found it highly unusual were it otherwise.

496. Akasaka's nFET and pFET gate electrodes in areas 301A and 301B are planarized to have the same total height. Akasaka ¶¶[0073]-[0076], ¶¶[0084]-[0086], FIGS. 19, 25. Thus, as the red arrow above indicates, the thickness of silicon nitride film 312 (brown), plus the thickness of inter-level insulating film 313 (blue), is necessarily equal to the total nFET gate height, i.e., the sum of thicknesses of gate dielectric film 315 and conductive films 319 and 320. Mathematically, that means:

$$\mathbf{T_{312} + T_{313} = T_{315} + T_{319} + T_{320}} \qquad \textbf{(Eq. 1)}$$

where $\mathbf{T_x}$ is the thickness of layer **x**.

497. Translating the requirement of claim 22 into these mathematical variables, claim 22 applied to Akasaka requires:

$$\mathbf{T_{312} < T_{319} + T_{320}} \qquad \textbf{(Eq. 2)}$$

498. Substituting Equation 2 into Equation 1, the following inequality obtains for Akasaka:

$$\mathbf{T_{319} + T_{320} + T_{313} > T_{315} + T_{319} + T_{320}} \qquad \textbf{(Eq. 3)}$$

499. Canceling the common variables on both sides of the inequality (T_{319} and T_{320}) gives the following relationship between the thickness of inter-level dielectric film 313 and the thickness of gate dielectric film 315:

$$\mathbf{T_{313} > T_{315}} \qquad \textbf{(Eq. 4)}$$

In other words, Akasaka satisfies claim 22 so long as the thickness of inter-level dielectric film 313 is greater than the thickness of gate dielectric film 315.

500. This inequality illustrates in stark terms why Akasaka renders obvious claim 22. A POSITA would have expected Akasaka's inter-level dielectric film 313 to be significantly thicker than gate dielectric film 315 and would have found it highly unusual were it otherwise.

501. A POSITA would have known the thickness of a gate dielectric is negligible compared to a gate electrode. The gate dielectric is famous for being an extremely thin insulating layer, which is necessary to achieve an extraordinarily ***large*** capacitance. *See* Baklanov, xiii (describing "the high drive current and gate capacitance required of scaled MOSFETs"). Interlayer dielectric films, on the other hand, require ***small*** capacitance and are thus much thicker. That is, "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. Baklanov, xiii.

502. According to Akasaka, gate dielectric layer 315 "is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less." Akasaka ¶[0075]. Mathematically, EOT = thickness × (3.9/κ), which means gate dielectric film 315 must have a thickness (in nm) of (1.5/3.9)κ or less. Baklanov, xiii (explaining that "t_{ox}(eq)= t_{diel}(3.9/k_{diel})"). For κ = 30 (an extreme case), the thickness would be less than about 11.5 nm. *See* Baklanov, xiii ("Dielectrics with values approximately between 10 and 30 are under consideration."). For κ = 10, the thickness would be about 3.8 nm. Being generous with the value of κ, a POSITA thus would have

understood Akasaka to disclose that the gate dielectric layer 315 has a thickness ***at most*** about 12 nm. Of course, the goal is to make the EOT of dielectric film 315 ***less*** than that, such that a more realistic number would have been in the range of about 2 nm to 4 nm. *See* Akasaka939 ¶[0004], ¶[0043] (less than 3.0 nm), Tbl. 1 (same); Aoyama ¶[0106] (2.0 nm); '686 Patent, 11:31-34 (2 nm), 24:36-39 (same). But the difference between 2 nm and 12 nm is immaterial to my analysis here. The point is that gate dielectric film 315, like all gate dielectric films in this technology, is extremely thin—much thinner than any interlayer dielectric film.

503. Any real-world device, such as the ones below, can be used to illustrate the point visually. *See also* James, Figs. 1-3, 5-6, 8-12; Mistry2007, Fig. 6; Thompson2004, Fig. 2; Morin, Fig. 1.

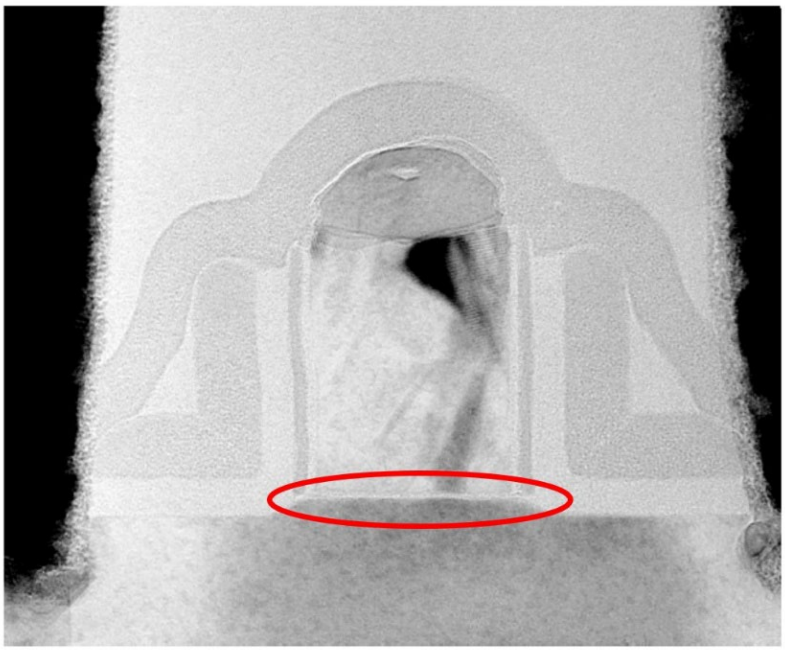


Figure 3. Transistor in TI DSP

James's Fig. 3 (annotated)

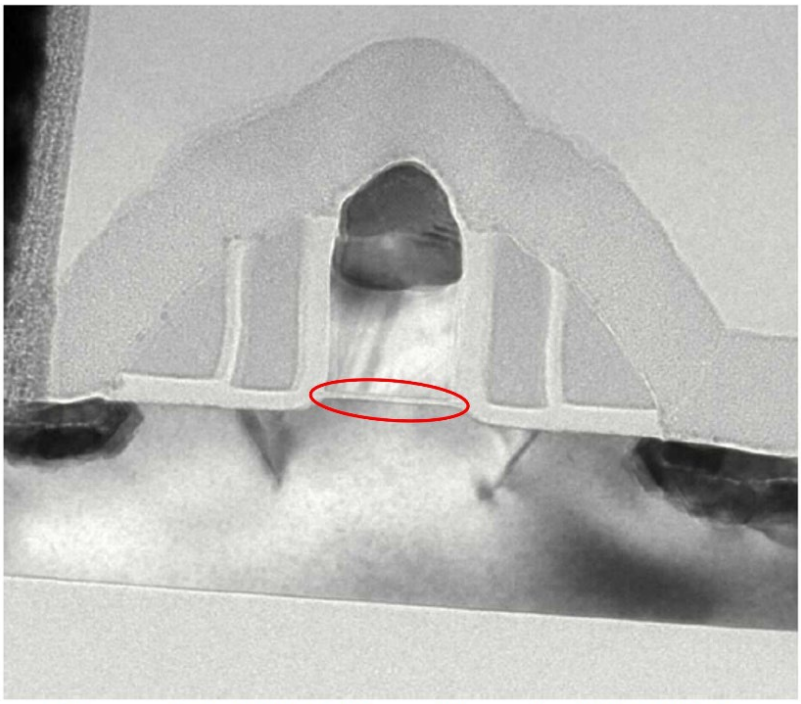
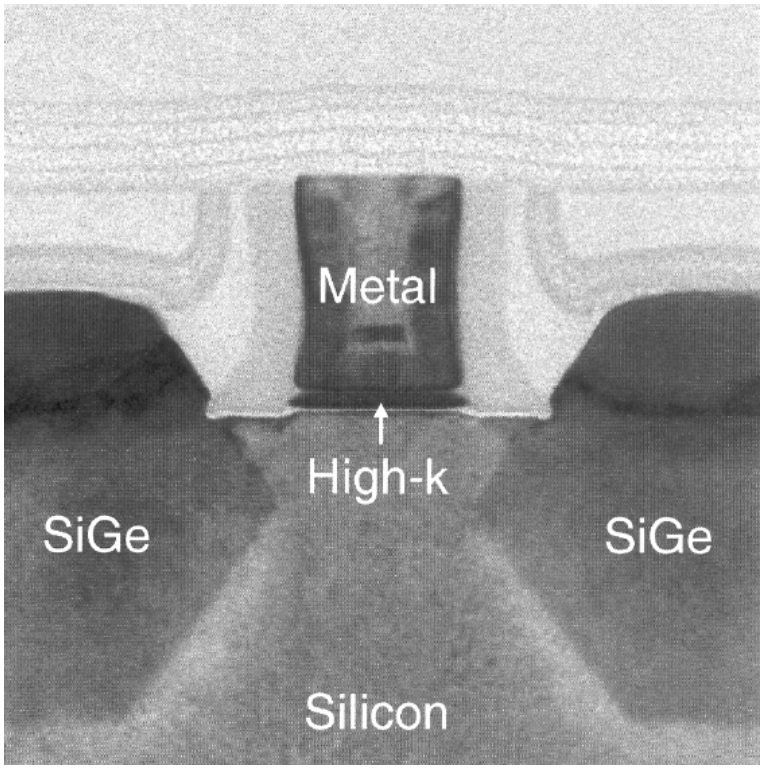


Figure 11. NMOS Transistor in AMD Athlon

James's Fig. 11 (annotated)



Mistry_Presentation, 16 (excerpted)

504. This is why I can say without any doubt that a POSITA would have found it obvious for Akasaka's inter-level dielectric film 313 to be significantly thicker than gate dielectric film 315 and would have found it highly unusual were it otherwise. The prior-art micrograph immediately above illustrates the point well. *See* Mistry2007, Fig. 6 (showing Intel's 45nm device); Mistry_Presentation, 16 (same). The interlayer dielectric is significantly thicker than the gate dielectric in the same type of device Akasaka discloses.

505. As another example that is similar to Akasaka, Nakajima (shown below) teaches a metal layer 403 that is 20 nm thick and a metal layer 405 that is 100 nm thick, meaning the gate electrode is at least about 120 nm thick (*see* Nakajima, FIG. 52 below). Nakajima ¶[0317]. The silicon nitride CESL 418 is only about 30 nm thick, and interlayer insulating layer 415a is initially 250 nm thick before being planarized down to what is still more than 90 nm thick (the difference between the thickness of gate electrode layers 403 and 405, minus the thickness of CESL 418). Nakajima ¶[0326], FIGS. 51-52. A thickness of 90 nm is more than an order of magnitude thicker than any conceivable gate dielectric layer, which is indicative of the relative thicknesses a POSITA would have expected.

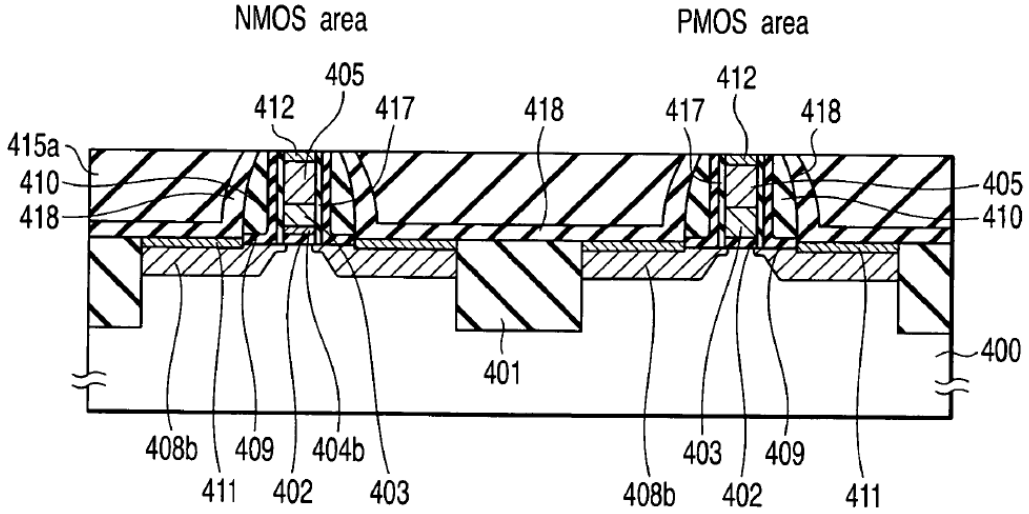


FIG. 52

Nakajima's FIG. 52

506. Again, without a doubt, a POSITA would have found it obvious for Akasaka's inter-level dielectric film 313 to be thicker than gate dielectric film 315 and would have found it highly unusual were it otherwise. Inter-level dielectric film 313 would have been expected to be significantly thicker than gate dielectric film 315.

507. Because Akasaka's silicon nitride film 312 is thinner than Akasaka's nFET gate electrode (conductive films 319 and 320) so long as inter-level dielectric film 313 is thicker than gate dielectric film 315, a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to be thinner than the nFET gate electrode. Not only would this have been obvious, but a POSITA would have found it very unusual were it otherwise in Akasaka's structure. *See* Akasaka, FIG. 26.

508. **The second reason** a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to have a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B is that this was one of only two or three possibilities. In fact, it was the most well-known of those very limited options.

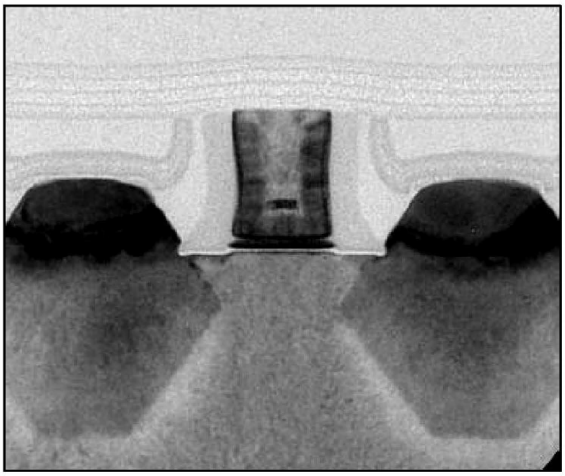
509. I have been told that when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.

510. There was a design need to make Akasaka's inter-level insulating film 313 thicker than Akasaka's gate dielectric film 315 because "gate and interlayer (ILD) dielectric films" have "opposing requirements" in terms of thickness. *See* Baklanov, xiii. The design need would have indicated to a person ordinarily skilled in the art that Akasaka's inter-level insulating film 313 should be thicker than Akasaka's gate dielectric film 315. The result, as I explain above, is that Akasaka's silicon nitride film 312 would be thinner than Akasaka's nFET gate electrode (i.e., the collective height of conductive films 319 and 320) as claimed.

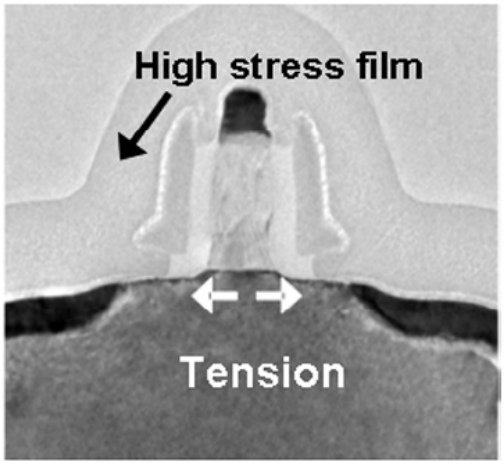
511. Additionally, the design needs of Akasaka's device dictate only two options for the thickness of Akasaka's silicon nitride film 312: either it is thinner than Akasaka's nFET gate electrode, or it is not. Even being generous, there are only

three options available in Akasaka's device structure: Akasaka's silicon nitride film 312 is thinner than Akasaka's nFET gate electrode; Akasaka's silicon nitride film 312 is thicker than Akasaka's nFET gate electrode; or Akasaka's silicon nitride film 312 has the same thickness as Akasaka's nFET gate electrode. Again, Akasaka's planarized structure sets a restriction that the collective thickness of silicon nitride film 312 and inter-level insulating film 313 cannot exceed the height of Akasaka's gate structures.

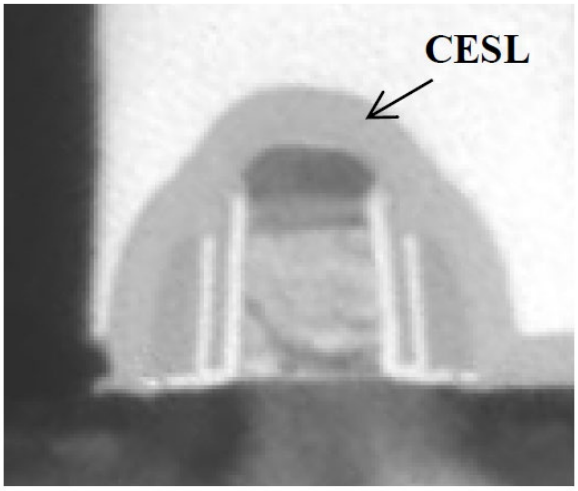
512. I have been told that two or three options qualify as a finite number of identified, predictable solutions under the law, and I agree in the context at issue here (i.e., the thickness of Akasaka's silicon nitride film 312 relative to the thickness of Akasaka's nFET gate electrode). Of the limited options available, a silicon nitride film 312 thinner than the nFET electrode was certainly within the technical grasp of a POSITA. Indeed, it would have been expected. A POSITA thus would have found it obvious. Numerous examples below illustrate the point. *See* Mistry2007, Fig. 6; James, Figs. 1-3, 5-6, 8-12; Morin, Fig. 1; Thompson2004, Fig. 2.



Mistry2007's Fig. 6



Thompson2004's Fig. 2 (excerpted)



Morin's Fig. 1

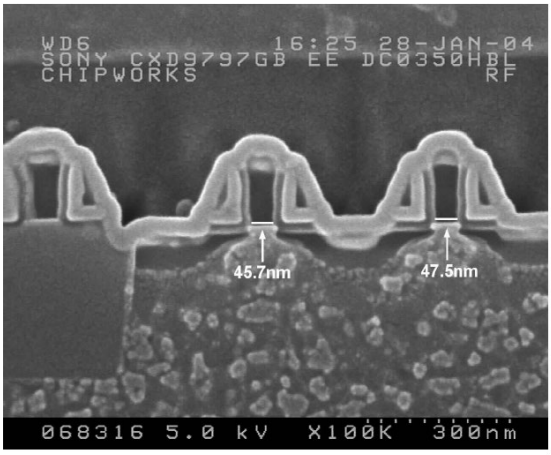


Figure 1. SEM Cross-Section of NMOS Transistors in Sony PSX

James's Fig. 1

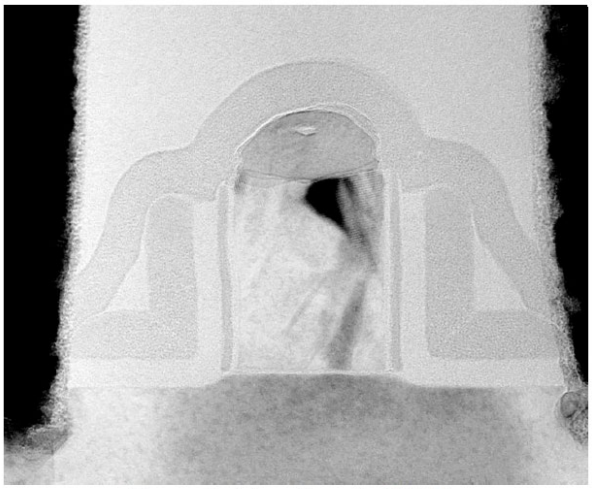


Figure 3. Transistor in TI DSP

James's Fig. 3

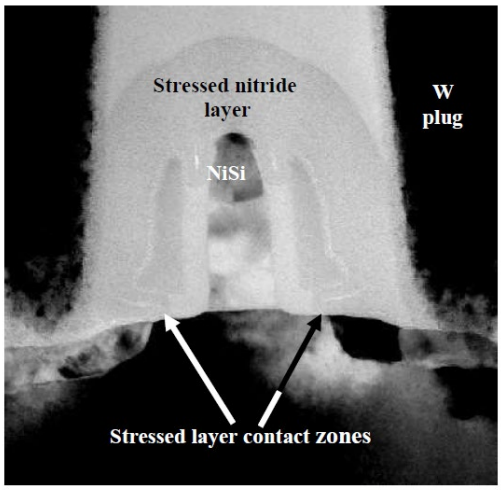


Figure 5. NMOS Transistor in Intel Prescott

James's Fig. 5

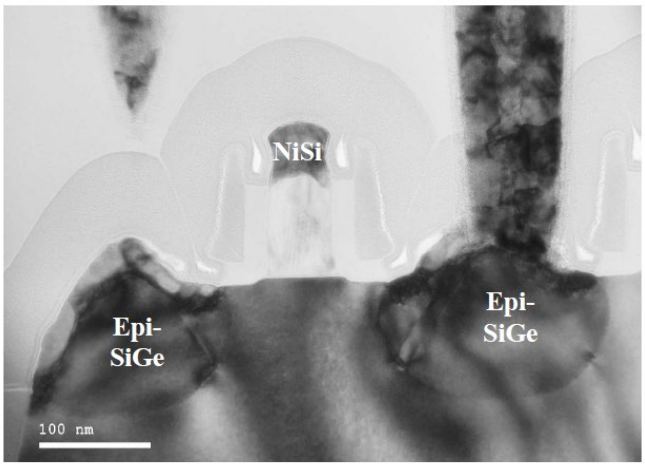


Figure 6. Intel PMOS Transistor

James's Fig. 6

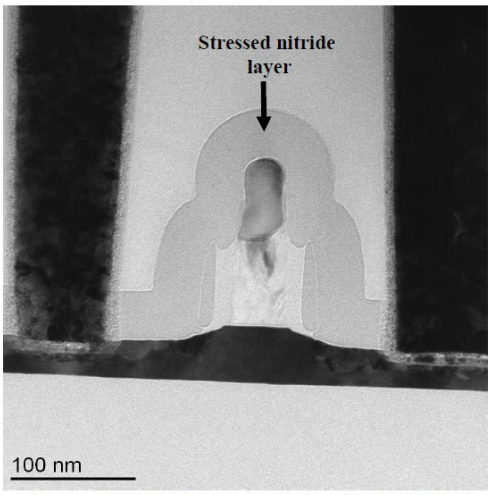


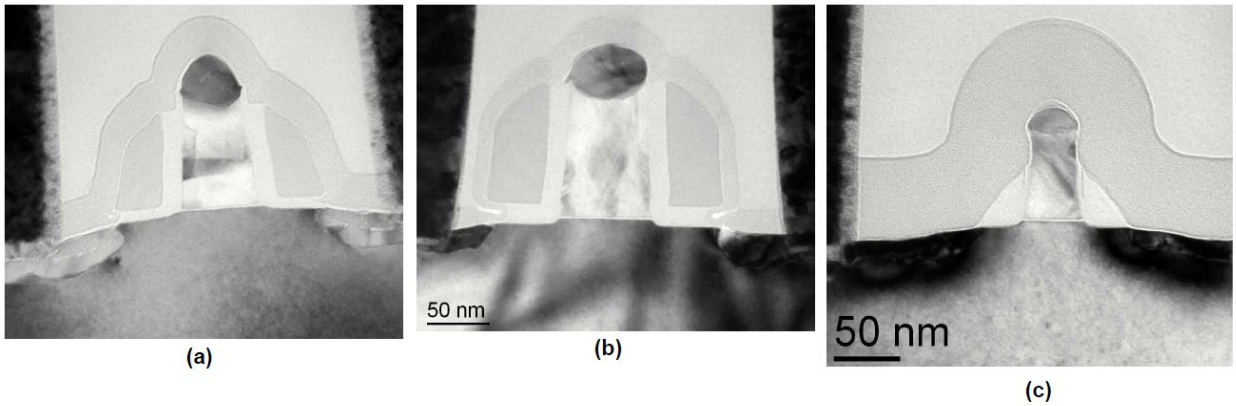
Figure 8. NMOS Transistor in IBM PPC970FX

James's Fig. 8



Figure 9. PMOS Transistor in IBM PPC970FX

James's Fig. 9



(a) (b) (c)

Figure 10. Transistors in (a) Xilinx Spartan-3, (b) Altera Stratix-II, (c) Transmeta Efficeon-2

James's Fig. 10

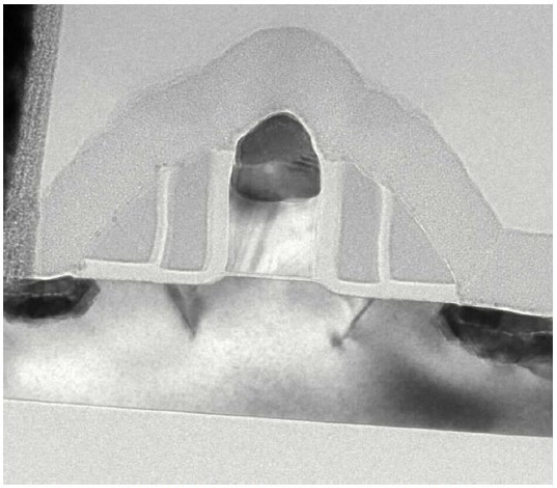


Figure 11. NMOS Transistor in AMD Athlon

James's Fig. 11

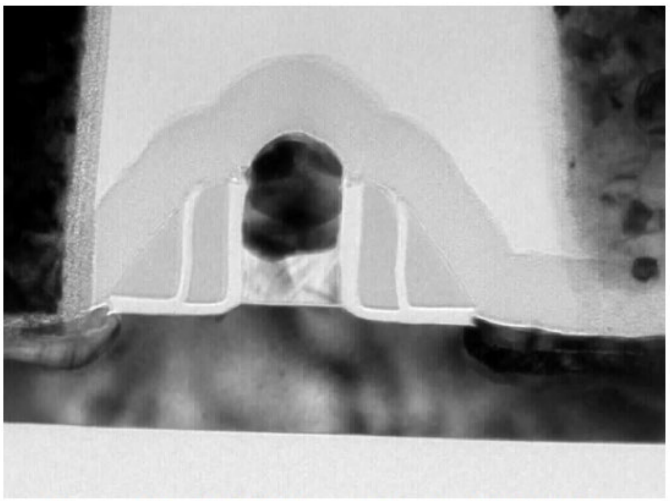


Figure 12. PMOS Transistor in AMD Athlon

James's Fig. 12

513. Thus, because there are only a finite number of identified, predictable solutions to comply with the design requirements of Akasaka's device, and because the most predictable solution would have been to make Akasaka's silicon nitride film 312 thinner than Akasaka's nFET gate electrode (i.e., thinner than conductive films 319 and 320, collectively, in area 301B), a POSITA would have found that solution obvious.

514. **The third reason** a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to have a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B is that the disclosed thickness of Akasaka's conductive films 319 and 320 significantly exceeds the typical thickness used for silicon nitride etch stopper films like Akasaka's silicon nitride film 312.

515. I have been informed that when evidence shows techniques and conditions were routine such that a POSITA would have understood a claimed property to be "typical," it would have been obvious. This leads me to the fourth reason a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to be thinner than Akasaka's nFET gate electrode (conductive films 319 and 320, collectively, in area 301B).

516. Akasaka discloses that conductive film 320 is "about 40 to 50 nm" and that conductive film 319 is "about 1 to 2 nm." Akasaka ¶¶[0085]-[0086]. Thus, at the absolute minimum, Akasaka's nFET gat electrode is about 41 nm to 52 nm thick. A POSITA would have understood that silicon nitride etch stopper films like Akasaka's silicon nitride film 312 "ha[ve] a typical thickness of 20 nm" or so—much less than the minimum thickness of Akasaka's nFET gate electrode. Eneman, 1446. That is, a typical silicon nitride CESL thickness was less than a typical gate electrode thickness in MOSFETs like Akasaka's. *See* Nakajima ¶[0317], ¶[0326], FIG. 52; Mistry2007, Fig. 6; James, Figs. 1-3, 5-6, 8-12; Morin, Fig. 1; Thompson2004, Fig. 2.

517. A POSITA thus would have found it obvious that Akasaka's silicon nitride film 312 is thinner than Akasaka's nFET gate electrode (i.e., conductive films 319 and 320, collectively, in area 301B).

518. **The fourth reason** a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to have a thickness smaller than the collective thickness of conductive films 319 and 320 in area 301B is that the thickness of silicon nitride film 312 affects the amount of stress, and tuning it would have been a matter of routine optimization.

519. I have been told that where claimed dimensions are known to be result-effective variables, it is not inventive to discover the optimum or workable ranges by routine experimentation. I have been told that such a claimed dimension is only patentable if it produces a new and unexpected result that differs in kind, not merely degree, from the prior art. This leads me to the fifth reason a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to be thinner than Akasaka's nFET gate electrode (conductive films 319 and 320, collectively, in area 301B).

520. Here, silicon nitride CESL thickness was a variable known to affect stress. *See generally* Eneman. Eneman, for example, details "[t]he effect [of scaling] on CESL-induced stress" due to silicon nitride CESL films. Eneman, 1447. Silicon nitride CESL thickness was thus a known, result-effective variable. *See, e.g.*, Eneman, 1447-48, Figs. 2-3.

521. Implementing Akasaka's silicon nitride film 312 to be thinner than Akasaka's nFET gate electrode, as claimed, would not have yielded any unexpected

results, as the relationship between silicon nitride CESL thickness and the stress it induces was known and predictable. *See generally* Eneman (including Fig. 3).

522. Applying the legal principles explained to me, this provides another reason a POSITA would have found it obvious for Akasaka's silicon nitride film 312 to be thinner than Akasaka's nFET gate electrode (conductive films 319 and 320, collectively, in area 301B). That is, making silicon nitride film 312 thinner than the nFET gate electrode would have involved nothing more than routine experimentation to discover the optimum or workable ranges of CESL thickness.

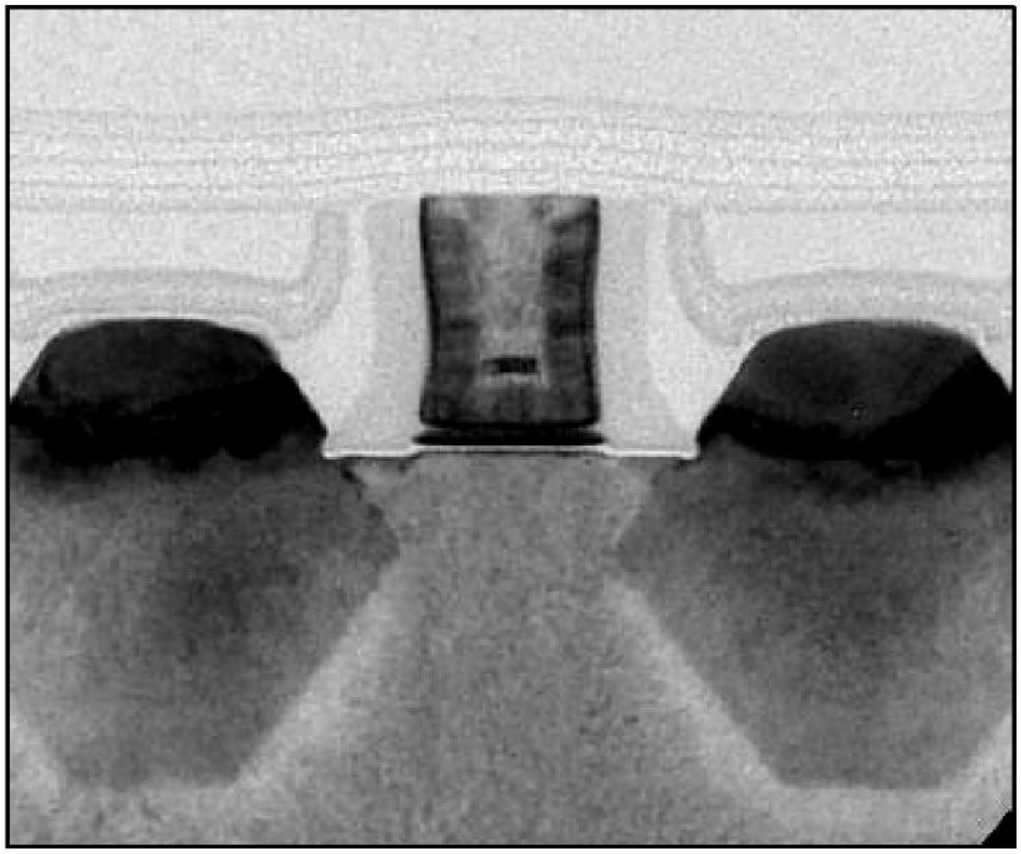
523. For all four of these additional reasons, in addition to the relative thicknesses disclosed by Akasaka's FIG. 26, it is my opinion that claim 22 would have been obvious in view of Akasaka's disclosures.

G. Ground 2C: The Akasaka-Hsu823 Combination Renders Obvious Claims 1-4, 6-10, 23-29, 31, and 33-35

1. A POSITA would have found it obvious to implement SiGe stressors in the source/drain regions of Akasaka's pFET

524. By the time the application for the '686 Patent was filed, SiGe stressors had already been known and used in three generations of high-volume commercial transistors. *See* Thompson2004, 1790-91 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry2007, 247-48 (describing Intel's 45nm devices); Mistry_Presentation (same). The most recent generation prior to the filing date of the '686 Patent, shown publicly in images like the one below

before the application for the '686 Patent, not only used SiGe stressors but also high-κ gate dielectrics and metal gates in an RMG process. *See generally* Mistry2007; Mistry_Presentation, 14-19. By the time the application for the '686 Patent was filed, such SiGe stressors were standard industry practice. *See* Section VI.D above.

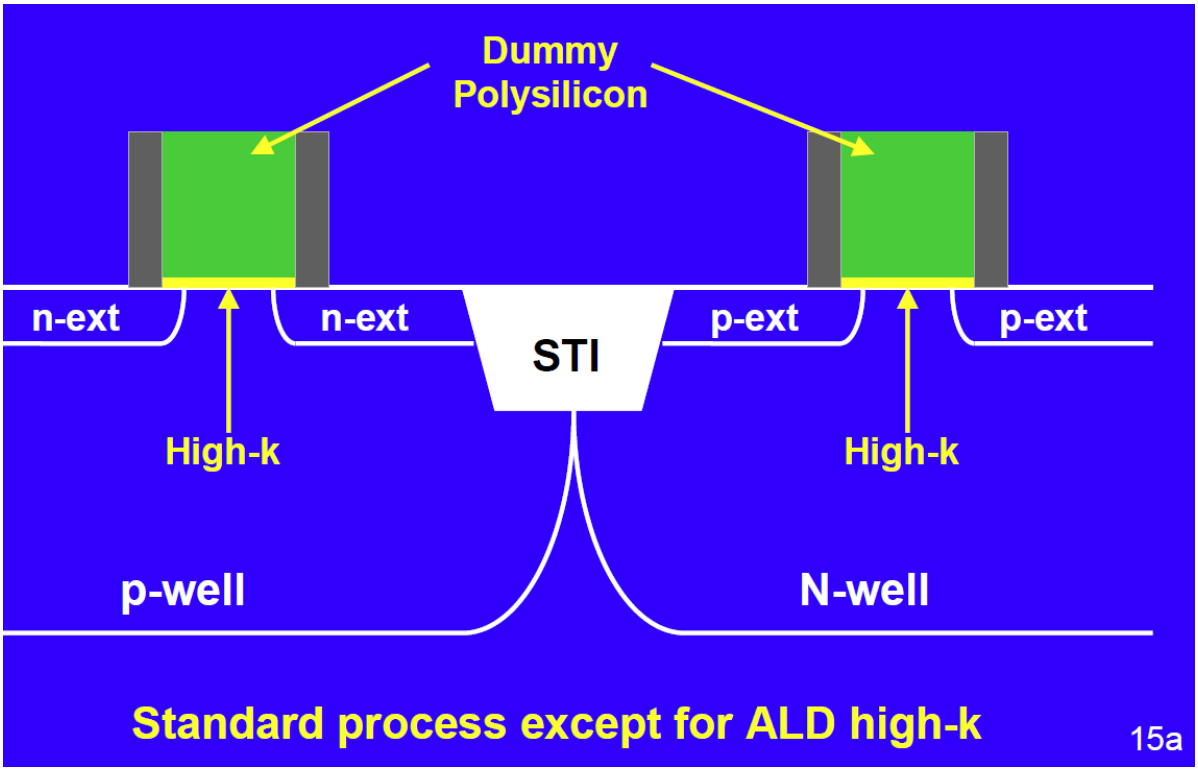


Mistry2007's Fig. 6

525. Although Akasaka may not expressly describe using SiGe stressors, it would have been obvious to use SiGe stressors in Akasaka's FIG. 26 transistor design, as the micrograph above—showing Intel's high-volume 45nm generation of devices that had been in production since 2007—should make abundantly clear. Mistry2007, Fig. 6; *see also* Mistry_Presentation, 16.

526. At the December 2007 International Electron Devices Meeting ("IEDM")[16] in Washington, D.C., which I attended and for which I organized a short course and two speakers on high-κ/metal gates, Kaizad Mistry of Intel described Intel's 45 nm process flow. Again, it was a high-κ/RMG process. *See generally* Mistry_Presentation, 14-19 (in-person IEDM presentation); Mistry2007 (publication of related IEDM paper).

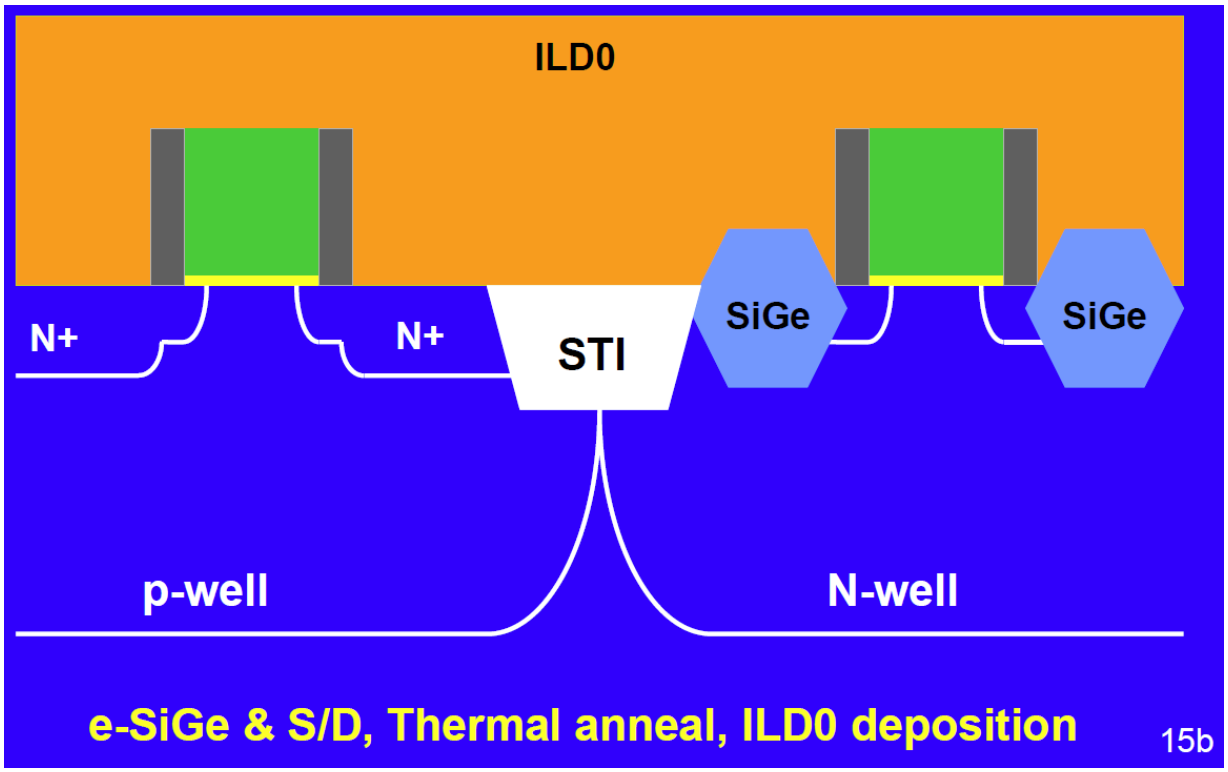
527. To begin, nFET and pFET dummy gate structures are formed. The dummy gates comprise high-κ dielectrics (yellow) and dummy polysilicon gate electrodes (green). Mistry_Presentation, 15a (below).



Mistry_Presentation, 15a

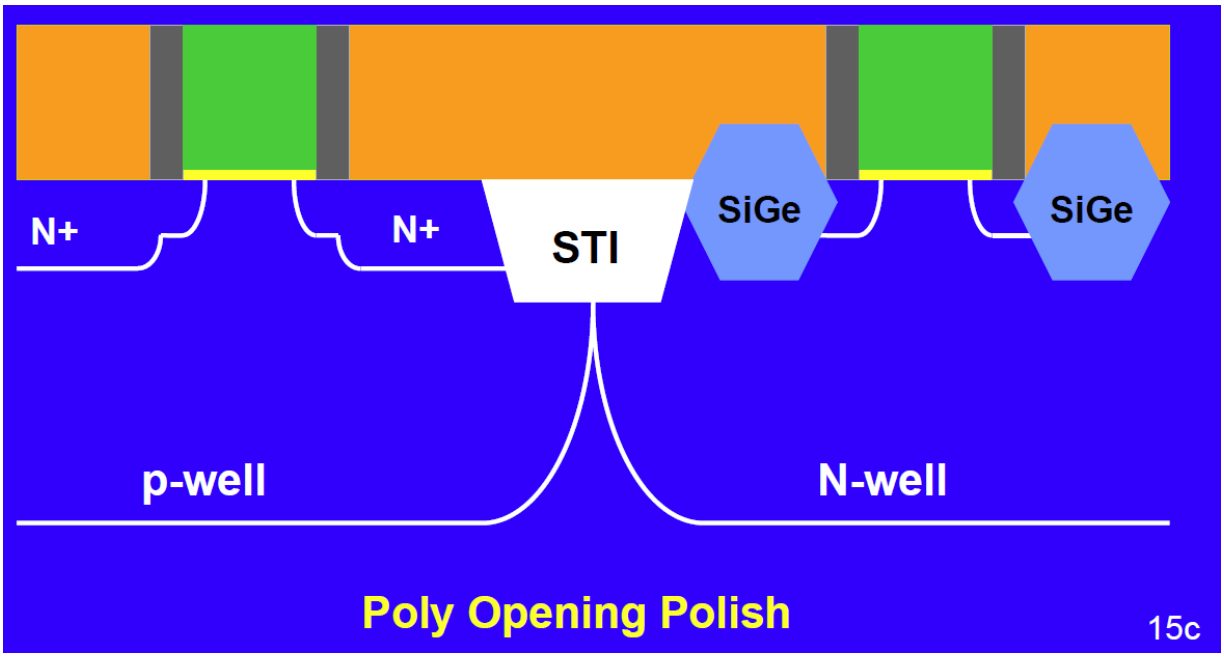
[16] IEDM is a very prominent and well attended conference in the field.

528. Next, the source/drain regions are formed, including the formation of embedded epitaxial SiGe source/drain regions for the pFET (light blue hexagons). *See* Section VI.D above. This is followed by thermal annealing to activate implanted dopants and then by a blanket deposition of interlayer dielectric ILD0 (orange), as shown below. Mistry_Presentation, 15b.



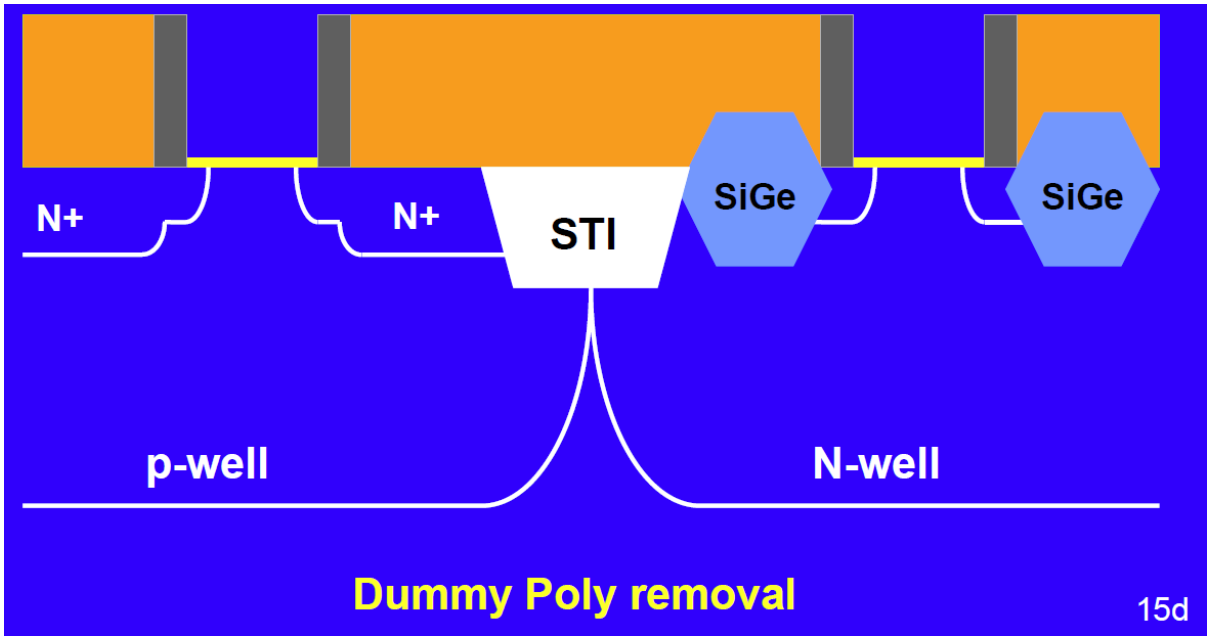
Mistry_Presentation, 15b

529. Following this, a polishing step is performed to planarize interlayer dielectric ILD0 (orange) such that its top surface aligns with the top surfaces of the dummy polysilicon gate electrodes (green). Mistry_Presentation, 15c.



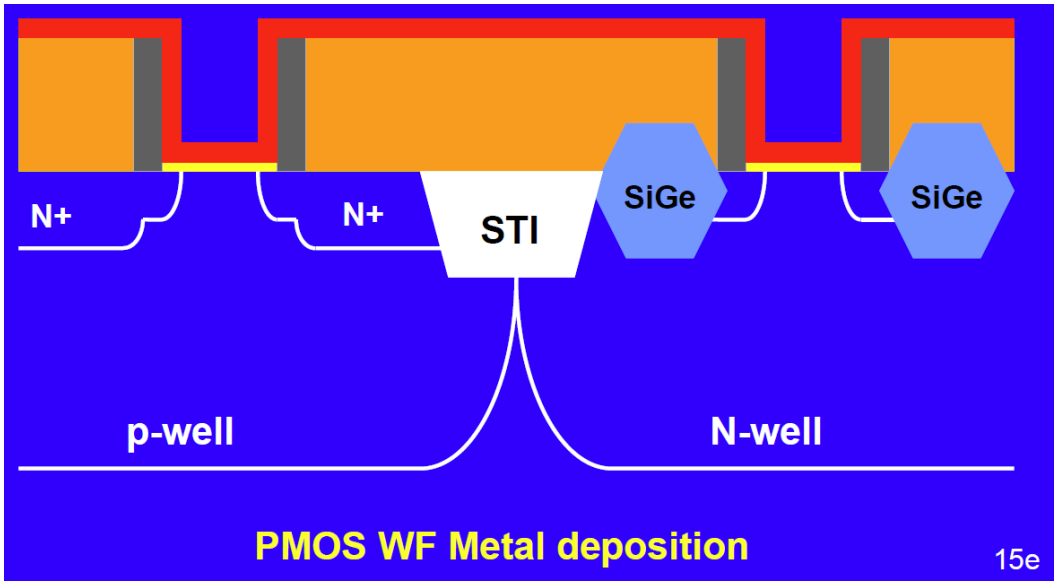
Mistry_Presentation, 15c

530. Next, the dummy polysilicon gate electrodes (green) are removed by etching. Mistry_Presentation, 15d.



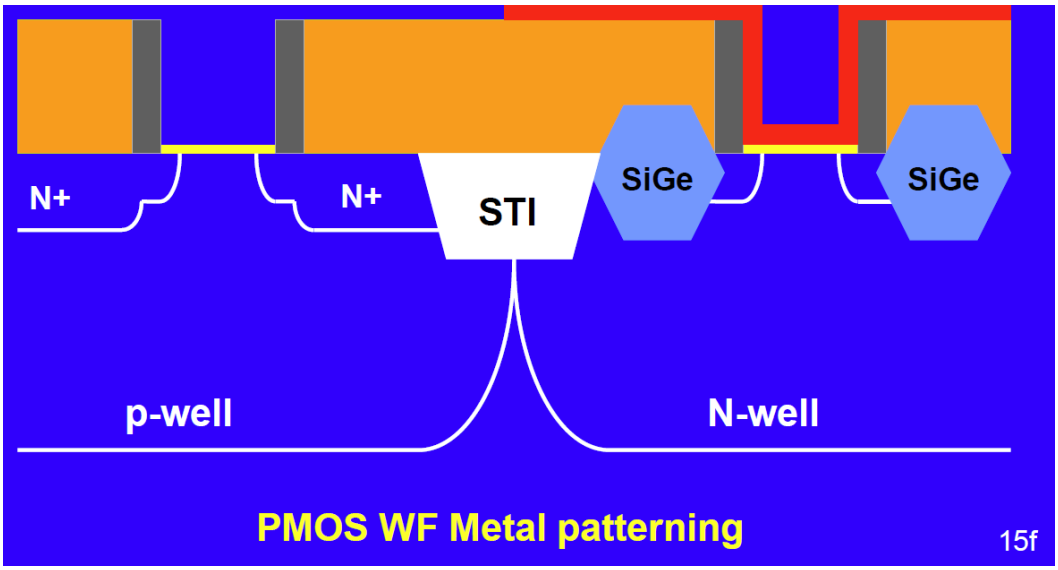
Mistry_Presentation, 15d

531. The pFET work-function metal (red) is then deposited over the wafer, including in the void left by removing the dummy polysilicon gate electrodes. Mistry_Presentation, 15e.



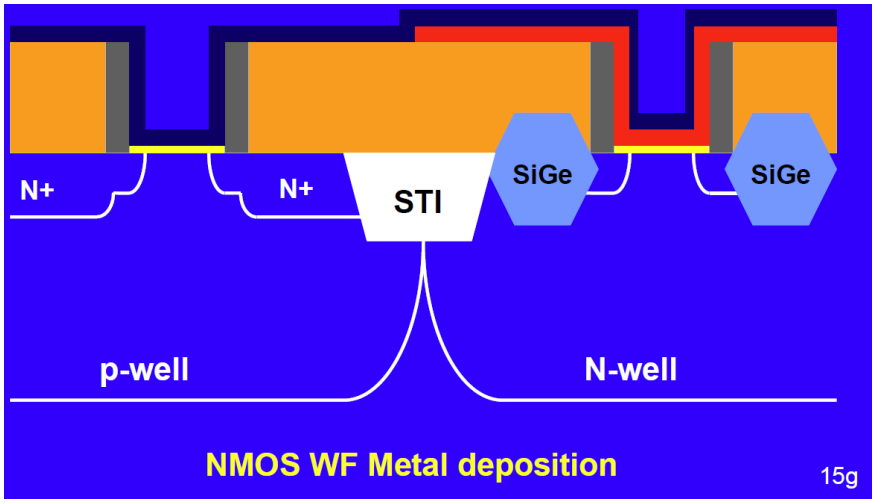
Mistry_Presentation, 15e

532. Because this is the pFET work-function metal, it is removed from the wafer by etching everywhere except in the pFET regions. Mistry_Presentation, 15f.



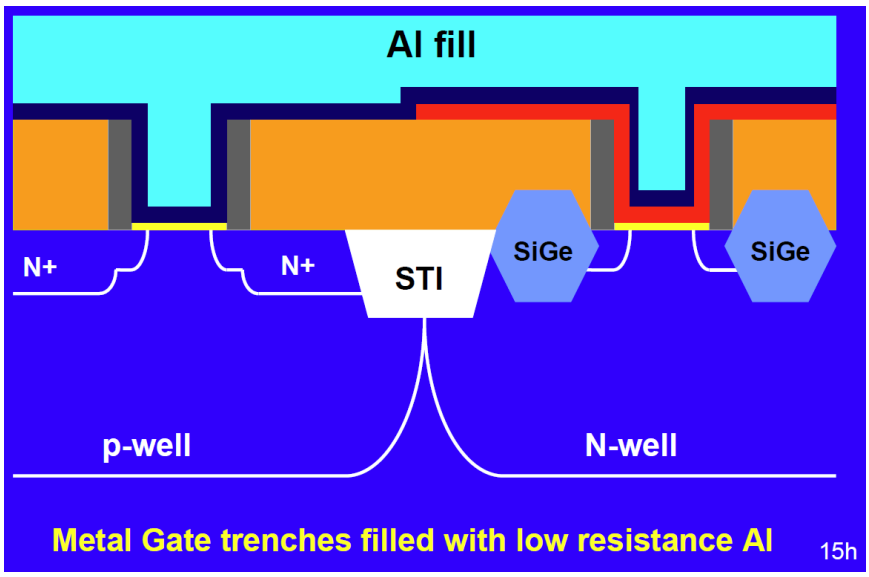
Mistry_Presentation, 15f

533. Next, the nFET work-function metal (dark blue) is deposited over the wafer, including in the voids left by removing the dummy polysilicon gate electrodes. Mistry_Presentation, 15g.



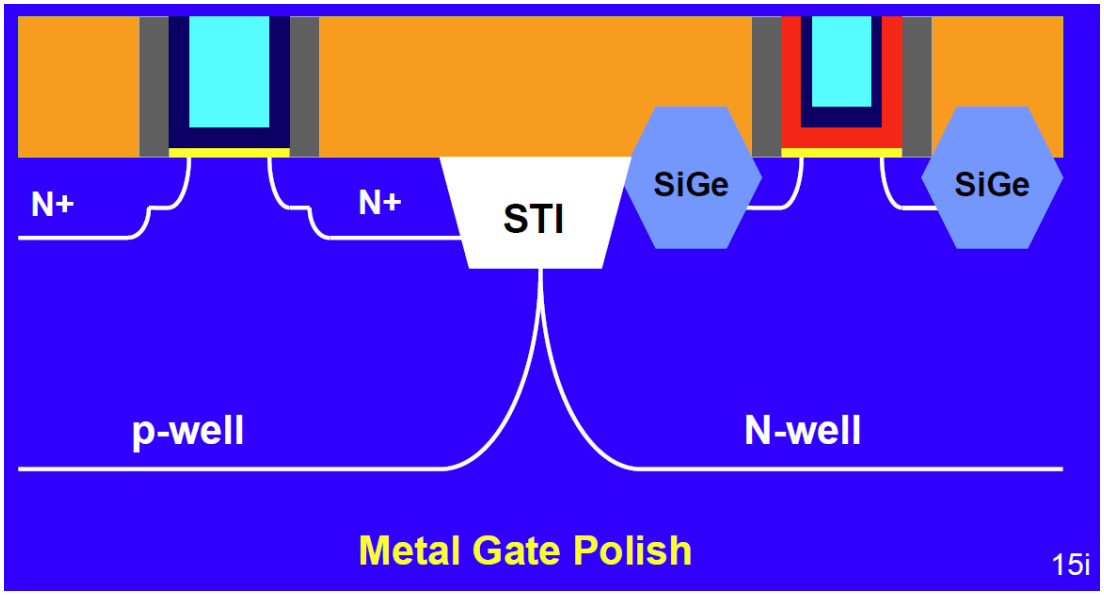
Mistry_Presentation, 15g

534. Then, an aluminum filler (turquoise) is deposited over the entire wafer to fill the remaining voids left in the nFET and pFET gate electrode regions. Mistry_Presentation, 15h.

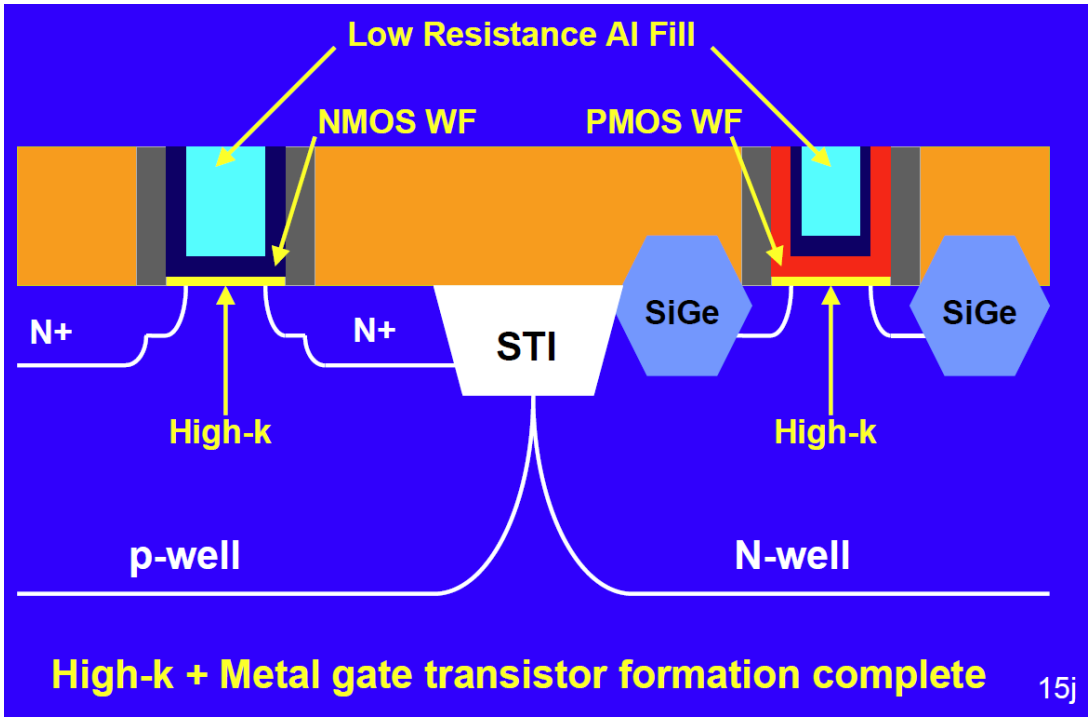


Mistry_Presentation, 15h

535. A second polishing step is done to planarize the metal films such that the top surfaces of the replacement metal gate electrodes are aligned with the top surface of interlayer dielectric film ILD0 (orange). Mistry_Presentation, 15i-15j.

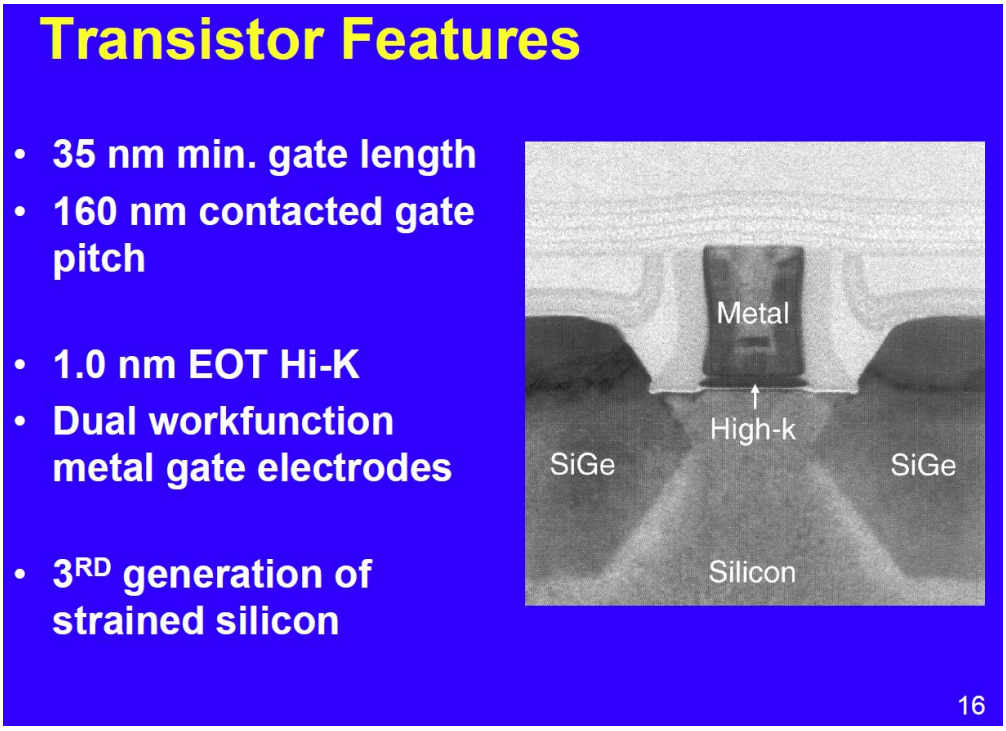


Mistry_Presentation, 15i

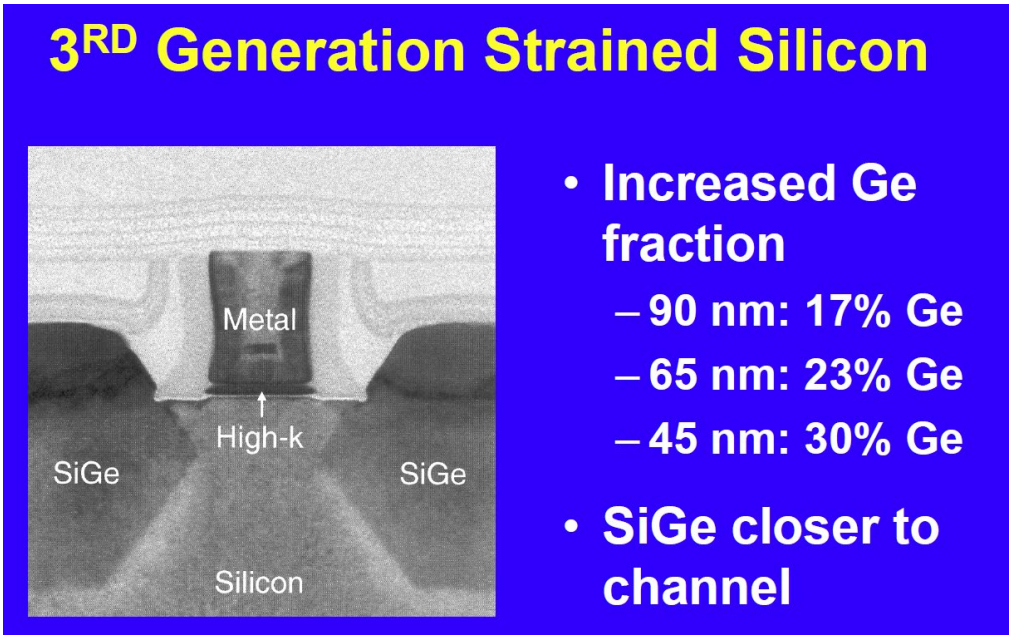


Mistry_Presentation, 15j (same as 15i but with additional labels)

536. The final structure made using Intel's 45 nm high-κ/RMG process appears below. Mistry_Presentation, 16, 19.



Mistry_Presentation, 16 (micrograph showing a pFET)



Mistry_Presentation, 19 (micrograph showing a pFET)

537. As the above presentation demonstrates, epitaxial SiGe had been fully integrated with high-κ/RMG technology in Intel's high-volume commercial 45 nm products, and that was common knowledge in the industry well before the application for the '686 Patent was filed. *See generally* Mistry2007; Mistry_Presentation. Given the stark similarity between Intel's 45 nm process above and the process used to make Akasaka's second embodiment (Akasaka ¶¶[0072]-[0088], FIGS. 15-26), there is no question a POSITA would have found it obvious to integrate epitaxial SiGe into Akasaka's second embodiment.

538. Although the commercial adoption of SiGe stressors by Intel demonstrates both motivation to use such technology and a reasonable expectation of success, there is no shortage of other literature explaining why that is. For example, as an alternative to forming pFET source/drain regions solely by ion implantation, Hsu823 teaches to form SiGe stressors 218 in trenches of pFET active regions to induce compressive stress in the pFET channel region. Hsu823 explains that, in one embodiment, "source/drain regions 120 and 220 are formed [only] by implanting impurities into semiconductor substrate 30." Hsu823 ¶[0032]. As an alternative, Hsu823 teaches that SiGe stressors may be used:

> In alternative embodiments, as shown in FIG. 7B, SiGe stressors 218 are formed in PMOS region 200. Preferably, a photo resist 121 is formed covering NMOS region 100. Recesses are formed in substrate 30 along the outside edges of the spacers 216, preferably by etching. SiGe stressors 218 are then formed in the recesses. In the

> preferred embodiment, SiGe stressors 218 are epitaxially grown. P-type impurities such as boron are preferably doped during the epitaxial growth. The photo resist 121 is then removed. After being annealed, SiGe stressors 218 will try to restore their lattice spacing, which is greater than the lattice spacing of the substrate 30. This introduces compressive stresses in the respective channel regions of the resulting PMOS devices, and the device drive currents of the respective PMOS devices are increased.

Hsu823 ¶[0033]. Hsu823's FIGS. 7A and 7B show this below.

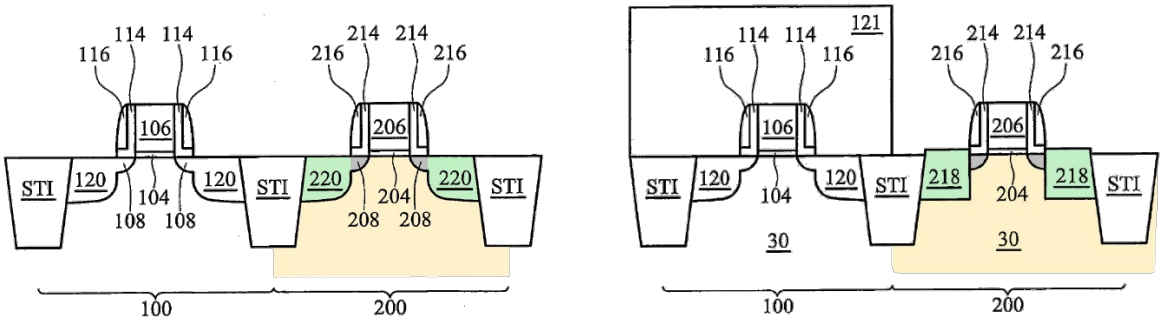


FIG. 7A FIG. 7B

Hsu823's FIGS. 7A and 7B (annotated)

539. A POSITA would have found it obvious to modify Akasaka's FIG. 26 pFET by using epitaxial SiGe stressors, as Hsu823 discloses (and as Intel's public disclosures confirm), to form Akasaka's pFET source/drain regions 309.

540. A POSITA would have been motivated to do so because SiGe stressors were known to increase hole mobility, thereby boosting drive current and operating speed. *See* Section VI.D above. As Hsu823 explains, SiGe stressors "introduce[] compressive stress[] in the . . . channel region[]" such that the "device drive current[] of the . . . PMOS device[] [is] increased." Hsu823 ¶[0033]. Again, this was already

standard industry practice when the application for the '686 Patent was filed, as Hsu823 further confirms:

> Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design. Research has revealed that . . . a compressive stress parallel to the channel length direction can improve PMOS device performance.

Hsu823 ¶¶[0002]-[0003].

541. A POSITA would have reasonably expected to succeed in implementing Hsu823's SiGe stressors in Akasaka's FIG. 26 semiconductor device because such SiGe crystal layers were known and widely used to induce compressive stress in pFETs. *See* Section VI.D above. The structure in Akasaka's FIG. 16 is materially the same as the structure in Hsu823's FIG. 7A. *Compare* Akasaka ¶¶[0072]-[0073], FIG. 16, *with* Hsu823 ¶¶[0028]-[0032], FIG. 7A. As I explain above, Hsu823 teaches (and the Intel disclosures confirm) that SiGe source/drain regions may be readily integrated into such a structure to boost PMOS performance. Hsu823 ¶[0033]; *see also* Mistry_Presentation, 14-19. Thus, as Figure F shows below, a POSITA would have known the same process steps Hsu823 describes regarding Figure 7B readily integrate into Akasaka's process at FIG. 16 with the

ordinary and expected result: SiGe stressors to boost pFET performance. Hsu823 ¶[0033]; *see also* Section VI.D above.

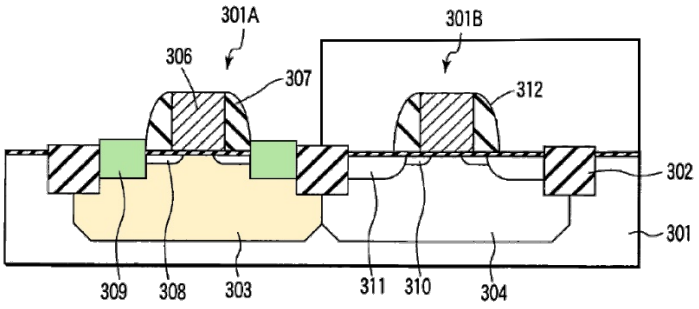


Figure F
(Akasaka's FIG. 16, modified and annotated)

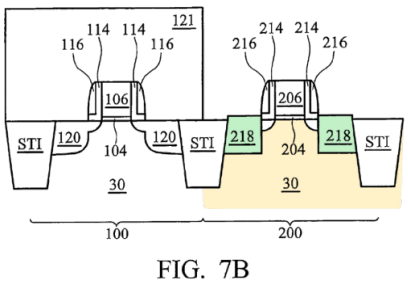


FIG. 7B

Hsu823's FIG. 7B
(annotated)

542. Figure G below illustrates Akasaka's semiconductor device, modified to include SiGe stressors as Hsu823 discloses. Hsu823 ¶[0033], FIG. 7B; Akasaka, FIG. 26; Hsu660, 6:27-31, FIGS. 3-10 (illustrating a similar implementation of SiGe stressors in an RMG device); Mistry2007, Fig. 6 (same).

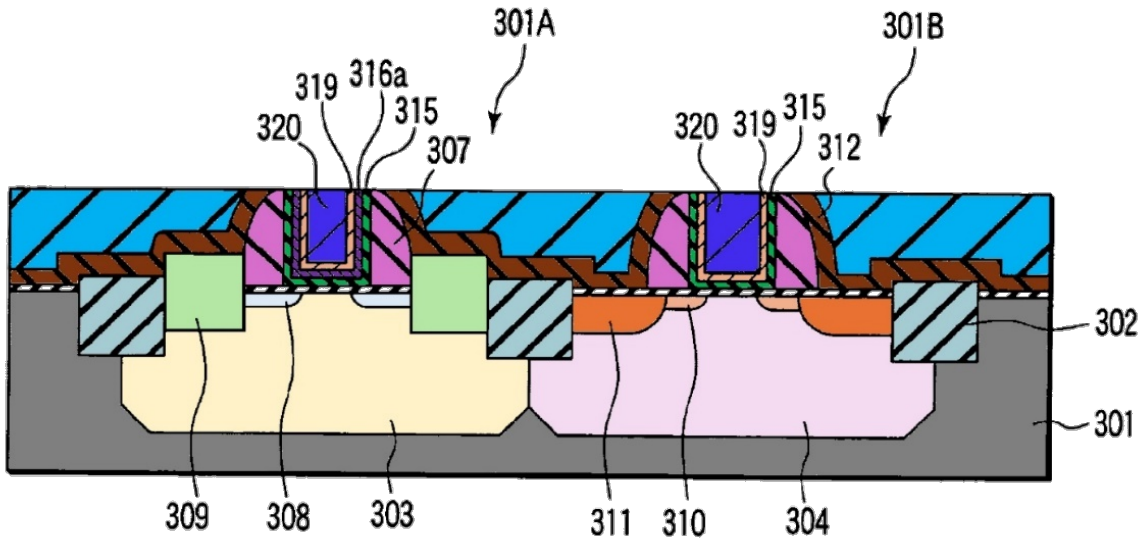


Figure G (Akasaka's FIG. 26, modified and annotated)

2. Independent Claim 1

a. [1Pre]-[1A], [1C]-[1J], and [1L]-[1M]

543. Feature [1Pre] recites "[a] semiconductor device." Akasaka discloses this feature for the same reasons I provide for feature [19Pre], which also recites "[a] semiconductor device." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19Pre] applies to feature [1Pre].

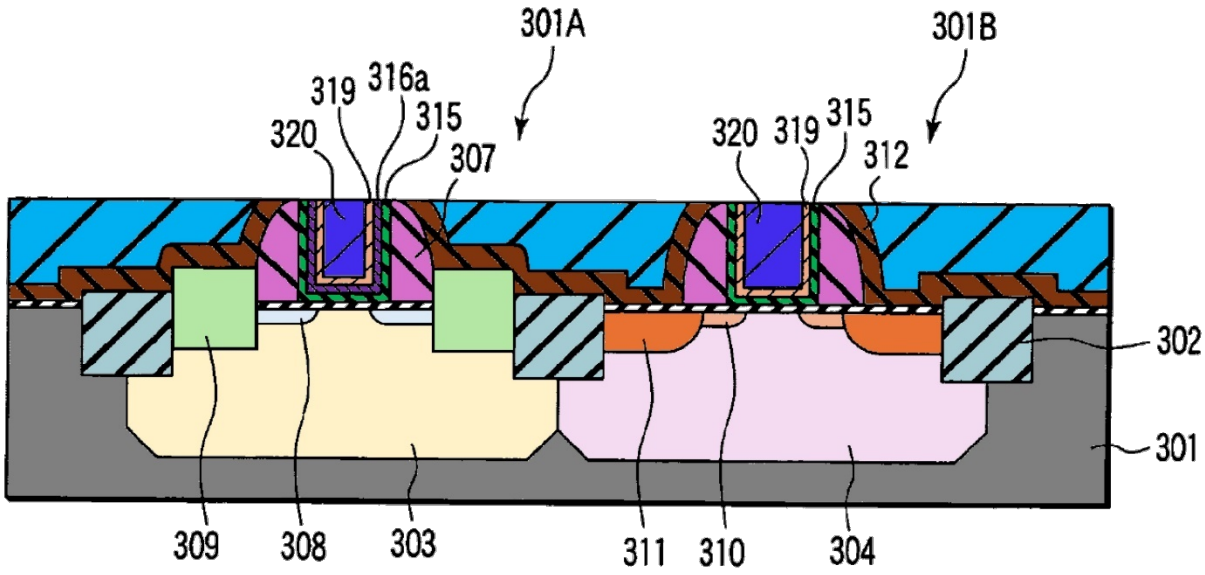


Figure G

544. Feature [1A] recites "a first MIS transistor." Akasaka discloses this feature for the same reasons I provide for feature [19A], which also recites "a first MIS transistor." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19A] applies to feature [1A].

545. Feature [1C] recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and

including a first high-k film made of oxide containing hafnium and silicon." Akasaka discloses this feature for the same reasons I provide for feature [19C], which also recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19C] applies to feature [1C].

546. Feature [1D] recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Akasaka discloses this feature for the same reasons I provide for feature [19D], which also recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19D] applies to feature [1D].

547. Feature [1E] recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Akasaka discloses this feature for the same reasons I provide for feature [19E], which also recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19E] applies to feature [1E].

548. Feature [1F] recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Akasaka discloses this feature for the same reasons I provide for feature [19F], which also recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19F] applies to feature [1F].

549. Feature [1G] recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon." Akasaka discloses this feature for the same reasons I provide for feature [19G], which also recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19G] applies to feature [1G].

550. Feature [1H] recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Akasaka discloses this feature for the same reasons I provide for feature [19H], which also recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19H] applies to feature [1H].

551. Feature [1I] recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Akasaka discloses this feature for the same reasons I provide for feature [19I], which also recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19I] applies to feature [1I].

552. Feature [1J] recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Akasaka

discloses this feature for the same reasons I provide for feature [19J], which also recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19J] applies to feature [1J].

553. Feature [1L] recites "the first and second metal films are made of different metal materials." Akasaka discloses this feature for the same reasons I provide for feature [19K], which also recites "the first and second metal films are made of different metal materials." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19K] applies to feature [1L].

554. Feature [1M] recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Akasaka discloses this feature for the same reasons I provide for feature [19L], which also recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Combining Hsu823 with Akasaka does not materially affect how my analysis for feature [19L] applies to feature [1M].

b. [1B]: "a second MIS transistor"

555. The Akasaka-Hsu823 combination includes "a second MIS transistor."

556. As Figure G shows below, the Akasaka-Hsu823 combination includes a pFET in area 301A, which is a modified version of Akasaka's pFET that incorporates epitaxial SiGe stressors as Hsu823 discloses. *See* Section IX.G.1 above; Akasaka ¶[0073], FIG. 26; Hsu823 ¶¶[0032]-[0033], FIGS. 7A-7B.

557. Akasaka's pFET, as modified to include SiGe source/drain stressors as in Hsu823, includes features [1G]-[1J] for the reasons I explain regarding [19G]-[19J], respectively.

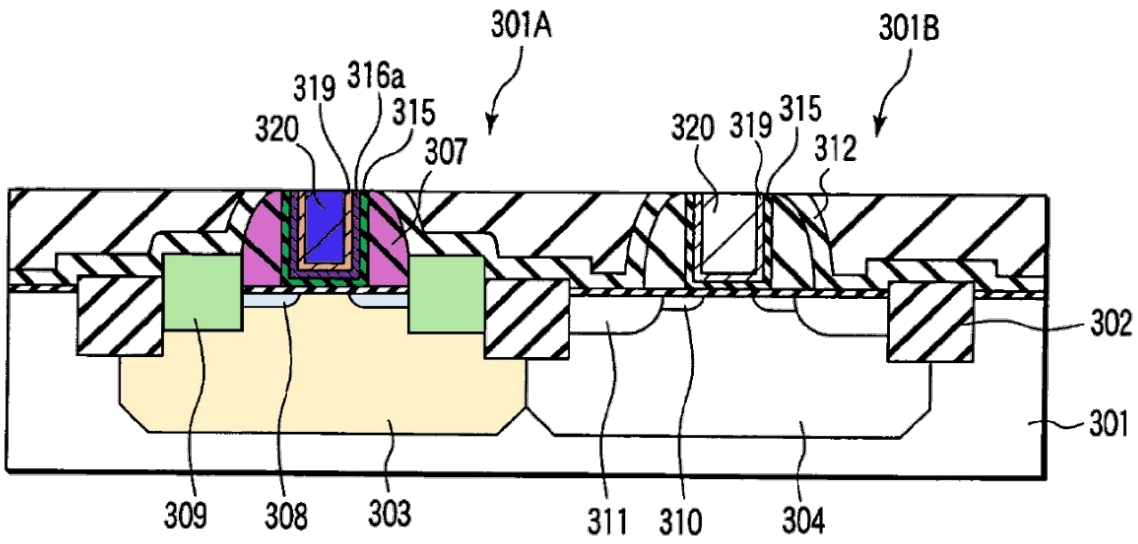


Figure G

c. [1K]: "the second MIS transistor includes: . . . source/drain regions formed in the second active region laterally outside the second sidewall spacers"

558. Akasaka and Hsu823 disclose "the second MIS transistor includes: . . . source/drain regions formed in the second active region laterally outside the second sidewall spacers."

559. Akasaka's semiconductor device, before being modified to incorporate SiGe stressors as Hsu823 describes, includes an "n-type well 303" in which ion-implanted "source/drain layers 309" and source/drain "extensions 308" are formed. *See* Akasaka ¶¶[0072]-[0073], FIG. 26.

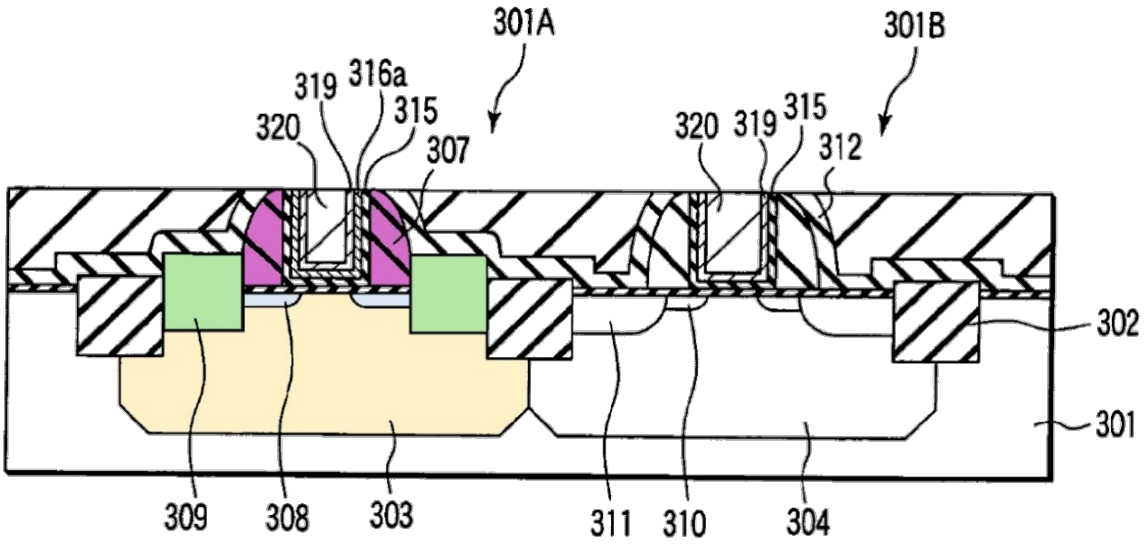


Figure G

560. As I explain in Section IX.G.1, a POSITA would have found it obvious to replace Akasaka's ion-implanted pFET source/drain regions 309 with epitaxial SiGe stressors, as Hsu823 teaches. Figure G above shows the resulting Akasaka-Hsu823 combination. It includes epitaxial SiGe source/drain regions 309 (green) formed in the active region of Akasaka's pFET laterally outside the sidewall spacers 307 (purple).

d. [1N]: "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region"

561. In the Akasaka-Hsu823 combination, "the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region."

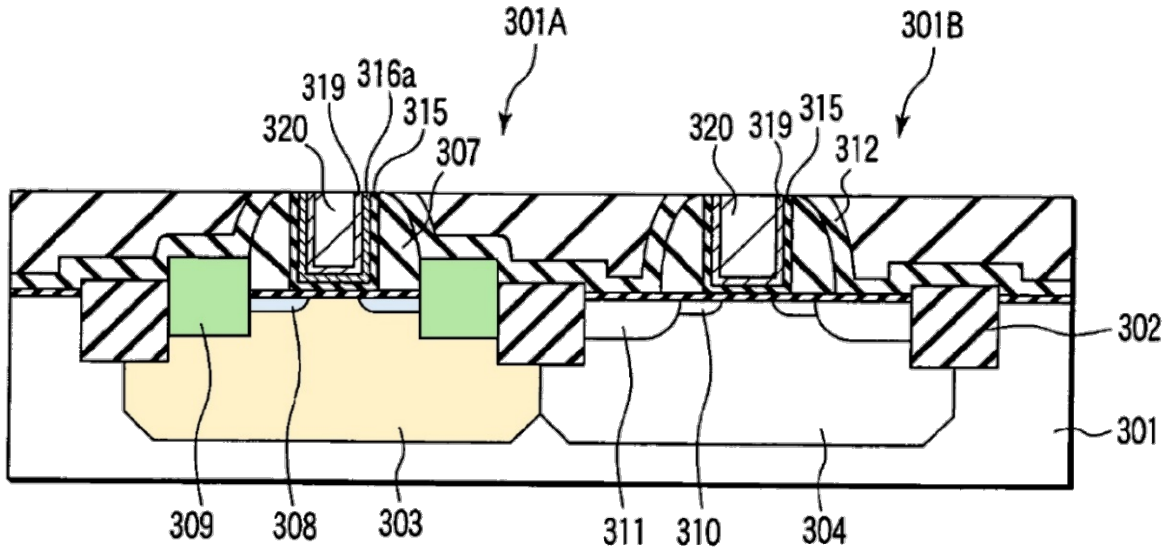


Figure G

562. As I explain in Section IX.G.1, a POSITA would have found it obvious to replace Akasaka's ion-implanted pFET source/drain regions 309 with epitaxial SiGe stressors, as Hsu823 teaches. Figure G above shows the resulting Akasaka-Hsu823 combination.

563. As Hsu823 explains, a POSITA would have recognized that such SiGe stressors (shown in green above) are "a silicon mixed crystal layer which is formed in trenches provided in" the pFET active region, as claimed, because they comprise silicon and germanium atoms that are "epitaxially grown" (i.e., a mixed crystal of Si and Ge grown) in "[r]ecesses [that] are formed . . . along the outside edges of the spacers" (i.e., in trenches of the pFET region). Hsu823 ¶[0033]. As Hsu823 further explains, a POSITA also would have recognized that such SiGe stressors "cause[] . . . stress in a gate length direction of a channel region in the . . . active region" of the pFET because they "introduce[] compressive stress[] in the . . . channel region[] of the resulting PMOS device[]." Hsu823 ¶[0033]; *see also* '686 Patent, 6:60-61 ("The silicon mixed crystal layer is preferably made of a SiGe layer."), 13:33-50 (similar), 19:62-20:20 (similar), claim 10 (similar). As I explain in Section VI.D, that is the fundamental purpose for which SiGe stressors were developed and why they were so rapidly adopted in the semiconductor industry.

e. [1O]: "the silicon nitride film has a thickness smaller than that of the first gate electrode."

564. In the Akasaka-Hsu823 combination, it would have been obvious that "the silicon nitride film has a thickness smaller than that of the first gate electrode" for the reasons I provide for claim 22 in Ground 2B (Section IX.F.4). Combining Hsu823 with Akasaka does not materially affect my analysis of Akasaka regarding claim 22 in the context of feature [1O].

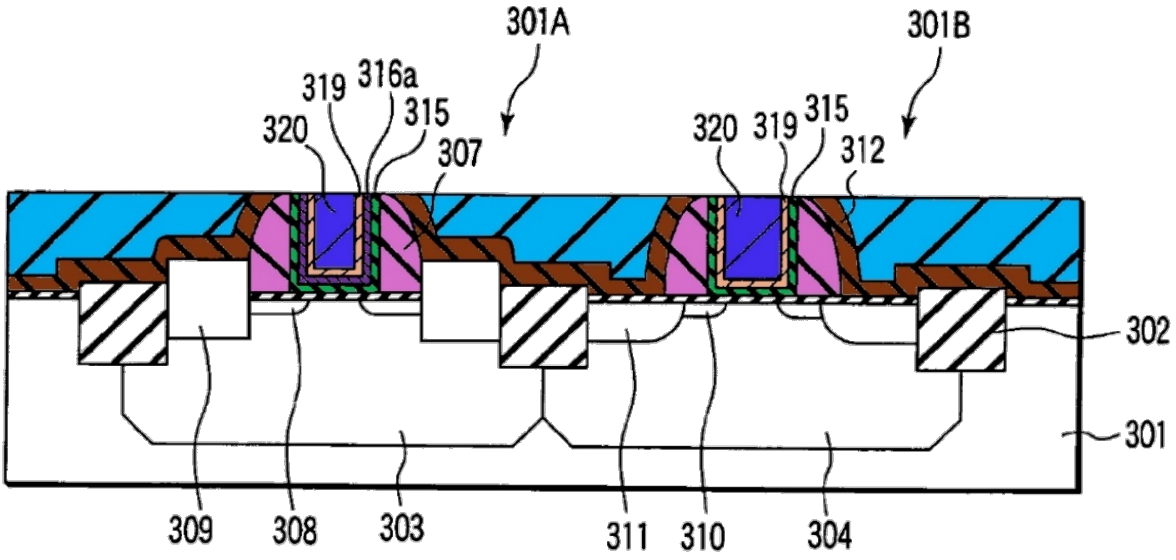


Figure G

3. Independent Claim 25

565. For purposes of claim 25, the Akasaka-Hsu823 combination may optionally include SiGe source/drain stressors, as I describe in Section IX.G.1 above, or it may optionally omit them. Either way, it is my opinion that a POSITA would have found claim 25 obvious in view of the Akasaka-Hsu823 combination.

a. [25Pre]-[25L]

566. Feature [25Pre] recites "[a] semiconductor device." Akasaka discloses this feature for the same reasons I provide for feature [19Pre], which also recites "[a] semiconductor device." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1Pre]) above.

567. Feature [25A] recites "a first MIS transistor." Akasaka discloses this feature for the same reasons I provide for feature [19A], which also recites "a first MIS transistor." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1A]) above.

568. Feature [25B] recites "a second MIS transistor." Akasaka discloses this feature for the same reasons I provide for feature [19B], which also recites "a second MIS transistor." If SiGe source/drain stressors are present, the Akasaka-Hsu823 combination also includes this feature for the reasons I provide above for feature [1B], which also recites "a second MIS transistor." *See* Section IX.G.2.b ([1B]) above.

569. Feature [25C] recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate." Akasaka discloses this feature for the same reasons I provide for feature [19C], which also recites "the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1C]) above.

570. Feature [25D] recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." Akasaka discloses this feature for the same reasons I provide for feature [19D],

which also recites "the first MIS transistor includes: . . . a first gate electrode including a second metal film formed on the first gate insulating film." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1D]) above.

571. Feature [25E] recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." Akasaka discloses this feature for the same reasons I provide for feature [19E], which also recites "the first MIS transistor includes: . . . first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1E]) above.

572. Feature [25F] recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers." Akasaka discloses this feature for the same reasons I provide for feature [19F], which also recites "the first MIS transistor includes: . . . a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the

first sidewall spacers." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1F]) above.

573. Feature [25G] recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate." Akasaka discloses this feature for the same reasons I provide for feature [19G], which also recites "the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1G]) above.

574. Feature [25H] recites "the second MIS transistor includes: . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." Akasaka discloses this feature for the same reasons I provide for feature [19H], which also recites "the second MIS transistor includes . . . a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1H]) above.

575. Feature [25I] recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." Akasaka discloses this feature for the same

reasons I provide for feature [19I], which also recites "the second MIS transistor includes: . . . second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1I]) above.

576. Feature [25J] recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." Akasaka discloses this feature for the same reasons I provide for feature [19J], which also recites "the second MIS transistor includes: . . . the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1J]) above.

577. Feature [25K] recites "the first and second metal films are made of different metal materials." Akasaka discloses this feature for the same reasons I provide for feature [19K], which also recites "the first and second metal films are made of different metal materials." This remains true whether or not SiGe

source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1L]) above.

578. Feature [25L] recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." Akasaka discloses this feature for the same reasons I provide for feature [19L], which also recites "the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes." This remains true whether or not SiGe source/drain stressors are present in the Akasaka-Hsu823 combination. *See* Section IX.G.2.a ([1M]) above.

b. [25M]: "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region."

579. In the Akasaka-Hsu823 combination, "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region."

580. As I explain regarding feature [19F], Akasaka's silicon nitride film 312 discloses the claimed "silicon nitride film." A POSITA would have found it obvious to implement Akasaka's silicon nitride film 312 as a tensile etch stop layer to "cause[] . . . stress in a gate length direction of a channel region in" Akasaka's nFET.

581. Akasaka explains that "silicon nitride film 312 serv[es] as an etching stopper." Akasaka ¶[0073]. Hsu823 discloses a similar CESL 34 made of silicon nitride and formed in a manner that causes tensile stress in a gate length direction of

a channel region in the active region of the nFET device. Hsu823 explains why doing so would have been beneficial:

> With circuits becoming smaller and faster, improvement in device driving current is becoming more important, which can be increased by improving carrier mobility. Among efforts made to enhance carrier mobility, forming a stressed channel region is a known practice. The performance of a MOS device can be enhanced through a stressed-surface channel. This technique allows performance to be improved at a constant gate length without adding complexity to circuit fabrication or design.
>
> Research has revealed that a bi-axial, in-plane tensile stress field can improve NMOS performance, and a compressive stress parallel to the channel length direction can improve PMOS device performance. A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.

Hsu823 ¶¶[0002]-[0003]; *see also* Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device. The stressed CESLs introduce stress into the channel region. Therefore, the carrier mobility is improved.").

582. As one example, a POSITA would have been motivated to implement Akasaka's silicon nitride film 312 as a tensile layer covering both pFET and nFET devices, which was well known in the art to improve electron mobility in the nFET channel regions. *See* Section VI.D above. Morin, for instance, explains that "in low

cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL." Morin, 356; *see also* Murthy151 ¶[0005] ("For n-MOS devices, carrier mobility (i.e. electron mobility) is enhanced by generating a tensile strain in the transistor's channel region."); Hsu823 ¶[0039] (teaching the option of applying a tensile CESL over both pFET and nFET devices because "the performance of PMOS devices can be easily improved . . . , while the performance of NMOS devices is relatively difficult to improve"); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c).

583. If SiGe source/drain stressors are present, as they optionally are in the asserted combination for claim 25, Bohr683 explains that a net compressive stress still obtains in the pFET channel region when a tensile CESL is formed over both pFET and nFET devices to apply tensile stress to the nFET channel region. Bohr683's FIG. 6 illustrates this below. Bohr683 ¶¶[0038]-[0039], FIG. 6; *see also* Hsu823 ¶[0039] (teaching the option of applying a tensile CESL over both pFET and nFET devices because "the performance of PMOS devices can be easily

improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 356 ("[I]t is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL."); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c).

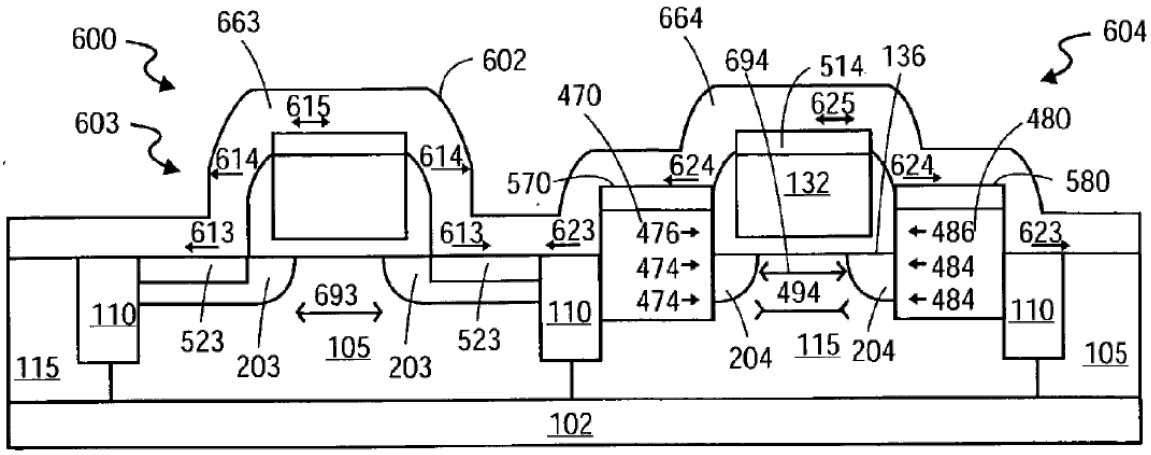


FIG. 6

Bohr683's FIG. 6

584. A POSITA would have reasonably expected to succeed at implementing Akasaka's silicon nitride film 312 as a tensile layer because such tensile CESLs were widely used to improve carrier mobility in nFETs. *See*

Section VI.D above. Moreover, it would have been well within a POSITA's ability to create a tensile silicon nitride CESL film. For example, Jung explains that "a stress-tuned silicon nitride film can be deposited . . . to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure." Jung ¶[0090]. Jung also describes exemplary recipes for forming a tensile CESL for this purpose. *See* Jung ¶[0099]-[0100] ("Table V shows the deposition conditions for silicon nitride films which were deposited under conditions which provided tensile stress films."), Tbl. V. Accordingly, a POSITA would have reasonably expected to succeed at implementing Akasaka's silicon nitride film 312 as a tensile layer, as such layers were ubiquitous in the industry by the time the application for the '686 Patent was filed. This remains true whether or not SiGe source/drain stressors are present.

4. Claims 2 and 26

585. Claim 2 depends from claim 1. I understand that means claim 2 requires all the same features as claim 1, plus the additional features recited in claim 2. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

586. Claim 26 depends from claim 25. I understand that means claim 26 requires all the same features as claim 25, plus the additional features recited in claim

26. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

587. Akasaka further discloses "wherein the first metal film has a thickness smaller than that of the second metal film" for the same reasons I provide in Section IX.F.2 regarding claim 20. Combining Hsu823 with Akasaka does not change Akasaka's structure as it relates to claim 20.

5. Claims 3 and 27

588. Claim 3 depends from claim 1. I understand that means claim 3 requires all the same features as claim 1, plus the additional features recited in claim 3. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

589. Claim 27 depends from claim 25. I understand that means claim 27 requires all the same features as claim 25, plus the additional features recited in claim 27. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

590. Akasaka further discloses "wherein the first and second metal films have different work functions" for the same reasons I provide in Section IX.F.3 regarding claim 21. Combining Hsu823 with Akasaka does not change Akasaka's structure as it relates to claim 21.

6. Claims 4 and 29

591. Claim 4 depends from claim 1. I understand that means claim 4 requires all the same features as claim 1, plus the additional features recited in claim 4. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

592. Claim 29 depends from claim 25. I understand that means claim 29 requires all the same features as claim 25, plus the additional features recited in claim 29. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

593. Further, in the Akasaka-Hsu823 combination, "the conductive film is made of the second metal film."

594. As I explain for feature [19D], either or both of Akasaka's conductive films 319 and 320 in nFET area 301B disclose the claimed "second metal film."

595. As I explain for feature [19H], either or both of Akasaka's conductive films 319 and 320 in pFET area 301A disclose the claimed "conductive film."

596. When Akasaka's conductive film 319 is mapped both to the claimed "second metal film" and to the claimed "conductive film," Akasaka discloses "the conductive film is made of the second metal film," as claimed, because conductive film 319 in the nFET region provides the "second metal film," and conductive film 319 in the pFET region provides the "conductive film."

597. When Akasaka's conductive film 320 is mapped both to the claimed "second metal film" and to the claimed "conductive film," Akasaka discloses "the conductive film is made of the second metal film," as claimed, because conductive film 320 in the nFET region provides the "second metal film," and conductive film 320 in the pFET region provides the "conductive film."

598. When Akasaka's conductive films 319 and 320, taken together, are mapped both to the claimed "second metal film" and to the claimed "conductive film," Akasaka discloses "the conductive film is made of the second metal film," as claimed, because conductive films 319 and 320 in the nFET region provide the "second metal film," and conductive films 319 and 320 in the pFET region provide the "conductive film."

599. Regardless of which mapping above is applied, the same physical layer (or layers) is used to form both the "second metal film" and the "conductive film." Accordingly, "the conductive film is made of the second metal film," as claimed. Combining Hsu823 with Akasaka does not change Akasaka's structure as it relates to conductive films 319 and/or 320 in that regard.

7. Claims 6 and 31

600. Claim 6 depends from claim 1. I understand that means claim 6 requires all the same features as claim 1, plus the additional features recited in claim 6. The

Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

601. Claim 31 depends from claim 25. I understand that means claim 31 requires all the same features as claim 25, plus the additional features recited in claim 31. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

602. Further, in the Akasaka-Hsu823 combination, "the first and second gate insulating films are made of the same insulating material."

603. Akasaka's gate dielectric film 315 "is depos[it]ed all over the substrate" at once using the same insulating material ($HfSi_xO_y$) for both nFET and pFET devices. *See* Akasaka ¶¶[0074]-[0075], FIG. 19. As I explain for features [19C] and [19G], Akasaka's gate dielectric film 315 discloses each of the claimed "first and second gate insulating films." The first gate insulating film is disclosed by Akasaka's gate dielectric film 315 in nFET area 301B, and the second gate insulating film is disclosed by Akasaka's gate dielectric film 315 in pFET area 301A. Akasaka's gate dielectric film 315 is formed of hafnium silicon oxide ($HfSi_xO_y$), which is "a gate dielectric (insulating) film 315." Akasaka ¶[0075]. In fact, hafnium silicon oxide is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicate (HfSiO) . . . ." '686 Patent, 29:16-24.

604. Because Akasaka's gate dielectric film 315 is used to form both the claimed "first gate insulating film" and the claimed "second gate insulating film," Akasaka discloses "the first and second gate insulating films are made of the same insulating material," as claimed. Combining Hsu823 with Akasaka does not change Akasaka's structure as it relates to gate dielectric film 315 in that regard.

8. Claims 7, 23, and 33

605. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

606. Claim 23 depends from claim 19. I understand that means claim 23 requires all the same features as claim 19, plus the additional features recited in claim 23. The Akasaka-Hsu823 combination contains all the features recited in claim 19 for the reasons I provide in Section IX.F.1 above.

607. Claim 33 depends from claim 25. I understand that means claim 33 requires all the same features as claim 25, plus the additional features recited in claim 33. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

608. For the reasons below, a POSITA would have found it further obvious in the Akasaka-Hsu823 combination that "each of the first sidewall spacers is made

of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape."

a. A POSITA would have found it obvious to implement Hsu823's L-shaped sidewalls

609. The Akasaka-Hsu823 combination includes Akasaka's gate sidewalls 307 formed of silicon nitride, as Figure G shows below (showing Akasaka's pFET source/drain regions as epitaxial SiGe layers). Akasaka ¶[0073].

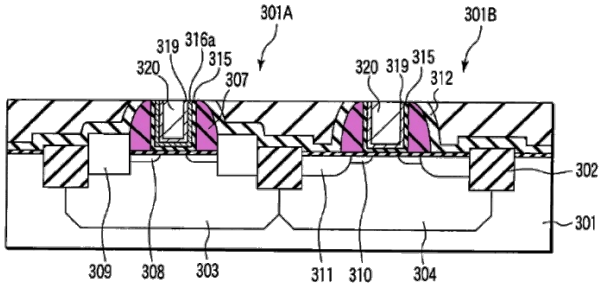


Figure G

610. Hsu823 similarly discloses forming silicon nitride sidewall spacers 116 and 216, as Hsu823's FIG. 7B shows below. Hsu823 ¶[0031], ¶[0035].

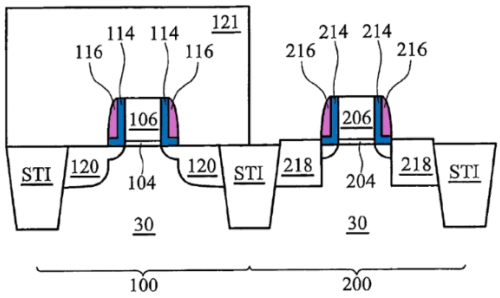


FIG. 7B

Hsu823's FIG. 7B (annotated)

252

611. In addition, Hsu823 discloses L-shaped spacer liners 114 and 214, which are formed before spacers 116 and 216, as FIG. 7B shows above. Hsu823's spacers and spacer liners, like Akasaka's gate sidewalls 307, define the location of the deep source/drain regions (whether ion-implanted or epitaxial SiGe). Hsu823 ¶¶[0032]-[0033], FIGS. 6, 7A, 7B; Akasaka ¶[0058], FIGS. 11-12.

612. As Hsu823's FIGS. 9 and 10 illustrate below, Hsu823 teaches to remove spacers 116 and 216—but not L-shaped spacer liners 114 and 214—before forming CESL 34. Hsu823 ¶¶[0035]-[0036]. Although Hsu823's FIG. 10 illustrates a "dielectric layer 32" formed prior to the contact etch stop layer 34, dielectric layer 32 is "optionally formed" and may be omitted. Hsu823 ¶[0036]. For purposes of this declaration, optional dielectric layer 32 is not present—an option a POSITA would have exercised so that CESL 34 is closer to the nFET channel region to improve stress transfer from the CESL to the channel regions. *See* Hsu823 ¶[0015]; Liu, 1-2, Tbls. I-II, Figs. 1-7.

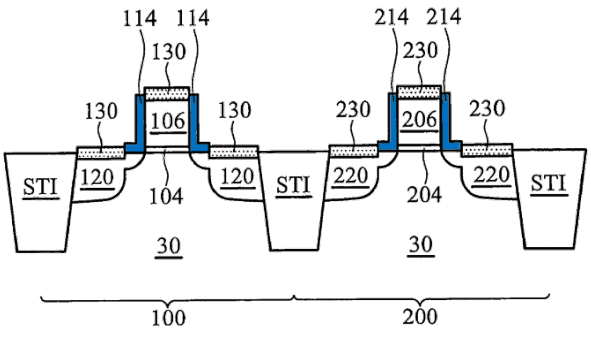


FIG. 9

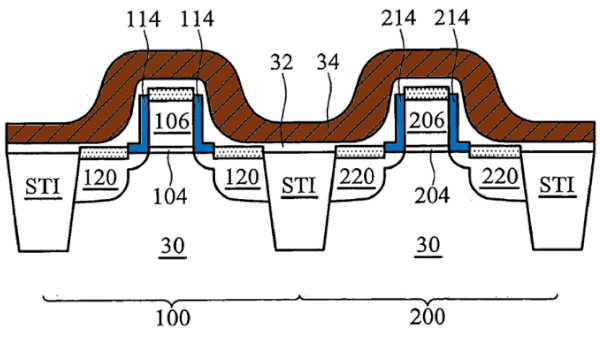


FIG. 10

Hsu823's FIGS. 9 and 10 (annotated)

613. More specifically, Hsu823 teaches to remove spacers 116 and 216 just before forming CESL 34 by applying a selective etchant, such as phosphoric acid (H_3PO_4) (a common etchant used to preferentially remove silicon nitride over silicon oxide):

> Referring to FIG. 9, spacers 116 and 216 are removed. Both wet and dry etchings can be used. The removal is preferably performed using an etchant that attacks the spacers 116 and 216, but not the spacer liners 114 and 214 and silicides 130 and 230. In the preferred embodiment wherein the spacers 116 and 216 are formed of silicon nitride and spacer liners 114 and 214 are formed of silicon oxide, . . . H_3PO_4 can be used to remove spacers 116 and 216. Referring to FIG. 10, a dielectric layer 32 is optionally formed. A contact etch stop layer (CESL) 34 is then formed.

Hsu823 ¶¶[0035]-[0036].

614. Hsu823 recommends using L-shaped spacer liners 114 and 214 and removing spacers 116 and 216 because it reduces the aspect ratio of the gap between neighboring FETs. Hsu823 explains: "With the scaling of integrated circuits, . . . the distance between devices decreases" and "subsequently performed gap-filling and contact etch processes suffer problems accordingly." Hsu823 ¶[0004] (referring to FIG. 1 and discussing "difficulty in subsequent processes," and "problems, such as short circuits," that occur due to voiding). By removing the spacers 116 and 216, Hsu823 teaches that the aspect ratio of the space between FETs becomes smaller, as FIGS. 15A and 15B show below.

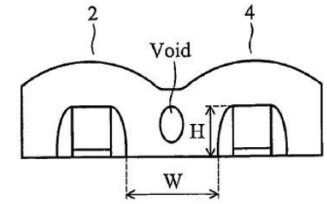
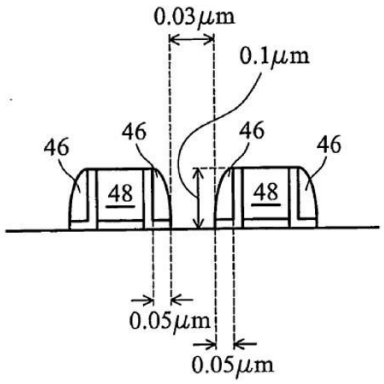


FIG. 1 (PRIOR ART)



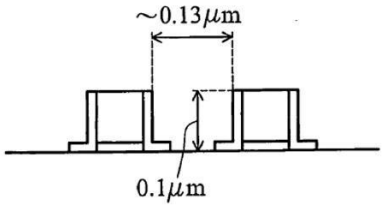


FIG. 15B

FIG. 15A

Hsu823's FIGS. 1, 15A, 15B

615. More specifically, Hsu823 explains:

> An example is shown in FIGS. 15A and 15B to explain the improvement of the aspect ratio. Referring to FIG. 15A, assuming the spacers have a thickness of 0.05 μm, and the spacing between spacers is 0.03 μm, and further assuming the height of the gates is 0.1 μm, the aspect ratio is 0.1/0.03, which is about 3.3. By removing spacers (refer to FIG. 15B), the spacing is increased to close to 0.13 μm, and the aspect ratio is reduced to 0.8. . . . By reducing the aspect ratio, gap-filling is improved and the contact etching process can be better controlled. Additionally, thicker CESLs can be applied without causing difficulty in subsequent processes, so that the performance of devices is improved.

Hsu823 ¶¶[0042]-[0043]. Hsu823 further explains: "With the spacers removed, the aspect ratio of the gap between neighboring MOS devices is reduced. Thus, the stresses applied by the CESL can be better applied to the channel regions of the respective MOS devices." Hsu823 ¶[0015].

616. Turning back to Akasaka's device structure, a POSITA would have found it obvious to add L-shaped spacer liners like Hsu823's spacer liners 114

and 214, and to remove Akasaka's gate sidewalls 307, leaving only the L-shaped spacer liners. Akasaka's gate sidewalls have just one "D"-shaped sidewall 307, which is the prior-art structure that Hsu823 recognizes as being conducive to void formation. *Compare* Akasaka ¶[0073], FIG. 26, *with* Hsu823 ¶[0004], FIG. 1. In view of that, and as I further explain below, a POSITA would have found it obvious to apply Hsu823's solution to Akasaka. Specifically, a POSITA would have found it obvious to add L-shaped spacer liners made of silicon oxide to Akasaka's silicon nitride gate sidewalls 307 so that Akasaka's gate sidewalls 307 may subsequently be removed (as Hsu823 teaches).

617. Like Hsu823's spacers 116 and 216, Akasaka's gate sidewalls 307 are made of silicon nitride, which means adding Hsu823's L-shaped sidewalls, made of silicon oxide, would readily integrate into Akasaka's FETs. *Compare* Akasaka ¶[0073] ("A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306."), FIG. 16, *with* Hsu823 ¶[0030] ("[S]ub-layer 110 is a liner oxide layer and sub-layer 112 is a nitride layer."), ¶[0031] ("FIG. 6 illustrates the patterning of sub-layer 110 and sub-layer 112. . . . The remaining portions of the sub-layer 110 and sub-layer 112 form spacer liner 114 and spacer 116 in region 100, and spacer liner 214 and spacer 216 in region 200, respectively."), FIGS. 5-6. Figure H below illustrates this modification to the Akasaka-Hsu823 combination.

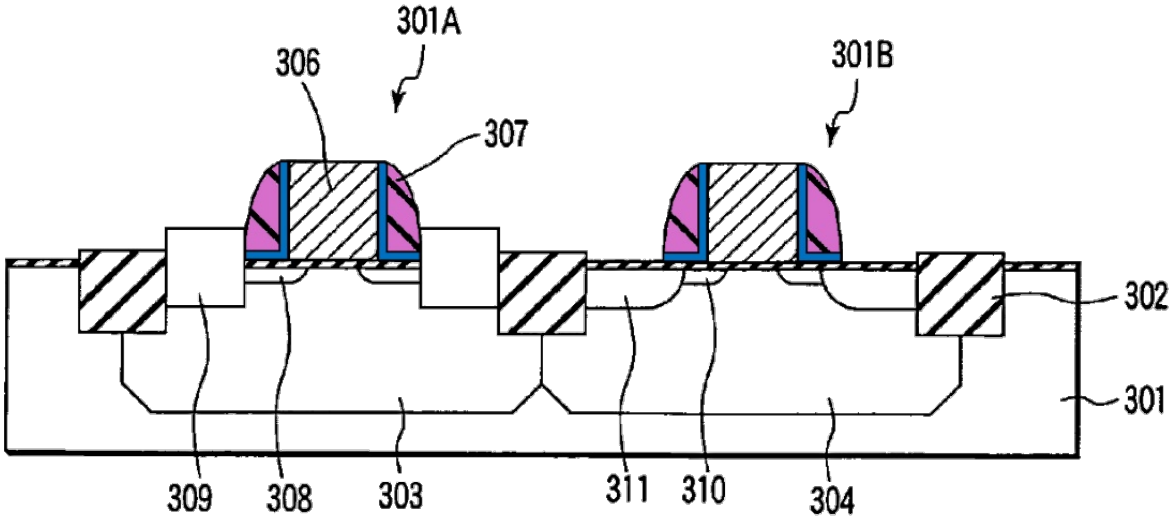


Figure H (Modification of Akasaka's FIG. 16)

618. Before forming Akasaka's silicon nitride film 312, a POSITA would have found it obvious to remove Akasaka's gate sidewalls 307 and to leave the L-shaped spacer liners intact, just as Hsu823 instructs. Hsu823 ¶¶[0035]-[0036], FIGS. 8-10. Hsu823 explains: "The removal is preferably performed using an etchant that attacks the [sidewalls 307], but not the [L-shaped spacer liners]." Hsu823 ¶[0035]. Since Akasaka's sidewalls 307 are (like Hsu823's spacers 116 and 216) made of silicon nitride, "H_3PO_4 can be used to remove [sidewalls 307]" without removing the silicon oxide L-shaped spacer liners underneath. Hsu823 ¶[0035]. Figure I below illustrates this intermediate modification to the Akasaka-Hsu823 combination.

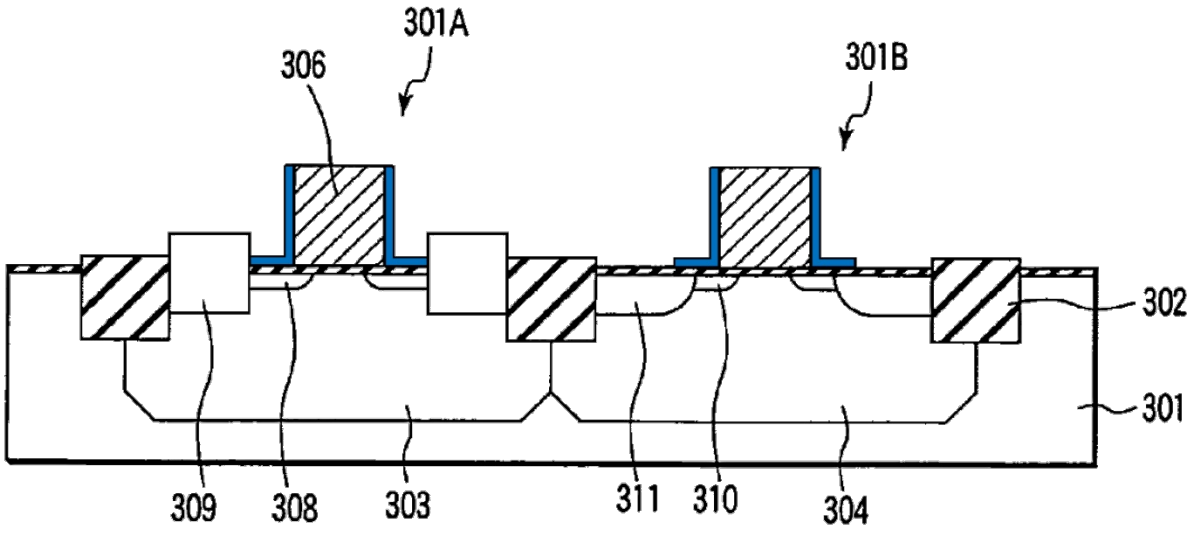


Figure I (Modification of Akasaka's FIG. 16)

619. Finally, a POSITA would have been motivated to continue Akasaka's process by forming silicon nitride film 312 over the L-shaped spacer liners, just as Hsu823 teaches to form CESL 34 over L-shaped spacer liners 114 and 214. *Compare* Akasaka ¶[0073] ("The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper."), *with* Hsu823 ¶[0036] ("A contact etch stop layer (CESL) 34 is then formed. . . . [T]he materials of CESL 34 include commonly used materials such as nitride . . . ."). Figure J below illustrates this modification to the Akasaka-Hsu823 combination when SiGe source/drain stressors are present (e.g., for claim 7 and optionally claim 33).

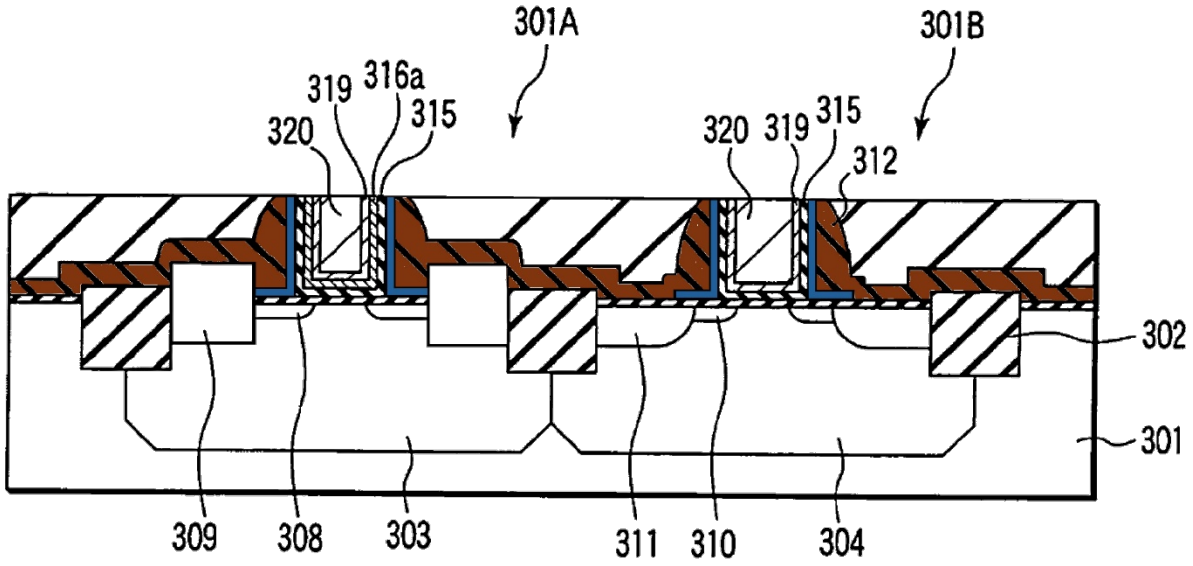


Figure J (Modification of Akasaka's FIG. 26)

620. A POSITA would have been motivated to modify Akasaka in this way to reduce the aspect ratio of the gap between neighboring FETs, thereby minimizing voiding that can cause "difficulty in subsequent processes" and "problems, such as short circuits." Hsu823 ¶[0004]. By the time the application for the '686 Patent was filed, it was well known that removing outer sidewalls but leaving L-shaped sidewalls (as Hsu823 teaches) increases the packing density in an integrated circuit, making it easier to fill gaps and preventing contact-to-gate shorts. Similar to Hsu823, Yeh explains:

> [T]he residual oxide layer 18 is removed by etching. The L-shaped portion of the nitride material layer 14 is not covered and it can be used as a portion of the L-shaped spacer of the gate structure 16. In accordance with the present invention, the design of the L-shaped spacer 14 of the gate structure 16 can benefit from increased packaging

> density because it causes easier gap filling and prevents contact-to-gate shorts.

Yeh ¶[0018]; *see also* Yeh, Abstract ("The gate structures having L-shaped spacers benefit from increased packaging density in an integrated circuit, and improve gap filling and prevent contact-to-gate shorts."), ¶[0019] ("[T]he L-shaped spacer 14 can benefit from the filling of the interlayer dielectric 20 so as to improve the packaging density of the integrated circuit.").

621. A POSITA also would have been motivated to remove Aoyama's sidewall spacers 143 as described above to improve stress transfer to the channel. For example, Hsu823 explains that, "[w]ith the spacers removed, the aspect ratio of the gap between neighboring MOS devices is reduced. Thus, the stresses applied by the CESL can be better applied to the channel regions of the respective MOS devices." Hsu823 ¶[0015]. Similarly, Liu explains that channel stress may be improved "by narrowing the nitride spacer width" and teaches to fabricate both nFETs and pFETs "without the nitride spacer to achieve the highest channel stress." Liu, 1; *see also* Liu, 2 ("Although the same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es], the drive current enhancement of USP is still higher by more than 7 %."), Tbls. I-II, Figs. 1-7.

622. A POSITA would have reasonably expected to succeed in modifying Akasaka's semiconductor device by adding L-shaped spacer liners and removing

gate sidewalls 307. Like Hsu823's spacers 116 and 216, Akasaka's gate sidewalls 307 are made of silicon nitride and can be removed selectively over the L-shaped spacer liners, which are made of silicon oxide, by using an etchant like H_3PO_4 that attacks silicon nitride preferentially over silicon oxide. *See* Hsu823 ¶¶[0035]-[0036], FIGS. 8-10.

b. Claim 7

623. In this version of the Akasaka-Hsu823 combination (which I describe in Section IX.G.8.a immediately above), "each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape."

624. As I explain regarding feature [19F], Akasaka's silicon nitride film 312 discloses the claimed "silicon nitride film." Akasaka ¶[0073] ("The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper.").

625. As I explain in Section IX.G.8.a, a POSITA would have found it obvious (as Hsu823 teaches) to add L-shaped spacer liners to Akasaka's FET structures and remove gate sidewalls 307, thereby increasing packing density, reducing void formation, and preventing contact-to-gate shorts. As Figure J

illustrates below, upon doing, so Akasaka's nFET and pFET both include L-shaped sidewall spacers that (like Hsu823's spacer liners 114 and 214) form an "inner sidewall having an L-shaped cross-section," and Akasaka's silicon nitride film 312 would contact surfaces of those sidewall spacers that are bent in an L-shape.

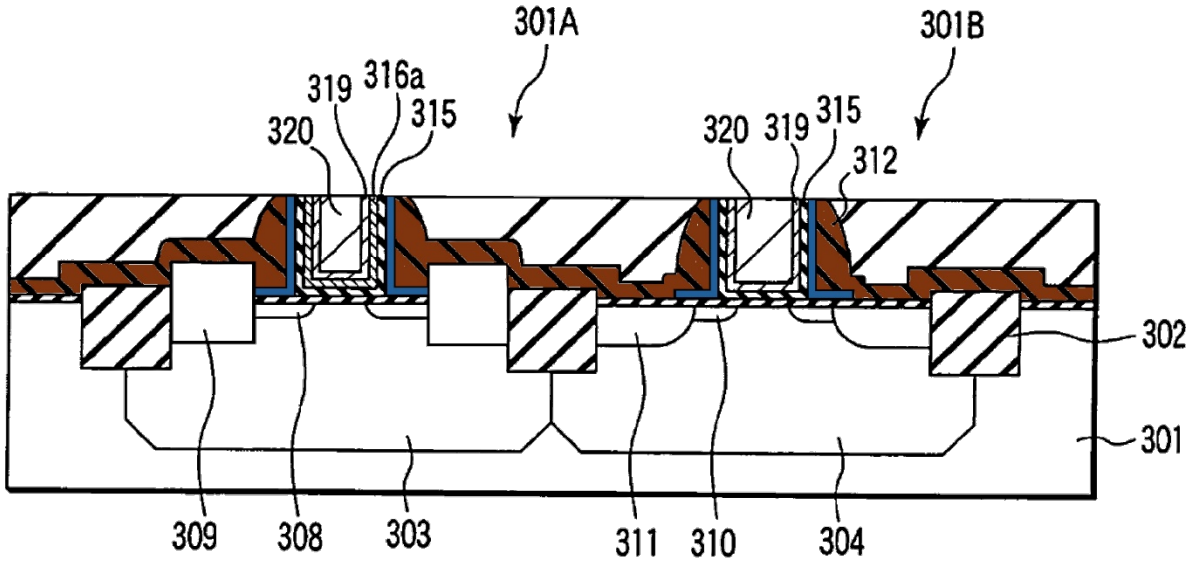


Figure J

c. Claims 23 and 33

626. The features of claims 23 and 33 would have been obvious based on the Akasaka-Hsu823 combination for the same reasons I explain above regarding claim 7.

627. Although optional in the context of claim 33, Hsu823's SiGe source/drain stressors are not required for claims 23 and 33 as they are for claim 7. Without such SiGe source/drain stressors, the Akasaka-Hsu823 combination for claims 23 and 33 would appear as in Figure K below.

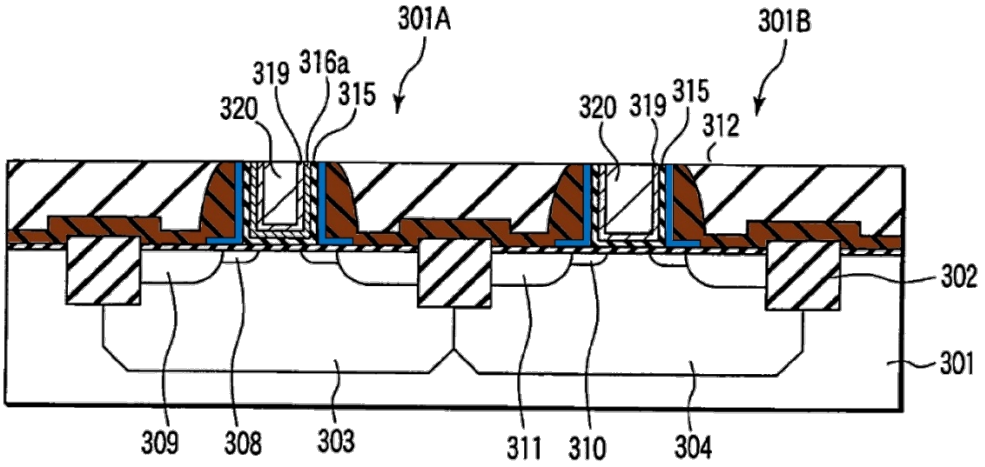


Figure K

628. As Figure K illustrates above, each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section (Hsu823's spacer liners 114 added in nFET region 301B), and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section (Hsu823's spacer liners 214 added in pFET region 301A), and the silicon nitride film (Akasaka's silicon nitride film 312) is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

9. Claim 8

629. Claim 8 depends from claim 1. I understand that means claim 8 requires all the same features as claim 1, plus the additional features recited in claim 8. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

630. Further, in the Akasaka-Hsu823 combination, "the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region" for the same reasons I provide in Section IX.G.3.b for feature [25M]. That is, a POSITA would have found it obvious to implement Akasaka's silicon nitride film 312 as a tensile etch stop layer to "cause[] . . . stress in a gate length direction of a channel region in" Akasaka's nFET. Because claim 8 depends from claim 1, it requires SiGe stressors, which would have been obvious for the reasons I explain in Section IX.G.1. The explanations I provide regarding feature [25M] also apply in the context of claim 8.

631. Although feature [25M] recites "the silicon nitride film causes ***first*** stress in a gate length direction of a channel region in the first active region," whereas claim 8 recites "the silicon nitride film causes ***second*** stress in a gate length direction of a channel region in the first active region" (emphases added), this difference is linguistic only. Independent claim 1 calls the SiGe stress the "first stress," and dependent claim 8 calls the CESL stress the "second stress." Conversely, feature [25M] calls the CESL stress the "first stress." This is a distinction without a difference.

10. Claim 9

632. Claim 9 depends from claim 8. I understand that means claim 9 requires all the same features as claim 8, plus the additional features recited in claim 9. The

Akasaka-Hsu823 combination contains all the features recited in claim 8 for the reasons I provide in Sections IX.G.1, IX.G.2, and IX.G.9 above.

633. Further, in the Akasaka-Hsu823 combination, "the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress."

634. As I explain for claim 8 and for feature [25M], a POSITA would have found it obvious to implement Akasaka's silicon nitride etch stopper film 312 as a tensile etch stop layer. A POSITA would have recognized that, to improve carrier mobility in Akasaka's nFET (the "first MIS transistor"), the silicon nitride etch stopper film 312 should be implemented with tensile stress. *See* Hsu823 ¶[0003] (explaining "bi-axial, in-plane tensile stress field can improve NMOS performance"), ¶[0037] (explaining "tensile stress is applied to the channel region of the resulting NMOS device, so that the NMOS device is improved"), ¶[0038] (explaining "NMOS device . . . prefers a tensile stress"), ¶[0039] (explaining it is preferable to apply tensile CESL across both nFETs and pFETs because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 356 ("[I]n low cost / low power CMOS flow approaches, it is important to work to improve nMOS transistors since other solutions . . . can enhance the pMOS performances. As a result, in these technologies, process induced stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as

CESL."); Liu, 1-2 ("[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow."), Tbls. I-II, Figs. 1-7; Thompson2004, Fig. 5(c). Accordingly, in the Akasaka-Hsu823 combination, the first MIS transistor (Akasaka's nFET) is n-type, and the second stress (applied by Akasaka's silicon nitride film 312) is tensile stress.

11. Claim 10

635. Claim 10 depends from claim 1. I understand that means claim 10 requires all the same features as claim 1, plus the additional features recited in claim 10. The Akasaka-Hsu823 combination contains all the features recited in claim 1 for the reasons I provide in Sections IX.G.1 and IX.G.2 above.

636. Further, in the Akasaka-Hsu823 combination, "the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress."

637. As I explain for feature [1N], a POSITA would have found it obvious to substitute SiGe source/drain stressors (a "silicon mixed crystal layer is made of a SiGe layer") for source/drain diffusion layers 309 in Akasaka's pFET. A POSITA would have understood those SiGe stressors apply compressive stress (the "first stress") to the pFET channel regions. *See* Section IX.G.2.d above. As Hsu823

explains, SiGe stressors "introduce[] compressive stress[] in the respective channel regions of the . . . PMOS device[]," such that the "device drive current[] of the . . . PMOS device[] [is] increased." Hsu823 ¶[0033]; *see also* Hsu823 ¶[0003] (explaining that "a compressive stress parallel to the channel length direction can improve PMOS device performance"), ¶[0037] (explaining that a "PMOS device . . . prefers a compressive stress").

12. Claims 24 and 34

638. Claim 24 depends from claim 19. I understand that means claim 24 requires all the same features as claim 19, plus the additional features recited in claim 24. The Akasaka-Hsu823 combination contains all the features recited in claim 19 for the reasons I provide in Section IX.F.1 above.

639. Claim 34 depends from claim 25. I understand that means claim 34 requires all the same features as claim 25, plus the additional features recited in claim 34. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

640. Further, for the same reasons I provide for features [1K] and [1N] and claim 10, a POSITA would have found it obvious for the Akasaka-Hsu823 combination to include "source/drain regions [SiGe stressors] formed in the second active region [pFET active region] laterally outside the second sidewall spacers [pFET gate sidewalls 307], wherein the source/drain regions include a SiGe layer

which is formed in trenches provided in the second active region." Figure G below illustrates this combination. *See* Sections IX.G.1, IX.G.2.c-d, and IX.G.11 above.

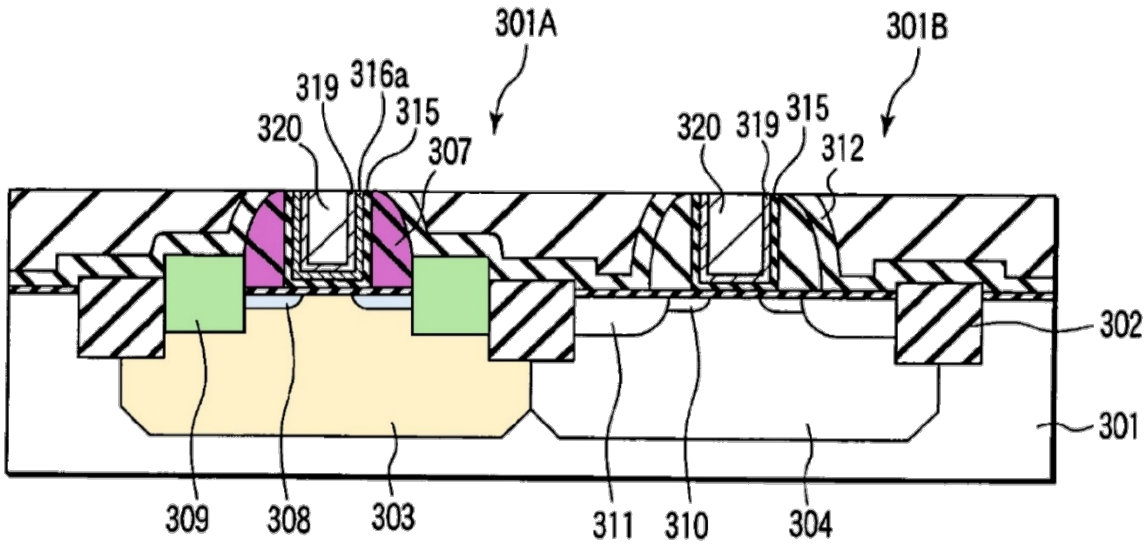


Figure G

13. Claim 28

641. Claim 28 depends from claim 25. I understand that means claim 28 requires all the same features as claim 25, plus the additional features recited in claim 28. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

642. Further, for the same reasons I provide regarding claim 22 in Ground 2B (Section IX.F.4), a POSITA would have found it obvious that "the silicon nitride film has a thickness smaller than that of the first gate electrode" in the Akasaka-Hsu823 combination. Combining Hsu823 with Akasaka does not

materially affect my analysis of Akasaka regarding claim 22 in the context of claim 28.

14. Claim 35

643. Claim 35 depends from claim 25. I understand that means claim 35 requires all the same features as claim 25, plus the additional features recited in claim 35. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

644. Further, in the Akasaka-Hsu823 combination, "the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more."

645. As I explain regarding claim features [19C] and [19G], respectively, Akasaka's gate dielectric film 315 in nFET area 301B discloses the claimed "first gate insulating film," and Akasaka's gate dielectric film 315 in pFET area 301A discloses the claimed "second gate insulating film." *See* Sections IX.F.1.d and IX.F.1.h above.

646. Akasaka's gate dielectric film 315 is formed of hafnium silicon oxide ($HfSi_xO_y$), which a POSITA would have understood to disclose a "high-k film made of a metal oxide having a relative dielectric constant of 10 or more." *See* Akasaka ¶[0075]; Akasaka939 ¶[0004] (listing "hafnium (Hf)-containing material such as . . . $HfSiO_x$" as a "high-k material [with] dielectricity of more than ten (10)"); Baklanov,

xiii ("Dielectrics with values approximately between 10 and 30 are under consideration."); Kavalieros ¶[0002] (explaining that a "high-k dielectric means having a dielectric constant higher than 10"), ¶[0008] (similar). In fact, hafnium silicon oxide is one of the exemplary gate dielectric films that the '686 Patent identifies. It says examples "include hafnium-based oxides such as . . . hafnium silicate (HfSiO) . . . ." '686 Patent, 29:16-24.

H. Ground 2D: The Akasaka-Hsu823-Hobbs Combination Renders Obvious Claim 32

647. Claim 32 depends from claim 25. I understand that means claim 32 requires all the same features as claim 25, plus the additional features recited in claim 32. The Akasaka-Hsu823 combination contains all the features recited in claim 25 for the reasons I provide in Section IX.G.3 above.

648. The Akasaka-Hsu823-Hobbs combination renders obvious the additional features recited in claim 32 for the reasons I explain below.

1. A POSITA would have found it obvious to use different gate insulating films for Akasaka's pFETs and nFETs

649. A POSITA would have found it obvious to use different gate dielectric materials for Akasaka's nFETs and pFETs.

650. It is no coincidence that Hobbs was filed in 1999. As I explain in Section VI.B above, the semiconductor industry recognized around 1999 that high-κ gate dielectrics would replace SiO_2-only gate dielectrics. ITRS_FEP, 2. And for

reasons I explain in Section VI.C, the industry immediately recognized that metal-based gate electrodes would replace polysilicon-only gate electrodes as part of that transition.[17]

651. Hobbs recognizes this as well. Hobbs notes that "[m]etals are an alternative material currently being investigated to replace polysilicon for use as gate electrodes." Hobbs, 1:50-51. According to Hobbs, because metals cannot be doped, the threshold voltages (VTs) of nFET and pFET devices may differ when using a metal gate. For example, when the same metal serves as the gate electrode for both nFET and pFET devices, the threshold voltages will differ unless the gate metal has a work function that lies close to the middle of the silicon bandgap. Such an approach, however, does not yield very good device performance. Hobbs explains:

> [M]erging metal gate technology into complementary MOS (CMOS) designs introduces new process integration and manufacturing issues. For example, current polysilicon gate CMOS processes can use a combination of doped N^+ and P^+ polysilicon in respective NMOS and PMOS devices to overcome problems associated with adjusting channel threshold voltages (VT). Metals, however, are not readily doped. Therefore, when replacing polysilicon with metal, efforts have focused on selecting those metals having work functions that are close to the mid band-gap of silicon. This allows the VT of the respective n-channel and p-channel devices to be

[17] The reason it took from 1999 to 2007 until commercial devices began implementing high-κ gate dielectrics and metal gates was not because it was unable to do so technologically, but because subsequent advancements prolonged the need to replace SiO_2. *See* ITRS_FEP, 2.

> symmetrical. Unfortunately, these mid-gap metal materials can result in transistor VTs that are not optimized for low-voltage, low-power, high-performance devices.

Hobbs, 1:53-67.

652. Akasaka and Hobbs use a better approach: selecting ***different*** gate metals with work functions appropriate to adjust the threshold voltages of nFET and pFET devices, respectively. *See* Akasaka ¶[0077] ("[T]o decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p^+-poly-crystalline silicon, such as a work function of 4.8 to 5.3 eV."), ¶[0085] ("[T]o decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n^+-poly-crystalline silicon, such as a work function of 3.9 to 4.2 eV."); Hobbs, 8:37-40 ("The work functions of the different materials can be selected such that the threshold voltages can be specifically matched to each of the NMOS and PMOS transistors."). Again, as I explain in Section VI.C above, this approach was not just well known by the time the application for the '686 Patent was filed; it was being used in high-volume commercial devices. *See generally* Mistry2007 (describing Intel's 45nm devices); Mistry_Presentation (same).

653. Both Akasaka and Hobbs implement this solution using what is an RMG process, in which a "dummy" gate electrode is replaced near the end of device

fabrication using the desired gate electrode materials. *See* Akasaka, FIGS. 16-26; Hobbs, FIGS. 4-10.

654. As Hobbs's FIGS. 6 and 7 illustrate below, Hobbs teaches that—in addition to removing and replacing the nFET dummy gate electrode—a dummy nFET gate ***dielectric*** may be removed and replaced as well. Hobbs explains: "[T]he dielectric layer 162 and portions of the liner layer 22 are removed and replaced with a gate dielectric layer 62, as shown in FIG. 7." *See* Hobbs, 4:60-62. "A gate electrode material 64 is then formed within the feature opening 66." Hobbs, 5:12-13.

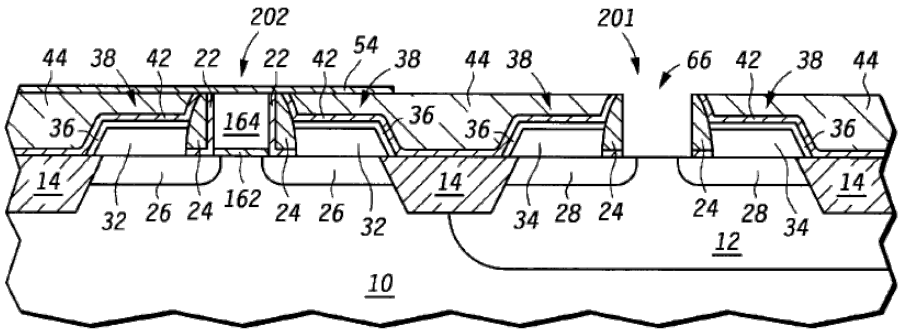


FIG. 6

Hobbs's FIG. 6

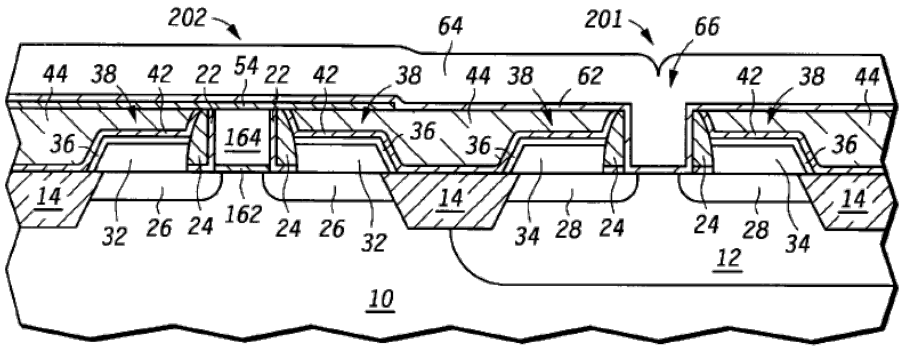


FIG. 7

Hobbs's FIG. 7

655. As Hobbs's FIGS. 8 and 9 similarly illustrate below, Hobbs teaches that a pFET dummy gate dielectric can be removed and replaced along with a pFET dummy gate electrode. "In FIG. 9, portions of capping layer 74, polysilicon layer 164, dielectric layer 162, and the liner layer 22, associated with dummy structure 202, have been removed and replaced with a gate dielectric layer 82 and a gate electrode material 84." Hobbs, 5:52-56.

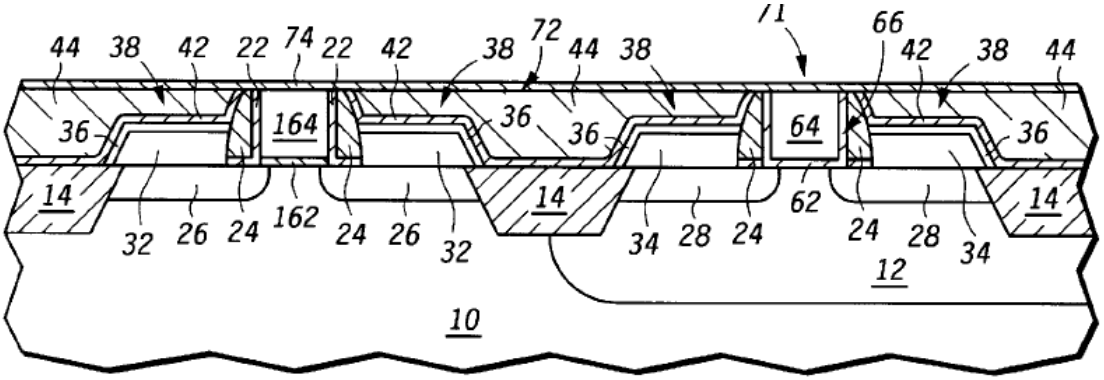


FIG. 8

Hobbs's FIG. 8

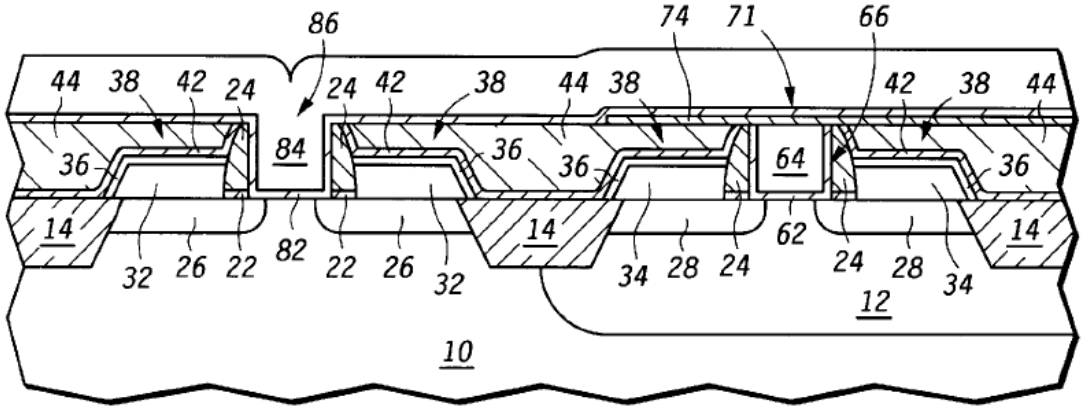


FIG. 9

Hobbs's FIG. 9

656. Hobbs teaches that this process allows for "different gate dielectric materials and thickness[es] as well as different gate materials [to] be selected to form . . . various transistors with different threshold voltages and operating characteristics." Hobbs, 8:40-45; *see also* Hobbs, 5:66-6:5 ("[T]he combination of materials or thicknesses used to form the gate structure from dielectric layer 82 and gate electrode material 84 is selected such that the VT or some other electrical parameter is different from that of the gate structure formed from the gate dielectric layer 62 and gate electrode material 64."), 7:33-37 ("These processing steps can subsequently be repeated to include different materials and thicknesses of gate dielectrics and gate electrodes in the formation of multiple transistors, thereby forming a number of transistors having different physical, operational, and performance characteristics."). This serves the same purpose as described in the '686 Patent, thereby confirming that the '686 Patent is employing this same well-known technique. *See* '686 Patent, 27:39-48 ("[T]he third gate insulating film 35a has a thickness optimized for the n-type MIS transistor and is made of an insulating material optimized for the n-type MIS transistor . . . . Also, the second gate insulating film 13b has a thickness optimized for the p-type MIS transistor and is made of an insulating material optimized for the p-type MIS transistor . . . . Therefore, the flexibility of transistor design is increased, whereby a desired transistor characteristic can be achieved.").

657. Consistent with Hobb's teachings (and also like the '686 Patent), Metz demonstrates that a POSITA would have understood "a single gate dielectric material may not provide the highest performance for both NMOS and PMOS structures" because of "poor band offset with conduction or valence bonds, incompatibility to the gate electrode material, incompatibility with gate electrode processing or thickness requirements." Metz ¶[0026]. "By selecting the better candidate dielectric film for each structure, . . . higher performance complementary metal oxide semiconductor devices may be created . . . ." Metz ¶[0026]. In other words, such devices "may exhibit higher mobility, higher saturation current, or better threshold voltage." Metz ¶[0026].

658. For these reasons—i.e., to achieve better band offset, better compatibility with gate electrode materials, and better compatibility with gate electrode processing and thickness requirements, thereby achieving higher performance CMOS devices with higher mobility, higher saturation current, or better threshold voltage—Hobbs teaches that "the thickness and composition of the second gate dielectric and second gate electrode material can be the same ***or different*** from those of the first gate dielectric and first gate electrode material." Hobbs, 7:65-8:2 (emphasis added); *see also* Hobbs, 8:40-45 ("[D]ifferent gate dielectric materials and thickness[es] as well as different gate materials can be selected to form . . . various transistors with different threshold voltages and operating characteristics.").

659. A POSITA would have understood that Hobbs's teachings in that regard apply equally to RMG devices using high-κ gate insulating films. In fact, Hobbs itself notes that "[t]he first gate dielectric layer can include high-k gate dielectric materials." Hobbs, 7:43-47. Other references confirm this as well. Metz, for instance, explains: "One gate dielectric may be a high-k material (having a dielectric constant greater than 10) and the other may be a low-k material (having a dielectric constant less than 10). Alternatively, both dielectrics may be high-k or both may be low-k dielectrics." Metz ¶[0019]; *see also* Metz ¶¶[0016]-[0017], ¶[0023], FIGS. 1-7. Okazaki similarly explains that suitable "high relative dielectric constant material[s]" in its RMG process "include zirconium oxide (ZrO_2), hafnium oxide (HfO_2), aluminum oxide (Al_2O_3), yttrium oxide (Y_2O_3), and lanthanum oxide (La_2O)," as well as "metal silicates such as HfSiO, ZrSiO, AlSiO, and LaSiO." Okazaki, 6:21-34; *see also* Okazaki, FIGS. 2B-2F. And Hsu660 explains that suitable gate dielectric films for its RMG process "include a metal oxide [or] a silicate of Hf, Al, Zr, combinations thereof, and multi-layers thereof." Hsu660, 5:16-30; *see also* Hsu660, FIG. 10.

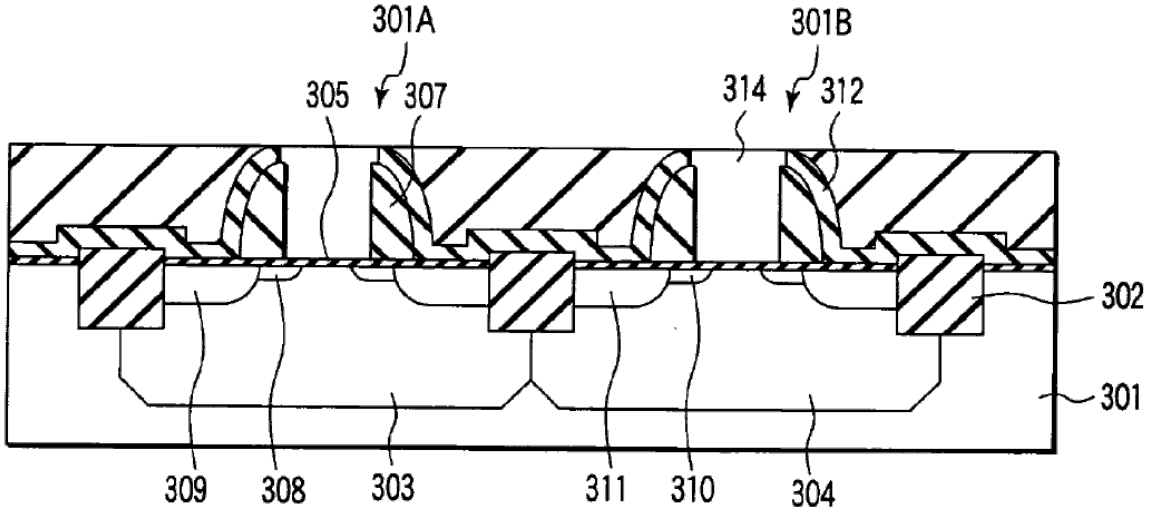


FIG. 18

Akasaka's FIG. 18

660. A POSITA also would have understood that the procedure Hobbs teaches is entirely compatible with Akasaka's RMG process. A POSITA thus would have reasonably expected to succeed in implementing different gate dielectric films in Akasaka's nFET and pFET devices according to Hobbs's teachings. For example, at the step of Akasaka's process shown in FIG. 18, a POSITA would have found it obvious to remove Akasaka's gate dielectric film from one or both of the nFET and pFET gate regions after removing the dummy nFET and pFET gate electrodes, and then to form a different gate dielectric film in each region so the gate dielectrics are uniquely tailored to each device.

661. A POSITA would have reasonably expected to succeed in doing so based on the success others previously had in doing the same. *See* Hobbs, FIGS. 4-10; Metz, FIGS. 1-7; Okazaki, FIGS. 2B-2F; Hsu660, FIGS. 10-11.

Moreover, a POSITA would have understood this would provide the known and predictable result that Hobbs teaches: forming pFET and nFET gate dielectric films with properties uniquely tailored to each. *See, e.g.*, Hobbs, 5:66-6:5 ("[T]he combination of materials or thicknesses used to form the [nFET] gate structure from dielectric layer 82 and gate electrode material 84 is selected such that the VT or some other electrical parameter is different from that of the [pFET] gate structure formed from the gate dielectric layer 62 and gate electrode material 64."), 8:40-45 ("[D]ifferent gate dielectric materials and thickness[es] as well as different gate materials can be selected to form . . . various transistors with different threshold voltages and operating characteristics.").

2. Claim 32

662. In the Akasaka-Hsu823-Hobbs combination, "the first and second gate insulating films are made of different insulating materials."

663. As I explain immediately above in Section IX.H.1, as an alternative to using the same high-κ gate dielectric film in both Akasaka's nFET and pFET devices, a POSITA would have found it obvious to use different gate dielectric films for Akasaka's nFET and pFET devices to improve device performance. *See* Hobbs, 7:43-47, 7:65-8:2; Metz ¶[0019], ¶[0026]; Okazaki, 6:21-34. In such an embodiment, Akasaka's first and second gate insulating films (i.e., the gate dielectric

films formed in nFET area 301B and pFET area 301A, respectively) would be made of different insulating materials as claimed.

X. Conclusion

664. As discussed above, it is my opinion that the Challenged Claims of the '686 Patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

665. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

666. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

667. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false

statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 11th day of March, 2025, in Gainesville, FL.

By: 

Dr. Scott E. Thompson, Ph.D.

Appendix A

Exhibit	Description
Ex-1001	U.S. Patent No. 8,198,686 B2 to Sato et al. ("'686 Patent").
Ex-1002	Prosecution File History of the '686 Patent ("'686 File History").
Ex-1003	Declaration of Dr. Scott E. Thompson, Ph.D.
Ex-1004	Curriculum Vitae of Dr. Scott E. Thompson, Ph.D.
Ex-1005	U.S. Pat. Pub. No. 2007/0215950 A1 to Aoyama ("Aoyama").
Ex-1006	U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. ("Hsu823").
Ex-1007	U.S. Patent No. 6,171,910 B2 to Hobbs et al. ("Hobbs").
Ex-1008	U.S. Pat. Pub. No. 2007/0066077 A1 to Akasaka et al. ("Akasaka").
Ex-1009	S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) (excerpted) ("Sze").
Ex-1010	J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (excerpted) ("Plummer").
Ex-1011	M. Baklanov et al., *Dielectric Films for Advanced Microelectronics* (2007) (excerpted) ("Baklanov").
Ex-1012	International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) ("ITRP_FEP").
Ex-1013	International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures (2007 ed.) ("ITRS_PIDS").
Ex-1014	U.S. Pat. Pub. No. 2006/0081939 A1 to Akasaka et al. ("Akasaka939").

Exhibit	Description
Ex-1015	U.S. Pat. Pub. No. 2006/0022277 A1 to Kavalieros et al. ("Kavalieros").
Ex-1016	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry2007").
Ex-1017	K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) ("Mistry_Presentation").
Ex-1018	U.S. Patent No. 6,881,631 B2 to Saito et al. ("Saito").
Ex-1019	U.S. Patent No. 7,812,414 B2 to Hou et al. ("Hou").
Ex-1020	U.S. Pat. Pub. No. 2005/0258468 A1 to Colombo et al. ("Colombo").
Ex-1021	U.S. Patent No. 6,849,511 B2 to Iriyama et al. ("Iriyama")
Ex-1022	U.S. Pat. Pub. No. 2002/0037615 A1 to Matsuo ("Matsuo").
Ex-1023	S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) ("Thompson2004").
Ex-1024	Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) ("Sun").

Exhibit	Description
Ex-1025	D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005) ("James").
Ex-1026	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. ("Murthy151").
Ex-1027	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. ("Bohr683").
Ex-1028	P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) ("Morin").
Ex-1029	U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al. ("Jung").
Ex-1030	Y.C. Liu et al., "Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-39 (Dec. 2005) ("Liu").
Ex-1031	U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al. ("Ke").
Ex-1032	P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) ("Bai").
Ex-1033	Westlinder et al., "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices," IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552 (Sept. 2003) ("Westlinder").
Ex-1034	U.S. Pat. Pub. No. 2007/0105317 A1 to Nakajima ("Nakajima").

Exhibit	Description
Ex-1035	G. Eneman et al., "Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study," IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-53 (June 2007) ("Eneman").
Ex-1036	M. Quirk & J. Serda, *Semiconductor Manufacturing Technology*, Ch. 12: Metallization (2001) (excerpted) ("Quirk").
Ex-1037	U.S. Patent No. 7,785,952 B2 to Chang et al. ("Chang").
Ex-1038	U.S. Patent No. 8,536,660 B2 to Hsu et al. ("Hsu660").
Ex-1039	U.S. Patent Pub. No. 2005/0048754 A1 to Yeh et al. ("Yeh").
Ex-1040	U.S. Patent Pub. No. 2006/0001106 A1 to Metz et al. ("Metz").
Ex-1041	U.S. Patent No. 8,486,789 B2 to Okazaki et al. ("Okazaki").

Appendix B

Claim 1	
[1Pre]	A semiconductor device comprising:
[1A]	a first MIS transistor; and
[1B]	a second MIS transistor, wherein:
[1C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;
[1D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[1E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[1F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[1G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;
[1H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

[1I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[1J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[1K]	[the second MIS transistor includes: …] source/drain regions formed in the second active region laterally outside the second sidewall spacers,
[1L]	the first and second metal films are made of different metal materials,
[1M]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[1N]	the source/drain regions include a silicon mixed crystal layer which is formed in trenches provided in the second active region, and causes first stress in a gate length direction of a channel region in the second active region, and
[1O]	the silicon nitride film has a thickness smaller than that of the first gate electrode.
Claim 2	
The semiconductor device of claim 1, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 3	
The semiconductor device of claim 1, wherein the first and second metal films have different work functions.	
Claim 4	
The semiconductor device of claim 1, wherein the conductive film is made of the second metal film.	

Claim 5
The semiconductor device of claim 1, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.
Claim 6
The semiconductor device of claim 1, wherein the first and second gate insulating films are made of the same insulating material.
Claim 7
The semiconductor device of claim 1, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
Claim 8
The semiconductor device of claim 1, wherein the silicon nitride film causes second stress in a gate length direction of a channel region in the first active region.
Claim 9
The semiconductor device of claim 8, wherein: the first MIS transistor is an n-type MIS transistor, and the second stress is tensile stress.
Claim 10
The semiconductor device of claim 1, wherein the second MIS transistor is a p-type MIS transistor, the silicon mixed crystal layer is made of a SiGe layer, and the first stress is compressive stress.

Claim 11	
[11Pre]	A semiconductor device comprising:
[11A]	a first MIS transistor; and
[11B]	a second MIS transistor, wherein:
[11C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;
[11D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[11E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[11F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[11G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;
[11H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[11I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;

[11J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[1K]	the first and second metal films are made of different metal materials,
[1L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[11M]	the conductive film is made of a silicon film,
[11N]	the semiconductor device further comprises a metal silicide film formed on the silicon film, and
[11O]	the silicon nitride film has a thickness smaller than that of the first gate electrode.
Claim 12	
The semiconductor device of claim 11, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 13	
The semiconductor device of claim 11, wherein the first and second metal films have different work functions.	
Claim 14	
The semiconductor device of claim 11, wherein the first and second gate insulating films are made of the same insulating material.	
Claim 15	
The semiconductor device of claim 11, wherein the first and second gate insulating films are made of different insulating materials.	

Claim 16
The semiconductor device of claim 11, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.

Claim 17
The semiconductor device of claim 11, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

Claim 18
The semiconductor device of claim 1, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

Claim 19	
[19Pre]	A semiconductor device comprising:
[19A]	a first MIS transistor; and
[19B]	a second MIS transistor, wherein:
[19C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, and including a first high-k film made of oxide containing hafnium and silicon;
[19D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[19E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and
[19F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which

	the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[19G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, and including a second high-k film made of oxide containing hafnium and silicon;
[19H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[19I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[19J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[19K]	the first and second metal films are made of different metal materials,
[19L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and
[19M]	the first metal film is made of titanium nitride.
Claim 20	
The semiconductor device of claim 19, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 21	
The semiconductor device of claim 19, wherein the first and second metal films have different work functions.	

Claim 22	
The semiconductor device of claim 19, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.	
Claim 23	
The semiconductor device of claim 19, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.	
Claim 24	
The semiconductor device of claim 19, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.	
Claim 25	
[25Pre]	A semiconductor device comprising:
[25A]	a first MIS transistor; and
[25B]	a second MIS transistor, wherein:
[25C]	the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;
[25D]	[the first MIS transistor includes: …] a first gate electrode including a second metal film formed on the first gate insulating film;
[25E]	[the first MIS transistor includes: …] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

[25F]	[the first MIS transistor includes: …] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,
[25G]	the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;
[25H]	[the second MIS transistor includes: …] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;
[25I]	[the second MIS transistor includes: …] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;
[25J]	[the second MIS transistor includes: …] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and
[25K]	the first and second metal films are made of different metal materials,
[25L]	the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,
[25M]	the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.
Claim 26	
The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.	
Claim 27	
The semiconductor device of claim 25, wherein the first and second metal films have different work functions.	

Claim 28
The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.
Claim 29
The semiconductor device of claim 25, wherein the conductive film is made of the second metal film.
Claim 30
The semiconductor device of claim 25, wherein the conductive film is made of a silicon film, and the semiconductor device further comprises a metal silicide film formed on the silicon film.
Claim 31
The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.
Claim 32
The semiconductor device of claim 25, wherein the first and second gate insulating films are made of different insulating materials.
Claim 33
The semiconductor device of claim 25, wherein: each of the first sidewall spacers is made of a first inner sidewall having an L-shaped cross-section, and each of the second sidewall spacers is made of a second inner sidewall having an L-shaped cross-section, and the silicon nitride film is formed in contact with surfaces of the first and second inner sidewalls which are bent in an L-shape.
Claim 34
The semiconductor device of claim 25, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

Claim 35
The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.