

Exhibit 686-02: Akasaka077

U.S. Patent Appl. Pub. No. 2007/0066077 A1 to Akasaka et al. (“Akasaka077”) was filed on September 20, 2006, and published on March 22, 2007. Accordingly, Akasaka077 constitutes prior art to U.S. Patent No. 8,198,686 (the “’686 patent”) under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

Akasaka077, including any material incorporated by reference into Akasaka077, anticipates claims 25-29, 31, 34, and 35 (the “asserted claims”) of the ’686 patent under pre-AIA 35 U.S.C. §§ 102(a) and (e).

To the extent any limitation is found not to be expressly or inherently disclosed in Akasaka077, such a limitation would have been obvious either based on Akasaka077 alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 686-01 and 686-03 through 686-09, because the ’686 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’686 patent in the aforementioned Exhibits may be combined with the disclosures of Akasaka077 identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.¹

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

¹ Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

Exemplary Disclosures

25[pre] A semiconductor device, comprising:

Defendant does not concede that the preamble is limiting. To the extent it is limiting, Akasaka077 discloses the preamble. For example, Akasaka077 discloses a semiconductor device according to a second embodiment. *See, e.g.*, the following:

“The present invention relates to a method for manufacturing a semiconductor device, particularly an FET (Field Effect Transistor) of the MIS (Metal Insulator Semiconductor) type, and to a method for forming a silicon containing dielectric (insulating) film, utilized in, e.g., a semiconductor processing system. The term ‘semiconductor process used herein includes various kinds of processes which are performed to manufacture a semiconductor device or a structure having wiring layers, electrodes, and the like to be connected to a semiconductor device, on a target substrate, such as a semiconductor wafer or a glass substrate used for an LCD (Liquid Crystal Display) or FPD (Flat Panel Display), by forming semiconductor layers, insulating layers, and conductive layers in predetermined patterns on the target substrate.”

Akasaka077 ¶ [0003].

“FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.”

Akasaka077 ¶ [0072].

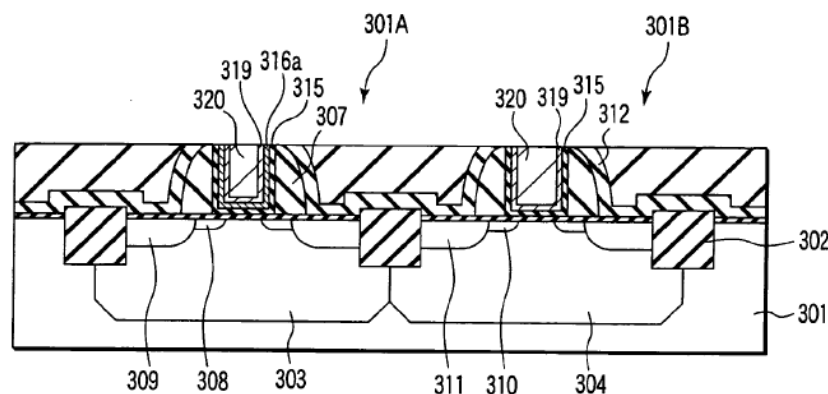


FIG. 26

Akasaka077, FIG. 26.

See also, e.g., Akasaka077, Title, Abstract, ¶¶ [0002]-[0032], ¶¶ [0072]-[0090], FIGS. 15-26.

To the extent that Akasaka077 is found not to disclose the preamble, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[a] a first MIS transistor; and

Akasaka077 discloses this feature. For example, Akasaka077 discloses an n-type MISFET (nFET) formed in an area 301B in the second embodiment. See, e.g., the following:

"FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.

"Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312."

Akasaka077 ¶¶ [0072]-[0073].

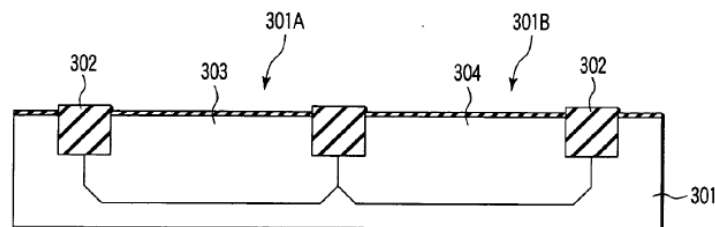


FIG. 15

Akasaka077, FIG. 15 (showing formation of nFET region 301B).

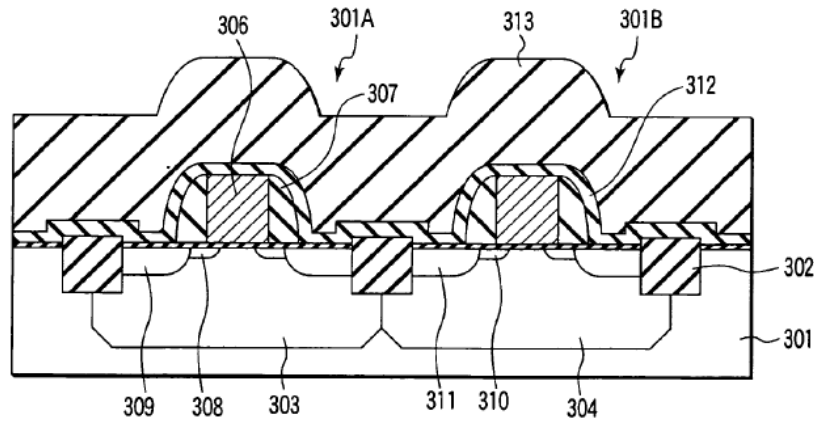


FIG. 16

Akasaka077, FIG. 16 (showing the early stages of forming an nFET in region 301B).

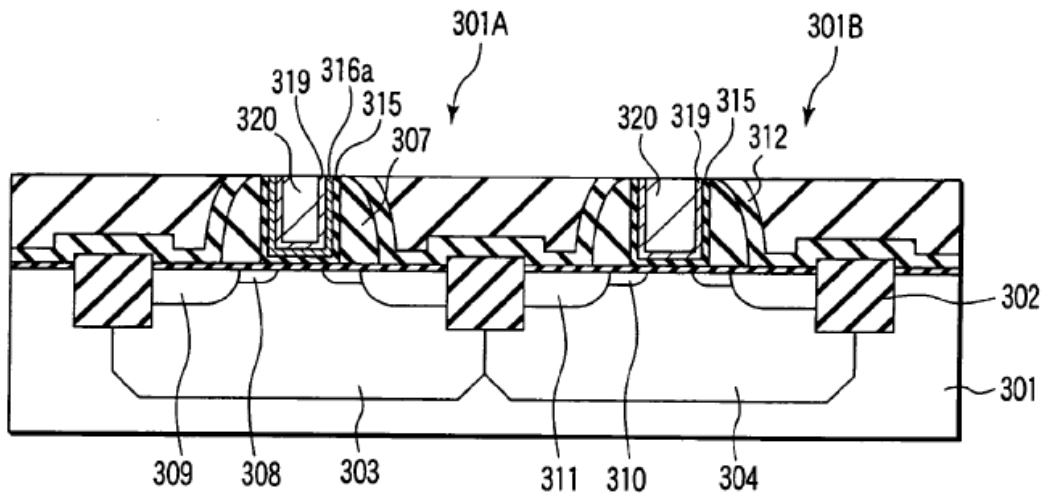


FIG. 26

Akasaka077, FIG. 26 (showing the final structure of the nFET in region 301B).

See also, e.g., Akasaka077, ¶¶ [0002]-[0008], ¶¶ [0072]-[0090], FIGS. 15-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[b] a second MIS transistor, wherein:

Akasaka077 discloses this feature. For example, Akasaka077 discloses a p-type MISFET (pFET) formed in an area 301A in the second embodiment. *See, e.g.*, the following:

“FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.

“Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.”

Akasaka077 ¶¶ [0072]-[0073].

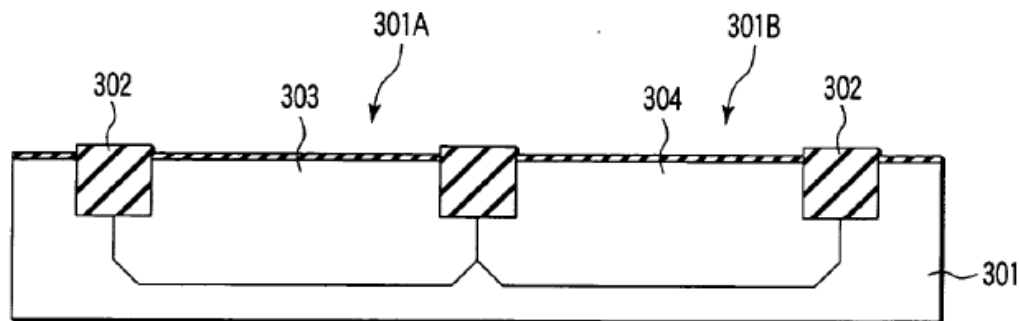


FIG. 15

Akasaka077, FIG. 15 (showing formation of pFET region 301A).

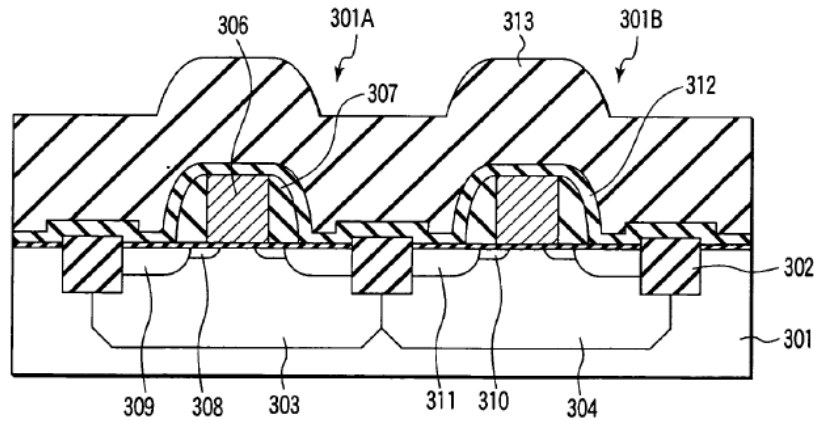


FIG. 16

Akasaka077, FIG. 16 (showing the early stages of forming a pFET in region 301A).

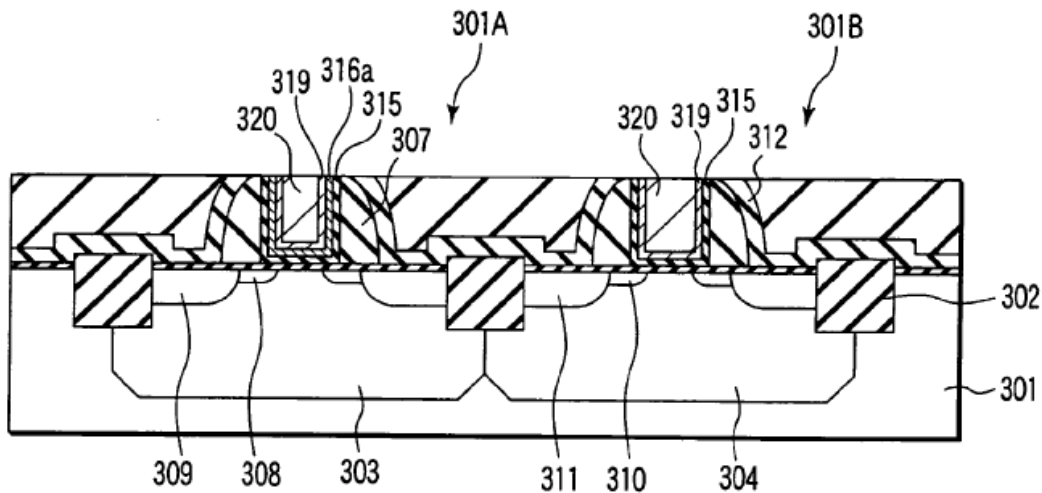


FIG. 26

Akasaka077, FIG. 26 (showing the final structure of the pFET in region 301A).

See also, e.g., Akasaka077, ¶¶ [0002]-[0008], ¶¶ [0072]-[0090], FIGS. 15-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[c] the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;

Akasaka077 discloses this feature. For example, Akasaka077 discloses gate dielectric (insulating) film 315 formed on nFET region 301B in the second embodiment. *See, e.g.*, the following:

“FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively.”

Akasaka077 ¶ [0072].

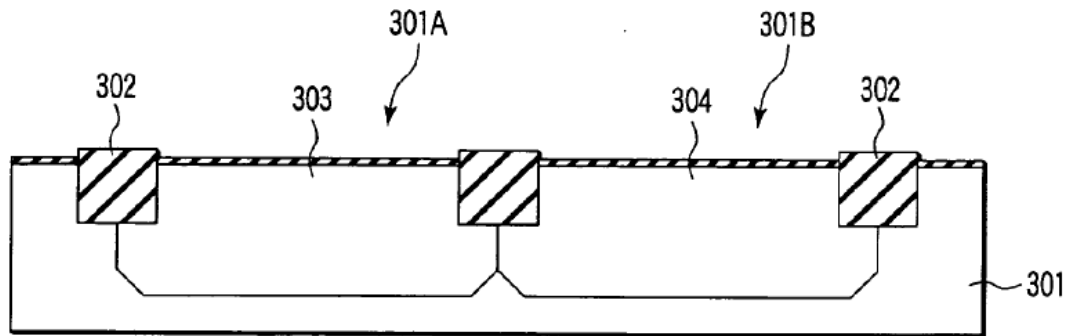


FIG. 15

Akasaka077, FIG. (showing the formation of nFET region 301B).

“Then, a gate dielectric (insulating) film 315 is deposited all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO_2 , HfSi_xO_y , HfAl_xO_y , or SiO_2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.”

Akasaka077 ¶ [0075].

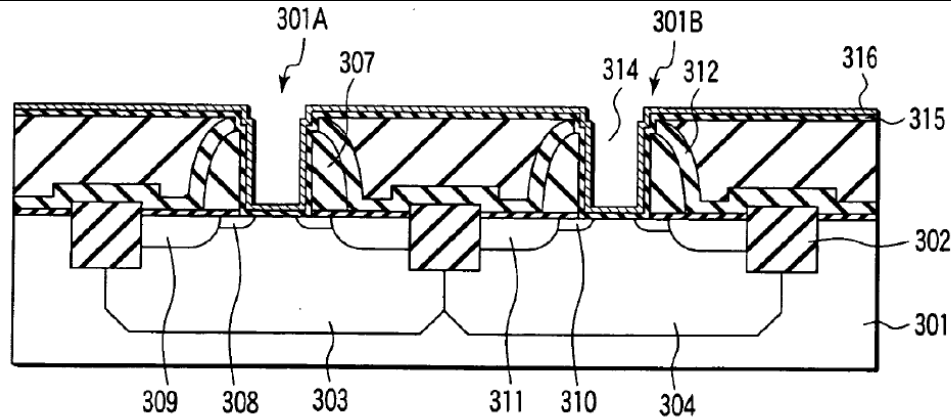


FIG. 19

Akasaka077, FIG. 19 (showing the initial formation of gate dielectric (insulating) film 315 on nFET region 301B).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077, ¶ [0087].

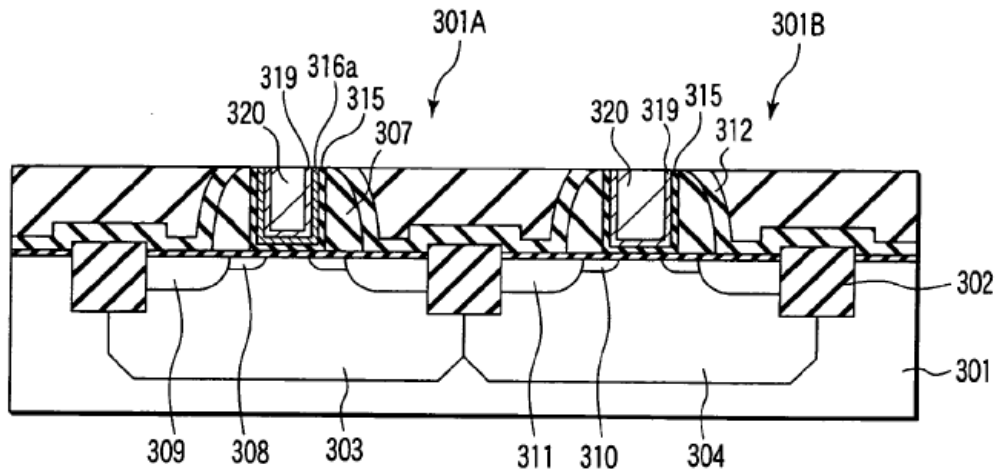


FIG. 26

Akasaka077, FIG. 26 (showing gate dielectric (insulating) film 315 formed on nFET region 301B after polishing / planarization by chemical-mechanical polishing (CMP)).

See also, e.g., Akasaka077 ¶ [0003], ¶ [0006], ¶ [0072], ¶ [0075], ¶ [0082]-[0083], ¶ [0087]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[d] [the first MIS transistor includes: . . .] a first gate electrode including a second metal film formed on the first gate insulating film;

Akasaka077 discloses this feature. For example, Akasaka077 discloses in its second embodiment an nFET gate electrode—which comprises (1) a conductive film 319 made of a pure metal, a metal silicide, a metal nitride, or another compound with a metallic band structure suitable for an nFET and (2) a conductive film 320 (e.g., tungsten (W))—formed on the nFET gate dielectric (insulating) film 315. Conductive film 319 and/or conductive film 320 constitute a second metal film. *See, e.g.*, the following:

“Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n-poly crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-Iva element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.

“Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth.

Akasaka077 ¶¶ [0084]-[0086].

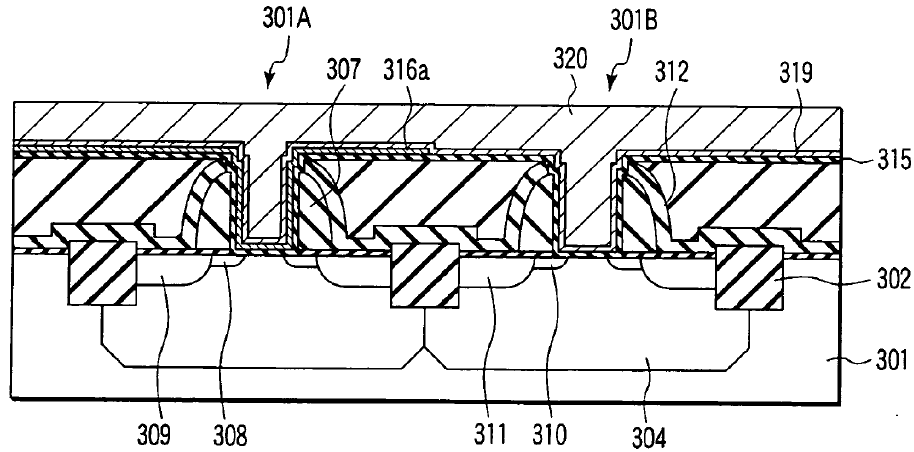


FIG. 25

Akasaka077, FIG. 25 (showing the formation of conductive films 319 and 320 on gate dielectric (insulating) film 315 in nFET region 301B prior to polishing / planarization by chemical-mechanical polishing (CMP)).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077 ¶ [0087].

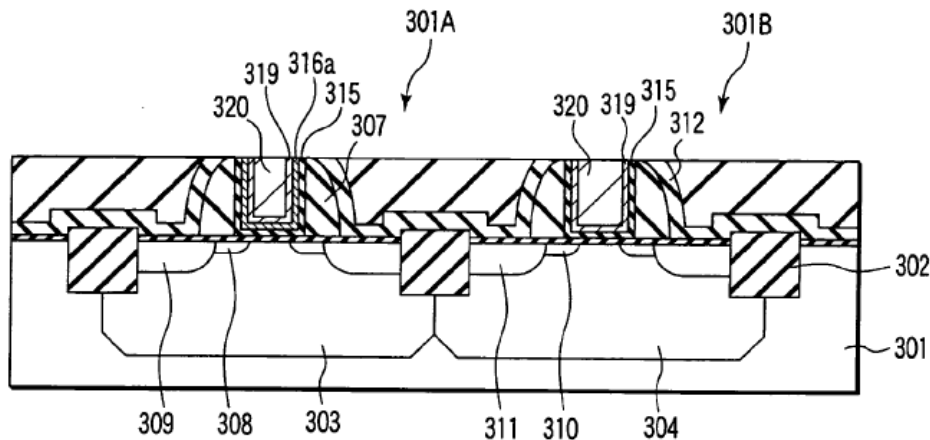


FIG. 26

Akasaka077, FIG. 26 (showing conductive films 319 and 320 formed on gate dielectric (insulating) film 315 in nFET region 301B in the final structure).

See also, e.g., Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0082]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[e] [the first MIS transistor includes: . . .] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

Akasaka077 discloses this feature. For example, Akasaka077 discloses gate sidewalls 307, which are made of an insulating film like silicon nitride, formed on side surfaces of the nFET gate electrode in nFET region 301B in the second embodiment. *See, e.g.,* the following:

"Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301 B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312."

Akasaka077 ¶ [0073].

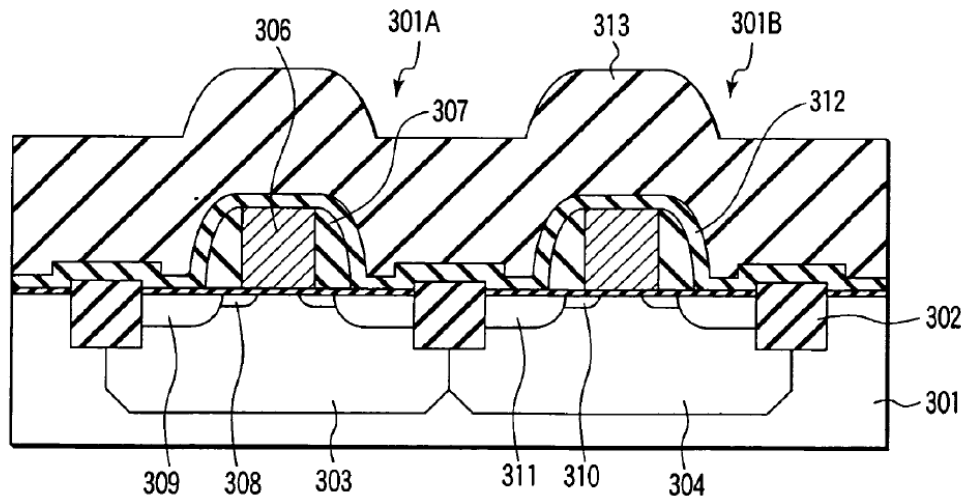


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of gate sidewalls 307 on side surfaces of the dummy gate electrode structures for the nFET gate electrode in nFET region 301B).

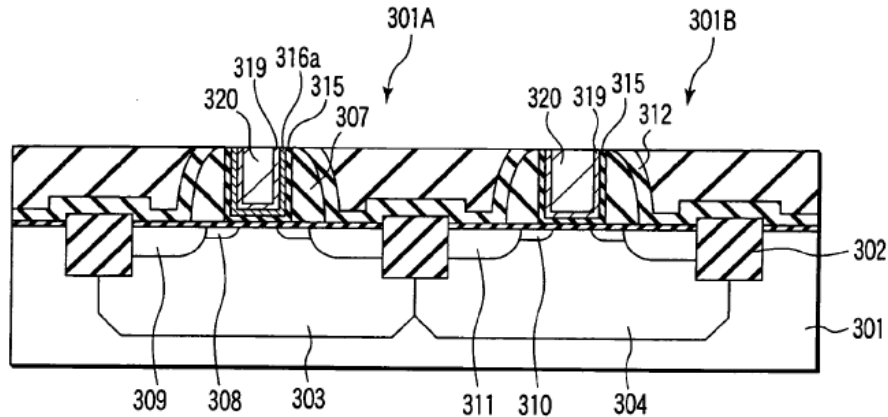


FIG. 26

Akasaka077, FIG. 26 (showing gate sidewalls 307 formed on side surfaces of the nFET gate electrode in nFET region 301B).

See also, e.g., Akasaka077 ¶ [0005], ¶ [0007], ¶ [0073], ¶¶ [0084]-[0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[f] [the first MIS transistor includes: . . .] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

Akasaka077 discloses this feature. For example, Akasaka077 discloses silicon nitride film 312 in the second embodiment, which extends over (1) the side surfaces of the gate electrode in nFET region 301B where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 311 located in the nFET active region laterally outside of gate sidewalls 307. See, e.g., the following:

“Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall

307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.”

Akasaka077 ¶ [0073].

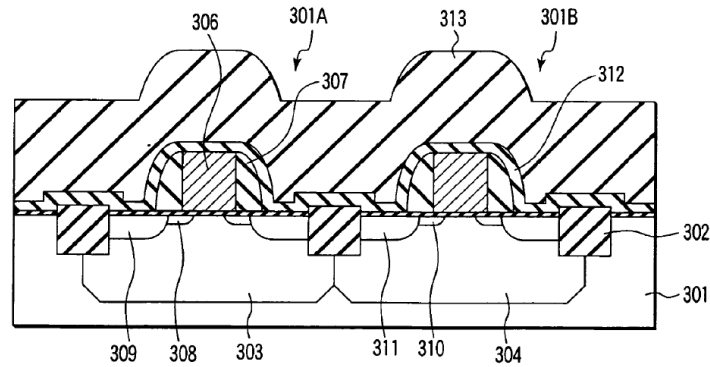


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of silicon nitride film 312 extending over (1) the side surfaces of the dummy structure for the gate electrode in nFET region 301B where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 311 located in the nFET active region laterally outside of gate sidewalls 307).

“Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.”

Akasaka077 ¶ [0074].

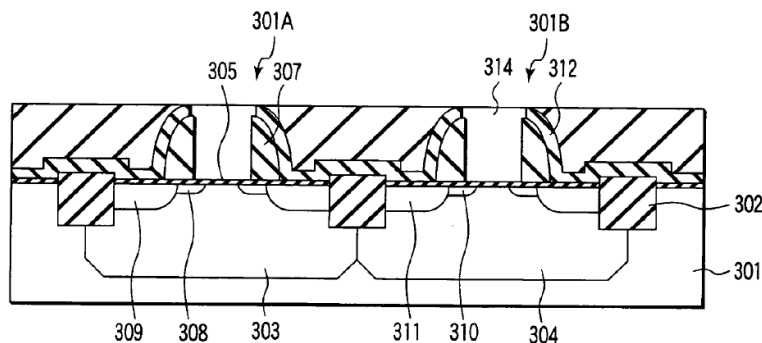


FIG. 18

Akasaka077, FIG. 18 (showing silicon nitride film 312 after CMP planarization and removal of silicon nitride film 312 from the upper surfaces of the nFET and pFET dummy gate electrodes).

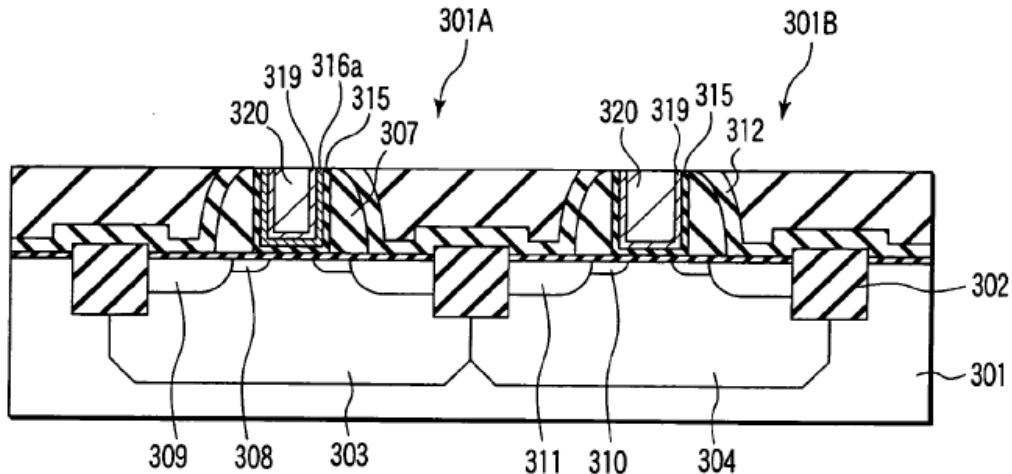


FIG. 26

Akasaka077, FIG. 26 (showing the silicon nitride film 312 in the final structure extending over (1) the side surfaces of the gate electrode in nFET region 301B where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 311 located in the nFET active region laterally outside of gate sidewalls 307).

See also, e.g., Akasaka077 ¶ [0007], ¶¶ [0072]-[0074], ¶¶ [0084]-[0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[g] the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;

Akasaka077 discloses this feature. For example, Akasaka077 discloses gate dielectric (insulating) film 315 formed on pFET region 301A in the second embodiment. See, e.g., the following:

"FIGS. 15 to 26 are sectional views showing sequentially ordered steps in a method for manufacturing a semiconductor device according to a second embodiment of the present invention. At first, as shown in FIG. 15, an n-type well 303 and a p-type well 304 are respectively formed in the surface of first and second areas 301A and 301B of a semiconductor substrate 301 consisting mainly of silicon. Further, a device isolation area 302 is formed in the surface of the substrate 301 to surround the first and second areas 301A and 301B. The first and second areas 301A and 301B correspond to areas for forming a p-type MISFET and an n-type MISFET, respectively."

Akasaka077 ¶ [0072].

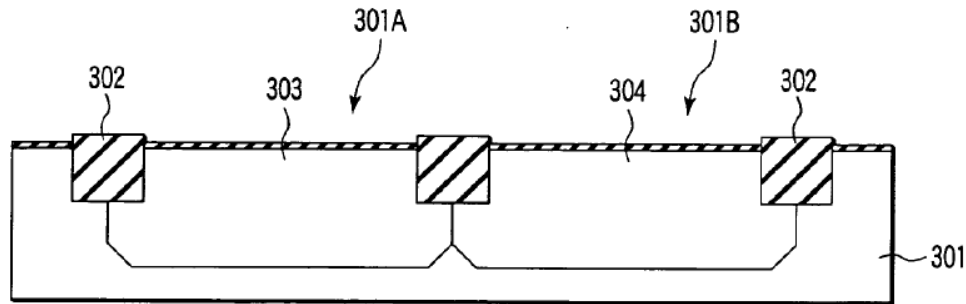


FIG. 15

Akasaka077, FIG. (showing the formation of pFET region 301A).

“Then, a gate dielectric (insulating) film 315 is deposited all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO_2 , HfSi_xO_y , HfAl_xO_y , or SiO_2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.”

Akasaka077 ¶ [0075].

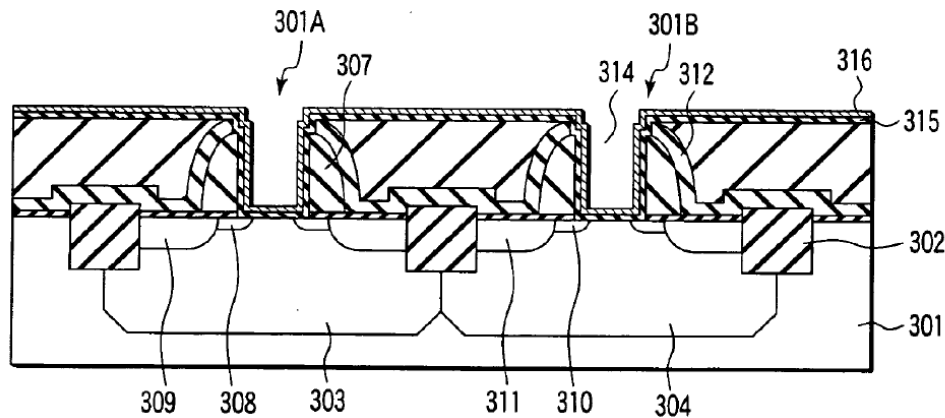


FIG. 19

Akasaka077, FIG. 19 (showing the initial formation of gate dielectric (insulating) film 315 on pFET region 301A).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077, ¶ [0087].

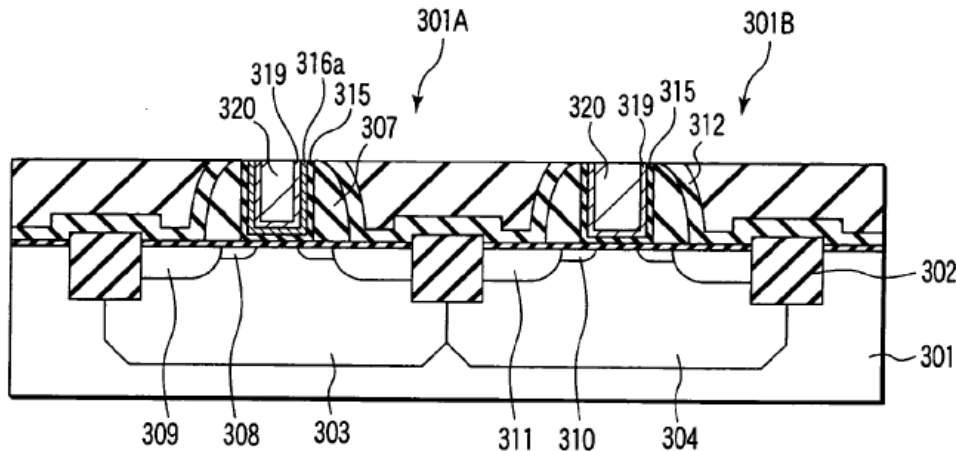


FIG. 26

Akasaka077, FIG. 26 (showing gate dielectric (insulating) film 315 formed on pFET region 301A after polishing / planarization by chemical-mechanical polishing (CMP)).

See also, e.g., Akasaka077 ¶ [0003], ¶ [0006], ¶ [0072], ¶ [0075], ¶¶ [0082]-[0083], ¶¶ [0087]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[h] [the second MIS transistor includes: . . .] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

Akasaka077 discloses this feature. For example, Akasaka077 discloses in its second embodiment a pFET gate electrode—which comprises (1) a conductive film 316a made of a pure metal, metal silicide, metal nitride (e.g., titanium nitride TiN), or another compound with a metallic band structure suitable for a pFET, (2) a conductive film 319 made of a pure metal, a metal silicide, a metal nitride, or another compound with a metallic band structure suitable for an nFET, and (3) a conductive film 320 (e.g., tungsten (W))—formed on the pFET gate dielectric (insulating) film 315. Conductive film 316a constitutes a first metal film. Conductive film 319 and/or conductive film 320 constitutes a conductive film formed on the first metal film. See, e.g., the following:

“Then, a TiN conductive film 316 to define the bottom portion of the gate electrode of the p-type MISFET is formed on the gate dielectric film 315 all over the substrate. The conductive film 316 is disposed to control the work function of the gate electrode of the p-type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p-poly crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co., Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p-poly crystalline silicon. The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm. In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316.”

Akasaka077 ¶¶ [0076]-[0077].

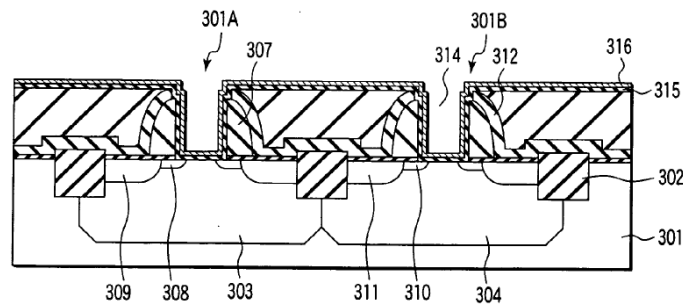


FIG. 19

Akasaka077, FIG. 19 (showing the initial formation of conductive film 316).

“Then, as shown in FIG. 24, wet etching using a solution of e.g., H_2O_2 , or a mixture of H_2SO_4 and H_2O_2 is performed thorough the etching mask 317a used as a mask. Consequently, a pre-patterned conductive film 316a is formed by patterning of the conductive film 316. The pre-patterned conductive film 316a is shaped to cover at least that part of the gate dielectric film 315 where the gate electrode of the p-type MISFET is to be formed in the first area 301A. On the other hand, this patterning exposes that part of the gate dielectric film 315 where the gate electrode of the n-type MISFET is to be formed in the second area 301B.”

Akasaka077 ¶ [0082].

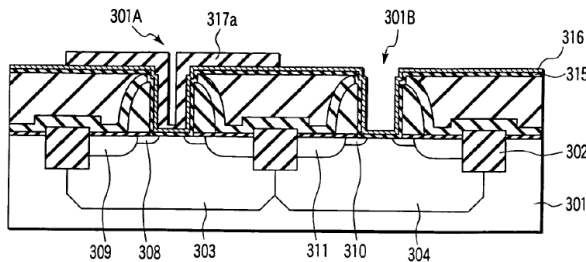


FIG. 23

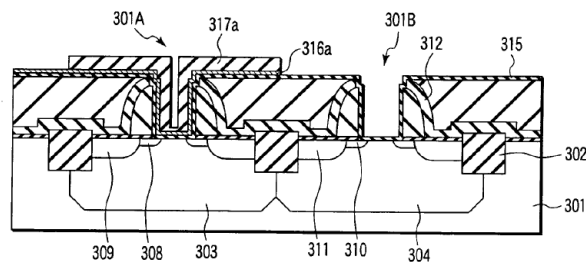


FIG. 24

Akasaka077, FIGS. 23 and 24 (showing removal of conductive film 316 in nFET region 301B, leaving conductive film 316a only in pFET region 301A).

“Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n-poly crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-IVa element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.

“Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth.”

Akasaka077 ¶¶ [0084]-[0086].

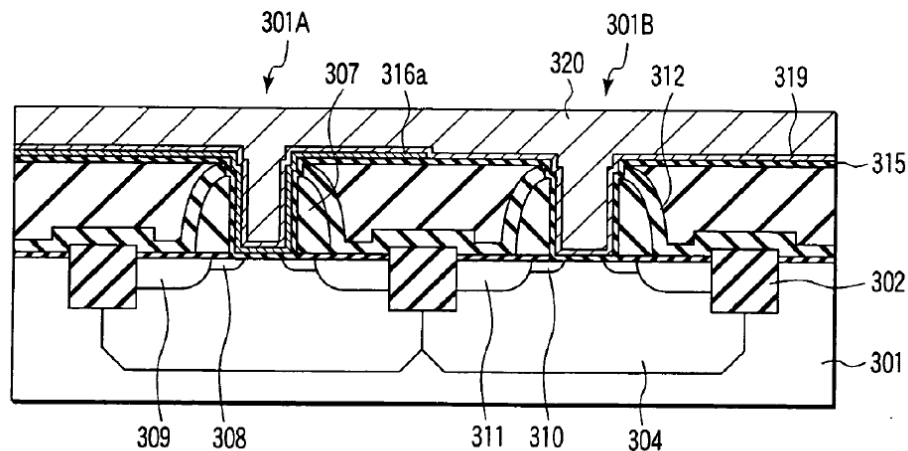


FIG. 25

Akasaka077, FIG. 25 (showing the formation of conductive films 319 and 320 on gate dielectric (insulating) film 315 in nFET region 301B prior to polishing / planarization by chemical-mechanical polishing (CMP)).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077 ¶ [0087].

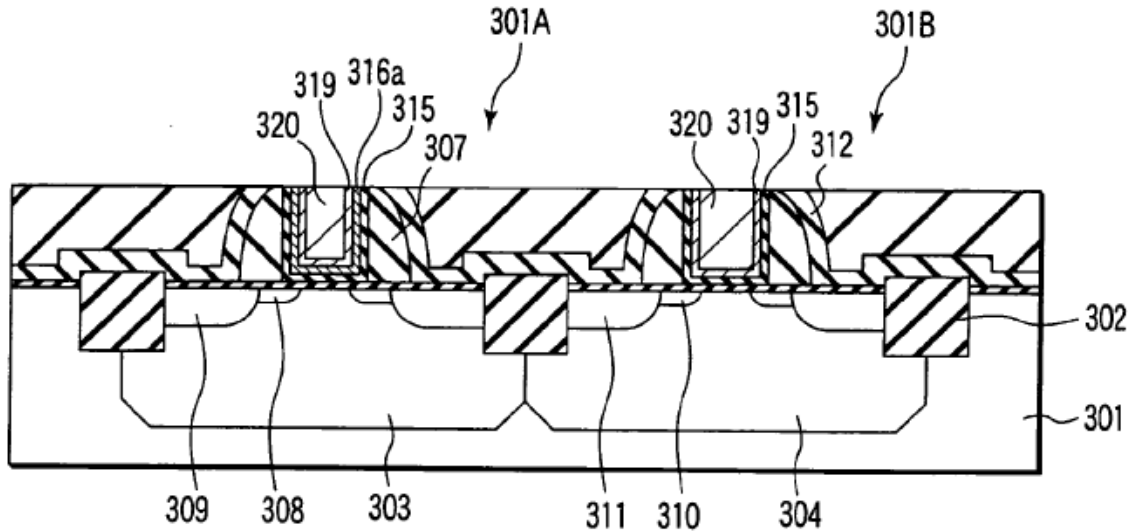


FIG. 26

Akasaka077, FIG. 26 (showing conductive films 319 and 320 formed on gate dielectric (insulating) film 315 in nFET region 301B in the final structure).

See also, e.g., Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

25[i] [the second MIS transistor includes: . . .] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;

Akasaka077 discloses this feature. For example, Akasaka077 discloses gate sidewalls 307, which are made of an insulating film like silicon nitride, formed on side surfaces of the pFET gate electrode in pFET region 301A in the second embodiment. *See, e.g.*, the following:

“Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301 B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.”

Akasaka077 ¶ [0073].

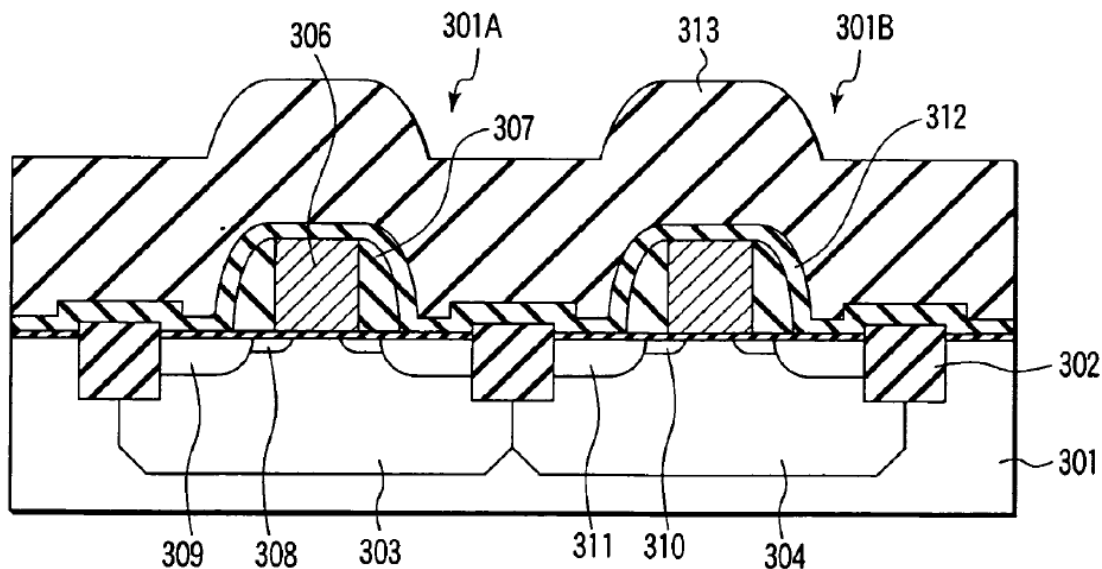


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of gate sidewalls 307 on side surfaces of the dummy gate electrode structures for the pFET gate electrode in pFET region 301A).

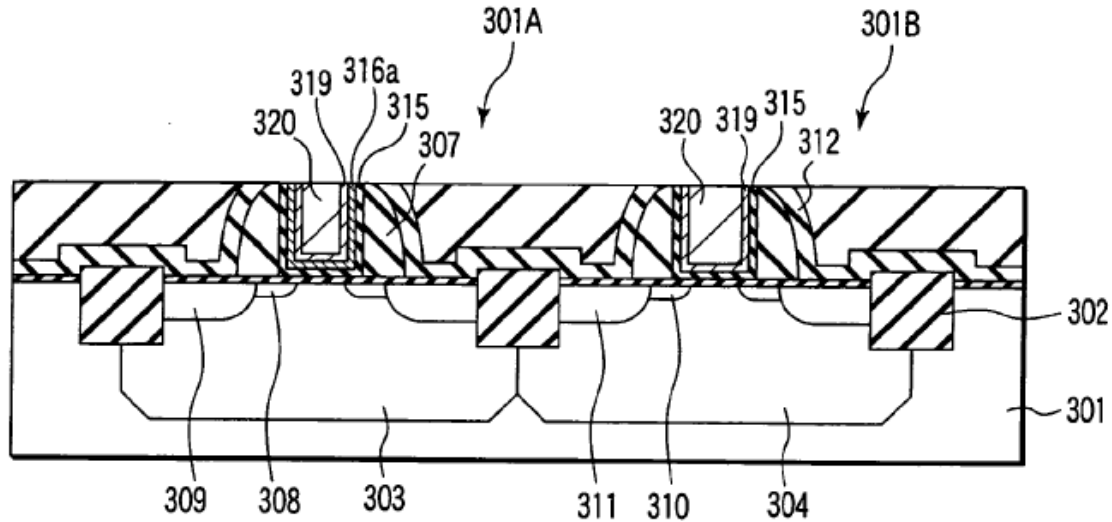


FIG. 26

Akasaka077, FIG. 26 (showing gate sidewalls 307 formed on side surfaces of the pFET gate electrode in pFET region 301A).

See also, e.g., Akasaka077 ¶ [0005], ¶ [0007], ¶ [0073], ¶¶ [0084]-[0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[j] [the second MIS transistor includes: . . .] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and

Akasaka077 discloses this feature. For example, Akasaka077 discloses silicon nitride film 312 in the second embodiment, which extends over (1) the side surfaces of the gate electrode in pFET region 301A where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 309 located in the pFET active region laterally outside of gate sidewalls 307. See, e.g., the following:

“Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of

predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.

Akasaka077 ¶ [0073].

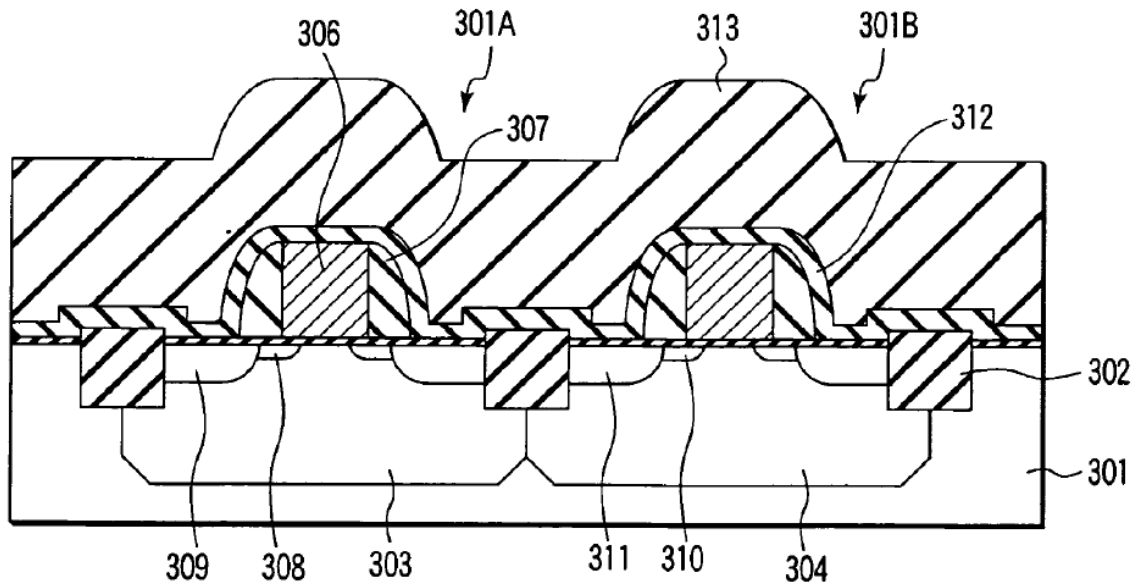


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of silicon nitride film 312 extending over (1) the side surfaces of the dummy structure for the gate electrode in pFET region 301A where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 309 located in the pFET active region laterally outside of gate sidewalls 307).

“Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.”

Akasaka077 ¶ [0074].

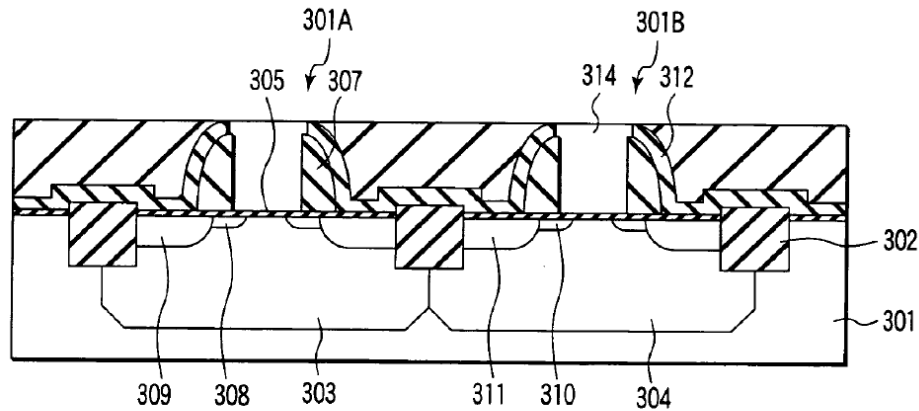


FIG. 18

Akasaka077, FIG. 18 (showing silicon nitride film 312 after CMP planarization and removal of silicon nitride film 312 from the upper surfaces of the nFET and pFET dummy gate electrodes).

Akasaka077 ¶ [0084].

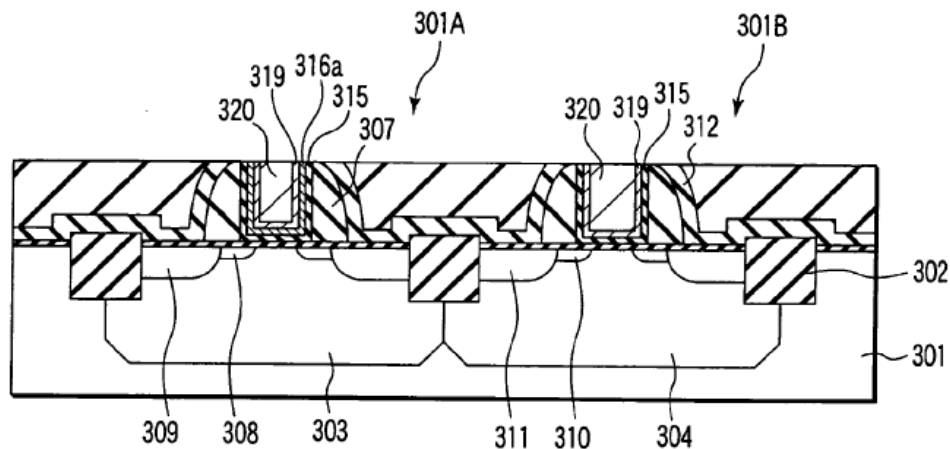


FIG. 26

Akasaka077, FIG. 26 (showing the silicon nitride film 312 in the final structure extending over (1) the side surfaces of the gate electrode in pFET region 301A where gate sidewalls 307 are formed and (2) upper surfaces of source/drain layers 309 located in the pFET active region laterally outside of gate sidewalls 307).

See also, e.g., Akasaka077 ¶ [0007], ¶¶ [0072]-[0074], ¶¶ [0084]-[0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[k] the first and second metal films are made of different metal materials,

Akasaka077 discloses this feature. For example, conductive film 316a is made of a material with a metallic band structure suitable for a pFET (e.g., titanium nitride (TiN)), conductive film 319 is made of a material with a metallic band structure suitable for an nFET, and a conductive film 320 is made of tungsten (W), for example. *See, e.g.,* the following:

“The conductive film 316 is disposed to control the work function of the gate electrode of the p-type MISFET. Accordingly, the type of the material of the conductive film 316 should be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p-poly crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element, such as Ni, Pd, Pt, Co., Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p-poly crystalline silicon. . . . In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316.”

Akasaka077 ¶¶ [0076]-[0077].

“The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n-poly crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-Iva element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n-poly-crystalline silicon. . . .

“Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth.”

Akasaka077 ¶¶ [0084]-[0086].

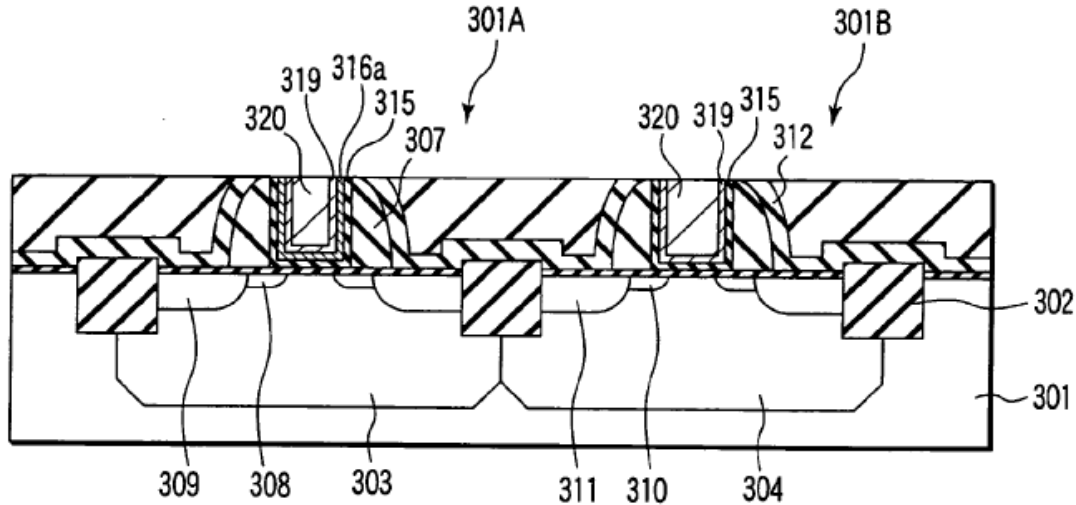


FIG. 26

Akasaka077, FIG. 26 (showing conductive films 316a, 319, and 320 in the final structure).

See also, e.g., Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[l] the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,

Akasaka077 discloses this feature. For example, silicon nitride film 312 in the second embodiment is planarized to the upper surfaces of the gate electrodes in pFET region 301A and nFET region 301B, thereby removing silicon nitride film 312 from the upper surfaces of both gate electrodes. See, e.g., the following:

"The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312."

Akasaka077 ¶ [0073].

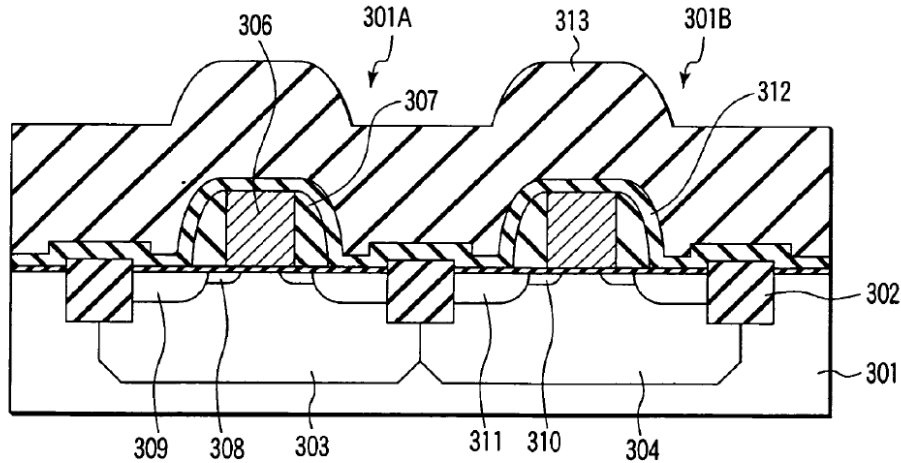


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of silicon nitride film 312).

“Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.”

Akasaka077 ¶ [0074].

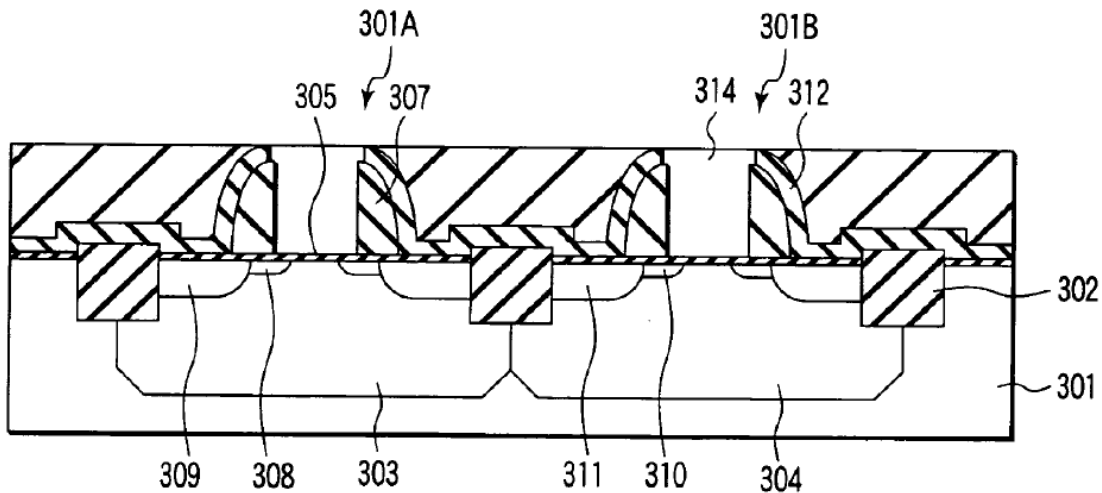


FIG. 18

Akasaka077, FIG. 18 (showing silicon nitride film 312 after CMP planarization and removal of silicon nitride film 312 from the upper surfaces of the nFET and pFET dummy gate electrodes).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077, ¶ [0087].

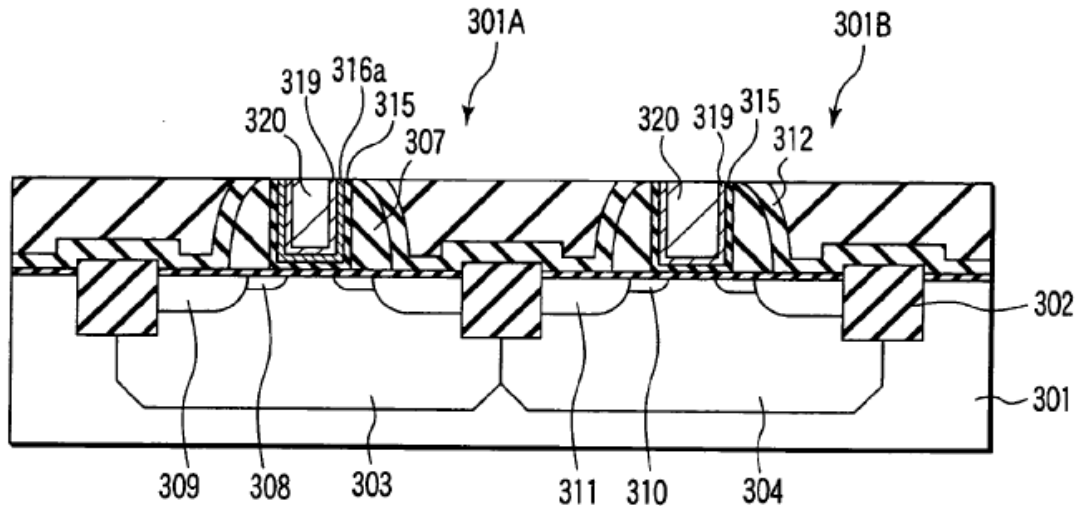


FIG. 26

Akasaka077, FIG. 26 (showing that silicon nitride film 312 does not remain on any upper surfaces of the gate electrodes in the final structure).

See also, e.g., Akasaka077 ¶¶ [0072]-[0074], ¶ [0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

25[m] the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

Akasaka077 discloses this feature. For example, Akasaka077 discloses silicon nitride film 312. See, e.g., the following:

“The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.”

Akasaka077 ¶ [0073].

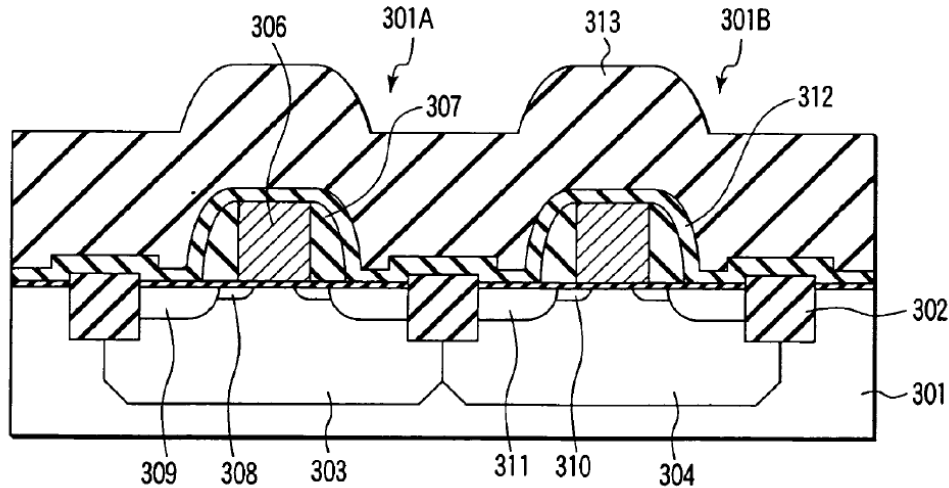


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of silicon nitride film 312).

“Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.”

Akasaka077 ¶ [0074].

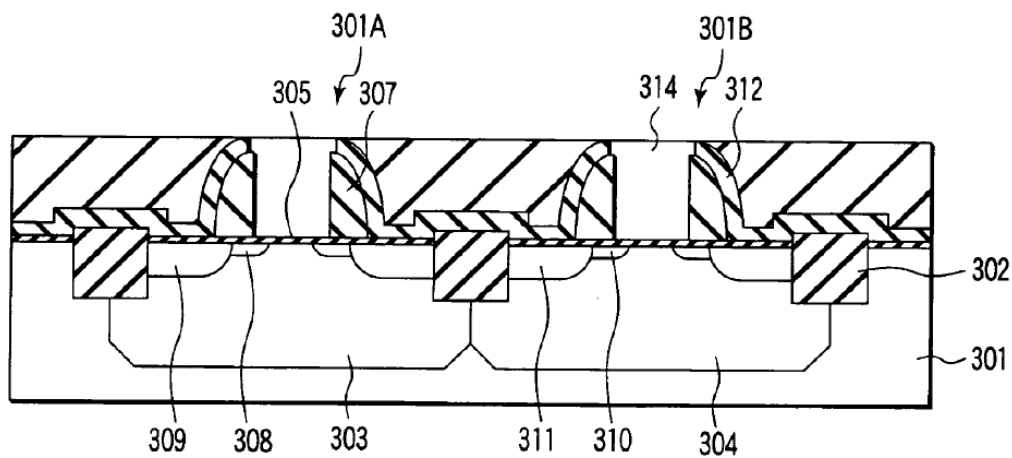


FIG. 18

Akasaka077, FIG. 18 (showing silicon nitride film 312 after CMP planarization and removal of silicon nitride film 312 from the upper surfaces of the nFET and pFET dummy gate electrodes).

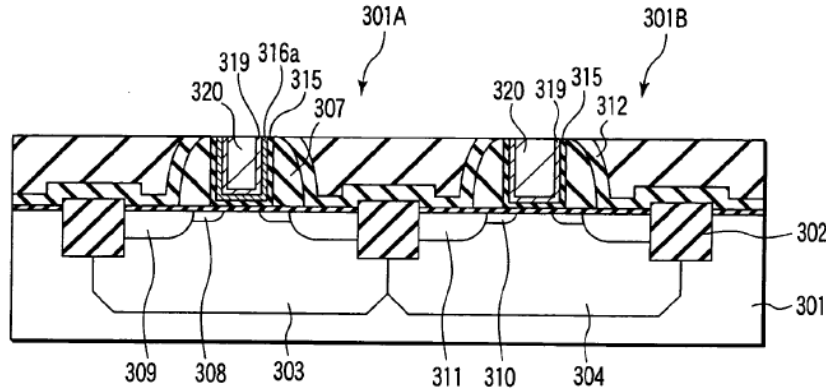


FIG. 26

Akasaka077, FIG. 26 (showing silicon nitride film 312 in the final structure).

See also, e.g., Akasaka077 ¶ [0007], ¶¶ [0072]-[0074], ¶¶ [0084]-[0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

26[a] The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.

Akasaka077 discloses this feature. In the second embodiment, conductive film 316a is about 5 nm thick and preferably about 1-2 nm thick; conductive film 319 is about 1-2 nm thick; and conductive film 320 is about 40-50 nm thick. See, e.g., the following:

"The film thickness of the conductive film 316 is preferably set to be about 5 nm, but it may be set at a very small value of about 1 to 2 nm."

Akasaka077 ¶ [0077].

"The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm. . . .

"The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film."

Akasaka077 ¶¶ [0085]-[0086].



See, e.g., Akasaka077 ¶ [0046], ¶¶ [0053]-[0054], ¶ [0077], ¶¶ [0085]-[0086], FIGS. 19-26.

27[a] The semiconductor device of claim 25, wherein the first and second metal films have different work functions.

See also, e.g., the following:

“Specifically, in order to decrease the threshold voltage of the p-type MISFET, the material is preferably selected to have a work function close to that of p-poly crystalline silicon, such as a work function of 4.8 to 5.3 eV. For example, in the case of a pure metal, a Group-VIII element,

such as Ni, Pd, Pt, Co., Rh, or Ru, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of p-poly crystalline silicon. . . . In this embodiment, a titanium nitride (TiN) film having a work function of about 4.8 eV is used as the conductive film 316.”

Akasaka077 ¶¶ [0076]-[0077].

“The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n-poly crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-Iva element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n-poly-crystalline silicon. . . .

“Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth.”

Akasaka077 ¶¶ [0084]-[0086].

See also, e.g., Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

28[a] The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

Akasaka077 discloses this feature. For example, silicon nitride film 312 has a thickness smaller than that of the gate electrode in nFET region 301B. *See, e.g.*, the following:

“Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312.”

Akasaka077 ¶ [0073].

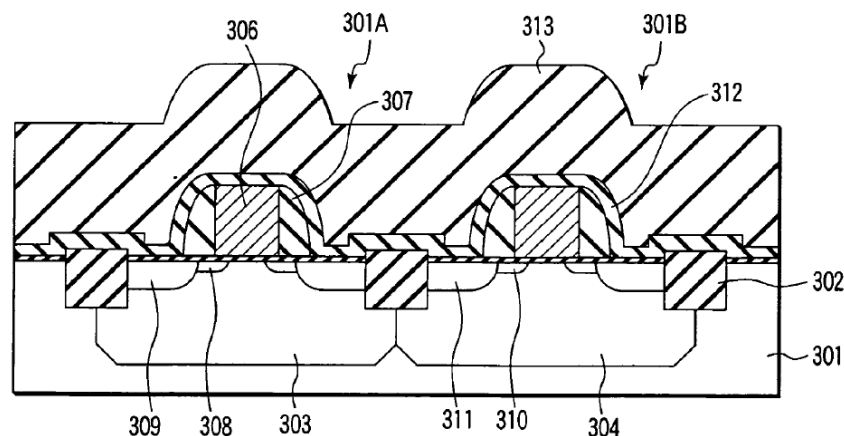


FIG. 16

Akasaka077, FIG. 16 (showing the initial formation of silicon nitride film 312).

“Then, as shown in FIG. 17, the inter-level insulating film 313 is polished from above by a CMP (Chemical Mechanical Polishing) method. This step is arranged to expose the upper surface of the dummy gate electrode 306 or the upper surface of the silicon nitride film 312 deposited on the dummy gate electrode 306. Then, as shown in FIG. 18, the exposed silicon nitride film 312 and the dummy gate electrodes are selectively removed to form recess portions 314. Then, as shown in FIG. 19, the portions of the dummy gate dielectric film 305 exposed at the bottom of the recess portions 314 are removed.”

Akasaka077 ¶ [0074].

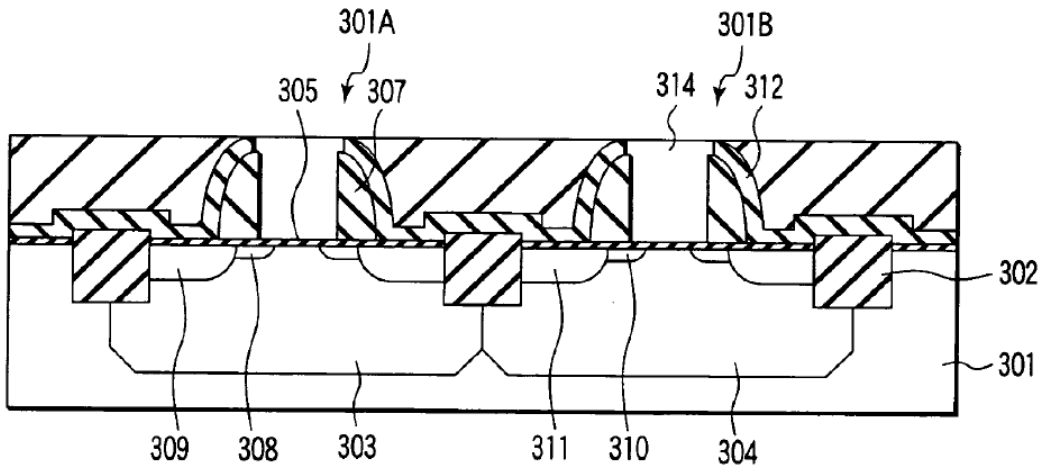


FIG. 18

Akasaka077, FIG. 18 (showing silicon nitride film 312 after CMP planarization and removal of silicon nitride film 312 from the upper surfaces of the nFET and pFET dummy gate electrodes).

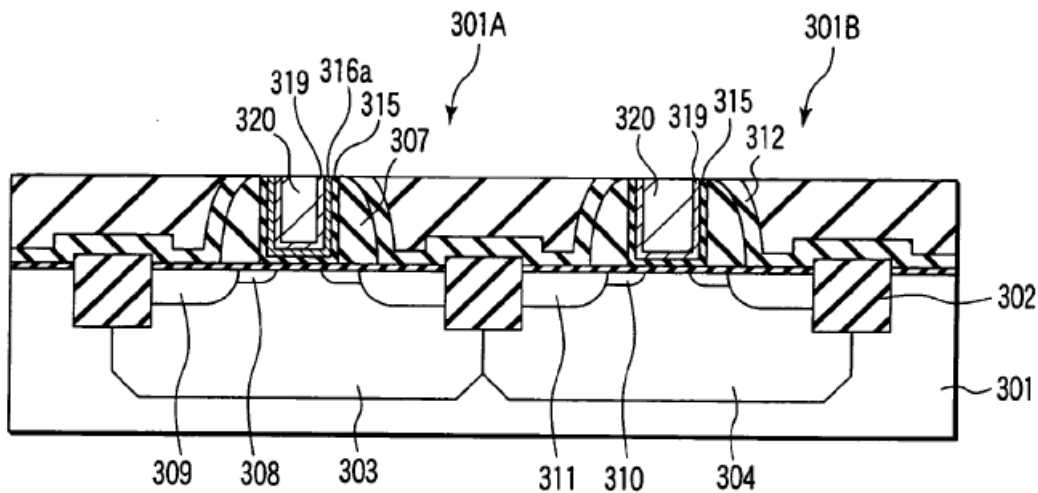


FIG. 26

Akasaka077, FIG. 26 (showing that silicon nitride film 312 is thinner than the gate electrode in nFET region 301B).

See also, e.g., Akasaka077 ¶¶ [0072]-[0074], ¶ [0087], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

29[a] The semiconductor device of claim 25, wherein the conductive film is made of the second metal film.

Akasaka077 discloses this feature. For example, the second metal film and the conductive film are both made from the same physical layer(s)—conductive film 319 and/or conductive film 320. *See, e.g.*, the following:

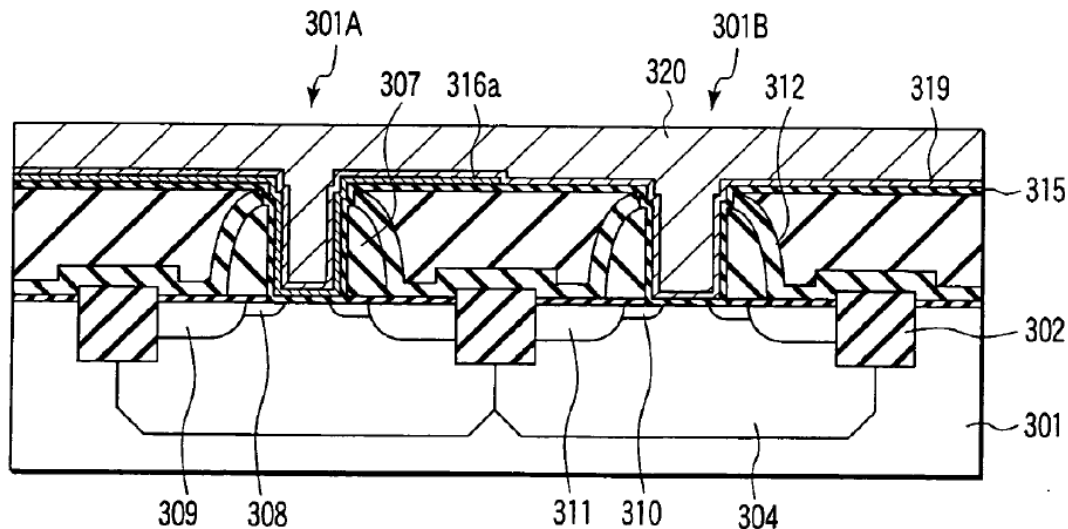


FIG. 25

Akasaka077, FIG. 25 (showing the formation of conductive films 319 and 320 before polishing / planarization by chemical-mechanical polishing (CMP)).

“Then, a conductive film 319 to define the bottom portion of the gate electrode of the n-type MISFET is formed all over the substrate. The conductive film 319 is disposed to control the work function of the gate electrode of the n-type MISFET. Accordingly, the type of the material of the conductive film 319 should also be determined in consideration of its work function.

“Specifically, in order to decrease the threshold voltage of the n-type MISFET, the material is preferably selected to have a work function close to that of n-poly crystalline silicon, such as a work function of 3.9 to 4.2 eV. For example, in the case of a pure metal, a Group-Iva element, such as Ti, Zr, or Hf, a Group-Va element, such as V, Nb, or Ta, or a Group-VIa element, such as Cr, Mo, or W, is preferably used. Alternatively, a metal silicide, a metal nitride, or another compound may be used, as long as it has a metallic band structure with a work function close to that of n-poly-crystalline silicon. The film thickness of the conductive film 319 may be set at a very small value of about 1 to 2 nm.

“Then, a conductive film 320 to decrease the resistance of the gate electrode is deposited all over the substrate. The film thickness of the conductive film 320 is preferably set to provide a sheet resistance of about $5\Omega/\square$ or less, such as about 40 to 50 nm in the case of W being used. In this embodiment, the conductive film 319 and conductive film 320 are made of different conductive materials. However, where the material selected for the conductive film 319 has a

resistivity almost equal to or less than that required for the conductive film 320 and suitable for the subsequent steps, the conductive film 319 and conductive film 320 are made of one integral film. The conductive film 316 for the gate electrode of the p-type MISFET and the conductive film 319 for the gate electrode of the n-type MISFET may be deposited in an order reverse to that of the embodiment, in consideration of their workability, reactivity, and so forth.”

Akasaka077 ¶¶ [0084]-[0086].

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077 ¶ [0087].

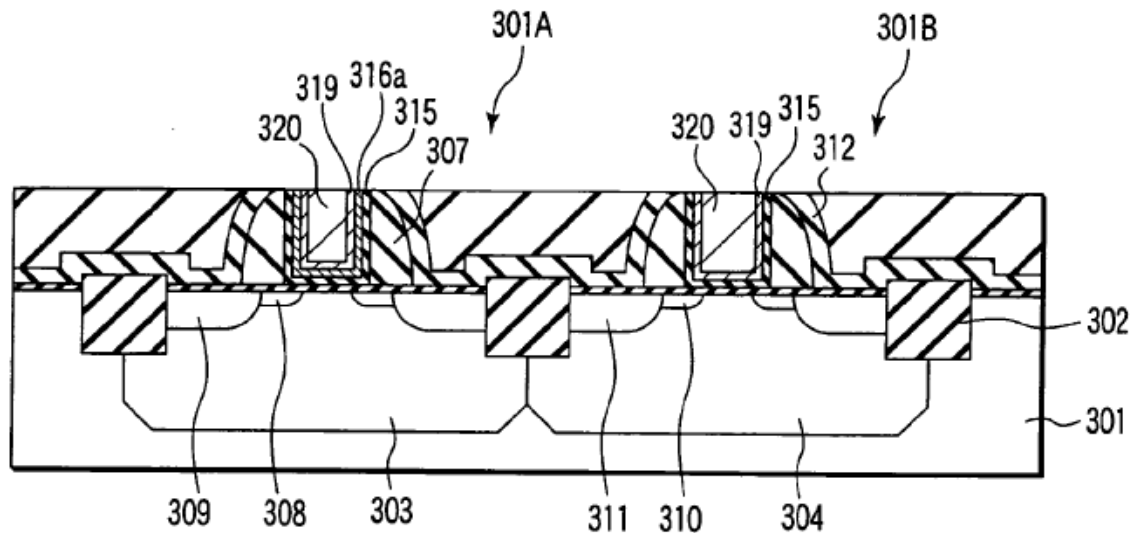


FIG. 26

Akasaka077, FIG. 26 (showing conductive films 319 and 320 in the final structure).

See also, e.g., Akasaka077 ¶¶ [0084]-[0088], FIGS. 25, 26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

31[a] The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.

Akasaka077 discloses this feature. For example, Akasaka077 discloses that gate dielectric (insulating) film 315 in pFET region 301A is patterned from the same physical layer as gate dielectric (insulating) film 315 in nFET region 301B. *See, e.g., the following:*

“Then, a gate dielectric (insulating) film 315 is deposited all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO_2 , HfSi_xO_y , HfAl_xO_y , or SiO_2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.”

Akasaka077 ¶ [0075].

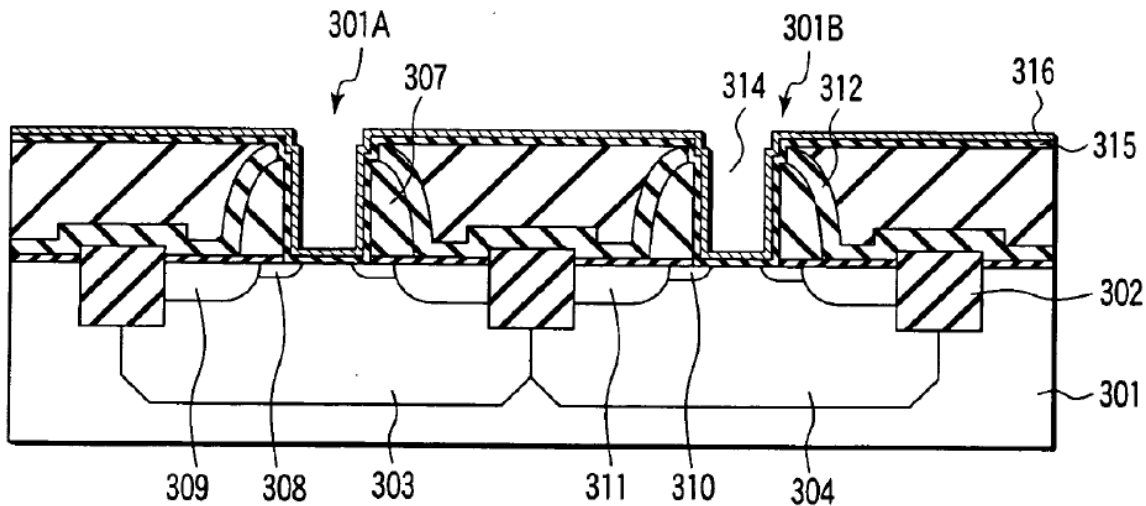


FIG. 19

Akasaka077, FIG. 19 (showing the initial formation of gate dielectric (insulating) film 315).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077, ¶ [0087].

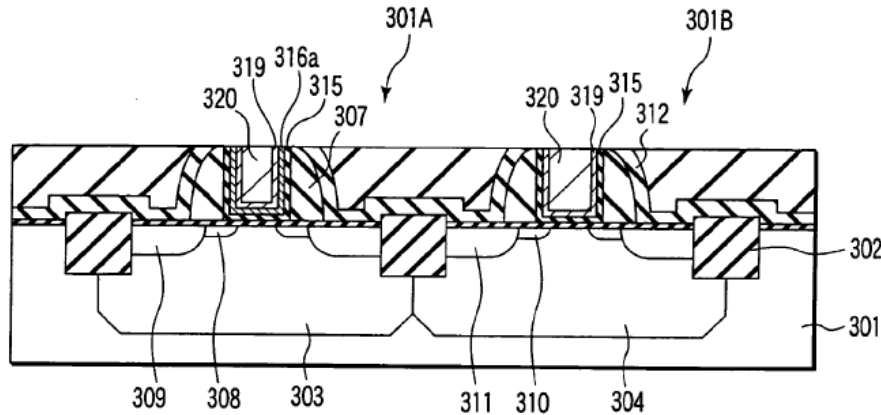


FIG. 26

Akasaka077, FIG. 26 (showing gate dielectric (insulating) film 315 in the final structure).

See also, e.g., Akasaka077 ¶ [0003], ¶ [0006], ¶ [0075], ¶¶ [0082]-[0083], ¶¶ [0087]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

34[a] The semiconductor device of claim 25, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

Akasaka077 discloses this feature. See, e.g., the following:

"Then, as shown in FIG. 16, a starting structure including a dummy gate electrode made of, e.g., polycrystalline silicon is formed by conventional techniques for forming transistors. In this starting structure, the source/drain layers 309 and extensions 308 of the p-type MISFET are formed in the n-type well 303 within the first area 301A. Similarly, the source/drain layers 311 and extensions 310 of the n-type MISFET are formed in the p-type well 304 within the second area 301B. Further, a dummy gate electrode 306 made of poly-crystalline silicon is disposed through a dummy gate dielectric (insulating) film 305 formed of a silicon oxide film, at each of predetermined positions on the substrate within the first and second areas 301A and 301 B. A gate sidewall 307 formed of an insulating film, such as a silicon nitride film is disposed on the side surface of each dummy gate electrode 306. The dummy gate electrode 306 and gate sidewall 307 are covered with a silicon nitride film 312 serving as an etching stopper. Further, an inter-level insulating film 313 is disposed on the silicon nitride film 312."

Akasaka077 ¶ [0073].

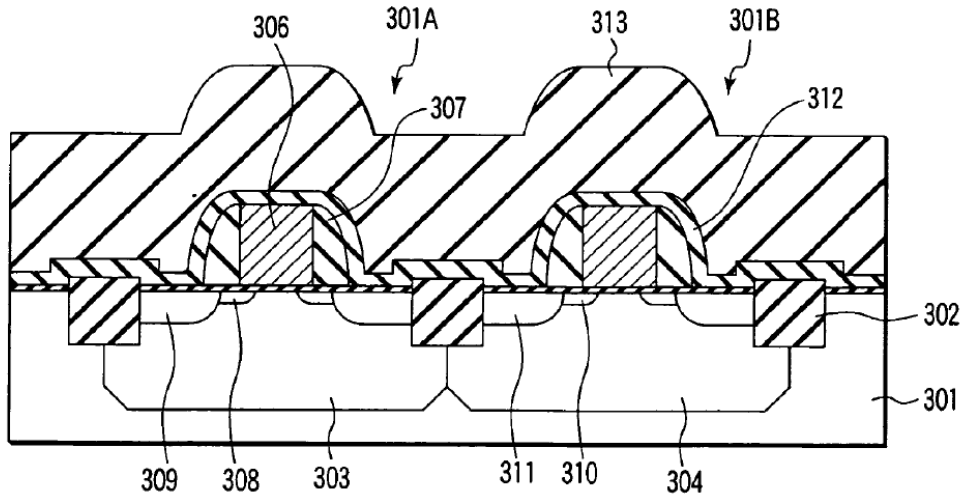


FIG. 16

Akasaka077, FIG. 16 (showing initial formation of source/drain regions 308/309 and 310/311).

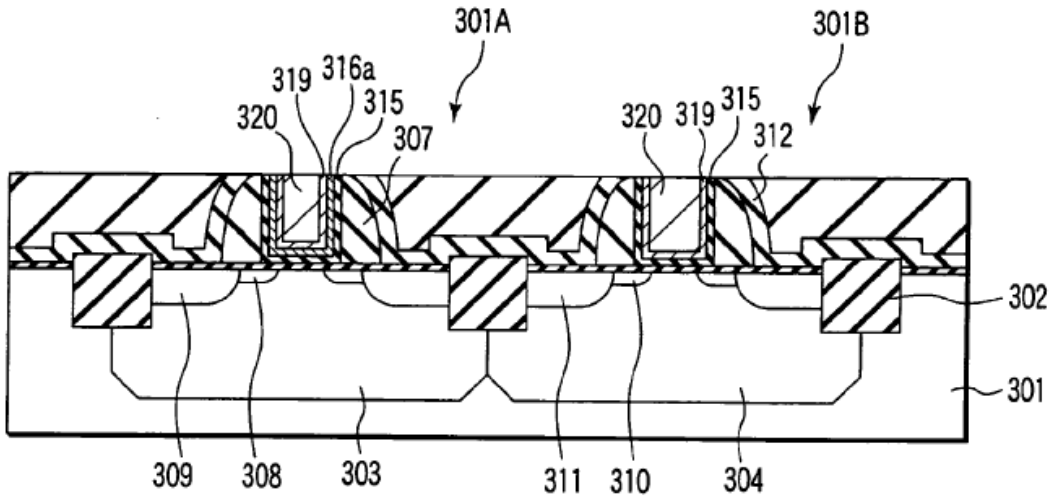


FIG. 26

Akasaka077, FIG. 26 (showing source/drain regions 308/309 and 310/311 in the final structure).

See also, e.g., Akasaka077 ¶ [0005], ¶ [0007], ¶¶ [0057]-[0058], ¶ [0073], FIGS. 16-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

35[a] The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

Akasaka077 discloses this feature. For example, gate dielectric (insulating) film 315 may be made of hafnium oxide or hafnium silicon oxide. Hafnium oxide and hafnium silicon oxynitride have a relative dielectric constant of 10 or more. *See, e.g.*, Akasaka939 ¶ [0004] (explaining “HfO₂, HfSiO_x . . . and oxynitrides thereof” have “dielectricity of more than ten”). *See, e.g.*, the following:

“Then, a gate dielectric (insulating) film 315 is deposited all over the substrate to cover the inner surface of the recess portions 314. The gate dielectric film 315 may be preferably made of a film of HfO_2 , HfSi_xO_y , HfAl_xO_y , or SiO_2 doped with nitrogen. The film thickness of the gate dielectric film 315 is preferably set to agree with an effective film thickness (EOT) of 1.5 nm or less, to manufacture a MISFET having a gate length of 100 nm or less. EOT is expressed by a value converted into the thickness of a silicon oxide film having an equivalent gate capacity.”

Akasaka077 ¶ [0075].

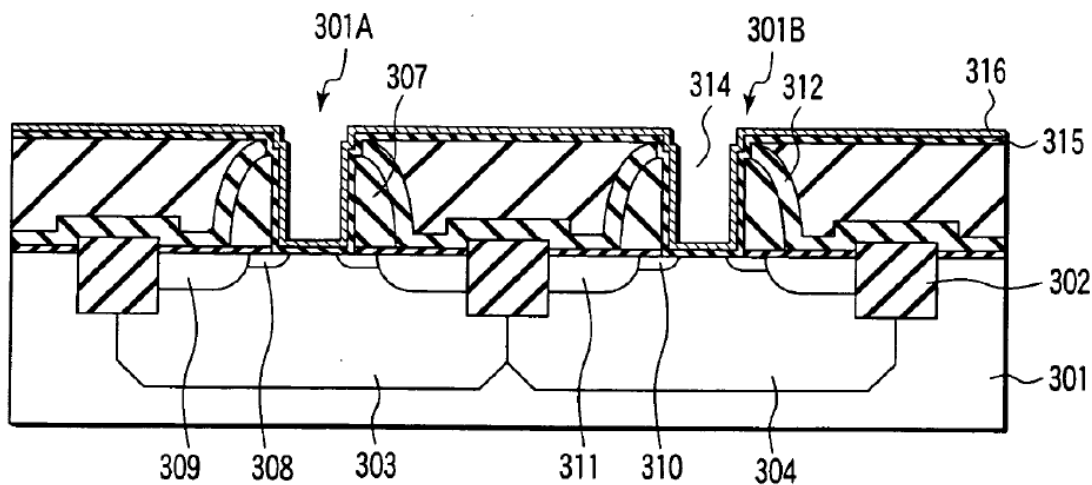


FIG. 19

Akasaka077, FIG. 19 (showing the initial formation of gate dielectric (insulating) film 315).

“Then, as shown in FIG. 26, a CMP method or the like is used to remove those portions of the insulating film 315 and conductive films 316, 319, and 320 which are deposited outside the recess portions 314. Thereafter, inter level insulating films, interconnections, and so forth are formed by conventional techniques to complete the MISFETS.”

Akasaka077, ¶ [0087].

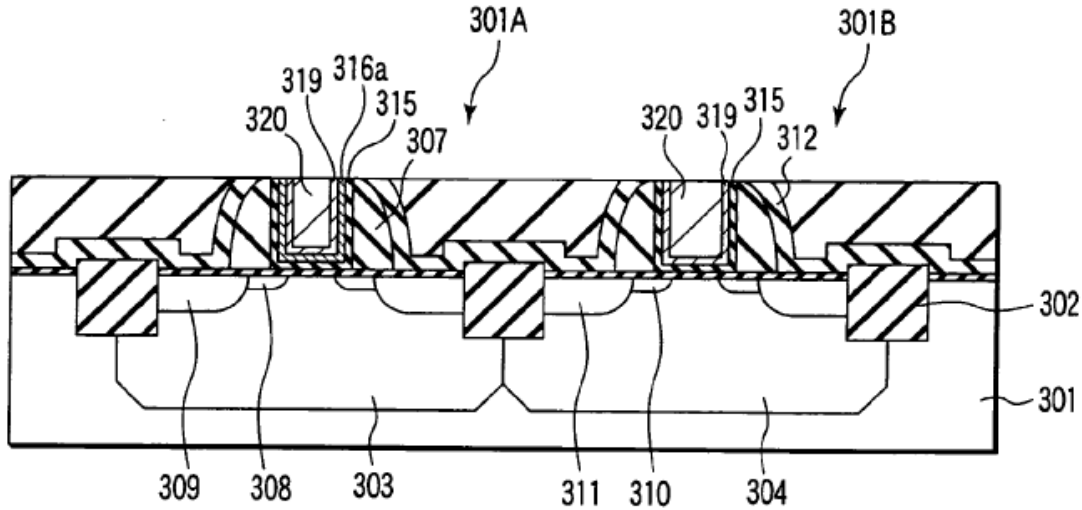


FIG. 26

Akasaka077, FIG. 26 (showing gate dielectric (insulating) film 315 in the final structure).

See also, e.g., Akasaka077 ¶ [0006], ¶ [0044], ¶ [0051], ¶ [0075], ¶¶ [0087]-[0088], FIGS. 19-26.

To the extent that Akasaka077 is found not to disclose this feature, it would have been obvious based on the disclosures of Akasaka077 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 and 686-03 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.