

Exhibit 686-04: Aoyama950

U.S. Patent Appl. Pub. No. 2007/0215950 A1 to Aoyama (“Aoyama950”) was filed on March 20, 2006, and published on September 20, 2007. Accordingly, Aoyama950 constitutes prior art to U.S. Patent No. 8,198,686 (the “’686 patent”) under at least pre-AIA 35 U.S.C. §§ 102(a) and (e).

Aoyama950, including any material incorporated by reference into Aoyama950, anticipates claims 25-28, 31, and 35 (the “asserted claims”) of the ’686 patent under pre-AIA 35 U.S.C. §§ 102(a) and (e).

To the extent any limitation is found not to be expressly or inherently disclosed in Aoyama950, such a limitation would have been obvious either based on Aoyama950 alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 686-01 through 686-03 and 686-05 through 686-09, because the ’686 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

Any disclosures identified for each limitation of the ’686 patent in the aforementioned Exhibits may be combined with the disclosures of Aoyama950 identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.¹

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

¹ Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

Exemplary Disclosures

25[pre] A semiconductor device, comprising:

Defendant does not concede that the preamble is limiting. To the extent it is limiting, Aoyama950 discloses the preamble. For example, Aoyama950 discloses a semiconductor device according to a third embodiment. *See, e.g.*, the following:

“The present invention relates to a semiconductor device and a manufacturing method thereof, for example, to a semiconductor device which includes a PMOSFET and an NMOSFET which are constituted by high-permittivity gate dielectric films (high-k gate dielectric films) and metal gate electrodes, and a manufacturing method thereof.”

Aoyama950 ¶ [0003].

“FIG. 5 is a side sectional view showing a semiconductor device according to a third embodiment. The semiconductor device in FIG. 5 includes a PMOSFET which is a specific example of a P-type FET and an NMOSFET which is a specific example of an N-type FET. The semiconductor device in FIG. 5 includes a CMOSFET which is constituted by the PMOSFET and the NMOSFET.”

Aoyama950 ¶ [0097].

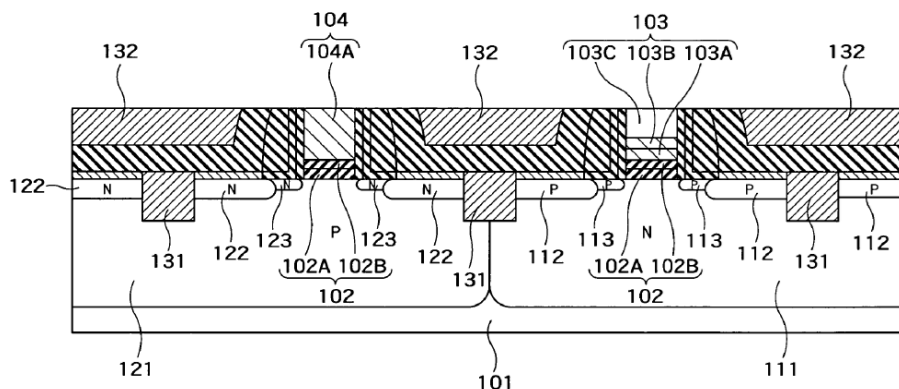


FIG. 5

Aoyama950, FIG. 5.

See also, e.g., Aoyama950, Title, Abstract, ¶¶ [0002]-[0031], ¶¶ [0036]-[0037], ¶¶ [0097]-[0122], FIGS. 5, 6A-6Q.

To the extent that Aoyama950 is found not to disclose the preamble, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

25[a] a first MIS transistor; and

Aoyama950 discloses this feature. For example, Aoyama950 discloses an NMOSFET formed in NMOSFET region 106 of the third embodiment. *See, e.g., the following:*

“With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOS FET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.”

Aoyama950 ¶ [106].

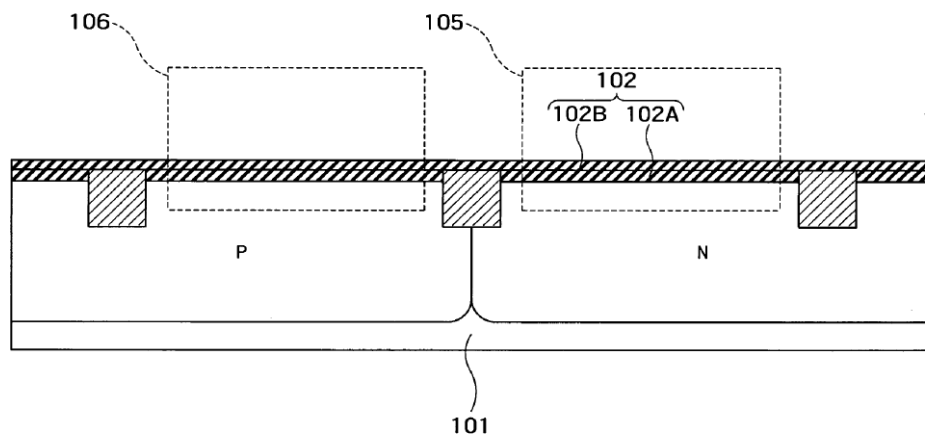


FIG. 6D

Aoyama950, FIG. 6D.

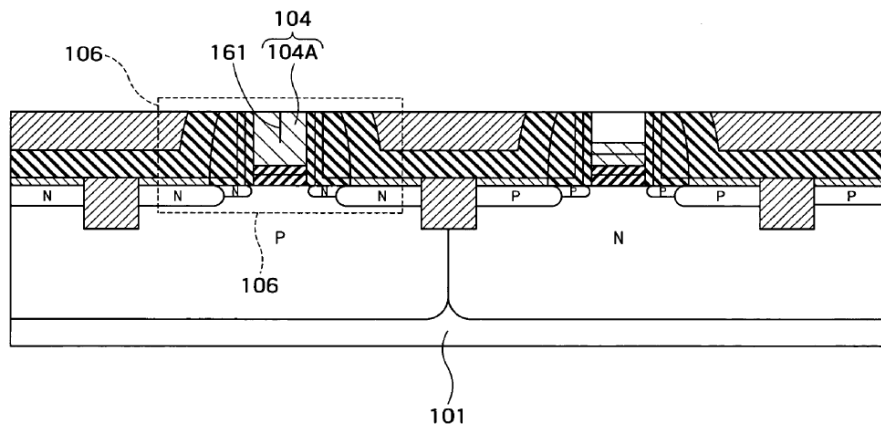


FIG. 6Q

Aoyama950, FIG. 6Q.

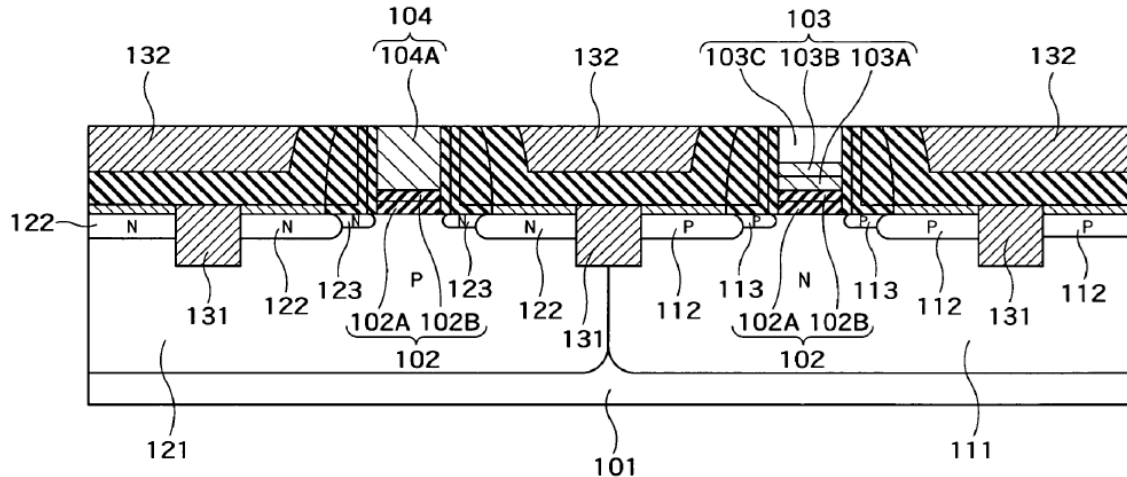


FIG. 5

Aoyama950, FIG. 5 (depicting the NMOSFET on the left-hand side).

See also, e.g., Aoyama950, Abstract, ¶¶ [0003]-[0005], ¶¶ [0007]-[0010], ¶¶ [0106]-[0119], FIGS. 5, 6D-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[b] a second MIS transistor, wherein:

Aoyama950 discloses this feature. For example, Aoyama950 discloses a PMOSFET formed in PMOSFET region 105 of the third embodiment. See, e.g., the following:

"With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOS FET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region."

Aoyama950 ¶ [0106].

Aoyama950, FIG. 6D.



See also, e.g., Aoyama950, Abstract, ¶¶ [0003]-[0005], ¶¶ [0007]-[0010], ¶¶ [0106]-[0119], FIGS. 5, 6D-6Q.

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25[c] the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate;

Aoyama950 discloses this feature. For example, Aoyama950 discloses gate insulating film 102 formed on NMOSFET region 106 of the third embodiment. *See, e.g.*, the following:

“The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film.”

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.”

Aoyama950 ¶ [0106].

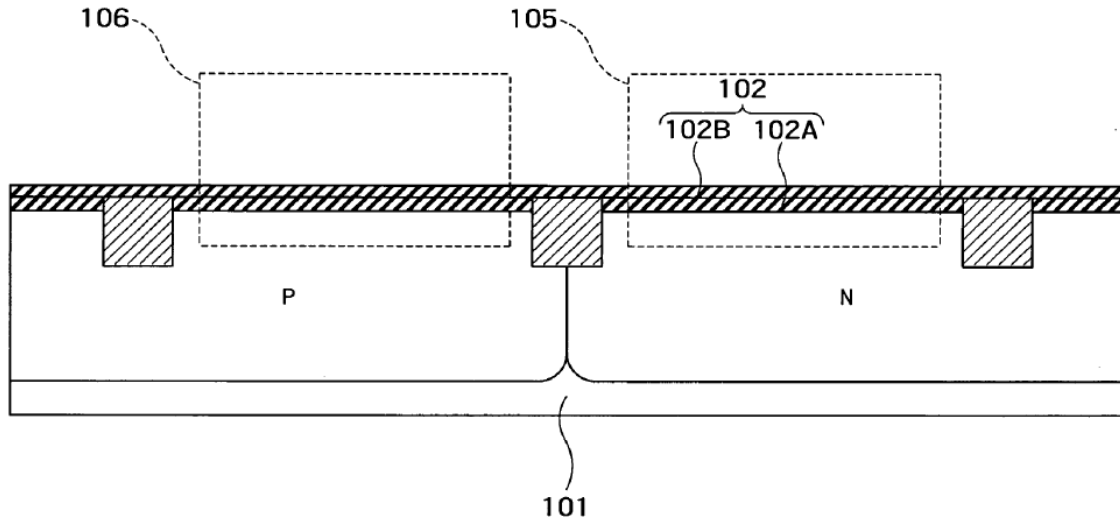


FIG. 6D

Aoyama950, FIG. 6D (depicting formation of gate insulating film 102 before patterning).

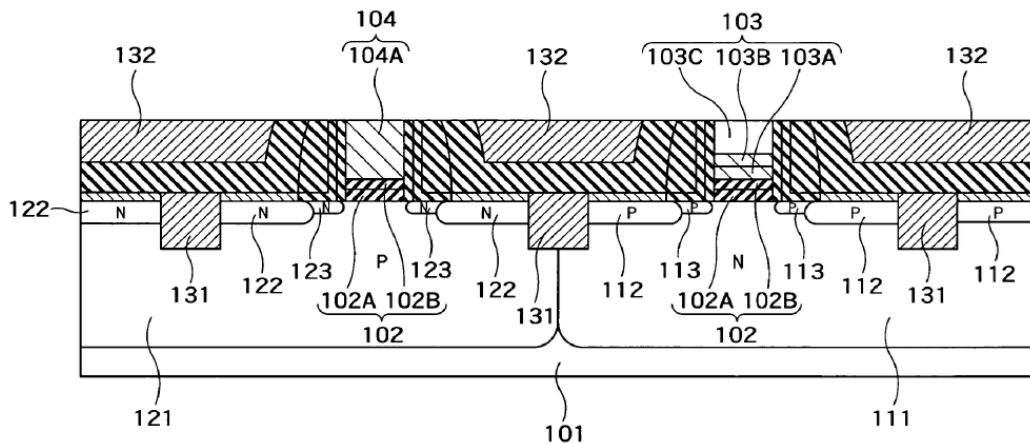


FIG. 5

Aoyama950, FIG. 5 (depicting gate insulating film 102, including on the left-hand side where the NMOSFET is located).

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[d] [the first MIS transistor includes: . . .] a first gate electrode including a second metal film formed on the first gate insulating film;

Aoyama950 discloses this feature. For example, Aoyama950 discloses gate electrode 104, which includes conductive layer 104A made of conductive metal, formed on gate insulating film 102 of the NMOSFET of the third embodiment. *See, e.g., the following:*

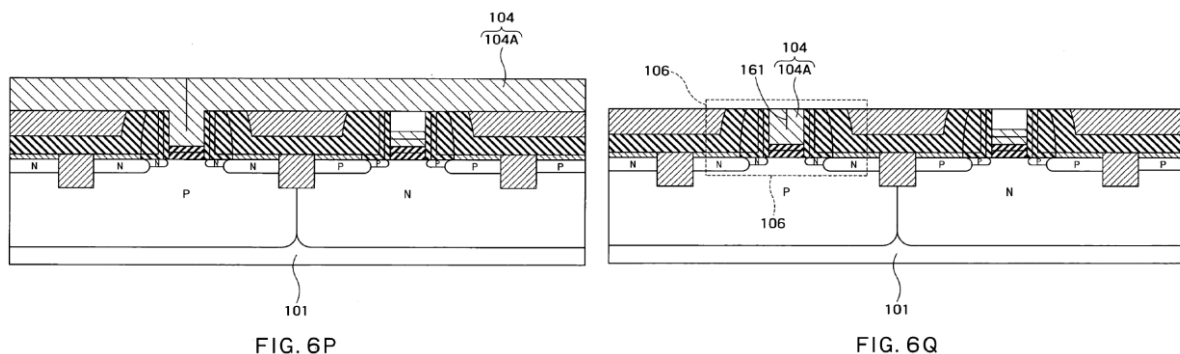
“The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. . . . The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. . . . The gate electrode 104 for the NMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 104 for the NMOSFET in this embodiment includes one electrode-constituting layer: a third conductive layer 104A which is made of conductive metal.”

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6P, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is formed over the entire surface by CVD. Examples of the conductive metal include TaCN, which is formed using trisdimethylamino mono-t-amyliminotantalum and monomethylamine.

“Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.”

Aoyama950 ¶¶ [0118]-[0119].



Aoyama950, FIGS. 6P, 6Q (showing formation of gate electrode 104).

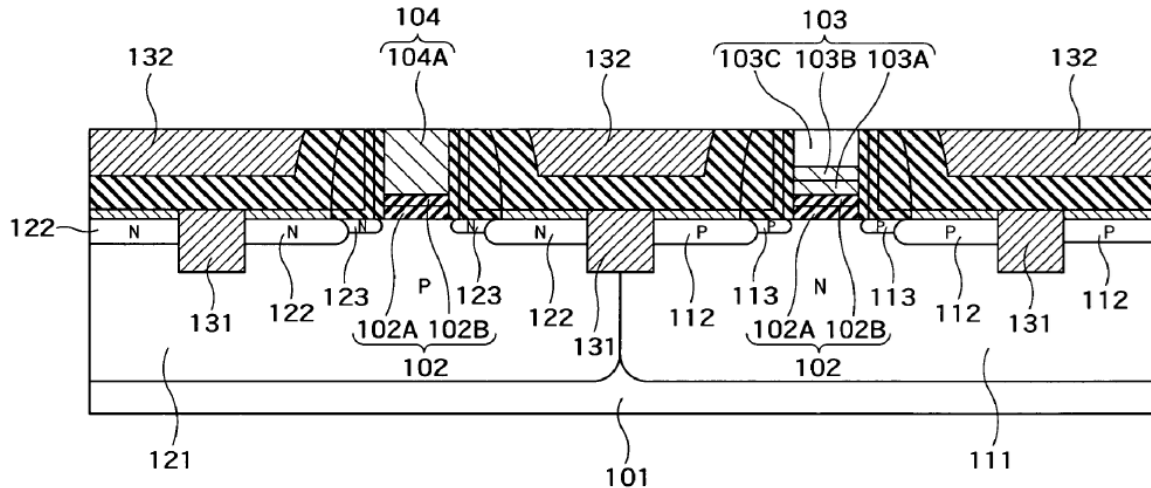


FIG. 5

Aoyama950, FIG. 5 (depicting gate electrode 104, including conductive layer 104A).

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0118]-[0119], FIGS. 5, 6P-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[e] [the first MIS transistor includes: . . .] first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and

Aoyama950 discloses this feature. For example, Aoyama950 discloses side wall spacers 142, which are made of silicon oxide (an insulator), formed on side surfaces of gate electrode 104 of the third embodiment. Additionally, offset spacers 141 and/or side wall spacers 143 may be considered part of the claimed first sidewall spacers. See, e.g., the following:

"Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or AS are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000°C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each

of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.”

Aoyama950 ¶ [0111].

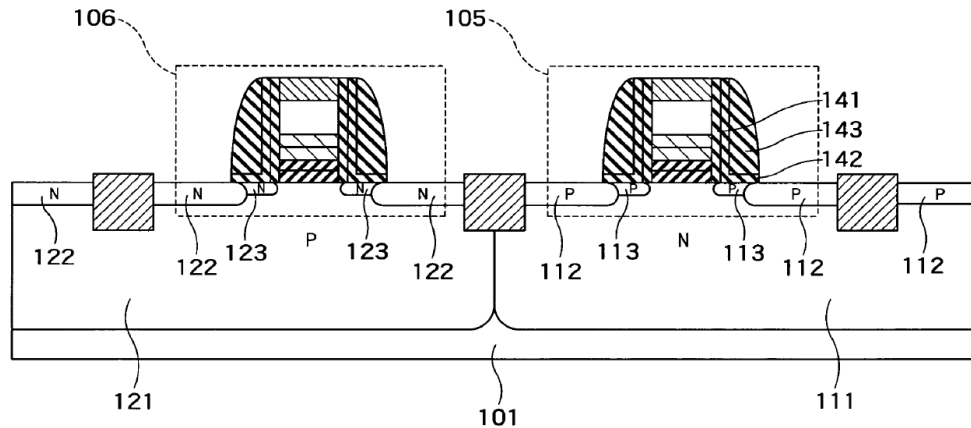


FIG. 6I

Aoyama950, FIG. 6I (depicting offset spacers 141 and side wall spacers 142 and 143 formed on side surfaces of the dummy gate electrode structure for the NMOSFET, on the left-hand side).

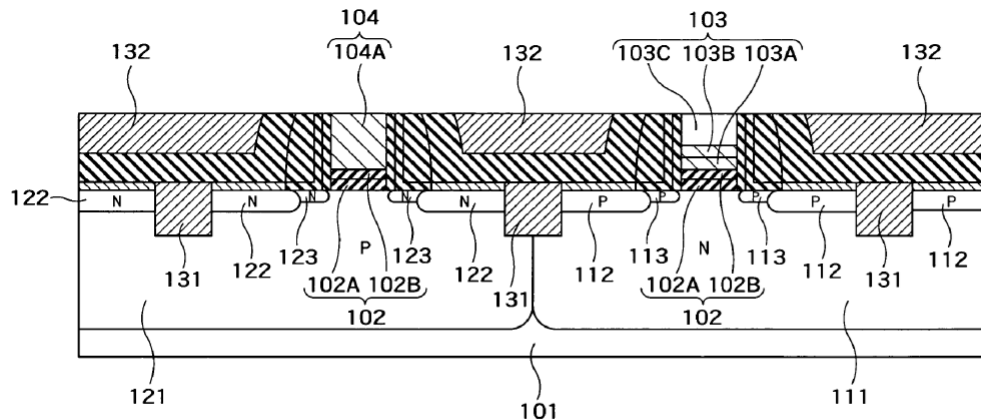


FIG. 5

Aoyama950, FIG. 5 (depicting offset spacers 141 and side wall spacers 142 and 143 formed on side surfaces of gate electrode 104).

See also, e.g., Aoyama950, ¶ [0054], ¶ [0086], ¶ [0111], FIGS. 5, 6I-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[f] [the first MIS transistor includes: . . .] a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,

Aoyama950 discloses this feature. For example, Aoyama950 discloses etch stopper film 145 in the third embodiment, which is made of silicon nitride and extends over (1) the side surfaces of gate electrode 104 where offset spacer 141 and side wall spacers 142 and 143 are formed and (2) upper surfaces of source/drain layer 122 located in the NMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143. *See, e.g.,* the following:

“Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the NMOSFET, a well diffusion layer 121 for the NMOSFET, a source/drain diffusion layer 122 for the NMOSFET, and an extension diffusion layer 123 for the NMOSFET.”

Aoyama950 ¶ [0100].

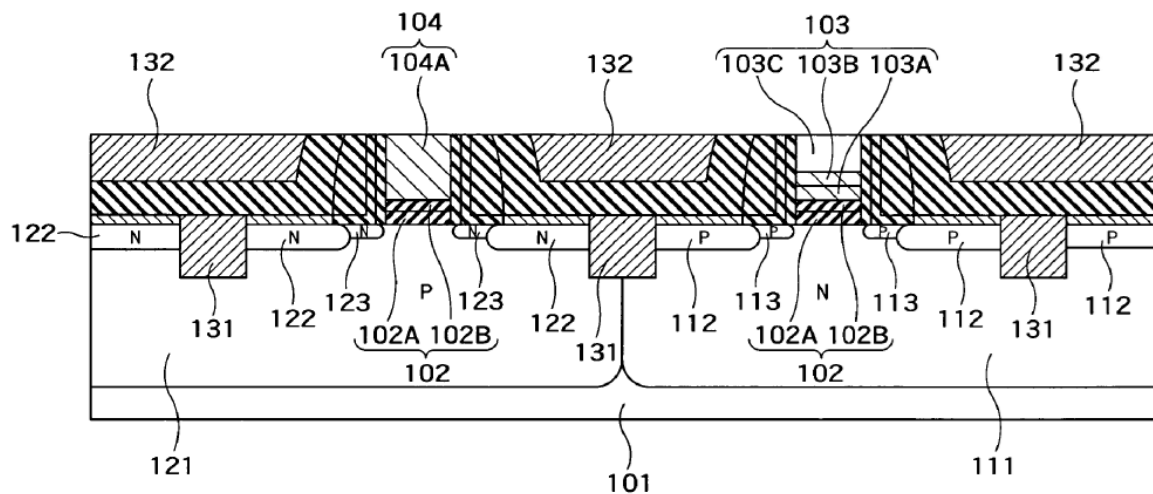


FIG. 5

Aoyama950, FIG. 5 (depicting etch stopper film 145 extending over (1) the side surfaces of gate electrode 104 where offset spacer 141 and side wall spacers 142 and 143 are formed and (2) upper surfaces of source/drain layer 122 located in the NMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143).

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“Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or AS are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000°C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.”

Aoyama950 ¶ [0111].

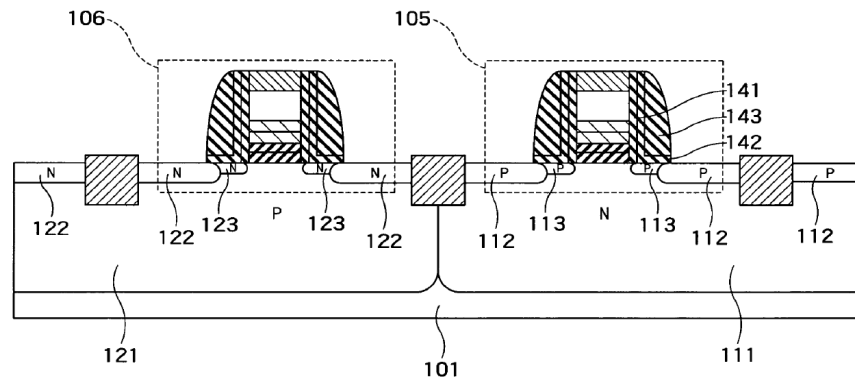


FIG. 6I

Aoyama950, FIG. 6I (depicting the formation of offset spacers 141, side wall spacers 142 and 143, and source/drain layers 122).

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

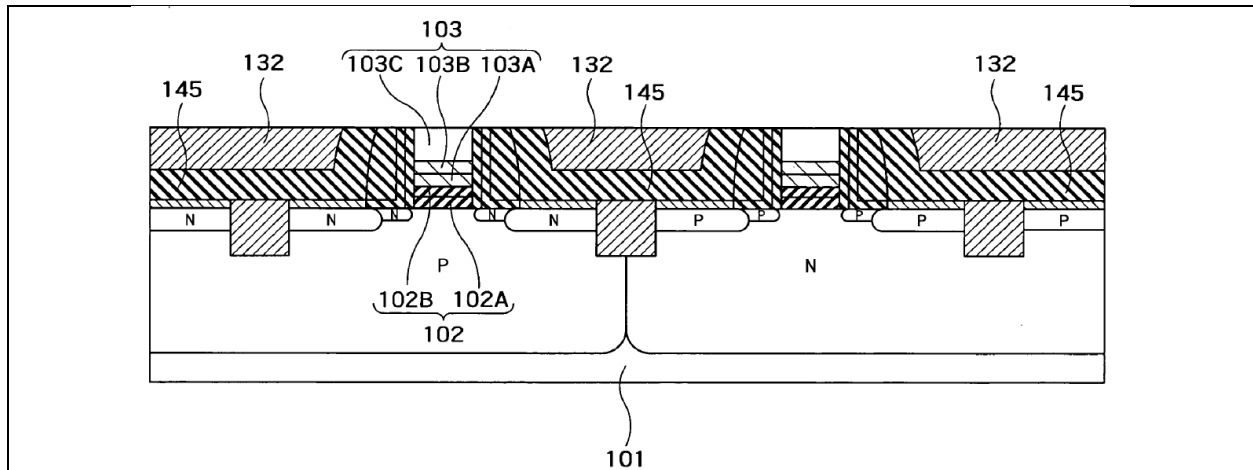


FIG. 6K

Aoyama950, FIG. 6K (depicting the formation of etch stopper film 145 extending over (1) the side surfaces of dummy gate electrode structure 103 for the NMOSFET, where offset spacer 141 and side wall spacers 142 and 143 are formed, and (2) upper surfaces of source/drain layer 122 located in the NMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143).

See also, e.g., Aoyama950, ¶ [0054], ¶ [0056], ¶ [0086], ¶ [0088], ¶¶ [0100]-[0101], ¶¶ [0111]-[0113], FIGS. 5, 6I-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[g] the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate;

Aoyama950 discloses this feature. For example, Aoyama950 discloses gate insulating film 102 formed on PMOSFET region 105 of the third embodiment. See, e.g., the following:

"The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film."

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.”

Aoyama950 ¶ [0106].

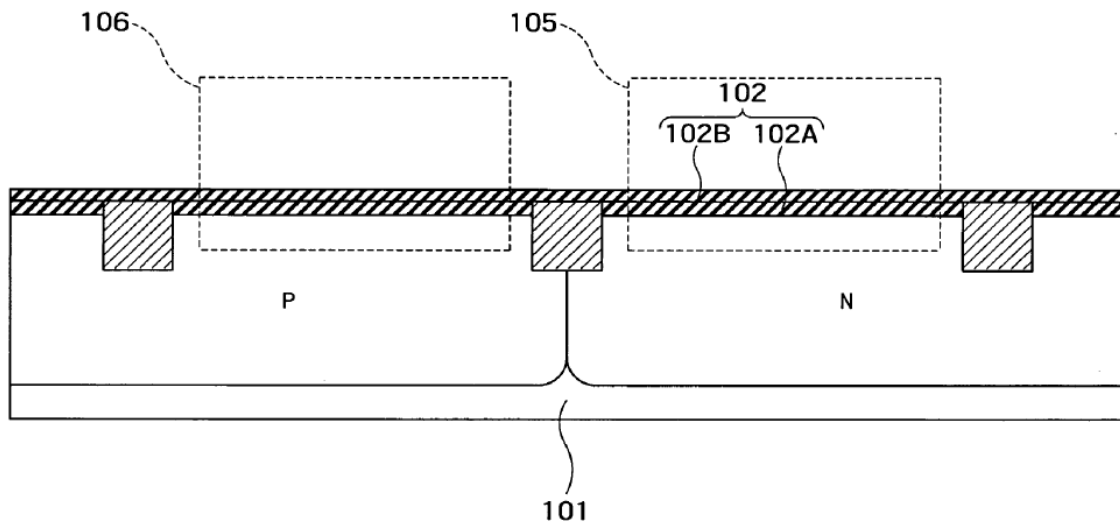


FIG. 6D

Aoyama950, FIG. 6D (depicting formation of gate insulating film 102 before patterning).

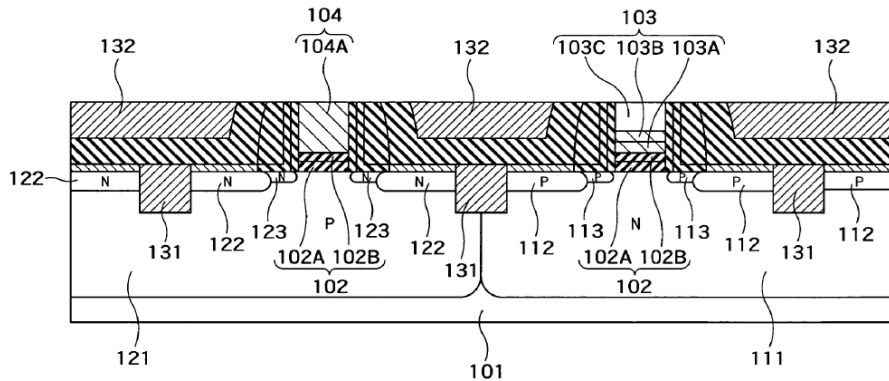


FIG. 5

Aoyama950, FIG. 5 (depicting gate insulating film 102, including on the right-hand side where the PMOSFET is located).

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[h] [the second MIS transistor includes: . . .] a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;

Aoyama950 discloses this feature. For example, Aoyama950 discloses gate electrode 103, which includes conductive layers 103A and 103B both made of conductive metal and a silicided semiconductor layer 103C, formed on gate insulating film 102 of the PMOSFET in the third embodiment. The claimed "first metal film" may be conductive layer 103A, and the "conductive film" may be conductive film 103B and/or part or all of silicided semiconductor layer 103C. Alternatively, the claimed "first metal film" may be conductive layer 103B, and the "conductive film" may be part or all of silicided semiconductor layer 103C. See, e.g., the following:

"The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. . . . The gate electrode 103 for the PMOSFET is a metal gate electrode, all or a part of which is made of conductive metal. The gate electrode 103 for the PMOSFET in this embodiment includes three electrode-constituting layers: a first conductive layer 103A which is made of conductive metal, a second conductive layer 103B which is made of conductive metal, and a semiconductor layer 103C which is made of semiconductor."

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.”

Aoyama950 ¶ [0107].

“Next, as shown in FIG. 6G, the W layer 103A, TiN layer 103B, and semiconductor layer 103C (non-diffusion layer 103Ca and diffusion layer 103Cb) are processed using a dielectric film 202 as a hard mask, the dielectric film 202 including a silicon oxide film or silicon nitride film. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate electrode 103 for the PMOSFET is formed in the PMOSFET region 105, and a dummy gate electrode (a gate electrode used as a dummy) 103 with the same configuration as that of the gate electrode 103 for the PMOSFET is formed in the NMOS FET region 106.”

Aoyama950 ¶ [0109].

“Next, as shown in FIG. 6L, a Ni (nickel) film (sacrificial film) 203 is formed over the entire surface. After that, the substrate 101 is subjected to annealing, thereby siliciding Ni in the Ni film 203. At this time, since the diffusion layer 103Cb contains P or As, the silicidation rate of the diffusion layer 103Cb becomes higher than that of the non-diffusion layer 103Ca. Accordingly, Ni monosilicide (NiSi) is formed in the non-diffusion layer 103Ca, and a Ni-rich silicide (NiSi₂, NiSi, or the like) is formed in the diffusion layer 103Cb.”

Aoyama950 ¶ [0114].

“In the third embodiment, the gate electrode 103 for the PMOSFET includes the first conductive layer 103A made of the conductive metal, the second conductive layer 103B made of the conductive metal, and the semiconductor layer (silicide layer) 103C made of the semiconductor (silicide). For this reason, in the third embodiment, the gate resistance of the PMOSFET is relatively low.”

Aoyama950 ¶ [0121].

FIG. 6G

FIG. 6L

Aoyama950, FIGS. 6G, 6L (showing formation of gate electrode 103).

FIG. 5

Aoyama950, FIG. 5 (depicting gate electrode 103, including conductive layers 103A and 103B and silicided semiconductor layer 103C).

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0107]-[0109], ¶¶ [0113]-[0117], ¶ [0119], ¶ [0121], FIGS. 5, 6E-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[i] [the second MIS transistor includes: . . .] second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative;

Aoyama950 discloses this feature. For example, Aoyama950 discloses side wall spacers 142, which are made of silicon oxide (an insulator), formed on side surfaces of gate electrode 103 of the third embodiment. Additionally, offset spacers 141 and/or side wall spacers 143 may be considered part of the claimed second sidewall spacers. *See, e.g.*, the following:

“Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or AS are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000°C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.”

Aoyama950 ¶ [0111].

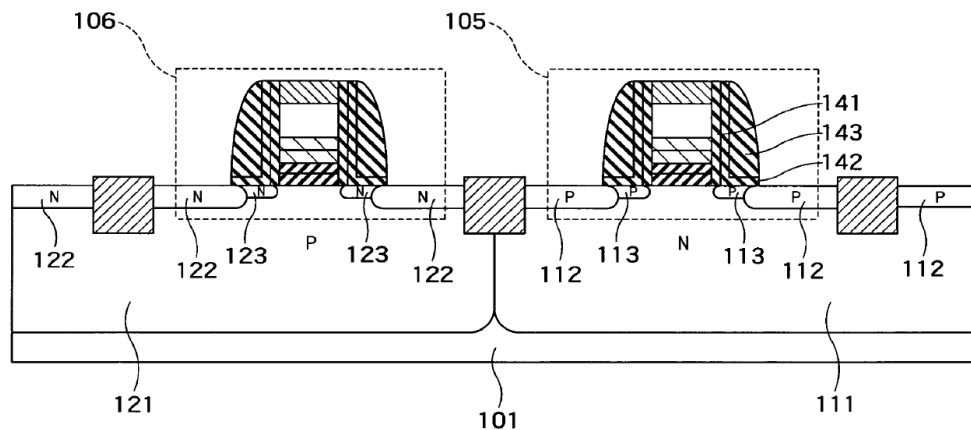


FIG. 6I

Aoyama950, FIG. 6I (depicting offset spacers 141 and side wall spacers 142 and 143 formed on side surfaces of the gate electrode structure for the PMOSFET, on the right-hand side).

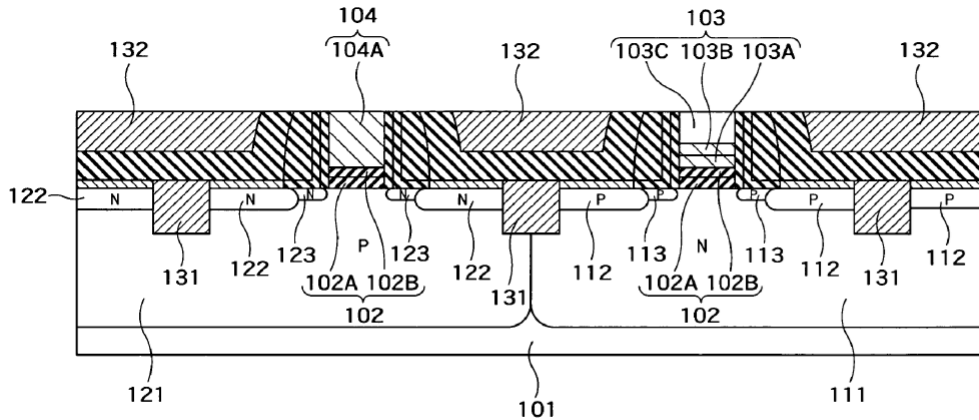


FIG. 5

Aoyama950, FIG. 5 (depicting offset spacers 141 and side wall spacers 142 and 143 formed on side surfaces of gate electrode 103).

See also, e.g., Aoyama950, ¶ [0054], ¶ [0086], ¶ [0111], FIGS. 5, 6I-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[j] [the second MIS transistor includes: . . .] the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers; and

Aoyama950 discloses this feature. For example, Aoyama950 discloses etch stopper film 145 in the third embodiment, which is made of silicon nitride and extends over (1) the side surfaces of gate electrode 103 where offset spacer 141 and side wall spacers 142 and 143 are formed and (2) upper surfaces of source/drain layer 112 located in the PMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143. See, e.g., the following:

“Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET.”

Aoyama950 ¶ [0099].

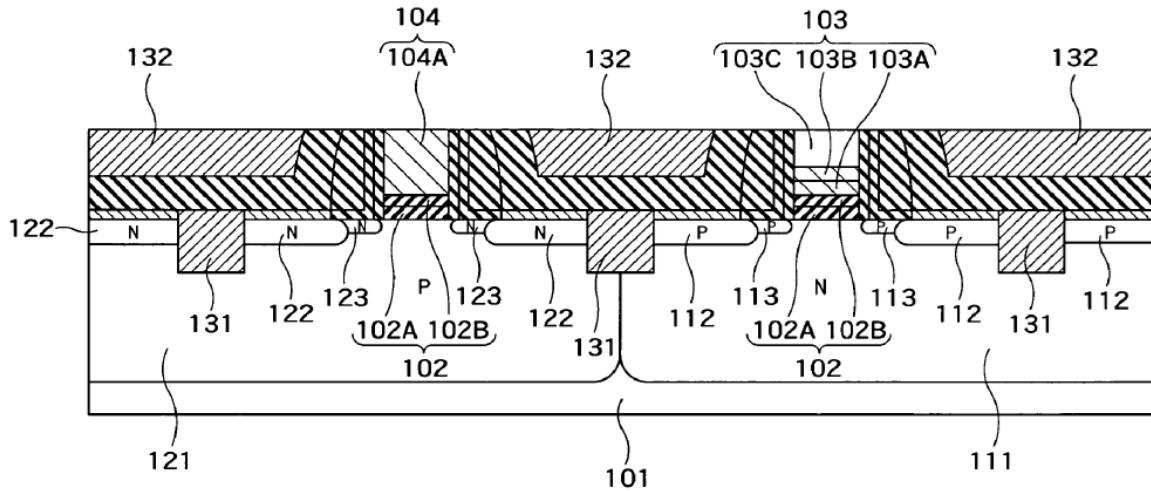


FIG. 5

Aoyama950, FIG. 5 (depicting etch stopper film 145 extending over (1) the side surfaces of gate electrode 103 where offset spacer 141 and side wall spacers 142 and 143 are formed and (2) upper surfaces of source/drain layer 112 located in the PMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143).

“Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or AS are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000°C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.”

Aoyama950 ¶ [0111].

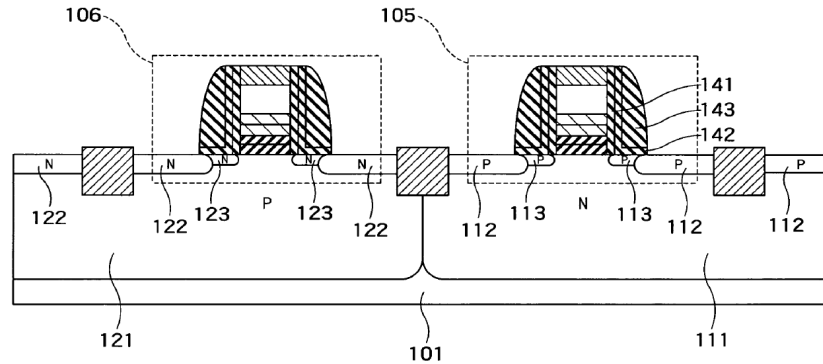


FIG. 6I

Aoyama950, FIG. 6I (depicting the formation of offset spacers 141, side wall spacers 142 and 143, and source/drain layers 112).

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

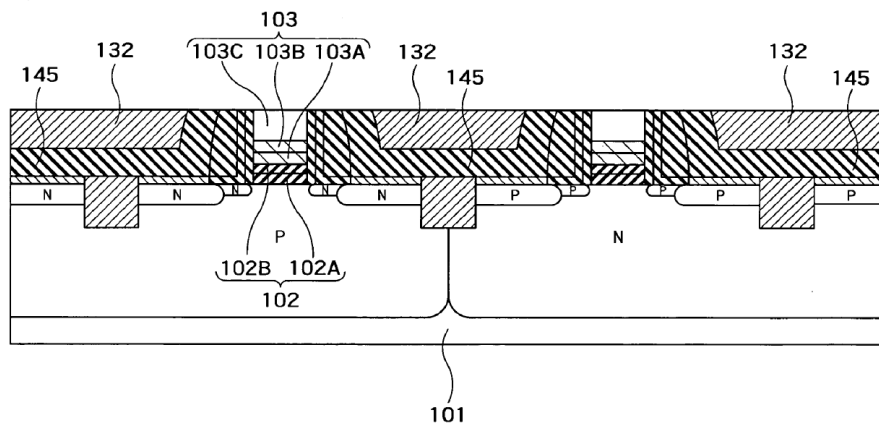


FIG. 6K

Aoyama950, FIG. 6K (depicting the formation of etch stopper film 145 extending over (1) the side surfaces of the gate electrode structure 103 for the PMOSFET on the right-hand side, where offset spacer 141 and side wall spacers 142 and 143 are formed, and (2) upper surfaces of source/drain layer 112 located in the PMOSFET active region laterally outside of offset spacer 141 and side wall spacers 142 and 143).

Exhibit 686-04: Aoyama950

See also, e.g., Aoyama950, ¶ [0054], ¶ [0056], ¶ [0086], ¶ [0088], ¶ [0099], ¶ [0101], ¶¶ [0111]-[0113], FIGS. 5, 6I-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

25[k] the first and second metal films are made of different metal materials,

Aoyama950 discloses this feature. For example, conductive layer 104A is made of tantalum carbonitride (TaCN), for example, whereas conductive films 103A and 103B are made of tungsten (W) and titanium nitride (TiN), respectively, for example. *See, e.g.,* the following:

“Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.”

Aoyama950 ¶ [0107].

“Next, as shown in FIG. 6P. conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is formed over the entire surface by CVD. Examples of the conductive metal include TaCN, which is formed using trisdimethylamino mono-t-amyliminotantalum and monomethylamine.”

Aoyama950 ¶ [0118].

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶¶ [0009]-[0011], ¶¶ [0065]-[0066], ¶ [0098], ¶ [0107], ¶ [0109], ¶¶ [0115]-[0119], ¶ [0121], FIGS. 6, 6E-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

25[l] the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes,

Aoyama950 discloses this feature. For example, silicon nitride etch stopper film 145 in the third embodiment is planarized to the upper surfaces of gate electrodes 103 and 104, thereby removing silicon nitride etch stopper film 145 from the upper surfaces of gate electrodes 103 and 104. *See, e.g., the following:*

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

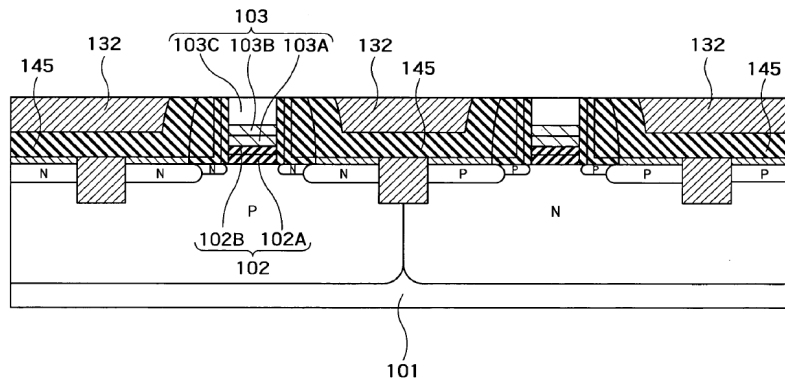


FIG. 6K

Aoyama950, FIG. 6K (depicting formation of etch stopper film 145, including a first planarization step to remove etch stopper film 145 from the upper surfaces of both gate electrodes).

“Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.”

Aoyama950 ¶ [0119].

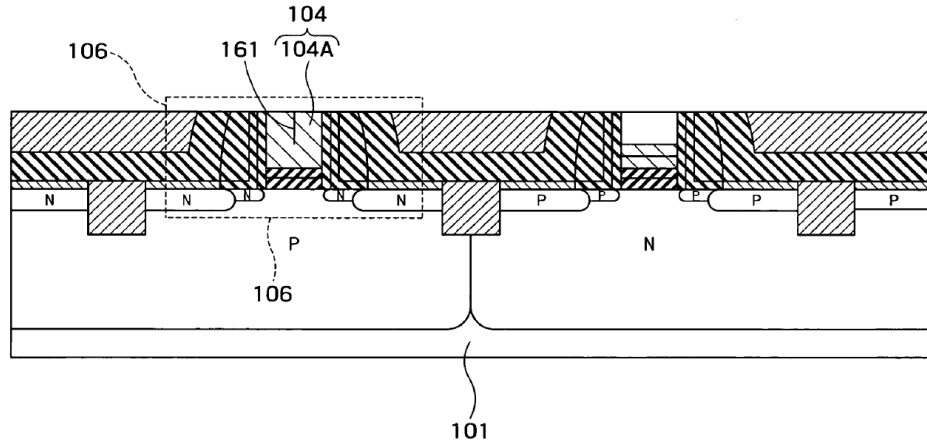


FIG. 6Q

Aoyama950, FIG. 6Q (depicting a second planarization step to remove material from the upper surfaces of both gate electrodes).

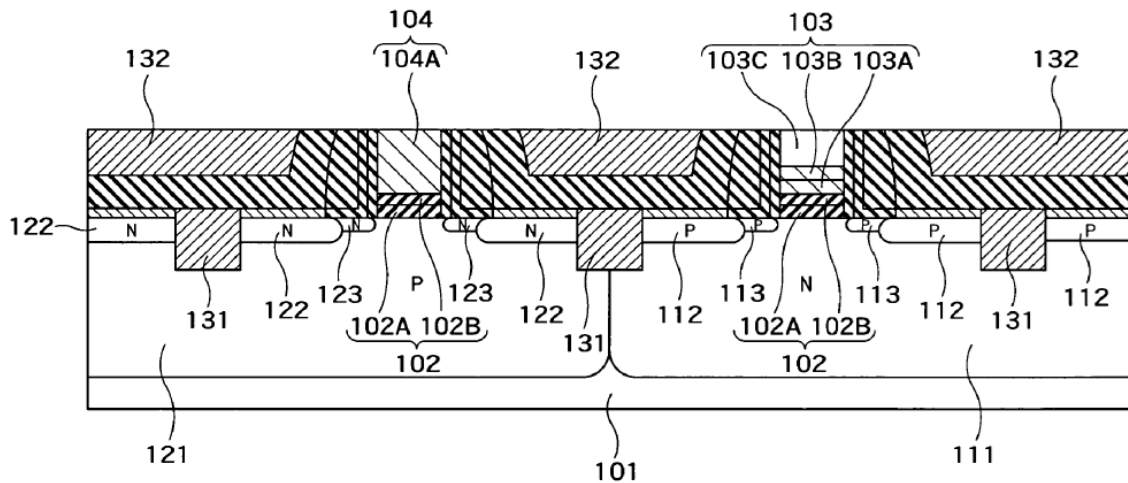


FIG. 5

Aoyama950, FIG. 5 (showing that etch stopper film 145 does not remain on any upper surfaces of gate electrodes 103 or 104).

See also, e.g., Aoyama950 ¶¶ [0113]-[0119], FIGS. 5, 6K-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

25[m] the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.

Aoyama950 discloses this feature. For example, Aoyama950 discloses etch stopper film 145 in the third embodiment, which is made of silicon nitride. *See, e.g.,* the following:

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

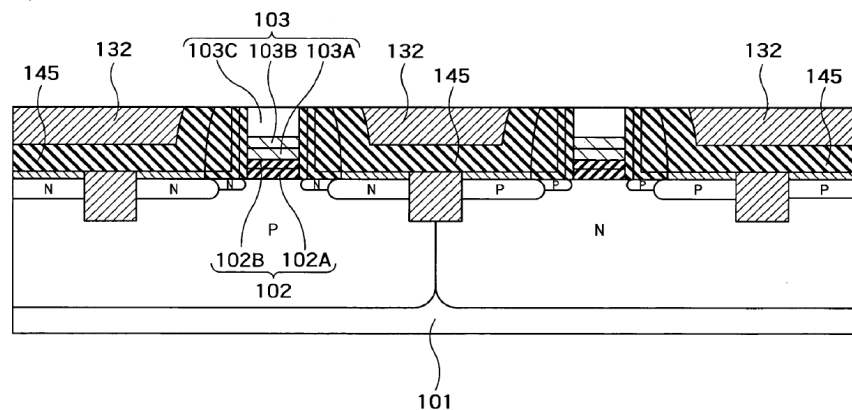


FIG. 6K

Aoyama950, FIG. 6K (depicting the formation of etch stopper film 145).

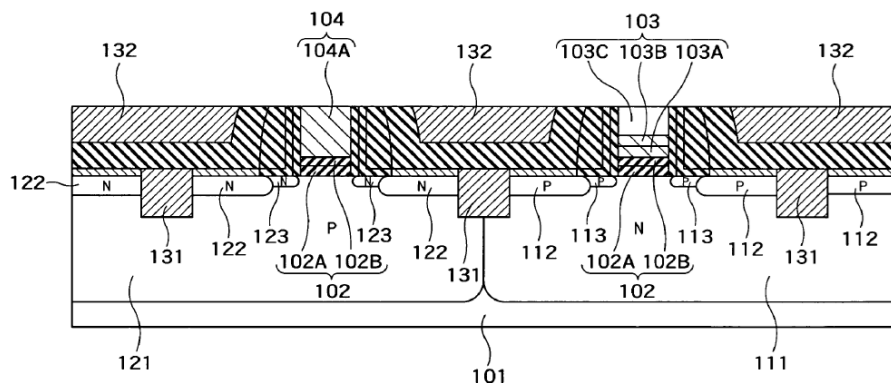


FIG. 5

Aoyama950, FIG. 5 (depicting etch stopper film 145 in the final structure).

Exhibit 686-04: Aoyama950

See also, e.g., Aoyama950, ¶ [0054], ¶ [0056], ¶ [0086], ¶ [0113], FIGS. 5, 6K-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

26[a] The semiconductor device of claim 25, wherein the first metal film has a thickness smaller than that of the second metal film.

Aoyama950 discloses this feature. For example, gate electrodes 103 and 104 have the same thickness because they are formed on the same gate dielectric film 102 and are planarized. Accordingly, the bottom surfaces of gate electrodes 103 and 104 are coplanar, and the top surfaces of gate electrodes 103 and 104 are coplanar. Thus, conductive layers 103A and 103B—whether considered individually or taken together—must be thinner than conductive layer 104A. *See, e.g.,* the following:

“The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film.”

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

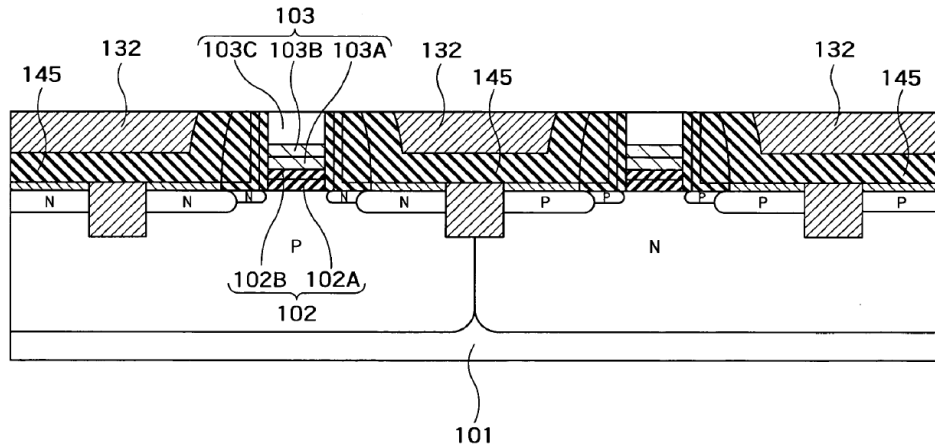


FIG. 6K

Aoyama950, FIG. 6K (showing a first planarization step).

“Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.”

Aoyama950 ¶ [0119].

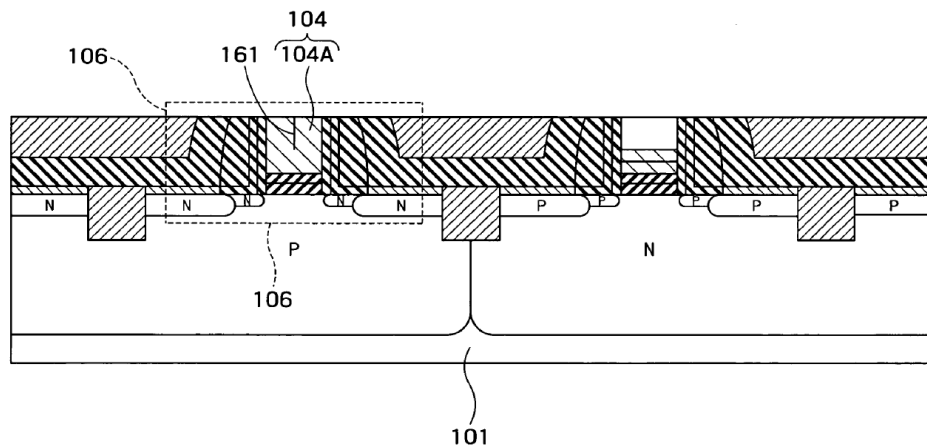


FIG. 6Q

Aoyama950, FIG. 6Q (depicting a second planarization step).

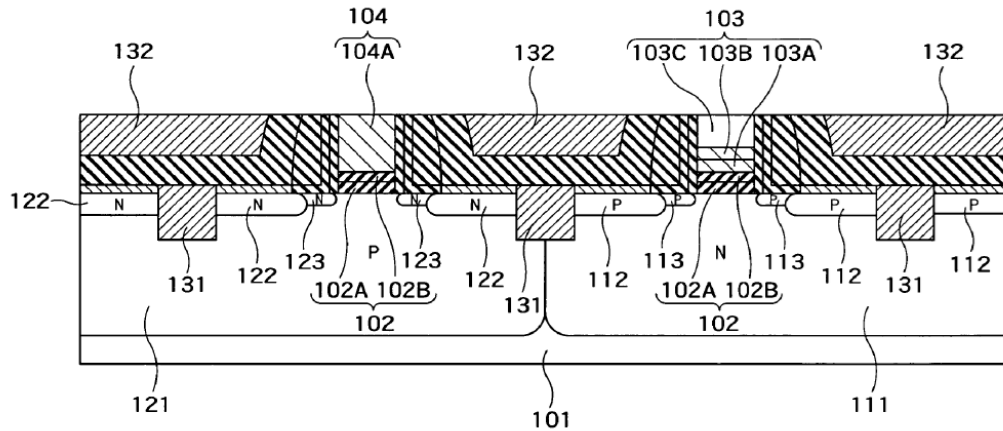


FIG. 5

Aoyama950, FIG. 5 (showing that conductive layers 103A and 103B, taken together or individually, are thinner than conductive layer 104A).

See also, e.g., Aoyama950 ¶ [0098], ¶¶ [0113]-[0119], FIGS. 5, 6D, 6K-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

27[a] The semiconductor device of claim 25, wherein the first and second metal films have different work functions.

Aoyama950 discloses this feature. For example, conductive layer 104A is made of tantalum carbonitride (TaCN), for example, whereas conductive films 103A and 103B are made of tungsten (W) and titanium nitride (TiN), respectively, for example. These materials all have different work functions. See, e.g., Aoyama950 ¶ [0010] (4.3 eV or less work function for TaCN; 4.8 eV or more work function for W); Nakajima317 ¶ (4.9 eV work function for W); Westlinder article, at 551 (5.1 eV work function for TiN).

See also, e.g., the following:

“When a PMOSFET was subjected to a heat resistance test using metals such as W, Ru, and Pt with a work function of 4.8 eV or more, it turned out that it was possible to keep the work function at 4.8 eV or more even after annealing at 1,000 to 1,030° C. However, when an NMOSFET was subjected to a heat resistance test using metals such as TaSi, TaSiN, TaC, TaCN, TaSiCN, HfN, HfSi, HfSiN, WSi, TaHf, and TaHfN with a work function of 4.3 eV or less, it turned out that spike annealing at about 1,000° C. changed the work function to about 4.5 eV, and that it was impossible to keep the work function at 4.3 eV or less. . . .

“[T]here is proposed a method, forming, when a high-permittivity gate dielectric film and a metal gate electrode are adopted in a CMOSFET, a dummy gate dielectric film made of a silicon oxide film and a dummy gate electrode made of polysilicon, removing the dummy gate dielectric film and dummy gate electrode after forming a source/drain diffusion layer, and forming a real high permittivity gate dielectric film and metal gate electrode; the method is called the “damascene gate process” (A. Chatterjee et al., IEDM Tech. Dig. 821 (1997) and A. Yagishita et al., US 2007/021595.0 A1, IEDM Tech. Dig. 785 (1998)). Since, in this method, a metal gate electrode is formed after a source/drain diffusion layer is formed, the work function of the metal gate electrode of an NMOSFET does not change in the step of forming the source/drain diffusion layer requiring annealing at about 1,000° C.”

Aoyama059 ¶¶ [0010]-[0011].

“Next, as shown in FIG. 6E, a W (tungsten) layer (a first conductive layer of a gate electrode for the PMOSFET) 103A with a thickness of about 20 nm is deposited on the hafnium silicon oxynitride film 102B by thermal CVD using tungsten hexacarbonyl or plasma CVD using tungsten hexacarbonyl and hydrogen, a TiN (titanium nitride) layer (a second conductive layer of the gate electrode for the PMOSFET) 103B with a thickness of about 60 nm is deposited on the W layer 103A using diethylaminotitanium and ammonia, and a semiconductor layer 103C made of polysilicon or amorphous silicon is deposited on the TiN (titanium nitride) layer 103B. With the above-described manufacturing steps, the gate electrode 103 for the PMOSFET is formed, ranging from the PMOSFET region 105 to the NMOSFET region 106, on the gate dielectric film 102.”

Aoyama950 ¶ [0107].

“Next, as shown in FIG. 6P, conductive metal, which is a material for forming a third conductive layer 104A of the gate electrode 104 for the NMOSFET, is formed over the entire surface by CVD. Examples of the conductive metal include TaCN, which is formed using tris-dimethylamino mono-t-amyliminotantalum and monomethylamine.”

Aoyama950 ¶ [0118].

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶¶ [0007]-[0012], ¶ [0098], ¶ [0107], ¶ [0109], ¶¶ [0115]-[0119], ¶ [0121], FIGS. 6, 6E-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

28[a] The semiconductor device of claim 25, wherein the silicon nitride film has a thickness smaller than that of the first gate electrode.

Aoyama950 discloses this feature. For example, silicon nitride etch stopper film 145 has a thickness smaller than that of gate electrode 104. *See, e.g., the following:*

“Next, as shown in FIG. 6K, an etch stopper film 145 made of a silicon nitride film is formed over the entire surface by CVD. Then, as shown in FIG. 6K, an inter layer dielectric film 132 made of a silicon oxide film is formed over the entire surface. Then, as shown in FIG. 6K, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (dry etching or wet etching). With the above-described manufacturing steps, the semiconductor layers 103C (non-diffusion layers 103Ca and diffusion layers 103Cb) are exposed both in the PMOSFET region 105 and the NMOSFET region 106.”

Aoyama950 ¶ [0113].

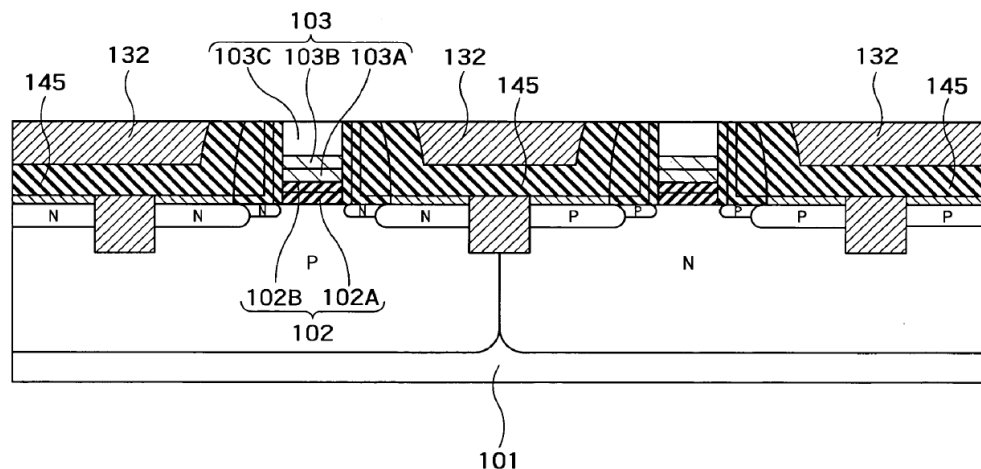


FIG. 6K

Aoyama950, FIG. 6K (depicting formation of etch stopper film 145, including a first planarization step, and showing that etch stopper film 145 is thinner than gate electrode 104).

“Next, as shown in FIG. 6Q, the surface of the substrate 101 is planarized by chemical mechanical polishing or etching (etchback). Through the above-described manufacturing steps, in the NMOSFET region 106, the material for forming the gate electrode is buried in the trench 151 on the gate dielectric film 102, thereby forming the gate electrode 104 for the NMOSFET with a different configuration from that of the gate electrode 103 for the PMOSFET. Since the gate electrode 104 for the NMOSFET (the third conductive layer 104A) is formed in the hole by CVD, a trace of a streaky seam 161 which does not remain in the gate electrode 103 for the PMOSFET (the first conductive layer 103A, second conductive layer 103B, and semiconductor layer 103C) remains in the gate electrode 104 for the NMOSFET.”

Aoyama950 ¶ [0119].

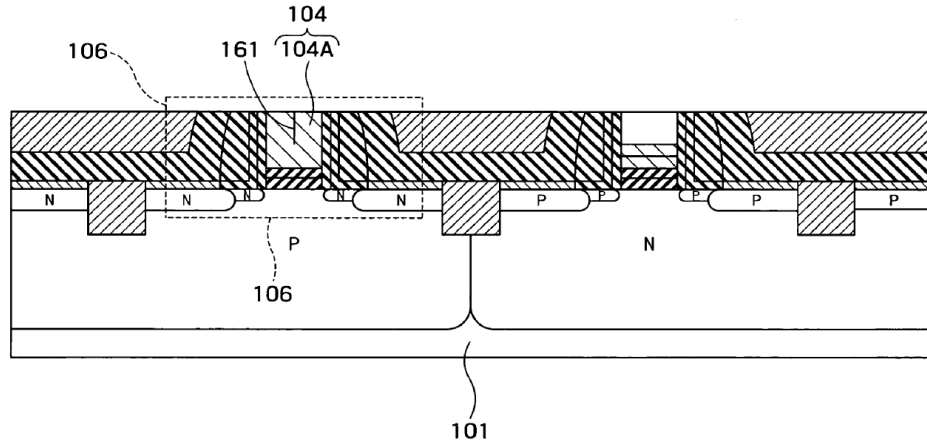


FIG. 6Q

Aoyama950, FIG. 6Q (depicting a second planarization step and showing that etch stopper film 145 is thinner than gate electrode 104).

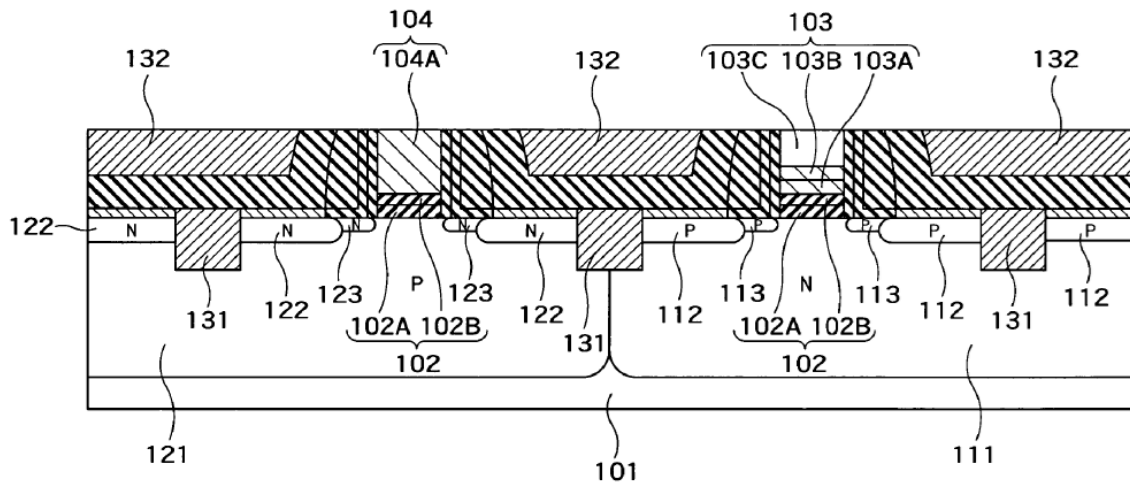


FIG. 5

Aoyama950, FIG. 5 (showing that etch stopper film 145 is thinner than gate electrode 104).

See also, e.g., Aoyama950 Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0113]-[0119], FIGS. 5, 6K-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

31[a] The semiconductor device of claim 25, wherein the first and second gate insulating films are made of the same insulating material.

Aoyama950 discloses this feature. For example, Aoyama950 discloses that gate insulating film 102 formed on NMOSFET region 106 is patterned from the same physical layers as gate insulating film 102 formed on PMOSFET region 105. *See, e.g.*, the following:

“The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film.”

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.”

Aoyama950 ¶ [0106].

“Next, as shown in FIG. 6H, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.”

Aoyama950 ¶ [0110].

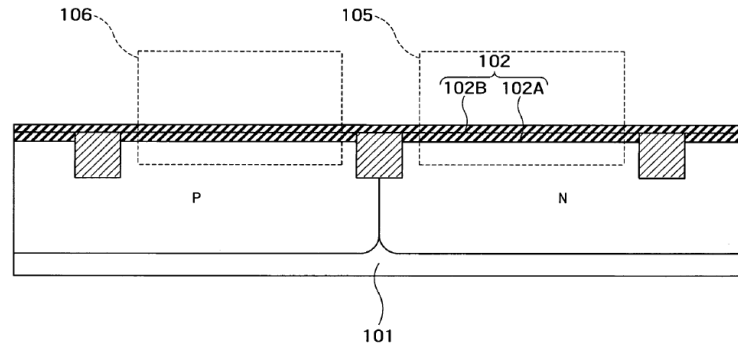


FIG. 6D

Aoyama950, FIG. 6D (depicting formation of gate insulating film 102 before patterning).

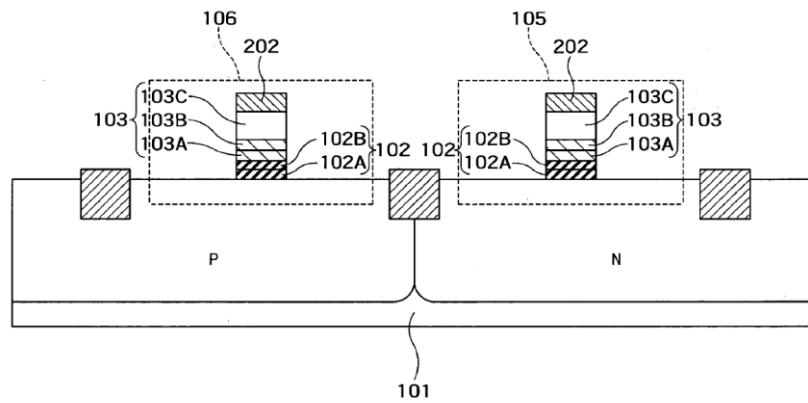


FIG. 6H

Aoyama950, FIG. 6H (depicting formation of gate insulating film 102 after patterning).

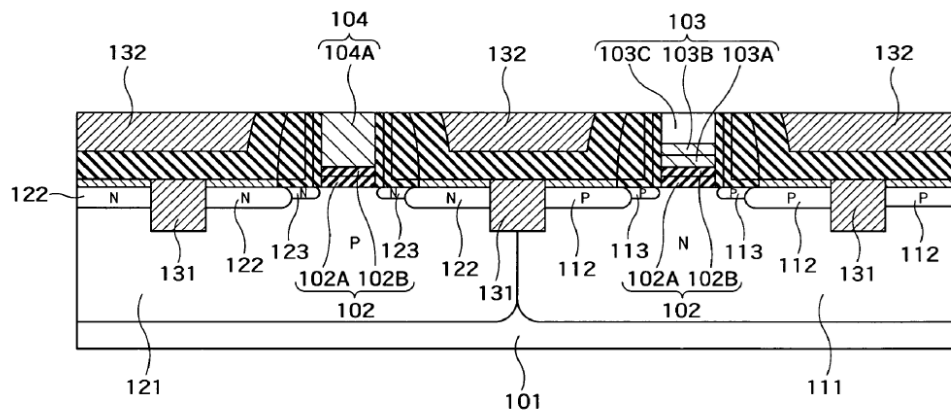


FIG. 5

Aoyama950, FIG. 5 (depicting gate insulating film 102 located on both the left-hand side where the NMOSFET is located and the right-hand side where the PMOSFET is located).

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant's cover pleading.

34[a] The semiconductor device of claim 25, further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

Aoyama950 discloses this feature. See, e.g., the following:

“Additionally, the semiconductor device shown in FIG. 5 has, as diffusion layers for the PMOSFET, a well diffusion layer 111 for the PMOSFET, a source/drain diffusion layer 112 for the PMOSFET, and an extension diffusion layer 113 for the PMOSFET.”

Aoyama950 ¶ [0099].

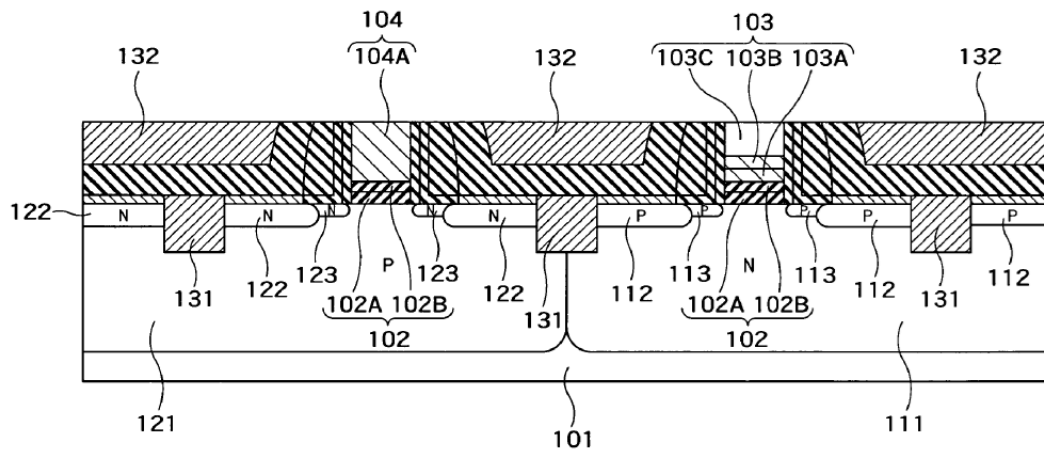


FIG. 5

Aoyama950, FIG. 5 (depicting source/drain layer 112 located in the PMOSFET active region).

“Next, an offset spacer 141 made of a silicon oxide film or silicon nitride film and a side wall spacer 142 made of a silicon oxide film, are formed on the lateral surface of each gate electrode and gate dielectric film by CVD and RIE. Then, ions of B are implanted into the well diffusion layer 111 for the PMOSFET, ions of P or AS are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000°C.; with this process, the source/drain diffusion layer 112 for the PMOSFET and the source/drain diffusion layer 122 for the NMOSFET are formed, as shown in FIG. 6I. Also, ions of B are implanted into the well

Exhibit 686-04: Aoyama950

diffusion layer 111 for the PMOSFET, ions of P or As are implanted into the well diffusion layer 121 for the NMOSFET, and the substrate 101 is subjected to annealing at 1,000° C.; with this process, the extension diffusion layer 113 for the PMOSFET and the extension diffusion layer 123 for the NMOSFET are formed, as shown in FIG. 6I. Then, side wall spacers 143, each of which is made of a silicon nitride film, are formed by CVD and RIE. With the above-described manufacturing steps, in the PMOSFET region 105 and NMOSFET region 106, the source/drain diffusion layer 112 and extension diffusion layer 113 for the PMOSFET and the source/drain diffusion layer 122 and extension diffusion layer 123 for the NMOSFET are formed in the substrate 101.”

Aoyama950 ¶ [0111].

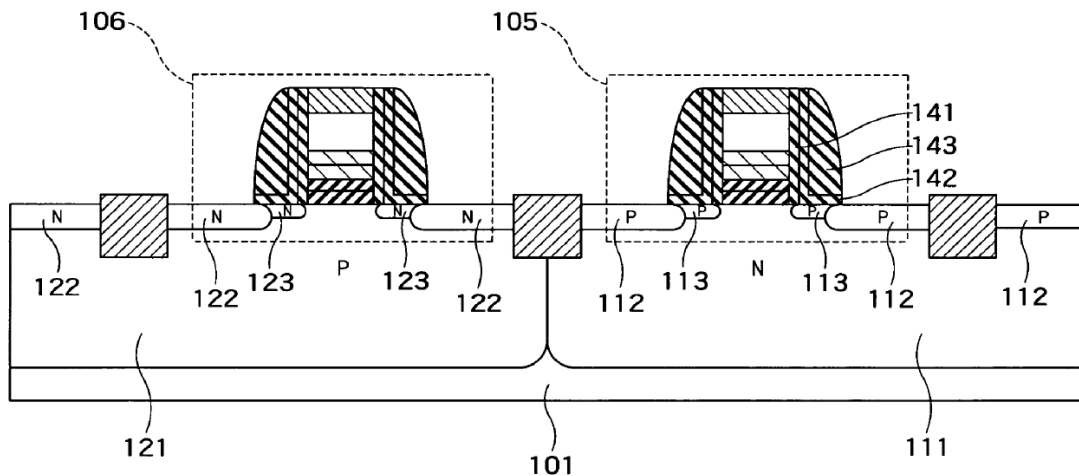


FIG. 6I

Aoyama950, FIG. 6I (depicting the formation of source/drain layers 112).

See also, e.g., Aoyama950, ¶ [0054], ¶ [0086], ¶ [0099], ¶ [0101], ¶¶ [0111]-[0113], FIGS. 5, 6I-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.

35[a] The semiconductor device of claim 25, wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more.

Aoyama950 discloses this feature. For example, gate insulating film 102 includes dielectric film 102B, which is made of hafnium silicon oxynitride. Hafnium silicon oxynitride has a relative dielectric constant of 10 or more. *See, e.g.*, Akasaka939 ¶ [0004] (explaining “HfSiO_x . . . and oxynitrides thereof” have “dielectricity of more than ten”).

See also, e.g., the following:

“The semiconductor device shown in FIG. 5 includes a substrate 101, gate dielectric films 102, a gate electrode 103 for the PMOSFET, and a gate electrode 104 for the NMOSFET. The substrate 101 is a semiconductor substrate, all or a part of which is made of a semiconductor. The substrate 101 in this embodiment is a silicon substrate, all or a part of which is made of silicon. Each gate dielectric film 102 is a high-permittivity gate dielectric film, all or a part of which is made of a high-permittivity dielectric film. Each gate dielectric film 102 in this embodiment includes two layers of dielectric films: a first dielectric film 102A which is a silicon oxide film and a second dielectric film 102B which is a high-permittivity dielectric film.”

Aoyama950 ¶ [0098].

“Next, as shown in FIG. 6D, the dielectric film 201 is removed from the substrate 101 using an ammonium fluoride aqueous solution, and the surface of the substrate 101 is cleaned using 0.5 to 5.0% hydrofluoric acid. Then, as shown in FIG. 6D, a silicon oxide film (a first dielectric film of a gate dielectric film) 102A with a thickness of 0.5 to 0.8 nm is formed on the substrate 101 in an atmosphere containing oxygen, and a hafnium silicate film (a second dielectric film of the gate dielectric film) 102B with a thickness of about 2.0 nm is formed on the silicon oxide film 102A using tetrakis(diethylamino)hafnium, tetrakis(dimethylamino)silicon, and oxygen. After that, the substrate 101 is subjected to annealing at 600° C., thereby densifying the silicon oxide film 102A and hafnium silicate film 102B. After that, the substrate 101 is processed in a nitrogen plasma atmosphere or ammonia atmosphere and then subjected to annealing at 1,000° C., thereby reforming the hafnium silicate film 102B into a hafnium silicon oxynitride film 102B. With the above-described manufacturing steps, the gate dielectric film 102 common to the PMOSFET and NMOSFET is formed, ranging from a PMOSFET region 105 to a NMOSFET region 106, on the substrate 101. The PMOSFET region 105 is a region where the PMOSFET is to be formed, which is a specific example of a P-type FET region, and the NMOSFET region 106 is a region where the NMOSFET is to be formed, which is a specific example of an N-type FET region.”

Aoyama950 ¶ [0106].

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“Next, as shown in FIG. 6H, the silicon oxide film 102A and hafnium silicon oxynitride film 102B are processed using the dielectric film 202 as a hard mask. With the above-described manufacturing steps, in the PMOSFET region 105 and the NMOSFET region 106, a gate dielectric film 102 for the PMOSFET is formed in the PMOSFET region 105, and a gate dielectric film 102 for the NMOSFET is formed in the NMOSFET region 106. Gate dielectric films 102 for the PMOSFET and the NMOSFET are formed from the gate dielectric film 102 common to the PMOSFET and the NMOSFET.”

Aoyama950 ¶ [0110].

See also, e.g., Aoyama950, Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶ [0117], FIGS. 5, 6D-6Q.

To the extent that Aoyama950 is found not to disclose this feature, it would have been obvious based on the disclosures of Aoyama950 alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 686-01 through 686-03 and 686-05 through 686-09 for the reasons discussed herein and in Defendant’s cover pleading.