

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL TECHNOLOGIES, INC.,

Petitioner

v.

LONGITUDE LICENSING LTD.,

Patent Owner

IPR2023-01286
U.S. Patent No. RE43,539

**DECLARATION OF SCOTT E. THOMPSON, PH.D.
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW**

EX1003 / Page 1 of 168
Western Digital Technologies, Inc.

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I. INTRODUCTION

1. I, Scott E. Thompson, have been retained by counsel for Western Digital Technologies, Inc., (“Western Digital” or “Petitioner”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Western Digital’s Petition for *Inter Partes* Review of U.S. Patent No. RE43,539 (“the ’539 patent”).

2. Compensation for my work in this matter is based on an hourly rate. In addition, reasonable and customary expenses associated with my work and testimony in this matter are reimbursed. This compensation is not contingent on the outcome of this matter, nor is it contingent on the specifics of my testimony. I have no personal or financial stake, nor any interest in the outcome of the present proceeding.

3. In the preparation of this declaration, I have studied:

- (1) The ’539 patent, EX1001;
- (2) Reissue Application File History of the ’539 patent (“’773 Reissue App”), EX1002;
- (3) Prosecution File History of the Original Patent of ’539 patent, (“’059 App”), EX1005;
- (4) U.S. Patent No. 6,924,669 to Itoh et al. (“Itoh”), EX1006;
- (5) U.S. Patent No. 3,943,551 to Skorup (“Skorup”), EX1007;

- (6) U.S. Patent No. 4,975,598 to Borkar (“Borkar”), EX1008;
- (7) U.S. Patent No. 3,356,858 to Wanlass (“Wanlass”), EX1009;
- (8) U.S. Patent No. 6,288,563 to Muljono et al. (“Muljono”),
EX1010;
- (9) U.S. Patent No. 5,194,765 to Dunlop et. al (“Dunlop”),
EX1014;
- (10) U.S. Patent No. 4,612,466 to Stewart (“Stewart”),
EX1015;
- (11) Sanjay Dabral et al., Basic ESD and IO Design (1998)
 (“Dabral”), EX1016.

4. In forming the opinions expressed below, I have considered:

- (1) The documents listed above;
- (2) Any additional documents discussed below; and
- (3) My own knowledge and experience based upon my work in the
fields of semiconductor technology as described below.

II. QUALIFICATIONS

5. My qualifications for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my *curriculum vitae*, which is attached as EX1004.

6. My academic and professional background is in electrical

engineering, and I have been working in those fields since the completion of my B.S. in 1987. The following is a brief summary of my relevant qualifications and professional experience.

7. I received B.S., M.S., and Ph.D. degrees in Electrical Engineering from the University of Florida. I am presently a full tenured professor of Electrical Engineering at the University of Florida, teaching classes directed to semiconductor technology. I am an IEEE Fellow for contributions on advancing MOSFETs, and I am a former Intel Corporation Fellow and Director of Computer Chip Technology. I am an inventor on 100 granted U.S. patents, and I have authored 60 publications and 1 book on semiconductor technology.

8. I am experienced in integrated circuit design through my work at Intel Corp. and other technology companies. I also developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design, and packaging technology and computer chip technology including CPU, DRAM, GPU, image sensor, 2D and 3D image sensor processing.

9. I'm also experienced with integrated circuit design for output buffers. I was the Director for Intel Corp.'s computer chip technology, which included output buffer circuits used for integrated circuits during the 2000 timeframe. I have authored articles and patents related to this work including output buffers and inverter circuit performance including circuit performance under transistor

variation (see US9,680,470 and US8,811,068)

III. LEVEL OF ORDINARY SKILL IN THE ART

10. I understand that the level of ordinary skill may be reflected by the prior art of record, and that a Person of Ordinary Skill in The Art (“POSITA”) to which the claimed subject matter pertains would have the capability of understanding the scientific and engineering principles applicable to the pertinent art. I understand that a POSITA has ordinary creativity, and is not an automaton.

11. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems.

12. I have been informed by counsel that the earliest claimed priority date for the ’539 patent is December 19, 2001, although any given claim of the ’539 patent may or may not be entitled to the earliest claimed priority date. I am familiar with the semiconductor technology pertinent to the ’539 patent. I am also aware of the state of the art at the time of the earliest claimed priority date.

13. Based on the technologies disclosed in the ’539 patent, I believe that a POSITA would include someone who had, as of the claimed priority date of the ’539 patent, a bachelor’s or the equivalent degree in electrical engineering or a

related field and 2-3 years of professional experience relating to integrated circuit design. In addition, I recognize that someone with less formal education but more experience, or more formal education but less experience could have also met the relevant standard for a POSITA. I believe that I am at least a POSITA and, furthermore, I have supervised students and engineers who were also POSITAs. Accordingly, I believe that I am qualified to opine from the perspective of a POSITA regarding the '539 patent.

14. For purposes of this Declaration, unless otherwise noted, my opinions and statements, such as those regarding the understanding of a POSITA (and specifically related to the references I consulted herein), reflect the knowledge that existed in the art before the earliest claimed priority date of the '539 patent.

IV. RELEVANT LEGAL STANDARDS

15. I have been asked to provide my opinions regarding whether claims 1-12 (the "Challenged Claims") of the '539 patent would have been obvious to a POSITA at the time of the alleged invention in light of the prior art.

16. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '539 patent, I am relying on certain legal principles explained to me by counsel.

17. I understand that a claim is unpatentable if it is anticipated under 35 U.S.C. § 102 or obvious under 35 U.S.C. § 103.

A. Anticipation

18. I have been informed by counsel that a patent claim is unpatentable as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

B. Obviousness

19. I have been informed and I understand that a claimed invention is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time the invention was made. I understand that the appropriate analysis for determining obviousness of a claimed invention takes into account factual inquiries, including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter as a whole.

20. I have been informed and I understand that the United States Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known

methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. I have also been informed and I understand that a demonstration of obviousness does not require a physical combination or bodily incorporation, but rather may be found based on consideration of what the combined teachings would have suggested to a POSITA at the time of the alleged invention.

V. TECHNICAL BACKGROUND

A. CMOS (Complementary Metal-Oxide-Semiconductor)

21. CMOS is a type of metal–oxide–semiconductor field-effect transistor (MOSFET) fabrication process that uses complementary and symmetrical pairs of p-channel and n-channel MOSFETs for logic functions. The CMOS process was originally conceived by Frank Wanlass and C.T Sah at Fairchild Semiconductor in 1963, and the invention was granted as US patent 3,356,858 (EX1009). Dr. Sah

toward the end of his career had an endowed Chair position at the University of Florida and he was my Ph.D advisor. In the 1980's CMOS became the dominate technology to make integrated circuits and is still the dominate technology used today. The circuits in the '539 are all based on CMOS.

1. Basic Transistor Operation

22. For digital circuits, a CMOS transistor is a semiconductor device that functions as a switch to turn the flow of current ON or OFF to create logic "1" or "0" which is the binary language of a computer. In analog circuits, the transistor can amplify which is increasing the strength of a signal. Millions to billions of digital and analog circuits are in a single integrated circuit chip or IC. These chips are the semiconductor technology found in mobile phone, laptop computers, cloud computing and nearly all modern electronic products.

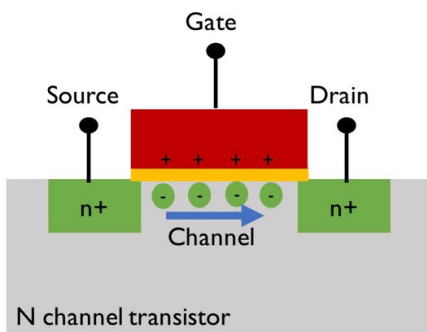
23. There are different types of transistor but modern products generally use a Field Effect Transistor (FET). Field effect transistors work by having an insulating layer between the gate and the channel. For an n-type FET, a voltage applied to the gate causes a vertical electric field in the channel that turns on the electrical switch by electrons being attracted to the gate. The electrons can not get all the way to the gate since there is an insulator between the gate and the semiconductor channel region. The electrons remain just below the insulator and form a channel in the top region of the semiconductor that allows current to flow

from source to drain. Generally, the gate material is a Metal, insulating material is an Oxide, and the channel material is a Semiconductor, so these FETs are called MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). For the past 40 years, MOSFETs are generally the main type of transistor used in all the different types of integrated circuits including the output buffers circuits in the '539 patents. For the past 40 years these MOSFETs are used in groups in standard configurations to make all types of standard Boolean logic functions such as OR, AND, NOR, and NAND gates.

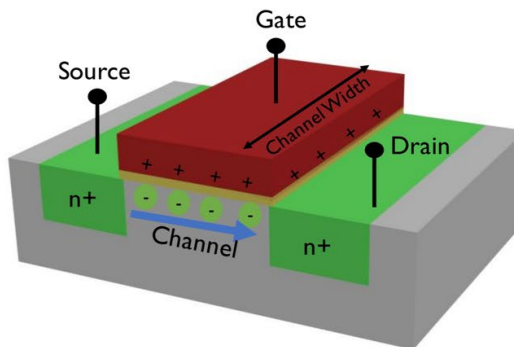
24. A simplified n-type MOSFET image is shown for a 2 dimensional cross section as well as a perspective view. The MOSFET has three terminals: source, drain and gate. The gate is above the channel and is separated from the channel by a thin insulation layer. For n-type MOSFET, a positive voltage places positive charge on the gate which causes negative charges to form under the gate. The negative charges under the gate forms a channel. These negative channel charge close the switch allowing current to flow from source to drain. The closed switch has a low on-state resistance (opposition) to current flow while the open switch has very very high resistance to current flow. The opposition to current flow is also called impedance. The closed switch resistance/impedance is also tailored by increasing the width of the transistor channels. Designers for the past 40 years adjusted the transistor width to provided circuits with low, moderate or

even high output impedance. As a specific example if the transistor width is doubled (i.e. two times larger), the current would have twice as much area to flow in and the impedance/resistance would be reduced by $\frac{1}{2}$. Alternately, two transistors in parallel would also double the size of the current flow path and would also results in the resistance/impedance being reducing by $\frac{1}{2}$.

25. A p-type MOSFET works similarly to a n-type except holes (positive charge) are in the source and drain and a negative gate voltage is used to close the switch when the gate voltage attracts holes to the region under the gate.



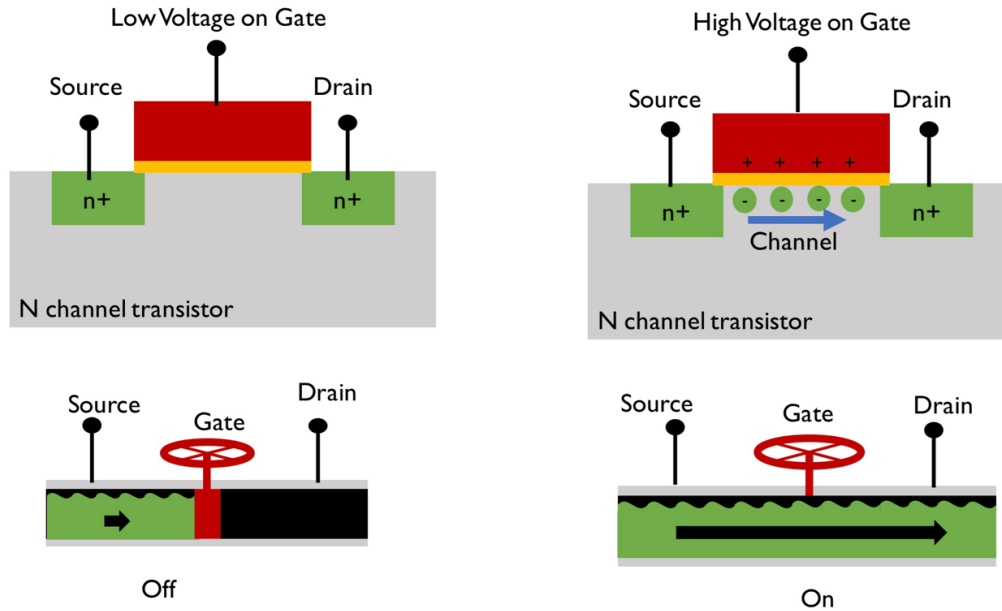
2D transistor cross section



Transistor Perspective View

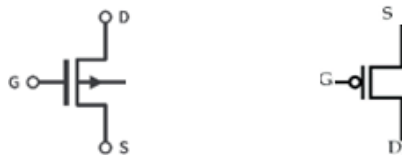
26. For an analogy to understand how a MOSFET works, electrons flowing from source to drain is similar to water flowing through a hose. Just as a valve can be used to control the flow of water between two ends of a hose (source and drain), a gate can be used to control the flow of electrons. A cartoon showing the water flow/ transistor analogy is shown below. For an n-type MOSFET, 0V on that's gate opens the switch while the power supply voltage (typically called VDD

or VCC) on the gate closes the switch hard.



2. P-Channel Transistor

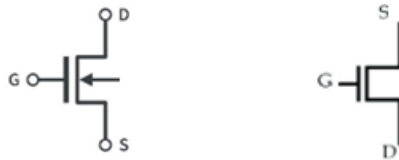
27. A P-channel transistor, or PMOS transistor, is a MOSFET with p-type source and drain regions, and forms a p-channel between the source and drain whenever a low or ground voltage is applied to a gate node. Below are two different drawing types¹ for a p-channel or PMOS transistor:



¹ See, e.g., EX1016, Dabral, 40; EX1006, Itoh, FIG. 1.

2. N-Channel Transistor

28. An N-channel transistor, or NMOS transistor, is a MOSFET with n-type source and drain regions, and forms an n-channel between the source and drain whenever a high voltage is applied to a gate node. Below are two different drawing types² for a n-channel or NMOS transistor:

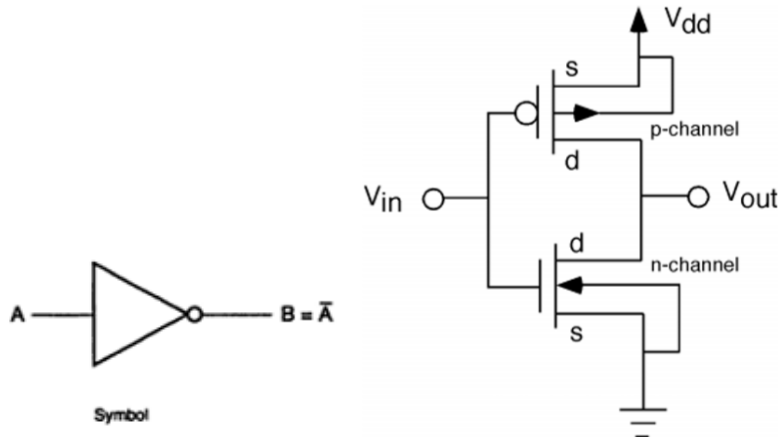


3. Logic Gate

29. A logic gate is a circuit element that performs a logic function, such as AND, OR, NOT, NAND, or NOR. In CMOS, logic gates are typically formed using a group of two or more transistors, including pairs of complementary PMOS and NMOS transistors.

30. An inverter gate (NOT gate) is the nucleus of all digital designs. The logic symbol and the CMOS implementation is shown below. When one transistor is ON, the other is OFF. When the PMOS transistor is ON, V_{out} is pulled up to the power supply voltage (generally called V_{dd} or V_{cc}); and when the NMOS transistor is ON, V_{out} is pulled down to ground (generally called V_{ss} or $0V$).

² See, e.g., EX1016, Dabral, 40; EX1006, Itoh, FIG. 1.

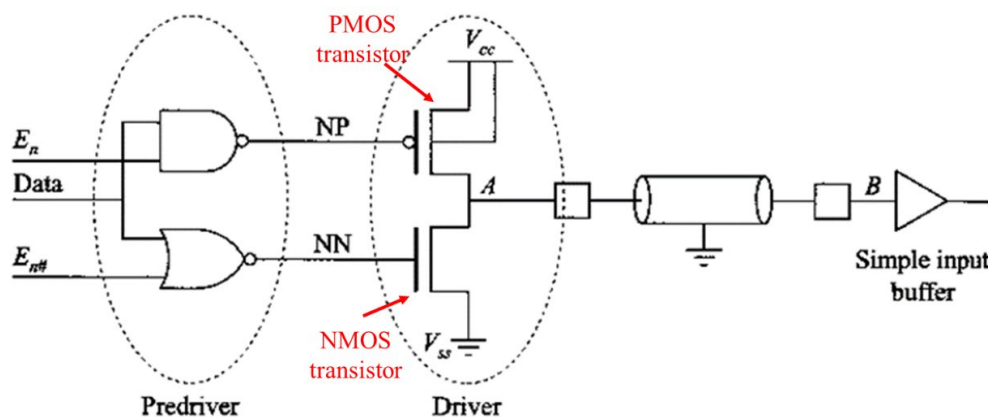


B. Output Buffer Circuit

31. An output buffer, or output driver, is a circuit used to drive internal signals from within an integrated circuit device, to an external signal line or bus that is outside of the integrated circuit. This is how data is transmitted out of the integrated circuit and generally all integrated circuits have had output buffers for the past 50 years. Output buffers typically use inverters with large size n and p-type transistors and addition circuits to control how and when the transistors turn on.

32. Two important inherent properties of an output buffer are output impedance (opposition to current flow) and slew rate (rate of change of the output voltage with time), and it was basic knowledge to design output buffers with output impedance and slew rate control well before the '539 and found in textbooks. The output impedance and slew rate are designed by choosing the number, size and speed that the transistors turn on.

33. A simple CMOS output buffer from a 1998 textbook³ is illustrated below, which includes a simple predriver (controls when and how the PMOS and NMOS turn on by controlling the gate voltages NP and NN), a main driver (inverter that drives logic “1” or “0” on the output node labeled A), and an input receiver (the input receiver is the wire and circuits on the right side of the output node A). The main driver is an inverter implemented with a pair of PMOS and NMOS transistors, which drives the output signal at node “A” (i.e. PMOS drives “node A” to the power supply voltage (V_{cc} which is a logic “1”) or NMOS drives “node A” to ground voltage (V_{ss} which is a logic “0”).



³ EX1016, Dabral, 122.

1. Output Impedance

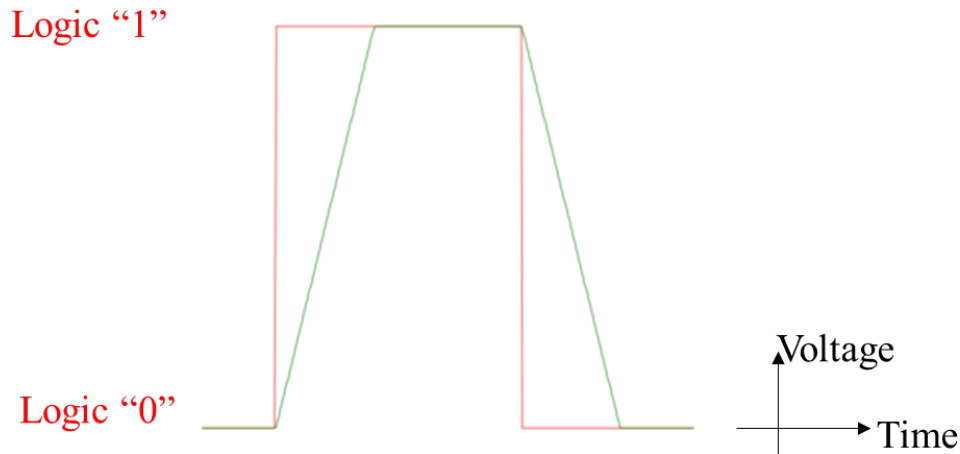
34. Output impedance measured the opposition or resistance to current flow. Output impedance for an output buffer refers to the impedance as it appears on the external signal line or bus. The impedance of the output buffer is set by the transistors connected to the output node, and the gate voltage applied to the gate of each transistor since the gate controls the channel charge which sets the resistance of the switch (transistor).

35. Generally, transistors with a large width or multiple transistors in parallel that are electrically fully ON provided low output impedance. Transistors that are turned OFF have high output impedance. Transistors turned on partially have output resistance between the on and off values. It is common in a high performance output buffer to provide matched output impedance to the line connected to the output node. Generally the output impedance is designed to be in a predetermined range, all based on the individual requirements for the integrated circuit device and the overall required circuit performance.

2. Slew Rate

36. Slew rate refers to the rate of change of an output buffer signal, when the output voltage changes from a low voltage “0” to a high voltage “1” or visa versa. The slew rate is the rising and falling slopes in the image below. For output buffers, the slew rate is generally defined as the change of voltage per unit

of time. Slew rate is usually expressed in V/ μ s.



slew rate:

red=fast slew rate (output voltage changes quickly), **green**=slower slew rate

slew rate effect on a square wave:

red=desired output, **green**=actual output

Electronic circuits may specify minimum or maximum limits on the slew rates for their inputs or outputs, with these limits only valid under some set of given conditions (e.g., output loading).

37. Different designs may have different requirements on slew rate.

Often it is desirable to have a high slew rate (fast rising and falling times) for cleanly changing between high and low outputs, but not too high where other problems (e.g., crosstalk) may occur. In other designs, a low slew rate (gentle rising and falling edges) is desirable. For example, an interface (e.g., USE (Universal Serial Bus)) used to connect a computer to a keyboard to achieve slow

data transfer, is equipped with an output buffer circuit which has a low slew rate (long signal rising and falling times). The use of the output buffer circuit having a low slew rate often makes it unnecessary to provide a bus cable with a shield for preventing undesirable radiation. EX1006, Itoh, 1:5-15.

VI. THE '539 PATENT

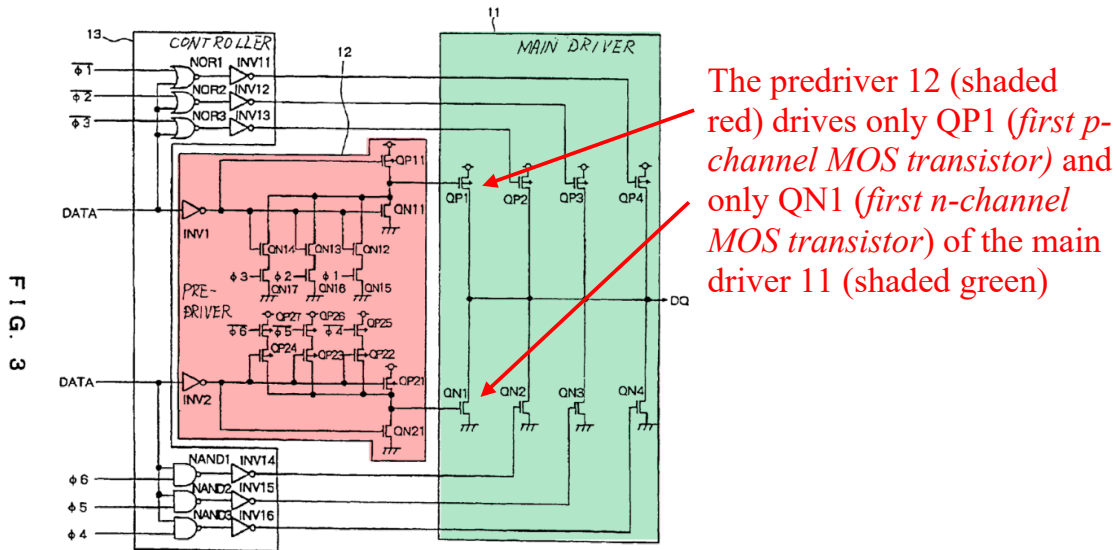
A. Summary of the '539 patent

38. The '539 patent is directed to “an output buffer circuit for use in an integrated semiconductor circuit device,” and more particularly “to an output buffer circuit which is capable of adjusting the output impedance thereof according to control signals from an external source.” EX1001, '539 patent, 1:15-19.

39. In the Background section, the '539 patent acknowledges that “[i]t is important for systems operating at higher speeds and under low voltage to suppress variations in the driving capability and slew rate of the output buffer circuit of the integrated semiconductor circuit device in view of fluctuations in the power supply voltage and the ambient temperature and different device performance capabilities.” EX1001, '539 patent, 1:30-35. The '539 patent recognizes prior art references that “propose arrangements for adjusting the driving capability of an output buffer circuit by changing the output impedance thereof,” and “adjust the slew rate of an output buffer circuit by changing the ratio of t_r (rise time)/ t_f (fall time) of an output pulse waveform.” EX1001, '539 patent, 1:36-43.

40. The '539 patent provides an object of the invention is to “provide an output buffer circuit which is capable of sufficiently compensating for variations in the cross-point between rising and falling waveforms of output pulses and variations in the slew rate against variations in the power supply voltage and the ambient temperature even when the output buffer circuit is incorporated in a system.” EX1001, '539 patent, 2:54-60. The '539 patent asserts that its output buffer circuit achieves this object, which has a main driver for driving a load and a predriver for driving the main driver. EX1001, '539 patent, 2:61-63. The predriver and main driver have an arrangement such that “the number of transistors of the main driver for driving the load according to control signals and the number of transistors of the predriver are changed to simultaneously adjust the cross-point of output pulses and the slew rate as well as the output impedance with the same control signals.” EX1001, '539 patent, 3:14-19.

41. The first embodiment of the '539 patent is illustrated in FIG. 3 below.



EX1001, '539 patent, FIG. 3, annotated

42. Representative independent claim 1 of the '539 patent is reproduced below:

1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:
a main driver having at least a pair of a first p-channel MOS transistor and a first n-channel MOS transistor for driving a load according to said data, and at least a pair of a second p-channel MOS transistor and a second n-channel MOS transistor for driving said load in coaction with said first p-channel MOS transistor and said first n-channel MOS transistor;

a predriver with outputs for driving only said first n-channel MOS transistor and only said first p-channel MOS transistor having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving said first p-channel MOS transistor according to said data, at least a pair of a fourth p-channel MOS transistor and a fourth n-channel MOS transistor for driving said first n-channel MOS transistor according to said data, at least one fifth n-channel MOS transistor for driving said first p-channel MOS transistor in coaction with said third n-channel MOS transistor, and at least one fifth p-channel MOS transistor for driving said first n-channel MOS transistor in coaction with said fourth p-channel MOS transistor; and

a controller for generating control signals to control said fifth n-channel MOS transistor into and out of operation in coaction with said second p-channel MOS transistor, and control said fifth p-channel MOS transistor into and out of operation in coaction with said second n-channel MOS transistor,

wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.

EX1001, '539 patent, 12:54-13:19 (emphasis added for amendments resulted in allowance).

43. As I discuss below in more detail, the semiconductor device presented in the '539 patent was well known to persons of ordinary skill in the art before the earliest claimed priority date of the '539 patent.

B. Prosecution History

1. '059 App (Original Patent Prosecution History)

44. U.S. Application No. 10/320,059 was filed December 16, 2002. The Office issued a non-final rejection on October 8, 2003, rejecting claims 1-16 as anticipated by Atsushi (JPub 2001-068986, cited by Applicant), where various components (e.g., a main driver including first and second p-channel transistors and n-channel transistors, and a predriver including third, fourth, and fifth p-channel transistors and n-channel transistors) are “all connected and operating similarly as recited by Applicant.” EX1005, '059 App., 91-95.

45. Applicant filed a response on January 5, 2004, attempting to

distinguish from Atsushi by asserting that “in FIG. 1 of Atsushi, in the pMOS transistor PMO3, there is no transistor to pull down the gate terminal of PMO3 except NT02 and NS02 (or NT01 and NS01),” while in the application, “a single nMOS transistor QN11 is also provided to pull down the gate terminal of QP1 which corresponds to PM03 in the above mentioned prior art,” together with “two serially connected transistors (QN14 and QN17, QN13 and N16, or QN12 and QN15).” EX1005, ’059 App, 89.

46. On April 6, 2004, in the Final Rejection, Examiner states that Applicant’s statements are not persuasive because none of Applicant’s statements “is directly relate[d to] what is recited in the claims.” EX1005, ’059 App, 80.

47. Applicant amended the claims on June 11, 2004, amending claim 1 to recite “wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.” EX1005, ’059 App, 66.

48. In the Non-Final Rejection on September 1, 2004, Examiner maintained the anticipation rejection over Atsushi, explaining that “[c]laim 1 expressly states that the purpose of the ‘predriver’ is ‘for driving the first n-channel MOS transistor’ and ‘for driving the first p-channel MOS transistor.’ Thus, according the ‘output’ is being read as the nodes connected to the gates of PMO3 and NMO3. While these nodes may be seen to be indirectly connected (i.e., via

circuitry such as R12 and R22) to other elements, these nodes are ‘only directly connected to said first p-channel MOS (PMO3) transistor and said first n-MOS transistor (NMO3).’” EX1005, ’059 App, 53.

49. Applicant further amended the claims on November, 8, 2004: “a predriver **with output for driving said first [n-channell] MOS transistor and said first p-channel MOS transistor** having at least a pair of a third p-channel MOS transistor and a third n-channel MOS transistor for driving....” EX1005, ’059 App, 38. Applicant further states that “numerous connections exist between the main driver and the predriver.” EX1005, ’059 App, 44.

50. Notice of Allowance issued January 14, 2005, with Examiner Amendment that changes “a predriver with outputs for driving said first in-channel MOS transistor and said first p-channel MOS transistor output” to “a predriver with outputs for driving **only** said first in-channel MOS transistor and **only** said first p-channel MOS transistor output.” EX1005, ’059 App, 23. Statement of Reasons for Allowance provides that Atsushi “discloses that outputs [of] the ‘predriver’ controls plural output stages, whereas the claims now recites that the outputs of the ‘predriver’ drive **only** the “first n-channel transistor’ and **only** the ‘first p-channel transistor.’” ’059 App, 23 (emphasis original).

2. ’773 Reissue App

51. Reissue App. No. 11/798,733 was filed May 16, 2007, adding new

claims 17-48 that “are broader than those in the originally issued patent.” EX1002, ’773 Reissue App, 25.

52. In non-final rejection of April 2, 2010, Examiner rejected the new claims as anticipated by Atsushi, and under 35 U.S.C. 251 as “being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based.” EX1002, ’773 Reissue App, 148.

53. On July 2, 2010, Applicant responded with various arguments regarding the recapture issue and the prior rejection. EX1002, ’773 Reissue App, 128-140.

54. On March 7, 2011, a final ejection issued, finding Applicant’s arguments not persuasive. EX1002, ’773 Reissue App, 94. In response, Applicant filed an updated Reissue Declaration, and cancelled claims 17-24. EX1002, ’773 Reissue App, 95.

55. On July 13, 2011, Examiner issued an office action rejecting claims 25-48 as being an improper recapture of broadened claimed subject matter, and indicated that claims 1-16 are allowed. EX1002, ’773 Reissue App, 57-58.

56. Notice of allowance issued April 4, 2012, after Applicant cancelled the new claims 25-48.

VII. CLAIM CONSTRUCTION

57. It is my understanding that in order to properly evaluate the '539 patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called Phillips standard, under which claim terms are given their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. I have also been informed that claim terms only need to be construed to the extent necessary to resolve the obviousness inquiry.

58. I have reviewed the entirety of the '539 patent, as well as its prosecution history. It is my opinion that for purposes of applying the prior art presented herein to evaluate the patentability of the claims no term requires express construction. Accordingly, I have analyzed the claims consistent with their ordinary and customary meaning as would have been understood by a POSITA.

VIII. GROUNDS

A. Overview of Prior Art

1. Itoh

59. Itoh is directed an “output buffer circuit and control method therefor,” and “more particularly, to an output buffer circuit that outputs an output signal having gentle rising and falling edges and a slew-rate control type output buffer

circuit.” EX1006, Itoh, Title, 1:5-8. Itoh describes that its objects include “to provide an output buffer circuit capable of outputting a signal which has less variation in transition time,” and “to provide a slew-rate control type output buffer circuit which can cope with a high or low operational frequency.” EX1006, Itoh, 4:60-65.

60. To achieve these objects, Itoh provides Embodiments 1-5, each Embodiment describes an output buffer circuit including a main driver, where the main driver includes transistors that directly drives VOUT. These transistors in the main driver are also referred to as output transistors. These embodiments are generally in two categories:

a. Category 1 (Embodiments 1-3): first method of slew rate control and additional pair(s) of output transistors for output impedance control

61. In Category 1, in the main driver, Embodiments 1, 2, and 3 each use a single pair of PMOS and NMOS transistors for achieving slew-rate control (e.g., using output transistors having a high impedance to achieve gentle rising and falling of VOUT). Embodiments 1, 2, and 3 each also include additional pair(s) of PMOS and NMOS transistors for additional impedance control during the static state when VOUT is sufficiently stable. In these embodiments, these additional pairs of PMOS and NMOS transistors are only turned on when VOUT is sufficiently stable (e.g. during stable periods B1 and B2 of the VOUT waveform of FIG. 6).

62. Embodiment 1 is described with FIGS. 5-7, and its advantages include that “a variation in the transition time of the output signal VOUT becomes smaller due to the low impedance characteristic of the second drive circuit 23 in the static state of the output signal VOUT.” EX1006, Itoh, 9:40-67.

63. Embodiment 2 is described with FIG. 8, which has the advantage of providing “sub-drive circuits 42a-42c with different impedances,” and by using select signals SEL0 to SEL2, “at least one of the sub-drive circuits 42a-42c is enabled to select the output impedance when the output signal VOUT is in a static state.” EX1006, Itoh, 10:36-42.

64. Embodiment 3 is described with FIG. 9, which provides an inversion output buffer circuit. EX1006, Itoh, 10:44-48.

b. Category 2 (Embodiments 4-5): second method of slew rate control and no additional pair(s) of output transistors for output impedance control

65. In Category 2, in the main driver, each of Embodiments 4 and 5 use a single pair of PMOS and NMOS transistors in the main driver for both slew-rate control and impedance control. Category 2 does not include additional pair(s) of PMOS and NMOS transistors for additional impedance control during the static state when VOUT is sufficiently stable.

66. Embodiment 4 includes FIGS. 10, 11, 12(a)-12(c), and provides a slew-rate control type output buffer circuit that controls a slew rate of the output

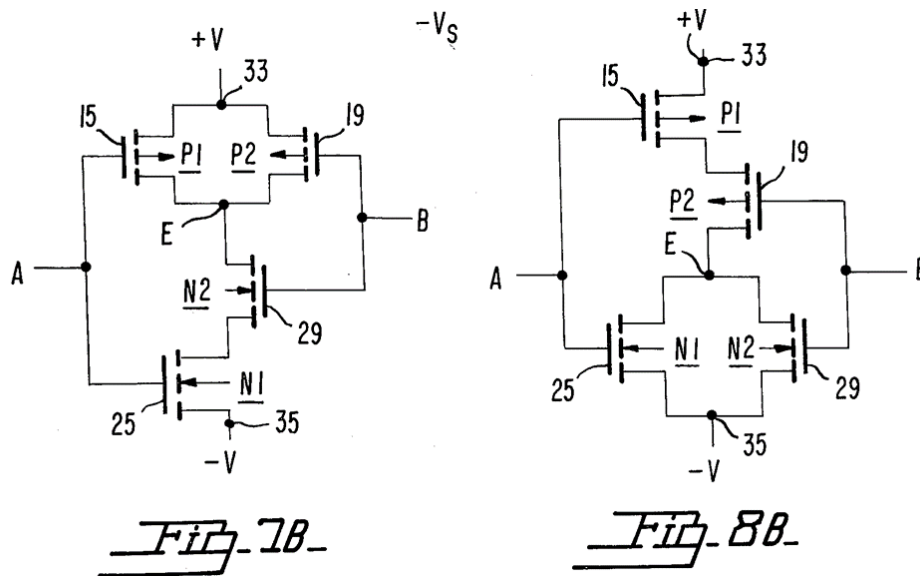
signal by controlling slew rates of the control signals applied to the output transistors. EX1006, Itoh, 11:11-13. Advantages of the fourth embodiment include “reduc[ing] consumed current,” “shortening the propagation delay time,” providing “a wide frequency band,” providing the VOUT “whose pulse width is substantially equal to the pulse width of the input signal VIN,” and “reduc[ing] the possible noise-oriented interference on the interface with the receiving side.”). EX1006, Itoh, 14:19-62.

67. Embodiment 5 includes FIGS. 13-14, and is substantially similar to Embodiment 4, other than that Embodiment 5 uses a Schmitt inverter circuit 243 having a hysteresis characteristic. As such, it has the advantages of conforming to the external interface specification including slew rate specifications by adjusting the hysteresis width and threshold voltage of the Schmitt inverter circuit 243. EX1006, Itoh, 15:54-64.

2. Skorup

68. Skorup was filed April 10, 1974, decades before the earliest claimed priority date of the '539 patent. While Skorup describes that its invention includes a large scale integrated (LSI) array of standard cells arranged in rows and columns adapted to receive different metallization patterns for producing custom circuits (EX1007, Skorup, Abstract), it also includes very fundamental schematic diagrams of CMOS implementation of logic gates (e.g., NAND gate, NOR gate).

69. Specifically, as shown in FIGS. 7B and 8B of Skorup⁴ below, Skorup provides the CMOS implementation of NAND gate and NOR gate respectively. A POSITA would have understood that these are the very fundamental building blocks in CMOS technology, and while CMOS was invented in 1963, these fundamental building blocks are still widely used today. *See, e.g.*, Wanlass (the CMOS patent filed in 1963 by CMOS inventor).



EX1007, Skorup, FIGS. 7B and 8B

3. Muljono

70. Muljono describes that “an output buffer includes a driver circuit

⁴ In drawings below illustrating the combination of Itoh and Skorup, the labels P1, P2, N1, and N2 on FIGS. 7B and 8B of Skorup are removed for clarity.

having an impedance and a predriver circuit to control a slew rate of the driver circuit based on the impedance of the driver circuit.” EX1010, Muljono, Abstract.

71. Muljono recognizes there is a need for output buffer that “operate with an approximately uniform output impedance and slew rate independent of variations in process, supply voltage, and temperature [PVT].” EX1010, Muljono, 2:6-9, 24-28. To address this need, as shown in FIG. 1 below, Muljono describes a compensation circuit 115 that receives signals from temperature detection circuit 117 and voltage detection circuit 119. The compensation circuit 115 generate impedance control signal for driver circuit 105, and generates slew rate control signal for predriver circuit 103 in response to the PVT and in response to the impedance control signal. EX1010, Muljono, 4:1-19.

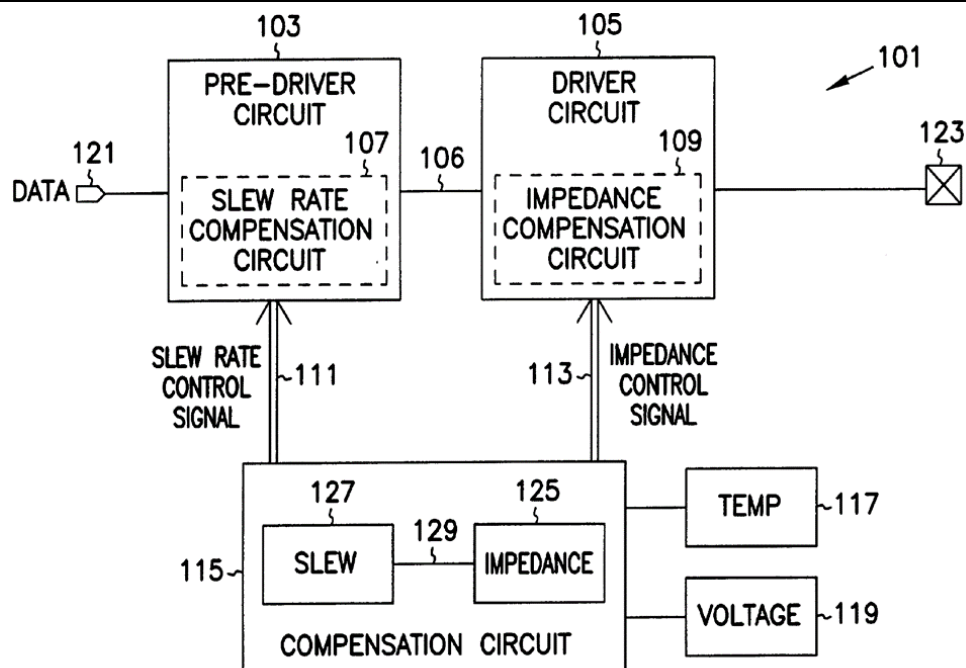


FIG. 1

EX1010, Muljono, FIG. 1

4. Borkar

72. Borkar describes an output driver “for high performance integrated circuits,” where the driver “dynamically compensates for variations in temperature, voltage, and process.” EX1008, Borkar, Abstract.

73. To achieve this, Borkar uses a closed loop feedback technique to compensate the driver for temperature, process, and voltage variations. Specifically, “a scaled down version of an output driver is used to monitor speed variations due to temperate, process, and voltage,” and “the output of which is fed back to the output driver which then performs the necessary compensation.”

EX1008, Borkar, Abstract.

B. Ground 1: Claims 1-3 and 5-7 are Rendered Obvious under 35 U.S.C. § 103(a) over Itoh in view of Skorup.

74. Claims 1-3 and 5-7 are obvious under Itoh combined with Skorup.

Limitations [1.1], [1.2.3], [1.3], [5.1], [5.2.3], [5.2.4], and [5.3] each recite the term “*in coaction with*.” The analysis below is based on POSITA’s understanding of its ordinary and customary meaning, which is consistent across these limitations. The analysis is further supported by the examples in ’539 patent. See, e.g., EX1001, ’539 patent, FIGS. 3 and 4 (illustrating that a pair of P2 and N2 (e.g., QP2 and QN2) drives the load using output DQ in coaction with a pair of P1 and N1 (QP1 and QN1) as recited in [1.1] because they work together to generate DQ); FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction, and illustrating QP21 and QP27 connected in series for driving QN1 in coaction as recited in [1.2.3]); FIGS. 3, 4, and 7 (illustrating driving QN17 in coaction with QP2 and illustrating driving QP27 in coaction with QN2).

1. Reasons to Combine Itoh and Skorup

75. A POSITA would have been motivated to apply Skorup’s teaching of implementing various logic gates (e.g., NOT, NAND, NOR, AND, and OR logic gates) using complementary and symmetrical pairs of p-type channel MOSFET (PMOS) and n-type channel MOSFET (NMOS) transistors in Itoh.

76. Itoh describes an output buffer circuit using CMOS process, using PMOS and NMOS transistors and CMOS logic gates. *See, e.g.*, EX1006, Itoh, FIG. 5, 6:59-8:5 (describing that output buffer circuit 21 of FIG. 5 includes PMOS and NMOS transistor pairs T1 and T2, T3 and T4, inverters 31, 32, 35-38, NAND gate 33, NOR gate 34); *see also* EX1006, Itoh, FIGS. 8 and 9 (each describing a output buffer circuit including PMOS and NMOS transistors and various logic gates).

77. In view of Itoh's need to implement the various logic gates, a POSITA would have implemented the fundamental and well-known teachings of Skorup of CMOS implementation of logical gates (e.g., NOT, NAND, NOR, AND, and OR) using complementary PMOS and NMOS transistors in embodiments of Itoh using complementary and symmetrical pairs of p-type channel and n-type channel MOSFETs, to achieve the benefits of the CMOS technology including high noise immunity and low static power consumption.

78. A POSITA would have been motivated to apply Skorup's teachings of CMOS logic gates (e.g., as shown in FIGS. 7B and 8B of Skorup) to implement the logic gates in embodiments of Itoh, because it would have been consistent with Itoh's use of CMOS technology (using complementary and symmetric PMOS and NMOS transistors), and the combination would have achieved various benefits provided by CMOS technology, including for example, providing "circuits in

which power losses are minimized” by not using passive load elements in logic gates, and “power dissipation is reduced during stand-by periods,” high noise immunity, and low static power consumption. EX1009, Wanlass, 1:22-63.

2. Claim 1

[1.0] 1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

79. To the extent that this preamble is limiting, Itoh teaches the preamble.

80. **First**, Itoh describes an output buffer circuit that receives data (VIN) in the form of an input pulse train and then drives a corresponding output signal VOUT. EX1006, Itoh, FIGS. 3 and 6 (illustrating generally VIN and VOUT are signals including pulses); 3:15-17 (explaining that VIN switches between L and H levels of the pulses).

81. **Second**, Itoh describes outputting data at a predetermined output impedance and slew rate. For example, regarding the embodiment of FIG. 5, Itoh describes that “the first drive circuit 22 causes the external output signal VOUT to **gently rise and fall**, and the second drive circuit 23 **secures the low-output impedance** characteristics.” EX1006, Itoh, 8:2-5. *See also* EX1006, Itoh, FIG. 6 (illustrating slew rate control by showing that VOUT has a gentle rise during A1 and a gentle fall during A2). Furthermore, a POSITA would have understood by securing the low-output impedance characteristics, the second drive circuit of FIG. 5

performs output impedance control to provide an output having a relatively low impedance.

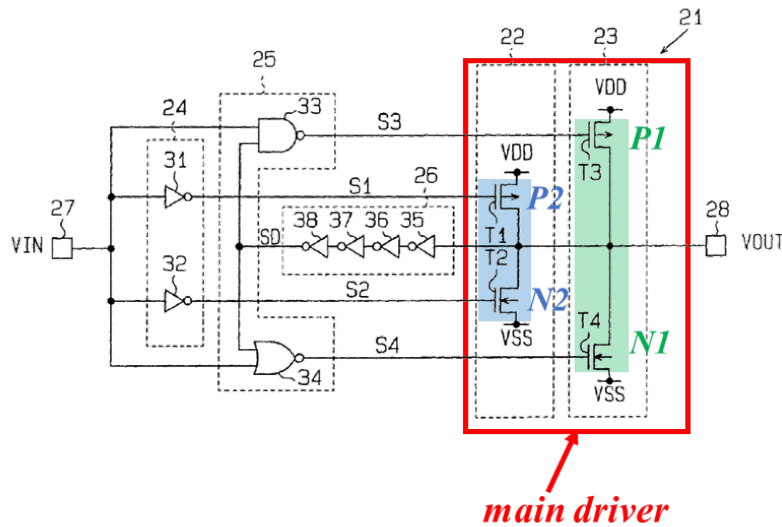
82. Therefore, Itoh discloses or at least renders obvious “[a]n output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate” as recited in the claim.

[1.1] a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];

83. Itoh teaches this element.

84. Specifically, embodiment of FIG. 5 teaches this element. As shown in annotated FIG. 5 of Itoh below, Itoh describes that an output driver circuit 21 includes a main driver (circuits 22 and 23) for driving a load at VOUT 28.

Fig.5



EX1006, Itoh, FIG. 5, annotated

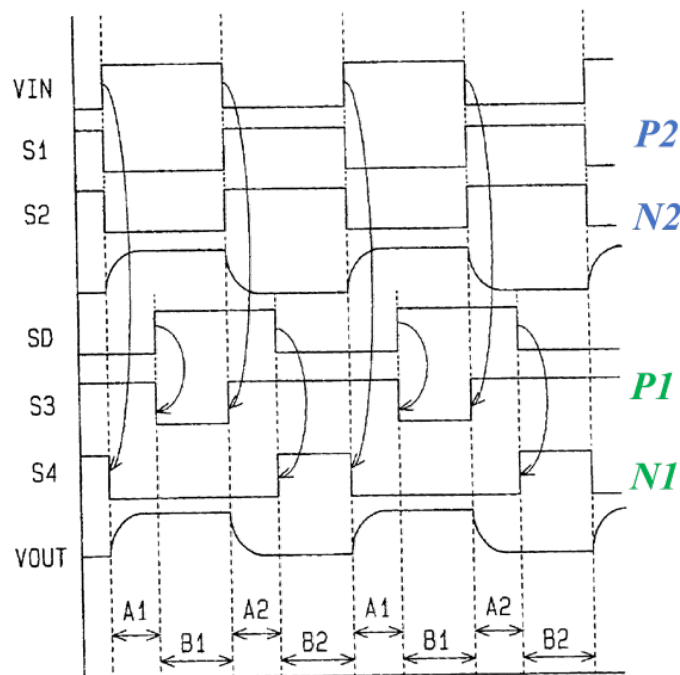
85. As shown in annotated FIG. 5 of Itoh above, the main driver includes circuit 23, which includes a pair of a first p-channel MOS transistor (transistor T3 annotated in green as P1) and a first n-channel MOS transistor (transistor T4 annotated in green as N1) for driving a load according to said input data (V_{IN}). It was well-known in the art that an output driver circuit as described in Itoh generates an output signal (e.g., V_{OUT}) that drives an external load. *See, e.g.*, EX1008, Borkar, 1:51-53 (“the drivers drive the external load by placing a signal on its corresponding pin or pad 19”).

86. In the embodiment of FIG. 5 of Itoh, the main driver further includes circuit 22, which includes a pair of a second p-channel MOS transistor (transistor T1 annotated in blue as P2) and a second n-channel MOS transistor (transistor T2

annotated in blue as N2). This pair of P2 and N2 works together with the pair of P1 and N2 for generating the VOUT for driving the load, and as such, drives the load in coaction with the pair of P1 and N1. As shown in FIG. 5 of Itoh, the configuration of P2 and N2 working in coaction with P1 and N1 for providing VOUT to drive the load is similar to the configuration of those corresponding transistors in the '539 patent. *See, e.g.*, EX1001, '539 patent, FIGS. 3 and 4 (illustrating a pair of P2 and N2 (e.g., QP2 and QN2) drives the load using output DQ in coaction with a pair of P1 and N1 (QP1 and QN1) because they work together to generate DQ).

87. As shown in annotated FIG. 6 of Itoh below, Itoh describes the operation of the output buffer circuit in FIG. 5 including the operation of the pair of P2 and N2 (controlled by S1 and S2 generated based on VIN) for providing VOUT in coaction with the pair of P1 and N1 (controlled by S3 and S4 generated based on VIN and the delayed feedback of VOUT). Referring to FIGS. 6 and 7, Itoh describes in detail the operation and how transistors P1, N1, P2, N2 work in coaction (as controlled by the corresponding control signals) for providing the VOUT for drive the load. EX1006, Itoh, 8:6-9:39.

Fig.6



EX1006, Itoh, FIG. 6, annotated

88. Similar analysis applies to embodiments of FIGS. 8 and 9, each embodiment also teaches this element. For example, FIG. 8 provides an output buffer circuit 41 including a main driver (circuits 22 and 42), which includes a pair of (P1, N1) (e.g., one of (T3a, T4a), (T3b, T4a), (T3c, T4c)), and a pair of (P2, N2) (e.g., T1 and T2) for generating a VOUT to drive a load in coaction with the pair of (P1, N1). The analysis above with regard to FIG. 5 similarly applies to FIG. 9, other than that FIG. 9 includes an inversion output buffer circuit, which generates the output signal VOUT whose phase is opposite to the phase of the input signal

VIN. EX1006, Itoh, 10, 44-48.

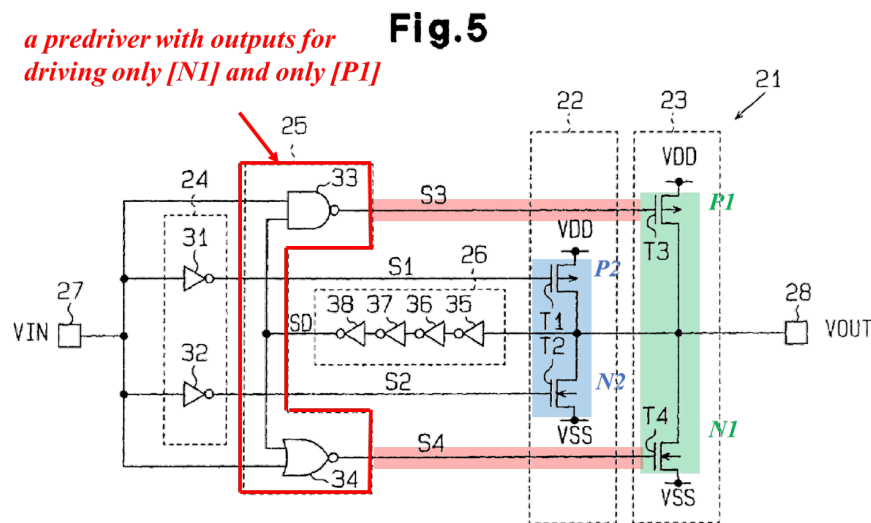
89. Therefore, Itoh discloses or renders obvious “a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1]” as recited in the claim.

[1.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]

90. Itoh teaches this element.

91. As shown in FIG. 5 of Itoh below, Itoh describes a predriver, namely a predriver circuit 25 positioned before the main driver 23, and drives output signals S3 and S4 to the main driver. While Itoh refers to circuit 25 as “control circuit 25,” a POSITA would have understood that circuit 25 is a predriver because it is a stage positioned before the main driver, and provides signals to the main driver. The output signal S3 drives only the n-channel transistor T3 (annotated as transistor N1) of the main driver 23 and the output signal S4 drives only the p-channel transistor T4 (annotated as transistor P1) of the main driver. EX1006, Itoh, 7:28-34 (“A third control signal S3 from the **second control circuit 25** is applied to the gate of the **third output transistor T3**, and a fourth control signal S4 from the **second control circuit 25** is applied to the gate of the **fourth output**

transistor T4.”). See also EX1006, Itoh, FIG. 6 (illustrating predriver outputs S3 and S4 of FIG. 5, which drive only P1 and only N1); see similarly EX1006, Itoh, FIG. 8 (e.g., predriver 43c with outputs S3c and S4c for driving only T3c and only T4c); FIG. 9 (predriver 53 with outputs S13 and S14 for driving only T3 and only T4).



EX1006, Itoh, FIG. 5, annotated

92. Therefore, Itoh teaches “a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1],” as recited in the claim.

[1.2.2] [the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

93. Itoh in view of Skorup renders obvious this element.

94. Itoh teaches NAND gate 33 and NOR gate 34. *See* Itoh Embodiment 1 (FIG. 5). As shown in the figure of Example Combination 1.1 below, Itoh's NAND gate 33 and NOR gate 34 are shown as being implemented using Skorup's teachings of CMOS logic gates using complementary pairs of PMOS and NMOS transistors. *See* EX1007, Skorup, FIGs. 7B and 8B.

which corresponds to the claimed “third n-channel transistor”. These two transistors, P3, N3, drive Itoh’s p-channel transistor T3 (annotated in green as P1) according to VIN, because signal S3 from Itoh’s NAND gate 33 is used for driving Itoh’s main driver transistor P1. Also, Itoh’s NAND gate 33 includes as one of its inputs, the input data signal VIN. *See e.g.*, EX1006, Itoh, FIG. 6 (S3 generated based on VIN for driving P1); EX1006, Itoh, 7:41-51:

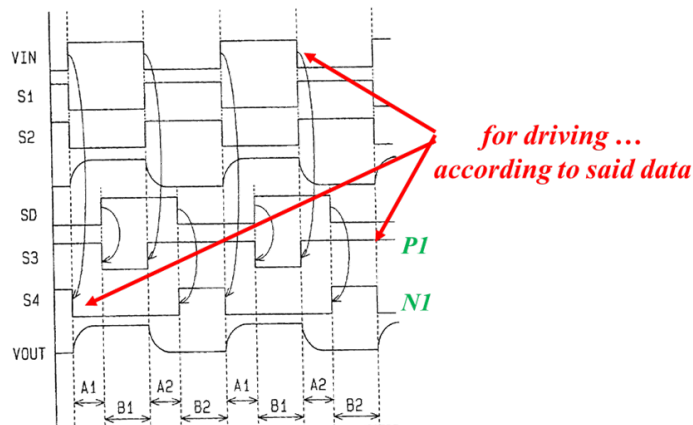
The second control circuit 25 includes a NAND gate 33 and a NOR gate 34. The NAND gate 33 receives the external input signal VIN and a delay signal SD from the delay circuit 26 and performs a NAND operation on the external input signal VIN and delay signal SD to generate the third control signal S3. The NOR gate 34 receives the external input signal VIN and the delay signal SD from the delay circuit 26 and performs a NOR operation on the external input signal VIN and delay signal SD to generate the fourth control signal S4.

96. Further, in the Example Combination 1.1 illustrated above, the NOR gate 34 of Itoh’s predriver circuit 25 is implemented with another pair of p-channel transistors and another pair of n-channel transistors as taught by Skorup. As shown in the figure above, Skorup’s NOR gate includes a p-channel transistor 19 (annotated in blue as P4), which corresponds to the claimed “third p-channel transistor.” Skorup’s NOR gate also includes an n-channel transistor 29 (annotated in blue as N4), which corresponds to the claimed “third n-channel transistor”. These two transistors, P4, N4, drive Itoh’s n-channel transistor T4 (annotated in green as N1) according to VIN, because signal S4 from NOR gate 34 is used for

driving Itoh's main driver transistor N1. Also, Itoh's NOR gate 34 includes as one of its inputs, the input data signal VIN. *See also*, Itoh FIG. 6, reproduced and annotated below.

97. As shown in the figure of Example Combination 1.1 (Itoh Embodiment 1 (FIG. 5) combined with Skorup), Skorup's teachings of CMOS logic gates using complementary pairs of PMOS and NMOS transistors are applied in Itoh, such that NAND gate 33 and NOR gate 34 of FIG. 5 of Itoh are CMOS gates. In the Example Combination 1.1, the predriver 25 has NAND gate 33 including a pair of P3 (EX1007, Skorup, FIG. 7B, 19) and N3 (EX1007, Skorup, FIG. 7B, 23) for driving P1 according to VIN, because S3 from NAND gate 33 for driving P1 is generated according to VIN. *See e.g.*, Itoh, FIG. 6 (S3 generated based on VIN for driving P1). Further, the predriver 25 has NOR gate 34 including a pair of P4 (EX1007, Skorup, FIG. 8B, 19) and N4 (EX1007, Skorup, FIG. 8B, 29) for driving N1 according to VIN, because S4 from NOR gate 34 for driving N1 is generated according to VIN. *See e.g.*, EX1006, Itoh, FIG. 6 (S4 generated based on VIN for driving N1).

Fig.6



EX1006, Itoh, FIG. 6, Annotated

98. Thus, the combination of Itoh and Skorup teaches this claim element

99. Furthermore, a POSITA would have reason to apply Skorup's implementation of NAND and NOR gates to Itoh because Skorup, because Skorup teaches the well-known fundamental knowledge of CMOS technology for implementing logic gates (e.g., NOT, NAND, and NOR) using pairs of PMOS and NMOS transistors. EX1007, Skorup, 2:29-32 ("FIG. 7B is a schematic diagram corresponding to the [two-input NAND gate] of FIG. 7A"); 33-36 ("FIG. 7B is a schematic diagram corresponding to the [two-input NOR gate] of FIG. 8A"); 2:49-52 ("The IGFETs illustrated in the figures each have a metal gate overlying the oxide insulator and are known as **metal-oxide-semiconductor (MOS) transistors.**").

100. In fact, the CMOS implementation of logic gates using

complementary PMOS and NMOS transistors were one of the fundamentals of CMOS, and a POSITA would have understood that the CMOS technology is not limited to any specific application described in Skorup, and would have implemented it in output driver circuits. *See, e.g.*, EX1009, Wanlass (the CMOS patent filed in 1963 by CMOS inventor), FIG. 6 (CMOS multi-input NAND gate with output $Y = \overline{ABC \dots}$), FIG. 7 (CMOS multi-input NOR gate with output $Y' = \overline{D + E + F \dots}$); EX1015, Stewart, FIGS. 1, 2B, and 2C (illustrating implementing logical gates (NAND, NOR) in output buffer circuits using complementary P-type and N-Type transistors with similar configurations as FIGS. 7B and 8B of Skorup).

101. A POSITA would have been motivated to apply Skorup's teachings of CMOS logic gates (e.g., as shown in FIGS. 7B and 8B of Skorup) to implement the logic gates in embodiments of Itoh, because it would have been consistent with Itoh's use of CMOS technology (using complementary and symmetric PMOS and NMOS transistors), and the combination would have achieved various benefits provided by CMOS technology, including for example, providing "circuits in which power losses are minimized" by not using passive load elements in logic gates, and "power dissipation is reduced during stand-by periods." EX1009, Wanlass, 22-63. See also Ground 1: Reasons to Combine Itoh and Skorup.

102. Similar analysis applies to the combination of Skorup with Embodiment 2 of FIG. 8 of Itoh and the combination of Skorup with Embodiment

3 of FIG. 9 of Itoh. In the combination of Skorup with Embodiment 2 of FIG. 8 of Itoh, a POSITA would have been motivated to apply Skorup's teachings of CMOS logic gates (using complementary PMOS and NMOS transistors) to logic gates of FIG. 8 (e.g., NAND gate 47c and NOR gate 48c). In the combination of Skorup with Embodiment 3 of FIG. 9 of Itoh, a POSITA would have been motivated to apply Skorup's teachings of CMOS logic gates (using complementary PMOS and NMOS transistors) to OR gate 57 (by adding an inverter to the CMOS NOR gate) and AND gate 58 (by adding an inverter to the CMOS NAND gate). *See, e.g.,* Maxfield, 48-49 (Figures 6-6 and 6-8).

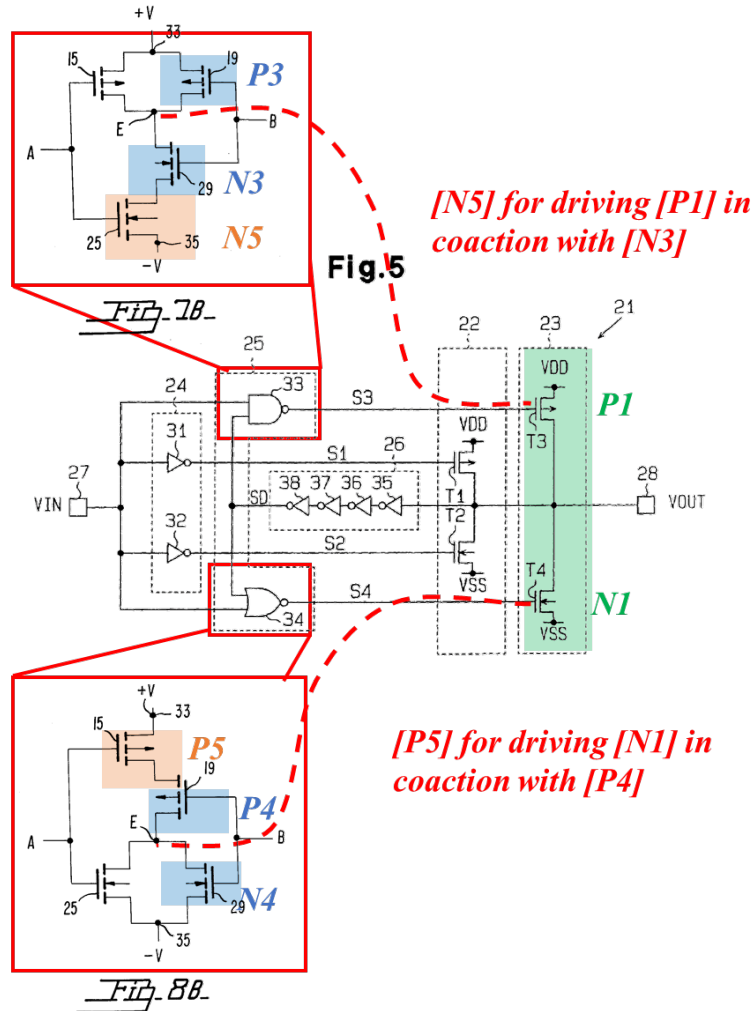
103. Therefore, Itoh in view of Skorup renders obvious “[a predriver...] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data” as recited in the claim.

[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

104. Itoh in view of Skorup renders obvious this element.

105. Continuing with the Example Combination 1.1 (Itoh Embodiment 1

(FIG. 5) combined with Skorup), the combination further includes the claimed fifth n-channel MOS transistor and fifth p-channel MOS transistor.



Example Combination 1.1
Itoh Embodiment 1 (FIG. 5) combined with Skorup (FIGS. 7B and 8B)

106. In the Example Combination 1.1 as illustrated above, Skorup's NAND gate further includes an n-channel transistor 25 (annotated in orange with N5) that teaches the claimed fifth n-channel MOS transistor. Skorup's NAND

gate, including transistor N5, is used for driving the main driver transistor P1 by sending the signal S3 generated at output terminal E of the NAND gate. N5 drives P1 in coaction with N3, because N3 and N5 are connected in series and work together for generating the output signal S3 at output terminal E of FIG. 7B.

107. Likewise, Skorup's NOR gate further includes a p-channel transistor 15 (annotated in orange with P5) that teaches the claimed fifth p-channel MOS transistor. Skorup's NOR gate, including transistor P5, is used for driving the main driver transistor N1 by sending the signal S3 generated at output terminal E of the NAND gate. P5 drives N1 in coaction with P4, because P5 and P4 are connected in series and work together for generating the output signal S4 at output terminal E of FIG. 8B.

108. In the Example Combination 1.1, the configuration of N5 for driving P1 in coaction with N3 (where N3 and N5 are connected in series for generating S3 for driving P1) and the configuration of P5 for driving N1 in coaction with P4 (where P4 and P5 are connected in series for generating S4 for driving N1) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g.,* EX1001, '539 patent, FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction; illustrating QP21 and QP27 connected in series for driving QN1 in coaction); see also [1.1] and examples

109. Example Combination 1.1's teaching of "in coaction with"

configuration as recited in [1.2.3] is further supported by claim language in other limitations of claim 1 and the examples of the '539 patent, see e.g., limitation [1.1] reciting that “a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];” EX1001, '539 patent, FIGs. 3 and 4 (illustrating that (QP1 and QN1) work in coaction with (QP2 and QN2), because they both contribute to generating DQ).

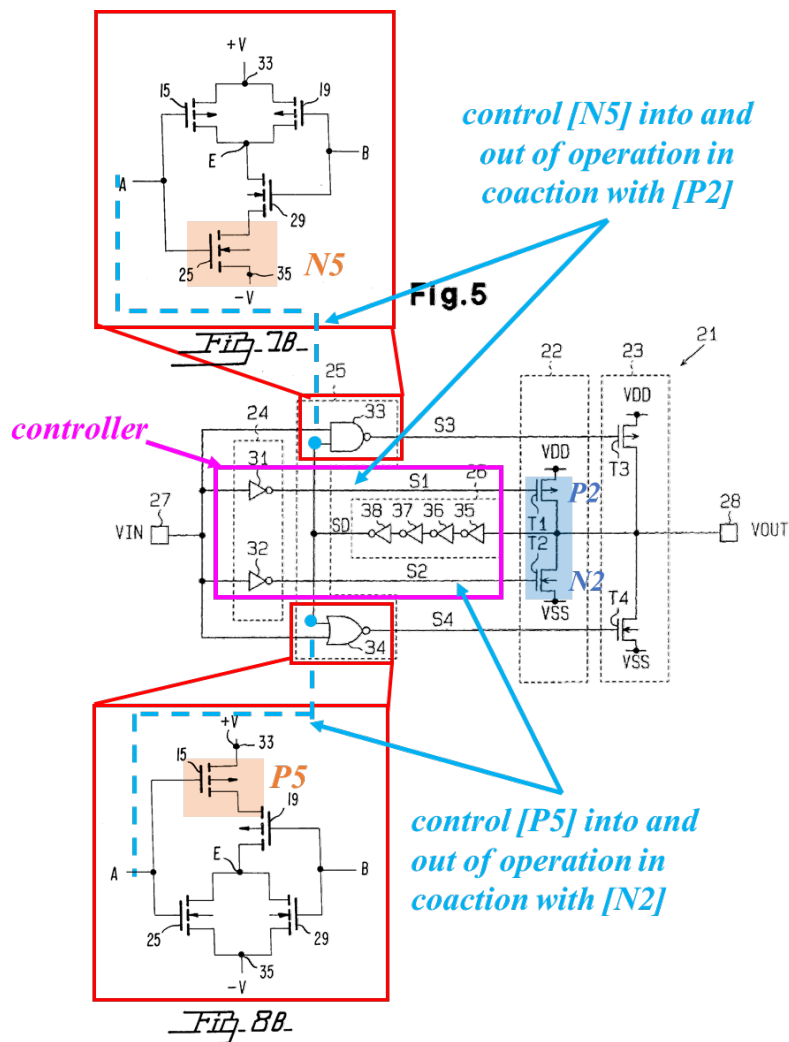
110. Similar analysis applies to the combination of Skorup with Embodiment 2 of FIG. 8 of Itoh (Example Combination 1.2) and the combination of Skorup with Embodiment 3 of FIG. 9 of Itoh (Example Combination 1.3).

111. Therefore, Itoh in view of Skorup renders obvious “[a predriver...having...] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]” as recited in the claim.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

112. Itoh in view of Skorup renders obvious this element.

113. Continuing with the Example Combination 1.1 (combination of Itoh Embodiment 1 of FIG. 5 and Skorup) as illustrated below, a controller (including inverter 24 and delay circuit 26) is supplied with the external output signal VOUT, and outputs the control signals (including SD, S1, and S2). The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters.



Example Combination 1.1
Itoh Embodiment 1 (FIG. 5) combined with Skorup

114. Referring to the delay circuit 26, Itoh describes:

The **delay circuit 26** includes an even number of (four in this case) inverter circuits 35 to 38 connected in series. The first inverter circuit 35 is supplied with the external output signal VOUT and the last inverter circuit 38 **outputs the delay signal SD**.... That is, because the output transistors T1 and T2 of the first drive circuit 22 have a high impedance characteristic, the external output signal VOUT that is generated by the first drive circuit 22 has gentle rising and falling edges. After the external output signal VOUT rises or falls sufficiently, the second drive circuit 23 is driven. The second drive circuit 23 has a low impedance characteristic. **Therefore, the first drive circuit 22 causes the external output signal VOUT to gently rise and fall, and the second drive circuit 23 secures the low-output impedance characteristic.**

Itoh, 7:51:8-5 (emphasis added).

115. The technique for using a delay circuit receiving VOUT and generating a control signal using VOUT was well-known in the art as a “self-timed control signal,” and the delayed time could be controlled by the inverters. For example, two inverters would result in a delay that is 2X the single inverter delay, and four inverters would result in 4X the single inverter delay.

116. Itoh further describes the generation of control signals S1 and S2:

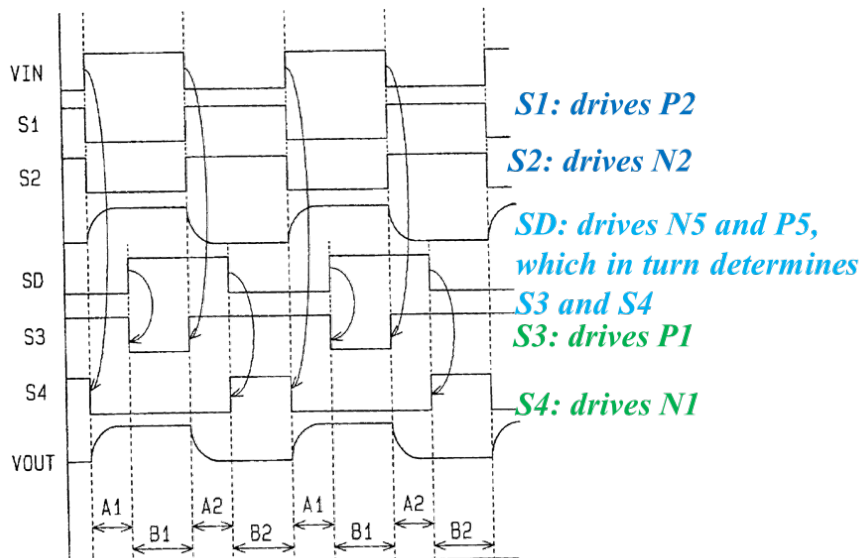
The **first control circuit 24** includes two inverter circuits 31 and 32. The first inverter circuit 31 receives the external input signal VIN and **generates the first control signal S1** which is the external input signal VIN inverted. The second inverter circuit 32 receives the external input signal VIN and **generates the second control signal S2** which is the external input signal VIN inverted.

Itoh, 7:34-40 (emphasis added).

117. In Example Combination 1.1 as illustrated, a POSITA would have been motivated to supply control signal SD to NAND gate 33, by supplying the control signal SD to the gate of N5 (e.g., through terminal A of FIG. 7B), which drives N5 into and out of operation. Further, a POSITA would have been motivated to supply the control signal SD to NOR gate 34, by supplying the control signal SD to the gate of P5 (e.g., through terminal A of FIG. 8B), which drives P5 into and out of operation. As discussed in more detail with reference to FIG. 6 of Itoh below, in the combination, control signal SD, working together with control signal S1, controls N5 into and out of operation in coaction with P2. Further, control signal SD, working together with control signal S2, controls P5 into and out of operation in coaction with N2.

118. As shown in annotated FIG. 6 of Itoh below, in Example Combination 1.1, signals (e.g., S1, S2, SD, S3, and S4) drive transitions (e.g., P1, N1, P5, N5, P2, N2) work in coaction to provide VOUT with the desired slew rate and impedance. I have also provided the corresponding operation states of the signals and transistors of Example Combination 1.1.

Fig.6



Itoh, FIG. 6, annotated

	A1	B1	A2	B2
VIN	L→H	H	H→L	L
S1/P2	L/On	L/On	H/Off	H/Off
SD/N5	L/Off	H/On	H/On	L/Off
S3/P1	H/Off	L/On	H/Off	H/Off
S2/N2	L/Off	L/Off	H/On	H/On
SD/P5	L/On	H/Off	H/Off	L/On
S4/N1	L/Off	L/Off	L/Off	H/On
VOUT	Rising	VPP	Falling	VSS

Example Combination 1.1, Operation States
Itoh Embodiment 1 (FIG. 5) combined with Skorup (FIGS. 7B and 8B)

119. As shown in the table of operation states above, control signal SD, together with control signal S1, controls N5 into and out of operation in coaction

with P2, so that N5 and P2 have the required states at each of the A1, B1, A2, and B2 periods to provide VOUT with the desired slew rate and impedance. For example, SD controls the state of N5, which determines S3 together with VIN, and S3 drives P1 in coaction with P2 to generate VOUT. When VIN is switching from L to H, during A1, the high-impedance P2 is turned on by control signal S1 to control slew rate for a gentle rising edge (VOUT increasing slower with P2 having a high impedance). In coaction with P2, low impedance P1 and N1 are turned off by S3 and S4, so that they do not decrease the impedance to affect the gentle rising. During B1 (static state where VOUT is sufficiently stable at VDD), low-impedance P1 is turned on to provide low output impedance.

120. Furthermore, as shown in the table of operation states above, control signal SD, together with control signal S2, controls P5 into and out of operation in coaction with N2, so that P5 and N2 have the required states at each of the A1, B1, A2, and B2 periods to provide VOUT with the desired slew rate and impedance. For example, SD controls the state of P5, which determines S4 together with VIN, and S4 drives N1 in coaction with N2 to generate VOUT. Specifically, when VIN is switching from H to L, during A2, the high-impedance N2 is turned on by control signal S2 to control the slew rate for a gentle falling edge (VOUT dropping slower with N2 having a high impedance). Low impedance P1 and N1 are turned off by S3 and S4. During B2 (static state where VOUT is sufficiently stable at

VSS), low-impedance N1 is turned on by S4 to provide low output impedance.

121. Example Combination 1.1's teaching of "in coaction with" configuration as recited in [1.3] is further supported by other limitations of claim 1 reciting "in coaction with" and the examples of the '539 patent, *see e.g.*, limitation [1.1] and the corresponding example in FIGS. 3 and 4 of '539 patent (illustrating that (QP1 and QN1) working in coaction with (QP2 and QN2), because they work together to generate DQ); limitation [1.2.3] and the corresponding example in FIG. 3 of '539 patent (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction, and QP21 and QP27 connected in series for driving QN1 in coaction).

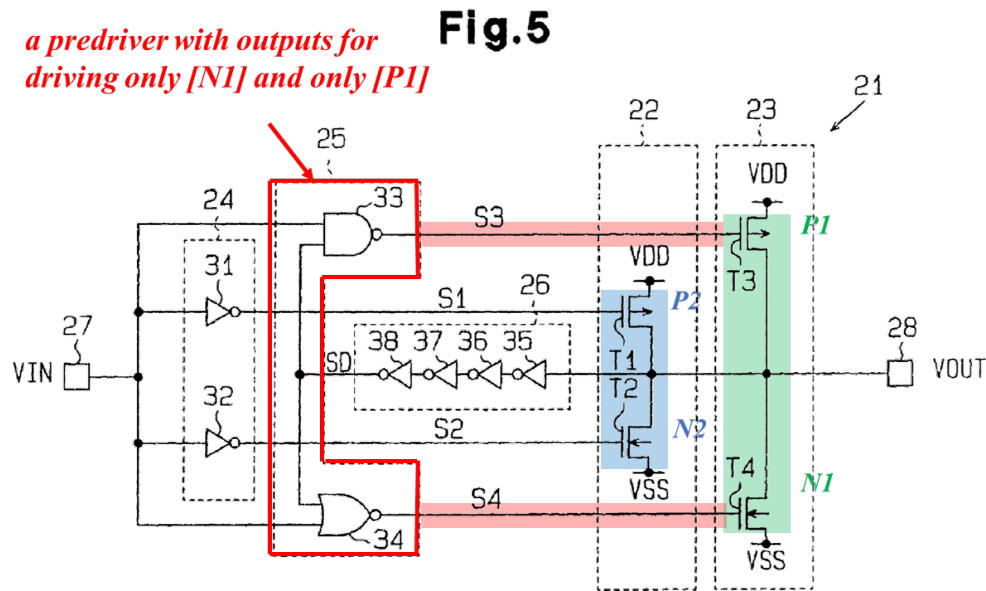
122. Therefore, Itoh in view of Skorup renders obvious "*a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2]*" as recited in the claim.

[1.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.

123. Itoh teaches this element.

124. First, as discussed at [1.2.1], Itoh teaches "a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]."

125. Second, as shown in annotated FIG. 5 of Itoh below, Itoh teaches the output of the predriver (S3 from NAND gate 33 and S4 from NOR gate 34 of predriver 25) is directly connected only to P1 and N1 of said main driver.



126. Therefore, Itoh discloses or renders obvious that “wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver” as recited in the claim.

3. Claim 2

[2.0] 2. The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other.⁵

127. Itoh in view of Skorup renders obvious this element.

128. Specifically, as shown in Example Combination 1.1 (Itoh

Embodiment 1 (FIG. 5) combined with Skorup), the number of P2 and N2 is two

(2). And the number of N5 and P5 is also two (2).

⁵ There is no antecedent basis for the term “*transistors*” recited in “*second p-channel MOS **transistors** and said second n-channel MOS **transistors** and the number of said fifth n-channel MOS **transistors** and said fifth p-channel MOS **transistors***” of claims 2 and 3. Instead, claim 1 recites “*at least a pair of a first p-channel MOS **transistor** and a first n-channel MOS **transistor** for driving a load according to said data, and at least a pair of a second p-channel MOS **transistor** and a second n-channel MOS **transistor**.*” As such, a POSITA would have understood that the term “*transistors*” as recited in claims 2 and 3 includes “at least a transistor.”

4. Claim 3

[3.0] *The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are different from each other.*

130. Itoh in view of Skorup, in further view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element.

131. First, as discussed at Ground 1: Claim 2 above, Itoh in view of Skorup renders obvious that the number of P2 and N2 and the number of N5 and P5 are equal to each other.

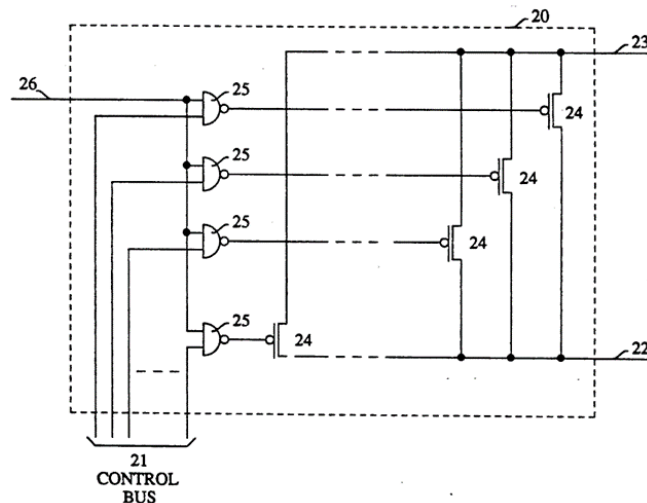
132. Second, it is important to understand the basic, fundamental knowledge of a POSITA. For example, it is fundamental that a resistor shown in a circuit diagram as a single resistor can be physically implemented using multiple resistors in series. Likewise, a capacitor shown in a circuit diagram as a single capacitor can be physically implemented using multiple capacitors in parallel.

133. Similarly, a POSITA would have been motivated to implement a transistor (e.g., P5 or N5) using two or more unit transistors connected in series or parallel, to achieve desired properties. Examples of such properties include a desired transistor size (e.g., using either fixed configuration or digitally controlled element sizing), for the benefits of design flexibility and element sizing control, as well-known in the art. *See, e.g.,* EX1014, Dunlop, Abstract, 5:7-12 (describing “an

integrated circuit transistor whose size is digitally controlled,” for example, with MOS transistors of “a parallel interconnection” or “series connection”).

134. As shown in FIG. 3 of Dunlop below, it was well-known technique to provide a transistor with a desired size by controlling the unit transistors connected in parallel or in series. *See also* EX1014, Dunlop, 4:59-60 (“The number of transistors 24 used is a design choice.”); 5:7-12 (“although FIG. 3 is depicted with a parallel interconnection of resistors, the principles of this invention can be applied with equal effectiveness, where the applications calls for, to other interconnection arrangements, such as a series connection of elements, or a series and parallel connection of elements.”).

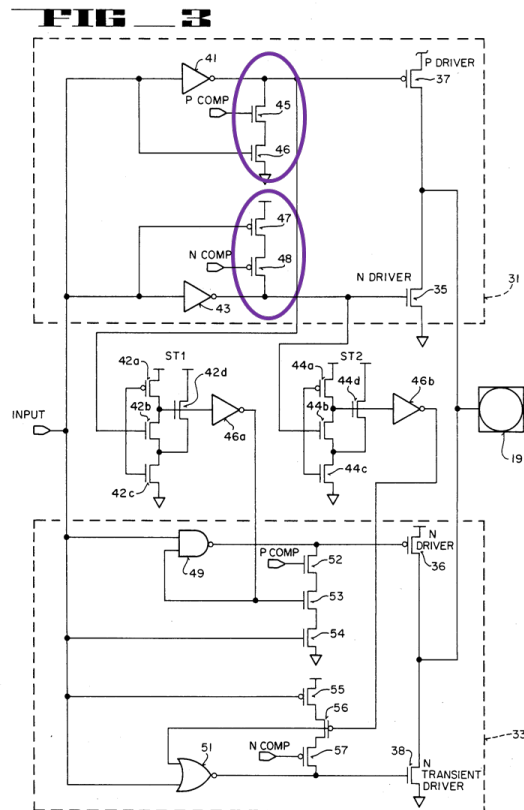
FIG. 3



EX1014, Dunlop, FIG. 3

135. Similarly, as shown in annotated FIG. 3 of Borkar below, it was well-

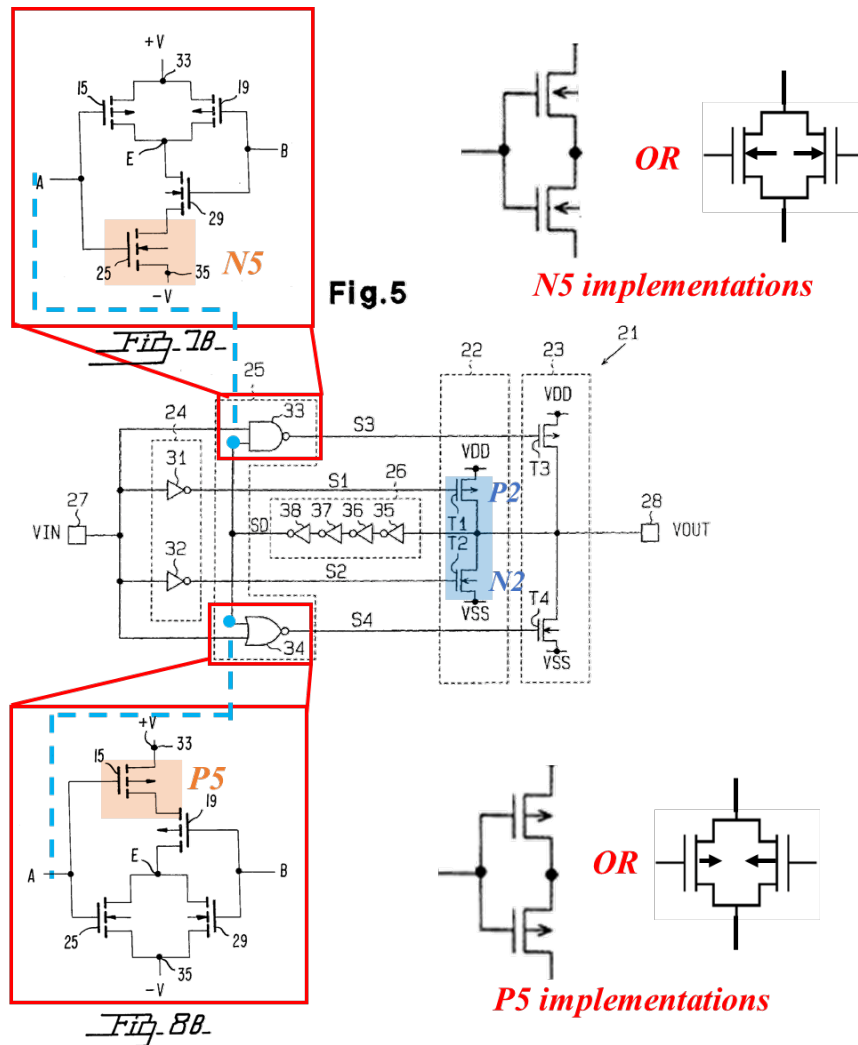
known to use transistors connected in series for driving output transistors. *See*, e.g., EX1008, Borkar, FIG. 3 (transistors 46 and 46 connected in series for driving transistor 37, and transistors 47 and 48 connected in series for driving output transistor 35).



EX1008, Borkar, FIG. 3, annotated

136. As shown in the figure below, in Example Combination 1.1, a POSITA would have been motivated to implement one or more transistors (e.g., P5 or N5) each using two or more MOS transistors (e.g., connected in series or parallel) of the same type as well-known in the art, for the benefit of design

flexibility and element sizing control. In such examples, the number of P2 and N2 (a total of two) is different from the number of N5 and P5 (e.g., 3, 4, etc.).



Example Combination 1.1
Itoh Embodiment 1 (FIG. 5) combined with Skorup

137. In another example, a POSITA would have been implemented have been motivated to implement one or more of the second p-channel MOS transistor (P2) and the second n-channel MOS transistor (N2) each using two or more MOS

transistors (e.g., connected in series or parallel) of the same type as well-known in the art, for the benefit of design flexibility and element sizing control. In such examples, the number of P2 and N2 (e.g., 3, 4) is different from the number of N5 and P5 (2).

138. Therefore, Itoh in view of Skorup in further view of a POSITA's general knowledge of basic transistors and logic design renders obvious that "*the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are different from each other*" recited in the claim.

5. Claim 5

[5.0] *5. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:*

139. Itoh teaches this element for the reasons discussed at [1.0].

[5.1] *a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [P2] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];*

140. Itoh teaches this element for the reasons discussed at [1.1].

[5.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [P1] and only said first p-channel MOS transistor [N1]

141. Itoh teaches this element for the reasons discussed at [1.2.1].

[5.2.2] [the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

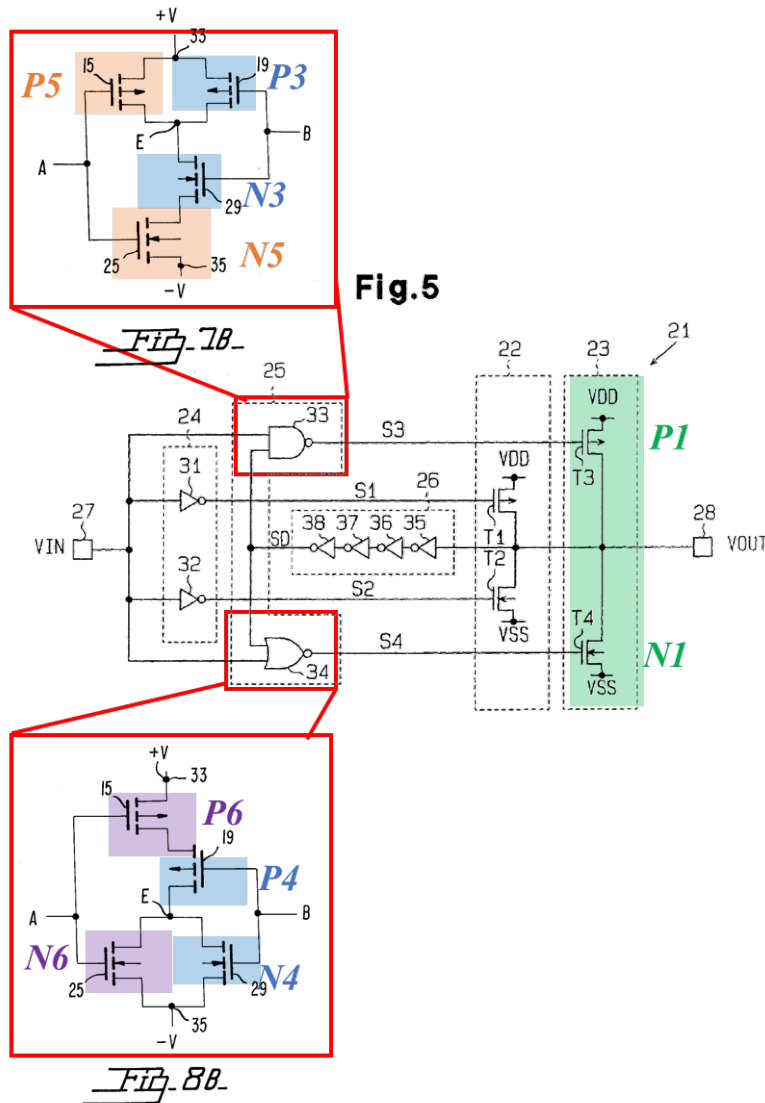
142. Itoh in view of Skorup renders obvious this element for the reasons discussed at [1.2.2].

[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

143. Itoh in view of Skorup renders obvious this element.

144. As shown in the figure of Example Combination 1.1 (Itoh Embodiment 1 (FIG. 5) combined with Skorup) below, in the combination, the predriver 25 includes NAND gate 33 and NOR gate 34, each implemented with complementary PMOS and NMOS transistors as taught by Skorup. In the Example Combination 1.1, the predriver 25 has N5 (EX1007, Skorup, FIG. 7B, 25) for driving P1 (by sending S3 generated at output terminal E of FIG. 7B to the gate of P1) in coaction with N3 (EX1007, Skorup, FIG. 7B, 29), because N3 and N5 are connected in series and work together for generating the output signal S3 at output

terminal E of FIG. 7B.



Example Combination 1.1
Itoh Embodiment 1 (FIG. 5) Combined with Skorup

145. Further, the predriver 25 has P5 (EX1007, Skorup, FIG. 7B, 15) for driving P1 (by sending S3 generated at output terminal E of FIG. 7B to the gate of

P1) in coaction with P3 (EX1007, Skorup, FIG. 7B, 19), because P3 and P5 are connected in parallel and work together for generating the output signal S3 at output terminal E of FIG. 7B.

146. In the combination, the configuration of P5 for driving P1 in coaction with P3 (where P3 and P5 are connected in parallel for generating S3 for driving P1) and the configuration of N5 for driving P1 in coaction with N3 (where N3 and N5 are connected in series for generating S3 for driving P1) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g., '539 patent, FIG. 3* (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction). A POSITA would have understood that two transistors connected either in series or in parallel are working in coaction for generating the output signal.

147. Similar analysis applies to the combination of Skorup with Embodiment 2 of FIG. 8 of Itoh (Example Combination 1.2) and the combination of Skorup with Embodiment 3 of FIG. 9 of Itoh (Example Combination 1.3).

148. Therefore, Itoh in view of Skorup renders obvious that “[a predriver ...having...] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],” as recited in the claim.

[5.2.4] *[the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and*

149. Itoh in view of Skorup renders obvious this element.

150. Continuing with the Example Combination 1.1 (Itoh Embodiment 1 (FIG. 5) combined with Skorup) below, the predriver 25 includes NAND gate 33 and NOR gate 34, each implemented with complementary PMOS and NMOS transistors as taught by Skorup. In the Example Combination 1.1, the predriver 25 has P6 (EX1007, Skorup, FIG. 8B, 15) for driving P1 (by sending S4 generated at output terminal E of FIG. 8B to the gate of N1) in coaction with P4 (EX1007, Skorup, FIG. 8B, 19), because P6 and P4 are connected in series and work together for generating the output signal 43 at output terminal E of FIG. 8B.

output terminal E of FIG. 8B.

152. As shown in the figure above, in the combination, the configuration of N6 for driving N1 in coaction with N4 (where N6 and N4 are connected in parallel for generating S4 for driving N1) and the configuration of P6 for driving N1 in coaction with P4 (where P4 and P5 are connected in series for generating S4 for driving N1) are similar to configurations of those corresponding transistors in the '539 patent. *See, e.g.,* '539 patent, FIG. 3 (illustrating QN11 and QN 15 connected in series for driving QP1 in coaction). A POSITA would have understood that two transistors connected either in series or in parallel are working in coaction for generating the output signal.

153. Similar analysis applies to the combination of Skorup with Embodiment 2 of FIG. 8 of Itoh (Example Combination 1.2) and the combination of Skorup with Embodiment 3 of FIG. 9 of Itoh (Example Combination 1.3).

154. Accordingly, Itoh in view of Skorup renders obvious “[a predriver ...having...] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [P1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]” as recited.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

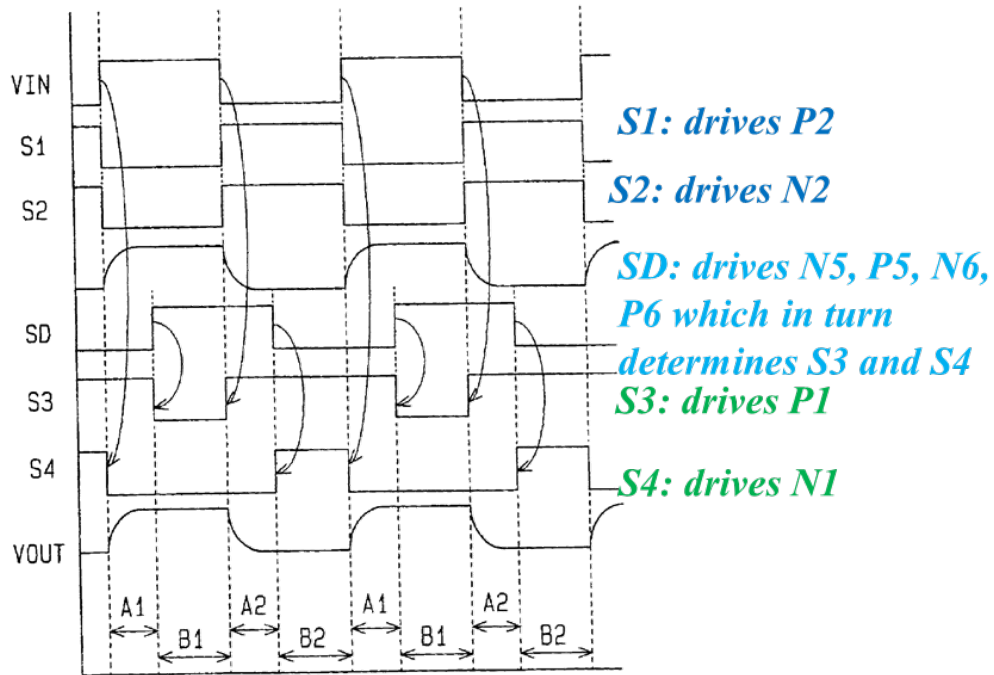
155. Itoh in view of Skorup renders obvious this element.

156. As shown in the figure of Example Combination 1.1 (combination of Itoh Embodiment 1 of FIG. 5 and Skorup) below, a controller (including inverter 24 and delay circuit 26) is supplied with the external output signal VOUT, and outputs the control signals (including SD, S1, and S2). The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters. Itoh, 7:51:8-5.

to supply the control signal SD to NOR gate 34, by supplying the control signal SD to the gates of P6 and N6 (e.g., through terminal A of FIG. 8B), which turns N6 and P6 into and out of operation. As discussed in more detail with reference to FIG. 6 of Itoh below, in the combination, control signal SD, working together with control signal S1, controls P5 and N5 into and out of operation in coaction with P2. Further, control signal SD, working together with control signal S2, controls P6 and N6 into and out of operation in coaction with N2.

158. As shown in annotated FIG. 6 of Itoh below, in Example Combination 1.1, signals (e.g., S1, S2, SD, S3, and S4) drive transitions (e.g., P1, N1, P5, N5, P2, N2, P6, N6) work in coaction to provide VOUT with the desired slew rate and impedance. I have also provided the corresponding operation states of the signals and transistors of Example Combination 1.1.

Fig.6



Itoh, FIG. 6, annotated

	A1	B1	A2	B2
VIN	L→H	H	H→L	L
S1/P2	L/On	L/On	H/Off	H/Off
SD/N5	L/Off	H/On	H/On	L/Off
SD/P5	L/On	H/Off	H/Off	L/On
S3/P1	H/Off	L/On	H/Off	H/Off
S2/N2	L/Off	L/Off	H/On	H/On
SD/P6	L/On	H/Off	H/Off	L/On
SD/N6	L/Off	H/On	H/On	L/Off
S4/N1	L/Off	L/Off	L/Off	H/On
VOUT	Rising	VPP	Falling	VSS

Example Combination 1.1, Operation States

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Itoh Embodiment 1 (FIG. 5) combined with Skorup (FIGS. 7B and 8B)

159. As shown in the table of operation states above, control signal SD, together with control signal S1, controls N5 and P5 into and out of operation in coaction with P2, so that N5, P5, and P2 have the required states at each of the A1, B1, A2, and B2 periods to provide VOUT with the desired slew rate and impedance. For example, SD controls the states of N5 and P5, which determines S3 together with VIN, and S3 drives P1 in coaction with P2 to generate VOUT. When VIN is switching from L to H, during A1, the high-impedance P2 is turned on by control signal S1 to control slew rate for a gentle rising edge (VOUT increasing slower with P2 having a high impedance). In coaction with P2, low impedance P1 and N1 are turned off by S3 and S4, so that they do not decrease the impedance to affect the gentle rising. During B1 (static state where VOUT is sufficiently stable at VDD), low-impedance P1 is turned on to provide low output impedance.

160. Furthermore, as shown in the table of operation states above, control signal SD, together with control signal S2, controls P6 and N6 into and out of operation in coaction with N2, so that P6, N6, and N2 have the required states at each of the A1, B1, A2, and B2 periods to provide VOUT with the desired slew rate and impedance. For example, SD controls the states of P6 and N6, which determine S4 together with VIN, and S4 drives N1 in coaction with N2 to generate

VOUT. Specifically, when VIN is switching from H to L, during A2, the high-impedance N2 is turned on by control signal S2 to control the slew rate for a gentle falling edge (VOUT dropping slower with N2 having a high impedance). Low impedance P1 and N1 are turned off by S3 and S4. During B2 (static state where VOUT is sufficiently stable at VSS), low-impedance N1 is turned on by S4 to provide low output impedance.

161. Accordingly, Itoh in view of Skorup renders obvious “a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2].”

[5.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.

162. Itoh teaches this element for the reasons discussed at [1.4].

6. Claim 6

[6.0] 6. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistor [P5], said sixth n-channel MOS transistor [N6], and said sixth p-channel MOS transistor [P6] are equal to each other.⁶

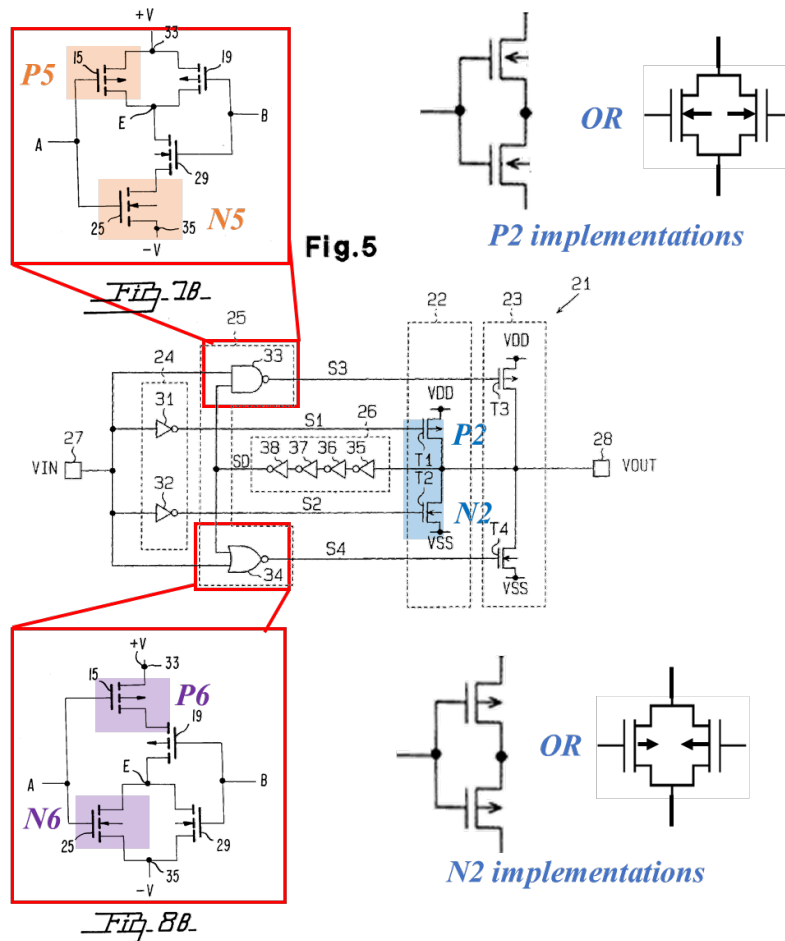
163. Itoh in view of Skorup, in further view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element.

164. As discussed at [3.0] above, it is the basic, fundamental knowledge of a POSITA that a transistor shown in a circuit diagram as a single transistor can be physically implemented using multiple resistors in series or in parallel. As shown below, as shown Example Combination 1.1 illustrated below, a POSITA would have been motivated to implement a transistor (e.g., P2 and N2) using two or more

⁶ There is no antecedent basis for the plural "*transistors*" as recited in "*second p-channel MOS **transistors** and said second n-channel MOS **transistors**,*" "*said fifth n-channel MOS **transistors**,*" "*said fifth p-channel MOS **transistors**,*" "*said sixth n-channel MOS **transistors**,*" and "*said sixth p-channel MOS **transistors***" of claims 6 and 7. Instead, claim 5 recites "*at least a pair of a first p-channel MOS **transistor** and a first n-channel MOS **transistor**,*" "*at least a pair of a second p-channel MOS **transistor** and a second n-channel MOS **transistor**,*" etc. As such, a POSITA would have understood that "*transistors*" as recited in claims 6 and 7 includes "at least a transistor."

unit transistors connected in series or parallel, to achieve desired properties

including desired transistor size.



Example Combination 1.1 Itoh Embodiment 1 (FIG. 5) combined with Skorup

165. In Example Combination 1.1 where P2 is implemented using two unit transistors and N2 is implemented using two unit transistors, the number of P2 and N2 is four. On the other hand, the number of N5, P5, N6, and P6 is 4. As such, the number of P2 and N2 is equal to the number of N5, P5, N6, and P6.

166. Therefore, Itoh in view of Skorup in further view of a POSITA's general knowledge of basic transistors and logic design renders obvious that "*the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistor [P5], said sixth n-channel MOS transistor [N6], and said sixth p-channel MOS transistor [P6] are equal to each other,*" as recited in the claim.

7. Claim 7

[7.0] *7. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistors [P5], said sixth n-channel MOS transistors [N6], and said sixth p-channel MOS transistors [P6] are different from each other.*

167. Itoh in view of Skorup renders obvious this element.

168. Specifically, as shown in Example Combination 1.1 illustrated below, in the output buffer circuit, the number of P2 and N2 is two. The number of N5, P5, N6, and P6 is four. As such, these numbers are different from each other.

C. Ground 2: Claims 1-8 are Rendered Obvious under 35 U.S.C. § 103(a) over Itoh.

170. In my opinion, Itoh renders claims 1–8 of the '539 patent obvious. To the extent that the Patent Owner argues that a single embodiment of Itoh does not disclose all the limitations of any of claims 1–8, a POSITA would have found claims 1-8 obvious, in view of the POSITA's own knowledge and the disclosures provided by Itoh's other embodiments as explained herein.

1. Reasons to Combine Embodiments of Itoh

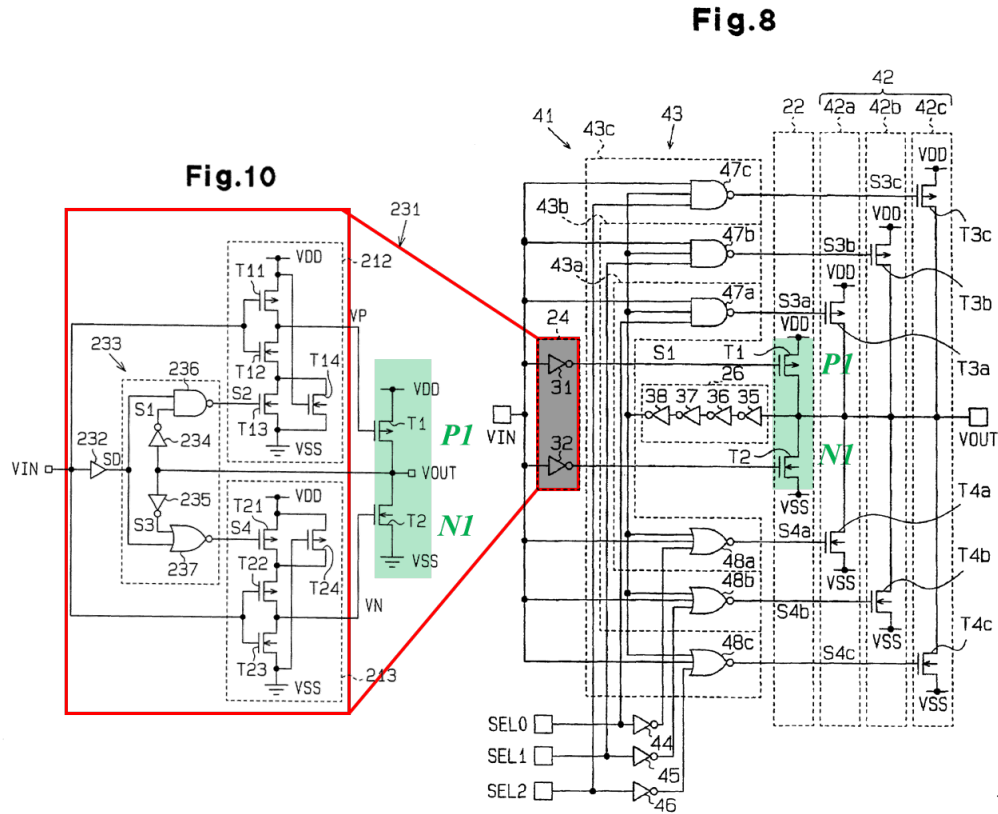
171. A POSITA would have been motivated to combine two embodiments in Itoh to provide an output buffer circuit with improved slew rate and output impedance control. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F. 3d 982, 991 (“Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.”).

172. As discussed at VIII.A.1, to provide an output buffer circuit capable of outputting a signal which has less variation in transition time and that can cope with a high or low operational frequency, Itoh describes embodiments of two categories. In Category 1 (Embodiments 1, 2, and 3), the main driver uses a single pair of PMOS and NMOS transistors for achieving slew-rate control, and additional pair(s) of PMOS and NMOS transistors for additional impedance control during the static state when VOUT is sufficiently stable. In Category 2

(Embodiments 4 and 5), the main driver uses a single pair of PMOS and NMOS transistors for both slew-rate control and impedance control, and the output buffer circuit has a controller that controls the slew rates of the control signals applied to the output transistors to control the slew rate of the output signal.

173. A POSITA would have been motivated to combine an embodiment from Category 1 and another embodiment from Category 2 to achieve the obvious, beneficial, and predictable results of an output buffer circuit having improved slew rate control (e.g., by using the slew-rate control type circuit as taught by Category 2) and improved impedance control (e.g., by using the additional pair(s) of output transistors turned on only during the static state as taught by Category 1).

174. A figure of Example Combination 2.1 (Embodiments 2 and 4 of Iton combined) is illustrated below. While the analysis below focuses on Example Combination 2.1 (Embodiments 2 and 4 of Iton combined), the analysis similarly applies to other combinations (e.g., one of Category 1 (Embodiments 1, 2, 3) combined with another of Category 2 (Embodiments 4 and 5)). Each embodiment has its own advantages, and a POSITA would have been motivated to select the corresponding embodiments for combination based on its design needs. For the sake of the present analysis, I will go forward with the combination of Embodiments 2 and 4.



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

175. As shown in Example Combination 2.1 illustrated above, a POSITA would have been motivated to combine Embodiment 2 (FIG. 8) with Embodiment 4 (FIG. 10) to achieve improved output impedance control and slew rate control. It would have been obvious to apply FIG. 10's slew-rate control type circuit for driving the pair of output transistors T1 and T2 (annotated as P1 and N1) to drive the same pair of output transistors T1 and T2 (also annotated as P1 and N1) in FIG. 8. Example Combination 2.1 achieves improved output impedance control (provided by circuit 42 of FIG. 8 with the additional pairs of output transistors) and

improved slew rate control (provided by the slew-rate control type circuit of FIG.

10), with advantages of FIG. 10 including “reduc[ing] consumed current,”

“shortening the propagation delay time,” providing “a wide frequency band,”

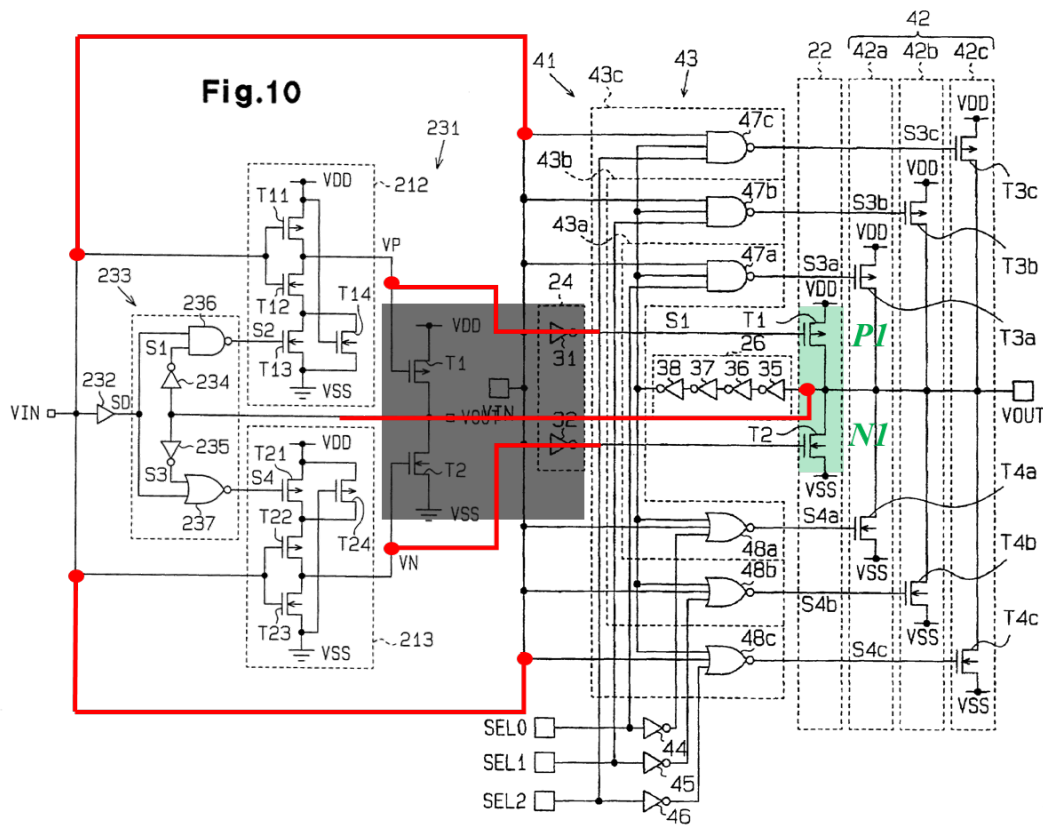
providing the VOUT “whose pulse width is substantially equal to the pulse width

of the input signal VIN,” and “reduc[ing] the possible noise-oriented interference

on the interface with the receiving side.” Itoh, 14:19-62.

176. As shown in an example implementation below, combining Embodiments of Itoh would have been no more than the combination of known elements (well-known components of an output driver) according to known methods (performing basic IC design).

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

177. As shown above, any modification required for the combination would have been within the skills of a POSITA⁷. It would have obvious to include

⁷ I have greyed-out circuits not used in Example Combination 2.1. These greyed out circuits include transistors T1 (P1) and T2 (P2) of Embodiment 4 (FIG. 10), which also exits in Embodiment 2 (FIG. 8). Further, circuit 24 driving T1 and T2 in Embodiment 2 (FIG. 8) is greyed out, because in the combination, T1 and T2 are driven by VP and VN from Embodiment 4 (FIG. 10). In analysis below, the greyed-out circuits are removed from the figure to avoid any confusion.

various connections (e.g., supplying VOUT of FIG. 8 as input control signal to circuit 233 of FIG. 10; supplying VP of FIG. 10 as S1₈ of FIG. 8 to control T1 (P1), and supplying VN of FIG. 10 as S2₈ of FIG. 8 to control T2 (N1))⁸. Further, it would have been obvious to adjust the delay time of delay circuit 26 (e.g., by adjusting the number of pairs of inverters according to the well-known self-timed control technique) according to the rising/falling times such that the additional pairs of output transistors in circuit 42 are only turned on during static state for impedance control. Further, it would have been obvious to adjust the sizes of one or more of the output transistors (T1, T2, T3a-c, T4a-c) based on the design needs (e.g., required output impedance and slew rate).

2. Claim 1

[1.0] 1. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

178. To the extent that this preamble is limiting, Itoh teaches the preamble.

179. First, as discussed at Ground 1:[1.0], embodiments of Itoh teach the preamble.

180. Second, as discussed in detail below, combinations of embodiments

⁸ The driving signals from circuit 24 to T1 and T2 in FIG. 8 are referred to as S1₈ and S2₈ to distinguish from S1 and S2 of FIG. 10.

of Itoh, e.g., Exmple Embodiment 2.1 (Embodiments 8 and 10 combined), similarly provide an output buffer circuit that outputting data (VIN) in the form of an input pulse train, with output impedance control and slew rate control.

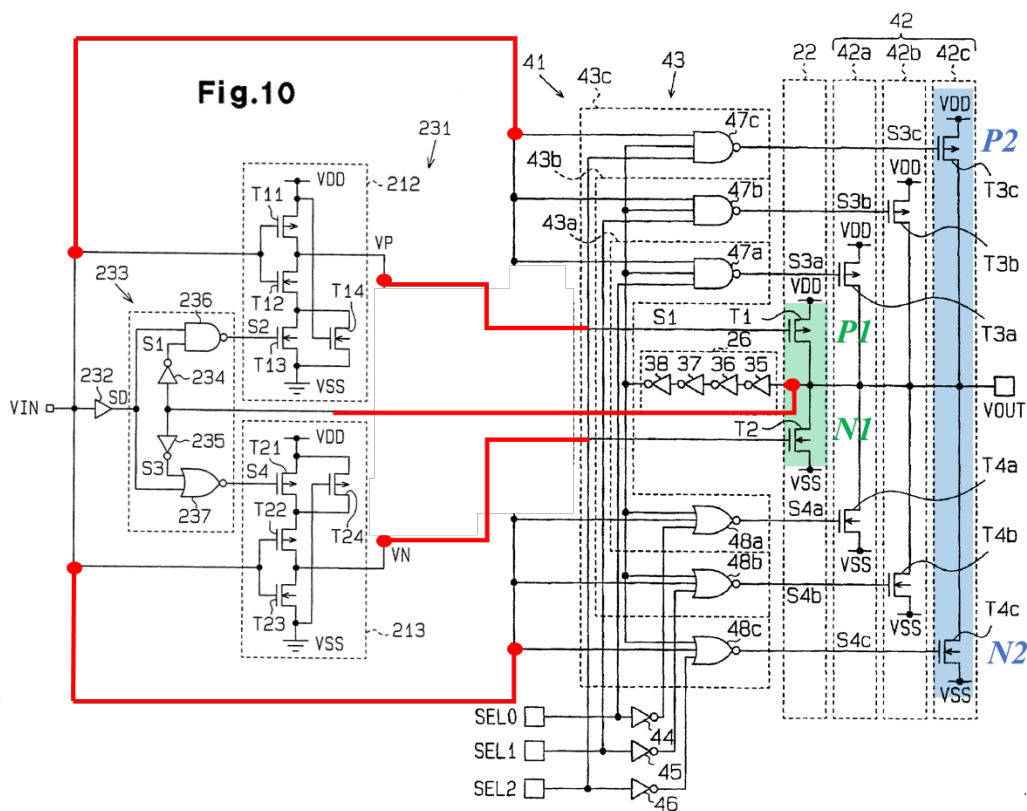
181. Therefore, Itoh teaches “an output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate” as recited.

[1.1] *a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];*

182. Itoh teaches this element.

183. As discussed at Ground 2: Reasons to Combine and as shown in Example Combination 2.1 (Combination of Embodiments 2 and 4) below, it would have been obvious to combine embodiments of Itoh to provide an output driver circuit with improved slew rate and output impedance control.

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

184. As shown in Example Combination 2.1, Itoh describes a main driver including circuits 22 and 42 with pairs of p-channel MOS transistor and n-channel MOS transistors for driving a load according to VIN by providing a VOUT. It was well-known in the art that an output driver circuit as described in Itoh generates an output signal (e.g., VOUT) that drives an external load. *See, e.g.,* EX1008, Borkar, 1:51-53 (“the drivers drive the external load by placing a signal on its

corresponding pin or pad 19”).

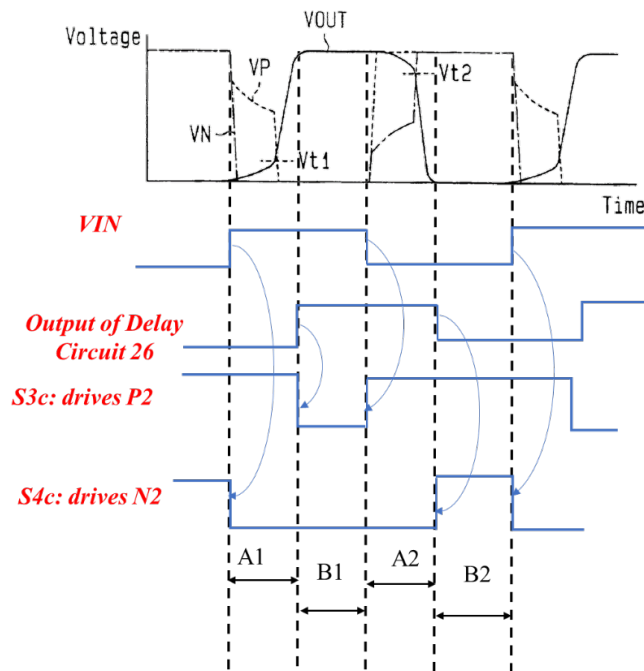
185. Specifically, the main driver includes circuit 22, which includes a pair of a first p-channel MOS transistor (transistor T1 in Fig. 8, annotated in green above as P1) and a first n-channel MOS transistor (transistor T2 in Fig. 8, annotated in green as N1) for driving a load at output VOUT according to the input data VIN. Specifically, P1 and N1 are controlled by VP and VN to achieved desired rising/falling times. EX1006, Itoh, 12:48-13:62.

186. The main driver further includes circuit 42, which includes a pair of a second p-channel MOS transistor (transistor T3c in Fig. 8, annotated in blue above as P2) and a second n-channel MOS transistor (transistor T4c in Fig. 8, annotated in blue above as N2). This pair of P2 and N2 works together with the pair of P1 and N2 for generating the VOUT for driving the load, and as such, drives the load in coaction with the pair of P1 and N1. EX1006, Itoh, 10:1-15 (The output buffer circuit 41 alters the output impedance value....The sub-drive circuits 42a, 42b and 42c respectively include **PMOS transistors (output transistors) T3a to T3c and NMOS transistors (output transistors) T4a to T4c**. At least one of the PMOS transistors T3a-T3c has a different impedance from those of the other.”); EX1006, Itoh, 10:37-42 (“The output buffer circuit 41 has the second drive circuit 42 that includes three sub-drive circuits 42a-42c having different impedances. In accordance with the select signals SEL0 to SEL2, at least one of the sub-drive

circuits 42a-42c is enabled to **select the output impedance** when the output signal VOUT is in a static state.”).

187. The waveforms of Example Combination 2.1⁹ below illustrate the details of how the pair of P2 and N2 (driven by signals S3c and S4c) drives the load in coaction with the pair of P1 and N1. Specifically, P2 and N2 are turned off during periods A1 and A2, during which period P1 and N1 are controlled by VP and VN (generated based on VOUT) for slew rate control. During B1 and B2 when VOUT is substantially stable, P2 and N2 are turned on for output impedance control. Each of VP, VN, S3c, and S4c for controlling P1, N1, P2, N2 are generated based on both VIN and VOUT.

⁹ Illustrating the case where P2 and N2 are selected.



**Waveforms of Example Combination 2.1
(Annotated using EX1006, Itoh, FIG. 11)**

188. Therefore, Itoh teaches “a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [N1] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1]” as recited in the claim.

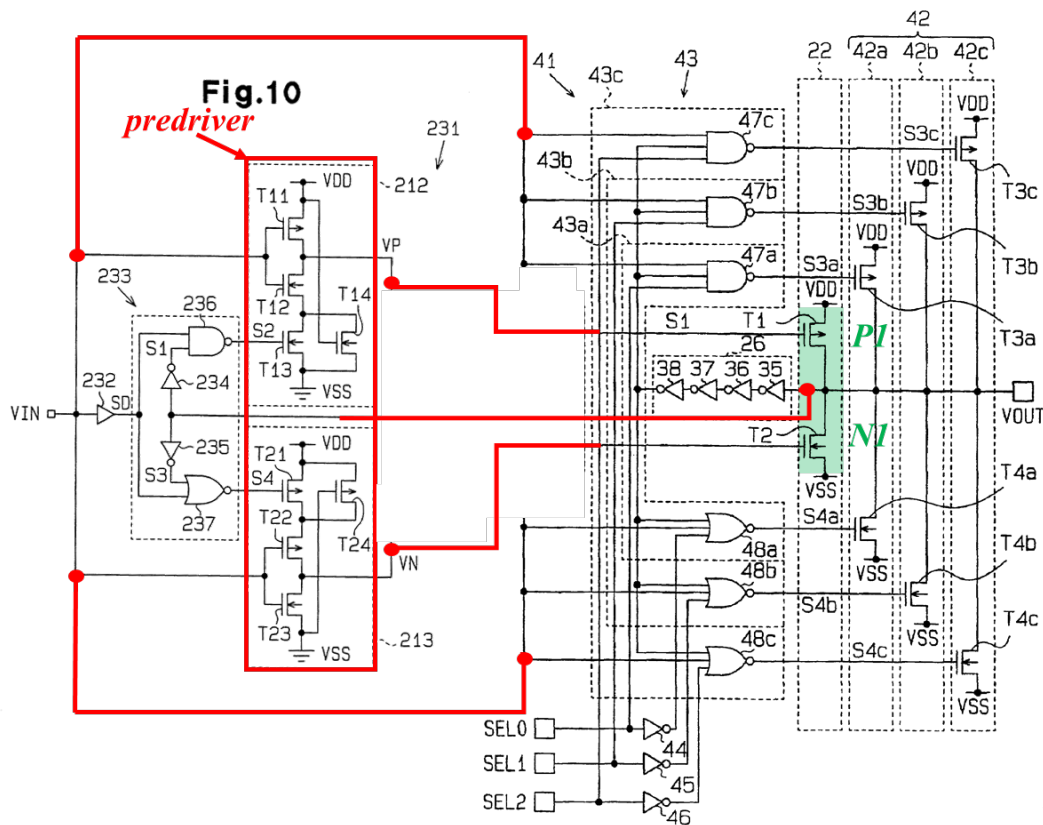
[1.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1]

189. Itoh teaches this element.

190. Continuing with Example Combination 2.1 as illustrated below,

Example Combination 2.1 discloses a predriver (circuits 212 and 213) positioned before the main driver (circuits 22 and 42), and provides signals VP and VN for driving only P1 and only N1 in the main driver.

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

191. Referring to FIG. 10, Itoh describes a predriver (including circuits 212 and 213) with outputs (VP and VN) for driving only a first in-channel p-channel MOS transistor (T1) and only a first n-channel MOS transistor (T2). EX1006,

Itoh, 11:11-20 (“first and second slew-rate control circuits (hereinafter simply called “control circuits”) 212 and 213 which perform the ON/OFF control of the respective output transistors T1 and T2 in response to the external input signal VIN, a delay circuit 232 and a signal generator 233.”). As shown in Example Combination 2.1, in the combination, these functions remain the same, where the predriver’s output (VP and VN) is for driving only said first n-channel MOS transistor (T1 annotated as P1) and only said first p-channel MOS transistor (T2 annotated as P2) of the main driver.

192. Therefore, Itoh teaches “a predriver with outputs for driving only said first n-channel MOS transistor [N1] and only said first p-channel MOS transistor [P1],” as recited in the claim.

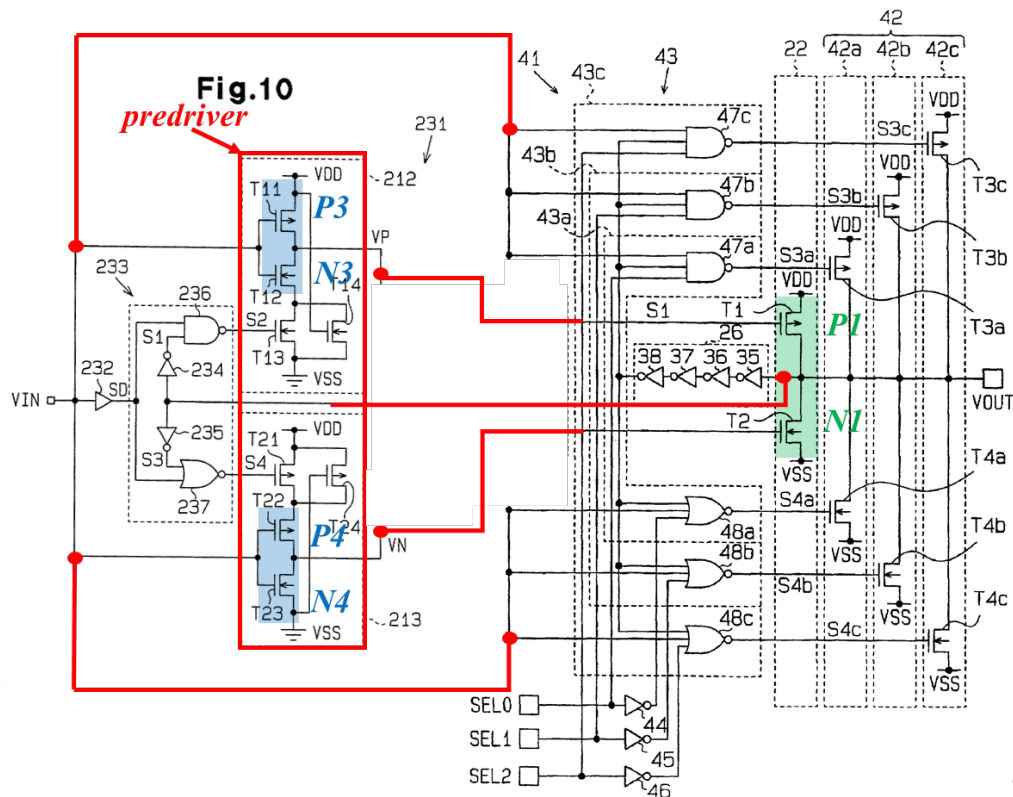
[1.2.2] [the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

193. Itoh teaches this element.

194. Continuing with Example Combination 2.1 as illustrated below, Example Combination 2.1 discloses a predriver (circuits 212 and 213), where its circuit 212 includes at least a pair of a third p-channel MOS transistor (T11 annotated as P3) and a third n-channel MOS transistor (T12 annotated as N3) for driving P1 according to said data (VIN). EX1006, Itoh, 13:24-30 (“When the

external input signal VIN changes its level to the L level from the H level, **the NMOS transistor T12 is turned off immediately and the PMOS transistor T11 is turned on.** This causes the **control signal VP to sharply rise to the H level from the L level**, so that the first output transistor T1 is turned off immediately.”).

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

195. Further, as shown in Example Combination 2.1 illustrated above, the predriver includes circuit 212, which includes has at least a pair of a fourth p-channel MOS transistor (T22 annotated as P4) and a fourth n-channel MOS

transistor (T23 annotated as N4) for generating VN, which drives N1 according to said data (VIN). EX1006, Itoh, 12:50-56 (“When the external input signal VIN changes its level to the H level from the L level, a **PMOS transistor T22** is turned off immediately and an **NMOS transistor T23** is turned on. **This causes the control signal VN to sharply fall to the L level from the H level**, so that **the second output transistor T2 is turned off immediately.**”). As such, in Example Combination 2.1, in the predriver, a fourth p-channel MOS transistor (T22 annotated as P4) and a fourth n-channel MOS transistor (T23 annotated as N4) are controlled by VIN, and generate VN for driving N1 according to said data (VIN).

196. Therefore, Itoh teaches “[a predriver...] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data” as recited in the claim.

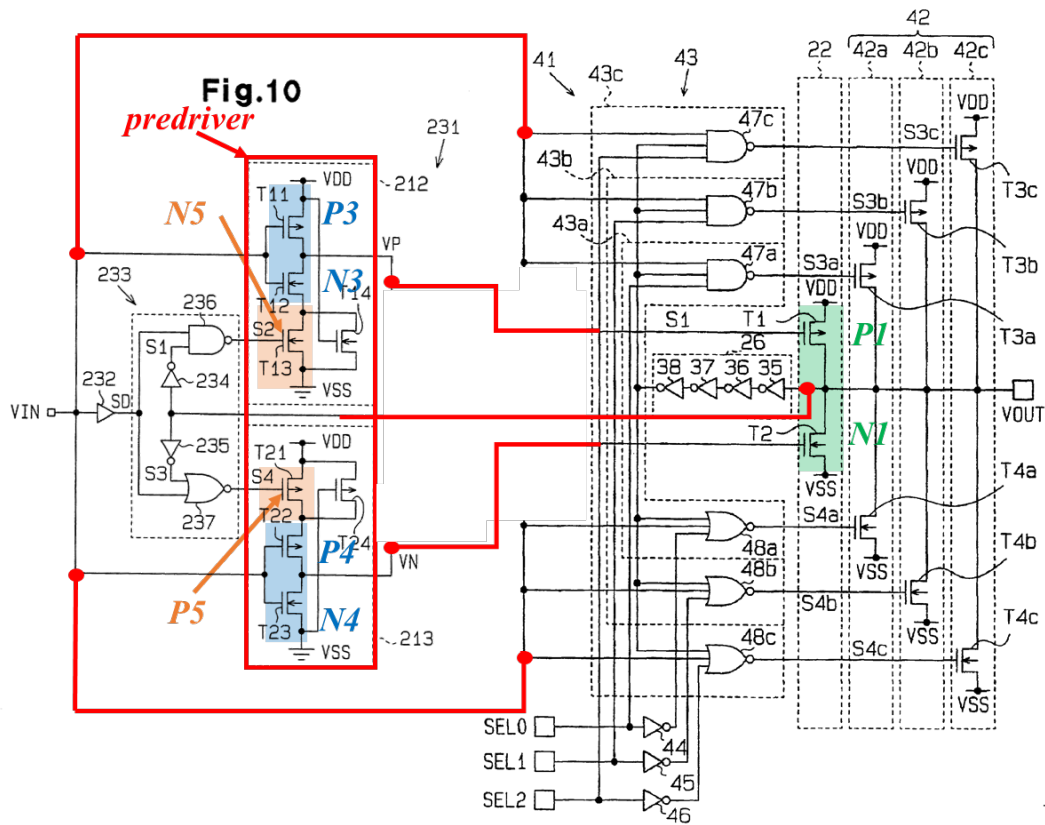
[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

197. Itoh teaches this element.

198. Continuing with Example Combination 2.1 as illustrated below,

Example Combination 2.1 discloses that the predriver's circuit 212 includes at least one fifth n-channel MOS transistor (T13 annotated as N5) for driving said first p-channel MOS transistor (T1 annotated as P1) in coaction with said third n-channel MOS transistor (T12 annotated as N3).

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

199. Specifically, as shown in Example Combination 2.1 above, N5 and N3 are connected in series and work together to generate VP (e.g., working

together to control how fast VP rises and falls), where VP drives P1. EX1006, Itoh, 11:51-12:4 (“the signal generator 233 turns on the NMOS transistor T13 for a predetermined time since the rising of the external input signal VIN, temporarily turns off the NMOS transistor T13, and turns on the NMOS transistor T13 again in accordance with the level of the external output signal VOUT. The **ON/OFF of the NMOS transistor T13 determines the falling waveform of a control signal VP** (i.e., the rising waveform of the external output signal VOUT.) Specifically, **the control signal VP falls sharply while the NMOS transistor T13 is on**, and falls gently due to the ON resistance of an NMOS transistor T14 while the NMOS transistor T13 is off. Therefore, the external output signal VOUT rapidly reaches an operation start point as the NMOS transistor T13 is turned on at the rising of the external input signal VIN, and the external output signal VOUT gently rises as the NMOS transistor T13 is turned off. When the external output signal VOUT exceeds the threshold voltage V_{t1} , the NMOS transistor T13 is turned on again, causing the external output signal VOUT to sharply rise to the H level.”).

200. Similarly, circuit 213 of the predriver includes at least one fifth p-channel MOS transistor (T21 annotated as P5) for driving said first n-channel MOS transistor (T2 annotated as N1) in coaction with said fourth p-channel MOS transistor (T22 annotated as P4). Specifically, P5 and P4 are connected in series and work together to generate VN (e.g., working together to control how fast VN

risers and falls), which drives N1. EX1006, Itoh, 12:28-47 (“the signal generator 233 turns on the PMOS transistor T21 for a predetermined time since the falling of the external input signal VIN, temporarily turns off the PMOS transistor T21, and turns on the PMOS transistor T21 again in accordance with the level of the external output signal VOUT. **The ON/OFF of the PMOS transistor T21 determines the rising waveform of a control signal VN (i.e., the falling waveform of the external output signal VOUT).** Specifically, **the control signal VN rises sharply while the PMOS transistor T21 is on**, and rises gently due to the ON resistance of a PMOS transistor T24 while the PMOS transistor T21 is off. Therefore, the external output signal VOUT rapidly reaches the operation start point as the PMOS transistor T21 is turned on at the falling of the external input signal VIN, and the external output signal VOUT gently falls as the PMOS transistor T21 is turned off. When the external output signal VOUT exceeds the threshold voltage V12, the PMOS transistor T21 is turned on again, causing the external output signal VOUT to sharply fall to the L level.”)

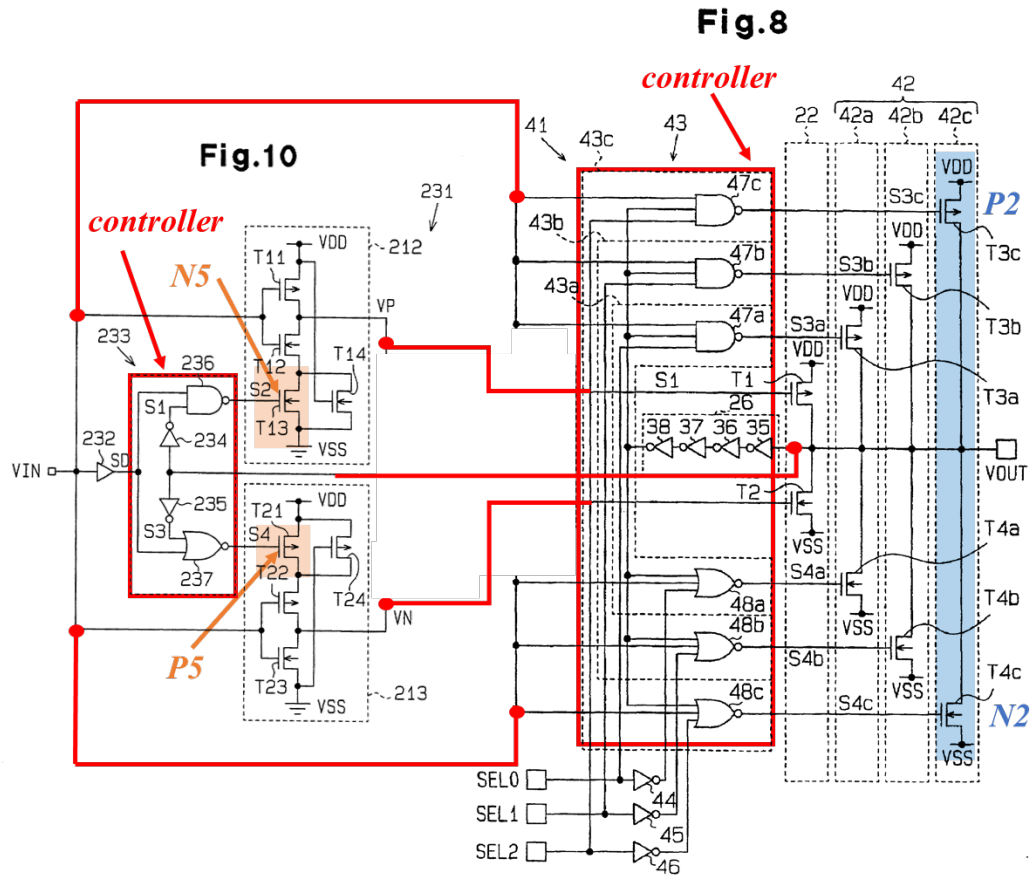
201. Therefore, Itoh teaches “[a predriver...having...] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]” as recited in the claim.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

202. Itoh teaches this element.

203. Continuing with Example Combination 2.1 as illustrated below,

Example Combination 2.1 teaches a controller (including signal generator 233 of FIG. 10 and control circuits 26 and 43 of FIG. 8) that receives VOUT as a feedback signal and VIN, and generates control signals (e.g., S2 for driving N5 in coaction with S3c for driving P2, and S4 for driving P5 in coaction with S4c for driving N2) based on VOUT and VIN. The delay circuit 26 was a well-known self-timed control circuit for providing a control signal based on the feedback VOUT (which by itself is considered a control signal) by adjusting the number of pairs of inverters.



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

204. As shown in Example Combination 2.1 illustrated above, controller generates control signals S2 to control said fifth n-channel MOS transistor N5 into and out of operation in coaction with said second p-channel MOS transistor P2, because the control signal S4 (driving N5 into and out of operation) and control signal S3c (driving P2) are generated using the same feedback VOUT (which itself is also considered a control signal) and VIN, and therefore are in coaction with each other. This configuration of controlling N5 into and out of operation in

coaction with P2 is similar to the configuration in the '539 patent. *See, e.g.,* '539 patent, FIGS. 3, 4, and 7 (illustrating controlling N5 (e.g., QN17) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for N5 and P2 are each generated using the same signals $\phi 3$ and VIN).

205. Further, in the combination, the controller generates control signal S4 to control said fifth p-channel MOS transistor P5 into and out of operation in coaction with said second n-channel MOS transistor N2, because the control signal S4 (driving P5 into and out of operation) and control signal S4c (driving N2) are generated using the same feedback VOUT (which itself is also considered a control signal) and VIN, and therefore are in coaction with each other. This configuration of controlling P5 into and out of operation in coaction with N2 is similar to the configuration in the '539 patent. *See, e.g.,* EX1001, '539 patent, FIGS. 3, 4, and 7 (illustrating controlling P5 (e.g., QP27) into and out of operation in coaction with N2 (e.g., QN2) where the control signals for P5 and N2 are each generated using the same signals $\phi 6$ and VIN).

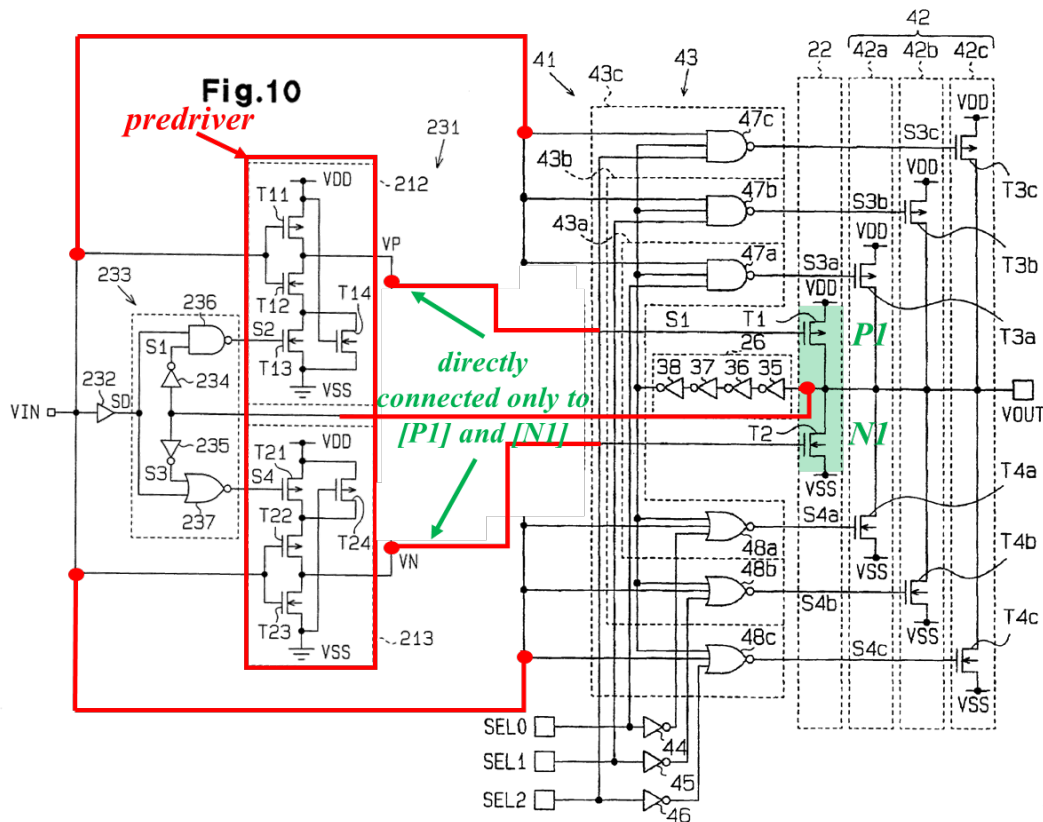
206. Therefore, Itoh teaches “a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],” as recited in the claim.

[1.4] wherein the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1] of said main driver.

207. Itoh teaches this element.

208. Continuing with Example Combination 2.1 as illustrated below, Itoh teaches the output (control signals VP and VN) of the predriver (circuits 212 and 213) is directly connected only to said first p-channel MOS transistor (T1 annotated as P1) and said first n-channel MOS transistor (T2 annotated as N1) of said main driver.

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

209. Therefore, Itoh discloses or renders obvious that “the output of the predriver is directly connected only to said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [P2] of said main driver” as recited in the claim.

3. Claim 2

[2.0] 2. The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other.¹⁰

210. Itoh teaches this element.

211. Example Combination 2.2 (Combination of Embodiments 1 and 4) as shown below¹¹ teaches this element. First, Example Combination 2.2 teaches

¹⁰ There is no antecedent basis for the term “*transistors*” recited in “*second p-channel MOS **transistors** and said second n-channel MOS **transistors** and the number of said fifth n-channel MOS **transistors** and said fifth p-channel MOS **transistors***” of claims 2 and 3. Instead, claim 1 recites “*at least a pair of a first p-channel MOS **transistor** and a first n-channel MOS **transistor** for driving a load according to said data, and at least a pair of a second p-channel MOS **transistor** and a second n-channel MOS **transistor**.*” As such, a POSITA would have understood that the term “*transistors*” as recited in claims 2 and 3 includes “at least a transistor.”

¹¹ The transistors T1 (P1) and T2 (P2) exist in both Embodiments 1 and 4. I have removed these transistors from Embodiment 4 (Fig. 10) to avoid any confusion. I have also removed circuit 24 driving T1 and T2 from Embodiment 1 (FIG. 5),

Fig. 10

The circuit in Fig. 10 is a differential pair. It features two PMOS transistors, T11 and T14, connected to VDD, and two NMOS transistors, T13 and T14, connected to VSS. The gates of T11 and T14 are connected to a common gate voltage VP. The gates of T13 and T14 are connected to a common gate voltage VN. The drains of T11 and T14 are connected to a common drain voltage VDD. The sources of T13 and T14 are connected to a common source voltage VSS. A current source 231 is connected between VDD and VSS. The input VIN is connected to the gates of T11 and T14. The output VOUT is connected to the drains of T11 and T14. The circuit is labeled with various components: 231, 212, 233, 236, 234, 235, 237, 22, 213, 232, and 23.

Fig. 5

The circuit in Fig. 5 is a differential pair. It features two PMOS transistors, T3 and T4, connected to VDD, and two NMOS transistors, T1 and T2, connected to VSS. The gates of T3 and T4 are connected to a common gate voltage VDD. The gates of T1 and T2 are connected to a common gate voltage VSS. The drains of T3 and T4 are connected to a common drain voltage VDD. The sources of T1 and T2 are connected to a common source voltage VSS. A current source 28 is connected between VDD and VSS. The input VIN is connected to the gates of T3 and T4. The output VOUT is connected to the drains of T3 and T4. The circuit is labeled with various components: 25, 33, S3, S1, 26, 38, 37, 36, 35, S2, S4, 34, 22, 23, 28, and 21.

212. Therefore, Itoh teaches that “the number of said second p-channel

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MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other,” as recited in the claim.

4. Claim 3

[3.1] The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are different from each other.

213. Itoh teaches this element.

214. Specifically, as shown in the Example Combination 2.1

(Embodiments 2 and 4 Combined) below, second drive circuit 42 includes 3 sub-drive circuits 42a, 42b, and 42c, and as such, the number of said second p-channel MOS transistors (T3a, T3b, and T3c, annotated as P2) and said second n-channel MOS transistors (T4a, T4b, and T4c, annotated as N2) is six (3+3). On the other hand, the number of said fifth n-channel MOS transistors (T21, annotated as N5) and the said fifth p-channel MOS transistors (T13, annotated as P5) is two (1+1). As such, these numbers are different from each other.

5. Claim 4

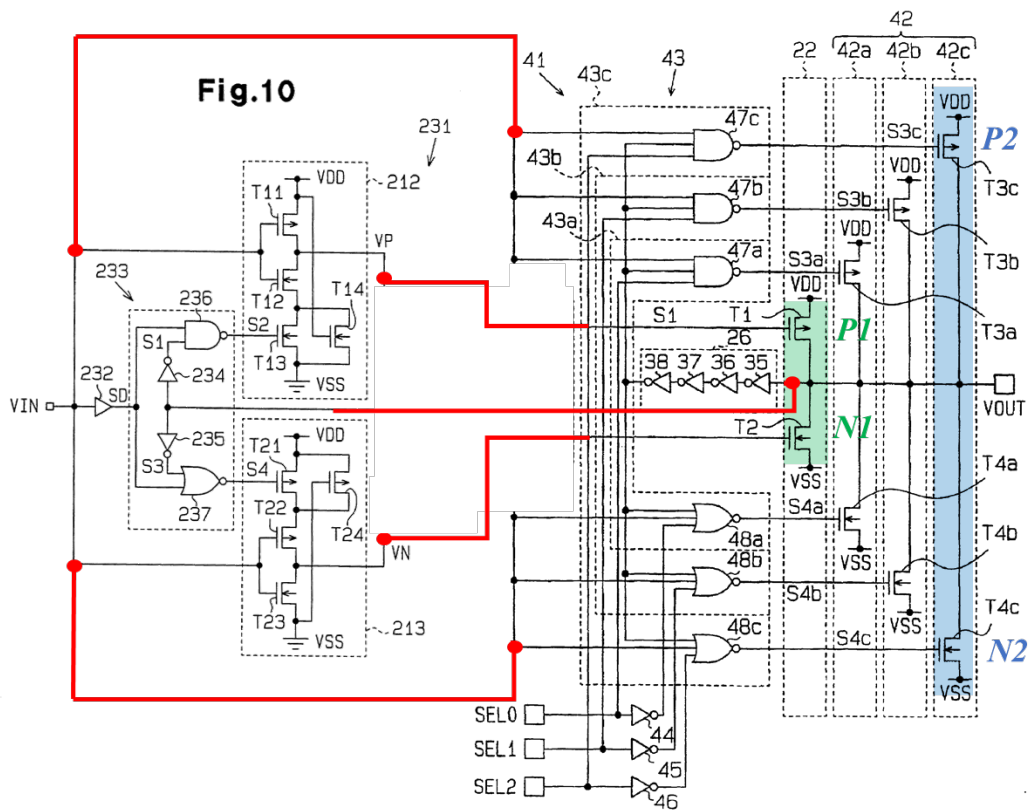
[4.1] The output buffer circuit according to claim 1, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.

216. Itoh teaches this element.

217. Continuing with Example Combination 2.1 as illustrated below, Itoh teaches that the second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a small effect on rise and fall times of pulses output from said main driver.

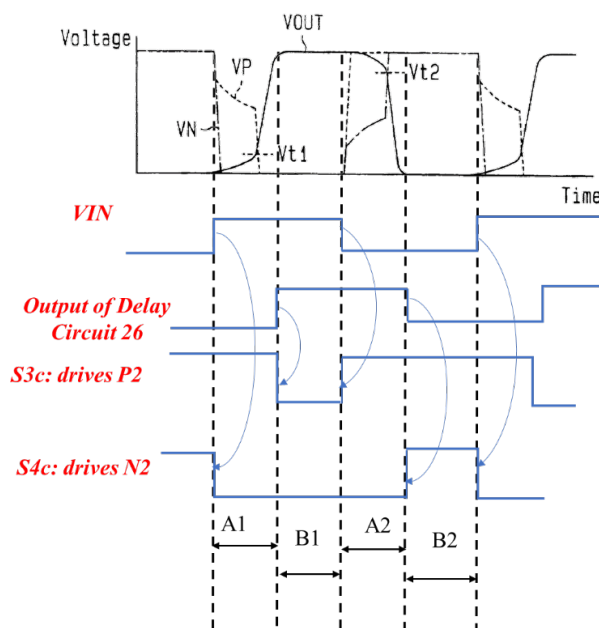
218. Specifically, in Example Combination 2.1, the first pair of first p-channel MOS transistor and first n-channel MOS transistor (T1 and T2, annotated as P1 and N1) of first-drive circuit 22 are used for controlling the slew rate (rising and falling times) of pulses output VOUT.

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

219. As shown in the waveforms of Example Combination 2.1 below, during A1 and A2, the slew rate of VOUT is primarily controlled by VP and VN controlling P1 and N1. During A1 and A2, P2 and N2 are turned off, as shown by control signals S3c and S4c, and as such, have small effect on rise and fall times of pulses output from said main driver VOUT.



**Waveforms of Example Combination 2.1
(Annotated using EX1006, Itoh, FIG. 11)**

220. Further, Example Combination 2.1 teaches that second p-channel MOS transistor (P2) and said second n-channel MOS transistor (N2) have a smaller device size with a smaller gate width than said first p-channel MOS transistor (P1) and said first n-channel MOS transistor (N1). As shown in the Example Combination 2.1, FIG. 8 provides that the second-drive circuit 42 include a plurality of pairs of P2 and N2 each having different impedances and are selectable to for controlling the output impedance. For each pair of P2 and N2 of the second-drive circuit 42, selecting a smaller device size with a smaller gate width than P1 and N1 is one of the two well-known design choices (the other is having a greater size), and a POSITA would have used this design option based on

corresponding design needs (e.g., specific contribution by this particular pair of P2 and N2 to the overall output impedance). *See, e.g.*, EX1008, Borkar, 5:8-9 (“[The transistors’] relative contribution depends on their sizes.”).

221. It is noted that the requirement of Embodiment 1 (FIG. 5) of Itoh that T1 and T2 have a higher impedance characteristic than T3 and T4 does not apply to Example Combination 2.1. First, Example Combination 2.1’s circuit 42 of FIG. 8 uses a plurality of pairs of P2 and N2, and as such, the size requirement of Embodiment 1 (applying to a single pair of P2 and N2) does not apply to the individual P2 and N2 of circuit 42 of FIG. 8. Second, in the combination, T1 (annotated as P1) and T2 (annotated as N1) are controlled using a different method for slew rate control by the slew rate control circuit of FIG. 10, and as such, the size requirement of Embodiment 1 (which is needed for slow rate control in Embodiment 1) no longer applies.

222. Therefore, Itoh teaches that “said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver,” as recited in the claim.

6. Claim 5

223. The analysis for claim 5 relies on the same analysis and evidence as

provided for claim 1, except for the differences provided below. For example, in the analysis for claim 5 below, the predriver includes circuits 212, 213, 236, and 237 (while in Ground 2: Claim 1, the predriver includes circuits 212 and 213 but does not include circuits 236 and 237). For further example, in the analysis for claim 5 below, the controller includes circuits 234, 235, 43, and 26 (while in Ground 2: Claim 1, controller includes circuits 233, 43, and 26). The analysis below explains in detail how Example Combination 2.1 with those mappings teach the elements of claim 5.

[5.0] 5. An output buffer circuit for outputting data in the form of an input pulse train at a predetermined output impedance and slew rate, comprising:

224. Itoh teaches this element for the reasons discussed at Ground 2:[1.0].

[5.1] a main driver having at least a pair of a first p-channel MOS transistor [P1] and a first n-channel MOS transistor [P2] for driving a load according to said data, and at least a pair of a second p-channel MOS transistor [P2] and a second n-channel MOS transistor [N2] for driving said load in coaction with said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1];

225. Itoh teaches this element for the reasons discussed at Ground 2:[1.1].

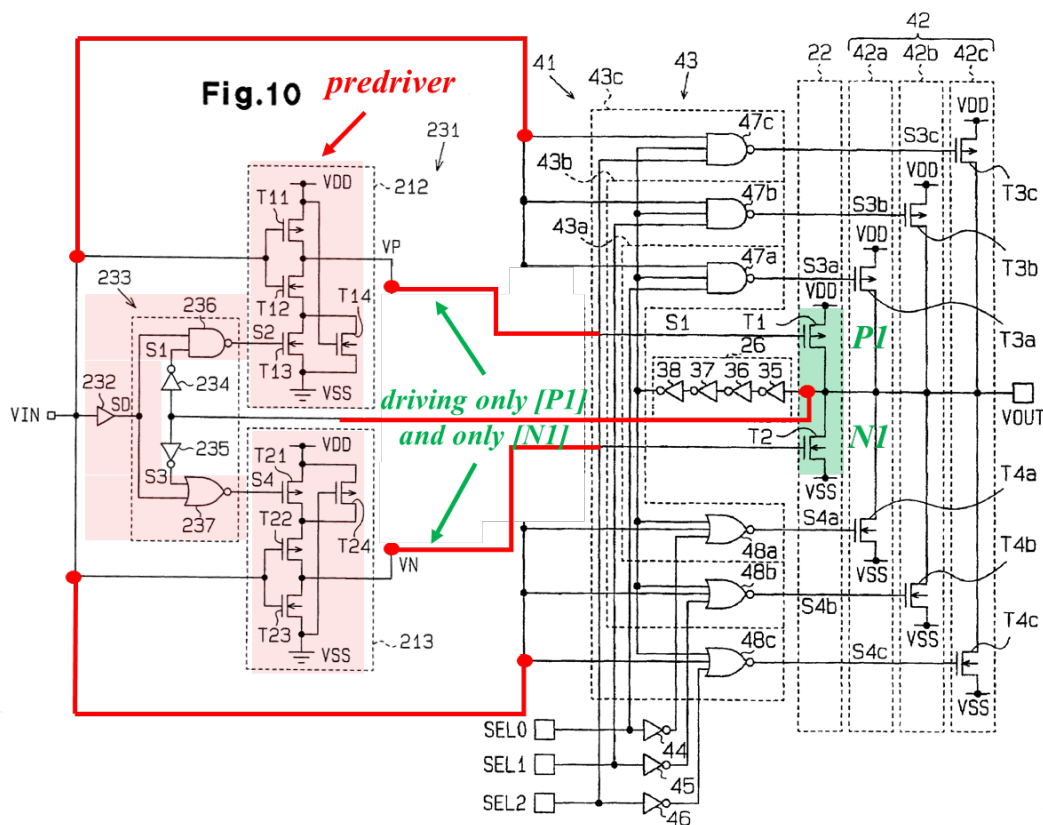
[5.2.1] a predriver with outputs for driving only said first n-channel MOS transistor [P1] and only said first p-channel MOS transistor [N1]

226. Itoh teaches this element for the reasons discussed at Ground 2:[1.2.2].

227. Continuing with Example Combination 2.1 as illustrated below,

Example Combination 2.1 discloses a predriver (pink area including circuits 212, 213, 236, and 237) positioned before the main driver (circuits 22 and 42), and provides signals VP and VN for driving only P1 and only N1 in the main driver. See also Ground 2:[1.2.1] (explaining outputs VP and VN for driving only P1 and N1).

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

228. Accordingly, Itoh teaches this element.

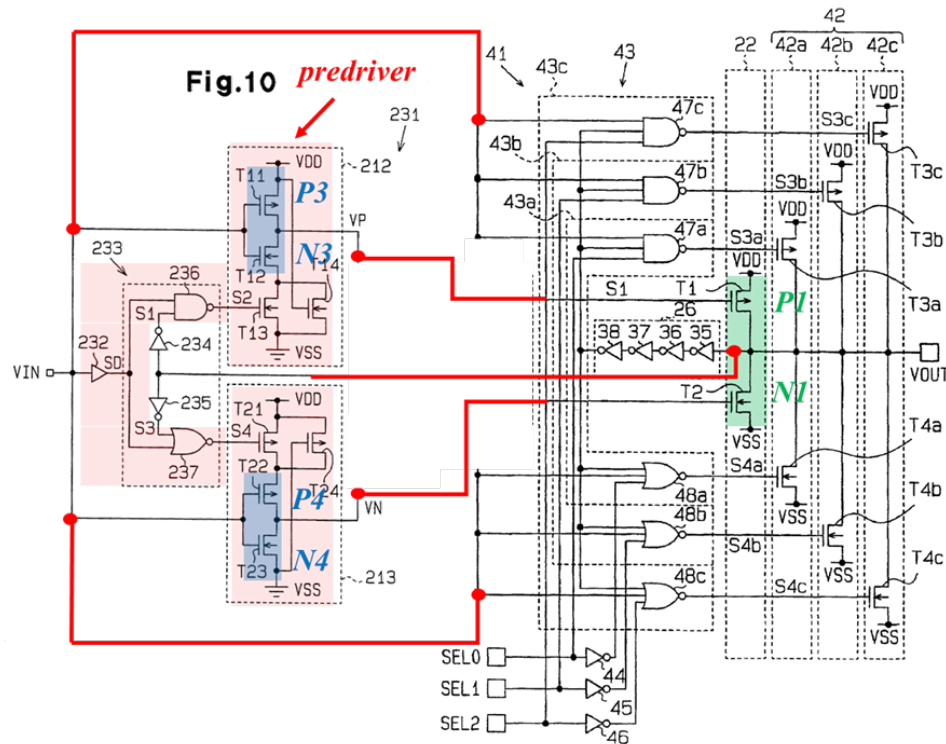
[5.2.2] [the predriver] having at least a pair of a third p-channel MOS transistor [P3] and a third n-channel MOS transistor [N3] for driving said first p-channel MOS transistor [P1] according to said data, at least a pair of a fourth p-channel MOS transistor [P4] and a fourth n-channel MOS transistor [N4] for driving said first n-channel MOS transistor [N1] according to said data,

229. Itoh teaches this element for the reasons discussed at Ground

2:[1.2.2].

230. Specifically, continuing with Example Combination 2.1 as illustrated below, Example Combination 2.1 discloses a predriver (circuits 212 and 213), where its circuit 212 includes at least a pair of a third p-channel MOS transistor (T11 annotated as P3) and a third n-channel MOS transistor (T12 annotated as N3) for driving P1 according to said data (VIN). EX1006, Itoh, 13:24-30.

Fig.8



231. Further, as shown in Example Combination 2.1 illustrated above, the predriver includes circuit 212, which includes has at least a pair of a fourth p-channel MOS transistor (T22 annotated as P4) and a fourth n-channel MOS transistor (T23 annotated as N4) for generating VN, which drives N1 according to said data (VIN). EX1006, Itoh, 12:50-56.

232. Accordingly, Itoh teaches this element.

[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

233. Itoh in view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element.

234. Continuing with Example Combination 2.1, the combination of Embodiments 2 and 4 in view of a POSITA's general knowledge teaches this element. For simplicity and clarity, only FIG. 10 as implemented in Example Combination 2.1 is illustrated below, and the analysis applies to Example Combination 2.1.

235. First, as discussed above at Ground 2:[1.2.3] and as shown in annotated FIG. 10 of Itoh below, Example Combination 2.1 includes a predriver (pink area including circuits 212, 213, 236, and 237), which includes N5 for driving for driving T1/P1 in coaction with N3, by working together to generate a signal VP for driving T1/P1.

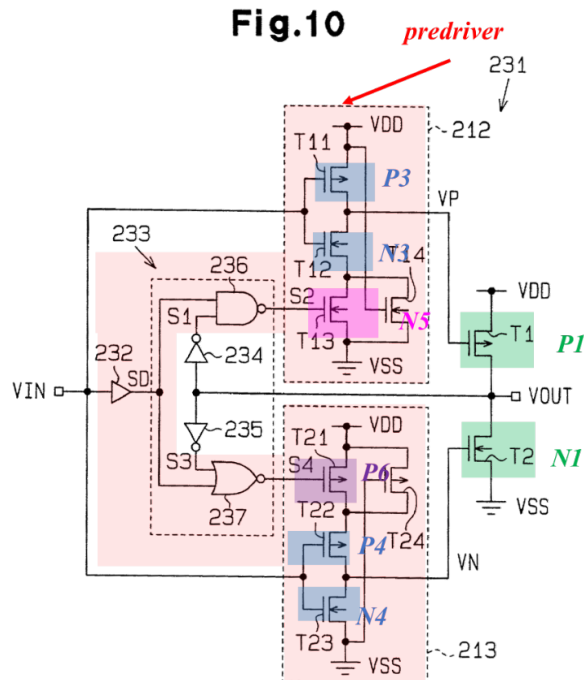
inverted VOUT), which in turn determines S2 that controls N5, where N5 connects with P3 in series and works in coaction to generate VP for controlling P1. As such, in Example Combination 2.1, P5 and P3 are working in coaction to generate the control signal for P1.

240. Therefore, Itoh teaches that “at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3]” as recited in the claim.

[5.2.4] [the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and

241. Itoh in view of a POSITA’s general knowledge of basic transistors and logic design, renders obvious this element.

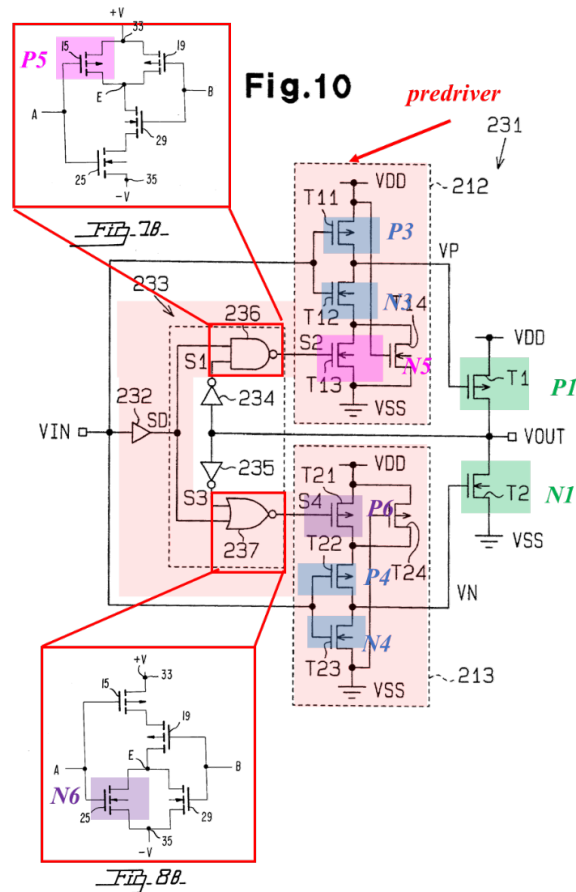
242. First, as shown in annotated FIG. 10 of Itoh below, the predriver (pink area including circuits 212, 213, 236, and 237) includes at least one sixth p-channel MOS transistor T21 (annotated as P6) for driving T2 (annotated N1) in coaction with said fourth p-channel MOS transistor T22 (annotated as P4), by working together to generate a signal VN for driving T2/N1. Specifically, P6 and P4 are connected in series and work together to generate VN (e.g., working



243. Second, it is important to understand the basic, fundamental knowledge of a POSITA. For example, it is fundamental that in CMOS process as used in Itoh, basic implementation of logic gates (e.g., NAND or NOR gates) include at least a pair of PMOS transistor and NMOS transistor.

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245. The figure below illustrates the CMOS implementation of NAND gate 236, where FIG. 8B of Skorup is used as an example to illustrate the fundamental knowledge that the basic CMOS implementation of NOR gate includes at least a NMOS transistor.



EX1006, Itoh, FIG. 10, annotated

246. With such implementation, Example Combination 2.1 teaches that the predriver includes one sixth p-channel MOS transistor (e.g., EX1007, Skorup, FIG. 8B, 25, annotated as P6) for driving said second p-channel MOS transistor (T2/P2)

in coaction with the fourth n-channel MOS transistor (T23, annotated as N4).

Specifically, N6 is turned on and off by control signal S3 (which is a delayed inverted VOUT), which in turn determines S4 that controls P6. P6 connects in series with N4 and works in coaction to generate VP for controlling N1. As such, in Example Combination 2.1, N6 and N4 work in coaction to generate the control signal for N1.

247. Accordingly, Itoh in view of a POSITA's general knowledge of basic transistors and logic design renders obvious "[a predriver ...having...] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]" as recited.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

248. Itoh in view of a POSITA's general knowledge of basic transistors and logic design, renders obvious this element.

249. Continuing with Example Combination 2.1, the combination of

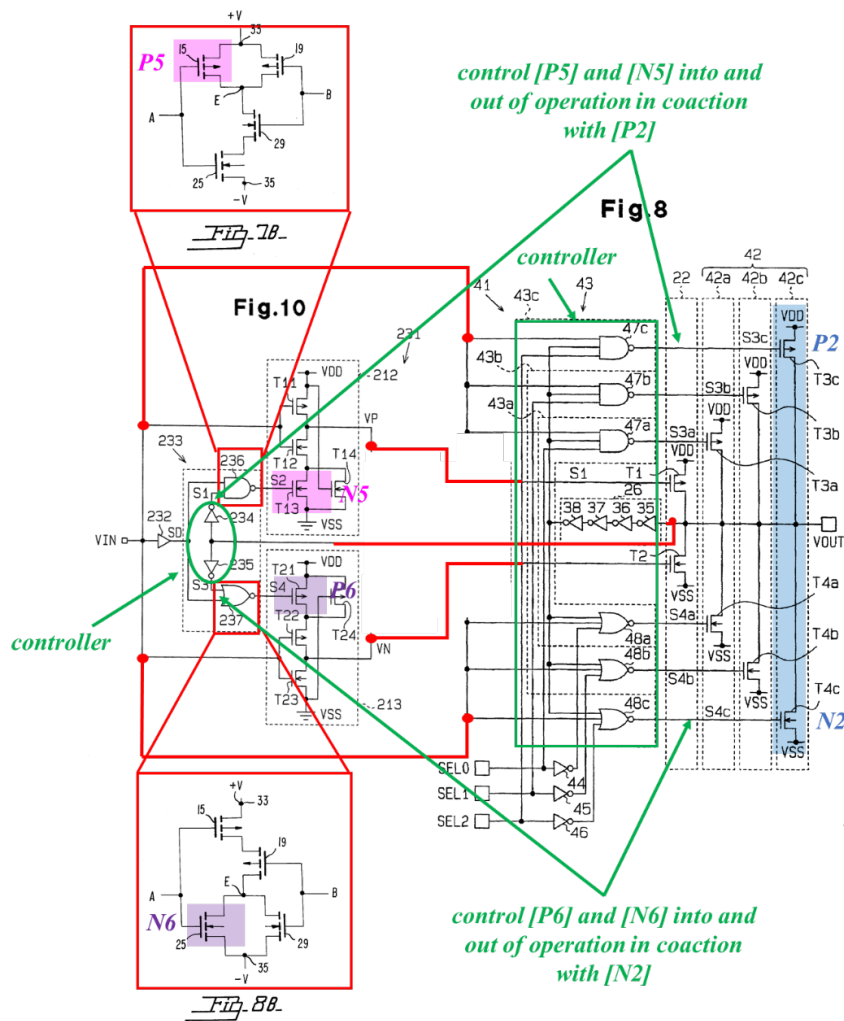
Embodiments 2 and 4 teaches this element. As shown in Example Combination

2.1 as illustrated below, the combination teaches a controller (including circuits

234, 235, 43, and 26) for generating control signals (including S1, S3, S3c, and

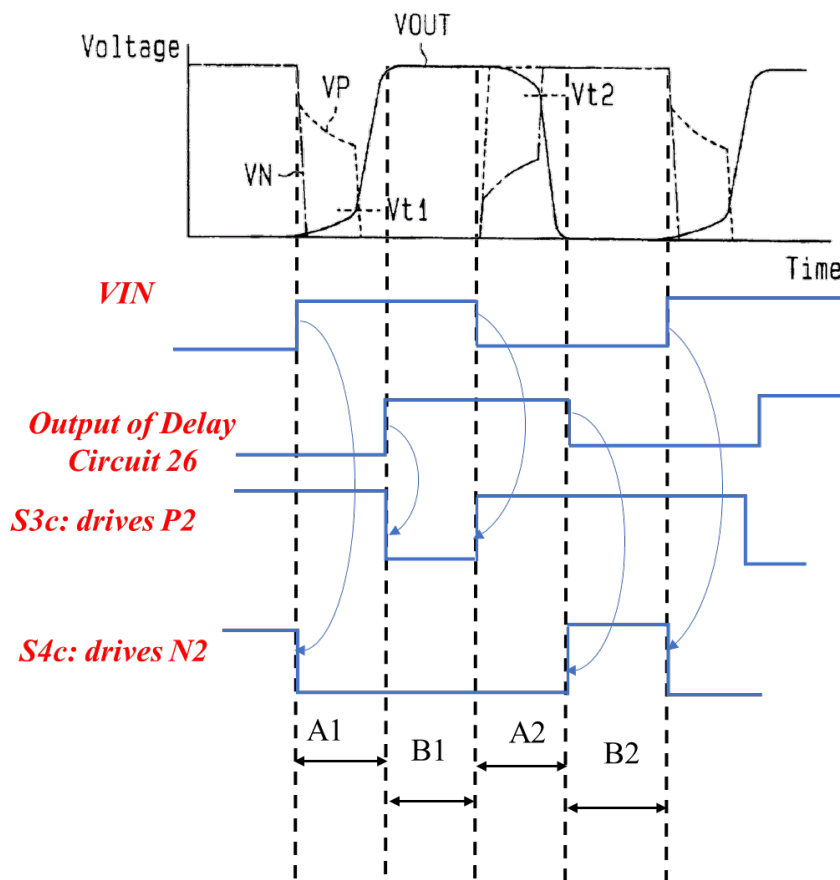
S4c). S1 is used to drive P5, S3 is used to drive N6, S3c is used to drive P2, and

S4c is used to drive N2.



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

250. In Example Combination 2.1 with the CMOS implementation of NAND and NOR gates, a POSITA would have been motivated to supply S1 (the output of controller 234) to the gate of P5 (e.g., through terminal A of FIG. 7B of Skorup), which controls said fifth p-channel MOS transistor (PMOS transistor 15 annotated as P5) into and out of operation in coaction with said second p-channel MOS transistor P2, because S1 (controlled by VOUT and is used to generate VP) and S3c (also controlled by VOUT and is used to control P2) work in coaction, as shown in the waveforms of Example Combination 2.1 below.



**Waveforms of Example Combination 2.1
(Annotated using EX1006, Itoh, FIG. 11)**

251. Referring to FIG. 10, Itoh explains that the inverter circuit 234 is used to generate the switching control signal S2 (by turning P5 in and out of operation), which determines VP, and sequentially controlling VOUT. S1 with P5 is used to control the slew rate during A1, while P1 works in coaction and is only turned on during B1 for output impedance control. EX1006, Itoh, 13:15-23 (“When the external output signal VOUT rises to the threshold voltage Vt1 of the first inverter circuit 234 thereafter, the inverted signal from **the inverter circuit 234** changes to the L level from the H level and the switching control signal S2 changes to the H level from the L level. As a result, the NMOS transistor T13 is turned on. The turned on NMOS transistor T13 causes the control signal VP to sharply fall to the L level. Accordingly, the external output signal VOUT sharply rises to the H level.”). As shown in the waveforms illustrated above, P2 is also controlled by S3c that determined by VOUT (through delay circuit 26).

252. As such, in the combination, P5 and N5 are controlled into and out of operation in coaction with P2, because P5, N5, and P2 are controlled using signals both generated based on the same VIN and feedback input VOUT signal. This configuration is similar to the configurations in the ’539 patent. *See, e.g.*, EX1001, ’539 patent, FIG. 7 (illustrating controlling P5 (e.g., QP36) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for P5 and P2

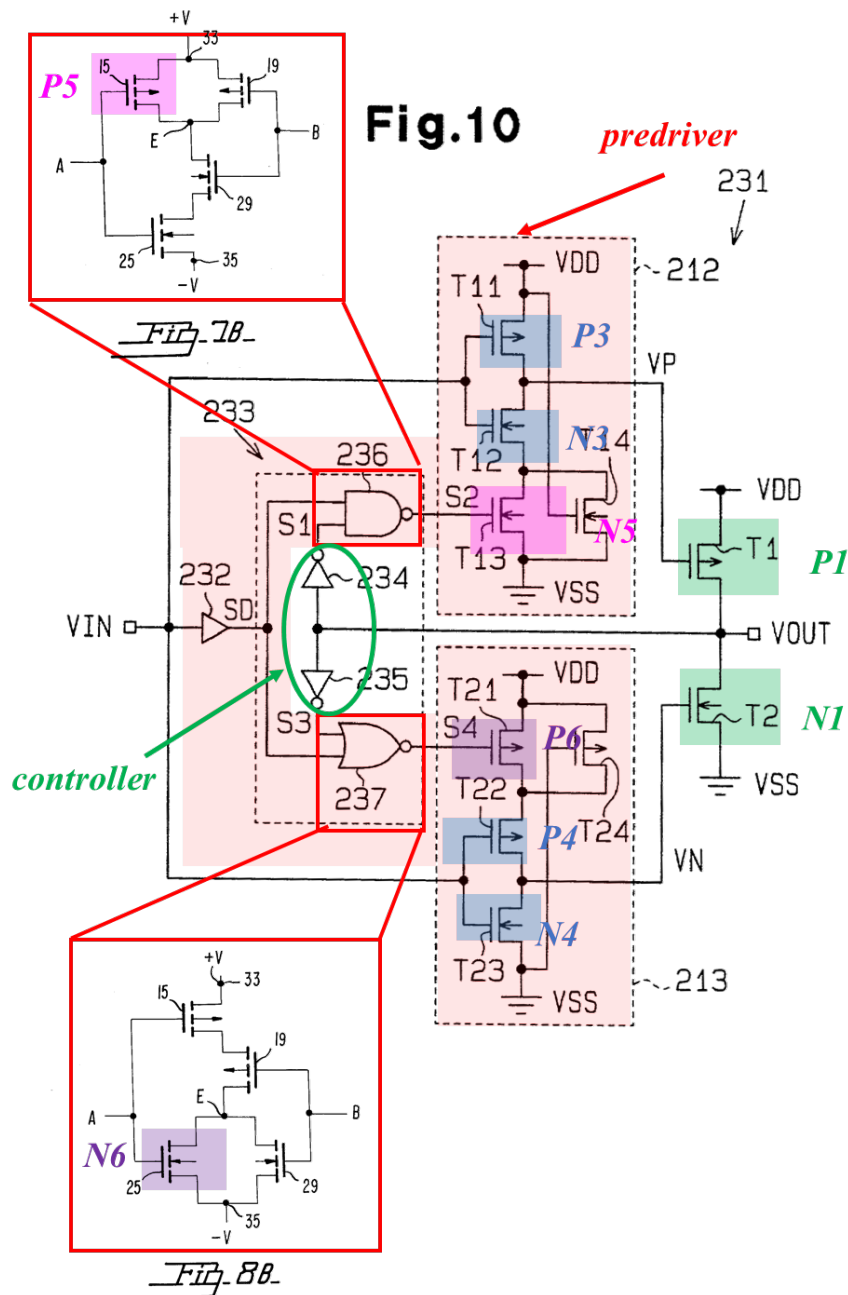
are each generated using the same signals ϕ_3 and VIN.

253. Further, in the combination, a POSITA would have been motivated to supply S3 (the output of controller 235) to terminal A of FIG. 8B of Skorup, which controls said sixth n-channel MOS transistor (NMOS transistor 25 annotated as N6) into and out of operation in coaction with said second n-channel MOS transistor N2, because S2 (controlled by VOUT and is used to generate VN) and S4c (also controlled by VOUT and is used to control N2) work in coaction, as shown in the waveforms of Example Combination 2.1 above. S3 with N6 is used to control the slew rate during A2, while N2 works in coaction and is only turned on during B2 for output impedance control. EX1006, Itoh, 13:56-64 (“When the external output signal VOUT falls to the threshold voltage V_{t2} of the inverter circuit 235 thereafter, the inverted signal from the inverter circuit 235 changes to the H level from the L level and the Switching control signal S4 changes to the L level from the H level. This turns on the PMOS transistor T21. The turned-on PMOS transistor T21 causes the control signal VN to sharply rise to the H level. Accordingly, the external output signal VOUT sharply falls to the L level.”).

254. As such, in the combination, N6 and P6 are controlled into and out of operation in coaction with N2, because N6, P6, and N2 are controlled using signals both generated based on the same VIN and feedback input VOUT signal. This configuration is similar to the configurations in the '539 patent. *See, e.g.*, EX1001,

'539 patent, FIG. 7 (illustrating controlling N6 (e.g., QN36) into and out of

operation in coaction with N2 (e.g., QN2) where the control signals for N6 and P2 are each generated using the same signals ϕ_6 and VIN.



EX1006, Itoh, FIG. 10, annotated

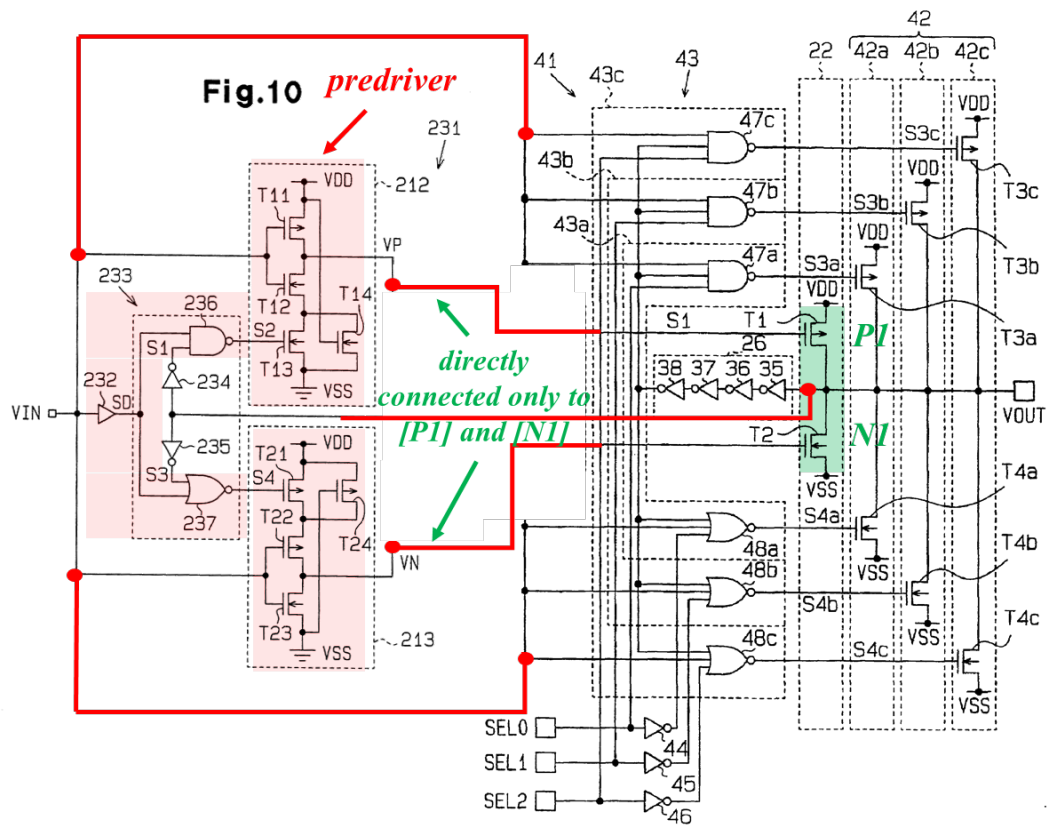
255. Accordingly, Itoh teaches “a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2]” as recited.

[5.4] *wherein the output of the predriver is directly connected only to said first p-channel MOS transistor and said first n-channel MOS transistor of said main driver.*

256. Itoh teaches this element for the reasons discussed at Ground 2:[1.4].

257. Specifically, continuing with Example Combination 2.1 as illustrated below, Itoh teaches the output (control signals VP and VN) of the predriver (circuits 212 and 213) is directly connected only to said first p-channel MOS transistor (T1 annotated as P1) and said first n-channel MOS transistor (T2 annotated as N1) of said main driver.

Fig.8



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

258. Accordingly, Itoh teaches this limitation.

7. Claim 6

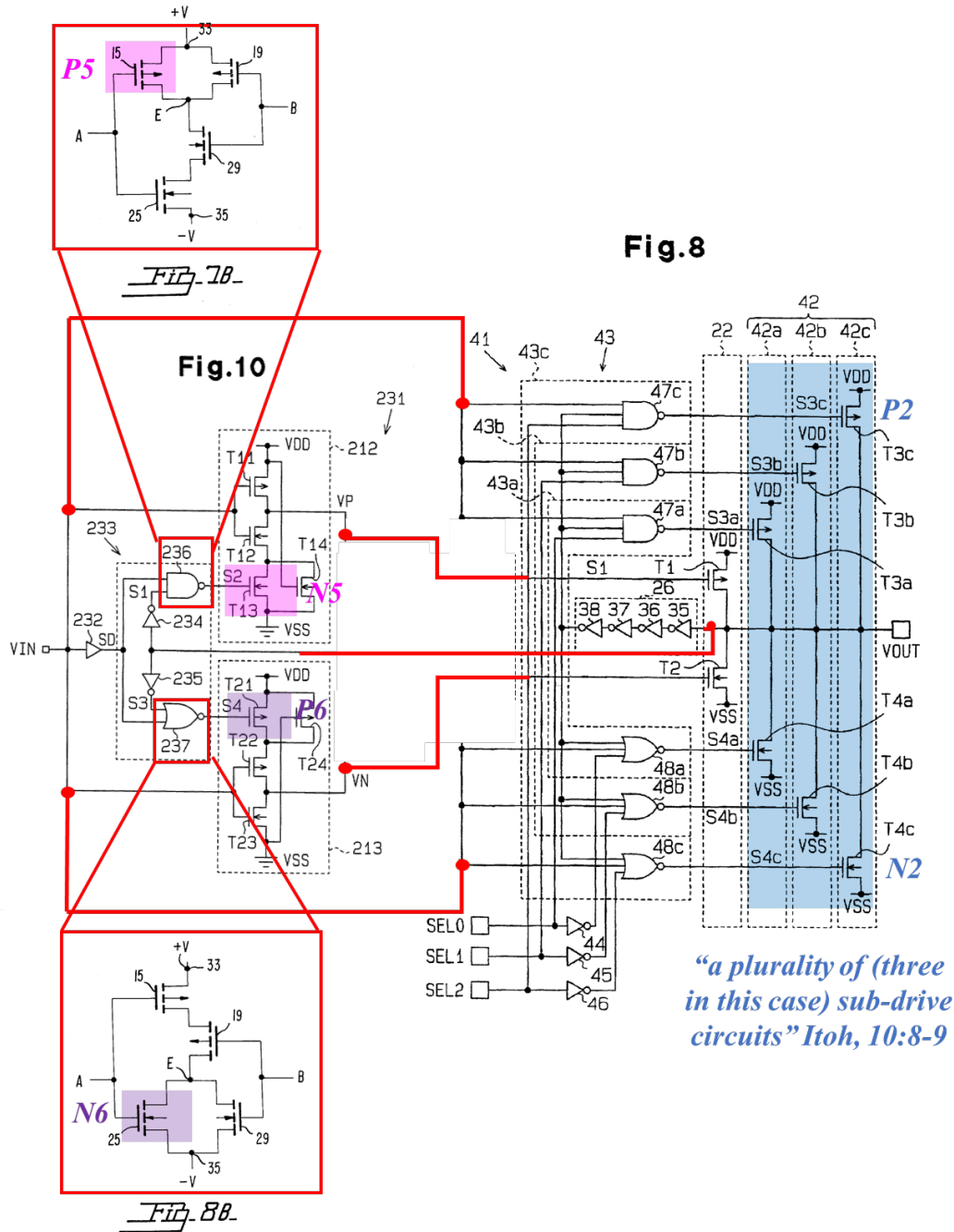
[6.0] 6. *The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistor [P5], said sixth n-channel MOS transistor [N6], and said sixth p-channel MOS transistor [P6] are equal to each other.*¹²

259. Itoh teaches this element.

260. Continuing with Example Combination 2.1 as illustrated below, the combination of Embodiments 2 and 4 teaches this element.

261. **First**, in Example Combination 2.1, the number of said fifth n-channel MOS transistors (N5), said fifth p-channel MOS transistor (P5), said sixth n-channel MOS transistor (N6), and said sixth p-channel MOS transistor (P6) is four.

¹² There is no antecedent basis for the plural “*transistors*” as recited in “*second p-channel MOS **transistors** and said second n-channel MOS **transistors**,*” “*said fifth n-channel MOS **transistors**,*” “*said fifth p-channel MOS **transistors**,*” “*said sixth n-channel MOS **transistors**,*” and “*said sixth p-channel MOS **transistors***” of claims 6 and 7. Instead, claim 5 recites “*at least a pair of a first p-channel MOS **transistor** and a first n-channel MOS **transistor**,*” “*at least a pair of a second p-channel MOS **transistor** and a second n-channel MOS **transistor**,*” etc. As such, a POSITA would have understood that “*transistors*” as recited in claims 6 and 7 includes “at least a transistor.”



Example Combination 2.1
(Combination of Embodiments 2 and 4 of Itoh)

262. Second, Itoh describes that "[t]he second drive circuit 42 [of FIG. 8]

includes **a plurality of (three in this case)** sub-drive circuits 42a, 42b and 42c.”

EX1006, Itoh, 10:8-9. As such, in Example Combination 2.1, a POSITA would have been motivated to implement any suitable plurality (e.g., 2, 3, 4, etc.) of pairs of P2 and N2 in the second drive circuit 42 based on design needs (e.g., number of selection signals, output impedance configuration requirements, etc.). *See also*, EX1006, Itoh, 18:3-5 (“the second drive circuit includes **a plurality of sub-drive circuits** having different impedances”).

263. In a case where the design requires two selection signals, a POSITA would have implemented second-drive circuit 42 with two pairs of P2 and N2, each controlled by the corresponding selection signal. In this case, the number of P2 and N2 is four, which is equal to the number (4) of N5, N6, P5, and P6.

264. Therefore, Itoh teaches this element.

8. Claim 7

[7.0] *7. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistors [P5], said sixth n-channel MOS transistors [N6], and said sixth p-channel MOS transistors [P6] are different from each other.*

265. Itoh teaches this element.

266. Specifically, as discussed above at Ground 2:[6.0] and as shown in the Example Combination 2.1 (Embodiments 2 and 4 Combined), second drive circuit

42 of the main driver includes 3 sub-drive circuits 42a, 42b, and 42c, and as such, the number of said second p-channel MOS transistors (T3a, T3b, and T3c annotated as P2) and said second n-channel MOS transistors (T4a, T4b, and T4c, annotated as N2) is six (3+3).

267. On the other hand, the number of said the number of said fifth n-channel MOS transistors, said fifth p-channel MOS transistors, said sixth n-channel MOS transistors, and said sixth p-channel MOS transistors is four (1+1+1+1). As such, these numbers are different from each other.

268. Therefore, Itoh discloses or renders obvious that “the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistors [P5], said sixth n-channel MOS transistors [N6], and said sixth p-channel MOS transistors [P6] are different from each other,” as recited in the claim.

9. Claim 8

[8.0] 8. The output buffer circuit according to claim 5, wherein said second p-channel MOS transistor [P2] and said second n-channel MOS transistor [N2] have a smaller device size with a smaller gate width than said first p-channel MOS transistor [P1] and said first n-channel MOS transistor [N1], and have a small effect on rise and fall times of pulses output from said main driver.

269. Itoh teaches this element for the reasons discussed at [4.0].

D. Ground 3: Claims 1-8 are Rendered Obvious under §103(a) over Itoh in view of Muljono.

270. The analysis for Ground 3 relies on the analysis and evidence as provided for Ground 2, except for where additional analysis is provided below.

1. Reasons to Combine Itoh and Muljono

271. A POSITA would have been motivated to combine Muljono's teaching of a compensation circuit in Itoh to achieve the obvious, beneficial, and predictable results of an output buffer circuit having "an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage and temperature" as taught by Muljono. EX1010, Muljono, 2:23-27.

272. First, Itoh and Muljono are analogous prior art to the '539 patent, and like the '539 patent, are in the same field of endeavor pertaining to output buffer circuits. *See, e.g.*, EX1001, 1:15-19; EX1006, Title, 1:6-7 ("The present invention relates to an output buffer circuit."); EX1010, Muljono, Abstract.

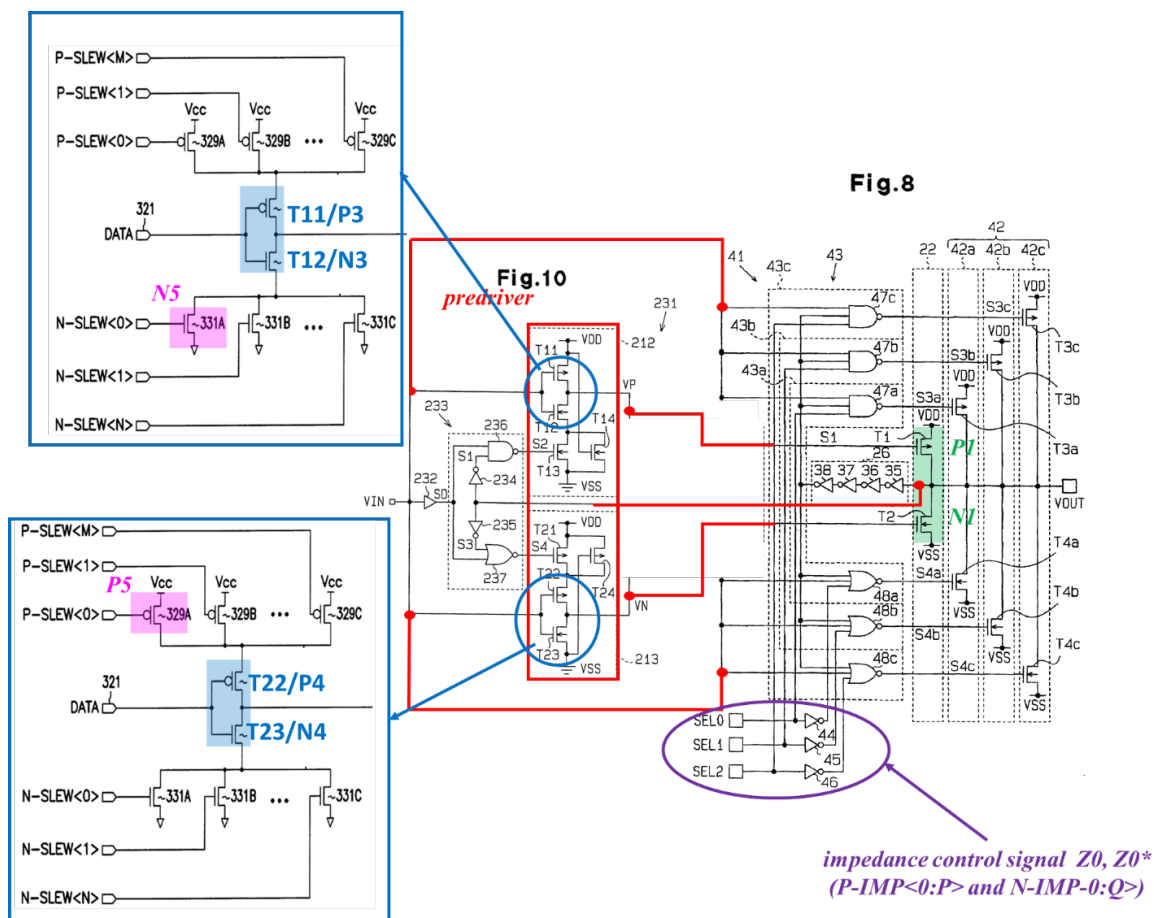
273. Second, Itoh and Muljono share the same goal of providing an output buffer circuit that generates an output signal with less variation. EX1006, Itoh, 14:38-53; EX1010, Muljono, 2:23-28.

274. Accordingly, a POSITA would have been motivated to apply the compensation circuit with output impedance and slew rate control signals as taught by Muljono in embodiments of Itoh, to produce the obvious, beneficial, and

predictable results of an improved output buffer circuit having “an approximately uniform output impedance and slew rate independent of variations in process skew, supply voltage, and temperature” as taught by Moljono. EX1010, 2:23-26.

275. Finally, applying Muljono’s teachings in embodiments of Itoh would have been no more than the combination of known elements according to known methods (e.g., incorporating compensations circuits to the predriver circuit and main driver circuit in an output buffer circuit according to the known IC design steps) obvious to a POSITA.

276. An example implementation of Example Combination 3.1 (Muljono combined with Example Combination 2.1 (Embodiments 2 and 4 of Itoh combined)) is illustrated below. While the analysis below focuses on Example 3.1, it similarly applies to combinations of Muljono with other similar Itoh embodiments.



Example 3.1
(Combination of Example 2.1 (Embodiments 2 and 4 of Itoh) and Muljono)

2. Claim 1

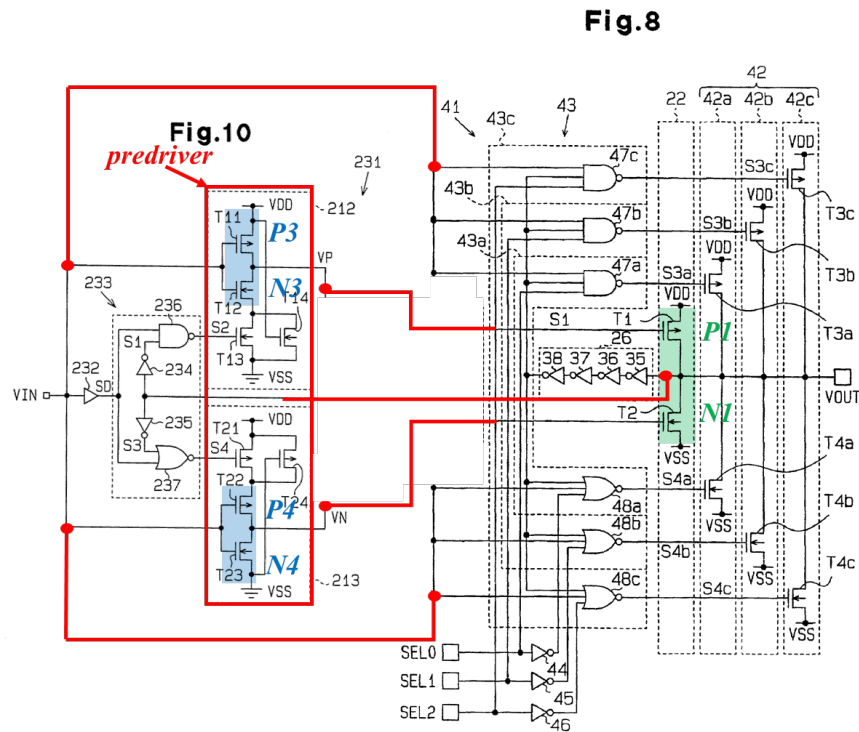
[1.0]-[1.2.2]

277. Itoh teaches this element for the reasons discussed at Ground 2:[1.0]-[1.2.2].

[1.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], and at least one fifth p-channel MOS transistor [P5] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4]; and

278. Itoh in view of Muljono renders obvious this element.

279. As shown in Example 2.1 as illustrated below, Example 2.1 teaches an output buffer circuit including a predriver circuit (e.g., circuits 212 and 213) and a main circuit (e.g., circuits 22 and 42). A POSITA would have been motivated to apply Muljono's compensation circuit teachings in Example 2.1 for PVT compensation.



Example 2.1
(Combination of Example Embodiments 2 and 4 of Itoh)

An example implementation of Example 2.1 combined with Muljono is provided below, which is referred to as Example 3.1 below. Specifically, a POSITA would have been motivated to, for slew rate control, apply Muljono's slew rate compensation circuit (e.g., as described in FIGS. 1 and 3) for the inverter pairs with the pairs T11/T12 (P3/N3) and T22/T23 (P4/N4) in FIG. 10 of Itoh. FIG. 10 of Itoh controls a slew rate of the output signal by controlling slew rates of the control signals VP and VN applied to the output transistors, and as such, a POSITA would have been motivated to apply Muljono's slew rate compensation circuit to the pairs T11/T12 (P3/N3) and T22/T23 (P4/N4) to further compensate/control the slew rates of the control signals VP and VN. Further, for output impedance control, it would have been obvious for a POSITA to apply Muljono's impedance control signals (e.g., as described in FIGS. 1 and 2) to select signals SEL0-SEL2 of FIG. 8, as they are used for selecting the sub-driver circuits for output impedance control.



(Combination of Example Embodiment 2.1 and Muljono)

As shown in Example 3.1, circuit 212 of the predriver includes at least one fifth n-channel MOS transistor (331A annotated as N5) for driving said first p-channel MOS transistor (T1 annotated as P1) in coaction with said third n-channel MOS transistor (T12 annotated as N3) for controlling the slew rate. EX1010, 5:67-6:21 (explaining a plurality of n-channel transistors 331A-C coupled in parallel for slew rate control). Specifically, N5 and N3 are connected in series and work together to generate VP, which drives P1.

Similarly, circuit 213 of the predriver includes at least one fifth p-channel MOS transistor (transistor 329A annotated as P5) for driving said first n-channel MOS transistor (T2 annotated as N1) in coaction with said fourth p-channel MOS transistor (T22 annotated as P4). Specifically, P5 and P4 are connected in series and work together to generate VN, which drives N1. EX1010, 5:67-6:21 (“The pre-driver circuit 303 includes slew rate compensation circuitry including a plurality of p-channel transistors 329A-C coupled in parallel between a supply voltage Vcc and the rail 315. A plurality of n-channel transistors 331A-C is coupled in parallel between the rail 317 and a ground. A slew rate control signal is generated by the slew rate control signal generator 127 shown in FIG. 1 as a set of digital slew rate control signals P-SLEW <0:M> and N-SLEW <0:N>. The signals P-SLEW-0:M> are coupled respectively to the gates of the p-channel transistors 329A-C, and the signals N-SLEW<0:N> are coupled respectively to the gates of the n-channel transistors 331 A-C. The p-channel transistors 329A-C provide a variable resistance between the rail 315 and the voltage Vcc in response to the signals P-SLEW<0:M>, and the n-channel transistors 331A-C provide a variable resistance between the rail 317 and ground in response to the signals N-SLEW<0:N>. The transistors 329A-C, 331A-C provide a resistance R to a charging of C_{LOAD} and a discharge of C_{LOAD} when the data signal transitions from high to low or low to high. The resistance R is determined by the signals P-

SLEW<0:M> and N-SLEW<0:N>. As discussed above, a product of R and C_{LOAD} determines the slew rate of the driver circuit 205.”).

280. Therefore, Itoh in view of Muljono renders obvious this element.

[1.3] a controller for generating control signals to control said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said fifth p-channel MOS transistor [P5] into and out of operation in coaction with said second n-channel MOS transistor [N2],

281. Itoh in view of Muljono renders obvious this element.

282. First, as discussed at Ground 2:[1.3], Example 2.1 renders this element obvious.

283. Second, additionally, continuing with Example 3.1, as shown in annotated Muljono FIG. 1 below, Example Combination 3.1 includes a controller (compensation circuit 115 as taught by Muljono) that generates control signals including slew rate control signal impedance control signal, which control the transistors in the pre-driver circuit (including N5 and P5) in coaction with the transistors in the main driver (including N2 and P2).

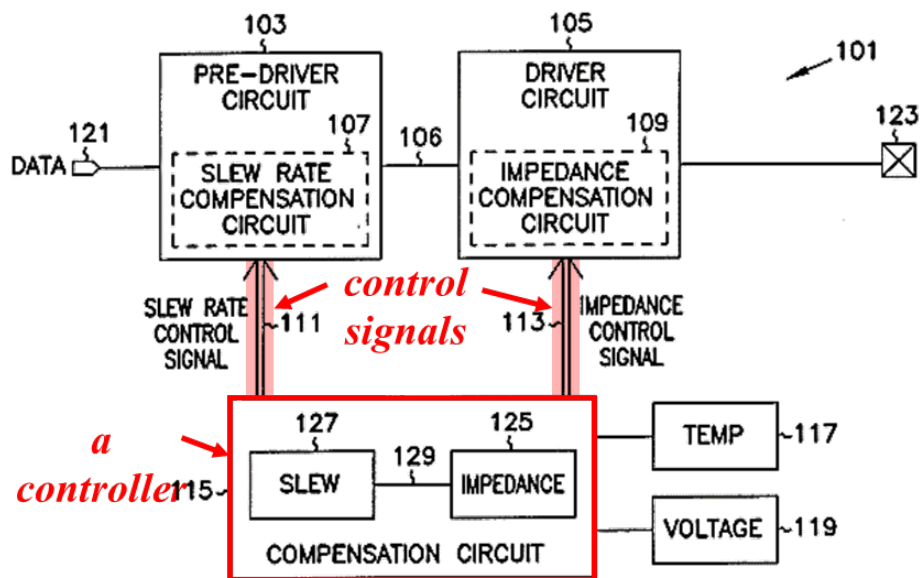
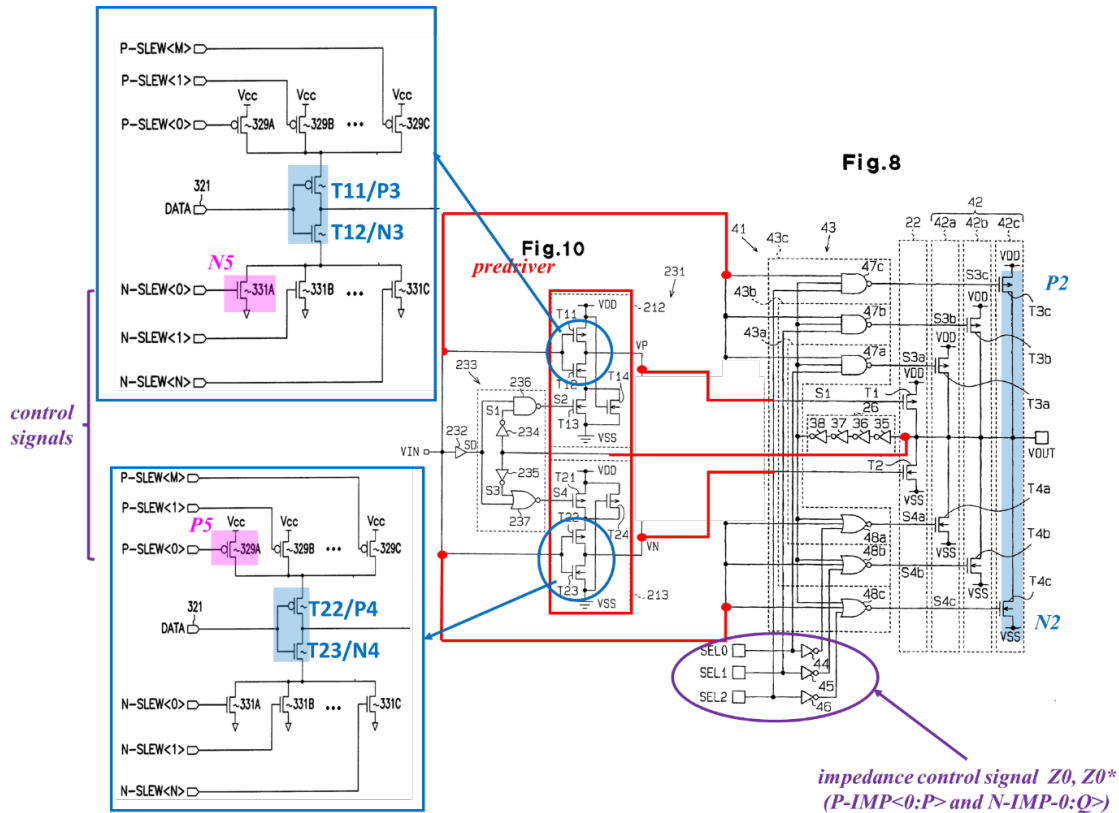


FIG. 1

EX1010, FIG. 1, annotated

As shown in Example 3.1 as illustrated below, the control signals control N5 (using control signal N-SLEW) into and out of operation in coaction with P2 (using control signal P-IMP provided to the SEL0-SEL2), and control P5 (using control signal P-SLEW) into and out of operation in coaction N2 (using control signal P-IMP provided to SEL0-SEL2 and inverter, or directly providing to SEL0-SEL2).



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

In Example 3.1, N5 is controlled into and out of operation in coaction with P2, because the slew rate control signal for controlling N5 (N-SLEW for generating VP to drive P1) is generated in response to the impedance control signal for controlling P2. EX1010, 6:36 (“The signals Z0, Z0* are generated by the impedance control signal generator 125 to control the transistors in the driver circuit 105 to maintain the output impedance of the output buffer 101 at a desired level as the temperature and Vcc change. The signals P-SLEW <0:M> and NSLEW <0:N> are generated by the slew rate control signal generator 127 in

response to the signals Z0, Z0* to compensate R and maintain the product of R and C_{LOAD} to be approximately uniform as C_{LOAD} changes.”). Similarly, P5 is controlled into and out of operation in coaction with N2, because the slew rate control signal for controlling P5 (P-SLEW for generating VN to drive N1) is generated in response to the impedance control signal for controlling N2.

This configuration of controlling N5 into and out of operation in coaction with P2 and controlling P5 in and out of operation in coaction with N2 is similar to the configuration in the '539 patent. *See, e.g.,* EX1001, FIGS. 3, 4, and 7 (illustrating controlling N5 (e.g., QN17) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for N5 and P2 are each generated using the same signals ϕ_3 and VIN).

Therefore, Itoh in view of Muljono renders obvious this this element.

[1.4]

284. Itoh teaches this element for the reasons discussed at Ground 2:[1.4].

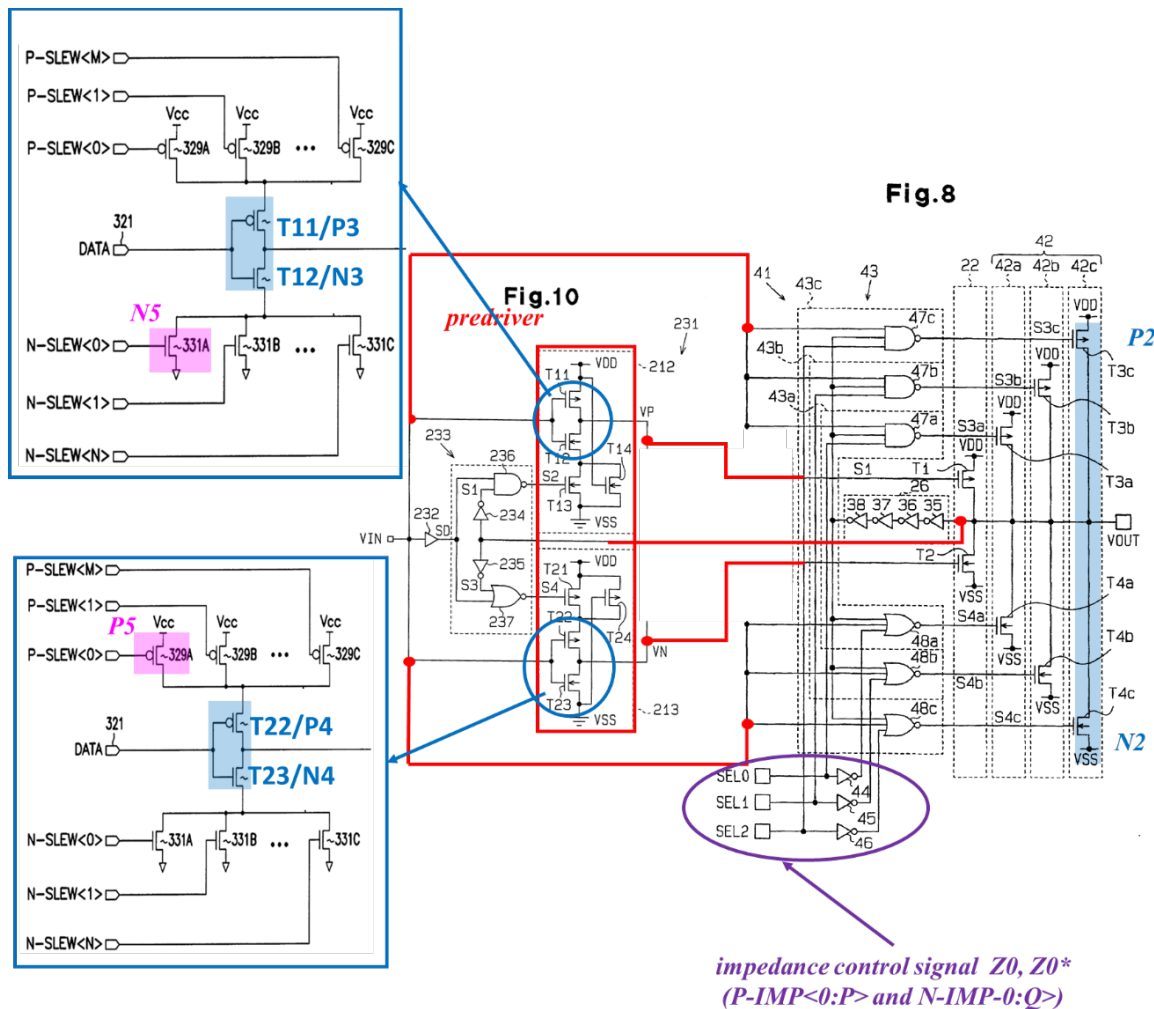
3. Claim 2

[2.0] *The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are equal to each other.*

285. Itoh in view of Muljono renders obvious this element.

286. As shown in Example 3.1 illustrated below, the number of P2 and N2

correspond to the plurality number of impedance control signals, which may be implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs. Similarly, the number of N5 and P5 correspond to the plurality of slew rate control signal numbers, which may be implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs.



Example 3.1
(Combination of Example Embodiment 2.1 and Muljono)

Accordingly, in a case where there are three N5 (NMOS transistors 331A, 331B, and 331C) and three P5 (PMOS transistor 329A, 329B, and 329C), and also three pairs of P2 and N2, then the number of N5 and P5 equal to the number of P2 and N2.

Accordingly, Itoh in view of Muljono renders obvious this element.

4. Claim 3

[3.0] The output buffer circuit according to claim 1, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2] and the number of said fifth n-channel MOS transistors [N5] and said fifth p-channel MOS transistors [P5] are different from each other.

287. Itoh in view of Muljono renders obvious this element.

288. As discussed at Ground 3:[2.0], the number of P2, N2, P5, and N5 may be implemented with any suitable numbers. Accordingly, in a case where there are four N5 and four P5, and three pairs of P2 and N2, then the number of N5 and P5 equal to eight, and the number of P2 and N2 is 6, and they are different from each other.

289. Accordingly, Itoh in view of Muljono renders obvious this element.

5. Claim 4

290. Itoh teaches this element for the reasons discussed at Ground 2:[4.0].

6. Claim 5

[5.0]-[5.2.2]

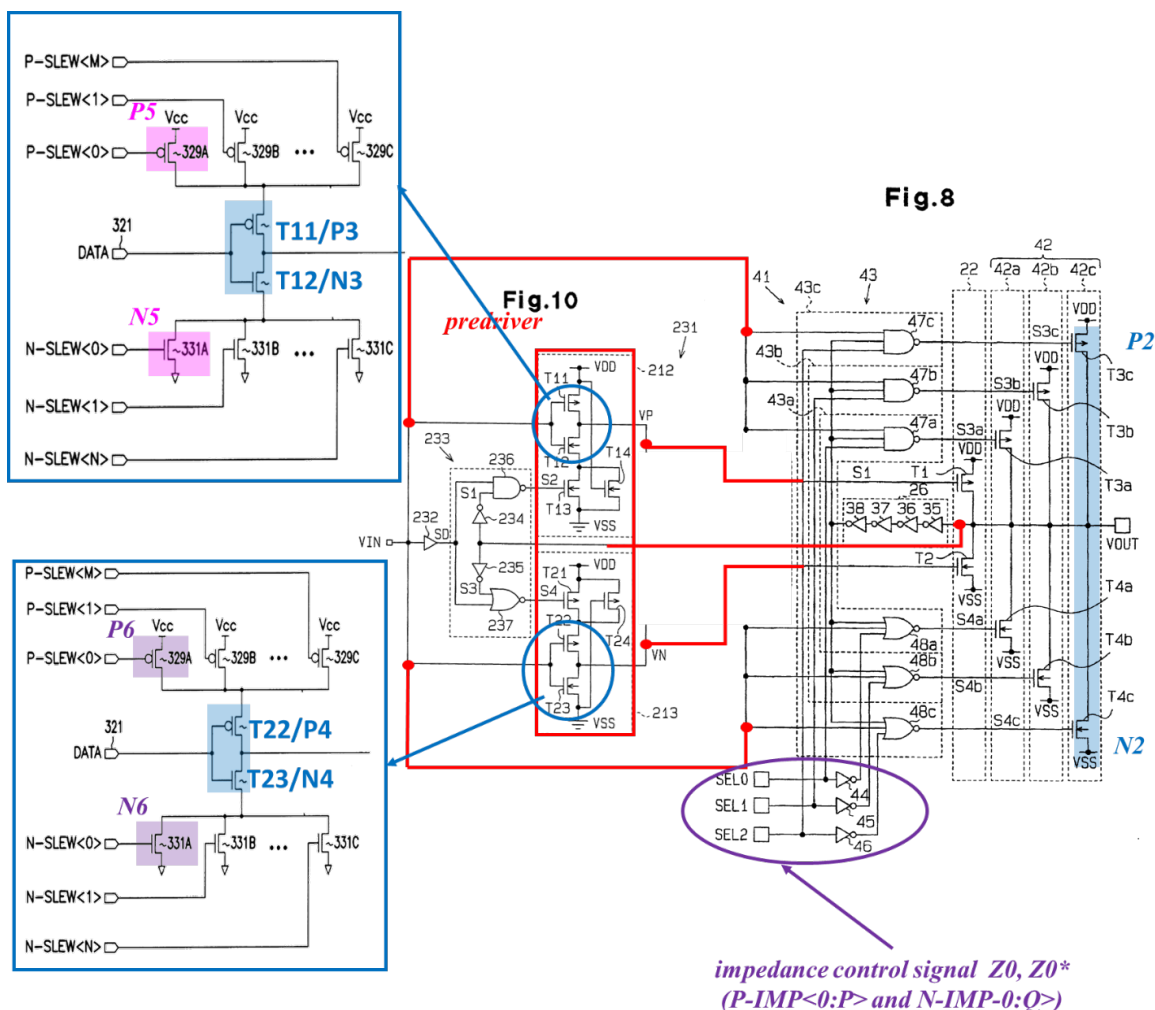
291. Itoh teaches these element for the reasons discussed at Ground

3:[1.0]-[1.2.2].

[5.2.3] [the predriver having] at least one fifth n-channel MOS transistor [N5] for driving said first p-channel MOS transistor [P1] in coaction with said third n-channel MOS transistor [N3], at least one fifth p-channel MOS transistor [P5] for driving said first p-channel MOS transistor [P1] in coaction with said third p-channel MOS transistor [P3],

292. Itoh in view of Muljono renders obvious this element.

293. Continuing with Example 3.1 as illustrated below, circuit 212 in the predriver has at least one fifth n-channel MOS transistor (transistor 331A, annotated as N5) for driving said first p-channel MOS transistor (T1, annotated as P1) using VP in coaction with said third n-channel MOS transistor (transistor T12, annotated as N3). N5 and N3 are connected in series and work in coaction to generate VP for driving P1. Further, circuit 212 in the predriver has at least one fifth p-channel MOS transistor (transistor 329A, annotated as P5) for driving said first p-channel MOS transistor (T1/P1) in coaction with said third p-channel MOS transistor (T11/P3). P5 and P3 are connected in series and work in coaction to generate VP for driving P1.



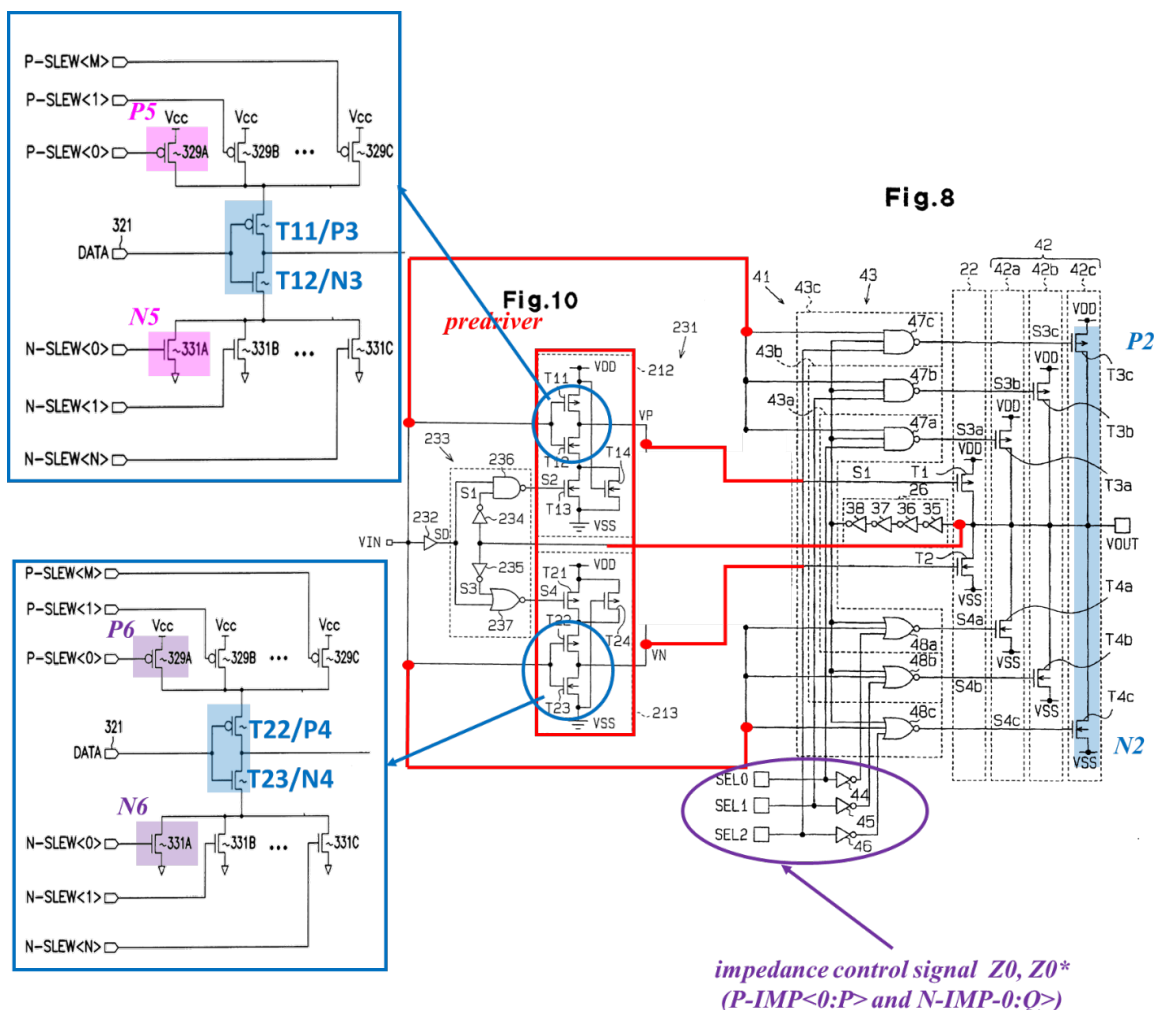
Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

Therefore, Itoh in view of Muljono renders obvious this element.

[5.2.4] [the predriver having] at least one sixth p-channel MOS transistor [P6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth p-channel MOS transistor [P4], and at least one sixth n-channel MOS transistor [N6] for driving said first n-channel MOS transistor [N1] in coaction with said fourth n-channel MOS transistor [N4]; and

294. Itoh in view of Muljono renders obvious this element.

295. Continuing with Example 3.1 as illustrated below, circuit 213 in the predriver has at least one at least one sixth p-channel MOS transistor (transistor 329A, annotated as P6) for driving said first n-channel MOS transistor (T2/N1) in coaction with said fourth p-channel MOS transistor (T22/P4). P6 and P4 are connected in series and work in coaction to generate VN for driving N1. Circuit 213 further includes at least one sixth n-channel MOS transistor (transistor 331A, annotated as N6) for driving said first n-channel MOS transistor (T2/N1) in coaction with said fourth n-channel MOS transistor (T23/N4). N6 and N4 are connected in series and work in coaction to generate VN for driving N1.



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

296. Accordingly, Itoh in view of Muljono renders obvious this element.

[5.3] a controller for generating control signals to control said fifth p-channel MOS transistor [P5] and said fifth n-channel MOS transistor [N5] into and out of operation in coaction with said second p-channel MOS transistor [P2], and control said sixth p-channel MOS transistor [P6] and said sixth n-channel MOS transistor [N6] into and out of operation in coaction with said second n-channel MOS transistor [N2],

297. Itoh in view of Muljono renders obvious this element.

298. Continuing with Example 3.1, as discussed at Ground 3:[1.3],

Example Combination 3.1 includes a controller (compensation circuit 115 as taught by Muljono) that generates control signals including slew rate control signal impedance control signal, which control the transistors in the pre-driver circuit in coaction with the transistors in the main driver.

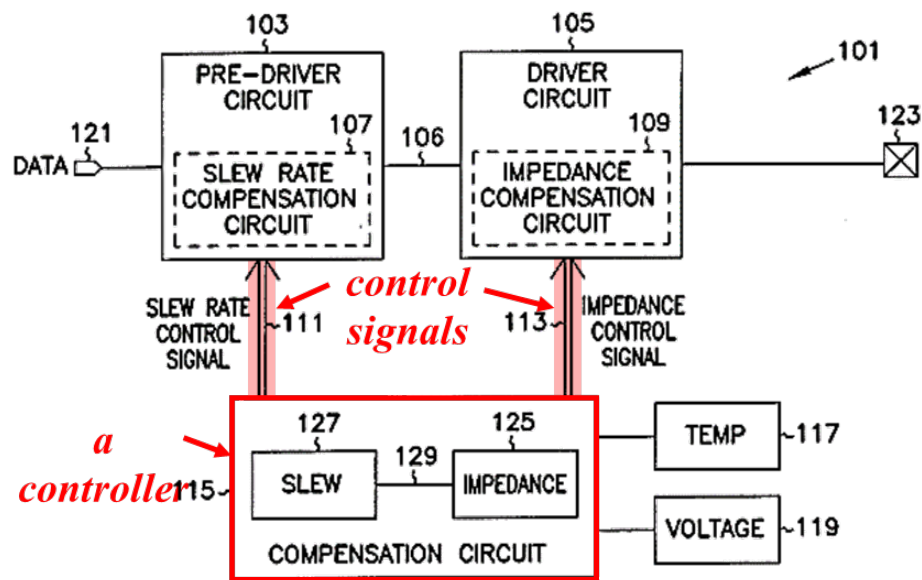
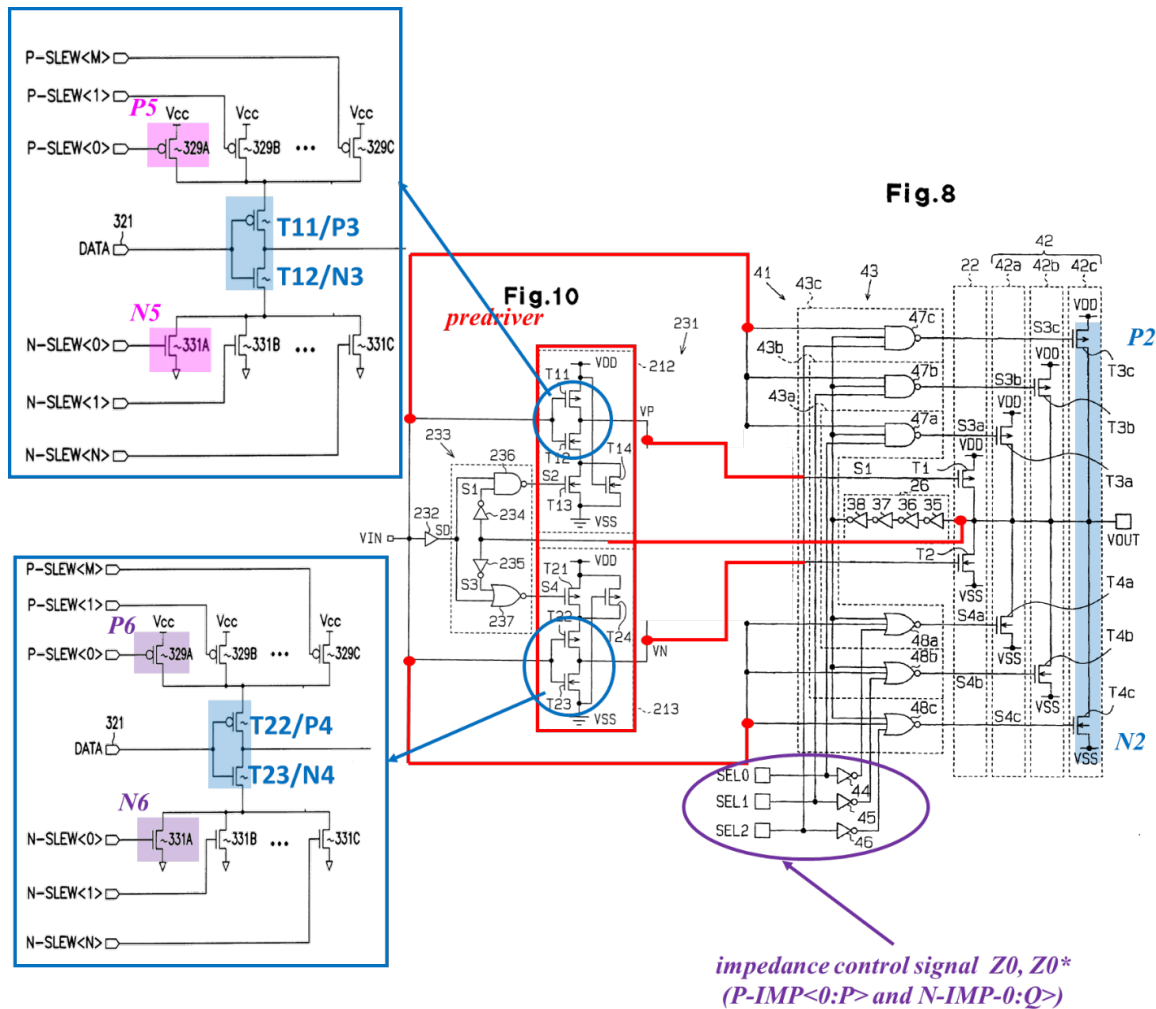


FIG. 1

EX1010, FIG. 1, annotated

As shown in Example 3.1 as illustrated below, the control signals control N5 and P5 (using slew rate control signals for generating VP to control P1) into and out of operation in coaction with P2 (using control signal P-IMP provided to the SEL0-SEL2 for controlling P2), and control P6 and N6 (using slew rate control signals for generating VP to control N1) into and out of operation in coaction N2

(using impedance control signal provided to SEL0-SEL2 and inverter, or directly providing to gates 48a, 48b, 48c).



Example 3.1 (Combination of Example Embodiment 2.1 and Muljono)

In Example 3.1, N5 and P5 in circuit 212 are controlled into and out of operation in coaction with P2, because the slew rate control signal for controlling N5 and P5 (for generating VP to drive P1) is generated in response to the

impedance control signal for controlling P2. EX1010, 6:36-45 (describing that the slew rate control signals are generated **in response to** the impedance control signals Z0, Z0*). Similarly, P5 is controlled into and out of operation in coaction with N2, because the slew rate control signal for controlling P5 (P-SLEW for generating VN to drive N1) is generated in response to the impedance control signal for controlling N2.

This configuration of controlling N5 into and out of operation in coaction with P2 and controlling P5 in and out of operation in coaction with N2 is similar to the configuration in the '539 patent. *See, e.g.*, EX1001, FIGS. 3, 4, and 7 (illustrating controlling N5 (e.g., QN17) into and out of operation in coaction with P2 (e.g., QP2) where the control signals for N5 and P2 are each generated using the same signals $\phi 3$ and VIN).

Accordingly, Itoh in view of Muljono renders obvious this limitation.

[5.4]

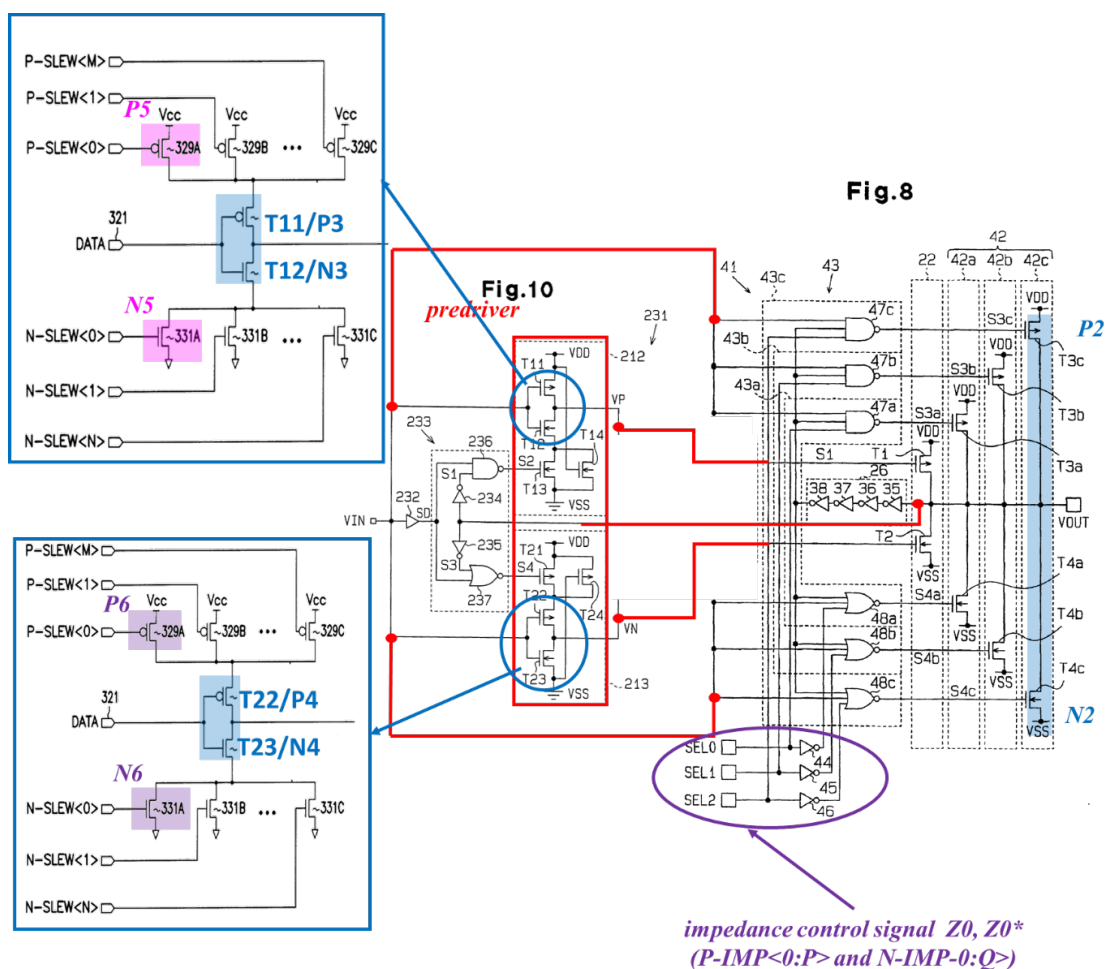
299. Itoh teaches this element for the reasons discussed at Ground 3:[1.4].

7. Claim 6

[6.0] *6. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistor [P5], said sixth n-channel MOS transistor [N6], and said sixth p-channel MOS transistor [P6] are equal to each other.*

300. Itoh in view of Muljono renders obvious this element.

301. As shown in Example 3.1 illustrated below, the number of P2 and N2 corresponds to the plurality of impedance control signals, which may be implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs. Similarly, the number of N5, P5, N6, and P6 corresponds to the plurality of slew rate control signals, each would have been implemented with any suitable number (e.g., 2, 3, 4, etc.) based on design needs.



Example 3.1
(Combination of Example Embodiment 2.1 and Muljono)

302. Accordingly, in a case where there are two N5, two P5, two N6, and two P6, and also circuit 42 in FIG. 8 includes four pairs of P2 and N2, then the number of N5, P5, N6, and P6 is eight, which is equal to the number (8) of P2 and N2.

303. Therefore, Itoh in view of Muljono renders obvious this element.

8. Claim 7

[7.0] *7. The output buffer circuit according to claim 5, wherein the number of said second p-channel MOS transistors [P2] and said second n-channel MOS transistors [N2], and the number of said fifth n-channel MOS transistors [N5], said fifth p-channel MOS transistors [P5], said sixth n-channel MOS transistors [N6], and said sixth p-channel MOS transistors [P6] are different from each other.*

304. Itoh in view of Muljono renders obvious this element.

305. As discussed at Ground 3:[6.0], the numbers of P2, N2, N5, P5, N6, and P6 may be implemented with any suitable numbers. Accordingly, in a case where there are three N5, three P5, three N6, and three P6, three P2, and three N2, then the number of N5, P5, N6, and P6 is twelve which is different from the number (6) of P2 and N2.

306. Accordingly, Itoh in view of Muljono renders obvious this element.

9. Claim 8

307. Itoh teaches this element for the reasons discussed at Ground 3:[4.0].

E. Grounds 4, 5, and 6: Combination of Itoh, Skorup, and Borkar (Ground 4), Combination of Itoh and Borkar (Ground 5), and Combination of Itoh, Muljono, and Borkar (Ground 6) Render Obvious Claims 9-12 Under §103(a)

308. The analysis for Grounds 4-6 relies on the analysis and evidence as provided for Grounds 1-3, respectively, except for where additional analysis (applying for each of Grounds 4-6) is provided below. Claims 9-12 are very similar to claims 1 and 5, with one new element—a delay monitor. The analysis for Grounds 4-6 is the same as the analysis for Grounds 1-3, respectively, with further reference to Borkar to show that the claimed delay monitor was obvious. For all the discussions below regarding Itoh, the analysis applies to Itoh’s embodiments (e.g., Fig. 5) as used in Ground 1, or a combination of Itoh’s embodiments (e.g., combination of Figs. 8 and 10) as applied in Grounds 2 and 3.

1. Reasons to Combine Itoh and Borkar

309. As discussed at Grounds 1-3 above, the combination of Itoh and Skorup, the combination of Itoh embodiments, and the combination of Itoh and Muljono similarly includes an output driver circuit as taught by Itoh.

310. A POSITA would have been motivated to apply Borkar’s teaching of dynamic compensation using a scaled down version of an output driver to monitor speed variations in the output driver circuit taught by Itoh (as applied at Grounds

1-3 above) to produce the obvious, beneficial, and predictable results of an improved “output driver design which is compensated to give steady performance for changes in temperature, process, and, power supply voltage” as taught by Borkar. EX1008, Borkar, 1:11-33.

311. First, Itoh and Borkar are analogous prior art to the ’539 patent, and like the ’539 patent, are in the same field of endeavor pertaining to output buffer circuits. *See, e.g.*, EX1001, ’539 patent, 1:15-19 (directed at “an output buffer circuit for use in an integrated semiconductor circuit device”); EX1006, Itoh, Title, 1:6-7 (“The present invention relates to an output buffer circuit.”); EX1008, Borkar, Abstract (describing an output driver “for high performance integrated circuits,” where the driver “dynamically compensates for variations in temperature, voltage, and process.”).

312. Second, Itoh and Borkar share the same goal of providing an output buffer circuit that generates an output signal with less variation. EX1006, Itoh, 14:38-53 (“As the control signals VP and VN and the external output signal VOUT swing fully, a change in pulse width **caused by the PTV variation is suppressed**, thus making it possible to generate the external output signal VOUT whose pulse width is substantially equal to the pulse width of the input signal VIN”); EX1008, Borkar, 1:11-34.

313. Accordingly, a POSITA would have been motivated to apply the

dynamic compensation using a scaled down version of an output driver to monitor speed variations as taught by Borkar in embodiments of Itoh, to produce the obvious, beneficial, and predictable results of an improved “output driver design which is compensated to give steady performance for changes in temperature, process, and, power supply voltage” as taught by Borkar. EX1008, Borkar, 1:11-33.

314. Finally, applying Borkar’s teachings in embodiments of Itoh would have been no more than the combination of known elements according to known methods (e.g., incorporating compensations circuits with a scaled down version of an output driver as delay monitor in an output buffer circuit according to the known IC design steps) obvious to a POSITA.

2. Claim 9

[9.0] 9. An integrated semiconductor circuit device comprising:

315. To the extent that the preamble is limiting, Itoh in view of Borkar renders it obvious.

316. Specifically, Itoh describes an integrated semiconductor circuit device. For example, Itoh describes that output driver circuits including PMOS and NMOS transistors, which are devices of an integrated semiconductor circuit device. *See, e.g.*, EX1006, Itoh, 7:9-13 (“The first drive circuit 22 includes a PMOS transistor (first output transistor) T1 and an NMOS transistor (second

output transistor) T2.”)

317. Similarly, Borkar describes an integrated semiconductor circuit device. Specifically, Borkar describes an “output driver for high performance **integrated circuits.**” EX1008, Borkar, Abstract. Borkar explains that “[o]utput drivers, which are also called output buffers, of **large scale integrated circuits (“chips”)**- when they switch-generate noise in the chip’s power supply lines,” and as such, there is a need for “a new output driver design which is compensated to give steady performance for changes in temperature, process, and power supply voltage.” EX1008, Borkar, 1:11-32.

318. Accordingly, the combination of Itoh and Borkar provides an integrated circuit including an output buffer circuit, which renders obvious “[a]n *integrated semiconductor circuit device*” as recited in the claim.

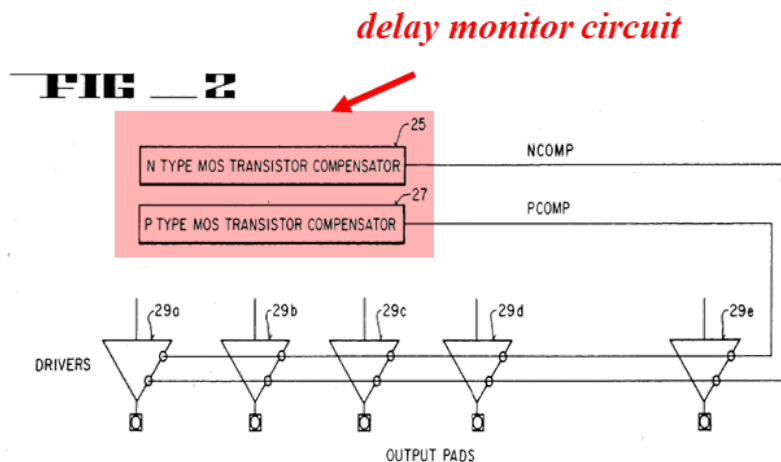
[9.1] an output buffer circuit according to claim 1;

319. Itoh in view of Skorup teaches this element for the reasons discussed at Ground 1:Claim 1; combination of embodiments Itoh teaches this element for the reasons discussed at Ground 2:Claim 1, and combination of Itoh and Muljono teaches this element for the reasons discussed at Ground 3:Claim 1.

[9.2] a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said control signals in the same manner as with said output buffer circuit,

320. Itoh in view of Borkar renders obvious this limitation.

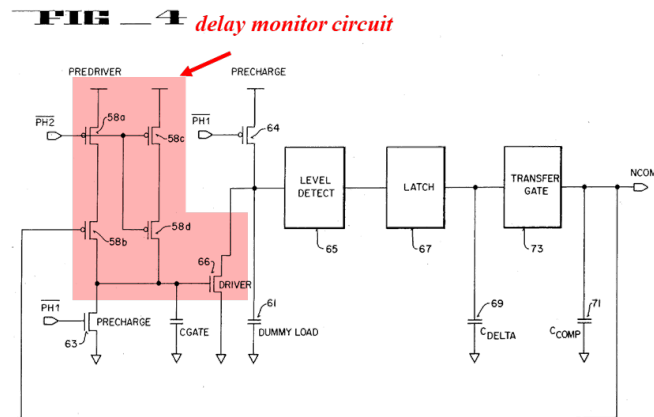
321. Specifically, as shown in annotated FIG. 2 of Borkar below, Borkar teaches a delay monitor circuit (compensator including N type MOS transistor compensator 25 and P type MOS transistor 27). EX1008, Borkar, 5:10-19 (“The compensator blocks 25 and 27 shown in FIG. 2 **track overall performance of the transistors, and produce two analog signals NCOMP and PCOMP**. The signals NCOMP and PCOMP vary between 0 volts and 5 volts (supply) and control the speed of the output drivers 29a-29e. Since the compensators 25 and 27 and the output drivers 29a-29e **reside on the same silicon die**, they track each other. The importance of this fact is that both are subject to the same thermal effects, the same process variations, and the same supply voltage.”).



EX1008, Borkar, FIG. 2, annotated

322. As shown in annotated FIG. 4 of Borkar below, Borkar’s compensator circuit includes a delay monitor circuit (including dummy driver 66 and predriver

including transistors 58c-58d) that is identical in circuit arrangement to an output buffer circuit and having transistors controlled according to said control signals (by assist transistors 58a and 58b) in the same manner as with said output buffer circuit. EX1008, Borkar, 7:5-9 (“The concept behind the compensator circuit, which generate the signals NCOMP and PCOMP, is shown in FIG. 4 which corresponds to N type MOS transistor compensator 25 of FIG. 2. It duplicates a scaled down version of a load that a driver usually drives.”); 7:11-15 (“To drive this load, it employs **a scaled down version of the driver, and a pre-driver**. This dummy driver 66 **is also compensated the same way the actual driver is**, by assist transistors 58a and 58b across the pre-drivers 58c and 58d.”).



EX1008, Borkar, FIG. 4, annotated

323. As such, in the embodiments of Itoh and Borkar, a delay monitor that is a scaled-down version of the output buffer circuit (e.g., Example Combination 1.1 of Ground 1, Example Combination 2.1 of Ground 2) is used to generate

compensation signals (e.g., NCOMP and PCOMP), where these compensation signals are provided to the output buffer circuit to compensating the PTV variations and control the speed of the output driver. *See, e.g.*, EX1008, Borkar, FIG. 3 (illustrating how NCOMP and PCOMP are used to compensate the PTV variations in the output driver).

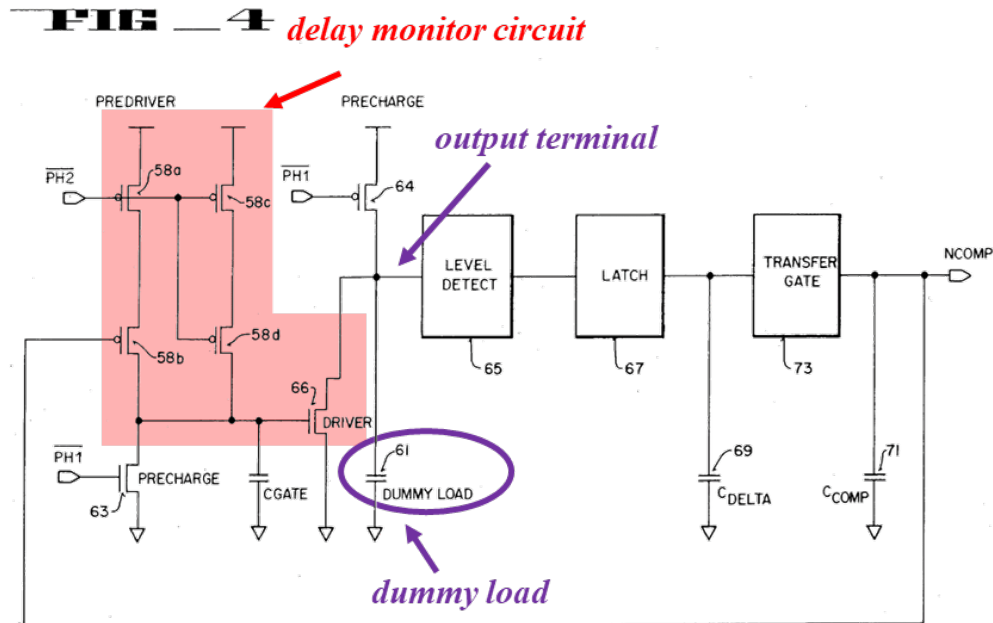
324. Therefore, Itoh in view of Borkar renders obvious that “a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said control signals in the same manner as with said output buffer circuit,” as recited in the claim.

[9.3] *said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.*

325. Itoh in view of Borkar renders obvious this limitation.

326. Specifically, as shown in annotated FIG. 5 of Borkar below, Borkar teaches that its delay monitor circuit (including predriver and dummy driver 66) having an output terminal connected to a dummy load 61. The dummy load 61 is a scaled down version determined from an actual load of said output buffer circuit, and it was well-known that such scaled down version is determined based on a transistor size ratio between said output buffer circuit and said delay monitor circuit. EX1008, Borkar, 7:5-9 (“The concept behind the compensator circuit, which generate the signals NCOMP and PCOMP, is shown in FIG. 4 which

corresponds to N type MOS transistor compensator 25 of FIG. 2. It duplicates a scaled down version of a load that a driver usually drives.”).



EX1008, Borkar, FIG. 4, annotated

327. Therefore, Itoh in view of Borkar renders obvious that “said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit,” as recited in the claim.

3. Claim 10

[10.0] 10. An integrated semiconductor circuit device comprising:

328. Itoh in view of Borkar renders obvious this limitation for the reasons

discussed at [9.0].

[10.1] *an output buffer circuit according to claims 5; and*

329. Itoh in view of Skorup teaches this element for the reasons discussed at Ground 1:Claim 5; combination of embodiments of Itoh teaches this element for the reasons discussed at Ground 2:Claim 5, and combination of Itoh and Muljono teaches this element for the reasons discussed at Ground 3:Claim 5.

[10.2] *a delay monitor circuit identical in circuit arrangement to said output buffer circuit and having transistors controlled according to said control signals in the same manner as with said output buffer circuit,*

330. Itoh in view of Borkar renders obvious this limitation for the reasons discussed at [9.2].

[10.3] *said delay monitor circuit having an output terminal connected to a dummy load determined from an actual load of said output buffer circuit based on a transistor size ratio between said output buffer circuit and said delay monitor circuit.*

331. Itoh in view of Borkar renders obvious this limitation for the reasons discussed at [9.3].

4. Claim 11

[11.0] *11. The integrated semiconductor circuit device according to claim 9, wherein said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit.*

332. Itoh in view of Borkar renders obvious this limitation.

333. Specifically, Borkar describes that “a **scaled down version** of an output driver is used to monitor speed variations due to temperature, process, and

voltage, the output of which is fed back to the output driver which then performs the necessary compensation.” EX1008, Borkar, 4:14-19. A POSITA would have understood that Borkar’s delay monitor circuit, which is a scaled down version of the output buffer, uses transistors having a smaller device size (having a smaller gate width) than the transistors of the output buffer circuit. Such scaled down version of the delay monitor circuit achieves the benefit of using less area than the output buffer circuit.

334. Therefore, Itoh in view of Borkar renders obvious that “said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit,” as recited in the claim.

5. Claim 12

[12.0] 12. The integrated semiconductor circuit device according to claim 10, wherein said delay monitor circuit has transistors having a smaller device size with a smaller gate width than the transistors of said output buffer circuit.

335. Itoh in view of Borkar renders obvious this limitation for the reasons discussed at [11.0].

IX. DECLARATION

336. I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: August 8, 2023

A handwritten signature in black ink that reads "Scott E. Thompson". The signature is written in a cursive, flowing style. Below the signature is a solid horizontal line.

Scott E. Thompson