

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING
COMPANY LTD.,
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

Case No. IPR2025-00683
U.S. Patent No. 8,907,425

Declaration of Shauna L. Wiest regarding *James 2005*

I, Shauna L. Wiest, state and declare as follows:

I. Introduction

1. I have prepared this Declaration in connection with a petition for *inter partes* review of U.S. Patent No. 8,907,425, which I understand will be filed concurrently with this Declaration.

2. I am currently a senior research analyst with the Research & Information Services team at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP located at 3300 Hillview Avenue, Palo Alto, CA 94304.

3. I am over eighteen years of age, and I am competent to make this Declaration. I make this Declaration based upon my own personal knowledge, and my professional knowledge of library science practices.

4. I earned a Master of Science in Library Science degree from the University of North Carolina at Chapel Hill in 1999, and a Bachelor of Arts in Political Science degree from the University of California at San Diego in 1989. I have worked as a law librarian for over eighteen years. I have been employed in the Research & Information Services Department at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP since 2021. Before that, from 2000-2015, I was employed as a Law Librarian at Stoel Rives LLP, and from 2015-2016, I was employed as a Competitive Intelligence Specialist for Nossaman LLP. Additionally, as a graduate student at the University of North

Carolina at Chapel Hill, I served as an intern at the Environmental Protection Agency at Research Triangle Park (“EPA-RTP”) where one of my rotations included original cataloging for EPA technical documents, state agency reports and documents, international organization documents, dissertations, and, on occasion, monographs. In this role, I accessed OCLC, MARC records, and the EPA National Library Catalog daily.

II. Standard Library Practice for Receiving, Cataloging, and Making Materials, including Conference Publications, Publicly Available

5. I have knowledge of and experience with standard library practices regarding the receipt, cataloging, shelving, and making materials, including conference publications, available to the public. I have knowledge of and experience with the Machine-Readable Cataloging (MARC) system, an industry-wide standard that libraries use to catalog materials. I also have knowledge of and experience with OCLC (previously called Online Computer Library Center, Inc.) and OCLC Control Numbers, which are unique accession numbers assigned by the OCLC system when a bibliographic record is catalogued and made available to the public through WorldCat. OCLC control numbers are often used by the public to search for specific records within WorldCat, the latter being an online global catalog of 559,887,458 individual bibliographic records from libraries all over the world (as of June 2024) (Source: <https://www.oclc.org/en/worldcat/inside-worldcat.html>).

6. Based on standard library practice, when a library receives a print item, the cataloguer or cataloguer's assistant will examine the item and date-stamp and/or affix a label to the item with the library name and/or barcode with the date it was received. Next, the library will catalog the item within a few days of receiving it. As a general practice, cataloguing is centralized and performed by a cataloguing department within a library or university setting.

7. Normally, after an item is cataloged, the public may access the item by searching a library online catalog, browsing the physical library shelves, searching a physical card catalog, or by seeking assistance from a Librarian to identify the item. Standard library practice is to make an item available to the public within several days of cataloging it. If an item requires original cataloguing, the item will be made available to the public up to and including one week from the date of receipt.

III. Ownership and Date-Stamp

8. Libraries have different policies on whether to date-stamp received publications. It is becoming increasingly common for libraries to no longer date-stamp the publications they receive. Historically, it was common practice to affix an ownership and date stamp somewhere within the publication, usually on the cover page, verso of the cover page, or a designated page within the publication. The timing of when an ownership/date stamp is placed on the monograph or

periodical can vary from one library to another. It could occur when the item is received in acquisitions after shipment to the library, or at the time of cataloging.

IV. MARC Records

9. The MARC system was developed during the 1960s to standardize bibliographic catalog records so they could be read by computers and shared among libraries. By the mid-1970s, MARC had become the international standard for cataloging bibliographic materials and is still used today. Many libraries provide public access to their MARC records via their electronic cataloging systems at the library. In a MARC record, each field provides specific information about the cataloged item, including how materials are held and when they were made available to the public.

10. The MARC record system uses specific three-digit numeric codes (“field tags”) (from 001-999) to identify each field in a catalog record. For example, field tag 008 provides the six-digit date an item was catalogued (*Date entered on file*). The first six characters of field tag 008 are always in the “**YYMMDD**” format. Descriptions and definitions of all the character positions of field tag 008 are outlined here:

<https://www.loc.gov/marc/bibliographic/bd008a.html>.

11. As is relevant to this Declaration, MARC field tag 020 sets forth the International Standard Book Number (“ISBN”), a unique identification number

assigned to every book or monograph publication. MARC field tag 245 sets forth the Title and statement of responsibility for a work. MARC field tag 264 sets forth information relating to the place of publication, printing, distribution, and copyright date. MARC field tag 505 sets forth notes regarding a work's formatted contents, including the individual titles of separate works, contained within a work.

V. Monograph versus Serials Cataloguing of Conference Proceedings

12. Conference proceedings often consist of a collection of individual papers presented at a meeting, symposium or conference held during a specific time-period in a designated geographic place. Although some ongoing conference publications are catalogued as serials (if a conference publication exhibits evidence of seriality after the first issue and it does not contain a distinctive title or series number), cataloguing a conference publication as a monograph can provide the public a way to easily locate and access the conference resource, and its papers, by searching by a unique title, topic, or other data points based on descriptive elements of the conference proceeding. Monographs are efficient for public searching and offer the public an easier way to discover what an institution holds, while changes to the record are not an issue.

VI. IEEE Xplore

13. The IEEE Xplore digital library located at <https://ieeexplore.ieee.org/Xplore/home.jsp> is an online resource for public searching, retrieval, and discovery of scientific and technical content published by the Institute of Electrical and Electronics Engineers (“IEEE”) and its publishing partners. IEEE Xplore provides web access to more than 6 million technical documents from some of the world’s most highly cited publications in electrical engineering, computer science, and electronics. Approximately 25,000 new documents are added to IEEE Xplore each month. Access to full-text documents in IEEE Xplore can be obtained through institutional subscriptions, subscriptions available to IEEE member and IEEE society members, and online purchase of individual documents by the public without a subscription. Anyone, including the public, may search IEEE Xplore for free without a subscription or membership. More details are here: <https://ieeexplore.ieee.org/Xplorehelp/overview-of-ieee-xplore/about-ieee-xplore>.

14. It is the regular practice of IEEE to publish articles and other writings including article abstracts and make them available to the public through IEEE Xplore. IEEE maintains copies of publications on IEEE Xplore in the ordinary course of its regularly conducted activities.

15. The date of publication for journals and standards on IEEE Xplore represents the first instance of public dissemination. IEEE Xplore previously made distinctions between the online publication date and the print publication date. This was simplified to reflect a single publication date of record as defined above and detailed here:

<https://ieeexplore.ieee.org/Xplorehelp/working-with-documents/publication-dates>.

16. IEEE publishes more than 2000 conference proceedings each year in various technology areas which are recognized by academia and industry worldwide. Conference proceedings in IEEE Xplore indicate the “Date of Conference,” which is the date of the event, and “Date Added to IEEE Xplore” which is the date the proceedings were made available to the public on the IEEE Xplore platform. Copies of conference proceedings are generally made available to the public no later than the last day of the conference.

VII. U.S. Copyright Office Records

17. The United States Copyright Office, a part of the Library of Congress, is the official U.S. government body that maintains copyright certificates and copyright records of registration in the United States, including providing public access to an online catalog of copyright records held by the Copyright Office. The copyright records contained in the public catalog are routinely used by copyright

title researchers who are attempting to clear a chain of title for copyrighted works. The records contained in the public catalog also denote the date of creation and the date of publication of the copyrighted work.

VIII. Public Availability of *James 2005*

18. This Declaration relates to the date of receipt, accessibility, and public availability of the following reference: D. James, “2004 - the year of 90-nm: a review of 90 nm devices,” in IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing, April 11-12, 2005, Munich, Germany, pages 72-76 (2005) (“*James 2005*”). I understand that *James 2005* is being submitted as **Exhibit Ex-1012** in this proceeding.

19. As detailed below, I have reviewed the print *James 2005* reference, which was supplied by North Carolina State University; the U.S. Copyright Record for the IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing 2005 containing *James 2005*; and the IEEE Xplore website record for the *James 2005* reference to determine the date of public accessibility and availability for this reference.

20. **Appendix A** to this Declaration is a true and accurate copy of the cover page, title page, and table of contents for the print issue of 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 11-12 April 2005, Munich, Germany, held by the James B. Hunt Jr. Library at North Carolina

State University. **Appendix A** also includes pages 72-77 of the conference proceedings, which comprise the reference: D. James, “2004 - the year of 90-nm: a review of 90 nm devices,” i.e., *James 2005*. **Appendix A** also sets forth the unique International Standard Book Number (ISBN) for 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 11-12 April, containing *James 2005* as 0780389964.

21. **Appendix B** to this Declaration is a true and accurate copy of the North Carolina State University James B. Hunt Jr. Library public catalog record for its copy of 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James 2005*, which was downloaded from <https://catalog.lib.ncsu.edu/catalog/NCSU1850414> on March 7, 2025.

22. The North Carolina State University, James B. Hunt Jr. Library public catalog record (**Appendix B**) sets forth the publication, contents, and holdings information for its copy of 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James 2005*. The public catalog record indicates that the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop contains “2004 -the year of 90-nm: a review of 90 nm devices / Dick James,” i.e., the *James 2005* reference. **Appendix B** also denotes that the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James 2005* bears the ISBN of 0780389964,

and that the print volume containing *James 2005* is located at Call Number TK7871.85. I25 2005 in the James B. Hunt Jr. Library located at North Carolina State University.

23. **Appendix C** to this Declaration is a true and accurate copy of the North Carolina State University James B. Hunt Jr. Library MARC record for its holdings of 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James 2005*, which was downloaded from <https://catalog.lib.ncsu.edu/catalog/NCSU1850414> (Click on “View MARC”) on March 7, 2025.

24. **Appendix C** confirms the fixed data elements of MARC field tag 008 as 050715t20052005nyuab1010engd. As discussed above, the first six characters “050715” are in typical “**YYMMDD**” format and indicate that the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James* was catalogued by North Carolina State University on July 15, 2005, and bears a publication date and copyright date of 2005.

25. MARC record (**Appendix C**) field tag 020 sets forth the unique ISBN number belonging to 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop containing *James 2005* as 0780389964. MARC field tag 245 sets forth the title and statement of responsibility for 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop as ASMC

2005 Proceedings: Advancing Semiconductor Manufacturing Excellence, IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 11-12 April 2005, Munich, Germany, bearing a copyright date of 2005. MARC field tag 264 sets forth information relating to the place of publication, printing, distribution, and copyright date for 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop as |a[New York] :|bIEEE ;|aPiscataway, N.J. :|bIEEE Operations Center,|c[2005].|c©2005. Finally, MARC field tag 505 in **Appendix C** includes the individual titles of the separate works contained within 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop. MARC field tag 505 denotes *t2004 -the year of 90-nm: a review of 90 nm devices* /rDick James, which constitutes the *James 2005* reference.

26. Based on the information set forth in **Appendices A, B, and C** attached to this Declaration, standard library practices, and my experience as a librarian, the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop print resource containing *James 2005* was catalogued by the North Carolina State University James B. Hunt Jr. Library on July 15, 2005.

27. Accordingly, the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop print resource containing *James 2005* would have subsequently been made available to the public within a few days of being checked-in and catalogued. The interested public could have accessed the

2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop print resource containing *James 2005* by (i) searching the North Carolina State Library catalog, visiting the James B. Hunt Jr. Library and searching the stacks at Call Number TK7871.85 .I25 2005; or (ii) by asking a Library staff member and being directed to the print resource located in the James B. Hunt Jr. Library at Call Number TK7871.85 .I25 2005 within a few days of July 15, 2005.

IX. United States Copyright Office Records for *James 2005*

28. Section IX of this Declaration relates to date of publication for the United States Copyright Office records for *James 2005*.

29. **Appendix D** to this Declaration is true and accurate copy of the United States Copyright Office public record for “2005 IEEE/SEMI advanced semiconductor manufacturing conference and workshop” containing *James 2005* with registration record number TX0006208233, which was retrieved from https://cocatalog.loc.gov/cgi-bin/Pwebrecon.cgi?Search_Arg=TX0006208233&Search_Code=REGS&PID=g8oI-3lrGE_wj-nnCpu8EmX&SEQ=20250307134052&CNT=25&HIST=1 on March 7, 2025. **Appendix D** denotes a publication date of “2005-04-11,” or April 11, 2005, and a date of creation of “2005.” It also denotes a copyright registration date of June 24, 2005. In my professional opinion, **Appendix D** is the official United States Copyright Office record for “2005 IEEE/SEMI

advanced semiconductor manufacturing conference and workshop” containing *James 2005*. I believe that the United States Copyright Office date of publication for TX0006208233 as April 11, 2005, a copyright registration date of June 24, 2005, with a date of creation noted as 2005, to be accurate, true, and correct.

30. **Appendix J** to this Declaration is true and accurate copy of the official United States Copyright Office Certificate of Registration for “2005 IEEE/SEMI Advanced semiconductor manufacturing conference and workshop (05CH37654)” containing *James 2005* with registration record number TX6208233.

31. **Appendix J** denotes an effective date of registration for *James 2005* as June 24, 2005 (including an application and two deposits received on June 24, 2005) and the date and nation of first publication for *James 2005* as April 11, 2005 in the United States.

32. In my professional opinion, **Appendix J** is the official United States Copyright Office Certificate of Registration for “2005 IEEE/SEMI advanced semiconductor manufacturing conference and workshop (05CH37654)” containing *James 2005*. I believe that the United States Copyright Office effective date of registration of publication for TX6208233 as June 24, 2005, and the date and nation of first publication for *James 2005* as

April 11, 2005 in the United States, to be accurate, true, and correct. The general public could have accessed *James 2005* by searching the United States Copyright Office physical and/or online catalogs on or around July 1, 2005.

X. IEEE Xplore Record for *James 2005*

33. Section X of this Declaration relates to the date of public availability for the following reference: D. James, “*2004 - the year of 90-nm: a review of 90 nm devices*,” in IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing, April 11-12, 2005, Munich, Germany, pages 72-76 (2005) (“*James 2005*”) retrieved from the IEEE Xplore online platform.

34. On March 7, 2025, I used Google Chrome to search for and navigate to the IEEE.org website at <https://www.ieee.org/>, which is attached to my Declaration as **Appendix E**. From **Appendix E**, I selected “IEEE Xplore Digital Library” located on the black banner at the top of the page. This brought me to the webpage for “IEEE Xplore Digital Library,” which is attached to my Declaration as **Appendix F**. Please note: **Appendix F** often displays a Finnegan banner even when I am signed out of the resource because Finnegan's access to IEEE Xplore is authenticated based on IP address. Although logged out, the system still recognizes the IP address from which I am accessing IEEE Xplore as belonging to Finnegan. It is important to note that what the public sees (including the type of banner) when

accessing IEEE Xplore will vary depending on their location and the conditions under which they access the platform.

35. From **Appendix F**, I entered “2004 - the year of 90-nm: a review of 90 nm devices” in the search box, which resulted in the webpage <https://ieeexplore.ieee.org/search/searchresult.jsp?newsearch=true&queryText=%E2%80%9C2004%20-%20the%20year%20of%2090-nm:%20a%20review%20of%2090%20nm%20devices%E2%80%9D>, attached here as **Appendix G**. From **Appendix G**, I clicked on the link for “2004 - the year of 90-nm: a review of 90 nm devices,” which brought me to the page <https://ieeexplore.ieee.org/document/1438770>, which is attached to my Declaration as **Appendix H**.

36. **Appendix H** sets forth that the IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing 2005 containing *James 2005* occurred on April 11-12, 2005, in Munich, Germany and was added to IEEE Xplore on June 13, 2005.

37. On March 7, 2025, from the website listed in **Appendix H** (<https://ieeexplore.ieee.org/document/1438770>), I clicked on “PDF” and was taken to a payment page to purchase a copy (“Purchase Now”) of “2004 - the year of 90-nm: a review of 90 nm devices.” I used my credit card and paid the cost of the article - \$34.98. I next clicked on “View PDF” and was taken to a “Get PDF”

viewer where I downloaded “2004 - the year of 90-nm: a review of 90 nm devices,” which is attached to my Declaration as **Appendix I**. I compared **Appendix I** with **Appendix A** and, except for formatting differences, they are the same document.

38. It is my professional opinion that members of the public could have accessed the conference proceeding titled “IEEE/SEMI Conference and Workshop on Advanced Semiconductor Manufacturing 2005” containing *James 2005* by either attending the conference in person during April 11-12, 2005 in Munich, Germany, or by visiting the IEEE Xplore website using the steps above on or after June 13, 2005.

XI. Conclusion

39. In signing this Declaration, I understand it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I understand I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

40. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that

Declaration of Shauna L. Wiest

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on March 10, 2025, in Palo Alto, California

/Shauna L. Wiest/

Shauna L. Wiest

Appendix A

2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop (ASMC)

**Munich, Germany
April 11-12, 2005**



**IEEE Catalog Number: 05CH37654
ISBN 0-7803-8996-4**

71.85

05

**Advanced Semiconductor
Manufacturing Conference and Workshop**



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ASMC 2005 PROCEEDINGS
11– 12 April, 2005
Munich, Germany

The IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop is an annual forum that provides a venue for the presentation of methodologies, approaches and techniques required to achieve world-class semiconductor manufacturing. A key role this conference plays is in promoting interaction among semiconductor professionals at all levels. The goal and objective of the conference are to assist in making the participating companies more knowledgeable of semiconductor production methods, encourage open communication between participants, and develop the strategic relationship between users and suppliers needed to achieve manufacturing excellence and improve global competitiveness.

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- Semiconductor Thermal and Temperature Management (SEMI-THERM) Symposium
- International Electron Devices Meeting (IEDM)
- International Symposium on Semiconductor Manufacturing (ISSM)
- Intersociety Conference on Thermal Phenomena in Electronic Systems (I-THERM)
- Electronic Components & Technology Conference (ECTC)
- International Electronic Manufacturing Technology (IEMT) Symposium

Copies of past proceedings of some of these conferences are available for purchase. In addition, EDS and CPMTS publish the Transactions on Semiconductor Manufacturing, the archival journal in this field. We invite you to consider membership for one of the IEEE Societies and to participate with us in furthering advancements in these fields. If you already belong to another professional society, you can affiliate with EDS or CPMT at reduced fees.

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2004 – The Year of 90-nm: A Review of 90 nm Devices

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Abstract

The year 2004 saw the introduction of the first 90-nm process node devices into the marketplace. This node is notable not only for the expected reduction in feature sizes, but also for the more general adoption of low-k dielectric layers, and the first use of nickel silicide and strained silicon.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of chip processes as they come into commercial production. Chipworks has obtained parts from leading edge manufacturers, and performed structural analyses to examine the features and manufacturing processes of the devices.

The paper shows how “90nm” has been interpreted by various vendors, details the physical transistor structures we have analyzed, and comments on the introduction of strain into CMOS processing.

INTRODUCTION – WHAT IS 90 NM?

We continually see parts labeled as “130 nm” or “90 nm”. To the uninitiated, this must seem to be some form of code, but it is actually just industry jargon for a process generation or ‘node’.

The 199□ NTRS (National Technology Roadmap for

Semiconductors) predicted a minimum feature size of 130 nm in 200□ with a 90 nm feature size in 2008. It is a reflection of the frenetic pace of process development that we are currently seeing feature sizes of less than 50 nm, and metal pitches ~230 nm.

Table 1 shows a comparison of the metal 1 half-pitch and minimum gate dimensions that we found in the samples analyzed by Chipworks. As can be seen, no manufacturer meets the actual ITRS numbers – Intel is closest in M1 dimensions, and Fujitsu the closest in gate length.

90-NM TRANSISTORS

Sony/Toshiba CXD9797GB from Sony PSX

Toshiba was the first off the mark in January, with the Sony PSX chip, which combined the Sony graphics synthesizer with their Emotion Engine™ on one die. The process used five layers of copper + one aluminium, two low-k layers at metal 2 and metal 3 (M2 and M3), and a □5 nm minimum gate.

Figure 1 shows a SEM image of NMOS transistors stained to show the source/drains. Figure 2 is a TEM image; the structure of the sidewall spacers can be seen. In essence, this seems to be a dimensional shrink from the previous generation.

Table 1. Comparison of Published and Found Dimensions with ITRS 2003 Dimensions for the 90nm Node

	Metal 1 Half-Pitch (nm)		Minimum Gate Length (nm)	
	Published	Found	Published	Found
ITRS 2003 (MPU/ASIC)	107		37	
Sony/Toshiba	120	130	65	□5
Texas Instruments	165	165	52	□7
Intel	110	120	50	□5
IBM	158	135	□6	□5
UMC (Xilinx)	2□0	2□0	70	55
TSMC (Altera)	120	125	59	55
Fujitsu (Transmeta)	1□0	1□5	□0	□0
AMD	N/A	130	N/A	□9

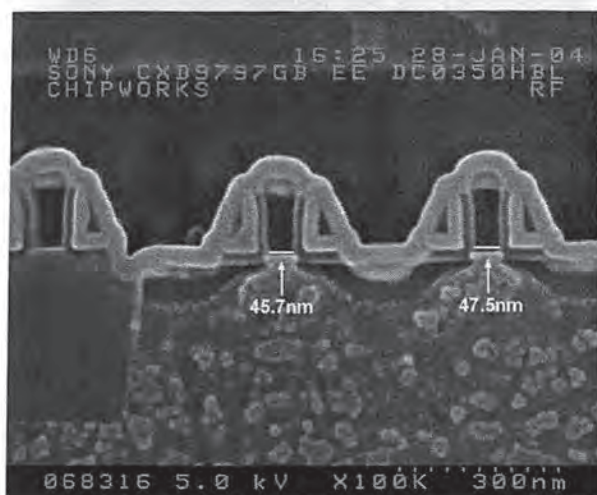


Figure 1. SEM Cross-Section of NMOS Transistors in Sony PSX

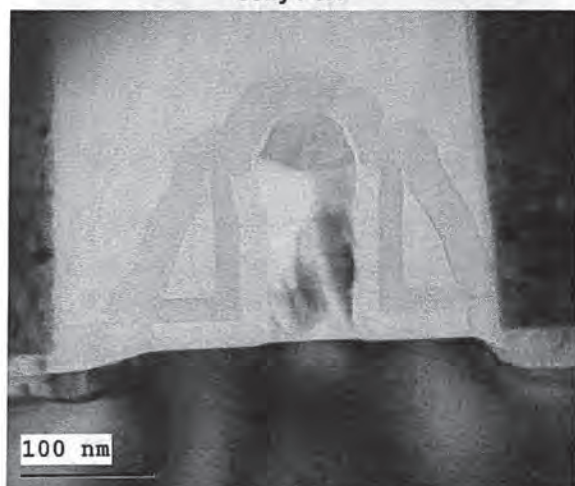


Figure 2. TEM Cross-Section of Sony PSX Transistor

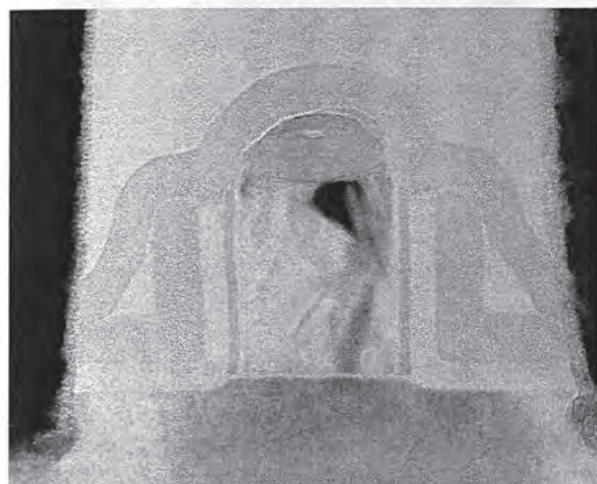


Figure 3. Transistor in TI DSP

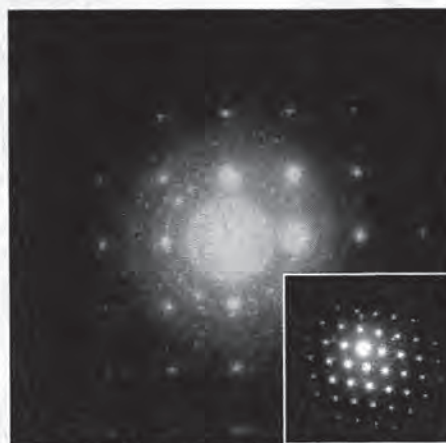


Figure 4. TEM Electron Diffraction Image of TI Transistor Channel Region (Inset – Intel Prescott, $\langle 110 \rangle$ Channel Direction)

Texas Instruments TMX320C6416T 1 GHz DSP

The TI DSP is a 7-metal part, with low-k at M1 – M7. The transistor again appears to be a shrink down to a 7 nm gate length, with a nitride liner on the side of the gate electrode. Figure 3 is a TEM image of the transistor cross-section.

The distinguishing feature of the TI process revealed itself in an electron diffraction image (Figure 4). This showed that the channel was oriented in the $\langle 100 \rangle$ direction, compared with the more normal $\langle 110 \rangle$ direction. This orientation gives higher PMOS mobility.

Intel Prescott

Intel first announced their 90-nm P1262 process in March 2002. Process details such as the use of strained silicon and nickel silicide were given later in the year and at the 2002 IEDM [1], and at IEDM 2003 Intel showed the different strain techniques for NMOS and PMOS transistors [2]. The Prescott die analysed by Chipworks had seven metal levels, with five low-k layers at M2 – M7.

An NMOS transistor is imaged in Figure 5. Localized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer, in undercut regions under the edges of the sidewall spacers. This increases electron mobility by ~10%. The gate oxide thickness is ~1.3 nm.

The PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress – this improves hole mobility by as much as 50%. The substrate is etched out in the source/drain regions, and local epi-SiGe (~17% Ge) is deposited into the cavities. Crystalline facets form raised source/drains, reducing the series resistance. The tensile stress from the nitride layer is counteracted by the compressive effect.

The strain has induced dislocations at the SiGe/Si interface. The SiGe was likely *in-situ* boron-doped, and also implanted with the polysilicon gate implant. The boron

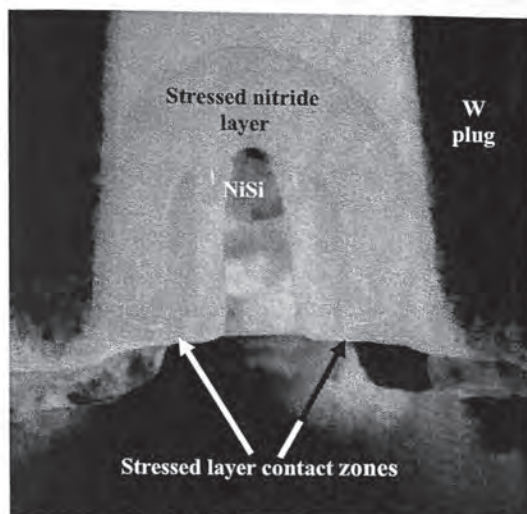


Figure 5. NMOS Transistor in Intel Prescott

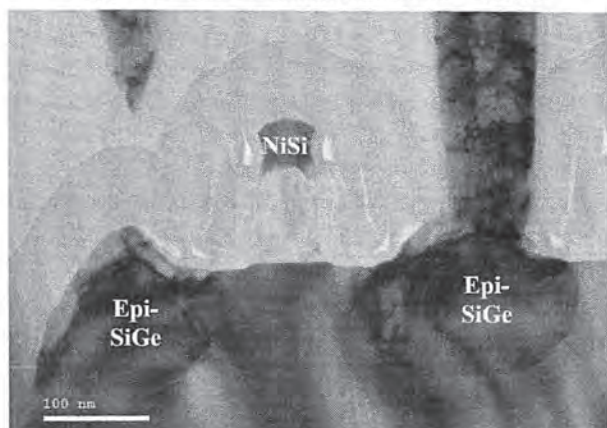


Figure 6. Intel PMOS Transistor

out-diffuses from the SiGe into the silicon to neutralize the potential leakage caused by the dislocations. Nickel silicide was chosen because it consumes less silicon and forms at a lower temperature, making it more compatible with the SiGe.

Figure 7 is a longitudinal section of a PMOS source/drain, clearly showing a stacking fault extending from the epitaxial interface to the silicide layer.

IBM PowerPC PC970FX

The IBM PowerPC is built on a 5 nm-thick SOI layer, with a 5 nm gate length with a 1.5 nm gate oxide thickness. The part has ten metal levels with a hybrid FSG/USG dielectric structure.

IBM had stated that the part would use strain technology, and press reports in the spring of 2000 speculated that the "Strained Silicon Directly on Insulator" (SSDOI) technique, which was announced at IEDM 2003 [3], would be used.

The device appears to use a stressed nitride layer to



Figure 7. Longitudinal Section of Intel PMOS Source/Drain

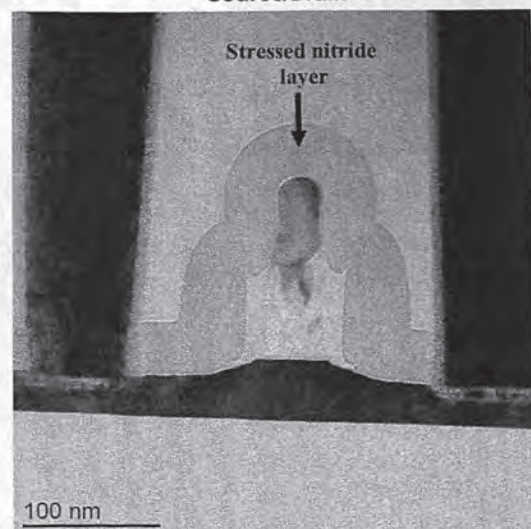


Figure 8. NMOS Transistor in IBM PPC970FX



Figure 9. PMOS Transistor in IBM PPC970FX

enhance the NMOS transistors. Figure 8 is a TEM image of a NMOS transistor, and it can be seen that the sidewall spacers are very slim, and it is only ~20 nm from the gate edge to the cobalt silicide of the source/drain. Comparison with a PMOS transistor (Figure 9) illustrates that the

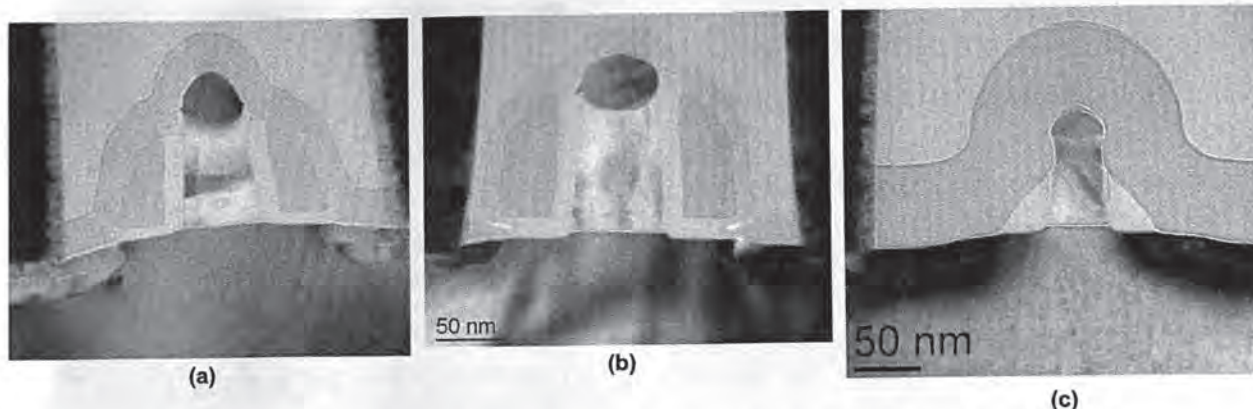


Figure 10. Transistors in (a) Xilinx Spartan-3, (b) Altera Stratix-II, (c) Transmeta Efficeon-2

NMOS spacers have indeed been etched back in order to reduce series resistance, and place the stressed nitride layer closer to the gate edge. Electron diffraction studies on the SOI body confirmed $\langle 110 \rangle$ -channel orientation, and there was no indication of a SSDOI substrate. The IEDM SSDOI paper indicated that $\sim 1.5\%$ lattice distortion was required to give useful mobility enhancement.

It is interesting to note that at IEDM 200 $\square$ IBM and AMD presented a joint paper [$\square$] on “dual stress liner” technology, which uses stressed nitride layers optimized to apply tensile stress to NMOS transistors, and compressive stress to PMOS devices.

This technique is to be integrated into 90-nm product in the first half of 2005. There was no mention of the use of SSDOI substrates.

UMC (Xilinx Spartan-3)

The Xilinx part was the first 90-nm part from a pure foundry analyzed by Chipworks. The transistor structure was very similar to the 130-nm node device, with the gate shrunk to 55 nm (Figure 10(a)). The gate length was smaller than the UMC-published value of 70 nm, but in other respects the part was manufactured using a more conservative process; FSG was used as the inter-metal dielectric, with seven copper + one aluminium metal levels (although UMC states that low-k dielectrics are available as an option).

There does not appear to be any use of strain to enhance mobility – the nitride layer is thinner than those used in strained devices, and there seems to be no structural changes to move the nitride contact zone closer to the gate edge. However, the gate edge/silicide distance is a respectably small $\square \sim 50$ nm.

TSMC (Altera StratixTM-II)

The other major foundry to launch a 90nm process in 200 $\square$ was TSMC. The product analyzed by Chipworks was the Altera StratixTM-II FPGA. This displayed a gate length of 55 nm, similar to UMC, although closer to the published 59

nm physical gate length of the NexsysTM process. This is another ten-metal part (9 Cu + 1 Al), using low-k at M1 – M6.

The transistor structure (Figure 10(b)) is not a direct shrink from the 130nm node; it has been modified to change the sidewall spacer structure from the typical L-shaped spacer of previous process generations. Again, the nitride layer appears to be too thin to be used as a stress layer for mobility enhancement. Gate/silicide spacing is ~ 55 nm.

The other major feature of the TSMC 90-nm process is its evolution towards a second-generation low-k dielectric process – the trench and via etching are noticeably cleaner than at the 130-nm node, and the cap layer has changed to a SiCO (rather than SiCN) composition.

Fujitsu (Transmeta Efficeon-2)

Transmeta announced shipment of its Efficeon-2 in September, fabricated by Fujitsu at their Akiruno Advanced Technology Center. This part also seems to use a strained nitride layer. Figure 10(c) displays what is becoming a characteristically thick nitride sealant layer, which combined with the heavily etched sidewall spacers, leads us to conclude that nitride stress is being used.

Fujitsu had announced the use of nitride strain for the 65-nm node at VLSI 2003 and 200 $\square$ [5][6], and they seem to have used the technique in their nominal 90-nm process. Given that the gate length is an impressively small $\square 0$ nm, and the gate length for the 65-nm process is quoted at 35 nm, this part could be regarded as an interim step to 65-nm. (They also published a dual-stress process at IEDM ‘0 $\square$ [7])

In addition, electron diffraction shows that the channels are oriented in the $\langle 100 \rangle$ direction, so Fujitsu is the first manufacturer to combine channel re-orientation and strain to optimise mobility.

The dielectric layers are also advanced, using Novellus Coral low-k (not SiLK!) with SiCO copper-cap and etch-stop layers at M1 – M5. It is an eight-metal part, again with a top aluminium layer.

AMD Athlon 64 Mobile

AMD continued their use of “double spacer” technology at the 90-nm node, with a gate shrink to ~50 nm. The NMOS device (Figure 11) consistently has dislocations under the inner spacer, presumably caused by the drain extension implant. These do not appear in the PMOS transistors (Figure 12), which likely have a different amorphisation implant to fix the drain extension.

There is no evidence of either nitride strain or substrate strain in this part; the nitride is relatively thick, and the double spacer places the contact zone further from the gate. The joint AMD/IBM “dual stress liner” paper [4] showed an Athlon fabricated with the technique, and announced production in 2005.

AMD have also evolved their interconnect structure for the 90-nm node, compared with the 130 nm; the metallisation (9 Cu + 1 Al) is now predominantly dual-damascene, although whilst the dielectric structure is still a hybrid low-k/FSG.

SUMMARY AND DISCUSSION

We have seen eight examples of 90-nm processes in this review, with transistor gate lengths ranging from 40 – 55 nm. Intel, IBM, and Fujitsu have introduced strain for mobility enhancement, and notably Intel has taken the extra steps of embedded SiGe strain for PMOS, and nickel silicide. Texas Instruments and Fujitsu have also used re-orientation of the substrates to improve mobility.

It appears that 90-nm is the node at which strained silicon is coming into production, although not by using epitaxially strained substrates. The strain method of choice has been localised uni-axial strain, as opposed to the bi-axial strain created by strained SiGe layers.

It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown), but the dual-stress approach announced by IBM/AMD and Fujitsu indicates that the layer can also be tuned to provide compressive stress to improve hole mobility for PMOS devices. This technique has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates.

It remains to be seen if the embedded SiGe approach used by Intel will become the dominant method of applying compressive stress for PMOS. Texas Instruments has indicated that it will be using local SiGe strain and nickel silicide in its 65-nm process [8], so Intel will not be alone.

All in all, 2004 was an important year in CMOS process evolution, with significant developments in transistor engineering, and further improvement in low-k dielectric usage. We will see what 2005 brings!

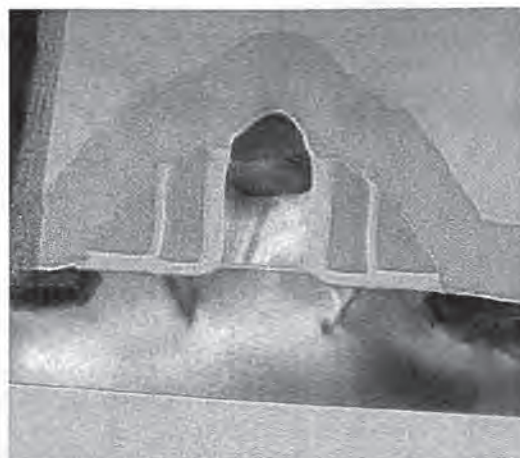


Figure 11. NMOS Transistor in AMD Athlon

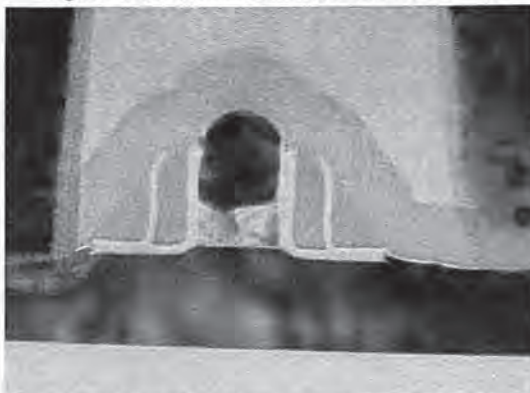


Figure 12. PMOS Transistor in AMD Athlon

ACKNOWLEDGEMENTS

I would like to thank Chipworks' laboratory staff and process analysts, and our contractors, who actually did all the hard work of analyzing these complex devices. They did a great job!

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BIOGRAPHY

Dick James graduated in 1971 with a Masters degree in Microelectronics and Semiconductor Devices from the University of Southampton in England, after gaining a B.Sc in Applied Chemistry from the University of Salford. He has spent over 30 years working in the process development, design, manufacturing, packaging and reverse engineering of semiconductor devices. He joined the Chipworks team in March 1995 as Manager, Microstructural Characterization, and is currently Senior Technology Analyst.

He is a member of the Electrochemical Society, the Institute of Electrical and Electronics Engineers, and the Society for Information Display.

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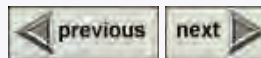
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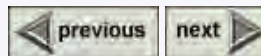
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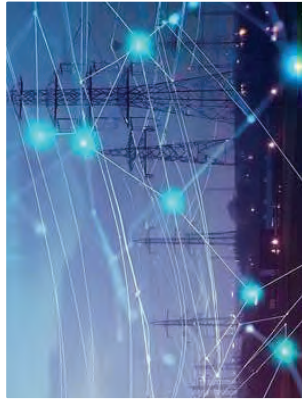
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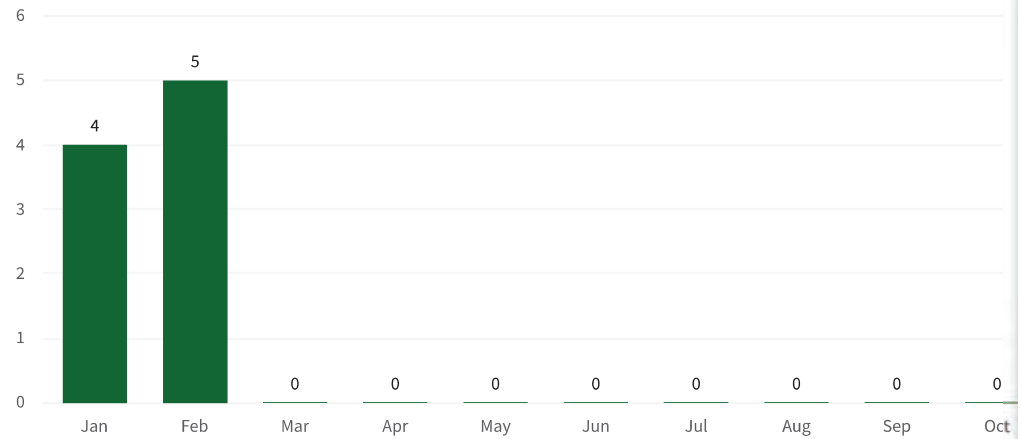
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Appendix

2004 – The Year of 90-nm: A Review of 90 nm Devices

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Abstract

The year 2004 saw the introduction of the first 90-nm process node devices into the marketplace. This node is notable not only for the expected reduction in feature sizes, but also for the more general adoption of low- k dielectric layers, and the first use of nickel silicide and strained silicon.

Chipworks, as a supplier of competitive intelligence to the semiconductor and electronics industries, monitors the evolution of chip processes as they come into commercial production. Chipworks has obtained parts from leading edge manufacturers, and performed structural analyses to examine the features and manufacturing processes of the devices.

The paper shows how “90nm” has been interpreted by various vendors, details the physical transistor structures we have analyzed, and comments on the introduction of strain into CMOS processing.

INTRODUCTION – WHAT IS 90 NM?

We continually see parts labeled as “130 nm” or “90 nm”. To the uninitiated, this must seem to be some form of code, but it is actually just industry jargon for a process generation or ‘node’.

The 1994 NTRS (National Technology Roadmap for

Semiconductors) predicted a minimum feature size of 130 nm in 2004, with a 90 nm feature size in 2008. It is a reflection of the frenetic pace of process development that we are currently seeing feature sizes of less than 50 nm, and metal pitches ~230 nm.

Table 1 shows a comparison of the metal 1 half-pitch and minimum gate dimensions that we found in the samples analyzed by Chipworks. As can be seen, no manufacturer meets the actual ITRS numbers – Intel is closest in M1 dimensions, and Fujitsu the closest in gate length.

90-NM TRANSISTORS

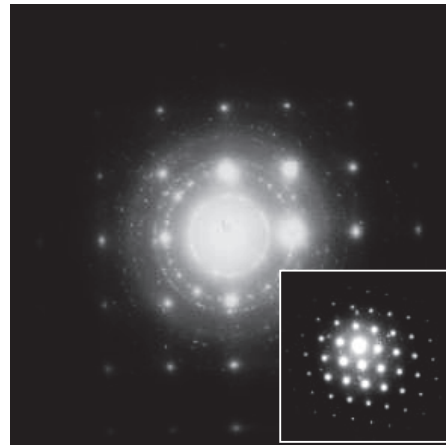
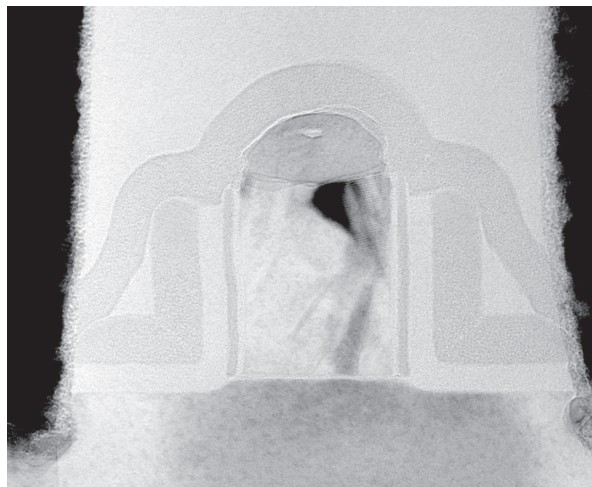
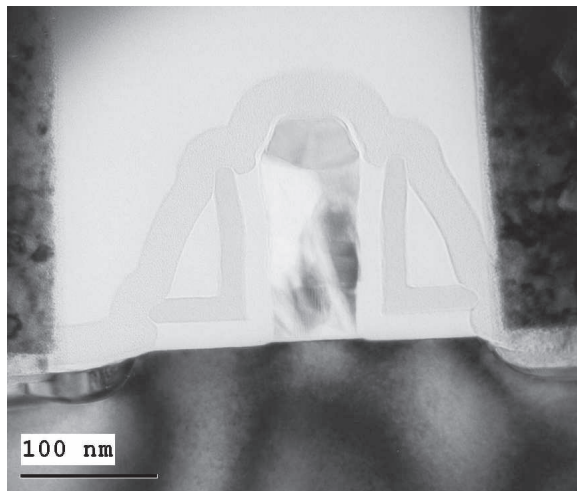
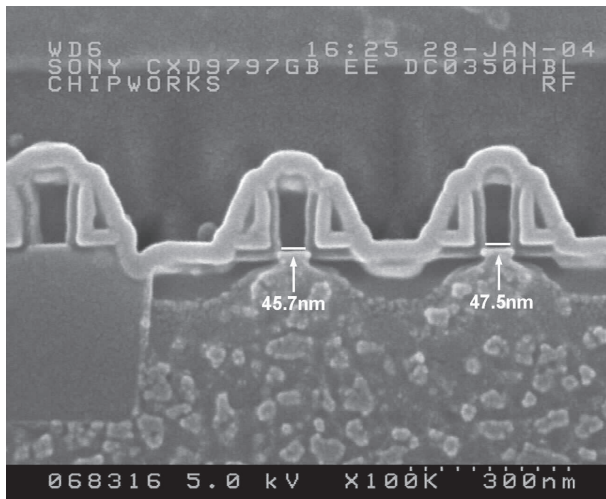
Sony/Toshiba CXD9797GB from Sony PSX

Toshiba was the first off the mark in January, with the Sony PSX chip, which combined the Sony graphics synthesizer with their Emotion Engine™ on one die. The process used five layers of copper + one aluminium, two low-k layers at metal 2 and metal 3 (M2 and M3), and a 45 nm minimum gate.

Figure 1 shows a SEM image of NMOS transistors stained to show the source/drains. Figure 2 is a TEM image; the structure of the sidewall spacers can be seen. In essence, this seems to be a dimensional shrink from the previous generation.

Table I. Comparison of Published and Found Dimensions with ITRS 2003 Dimensions for the 90nm Node

	Metal 1 Half-Pitch (nm)		Minimum Gate Length (nm)	
	Published	Found	Published	Found
ITRS 2003 (MPU/ASIC)	107		37	
Sony/Toshiba	120	130	65	45
Texas Instruments	165	165	52	47
Intel	110	120	50	45
IBM	158	135	46	45
UMC (Xilinx)	240	240	70	55
TSMC (Altera)	120	125	59	55
Fujitsu (Transmeta)	140	145	40	40
AMD	N/A	130	N/A	49



Texas Instruments TMX320C6416T 1 GHz DSP

The TI DSP is a 7-metal part, with low-k at M1 – M4. The transistor again appears to be a shrink down to a 47 nm gate length, with a nitride liner on the side of the gate electrode. Figure 3 is a TEM image of the transistor cross-section.

The distinguishing feature of the TI process revealed itself in an electron diffraction image (Figure 4). This showed that the channel was oriented in the $\langle 100 \rangle$ direction, compared with the more normal $\langle 110 \rangle$ direction. This orientation gives higher PMOS mobility.

Intel Prescott

Intel first announced their 90-nm P1262 process in March 2002. Process details such as the use of strained silicon and nickel silicide were given later in the year and at the 2002 IEDM [1], and at IEDM 2003 Intel showed the different strain techniques for NMOS and PMOS transistors [2]. The Prescott die analysed by Chipworks had seven metal levels, with five low-k layers at M2 – M7.

An NMOS transistor is imaged in Figure 5. Localized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer, in undercut regions under the edges of the sidewall spacers. This increases electron mobility by $\sim 10\%$. The gate oxide thickness is ~ 1.3 nm.

The PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress – this improves hole mobility by as much as 50%. The substrate is etched out in the source/drain regions, and local epi-SiGe (~17% Ge) is deposited into the cavities. Crystalline facets form raised source/drains, reducing the series resistance. The tensile stress from the nitride layer is counteracted by the compressive effect.

The strain has induced dislocations at the SiGe/Si interface. The SiGe was likely *in-situ* boron-doped, and also implanted with the polysilicon gate implant. The boron

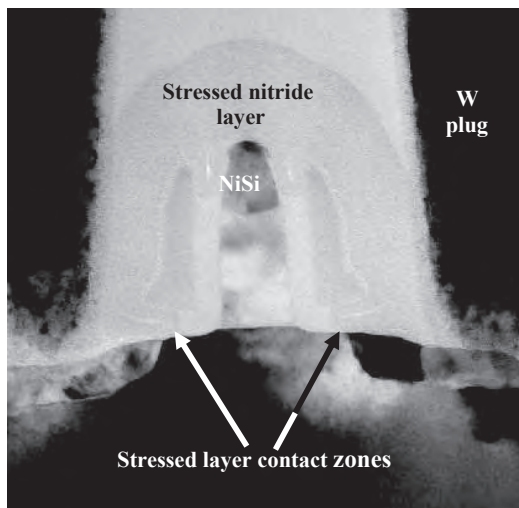


Figure 5. NMOS Transistor in Intel Prescott

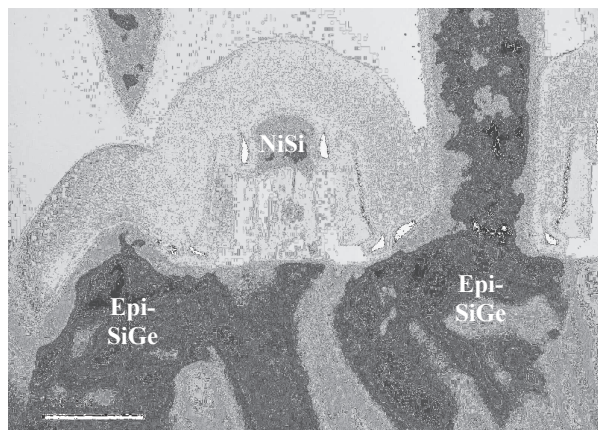


Figure 6. Intel PMOS Transistor

out-diffuses from the SiGe into the silicon to neutralize the potential leakage caused by the dislocations. Nickel silicide was chosen because it consumes less silicon and forms at a lower temperature, making it more compatible with the SiGe.

Figure 7 is a longitudinal section of a PMOS source/drain, clearly showing a stacking fault extending from the epitaxial interface to the silicide layer.

IBM PowerPC PC970FX

The IBM PowerPC is built on a 45 nm-thick SOI layer, with a 45 nm gate length with a 1.5 nm gate oxide thickness. The part has ten metal levels with a hybrid FSG/USG dielectric structure.

IBM had stated that the part would use strain technology, and press reports in the spring of 2004 speculated that the “Strained Silicon Directly on Insulator” (SSDOI) technique, which was announced at IEDM 2003 [3], would be used.

The device appears to use a stressed nitride layer to

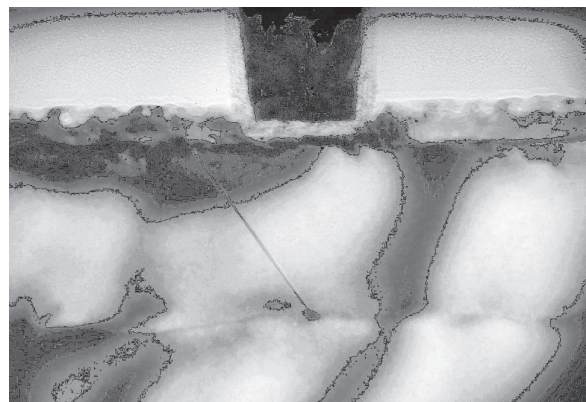


Figure 7. Longitudinal Section of Intel PMOS Source/Drain

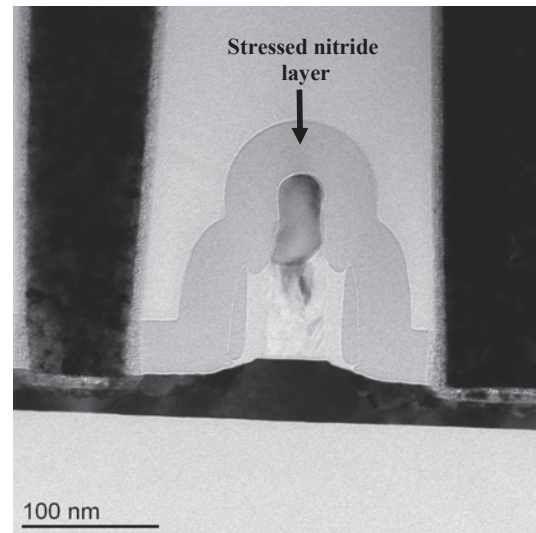


Figure 8. NMOS Transistor in IBM PPC970FX



Figure 9. PMOS Transistor in IBM PPC970FX

enhance the NMOS transistors. Figure 8 is a TEM image of a NMOS transistor, and it can be seen that the sidewall spacers are very slim, and it is only ~20 nm from the gate edge to the cobalt silicide of the source/drain. Comparison with a PMOS transistor (Figure 9) illustrates that the

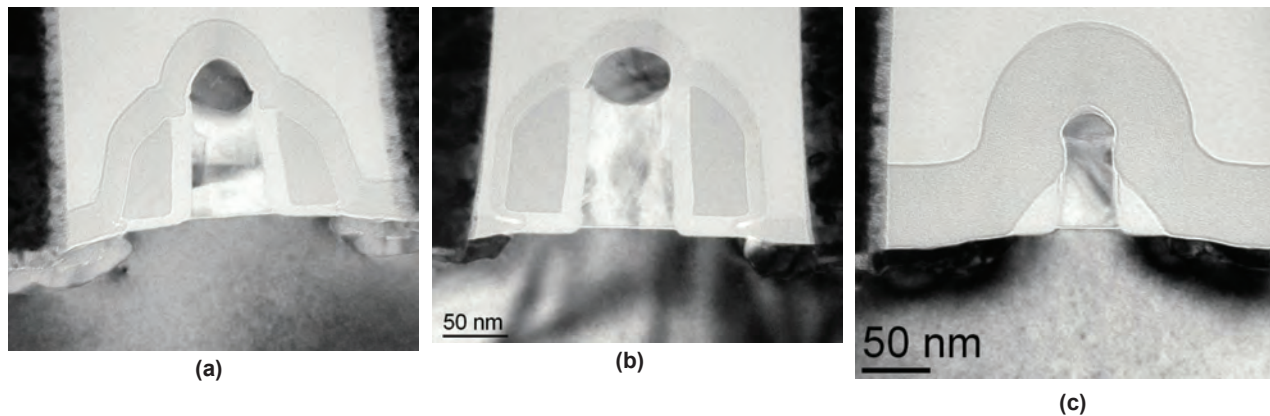


Figure 10. Transistors in (a) Xilinx Spartan-3, (b) Altera Stratix-II, (c) Transmeta Efficen-2

NMOS spacers have indeed been etched back in order to reduce series resistance, and place the stressed nitride layer closer to the gate edge. Electron diffraction studies on the SOI body confirmed $\langle 110 \rangle$ -channel orientation, and there was no indication of a SSDOI substrate. The IEDM SSDOI paper indicated that $\sim 1.5\%$ lattice distortion was required to give useful mobility enhancement.

It is interesting to note that at IEDM 2004, IBM and AMD presented a joint paper [4] on “dual stress liner” technology, which uses stressed nitride layers optimized to apply tensile stress to NMOS transistors, and compressive stress to PMOS devices.

This technique is to be integrated into 90-nm product in the first half of 2005. There was no mention of the use of SSDOI substrates.

UMC (Xilinx Spartan-3)

The Xilinx part was the first 90-nm part from a pure foundry analyzed by Chipworks. The transistor structure was very similar to the 130-nm node device, with the gate shrunk to 55 nm (Figure 10(a)). The gate length was smaller than the UMC-published value of 70 nm, but in other respects the part was manufactured using a more conservative process; FSG was used as the inter-metal dielectric, with seven copper + one aluminium metal levels (although UMC states that low-k dielectrics are available as an option).

There does not appear to be any use of strain to enhance mobility – the nitride layer is thinner than those used in strained devices, and there seems to be no structural changes to move the nitride contact zone closer to the gate edge. However, the gate edge/silicide distance is a respectably small 45–50 nm.

TSMC (Altera Stratix™-II)

The other major foundry to launch a 90nm process in 2004 was TSMC. The product analyzed by Chipworks was the Altera Stratix™-II FPGA. This displayed a gate length of 55 nm, similar to UMC, although closer to the published 59

nm physical gate length of the Nexsys™ process. This is another ten-metal part (9 Cu + 1 Al), using low-k at M1 – M6.

The transistor structure (Figure 10(b)) is not a direct shrink from the 130nm node; it has been modified to change the sidewall spacer structure from the typical L-shaped spacer of previous process generations. Again, the nitride layer appears to be too thin to be used as a stress layer for mobility enhancement. Gate/silicide spacing is ~ 55 nm.

The other major feature of the TSMC 90-nm process is its evolution towards a second-generation low-k dielectric process – the trench and via etching are noticeably cleaner than at the 130-nm node, and the cap layer has changed to a SiCO (rather than SiCN) composition.

Fujitsu (Transmeta Efficen-2)

Transmeta announced shipment of its Efficen-2 in September, fabricated by Fujitsu at their Akiruno Advanced Technology Center. This part also seems to use a strained nitride layer. Figure 10(c) displays what is becoming a characteristically thick nitride sealant layer, which combined with the heavily etched sidewall spacers, leads us to conclude that nitride stress is being used.

Fujitsu had announced the use of nitride strain for the 65-nm node at VLSI 2003 and 2004 [5][6], and they seem to have used the technique in their nominal 90-nm process. Given that the gate length is an impressively small 40 nm, and the gate length for the 65-nm process is quoted at 35 nm, this part could be regarded as an interim step to 65-nm. (They also published a dual-stress process at IEDM ‘04 [7])

In addition, electron diffraction shows that the channels are oriented in the $\langle 100 \rangle$ direction, so Fujitsu is the first manufacturer to combine channel re-orientation and strain to optimise mobility.

The dielectric layers are also advanced, using Novellus Coral low-k (not SiLK!) with SiCO copper-cap and etch-stop layers at M1 – M5. It is an eight-metal part, again with a top aluminium layer.

AMD Athlon 64 Mobile

AMD continued their use of “double spacer” technology at the 90-nm node, with a gate shrink to ~50 nm. The NMOS device (Figure 11) consistently has dislocations under the inner spacer, presumably caused by the drain extension implant. These do not appear in the PMOS transistors (Figure 12), which likely have a different amorphisation implant to fix the drain extension.

There is no evidence of either nitride strain or substrate strain in this part; the nitride is relatively thick, and the double spacer places the contact zone further from the gate. The joint AMD/IBM “dual stress liner” paper [4] showed an Athlon fabricated with the technique, and announced production in 2005.

AMD have also evolved their interconnect structure for the 90-nm node, compared with the 130 nm; the metallisation (9 Cu + 1 Al) is now predominantly dual-damascene, although whilst the dielectric structure is still a hybrid low-k/FSG.

SUMMARY AND DISCUSSION

We have seen eight examples of 90-nm processes in this review, with transistor gate lengths ranging from 40 – 55 nm. Intel, IBM, and Fujitsu have introduced strain for mobility enhancement, and notably Intel has taken the extra steps of embedded SiGe strain for PMOS, and nickel silicide. Texas Instruments and Fujitsu have also used re-orientation of the substrates to improve mobility.

It appears that 90-nm is the node at which strained silicon is coming into production, although not by using epitaxially strained substrates. The strain method of choice has been localised uni-axial strain, as opposed to the bi-axial strain created by strained SiGe layers.

It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown), but the dual-stress approach announced by IBM/AMD and Fujitsu indicates that the layer can also be tuned to provide compressive stress to improve hole mobility for PMOS devices. This technique has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates.

It remains to be seen if the embedded SiGe approach used by Intel will become the dominant method of applying compressive stress for PMOS. Texas Instruments has indicated that it will be using local SiGe strain and nickel silicide in its 65-nm process [8], so Intel will not be alone.

All in all, 2004 was an important year in CMOS process evolution, with significant developments in transistor engineering, and further improvement in low-k dielectric usage. We will see what 2005 brings!

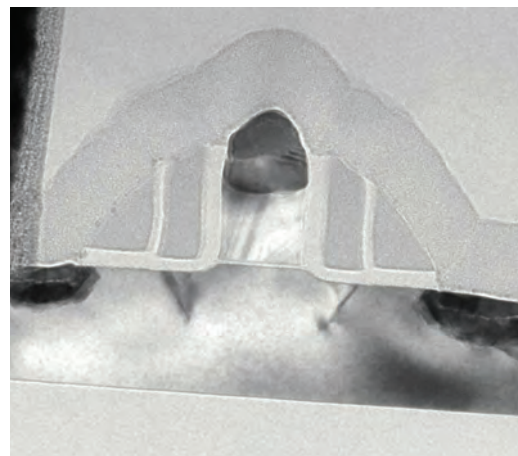


Figure 11. NMOS Transistor in AMD Athlon



Figure 12. PMOS Transistor in AMD Athlon

ACKNOWLEDGEMENTS

I would like to thank Chipworks' laboratory staff and process analysts, and our contractors, who actually did all the hard work of analyzing these complex devices. They did a great job!

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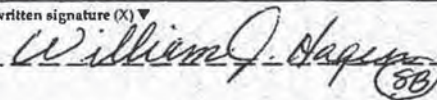
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*17 U.S.C. § 506(e). Any person who knowingly makes a false representation of a material fact in the application for copyright registration provided for by section 409, or in any written statement filed in connection with the application, shall be fined not more than \$2,500.

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