

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING
COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

Case No. IPR2025-00683

U.S. Patent No. 8,907,425

Declaration of Lauren Gluckman regarding *Wolf 2002*

I, Lauren Gluckman, state and declare as follows:

I. Introduction

1. I have prepared this Declaration in connection with a petition for *inter partes* review of U.S. Patent No. 8,907,425, which I understand will be filed concurrently with this Declaration.

2. I am currently a Senior Research Analyst at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, 901 New York Avenue, NW, Washington, DC 20001-4413.

3. I am over eighteen years of age and am competent to make this Declaration. I make this Declaration based on my own personal knowledge and based on my knowledge of library science practices.

4. I earned a Master of Library Science (“MLS”) from Rutgers University in 1993, and a Bachelor of Arts in Political Science from Rutgers University in 1991. I have worked as a librarian for over thirty years. I have been employed at Finnegan since August 2021. My previous position, from 2006-2021, was as the Head of Collection Management and Reference Librarian at the Montague Law Library at Penn State Law of the Pennsylvania State University. From 2002-2006, I was employed as a Reference Librarian at Sutherland Asbill & Brennan. I was employed as a Senior Reference Librarian at the United States

Senate Library from 1996-2002 and from 1993-1995 I was an Assistant Librarian at Debevoise & Plimpton.

5. I am a member of the American Association of Law Libraries.

II. Standard Library Practice for Receiving, Cataloging, and Making Materials, including Serial and Monograph Publications, Publicly Available

6. I have knowledge of and experience with standard library practices regarding the receipt, cataloging, shelving, and making materials, including serial and monograph publications, available to the public. I have knowledge of and experience with the Machine-Readable Cataloging (MARC) system, an industry-wide standard that libraries use to catalog materials. I also have knowledge of and experience with OCLC (previously called Online Computer Library Center, Inc.) and OCLC Control Numbers, which are unique accession numbers assigned by the OCLC system when a bibliographic record is catalogued and made available to the public through WorldCat. OCLC control numbers are often used by the public to search for specific records within WorldCat, the latter being an online global catalog of 586,648,074 bibliographic records from libraries throughout the world as of December 2024 (Source: <https://www.oclc.org/en/worldcat/inside-worldcat.html>).

7. Based on standard library practice, when a library receives a print item, the cataloguer or cataloguer's assistant will examine the item and date-

stamp and/or affix a label to the item with the library name and/or barcode with the date it was received. Next, the library will catalog the item within a few days of receiving it. As a general practice, cataloguing is centralized and performed by a cataloguing department within a library or university setting.

8. Normally, after an item is cataloged, the public may access the item by searching a library online catalog, browsing the physical library shelves, searching a physical card catalog, or by seeking assistance from a Librarian to identify the item. Standard library practice is to make an item available to the public within several days of cataloging it. If an item requires original cataloguing, the item will be made available to the public up to and including one week from the date of receipt.

III. Ownership and Date-Stamp

9. Libraries have different policies on whether to date-stamp received publications. It is becoming increasingly common for libraries to no longer date-stamp the publications they receive. In the past, it was common practice to affix an ownership and date stamp somewhere within the publication, usually on the cover page, verso of the cover page, or a designated page within the publication. The timing of when an ownership/date stamp is entered on the monograph or periodical can vary from one library to another. It could occur when the item is received in acquisitions after shipment to the library, or at the time of cataloging. Therefore, it

is possible for there to be instances when the date of receipt precedes the cataloging date or vice versa.

IV. MARC Records

10. The MARC system was developed during the 1960s to standardize bibliographic catalog records so they could be read by computers and shared among libraries. By the mid-1970s, MARC had become the international standard for cataloging bibliographic materials and is still used today. Many libraries provide public access to their MARC records via their electronic cataloging systems at the library. In a MARC record, each field provides specific information about the cataloged item, including how materials are held and when they were made available to the public.

11. The MARC record system uses specific three-digit numeric codes (“field tags”) (from 001-999) to identify each field in a catalog record. For example, field tag 008 provides the six-digit date an item was catalogued (*Date entered on file*). The first six characters of field tag 008 are always in the “**YYMMDD**” format. Descriptions and definitions of all the character positions of field tag 008 are outlined here: <https://www.loc.gov/marc/bibliographic/bd008a.html>.

12. As is relevant to this Declaration, MARC field tag 020 sets forth the International Standard Book Number (“ISBN”), a unique identification number

assigned to every book or monograph publication. MARC field tag 245 sets forth the Title and statement of responsibility for the work. MARC field tag 264 sets forth information relating to the place of publication, printing, distribution, and copyright date. MARC field tag 505 sets forth notes regarding a work's formatted contents, including the individual titles of separate works, contained within the work.

V. Monographic Series

13. A series is a sequential group of bibliographic items related to one another by the fact that each item often bears, in addition to its own title proper, a collective title applying to the group as a whole with or without numbering or, may contain a separately numbered sequence of volumes or issues within a series. A **Monographic series** is a scholarly and scientific book released in successive volumes, over time, each of which may be structured like a separate book or scholarly monograph each bearing its own unique titles, while the entire series bears its own title proper.

14. There are differences between cataloging finite resources (books/monographs) and continuing resources (series). For a series, the catalog record, such as MARC records, provides information about the series as a whole, including the first or earliest available issue. It also provides information as to particular holdings at a library – the volumes and issues, with dates, and unique

ISBN numbers received by the library and made available to the public. In series cataloging, there are identifying characteristics unique to a series that are slightly different from an individual monograph (book). A series may be classed-together (all items have the same call number; call numbers are distinguished by the volume number) or classed separately (each item in the series has a different call number). A series may or may not be analyzed (separate bibliographic records created for each distinct item in the series). An analyzed monographic series may be classed-together (all items have the same call number with call numbers distinguished by the volume number) or classed separately (each item in the series has a different call number).

VI. Public Availability of *Wolf 2002*

15. This Declaration relates to the date of receipt, accessibility, and public availability of the following reference: S. Wolf, *Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology* (2002) (“*Wolf 2002*”). I understand the excerpts of the *Wolf 2002* reference are being submitted as **Exhibit 1007** in this proceeding.

16. As detailed below, I have reviewed the print excerpts of the *Wolf 2002* reference, which was supplied by Wisconsin Tech Search (WTS), Article Delivery, an outreach service of the General Library System, University of Wisconsin-Madison.

17. **Appendix A** to this Declaration is a true and accurate copy of the title page, verso and table of contents for the print version of Silicon Processing for the VSLA ERA Volume 4: Deep-Submicron Process Technology at University Library of the University of Wisconsin-Madison. **Appendix A** also includes the preface and pages 216-219 which are excerpts of Chapter 5. **Appendix A** also sets forth the International Standard Book Number (ISBN) for Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology containing *Wolf 2002* as 096167217X and was received by the University of Wisconsin-Madison Library on NOV 26 2002, as indicated with a date stamp.

18. **Appendix B** to this Declaration is a true and accurate copy of the University of Wisconsin-Madison public catalog record for its copy of the *Wolf 2002* reference, which was downloaded from <https://search.library.wisc.edu/catalog/999930512302121> on March 5, 2025.

19. The University of Wisconsin-Madison Library public catalog record (**Appendix B**) sets forth the publication, contents, and holdings information for its copy of the *Wolf 2002* reference. **Appendix B** also denotes that the *Wolf 2002* reference bears the unique ISBN, 096167217X, and the print volume of *Wolf 2002* is located at Call Number TK7874 W635 2000 v. 4 in the Steenbock Library located at the University of Wisconsin-Madison.

20. **Appendix B** also contains the MARC record for its holdings of the *Wolf 2002* reference.

21. **Appendix B** confirms the fixed data elements of MARC field tag 008 as 000323t20002000caua 000 0 eng d. As discussed above, the first six characters “000323” are in typical “YYMMDD” format and indicate the series, Silicon Processing for the VLSI Era, was catalogued by University of Wisconsin-Madison on March 23, 2000. The “t” refers to the date of publication of the first volume in the series followed by the year of publication “2000”.

22. MARC record (**Appendix B**) field tag 020 sets forth the unique ISBN number belonging to the *Wolf 2002* reference as 096167217X (v. 4). MARC field tag 245 sets forth the title and statement of responsibility for Silicon Processing for the VLSI Era by Stanley Wolf and Richard N. Tauber. MARC field tag 264 sets forth information relating to the place of publication, printing, distribution, and the initial copyright date for Silicon Processing for the VLSI Era as \$a Sunset Beach, Calif. :\$bLattice Press,\$c[2000-], indicating that the first volume was published by Lattice Press of Subset Beach, California. MARC field tag 505 in **Appendix B** includes the titles of the separate volumes contained within the series Silicon Processing for the VLSI Era held by the University of Wisconsin-Madison as \$a v. 1. Process technology -- v. 4. Deep-submircon [sic] process technology. V. 4.

Deep-submicron [sic] process technology (i.e., volume 4) corresponds to the *Wolf 2002* reference.

23. Based on the information set forth in **Appendices A and B** attached to this Declaration, standard library practices, and my experience as a librarian, Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology (“*Wolf 2002*”) was received by the University of Madison-Wisconsin NOV 26 2002 as set forth in the date stamp within the pages of the volume.

24. Accordingly, based on the information set forth in **Appendices A and B** attached to this Declaration, standard library practices, and my experience as a librarian, the *Wolf 2002* reference would have been made available to the public within a few days of being checked-in and catalogued on NOV 26 2002. The interested public could have been able to access the *Wolf 2002* reference by (i) searching the University of Wisconsin-Madison Library catalog, visiting the Steenbock Library and searching the stacks at TK7874 W635 2000 v. 4; or (ii) by asking a Library staff member and being directed to the print resource located in the Steenbock Library at Call Number TK7874 W635 2000 v. 4 within a few days of November 26, 2002.

VI. Conclusion

25. In signing this Declaration, I understand it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United

States Patent and Trademark Office. I understand I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

26. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on March 6, 2025, in State College, Pennsylvania.



Lauren Gluckman

Appendix A

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 4:
DEEP-SUBMICRON
PROCESS TECHNOLOGY**

STANLEY WOLF Ph.D.

LATTICE PRESS

Sunset Beach, California

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PREFACE

With the dawn of the new millennium, IC technology-nodes have evolved beyond 0.18-micron. New processes also had to be developed to meet the needs of this *Deep-Submicron Era*, including: copper/low-*k* dual-damascene interconnects; high-*k* MOSFET-gate and DRAM dielectrics; 300-mm wafers; chemical-mechanical polishing (CMP); excimer-laser-based DUV-lithography; chemically-amplified (CA) resists; silicon:germanium (Si:Ge); and silicon-on-insulator (SOI).

The semiconductor industry, however, also experienced an economic decline of unprecedented severity at the start of the 2000 decade. It seems clear that to fuel the recovery, chip manufacturers will have to exploit the above innovations. Such processes are a path to achieving the performance goals of future IC technology-nodes that will be needed for manufacturing new and profitable electronic products.

This is the *first available book dedicated exclusively to describing such deep-submicron process technologies* (including those listed above). It is intended to provide semiconductor engineers and researchers with a comprehensive, state-of-the-art reference about these emerging and leading-edge processes. While many other books have been written about the “traditional” IC fabrication processes, none offer what this volume contains. Its sole focus is those techniques needed to *manufacture chips for 0.18- μm (and smaller) generations*. Thus, it belongs on the shelf of every microelectronic professional whose livelihood depends on having a thorough grasp of the latest advances in IC fabrication techniques. There is no faster way to gain this information. As with our other volumes, owners will find themselves referring to this text again and again!

Readers can still consult Vol.1, 2nd Edition for background material on basic IC fabrication modules, as this book (Vol. 4) does not repeat that information. Instead, it presents over 800 pages of new content about the process technologies of the 2000's. It also has over 900 references (with 200 of these being published since 2000), and more than 500 illustrations. It is written in the same lucid, user-friendly style that has been widely praised in the other volumes of *Silicon Processing for the VLSI Era*.

As with the previous volumes, this text was produced using an accelerated book-production schedule. By employing revolutionary publishing techniques made available in the 1990's, Lattice Press can turn a finished manuscript into a published text in less than 3 months (a task that takes most publishers of technical books 15-18 months). This allows our books to be released faster, and to contain the most-up-to-date information at the time of publication.

SILICON PROCESSING FOR THE VLSI ERA is a multi-volume treatise designed to provide a comprehensive and up-to-date treatment of this important and rapidly changing field. The volume in hand is the fourth in the series. Volume 1 (*Process Technology*, 2nd Edition) was published in 2000 and deals with individual processes employed in the fabrication of silicon ULSI circuits (such as silicon wafering, thermal oxidation of silicon, CVD and PVD of amorphous and polycrystalline films, diffusion and ion implantation of dopants in silicon, microlithography, and patterning technology). Volume 2 (*Process Integration*) was released in 1990, and describes how the individual processes of Volume 1 are combined in various ways to produce MOS and bipolar VLSI and ULSI circuits. The task of integrating these various fabrication processes together is referred to as *process integration*. In Volume 3 (*The Submicron MOSFET*, published in 1995) the topics of submicron MOSFET device physics and the relationship between such device physics and submicron MOSFET fabrication are addressed.

A book of this length and diversity would not have been possible without the indirect and direct assistance of many others. From an indirect perspective, virtually all of the information presented here is based on the research efforts of countless numbers of scientists and engineers. Their contributions are recognized to a small degree in citations of their articles given in the references at the end of each chapter. The direct help was also provided by many people, and the resulting text is thus significantly better. The author expresses heartfelt thanks to those who gave their time, energy, and intellect.

Important direct help came from members of my immediate family. My wife, Carrol, read the manuscript for grammatical and stylistic correctness. My son, Ross, designed the cover and improved many of the graphics. My daughter, Jennifer, helped in marketing the book. Thus, it truly represents a family enterprise.

Stanley Wolf

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The final cause of dopant-loss in sub-keV implants is due to the presence of an *oxide on the silicon-surface during implant*. Such an oxide is often deliberately grown to protect the silicon surface from metal contamination during the implant process (see Chap. 10, Vol. 1, 2nd Ed.). While this protective oxide layer can be made quite thin, it nevertheless has a finite thickness. It is clear that as the implant energy is reduced, a larger fraction of the as-implanted dose will be located in the protective oxide. Since the oxide is stripped off at the end of the implant step, the dopant that remains in the oxide cannot contribute to the formation of the junction. Approximately 25% of the B implanted at 0.5-keV is lost by removal of a 15-nm-thick surface-oxide, while more than 40% is lost for 0.2-keV implants. With these results, it is possible to estimate the equivalent-dose needed at lower energies (such as 0.2-keV) to make up for the larger loss as compared to 0.5-keV implants. For example, it has been calculated that to successfully implant a dose of $4 \times 10^{14}/\text{cm}^2$ B-atoms at 0.2-keV into the silicon beyond the protective oxide, the beam-current would have to be as much as 60% greater than the beam-current at 0.5-keV to obtain an equivalent throughput process.³² To circumvent the oxide dose-loss problem, some ultra-low-energy implant processes are being carried out without the use of a protective oxide.

In summary, the dose-loss effects are significant for sub-keV implant processes, and the loss increases as the implant-energy is reduced. For the extreme case of 0.2-keV implants, as much as 40% of the B-dose can be lost due to the combined effects of self-sputtering, out-diffusion, and native-oxide removal for the high doses needed for an SDE-implant.

5.3.4 Effect of the Overlap of the SDE-Region and Gate-Edge on MOSFET Performance

In addition to being able to carefully set the junction-depth X_j and length of the SDE region l_{SDE} , it has also been reported that the amount of overlap of the SDE-region with the gate-edge is also critical for optimum device performance.^{42,57} That is, if the overlap of the SDE-region and the gate-edge is too great, the deep-submicron MOSFET will suffer excessive leakage (due to larger short-channel effects that arise if the channel-length is too small). Excessive leakage means that the off-state current exceeds its maximum design value (e.g., 1 nA/ μm). In addition, the gate-to-(drain/source) overlap-capacitance increases, which negatively impacts device switching speed.

On the other hand, if the SDE-to-gate-edge-overlap is too small, the ON-state saturated-drain-current I_{Dsat} will decrease because the SDE-region and the end of the channel are not electrically well-coupled. Thus, an excessively-high-resist-

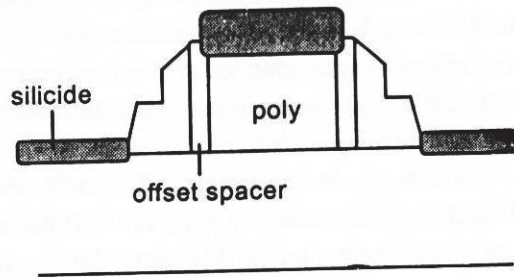


Fig. 5-25 Schematic of a deep-submicron MOSFET with an offset-sidewall spacer.⁵⁷

ance-region separates them (and this increases the parasitic resistance of the source/drain regions, which leads to a decrease in the value of I_{Dsat}).

Controlling the position of the edge of the SDE region with respect to the gate edge can be done in the following way. First, the implant-and-annealing processes for forming the SDE (and contact) region of the drain structure are determined, and the drain structure is formed using these process conditions. However, an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out, Fig. 5-25).⁵⁷ The width of this off-set spacer is varied from zero (no-spacer) to some upper-bound (e.g., 50-nm). Measurements are then made for the MOSFET having different offset-spacer-widths. The offset-spacer-width that yields optimum device characteristics (i.e., the best combination of off-current and I_{Dsat}) is taken to be the value that produces the correct overlap of the SDE-region and the gate edge.

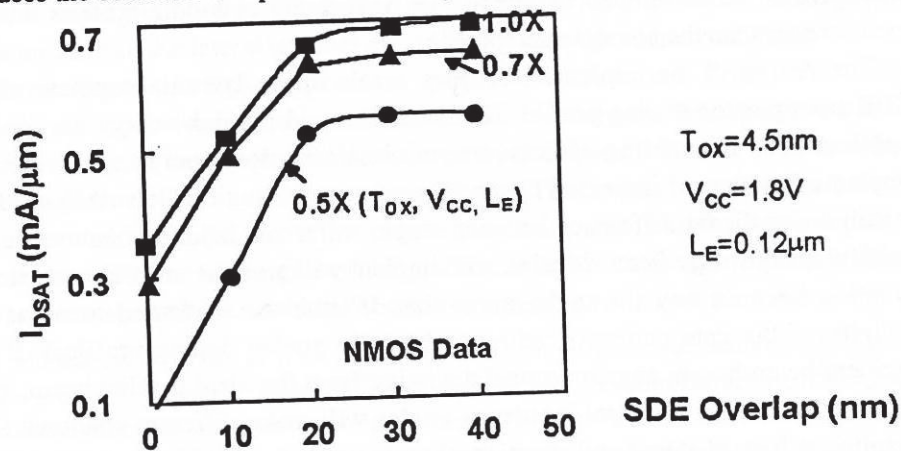


Fig. 5-26 I_{Dsat} versus SDE overlap (NMOS).⁴²

The results of such a study are shown in Fig. 5-26. In this case, the effects of SDE-overlap on 0.25- μm NMOSFETs were analyzed. The arsenic-implanted SDE junction-depth X_j was measured to be 50-nm. Since the lateral diffusion of the SDE junction under the gate-edge is estimated to be 0.6-0.7 times the vertical depth (about 30-nm), minus the width of the offset spacer, the SDE-overlap for each offset spacer width can be determined. Fig. 5-26 shows that if the SDE-overlap is less than 20-nm, the value of I_{Dsat} falls off rapidly. Thus, a minimum overlap of ~20-nm is recommended by this study. Information as to how to form the offset spacer was not given, but a method (such as re-oxidizing the polysilicon gate-structure after it has been etched) is one possible way of doing so.

5.3.5 SDE-Junction Abruptness

The SDE-region must not only have the correct junction-depth, average-doping-concentration, and position under the edge of the gate, but recent studies have shown that there must also be a highly-abrupt lateral-doping-gradient at the interface of the SDE and the MOSFET channel-regions.^{43,44} Not only does such an abrupt-doping-gradient help limit the lateral-encroachment of the extension-depletion-regions into the channel, but more importantly it minimizes R_{sp} . The design rules for lateral-junction-abruptness are that the doping-falloff must be at least one decade in a distance equal to ~3% of the size of the gate-length (for a spreading-resistance less than 5% of R_{sat}). For 100-nm MOSFETs this means that the junction-abruptness must be ~3 nm/decade, which is about the profile slope of as-implanted B at 0.2-keV.⁴⁵ Since the abruptness will have to increase even further as smaller MOSFETs are designed, this implies that new techniques will have to be developed that result in final junction-doping-profiles that are even steeper than the as-implanted profiles.

The design of the implanter can play a role in the lateral-abruptness of the SDE as-implanted doping profile. That is, unlike mid- to high-energy ion-implant applications, channeling-effects are minimal for low-energy, high-current implants (because of increased channeling acceptance angle). Nevertheless, there is still a significant difference between single-wafer and batch-implanters due to implant shadowing effects. Ideally, a 0°-implant will give the most-abrupt lateral-junction because any tilt-angle larger than 0° induces shadowed areas at the vicinity of the gate pattern (leading to laterally-graded doping-profiles). If the incident beam has an angular-spread deviating from the ideal parallel beam, each of the ions having different incidence angles will make different shadows. The result is a loss of dose- and junction-abruptness at the outskirts of the gate. A single-wafer, parallel-beam-implanter minimizes the incident-angle-variations.

Spinning-disk batch-implanters use a stationary-spot ion-beam. The wafers pass through the beam due to the rotation of the disk. Such batch-implanters use a concave-shaped disk to secure wafers in their respective sites during the high-speed motion of the disk. Centrifugal force exerted on the disk surface holds them in place. Since the conical disk has a curved surface and the wafer-surface is flat, this leads to an incident-beam angle-variation across the wafer during the implant process. Depending on the dimensions of the disk, cone-angle, and wafers, this can amount to 1.5° -variation across a wafer.⁴⁶

Recently, the abruptness of the SDE-lateral-doping was measured using both scanning capacitance microscopy (SCM)⁴⁷ and scanning tunneling microscopy (STM).⁴⁸ The latter measurement detected a tail-region of dopant at the end of the doping profile, spreading from the extension-region in the horizontal direction near the gate oxide. The cause of this anomalous diffusion tail was not understood.

5.4 ANTI-PUNCHTHROUGH STRUCTURES IN DEEP-SUBMICRON CMOS

Lateral tailoring of the channel doping profile can provide some additional flexibility to control V_T and punchthrough. Recently, such lateral tailoring of the channel profile has been carried out with the use of *large-angle-tilt implanted punchthrough stopper* (LATIPS), which are also referred to as *pocket-implants* (and are depicted in Fig. 5-27). Such a pocket-implant puts additional dopants in the channel close to the source/drain-junctions for punchthrough control, and leaves much of the channel region with a lighter doping, as needed for a low V_T .^{*} The peak doping values of the pocket-implants must be somewhat larger than the doping-concentration values needed for a punchthrough-control layer that is uniform in the lateral channel direction between the source and drain.

These punchthrough-suppression pocket-implants are done after the source/drain-extension-implant (and before the formation of the spacer used to define the edge of the deeper contact-source/drain-implant). This ensures that the pocket-implant-dopant is self-aligned to the gate. The dopant is placed just below the active channel, adjacent to the source and drain, and is of the same dopant-type as the well. Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements. As noted

* As pointed out in Chap. 1, if an implant with a beam directed normally to the wafer surface is used to introduce dopants to create a punchthrough-control structure, instead of one whose direction is tilted at a large angle to the wafer surface, the resulting punchthrough-control structure is termed a *halo* structure. Such a halo structure is described in Chap. 1, and is depicted in Fig. 1-2b.

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