UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd.,

Petitioner

v.

Advanced Integrated Circuit Process LLC,

Patent Owner

Patent No. 8,907,425 B2
Filing Date: June 20, 2012
Issue Date: December 9, 2014

Title: SEMICONDUCTOR DEVICE

Inter Partes Review No. IPR2025-00683

**DECLARATION OF SCOTT THOMPSON, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,907,425**

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(3) [9B]: "the first stress is a tensile stress" 188

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(3) [11B]: "a second gate insulating film formed on a second active region in the semiconductor substrate" 190

(4) [11C]: "a second gate electrode formed on the second gate insulating film" 192

(5) [11D]: "a second sidewall spacer formed on a side surface of the second gate electrode" 192

(6) [11E]: "a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer" 194

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(3) [1B]: "a first gate insulating film formed on a first active region in a semiconductor substrate" 242

(4) [1C]: "a first gate electrode formed on the first gate insulating film" 243

(5) [1D]: "a first sidewall spacer formed on a side surface of the first gate electrode" 244

(6) [1E]: "a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region" 245

(7) [1F]: "a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress" 248

(8) [1G]: "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode"..... 249

(9) [1H]: "a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer" 251

(10) [1I]: "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween"..... 255

(11) [1J]: "the first stress-relief film is not in direct contact with the side surface of the first gate electrode" 257

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(3) [8B]: "the stress insulating film is a silicon nitride film" 264

(4) [8C]: "the first stress-relief film is a silicon oxide film" 265

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(3) [10B]: "a gate interconnect formed on the isolation region" 269

(4) [10C]: "an interconnect sidewall spacer formed on a side surface of the gate interconnect" 272

(5) [10D]: "a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer" 274

(6) [10E]: "the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film" 276

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I, Dr. Scott E. Thompson, Ph.D., declare as follows:

I. INTRODUCTION

1. My name is Dr. Scott E. Thompson. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited ("TSMC") in connection with a petition for *inter partes* review of U.S. Patent No. 8,907,425 ("the '425 Patent"), which I have been told TSMC is submitting to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-15 of the '425 Patent ("Challenged Claims").

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the bases for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the '425 Patent is unpatentable for at least the reasons I discuss below.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

5. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

6. I received a Ph.D. degree in Electrical Engineering from the University of Florida in 1992. Before that, I received a Master of Science degree in 1988 and a Bachelor of Electrical Engineering with Highest Honors in 1987, both from the University of Florida.

7. I was employed at Intel Corporation ("Intel") from 1992 to 2004. During that time, I worked on evaluating, implementing, and ramping into high-volume production new materials, process architectures, and transistor structures. I was the yield manager and overall program manager for Intel's 90 nanometer (nm) process.

8. Of specific relevance to this case, I played a key role at Intel in the development of a form of strained silicon using silicon germanium ("SiGe") implemented in the source and drain regions of p-type field effect transistors ("pFETs") that I refer to as "SiGe/Strained Silicon" technology in this report. The original SiGe/Strained Silicon technology concept was developed around the year

2000 (about a decade before the earliest claimed priority date for the '425 Patent). SiGe/Strained Silicon is now a nearly universal technology that speeds up transistors and hence all types of integrated circuits. Modern integrated circuits use both nFETs (negative charge flows) and pFETs (positive charge flows). Before the development of SiGe/Strained Silicon, pFETs were about half the speed of nFETs. SiGe/Strained Silicon improved pFET speed to equal that of nFETs, which provides a large benefit to power and performance.

9. Through my work in the industry, I was aware of a report that TSMC had adopted a strained silicon technology in 2003.[1] By 2010, TSMC had added many inventions to the field of SiGe/Strained Silicon. Today, TSMC is the undisputed leader in producing integrated circuits, as even Intel's current CEO has acknowledged.[2]

[1] *See* M. LaPedus, "TSMC to Offer Strained-Silicon at 90- and 65-nm Nodes," EE Times (Apr. 22, 2003), https://www.eetimes.com/tsmc-to-offer-strained-silicon-at-90-and-65-nm-nodes/.

[2] *See* K. Tarasov, "How Intel Plans to Catch Samsung and TSMC and Regain Its Dominance in the Chip Market," CNBC (Nov. 6, 2021) ("'We had some missteps,' said Pat Gelsinger, who took over as Intel's CEO in February [2021]. . . . Gelsinger has an ambitious roadmap to catch and surpass . . . TSMC by 2025."), *available at* https://www.cnbc.com/2021/11/06/how-intel-plans-to-catch-up-to-samsung-and-tsmc-with-44-billion-of-new-global-chip-fabs.html; *see also* Vested Finance, "The Empires that TSMC Built" (Mar. 28, 2022), *available at* https://vestedfinance.com/in/blog/the-empires-that-tsmc-built/.

10. Working at Intel, I announced the SiGe/Strained Silicon technology to the industry in 2002.[3] I managed a team of about 100 engineers that developed and implemented the SiGe/Strained Silicon technology in pFETs that went into high-volume manufacturing in 2003 as part of Intel's 90 nm process (codenamed "Prescott"). My team was responsible for fabricating, ramping into production, and transferring the SiGe/Strained Silicon technology to Intel's design and fabrication sites worldwide. The SiGe/Strained Silicon technology has been used by Intel for its entire microprocessor product line since the 90 nm process, including its latest 7th generation of SiGe/Strained Silicon. Within a few years after 2002, every advanced computer chip manufacturer was using SiGe/Strained Silicon technology.[4]

11. My work on the SiGe/Strained Silicon technology helped me earn an **I**nstitute of **E**lectrical and **E**lectronics **E**ngineers (IEEE) Fellow rank (awarded in 2006), along with numerous industry awards for our Intel development team. In 2008, I and key members of the Intel SiGe/Strained Silicon development team were awarded the SEMI AWARD NORTH AMERICA for "Process Integration of Strain-

[3] *See* D. Lammers, "Industry Reacts to Intel's Strained Silicon Move," EE Times (Aug. 16, 2002), *available at* https://www.eetimes.com/industry-reacts-to-intels-strained-silicon-move/#.

[4] *See* note 3 above.

enhanced Mobility Techniques for CMOS Transistors."[5] This award is the highest honor achievable through SEMI, a 2,000-member trade organization.

12. In 2007, my Intel colleague Mark Bohr described my role and how Intel came to invent the SiGe/Strained Silicon technology.[6] At Intel, I worked on several generations of Intel's transistors, each of which implemented SiGe/Strained Silicon technology after 2002.

13. I have given invited talks and organized and taught international courses on SiGe/Strained Silicon technology. For example, I was asked to give a lecture on strained silicon at the 2006 International Electron Devices Meeting.

14. I have also developed and taught graduate level courses on SiGe/Strained Silicon technology at the University of Florida, including a course entitled "EEE5400: Future of Nano/Micro Electronics."

15. As a professor at the University of Florida, I have been awarded over $4 million in research funding largely directed towards understanding the scalability of SiGe/Strained Silicon transistors. I have received research funding from the

[5] *See* SEMI AWARD NORTH AMERICA RECIPIENTS, https://www.semi.org/en/semi-organization/awards/north-american-semi-award/recipients.

[6] *See* https://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.488.9606&rep=rep1&type=pdf. As explained by Mark, "By early 2002 [Scott Thompson] became the 90 nm program manager and was responsible for getting strained silicon transistors along with copper plus low-k interconnects to meet performance, yield and reliability requirements in time for the first product shipments in 2003."

National Science Foundation, Semiconductor Research Corporation, and other agencies. I am currently conducting industry-funded research to investigate strained transistors.

16. As a result of my industry work, I am familiar with various areas of advanced CMOS technology. I have worked extensively on the use of shallow trench isolation ("STI") in manufacturing processors, novel low-resistance source and drain regions, silicides (titanium, cobalt, and nickel silicide), and low-resistance tungsten plugs. Throughout 1991-2004, I was part of the Intel development team that introduced titanium, cobalt, and nickel silicide into the production of high-performance microprocessors.[7] My work experience has also extended to layout design rules, oxide and nitride spacer formation, source/drain formation and SiGe epitaxy, gate patterning, gate oxides, gate electrodes, contacts, silicide, interconnects, process integration (lithography, etch, diffusion, thin film deposition, and chemical mechanical polishing), and yield and reliability.

17. As one of the original inventors of SiGe/Strained Silicon technology, I am extremely familiar with MISFETs (**M**etal-**I**nsulator-**S**emiconductor **F**ield **E**ffect **T**ransistors), including related technology and manufacturing techniques. I have

[7] *See, e.g.*, S. Thompson et al., "A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm^2 SRAM Cell," Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002); A. Brand et al., "Intel's 0.25 Micron, 2.0Volts Logic Process Technology," Intel Technology Journal (Q3 1998).

authored numerous papers, given many invited talks, and organized and taught international courses on MISFETs, including, for example, courses for the IEEE.

18. Every year since 2004 (except for one year when I took a sabbatical and the course was taught by video), I have taught a course I developed at the University of Florida on future MISFET technologies and designs. I have also taught other undergraduate- and graduate-level courses on MISFETs, transistor layout, and fabrication at the University of Florida, including courses covering the scaling and scaling limits of MISFETs.

19. I have experience analyzing transmission electron microscope ("TEM") images at Intel and other places in industry, including as a consultant of Chipworks, an independent reverse engineering firm that merged with TechInsights, another independent reverse engineering firm. I helped Chipworks staff understand features of transistors in electron micrographs (pictures obtained using electrons to image transistor structures).

20. I also co-founded a low-power transistor technology company called SuVolta in 2009 that developed transistors that could operate at ultra-low power for internet-of-things applications. SuVolta's intellectual property was sold to Fujitsu and included patents on FETs that could operate at ultra-low power.

21. As the co-founder and Chief Technology Officer of SuVolta, and as an inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

22. I am a named inventor on over 100 granted United States patents and have authored over 60 peer-reviewed academic journal publications. I have co-authored a book on strained silicon transistors titled *Strain Effects in Semiconductors: Theory and Device Applications* (2009). I have patents and publications on SiGe/Strained Silicon technology, nanoscale transistors, and SRAM cell designs that are relevant technologies in this case. A few examples are:

- My work on the SiGe/Strained Silicon technology is described in frequently cited IEEE peer-reviewed papers, including
    - S. Thompson et al., "Source/Drain Extension Scaling for 0.1μm and Below Channel Length MOSFETS," Digest of Technical Papers for the 1998 Symposium on VLSI Technology, pp. 132-33 (1998);
    - S. Thompson et al., "A 90 nm Logic Technology Featuring 50 nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 μm2 SRAM Cell," Technical Digest of the 2002 International Electron Devices Meeting (IEDM), pp. 61-64 (2002) (cited over 450 times in peer-reviewed literature);
    - S.E. Thompson et al., "A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, vol. 25, No. 4, pp. 191-93 (Apr. 2004) (cited nearly 700 times in peer-reviewed literature); and

  - S. Thompson et al., "In Search of 'Forever,' Continued Transistor Scaling One New Material at a Time," IEEE Transactions on Semiconductor Manufacturing, vol. 18, No. 1, pp. 26-36 (2005) (cited over 250 times in peer-reviewed literature).

- The history of the SiGe/Strained Silicon invention is explained in the frequently cited IEEE peer-reviewed paper S.E. Thompson et al., "Uniaxial-Process-Induced Strained-Si: Extending the CMOS Roadmap," IEEE Transactions on Electron Devices, vol. 53, no. 5, pp. 1010-20 (May 2006) (cited nearly 750 times in peer-reviewed literature).

- My work on shallow trench isolation is described in a 1998 paper published in the Intel Technology Journal: A. Brand et al., "Intel's 0.25 Micron, 2.0 Volts Logic Process Technology," Intel Technology Journal, Q3 (1998).

23. My work at Intel noted above included developing the strained-transistor technology in Intel's 90 nm process (codenamed "Prescott"), which is described in my own publications and in publications by others, including D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005).

24. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which I understand is being included as Ex-1004.

25. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae.

26. I am being compensated for services provided in this matter at my standard consulting rate, plus travel expenses. My compensation is in no way conditioned on the outcome of this proceeding or any issue therein, nor is it contingent upon the results of my study or the substance of my testimony. Similarly, my compensation is in no way dependent upon and in no way affects the substance of my statements in this declaration.

27. I have no financial interest in TSMC or any of its subsidiaries. I also do not have any financial interest in the Patent Owner. I do not have any financial interest in the '425 Patent and have not had any contact with any of the named inventors of the '425 Patent (Satoru Itou, Toshie Kutsunai) about the '425 Patent or any issues in this proceeding

III. MATERIALS REVIEWED

28. In forming my opinions regarding the '425 Patent, I reviewed the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

29. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '425 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

30. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by a preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior art patent or publication.

31. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

32. I have been told that under 35 U.S.C. §103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by a preponderance of the evidence (i.e., it is more likely than not) that it would have

been obvious to a person of ordinary skill in the art at the earliest priority date of the patent.

33. When considering the issues of obviousness, I have been told that I am to do the following:

a. Determine the scope and content of the prior art;

b. Ascertain the differences between the prior art and the claims at issue;

c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of non-obviousness (if available).

34. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have assumed is just before the earliest claimed priority date of the ’425 Patent (January 7, 2010).

35. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the ’425 Patent).

36. I have been told that a prior art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

37. In determining whether the teachings contained in one prior art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

38. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

39. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

40. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand—not scientific literature—may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

41. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told that this "teaching, suggestion, or motivation" test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

42. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

43. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. LEVEL OF ORDINARY SKILL IN THE ART

44. I have been informed that a person of ordinary skill in the art ("POSITA") is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

45. I have been instructed to assume a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

46. In my opinion, a POSITA in reference to the ’425 Patent would have possessed at least a master’s degree in electrical engineering, physics, materials science, or a related field and at least three years of work experience in integrated circuit device design and manufacturing, including strained-channel MISFETs and fabrication of such devices. Additional education could substitute for professional experience, and significant work experience or training could substitute for formal education.

47. I have not analyzed the priority date of the ’425 Patent, but I note that the earliest claim of priority listed on the face of the ’425 Patent is January 7, 2010, the filing date of Japanese Patent Application No. 2010-002225. Because all the prior art discussed in this declaration predates January 7, 2010, I have been asked for simplicity to treat **January 7, 2010**, as the priority date for the ’425 Patent. I have also treated this date as the date from which to assess the knowledge available to a POSITA.

VI. TECHNOLOGICAL BACKGROUND

48. I understand that **January 7, 2010**, may be the earliest claimed priority date for the ’425 Patent. In my opinion, all the elements in the ’425 Patent were well known before this date—in fact, already commonplace in high-volume commercial production. For example, as explained below, SiGe/Strained Silicon technology was in widespread use well before 2010. In fact, each of the four preceding generations

of high-volume commercial devices (i.e., 90nm, 65nm, 45nm, and 32nm devices) used SiGe/Strained Silicon technology. So has every generation of high-volume commercial transistors ever since.

A. MISFETs

49. A "MISFET" is a "**M**etal-**I**nsulator-**S**emiconductor **F**ield-**E**ffect **T**ransistor."[8] MISFETs have a ***source*** and a ***drain*** for current input and output. Sze, 433-34, Figs. 3, 6; Plummer, 76-82. Electrodes on the source/drain regions allow current into and out of the MISFET. Sze, 433-34, Figs. 3, 6; Plummer, 82-90. MISFETs like the ones at issue here also have a ***gate*** above a ***channel*** region between the source and drain. Sze, 433-34, Fig. 3; Plummer, 71-76. The ***gate*** includes a ***gate electrode*** separated from the channel region by a ***gate dielectric*** (also called a gate "oxide" or gate "insulator"). Sze, 433-34, Fig. 3; Plummer, 71-76. Applying appropriate voltage to the gate electrode controls a conductive channel in the channel region to connect or disconnect the source and drain regions. Sze, 433-34, 438, Figs. 3, 6.

[8] The term "MOSFET" is also used to describe such devices. MOSFET stands for "Metal-***Oxide***-Semiconductor Field-Effect Transistor," which refers specifically to oxide-based insulators. A POSITA would have understood MISFET and MOSFET are interchangeable terms.

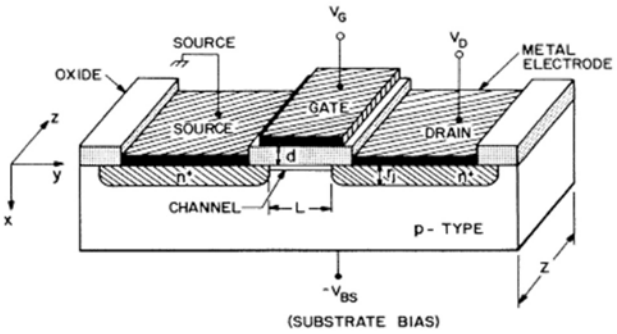
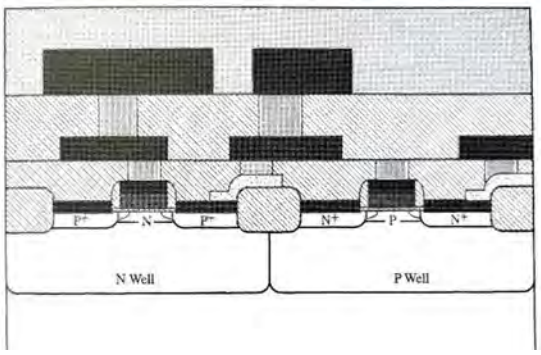


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

Sze's Fig. 3



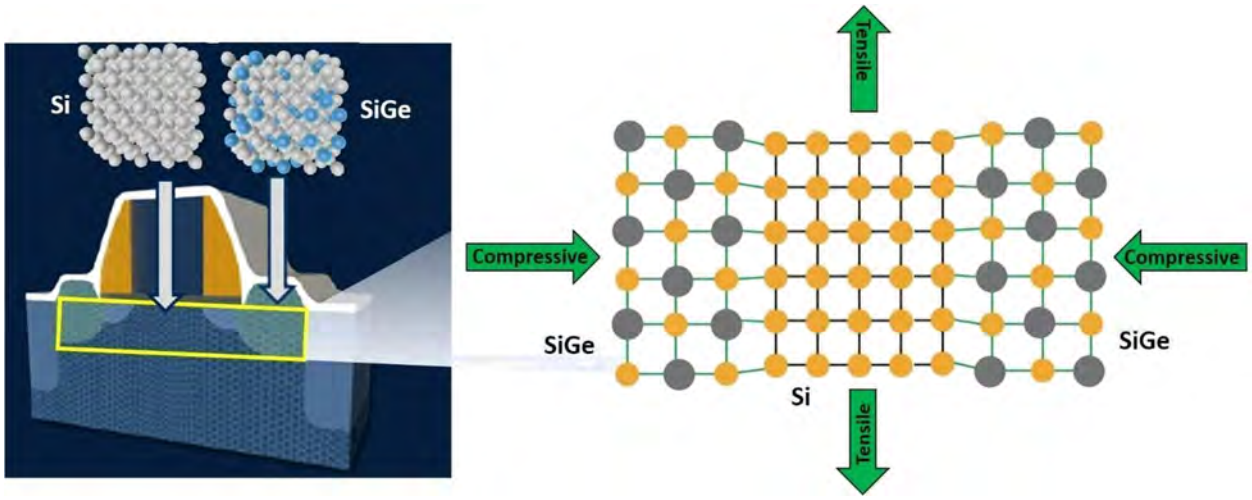
Plummer's Fig. 1-11

50. Source/drain regions are generally ***doped*** with either a ***p-type*** or ***n-type*** impurity, and the channel region is generally doped with the opposite impurity type. *See* Sze, 433-34; Plummer, 76-82. A MISFET with ***p***-type source/drain regions is called ***PMOS*** (or "nMIS" or "nFET"), and one with ***n***-type source/drain regions is called ***NMOS*** (or "pMIS" or "pFET"). Plummer, 12-13, 50-51, Figs. 1-11, 2-2. An integrated circuit with both PMOS and NMOS devices is called ***CMOS*** ("Complementary MOS"), as in Plummer Fig. 1-11 above. Plummer, 12-13, 50-51, Figs. 1-11, 2-2.

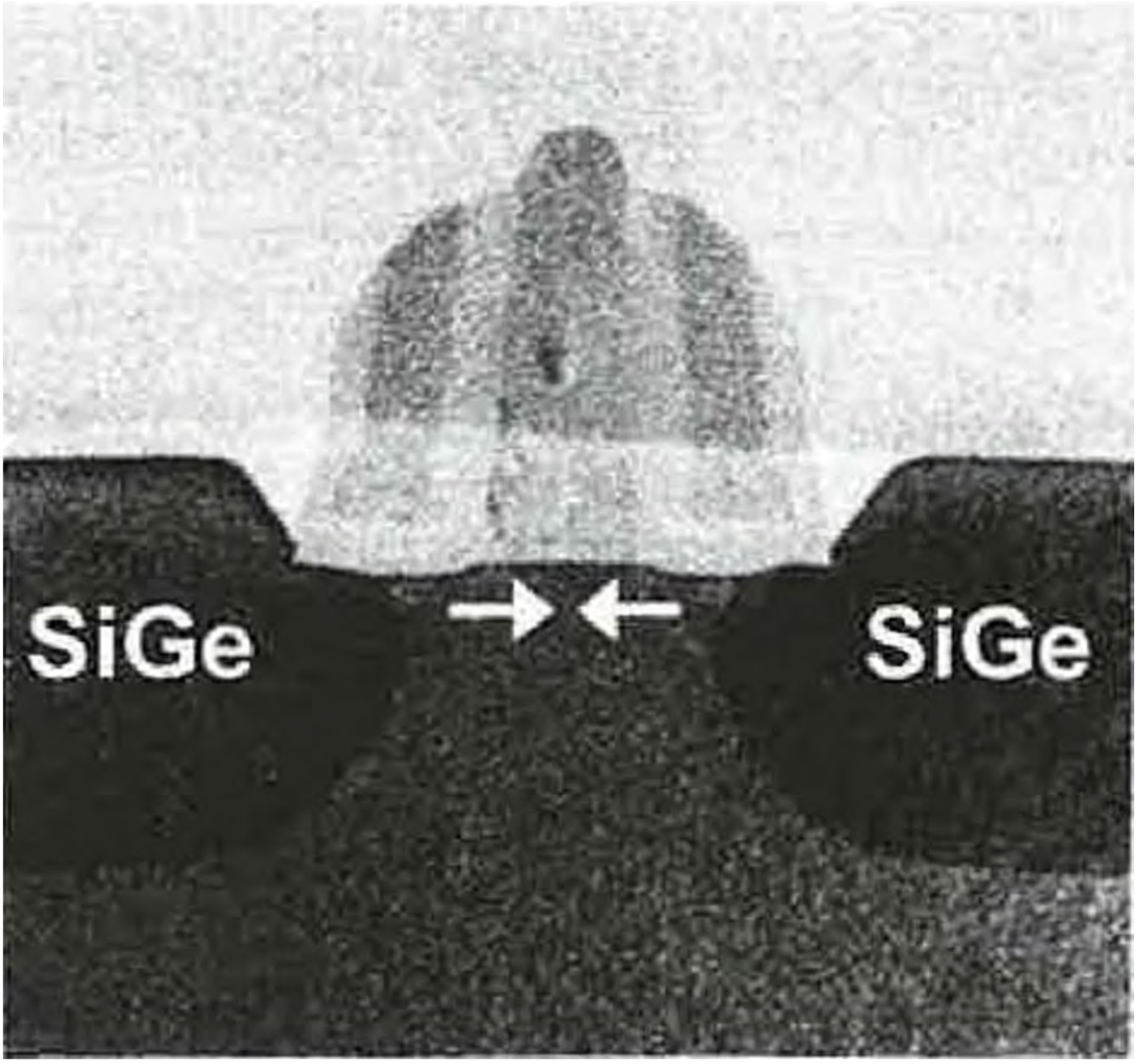
B. Strained-Silicon Technology and Raised Epitaxial Source/Drain Growth

51. PMOS was once much slower than NMOS. Strained-silicon technology changed that. Because germanium atoms are larger than silicon atoms, epitaxial silicon-germanium ("SiGe," i.e., $Si_{1-x}Ge_x$) source/drain regions ***compressively*** strain the Si channel region along the direction of current flow (left to right in the illustrations below). In PMOS, this compressive strain improves carrier (hole)

mobility and boosts operating speed. *See* Thompson2004, 1790-96; Sun, 2. By 2005, compressively strained SiGe source/drain regions increased PMOS "hole mobility by as much as 50%" (James, 2), and had doubled PMOS operating speeds.



52. To further improve PMOS performance, it was common to grow strained SiGe source/drain regions extending above the substrate surface. *See* Cheng, Figs. 4e-4j; Wang ¶¶[0030]-[0032], FIG. 9; Bohr683 ¶¶[0038]-[0039], FIGS. 4-7; Kavalieros, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13; Wang ¶[0031], FIG. 9. The '425 Patent acknowledges this fact by referencing Tahir Ghani's 2003 paper describing the raised SiGe source/drain layers in Intel's 90nm devices. *See* '425 Patent, 1:31-43. The raised SiGe source/drain regions are readily apparent from Ghani's Fig. 1, reproduced below. *See also* Ghani, 978, Figs. 1-4. I note that I was listed as a co-author of that paper. *See* Ghani, 978.



Ghani's Fig. 1

53. Such raised SiGe regions improve PMOS performance by imparting compressive strain to the channel. *See* James, 2. James shows one example of this with the Intel Prescott device shown below, where "[c]rystalline facets form raised source/drains, reducing the series resistance" of the SiGe, and the "tensile stress from the nitride layer is counteracted by the compressive effect" of the SiGe. James, 2.

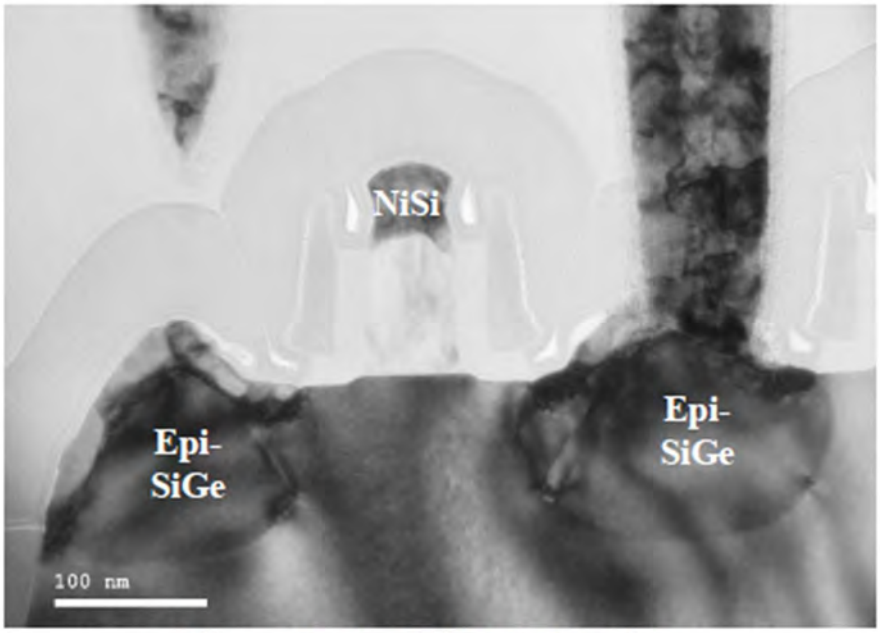


Figure 6. Intel PMOS Transistor

James's Fig. 6

54. The same strain engineering principles apply to NMOS, except that improving NMOS carrier (electron) mobility in NMOS requires ***tensile*** strain instead of ***compressive*** strain along the current-flow direction. *See* Murthy151 ¶[0005], ¶[0048], ¶[0072]; Wu ¶[0037]; James, 2; Bohr683 ¶[0045]; Chen729 ¶¶[0021]-[0022]. Creating tensile strain with epitaxial source/drain regions requires using a smaller atom, like carbon, to grow a material like silicon carbide (SiC) instead of SiGe, which was also known. *See* Murthy151 ¶[0005], ¶[0048], ¶[0072]; Wu ¶[0037]; James, 2; Bohr683 ¶[0045]; Chen729 ¶¶[0021]-[0022].

55. As an alternative or supplement to source/drain epitaxy, by 2010, the semiconductor industry was also already depositing compressive or tensile stress-inducing films over PMOS and NMOS devices to induce a desired strain. *See* James, 2, 4; Morin, 355-56, 367; Alvarez ¶[0022], ¶[0025], ¶[0033]; Hsu823 ¶[0003]; Jung,

Abstract, ¶[0090] ("In addition to being deposited as part of a structure to control electron mobility, . . . a stress-tuned silicon nitride film can be deposited for other purposes . . . , for example . . . , to provide an etch stop layer . . . ."). Most commonly, a contact etch stop layer ("CESL") made of silicon nitride was used. If prepared under certain conditions, a silicon nitride CESL may be "used . . . for applying stress to [a] channel region" to improve carrier mobility. Hsu823 ¶[0003]; *see also* Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Jung ¶[0090] ("In addition to being deposited as part of a structure to control electron mobility, . . . a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure."); Morin, 355-56. Depending on how such a silicon nitride layer is prepared, it may provide tensile stress, compressive stress, or no stress at all. *See, e.g.*, Jung ¶[0017], ¶¶[0099-[0100], ¶¶[0131]-[0132], Tbls. IV-V, VII, Fig. 15.

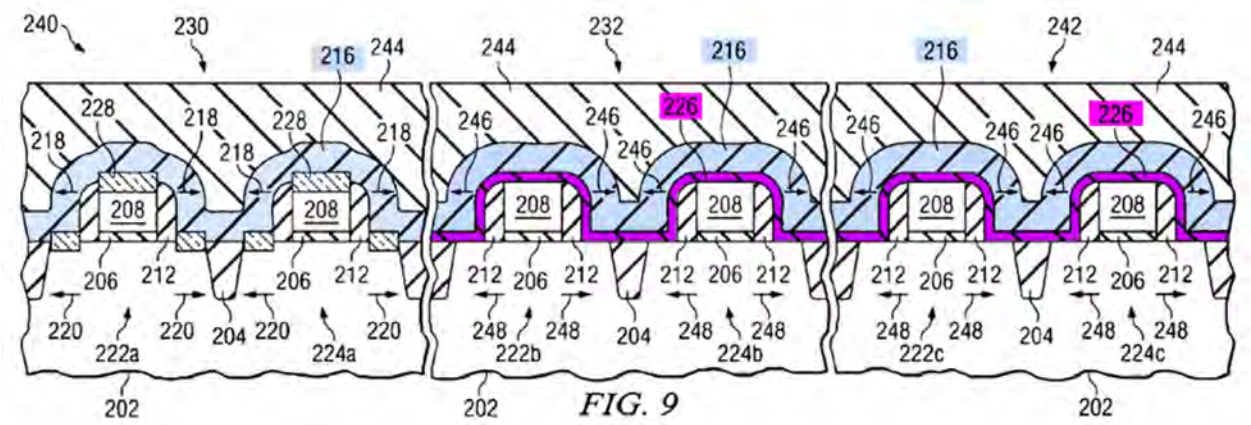
56. Strained silicon technology has a long history and was well known before January 2010, which the '425 Patent acknowledges. *See* Sun, 1-2; '425 Patent, 1:23-2:62, FIGS. 8A-10C. At least four generations of high-volume commercial devices by Intel alone already used it by 2009. *See* Thompson2004,

1790-96 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry, 247-50 (describing Intel's 45nm devices); Natarajan, 1 (describing Intel's 32nm devices).

C. Stress Buffering Layers

57. When a tensile CESL is placed near the channel of a PMOS device, it generally applies a tensile stress to the channel region. Morin, 355-56, 367; Doris ¶[0005], ¶[0013]; Hsu823 ¶[0037]. In the case of a PMOS device with epitaxial SiGe source/drain regions, that tensile stress offsets at least some of the compressive stress the SiGe applies to the channel region, thereby reducing improvements in the device's performance. Morin, 355-56, 367; Kavalieros ¶[0002], ¶[0026]; Doris ¶[0005]. In a PMOS device without SiGe source/drain regions, the tensile stress degrades device performance. Morin, 355-56, 367. Those ordinarily skilled in the art would have known, however, how to mitigate such tensile stress by placing a stress-relief layer as a buffer between the compressed SiGe and the tensile CESL layer. Murthy556, 9:27-29, FIGS. 2, 9, 13-15; Doris ¶[0042], Figs. 1-2, 14-15; Alvarez, Abstract, ¶[0043], FIG. 9; Lee ¶[0029], ¶¶[0046]-[0067] (explaining that pFET performance degradation "is reduced/eliminated due to the inclusion of the stress relief layer 64 under the nitride layer 70 that reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810 ¶¶[0022]-[0031], Figs. 1B-1F (describing similar); Baik ¶[0037] (explaining that "the tensile stresses of the [stressor layer]

ha[ve] relatively little or no adverse impact [on] the adjacent PMOS device" because the intermediate layer "reduce[s] the amount of stresses induced in the PMOS device by acting as a physical barrier"). In other words, it was known that using an appropriate intermediate layer "buffers the large stress inherent silicon nitride layer." Murthy556, 9:27-29; Alvarez ¶[0049], ¶[0066], ¶[0068], ¶[0077], FIGS. 9-11. Alvarez shows one such example, in FIG. 9 below, having a stress-inducing layer 216 that is buffered by stress-control layer 226 to mitigate the adverse tensile effects on PMOS devices 224b and 224c in circuit regions 232 and 242.

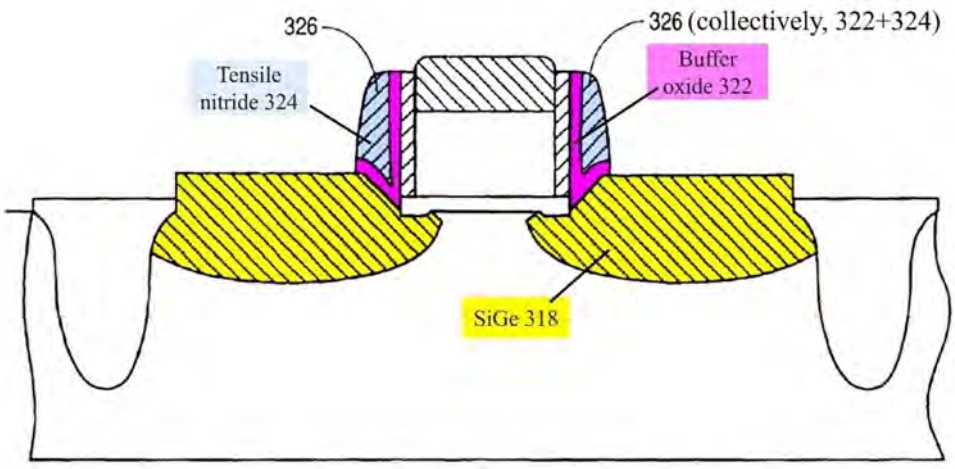


Alvarez's FIG. 9
(annotated, showing stress buffer layer 226 and stress-inducing layer 216)

58. The prior art also teaches that a buffer layer like the one Alvarez discloses (e.g., dual-purpose stress-controlling and masking layer) may be applied over both the NMOS and PMOS transistor regions, as Alvarez's FIG. 9 shows above. Alvarez ¶[0043], ¶[0045], ¶[0047], ¶[0049], ¶¶[0053]-[0055], ¶[0078], FIGS. 7-9. Alvarez explains that this can be done because "different types of transistors . . .

hav[e] different operating parameters and requirements" and/or "due to the performance requirements of transistors in the particular regions." Alvarez ¶[0027], ¶[0032], FIGS. 7-9. By leaving the stress-controlling layer over the NMOS and PMOS, the number of fabrication steps may be reduced, thus lowering the cost of manufacturing and is "advantageous in many types of circuits." Alvarez ¶[0075]; *see also* Alvarez ¶[0074], ¶[0078].

59. As shown below, such a buffer layer forms in the space between the SiGe and the gate when raised SiGe source/drain layers are present. Murthy556, 9:11-15, 9:30-35, FIGS. 7-9; *see also* Miyashita ¶¶[0052]-[0053], FIGS. 1U-1W; Koutny ¶[0088], ¶[0108] (silicon dioxide liner 485A between tensile stress-inducing layer 504A and source/drain "reduces the cumulative stress" caused by tensile layer); Doris ¶[0034], ¶[0042]; Cheng810 ¶[0030]; Lee ¶[0067].



Murthy556's FIG. 9 (annotated)

60. In these examples, an intermediate SiO_2 layer between the PMOS channel region and a tensile CESL layer "prevents the tension from materially adversely influencing the charge carrier mobility in the pFET," and the pFET "experiences a performance improvement" through "enhanc[ed] hole mobility in the pFET channel." Doris ¶¶[0034]-[0035], Figs. 2, 14, 15. Using a low-stress dielectric film in this way "defines a neutral buffer layer" between a compressively stressed region near the PMOS channel and a tensile CESL layer above it, which allows the compressively strained region "to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer." Doris ¶[0042]; *see also* Lee ¶[0029], ¶¶[0046]-[0067] (explaining that an intermediate stress relief layer "with neutral stress or opposite stress relative to the [CESL]" reduces or eliminates any pFET performance degradation because it "reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810 ¶¶[0022]-[0031], Figs. 1B-1F (describing similar).

VII. THE '425 PATENT

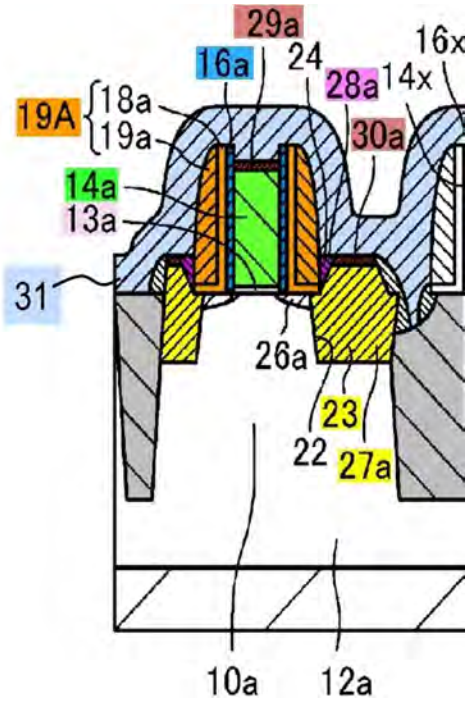
A. Overview

61. The '425 Patent is directed to "semiconductor devices and methods for fabricating the semiconductor devices," including "semiconductor devices which include a metal-insulator-semiconductor field-effect-transistor (MISFET) having a source/drain region including a silicon compound layer." '425 Patent, 1:15-22.

62. The ’425 Patent acknowledges it was previously known to use a “distortion technique of enhancing the drive capability of a MISFET . . . by applying a stress to the channel region . . . to improve the performance of a semiconductor integrated circuit device.” ’425 Patent, 1:23-27. It was also known in the prior art that, for PMOS devices, “if a ***compressive*** stress is applied to the channel region in the gate length direction, the mobility of carriers is increased, and the drive capability . . . is enhanced.” ’425 Patent, 1:27-43 (emphasis added) (citing examples). Similarly, the ’425 Patent acknowledges the well-known prior art fact that, for NMOS devices, “the drive capability . . . is enhanced” “if a ***tensile*** stress is applied to the channel region of the active region in the gate length direction.” ’425 Patent, 3:1-4 (emphasis added). The corollary is also relevant that, because PMOS devices require ***compressive*** stress to enhance drive capability, “the drive capability . . . is reduced” in PMOS devices if tensile stress is applied to the channel. ’425 Patent, 3:1-4. The ’425 Patent thus purports to mitigate reduction in the compressive stress in PMOS device regions when a tensile stress-inducing film is applied to enhance NMOS channel conductivity in NMOS devices. *See* ’425 Patent, 3:13-17.

63. FIG. 6B, excerpted and annotated below, illustrates an exemplary PMOS device of the ’425 Patent. *See* ’425 Patent, 13:66-15:5, FIG. 6B.

10a: active region
13a: gate insulating film
14a: gate electrode



16a: offset spacer
19A: sidewall
22: trench
23: silicon compound layer
24: space
27a: p-type source/drain region
28a: first stress-relief film
29a: first silicide layer
30a: second silicide layer
31: stress insulating film

'425 Patent's FIG. 6B (excerpted, annotated)

64. Annotated FIG. 6B above shows a PMOS transistor structure with known features, including a "first stress-relief film 28a . . . formed in [a] space 24 located between the silicon compound layer 23 [e.g., SiGe] and the first sidewall 19A." '425 Patent, 13:6-8. In this example, "stress insulating film 31 can be separated from the channel region in the first active region 10a by the thicknesses of the protruding portion of the silicon compound layer 23 and the first stress-relief film 28a." '425 Patent, 16:2-6. According to the '425 Patent, this makes it "possible to reduce the tensile stress applied from the stress insulating film 31 to the channel region in first active region 10a in the gate length direction" and "to prevent a reduction in drive capability." '425 Patent, 16:6-11.

B. Prosecution File History

65. The File History of the ’425 Patent includes two office actions and two amendments. *See generally* File History.

66. In the first Office Action, the Examiner asserted that the original claims were obvious. File History, 1-11. According to the Examiner, the prior art disclosed “a first stress-relief film . . . formed in a space between the silicon compound layer and the first sidewall.” File History, 5.

67. In response, the Applicant amended independent claim 1 to additionally recite that “the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween.” File History, 18. The Applicant distinguished the alleged stress-relief film in the prior art as being “formed in a space between the gate electrode 202 and the epitaxial source/drain region 218, and in **direct** contact with a side surface of the gate electrode 202.” File History, 23-24. Thus, according to the Applicant, the resulting combination of prior art still would fail “to disclose or suggest a device in which ***the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween***.” File History, 23-24.

68. The Examiner then issued a Final Office Action, rejecting Applicant’s arguments and maintaining that the prior art rendered the amended claims obvious. *See* File History, 27-39. According to the Examiner, the alleged stress-relief film in

the prior art was "formed on the side surface of the first gate electrode(202) with the first sidewall spacer(265) interposed therebetween." File History, 30. The Examiner rejected Applicant's position because "[t]he claim language does not specify whether [the stress-relief film] can or cannot be in direct contact with a side surface of the gate electrode(202)." File History, 36. The Examiner also provided the annotated figure below, using the red annotation to show that upper portion 265 (first sidewall spacer) in the prior art lies between the first gate electrode 202 and first stress-relief film 255. *See* File History, 36-37 ("[T]he right triangle sides of the first sidewall spacer(265) is [sic] bordering with the first gate electrode(255 [sic:202]) and the first stress-relief film(255).").

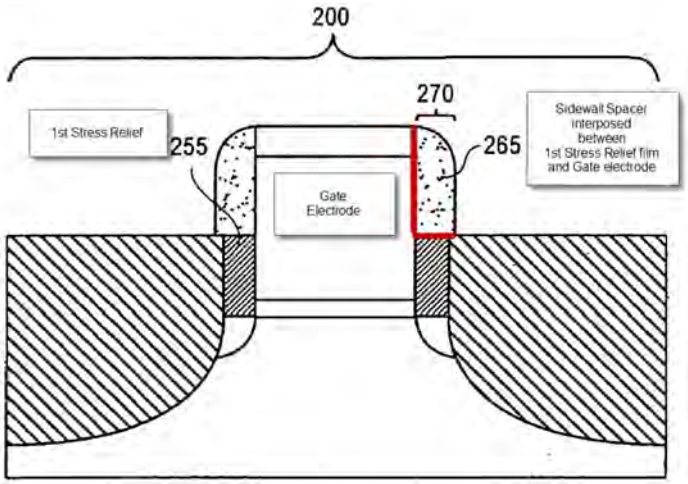


FIG. 2K

File History, 37 (annotated)[9]

[9] I have been informed that this colored figure was obtained by downloading the document from the U.S. Patent Office's Patent Center website in .docx format and appears as it did in the .docx document.

69. In response, the Applicant further amended claim 1 to recite: "the first stress-relief film is not in direct contact with the side surface of the first gate electrode." File History, 42-43. The Applicant explained that this amendment "is intended to address the Examiner's interpretation of the prior art." File History, 48. The Applicant also maintained that the prior art "would still fail to disclose or suggest a device in which ***the first stress-relief film is not in direct contact with the side surface of the first gate electrode***." File History, 48-49.

70. The Examiner then allowed the claims. File History, 51-58. In a statement of reasons for allowability, the Examiner maintained that the prior art taught "a first stress-relief film . . . formed in a space between the silicon compound layer and the first sidewall spacer," and that "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween." File History, 56-57. The Examiner found, however, that the prior art did not disclose or render obvious that "the first stress-relief film is not **in** direct contact with the side surface of the first gate [electrode]." File History, 57.

C. Claim Construction

71. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art ("POSITA") in the context of the patent document. In my analysis of the Challenged Claims, I have therefore applied

the meanings of the claim terms as understood by a POSITA in the context of the '425 Patent's disclosures and asserted claims.

72. In forming my opinions, I do not believe that any express constructions are required because the prior art teaches substantially the same teachings as the '425 Patent's disclosures.

73. If Patent Owner offers constructions of any terms, I reserve the right to address those constructions at a future time.

VIII. DESCRIPTIONS OF ASSERTED PRIOR ART REFERENCES

A. Overview of Wu (U.S. Patent Appl. Pub. No. 2009/0246922)

74. Wu was published on October 1, 2009, from an application filed March 27, 2008. I have been told this qualifies Wu as prior art.

75. In my opinion, Wu is analogous art to the '425 Patent because Wu is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; Wu ¶¶[0001]-[0002]. In my opinion, Wu is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* '425 Patent, 1:15-7:54; Wu ¶¶[0001]-[0007].

76. Wu discloses "strained CMOS" structures with, e.g., a PMOS transistor region 31 and an NMOS transistor region 33. Wu ¶[0009], ¶[0017], FIG. 14. Wu

explains that "[a] plurality of first active area[s] and a plurality of second active area[s] are defined on the semiconductor substrate 30," whereby "[e]ach of the first active area[s] includes a first-type well and a gate structure, and each of the second active area[s] includes a second-type well and a respective gate structure thereon." Wu ¶[0017]. In a "preferred embodiment," Wu's "first active area is a PMOS transistor region 31" and the "second active area is an NMOS transistor region 33." Wu ¶[0017].

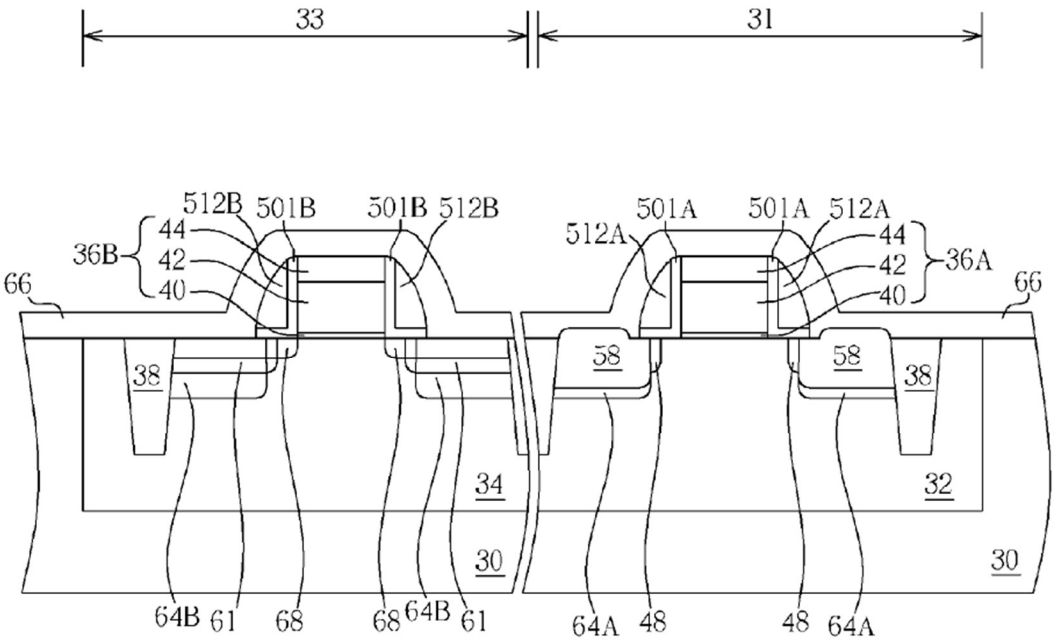


FIG. 14

Wu's FIG. 14

77. In the PMOS transistor region, Wu describes "an epitaxial layer 58 of silicon germanium" that is "slightly projected from the top surface of the semiconductor substrate 30 to compress the channel." Wu ¶[0021], ¶[0041], FIG. 14. Wu also describes removing a "sacrificial layer 52" that creates a space

between the raised edge of the SiGe epitaxial layer 58 and the sidewall structure of the gate electrode. *See, e.g.*, Wu ¶[0022], ¶[0042], FIGS. 5-7, 13-14. After depositing sidewalls 512A, Wu teaches a strained contact etch stop layer (CESL) 66 deposited over PMOS transistor 31 and NMOS transistor 33. Wu ¶[0025], ¶[0044], FIG. 14. Further, "a self-aligned silicide process (salicide process) is optionally performed" in certain areas before depositing CESL 66. Wu ¶[0024], ¶[0043].

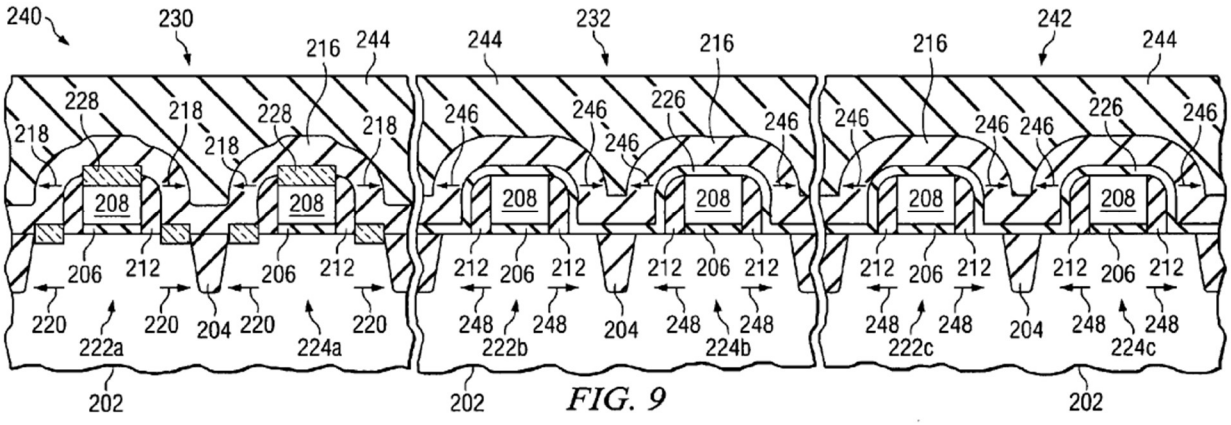
B. Overview of Alvarez (U.S. Patent Appl. Pub. No. 2007/0249069)

78. Alvarez was published on October 25, 2007, from an application filed April 25, 2006. I have been told this qualifies Alvarez as prior art.

79. In my opinion, Alvarez is analogous art to the '425 Patent because Alvarez is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; Alvarez ¶[0001]. In my opinion, Alvarez is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* '425 Patent, 1:15-7:54; Alvarez ¶[0001].

80. Alvarez discloses a "semiconductor device" with "a plurality of active areas," such as silicide region 230, non-silicide region 232, and stress-control region 242, each including PMOS transistors 224*x* and NMOS transistors 222*x*. Alvarez, Abstract, ¶¶[0037]-[0038], FIGS. 9-11. In regions 232 and 242, Alvarez

discloses a "stress-controlling material 226" to mitigate stress caused by a "stress-increasing material 216" and to prevent silicidation in certain regions, such as "non-silicide region" 232 and "stress-control region" 242. Alvarez ¶[0035], ¶[0037], ¶[0045], ¶[0049], ¶[0054], ¶[0078], FIG. 9. Alvarez teaches that "stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases the first amount of stress by about the second amount of stress 218 less the third amount of stress 246, for example." Alvarez ¶[0045], ¶[0049], ¶[0054], FIG. 9. For example, "stress-increasing material 216 is formed over the at least one first active area and over the stress-controlling material 226," and "the stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases a stress level" in the active area. Alvarez ¶[0061], FIG. 9, *see also* Alvarez ¶[0054], Tbl. 1.

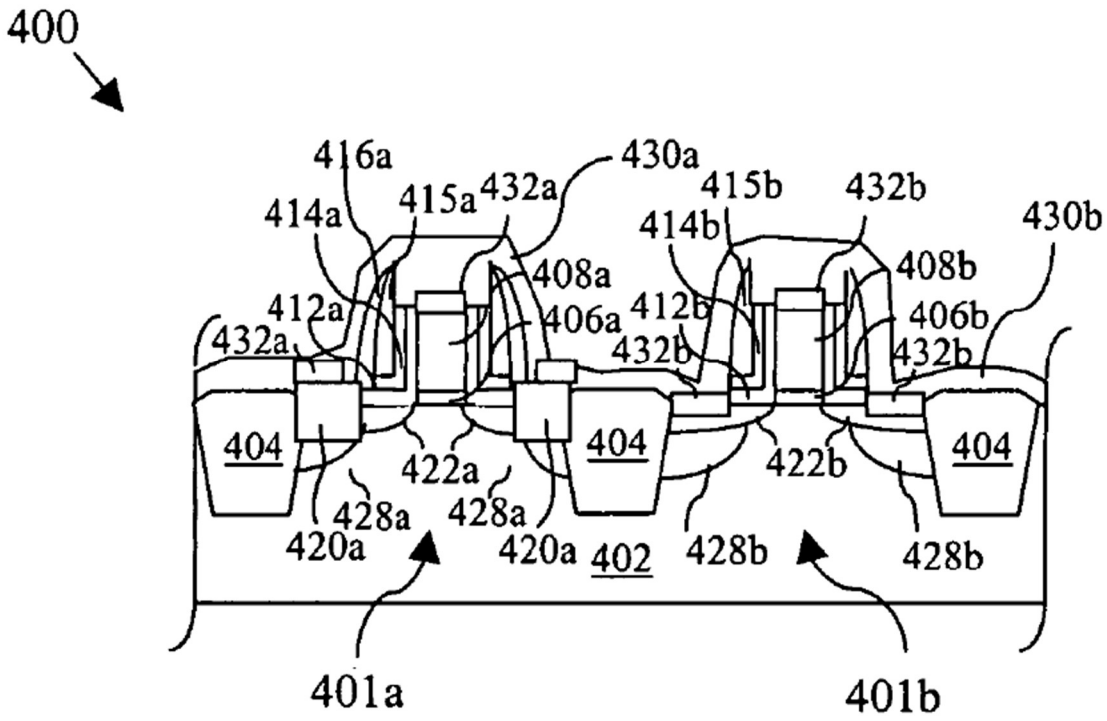


Alvarez's FIG. 9

C. Overview of Cheng (U.S. Patent Appl. Pub. No. 2005/0112817)

81. Cheng was published on May 26, 2005, from an application filed August 11, 2004. I have been told this qualifies Cheng as prior art.

82. In my opinion, Cheng is analogous art to the ’425 Patent because Cheng is in the same field of endeavor as the ’425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* ’425 Patent, 1:15-7:54; Cheng ¶[0013]. In my opinion, Cheng is also analogous art to the ’425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* ’425 Patent, 1:15-7:54; Cheng ¶¶[0002]-[0003], ¶[0013].



Cheng’s Fig. 4j

83. Cheng discloses “a P-type MOS device” 401a and an “N-type MOS device” 401b. Cheng ¶[0056], Fig. 4j. The PMOS device 401a includes raised SiGe “source and drain regions 420a” that are “built-up” to “extend above the substrate

surface" and impart compressive stress to the PMOS channel. Cheng ¶[0022], ¶[0065], Fig. 4j. Additionally, an etch stop layer 430a/430b may be a "tensile film" or "compressive film" made of "silicon nitride (Si_xN_y)." Cheng ¶[0070], Fig. 4j.

D. Overview of Wang (U.S. Patent Appl. Pub. No. 2007/0034906)

84. Wang was published on February 15, 2007, from an application filed December 27, 2005. I have been told this qualifies Wang as prior art.

85. In my opinion, Wang is analogous art to the '425 Patent because Wang is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; Wang ¶[0002]. In my opinion, Wang is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* '425 Patent, 1:15-7:54; Wang ¶[0002].

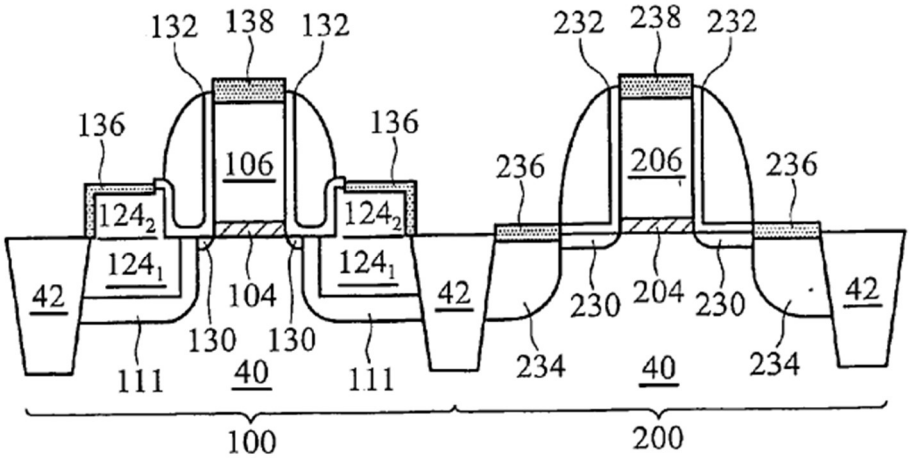


FIG. 16

Wang's FIG. 16

86. Wang, like Cheng, discloses "a region 100 for forming a pMOS device and a region 200 for forming an nMOS device." Wang ¶[0023], FIG. 16. Wang explains that "to strengthen the compressive stress applied by the silicon [SiGe] alloy regions 124 [in pMOS devices], the silicon alloy regions 124 preferably outgrow the top surface of the substrate 40, forming raised portions 124_2," having a height between 10 and 70 nm. Wang ¶[0031], FIG. 16.

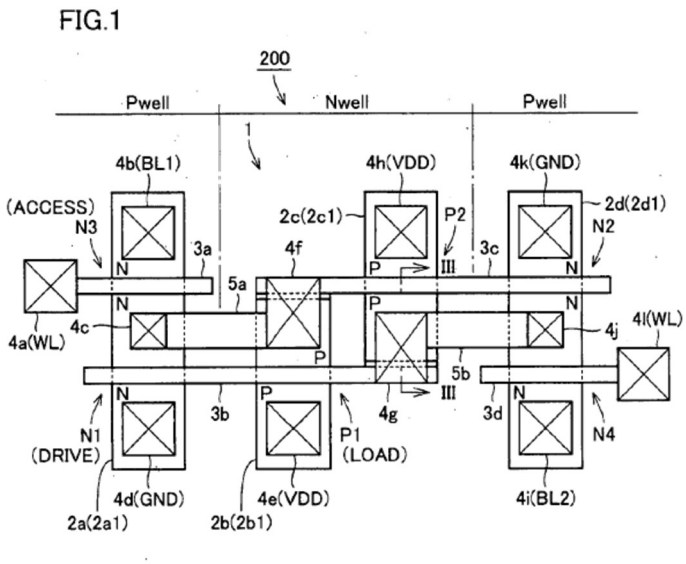
E. Overview of Saito (U.S. Patent Appl. Pub. No. 2008/0029825)

87. Saito was published on February 7, 2008, from an application filed August 2, 2007. I have been told this qualifies Saito as prior art.

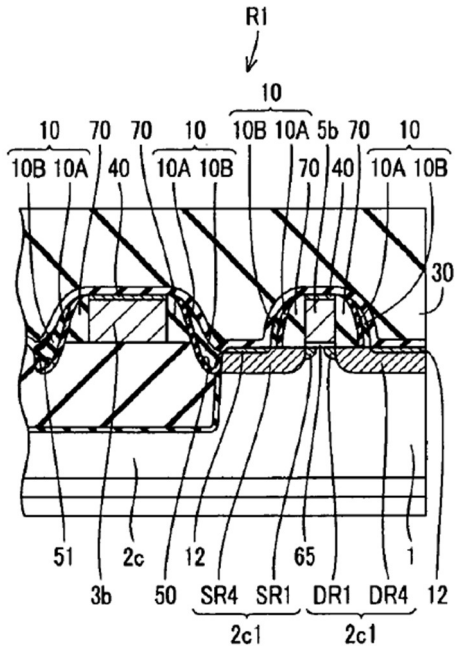
88. In my opinion, Saito is analogous art to the '425 Patent because Saito is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; Saito ¶[0002]. In my opinion, Saito is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating semiconductor devices with polysilicon interconnects that, when fabricated, create recesses in the neighboring isolation regions. *See* '425 Patent, 1:15-7:54, 10:61-64, FIG. 2A; Saito ¶[0002], ¶[0096], ¶[0099], FIGS. 5, 17.

89. Saito discloses an SRAM circuit with PMOS transistors P1-P2 and NMOS transistors N1-N4. Saito ¶¶[0056]-[0059], FIG. 1. During manufacturing,

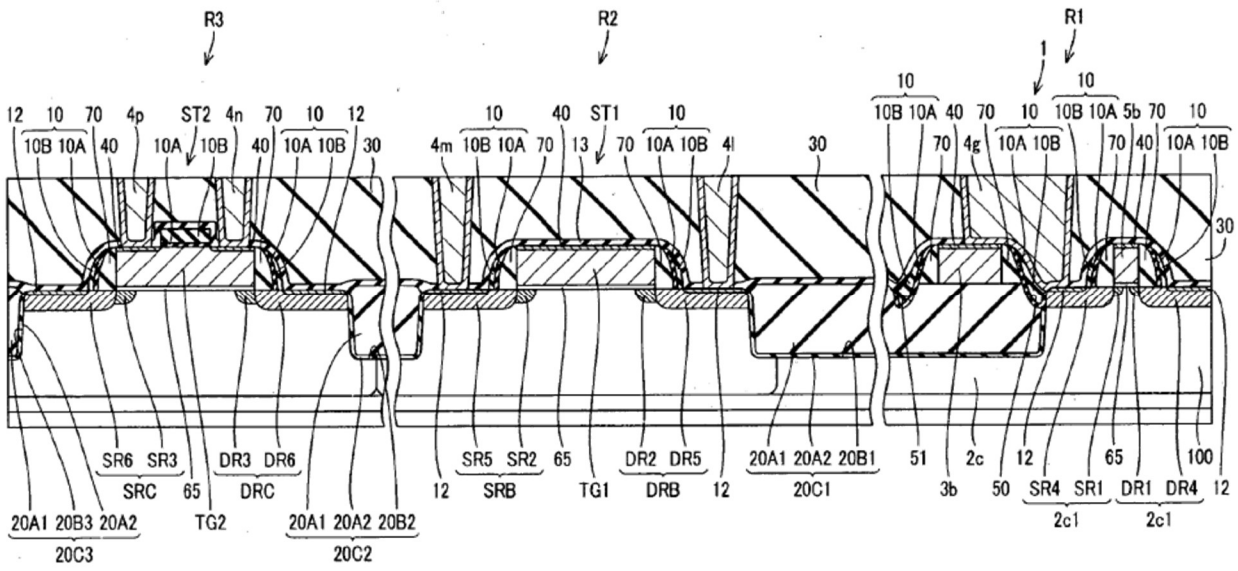
Saito discloses that recesses 50 form in isolation regions 20A1 located next to polysilicon wirings 3b and 3c in PMOS active regions 2b and 2c. Saito ¶[0096], ¶[0099], FIGS. 1, 5, 17. Saito teaches "fill[ing] up" recesses 50 by depositing silicon oxide layer 10A and nitride layer 10B. Saito ¶¶[0074]-[0076], ¶¶[0112]-[0113], FIGS. 3, 11, 12, 21. Saito also discloses a nitride insulating film 13 formed over the entire wafer. *See* Saito ¶[0091] (explaining that FIG. 12 includes "well region[s] of various conductivity types"), FIGS. 12, 21.



Saito's FIG. 1



Saito's FIG. 21 (excerpted)



Saito's FIG. 21

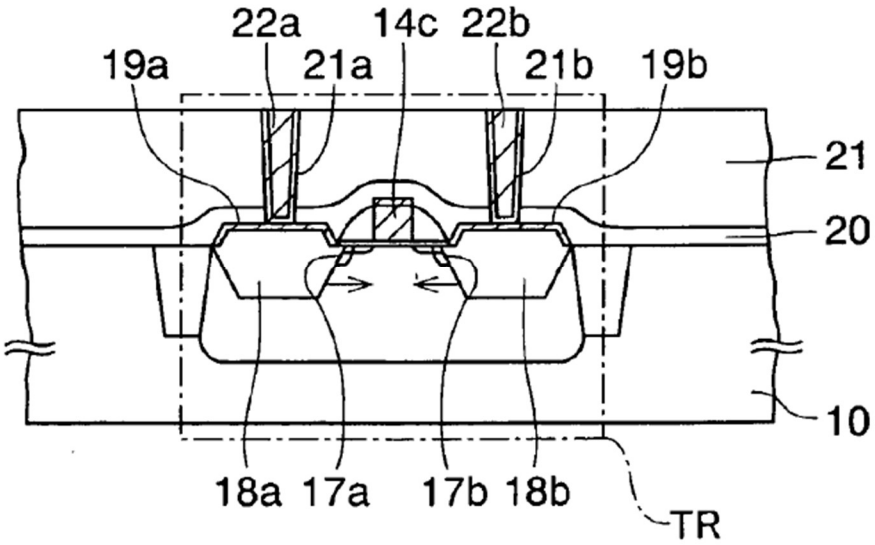
F. Overview of Fukutome (U.S. Patent Appl. Pub. No. 2005/0285203)

90. Fukutome was published on December 29, 2005, from an application filed December 13, 2004. I have been told this qualifies Fukutome as prior art.

91. In my opinion, Fukutome is analogous art to the '425 Patent because Fukutome is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; Fukutome ¶¶[0002]-[0003]. In my opinion, Fukutome is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* '425 Patent, 1:15-7:54; Fukutome ¶¶[0002]-[0012].

92. Fukutome discloses a semiconductor device in which faceted epitaxial SiGe "source/drain material layers 18a and 18b" are grown to "positions higher than the surface of the silicon substrate." Fukutome ¶[0092], ¶[0096], ¶[0100], FIGS. 5D-5G. According to Fukutome, growing the SiGe higher than the substate "increases the distances between the p-n junction at the bottom surface of the n-well 12 and conductive plugs to be formed on the source/drain material layers 18a and 18b later." Fukutome ¶[0100]. Fukutome explains that, in such cases, "a junction leakage in the above-described p-n junction can be suppressed, and the reliability of the transistor can be improved." Fukutome ¶[0100]. Fukutome also teaches a silicon nitride layer 20 deposited "on the entire surface" of the device. Fukutome ¶[0106], FIG. 5G.

FIG. 5G



Fukutome, FIG. 5G

G. Overview of James (D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (Apr. 2005))

93. James was presented in April 2005 at the 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, and I have been told that it was added to the IEEE Xplore database not later than June 2005. James was published at a well-known conference those skilled in the art would have attended, and anyone skilled in the art would have been able to locate and obtain a copy of James in the conference proceedings. It was also common for those skilled in the art to review the conference proceedings when they became available on IEEE Xplore shortly after the conference, for example. I am familiar with the James publication and possessed a copy obtained through publicly available IEEE sources more than a year before January 7, 2010.

94. In my opinion, James is analogous art to the '425 Patent because James is in the same field of endeavor as the '425 Patent (semiconductor devices and methods for fabricating semiconductor devices, including MISFETs). *See* '425 Patent, 1:15-7:54; *see generally* James. In my opinion, James is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '425 Patent addresses, for example, fabricating strain-engineered semiconductor devices. *See* '425 Patent, 1:15-7:54; *see generally* James.

95. James describes various "physical transistor structures" of commercial devices, including devices made by Intel's 90nm process (codenamed Prescott or P1262). James, 1-5, Figs. 1-3, 5-12. James explains that, in Prescott, "[l]ocalized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer" that " increases electron mobility by ~10%." James, 2, Figs. 5, 6. Prescott's "PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress," which "improves hole mobility by as much as 50%." James, 2, Fig. 6. The raised PMOS SiGe source/drain regions in FIG. 6 have "[c]rystalline facets" that "reduc[e] the series resistance" and apply compressive stress that "counteract[s]" the "tensile stress from the nitride layer." James, 2, Fig. 6.

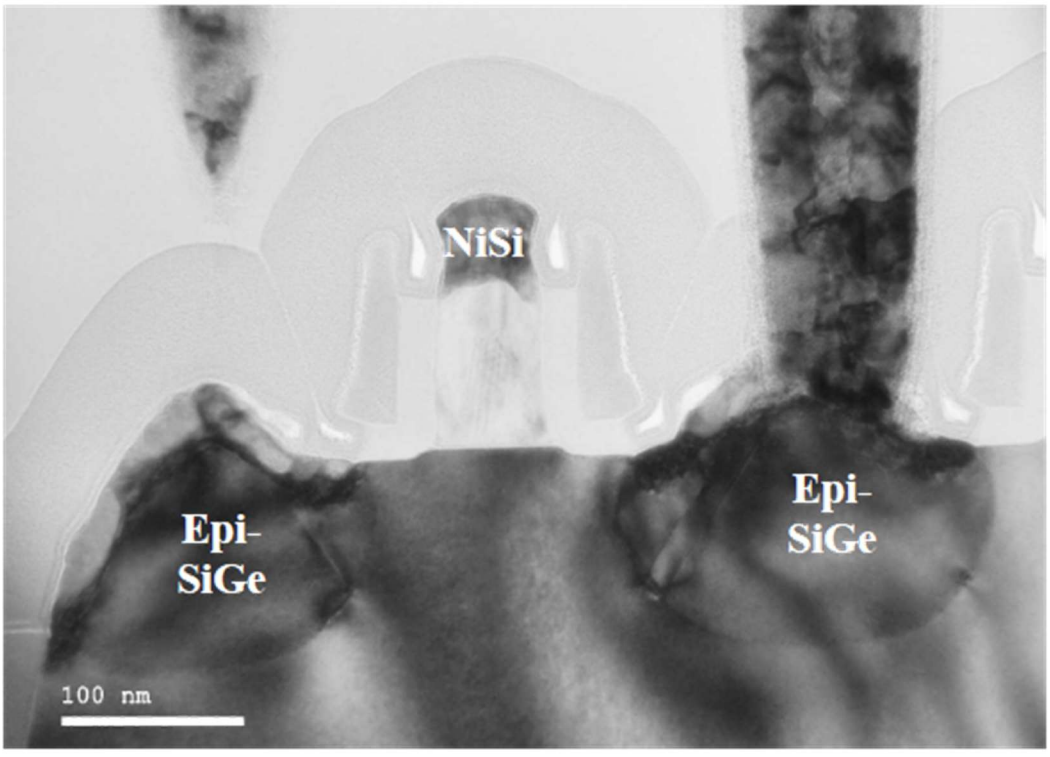


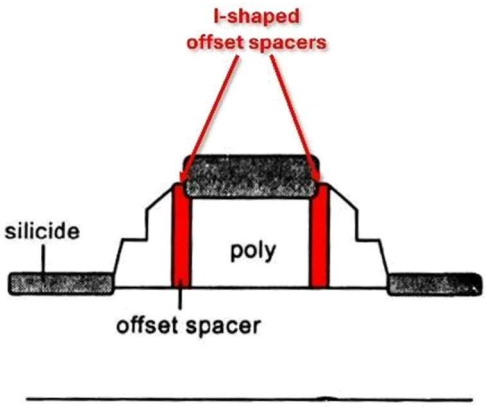
Figure 6. Intel PMOS Transistor
James, Fig. 6

H. Overview of Wolf (S. Wolf, "Silicon Processing for the VLSI Era Volume 4: Deep-Submicron Process Technology")

96. Wolf is a well-known textbook for semiconductor processing published in 2002 by Lattice Press. It is the fourth volume in a four-part series of textbooks that was widely known in the field before January 7, 2010. I am familiar with Wolf and possessed a copy obtained through publicly available sources before January 7, 2010.

97. In my opinion, Wolf is analogous art to the '425 Patent because Wolf is in the same field of endeavor (MISFETs). *See* '425 Patent, 1:15-7:54; Wolf, Preface, 216-19. In my opinion, Wolf is also analogous art to the '425 Patent because a POSITA would have found it reasonably pertinent to a problem the '425 Patent addresses, for example, manufacturing source/drain extensions in MISFET devices using offset spacers. *See* '425 Patent, 1:15-7:54; Wolf, 216-19.

98. Wolf, like Wu and Cheng, teaches semiconductor device structures. Wolf, Preface, 216-19. Wolf teaches using an I-shaped "offset-spacer" to space apart doping in the channel source-drain extension ("SDE") region to prevent "excessive leakage (due to larger short-channel effects that arise if the channel length is too small)" and "yield[] optimum device characteristics." Wolf, 216-17, Fig. 5-25.



Wolf's Fig. 5-25 (annotated)

IX. CLAIMS 1-15 OF THE '425 PATENT WOULD HAVE BEEN OBVIOUS TO A PERSON OF ORDINARY SKILL IN THE ART

99. I have reviewed the materials listed in Exhibit A and, in my opinion, a POSITA would have found claims 1-15 of the '425 Patent obvious as of January 7, 2010.

A. Summary of Bases of Unpatentability

100. The table below summarizes the bases for my opinion in this declaration that claims 1-15 of the '425 Patent are unpatentable:

Ground	Claim(s) Challenged	Basis	Reference(s)
1A	1, 3-5, 7-9, 11-15	Obviousness	Wu, Alvarez
1B	2	Obviousness	Wu, Alvarez, Wolf
2A	1, 3-9, 11, 12	Obviousness	Cheng
2B	2	Obviousness	Cheng, Wolf
2C	1, 3-9, 11, 12	Obviousness	Cheng, Wang

Ground	Claim(s) Challenged	Basis	Reference(s)
2D	2	Obviousness	Cheng, Wang, Wolf
3	1, 3, 4, 7, 8, 10	Obviousness	Saito, Fukutome, James

B. Grounds 1A and 1B: Wu Grounds

1. Ground 1A: The Combination of Wu and Alvarez Renders Claims 1, 3-5, 7-9, and 11-15 Obvious

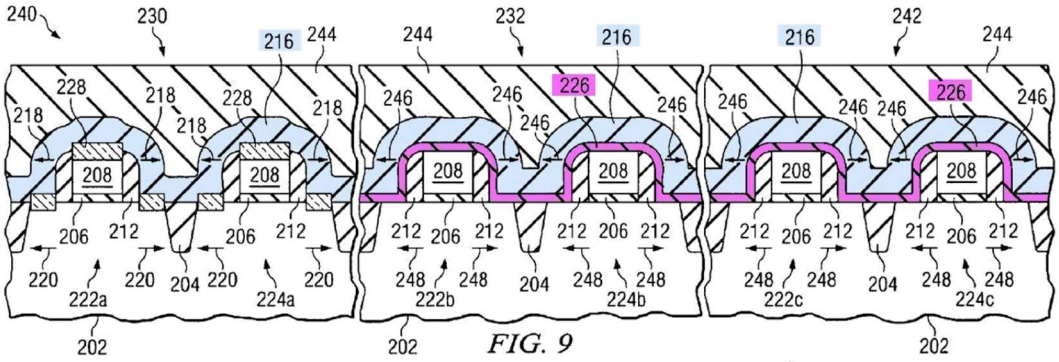
a. The Wu-Alvarez Combination Would Have Been Obvious

101. In my opinion, a POSITA would have found claims 1, 3-5, 7-9, and 11-15 of the '425 Patent obvious. More specifically, it is my opinion that a POSITA would have found it obvious to include a stress-relief layer like the one Alvarez discloses (e.g., Alvarez's stress-control layer 226/326/426) selectively on Wu's transistors. Further, it is my opinion that a POSITA would have found it obvious to make Wu's CESL 66 tensile, as Alvarez also discloses (e.g., Alvarez's tensile stress-insulating layer 216/316/416).

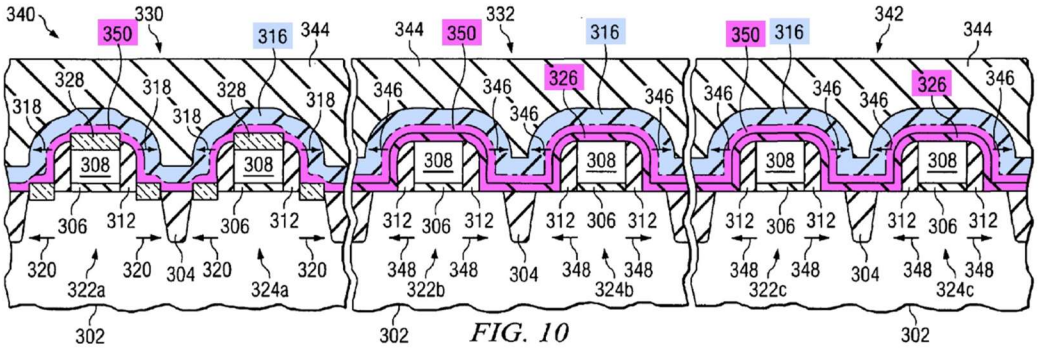
(1) A POSITA would have been motivated to impart tensile strain to Wu's strained CESL layer to boost nFET carrier mobility and to include Alvarez's stress-controlling layer to mitigate the effects of a tensile CESL on pFET carrier mobility

102. In my opinion, a POSITA would have found it obvious to make Wu's CESL tensile, which would have improved Wu's nFETs by boosting carrier (electron) mobility in those devices.

103. In my opinion, a POSITA also would have found it obvious to add a stress-controlling layer like Alvarez's layer(s) 226/326/426 and/or 350/450[10] to Wu's semiconductor device to mitigate the effects of this tensile stress on pFETs. As Alvarez confirms, a POSITA would have found such an approach obvious to balance improvements to both nFET and pFET devices while also reducing the number of manufacturing steps to manage costs.



Alvarez's FIG. 9 (annotated)



Alvarez's FIG. 10 (annotated)

[10] Although I may refer to multiple designations in this declaration (e.g., 226/326/426), Alvarez explains that common designations of the last two digits of reference numerals refer to similar features. For example, x06 refers to the gate dielectric material. Alvarez ¶[0063]. Similarly, x22 refers to nFETs, whereas x24 refers to pFETs. *See* Alvarez ¶[0025], ¶[0028], ¶[0063].Therefore, even if I refer to only one feature (e.g., 226), my discussion generally applies to Alvarez's discussion of similar features (e.g., 326, 426).

104. As I explain in further detail below, a POSITA would have found it obvious to combine certain teachings from Alvarez with Wu's basic device design. First, a POSITA would have found it obvious to add a stress-controlling layer (like Alvarez's stress-controlling layer(s) 226/326/426 and/or 350/450) over both nFET and pFET devices, as Alvarez's FIGS. 9 and 10 show (see above). Second, a POSITA would have found it obvious to implement Wu's device structures in different circuit regions (like Alvarez's silicide region 230/330, non-silicide region 232/332, and stress-control region 242/342). In such a combination, the pFETs in stress-control region 242/342 would satisfy the requirements of claims 1, 4, 5, 7, and 8, and would have rendered obvious the nFET of claim 9. Additionally, the pFETs in silicide region 330 would satisfy the requirements of claims 1 and 3. The nFETs in silicide region 230 would satisfy the requirements of claims 11 and 12 and, alternatively, the nFETs in stress-control region 242/342 would satisfy the requirements of claim 11. Finally, pFETs in non-silicide region 232/332 would satisfy the requirements of claims 13-15.

(a) Relevant descriptions from Wu

105. Wu discloses "a method of forming a strained CMOS transistor to improve CMOS transistor performance and reliability." Wu ¶[0009], FIGS. 1-7, 9-14. Wu explains that the semiconductor device includes a first active region 31, such as "PMOS transistor region 31." Wu ¶[0017], ¶[0023], ¶[0038], ¶¶[0042]-

[0043], FIGS. 1-7, 9-14. PMOS transistor region 31 includes conventional structures and layers, such as gate structure 36A, which includes "a gate dielectric layer 40, a gate 42, and a cap layer 44." Wu ¶[0017], ¶[0039], FIGS. 1-7, 9-14. To illustrate these and other features, I have provided an annotated version of Wu's FIG. 14 below.

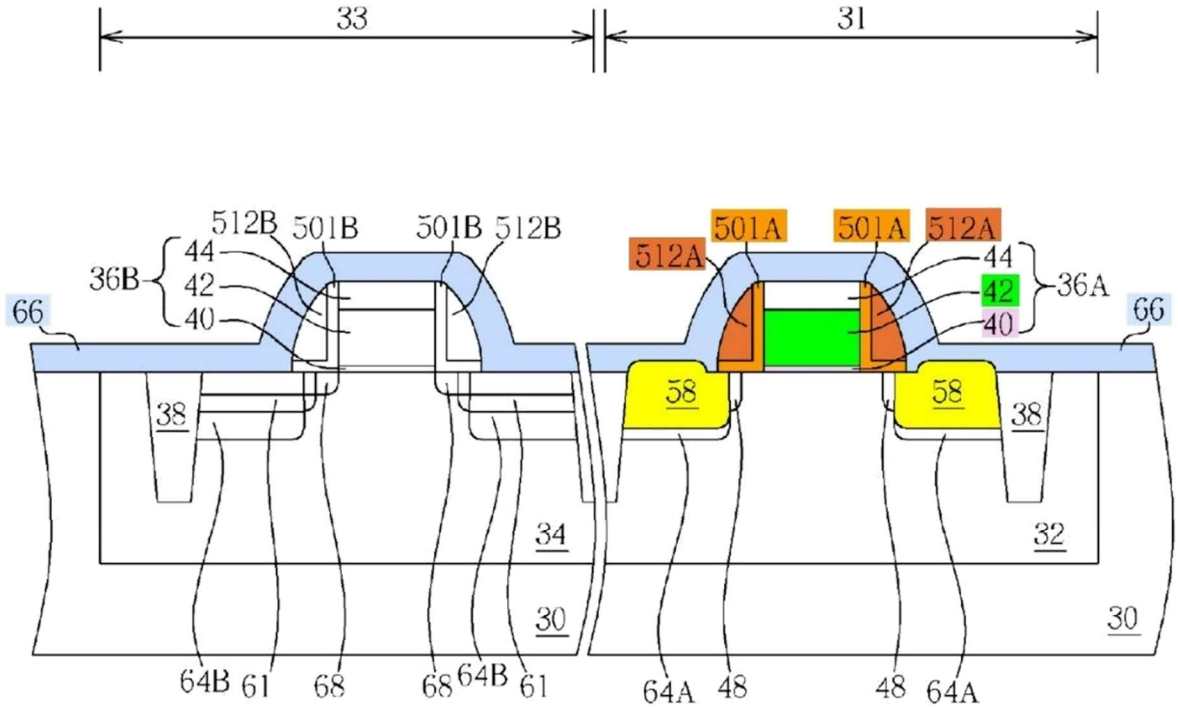


FIG. 14

Wu's FIG. 14 (annotated)

106. Wu's gate structure includes sidewalls 501A, 502A. Wu ¶[0017], ¶[0039], FIGS. 1-7, 9-14. After forming sidewalls 501A, 502A, Wu describes providing sacrificial layer 52 an additional spacer. Wu ¶¶[0019]-[0021], ¶¶[0040]-[0041], FIGS. 2-4, 10-12. For example, "sacrificial layer 52, such as a silicon nitride layer, is formed covering the semiconductor substrate 30." Wu

¶[0040]. After forming sacrificial layer 52 on gate structure 36A, Wu describes etching a trench 56 into the silicon substrate, then growing epitaxial silicon germanium (SiGe) layer 58 in trench 56. Wu ¶¶[0019]-[0021], ¶¶[0040]-[0041], FIGS. 2-4, 10-12. More specifically, Wu explains that "an etch process . . . is performed . . . to etch the sacrificial layer 52 and the semiconductor substrate 30 beside the gate structure 36A" to form "recess 56 . . . on the surface of the N well 32 beside the gate structure 36A." Wu ¶[0040], ¶[0020], FIGS. 2-3, 10-11.

107. Wu teaches that the epitaxial SiGe layer 58 may be grown such that the top surface is raised above the surface of the substrate, which Wu explains and a POSITA would have recognized imparts a compressive stress in the PMOS channel region of PMOS transistor region 31. Wu ¶¶[0019]-[0021], ¶¶[0040]-[0041], FIGS. 2-4, 10-12. The "epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30," which a POSITA would have understood describes the epitaxial SiGe layer 58 being raised above the surface of substrate 30, as FIGS. 4-7 and 12-14 show. Wu ¶[0021], ¶[0041], FIGS. 4-7, 12-14. Raised epitaxial layer 58 is separated from sidewalls 501A/502A by the width of sacrificial layer 52.

108. Wu's epitaxial SiGe layers 58 are source/drain regions that "ha[ve] a lattice constant greater than that of the semiconductor substrate 30." Wu ¶[0021], ¶¶[0040]-[0041], FIGS. 4-5, 12. Wu explains that, as was well known (*see* Section

VI.B above), the larger lattice constant of the SiGe "compress[es] the channel" under PMOS transistor 31, which improves PMOS hole mobility and PMOS performance. *See* Wu ¶[0021], ¶[0041], FIGS. 4, 12.

109. Wu teaches that, after forming the raised SiGe source/drains 58, sacrificial layer 52 and sidewall 502A are removed by etching. Wu ¶¶[0022]-[0024], ¶¶[0042]-[0043], FIGS. 5-7, 13-14. A new sidewall spacer 512A is then "formed on the sidewalls of the gate structures 36A, 36B" using "the same . . . processes [as] for forming the first spacers 502A." Wu ¶[0024], FIGS. 7, 14. This process leaves a space between sidewalls 501A/512A and the raised SiGe 58, as annotated FIG. 14 shows below. Wu ¶¶[0022]-[0024], ¶[0032], ¶¶[0042]-[0043], FIGS. 5-7, 13-14.

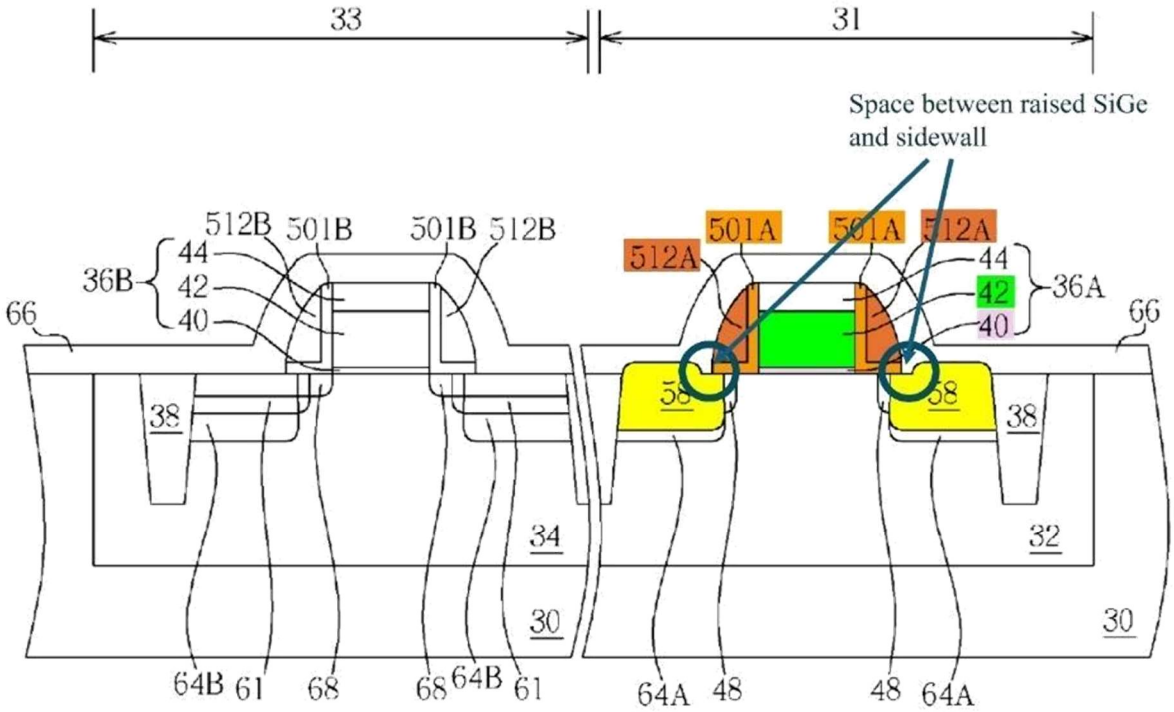


FIG. 14

Wu's FIG. 14 (annotated)

110. Although not illustrated in Wu's FIG. 14, after growing the raised epitaxial SiGe layer 58 in the trench 56, Wu explains that "a self-aligned silicide process (salicide process) is optionally performed." Wu ¶[0024]; *see also* Wu¶[0043] ("[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain."); Wu ¶[0036] ("A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor."), ¶[0055] (same). To do this, "[a] metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B." Wu ¶[0024].

111. After the source/drain regions are complete, Wu discloses "form[ing] a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B," as well as oxide layers 501A/501B. Wu ¶[0025], ¶[0044], FIGS. 7, 14. Wu explains that CESL 66 may be "a strained silicon material, i.e. silicon nitride." Wu ¶[0025]. It "exert[s] tensile stress or compressive stress upon the MOS transistor" to "reduce carrier mobile resistance[,] thereby improving carrier mobility and MOS transistor

performance," which was well known in the art. Wu ¶[0005], ¶[0025]; *see* Section VI.B above.

112. Although Wu explains that CESL may be strained silicon, it does not state whether strained CESL 66 imparts tensile strain to boost NMOS electron mobility or compressive strain to boost PMOS hole mobility. *See* Wu ¶[0005], ¶[0025]; *see* Section VI.B above. Wu's general description of improving "carrier mobility" (as opposed to "hole" or "electron" mobility more specifically) would have suggested to a POSITA that the CESL layer 66 could have either tensile strain to improve nFET carrier mobility or compressive strain to improve pFET carrier mobility. Again, it was well known in the art to use a strained CESL to enhance carrier mobility of MOS transistors. *See* Section VI.B above.

(b) Known advantages of making Wu's CESL 66 tensile and adding a strain-buffer layer

113. A POSITA, reading Wu in view of Alvarez, in my opinion, would have found it obvious to form Wu's CESL 66 as a tensile layer to improve pFET carrier (electron) mobility. First, a tensile CESL was well known in the prior art to improve carrier mobility and had appeared in several generations of commercial devices. *See* Section VI.B above. Second, a POSITA would have recognized that imparting tensile strain using CESL 66 would have benefitted nFETs that are "relatively difficult to improve" while, at the same time, Wu's compressive epitaxial SiGe layer 58 improves the pFET carrier mobility. Hsu823 ¶[0039].

114. A POSITA would have known that, historically, nFETs had better performance than pFETs because electrons (in nFETs) have a naturally higher mobility in silicon than do holes (in pFETs). A POSITA thus would have recognized the design choice to balance carrier mobility improvements in pFETs and nFETs with other factors, such as ease of manufacturing. A POSITA would have recognized, as a design choice, that stress from a tensile CESL could be offset by a strain-buffer layer to mitigate the negative effects of tensile stress on pFET mobility. *See* Section VI.C above. In fact, Alvarez itself teaches that a stress-controlling layer (e.g., stress-control layer 226/326/426 and/or 350/450) mitigates the adverse effects of a tensile CESL on pFET carrier (hole) mobility.

115. A POSITA also would have recognized additional benefits from using a strain-buffer layer like the one Alvarez discloses, including to match "performance requirements of transistors in the particular regions," "tun[ing]" channel strain, and reducing the number of manufacturing steps to reduce cost. *See* Alvarez ¶[0028], ¶[0032], ¶¶[0034]-[0035], ¶¶[0045]-[0046], ¶[0055], ¶¶[0063]-[0068], ¶[0075], ¶[0078], FIGS. 8-11.

116. Alvarez confirms the well-known proposition that "[s]ome NMOS FETs have demonstrated performance enhancement" introducing "tensile stress to the channel region," but "some PMOS FETs may suffer from decreased performance" when a tensile nitride material layer is deposited over the PMOS

transistor. Alvarez ¶[0025]; *see also* Section VI.B above; Morin, 355-56. Alvarez also teaches that the adverse effects from a tensile CESL on PMOS carrier mobility can be mitigated by applying an intermediate stress-controlling layer 226/326/426 and/or 350/450 underneath the tensile CESL layer (216/316/416). Alvarez ¶[0028], ¶[0032], ¶¶[0034]-[0035], ¶¶[0045]-[0046], ¶[0055], ¶¶[0063]-[0068], ¶[0075], ¶[0078], FIGS. 8-11. Alvarez explains that, "due to the presence of the first material or stress-controlling material 226 in the second region 232 and the third region 242, the stress-increasing material 216 has less of an impact [on] the stress 248 in the channel regions of the [PMOS] transistors . . . 224b, . . . and 224c in the second region 232 and the third region 242." Alvarez ¶[0049]; *see also* Alvarez ¶[0043], ¶¶[0053]-[0055], ¶[0065], Tbl. 1 ("The first material 226 preferably comprises a material adapted to screen or control the amount of stress that a subsequently deposited stress-increasing material has on an underlying material layer, such as channel regions . . . .").

117. Alvarez teaches that stress-control layer 226/326/426 and/or 350/450 has several benefits, including (i) reducing the adverse effects from stress-inducing layer 216/316/416 on PMOS channel regions by "screen[ing] or control[ling] the amount of stress" imparted by the stress-inducing layer 216/316/416; (ii) selectively blocking unwanted silicide formation in certain circuit regions, such as non-silicide region 232 and stress-control region 242; and (iii) reducing or eliminating

processing steps to lower manufacturing costs. Alvarez ¶[0037], ¶[0043], ¶[0049], ¶[0061], ¶¶[0063]-[0064], ¶¶[0069]-[0075], ¶[0078], ¶[0081], FIGS. 9-13.

118. In my opinion, a POSITA would have recognized that these benefits, in some cases, may be interrelated with one other. For example, Alvarez discloses using stress-control layer 226/326/426 to selectively block silicide formation in non-silicide region 232 and stress-control region 242, for example. Alvarez ¶¶[0045]-[0047], ¶[0068], ¶[0078], FIGS. 7-10. Moreover, by leaving stress-control layer 226/326/426 and/or 350/450 intact when depositing a tensile CESL 216/316/416, the number of process steps is reduced. Alvarez ¶[0033] (describing "costly and time-consuming" process" of depositing both tensile and compressive layers), ¶[0045] (explaining that stress-control layer 226 is also used as silicide masking material layer), ¶[0074], ¶[0078] (explaining that using stress-control layer as silicide masking layer "results in a cost savings").

119. A POSITA, in my opinion, would have found it obvious to achieve these benefits by implementing Wu's strained CESL 66 with tensile strain to improve NMOS carrier mobility (as Alvarez demonstrates with examples like the ones in FIGS. 9-11 and Tbl. 1). *See* Alvarez ¶¶[0053]-[0055] ("Preferably the material and deposition process for the first [stress-controlling] material 226 is selected or tuned to achieve the amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b,

224b, 222c, and 224c in the second region 232 and the third region 242, of the effect of the second [stress-increasing] material 216."). A POSITA also would have found it obvious to achieve these benefits using Wu's basic transistor structure by adding a stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 to (i) mitigate (e.g., screen or control) the adverse effects of tensile CESL on PMOS carrier mobility by "tuning" the relevant films to balance the stresses applied to the NMOS and PMOS transistors; (ii) prevent unwanted silicide formation in certain circuit regions (e.g., regions analogous to Alvarez's non-silicide region 232/332 and stress-control region 242/342); and (iii) reduce manufacturing costs by reducing the number of lithography steps. Alvarez ¶[0037], ¶[0049], ¶¶[0053]-[0055], ¶[0061], ¶¶[0070]-[0075], ¶[0078], ¶[0081], FIGS. 9-11.

120. Alvarez further explains that placing a stress-controlling layer 226/326/426 and/or 350/450 between the source/drain regions and a tensile CESL has benefits compared to applying a tensile CESL over the nFETs and a compressive CESL over the pFETs. Although a two-layer/dual-strain approach may have other advantages, it results in "stress mismatch . . . at the lateral interface of the tensile stress material layer and the compressive stress material layer," and is more "costly and time-consuming" than using one CESL with one kind of strain. Alvarez ¶[0033], ¶[0074] (explaining that the "lateral interface between a tensile stress layer and a compressive stress layer is avoided" using a single CESL over both nFETs and

pFETs); *see also* Hsu823 ¶[0039] (preferable to apply tensile CESL across both NMOS and PMOS devices because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 355-56; Bohr683 ¶¶[0038]-[0039], FIG. 6.

121. A POSITA, in my opinion, would have been motivated to implement Alvarez's teaching to apply a stress-controlling layer (like Alvarez's layers 226/326/426 and/or 350/450) over the pFETs in certain circuit regions, including certain silicide regions (like Alvarez's region 330), non-silicide regions (like Alvarez's non-silicide regions 232/332), and stress-control regions (like Alvarez's stress-control regions 242/342) because of Alvarez's benefits discussed in the paragraphs above. Alvarez ¶[0037], ¶[0049], ¶[0061], ¶¶[0074]-[0075], ¶[0078], ¶[0081], FIGS. 9-13. A POSITA would have recognized that implementing Wu's devices in this way would "tun[e]" the stress in various circuit regions such that it "is introduced or increased in some regions, but . . . is reduced or controlled" in others. Alvarez ¶[0026]; *see also* Alvarez ¶¶[0053]-[0055]. Because different transistors in different circuit regions have different requirements (Alvarez ¶[0027] ¶[0032]), a POSITA would have been motivated to apply these teachings from Alvarez to Wu's FETs to tune stress and selectively control silicide formation in a cost-effective way.

(c) How the Wu-Alvarez combination would have worked

122. As others recognized at the time, a POSITA would have found Alvarez's approach advantageous because "it [wa]s important to work to improve nMOS transistors" with tensile CESL, as "other solutions [e.g., SiGe] . . . can enhance the pMOS performances." Morin, 356; *see also* Hsu823 ¶[0039] ("[T]he performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve . . . ."); Bohr683 ¶¶[0038]-[0039], FIG. 6. A POSITA would have recognized that Alvarez's teachings work towards this goal since it allows "stress on underlying materials [to be] introduced or increased in some regions, but wherein the stress introduced in other regions is reduced or controlled." Alvarez ¶[0026]. In the Wu-Alvarez combination, a POSITA would have reasonably expected tensile CESL stress to improve nFET carrier mobility, whereas the stress-controlling film would mitigate degradation of the compressive stress in Wu's pFETs due to epitaxial SiGe layer 58. Alvarez ¶[0026], ¶¶[0053]-[0055]; Wu ¶[0021], ¶[0041]; *see* Sections VI.B and VI.C above.

123. Alvarez teaches that stress-controlling layer 226/326/426 and/or 350/450 reduces, but does not eliminate, the stress from a tensile CESL. It "tunes" the stress to balance the benefits and drawbacks in various regions. *See* Alvarez ¶[0049], ¶¶[0053]-[0055], ¶[0064], Tbl. 1. In other words, one can "achieve the

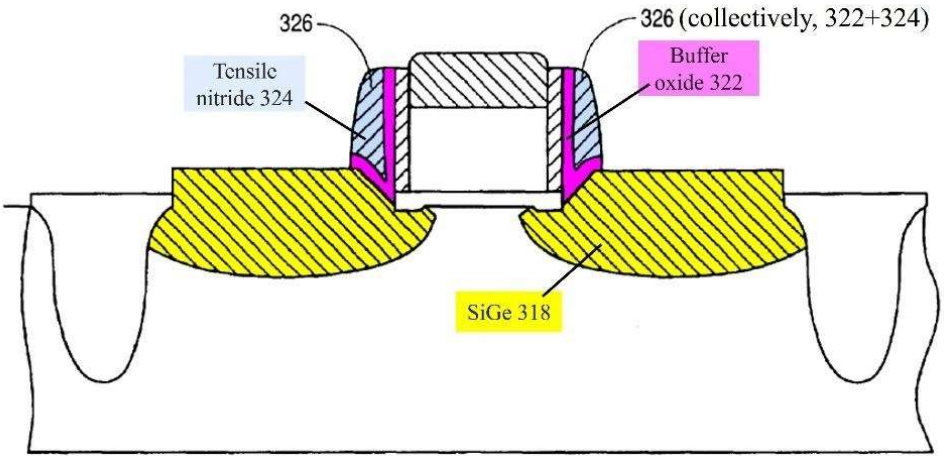
amount of control desired on the stress of the underlying material layer, e.g., such as the channel regions of the transistors 222b, 224b, 222c, and 224c." Alvarez ¶[0053]; *see also* Alvarez ¶¶[0054]-[0055], ¶[0080]. By tuning the stress in devices using Wu's transistor design, a POSITA would have reasonably expected to stress the nFET and pFETs channel regions appropriately while also controlling silicidation and keeping down manufacturing costs. Alvarez ¶[0037], ¶[0049], ¶[0061], ¶¶[0063]-[0064], ¶¶[0069]-[0075], ¶[0078], ¶[0081], FIGS. 9-13.

124. Alvarez confirms this in several different embodiments. In FIG. 9, stress-controlling film 226/326/426 extends over both nFETs 222b/222c and pFETs 224b/224c. In FIG. 10, an additional stress-controlling film 350/450 extends over both nFETs 322a/322b/322c and pFETs 324a/324b/324c. Alternatively, in FIG. 11, the stress-controlling film (or films) extends over only the pFETs to further enhance nFET performance. Alvarez ¶¶[0065]-[0068]. A POSITA would have found these various alternatives obvious as design choices when applying Alvarez's teachings to Wu or any similar MISFET structure with a strained CESL film.

125. Alvarez is not alone in teaching to apply a tensile CESL over both nFETs and pFETs while also using an intermediate stress-relief layer to mitigate the effects on pFETs. It was widely known. *See* Sections VI.B-VI.C above; Wu ¶[0005]; Murthy556, 9:10-29 (explaining that "[o]xide layer 322 buffers the large stress" in silicon nitride layer 324 overlying it), FIG. 8; Doris ¶[0034] ("A tensile barrier etch

stop layer 80, such as CVD or PECVD SiN, is applied to the entire wafer."), ¶[0042] (disclosing "a neutral buffer layer between the compressive spacer and the tensile etch stop layer"), Figs. 2, 14, 15; Lee ¶[0029], ¶¶[0046]-[0067] (explaining that an intermediate stress relief layer "with neutral stress or opposite stress relative to the [CESL]" reduces or eliminates any pFET performance degradation because it "reduces the tensile stress in the channel region"), FIG. 5; Cheng810 ¶¶[0022]-[0031], Fig. 1F (describing similar).

126. For example, Murthy556 discloses an "[o]xide layer 322 [that] buffers the large stress" in an overlying silicon nitride layer 324. Murthy556, 9:27-29. Murthy556's FIGS. 7-9 show a pFET with faceted SiGe source/drain regions 318. Buffer oxide layer 322 forms in the space between the SiGe facets and a gate electrode spacer. Murthy556, 8:59-9:43, FIGS. 7-9. In annotated FIG. 9 below, oxide buffer layer 322 mitigates the tensile effect of a tensile silicon nitride layer 324. Murthy556, 9:27-33.



Murthy556's FIG. 9 (annotated)

127. Doris similarly explains that a silicon dioxide film between an epitaxially grown SiGe source/drain and a tensile etch stop layer can "prevent[] the tension from materially adversely influencing the charge carrier mobility in the pFET 150" by "defin[ing] a neutral buffer layer between the compressive spacer [220] and the tensile etch stop layer [340]." Doris ¶[0034], ¶[0042]; *see also* Lee ¶[0029], ¶¶[0046]-[0067] (explaining that an intermediate stress relief layer "with neutral stress or opposite stress relative to the [CESL]" reduces or eliminates any pFET performance degradation because it "reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810 ¶¶[0022]-[0031], Figs. 1B-1F (describing similar).

128. As Wu's FIGS. 7 and 14 below illustrate, CESL 66 forms in the space between epitaxial SiGe layer 58 and gate sidewalls 501A/512A. When placing a stress-controlling film (like Alvarez's layer 226/326/426 and/or 350/450) under Wu's CESL 66, as in the Wu-Alvarez combination, a POSITA would have understood that the stress-controlling film would form in that space.

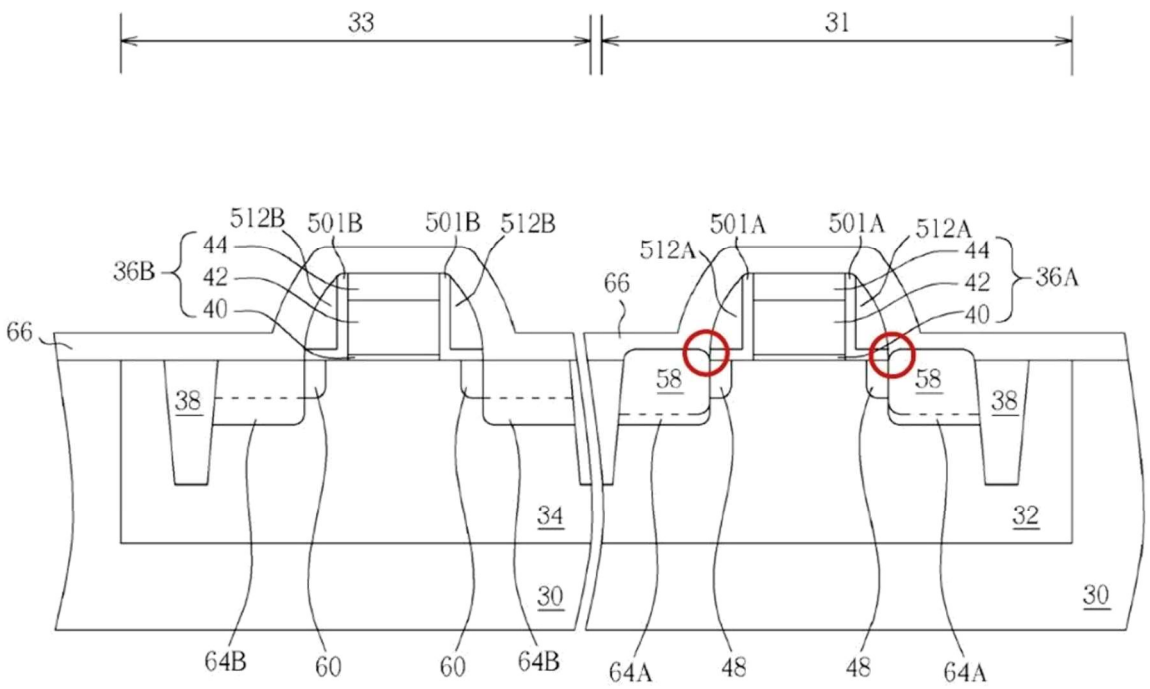


FIG. 7

Wu's FIG. 7 (annotated)

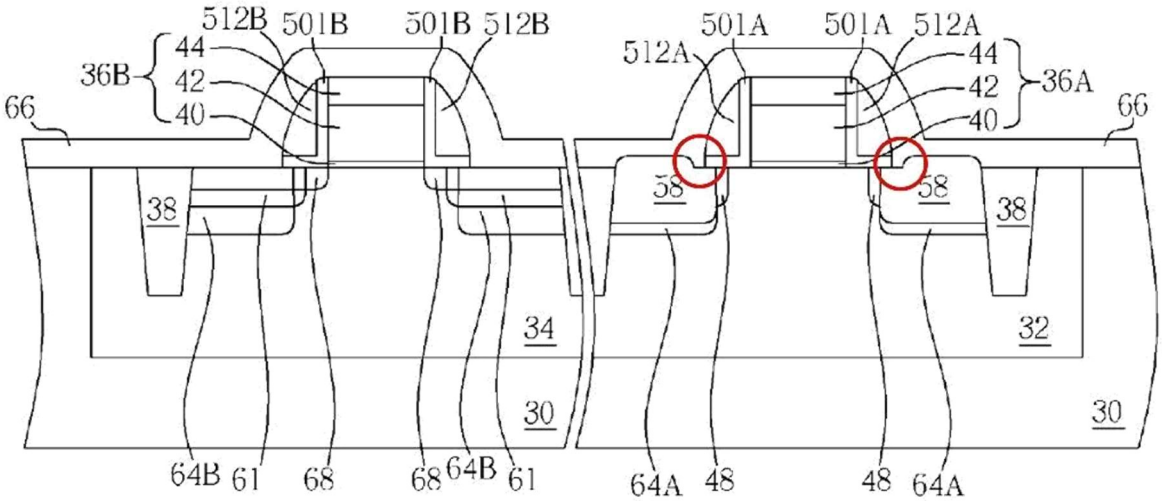
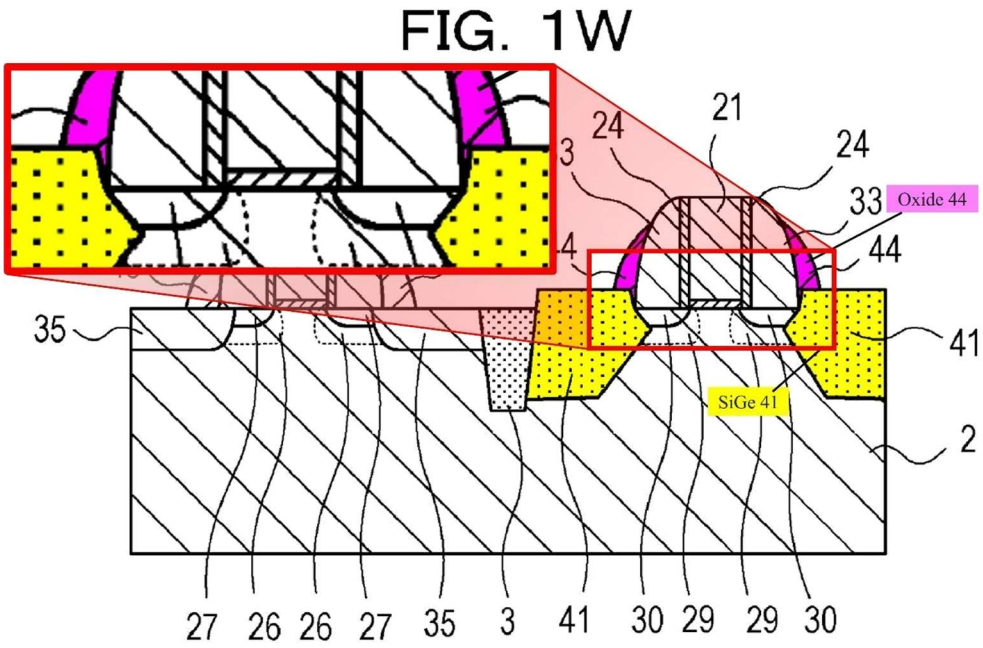


FIG. 14

Wu's FIG. 14 (annotated)

129. Miyashita, for example, confirms this in FIGS. 1V-1W. As shown below, a silicon oxide layer 44 is deposited over a region with a space between a raised, faceted SiGe source/drain 41 and a gate sidewall spacer. Oxide layer 44 forms in that space. Miyashita ¶¶[0052]-[0053], FIGS. 1V-1W; *see also* Murthy556, 8:59-9:43, FIGS. 7-9.

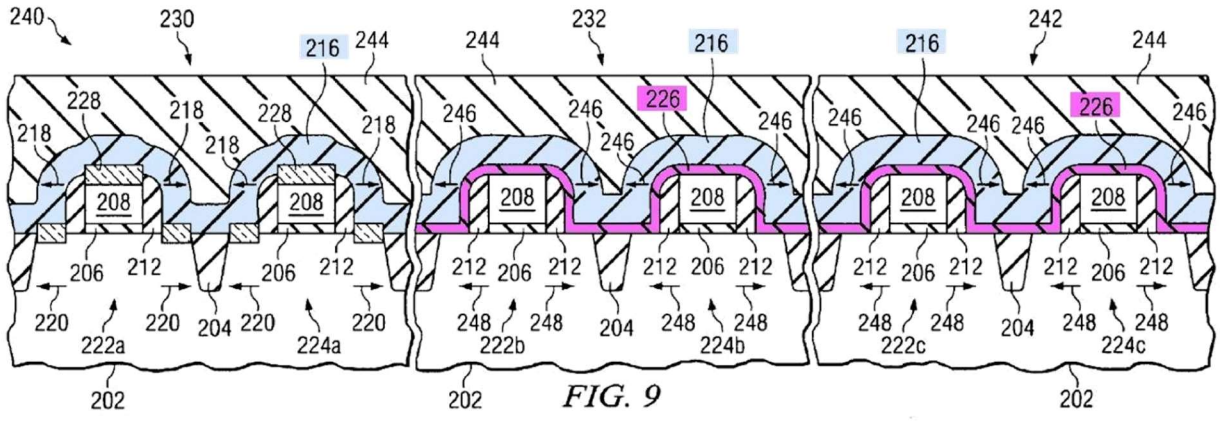


Miyashita's FIG. 1W

(d) Realization of the Wu-Alvarez combination

130. As explained above, a POSITA would have been motivated to add a stress-controlling layer (like Alvarez's layer 226/326/426 and/or 350/450) to Wu's FETs in certain circuit regions (like Alvarez's silicide region 330, non-silicide region 232/332, and stress-control region 242/342) to block silicide and/or mitigate tensile CESL stress on pFETs in a cost-effective way. *See* Alvarez ¶[0033], ¶[0037],

¶[0045], ¶¶[0063]-[0075], ¶[0078]. Alvarez's FIG. 9 below represents a "preferred embodiment . . . wherein a stress-controlling material [226] is disposed over some regions of a semiconductor device, but not over other regions of the semiconductor device." Alvarez ¶[0013].



Alvarez's FIG. 9
(annotated, showing stress-control layer 226 and stress-inducing layer 216)

131. As FIG. 9 shows, stress-controlling layer 226 blocks silicide formation and mitigates CESL stress in non-silicide region 232 and stress-control region 242 while allowing silicidation in silicide region 230. Alvarez ¶[0037]; *see also* Alvarez ¶¶[0045]-[0047], FIGS. 7-9. In silicide region 230, the tensile CESL 216 directly contacts the gate sidewalls of transistors 222a/224a in region 230, whereas in regions 232 and 242, stress-controlling layer 226 is used for "tuning" the stress applied to the FETs. *See* Alvarez ¶[0026], ¶[0049], ¶¶[0053]-[0055], ¶[0061], ¶[0081], Tbl. 1, FIG. 9.

132. Wu's FIG. 14 below shows an nFET on the left and a pFET on the right. Wu ¶[0017], ¶[0038], FIG. 14. It also shows "a [contact etch stop layer] CESL 66

on the surface of the gate structures 36A [PMOS], 36B [NMOS], the second spacers 512A [PMOS], 512B [NMOS], and the sources/drains 64A [PMOS], 64B [NMOS]." Wu ¶[0044]. CESL 66 is "a strained silicon material, i.e. silicon nitride." Wu ¶[0025].

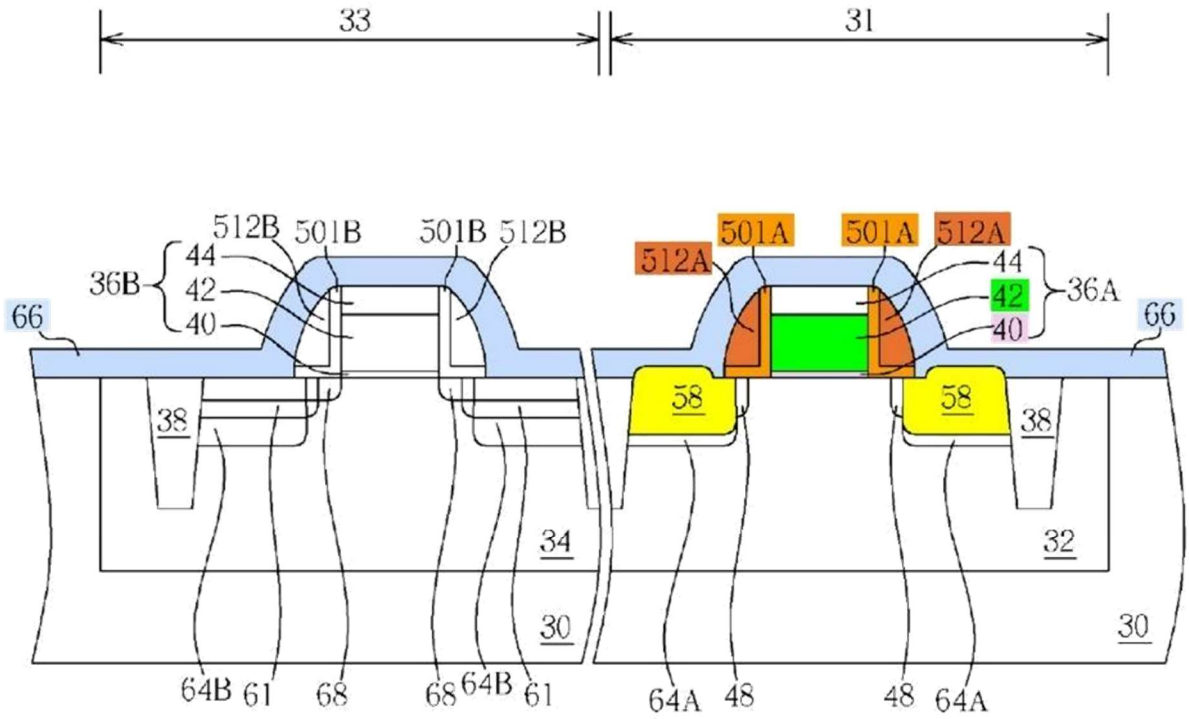


FIG. 14

Wu's FIG. 14 (annotated)

133. Composite Figure A below shows one example of how the Wu-Alvarez combination would have looked. Consistent with Alvarez's disclosures, and for all the reasons noted above, a POSITA would have found it obvious to deposit a stress-controlling layer (like Alvarez's layer 226/236/426 and/or 350/450) just before forming CESL 66 (which would be tensile, like Alvarez's layer 216/316/416). For reasons I also explain above, such a stress-controlling layer would lie beneath

CESL 66 and form in or fill the space between Wu's epitaxial source/drain regions 58 and gate sidewall spacers 501A/512A. Figure A shows how devices would appear in the equivalent of what Alvarez calls stress-control region 242 (also referred to as third region 242).[11] A similar structure would appear in what Alvarez calls non-silicide region 232 (also referred to as second region 232).

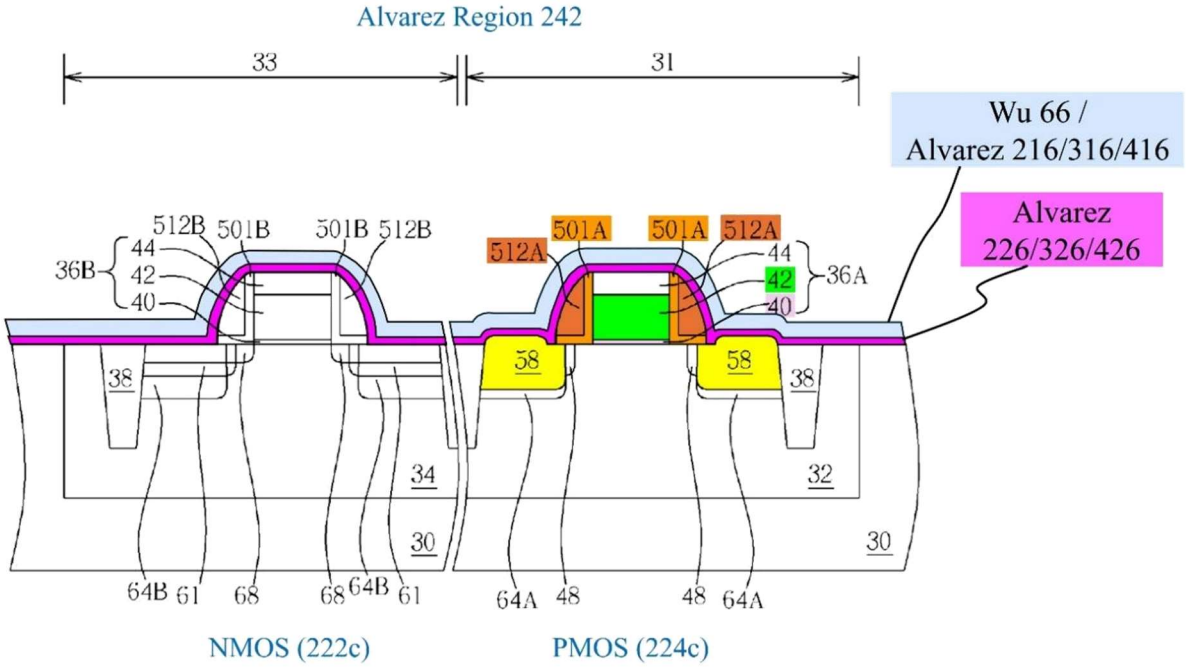


Figure A

134. Composite Figure B below shows an example of how this embodiment of the Wu-Alvarez combination might appear in all the circuit regions described in Alvarez's FIG. 9.

[11] To maximize the beneficial stresses for both nFETs and pFETs, Alvarez's stress-control layer may be removed from nFETs. *See* Alvarez ¶¶[0065]-[0068], FIG. 11. Such embodiments of the Wu-Alvarez combination also would have been obvious.

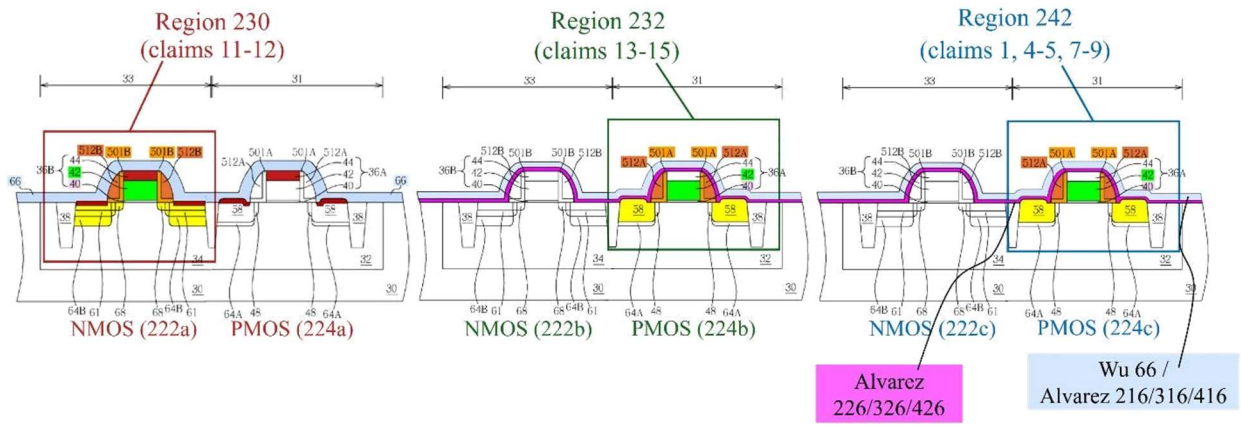
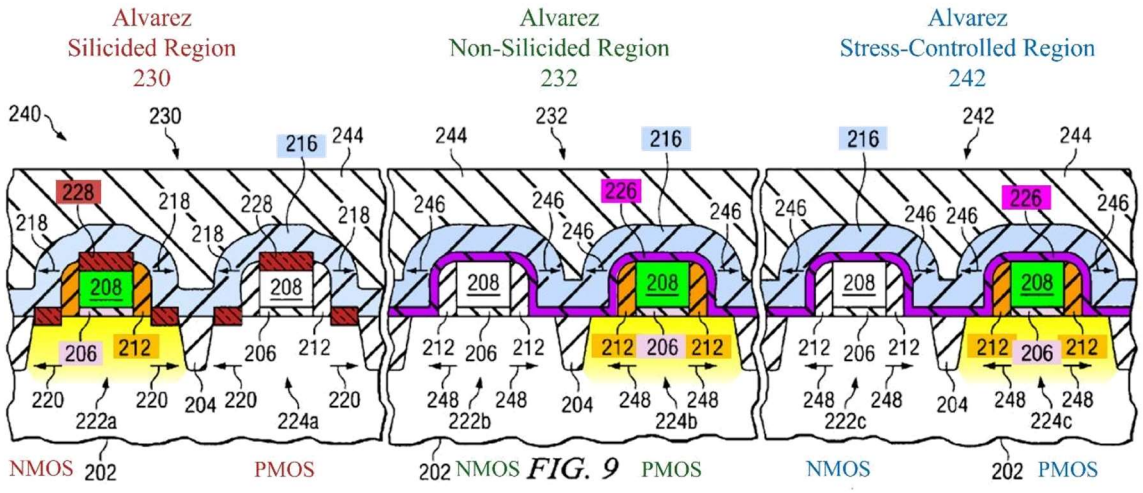


Figure B



Alvarez's FIG. 9 (annotated)

135. In this declaration, I discuss the Wu-Alvarez combination for claims 1, 3-5, 7-9, and 11-15. For ease of understanding, the list below and the annotations at the top of Figure B above explain the relevance of each circuit region to the claims:

- **Claims 1, 4, 5, and 7-9** map to Figure A's exemplary implementation of pFET 224c in Alvarez's stress-control region 242, as Figure B shows above (also shown in Figure A above). *See* Section IX.B.1.b below.

- **Claims 1 and 3** alternatively map to the exemplary implementation of pFET 324a in Alvarez's silicide region 330, as Figure A' shows in the section below where I discuss claim 3 (similar to Figure A above, but with Wu's optional silicide added). *See* Section IX.B.1.c below.
- **Claims 11-12** map to nFET 222a in silicide region 230 of Figure B above. Alternatively, claim 11 maps to nFET 222c in stress-control region 242 of Figure B above (also shown in Figure A above). *See* Section IX.B.1.i below.
- **Claims 13-15** map to pFET 224b in non-silicide region 232 of Figure B above, which is like pFET 224c shown in Figure A above. *See* Section IX.B.1.k below.

136. Compared to an approach that employs a tensile CESL over nFETs and a compressive CESL over pFETs, a POSITA would have recognized that a combination of Wu and Alvarez like the one described above—which uses a single tensile CESL over both nFETs and pFETs—reduces "stress mismatch" by eliminating "the lateral interface" between the tensile and compressive CESLs. Alvarez ¶[0033], ¶[0074]. Alvarez teaches that it is less "costly and time-consuming." Alvarez ¶[0033].

137. As I explain in greater detail above, a POSITA also would have found a combination like the one in Figure A advantageous because it provides a cost-

effective way to satisfy different performance requirements in different circuit regions, e.g., by tuning stress to enhance both nFET and pFET mobility and selectively blocking silicide in certain regions. Alvarez ¶[0027], ¶¶[0032]-[0033], ¶[0037], ¶¶[0053]-[0055], ¶[0074]; *see also* Morin, 355-56 (explaining that it "is important to work to improve the nMOS transistors since other solutions . . . can enhance the pMOS performances"); Hsu823 ¶[0039] ("[T]he performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve . . . ."); Bohr683 ¶¶[0038]-[0039], FIG. 6.

138. Although the discussions above generally describe mitigating the adverse effects of a tensile CESL on pFETs, Wu and Alvarez also disclose and render obvious the analogous situation where the roles are reversed: mitigating the adverse effects of a compressive CESL by using a stress-controlling layer when epitaxial SiC source/drain regions are present in the nFETs. *See* Alvarez ¶[0065], ¶[0067]; Wu ¶[0037], ¶[0057]. I discuss this in the context of claim 9 below. *See* Section IX.B.1.h below.

(2) A POSITA would have reasonably expected to succeed in combining Wu and Alvarez

139. As I explain above in Section IX.B.1.a(1), a POSITA would have been motivated to (1) add a stress-controlling layer (like Alvarez's layer 226/326/426 and/or 350/450) to Wu's FETs and (2) make Wu's CESL 66 tensile (like Alvarez's

layer 216/316/416). In my opinion, a POSITA would have reasonably expected to succeed in doing so.

140. The embodiments of the Wu-Alvarez combination shown in Figures A and B above would have required nothing more than the conventional steps of (1) forming a layer (like Alvarez's layer 226/326/426 and/or 350/450) in the desired circuit regions (*see* Alvarez ¶[0027], ¶[0032], ¶[0035], ¶[0045], ¶¶[0063]-[0068], ¶[0074], ¶[0078], FIGS. 7-11); and (2) depositing Wu's silicon nitride CESL 66 under conditions that would make it tensile (like Alvarez's layer 216/316/416) (*see* Jung ¶[0090], ¶¶[0099]-[0100], Tbl. V). Both of these steps were conventional and well known. *See* Sections VI.B and VI.C above.

141. A POSITA also would have understood how to mask certain circuit regions (like Alvarez's silicide region 230) to prevent deposition of a stress-controlling film in those areas while allowing it to deposit in other circuit regions (like Alvarez's non-silicide region 232 and stress-control region 242). *See* Alvarez ¶[0044], ¶¶[0052]-[0053], ¶¶[0063]-[0068]. Alvarez, Murthy556, and Miyashita, for example, confirm that the stress-controlling layer would form in the space between the facets of Wu's SiGe source/drain regions 58 and gate sidewalls 501A/512A because of the manner in which the stress-controlling layer would be blanketed over the pFETs in the exposed circuit regions. *See* Section IX.B.1.a(1)(c) above; Wu ¶[0042], FIGS. 7, 14; Alvarez ¶¶[0043]-[0049], ¶[0052], ¶¶[0063]-[0068], ¶¶[0070]-

[0071], ¶¶[0073]-[0075], ¶[0078], FIGS. 6-11; Murthy556, 9:10-29, FIG. 8; Miyashita ¶¶[0052]-[0053], FIGS. 1U-1W.

142. A POSITA would have recognized that depositing a stress-controlling layer (like Alvarez's layer 226/326/426 and/or 350/450) just before depositing a tensile CESL 66 (like Alvarez's layer 216/316/416) would have involved nothing more than a conventional deposition process (e.g., SiO_2 deposition). *See* Alvarez ¶[0026], ¶[0033], ¶[0037], ¶¶[0043]-[0049], ¶¶[0053]-[0055], ¶¶[0063]-[0068], ¶¶[0070]-[0071], ¶¶[0073]-[0075], ¶[0078], FIGS. 6-11 (depositing oxide stress-controlling layer 226/326/426 and/or 350/450 just before depositing a tensile silicon nitride layer 216/316/416); Murthy556, 9:10-29, FIG. 8 (same).

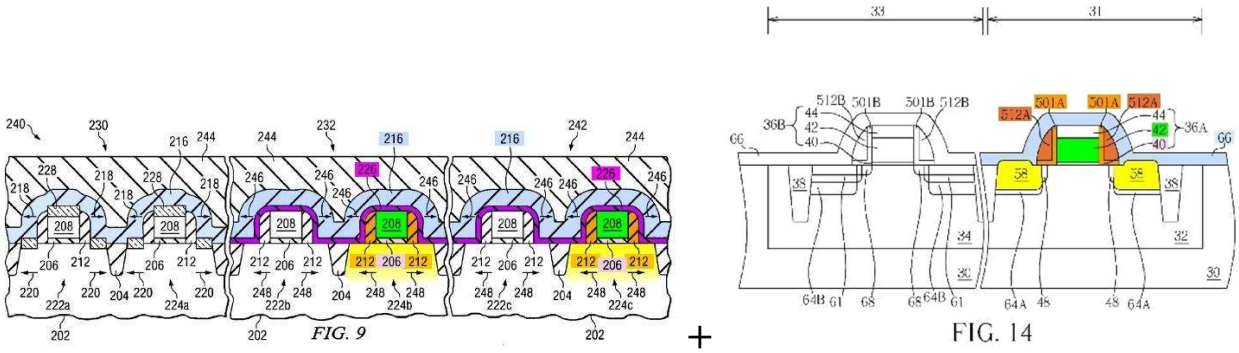
143. Wu's CESL 66 is made of a "strained silicon material, i.e. silicon nitride." Wu ¶[0025]. Depositing a tensile silicon nitride CESL also would have involved nothing more than applying a conventional, well-known deposition process. *See* Section VI.B above; Jung ¶[0090], ¶¶[0099]-[0100], Tbl. V; Alvarez ¶[0047]; Wu ¶[0005]; Doris ¶¶[0016]-[0017], ¶¶[0029]-[0030], ¶[0038], ¶[0042], ¶[0051], Figs. 1, 2, 14, 15; James, 2, 5, Fig. 6; Morin, 355-56; Hsu823 ¶[0003]; Ke ¶[0003] (explaining that "applying stress to the channel region [by] forming a stressed contact etch stop layer (CESL) on a MOS device" was "commonly used" to "introduce stress into the channel region" and improve carrier mobility). A POSITA also would have been aware of such processes and therefore would have reasonably

expected to succeed in making Wu's CESL 66 tensile. In fact, this approach was already known and used ubiquitously in commercial devices to achieve similar benefits. *See* Section VI.B above; James, 2, 5, Fig. 6.

144. A POSITA also would have known how to use a stress buffer layer to mitigate the effects of a tensile CESL on pFETs. Alvarez explains, for example, that stress-controlling layer 226 "controls, screens, or limits the effect of the stress of the second material 216 on the channel regions of the transistors 222b, 224b, 222c, and 224c." Alvarez ¶[0050]; *see also* Alvarez, FIGS. 9-11. Further, Alvarez explains that "[t]he stress-controlling material 226 reduces the amount that the stress-increasing material 216 increases the first amount of stress by about the second amount of stress 218 less the third amount of stress 246, for example." Alvarez ¶[0049]; *see also* Murthy556, 9:10-29 ("Oxide layer 322 buffers the large stress inherent silicon nitride layer 324 and provides an etch step for silicon nitride layer 324 during a subsequent spacer etch."), FIG. 8; Doris ¶[0042] ("The stress level along with the thickness of the film also defines a neutral buffer layer between the compressive spacer and the tensile etch stop layer."), Figs. 14, 15; Lee ¶[0029], ¶¶[0046]-[0067] (explaining that an intermediate stress relief layer "with neutral stress or opposite stress relative to the [CESL]" reduces or eliminates any pFET performance degradation because it "reduces the tensile stress in the channel region"), FIGS. 2-5; Cheng810 ¶¶[0022]-[0031], Figs. 1B-1F (describing similar). A POSITA would

have reasonably expected the same effects to obtain when placing a stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 underneath Wu's CESL 66.

145. As I explain above in Section IX.B.1.a(1)(d), I conclude that a POSITA would have found it obvious to deposit a stress-controlling layer (like Alvarez's layer 226/326/426 and/or 350/450) immediately before depositing Wu's CESL 66 as a tensile film (like Alvarez's layer 216/316/416). I illustrate this below in Figure A.



Alvarez's FIG. 9 (annotated) + **Wu's FIG. 14 (annotated)**

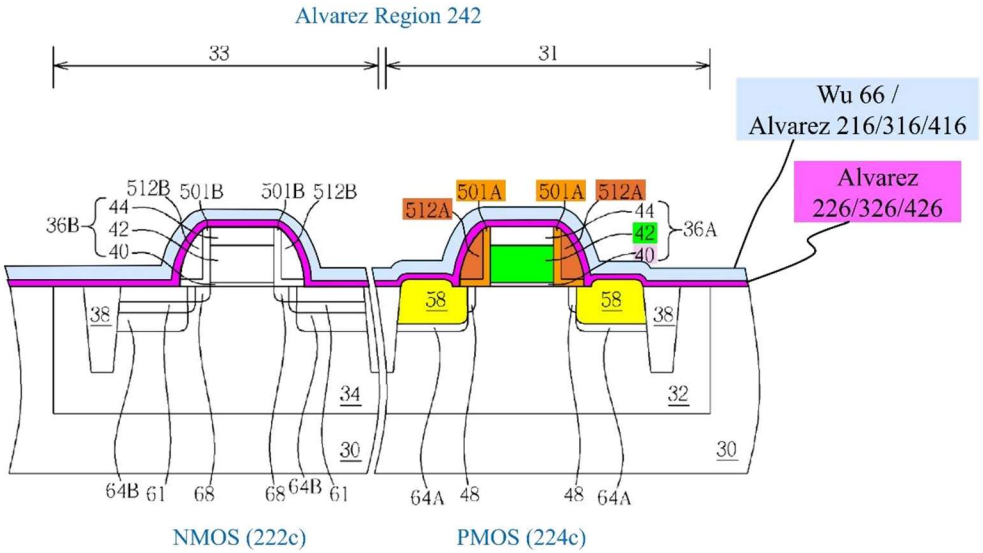


Figure A

146. A POSITA would have reasonably expected to succeed in depositing a stress-controlling film (e.g., silicon oxide) in the space between the facets of Wu's epitaxial SiGe layer 58 and gate sidewalls 501A/512A before applying a tensile CESL 66 because this would have been expected to achieve the ordinary and expected benefits I explain in Sections VI.B, VI.C, and IX.B.1.a(1) above, including (i) reducing the adverse effects from a tensile CESL 66 on pFETs by controlling the stress; (ii) selectively blocking unwanted silicide formation in certain circuit regions (regions like Alvarez's non-silicide region 232/332 and stress-control region 242/342); and (iii) keeping manufacturing costs low. *See* Alvarez ¶[0037], ¶[0043], ¶[0049], ¶[0061], ¶¶[0063]-[0064], ¶¶[0069]-[0075], ¶[0078], ¶[0081], FIGS. 9-13.

(3) Summary of the Wu-Alvarez combination

147. To summarize briefly, it is my opinion that a POSITA would have found the Wu-Alvarez combination obvious for at least the following reasons:

- It combines known prior art elements (e.g., Wu's MOSFET structures with Alvarez's teachings to use a tensile CESL and intermediate stress-controlling layer) according to known methods (silicon oxide deposition followed by tensile silicon nitride deposition) to yield predictable results (a tensile CESL over both nFETs and pFETs with a buffer oxide to tune the stress and inhibit silicide formation in certain circuit regions).

- It uses known techniques (e.g., depositing a stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 and then depositing a tensile CESL like Alvarez's layer 216/316/416) to improve similar devices (Wu's FETs) in the same way as known in the prior art (e.g., by selectively blocking silicide formation in certain circuit regions, improving nFET and pFET carrier mobility through stress tuning, and keeping manufacturing costs low).
- It applies known techniques (e.g., depositing a stress-controlling layer like Alvarez's layer 226/326/426 and/or 350/450 and then depositing a tensile CESL like Alvarez's layer 216/316/416) to a known device that is ready for improvement (Wu's FETs) to yield predictable results (matching different performance requirements in different circuit regions by adjusting nFET and pFET carrier mobility via stress tuning and selectively blocking silicide formation).
- It applies a known teaching, motivation, or suggestion in the prior art (e.g., Alvarez's teaching, motivation, and suggestion to use a tensile CESL (like layer 216/316/416) and a stress-controlling layer (like layer 226/326/426 and/or 350/450) to tune nFET and pFET stresses and selectively block silicide formation in a cost-

effective manner) that would have led a POSITA to modify Wu according to, or to combine Wu with, the teachings of Alvarez to arrive at the claimed invention. *See* Sections VI.B, VI.C, and IX.B.1.a(1) above; Alvarez ¶[0047], ¶¶[0053]-[0055], ¶[0065], Tbl. 1, FIG. 9; Murthy556, 5:55-57; Doris ¶[0005], ¶[0008], ¶[0042]; Lee ¶[0029], ¶¶[0046]-[0067], FIGS. 2-5; Cheng810 ¶¶[0022]-[0031], Figs. 1B-1F.

b. Independent Claim 1

148. In my opinion, the Wu-Alvarez combination renders claim 1 obvious.

(1) [1Pre]: "A semiconductor device"

149. Wu discloses "a strained CMOS transistor." Wu ¶[0009], FIGS. 1-7, 9-14. Wu's semiconductor device includes a first active region 31, which may be a "PMOS transistor region 31," and a second active region 33, which may be an "NMOS transistor region 33." Wu ¶[0017], ¶¶[0023]-[0024], ¶[0038], ¶¶[0042]-[0043], FIGS. 1-7, 9-14. Composite Figure A below, based on Wu's FIG. 14, shows an embodiment of the Wu-Alvarez combination as modified by Alvarez to include a tensile CESL (light blue) and stress-controlling layer (magenta).

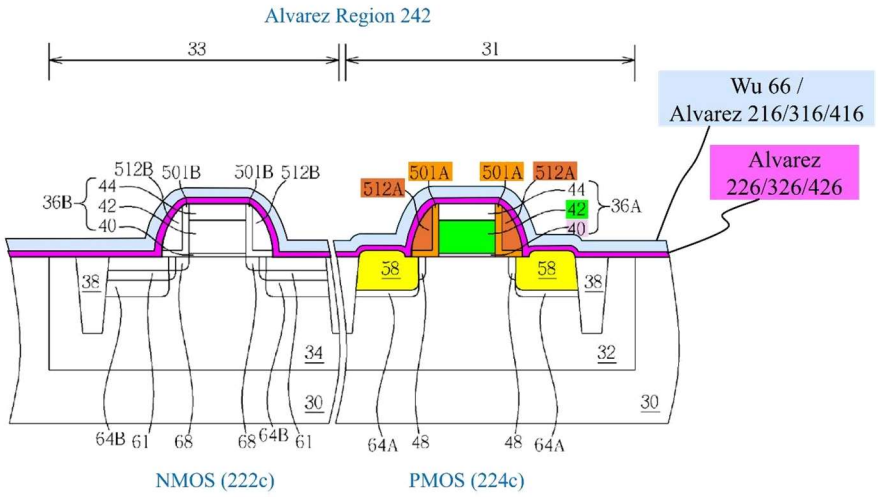


Figure A

150. Composite Figure A' below shows an alternative embodiment of the Wu-Alvarez combination, which I discuss in the context of claim 3. *See* Section IX.B.1.c below. The alternative embodiment shown in Figure A' is similar to Figure A above, but it further includes Wu's optional silicide layer (burgundy) formed on the source/drain regions and gate electrode. *See* Wu ¶[0024], ¶[0036], ¶[0043], ¶[0055], FIGS. 7, 14; Alvarez ¶¶[0063]-[0064], FIG. 10.

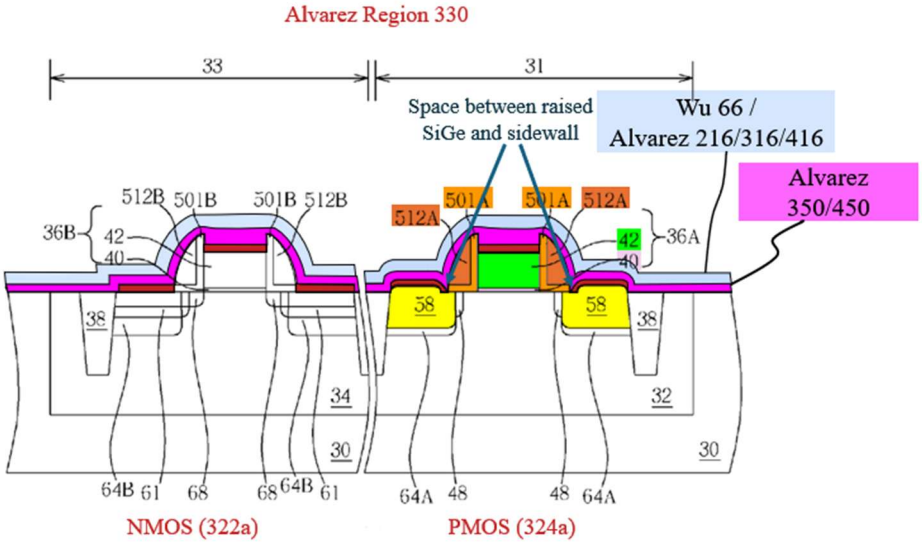


Figure A'

(2) [1A]: "a first MIS transistor . . . includ[ing]:"

151. In my opinion, the Wu-Alvarez combination, as shown in exemplary Figure A, satisfies the particular features of the first MIS transistor in element [1A], including the subsequent limitations of elements [1B]-[1J] discussed below.

152. Wu discloses a first MIS transistor, such as the pEFT in "PMOS transistor region 31." Wu ¶[0017], ¶[0023], ¶¶[0027]-[0036], ¶[0038], ¶¶[0042]-[0043], ¶¶[0046]-[0055], FIGS. 1-7, 9-14. Figure A below shows an exemplary first MIS transistor in PMOS region 31.

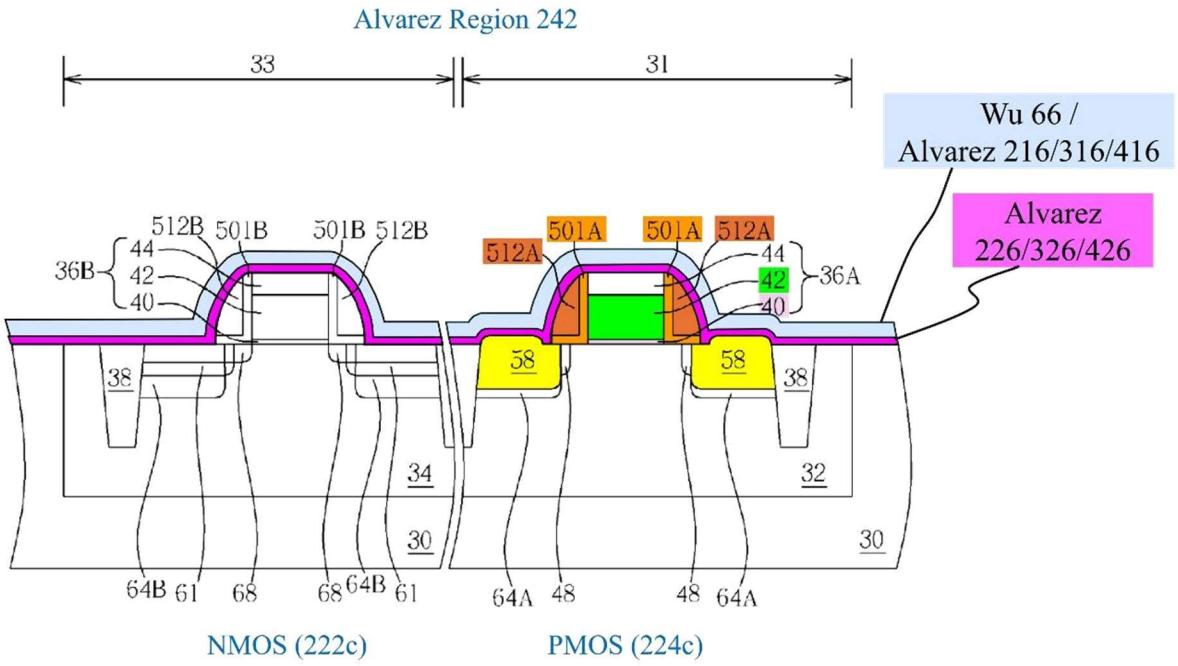


Figure A

(3) [1B]: "a first gate insulating film formed on a first active region in a semiconductor substrate"

153. Wu discloses a "gate dielectric layer 40" formed on the "first active area," e.g., "PMOS transistor region 31," of "semiconductor substrate 30." Wu

¶[0017] ("the first active area is a PMOS transistor region 31"), ¶¶[0038]-[0039] (describing "gate structures 36A, 36B"). Wu's gate dielectric layer 40 corresponds to a first gate insulating film because it is made of "dielectric materials," such as "silicon oxide," which are insulating. Wu ¶[0017]. This is the same "silicon oxide" material used for the "gate insulating film" in the '425 Patent. '425 Patent, 9:15-19. Excerpted Figure A below shows gate dielectric layer 40 (light purple) on PMOS active region 31 of substrate 30 in one embodiment of the Wu-Alvarez combination. *See* Wu ¶[0017], FIGS. 1-7, 9-14.

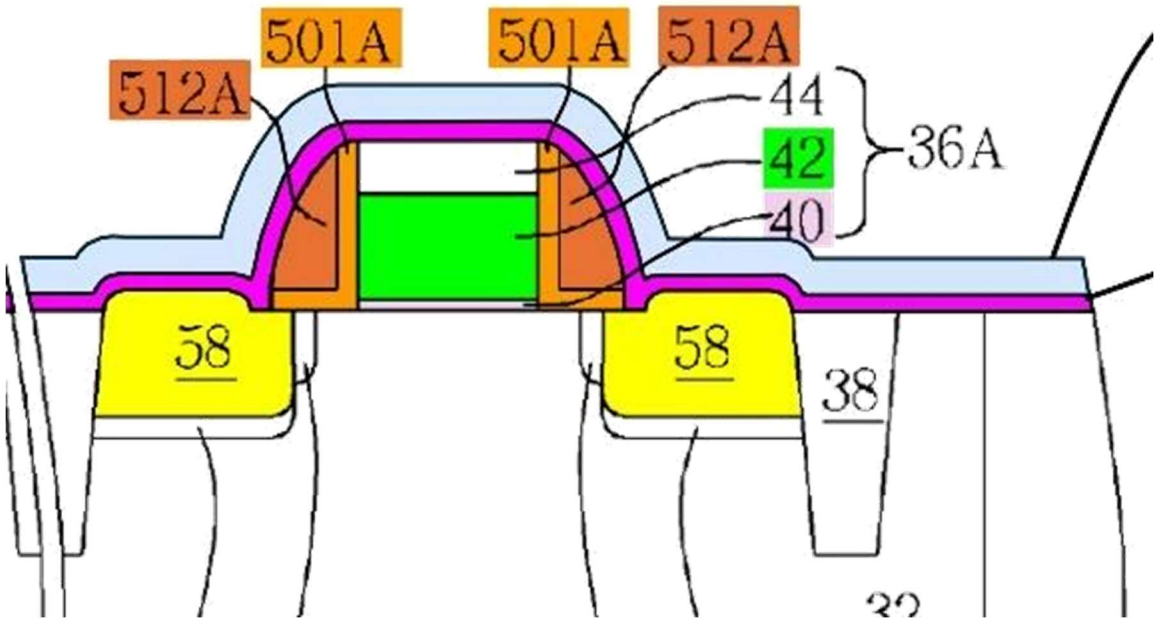


Figure A (excerpted)

(4) [1C]: "a first gate electrode formed on the first gate insulating film"

154. Wu discloses a first gate electrode ("gate 42") formed on the first gate insulating film ("gate dielectric layer 40"). Wu ¶[0017], FIGS. 7, 14.

155. A POSITA would have understood that Wu's gate 42 is a gate electrode made from polysilicon or other materials to permit "connections between the gate structures 36A, 36B . . . with other electrical devices." Wu ¶[0017], ¶[0025], ¶[0036], ¶[0055], FIGS. 1-7, 9-14. As Figure A shows below, gate electrode 42 in this embodiment of the Wu-Alvarez combination lies on the first gate insulating film (gate dielectric film 40), just as Wu's FIG. 14 shows.

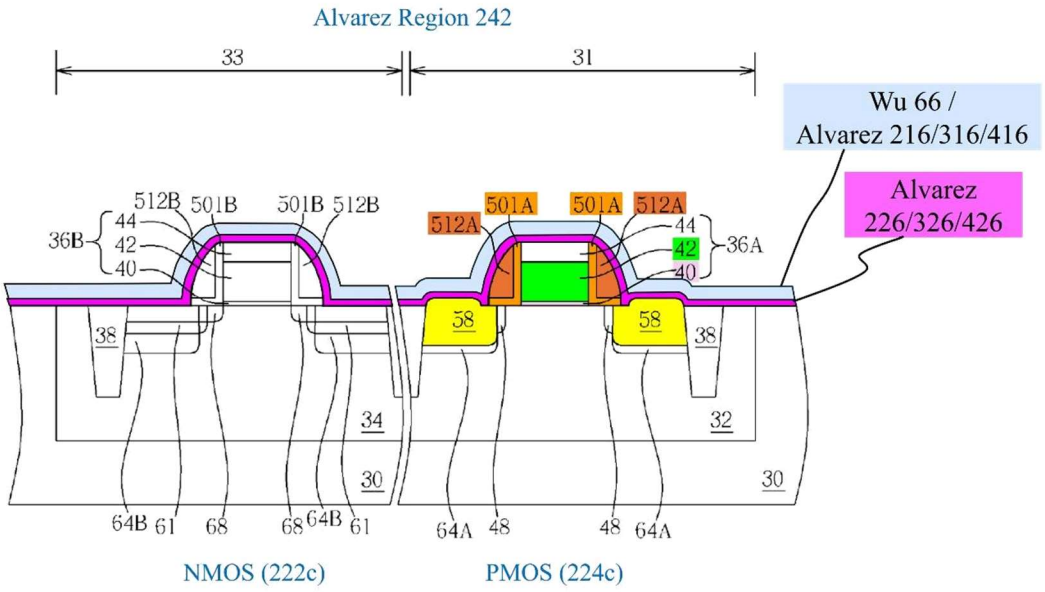


Figure A

(5) [1D]: "a first sidewall spacer formed on a side surface of the first gate electrode"

156. Wu discloses a first sidewall spacer comprising "oxide layer 501A" and optionally "second [sidewall] spacer 512A[12] . . . formed on the sidewalls of the gate structure[] 36A" of the pFET. Wu ¶[0017], ¶[0024], ¶[0043], FIGS. 7, 14.

[12] *See* note 13 below, Section IX.B.1.b(6).

157. Wu's FIGS. 7 and 14 show oxide layer 501A and sidewall spacer 512A, both of which sit on the sidewalls of pFET gate structure 36A. Wu ¶[0017], ¶[0024], FIGS. 7, 14. As Wu's FIG. 14 shows below, oxide layer 501A and optionally sidewall spacer 512A (the first sidewall spacer) are located on the side surfaces of gate electrode 42 in PMOS transistor region 31. In the embodiment of the Wu-Alvarez combination shown in Figure A below, the same is true.

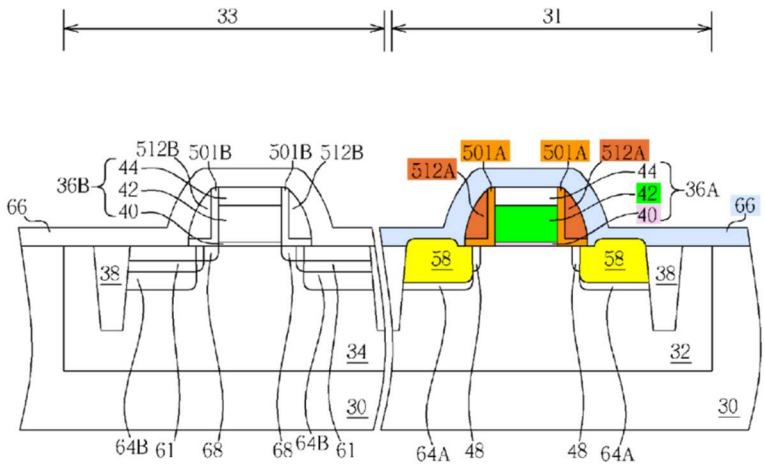


FIG. 14

Wu's FIG. 14 (annotated)

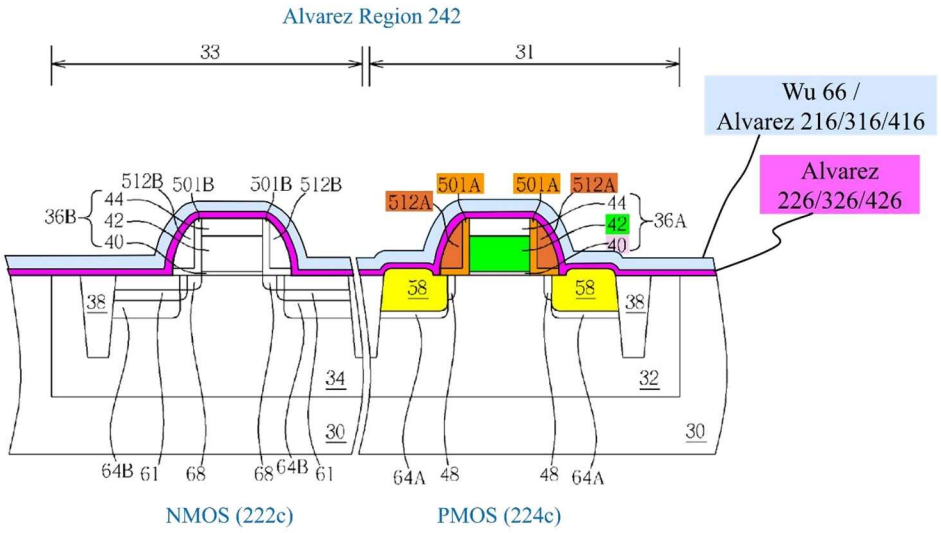


Figure A

(6) [1E]: "a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region"

158. Wu discloses a first source/drain region in the first active area ("PMOS transistor region 31") that includes "an epitaxial layer 58 of silicon germanium [SiGe]" and comprises a first conductivity type (p-type). Wu ¶[0019], ¶[0021], ¶[0041], FIGS. 7, 14. Wu's epitaxial SiGe is a silicon compound layer that causes a first, compressive stress in the gate length direction of the pFET channel region in PMOS transistor region 31.

159. Wu discloses that epitaxial SiGe layer 58 (the silicon compound layer) is formed in "a recess 56 [trench] . . . formed on the surface of the N well 32 beside the gate structure 36A." Wu ¶[0020], ¶[0031], ¶[0040], ¶[0050], FIGS. 3, 11. As Wu's FIGS. 11-14 illustrate, for example, recess 56 is located "beside the gate structure 36A" in the "first active area" of "PMOS transistor region 31" on a lateral side of the first sidewall spacer comprising oxide layer 501A and optionally sidewall spacer 512A.[13] Wu ¶[0017], ¶[0020], ¶[0031], ¶[0040], ¶[0050], FIGS. 3-7, 11-14.

[13] Wu's epitaxial SiGe layer 58 is actually formed in recess 56 before the sidewall spacer 512A exists. To the extent it may be determined that the "first sidewall spacer" does not need to exist when the first source/drain region is actually formed, then the claimed "first sidewall spacer" may include Wu's spacer 512A. *See* Wu ¶¶[0024]-[0025], ¶¶[0043]-[0044].

As Wu explains, the "preferred epitaxial [SiGe] layer 58 has a lattice constant greater than that of the semiconductor substrate 30," and the SiGe "compress[es] the channel" (causes compressive stress (first stress) in the channel direction of the channel region) of the pFET as a result. Wu ¶[0021], ¶[0041] ("The preferred epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30, and is extended approaching to the channel. In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30."), FIGS. 7, 14. As I explain in Section VI.B, such compressive stress is the fundamental purpose of growing epitaxial SiGe source/drain regions.

160. Wu's FIG. 14, annotated below, shows epitaxial SiGe layers 58 in yellow. The embodiment of the Wu-Alvarez combination shown in Figure A below likewise includes such epitaxial SiGe source/drain layers 58.

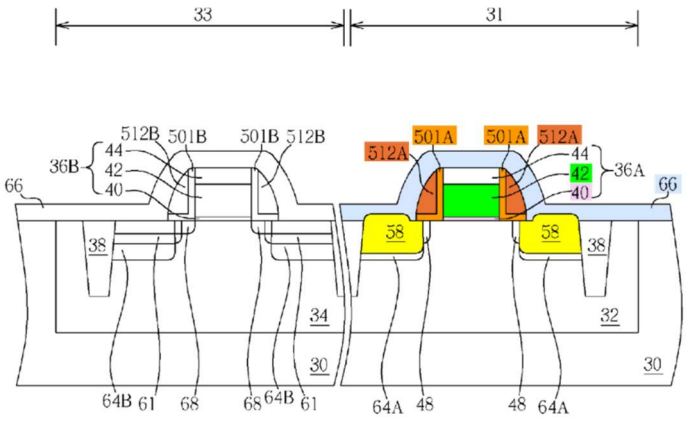


FIG. 14

Wu's FIG. 14 (annotated)

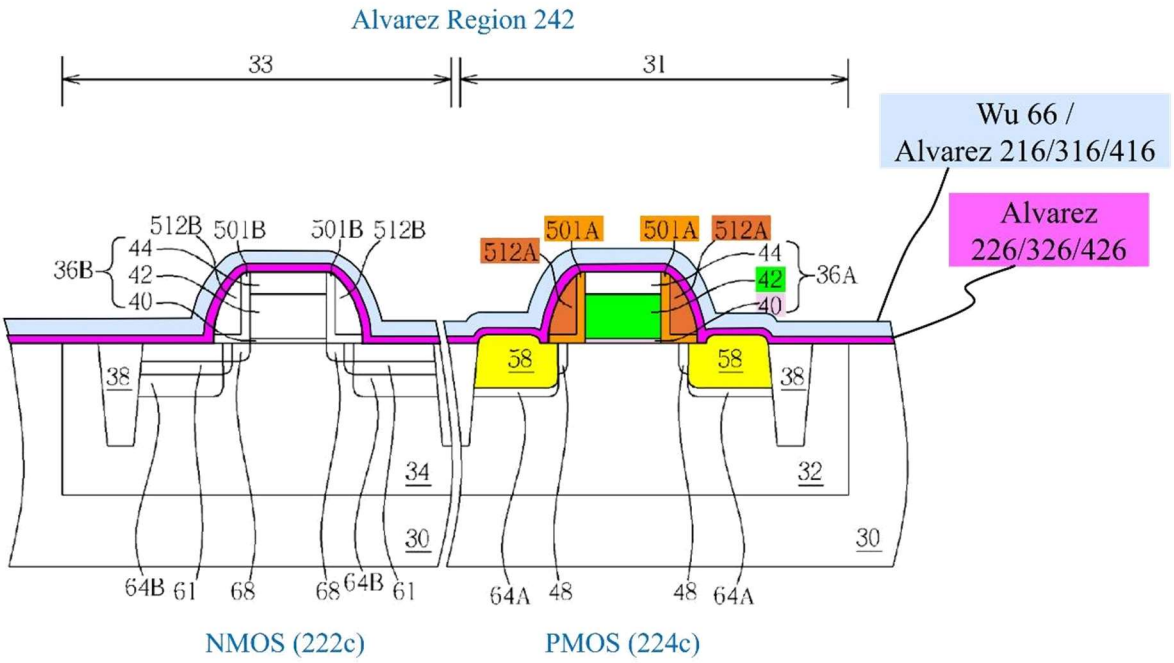


Figure A

(7) [1F]: "a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress"

161. Wu discloses a stress insulating film (CESL 66) formed over the first active region (PMOS transistor region 31). Wu ¶[0025], ¶[0044], FIGS. 7, 14. Wu discloses "deposit[ing] . . . a contact etch stop layer (CESL) 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B." Wu ¶[0025], ¶[0044]. Wu explains that "CESL 66 may include . . . a strained silicon material, i.e. silicon nitride." Wu ¶[0025]. Because Wu discloses depositing CESL 66 (shown below in blue) over "gate structures 36A, 36B" and

"[sidewall] spacers 512A, 512B," it also discloses depositing CESL 66 over oxide sidewalls 501A and 501B located between gate structures 36A and 36B, as well as sidewall spacers 512A and 512B. *See* Wu, ¶[0025], ¶[0044], FIGS. 7, 14 (annotated below).

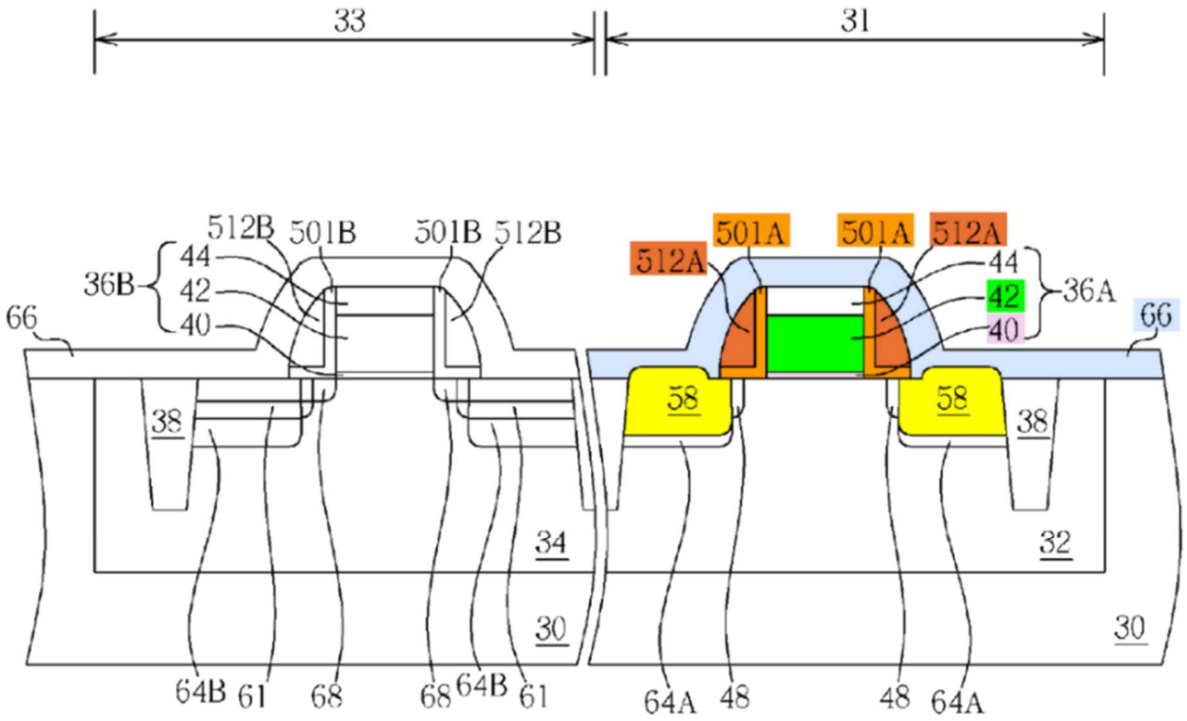


FIG. 14

Wu's FIG. 14 (annotated)

162. Although Wu describes CESL 66 as "strained," it does not specify whether the strain is tensile or compressive. As I explain above, a POSITA would have found it obvious to make Wu's CESL 66 tensile (like Alvarez's stress-inducing layer 216/316/416). *See* Sections VI.B and IX.B.1.a above; Alvarez ¶[0065] (explaining that "stress-increasing material 416 comprises tensile stress"), Tbl. 1.

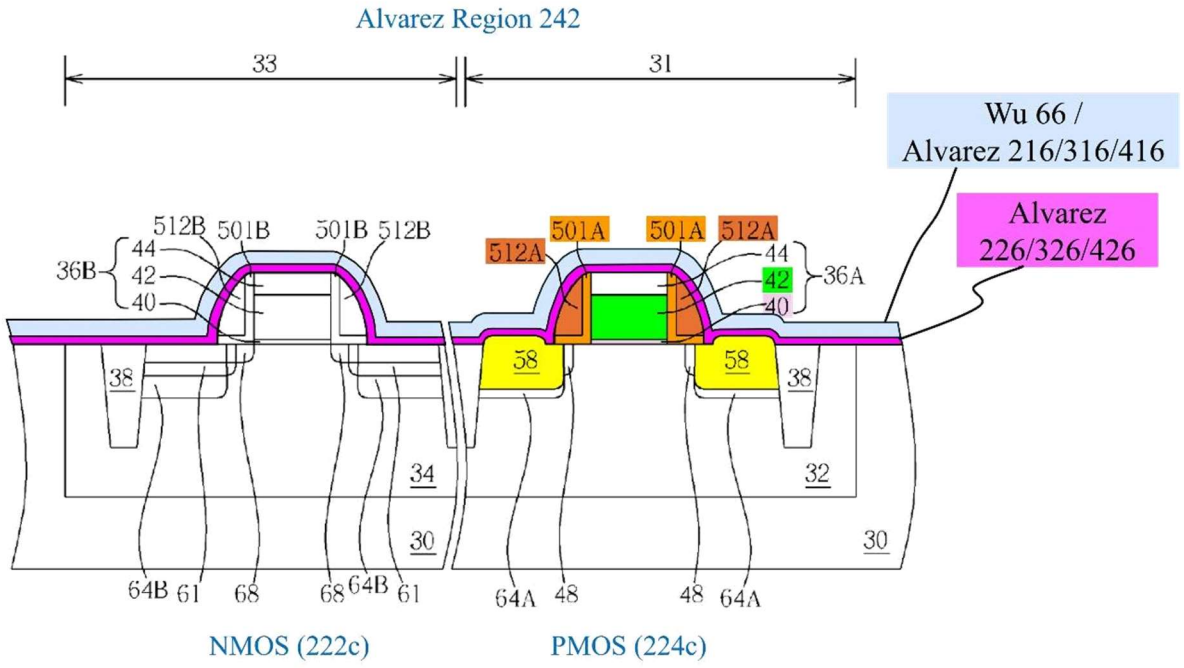


Figure A

163. For the reasons I discuss in Section IX.B.1.a above, it is my opinion that a POSITA would have found it obvious to make Wu's CESL 66 tensile. As with CESL 66 in Wu's FIG. 14, and, as the embodiment of the Wu-Alvarez combination shown in Figure A above indicates, the tensile CESL 66 in the Wu-Alvarez combination extends over the first gate electrode (gate 42), the first sidewall spacer (oxide layer 501A and optionally sidewall spacer 512A[14]), and the first source/drain region (epitaxial SiGe layer 58). Because it is tensile, CESL 66 in the Wu-Alvarez combination would exert a second stress (tensile) that is opposite the first stress (compressive) caused by the epitaxial SiGe source/drain regions.

[14] *See* note 13 above, Section IX.B.1.b(6).

(8) [1G]: "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode"

164. Wu discloses that the uppermost surface of epitaxial SiGe layer 58 (silicon compound layer) extends above the surface of semiconductor substrate 30, as Wu's FIGS. 4-7 and 12-14 show. *See* Wu ¶[0021], ¶[0041]. Wu explains that "epitaxial [SiGe] layer 58 is slightly projected from the top surface of the semiconductor substrate 30 to compress the channel and to keep silicon layers formed in the following steps from the interface between the source/drain in a distance." Wu ¶[0021]; *see also* Wu ¶[0041] ("In order to compress the channel and to keep the silicon layer formed in the following steps from the interface between the source/drain in a distance, the preferred epitaxial layer 58 is slightly projected from the top surface of the semiconductor substrate 30."), FIGS. 7, 14. A POSITA would have readily understood that Wu's descriptions refer to the same kind of raised epitaxial SiGe layers that were well known in the art. *See* Section IX.B.1.a above.

165. As Wu's FIGS. 4-7 and 12-14 show, the top surface of epitaxial SiGe layer 58 (red dashed line) is higher than the top surface of substrate 30 under gate 42 (blue dashed line). *See* Wu ¶[0021], ¶[0041], FIGS. 4-7, 12-14. The embodiment of the Wu-Alvarez combination shown in Figure A, shown below, retains this feature.

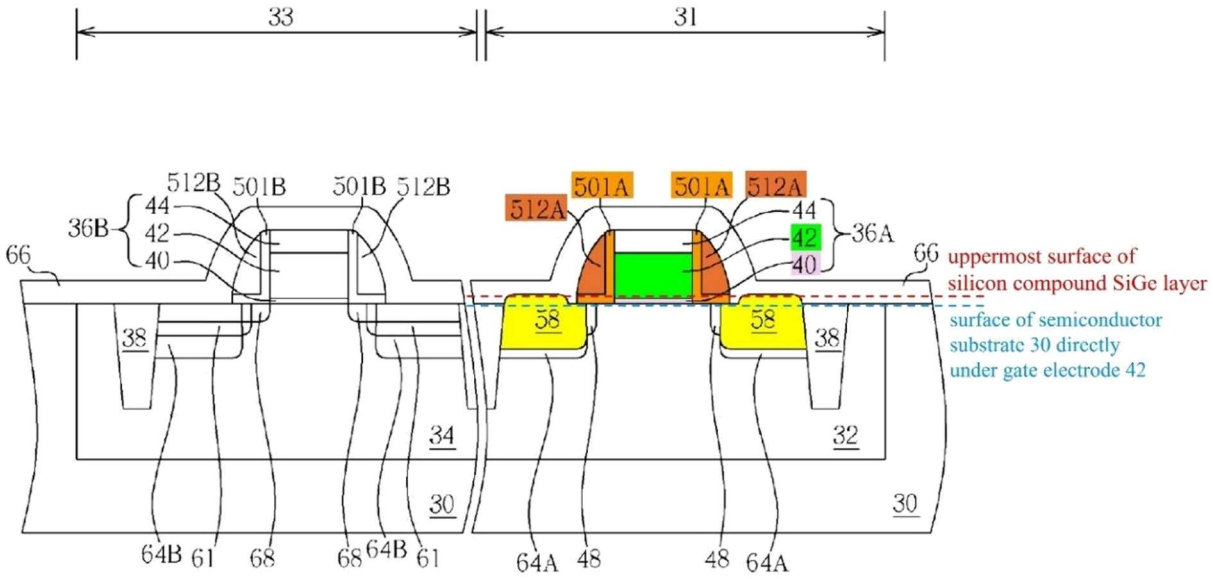


FIG. 14

Wu's FIG. 14 (annotated)

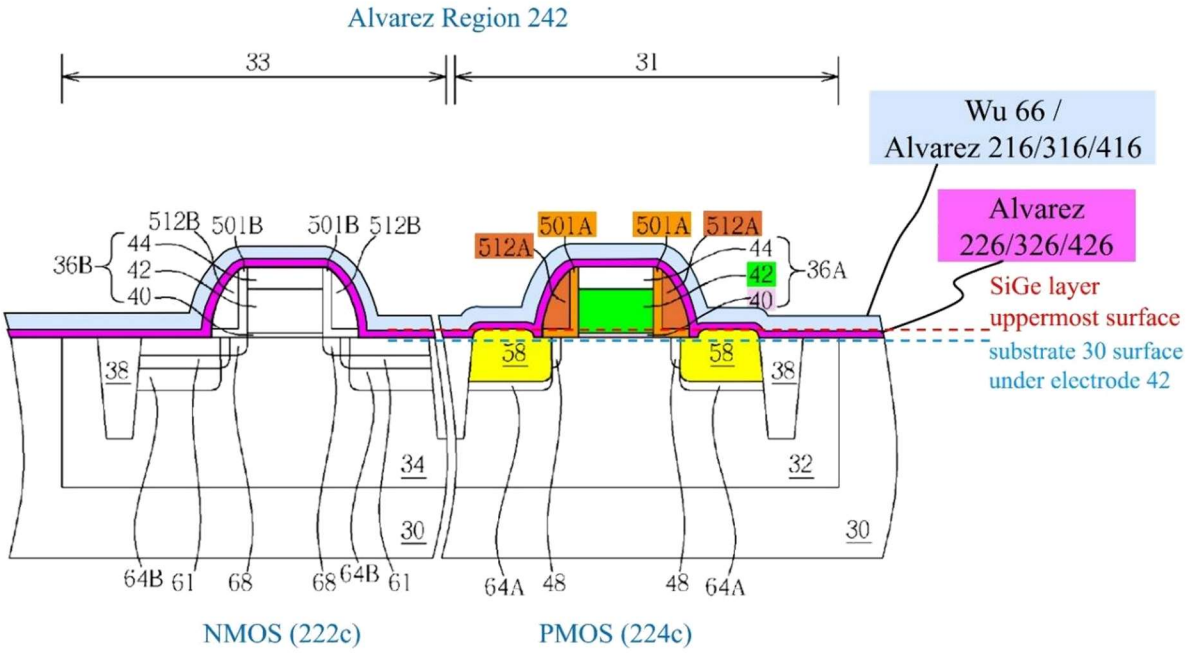


Figure A (further annotated)

(9) [1H]: "a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer"

166. As I explain in Section IX.B.1.a above, the Wu-Alvarez combination includes a first stress-relief film formed in a space between epitaxial SiGe layer 58 and the first sidewall spacer (spacer 501A and optionally 512A).[15] A POSITA would have understood that, when a stress-controlling layer (magenta) like Alvarez's layer 226/326/426 is deposited over Wu's PMOS transistor region 31, it would have formed in the space between raised SiGe layer 58 (yellow) and sidewall spacer layers 501A (light orange) and 512A (dark orange), as Wu's FIG. 14 and Figure A demonstrate below. *See* Sections VI.C and IX.B.1.a above; Wu, FIGS. 7, 14.

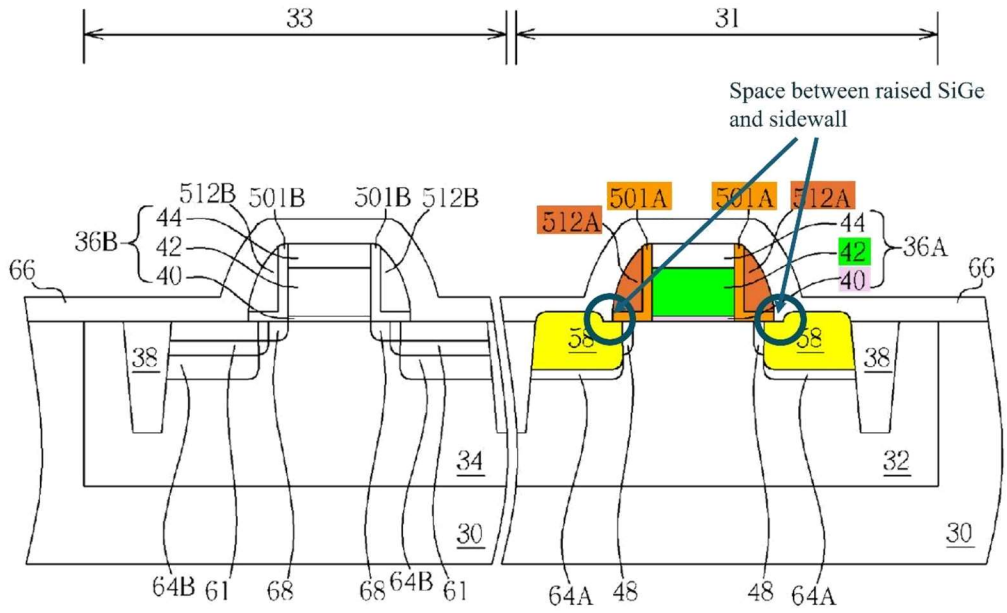


FIG. 14

Wu's FIG. 14 (annotated)

[15] *See* note 13 above, Section IX.B.1.b(6).

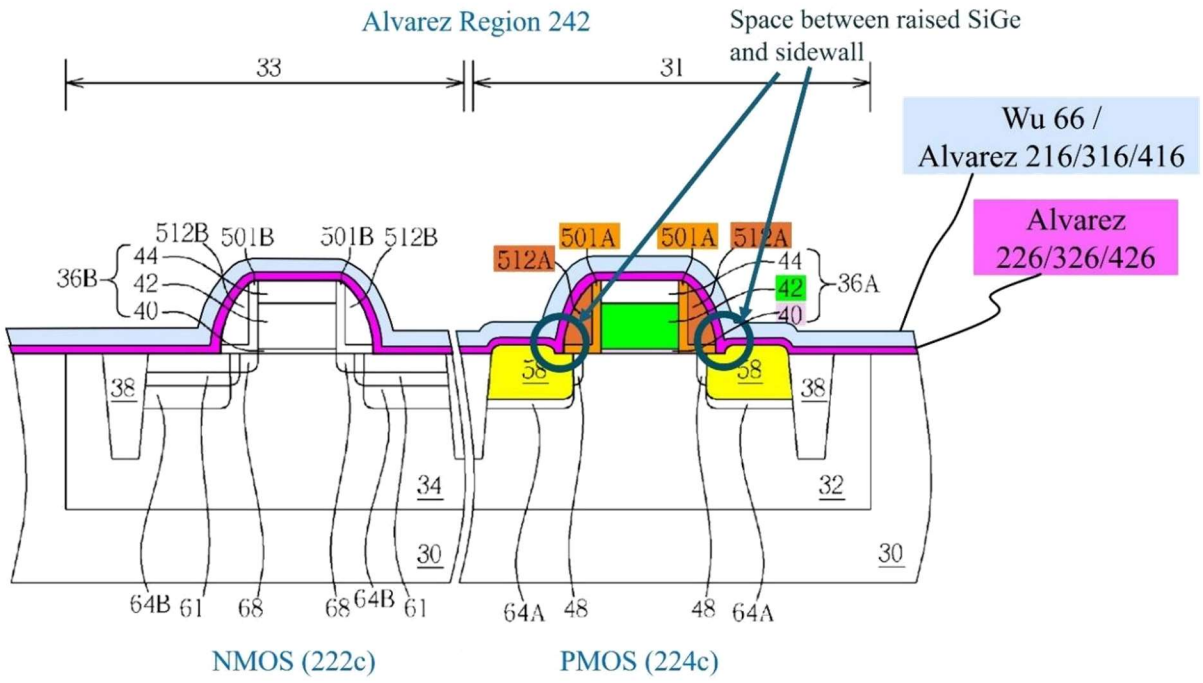


Figure A (further annotated)

(10) [1I]: "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween"

167. As I explain above for the Wu-Alvarez combination, the first stress-relief film (a stress-controlling film like Alvarez's layer 226/326/426) is formed on the side surface of the first gate electrode (gate 42) of the pFET with the first sidewall spacer layer (spacer 501A and optionally 512A) interposed therebetween. *See* Section IX.B.1.a above. The embodiment of the Wu-Alvarez combination shown in Figure A above demonstrates this.

168. Like stress-controlling film 226/326/426 in Alvarez's FIG. 9, a POSITA would have understood that the stress-controlling film in the Wu-Alvarez combination (magenta above) would blanket Wu's pFETs in circuit regions like

Alvarez's stress-control region 242. *See* Section IX.B.1.a above. Accordingly, a POSITA would have understood that the stress-controlling layer (magenta) forms on the side surfaces of gate 42 (green), including in the space between the first sidewall spacer layer (spacer 501A (light orange) and optionally 512A (dark orange)) and epitaxial SiGe layer 58 (yellow). *See* Sections VI.C and IX.B.1.a above. As Figure A shows above, the first sidewall spacer layer (orange) is interposed between the stress-relief film (magenta) and the first gate electrode (green). *See also* Sections VI.C and IX.B.1.a above.

(11) [1J]: "the first stress-relief film is not in direct contact with the side surface of the first gate electrode"

169. As I explain above for elements [1H] and [1I] and in Section IX.B.1.a, the first stress-relief film of the Wu-Alvarez combination (akin to Alvarez's stress-controlling film 226/326/426 (magenta)) does not directly contact the side surface of the first gate electrode (gate 42 (green)) because the first sidewall spacer layer (oxide layer 501A (light orange) and optionally spacer 512A[16] (dark orange)) (orange) separates the first stress-relief film from the first gate electrode. Figure A shows this below.

[16] *See* note 13 above, Section IX.B.1.b(6).

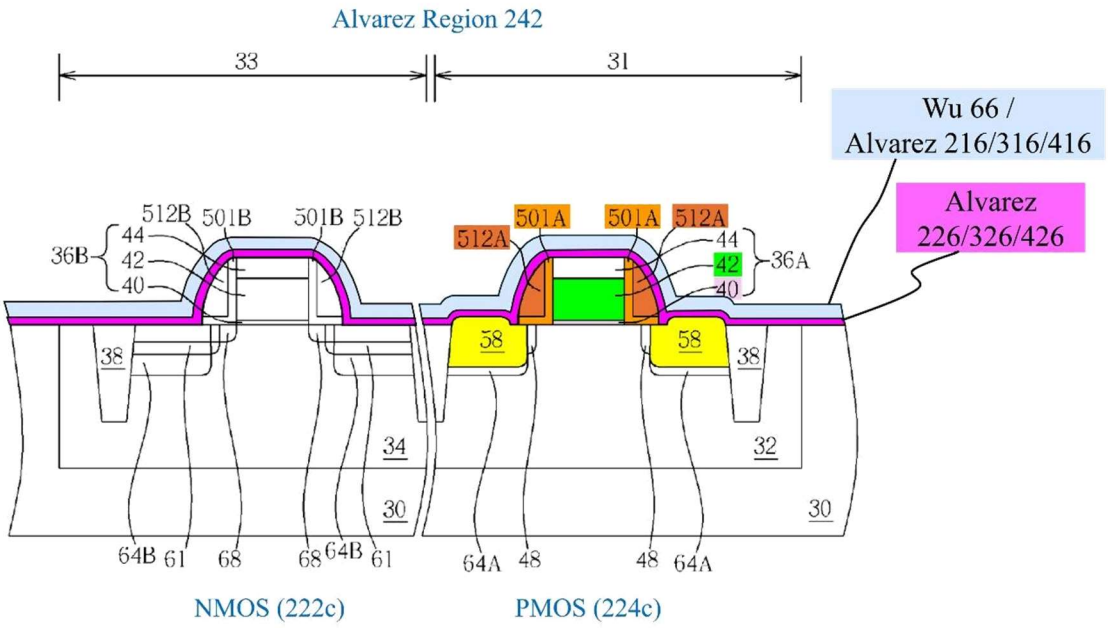
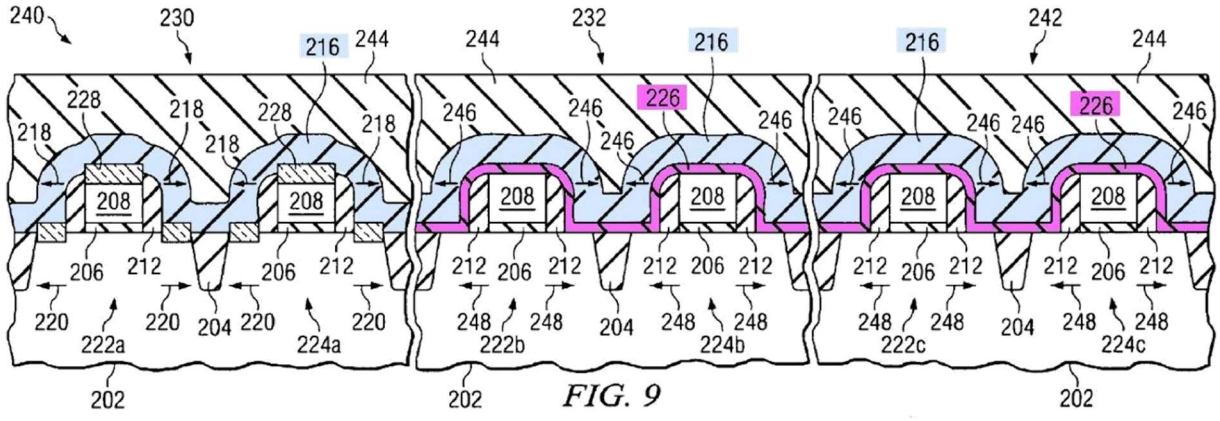


Figure A

170. Alvarez confirms this. For example, Alvarez's FIG. 9 shows that stress-controlling film 226 lies over gate electrode 208 and sidewalls 212 in stress-control region 242, such that stress-controlling film 226 does not directly contact the side surfaces of gate electrode 208 because sidewall 212 sits between them. The Wu-Alvarez combination preserves this arrangement, as the embodiment in Figure A above illustrates. *See* Section IX.B.1.a above.



Alvarez's FIG. 9 (annotated)

c. Claim 3: "The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer"

171. In my opinion, the Wu-Alvarez combination renders claim 3 obvious.

172. As I further explain below, this alternative embodiment also satisfies claim 1 for the same reasons I explain above regarding Figure A. *See* Sections IX.B.1.a above.

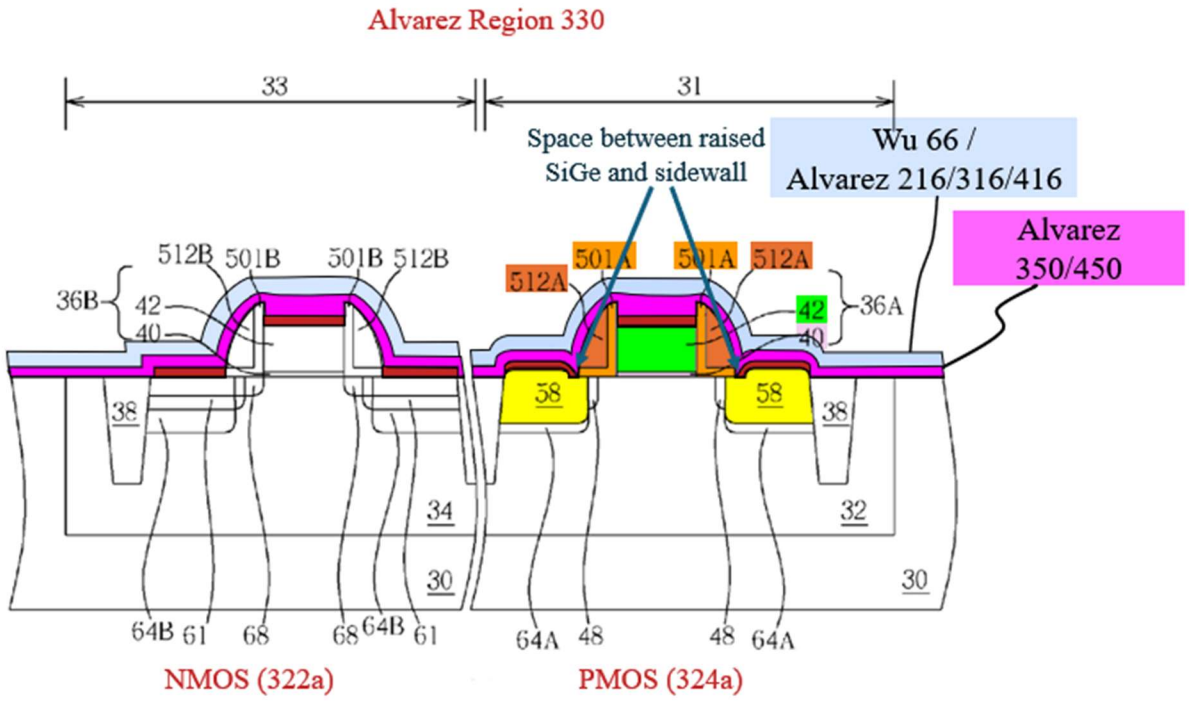
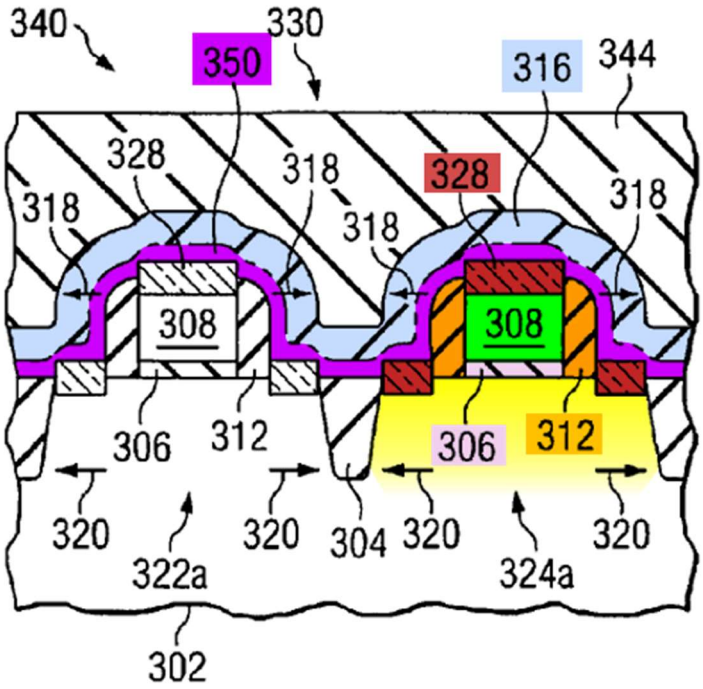


Figure A'

173. As shown above, Wu teaches an optional silicidation step for source/drain regions 64A and 64B, as well as for gate electrode 42. *See* Wu ¶[0024] ("[A] self-aligned silicide process (salicide process) is optionally performed.");

Wu ¶[0043] ("[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain."); Wu ¶[0036] ("A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor."), ¶[0055] (same). Figure A' above shows an embodiment of the Wu-Alvarez combination in a silicide region like Alvarez's silicide region 330 in FIG. 10 (excerpted, annotated below). Unlike Alvarez's silicide region 230 in FIG. 9, Alvarez's silicide region 330 in FIG. 10 applies a second stress-controlling film 350/450 after silicidation takes place. Alvarez ¶[0044], ¶[0046], ¶¶[0063]-[0064], FIGS. 9-10. Figure A' above shows how this applies to the Wu-Alvarez combination.



Alvarez's FIG. 10 (excerpted, annotated)

174. Compared to Figure A, the only material difference regarding the alternative embodiment of the Wu-Alvarez combination shown in Figure A' is the addition of the silicide regions (burgundy). Since this addition does not materially affect my analysis of claim 1, I do not repeat that analysis for Figure A'. It suffices to note my analysis in Section IX.B.1.b applies to Figure A' with the following substitutions:

- Figure A' shows the Wu-Alvarez combination in a region like Alvarez's silicide region 330, whereas Figure A shows the Wu-Alvarez combination in a region like Alvarez's stress-controlling region 242.
- All references to FIG. 9 in my discussion of claim 1 in Section IX.B.1.b would refer to FIG. 10 instead.
- All references to Alvarez's stress controlling layer 226/326/426 in Section IX.B.1.b would refer to Alvarez's stress-controlling layer 350/450.[17]

See Section IX.B.1.b above; Wu ¶[0024], ¶[0036], ¶[0043], ¶[0055]; Alvarez ¶¶[0063]-[0064], FIGS. 9-10. The PMOS structure in Figure A', however, is essentially the same as the structure I analyze for claim 1 in Section IX.B.1.b above. The addition of the silicide layer does not materially affect my analysis, such that the PMOS structure in Figure A' also satisfies claim 1.

[17] *See* Alvarez ¶[0064] ("The third material 350 preferably comprises similar materials, dimensions, and deposition methods and parameters as described for the first material 226 or stress-controlling material 226 shown in FIGS. 5 through 9, for example. . . . The third material 350 may also be formed over the first region 330 after the formation of the silicide 328, as shown in phantom.").

175. The embodiment of the Wu-Alvarez combination shown in Figure A' also includes the additional features recited in claim 3: "a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer."

176. Although not illustrated in Wu's FIG. 14, after growing the raised epitaxial SiGe layer 58 in the trench 56, Wu explains that "a self-aligned silicide process (salicide process) is optionally performed." Wu ¶[0024]; *see also* Wu ¶[0043] ("[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain."); Wu ¶[0036] ("A silicide layer, a CESL, and an ILD layer, and contact holes for connecting the components of the CMOS transistor to or other electrical devices may be formed on the CMOS transistor to accomplish the CMOS transistor."), ¶[0055] (same). To do this, "[a] metal layer, including titanium (Ti), cobalt (Co), nickel (Ni), palladium (Pd), platinum (Pt) or the like, is deposited. And a rapid thermal process is performed to form a silicide layer (not shown) on the surfaces of the source/drain 64A, 64B." Wu ¶[0024].

177. Alvarez explains that stress-controlling layer 350/450 may "be formed over the first region 330 after the formation of the silicide 328" in the source/drain and gate electrode regions. Alvarez ¶[0064]; *see also* Alvarez, FIG. 10.

178. Putting these descriptions together, a POSITA would have found the embodiment of the Wu-Alvarez combination in Figure A' below obvious for the reasons I explain in Section IX.B.1.a above.

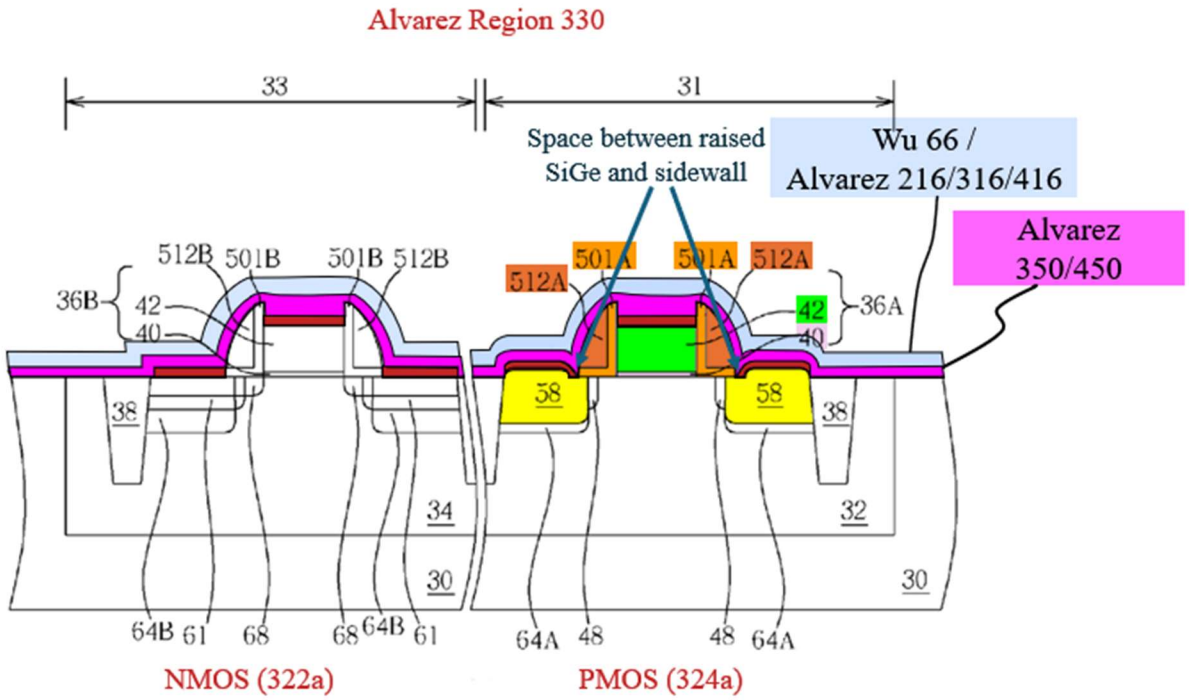


Figure A'

179. As Figure A' shows above, this embodiment of the Wu-Alvarez combination includes a first silicide layer (shown in burgundy) formed on the first gate electrode (gate 42, shown in green) and a second silicide layer (also shown in burgundy) formed on the first source/drain region which includes the silicon compound layer (epitaxial SiGe layer 58, shown in yellow). *See* Wu ¶[0024], ¶[0036], ¶[0043], ¶[0055]; Alvarez ¶¶[0063]-[0064], FIG. 10. Accordingly, it is my opinion that a POSITA would have found claim 3 obvious in view of the Wu-Alvarez combination as depicted in Figure A'.

d. Claim 4: "The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer"

180. In my opinion, the Wu-Alvarez combination renders claim 4 obvious.

181. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

182. In the embodiment of the Wu-Alvarez combination shown in Figure A, excerpted and further annotated below, the first stress-relief film (akin to Alvarez's stress-controlling film 226/326/426 (magenta)) is formed on a side surface of epitaxial SiGe layer 58 (yellow). *See* Section IX.B.1.a above.

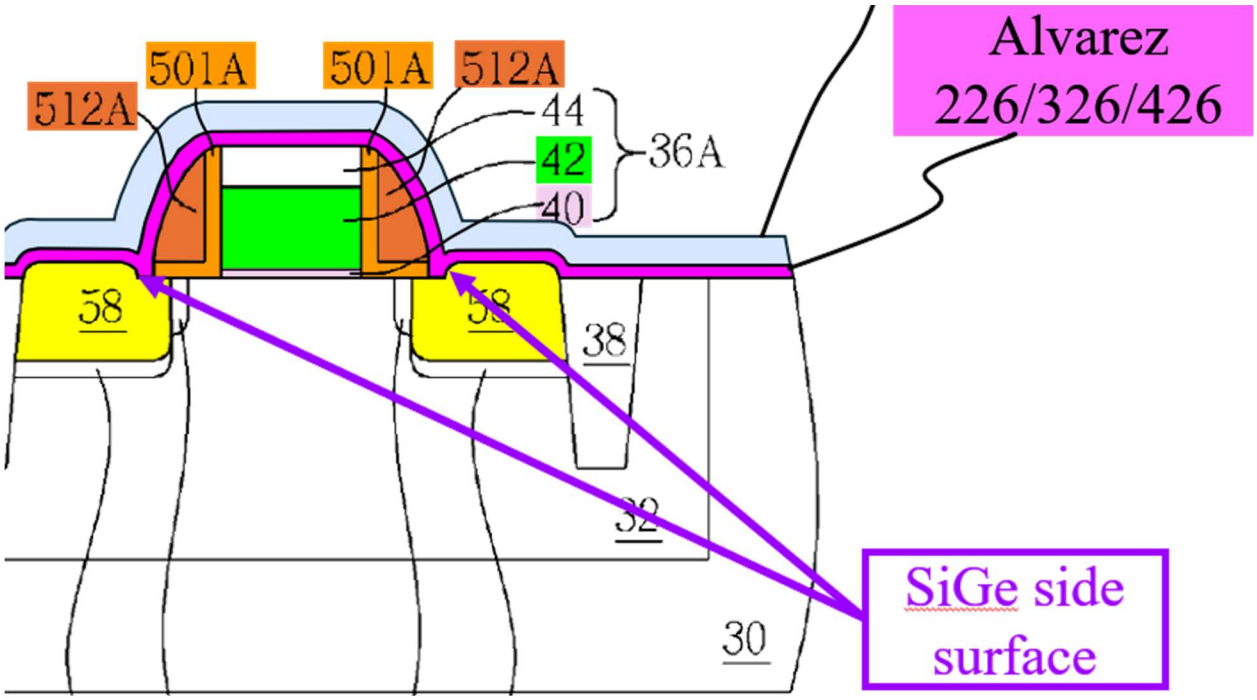


Figure A (excerpted and further annotated)

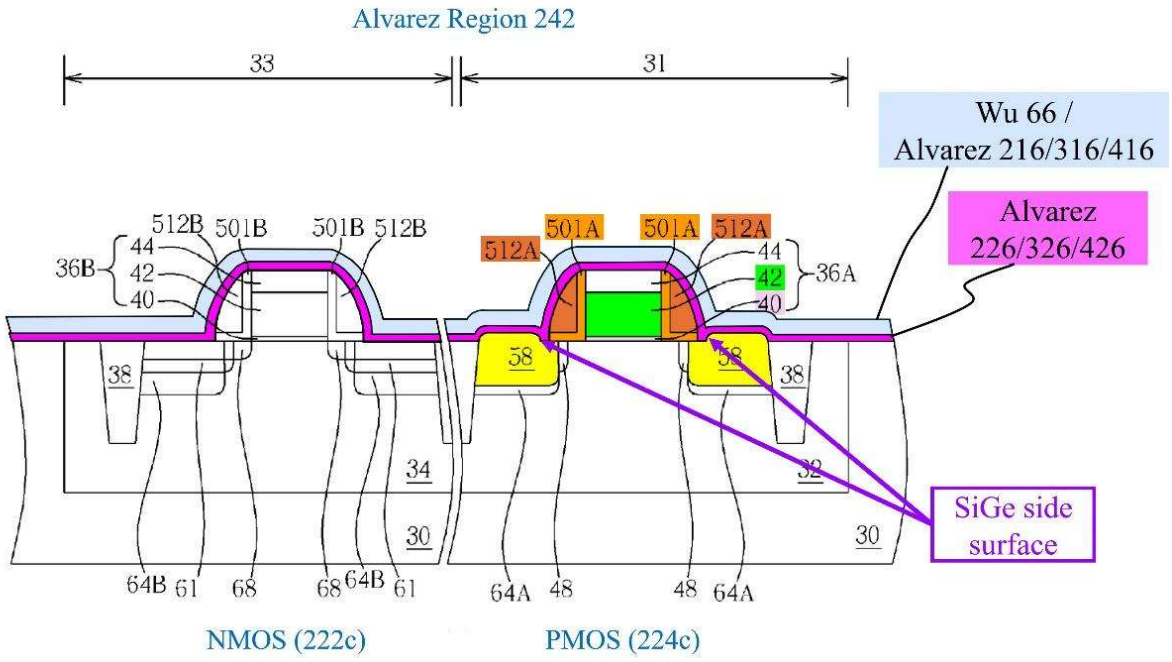


Figure A (further annotated)

e. Claim 5: "The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer"

183. In my opinion, the Wu-Alvarez combination renders claim 5 obvious.

184. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

185. In the Wu-Alvarez combination, the first sidewall spacer comprises Wu's "oxide layer 501A" and "second spacer 512A."[18] *See* Section IX.B.1.b(5) above.

[18] *See* note 13 above, Section IX.B.1.b(6).

186. Wu discloses that "oxide layer 501A, 501B [forms] on sidewalls of the gate structures 36A, 36B for protecting the gate structures 36A, 36B." Wu ¶[0017]. Wu's FIGS. 1-7 and 9-14 show that oxide layer 501A is an inner sidewall spacer that lies closest to, and is formed on, the side surfaces of gate electrode 42. Wu ¶[0017], FIGS. 1-7, 9-14; *see* Section IX.B.1.b(5) above. As Wu's FIGS. 1-7 and 9-14 also show, Wu's inner oxide sidewall spacer 501A has an "L"-shaped cross-section. Wu, FIGS. 1-7, 9-14; *see* Section IX.B.1.b(5) above.

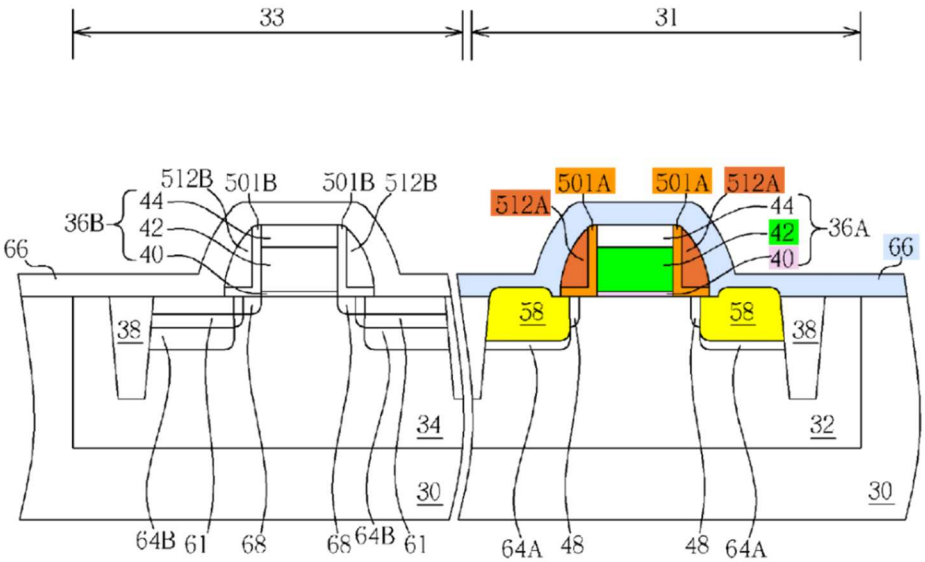


FIG. 14

Wu's FIG. 14 (annotated)

187. Wu further discloses that "spacer 512A, 512B is formed on the sidewalls of the gate structures 36A, 36B" using "the same . . . processes for forming first spacers 502A." Wu ¶[0024], FIGS. 7, 14. Like spacers 512A, spacers 502A are formed "beside the thermal oxide layers 501A." Wu ¶[0018]; *compare* Wu, FIG. 9, *with* Wu, FIG. 14. As Wu's FIGS. 7 and 14 show, second spacers 512A are outer

sidewall spacers located on the outer part of the L-shaped cross-section of oxide layers 501A. Wu ¶[0018], FIGS. 7, 14; *see* Section IX.B.1.b(5) above. The Wu-Alvarez combination preserves this arrangement, as the embodiment in Figure A below illustrates.

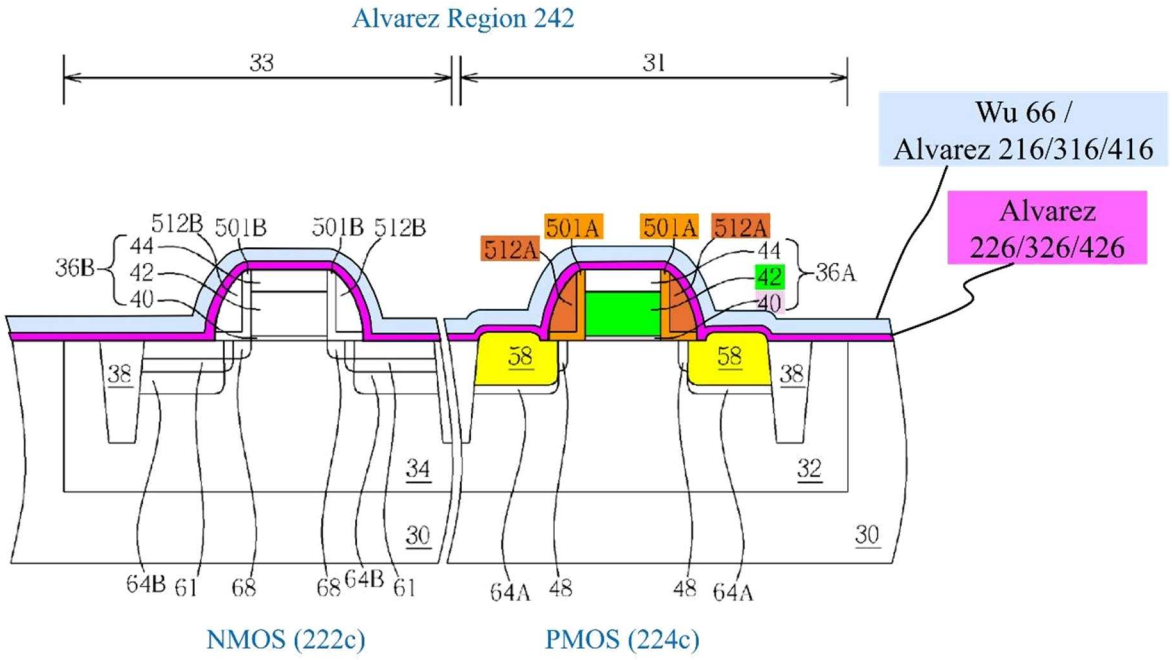


Figure A

f. Claim 7:

188. In my opinion, the Wu-Alvarez combination renders claim 7 obvious.

(1) [7Pre]: "The semiconductor device of claim 1"

189. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

(2) [7A]: "the first MIS transistor is a p-type MIS transistor"

190. As I explain above for claim 1, Wu discloses that the first MIS transistor is a pFET (i.e., p-type MIS transistor) in "PMOS transistor region 31." *See* Section IX.B.1.b(2) above. The embodiment of the Wu-Alvarez combination discussed for claim 1 (and shown in Figure A) includes the pFET in a region like Alvarez's stress-control region 242. *See* Section IX.B.1.b(2) above.

(3) [7B]: "the first stress is a compressive stress"

191. As I explain above for claim 1, Wu discloses that the "epitaxial [SiGe] layer 58" preferably causes a first, compressive stress "to compress the channel" because "epitaxial layer 58 has a lattice constant greater than that of the semiconductor substrate 30." Wu ¶[0021], ¶[0041]; *see also* Wu ¶[0005]; Section IX.B.1.b(6) above. The embodiment of the Wu-Alvarez combination discussed for claim 1 (and shown in Figure A) retains Wu's epitaxial SiGe regions 58 to cause a first, compressive stress in the pFET channel region. *See* Sections IX.B.1.a and IX.B.1.b(6) above.

(4) [7C]: "the second stress is a tensile stress"

192. As I explain above for claim 1, the embodiment of the Wu-Alvarez combination shown in Figure A includes a tensile CESL 66 (like Alvarez's stress-inducing layer 216/316/416) that causes a tensile stress. *See* Sections IX.B.1.a and IX.B.1.b(7) above; Alvarez ¶[0022], ¶[0054], ¶¶[0065]-[0066], ¶[0069].

g. Claim 8:

193. In my opinion, the Wu-Alvarez combination renders claim 8 obvious.

(1) [8Pre]: "The semiconductor device of claim 1"

194. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

(2) [8A]: "the silicon compound layer is a SiGe layer"

195. As I explain above for claim 1, Wu discloses that "epitaxial layer 58" may be "silicon germanium" (SiGe) when the first active area is PMOS transistor region 31. *See* Wu ¶[0021], ¶[0041], ¶[0050]; Section IX.B.1.b(6) above. Wu's epitaxial SiGe layer 58 corresponds to the silicon compound layer in the embodiment of the Wu-Alvarez combination shown in Figure A and discussed above. *See* Sections IX.B.1.a and IX.B.1.b(6) above.

(3) [8B]: "the stress insulating film is a silicon nitride film"

196. As I explain above for claim 1, "[t]he material of [Wu's] CESL 66 may include . . . a strained silicon material, i.e.[,] silicon nitride." Wu ¶[0025]; *see also* Alvarez ¶[0022], ¶[0047] ("The second material 216 preferably comprises a nitride material such as silicon nitride . . . ."); Sections IX.B.1.a and IX.B.1.b(7) above. In the embodiment of the Wu-Alvarez combination shown in Figure A, the stress insulating film (Wu's CESL 66) is a tensile silicon nitride film (like Alvarez's stress-inducing layer 216/316/416). *See* Sections IX.B.1.a and IX.B.1.b(6) above.

(4) [8C]: "the first stress-relief film is a silicon oxide film"

197. As I explain above for claim 1, the embodiment of the Wu-Alvarez combination shown in Figure A includes a stress-relief film like Alvarez's stress-controlling film 226/326/426. *See* Sections IX.B.1.a and IX.B.1.b(9) above. This film may be "an oxide such as silicon dioxide." Alvarez ¶[0043]; *see also* Alvarez, claim 13 (reciting a "silicon dioxide" stress-controlling material); Sections IX.B.1.a and IX.B.1.b(9) above.

h. Claim 9: "The semiconductor device of claim 1, wherein the first MIS transistor is an n-type MIS transistor, the first stress is a tensile stress, and the second stress is a compressive stress"

198. In my opinion, the Wu-Alvarez combination renders claim 9 obvious.

199. In my discussion of claim 1 above, the first MIS transistor is a pFET. *See* Section IX.B.1.b above. Additionally, as I explain below, Wu and Alvarez render obvious a first MIS transistor that is an nFET, a first stress being tensile (e.g., caused by epitaxial silicon carbide (SiC) source/drain regions), and a second stress caused by a compressive insulating layer located above the nFET.

200. Wu explains that its descriptions of nFETs and pFETs may be reversed with respect to the epitaxially grown source/drain regions. In other words, "first active area" 31 may include an nFET, and "second active area" 33 may include a pFET. *See* Wu ¶[0037], ¶[0057]. Although Wu's "first preferred embodiment is

illustrated using a PMOS transistor as the first active area, and an NMOS transistor as the second active area," as I discuss for claim 1, "the first preferred embodiment can be modified to form a CMOS transistor having **an NMOS transistor as the first active area** [31], and a **PMOS as the second active area** [33]." Wu ¶[0037], ¶[0057] (emphases added).

201. In this alternative embodiment that switches the nFETs and pFETs, Wu further discloses that the epitaxial source/drain regions 58 may comprise "silicon carbide" for an nFET rather than SiGe for a pFET. Wu ¶[0037] ("As shown in FIG. 4, the epitaxial layer of silicon carbide is formed."), ¶[0057] ("As shown in FIG. 12, the epitaxial layer of silicon carbide is formed."); *see also* Chen729 ¶[0022]; Bohr683 ¶[0045]; Murthy151 ¶[0046]. Viewing Wu's FIG. 14 in the context of Wu's alternative embodiment, epitaxial regions 58 would have been SiC regions, and the nFET would be located in active region 31 on the right.

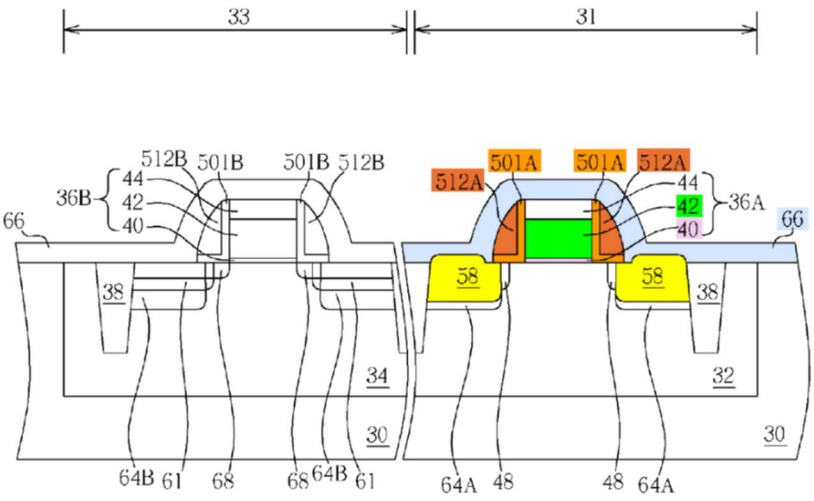


FIG. 14

Wu's FIG. 14 (annotated)

202. In my opinion, a POSITA would have recognized that Wu's raised epitaxial SiC layer 58 applies a tensile stress to the nFET channel in the first transistor region 31. A POSITA would have known that SiC has a smaller lattice constant than silicon (the opposite of SiGe, which has a larger lattice constant), such that epitaxial SiC source/drain regions 58 would impart tensile stress along the gate length direction of the nFET channel in an NMOS first active region 31. *See* Wu ¶[0037], ¶[0057]; Bohr683 ¶[0045] ("A silicon alloy material having a lattice spacing that is smaller than the silicon substrate (e.g., such as silicon carbide . . .) can be deposited into a first and second NMOS junction region void (e.g., the NMOS equivalence of voids 340 and 360) to cause a tensile or tension in the channel of the NMOS device (e.g., such as by creating the opposite vectors of those shown by 474, 476, 484, 486, and 494)."); Murthy151 ¶[0046] ("[M]aterial 370 may be thickness of T4 of an epitaxial thickness of crystalline silicon-carbon alloy material (e.g., Si_xC_{1-x}), where the size and/or thickness of T4 is sufficient to cause a tensile strain in substrate 120. . . . For example, material 370 may be a thickness of silicon-carbon alloy (Si_xC_{1-x}) having a lattice spacing smaller than a lattice spacing of substrate 120.").

203. In this alternative embodiment, a POSITA would have found it obvious to make Wu's strained CESL 66 compressive rather than tensile. This is because Wu's alternative nFETs already experience tensile strain from epitaxial SiC

source/drain regions 58 to boost electron mobility, and the pFETs (now lacking epitaxial SiGe source/drain regions 58) would not experience a compressive stress to boost hole mobility. *See* Wu ¶[0005], ¶[0025], ¶[0044]; Alvarez ¶[0025], ¶[0033], ¶[0049], ¶[0065], ¶[0067], ¶[0070]; Section VI.B above. In other words, a POSITA would have recognized and found it obvious that the first MIS transistor of claim 9 would be constructed with the opposite stresses and of the opposite conductivities than those I discuss in the context of claim 1. The other aspects of the embodiment of the Wu-Alvarez combination I discuss in the context of claim 1 would remain essentially the same.

204. As I explain above in Section IX.B.1.a, Wu discloses "deposit[ing] . . . a contact etch stop layer (CESL) 66" that "may include . . . a strained silicon material, i.e.[,] silicon nitride." Wu ¶[0025]; *see also* Wu ¶[0005] (describing compressive strained CESL to improve PMOS), ¶[0044] ("A deposition process is performed to form a CESL 66 on the surface of the gate structures 36A, 36B, the second spacers 512A, 512B, and the sources/drains 64A, 64B."), FIGS. 7, 14. But Wu does not specify whether the strained CESL 66 is tensile or compressive. *See* Section IX.B.1.a above.

205. Alvarez discloses that stress-increasing material 216 (equivalent to 316 and 416) applies a "third amount of stress 246 [that] may comprise tensile or compressive stress." Alvarez ¶[0049]; *see also* Alvarez ¶[0067] (explaining that

stress-increasing material 416 (equivalent to 216 and 316) may "comprise[] compressive stress"). Alvarez explains that a compressive stress-inducing layer 216/316/416 can be offset in nFETs by a stress-controlling film 226/326/426:

> [I]f the stress-increasing material 416 comprises compressive stress, the stress-controlling material 426 . . . may be formed over an NMOS FET . . . , resulting in the formation of a PMOS FET with increased operating current and improved performance due to the stress-increasing material 416 formed directly over and abutting portions of the workpiece 402 in the source and drain regions of the PMOS FET, yet wherein the NMOS FET has less performance degradation, due to the presence of the stress-controlling material 426 . . . between the NMOS FET and the [compressive] stress-increasing material 416, for example.

Alvarez ¶[0067]; *see also* Alvarez ¶[0070] ("Similar improvements in NMOS FETs may be achieved if the stress of the stress-increasing material 216, 316, or 416 comprises compressive stress, for example, by disposing the novel stress-controlling materials 226, 326, 350, 426, and 450 between the NMOS FETs and the stress-increasing material 216, 316, or 416 described herein."); Section VI.B above. Thus, as the disclosures in Wu and Alvarez confirm, a POSITA would have found it obvious to reverse the first and second stresses in the embodiment of the Wu-Alvarez combination Figure A shows, such that an nFET lies in first active area 31 and strained CESL 66 is compressive.

206. In my opinion, a POSITA would have reasonably expected to succeed in forming a compressive CESL (like Alvarez's layer 216/316/416) over such an

nFET because it was well known how to control the stress of a silicon nitride CESL by using appropriate deposition conditions. *See, e.g.*, Jung ¶[0090], ¶¶[0099]-[0100], Tbl. IV; Alvarez ¶[0067], ¶[0070].

207. Thus, it is my opinion that a POSITA would have found it obvious to reverse the roles of Wu's nFET and pFET and to reverse the stresses accordingly to yield the same benefits of strain-engineering (i.e., enhanced electron and hole mobilities). To do so, as I explain above, a POSITA would have found it obvious to enhance the electron mobility of the nFET in first active area 31 by using tensile SiC epitaxial layers 58 and to enhance the hole mobility of the pFET in second active area 33 by using a compressive CESL 66. *See* Wu ¶[0037], ¶[0057]; Alvarez ¶[0049], ¶[0067], ¶[0070]; Chen729 ¶[0022]; Bohr683 ¶[0045]; Murthy151 ¶[0046]. And a POSITA would have reasonably expected to enhance electron and hole mobilities in the nFET and pFET, respectively. Moreover, for essentially the same reasons I discuss in Section IX.B.1.a above (but with the stresses reversed), a POSITA would have included a stress-controlling layer (like Alvarez's stress-controlling layer 226/326/426) to mitigate the effects of the compressive CESL 66 on the nFET and to prevent silicide formation in certain circuit regions (like Alvarez's non-silicide region 232 and stress-control region 242).

208. Such an embodiment of the Wu-Alvarez combination would satisfy claim 1 for essentially the same reasons I describe in Section IX.B.1.b, except with the following role reversals:

- The first MIS transistor 31 is an nFET rather than a pFET. *See* Wu ¶[0037], ¶[0057].
- The silicon compound layer 58 is an epitaxial SiC layer instead of an epitaxial SiGe layer, and it exerts a tensile stress rather than a compressive stress, along the channel direction of the first MIS transistor. *See* Wu ¶[0037], ¶[0057]; *see* Section VI.B above (describing SiC and SiGe epitaxy).
- CESL 66 is compressive rather than tensile. *See* Wu ¶[0005], ¶[0025]; Alvarez ¶[0025], ¶[0033], ¶[0049], ¶[0065], ¶[0067]; Jung ¶[0090], ¶¶[0099]-[0100], Tbls. IV-V.

i. Claim 11:

209. In my opinion, the Wu-Alvarez combination renders claim 11 obvious in two ways, which I discuss further below.

(1) [11Pre]: "The semiconductor device of claim 1"

210. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

(2) [11A]: "a second MIS transistor"

211. Under a first mapping of the Wu-Alvarez combination to claim 11, Wu discloses a second MIS transistor: the nFET in a "second active area [that] is an NMOS transistor region 33." Wu ¶[[0017], ¶[0038] ("the second active area is an NMOS transistor region 33"), FIGS. 1-7, 9-14. In the embodiment of the Wu-Alvarez combination I discuss in Section IX.B.1.a above, nFET 222c shown in Figures A and B includes all features of the second MIS transistor recited in elements [11B]-[11F].

212. In this embodiment of the Wu-Alvarez combination, shown below in Figure C (same as Figure A but with additional highlighting) and Figure D (similar to Figure B but with additional highlighting), the second MIS transistor is nFET 222c in the equivalent of Alvarez's stress-control region 242. It includes a stress-control layer (like Alvarez's layer 226/326/426), and CESL 66 is tensile.

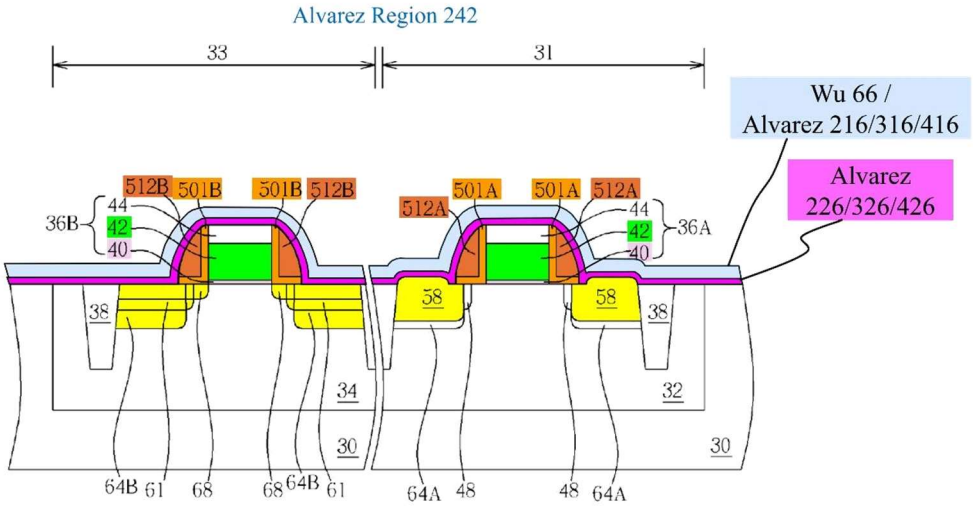


Figure C

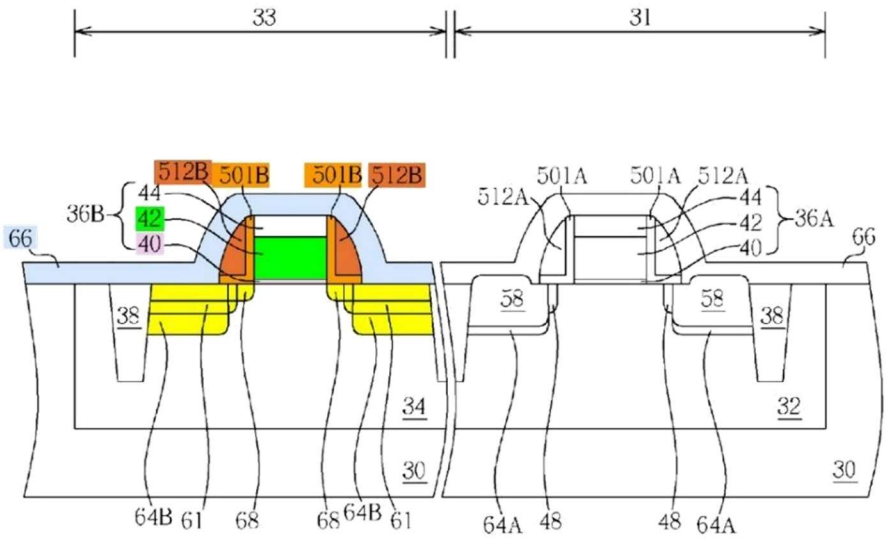


FIG. 14

Wu's FIG. 14 (annotated)

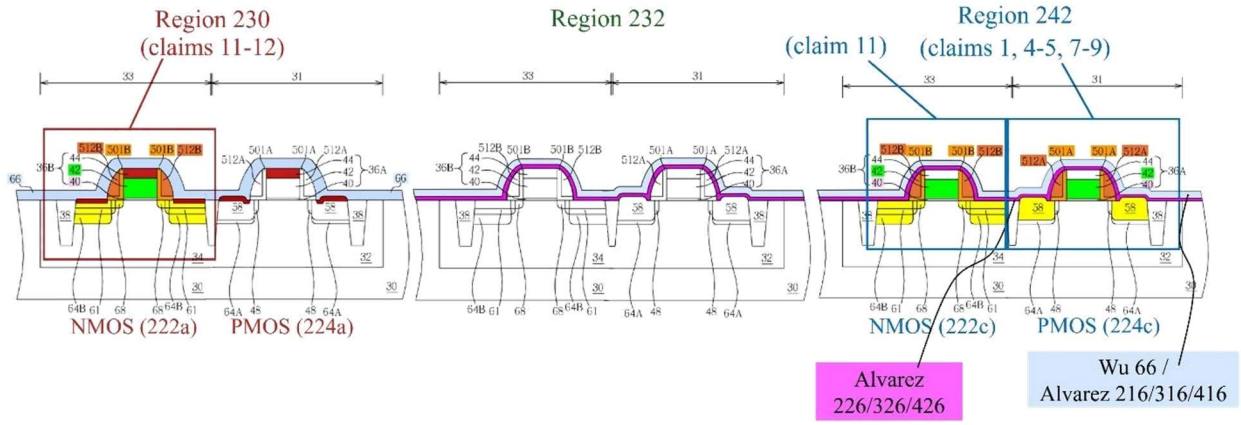


Figure D

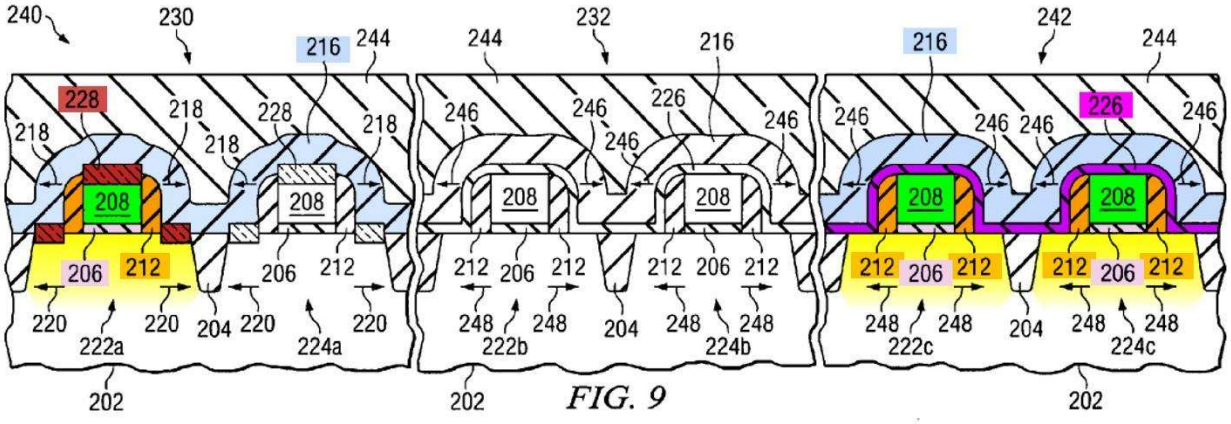


FIG. 9

Alvarez's FIG. 9 (annotated)

213. Under a second mapping of the Wu-Alvarez combination to claim 11, nFET 222a shown in composite Figure D above includes all features of the second MIS transistor recited in elements [11B]-[11F]. Alvarez teaches that some circuit regions, such as silicide region 230, do not include stress-control film 226/326/426 so that silicidation can occur. *See* Section IX.B.1.a above; Alvarez ¶[0042], ¶[0044], ¶¶[0046]-[0047], FIGS. 8-10. Wu also teaches that such silicidation is optional in its FETs. Wu ¶[0043] ("[A] self-aligned silicide process is optionally performed to form a silicide layer (not shown) on the surfaces of the gate structures or the source/drain."). In such cases, Wu's nFET in transistor region 33 would include a tensile CESL 66 (analogous to Alvarez's layer 216/316/416) but would not include the stress-relief layer (analogous to Alvarez's stress-controlling layer 226/326/426). Figure D above shows such an embodiment of the Wu-Alvarez combination. Under the second mapping, nFET 222a in the region equivalent to Alvarez's silicide region 230 corresponds to the second MIS transistor of claim 11 (and claim 12). In both the first and second mappings of claim 11, pFET 224c in a region equivalent to Alvarez's stress-control region 242 corresponds to the transistor of claim 1. *See* Sections IX.B.1.a and IX.B.1.b above.

(3) [11B]: "a second gate insulating film formed on a second active region in the semiconductor substrate"

214. Applicable to both of the mappings I discuss for [11A] (*see* Section IX.B.1.i(2) above), Wu discloses a second gate insulating film ("gate dielectric

layer 40") formed on "NMOS transistor region 33" of the "second active area" (second active region) of "semiconductor substrate 30." Wu ¶[0017] (explaining that "the second active area is an NMOS transistor region 33" having a "gate dielectric layer 40" in "gate structure[] . . . 36B"), ¶¶[0038]-[0039] (describing "gate structures 36A, 36B"). A POSITA would have understood that gate dielectric 40 is a second gate insulating film for the same reasons it is a first gate dielectric in claim 1. *See* Section IX.B.1.b(3) above. The only difference is the location of gate dielectric layer 40. Gate dielectric layer 40 in pFET 224c is the first gate insulating film, and gate dielectric layer 40 in nFET 222c (first mapping) or nFET 222a (second mapping) is the second gate insulating film. As composite Figures C and D show below, nFETs 222a and 222c in this embodiment of the Wu-Alvarez combination both include a gate dielectric film 40 (light purple) on the NMOS active region.

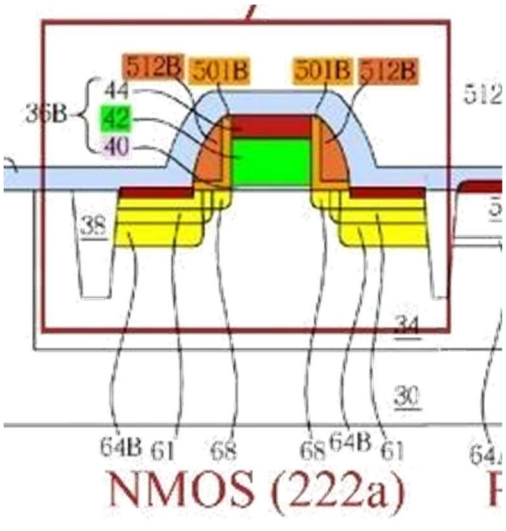


Figure D (excerpted)

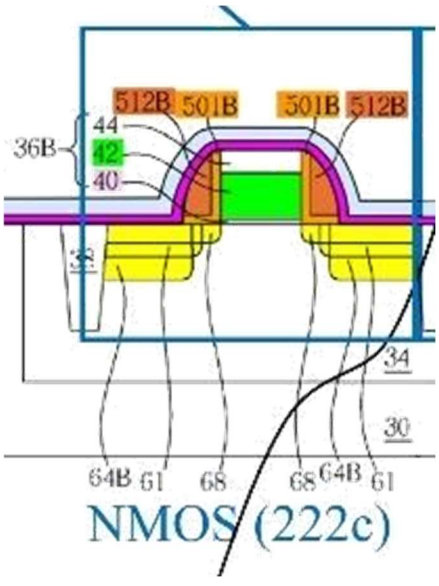


Figure D (excerpted)

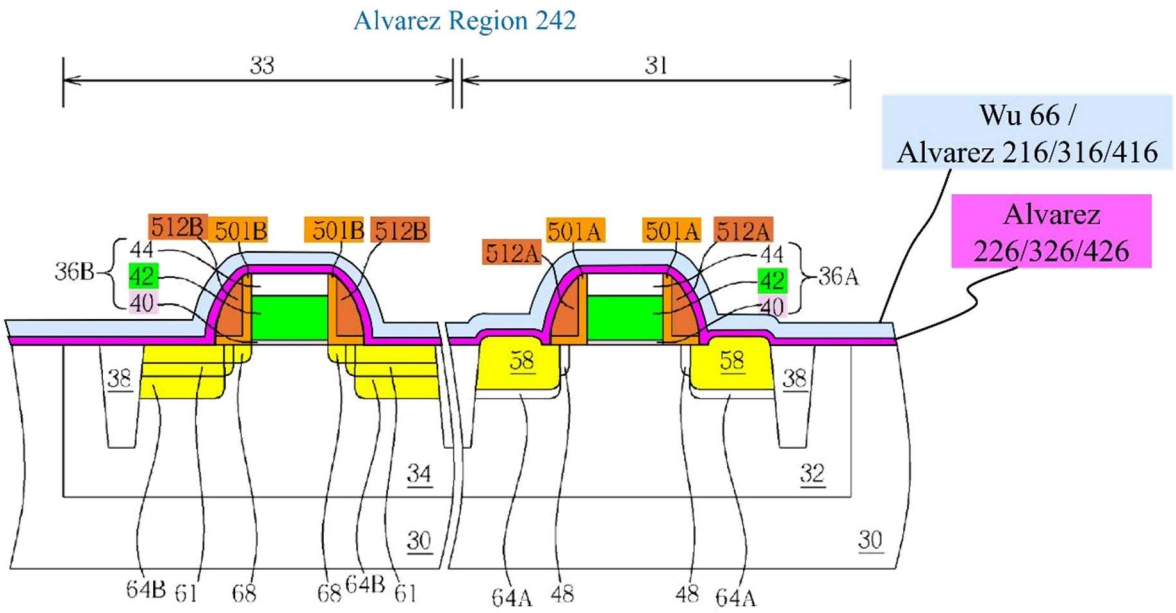


Figure C

(4) [11C]: "a second gate electrode formed on the second gate insulating film"

215. Applicable to both of the mappings I discuss for [11A] (*see* Section IX.B.1.i(2) above), Wu discloses a second gate electrode ("gate 42") formed on gate dielectric 40. Wu ¶[0017]. A POSITA would have understood gate 42 is a gate electrode for the reasons I discuss above in claim 1. *See* Section IX.B.1.b(4) above. The only difference is the location of gate 42. Gate 42 in pFET 224c of the Wu-Alvarez combination is the first gate electrode, and gate 42 in nFET 222c (first mapping) or nFET 222a (second mapping) is the second gate electrode.

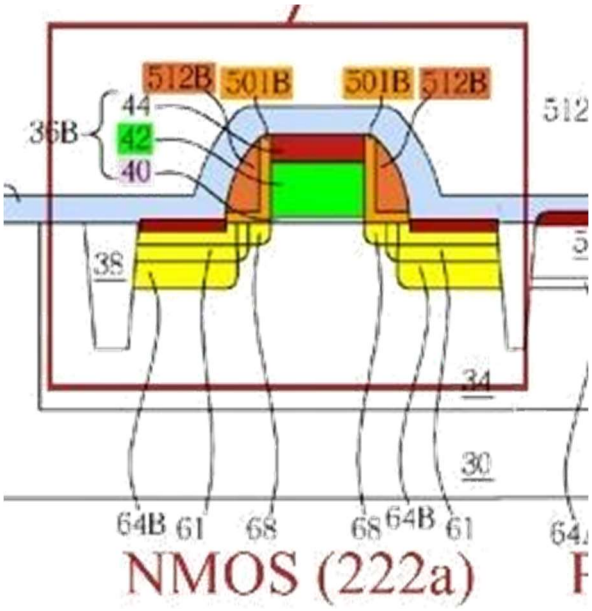


Figure D (excerpted)

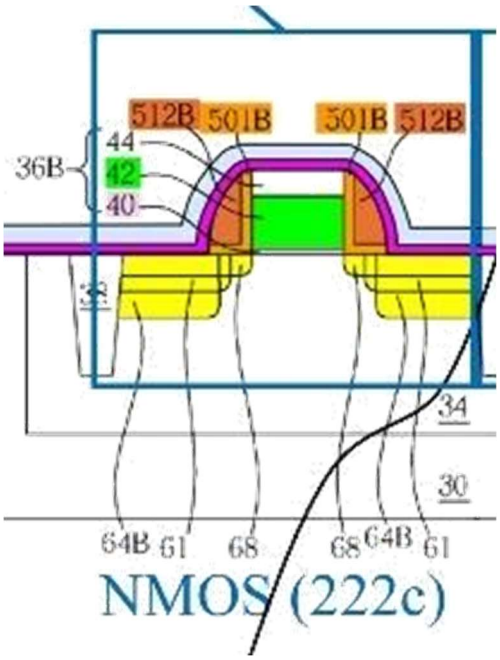


Figure D (excerpted)

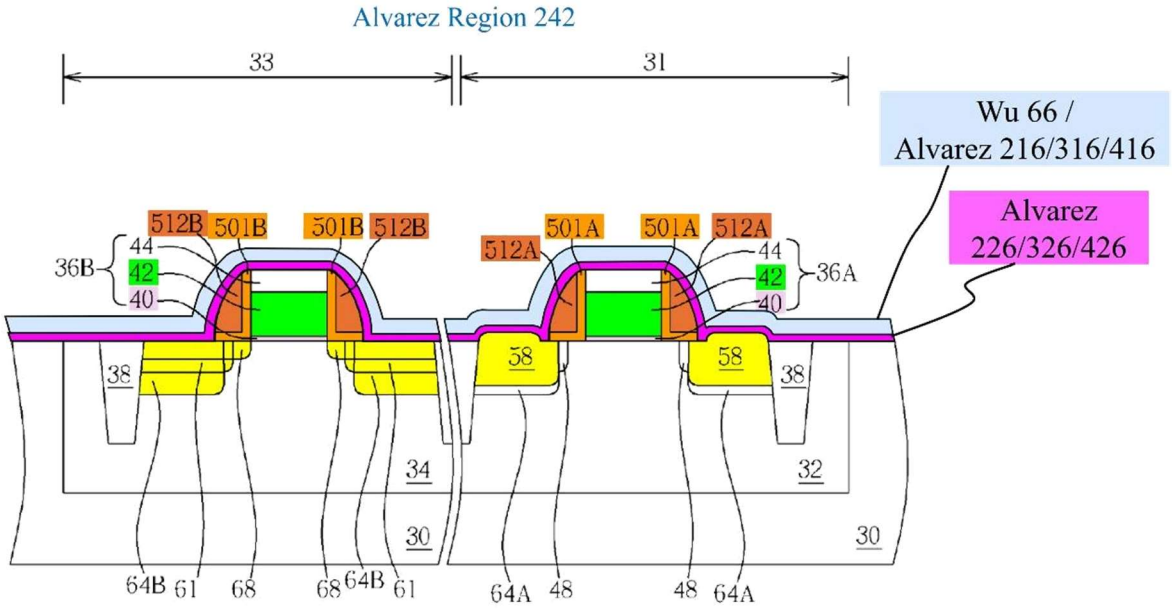


Figure C

216. Gate 42 may be made from "polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof." Wu ¶[0017],

FIGS. 7, 14. As composite Figures C and D show above, nFETs 222a and 222c both include a gate 42 (green) formed on the gate dielectric 40 (light purple).

(5) [11D]: "a second sidewall spacer formed on a side surface of the second gate electrode"

217. Applicable to both of the mappings I discuss for [11A] (*see* Section IX.B.1.i(2) above), Wu discloses a second sidewall spacer comprising "an oxide layer . . . 501B on sidewalls of the [nFET] gate structure[] . . . 36B" and "second [sidewall] spacer . . . 512B . . . formed on the sidewalls of the [nFET] gate structure[] . . . 36B." Wu ¶[0017], ¶[0024], FIGS. 7, 14. Thus, like pFET 224c of the Wu-Alvarez combination, which I discuss for claim 1, nFETs 222c (first mapping) and 222a (second mapping) include a second sidewall spacer comprising oxide layer 501B and second sidewall spacer 512B. *See* Section IX.B.1.b(5) above.

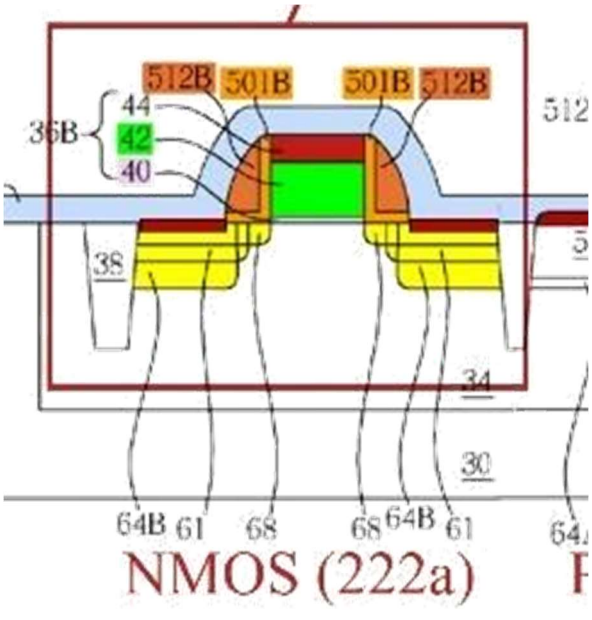


Figure D (excerpted)

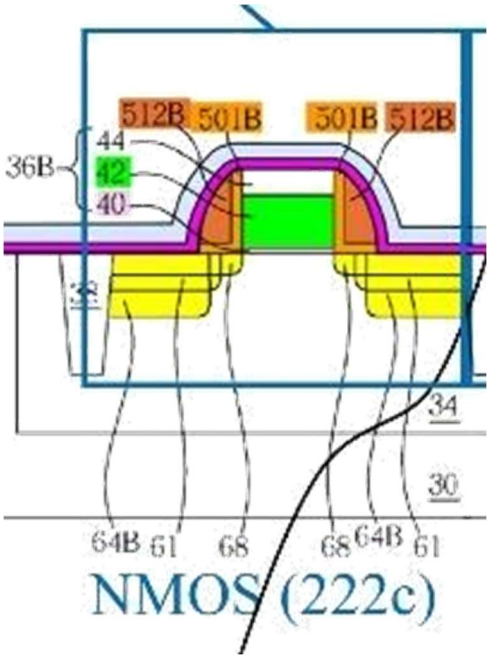


Figure D (excerpted)

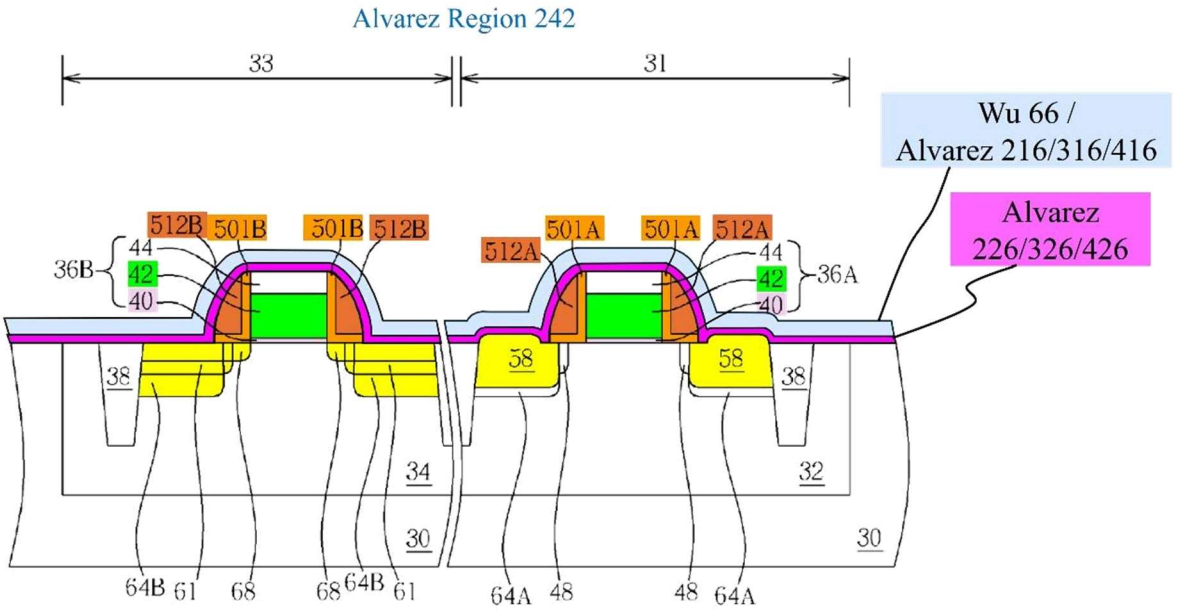


Figure C

218. As with pFET 224c of the Wu-Alvarez combination, oxide layer 501B and sidewall spacer 512B sit on the side surfaces of gate 42 in NMOS transistor region 33. *See* Section IX.B.1.b(5) above; Wu, FIGS. 7, 14. Together or individually, oxide layer 501B and sidewall spacer 512B disclose a second sidewall spacer formed on a side surface of the second gate electrode (gate 42) of nFETs 222c (first mapping) and 222a (second mapping). As composite Figures C and D show above, nFETs 222a and 222c both include a second sidewall spacer comprising oxide spacer 501B (light orange) and/or second sidewall spacer 512B (dark orange) formed on the side surfaces of gate electrode 42 (green) of gate structure 36B.

(6) [11E]: "a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer"

219. Applicable to both of the mappings I discuss for [11A] (*see* Section IX.B.1.i(2) above), Wu discloses an n-type (second conductivity type) second source/drain region in NMOS transistor region 33 (second active region). It includes n-type source/drain regions 64B, n-type lightly doped drain extensions NLDD1 61, and n-type lightly doped drain extensions NLDD2 68. Wu ¶¶[0023]-[0024], ¶¶[0038]-[0039], ¶¶[0042]-[0044], FIGS. 7, 14. As Figures C and D show below for this embodiment of the Wu-Alvarez combination, the n-type source/drain regions (yellow) of both nFET 222c (first mapping) and nFET 222a (second mapping) are formed on a lateral side of second sidewall spacer layers 501B (light orange) and 512B (dark orange) and beside nFET gate structure 36B.

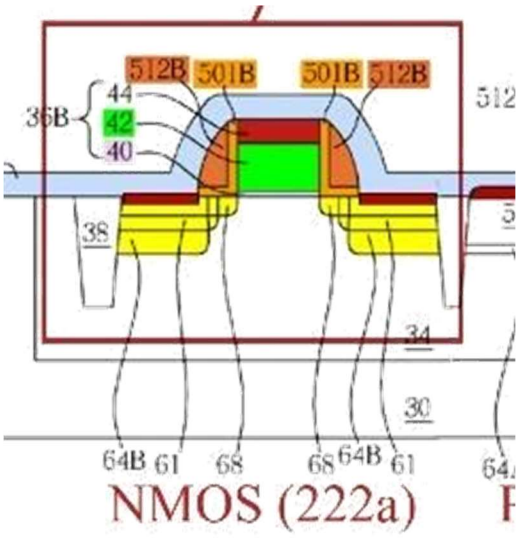


Figure D (excerpted)

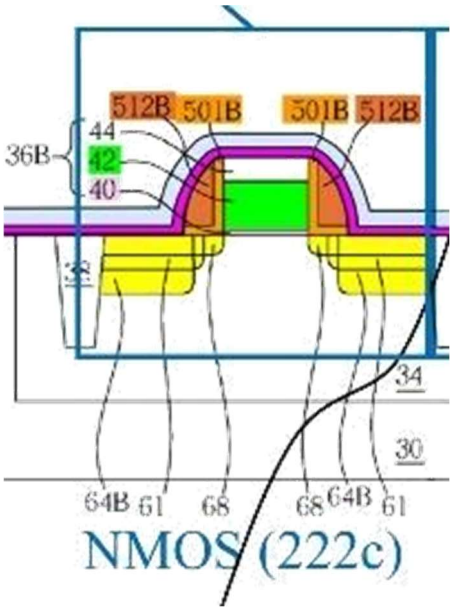


Figure D (excerpted)

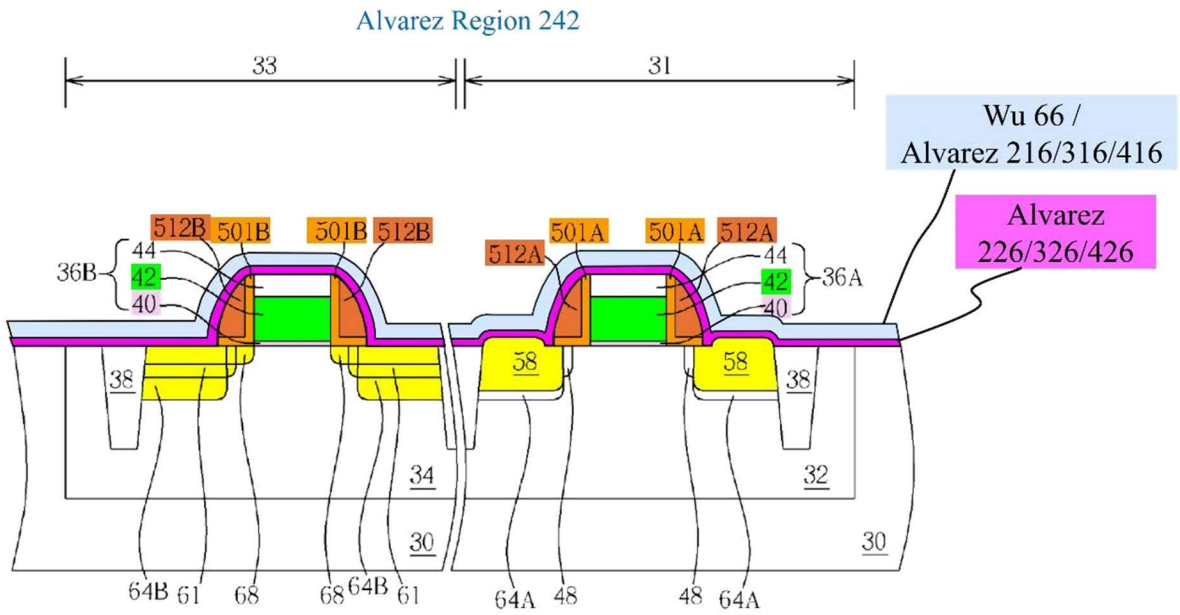


Figure C

(7) [11F]: "the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region"

220. Applicable to both of the mappings I discuss for [11A] (*see* Section IX.B.1.i(2) above), this embodiment of the Wu-Alvarez combination includes the stress insulating film (tensile CESL 66, light blue) formed over both the pFETs and the nFETs in circuit regions analogous to Alvarez's silicide region 230 and stress-control region 242. *See* Sections IX.B.1.a and IX.B.1.b(7) above.

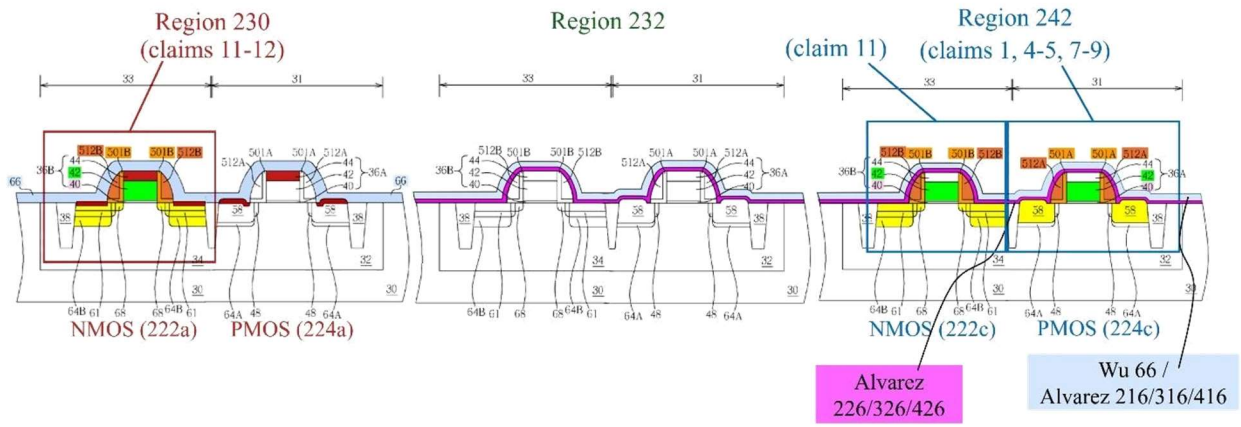
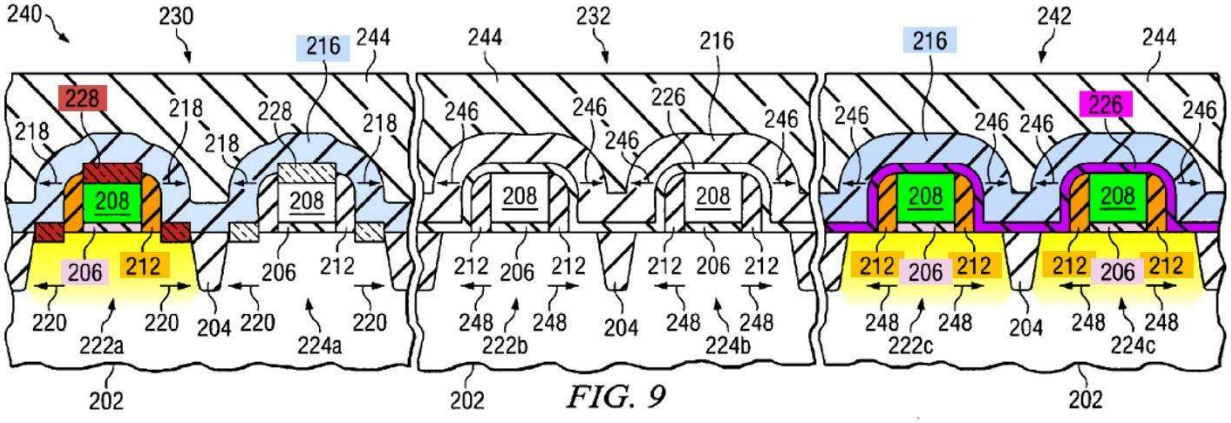


Figure D



Alvarez's FIG. 9 (annotated)

221. As composite Figures C and D illustrate for this embodiment of the Wu-Alvarez combination, nFET 222c (first mapping) and nFET 222a (second mapping) both include tensile CESL 66 (light blue) covering gate electrode 42 (green), second sidewall spacer layers 501B (light orange) and 512B (dark orange), and n-type source/drain regions 61/64B/68 (yellow). I include an annotated version of Alvarez's FIG. 9 for comparison with Figure D and an annotated version of Wu's FIG. 14 for comparison with the general FET structures shown in Figures C and D.

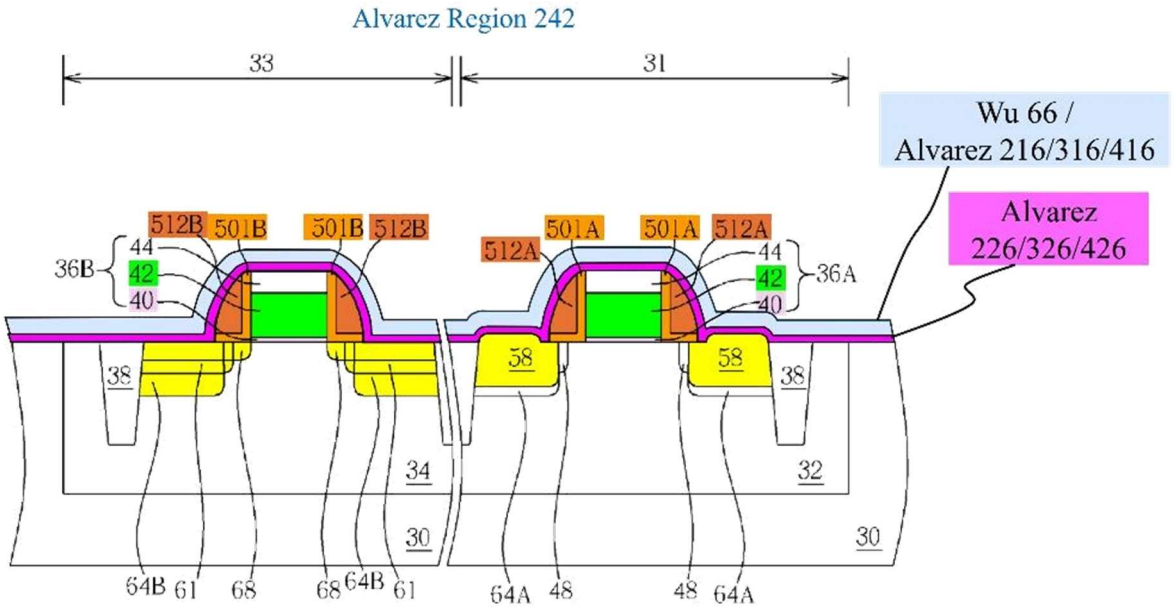


Figure C

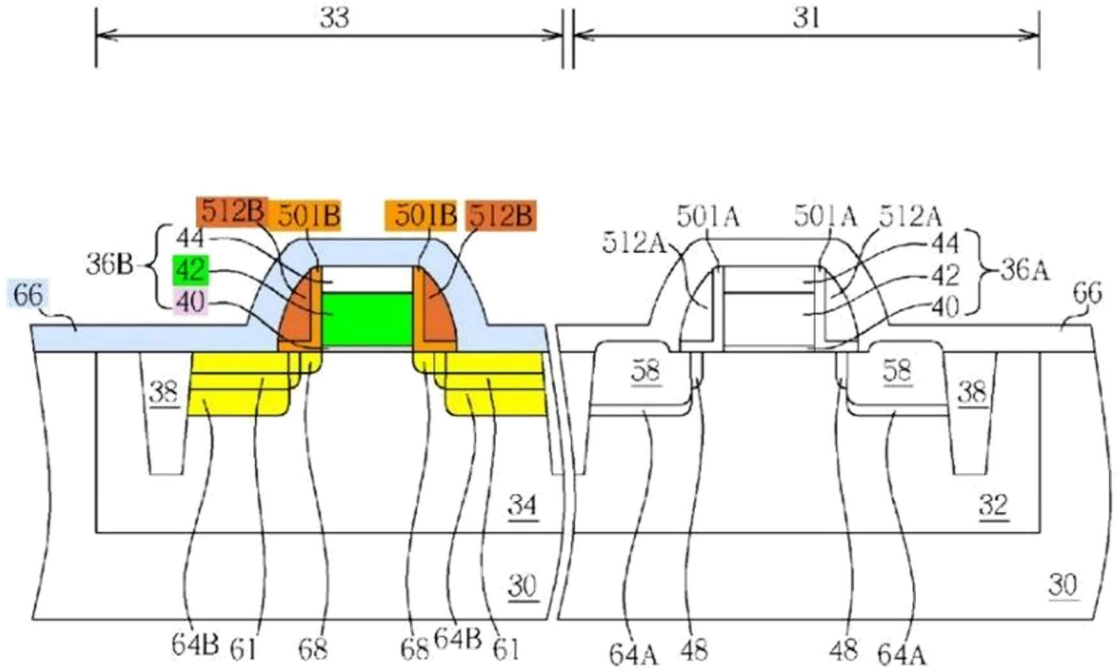


FIG. 14

Wu's FIG. 14 (annotated)

j. Claim 12: "The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region"

222. In my opinion, the Wu-Alvarez combination renders claim 12 obvious.

223. The Wu-Alvarez combination renders the semiconductor device of claim 11 obvious. *See* Sections IX.B.1.a and IX.B.1.i above.

224. As I discuss for claim 11, the embodiment of the Wu-Alvarez combination shown in Figure D includes nFET 222a in a region analogous to Alvarez's silicide region 230. It satisfies claim 11 under the second mapping. *See* Section IX.B.1.i above. As I discuss for the second mapping of claim 11 (*see* Section IX.B.1.i(2) above), certain NMOS devices (nFETs) in the Wu-Alvarez combination do not include the first stress-relief film, just as nFET 222a in Alvarez's silicide region 230 does not include Alvarez's stress-control film 226/326/426. *See* Alvarez ¶[0037], ¶¶[0042]-[0047], FIGS. 8-10; Wu ¶[0043].

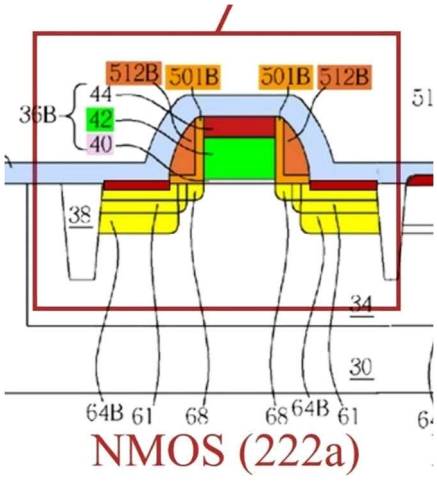
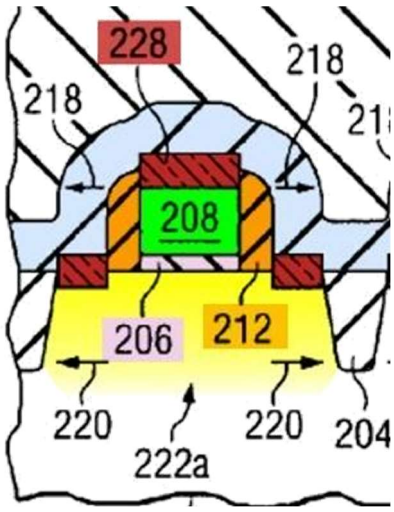


Figure D (excerpted)



Alvarez's FIG. 9 (annotated, excerpted)

k. Claim 13:

225. In my opinion, the Wu-Alvarez combination renders claim 13 obvious.

(1) [13Pre]: "The semiconductor device of claim 1"

226. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

227. A POSITA would have understood that Wu's nFET and pFET structures would be repeated many times in various circuit arrangements over the substrate because it is fundamental to semiconductor technology. For example, Wu discloses "[a] plurality of first active area[s] . . . defined on the semiconductor substrate 30." Wu ¶[0017], ¶[0038]. As I explain for claim 1, first active areas 31 are PMOS active areas. Wu explains that "[e]ach of the first [PMOS] active area[s] includes a first-type well and a gate structure, and each of the second active area[s] includes a second-type well and a respective gate structure thereon." Wu ¶[0017], ¶[0038].

228. As I mention in Section IX.B.1.a(1)(d), pFET 224b in non-silicide region 232 of this embodiment of the Wu-Alvarez combination corresponds to the third MIS transistor of claims 13-15. Composite Figure E below (same as Figure A but in non-silicide region 232 rather than stress-control region 242) shows the general structure of the third MIS transistor. Composite Figure F below (same as Figure D but with different highlights) shows how a POSITA would have understood

the third MIS transistor in the context of other circuit regions. *See* Section IX.B.1.a above.

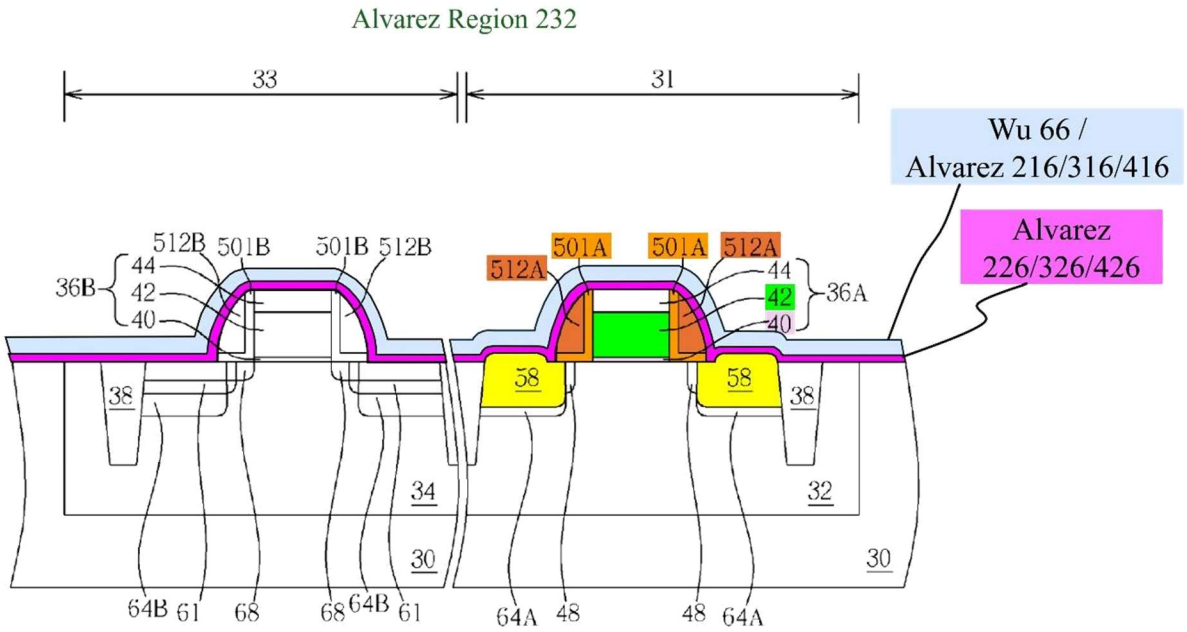


Figure E

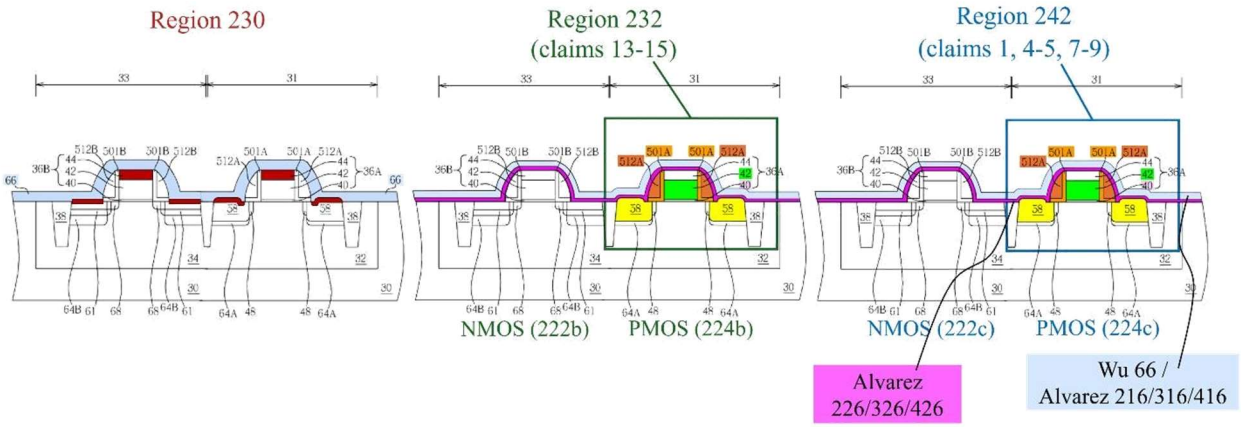


Figure F

229. Alvarez's FIG. 9 confirms the obviousness of Figures E and F, showing, for example, two pFETs 224b and 224c in regions 232 and 242, respectively. *See* Section IX.B.1.a above. Composite Figure F shows this

embodiment of the Wu-Alvarez combination in the equivalent of Alvarez's non-silicide region 232 and stress-control region 242.

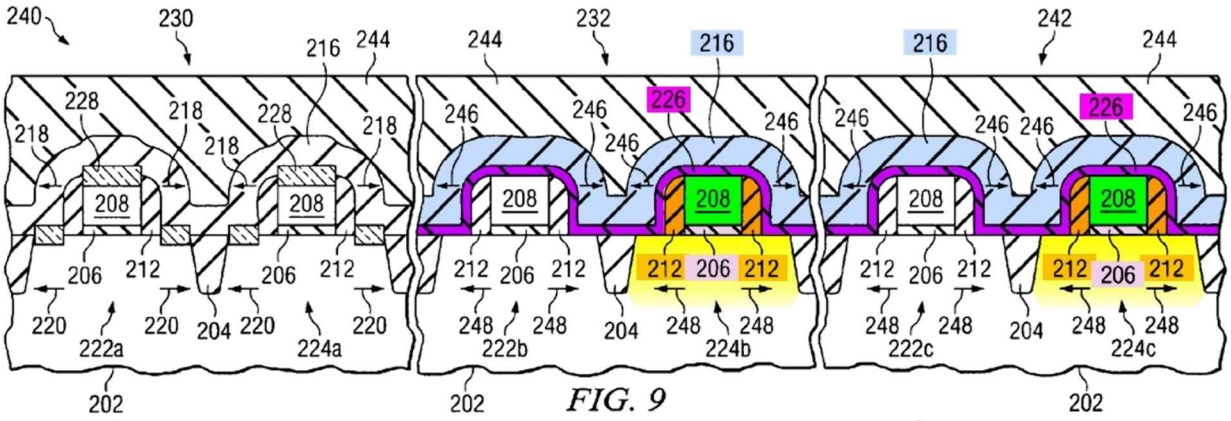


FIG. 9

Alvarez's FIG. 9 (annotated)

(2) [13A]: "a third MIS transistor"

230. A POSITA would have understood that Wu's nFET and pFET structures would be repeated many times in various circuit arrangements over the substrate because it is fundamental to semiconductor technology. *See* Section IX.B.1.k(1) above. For example, Wu discloses a third MIS transistor, such as a second pFET in a second one of the "plurality of first active area[s] [31]." Wu ¶[0017] (explaining that "[a] plurality of first active area[s] and a plurality of second active area[s] are defined on the semiconductor substrate 30"); *see also* Wu ¶[0023], ¶¶[0027]-[0036], ¶[0038], ¶¶[0042]-[0043], ¶¶[0046]-[0055], FIGS. 1-7, 9-14. In the embodiment of the Wu-Alvarez combination shown in Figures E and F below, pFET 224b in PMOS area 31 of non-silicide region 232 corresponds to the third MIS transistor. *See* Section IX.B.1.k(1) above.

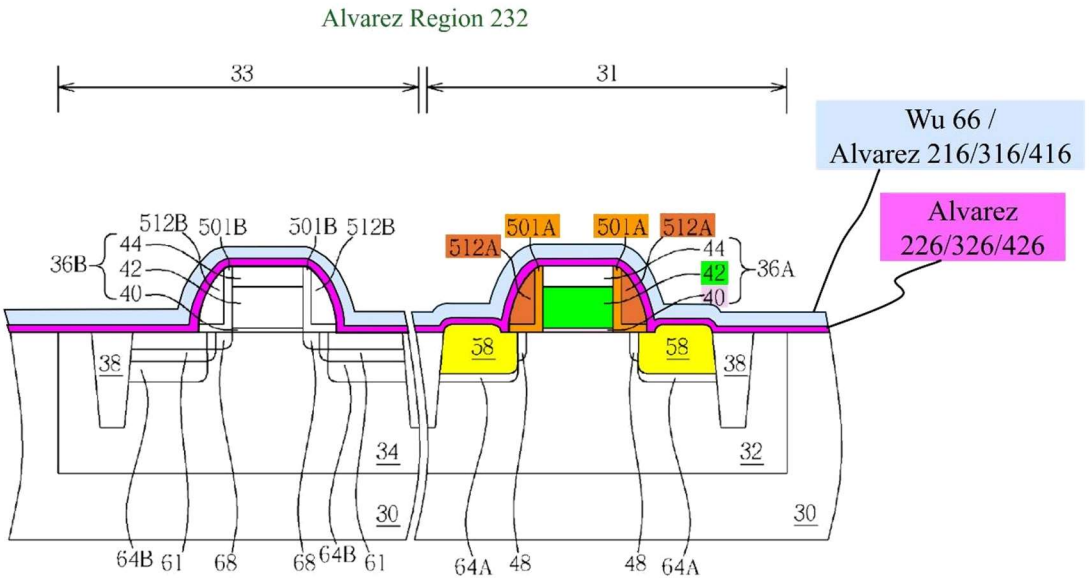


Figure E

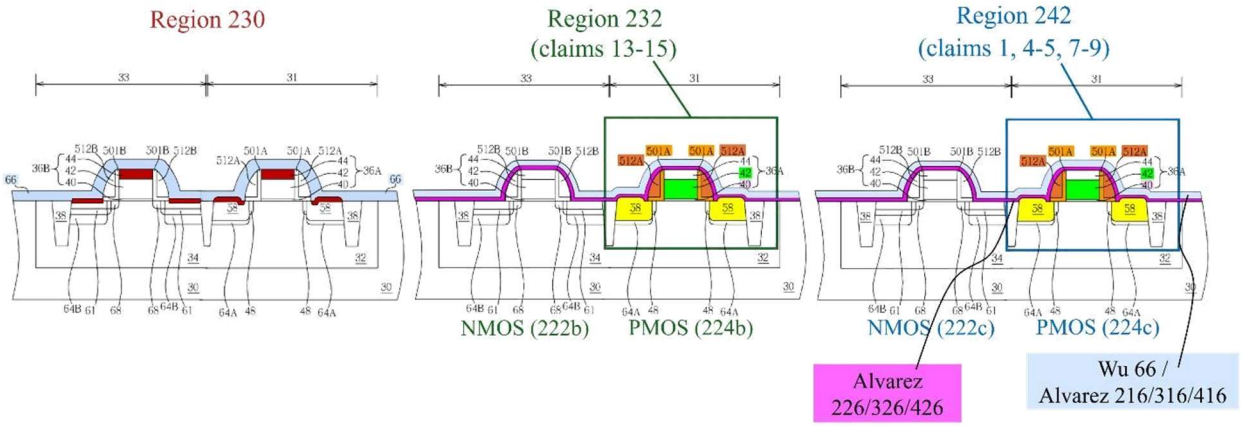
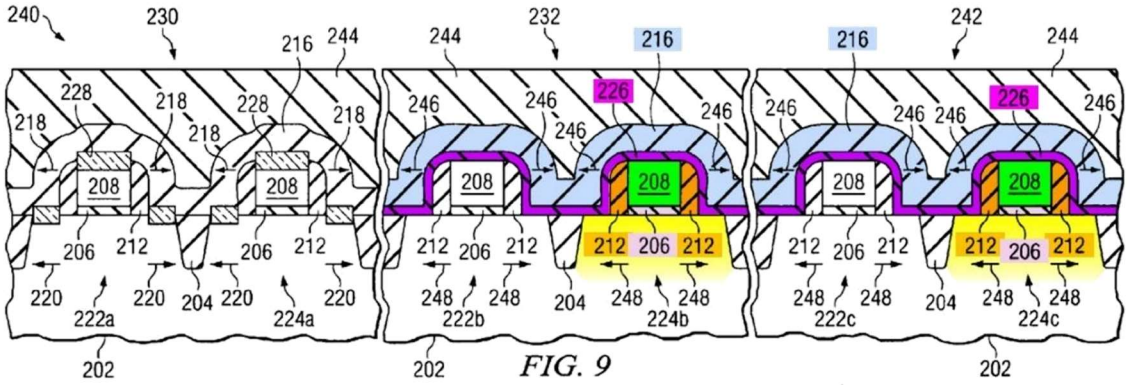


Figure F



Alvarez's FIG. 9 (annotated)

(3) [13B]: "a third gate insulating film formed on a third active region in the semiconductor substrate"

231. The third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, includes a third gate insulating film formed on a third PMOS active region of the semiconductor substrate for the same reasons the first MIS transistor of claim 1 includes a first gate insulating film formed on a first PMOS active region of the semiconductor substrate. *See* Section IX.B.1.b(3) above.

232. Wu discloses a third gate insulating film ("gate dielectric layer 40") formed on a second one of the "plurality of first active area[s]" 31 of "semiconductor substrate 30." Wu ¶[0017] (explaining that "the first active area is a PMOS transistor region 31" and "[a] plurality of first active area[s] . . . are defined on the semiconductor substrate 30"), ¶¶[0038]-[0039] (describing gate structures 36A). As composite Figures E and F show below for this embodiment of the Wu-Alvarez combination, gate dielectric layer 40 (light purple) is formed on a PMOS transistor region 31 in semiconductor substrate 30. *See* Wu ¶[0017], FIGS. 1-7, 9-14. Specifically, pFET 224b in non-silicide region 232 includes a gate dielectric layer 40 formed on a PMOS transistor region 31. *See* Section IX.B.1.a above.

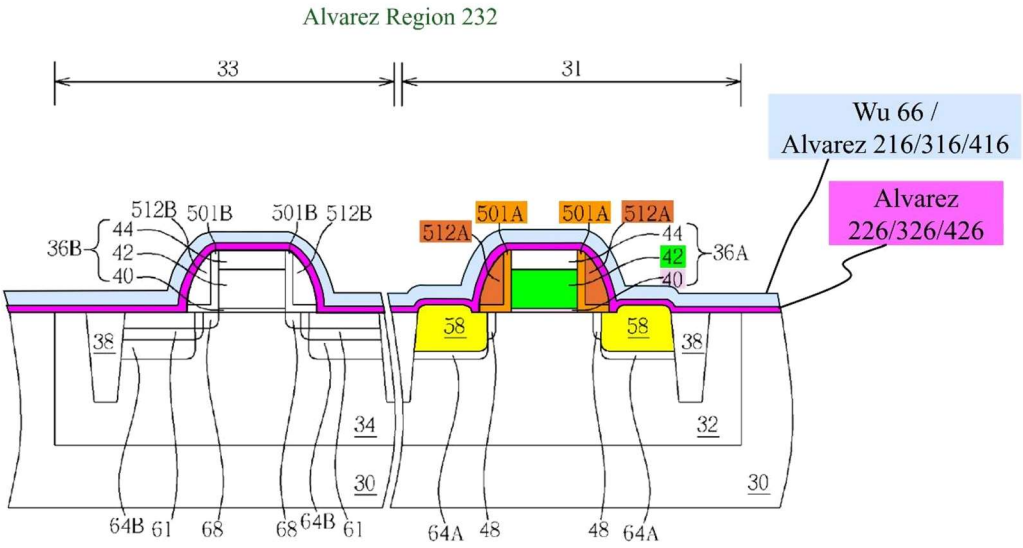


Figure E

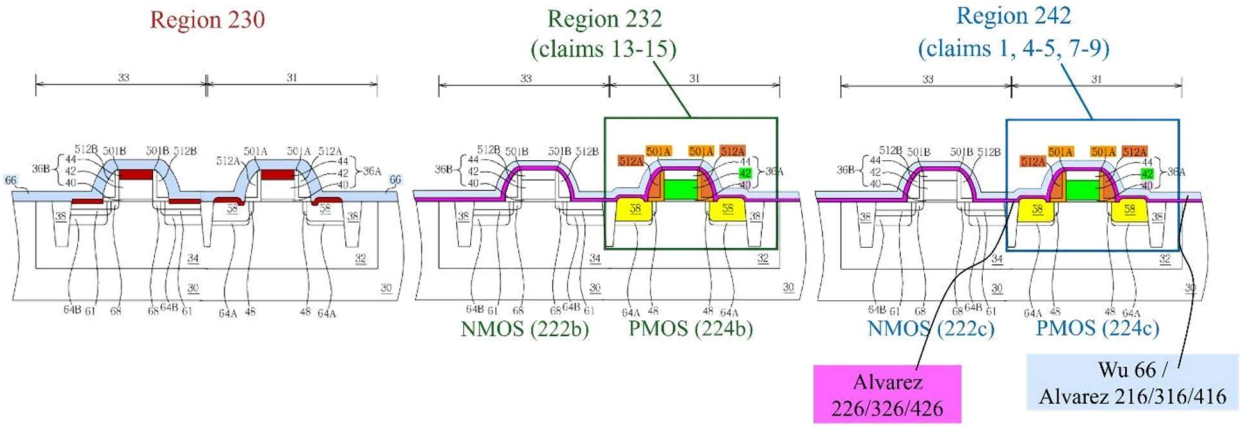
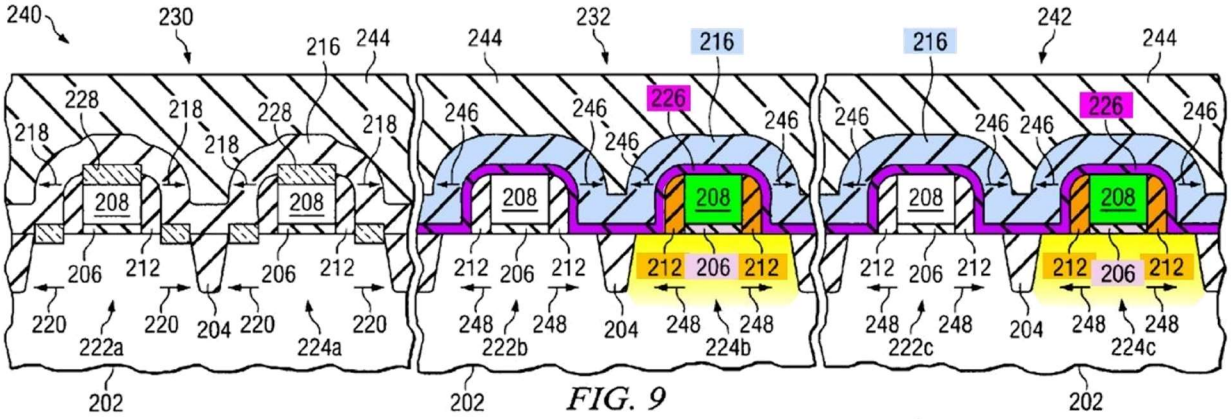


Figure F



Alvarez's FIG. 9 (annotated)

(4) [13C]: "a third gate electrode formed on the third gate insulating film"

233. The third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, includes a third gate electrode 42 formed on the third gate insulating film 40 for the same reasons the first MIS transistor of claim 1 includes a first gate electrode 42 formed on the first gate insulating film 40. *See* Section IX.B.1.b(4) above. Wu discloses a third gate electrode ("gate 42") formed on the third gate insulating film (gate insulating film 40). Wu ¶[0017], FIGS. 7, 14.

234. A POSITA would have understood that gate 42 is a gate electrode made from "polysilicon, silicon germanium (SiGe), metal, silicide, metal nitride, metal oxide, or combinations thereof." Wu ¶[0017]. Gate 42 is used to "connect[] . . . the gate structures 36A, 36B . . . with other electrical devices." Wu ¶[0025]; *see also* Wu ¶[0036], ¶[0055]. As Figures E and F show below for this embodiment of the Wu-Alvarez combination, gate electrode 42 (green) is formed on gate dielectric layer 40 (light purple). *See* Wu ¶[0017], FIGS. 1-7, 9-14. Specifically, pFET 224b in non-silicide region 232 includes a gate electrode 42 (green) formed on gate dielectric layer 40 (light purple). *See* Section IX.B.1.a above.

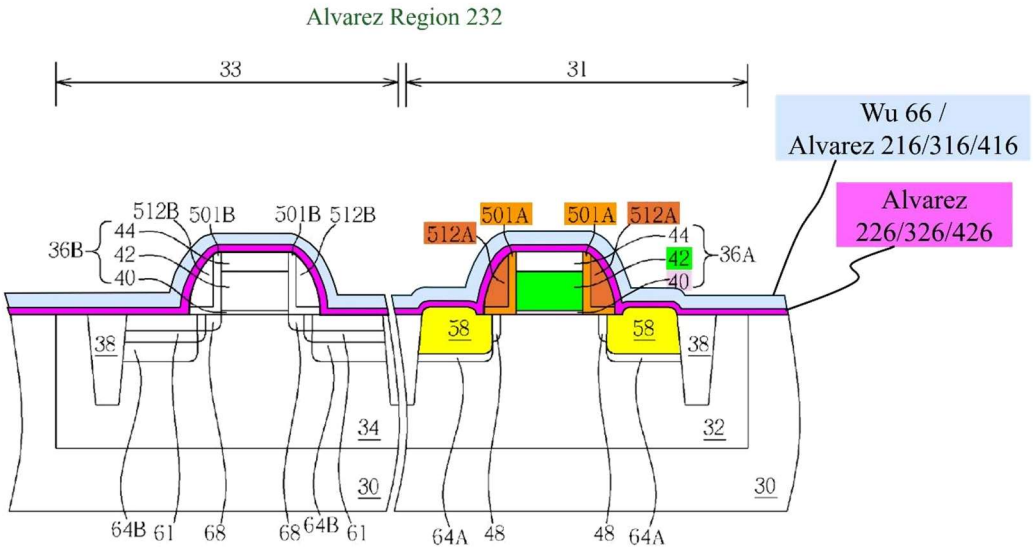


Figure E

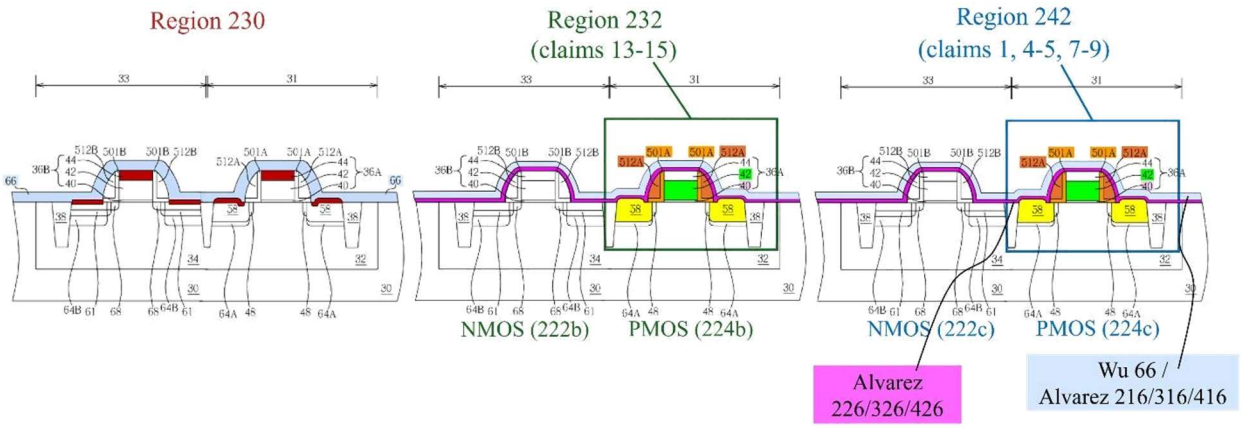


Figure F

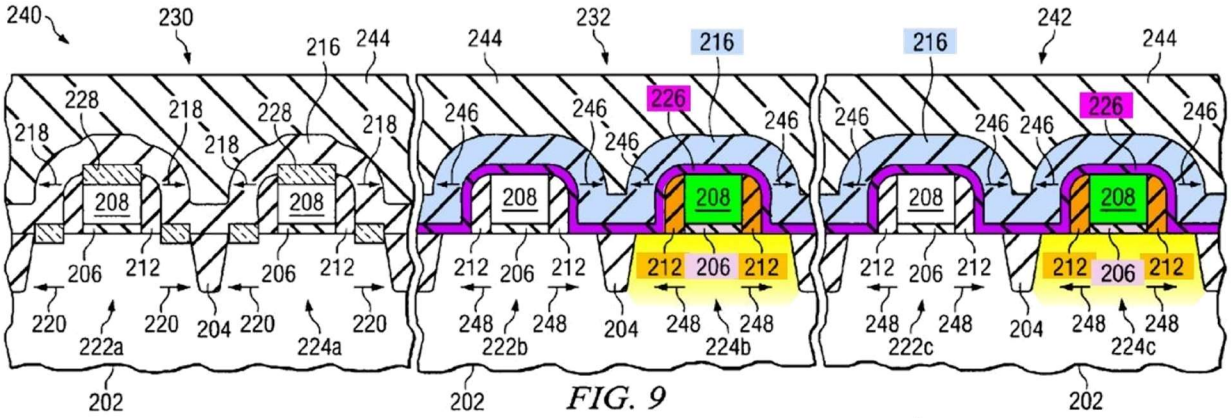


FIG. 9

Alvarez's FIG. 9 (annotated)

(5) [13D]: "a third sidewall spacer formed on a side surface of the third gate electrode"

235. The third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, includes a third sidewall spacer comprising oxide layer 501A[19] for the same reasons the first MIS transistor of claim 1 includes a first sidewall spacer comprising oxide layer 501A. *See* Section IX.B.1.b(5) above.

236. Wu discloses a third sidewall spacer comprising "oxide layer 501A . . . on sidewalls of the gate structure[] 36A." Wu ¶[0017] (further explaining that "[a] plurality of first active area[s] and a plurality of second active area[s] are defined on the semiconductor substrate 30"), ¶[0024], ¶[0043], FIGS. 7, 14. As Wu's FIGS. 7 and 14 show, oxide layer 501A sits on the side surfaces of gate electrode 42 in the plurality of PMOS transistor regions 31. Oxide layer 501A[20] (light orange) forms a third sidewall spacer located on a side surface of third gate electrode 42 (green). As Figures E and F show below for this embodiment of the Wu-Alvarez combination, sidewall spacer layers 501A (orange) are formed on the side surfaces of gate electrode 42 (green). *See* Wu ¶[0017], ¶[0024], ¶[0043], FIGS. 1-7, 9-14. Specifically, pFET 224b in non-silicide region 232 includes third sidewall spacer

[19] *See* note 13 above, Section IX.B.1.b(6).

[20] *See* note 13 above, Section IX.B.1.b(6).

layers 501A[21] (light orange) formed on the side surfaces of gate electrode 42 (green). *See* Section IX.B.1.a above.

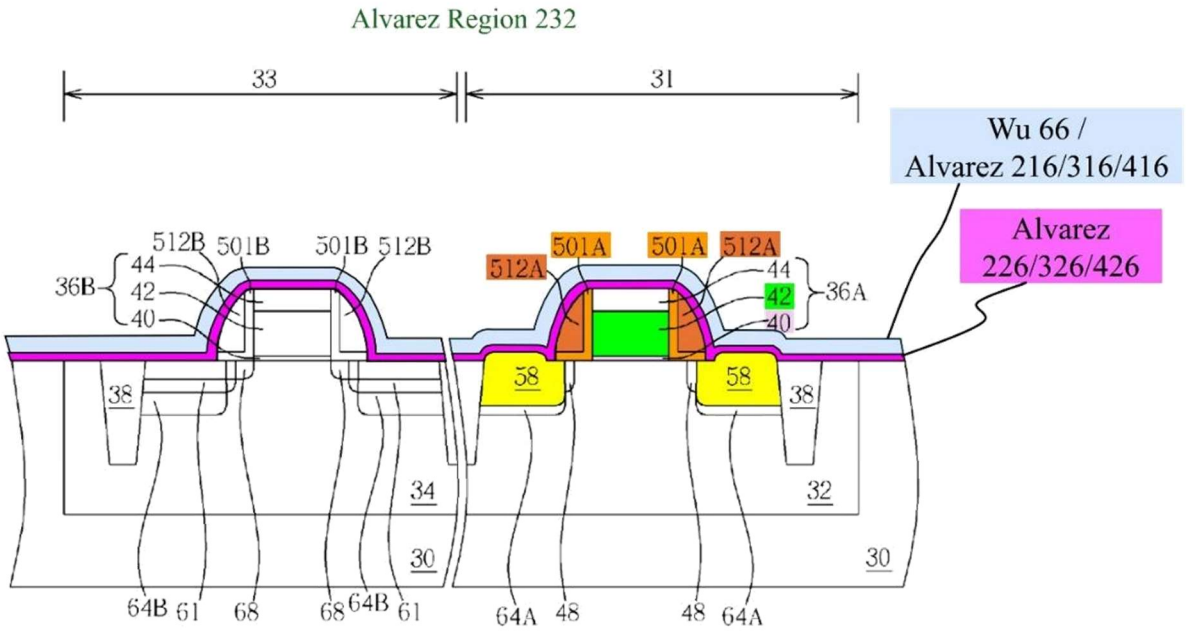


Figure E

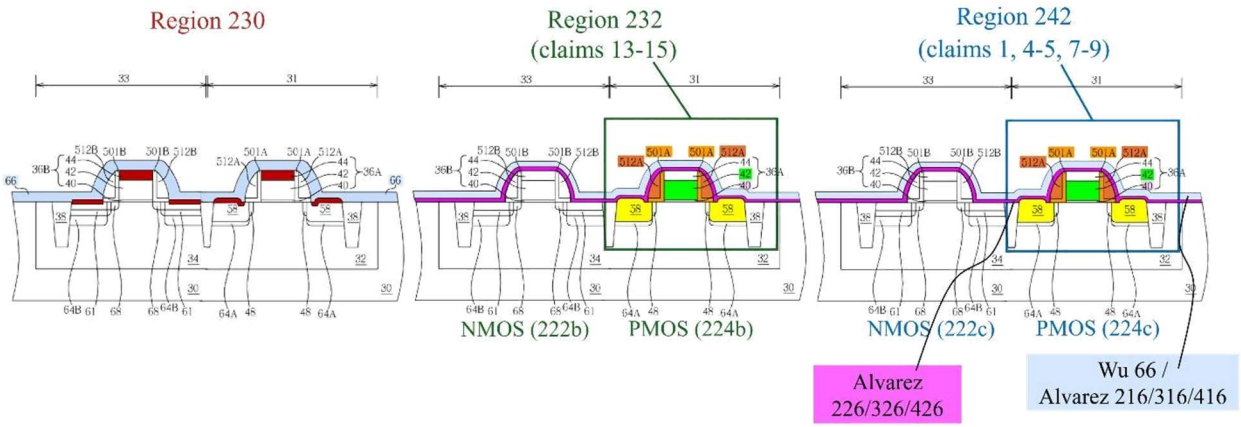
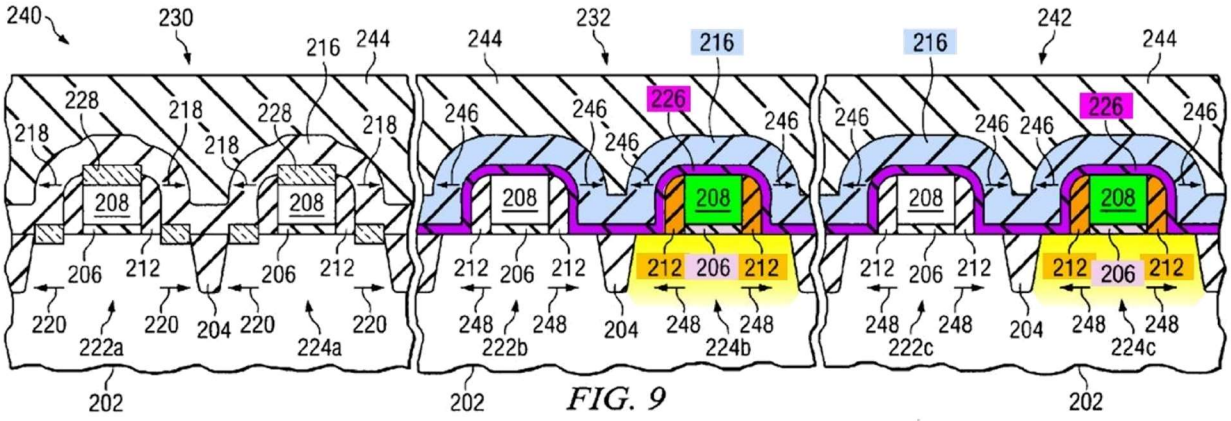


Figure F

[21] *See* note 13 above, Section IX.B.1.b(6).



Alvarez's FIG. 9 (annotated)

(6) [13E]: "a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer"

237. The third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, includes a third source/drain region of a third (p-type) conductivity type formed on the third active region (a second PMOS active region 31) on a lateral side of third sidewall spacer layer 501A[22] for the same reasons the first MIS transistor of claim 1 includes a first source/drain region of a first (p-type) conductivity type formed on the first active region (a first PMOS active region 31) on a lateral side of first sidewall spacer layers 501A. *See* Sections IX.B.1.b(4) and IX.B.1.b(6) above.

238. Wu discloses a third source/drain region in a second one of the "plurality of first active area[s]" 31. Wu ¶[0017]. Like the first source/drain region,

[22] *See* note 13 above, Section IX.B.1.b(6).

the third source/drain region includes a p-type "epitaxial layer 58 of silicon germanium." *See* Wu ¶[0021], ¶[0041], FIGS. 7, 14. Wu's third source/drain region is formed in the third active region on a lateral side of the third sidewall spacer for the same reasons the first source drain region is formed in the first active region on a lateral side of the first sidewall spacer because the third and first MIS transistors are essentially the same structures. *See* Sections IX.B.1.k(1) and IX.B.1.b(6) above. As Figures E and F show below for this embodiment of the Wu-Alvarez combination, the third source/drain region (SiGe layer 58, yellow) is formed in the third active region 31 on a lateral side of third sidewall spacer layers 501A (light orange) and 512A (dark orange). *See* Wu ¶¶[0017]-[0018], ¶[0021], ¶[0024], ¶[0038], FIGS. 7, 14. Specifically, pFET 224b in non-silicide region 232 includes epitaxial SiGe layers 58 (yellow) formed in the third active region (second PMOS area 31) on a lateral side of third sidewall spacer layers 501A (light orange) and 512A (dark orange). *See* Section IX.B.1.a above.

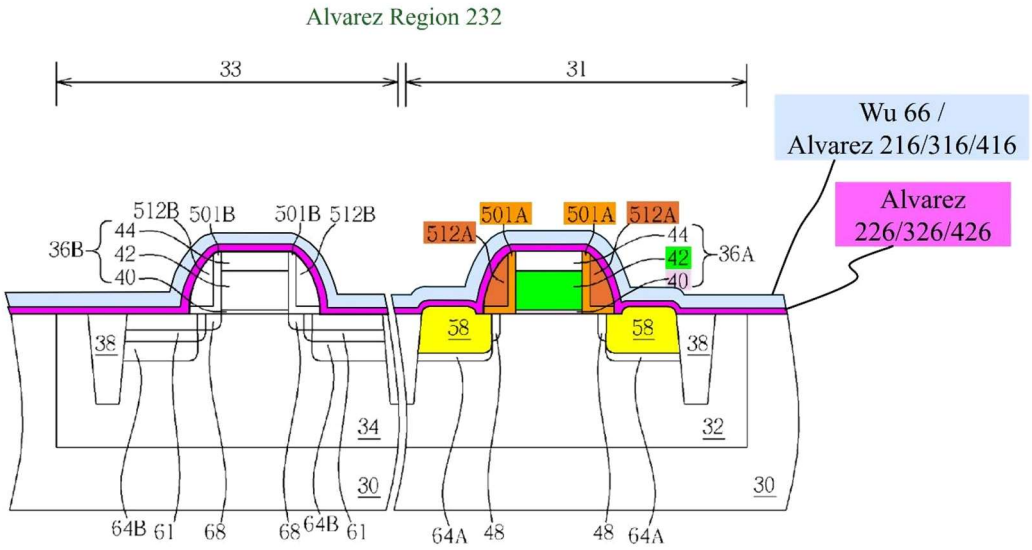


Figure E

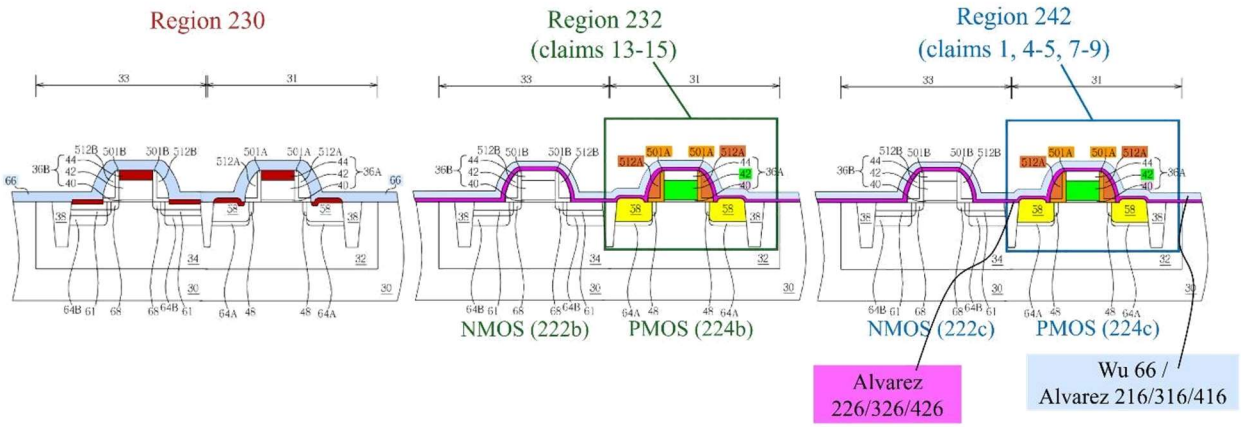
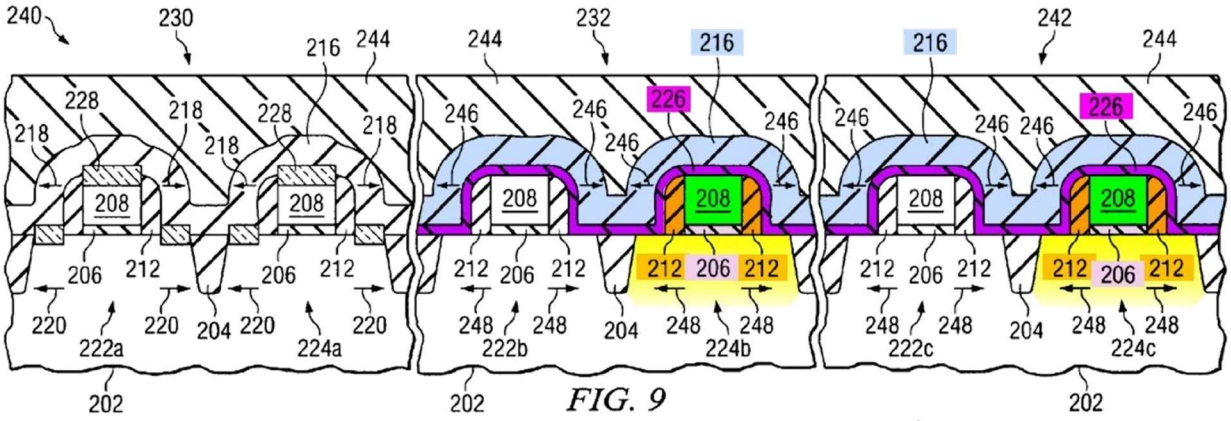


Figure F



Alvarez's FIG. 9 (annotated)

(7) [13F]: "a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region"

239. The third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, includes the same protective film that corresponds to the stress-relief film of claim 1 (the one like Alvarez's stress-controlling layer 226/326/426). *See* Section IX.B.1.a. Like the stress-relief film of claim 1, it covers the third gate electrode, third sidewall spacer, and third source/drain region for the same reasons it covers the first gate electrode, first sidewall spacer, and first source/drain region in claim 1. *See* Sections IX.B.1.a and IX.B.1.b(9)-IX.B.1.b(11) above.

240. In the Wu-Alvarez combination, the stress-relief film (analogous to Alvarez's layer 226/326/426) is used both as a stress-relief film to mitigate CESL stress and as a protective film to prevent silicide formation in certain circuit regions (like in Alvarez's non-silicide region 232 and stress-control region 242). *See* Sections IX.B.1.a and IX.B.1.b(9) above. As in Alvarez's FIG. 9, composite Figures E and F below show the stress-controlling film/protective film (magenta) covering a plurality of transistors (including pFET 224b in non-silicide region 232 and pFET 224c in stress-control region 242) across the plurality of PMOS active regions 31. *See* Section IX.B.1.a above; Alvarez, FIG. 9. Specifically, in the embodiment of the Wu-Alvarez combination shown in Figures E and F, the stress-

controlling film/protective film (magenta) covers the third gate electrode 42 (green), the third sidewall spacer layers 501A (light orange) and 512A (dark orange), and the third epitaxial SiGe source/drain regions 58 (yellow) of the third MIS transistor (pFET 224b in non-silicide region 232). *See* Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶[0078], FIGS. 9-11; Section IX.B.1.a above.

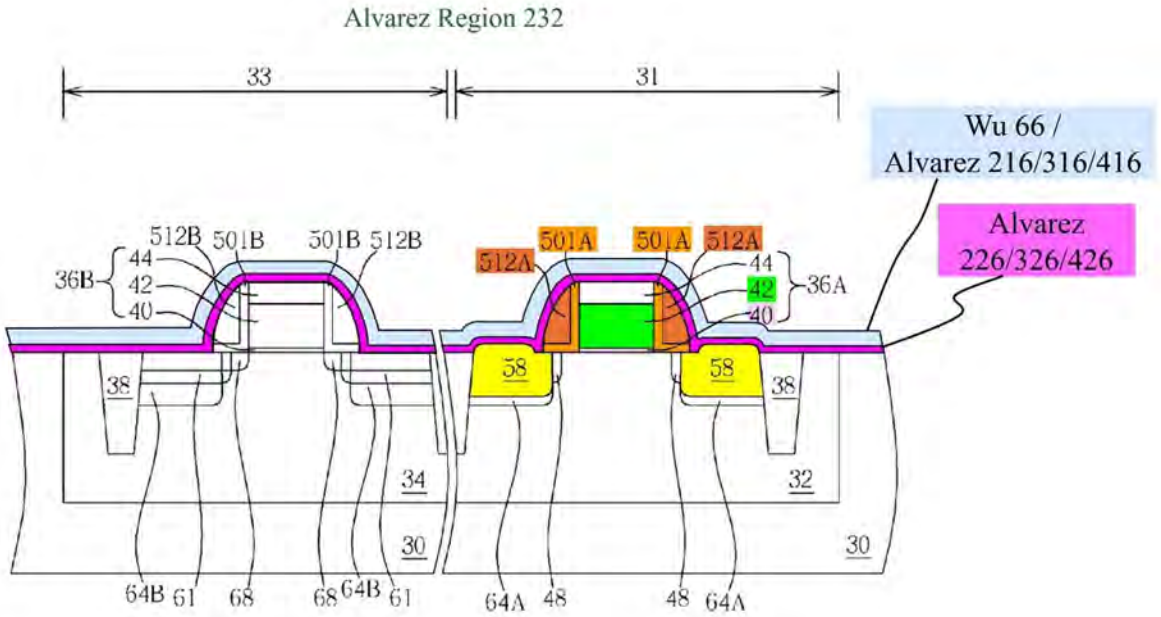


Figure E

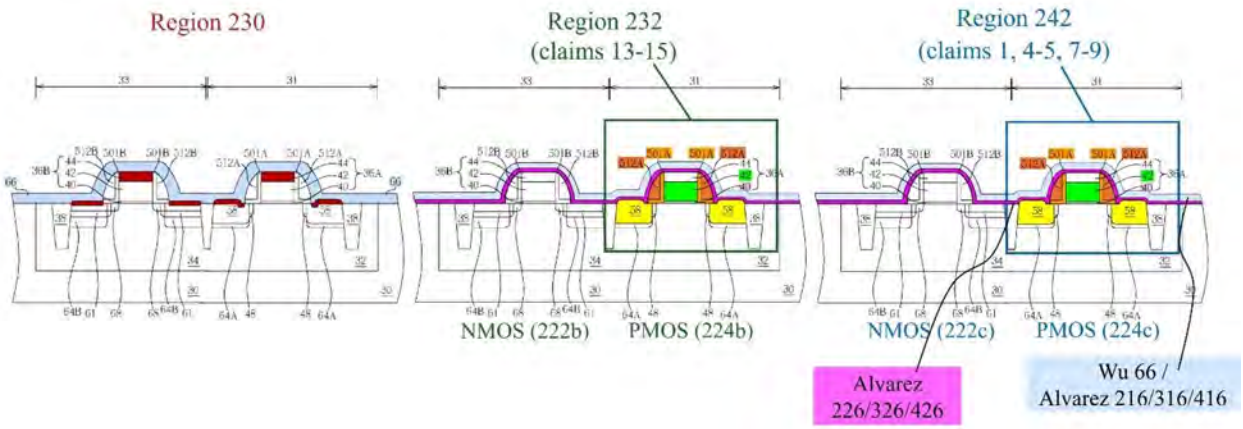
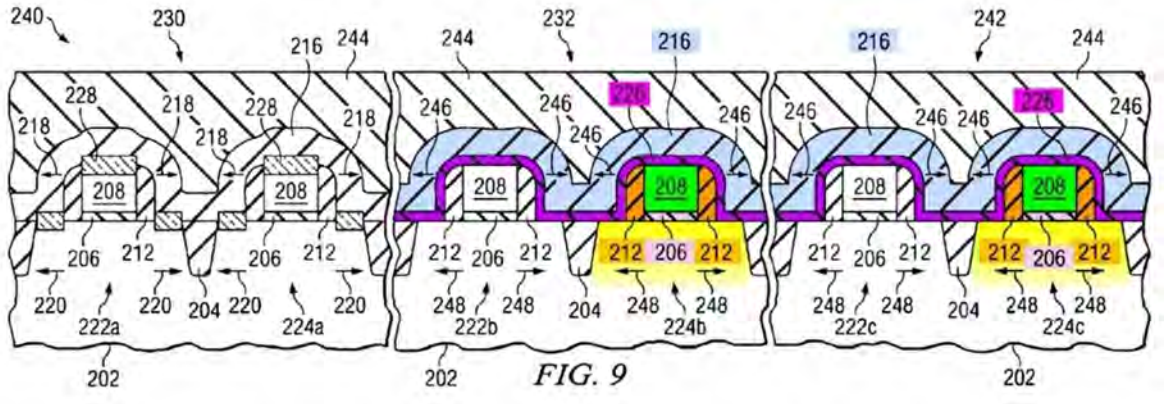


Figure F



Alvarez's FIG. 9 (annotated)

(8) [13G]: "the stress insulating film formed on the protective film"

241. In the third MIS transistor of claim 13, which has essentially the same structure as the first MIS transistor of claim 1, the stress insulating film (tensile CESL 66 analogous to Alvarez's tensile stress-inducing film 216/316/416) is formed on the protective film/stress relief film (analogous to Alvarez's stress-controlling layer 226/326/426) for the same reasons discussed for the first MIS transistor of claim 1. *See* Sections IX.B.1.a and IX.B.1.b(7) above.

242. This embodiment of the Wu-Alvarez combination, shown in composite Figures E and F, includes a stress-inducing film (a tensile CESL 66, analogous to Alvarez's stress-inducing layer 216/316/416) formed over the protective film/stress relief film (analogous to Alvarez's layer 226/326/426). *See* Sections IX.B.1.a and IX.B.1.b(7) above; Alvarez ¶[0043], ¶[0047], ¶¶[0055]-[0056], ¶[0073] (explaining that "one material layer 226, 326, 350, 426, and 450 is disposed under another material layer 216, 316, or 416"), FIGS. 9-11; Wu ¶[0025], ¶[0044], FIGS. 7, 14.

243. As in Alvarez's FIG. 9, Figures E and F below show that the stress insulating film (a tensile CESL 66, analogous to Alvarez's stress-inducing layer 216/316/416, light blue) is formed over the stress-controlling film/protective film (analogous to Alvarez's layer 226/326/426, magenta). *See* Sections IX.B.1.a and IX.B.1.b(9) above; Alvarez ¶[0037], ¶¶[0043]-[0044], ¶[0047], ¶¶[0050]-[0056], ¶[0073], FIGS. 9-11. Specifically, in the embodiment of the Wu-Alvarez combination shown in Figures E and F, the stress insulating film (light blue) is formed over the stress-controlling film/protective film (magenta) in the third MIS transistor (pFET 224b in non-silicide region 232). *See* Alvarez ¶[0037], ¶¶[0043]-[0044], FIGS. 9-11; Section IX.B.1.a above.

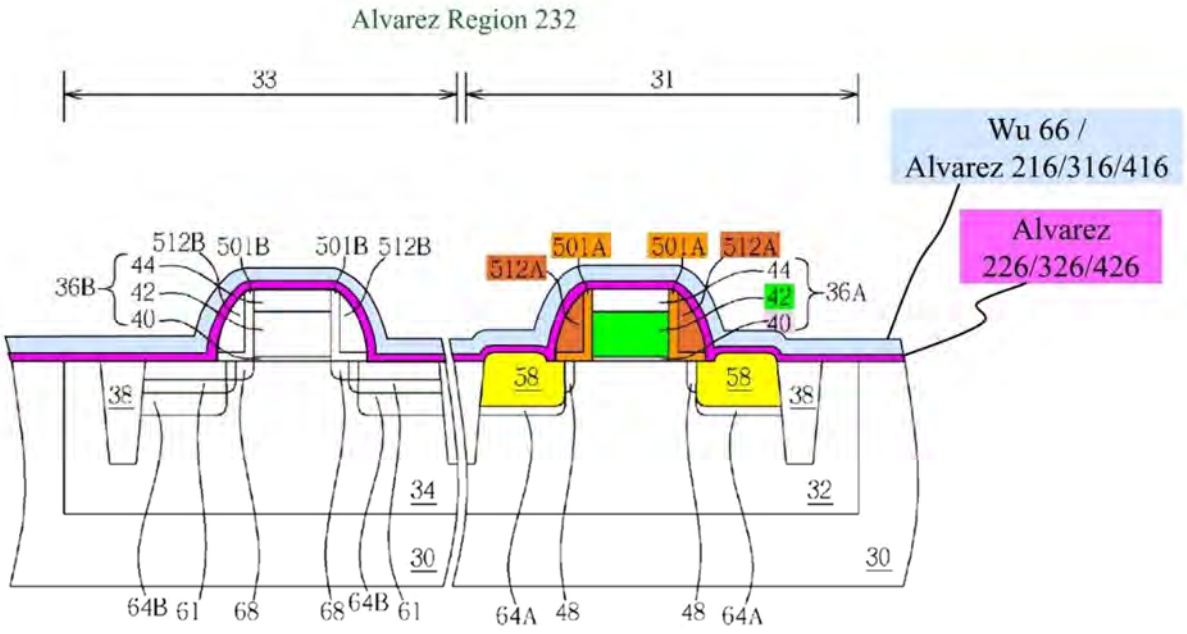


Figure E

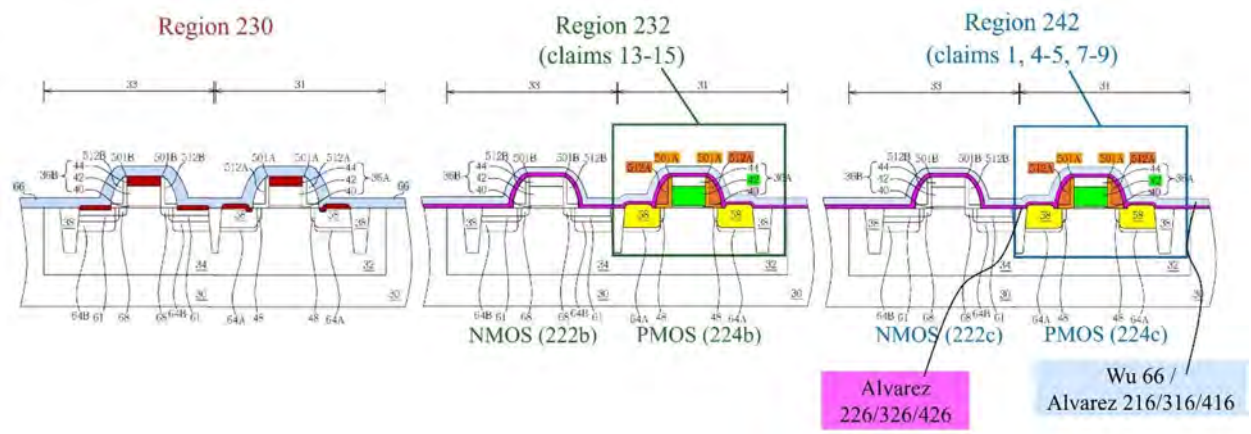
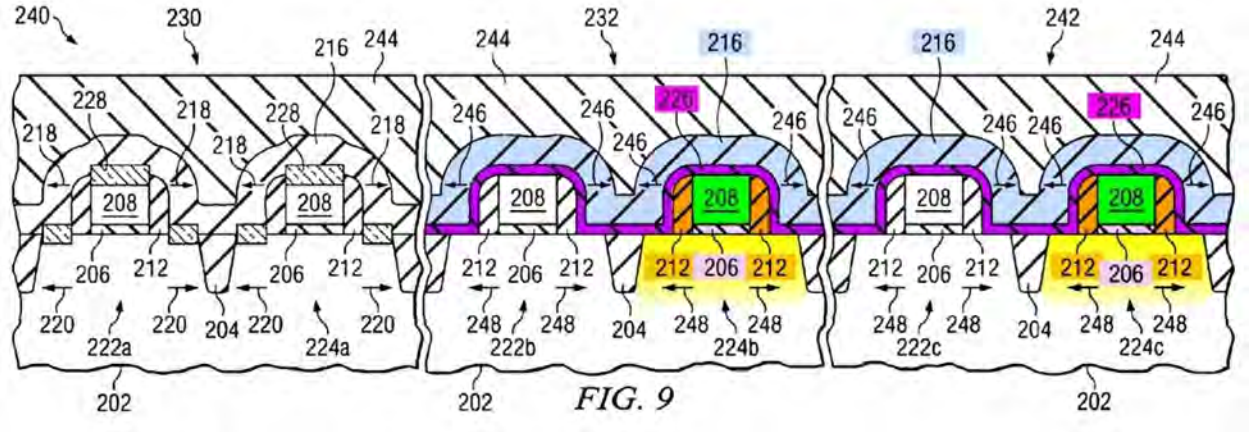


Figure F



Alvarez's FIG. 9 (annotated)

l. Claim 14: "The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region"

244. In my opinion, the Wu-Alvarez combination renders claim 14 obvious.

245. The Wu-Alvarez combination renders the semiconductor device of claim 13 obvious. *See* Sections IX.B.1.a and IX.B.1.k above.

246. As I explain above in Section IX.B.1.a and for claim 13 (*see* Section IX.B.1.k above), a POSITA would have found it obvious to block silicide formation in certain circuit regions (analogous to Alvarez's non-silicide region 232) by using

a protective film/stress-controlling film (analogous to Alvarez's stress-controlling layer 226/326/426). *See* Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶[0078], FIG. 9; Sections IX.B.1.a, IX.B.1.b(9), and IX.B.1.k above. In these protected regions, no silicide forms on the gate electrode or the source/drain regions of the third MIS transistor because the protective film/stress-controlling film blocks silicide formation there. Alvarez explains that stress-controlling film 226/326/426 "preferably comprises a masking material layer (e.g., such as the masking material layer 126 shown in FIGS. 3 and 4) that was previously used, e.g., in earlier design stages of the semiconductor device 240 for other purposes, such as for silicidation protection." Alvarez ¶[0045]; *see also* Alvarez ¶[0012], ¶[0028], ¶[0068], ¶[0075], FIGS. 7-9. Alvarez further explains that "the first material 226 or masking material layer provides stress control in those regions, e.g., in the third region 242, as shown in FIG. 7." Alvarez ¶[0045]. Accordingly, in the embodiment of the Wu-Alvarez combination Figures E and F show below, the third MIS transistor (pFET 224b in non-silicide region 232) lacks a silicide layer like the ones (dark red) that form in silicide region 230. *See* Section IX.B.1.a above.

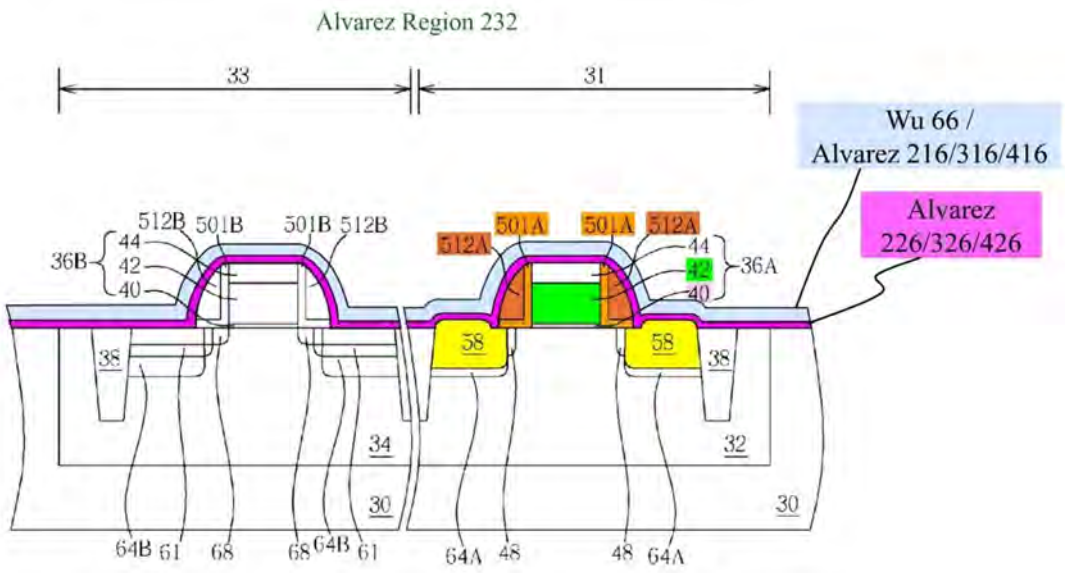


Figure E

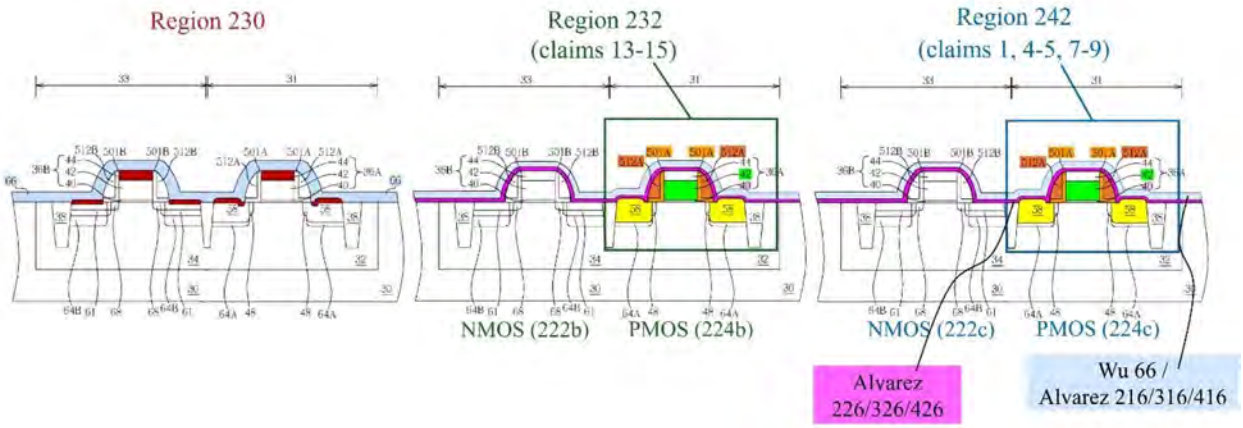
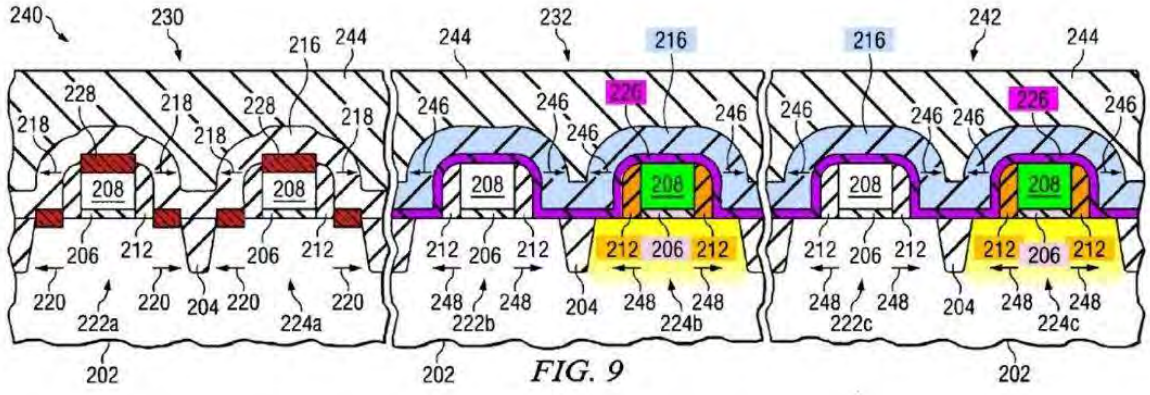


Figure F



Alvarez's FIG. 9 (annotated)

m. Claim 15: "The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material"

247. In my opinion, the Wu-Alvarez combination renders claim 15 obvious.

248. The Wu-Alvarez combination renders the semiconductor device of claim 13 obvious. *See* Sections IX.B.1.a and IX.B.1.k above.

249. As I explain for claims 1 and 13, the first stress-relief film (claim 1) and the protective film (claim 13) are both analogous to Alvarez's stress-controlling/silicide masking layer 226/326/426. *See* Sections IX.B.1.a, IX.B.1.b(9), and IX.B.1.k above; Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶¶[0063]-[0065], ¶[0078], FIGS. 9-11. The same film serves as both the stress-relief film and the protective film, the only difference being that the former covers pFET 224c in stress-control region 242, whereas the latter covers pFET 224b in non-silicide region 232. *See* Sections IX.B.1.a, IX.B.1.b(9), and IX.B.1.k above.

250. Accordingly, as Figure E shows above (and as in Alvarez's FIG. 9), both the stress-relief film and the protective film—being part of the same physical layer—are made of the same insulating material: silicon oxide. *See* Alvarez ¶[0043] (explaining that this film may be "an oxide such as silicon dioxide"), claim 13 (reciting a "silicon dioxide" stress-controlling/silicide masking material), FIGS. 9-10; Sections IX.B.1.a, IX.B.1.b(9), IX.B.1.k, and IX.B.1.l above.

251. The ’425 Patent is the same in this regard. In the ’425 Patent, a single material layer provides both the stress-relief film for claim 1 and the protective film for claims 13-15. *Compare* Alvarez ¶¶[0034]-[0035], ¶[0037], ¶¶[0043]-[0045], ¶¶[0063]-[0065], ¶[0078], FIGS. 9-10, *with* ’425 Patent, 12:59-13:19, FIGS. 5A-6B.

2. Ground 1B: The Combination of Wu, Alvarez, and Wolf Renders Claim 2 Obvious

a. The Wu-Alvarez-Wolf Combination Would Have Been Obvious

252. In my opinion, a POSITA would have found it obvious to modify the Wu-Alvarez combination described above (*see* Section IX.B.1.a above) to add an I-shaped offset spacer, as Wolf discloses, to Wu’s sidewall structures 36A and 36B.

253. Wolf discloses an I-shaped “offset-spacer [being] fabricated on the side of the gate after the gate-poly is etched.” Wolf, 217, Fig. 5-25. Wolf explains that the I-shaped offset spacer “yields optimum device characteristics” in the channel region by spacing it apart from the source-drain extension (“SDE”) and preventing “excessive leakage (due to larger short-channel effects that arise if the channel-length is too small).” Wolf, 216-17, Fig. 5-25.

254. In addition to Wolf’s teachings, a POSITA would have known I-shaped offset spacers were commonly used structures to facilitate control over source/drain extension profiles and to mitigate short channel effects. *See* Thompson1998, 132, Fig. 2 (describing offset spacers to control source/drain extension profiles);

Suzuki995 ¶[0061] (explaining that offset spacers act as masks to "form p-type extension regions"), FIG. 1(b); Fleetwood, Tbl. 3.1 (describing I-shaped offset spacers as "optional" in a "Typical CMOS Process Flow"); Wiatr ¶[0033]; Kammler ¶[0024] ("A width of the offset spacer 105 is selected in accordance with process requirements for forming the lateral dopant profile of extension regions 106 formed within the substrate 101 adjacent to the channel region 104."), FIGS. 1a-2; Wei ¶[0058] (explaining that "offset spacer 231 may be used for defining an extension region 211"), FIGS. 2c-2h; Suzuki465 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C.

255. Having known of Wolf's teachings and being aware of the purpose and benefits of I-shaped offset spacers, a POSITA would have been motivated to add Wolf's I-shaped offset spacers to Wu's transistors, as the exemplary embodiment of Figure G below shows, to mitigate short channel effects and better control the doping profiles of PLDD regions 48 and NLDD regions 61. Figure G shows Wu's FIG. 9 as modified to show I-shaped offset spacers, as Wolf discloses, as that structure would have existed before implanting extension regions 48 in PMOS transistor region 31.

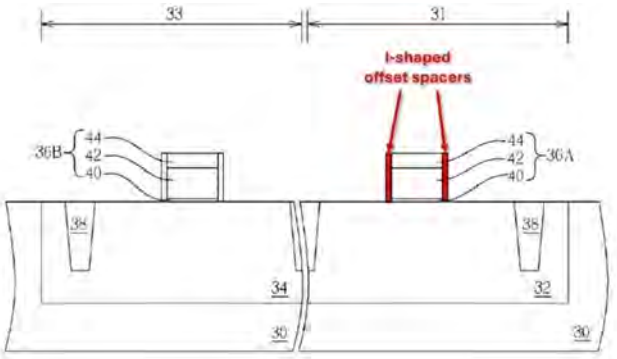
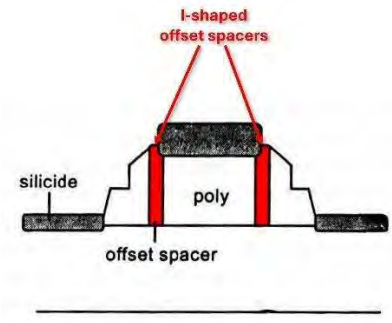


Figure G



Wolf's Fig. 5-25 (annotated)

256. In my opinion, a POSITA would have reasonably expected to succeed when adding an I-shaped offset spacer, as Wolf discloses, to Wu's FETs (*see* Figure G) because it represents a conventional use of known techniques to achieve ordinary and expected results (i.e., reduced short channel effects and better control over source/drain extension regions). *See* Wolf, 217, Fig. 5-25; Suzuki995 ¶[0061]; Thompson1998, 132, Fig. 2; Fleetwood, Tbl. 3.1; Wiatr ¶[0033]; Kammler ¶[0024], FIGS. 1a-2; Wei ¶[0058], FIGS. 2c-2h; Suzuki465 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C. Such known techniques include forming an offset spacer either by thermal oxidation or by deposition and etching, as the references cited above describe. As Wolf demonstrates, a POSITA would have understood to form such I-shaped offset spacers before forming Wu's sidewalls 501A/502A, as in Figures G (above) and H (below), then subsequently forming source/drain extension regions 48 and 61. Wolf, 216-17, Fig. 5-25. A POSITA would have understood that Wu's processing would then proceed as described. *See* Section IX.B.1.a above; Suzuki995 ¶¶[0062]-[0068], FIGS. 1(b)-2(c).

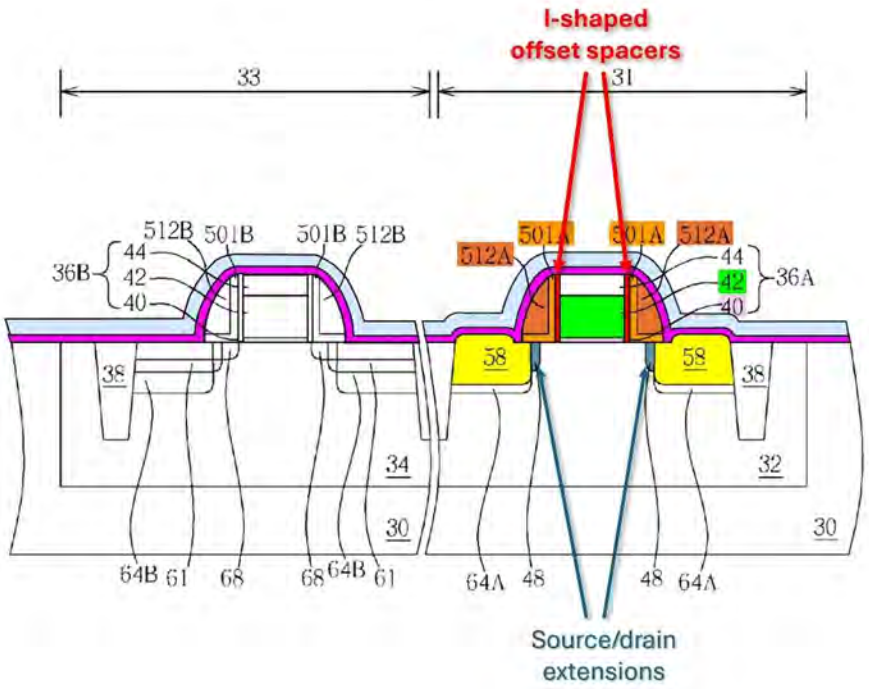
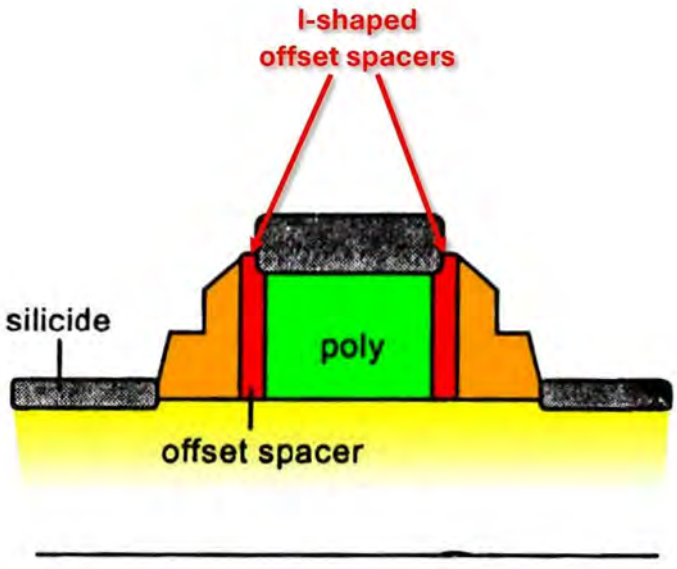


Figure H



Wolf, Fig. 5-25 (annotated)

257. In my opinion, a POSITA would have found it obvious to add I-shaped offset spacers, as Wolf discloses, to Wu's FETs in the Wu-Alvarez combination of claim 1 because it is an example of the following:

- It combines known prior art elements according to known methods (forming an I-shaped offset spacer before forming source/drain extension regions) to yield predictable results (better control over source/drain extension profiles and reduced short channel effects).
- It uses a known technique (forming a standard I-shaped offset spacer, as Wolf and others disclose) to improve similar devices (Wu's MOSFETs) in the same way (e.g., by mitigating short channel effects and better controlling source/drain extension profiles).
- It applies known techniques (forming a standard I-shaped offset spacer, as Wolf and others disclose) to a known device ready for improvement (Wu's MOSFETs) to yield predictable results (reduced short channel effects and better control over source/drain extension profiles).
- It applies a known teaching, motivation, or suggestion in the prior art (e.g., the teachings of Wolf and others described above) that would have led a POSITA to modify Wu according to, or to combine Wu with, the teachings of Wolf to arrive at the claimed invention.

b. Claim 2: "The semiconductor device of claim 1, further comprising: a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape"

258. In my opinion, the Wu-Alvarez-Wolf combination renders claim 2 obvious.

259. The Wu-Alvarez combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.B.1.a and IX.B.1.b above.

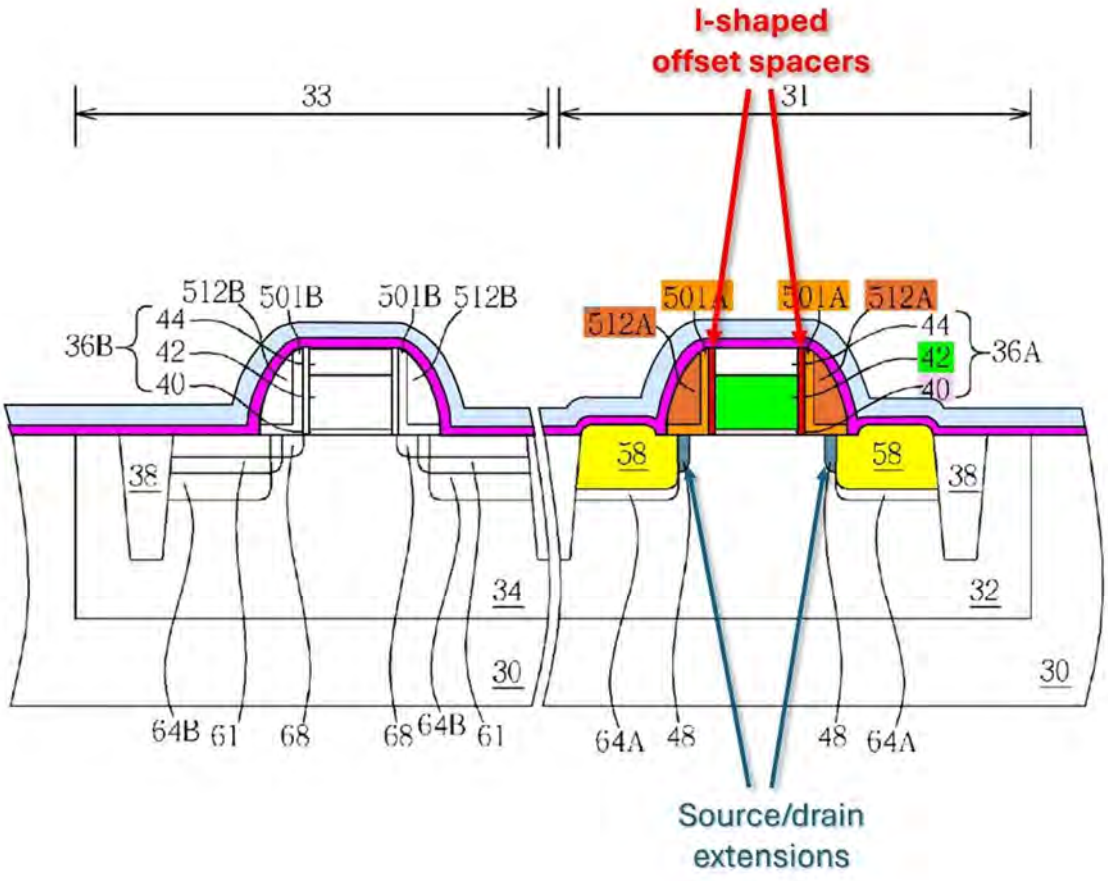


Figure H

260. As I explain above in Section IX.B.2.a, a POSITA would have found it obvious to add I-shaped offset spacers (like the ones Wolf discloses) between Wu's gate electrode 42 and sidewall spacer layers 501A and 512A to control the profile of extension regions PLDD 48 and NLDD 61. *See* Section IX.B.2.a above. As I also explain above, a POSITA would have recognized that this modification would have yielded a structure like the one in Figure H above, which represents an embodiment of the Wu-Alvarez-Wolf combination. *See* Section IX.B.2.a above.

C. Grounds 2A-2D: Cheng Grounds

261. In my opinion, Cheng alone and the combination of Cheng and Wang both render claims 1, 3-9, 11, and 12 obvious.

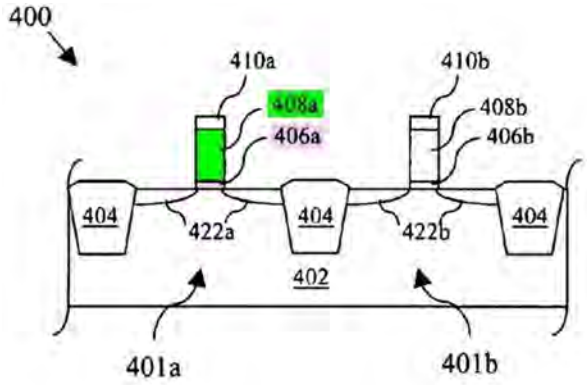
262. Further, in my opinion, the combination of Cheng and Wolf and the combination of Cheng, Wang, and Wolf both render claim 2 obvious.

263. In reviewing Cheng, I have analyzed its description and figures and, in my opinion, a POSITA would have found that Cheng's textual descriptions are clear. Although some of the figures do not accurately reflect all the details described in the text because of variations from figure to figure, such as in Figs. 4e-4j, a POSITA would have understood the processes clearly described in Cheng's text and would have understood how its figures, including Fig. 4j, should appear in that context.

264. Additionally, Wang provides clear evidence confirming what those understandings would have been. Wang, like Cheng, describes an MOS device

structure formed using similar processes, and a POSITA would have understood that Wang's figures help to illustrate how a POSITA would have understood Cheng's textual descriptions. *Compare* Cheng ¶¶[0056]-[0070], Figs. 4a-4j, *with* Wang ¶¶[0023]-[0032], FIGS. 4-9.

265. Cheng explains that Figs. 4a-4j show "sectional views . . . for making semiconductor devices 401a and 401b." Cheng ¶[0056]. Wang's FIGS. 4-9 show similar "cross-sectional views of intermediate stages in the fabrication of" a pMOS device. Wang ¶[0019]. As the comparison below illustrates, Cheng's Fig. 4a mirrors Wang's FIG. 4. Both figures show the formation of a gate dielectric film (layer 406a in Cheng and layer 104 in Wang, both shaded light purple below) and a gate electrode (layer 408a in Cheng and layer 106 in Wang, both shaded green below). *Compare* Cheng ¶[0056], Fig. 4a, *with* Wang ¶[0023], FIG. 4.



Cheng's Fig. 4a (annotated)

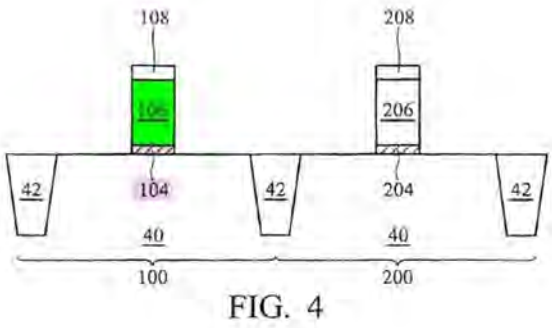
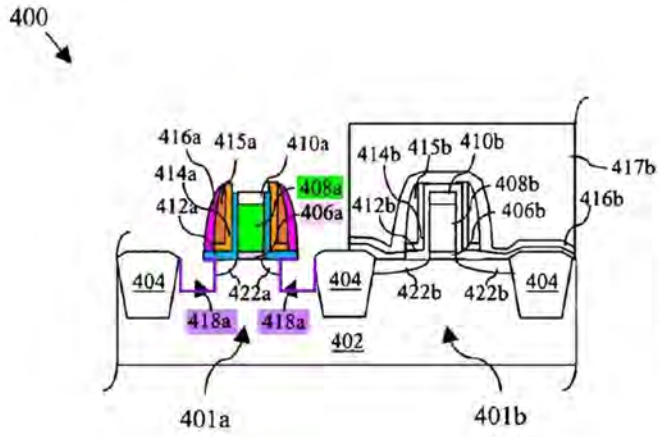


FIG. 4

Wang's FIG. 4 (annotated)

266. As shown in the next figure comparison below, Cheng's Figs. 4b-4d show the same processes as Wang's FIGS. 5-8, including the formation of gate

electrode sidewalls (orange, blue) and dummy spacers (magenta), which are followed by etching recesses (purple) into the substrate for subsequent epitaxial SiGe growth. *Compare* Cheng ¶¶[0061]-[0063], Figs. 4b-4c, *with* Wang ¶¶[0025]-[0028], FIGS. 5-8. Wang's FIG. 9 on the right below has been modified to remove the epitaxially grown SiGe to correspond to Cheng's process step shown in Fig. 4d. In Cheng's pFET 401a of Fig. 4d (on the left below), the sidewall dielectric layer 412a (blue) sits beneath the dummy spacer 416a (magenta). Because of the way in which it is formed, sidewall dielectric layer 412a (blue) stops laterally at the outer edge of dummy spacer 416a (magenta). Cheng ¶[0064], Fig. 4d. Wang's modified FIG. 9 on the right below is similar. Wang's sidewall spacer inner portion 120_1 (burnt orange) also sits beneath sidewall spacer outer portion 120_2 (magenta). Because of the way in which it is formed, sidewall spacer inner portion 120_1 (burnt orange) stops laterally at the outer edge of sidewall spacer outer portion 120_2 (magenta). *See* Wang ¶[0030], FIG. 9.



Cheng's Fig. 4d (annotated)

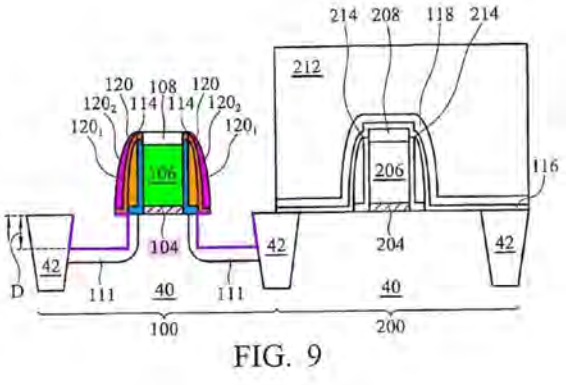
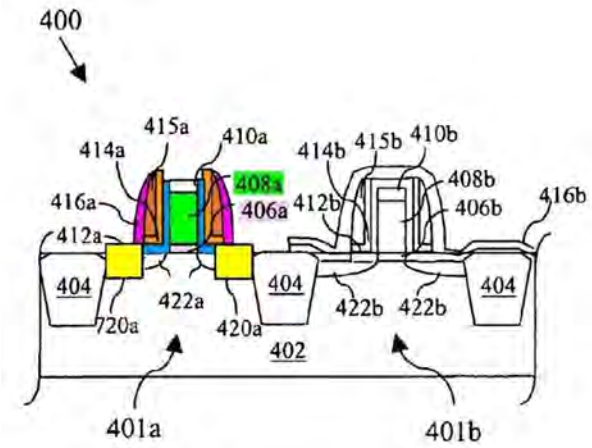


FIG. 9

Modified Wang's FIG. 9

(modified to remove SiGe, annotated)

267. As the next figure comparison below illustrates, Cheng's Fig. 4e and Wang's FIG. 9 both show growing epitaxial SiGe layers (Cheng's layers 420a[23] and Wang's layers 124_1, 124_2, both shaded in yellow below) in trenches (recesses) of the substrate, such that the SiGe layers extend above the substrate surface. *Compare* Cheng ¶[0022], ¶[0065], Fig. 4e, *with* Wang ¶¶[0030]-[0032], FIG. 9.



Cheng's Fig. 4e (annotated)

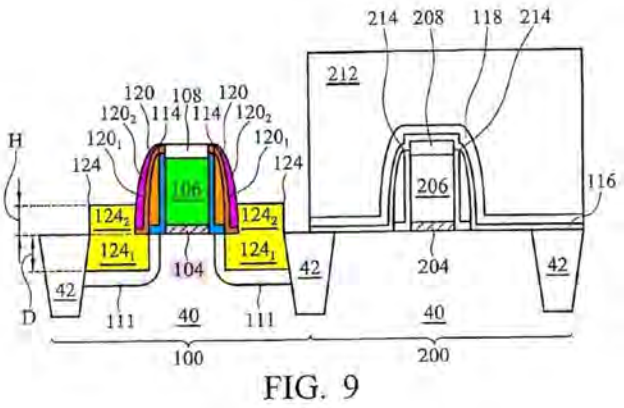


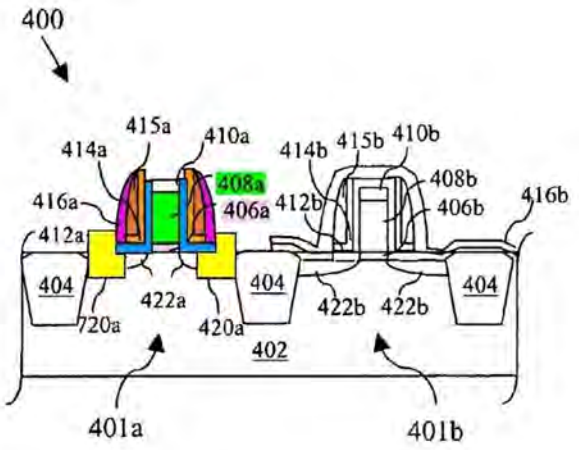
FIG. 9

Wang's FIG. 9 (annotated)

268. A POSITA, reviewing Cheng's descriptions and Figs. 4a-4e, would have understood from the descriptions that Cheng's Fig. 4e contains a rendering error. Comparing Cheng's Figs. 4d and 4e, the epitaxial SiGe regions in Fig. 4e (720a [sic:420a] and 420a, both shown in yellow) are drawn such that they appear to replace part of the non-crystalline sidewall structures 412a (blue). A POSITA, understanding how epitaxial SiGe grows, would have recognized that Cheng's

[23] The layer mislabeled "720a" on the left of Cheng's Fig. 4e should read "420a."

epitaxial SiGe regions in Fig. 4e would instead grow selectively on the crystalline surfaces of the recesses and would then extend up and around the non-crystalline sidewalls 412a and 416a on the outer side of Cheng's pFET. This understanding has been used to correct Cheng's Fig. 4e below (left). Wang's FIG. 9 confirms this, as Wang's textual descriptions track Cheng's textual descriptions. *Compare* Cheng ¶[0065], Fig. 4(e), *with* Wang ¶¶[0030]-[0031], FIG. 9; *see also* Bohr683 ¶¶[0024]-[0028], FIGS. 4-6.



Corrected Cheng's Fig. 4e (annotated)

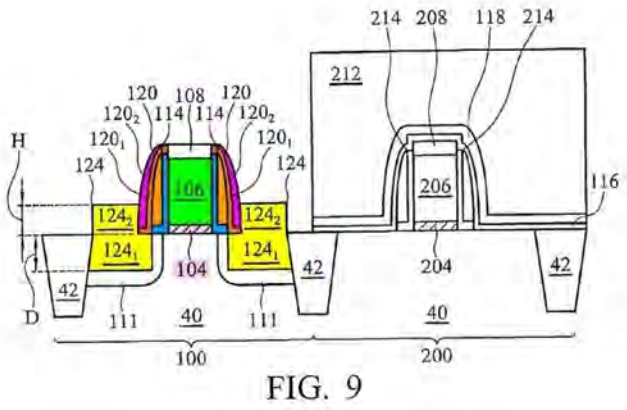


FIG. 9

Wang's FIG. 9 (annotated)

269. Consistent with a POSITA's understanding in Cheng's corrected Fig. 4e above, Cheng discloses that gate dielectric 406a (light purple) "may have a thickness ranging between about 0.5 nm and about 10 nm," and "[t]he height of raised source/drain regions may range" as much as "about 100 nm" above the substrate surface—substantially higher than the thickness of the gate dielectric 406a and spacer 412a (blue). Cheng ¶[0018], ¶[0022]. In other words, Cheng teaches that the SiGe could be as high as 99 nm above the top edge of the horizontal portion of

the "L" shape of sidewall portion 412a as it appears in Cheng's Fig. 4e, such that the epitaxial SiGe (yellow) would grow up and around the dummy spacer 416a (magenta). Cheng ¶[0018], ¶[0022]. Wang, like Cheng, similarly explains that "raised [SiGe] portions 124_2 [(yellow])] preferably have a height H of less than the height of the gate electrode 106 [(green)], and more preferably between about 100 Å and about 700 Å [10-70 nm]." Wang ¶[0031]. Thus, both Cheng and Wang disclose that the epitaxial SiGe (shown in yellow above) is grown above the height of the lower, horizontal portion of the L-shaped sidewall (shown in blue above) such that it grows up and around Cheng's dummy spacer 416a or Wang's comparable sidewall spacer outer portion 120_2 (both shown in magenta above).

270. A POSITA would have recognized that the above correction to Cheng's Fig. 4e would carry through Cheng's Figs. 4f-4j as Cheng's process continues. Those steps do not alter the shape of the epitaxially grown SiGe regions, the sidewalls, or dummy spacer 416a. *See* Cheng ¶¶[0066]-[0070].

271. Figure I below shows the final product of Cheng's Figs. 4a-4j by modifying Cheng's Fig. 4j to show how this correction would carry through to Cheng's final pFET structure. A POSITA would have understood and found obvious—based on Cheng's disclosures alone (which are clear from the textual descriptions) or in combination with Wang's disclosures (which confirm a POSITA's understanding of Cheng's textual descriptions)—that Cheng describes a

pFET consistent with Figure I below (correcting Cheng's Fig. 4j). In other words, Figure I more accurately illustrates the result of Cheng's fabrication process shown in Figs. 4a-4j as described in Cheng's text. *See* Cheng ¶¶[0056]-[0070].

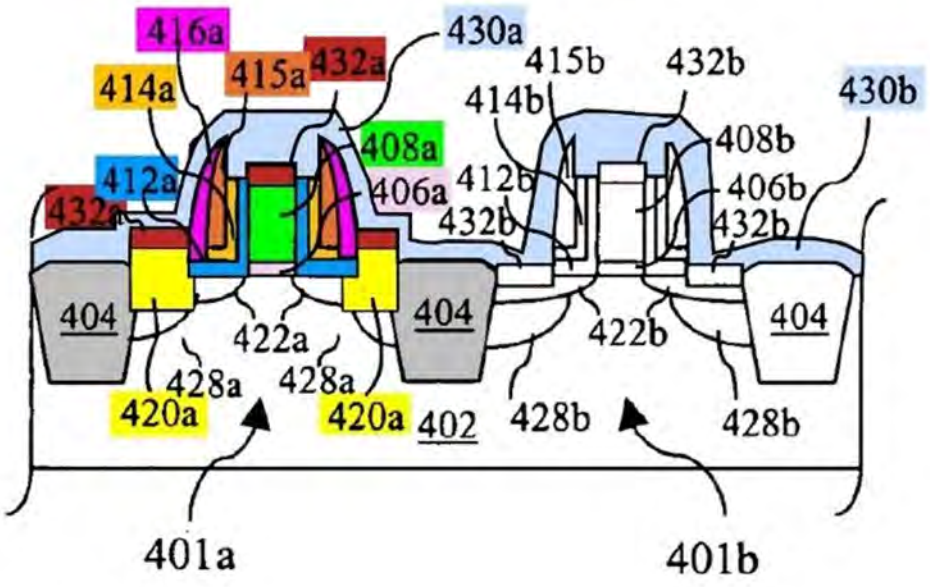


Figure I (annotating and correcting Cheng's Fig. 4j)

272. It is my opinion that a POSITA would have found the structure shown in Figure I obvious based on Cheng's textual disclosures alone, or further in view of Wang's disclosures, because it is an example of applying a known teaching, motivation, or suggestion in the prior art (Cheng's express disclosures relating to Figs. 4a-4j, either alone or in combination with Wang's express disclosures in conjunction with FIGS. 4-9) to arrive at the claimed invention (as reflected in the more accurate Figure I shown above rather than Cheng's Fig. 4j as drawn).

273. To put it simply, a POSITA would have understood that Figure I above more accurately reflects the end result of the process Cheng describes in connection with Figs. 4a-4j for the reasons described above. This is true whether considering Cheng's textual descriptions alone or in conjunction with Wang's disclosures.

274. To summarize, in my opinion, a POSITA would have found the structure of Figure I obvious based on Cheng's textual descriptions alone or in conjunction with Wang's disclosures, because the modification of Cheng's Fig. 4j reflected in Figure I is an example of the following:

- It combines known prior art elements (Cheng's epitaxial SiGe source/drains 420a being deposited to a height well above the surface of the substrate, as Cheng expressly describes and Wang confirms) according to known methods (growing SiGe in a recess of the substrate for enough time that it extends to a height above the top of the substrate) to yield predictable results (conventional raised SiGe layers like the ones used in several generations of high-volume commercial products).
- It uses a known technique (epitaxially growing SiGe in a recess of the substrate to a height above the top of the substrate, as Cheng expressly describes and Wang confirms) to improve similar devices (Cheng's own MOSFETs) in the same way (by applying

compressive stress to the pFET channel region to boost hole mobility).

- It applies a known technique (epitaxially growing SiGe in a recess of the substrate to a height above the top of the substrate, as Cheng expressly describes and Wang confirms) to a known device ready for improvement (Cheng's own MOSFETs) to yield predictable results (conventional raised SiGe layers like the ones used in several generations of high-volume commercial products).
- It applies a known teaching, motivation, or suggestion in the prior art (Cheng's and/or Wang's express disclosures, as discussed above, about growing conventional, raised SiGe layers) that would have led a POSITA to modify Cheng according to, or to combine Cheng with, its own textual descriptions and/or the teachings of Wang to arrive at the claimed invention.

1. Ground 2A: Cheng Renders Claims 1, 3-9, 11, and 12 Obvious

a. Independent Claim 1

275. In my opinion, Cheng alone renders claim 1 obvious based on the simple correction to Figs. 4e-4j that I explain above. *See* Section IX.C (introduction) above.

(1) [1Pre]: "A semiconductor device"

276. Cheng discloses a semiconductor device. *See* Cheng ¶¶[0056]-[0071], Fig. 4j. For example, Cheng discloses an "embodiment of a method for making semiconductor devices 401a and 401b with high drive current." Cheng ¶[0056], FIGS. 4a-4j. As Cheng explains, "[t]he semiconductor device 401a may be a P-type MOS device and the semiconductor device 401b may be an N-type MOS device." Cheng ¶[0056], Figs. 4a-4j.

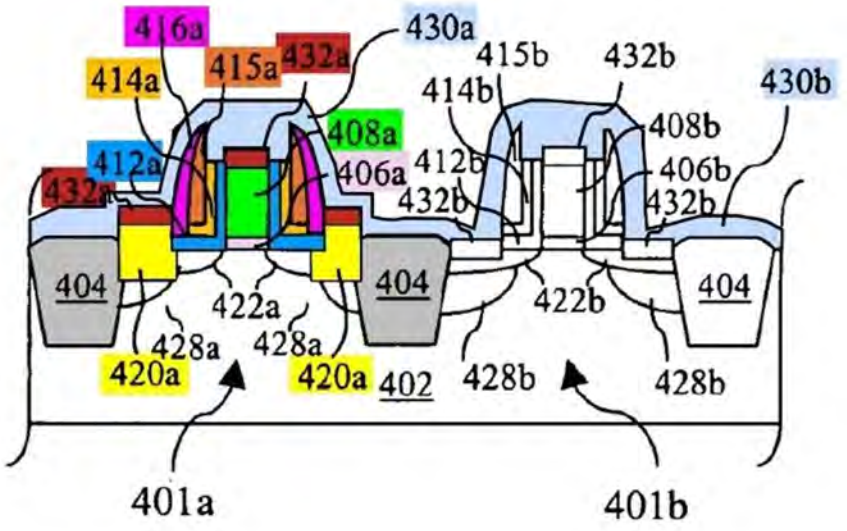


Figure I

(2) [1A]: "a first MIS transistor . . . includ[ing]"

277. Cheng discloses a first MIS transistor. *See* Cheng ¶¶[0056]-[0071], Fig. 4j. For example, Cheng discloses that "semiconductor device 401a may be a P-type MOS device," i.e., a pFET. Cheng ¶[0056], Figs. 4a-4j.[24] Figure I above

[24] Alternatively, as I discuss below in claim 9, the first MIS transistor "may be an N-type MOS device," i.e., an nFET. *See* Cheng ¶[0056]; Section IX.C.1.h below.

shows and annotates "P-type MOS device" 401a (first MISFET transistor) of Cheng's semiconductor device. *See* Section IX.C (introduction) above.

(3) [1B]: "a first gate insulating film formed on a first active region in a semiconductor substrate"

278. Cheng discloses "a first gate insulating film formed on a first active region in a semiconductor substrate." For example, Cheng discloses that "gate dielectric 406a [PMOS] and 406b [NMOS] are formed over a substrate 402 for devices [PMOS] 401a and [NMOS] 401b, respectively." Cheng ¶[0056], Figs. 4a-4j. Cheng's gate dielectric layer 406a corresponds to a first gate insulating film because it is made of materials such as "silicon oxide" or "SiO_2" (i.e., silicon dioxide). Cheng ¶[0058]; *see also* Cheng ¶[0020]. This is the same as the '425 Patent's disclosure that the "gate insulating film" is made of "silicon oxide." '425 Patent, 9:15-19.

279. Cheng's substrate 402, on which gate dielectric 406a is formed, contains an active region, which refers to the portion of the substrate where a MIS transistor (e.g., PMOS device 401a) is located. It includes, for example, "lightly doped regions 422a" having "P-type . . . dopants," "doped source and drain regions 420a," and "heavily doped . . . regions 428a." Cheng ¶[0056], ¶[0060], ¶¶[0065]-[0068], Fig. 4j.

280. In Figure I below, pFET 401a is the first MISFET transistor. *See* Section IX.C (introduction) above. Cheng's gate insulating film 406a (light purple) of pFET 401a is formed on a portion of the substrate between the two lightly doped

regions 422a. This portion of the substrate is the channel region, which, by definition, is part of the "active region" of pFET 401a.

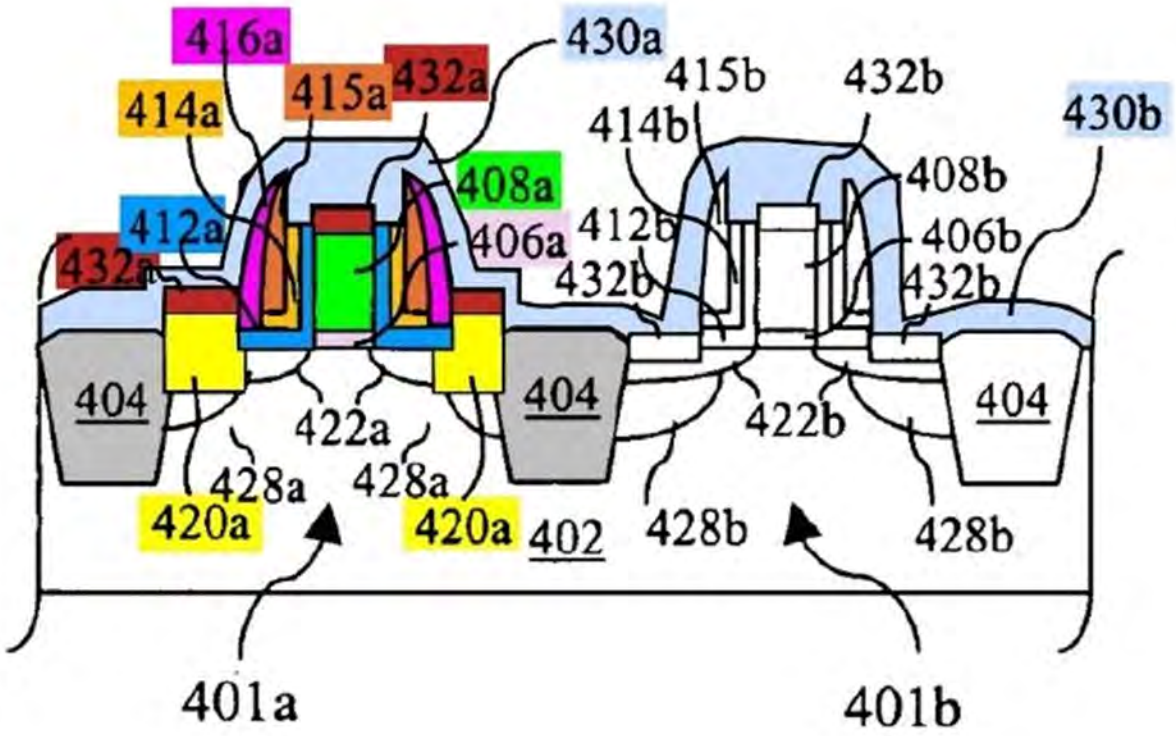


Figure I

(4) [1C]: "a first gate electrode formed on the first gate insulating film"

281. Cheng discloses "a first gate electrode formed on the first gate insulating film." For example, Cheng discloses that "[g]ate electrodes 408a and 408b are formed over the gate dielectric layer [406a, 406b]." Cheng ¶[0056]. Figure I above shows that gate electrode 408a (green) is formed on the first gate dielectric 406a (light purple) of Cheng's pFET 401a. *See* Section IX.C (introduction) above.

(5) [1D]: "a first sidewall spacer formed on a side surface of the first gate electrode"

282. Cheng discloses "a first sidewall spacer formed on a side surface of the first gate electrode." For example, Cheng discloses a first sidewall spacer that includes "sidewall dielectric layer[] . . . 414[] and spacer material 415 . . . disposed over the semiconductor device(s) 410a [sic:401a] and 401b." Cheng ¶[0061]. Cheng explains that, during "subsequent process[ing], such as by etching," the dielectric layer 414 and spacer material 415 layer are etched and formed into "sidewall dielectric structures" 414a and "spacers" 415a, as Cheng's Fig. 4c shows. Cheng ¶[0061], Figs. 4b-4c. As Cheng's Fig. 4c shows, dielectric structure 414a and spacer 415a (together, the claimed sidewall spacer) are formed on a side surface of gate electrode 408a because, like the '425 Patent, they are formed laterally on the sides of gate electrode 408a. *Compare* Cheng ¶[0061], Fig. 4c, *with* '425 Patent, FIG. 6B (transistor pTr1, sidewall 19A).

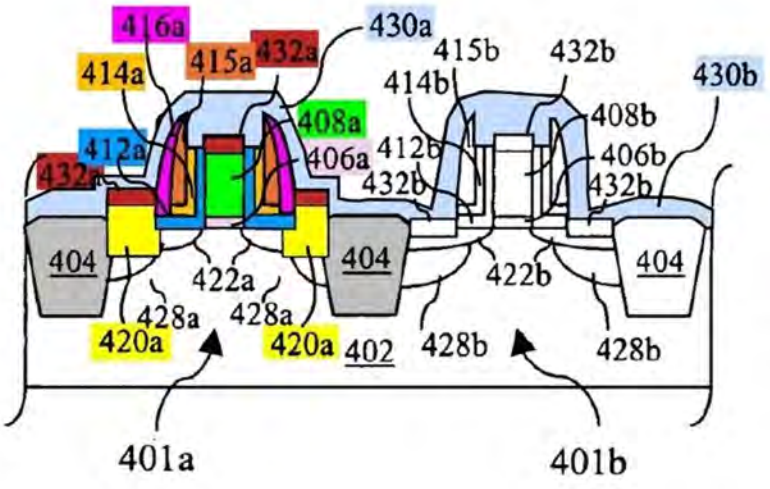


Figure I

283. As I explain above in Section IX.C (introduction), a POSITA would have recognized and found obvious (from considering Cheng's textual descriptions alone or in view of Wang's disclosures) that these structures would be carried through Cheng's processing as Figure I shows above. As Figure I shows, the first sidewall spacer (sidewall dielectric structure 414a (light orange) and spacer 415a (dark orange), collectively) is formed on the sides of gate electrode 408a (green) in Cheng's pFET 401a.

(6) [1E]: "a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region"

284. Cheng discloses "a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region."

285. As I explain above in Section IX.C (introduction), Cheng discloses recessed regions 418a in substrate 402. Recessed regions 418a are trenches "formed by a process such as chemical etch, focused ion beam (FIB), and/or plasma etch." Cheng ¶[0064], Fig. 4d. Cheng further discloses that "doped source and drain regions 420a are formed or built-up in the recessed regions 418a." Cheng ¶[0065],

Fig. 4e. They "may be formed by selective epitaxial growth (SEG)" of "silicon germanium." Cheng ¶[0065], Fig. 4e; *see* Section IX.C above. Cheng's SiGe source/drain regions 420a comprise a first, p-type conductivity type and comprise part of the pFET source/drain regions. Cheng ¶[0065]; *see also* Miyashita ¶¶[0050]-[0051]; Chen729 ¶[0021]; Bohr683 ¶[0028], FIGS. 4-7.

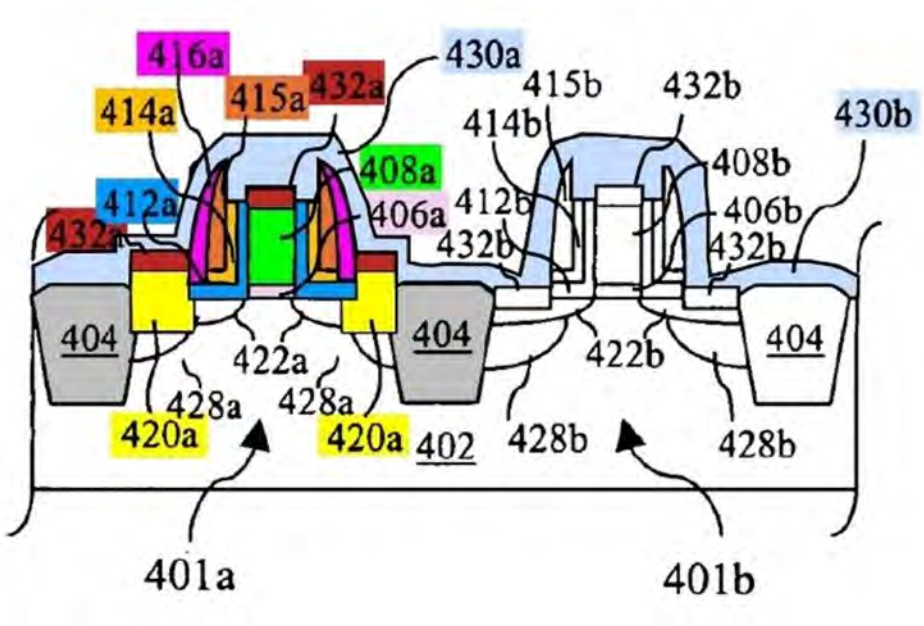


Figure I

286. Cheng's SiGe source/drain region 420a constitutes a strained silicon layer, the purpose of which was to impart compressive stress along gate length direction of the silicon channel region of pFET 401a. Cheng ¶[0065]; *see also* Section VI.B above (strained SiGe background); Wang ¶¶[0030]-[0032], FIG. 9; Thompson2004, 1790-96; Sun, 2; Bohr683 ¶[0024], ¶[0026], ¶[0028], FIGS. 4, 6, 7; Miyashita ¶[0051]; Fukutome ¶[0110], FIGS. 5E-5G. As I explain above in Section IX.C (introduction), and as Figure I shows above, a POSITA would have recognized

and found obvious (from considering Cheng's textual descriptions alone or in view of Wang's disclosures) that Cheng's SiGe source/drain regions 420a (yellow)—which are part of the pFET active region—are located on a lateral side of the first sidewall spacers (layers 414a (light orange) and 415a (dark orange)).

(7) [1F]: "a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress"

287. Cheng discloses "a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress."

288. Cheng discloses a stress insulating film, such as tensile etch stop layer 430a/430b, "formed over the semiconductor device(s) 401a and 401b." Cheng ¶[0070], Fig. 4j. As Fig. 4j shows, etch stop layer 430a/430b is formed over Cheng's pFET 401a to cover the gate electrode 408a, sidewall spacer layers 414a and 415a, and raised SiGe source/drain regions 420a. Cheng ¶[0070], Fig. 4j. Cheng explains that the etch stop layer 430a/430b may be a tensile silicon nitride film (stress opposite the compressive stress caused by epitaxial SiGe layers 420a) and that the "stress level . . . may range between about +0.001 and about +50 GPa for [a] tensile film." Cheng ¶[0070].

289. As Figure I below shows, tensile etch stop film 430a/430b (light blue) is formed over the gate electrode 408a (green), first sidewall spacer layers 414a (light orange) and 415a (dark orange), and source/drain regions 420a (yellow) of Cheng's pFET 401a. *See* Section IX.C (introduction) above.

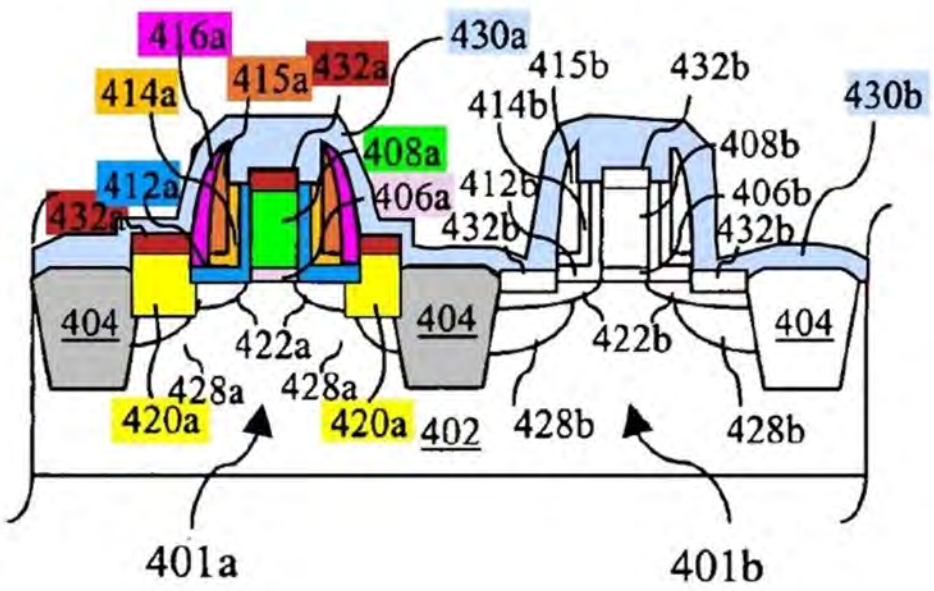


Figure I

290. Although Cheng expressly discloses that etch stop layer 430a/430b may be a tensile layer, a POSITA also would have selected and readily envisioned Cheng's etch stop layer 430a/430b as a tensile etch stop layer covering both pFET 401a and nFET 401b, as Figure I shows above. *See* Cheng, Fig. 4j. It was well known in the art that a tensile CESL improves electron mobility in nFETs without negating the compressive stress in pFETs caused by epitaxial SiGe source/drain layers. *See* Sections VI.B and VI.C above; Hsu823 ¶[0039] (preferable to apply tensile CESL across both NMOS and PMOS devices because "the performance of PMOS devices

can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 355-56; Bohr683 ¶¶[0038]-[0039], FIG. 6.

(8) [1G]: "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode"

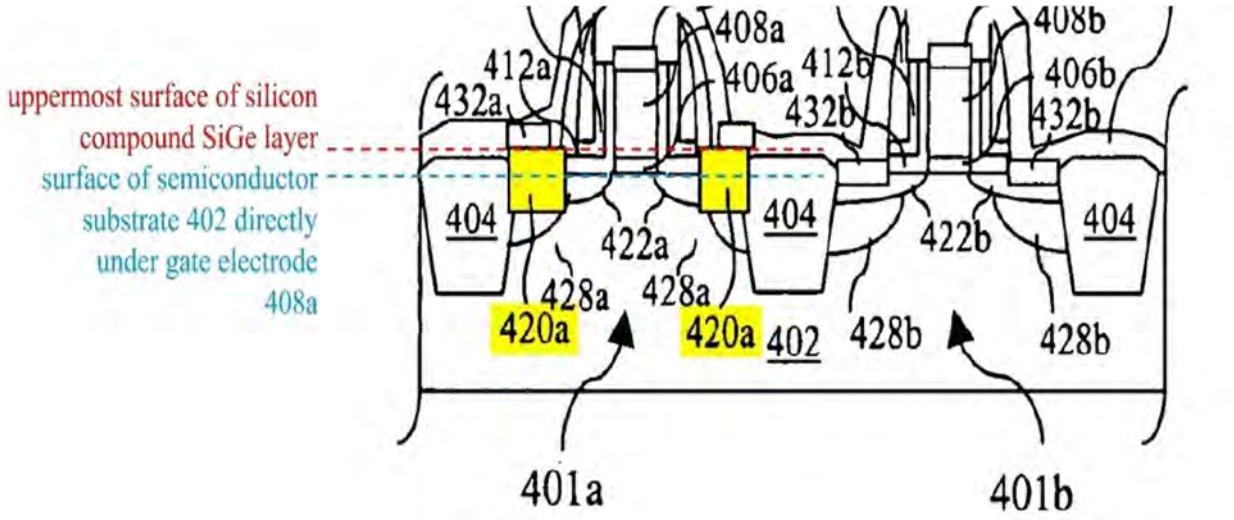
291. Cheng discloses or renders obvious "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode."

292. Cheng discloses that "the source/drain regions 136 may extend above the substrate surface 106." Cheng ¶[0022], ¶[0065]. For example, the "recesses 144" in the substrate "may be filled to a height above the surface 106 of the substrate 104, such that the source/drain regions 136 may be raised source/drain regions." Cheng ¶[0022], ¶[0065]. Cheng explains that "[t]he height of raised source/drain regions may range between about 5 nm and about 100 nm." Cheng ¶[0022].

293. Cheng's Figs. 4e-4j similarly show source/drain regions 420a "built-up" above the height of the surface of the substrate 402. Cheng ¶[0065], Figs. 4e-4j. A POSITA would have understood from reading Cheng that SiGe source/drain regions 420a of P-type MOS device 401a being "built-up" above the surface of the substrate describes the source/drains 420a being raised above the surface of the substrate 402. *See* Cheng ¶[0054] (explaining that "a P-type MOS

device[] comprises raised source and drain regions"), ¶[0065], Abstract, claims 1, 5, 7, 8, 22-28, Figs. 4e-4j.

294. I have annotated Cheng's Fig. 4j below to show the height of Cheng's raised SiGe source/drain region 420 (red line) and the height of the surface of the substrate 402 under the gate electrode (blue line). As Fig. 4j indicates, the uppermost surface of the raised SiGe source/drain region 420 is higher than the uppermost surface of substrate 402 under the gate electrode (i.e., "built-up" over it).



Cheng's Fig. 4j (excerpted, annotated)

295. As I explain above in Section IX.C (introduction), a POSITA would have understood that Figure I below more accurately reflects the pFET shown in Cheng's Fig. 4j, but this aspect of Cheng's pFET, which the text expressly describes, would have been understood to carry through Cheng's process as shown.

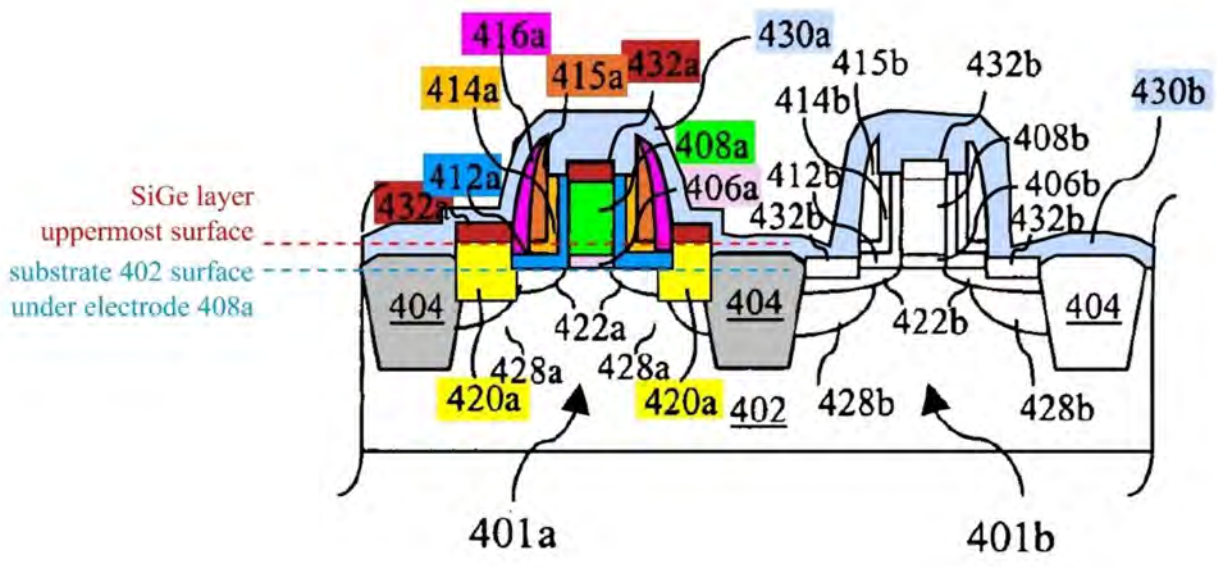


Figure I (further annotated)

(9) [1H]: "a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer"

296. Cheng discloses that "a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer."

297. Cheng discloses "dummy spacers 416a," which may be made of "silicon dioxide (SiO_2)," located between raised SiGe source/drain regions 420a and sidewall spacers 414a/415a. Cheng ¶[0063]. As I explain above in Section IX.C (introduction), a POSITA reading Cheng would have understood or found it obvious that Cheng's SiGe source/drain regions 420a extend to a height above gate dielectric 406a (light purple), such that SiGe source/drain regions 420a (yellow) grow around dummy spacer 416a (magenta). Figure I below illustrates Cheng's textual descriptions, including this aspect. *See* Section IX.C (introduction) above.

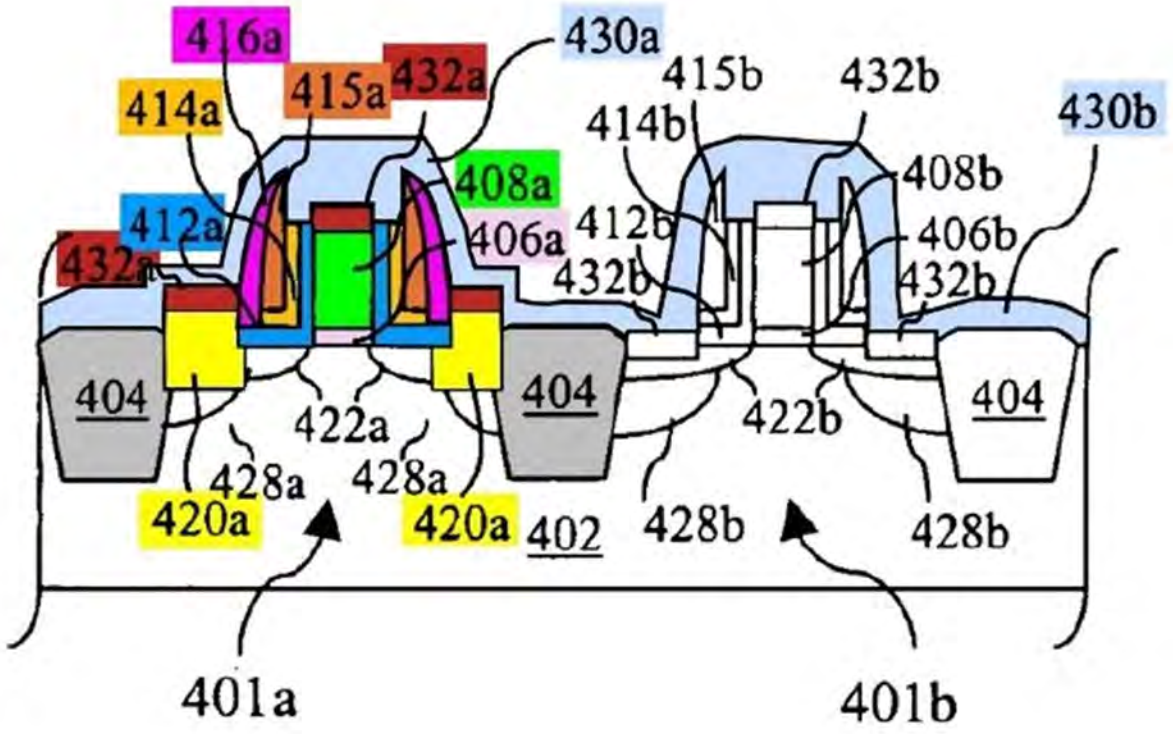


Figure I

298. Cheng's disclosures in this regard are similar to the '425 Patent's description of the stress-relief film. The '425 Patent describes an embodiment in which "[a] first stress-relief film 28a is formed in the space 24 between the silicon compound layer 23 and the first sidewall 19A." '425 Patent, 14:51-54. The stress-relief film 28a is made of silicon oxide, like Cheng's dummy spacer 416a. *See* '425 Patent, 12:59-62; Cheng ¶[0063].

299. As Figure I above illustrates, Cheng's dummy spacer 416a (first stress-relief film, magenta) is formed in a space between SiGe silicon compound layer 420a (yellow) and the first sidewall spacer (comprising light and dark orange layers 414a and 415a) of pFET 401a. *See* Section IX.C (introduction) above.

(10) [1I]: "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween"

300. Cheng discloses that "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween."

301. As I discuss above for element [1H], Cheng's Fig. 4j shows that dummy spacers 416a are formed on the side surfaces of gate electrode 408a with the first sidewall spacer (sidewall layers 414a and 415a, collectively) located between them. As I explain in Section IX.C (introduction), a POSITA would have understood from Cheng's disclosures, either alone or in view of Wang's similar disclosures, that Figure I represents a more accurate description of Cheng's pFET than Cheng's Fig. 4j. As Figure I shows below, Cheng's stress-relief film (dummy spacer 416a, magenta) is formed on the side surface of gate electrode 408a (green) with the first sidewall spacer (light and dark orange layers 414a and 415a) lying between them. *See* Section IX.C (introduction) above.

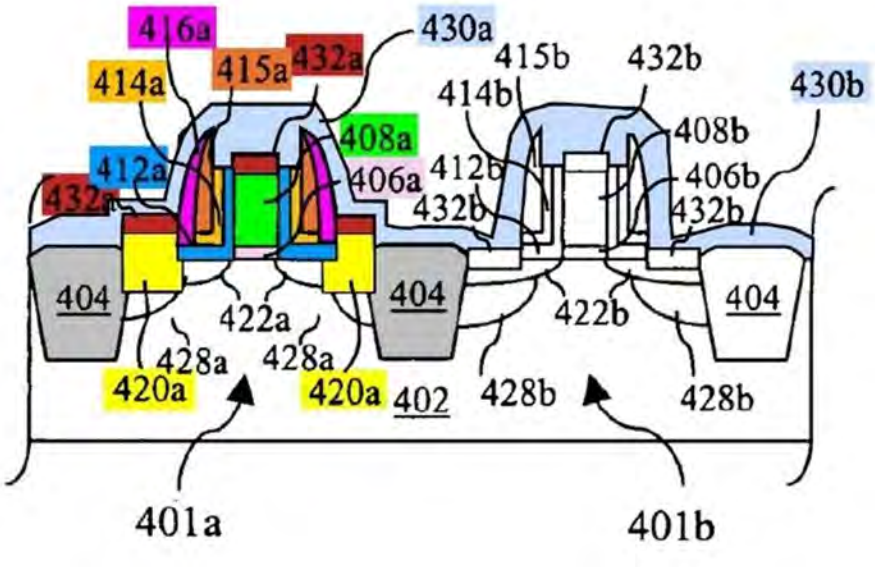


Figure I

(11) [1J]: "the first stress-relief film is not in direct contact with the side surface of the first gate electrode"

302. Cheng discloses that "the first stress-relief film is not in direct contact with the side surface of the first gate electrode."

303. As I discuss above for [1H] and [1I], Cheng's Fig. 4j shows that dummy spacers 416a do not directly contact the side surface of gate electrode 408a because the first sidewall spacer (sidewall dielectric structure 414a and spacer 415a, collectively) lies between them. As I explain above in Section IX.C (introduction), a POSITA would have understood from Cheng's disclosures, either alone or in view of Wang's similar disclosures, that Figure I below represents a more accurate description of Cheng's pFET than Cheng's Fig. 4j. As Figure I shows below, Cheng's stress-relief film (dummy spacer 416a, magenta) does not directly contact the side of gate electrode 408a (green) because the first sidewall spacer (light and

dark orange layers 414a and 415a) lies between them. *See* Section IX.C (introduction) above.

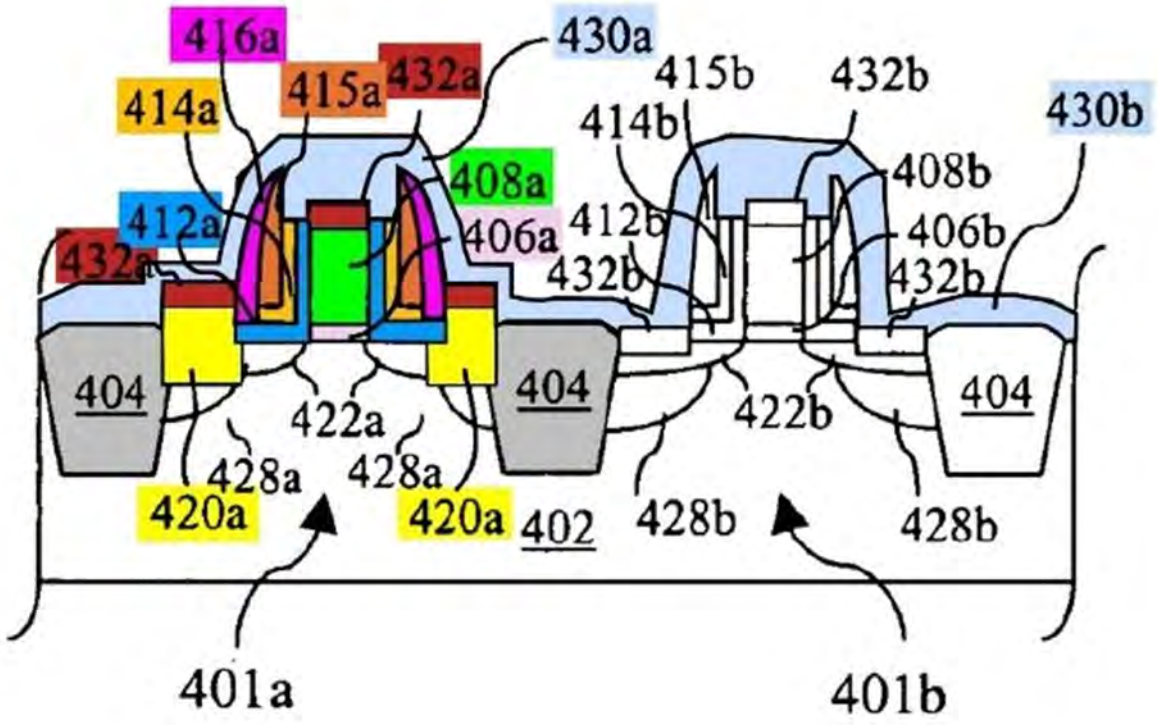


Figure I

b. Claim 3: "The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer"

304. In my opinion, Cheng renders claim 3 obvious.

305. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

306. Cheng also renders obvious a first silicide layer formed on the first gate electrode and a second silicide layer formed on the first source/drain region, which includes the silicon compound layer.

307. Cheng explains that "salicided[25] contacts 432a . . . are formed over the gate [408a]" and over "source and drain [420a]." Cheng ¶[0069]; *see also* Cheng, Figs. 4i, 4j. Cheng explains that "salicided contacts 432a and 432b may include the formation of a metal silicide such as . . . nickel silicide" or others. Cheng ¶[0069], Figs. 4i, 4j. As I explain above for claim 1, Cheng's pFET gate 408a corresponds to the first gate electrode, and the claimed source and drain region includes epitaxial SiGe layer 420a. *See* Sections IX.C.1.a(4) and IX.C.1.a(6) above.

308. As I describe above in Section IX.C (introduction), a POSITA would have understood from Cheng's disclosures, either alone or in view of Wang's similar disclosures, that Figure I represents a more accurate description of Cheng's pFET than Cheng's Fig. 4j. As Figure I shows, a first silicide layer 432a (red) is formed on the first gate electrode 408a (green), and a second silicide layer 432a (red) is formed on the epitaxial SiGe source/drain regions 420a (yellow). *See* Section IX.C (introduction) above; Cheng, Fig. 4j.

[25] The term "salicide" refers to a **s**elf-**a**ligned si**licide**. It is a silicide layer.

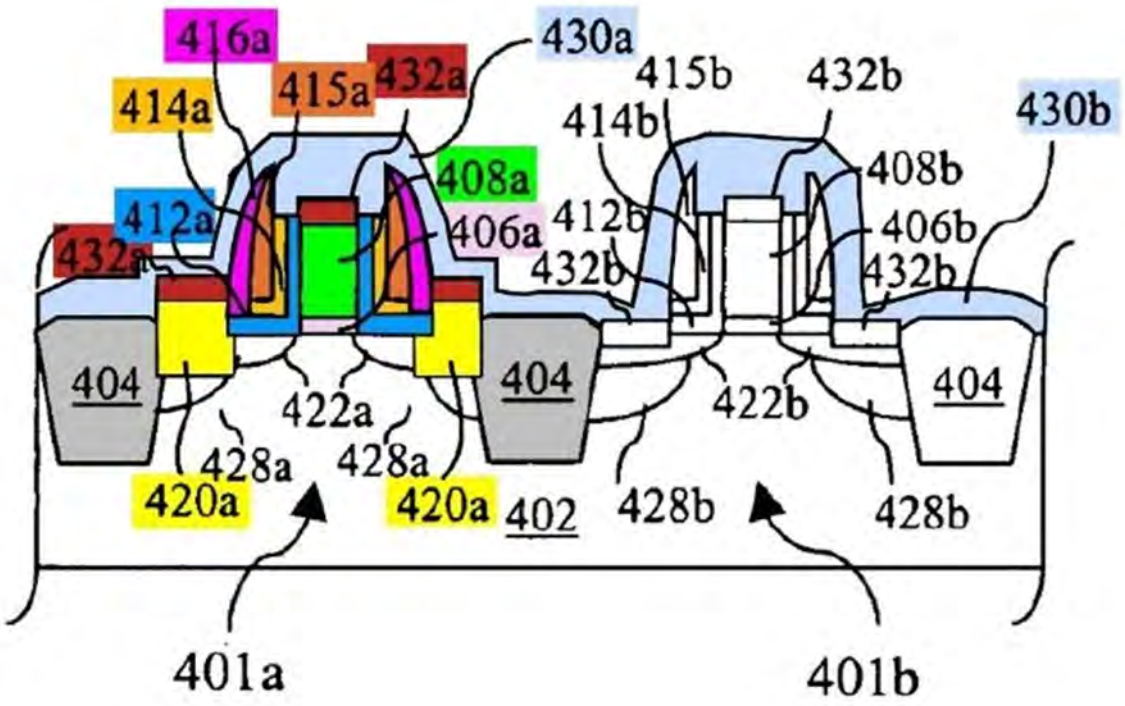


Figure I

c. Claim 4: "The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer"

309. In my opinion, Cheng renders claim 4 obvious.

310. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

311. Cheng also discloses that the first stress-relief film is formed on a side surface of the silicon compound layer.

312. As I discuss above for [1H]-[1J] and in Section IX.C (introduction), Cheng's dummy spacer 416a (stress-relief film) is formed on a side surface of the epitaxial SiGe source/drain regions 420a (silicon compound layer). Cheng, Fig. 4j;

see also Sections IX.C and IX.C.1.a(9)-IX.C.1.a(11) above. A POSITA would have understood that Cheng's SiGe layer would grow up and around Cheng's sidewall structures and dummy spacer 416a, as Figure I shows below. *See* Section IX.C (introduction) above; Cheng ¶[0022], ¶[0065], Fig. 4e; Wang ¶¶[0030]-[0032], FIG. 9.

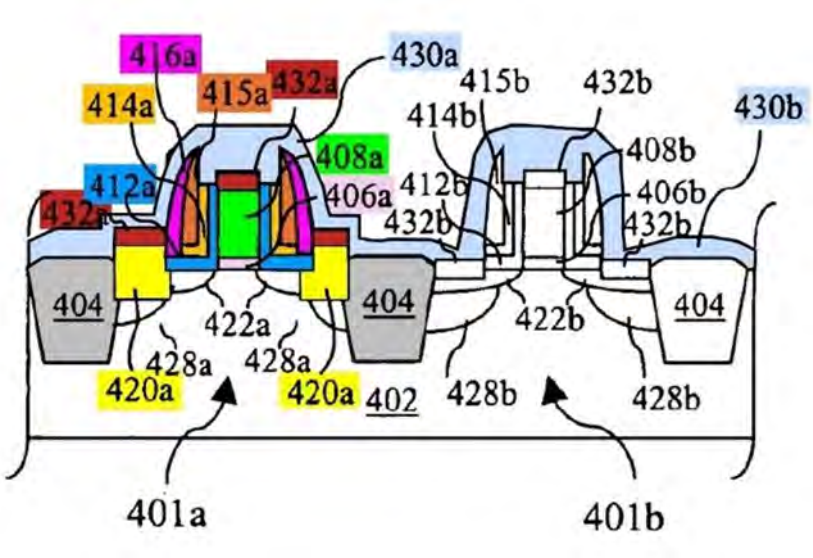


Figure I

313. As I describe above in Section IX.C (introduction), a POSITA would have understood from Cheng's disclosures, either alone or in view of Wang, that Figure I represents a more accurate description of Cheng's pFET than Cheng's Fig. 4j. As Figure I shows, Cheng's stress-relief film (dummy spacer 416a, shown above in magenta) is formed on a side surface of Cheng's silicon compound layer (epitaxial SiGe source/drain layer 420a, shown above in yellow) as the SiGe layer (yellow) is "built-up" adjacent to the dummy spacers 416a (magenta). *See* Section IX.C (introduction) above.

d. Claim 5: "The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer"

314. In my opinion, Cheng renders claim 5 obvious.

315. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

316. Cheng also discloses that "the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer."

317. As I explain above for [1D], Cheng's first sidewall spacer comprises both sidewall dielectric structures 414a and spacers 415a. *See* Cheng ¶[0061], Figs. 4c, 4j; Section IX.C.1.a(5) above. Layers 414a and 415a are both formed on the side surface of gate electrode 408a, and Cheng explains that "dielectric structures 714a [sic:414a] . . . are substantially L-shaped." Cheng ¶[0061]; *see also* Cheng, Fig. 4c. Cheng further discloses in Fig. 4c, for example, that outer sidewall spacer 415a is formed in the bend of the "L"-shaped cross-section of inner sidewall dielectric structure 414a. *See* Cheng ¶[0061], Figs. 4c, 4j.

318. As I describe above in Section IX.C (introduction), a POSITA would have understood from Cheng's disclosures, either alone or in view of Wang, that

Figure I represents a more accurate description of Cheng's pFET than Cheng's Fig. 4j. As Figure I shows, the first sidewall spacer includes an inner sidewall spacer (sidewall spacer layer 414a (light orange)) formed on the side surface of first gate electrode 408a (green) and having an L-shaped cross-section. Figure I further shows that the first sidewall spacer includes an outer sidewall spacer (sidewall spacer layer 415a (dark orange)) that is formed in the "L"-shaped cross-section of the inner sidewall spacer (layer 414a (light orange)). *See* Section IX.C (introduction) above.

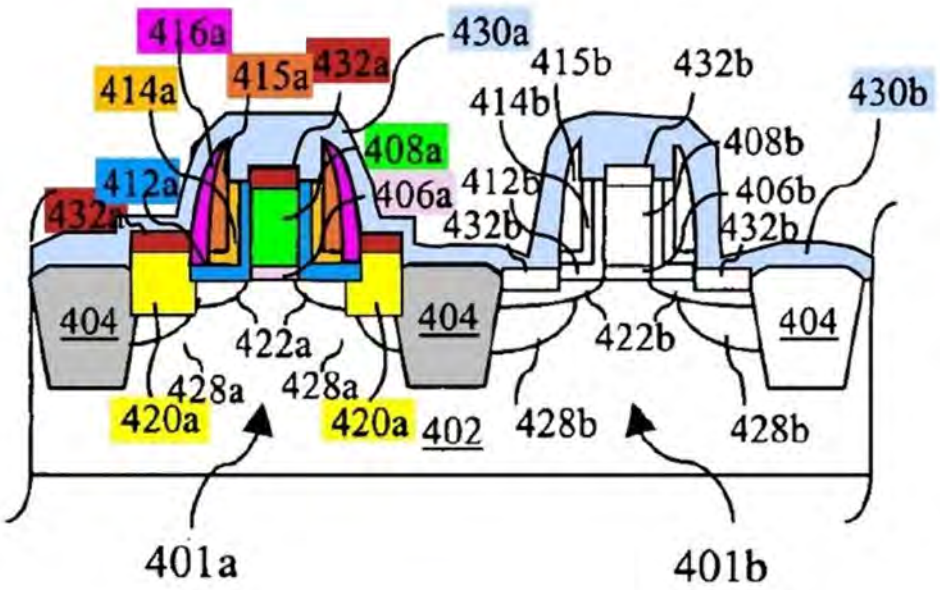


Figure I

e. Claim 6:

319. In my opinion, Cheng renders claim 6 obvious.

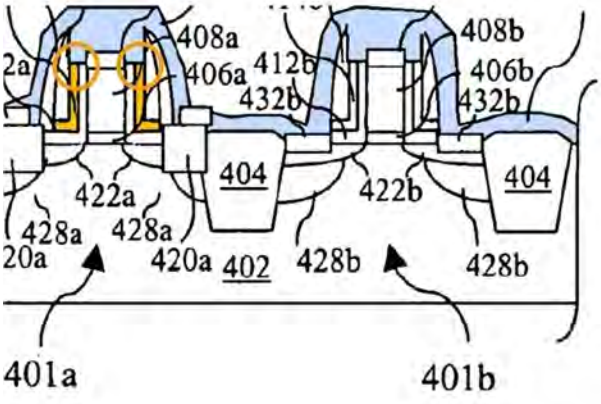
(1) [6Pre]: "The semiconductor device of claim 1"

320. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

(2) [6A]: "the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape"

321. Cheng discloses that "the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape."

322. As I explain above in claim 5, Cheng discloses that sidewall dielectric structures 414a (inner sidewall spacers) are formed on the side surface of gate electrode 408a and "are substantially L-shaped." Cheng ¶[0061]; *see also* Cheng, Fig. 4c; Section IX.C.1.d above. As I show in annotated Fig. 4j of Cheng and Figure I (*see* Section IX.C (introduction) above), Cheng's sidewall dielectric structures 414a (light orange) are L-shaped.



Cheng's Fig. 4j (annotated)

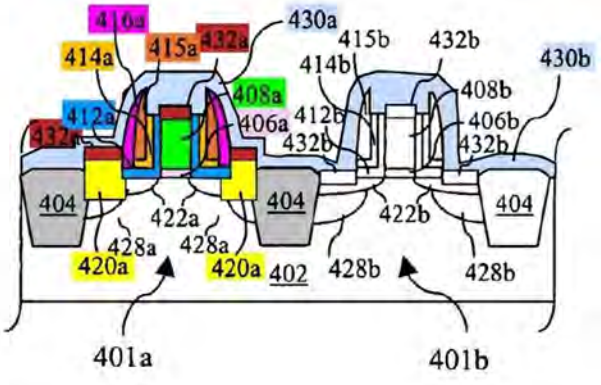
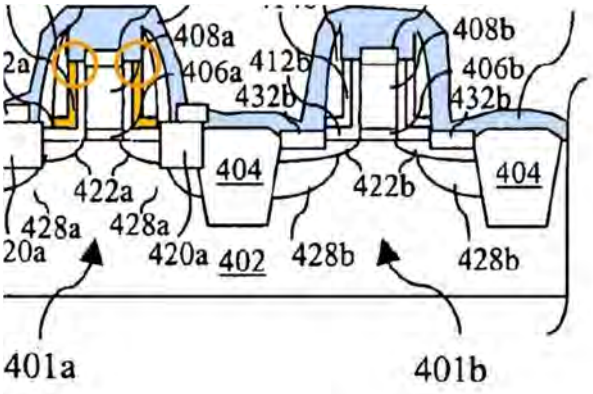


Figure I

(3) [6B]: "the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section"

323. Cheng discloses that "the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section."

324. As I discuss above for [1F], Cheng discloses that the etch stop layer 430a/430b is "formed over the semiconductor device(s) 401a and 401b." Cheng ¶[0070]; *see also* Section IX.C.1.i(7) above. Cheng shows in Fig. 4j that the top of the L-shaped dielectric structure 414a is exposed before etch stop layer 430a/430b is formed, and that etch stop layer 430a is formed in contact with the exposed top surface of the "L"-shaped cross-section of dielectric structure 414a. Below, annotated Fig. 4j and Figure I (*see* Section IX.C (introduction) above) show this.



Cheng's Fig. 4j (annotated)

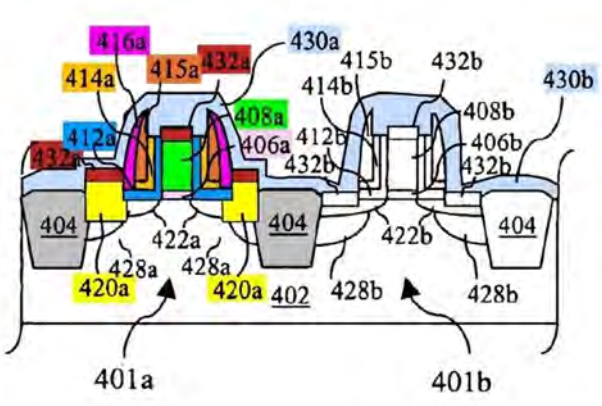


Figure I

f. Claim 7:

325. In my opinion, Cheng renders claim 7 obvious.

(1) [7Pre]: "The semiconductor device of claim 1"

326. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

(2) [7A]: "the first MIS transistor is a p-type MIS transistor"

327. Cheng discloses that "the first MIS transistor is a p-type MIS transistor." As I explain in claim 1 above, Cheng discloses that "semiconductor device 401a may be a P-type MOS device," i.e., a p-type MIS transistor. Cheng ¶[0056]; *see also* Section IX.C.1.a above.

(3) [7B]: "the first stress is a compressive stress"

328. Cheng discloses that "the first stress is a compressive stress." As I explain for claim 1 above, Cheng's raised SiGe source/drain regions 420a impart a first stress that is compressive because "increasing the compressive stress in the substrate can improve the performance of p-channel metal-oxide-semiconductor (PMOS) devices." Cheng ¶[0002]; *see also* Sections VI.B, IX.C (introduction), and IX.C.1.a above.

(4) [7C]: "the second stress is a tensile stress"

329. Cheng discloses that "the second stress is a tensile stress." As I explain for claim 1 above, Cheng's etch stop layer 430a/430b imparts a second stress that is tensile. Cheng ¶[0070]; *see* Sections VI.B, IX.C (introduction), and IX.C.1.a above.

g. Claim 8:

330. In my opinion, Cheng renders claim 8 obvious.

(1) [8Pre]: "The semiconductor device of claim 1"

331. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

(2) [8A]: "the silicon compound layer is a SiGe layer"

332. Cheng discloses that "the silicon compound layer is a SiGe layer." As I explain for claim 1 above, Cheng's silicon compound layer includes epitaxial source/drain layer 420a, which comprises "silicon germanium." Cheng ¶[0065]; *see also* Sections VI.B, IX.C (introduction), and IX.C.1.a above.

(3) [8B]: "the stress insulating film is a silicon nitride film"

333. Cheng discloses that "the stress insulating film is a silicon nitride film." As I explain for claim 1 above, Cheng's "etch stop layer 430a and 430b may include silicon nitride (Si_xN_y)." Cheng ¶[0070]; *see also* Sections VI.B, IX.C (introduction), and IX.C.1.a above.

(4) [8C]: "the first stress-relief film is a silicon oxide film"

334. Cheng discloses that "the first stress-relief film is a silicon oxide film." As I explain for claim 1 above, Cheng's "dummy spacer material 416 [stress-relief film] may include silicon dioxide (SiO_2)." Cheng ¶[0063]; *see also* Sections VI.C, IX.C (introduction), and IX.C.1.a above.

h. Claim 9:

335. In my opinion, Cheng renders claim 9 obvious.

(1) [9Pre]: "The semiconductor device of claim 1"

336. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above. Similar to my discussion of Wu and Alvarez in Section IX.B.1.h (Ground 1A, claim 9), Cheng discloses the structure recited in claim 1 but also explains that the roles of the stresses and conductivity types may be reversed. For example, the pFET and nFET may be switched, with the epitaxial SiGe source/drain layer being replaced by an epitaxial SiC layer, and the tensile CESL may be swapped for a compressive CESL. These substitutions, like in Section IX.B.1.h (Ground 1A, claim 9), would have been obvious to a POSITA because the SiC causes a tensile strain in the nFET channel region to improve electron mobility, and a compressive CESL would benefit the pFETs to improve hole mobility. *See* Section VI.B above.

(2) [9A]: "the first MIS transistor is an n-type MIS transistor"

337. Cheng discloses several alternative embodiments. The pFETs and nFETs may include no epitaxial layers, the pFETs and nFETs may both include epitaxial source/drain layers (SiGe for the former and SiC for the latter), or either the pFET or the nFET may include epitaxial source/drain layers (SiGe for the former

or SiC for the latter). Cheng ¶[0036]. For purposes of claim 9, I consider the situation in which either the pFET or the pFET includes epitaxial source/drain layers.

338. Cheng explains that "[a] first one of the NMOS and PMOS devices includes one of: (1) first source/drain regions located at least partially within the substrate and comprising SiC; and (2) first source/drain regions located at least partially within the substrate and comprising SiGe." Cheng ¶[0036]. In other words, the first device is either an nFET or a pFET, and it comprises either epitaxial SiC or SiGe, respectively. The embodiment described in the context of Cheng's Figs. 4a-4j shows the latter option. But, for essentially the same reasons I explain in Section IX.B.1.h (Ground 1A, claim 9), a POSITA would have found the former option obvious as well. That is, a POSITA would have found it obvious to switch the roles of Cheng's FETs 401a and 401b by swapping their conductivity types, changing epitaxial SiGe layer 420 to be an epitaxial SiC layer, and changing etch stop layer 430a/430b from tensile to compressive. *See* Cheng ¶[0036]; Sections VI.B and IX.B.1.h (Ground 1A, claim 9) above.

339. Thus, for claim 9, a POSITA would have found it obvious for the "first MIS transistor" to be an nFET with epitaxial SiC source/drain regions analogous to the SiGe source/drain regions described in the context of Cheng's Fig. 4a-4j. *See* Cheng ¶[0033], ¶[0036]; *see also* Section VI.B above. A POSITA would have recognized that "first source/drain regions located at least partially within the

substrate and comprising SiC" refers to raised epitaxial SiC source/drain regions 420a in the context of Cheng's Figs. 4a-4j. Cheng ¶[0036]; *see also* Cheng ¶[0033] ("A first one of the NMOS and PMOS devices includes one of: . . . (2) first source/drain regions extending from the surface.").

340. Cheng also discloses that "the first semiconductor device" may include "a dummy spacer on either side of the gate structure," irrespective of whether the device is a pFET or nFET. Cheng, claim 5.

341. Thus, a POSITA would have understood that when the first MIS transistor is an nFET, it has the same structure as FET 401a shown in Figure I (*see* Section IX.C (introduction) above), except that it is n-type instead of p-type and the raised source/drain layer 420a comprises SiC instead of SiGe. *See* Cheng ¶[0033], ¶[0036].

(3) [9B]: "the first stress is a tensile stress"

342. As Cheng explains, "source/drain regions [are] located at least partially within the substrate and compris[e] SiC," where "at least partially within" describes SiC source/drain regions extending above the substrate. Cheng ¶[0036]; *see also* Cheng ¶[0025], ¶[0033]. As I explain above, a POSITA would have recognized that raised epitaxial SiC source/drain regions 420a of an nFET cause a tensile stress along the gate length direction because the SiC has a smaller lattice constant than silicon. *See* Sections VI.B and IX.B.1.h above.

(4) [9C]: "the second stress is a compressive stress"

343. Cheng teaches that "etch stop layer 430a and 430b may include a stress level that may range . . . between about -0.001 and about -50 GPa for compressive film." Cheng ¶[0070]. As I explain above, a POSITA would have found it obvious for Cheng's etch stop layer 430a/430b to impart compressive stress when the nFET comprises epitaxial SiC source/drain regions. The SiC acts as a source of tensile stress for the nFET, but the pFET, which now lacks an analogous epitaxial SiGe layer, would benefit from a compressive CESL to boost in carrier hole mobility. *See* Sections VI.B and IX.B.1.h above.

i. Claim 11:

344. In my opinion, Cheng renders claim 11 obvious.

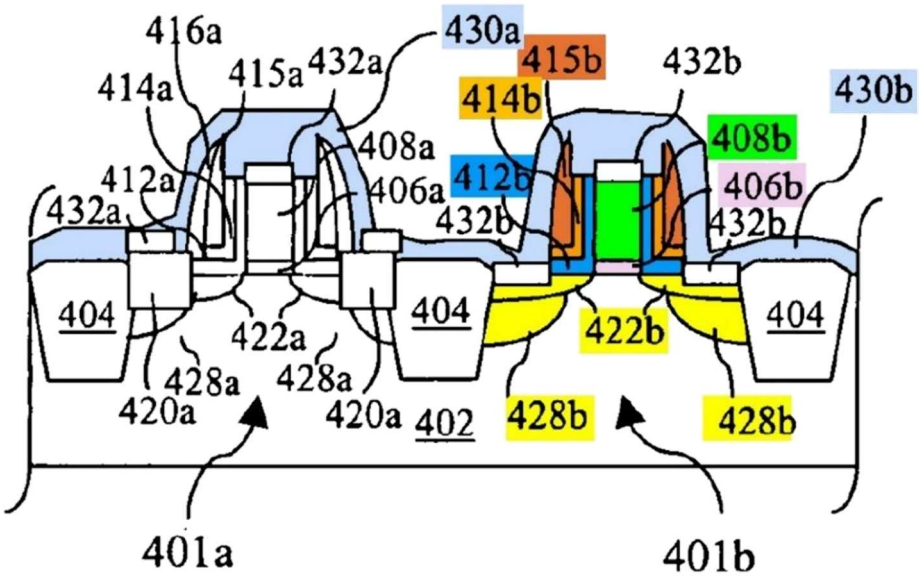
(1) [11Pre]: "The semiconductor device of claim 1"

345. Cheng renders the semiconductor device of claim 1 obvious. *See* Sections IX.C (introduction) and IX.C.1.a above.

346. For claim 11, because Cheng's NMOS 401b in Fig. 4j does not include the same rendering errors as pFET 401a, I annotate Cheng's original Fig. 4j. But because nFET 401b is the same in both Fig. 4j and Figure I, my discussion below applies equally to both. *See* Section IX.C (introduction) above.

(2) [11A]: "a second MIS transistor"

347. Cheng discloses "a second MIS transistor." Cheng explains that "semiconductor device 401b may be an N-type MOS device," i.e., an nFET. Cheng ¶[0056]; *see also* Cheng, Fig. 4j.



Cheng's Fig. 4j (annotated)

(3) [11B]: "a second gate insulating film formed on a second active region in the semiconductor substrate"

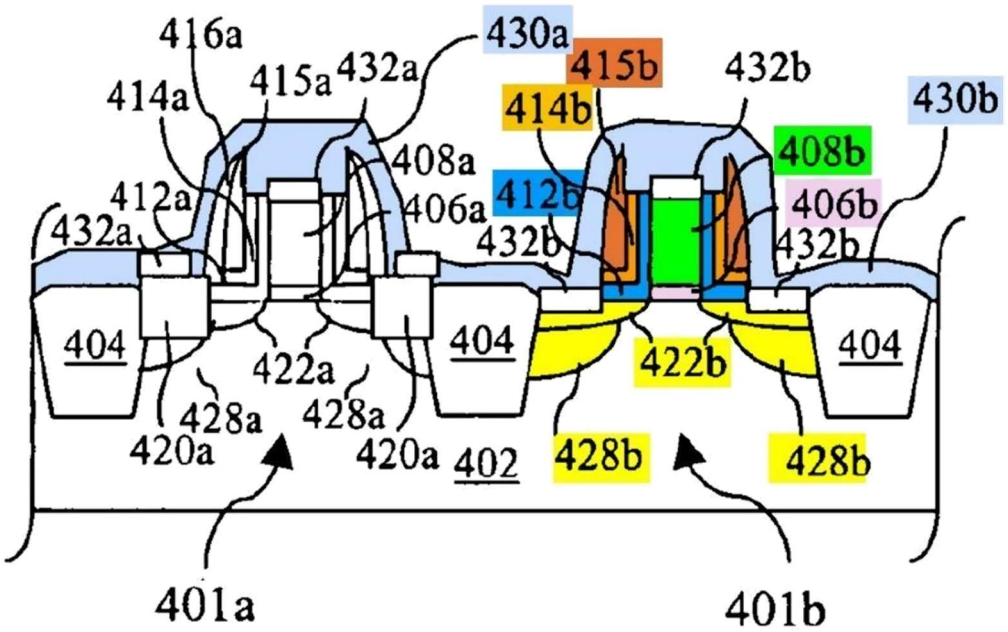
348. Cheng discloses "a second gate insulating film formed on a second active region in the semiconductor substrate."

349. Cheng discloses an nFET "gate dielectric . . . 406b" being "formed over a substrate 402." Cheng ¶[0056]; *see also* Cheng, Figs. 4a-4j. Cheng's gate dielectric layer 406b corresponds to a second gate insulating film because it is made of materials such as "silicon oxide" or "SiO_2" (i.e., silicon dioxide). Cheng ¶[0058].

This is the same as the '425 Patent's disclosure that the "gate insulating film" is made of "silicon oxide." '425 Patent, 9:15-19.

350. Cheng's substrate 402, on which gate dielectric 406b is formed, contains an active region—i.e., the portion of the substrate where a MIS transistor (here, nFET 401b) is located. The nFET active region includes, for example, "lightly doped regions . . . 422b" having "N-type dopants" and "heavily doped regions 428b." Cheng ¶[0056], ¶[0060], ¶¶[0065]-[0068], Fig. 4j.

351. In Fig. 4j below, nFET 401b is the second MISFET transistor. Cheng's gate insulating film 406b (light purple) of nFET 401b is formed on a portion of the substrate between the two lightly doped regions 422b. This portion of the substrate is the channel region, which, by definition, is part of the "active region" of nFET 401b.

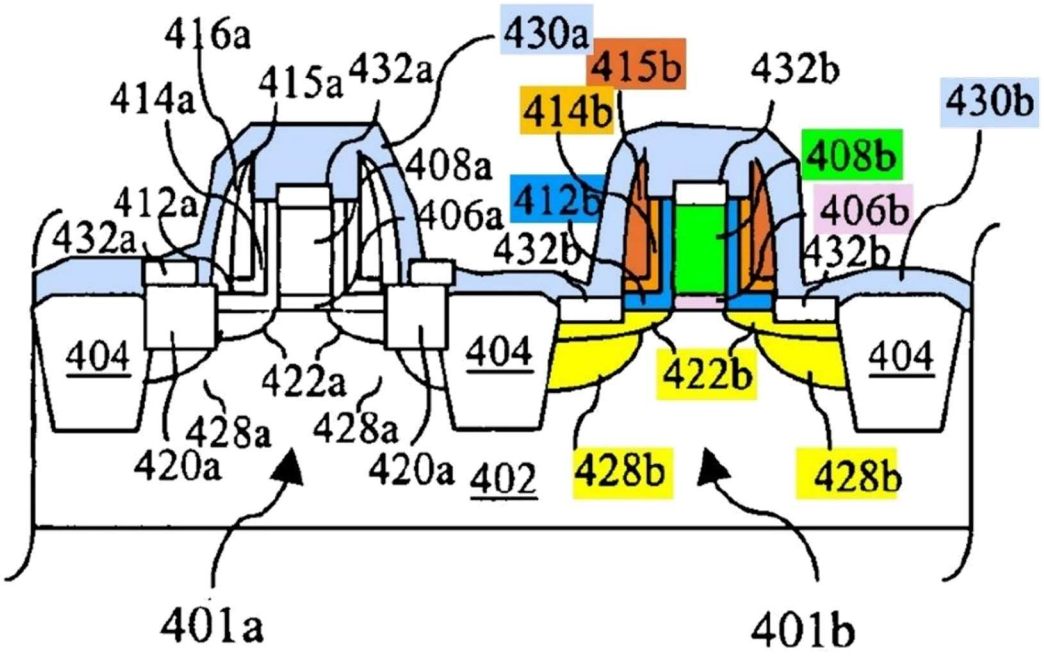


Cheng's Fig. 4j (annotated)

(4) [11C]: "a second gate electrode formed on the second gate insulating film"

352. Cheng discloses "a second gate electrode formed on the second gate insulating film."

353. Cheng discloses that "[g]ate electrode[] . . . 408b [is] formed over the gate dielectric layer [406b]." Cheng ¶[0056]. As annotated Fig. 4j shows below, second gate electrode 408b (green) is formed on the second gate dielectric 406b (light purple).



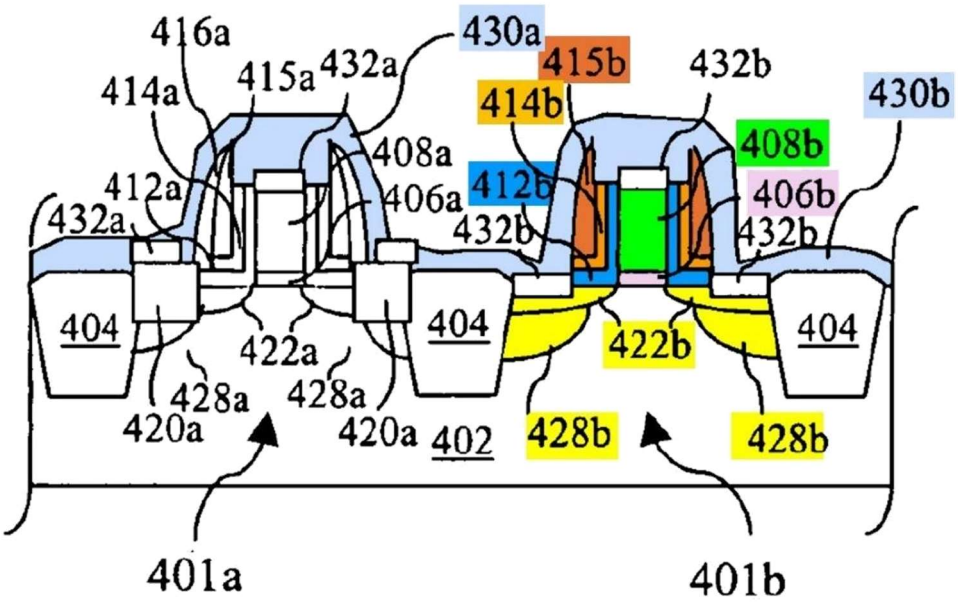
Cheng's Fig. 4j (annotated)

(5) [11D]: "a second sidewall spacer formed on a side surface of the second gate electrode"

354. Cheng discloses "a second sidewall spacer formed on a side surface of the second gate electrode."

355. Cheng discloses a second sidewall spacer comprising "sidewall dielectric layer[] . . . 414[] and spacer material 415 . . . disposed over the semiconductor device[] . . . 401b" (nFET). Cheng ¶[0061]. As I explain above for claim 1, Cheng teaches "etching" layers 414 and 415 to form "sidewall dielectric structures . . . 414b, and spacers . . . 415b, as shown in FIG. 4c." Cheng ¶[0061]. Cheng's Figs. 4c and 4j show that the second sidewall spacer (collectively, dielectric structure 414b and spacer 415b) is formed on a side surface of gate electrode 408b because, like the '425 Patent, they are formed laterally on the gate electrode. *See* Cheng ¶[0061], Figs. 4c, 4j; '425 Patent, FIG. 6B (transistor NTr, sidewall 19B).

356. As Fig. 4j shows below, the second sidewall spacer (sidewall dielectric structure 414b (light orange) and spacer 415b (dark orange), collectively) is formed on the sides of gate electrode 408b (green) in Cheng's nFET 401b.



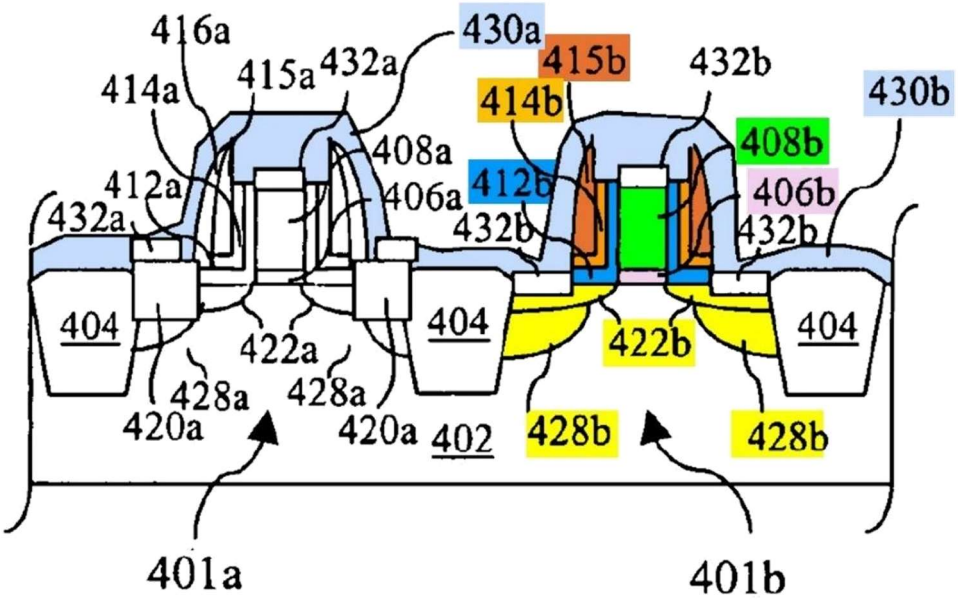
Cheng's Fig. 4j (annotated)

(6) [11E]: "a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer"

357. Cheng discloses "a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer."

358. Cheng discloses that "N-type MOS device" 401b includes "lightly doped regions . . . 422b [that] may include . . . N-type dopants for the device[] . . . 401b." Cheng ¶[0060]. N-type MOS device 401b also includes "heavily doped regions 428b" that "include N-type impurities." Cheng ¶[0066]. Lightly doped regions 422b and heavily doped regions 428b are classic examples of implanted source/drain layers. Additionally, "N-type dopants" are a second conductivity type (n-type) when the first conductivity type of claim 1 is p-type. *See* Cheng ¶[0060]; Section IX.C.1.a(6) above.

359. As Cheng's Fig. 4j shows below, source/drain regions 422b and 428b (yellow)—which are part of the nFET active region—are formed on a lateral side of the second sidewall spacers (layers 414b (light orange) and 415b (dark orange)). *See* Cheng, Fig. 4j.



Cheng's Fig. 4j (annotated)

(7) [11F]: "the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region"

360. Cheng discloses that "the stress insulating film [is] formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region." Cheng discloses a stress insulating film, such as tensile etch stop layer 430a/430b, which is "formed over the semiconductor device[] . . . 401b." Cheng ¶[0070], Fig. 4j.

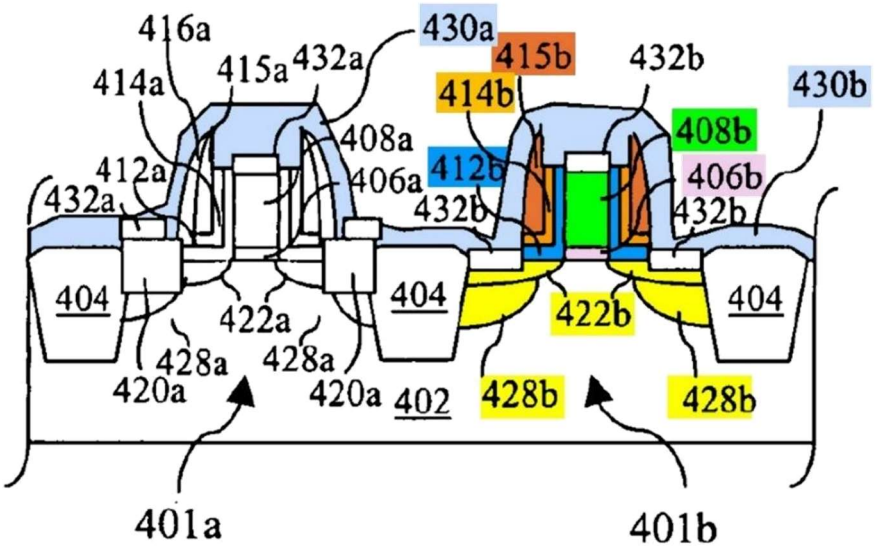
361. As Fig. 4j shows above, Cheng's etch stop layer 430a/430b (light blue) is formed over Cheng's nFET 401b to cover the gate electrode 408b (green), sidewall spacer (collectively, layers 414b (light orange) and 415b (dark orange)), and source/drain regions 422b and 428b (yellow). Cheng ¶[0070], Fig. 4j.

j. Claim 12: "The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region"

362. In my opinion, Cheng renders claim 12 obvious.

363. Cheng renders the semiconductor device of claim 11 obvious. *See* Sections IX.C (introduction), IX.C.1.a, and IX.C.1.i above.

364. Cheng discloses that no first stress-relief film (e.g., dummy spacer 416a) is formed on the second active region. For example, Cheng discloses that "the dummy spacer 716b [sic:416b] is removed from the [NMOS] device 401b," for example, "by chemical etch, plasma etch, CMP focused ion beam (FIB), and/or other processing techniques." Cheng ¶[0066], Figs. 4f-4j. Removing dummy spacer 416b removes the stress-relief film from the active region of NMOS 401b. Cheng ¶[0066], Figs. 4e-4j. As Fig. 4j shows below, dummy spacer 416a is present only on pFET 401a, not on nFET 401b.



Cheng's Fig. 4j (annotated)

2. Ground 2B: Cheng and Wolf Render Claim 2 Obvious

365. In my opinion, the Cheng-Wolf combination renders claim 2 obvious.

a. The Cheng-Wolf Combination Would Have Been Obvious to a POSITA

366. In my opinion, a POSITA would have found it obvious to modify Cheng's transistors described in claim 1 to add an I-shaped offset spacer, as Wolf discloses, for the same reasons I describe above in Section IX.B.2 for the Wu-Alvarez-Wolf combination.

367. Wolf discloses an I-shaped "offset-spacer [being] fabricated on the side of the gate after the gate-poly is etched." Wolf, 217, Fig. 5-25. Wolf further explains that an I-shaped offset spacer "yields optimum device characteristics" by spacing the channel region apart from the source-drain extension ("SDE") region and preventing "excessive leakage (due to larger short-channel effects that arise if the channel-length is too small)." Wolf, 216-17, Fig. 5-25.

368. In addition to Wolf's teachings, a POSITA would have known that I-shaped offset spacers were commonly used structures to facilitate control over source/drain extension profiles and to mitigate short channel effects. *See* Thompson1998, 132 (describing offset spacers to control source/drain extension profiles), Fig. 2; Suzuki995 ¶[0061] (explaining that offset spacers act as masks to "form p-type extension regions"), FIG. 1(b); Fleetwood, Tbl. 3.1 (describing I-shaped offset spacers as "optional" in a "Typical CMOS Process Flow"); Wiatr

¶[0033]; Kammler ¶[0024] ("A width of the offset spacer 105 is selected in accordance with process requirements for forming the lateral dopant profile of extension regions 106 formed within the substrate 101 adjacent to the channel region 104."), FIGS. 1a-2; Wei ¶[0058] (explaining that "offset spacer 231 may be used for defining an extension region 211"), FIGS. 2c-2h; Suzuki465 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C.

369. Having known of Wolf's teachings and being aware of the purpose and benefits of I-shaped offset spacers, a POSITA would have been motivated to add Wolf's I-shaped offset spacers to Cheng's transistors, as the exemplary embodiment of Figure J below shows, to mitigate short channel effects and better control the doping profiles of lightly doped regions 422a and 422b. Figure J shows Cheng's Fig. 4a as modified to show an embodiment with I-shaped offset spacers, as Wolf discloses, before implanting lightly doped regions 422a and 422b.

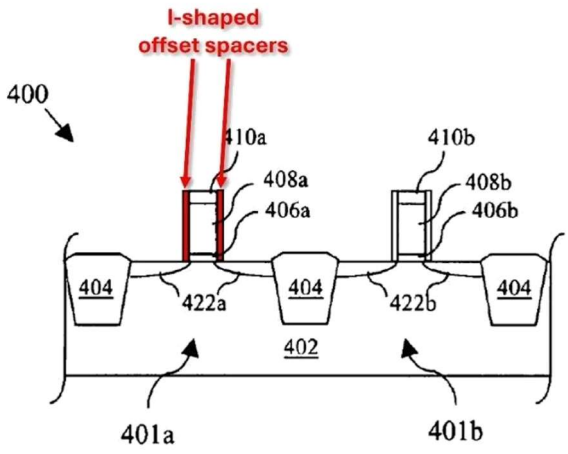
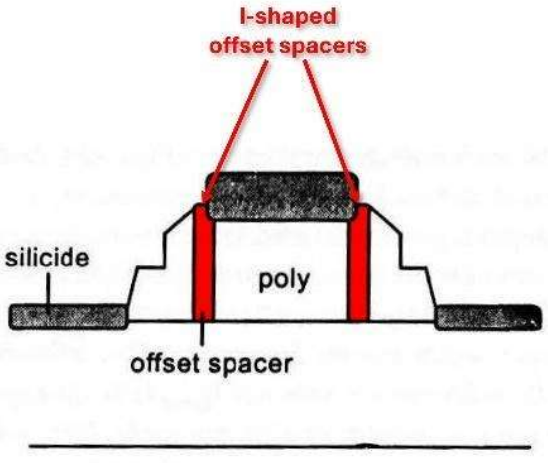
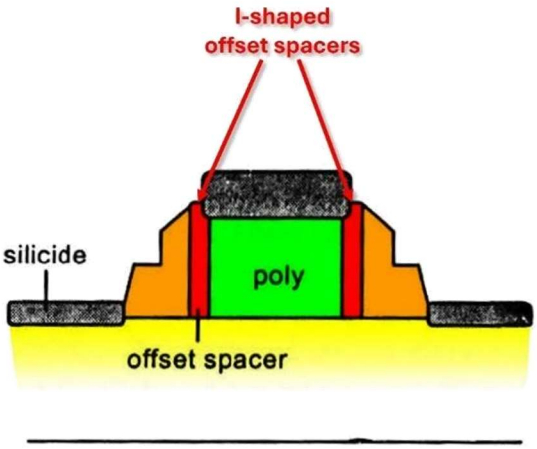


Figure J



Wolf's Fig. 5-25 (annotated)

370. In my opinion, a POSITA would have reasonably expected to succeed when adding an I-shaped offset spacer, as Wolf discloses, to Cheng's FETs (*see* Figure J) because it represents a conventional use of known techniques to achieve ordinary and expected results (i.e., reduced short channel effects and better control over lightly doped source/drain extension regions). *See* Wolf, 217, Fig. 5-25; Suzuki995 ¶[0061]; Thompson1998, 132, Fig. 2; Fleetwood, Tbl. 3.1; Wiatr ¶[0033]; Kammler ¶[0024], FIGS. 1a-2; Wei ¶[0058], FIGS. 2c-2h; Suzuki465 ¶[0080], ¶[0088], ¶[0091], FIGS. 8A-11C. Such known techniques include forming an offset spacer either by thermal oxidation or by deposition and etching, as the references cited above describe. As Wolf demonstrates, a POSITA would have understood to form such I-shaped offset spacers before forming Cheng's sidewalls 412a/412b, 414a/414b, and 415a/415b, as Figures J (above) and K (below) show, and then forming lightly doped source/drain regions 422a and 422b. *See* Wolf, 216-17, Fig. 5-25. A POSITA would have understood that Cheng's processing would then proceed as described. *See* Sections IX.C and IX.C.1.a above; Wiatr ¶[0033], FIG. 2h.



Wolf's Fig. 5-25 (annotated)

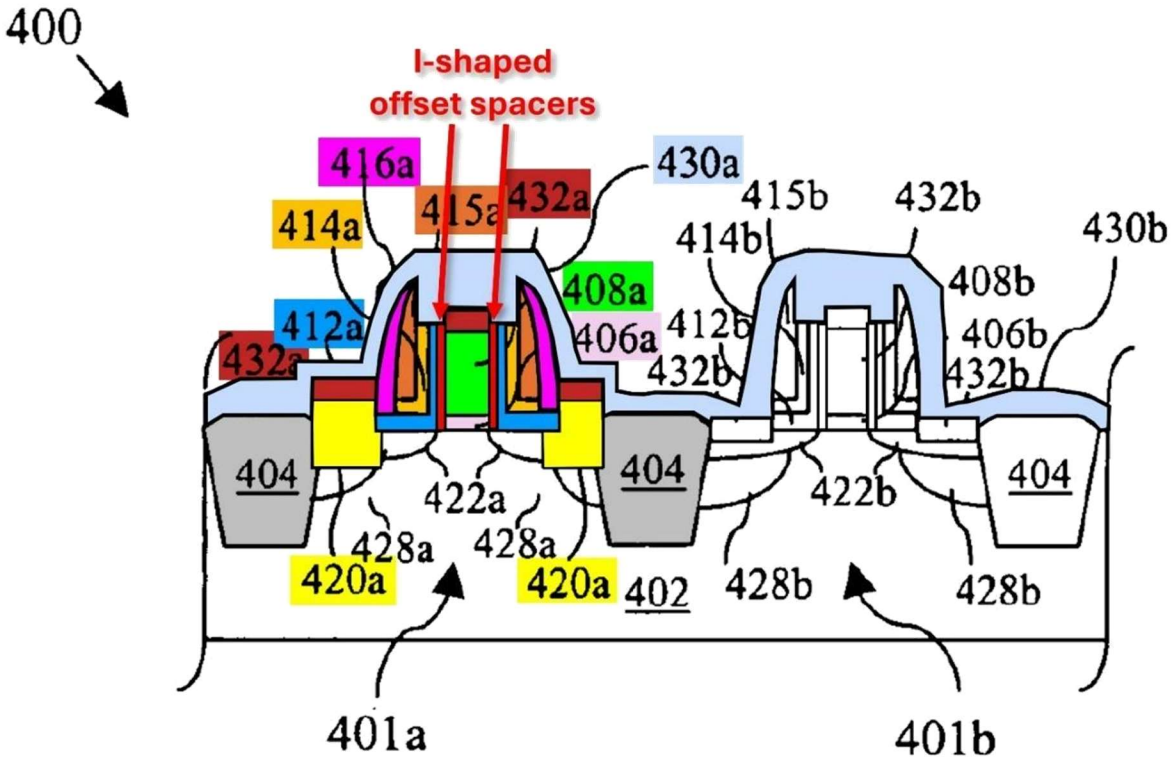


Figure K

371. In my opinion, a POSITA would have found it obvious to add I-shaped offset spacers, as Wolf discloses, to Cheng's FETs of claim 1 because it is an example of the following:

- It combines known prior art elements according to known methods (forming an I-shaped offset spacer before forming source/drain extension regions) to yield predictable results (better control over lightly doped source/drain extension profiles and reduced short channel effects).
- It uses a known technique (forming a standard I-shaped offset spacer, as Wolf and others disclose) to improve similar devices (Cheng's MOSFETs) in the same way (e.g., by mitigating short channel effects and better controlling lightly doped source/drain extension profiles).
- It applies known techniques (forming a standard I-shaped offset spacer, as Wolf and others disclose) to a known device ready for improvement (Cheng's MOSFETs) to yield predictable results (reduced short channel effects and better control over source/drain extension profiles).
- It applies a known teaching, motivation, or suggestion in the prior art (e.g., the teachings of Wolf and others described above) that would have led a POSITA to modify Cheng according to, or to combine Cheng with, the teachings of Wolf to arrive at the claimed invention.

b. Claim 2: "The semiconductor device of claim 1, further comprising: a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape"

372. In my opinion, the Cheng-Wolf combination renders claim 2 obvious.

373. As I explain above in Section IX.C.2.a, a POSITA would have found it obvious to incorporate I-shaped offset spacers, as Wolf discloses, between Cheng's gate electrode 408a and sidewall spacer layers 414a and 415a to mitigate short channel effects and better control the profile of lightly doped source/drain regions 422a. *See* Section IX.C.2.a above. Additionally, a POSITA would have recognized that such a modification would have yielded a structure like the one in Figure K below. *See* Section IX.C.2.a above; Wiatr ¶[0033], FIG. 2h.

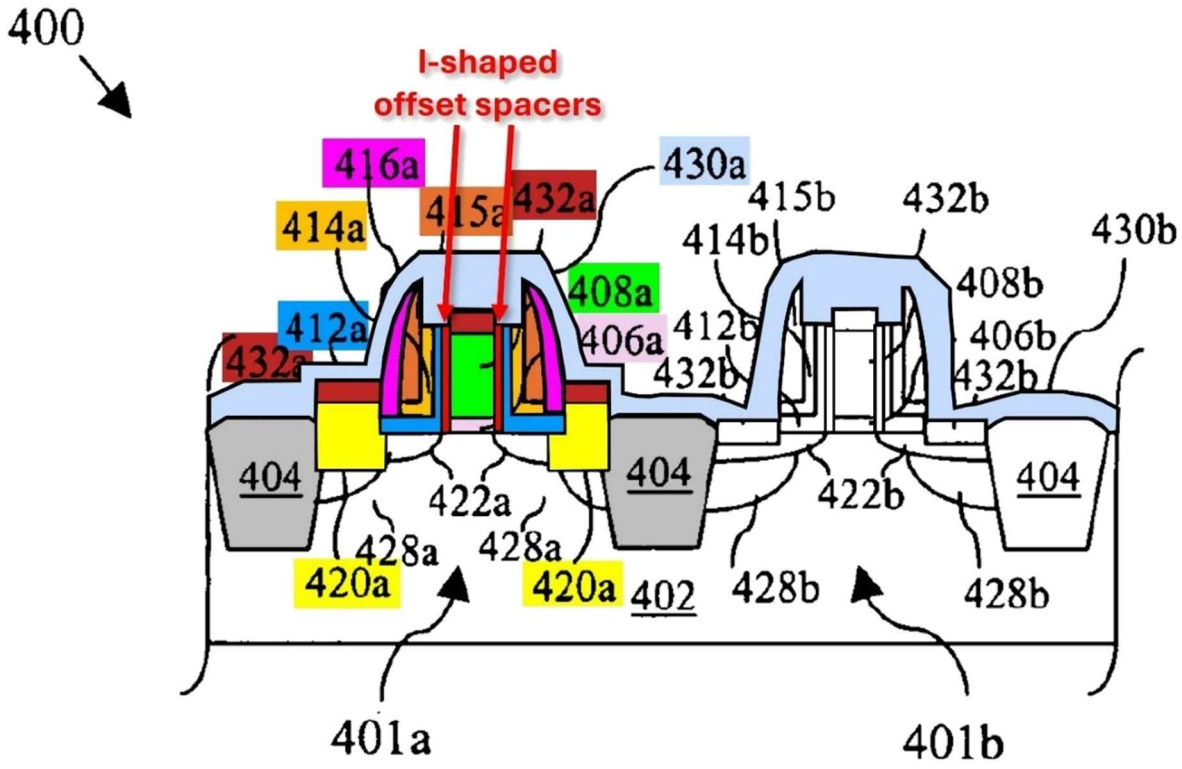


Figure K

3. Ground 2C: Cheng and Wang Render Claims 1, 3-9, 11, and 12 Obvious

374. I have also been asked to consider a situation in which the Patent Owner may argue that Cheng alone does not render claims 1, 3-9, 11, and 12 obvious based on its textual descriptions of Figs. 4a-4j. In that situation, although I disagree for the reasons I discuss above in Section IX.C (introduction), it is my opinion that a POSITA would have found those claims obvious based on the combination of Cheng and Wang for the reasons I explain in Sections IX.C (introduction) through IX.C.1.j above, as well as for the well-known advantages of using raised epitaxial SiGe stressors discussed in Section VI.B above. Adding Wang to Cheng does not alter any of the invalidity analysis I provide above for claims 1, 3-9, 11, or 12; Wang merely confirms the obviousness of the structure I present in Figure I.

4. Ground 2D: Cheng, Wang, and Wolf Render Claim 2 Obvious

375. I have also been asked to consider the situation in which the Patent Owner argues that Cheng and Wolf do not render claim 2 obvious for essentially the same reasons noted above in Section IX.C.3. In that situation, although I disagree for the reasons I discuss above in Section IX.C (introduction), it is my opinion that a POSITA would have found claim 2 obvious based on the combination of Cheng, Wang, and Wolf for the reasons I explain in Sections IX.C (introduction), IX.C.2, and IX.C.3 above, as well as for the well-known advantages of using raised epitaxial

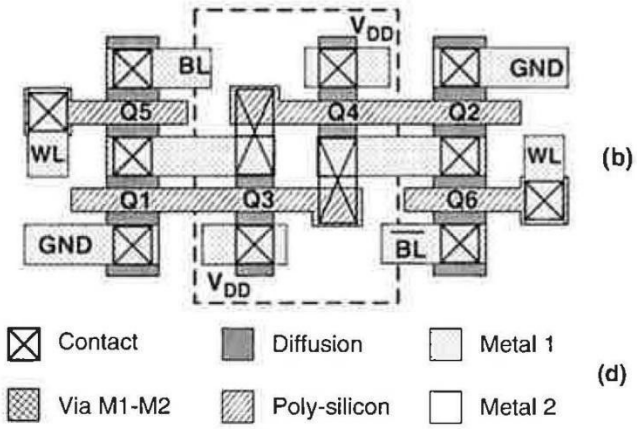
SiGe stressors discussed in Section VI.B above. Adding Wang to the Cheng-Wolf combination does not alter any of the invalidity analysis I provide above for claim 2; Wang merely confirms the obviousness of the structure I present in Figures I and K.

D. Ground 3: Saito Grounds

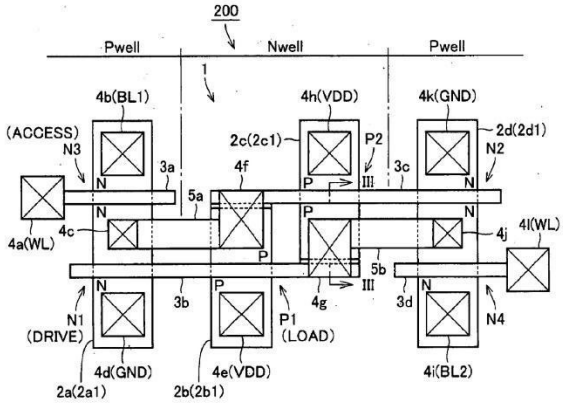
1. Ground 3: Saito, Fukutome, and James Render Claims 1, 3, 4, 7, 8, and 10 Obvious

376. In my opinion, the combination of Saito, Fukutome, and James renders claims 1, 3, 4, 7, 8, and 10 obvious.

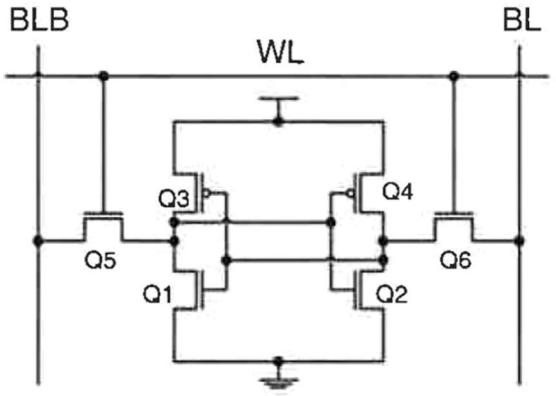
377. Saito describes a textbook SRAM cell. *See* Saito ¶¶[0003]-[0005], ¶¶[0049]-[0050], FIGS. 1-2; Pavlov, 24-25, Figs. 2.10(b)-(d); Matsui ¶[0055], FIGS. 1-3; Ishida, Tbl. 1; Balobas, 1, Fig. 1; Thompson498, ¶¶[0063]-[0065], FIGS. 39-40B. More specifically, it describes an SRAM cell known in the art as a 6T (six-transistor) "wide" SRAM cell. Pavlov, 24-25, Figs. 2.10(b)-(d). Below, I compare Saito's SRAM cell layout and circuit to the examples from a textbook called "CMOS SRAM: Circuit Design and Parametric Test in Nano-Scaled Technologies." *Compare* Pavlov, 24-25, Figs. 2.10(b)-(d), *with* Saito ¶¶[0028]-[0029], FIGS. 1-2. As these comparisons make clear, their layouts and circuits are the same. Saito's SRAM cell is literally "textbook."



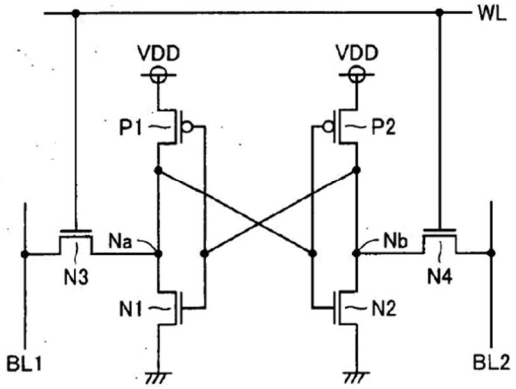
Pavlov's Figs. 2.10(b), (d)



Saito's FIG. 1



Pavlov's Fig. 2.10(c)



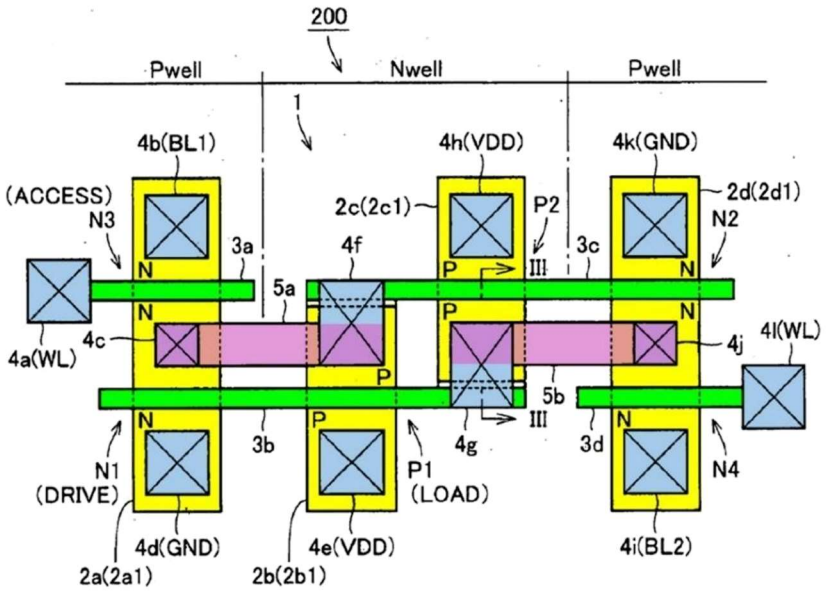
Saito's FIG. 2

378. As a POSITA would have expected of such an SRAM cell, Saito discloses five traditional SRAM layers, with each layer sharing similar numbers. In other words, the item numbers 2*x* correspond to one layer, item numbers 3*x* correspond to another layer, and so on. The list below identifies each of these layers, including the color in which they appear in annotated FIG. 1 below:

- Substrate layer: **1**00 (uncolored). *See* Saito ¶[0072].

- Active regions and source/drains: **2**a-**2**d (yellow). *See* Saito ¶¶[0060]-[0061].
- Polysilicon wirings: **3**a-**3**d (green). *See* Saito ¶¶[0067]-[0068], ¶[0124].
- Contact parts: **4**a-**4**l (blue). *See* Saito ¶¶[0068]-[0069].
- Metal wirings: **5**a-**5**b (purple). *See* Saito ¶¶[0070]-[0071].

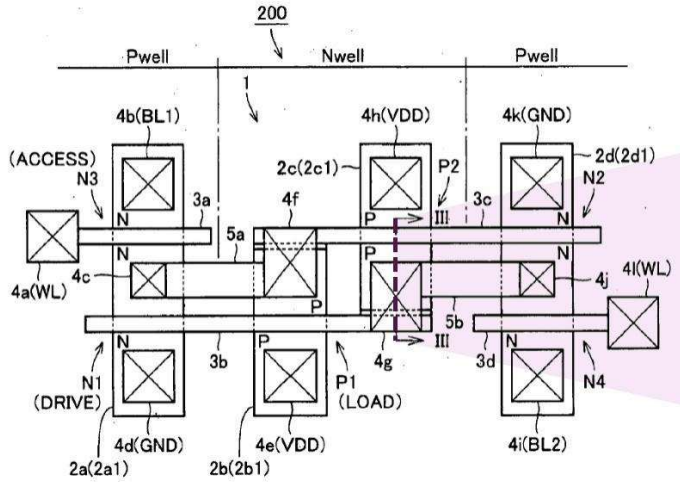
FIG.1

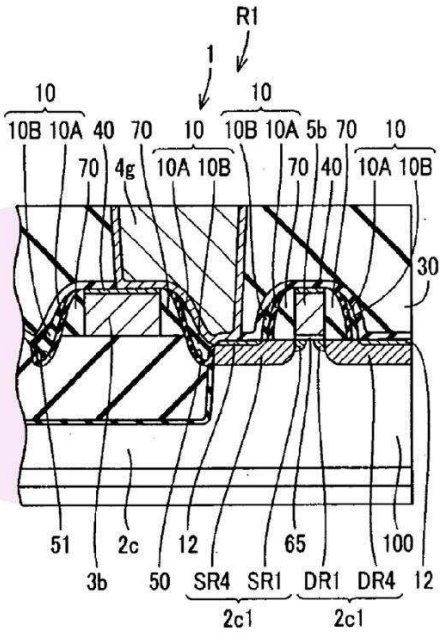


Saito's FIG. 1 (annotated)

379. In Saito's figures and description, "[p]olysilicon wirings 3a-3d constitute a gate of each MOS transistor." Saito ¶[0067]. "[C]ontact parts 4a-4l" provide a connection with an "upper wiring" layer. Saito ¶[0068]. The "upper wiring" layer includes "metal wiring[s]," including "metal wiring 5b" that connects "the drain of second [pFET] load transistor P2" at "contact part[] (common contact) 4g" and the "drain of second driver NMOS transistor N2" at "contact part 4j." Saito ¶[0071]; *see also* Saito, FIG. 1.

380. Because metal wiring 5b connects contact parts 4g and 4j, a POSITA would have recognized that metal wiring layer 5b is an "upper wiring" layer that would have been formed above the cross-sections shown in Saito's FIGS. 12-21 (e.g., connecting the top of contacts 4g/4j as was conventional). More specifically, the cross-sections shown in Saito's FIGS. 12-21 do not actually show metal wiring 5b because it is a higher layer formed on top of contact part 4g.





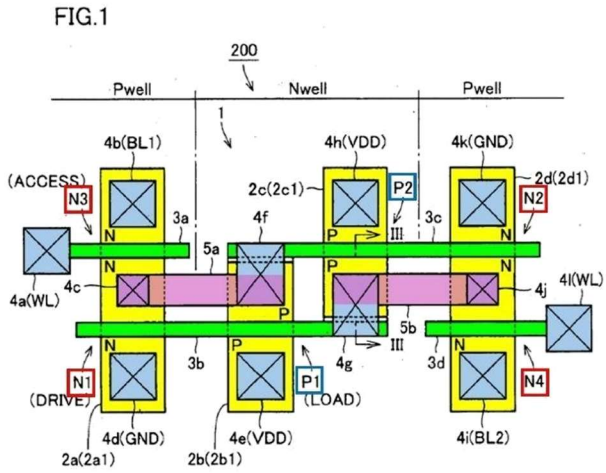
Saito's FIG. 1 **Saito's FIG. 12 (excerpted)**

381. Region R1 on the right sides of Saito's FIGS. 12-21 corresponds to the cross-sections along cutline III-III in FIG. 1 (see above). *Compare* Saito ¶[0030], ¶[0072], FIGS. 3-11, *with* Saito, FIGS. 12-21. A POSITA reading Saito's specification would have recognized that FIGS. 12-21 contain a typographical error: the label "5b" should read "3c." *See* Saito ¶¶[0065]-[0067], ¶[0071], FIGS. 1, 12-21.

382. For several reasons, a POSITA would have understood the label "5b" in FIGS. 12-21 should read "3c." First, the identifier "5b" refers to a "metal wiring 5b," not a polysilicon wiring like the one it purports to represent in FIGS. 12-21. Saito ¶¶[0070]-[0071]. Second, Saito discloses a conventional SRAM cell, and the gate electrode in FIGS. 12-21 is the polysilicon layer that Saito consistently identifies with a 3*x* identifier. All polysilicon wirings should be identified by a number 3*x*. Third, a POSITA would have immediately recognized that it makes no sense for a polysilicon wiring to have a 5*x* identifier because, as Saito explains, the metal wirings 5*x* connect contact parts 4*x* in the upper layer metal wirings that are not shown in FIGS. 12-21. Fourth, a POSITA would have recognized that when this typographical error is corrected to read "polysilicon wiring **3c**" rather than "polysilicon wiring **5b**" in FIGS. 12-21 and the accompanying text, Saito's descriptions match what would be expected along cutline III-III in FIG. 1. This confirms both the typographical error and the appropriate correction, bringing Saito's FIGS. 12-21 in line with the textbook understanding of such an SRAM cell.

383. Below, I have annotated Saito's FIG. 1 and placed it next to an annotated version of FIG. 40B from one of my own patents that shows a perspective view of an SRAM cell like the one Saito describes in FIG. 1. *See* Thompson498, FIG. 40B. The annotated figure from my patent shows Saito's layers 1*x*, 2*x*, and 3*x* but stops there. It does not show contact parts 4*x* or metal wirings 5*x*. As should be

readily apparent, polysilicon wirings 3*x* (green) match in these two figures, as expected. Cutline III-III has also been annotated onto FIG. 40B for clarity.



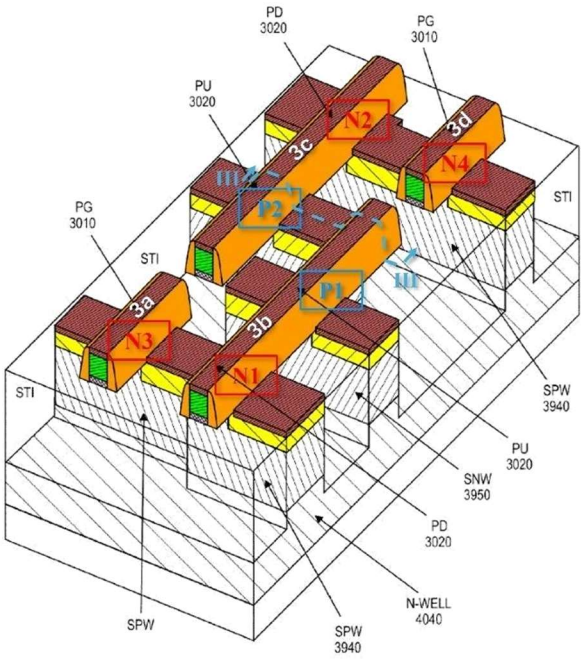


FIG. 40B

Saito's FIG. 1 (annotated) **Thompson498's FIG. 40B (annotated)**

384. A POSITA also would have recognized that, because Saito's contact parts 4g and 4j and metal wiring 5b are conventional SRAM structures, they would have appeared as shown below in annotated Figure L (amending, annotating Thompson498, FIG. 40B),[26] with the layer for the metal wirings (5*x*) located above the polysilicon lines (3*x*) and connecting contact parts (4*x*) as upper-level wirings, as described in Saito. Saito ¶¶[0070]-[0071], FIG. 1; *see also* Pavlov, 24-25, Figs. 2.10(b)-(d); Balobas, Figs. 1-2.

[26] For ease of reference, I do not include Saito's other contact parts 4*x* or metal wiring 5*a*, because they would obscure the relevant parts of Figure L.

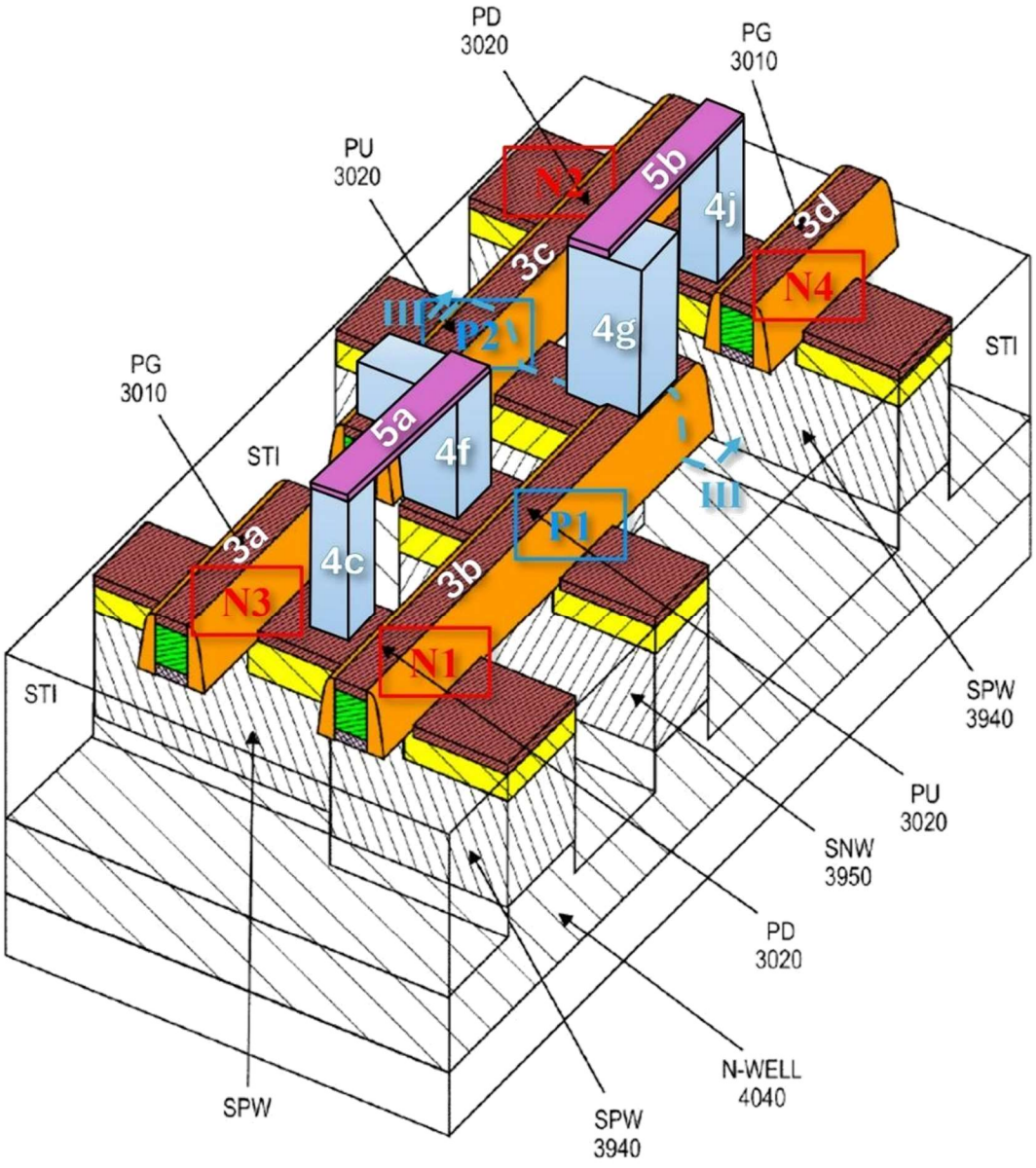


FIG. 40B

Figure L

385. A POSITA would have immediately recognized that this clerical error (i.e., referring to polysilicon wiring 3c as "5b") is repeated through Saito's description of FIGS. 12-21, such that "polysilicon wiring 5b" should refer to "polysilicon wiring ***3c***" throughout those descriptions.

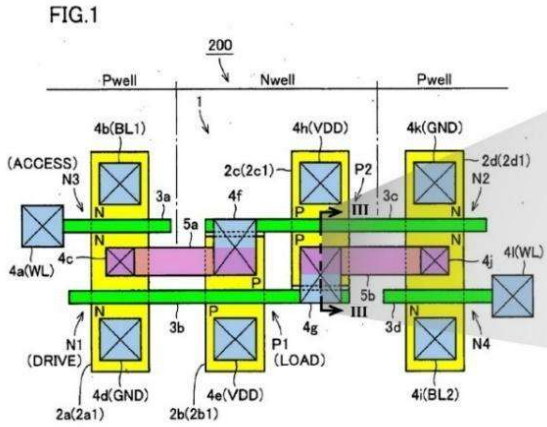
386. Based on Saito's description that each identifier 2*x*, 3*x*, 4*x*, and 5*x* corresponds to a different material layer of the SRAM cell and generally similar structures (e.g., source/drain, gate, contact, or metal wiring), a POSITA would have recognized that "polysilicon wiring 5b" in Saito's FIGS. 12-21 should refer to "polysilicon wiring ***3c***." Saito ¶¶[0066]-[0068], ¶[0124]. A POSITA would have immediately noted that "polysilicon wirings" are designated 3*x* consistently in the specification and figures, and that a designation of "5*x*" (the designation for upper metal wirings) does not match. Thus, FIGS. 12-21 should show polysilicon wiring "**3c**" of FIG. 1 to match cutline III-III, and the polysilicon should not be designated with "5b." Saito confirms this clerical error because it refers to "5b" correctly in other figures as a "metal wiring" that connects contact parts 4g and 4j, not a polysilicon line like the ones in FIGS. 12-21. Saito ¶¶[0066]-[0068], ¶[0071], ¶[0124]. A POSITA would have recognized this discrepancy and noted that polysilicon 3c is part of cutline III-III of FIG. 1, concluding that the polysilicon line marked "5b" in FIGS. 12-21 should be "polysilicon wiring ***3c***" instead of "5b."

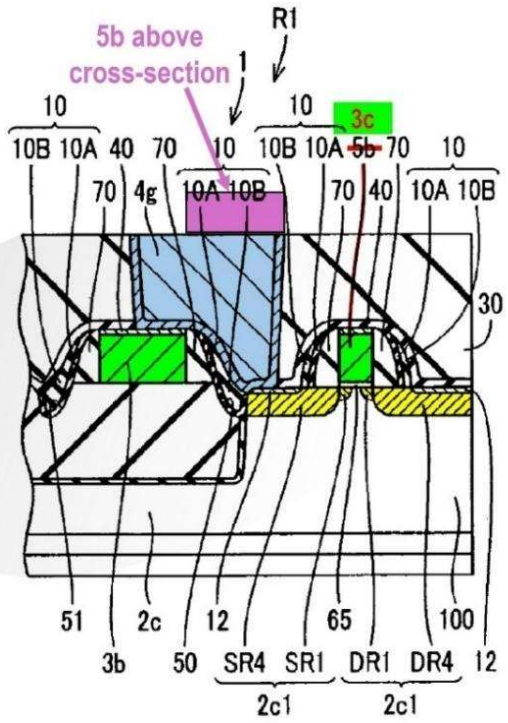
387. A POSITA also would have recognized that the "5b" label for polysilicon would not make sense in the context of Saito's figures because cross-section line III-III in FIG. 1 crosses two polysilicon wirings, 3b and 3c, and contact 4g touches polysilicon wiring 3b and metal wiring 5b, but not polysilicon wiring 3c. *See* Saito FIG. 1. Saito's FIGS. 12-21 do not show contact part 4g

touching the polysilicon wiring labeled "5b," as expected from FIG. 1. This further confirms that the polysilicon gate in FIGS. 12-21 should be labeled "3c." Moreover, "polysilicon wiring 3c" is the polysilicon gate for PMOS transistor P2, as shown in FIG. 1, and thus corresponds to a gate structure. Saito describes "polysilicon wiring 5b" as part of a transistor, shows it as a gate structure, and does not show it touching contact 4g, all of which confirms that "polysilicon wiring 5b" should be "polysilicon wiring ***3c***" of PMOS transistor P2, consistent with Saito's FIG. 1. Saito ¶¶[0093]-[0096], ¶[0101].

388. Moreover, if wiring "5b" indicated in FIGS. 12-21 corresponded with wiring "5b" shown in FIG. 1, then the wire needed to connect node Nb to transistor N4 in Saito's FIG. 2 would be disconnected due to the presence of "gate **insulating film** 65," which would block current from flowing. Saito ¶[0051] (emphasis added); *see also* Saito, FIGS. 1-2, 12. A POSITA would have recognized that such a structure would be absurd and at odds with the fundamental basics of SRAM circuit design. *See* Saito ¶[0071], FIGS. 1-2, 12; Pavlov, 24-25, Figs. 2.10(b)-(d). No one skilled in the art reading Saito would have fairly read Saito in that way.

389. Instead, a POSITA would have immediately recognized that Saito's polysilicon wiring labeled "5b" in FIGS. 12-21 should read "***3c***," as shown below.



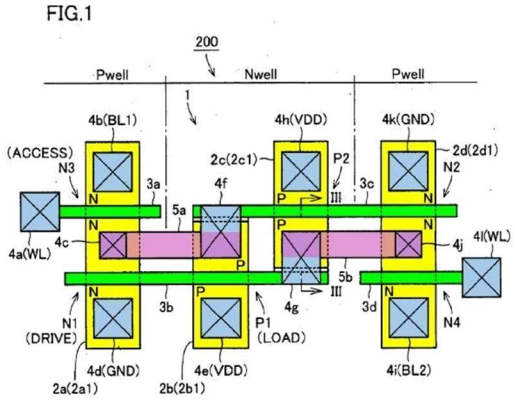


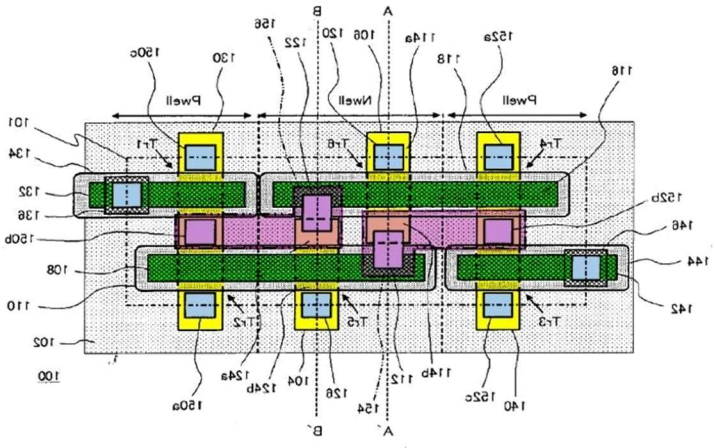
Saito's FIG. 1 (annotated) **Saito's FIG. 12 (excerpted, annotated)**

390. Correcting this obvious typographical error, region R1 in FIGS. 12-21 then reflects the correct cross-section corresponding to line III-III of FIG. 1. As illustrated above, polysilicon wiring 3b appears on the isolation region, polysilicon wiring ***3c*** appears as the gate electrode of pFET P2, and common contact part 4g connects polysilicon wiring 3b to the drain of pFET P2. Saito ¶[0071], ¶[0081], FIGS. 1, 12. A POSITA would have understood that "metal wiring 5b" is an "upper wiring" lying above and connected to contact parts 4g and 4j (and thus not shown in Saito's cross-sections of FIGS. 12-21). *See* Saito ¶[0068], ¶[0071]; Pavlov, 24-25, Figs. 2.10(b)-(d); Balobas, Figs. 1-2; Matsui, FIGS. 1-3. Again, this is textbook.

391. In addition to the textbook I discuss above, other prior art confirms this understanding. Below, for example, I show Saito's FIG. 1 side-by-side with Matsui's

FIG. 1 (which I flipped over the vertical axis for easier comparison). They both have the same 6T "wide" SRAM layout. *Compare* Saito, FIG. 1, *with* Matsui, FIG. 1; *see* Pavlov, 24-25, Figs. 2.10(b)-(d).





Saito's FIG. 1 (annotated) **Matsui's FIG. 1 (annotated, flipped)**

392. Matsui's cross-section lines A-A' and B-B' in FIG. 1 are similar to Saito's cross-cut line III-III. As I explain below, Matsui's cross-sections confirm my opinion regarding Saito's typographical error, which would have been readily apparent to a POSITA who understands this technology.

393. Matsui's "FIG. 1 is a top view" of the SRAM cell. Matsui ¶[0055]. Like Saito's PMOS active regions 2b and 2c, Matsui's SRAM includes PMOS active regions 104 (FIG. 3) and 106 (FIG. 2). *See* Matsui ¶[0056], FIGS. 1-3; Saito ¶[0060], FIGS. 1, 12. Matsui's SRAM includes PMOS source/drain regions 124a/124b (FIG. 3) and 114a/114b (FIG. 2), similar to Saito's source/drain regions 2b1 and 2c1. *See* Matsui ¶[0062], ¶[0065], FIGS. 1-3; Saito ¶[0060], FIGS. 1, 12. Matsui further

includes PMOS gate electrodes 108 and 116, similar to Saito's polysilicon layers 3b and 3c. *See* Matsui ¶[0062], ¶[0065], FIGS. 1-3; Saito ¶[0066], FIGS. 1, 12. And Matsui's contacts 112 and 122 connect the source/drain regions with upper-layer interconnections 154 and 156, similar to Saito's contacts 4f and 4g. *See* Matsui ¶[0063], ¶[0066], FIGS. 1-3; Saito ¶[0069], FIGS. 1, 12.

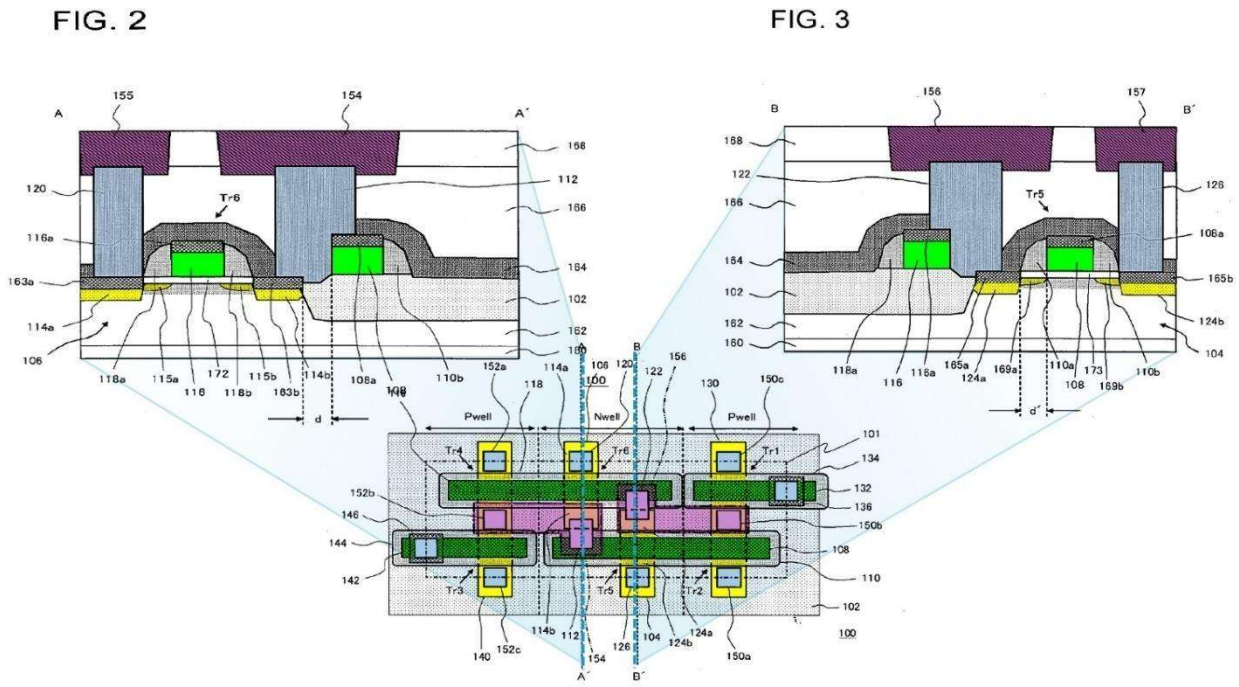


Figure O (Matsui's FIGS. 1-3 (annotated))

394. Figure O above shows Matsui's FIG. 1 with callouts to FIG. 2 (cross-section taken along FIG. 1 cutline A-A') and FIG. 3 (cross-section taken along FIG. 1 cutline B-B'). *See* Matsui ¶¶[0038]-[0040], ¶¶[0060]-[0061], ¶[0064], ¶[0069], FIGS. 1-3. In both cross-sections, the metal wirings 154 and 156 (purple) lie above the contact parts (light blue) and well above the polysilicon layers (green). This is what I indicated above regarding Saito, and it further confirms that a POSITA

would have understood Saito's clerical error. To be clear, there is no other way a POSITA could have interpreted Saito's disclosures.

395. A POSITA would have readily understood the typographical error in Saito because Saito's disclosure does not purport to alter the conventional layout, circuit, or structure of this textbook SRAM cell. Instead, it addresses issues associated with recesses (50) formed in the isolation regions adjacent to the source/drain regions. *See* Saito, Abstract, ¶[0011], ¶¶[0022]-[0023], ¶[0027], ¶¶[0074]-[0075], FIGS. 1-3; Pavlov, 24-25, Figs. 2.10(b)-(d). Immediately recognizing and mentally correcting the typographical error in Saito, a POSITA would have recognized that FIGS. 12-21 show conventional SRAM cross-sections along cutline III-III of FIG. 1.

396. No matter how one views Saito's disclosures, a POSITA would have recognized that polysilicon wiring 3c of FIG. 1 has the same structure as the one labeled "5b" in FIGS. 12-21. *See* Saito ¶[0124] ("In FIG. 1, other polysilicon wirings 3a, 3c, and 3d are formed similarly, and contact parts 4f are formed like contact parts 4g."). In other words, a POSITA would have immediately recognized (1) that Saito contains a clerical error whereby "polysilicon wiring 5b" refers to and should be labeled "polysilicon wiring 3c" in FIGS. 12-21, and, regardless, (2) that the structure labeled "polysilicon wiring 5b" in FIGS. 12-21 is part of a MIS transistor with the structure I rely on in forming my opinions below.

397. All of my observations above regarding Saito's typographical error and disclosed structures remain true when substituting Fukutome's epitaxial SiGe source/drain regions for Saito's non-epitaxial source/drain regions in active regions 2b and 2c.

a. The Saito-Fukutome-James Combination Would Have Been Obvious

398. In my opinion, a POSITA would have found it obvious to incorporate epitaxial SiGe source/drain layers, as Fukutome discloses, into Saito's source/drain regions 2c1 to improve pFETs P1 and P2 with compressive strain. Figure M below shows an embodiment of this. *See* Section VI.B above; Fukutome ¶[0110], FIG. 5G. Figure M shows a composite version equivalent to Saito's FIG. 21 before the ILD layer 30 is added over CESL 13.[27]

399. Again, Figure M below shows an embodiment of the Saito-Fukutome-James combination.[28] This combination simply involves (1) incorporating epitaxial SiGe source/drain regions (yellow), as Fukutome and James both disclose, into Saito's source/drain regions 2c1, and (2) making Saito's "plasma nitride (SiN)" insulating film 13 tensile, as James discloses.

[27] I based Figure M on composite FIG. 21 for ease of reference because this figure shows an intermediate step corresponding to FIG. 11 before contact plug 4g is added.
[28] I have corrected Saito's clerical error to replace "5b" with "3c." *See* Section IX.D.1 above. I show label "3c" in red to mark it as corrected.

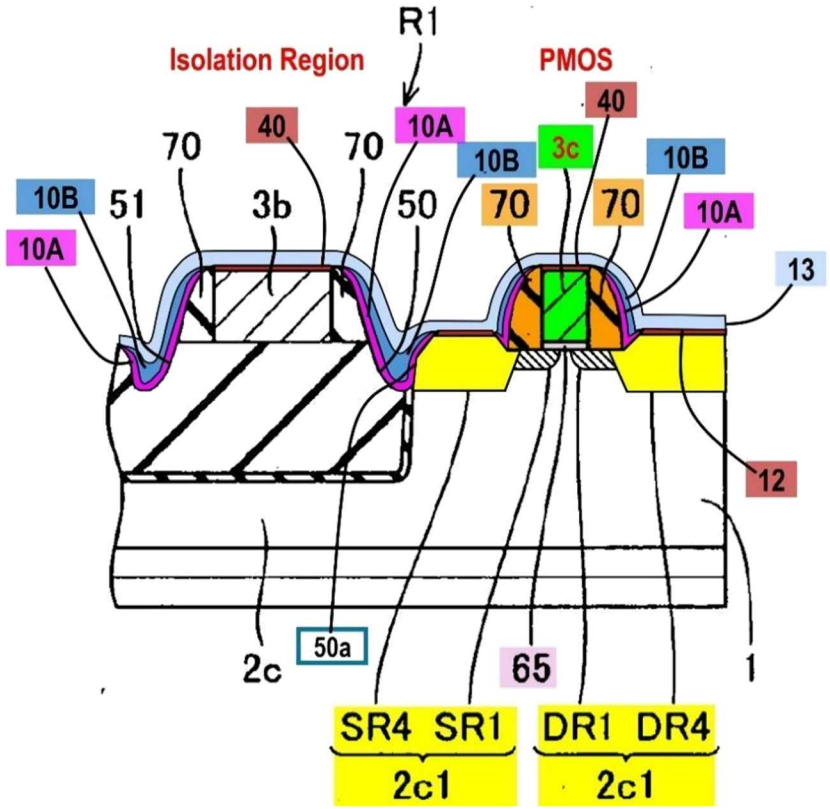


Figure M

400. By the time the application for the '425 Patent was filed, faceted epitaxial SiGe source/drain regions were standard industry practice to enhance pFET performance. Such SiGe source/drain regions had been widely known and used in each of the four previous generations of high-volume commercial transistors. *See* Section VI.B above; Thompson2004, 1790-96 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry, 247-50 (describing Intel's 45nm devices); Natarajan, 1 (describing Intel's 32nm devices). In my opinion, a POSITA would have found it obvious to incorporate epitaxial SiGe source/drain regions (as Fukutome discloses) into Saito's source/drain regions 2c1 because doing so was a very well-known way to improve pFET performance. *See* Section VI.B.

401. Using a tensile CESL to boost nFETs performance was equally well known. *See* Section VI.B above; James, 2, 4; Morin, 355-56, 367; Hsu823 ¶[0003]; Jung, Abstract, ¶[0090]; Ke ¶[0003]; Bohr683 ¶¶[0038]-[0039], FIG. 6. A POSITA would have understood that Saito's "plasma nitride (SiN)" insulating film 13 describes a CESL. *See* Saito ¶[0072], ¶¶[0080]-[0084], FIGS. 3, 12, 21. In my opinion, a POSITA would have found it obvious to implement Saito's "plasma nitride (SiN)" insulating film 13 as a tensile CESL, consistent with James's disclosures, because it was a very well-known way to improve nFET performance. *See* Sections VI.B and IX.B.1.a above; Jung ¶[0090], ¶¶[0099]-[0100], Tbl. V.

402. When incorporating epitaxial SiGe source/drain stressor layers into Saito's source/drain regions 2c1, a POSITA would have recognized that Saito's oxide layer 10A (magenta in Figure M above) would deposit and remain in the spaces between the facets of the raised epitaxial SiGe source/drain regions (yellow in Figure M above) and sidewalls 70 (orange in Figure M above). *See* Murthy556, 9:11-15, 9:30-35, FIGS. 7-9. This is similar to how oxide layer 10A remains in Saito's recesses 50. *See* Saito, FIGS. 11, 12. I discuss this aspect of the Saito-Fukutome-James combination in greater detail below.

(1) A POSITA would have been motivated to arrive at the claimed invention using the Saito-Fukutome-James combination

(a) Compressive raised SiGe source/drain regions would have been obvious to a POSITA

403. In my opinion, a POSITA would have found it obvious to incorporate Fukutome's raised SiGe source/drain regions into Saito's pFETs (including P2) to improve transistor performance by boosting channel mobility and limiting junction leakage. *See* Sections VI.B and IX.D.1.a (introduction) above.

404. Saito discloses PMOS source/drain regions 2c1 that include source/drain impurity diffused layers SR1/DR1 and source/drain impurity diffused layers SR4/DR4. Saito ¶[0101]; *see also* Saito ¶[0094], ¶[0097], FIGS. 12, 16, 17, 21. As Saito's FIGS. 16 and 17 show, Saito's source/drain diffusion regions SR1 and DR1 are formed before sidewalls 70, using polysilicon wiring "5b" [sic:3c] as an ion implantation mask. *See* Saito ¶[0094], FIG. 16. Source/drain diffusion regions SR4 and DR4 are then formed after sidewalls 70, using both polysilicon wiring 3c and sidewalls 70 as an ion implantation mask. *See* Saito ¶[0097], ¶[0101] ("Then, as shown in FIG. 17, an impurity is introduced into the main front surface of semiconductor substrate 100 which adjoins polysilicon wiring 5b [sic:3c], and impurity diffused layer SR4 and DR4 are formed in it. Hereby, impurity diffused layer 2c1 which consists of impurity diffused layer SR1 and impurity diffused layer SR4 is formed in the main front surface of semiconductor substrate 100 located in

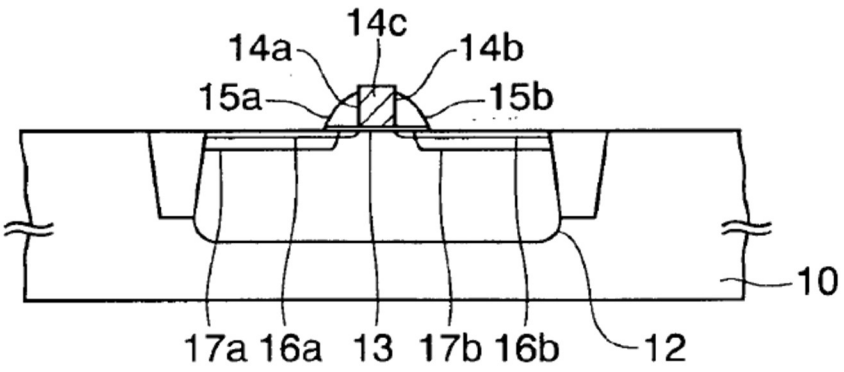
one side surface side of polysilicon wiring 5b [sic:3c]. On the main front surface of semiconductor substrate 100 located in the other side surface side of polysilicon wiring 5b [sic:3c], impurity diffused layer 2c1 which consists of impurity diffused layer DR1 and impurity diffused layer DR4 is formed."), FIG. 17.

405. Saito explains that source/drain regions 2c1 are formed by implanting boron impurities, confirming that the associated transistor P2 is a pFET. *See* Saito ¶[0060] ("P type impurities, such as a boron, are selectively implanted into active regions 2b, 2c formed in [the] N well region, and impurity diffusion region 2b1 and 2c1 are formed."), ¶[0066] ("Second access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c.").

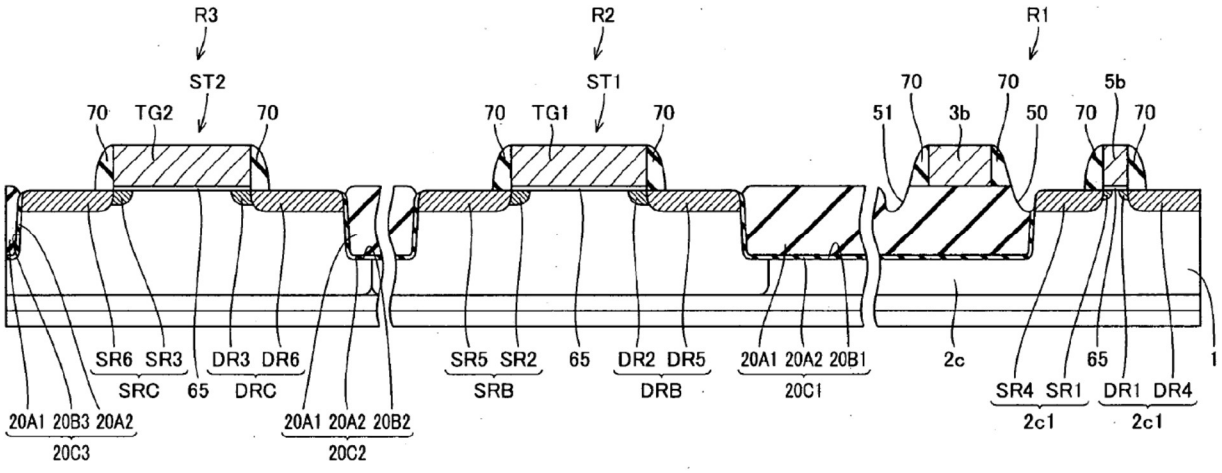
406. A POSITA would have recognized that Fukutome's FIGS. 5B-5E disclose a substantially similar implantation process to Saito's process discussed above. *See* Fukutome ¶[0083], ¶[0087], FIGS. 5B-5C. Like Saito, Fukutome "us[es] the gate electrode 14c as a mask" to implant "boron ions as p-type impurities" to form "first and second source/drain extensions 16a and 16b [that] are shallowly formed in the silicon substrate 10 beside the first and second side surfaces 14a and 14b of the gate electrode 14c." Fukutome ¶[0083]; *see also* Fukutome, FIG. 5B. Fukutome then "us[es] the gate electrode 14c and the first sidewalls 15a and 15b as a mask" to implant "source/drain regions 17a and 17b[,] which are deeper and denser

than the source/drain extensions 16a and 16b," in substrate 10 "beside the gate electrode 14c." Fukutome ¶[0087]; *see also* Fukutome, FIG. 5C. Like Saito, because Fukutome implants "boron ions as p-type impurities," it describes a pFET. *See* Fukutome ¶[0083], ¶[0087].

407. Like Saito's sidewalls 70, Fukutome's sidewalls 15a and 15b on the side of the gate electrodes are made of silicon oxide. *See* Saito ¶[0073], FIG. 17; Fukutome ¶¶[0084]-[0086], FIG. 5C. At this point in the processing, Saito's and Fukutome's FETs have essentially the same structure. *Compare* Saito, FIG. 17, *with* Fukutome, FIG. 5C.

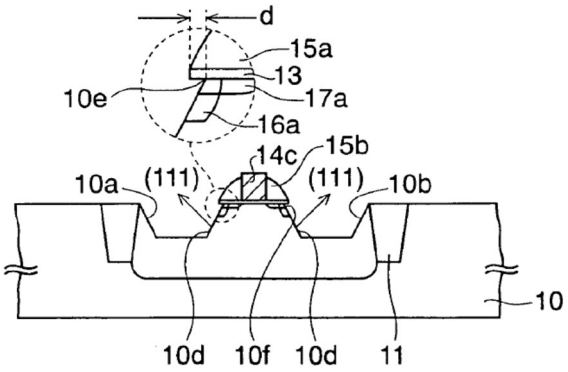


Fukutome's FIG. 5C

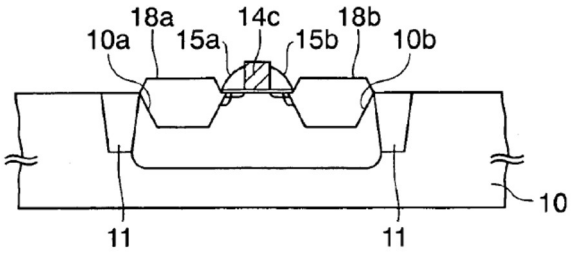


Saito's FIG. 17

408. Fukutome discloses improvements to that structure by etching trenches in the substrate and epitaxially growing SiGe source/drain regions 18a/18b in them. *See* Fukutome ¶¶[0089]-[0102], FIGS. 5D-5E. More specifically, Fukutome teaches to etch recesses (i.e., trenches) 10a and 10b into substrate 10 to expose the (111) silicon planes on side surfaces 10c and 10d of the etched substrate. *See* Fukutome ¶[0092], FIG. 5D.



Fukutome's FIG. 5D



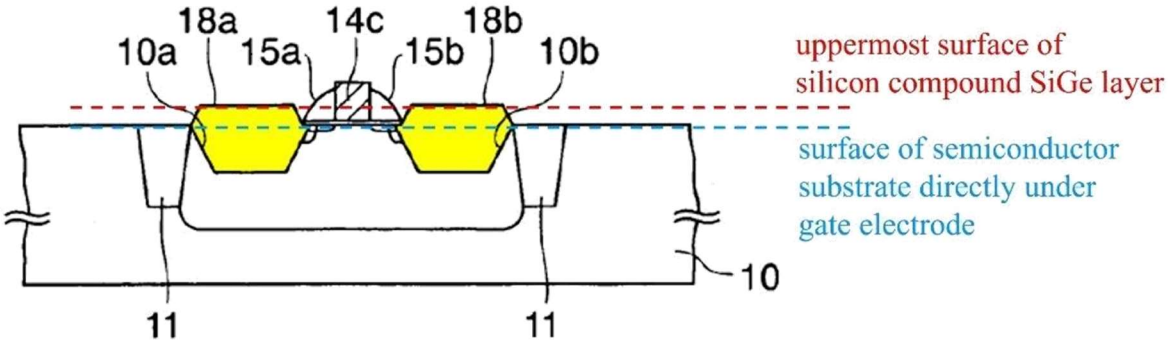
Fukutome's FIG. 5E

409. Fukutome then teaches growing raised SiGe epitaxial layers 18a and 18b.[29] Fukutome ¶¶[0098]-[0102], FIG. 5E. Fukutome explains that "[t]he distances between the bottom surface of the n-well 12 and the upper surfaces of the source/drain material layers 18a and 18b are increased by forming the upper surfaces of the source/drain material layers 18a and 18b at positions higher than the surface

[29] These epitaxial SiGe source/drain regions are doped with boron either "in-situ" (i.e., during growth) or by ion implantation and annealing heat treatment after growth. Fukutome ¶[0102]. A POSITA would have recognized both of these techniques as common and conventional design choices in the prior art. This design choice does not affect my opinion on unpatentability, nor would it change that a POSITA would have found the Saito-Fukutome-James combination obvious.

of the silicon substrate 10." Fukutome ¶[0100]; *see also* Fukutome, FIG. 5E. According to Fukutome, this suppresses source/drain contact junction leakage and improves reliability. Fukutome ¶[0100].

410. In annotated FIG. 5E below, I show the uppermost surface of Fukutome's SiGe source/drain regions 18a and 18b compared to the uppermost surface of substrate 10, which confirms that the SiGe source/drain regions extend above the top surface of the substrate.



Fukutome's FIG. 5E (annotated)

411. Fukutome also explains that epitaxially grown SiGe regions 18a and 18b "introduc[e] strain into a channel" to compressively stress the pFET channel region along the gate length direction "by utilizing a difference in lattice constant between silicon and SiGe." Fukutome ¶[0005]; *see also* Fukutome ¶[0110] ("In the MOS transistor TR, [the] silicon lattice in the silicon substrate 10 is forcefully stretched so as to match the large lattice spacing of SiGe due to a mismatch between the lattice constant of the silicon substrate 10 and those of the source/drain material layers 18a and 18b, and stress in the directions of the arrows in the drawing [is]

applied to a channel under the gate electrode 14c. As a result, compared to the case where stress is not applied, the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved."), ¶[0249]. As I explain above, the lattice mismatch between the SiGe layers and the silicon substrate exerts a compressive stress on the channel region. *See* Section VI.B above. The arrows in Fukutome's FIG. 5G indicate this phenomenon. Fukutome ¶[0110] (explaining that "stress in the directions of the arrows in the drawing [is] applied to a channel under the gate electrode 14c").

412. In my opinion, a POSITA would have found it obvious to incorporate Fukutome's epitaxial SiGe source/drain regions into Saito's pFETs P1 and P2 so that "the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved." Fukutome ¶[0110]. This was a well-known technique in the prior art to improve PMOS carrier (hole) mobility, as I explain in Section VI.B above. As Fukutome teaches, a POSITA also would have found it obvious to incorporate Fukutome's SiGe source/drain regions into Saito's pFETs P1 and P2 to suppress junction leakage and improve reliability. Fukutome ¶[0100].

413. The benefits of using epitaxial SiGe source/drain regions like the ones Fukutome discloses were well known in the art. *See* Section VI.B above; Fukutome ¶[0100], ¶[0110]; Wu ¶[0004]; Wang ¶¶[0004]-[0005]; Bohr683, ¶[0024]; James, 2. Such SiGe source/drain regions had been used in each of the four preceding high-

volume commercial processes to boost pFET performance. *See* Section VI.B above; Thompson2004, 1790-96 (describing Intel's 90nm devices); Bai, 657-58 (describing Intel's 65nm devices); Mistry, 247-50 (describing Intel's 45nm devices); Natarajan, 1 (describing Intel's 32nm devices).

414. James, for example, notes that "epitaxial SiGe source/drains . . . create compressive stress" and "improve[] hole mobility [in PMOS transistors] by as much as 50%." James, 2. James also explains that the "[c]rystalline [SiGe] facets form raised source/drains," like those shown in Fukutome's FIGS. 5E-5G, and that these facets "reduc[e] series resistance" and "counteract[]" "tensile stress from . . . nitride [etch stop] layer[s]," which also helps improve pFET performance. James, 2; *see also* Fukutome, FIGS. 5E-5G; Section VI.B above.

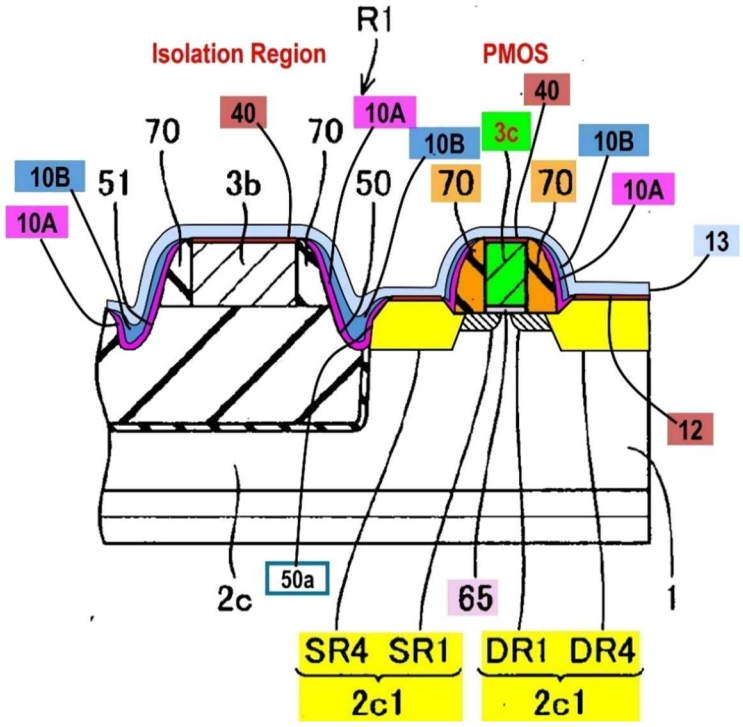


Figure M

415. Composite Figure M above illustrates an intermediate structure[30] for the combination of Saito with Fukutome's faceted SiGe source/drain regions.[31] A POSITA would have been motivated to incorporate Fukutome's epitaxial SiGe source/drain regions into Saito's pFETs P1 and P2 to improve carrier (hole) mobility and reduce source/drain resistance, thereby improving performance. *See* Fukutome ¶[0110]; James, 2; Section VI.B above.

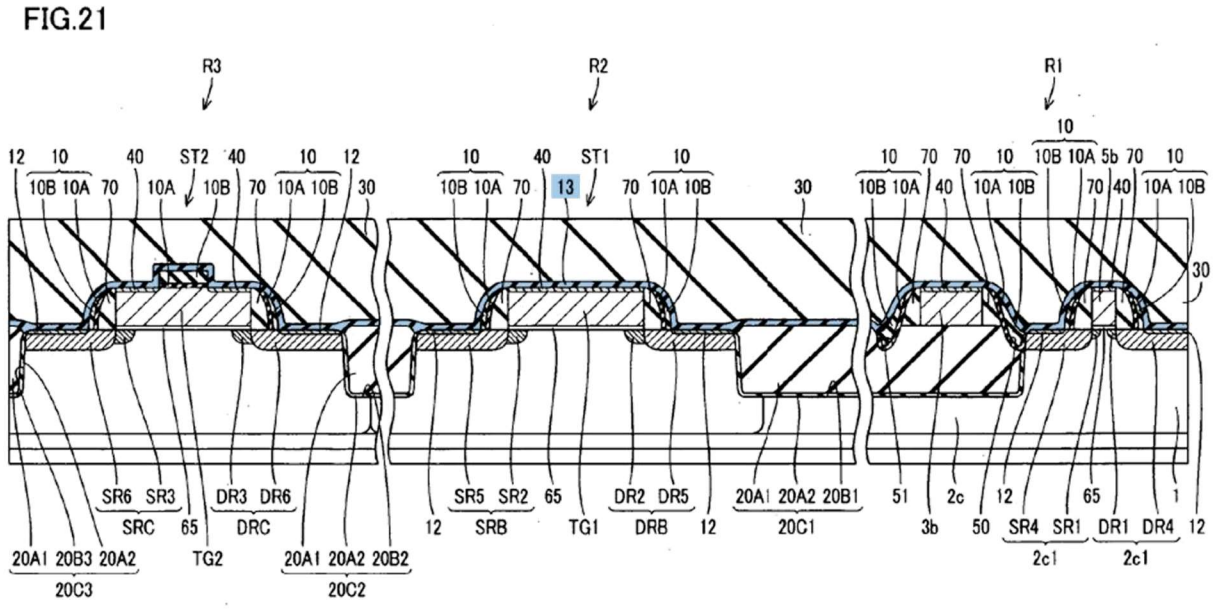
(b) Implementing Saito's SiN layer 13 with tensile strain would have been obvious

416. In my opinion, a POSITA further would also have been motivated to make Saito's SiN layer 13 tensile to improve carrier (electron) mobility in Saito's nFETs. *See* Sections VI.B and IX.D.1.a (introduction) above.

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[30] This illustration is intermediate because, after incorporating Fukutome's epitaxial SiGe source/drain regions 18a and 18b into Saito's source/drain regions 2c1, the process flow for the Saito-Fukutome-James combination continues as disclosed in Saito.

[31] In Figure M, I assume—as Fukutome discloses—that the epitaxial SiGe layers are doped in-situ with boron, eliminating the need to form Saito's diffusion regions SR4 and DR4. *See* Fukutome ¶[0102] ("In the case where in-situ doping is performed when the source/drain regions 17a and 17b are formed, impurity implantation and heat treatment may be omitted."). Alternatively, the SiGe layers may be doped by ion implantation. *See* Fukutome ¶[0101] ("[T]he source/drain material layers 18a and 18b are formed after the source/drain regions 17a and 17b have been formed. However, the order of formation of these is not particularly limited. The source/drain regions 17a and 17b may be formed after the source/drain material layers 18a and 18b have been formed."). A POSITA would have understood that both approaches are equally viable design choices. This choice does not affect my analysis in any material way.



Saito's FIG. 21 (annotated)

417. A POSITA would have understood that Saito's "plasma nitride (SiN)" "insulating film 13" is a CESL that blankets Saito's entire SRAM cell, including transistors N1-N4 and P1-P2, polysilicon wirings 3b and 3c, etc. Saito ¶[0080]; *see also* Saito, FIGS. 1, 12, 21.[32] For example, Saito explains that FIG. 12 shows "well region[s] of various conductivity types." Saito ¶[0091]. As FIG. 21 shows above, insulating film 13 blankets all of those "well region[s] of various conductivity types." Saito ¶[0091]; *see also* Saito, FIGS. 12, 21. For example, Saito explains that "interlayer insulation film 30 is provided with insulating film 13," both being formed over "polysilicon wiring 3b." Saito ¶[0080]. A POSITA would have recognized that

[32] FIGS. 12 and 21 show similar cross-sections. *See* Saito ¶¶[0030]-[0048] (describing same embodiment for FIGS. 3-21), ¶[0049], ¶¶[0084]-[0085] (same). While I may sometimes specifically discuss either FIG. 12 or FIG. 21, my discussion applies to both figures.

both insulating film 13 and insulation layer 30 would therefore cover the various regions of the SRAM device because polysilicon wiring 3b (and analogous polysilicon wiring 3a) do as well.

418. Before depositing insulating film 13, the source/drain regions are formed, and insulating films 10A and 10B are deposited and patterned. *See* Saito ¶¶[0091]-[0092], ¶[0101], ¶[0104], FIGS. 5-6, 15-18. Insulating films 10A and 10B are then etched to expose the top surfaces of the polysilicon wirings, leaving remnants of films 10A and 10B on sidewalls and in recesses. Saito ¶[0107], FIGS. 7, 19. The polysilicon wirings are then silicided. Saito ¶¶[0077]-[0081], ¶[0084], ¶[0114] ("[B]y etching into insulating film 10A, lamination insulating film 10 which consists of insulating film 10A and insulating film 10B is formed over the upper surface of sidewall 70 from the boundary region of the upper surface and the side surface of active region 2c, and it fills up with it in recess 50."), ¶¶[0116]-[0117], FIGS. 8, 20. A thin silicide film 12 forms on the upper surfaces of the source/drain regions and the upper surfaces of the gate electrodes. Saito ¶¶[0077]-[0079], ¶¶[0117]-[0119], FIGS. 8, 20. After silicidation, Saito's insulating film 13 is deposited over the entire SRAM cell, as FIG. 21 shows above. *See* Saito ¶[0080], ¶[0091], ¶[0120], ¶[0124] (explaining that all polysilicon wirings "are formed similarly"), FIGS. 12, 21.

419. Saito is silent as to whether insulating SiN layer 13 imparts a tensile or compressive strain. In my opinion, James would have motivated a POSITA to make Saito's SiN insulating layer 13 tensile because James explains that a tensile CESL improves nFET performance. *See* James, 2 (explaining that "[l]ocalized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer," and that "[t]his increases electron mobility by ~10%").

420. James further explains that using a tensile CESL to apply strain "involves no extra cost for either capital equipment or special substrates." James, 5 ("It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown) . . . . This technique has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates."); *see also* Section VI.B above. In other words, a POSITA would have recognized that making Saito's SiN insulating film 13 tensile would have improved nFET performance in a very cost-effective way.

421. A POSITA, therefore, would have been motivated to impart a tensile strain using Saito's insulating SiN film 13 to improve performance in nFETs N1-N4, recognizing that pFETs P1 and P2 would be similarly improved by incorporating

Fukutome's epitaxial SiGe source/drain regions. *See* Sections VI.B and IX.D.1.a(1)(a) above.

422. It was well known in the art that applying compressive or tensile stress-inducing films could improve carrier mobility and performance. *See* Section VI.B above; James, 2, 4; Morin, 355-56, 367; Hsu823 ¶[0003], ¶¶[0037]-[0038]; Jung, Abstract, ¶¶[0099]-[0100], Tbls. IV, V. For example, a contact etch stop layer ("CESL") made of silicon nitride, if prepared under certain conditions, may be "used . . . for applying stress to [a] channel region" to improve carrier mobility. Hsu823 ¶[0003]; *see also* Jung ¶[0090], ¶¶[0099]-[0100], Tbl. V; Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Morin, 355-56; Bohr683 ¶¶[0038]-[0039], FIG. 6. For example, Morin explains that it "is important to work to improve the nMOS transistors since other solutions" like epitaxial SiGe "can enhance the pMOS performances." Morin, 355-56.

423. Thus, in my opinion, a POSITA would have been motivated to use tensile SiN as Saito's SiN layer 13 to improve nFET carrier (electron) mobility in a simple and inexpensive manner. *See* Morin, 355-56; James, 2, 5; Hsu823 ¶[0039] (preferable to apply tensile CESL across both NMOS and PMOS devices because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Alvarez

¶[0033], ¶[0047], ¶[0049], ¶[0054], ¶[0065], Tbl. 1, FIG. 9 (explaining that a single tensile CESL layer avoids "additional lithography and etch step[s] . . . , which [are] costly and time-consuming"); Ke ¶[0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Bohr683 ¶¶[0038]-[0039], FIG. 6.

424. A POSITA also would have understood that the tensile stress from Saito's SiN layer 13 in PMOS regions would be mitigated by the presence of a buffer layer and the compressive SiGe source/drain layers. *See* Sections VI.C and IX.B.1.a (describing benefits of Alvarez's stress-controlling layer); James, 2; Alvarez ¶[0047], ¶[0049], ¶[0054], ¶[0065], Tbl. 1, FIG. 9; Murthy556, 9:27-29; Doris ¶[0005]; Lee ¶[0067], FIG. 5; Cheng810 ¶[0030], Fig. 1F; Bohr683 ¶¶[0038]-[0039], FIG. 6; Baik ¶[0037]; Hsu823 ¶[0039]; Morin, 355-56. For example, a POSITA would have recognized that the presence of Saito's intermediate oxide layer 10A would have mitigated the tensile stress on the pFETs by acting like Alvarez's stress-controlling layer discussed above. *See* Sections VI.C and IX.B.1.a above.

425. In my opinion, a POSITA thus would have been motivated to use a tensile SiN layer 13 to improve nFET performance in a cost-effective way, as discussed above.

(2) A POSITA would have reasonably expected to succeed in realizing the Saito-Fukutome-James combination

426. A POSITA would have reasonably expected to succeed with incorporating epitaxial SiGe source/drain regions into Saito's PMOS source/drain regions (as Fukutome discloses) while also making Saito's SiN insulating film 13 tensile (as James discloses). *See* Section IX.D.1.a(1) above.

427. Incorporating epitaxial SiGe source/drain regions like those Fukutome discloses was conventional. It had already been used in each of the previous four generations of high-volume commercial devices (*see* Section VI.B above) and would have required nothing more than following the conventional steps of etching trenches into the silicon substrate and filling them by growing epitaxial SiGe source/drain layers, as I explain above. *See* Section IX.D.1.a(1)(a) above; *compare* Saito ¶¶[0092]-[0103], FIGS. 16-17, *with* Fukutome ¶¶[0085]-[0102], FIGS. 5C-5E. Once those faceted and raised SiGe layers have been epitaxially grown (as Fukutome discloses), Saito's fabrication process would continue as described by forming layers 10A and 10B and eventually depositing insulating SiN film 13 as a tensile film (as James discloses). *See* Saito ¶¶[0104]-[0106], FIG. 18; James, 2; Section VI.B above.

428. A POSITA would have recognized that incorporating epitaxial SiGe source/drain regions (like the ones Fukutome discloses) into Saito's PMOS transistors P1 and P2 would have achieved the ordinary and expected result of

providing compressive strain to those pFETs to boost carrier (hole) mobility and improve performance. *See* Section VI.B above; James, 2. Accordingly, the Saito-Fukutome-James combination, including the exemplary embodiment shown in Figure M below, represents the application of known processes to achieve ordinary and expected results.

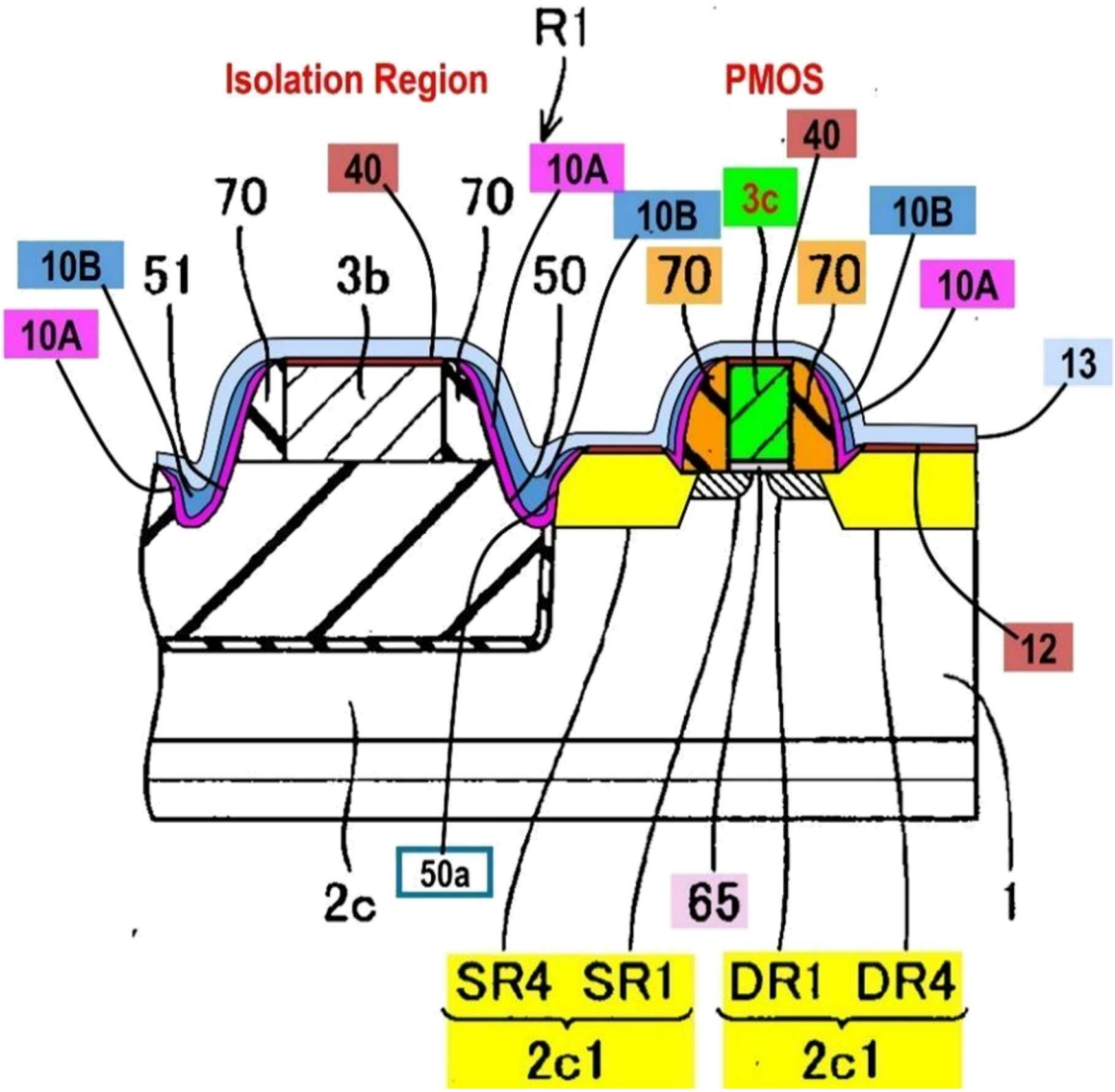


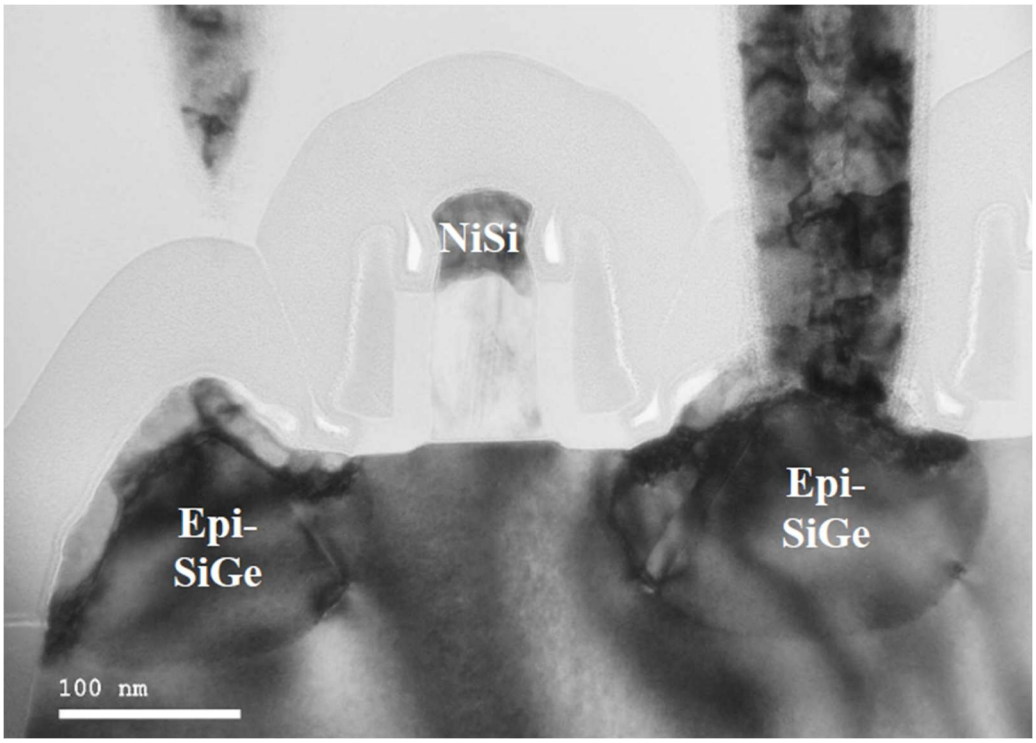
Figure M

429. Additionally, a POSITA also would have reasonably expected to succeed in depositing Saito's SiN insulating layer 13 as a tensile layer. *See* James, 2, 5. A POSITA would have known and recognized that this would have required nothing more than the conventional steps of depositing Saito's SiN insulating layer 13 under conditions known to form a tensile layer. *See* Jung ¶[0090], ¶¶[0099]-[0100], Tbl. V; Saito ¶[0080], ¶¶[0120]-[0121], FIGS. 12, 18; James, 2, 5 ("It is perhaps ironic that stress in silicon nitride layers, a problem in previous process generations, has now been harnessed to apply strain. So far, it has been used only to provide tensile stress to enhance NMOS performance (at least in the three examples we have shown) . . . ."); Alvarez ¶[0054], ¶[0065], ¶[0069], Tbl. 1 (stress-insulating material 216 imparts tensile stress); Hsu823 ¶[0039] (preferable to apply a tensile insulating layer across both NMOS and PMOS devices because "the performance of PMOS devices can be easily improved with SiGe stressors, while the performance of NMOS devices is relatively difficult to improve"); Morin, 355-56; Bohr683 ¶¶[0038]-[0039], FIG. 6. Indeed, James acknowledges that the tensile CESL, in addition to being used successfully in commercial devices, also "has the noteworthy convenience that it can be accomplished by process tuning, and involves no extra cost for either capital equipment or special substrates." James, 5.

430. Thus, in my opinion, a POSITA would have recognized that depositing Saito's silicon nitride insulating layer 13 as a tensile layer (as James discloses) would

have achieved the ordinary and expected result of boosting carrier (electron) mobility and improve performance in Saito's NMOS transistors N1-N4. James, 2; *see also* Section VI.B above. Therefore, the Saito-Fukutome-James combination represents nothing more than the application of known processes to achieve ordinary and expected results.

431. James further confirms that a POSITA would have reasonably expected to succeed with incorporating raised, faceted epitaxial SiGe source/drain regions into Saito's pFETs while, at the same time, also making Saito's SiN insulating film 13 tensile. Intel's high-volume 90nm process (codenamed Prescott) put both features together simultaneously in countless commercial products. James's Fig. 6 below shows a micrograph of such a prior-art pFET.



James's Fig. 6

432. Predictably, this approach improved both nFETs and pFETs. *See* James, 2-3 ("Localized tensile stress is applied to the channels of NMOS devices by a highly stressed nitride sealant layer . . . . This increases electron mobility by ~10%. . . . . The PMOS transistors (Figure 6) use epitaxial SiGe source/drains to create compressive stress – this improves hole mobility by as much as 50%. . . . Crystalline facets form raised [SiGe] source/drains, reducing the series resistance. The tensile stress from the nitride layer is counteracted by the compressive effect."); *see* Section VI.B above. Such known commercial use before the '425 Patent confirms that a POSITA also would have reasonably expected this to work when applied to Saito's MISFETs N1-N4 and P1-P2.

433. To summarize, it is my opinion that a POSITA would have found the Saito-Fukutome-James combination obvious because it is an example of the following:

- It combines known prior art elements (Saito's SRAM cell with epitaxial SiGe source/drain regions, as Fukutome and James both disclose, and a tensile silicon nitride CESL, as James discloses) according to known methods (known epitaxial SiGe growth and tensile SiN deposition techniques) to yield predictable results (SiGe source/drain regions that impart compressive stress to pFET

channels and a silicon nitride layer that imparts tensile stress to nFET channels).

- It simply substitutes one known element for another (e.g., substituting Fukutome's epitaxial SiGe source/drain regions for Saito's non-epitaxial deep source/drain regions, and substituting James's tensile SiN CESL for Saito's silicon nitride insulating layer 13) to obtain predictable results (SiGe source/drain regions that impart compressive stress to pFET channels and a silicon nitride layer that imparts tensile stress to nFET channels).
- It uses known techniques (epitaxial growth of SiGe source/drain regions, as Fukutome and James disclose, and a tensile silicon nitride CESL, as James discloses) to improve similar devices (the MISFETs in Saito's SRAM cell) in the same way (e.g., by using strain engineering to boost carrier mobility in Saito's pFETs and nFETs).
- It applies known techniques (epitaxial growth of SiGe source/drain regions, as Fukutome and James disclose, and a tensile silicon nitride CESL, as James discloses) to a known device ready for improvement (the MISFETs in Saito's SRAM cell) to yield

predictable results (improved carrier mobility in Saito's pFETs and nFETs).

- It applies a known teaching, motivation, or suggestion in the prior art (e.g., using epitaxial SiGe source/drain regions to improve pFET performance, as Fukutome and James teach, and a tensile SiN CESL, as James teaches, to improve nFET performance) that would have led a POSITA to modify Saito according to, or to combine Saito with, the teachings of Fukutome and James to arrive at the claimed invention.

b. Independent Claim 1

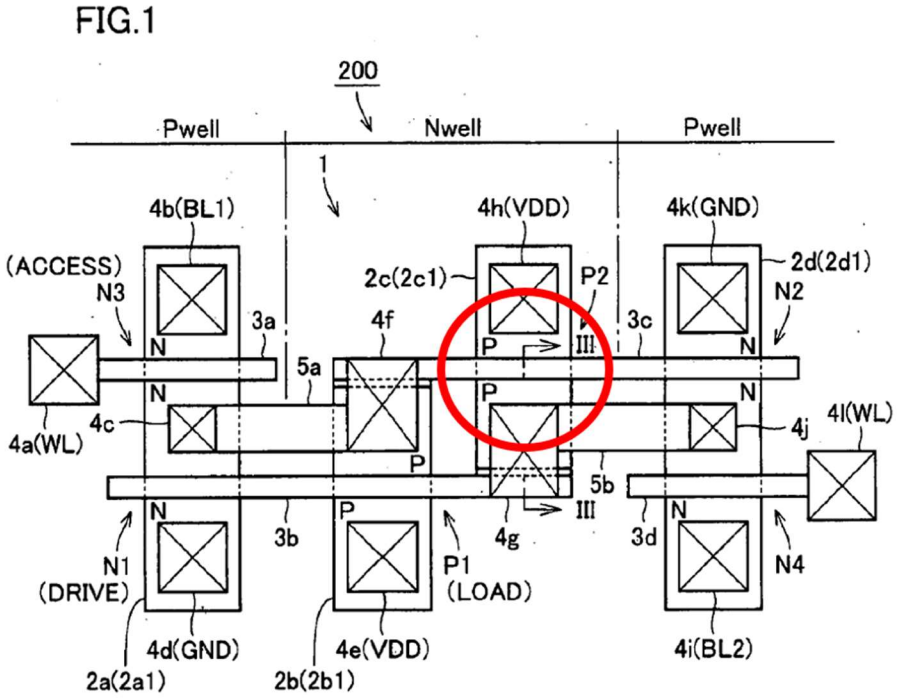
(1) [1Pre]: "A semiconductor device"

434. Saito describes "a semiconductor device and its manufacturing method." Saito ¶[0002], ¶¶[0023]-[0026], FIGS. 1, 12, 21. As I explain above, Saito's "FIG. 1 is a plan view of the memory cell of the semiconductor device (static semiconductor memory device)." Saito ¶[0028]; *see also* Saito ¶[0049] ("FIG. 1 is the plan view of memory cell 1 of [the] full CMOSSRAM" memory device), FIG. 1. Saito's FIGS. 12 and 21 are "cross-sectional view[s]" of the "semiconductor device." Saito ¶[0039], ¶[0048]; *see also* Saito, FIGS. 12, 21.

(2) [1A]: "a first MIS transistor . . . includ[ing]:"

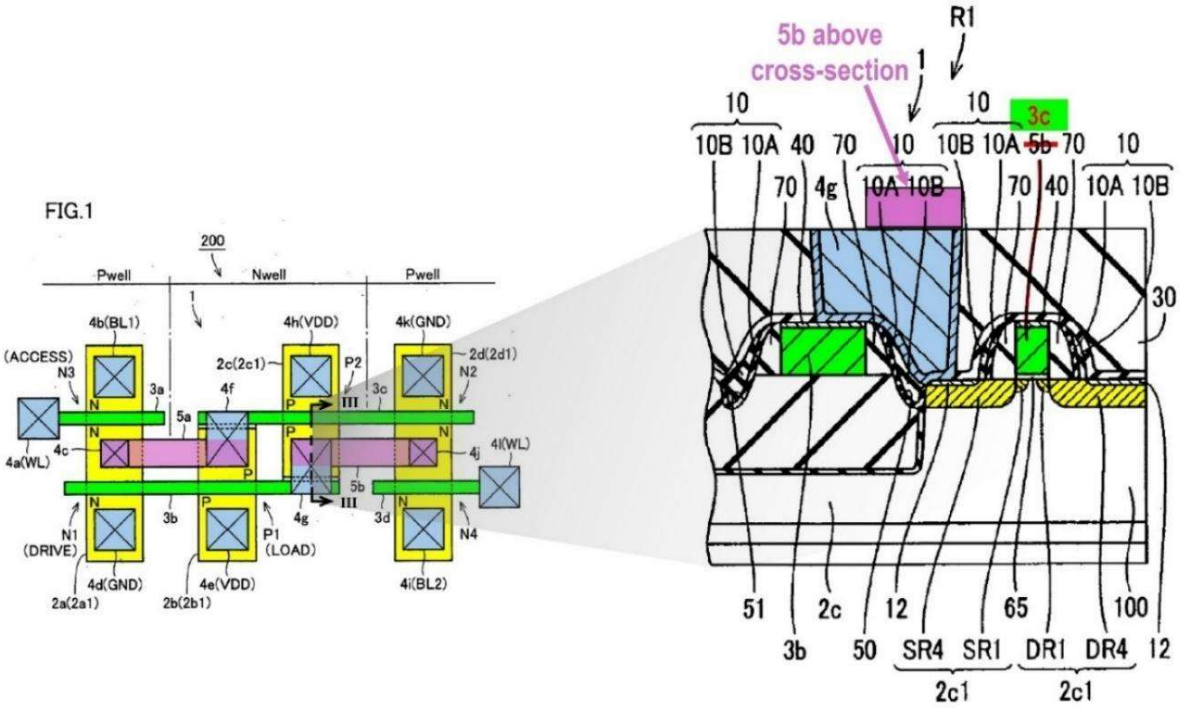
435. Saito discloses a first MIS transistor, such as PMOS transistor P2 in active region 2c. *See* Saito ¶[0057], FIGS. 1, 3, 12, 21.

436. Saito explains that "[s]econd access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito ¶[0066]. PMOS transistor P2 is identified below in annotated FIG. 1.



Saito's FIG. 1 (annotated)

437. As I explain in Section IX.D.1 above, a POSITA would have recognized that Saito includes a clerical error in which polysilicon wiring 3c is misidentified as polysilicon wiring "5b" in the context of FIGS. 12-21. I provide annotated FIGS. 1 and 12 below to correct this error. *See* Section IX.D.1 above.



Saito's FIG. 1 **Saito's FIG. 12 (excerpted, annotated)**

438. As I explain above in Section IX.D.1.a and in further detail for elements [1B]-[1J], a POSITA would have found the Saito-Fukutome-James combination obvious, including as shown in the embodiment of Figure M below.

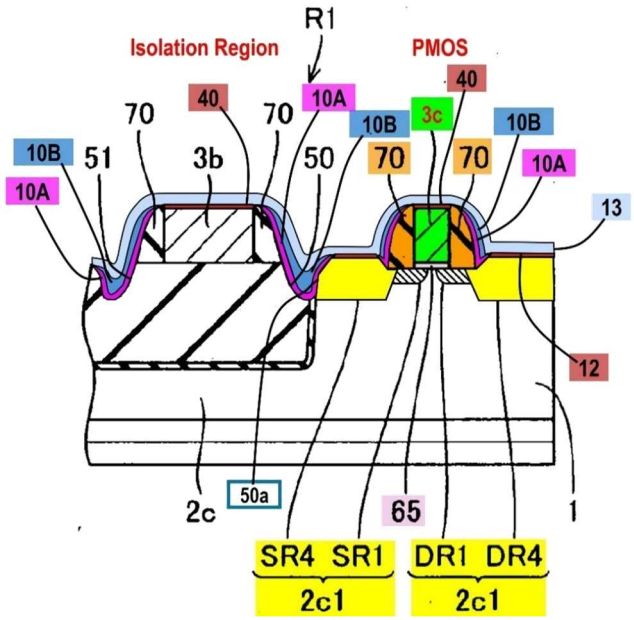


Figure M

(3) [1B]: "a first gate insulating film formed on a first active region in a semiconductor substrate"

439. Saito discloses a "gate insulating film 65" formed on "active region 2c" of a "semiconductor substrate 100." Saito ¶[0051] ("[O]n the main front surface of semiconductor substrate 100 in which active region 2c is located, gate insulating film 65 . . . [is] formed."); *see also* Saito, FIG. 21. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, gate insulating film 65 (light purple) is formed on first active region 2c of PMOS transistor P2. *See* Section IX.D.1.a above.

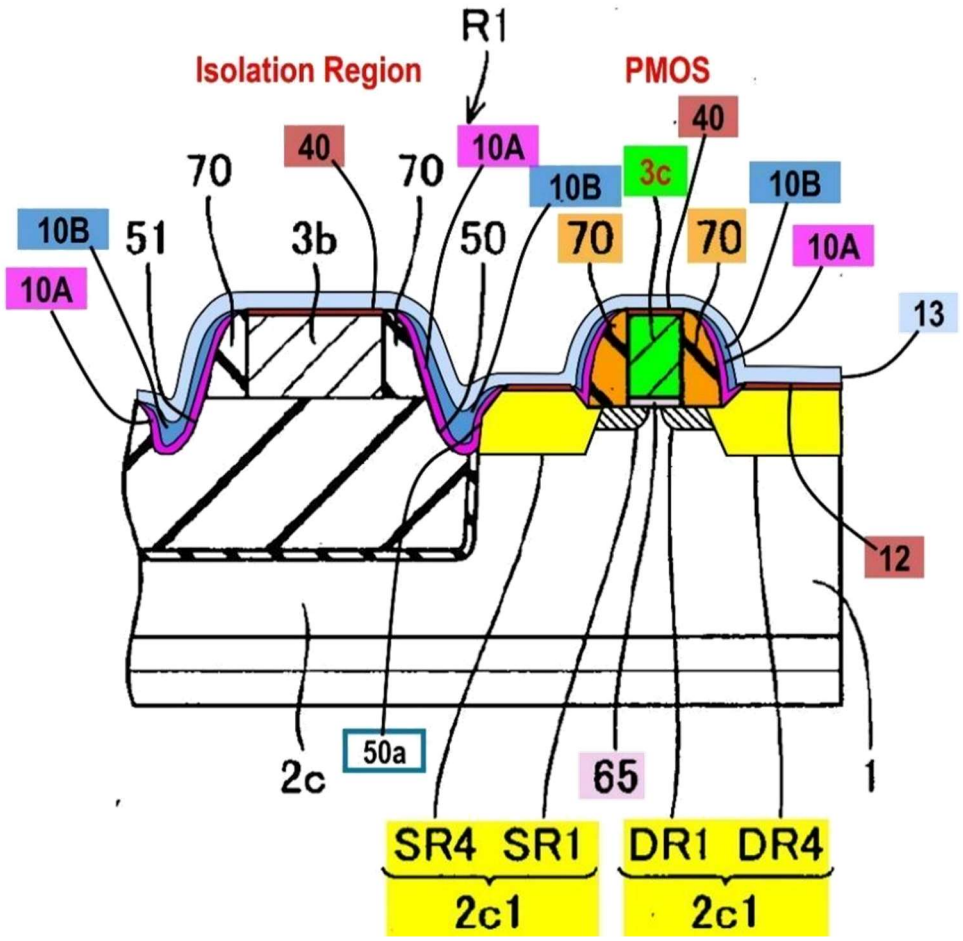


Figure M

(4) [1C]: "a first gate electrode formed on the first gate insulating film"

440. Saito discloses an "active region 2c" comprising "gate insulating film 65" and "polysilicon wiring 5b [sic:3c] formed on the upper surface of this gate insulating film 65, and impurity diffused layer 2c1 located in the both sides [sic] of this polysilicon wiring 5b." Saito ¶[0051]; *see also* Saito, FIG. 12. Saito further explains that the "[s]econd access PMOS transistor P2 is formed in the intersection part of impurity diffusion region 2c1 comprising the region used as a source/drain, and polysilicon wiring 3c." Saito ¶[0066]; *see also* Saito ¶[0124], FIGS. 1, 12.

441. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, polysilicon wiring 3c (green) is formed on gate insulating film 65 (light purple). *See* Section IX.D.1.a above.

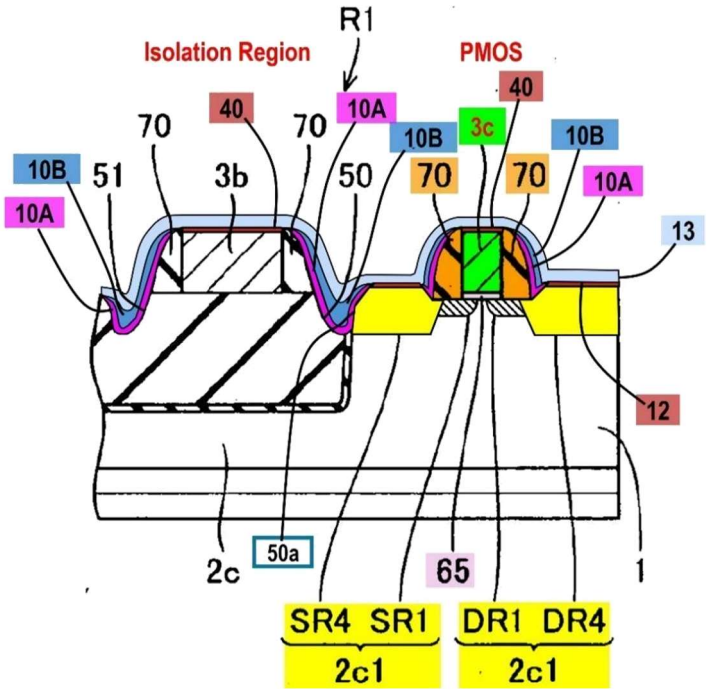


Figure M

(5) [1D]: "a first sidewall spacer formed on a side surface of the first gate electrode"

442. Saito discloses a "sidewall 70 [that] is formed on the both [sic] side surfaces of . . . polysilicon wiring 5b [sic:3c], and polysilicon wiring 3b." Saito ¶[0096]; *see also* Saito, FIG. 17. Saito explains that "[t]he sidewall [70] is formed also on the side surface of th[e] polysilicon wiring 3c," which further confirms my opinion that a POSITA would have understood that FIGS. 12-21 show polysilicon wiring 3c. Saito ¶[0077]; *see also* Saito ¶[0124]; Section IX.D.1 above.

443. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, first sidewall spacer 70 (orange) is formed on the side surfaces of the first gate electrode 3c (green). *See* Section IX.D.1.a above.

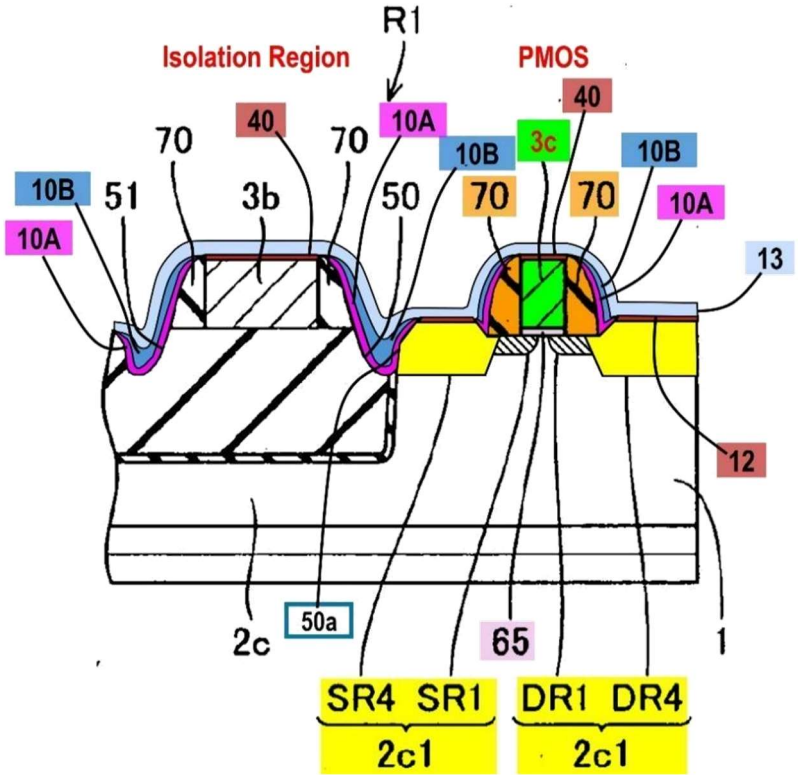


Figure M

(6) [1E]: "a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region"

444. The pFETs in the Saito-Fukutome-James combination include raised, faceted epitaxial SiGe source/drain layers like the ones Fukutome discloses. *See* Section IX.D.1.a(1)(a) above. Fukutome explains that "a SiGe layer with a Ge concentration of 3 to 30% is selectively epitaxially grown in each of the recesses [trenches] 10a and 10b." Fukutome ¶[0098]; *see also* Fukutome ¶[0005], ¶[0110]. Figure M below shows one embodiment of the Saito-Fukutome-James combination, including the incorporation of epitaxial SiGe layers (yellow) into Saito's pFETs. *See* Section IX.D.1.a above.

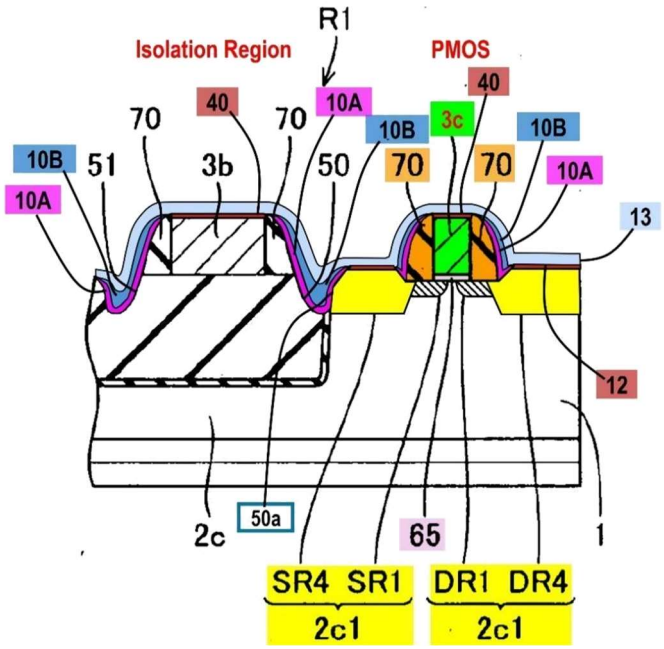


Figure M

445. Fukutome teaches that such epitaxial SiGe layers apply compressive stress along the gate length direction in the channel region because the lattice spacing in the SiGe layers is larger than the lattice spacing in the silicon substrate. Fukutome ¶[0005], ¶[0110] ("In the MOS transistor TR, [the] silicon lattice in the silicon substrate 10 is forcefully stretched so as to match the large lattice spacing of SiGe due to a mismatch between the lattice constant of the silicon substrate 10 and those of the source/drain material layers 18a and 18b, and stress in the directions of the arrows in the drawing [is] applied to a channel under the gate electrode 14c. As a result, compared to the case where stress is not applied, the mobility of carriers in the channel is improved, and the drive capability of the MOS transistor can be improved."). Fukutome's FIG. 5G shows that this stress is compressive in the channel region, as the stress direction arrows indicate.

446. Fukutome's raised SiGe source/drains have p-type conductivity, like Saito's PMOS source/drain regions in PMOS transistors P1 and P2. *See* Section IX.D.1.a above; Fukutome ¶[0102] ("[B]oron ions are implanted as p-type impurities into the source/drain material layers 18a and 18b . . . . In the case where in-situ doping is performed . . . , impurity implantation and heat treatment may be omitted."); Saito ¶[0060] ("P type impurities, such as a boron, are selectively implanted into active regions 2b, 2c . . . .").

447. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, the SiGe silicon compound layer (yellow) forms source/drain regions in a trench provided in first active region 2c on a lateral side of the first sidewall spacer 70 (orange) to compressively stress transistor P2 in a gate length direction of the channel region. *See* Section IX.D.1.a above; Fukutome ¶¶[0089]-[0102], FIGS. 5D-5G.

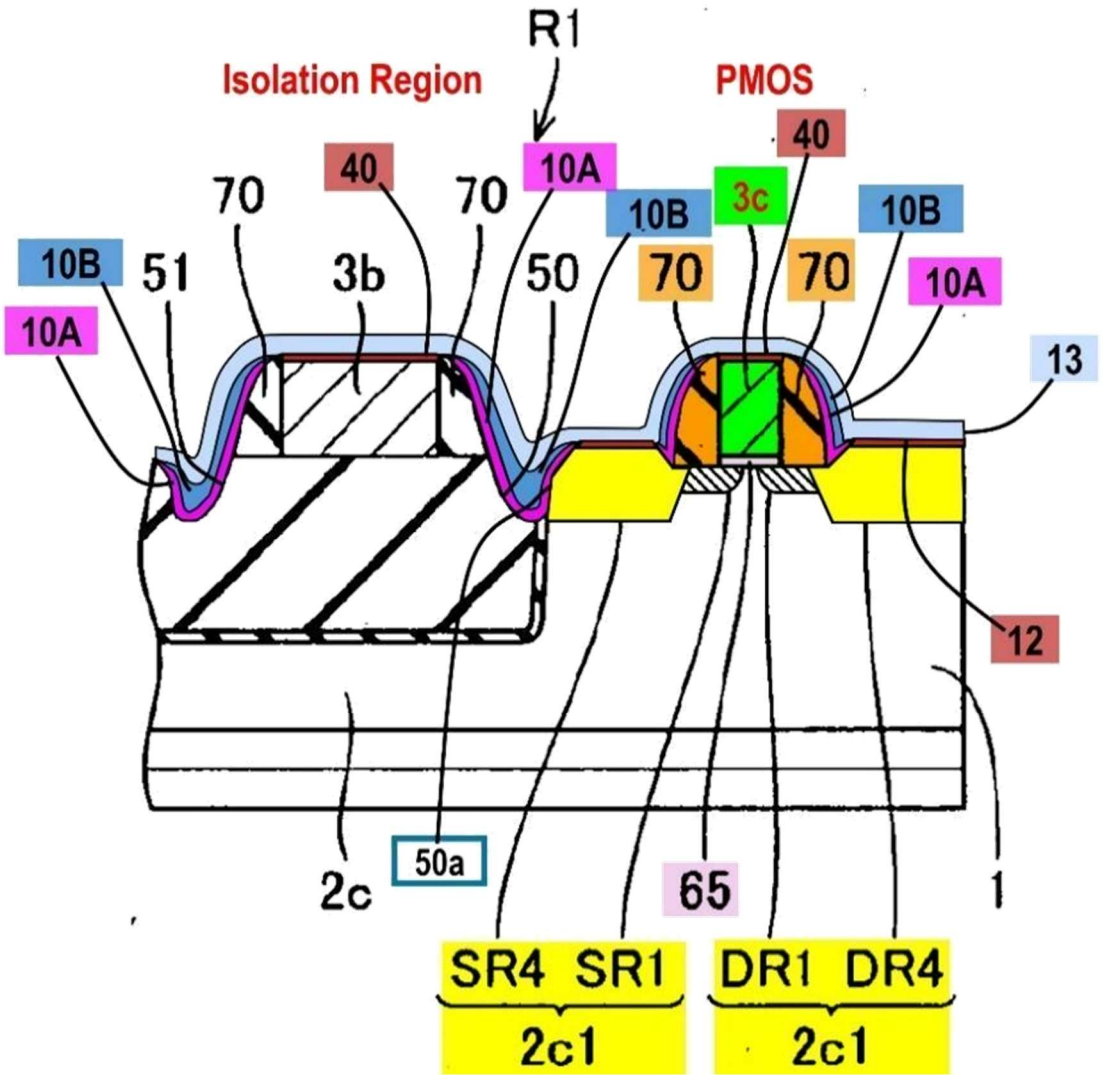


Figure M

(7) [1F]: "a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress"

448. In Saito's final step, shown in FIG. 21, an "insulating film 13" that "consists of a plasma nitride (SiN)" is deposited over the entire SRAM cell. *See* Section IX.D.1.a(1)(b) above; Saito ¶[0080], ¶[0091], ¶[0120], ¶[0124], FIGS. 12, 21.

449. James demonstrates that implementing Saito's insulating film 13 as a tensile film would have been obvious. *See* Section IX.D.1.a above. A POSITA would have understood that doing so would "increase[] electron mobility" in NMOS transistors N1-N4, for example, with "no extra cost for either capital equipment or special substrates." James, 2, 5; *see also* James, Fig. 6. The tensile stress of insulating film 13 in the Saito-Fukutome-James combination is opposite the compressive stress supplied by the epitaxial SiGe source/drain layers.

450. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, tensile stress insulating film 13 (light blue) is formed on first active region 2c such that it covers the first gate electrode 3c (green), the first sidewall spacer 70 (orange), and the first source/drain region (epitaxial SiGe layers, yellow). *See* Section IX.D.1.a above.

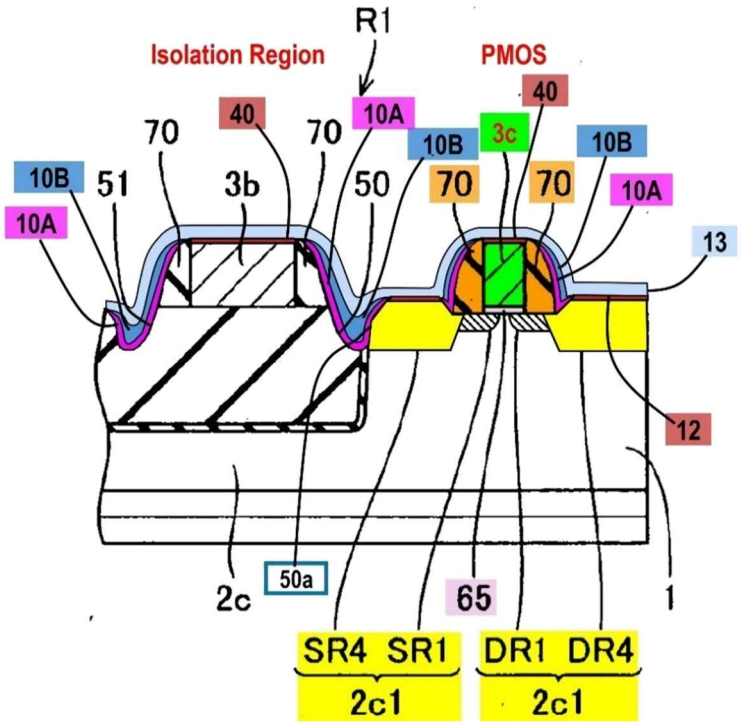
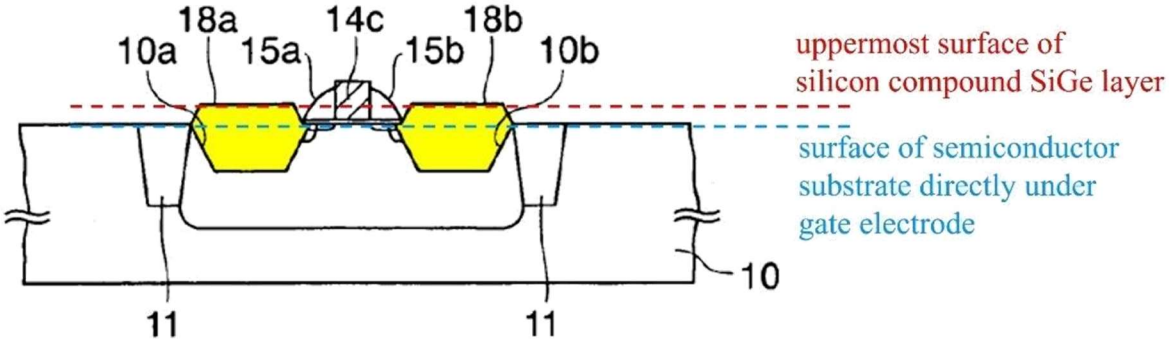


Figure M

(8) [1G]: "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode"

451. Fukutome teaches growing the epitaxial SiGe source/drain layers to a height extending above the substrate surface, as annotated FIG. 5E shows below. *See* Sections IX.D.1.a and IX.D.1.b(6) above.



Fukutome's FIG. 5E (annotated)

452. Fukutome teaches that "the distances between the bottom surface of the n-well 12 and the upper surfaces of the source/drain material layers 18a and 18b are increased by forming the upper surfaces of the source/drain material layers 18a and 18b at positions higher than the surface of the silicon substrate 10 as in the present embodiment." Fukutome ¶[0100]; *see also* Fukutome, FIG. 5E. These raised SiGe layers ensure strain transfer to the pFET channel region and suppress source/drain junction leakage. *See* Fukutome ¶[0100], FIG. 5E; Sections VI.B and IX.D.1.a above.

453. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, the uppermost surface (red line) of the SiGe silicon compound layers (yellow) are located higher than a surface of the semiconductor substrate (blue line) located directly under the first gate electrode 3c (green), just as Fukutome describes.[33] *See* Section IX.D.1.a above.

[33] Fukutome discloses that the uppermost surface of the epitaxial SiGe layer remains higher than the substrate surface even after silicide 12 is formed. *See* Fukutome FIG. 5F; Section IX.D.1.a above.

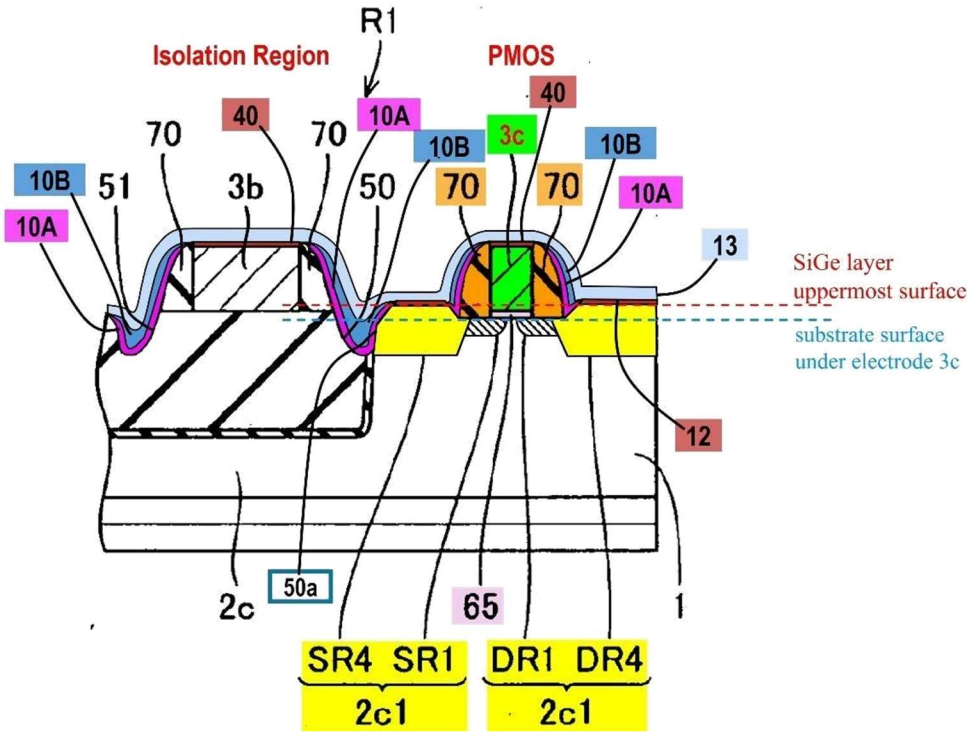
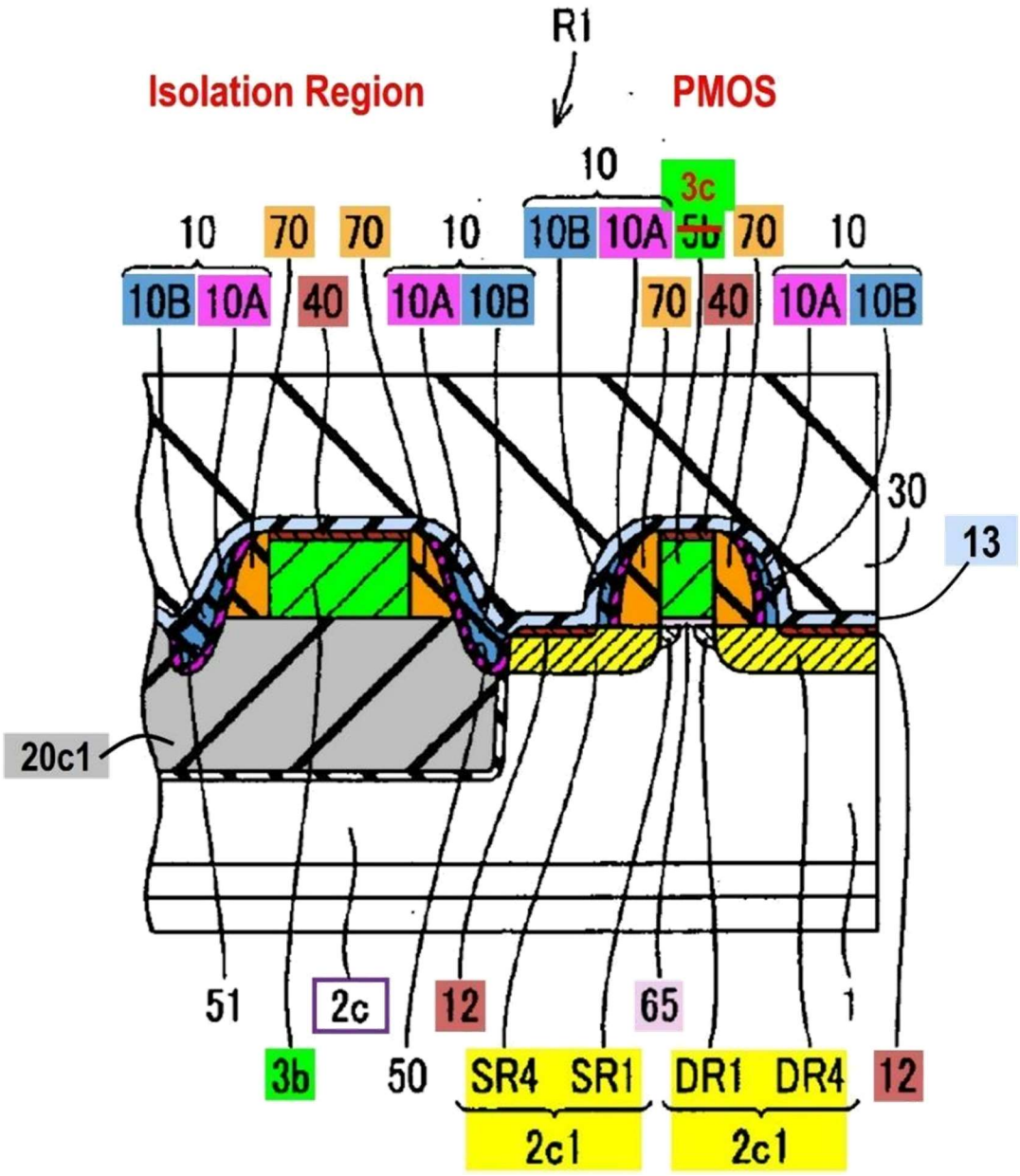


Figure M (further annotated)

(9) [1H]: "a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer"

454. Saito discloses that, before depositing the tensile CESL film 13 (*see* Section IX.D.1.b(7) ([1F]) above), an insulating film 10A is formed over the semiconductor device surface, including in the recesses 50/51 of Saito's isolation region 20c1. Saito ¶[0074], ¶[0078], ¶[0082], ¶[0104], ¶[0107], ¶[0113], FIGS. 6-12, 18-21. Saito teaches and shows that, after etching to expose the gate electrode and source/drain regions for silicidation, first insulating film 10A (magenta below) remains in the recesses 50/51 and on the edges of sidewalls 70 (orange below). *See* Saito ¶[0074], ¶[0078], ¶[0082], ¶[0104], ¶[0107], ¶[0113], FIGS. 7-12, 18-21.



Saito's FIG. 21 (excerpted, annotated)

455. Saito teaches that "insulating film 10A . . . consists of a silicon oxide film etc. . . . formed so that the front surface of this recess 50 may be covered" and "formed on the side surface of sidewall 70." Saito ¶[0074]; *see also* Saito, ¶[0076], FIG. 18. Insulating film 10A covers "the internal surfaces of recess 50, the front surface of impurity diffused layer 2c1, and active region 2c located under impurity

diffused layer 2c1." Saito ¶[0076]; *see* Saito ¶[0078], ¶[0082], ¶[0104], FIGS. 6-12, 18-21. As Saito's FIGS. 19-21 show, insulating film 10A remains in recesses 50/51 and on gate sidewalls 70 even after being etched to expose the top surfaces of the source/drain regions and gate electrodes for silicidation. Saito ¶[0075], ¶[0089], ¶¶[0107]-[0114], FIGS. 19-21.

456. As I explain above, and as well known in the prior art, a POSITA would have found it obvious that insulating film 10A would have deposited into the spaces between the raised SiGe facets and sidewalls 70 and remained there in the final structure. *See* Sections IX.D.1.a and VI.C above. Thus, insulating film 10A, which is silicon oxide like the stress-relief film 28a of the '425 Patent, forms a stress-relief film in a space between the raised SiGe silicon compound layer and the first sidewall spacer 70 in the Saito-Fukutome-James combination. *See* Saito ¶[0074]; '425 Patent, 12:59-13:8.

457. Because Saito teaches that the first insulating film 10A (silicon oxide) remains in the recess 50 and on the sidewalls 70, a POSITA would have recognized that first insulating film 10A would have formed in, and remained in, the space between the raised SiGe facets and sidewalls 70 in the Saito-Fukutome-James combination, as was well known when depositing such films over contoured surfaces like this. *See* Sections IX.D.1.a and VI.C above; Miyashita ¶¶[0052]-[0053], FIGS. 1U-1W; Murthy556, 2:15-24, 9:10-44, FIGS. 2, 7-9; Fukutome, FIG. 5G

(showing CESL 20 forming in [the] space between the facets of SiGe layers 18a/18b and sidewalls 15a/15b); Wu, FIG. 7 (showing CESL 66 forming in the space between the facets of SiGe layers 58 and sidewalls 501A/512A).

458. A POSITA would have found it obvious that Saito's silicon oxide insulating film 10A is a stress-relief film in the Saito-Fukutome-James combination because silicon dioxide layers were known to buffer stress in such a configuration. *See* Sections VI.C and IX.D.1.a above; Murthy556, 8:59-9:43, FIGS. 7-9 (showing oxide buffer in space between raised SiGe facet and electrode to buffer nitride layer above oxide); Alvarez ¶[0049], ¶[0066], ¶[0068], ¶[0077], FIGS. 9-11; Baik ¶[0037], FIG. 1F. Moreover, Saito's teaching that silicon oxide film 10A remains in the recesses and on the sidewalls even after etching is essentially what the '425 Patent describes in terms of stress-relief film 28a. *Compare* Saito ¶[0074], FIG. 21, *and* Figure M (below), *with* '425 Patent, 12:59-13:8, FIG. 6B (item 28a); *see also* Section IX.D.1.a above.

459. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, Saito's insulating film 10A (first stress-relief film, magenta) is formed in a space between the raised facets of the SiGe silicon compound layer (yellow) and the first sidewall spacer (orange). *See* Section IX.D.1.a above; Saito, FIGS. 12, 21.

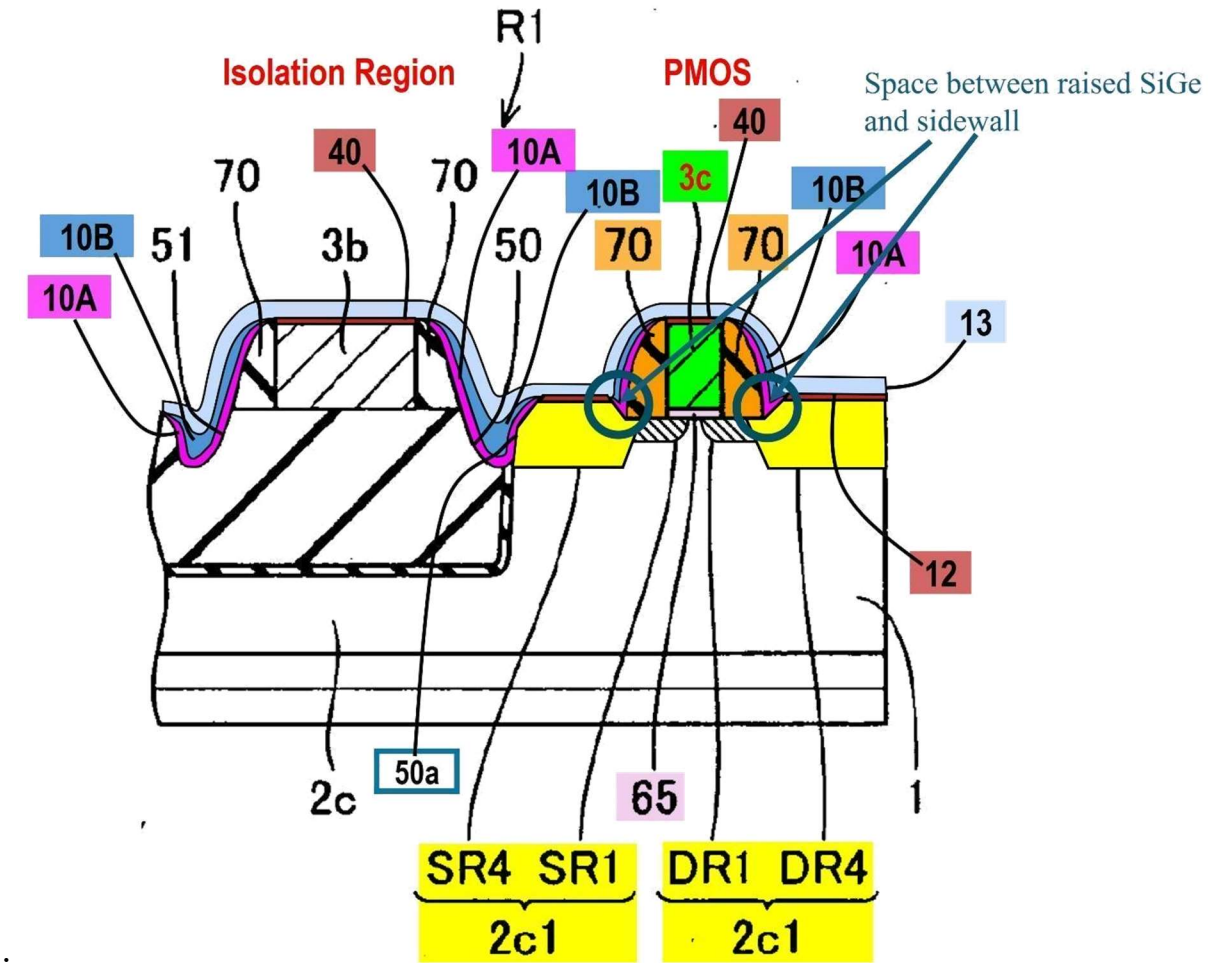


Figure M (further annotated)

(10) [1I]: "the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween"

460. As I explain above for [1H], the stress-relief film in the Saito-Fukutome-James combination (oxide film 10A, magenta) would have been formed on the side surfaces of polysilicon wiring 3c (green) with sidewalls 70 (orange) lying between them. *See* Section IX.D.1.b(9) above. Indeed, as I explain for [1H], Saito's FIGS. 12 and 19-21 show stress-relief oxide film 10A remaining on the sidewalls 70

of the polysilicon gate electrode. *See* Saito ¶[0075], ¶[0089], ¶¶[0107]-[0114], FIGS. 12, 19-21; Section IX.D.1.b(9) above.

461. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, the first stress-relief film 10A (magenta) is formed on the side surfaces of the first gate electrode (green) with the first sidewall spacer 70 (orange) interposed between. *See* Section IX.D.1.a above; Saito, FIGS. 12, 19-21.

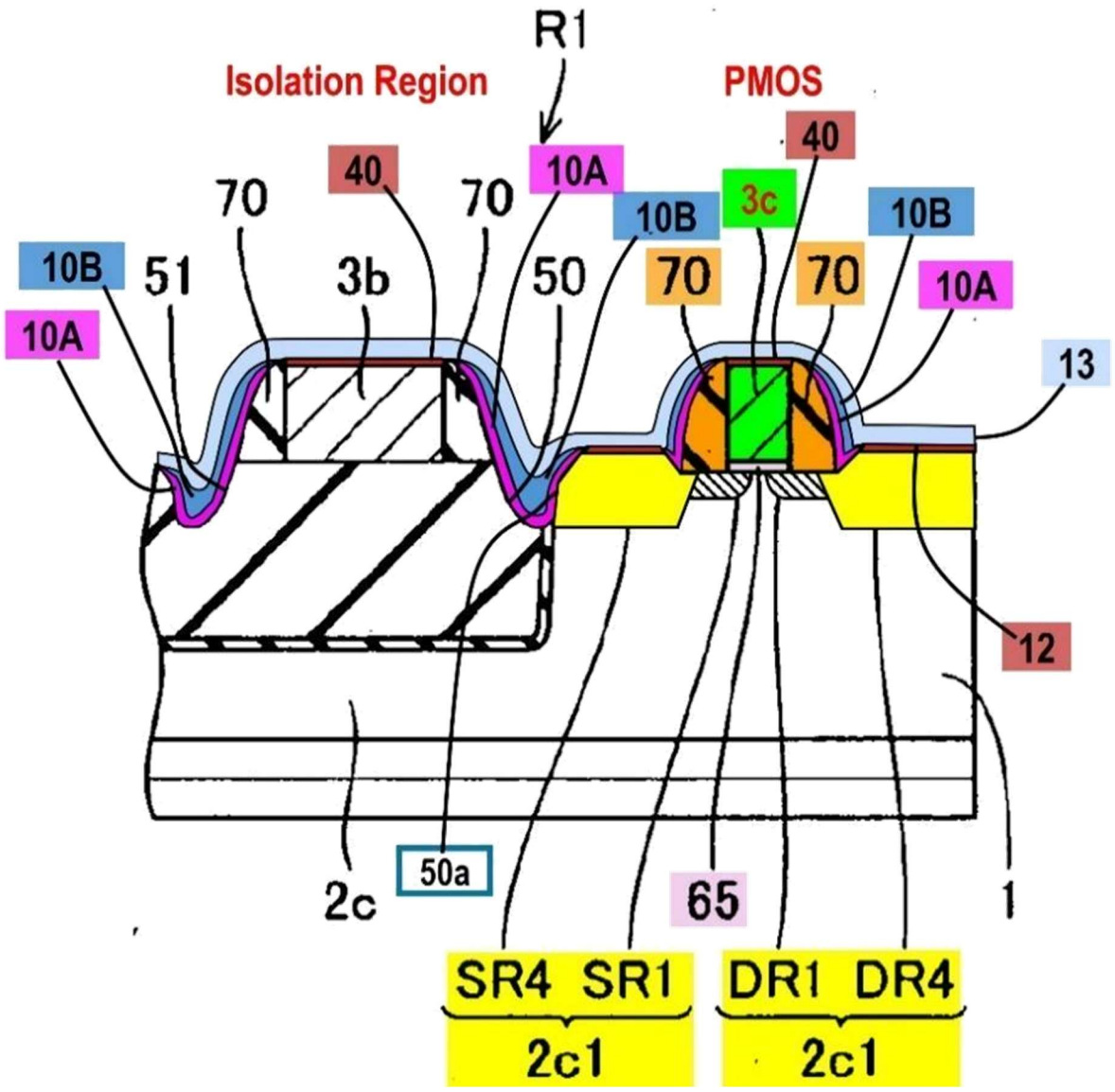


Figure M

(11) [1J]: "the first stress-relief film is not in direct contact with the side surface of the first gate electrode"

462. As I discuss for [1H] and [1I] above, Saito's insulating film 10A (magenta) does not directly contact the side surfaces of the polysilicon gate electrode (green) because sidewalls 70 (orange) lie between insulating film 10A (magenta) and the polysilicon gate electrode (green). *See* Sections IX.D.1.a, IX.D.1.b(9), and IX.D.1.b(10) above.

463. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, the first stress-relief film 10A (magenta) is not in direct contact with the side surfaces of the first gate electrode (green). *See* Section IX.D.1.a above.

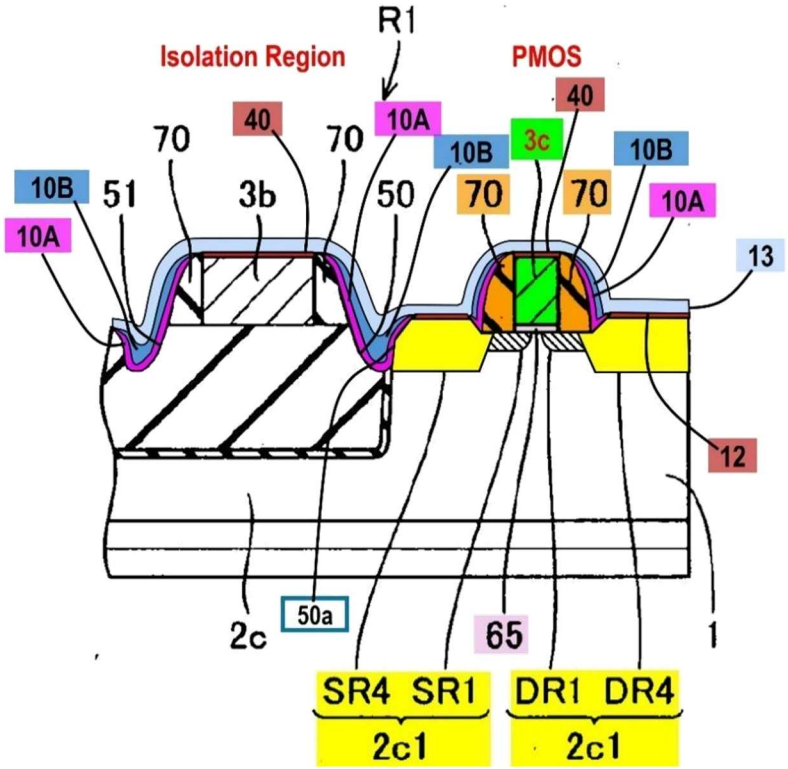


Figure M

c. Claim 3: "The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer"

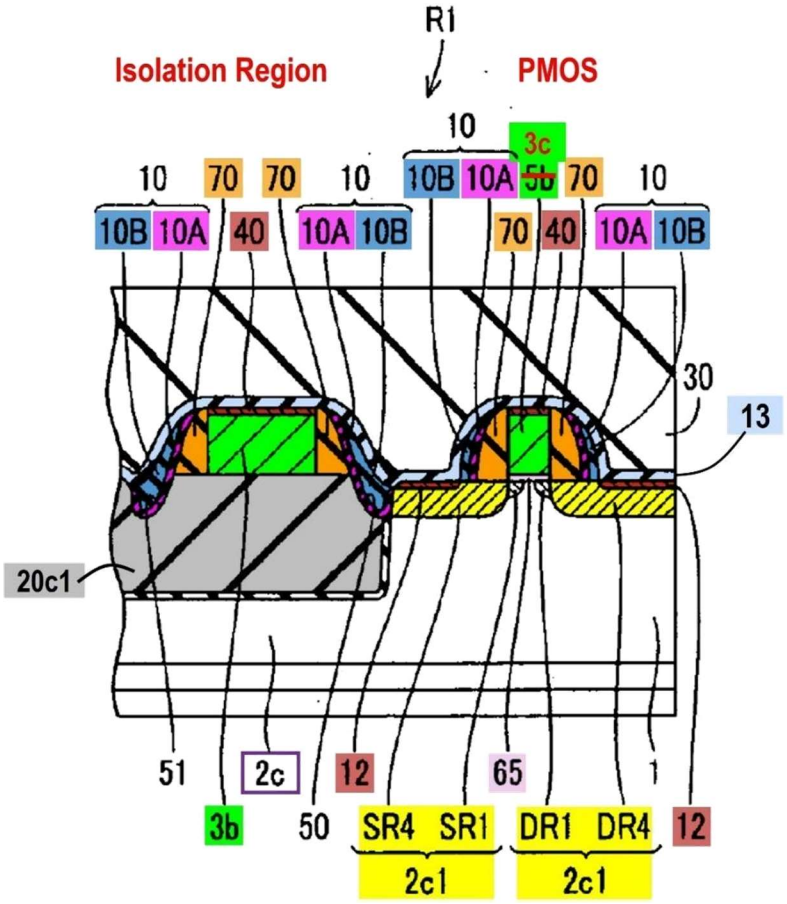
464. In my opinion, the Saito-Fukutome-James combination renders claim 3 obvious.

465. The Saito-Fukutome-James combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.D.1.a and IX.D.1.b above.

466. Saito discloses a silicide film 40 (first silicide layer) formed on the polysilicon wirings and a silicide film 12 (second silicide layer) formed on source/drain regions 2c1 of PMOS transistor P2. Saito ¶[0077], ¶[0117], FIGS. 12, 20-21. Saito explains that "metallic films, such as cobalt (Co), are deposited," "heat treatment" is applied, and "silicide films 12 and 40 are formed," such that "silicide film 12 is formed on the front surface of impurity diffused layer 2c1" and "[s]ilicide film 40 is formed on the upper surface of polysilicon wiring 5b [sic:3c] and 3b . . . ." Saito ¶¶[0116]-[0117], *see also* Saito ¶[0077] ("On the main front surface located in the opposite side with polysilicon wiring 3b, polysilicon wiring 3c shown in FIG. 1 is formed to this silicide film 12 . . . on the main front surface of active region 2c."), FIGS. 12, 20-21.

467. The annotated version of Saito's FIG. 21 below shows that first silicide film 40 (red) is formed on the polysilicon wiring 5b [sic:3c] (green), and the second

silicide film 12 (also red) is formed on the source/drain regions 2c1 (yellow) of PMOS transistor P2.



Saito's FIG. 21 (excerpted, annotated)

468. When incorporating Fukutome's epitaxial SiGe source/drain regions into Saito's PMOS transistors P1 and P2, a POSITA would have understood that a silicide film 12 would form on the epitaxial SiGe regions just as it forms on Saito's non-epitaxial source/drain regions SR4 and DR4, and silicide film 40 would form on the polysilicon wirings 3b/5b [sic:3b/3c] just as it does in Saito. *See* Sections IX.D.1.a and IX.D.1.b above. In fact, Fukutome teaches such silicide layers as well. *See* Fukutome ¶¶[0103]-[0104], FIGS. 5E-5G.

469. As the embodiment of the Saito-Fukutome-James combination in Figure M shows below, the first silicide film 40 (red) forms on the polysilicon wiring 5b [sic:3c] (green), and the second silicide film 12 (also red) forms on the top surfaces of the raised SiGe source/drain regions (yellow). *See* Section IX.D.1.a above.

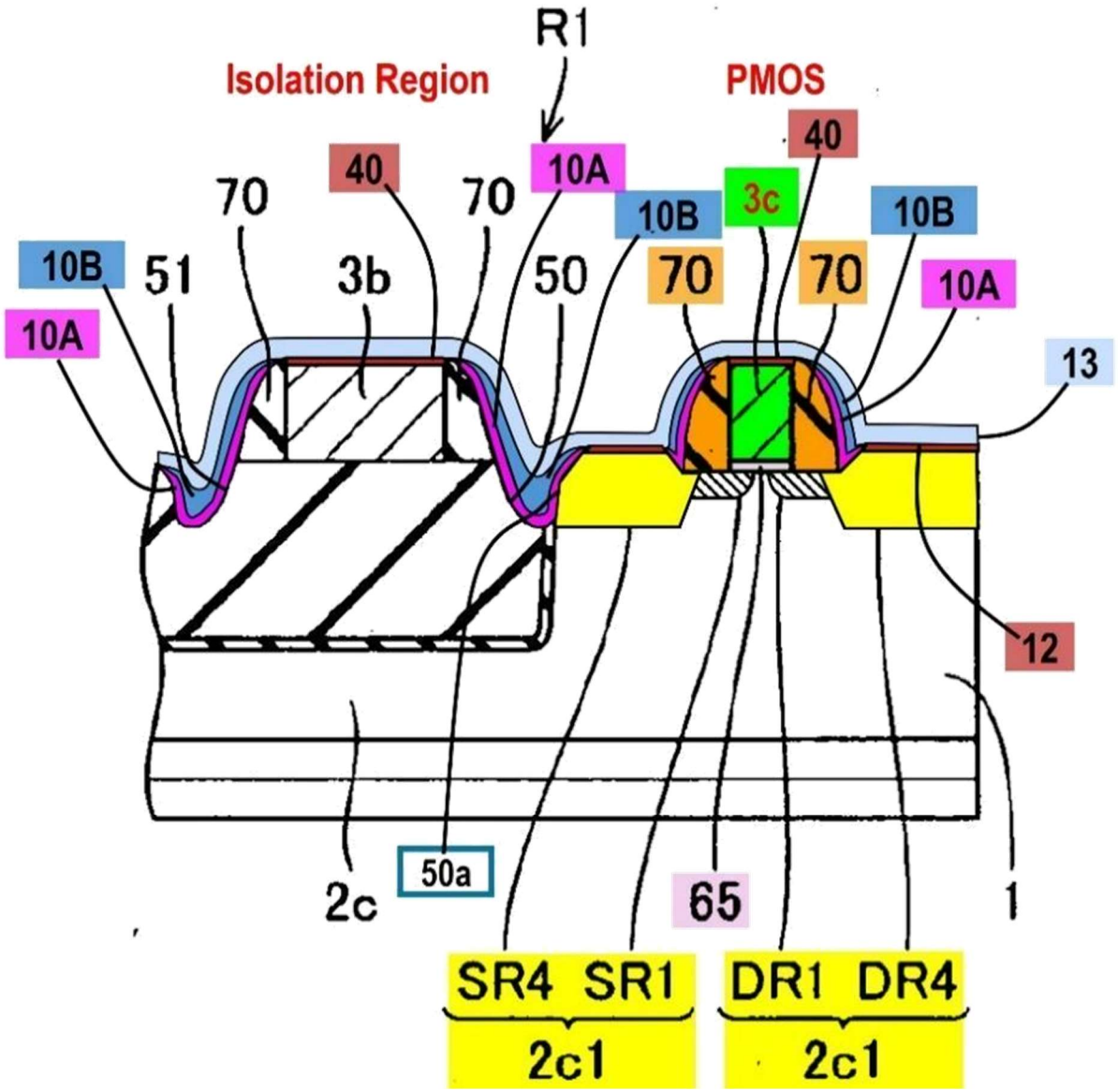


Figure M

470. Fukutome discloses that, even after silicide formation on the SiGe regions, the top surface of the raised SiGe remains above the top surface of the substrate. *See* Fukutome ¶¶[0103]-[0104], FIGS. 5F-5G. As exemplary dimensions, Fukutome teaches that the SiGe layers may have a thickness up to about 120 nm, whereas the trenches in which they grow have a maximum depth of about 20-70 nm, meaning the SiGe extends about 50-100 nm above the substrate. *See* Fukutome ¶[0093], ¶[0099]. Saito contemplates adding a silicide about 10 nm thick, which would have been typical at the time. Saito ¶[0116]. A POSITA would have understood that such dimensions would have been consistent with the representations in Fukutome's FIGS. 5F and 5G, where the top surface of the SiGe layers remain above the top surface of the substrate after silicidation. This is also what James shows in Intel's 90 nm pFET. *See* James, Fig. 6.

471. A POSITA would have found it obvious to maintain the top level of the SiGe source/drains above the surface of the substrate to suppress source/drain junction leakage and to improve reliability, as discussed above. *See* Fukutome ¶[0100]; Sections IX.D.1.a and IX.D.1.b.

d. Claim 4: "The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer"

472. In my opinion, the Saito-Fukutome-James combination renders claim 4 obvious.

473. The Saito-Fukutome-James combination renders the semiconductor device of claim 1 obvious. *See* Sections IX.D.1.a and IX.D.1.b above.

474. As I explain for [1H], and as the embodiment of the Saito-Fukutome-James combination in Figure M shows below, stress-relief film 10A (magenta) would have formed on the facets (side surfaces) of the raised SiGe source/drain regions (silicon compound layers, yellow). *See* Sections IX.D.1.a and IX.D.1.b(9).

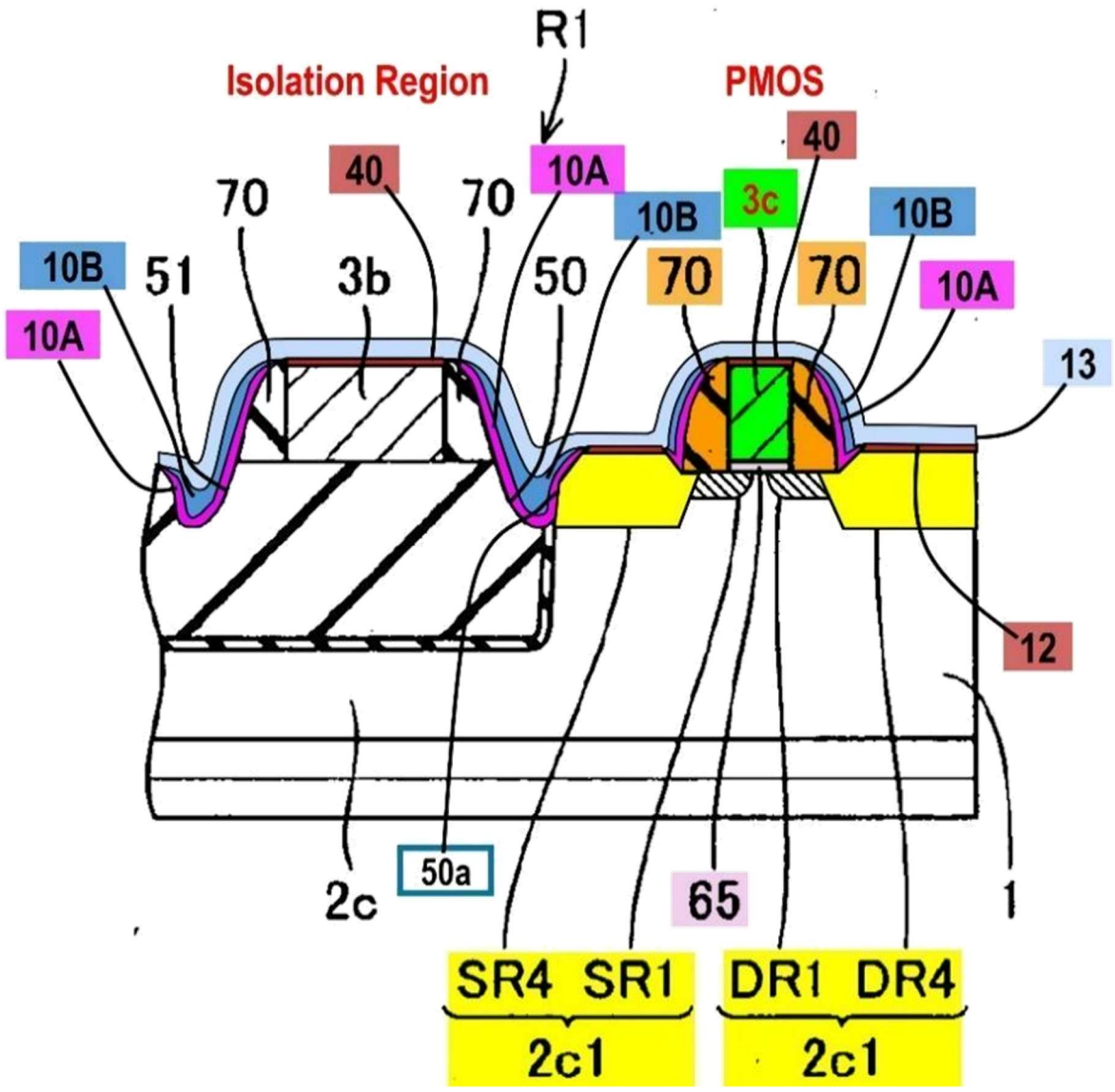


Figure M

e. Claim 7:

(1) [7Pre]: "The semiconductor device of claim 1"

475. The Saito-Fukutome-James combination renders the semiconductor device of claim 1 obvious. *See* Section IX.D.1.b above.

(2) [7A]: "the first MIS transistor is a p-type MIS transistor"

476. As I explain above for claim 1, Saito discloses that the first MIS transistor is a PMOS transistor (e.g., PMOS transistor P2). *See* Section IX.D.1.b(2) above. The Saito-Fukutome-James combination relies on this PMOS transistor, as modified according to the embodiment shown in Figure M, for example. *See* Section IX.D.1.b(2) above.

(3) [7B]: "the first stress is a compressive stress"

477. As I explain above for claim 1, the addition of raised SiGe source/drain regions (like the ones Fukutome discloses) would compressively stress the pFET channel region. *See* Sections IX.D.1.a and IX.D.1.b(6) above. The Saito-Fukutome-James combination, such as the exemplary embodiment Figure M illustrates, relies on this compressive stress caused by the raised SiGe source/drain regions. *See* Sections IX.D.1.a and IX.D.1.b(6) above; Fukutome ¶[0110]; James, 2.

(4) [7C]: "the second stress is a tensile stress"

478. As I explain above for claim 1, a POSITA would have found it obvious to make Saito's SiN insulating film 13 tensile, as James teaches. *See* Sections

IX.D.1.a and IX.D.1.b(7); James 2, 5. The Saito-Fukutome-James combination, such as the exemplary embodiment Figure M illustrates, relies on this tensile stress caused by tensile SiN insulating film 13. *See* Sections IX.D.1.a and IX.D.1.b(7) above; James, 2, 5.

f. Claim 8:

(1) [8Pre]: "The semiconductor device of claim 1"

479. The Saito-Fukutome-James combination renders the semiconductor device of claim 1 obvious. *See* Section IX.D.1.b above.

(2) [8A]: "the silicon compound layer is a SiGe layer"

480. As I explain above for claim 1, the Saito-Fukutome-James combination relies on epitaxial SiGe source/drain regions (like the ones Fukutome discloses) as the silicon compound layer. *See* Sections IX.D.1.a and IX.D.1.b(6) above; Fukutome ¶[0005], ¶[0098], ¶[0110], FIGS. 5D-5G.

(3) [8B]: "the stress insulating film is a silicon nitride film"

481. As I explain above for claim 1, Saito's silicon nitride insulating film 13 maps onto the stress insulating film. *See* Sections IX.D.1.a and IX.D.1.b(7) above; Saito ¶[0080], ¶[0120], FIG. 21. The Saito-Fukutome-James combination, such as the exemplary embodiment Figure M illustrates, relies on this silicon nitride insulating film 13 as the stress insulating film. *See* Sections IX.D.1.a and IX.D.1.b(7) above; Saito ¶[0080], ¶[0120], FIG. 21; James, 2, 5, Fig. 6.

(4) [8C]: "the first stress-relief film is a silicon oxide film"

482. As I explain above for claim 1, Saito's silicon oxide film 10A maps onto the stress-relief film. *See* Sections IX.D.1.a and IX.D.1.b(9) above. The Saito-Fukutome-James combination, such as the exemplary embodiment Figure M illustrates, relies on this silicon oxide film 10A as the first stress-relief film. *See* Sections IX.D.1.a and IX.D.1.b(9) above; Saito ¶¶[0074]-[0076], FIGS. 18-21.

g. Claim 10:

(1) [10Pre]: "The semiconductor device of claim 1"

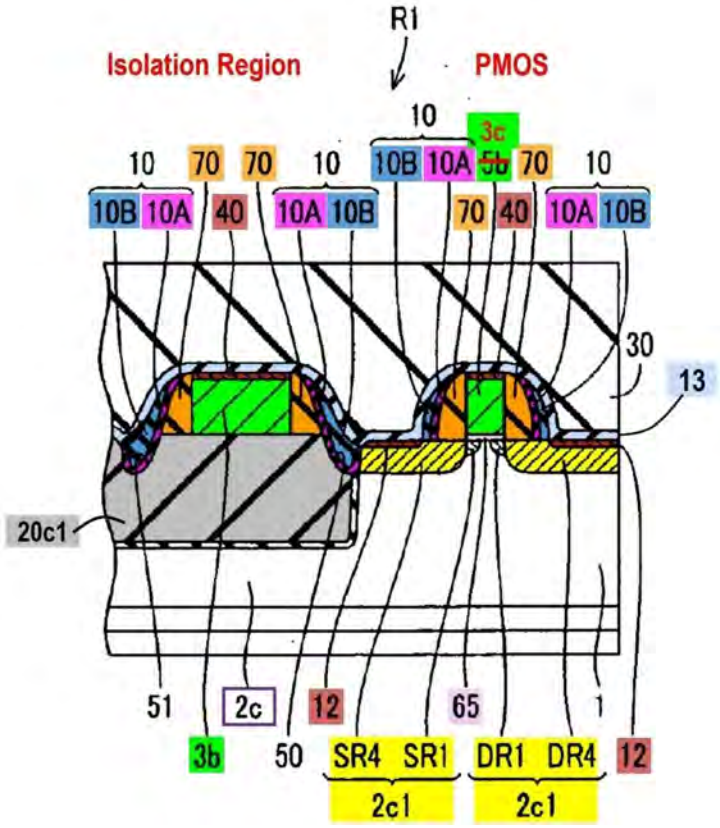
483. The Saito-Fukutome-James combination renders the semiconductor device of claim 1 obvious. *See* Section IX.D.1.b above.

(2) [10A]: "an isolation region formed in the semiconductor substrate to surround the first active region"

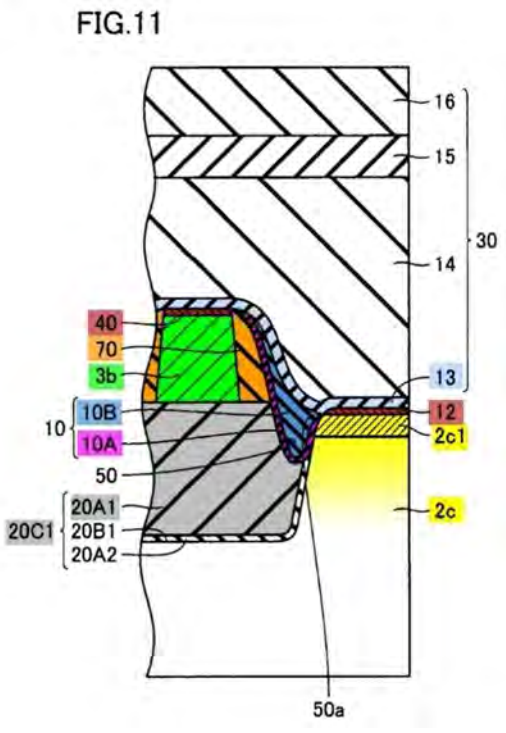
484. Saito discloses an isolation region 20C1 that comprises a trench 20B1 lined with a thermal silicon oxide film 20A2 and then filled with a deposited silicon oxide film 20A1. Saito ¶[0073], ¶¶[0088]-[0089], FIGS. 3, 11-14, 21. Isolation region 20C1 defines the portion of Saito's substrate 100 where active region 2c is located, for example (i.e., where PMOS transistor P2 is located), and surrounds active region 2c. *See* Saito ¶[0051] ("On the main front surface of semiconductor substrate 100 in which memory cell region R1 is located, isolation region 20c1 and active region 2c specified by this isolation region 20c1 are formed."), ¶¶[0072]-

[0073] ("[I]isolation region 20c1 selectively formed on the main front surface of semiconductor substrate 100 and active region 2c specified by isolation region 20c1 on the main front surface of semiconductor substrate 100 are formed."), ¶¶[0086]-[0090], FIGS. 1, 3, 11-14, 21. This is a fundamental role isolation regions play.

485. The annotated versions of Saito's FIGS. 11 and 21 below, as well as Figure N (same as Figure M but with additional annotations), show isolation region 20c1 (gray) formed in the semiconductor substrate to surround first active region 2c.



Saito's FIG. 21 (excerpted, annotated)



Saito's FIG. 11 (annotated)

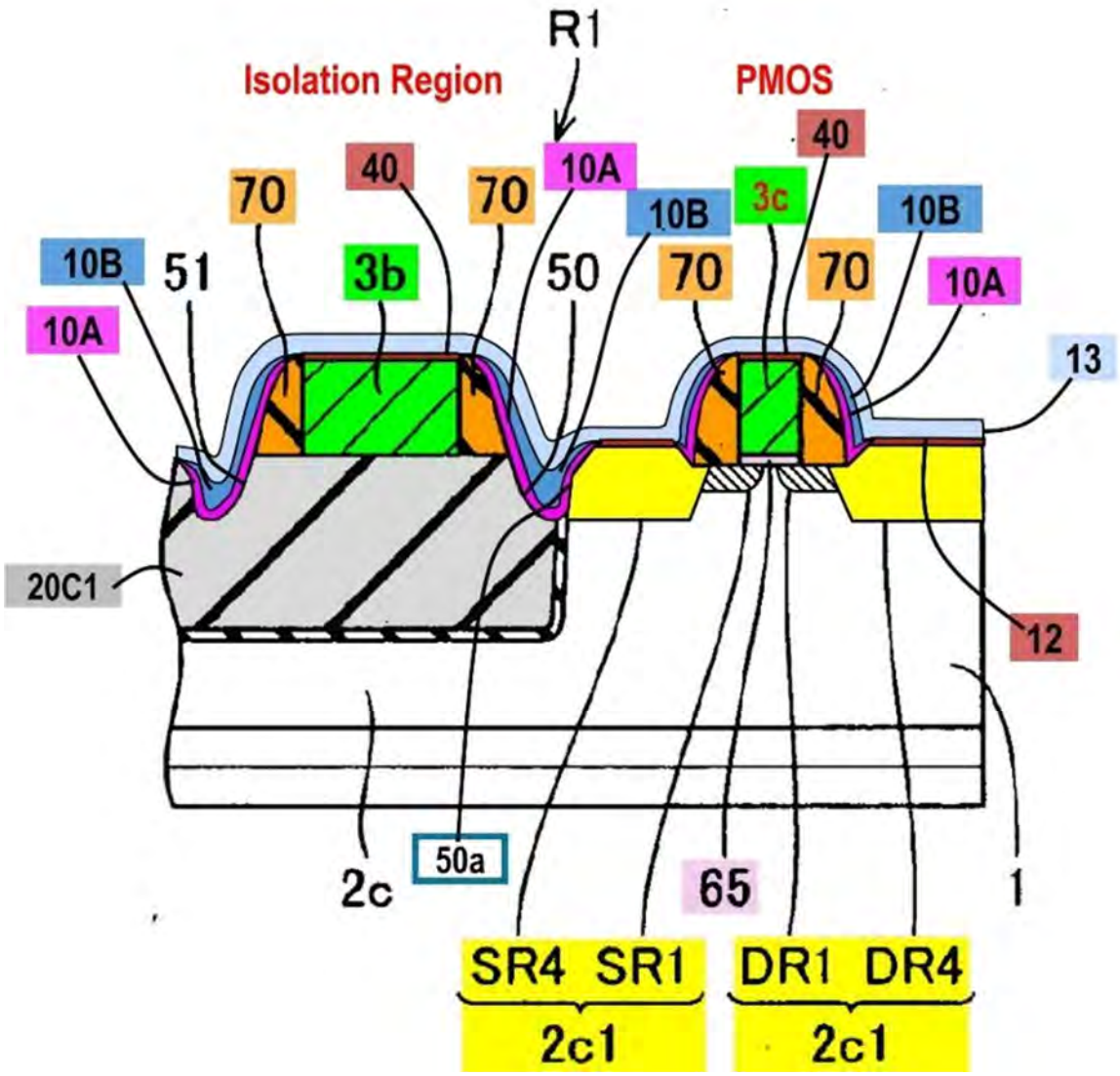
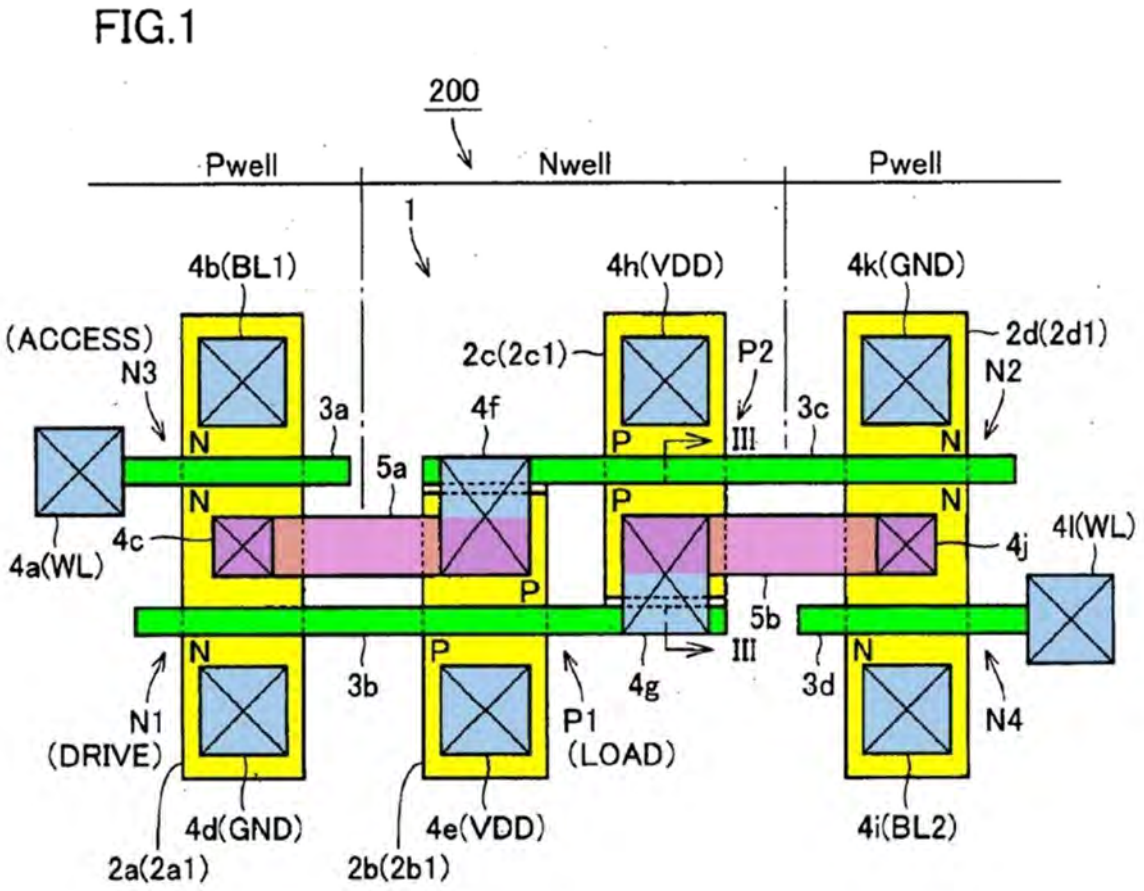


Figure N

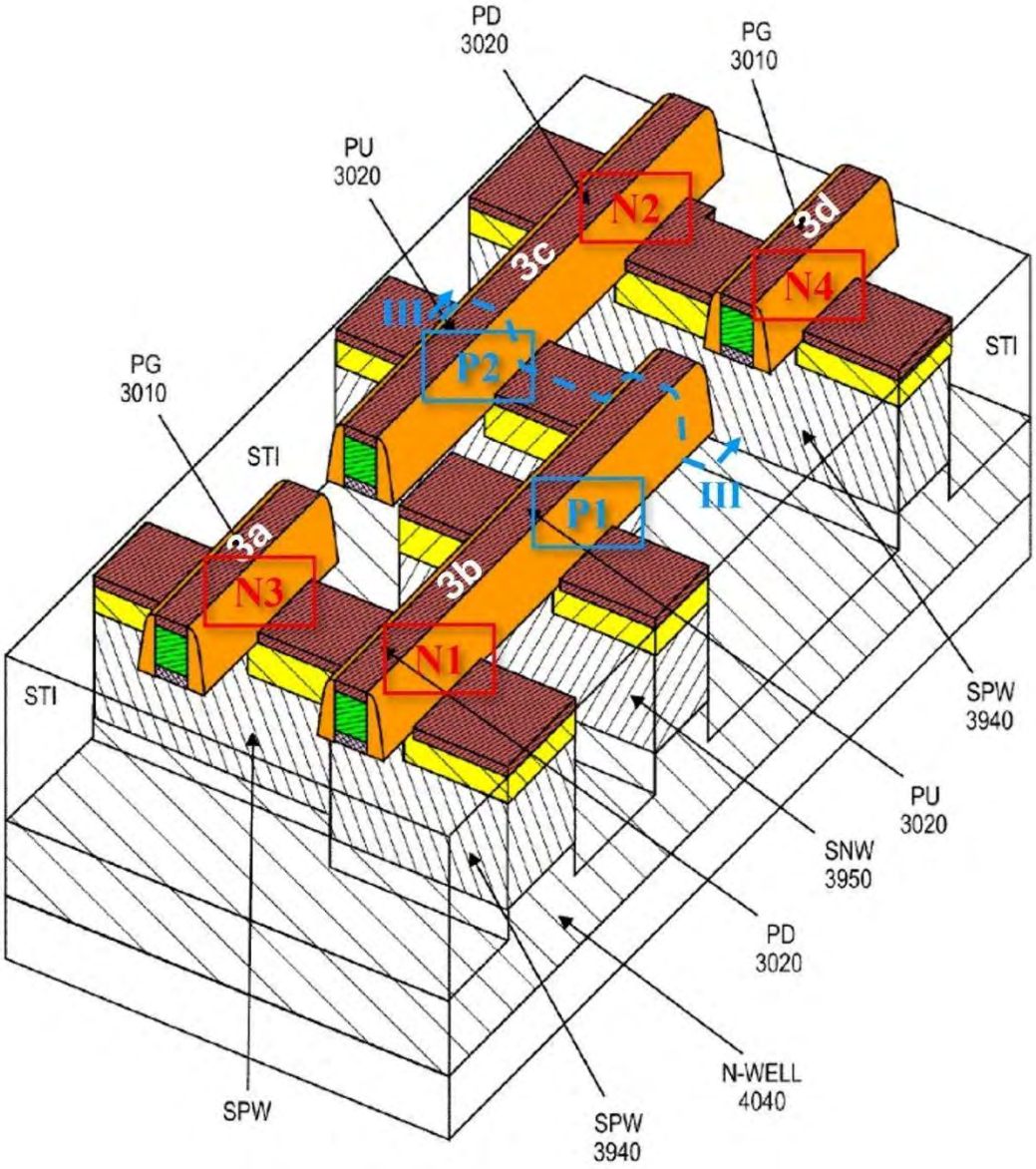
486. Just as any typical "STI" (shallow trench isolation) surrounds the active regions in a wafer, a POSITA would have understood that Saito's isolation region 20C1 surrounds active region 2c. *Compare* Saito ¶[0049], ¶¶[0060]-[0070], FIGS. 1-2, *with* Thompson498 ¶¶[0204]-[0205], FIGS. 39-40B. Saito's FIG. 1 shows this, for example, because the PMOS active regions 2b and 2c are specific regions within a larger n-type well ("N-well") region. The isolation regions must surround those

active regions (and all active regions 2a-2d) to electrically isolate those portions of the substrate. This has been a fundamental aspect of semiconductor manufacturing almost since its inception. *See* Plummer, 52-60.



Saito's FIG. 1 (annotated)

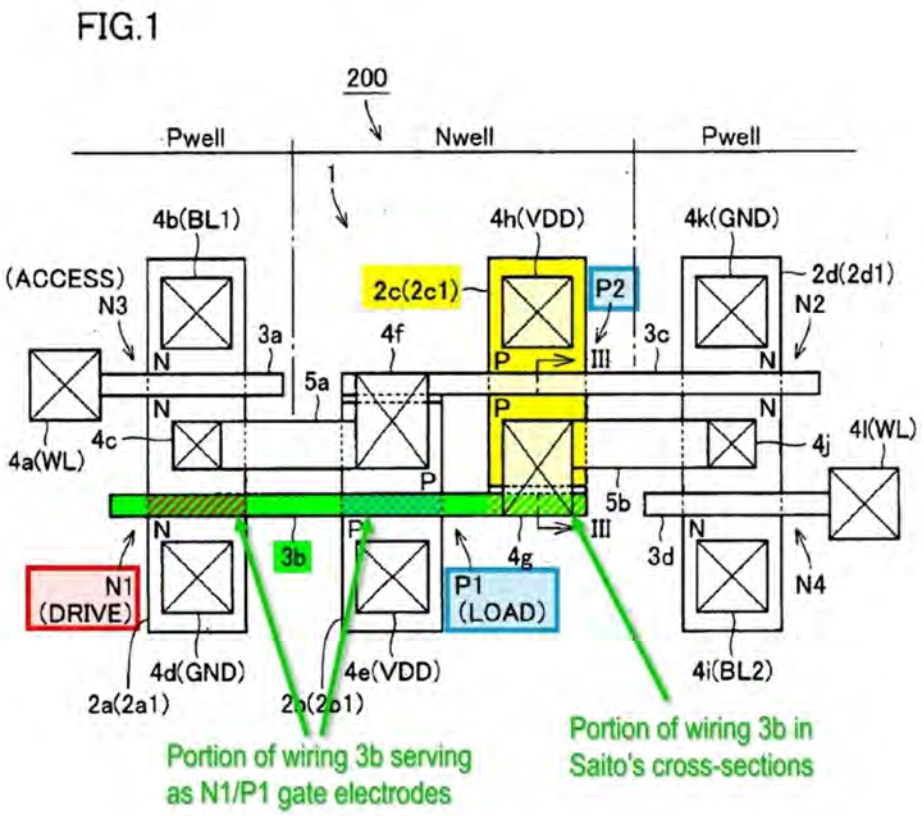
487. The annotated version of FIG. 40B below from one of my SRAM patents illustrates how this would look in Saito's SRAM. It shows that the isolation regions (labeled "STI") surround the active regions (yellow). *See* Thompson498, FIG. 40B. The same would also be true in Saito's analogous SRAM cell. *See* Section IX.D.1 (introduction) above.



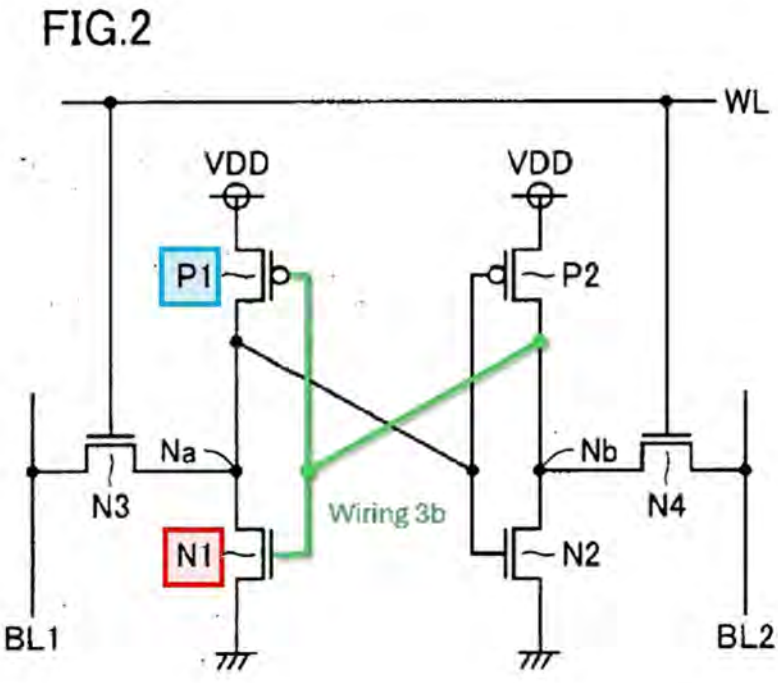
Thompson498's FIG. 40B (annotated)

(3) [10B]: "a gate interconnect formed on the isolation region"

488. Saito discloses "polysilicon wiring 3b" formed on isolation region 20C1. Saito ¶[0073], ¶[0093], FIGS. 1, 3, 11-12, 16, 21. Polysilicon wiring 3b forms a gate interconnect because it interconnects the gate electrodes of transistors N1 and P1, as annotated FIGS. 1 and 2 show below. *See* Saito ¶¶[0065]-[0066], FIGS. 1-2.

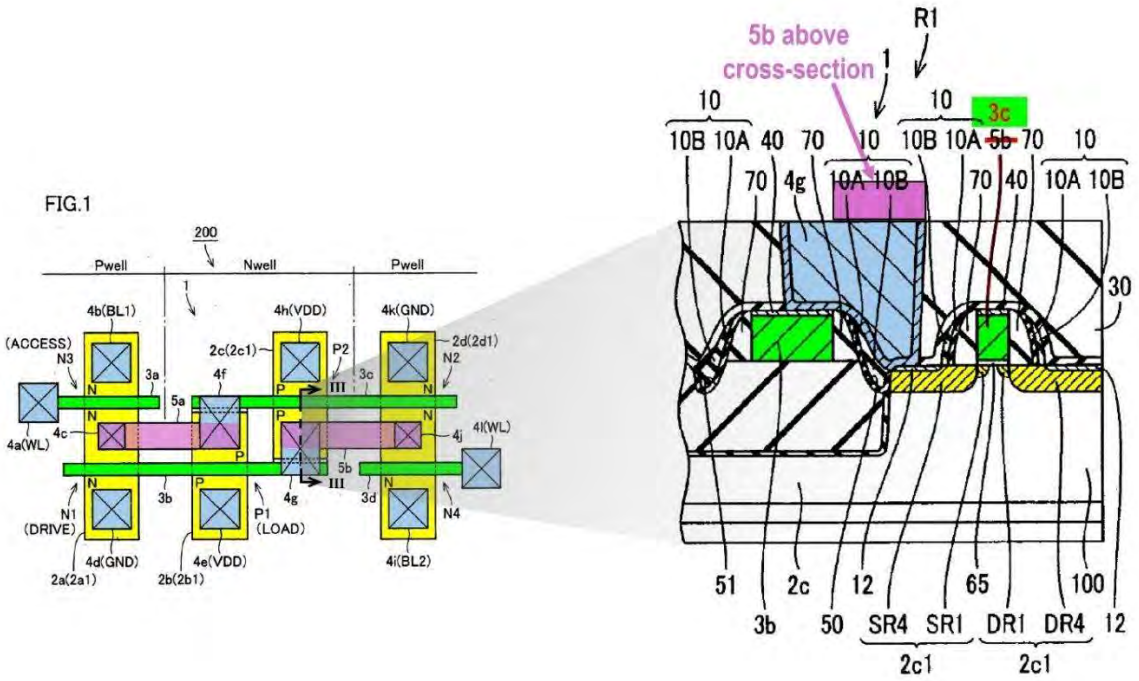


Saito's FIG. 1 (annotated)



Saito's FIG. 2 (annotated)

489. Saito explains the gate electrodes of transistors N1 and P1 are "formed in the intersection" of polysilicon wiring 3b and the respective active regions 2a (for transistor N1) and 2b (for transistor P1). Saito ¶¶[0065]-[0066]. Saito confirms that "polysilicon wiring (wiring layer) 3b is [also] formed" on isolation insulating film 20A1. Saito ¶[0073] ("[O]n isolation insulating film 20A1, polysilicon wiring (wiring layer) 3b is formed."); *see also* Saito ¶[0093], FIGS. 11, 21. Saito's annotated FIGS. 1 and 12 below emphasize this point, showing polysilicon wiring 3b (green) sitting atop isolation region 20C1 (not colored). *See also* Saito, FIG. 3.



Saito's FIG. 1 **Saito's FIG. 12 (excerpted, annotated)**

490. As the embodiment of the Saito-Fukutome-James combination in Figure N shows below, polysilicon wiring 3b (green) performs the same interconnect function in the Saito-Fukutome-James combination. *See* Section IX.D.1.a above.

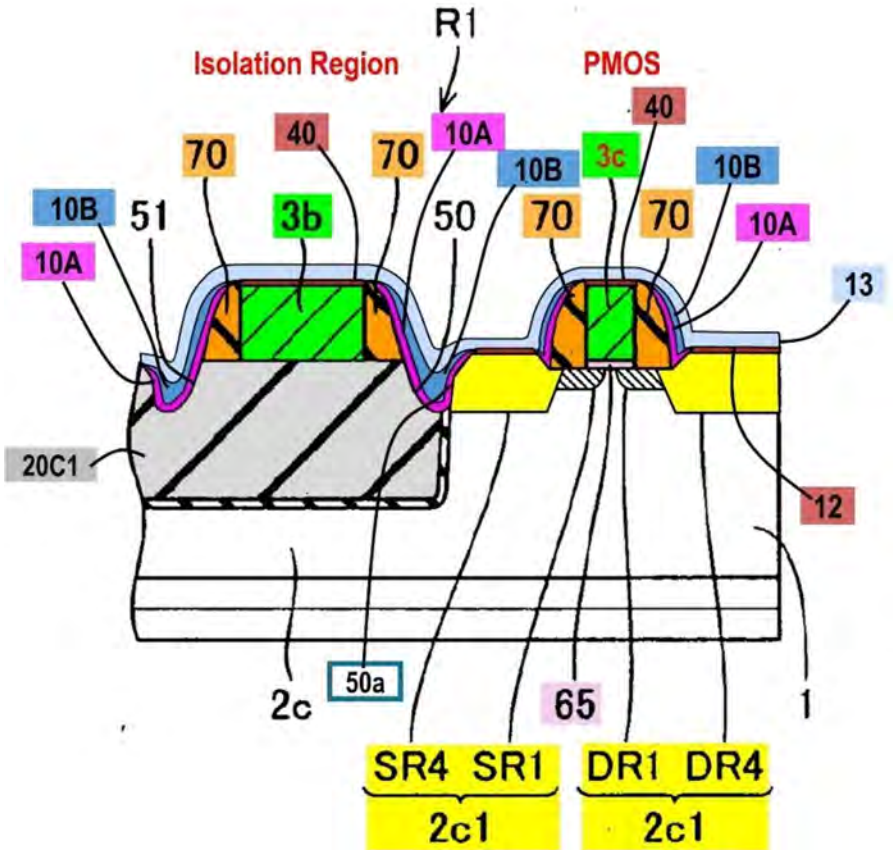
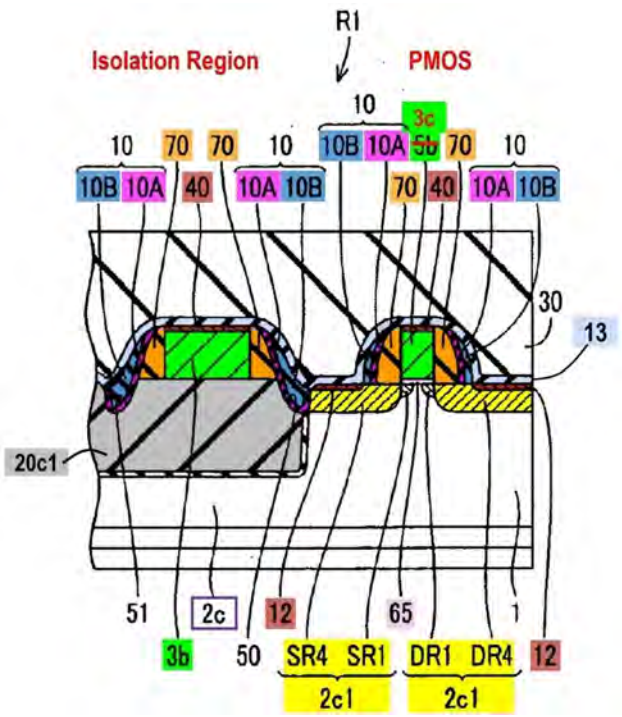


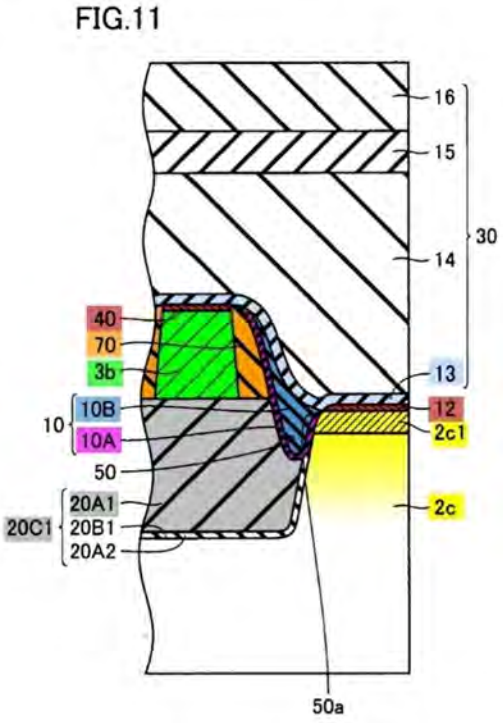
Figure N

(4) [10C]: "an interconnect sidewall spacer formed on a side surface of the gate interconnect"

491. Saito discloses that sidewall 70 forms on the side surfaces of polysilicon wiring 3b (the gate interconnect). Saito ¶[0073], ¶[0096], FIGS. 3, 5, 11, 12, 17, 21. Saito discloses that "[o]n the both side [sic] surfaces of this polysilicon wiring 3b, sidewall (side wall oxide film) 70 which consists of a silicon oxide film etc. is formed." Saito ¶[0073]; *see also* Saito ¶[0096] ("[S]idewall 70 is formed on the both [sic] side surfaces of . . . polysilicon wiring 3b."). The annotated versions of Saito's FIGS. 11 and 21 show that Saito's interconnect sidewall spacers 70 (orange) are formed on the side surfaces of gate interconnect polysilicon wiring 3b (green).



Saito's FIG. 21 (excerpted, annotated)



Saito's FIG. 11 (annotated)

492. As the embodiment of the Saito-Fukutome-James combination in Figure N shows below, interconnect sidewall spacers (orange) also sit on the sides of polysilicon wiring 3b (green) in the combination. *See* Section IX.D.1.a above.

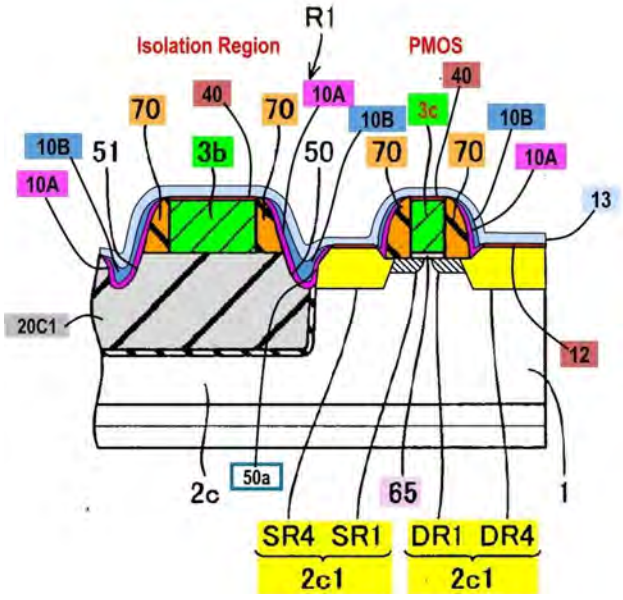


Figure N

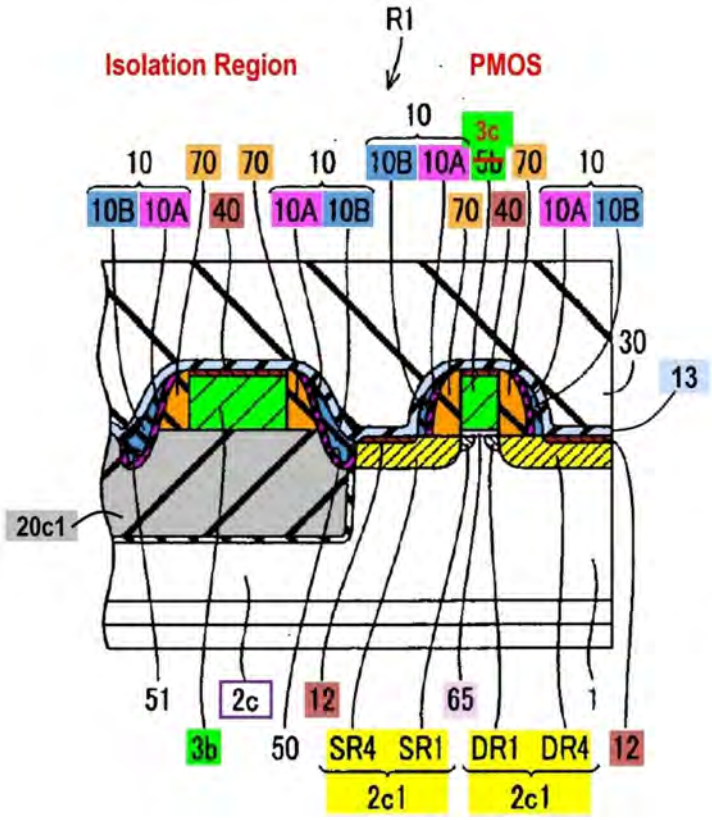
(5) [10D]: "a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer"

493. Saito discloses that insulating film 10A forms on a side surface 50a of a recessed portion 50 provided in isolation region 20C1 on a lateral side of the interconnect sidewall spacer 70. *See* Saito ¶¶[0074]-[0076], ¶[0082], ¶[0107], ¶¶[0113]-[0114], FIGS. 3, 6-7, 11-12, 21.

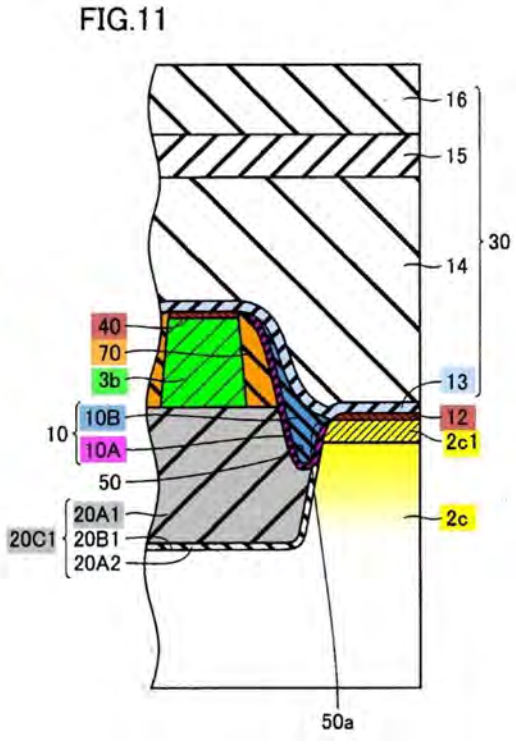
494. Insulating film 10A is the same oxide layer identified as the stress-relief film recited in claim 1, except for purposes of claim 10, I focus on insulating film 10A where it forms on the sides of recess 50 in isolation region 20C1. *See* Sections IX.D.1.a and IX.D.1.b above. Saito explains that "insulating film 10A which consists of a silicon oxide film etc. is formed so that the front surface of this recess 50 may be covered. . . . This insulating film 10A is formed on the side surface of sidewall 70 while it covers the internal surface of recess 50." Saito ¶[0074]; *see also* Saito ¶[0113] ("[I]nsulating film 10A [is] formed along the internal surface of recesses 50 and 51 . . . ."); Saito ¶[0076], ¶[0082], ¶[0104].

495. This is similar to the '425 Patent, in which first stress-relief film 28a of the pMIS device is formed from the same film 28 as second stress-relief film 28*x* in the recessed portion 20 of isolation region 11. *Compare* '425 Patent, 12:59-13:12, FIGS. 5A, 5B, *with* Saito ¶[0076], ¶[0082], ¶¶[0104]-[0107], ¶¶[0113]-[0114], FIGS. 6-7, 18-19.

496. The annotated versions of Saito's FIGS. 11 and 21 below illustrate the insulating oxide film 10A (second stress-relief film, magenta) being formed on the side surfaces of a recessed portion 50 provided in isolation region 20c1 (gray) on a lateral side of the interconnect sidewall spacer 70 (orange).



Saito's FIG. 21 (excerpted, annotated)



Saito's FIG. 11 (annotated)

497. The same is true in the Saito-Fukutome-James combination. As the exemplary embodiment shown in Figure N below shows, insulating oxide film 10A (second stress-relief film, magenta) is formed on a side surface of a recessed portion 50/51 provided in the isolation region 20c1 (gray) on a lateral side of the interconnect sidewall spacer 70 (orange). *See* Sections IX.D.1.a and IX.D.1.b above.

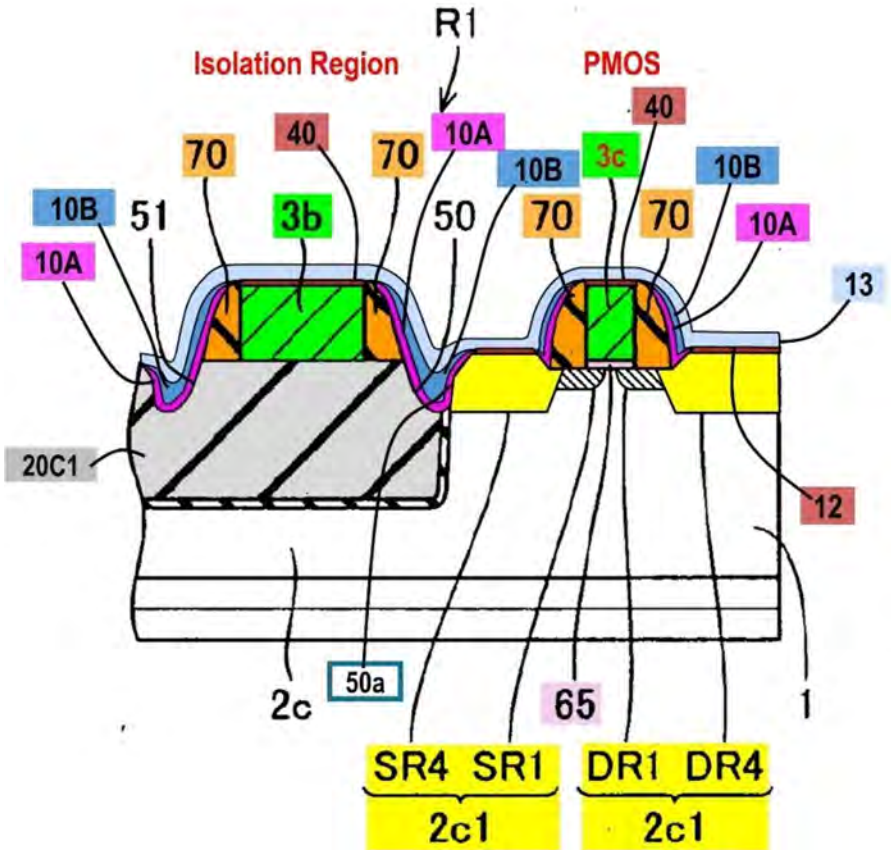


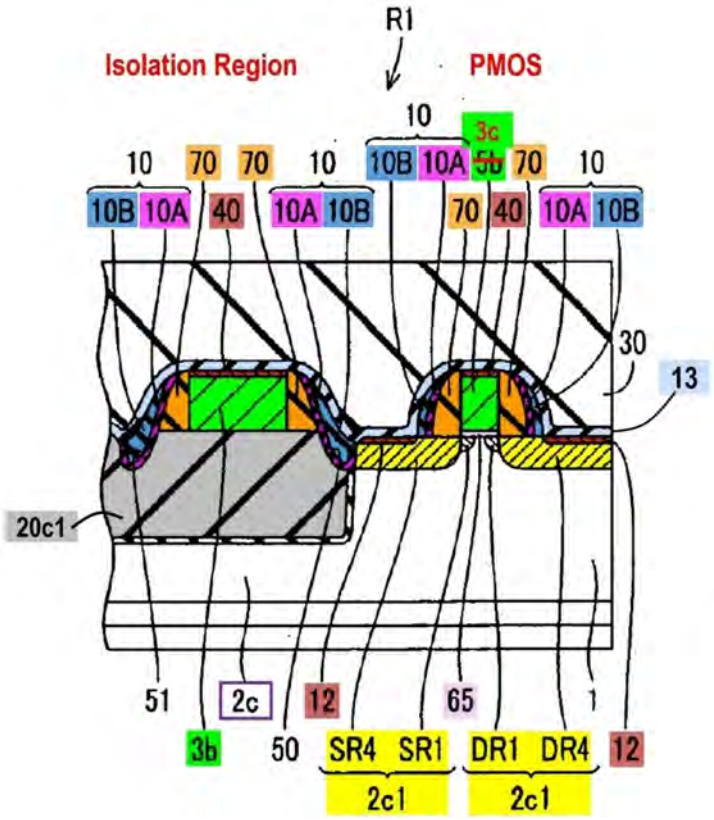
Figure N

(6) [10E]: "the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film"

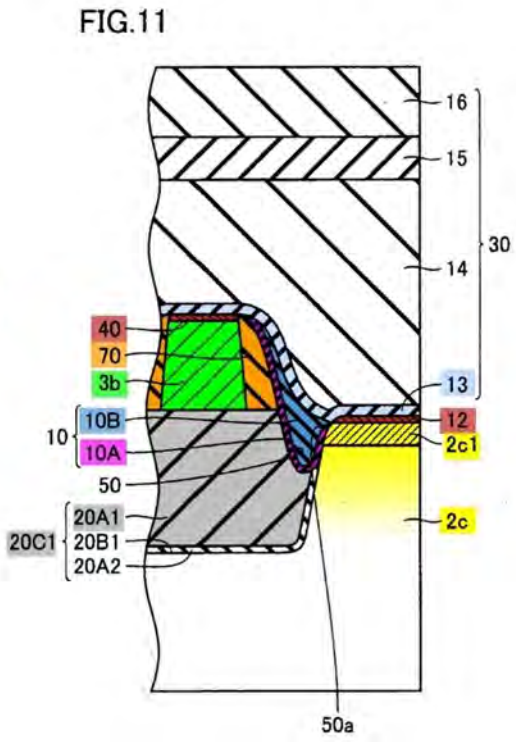
498. Saito discloses that insulating film 13 (the stress insulating film) is formed on isolation region 20C1 such that it covers polysilicon wiring 3b (the gate interconnect), sidewall 70 (interconnect sidewall spacer), and oxide insulating film 10A (the second stress-relief film). Saito ¶[0080], ¶[0120], FIGS. 3, 9, 11, 12, 21.

499. Saito explains that "insulating film 13 . . . is formed on polysilicon wiring 3b, sidewall 70, and the main front surface of semiconductor substrate 100 formed on impurity diffusion region 2c1." Saito ¶[0120]. The annotated versions of

Saito's FIGS. 11 and 21 below demonstrate that tensile stress insulating film 13 (light blue) is formed on the isolation region 20c1 (gray) to cover polysilicon gate interconnect wiring 3b (green), interconnect sidewall spacer 70 (orange), and second stress-relief oxide film 10A (magenta). As I discuss elsewhere in detail, a POSITA would have found it obvious to form Saito's insulating film 13 such that it is tensile. *See* Sections VI.B, IX.D.1.a, and IX.D.1.b above; James, 2, 5, Fig. 6.



Saito's FIG. 21 (excerpted, annotated)



Saito's FIG. 11 (annotated)

500. The same is true in the Saito-Fukutome-James combination. As the exemplary embodiment shown in Figure N below shows, tensile stress insulating film 13 (light blue) is formed on isolation region 20c1 (gray) to cover polysilicon gate interconnect wiring 3b (green), interconnect sidewall spacer 70 (orange), and

second stress-relief oxide film 10A (magenta). *See* Sections IX.D.1.a and IX.D.1.b above.

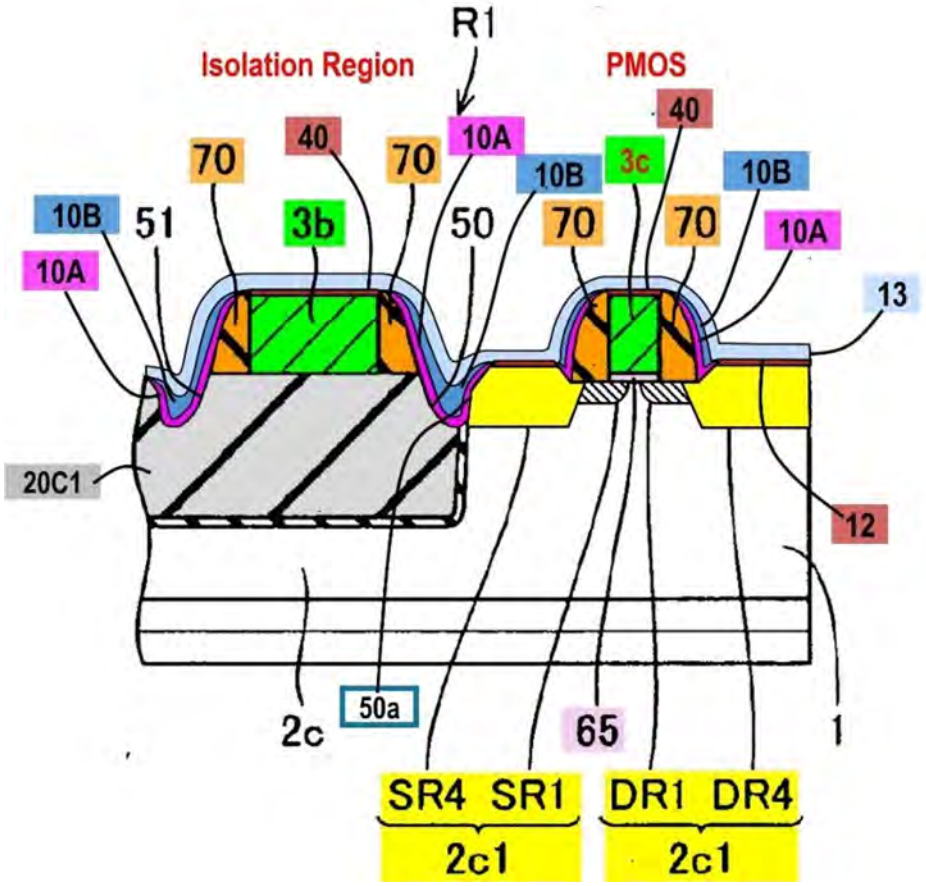


Figure N

X. CONCLUSION

501. As I discuss above, it is my opinion that the Challenged Claims of the '425 Patent (claims 1-15) are unpatentable because they would have been obvious to a person of ordinary skill in the art.

502. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject

to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

503. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

504. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 14th day of March, 2025, in Gainesville, FL.

By: 

Dr. Scott E. Thompson, Ph.D.

Appendix A

Exhibit	Description
Ex-1001	U.S. Patent No. 8,907,425 B2 to Itou et al. ("the '425 Patent").
Ex-1002	Prosecution History of the '425 Patent (excerpted) ("File History").
Ex-1005	U.S. Pat. Pub. No. 2009/0246922 A1 to Wu et al. ("Wu").
Ex-1006	U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al. ("Alvarez").
Ex-1007	S. Wolf, *Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology* (2002) (excerpted) ("Wolf").
Ex-1008	U.S. Pat. Pub. No. 2005/0112817 A1 to Cheng et al. ("Cheng").
Ex-1009	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. ("Wang").
Ex-1010	U.S. Pat. Pub. No. 2008/0029825 A1 to Saito et al. ("Saito").
Ex-1011	U.S. Pat. Pub. No. 2005/0285203 A1 to Fukutome et al. ("Fukutome").
Ex-1012	D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) ("James").
Ex-1013	S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) (excerpted) ("Sze").
Ex-1014	J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (excerpted) ("Plummer").
Ex-1015	S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) ("Thompson2004").

Exhibit	Description
Ex-1016	Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) ("Sun").
Ex-1017	T. Ghani et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," Technical Digest of the 2003 IEEE International Electron Devices Meeting ("IEDM"), pp. 278-80 (Dec. 10, 2003) ("Ghani").
Ex-1018	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. ("Bohr683").
Ex-1019	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros").
Ex-1020	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. ("Murthy151").
Ex-1021	U.S. Pat. Pub. No. 2011/0042729 A1 to Chen et al. ("Chen729").
Ex-1022	P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) ("Morin").
Ex-1023	U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. ("Hsu823").
Ex-1024	U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al. ("Jung").
Ex-1025	U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al. ("Ke").

Exhibit	Description
Ex-1026	P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) ("Bai").
Ex-1027	K. Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) ("Mistry").
Ex-1028	S. Natarajan et al., "A 32nm Logic Technology Featuring 2^{nd}-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171μm^2 SRAM Cell Size in a 291Mb Array," Technical Digest of the of the 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1-3 (Dec. 2008) ("Natarajan").
Ex-1029	U.S. Pat. Pub. No. 2004/0262784 A1 to Doris et al. ("Doris").
Ex-1030	U.S. Pat. No. 6,797,556 B2 to Murthy et al. ("Murthy556").
Ex-1031	U.S. Pat. Pub. No. 2007/0134870 A1 to Lee et al. ("Lee").
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Ex-1033	U.S. Pat. Pub. No. 2009/0020820 A1 to Baik et al. ("Baik").
Ex-1034	U.S. Pat. Pub. No. 2008/0293207 A1 to Koutny et al. ("Koutny").
Ex-1035	U.S. Pat. Pub. No. 2010/0075476 A1 to Miyashita ("Miyashita").

Exhibit	Description
Ex-1039	S. Thompson et al., "Source/Drain Extension Scaling for 0.1µm and Below Channel Length MOSFETS," Digest of Technical Papers for the 1998 Symposium on VLSI Technology, pp. 132-33 (1998) ("Thompson1998").
Ex-1040	D.M. Fleetwood et al., *Defects in Microelectronic Materials and Devices* (2008) (excerpted) ("Fleetwood").
Ex-1041	U.S. Pat. Pub. No. 2006/0246641 A1 to Kammler et al. ("Kammler").
Ex-1042	U.S. Pat. Pub. No. 2007/0228482 A1 to Wei et al. ("Wei").
Ex-1043	U.S. Pat. Pub. No. 2008/0203486 A1 to Wiatr et al. ("Wiatr").
Ex-1044	U.S. Pat. Pub. No. 2009/0242995 A1 to Suzuki et al. ("Suzuki995").
Ex-1045	U.S. Pat. Pub. No. 2007/0090465 A1 to Suzuki et al. ("Suzuki465").
Ex-1046	A. Pavlov & M. Sachdev, *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test* (2008) (excerpted) ("Pavlov").
Ex-1047	U.S. Pat. Pub. No. 2007/0023832 A1 to Matsui ("Matsui").
Ex-1048	M. Ishida et al., "A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable Beyond 0.18 µm Generation and Desirable for Ultra High Speed Operation," Proceedings of the 1998 International Electron Devices Meeting (IEDM), pp. 201-04 (1998) ("Ishida").
Ex-1049	D. Balobas & N. Konofaos, "Design and Evaluation of 6T SRAM Layout Designs at Modern Nanoscale CMOS Processes," 4th International Conference on Modern Circuits and System Technologies (2015) ("Balobas").

Exhibit	Description
Ex-1050	U.S. Pat. Pub. No. 2011/0074498 A1 to Thompson et al. ("Thompson498").

Appendix B

Claim 1	
[1Pre]	A semiconductor device, comprising:
[1A]	a first MIS transistor, wherein: the first MIS transistor includes:
[1B]	a first gate insulating film formed on a first active region in a semiconductor substrate,
[1C]	a first gate electrode formed on the first gate insulating film,
[1D]	a first sidewall spacer formed on a side surface of the first gate electrode,
[1E]	a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and
[1F]	a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress,
[1G]	an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode,
[1H]	a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer,
[1I]	the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and
[1J]	the first stress-relief film is not in direct contact with the side surface of the first gate electrode.

Claim 2	
The semiconductor device of claim 1, further comprising: a first offset spacer which is formed between the first gate electrode and the first sidewall spacer, and whose cross-section has an I shape.	
Claim 3	
The semiconductor device of claim 1, further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer.	
Claim 4	
The semiconductor device of claim 1, wherein the first stress-relief film is formed on a side surface of the silicon compound layer.	
Claim 5	
The semiconductor device of claim 1, wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer.	
Claim 6	
[6Pre]	The semiconductor device of claim 1, wherein
[6A]	the first sidewall spacer includes an inner sidewall spacer whose cross-section has an L shape, and
[6B]	the stress insulating film is formed in contact with a surface of the inner sidewall spacer which is curved to have an L-shaped cross-section.

Claim 7	
[7Pre]	The semiconductor device of claim 1, wherein
[7A]	the first MIS transistor is a p-type MIS transistor,
[7B]	the first stress is a compressive stress, and
[7C]	the second stress is a tensile stress.
Claim 8	
[8Pre]	The semiconductor device of claim 1, wherein
[8A]	the silicon compound layer is a SiGe layer,
[8B]	the stress insulating film is a silicon nitride film, and
[8C]	the first stress-relief film is a silicon oxide film.
Claim 9	
[9Pre]	The semiconductor device of claim 1, wherein
[9A]	the first MIS transistor is an n-type MIS transistor,
[9B]	the first stress is a tensile stress, and
[9C]	the second stress is a compressive stress.

Claim 10	
[10Pre]	The semiconductor device of claim 1, further comprising:
[10A]	an isolation region formed in the semiconductor substrate to surround the first active region;
[10B]	a gate interconnect formed on the isolation region;
[10C]	an interconnect sidewall spacer formed on a side surface of the gate interconnect;
[10D]	a second stress-relief film formed on a side surface of a recessed portion provided in the isolation region on a lateral side of the interconnect sidewall spacer; and
[10E]	the stress insulating film formed on the isolation region to cover the gate interconnect, the interconnect sidewall spacer, and the second stress-relief film.
Claim 11	
[11Pre]	The semiconductor device of claim 1, further comprising:
[11A]	a second MIS transistor, wherein: the second MIS transistor includes:
[11B]	a second gate insulating film formed on a second active region in the semiconductor substrate,
[11C]	a second gate electrode formed on the second gate insulating film,
[11D]	a second sidewall spacer formed on a side surface of the second gate electrode,

[11E]	a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and
[11F]	the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.
Claim 12	
The semiconductor device of claim 11, wherein no first stress-relief film is formed on the second active region.	
Claim 13	
[13Pre]	The semiconductor device of claim 1, further comprising:
[13A]	a third MIS transistor, wherein: the third MIS transistor includes:
[13B]	a third gate insulating film formed on a third active region in the semiconductor substrate,
[13C]	a third gate electrode formed on the third gate insulating film,
[13D]	a third sidewall spacer formed on a side surface of the third gate electrode,
[13E]	a third source/drain region of a first conductivity type which is formed in the third active region on a lateral side of the third sidewall spacer,
[13F]	a protective film formed on the third active region to cover the third gate electrode, the third sidewall spacer, and the third source/drain region, and
[13G]	the stress insulating film formed on the protective film.

Claim 14
The semiconductor device of claim 13, wherein no silicide layer is formed on the third gate electrode and the third source/drain region.
Claim 15
The semiconductor device of claim 13, wherein the first stress-relief film and the protective film are made of a same insulating material.